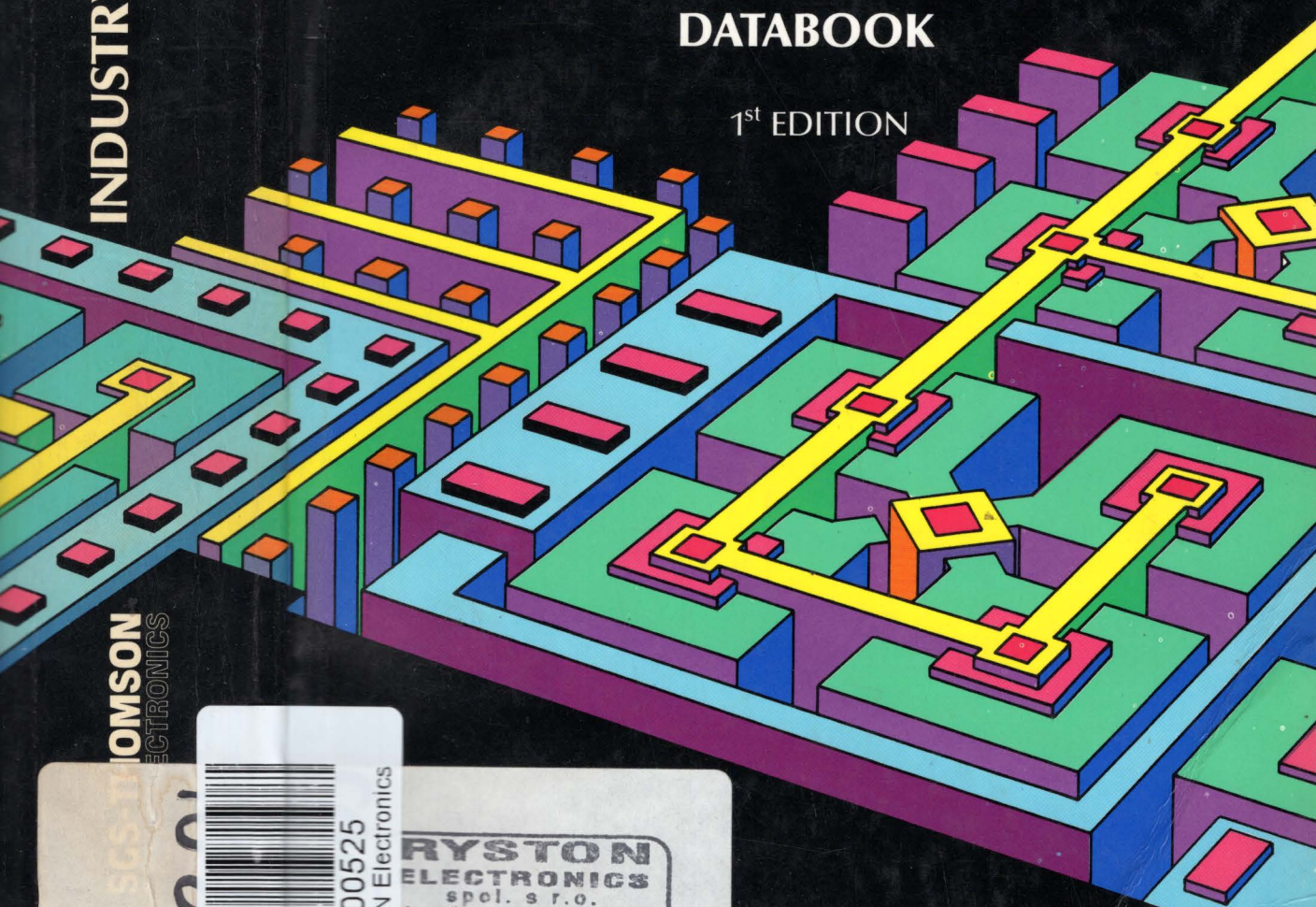
INDUSTRY STANDARD ANALOG ICs

DATABOOK

1st EDITION



SGS-THOMSON MICROELECTRONICS

INDUSTRY STANDARD ANALOG ICs

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1st EDITION

JUNE 1989

USE IN LIFE SUPPORT MUST BE EXPRESSLY AUTHORIZED

SGS-THOMSON' PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices to systems are devices or systems which, are intended for surgical implant into the body to support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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PRODUCT GUIDE

CMOS OP-AMPs

Type	Description	Pins	Package D: Plastic micropackage H: Metal can J: Cerdip N: Plastic dual in line
CMOS SINGLE			
TS 271,A,B	Programmable	8	N,D,J
CMOS-DUAL			
TS 27L2,A,B	Low Power	8	N,D,J
TS 27M2,A,B	Medium Supply Current	8	N,D,J
TS 272,A,B	High Speed	8	N,D,J
CMOS-QUAD			
TS 27L4,A,B	Low Power	14	N,D,J
TS 27M4,A,B	Medium Supply Current	14	N,D,J
TS 274,A,B	High Speed	14	N,D,J

JFET OP-AMPs

JFET SINGLE			
LF 351,A,B	Wide Bandwidth	8	N,D,H
LF 355,A	Low Power	8	N,D,H
LF 356,A	High Speed	8	N,D,H
LF 357,A	Very High Speed	8	N,D,H
MC 34001,A,B	Standard	8	N,D,H
TL 061,A,B	Low Power	8	N,D,H
TL 071,A,B	Low Noise	8	N,D,H
TL 081,A,B	Standard	8	N,D,H
JFET DUAL			
LF 353,A,B	Wide Bandwidth	8	N,D,H
MC 34002,A,B	Standard	8	N,D,H
TL 062,A,B	Low Power	8	N,D,H
TL 072,A,B	Low Noise	8	N,D,H
TL 082,A,B	Standard	8	N,D,H
JFET-QUAD			
LF 347,A,B	Wide Bandwidth	14	N,D,J
MC 34004,A,B	Standard	14	N,D,J
TL 064,A,B	Low Power	14	N,D,J
TL 074,A,B	Low Noise	14	N,D,J,
TL 084,A,B	Standard	14	N,D,J,

Note: All OP-AMPs are available in 3 Temperature ranges (0°C to 70°C, −40°C to +105°C, −55°C to +125°C) unless otherwise specified.

BIPOLAR OP-AMPs

Type	Description	Pins	Package D: Plastic micropackage H: Metal can J: Cerdip N: Plastic dual in line
BIPOLAR OP-AMPs			
LM301A	Low Offset-External Frequency Compensation	8	N,D,J,H
LM 308,A	Precision, High Gain	8	N,D,J,H
LM 318	High Speed	8	N,D,J,H
TDB 7910	Power (Temp. Range: 0°C to +70°C)	16	N
UA 741	Standard	14	N,D,J,H
UA 748	Precision	8	N,D,H
UA 776	Programmable	8	N,D,H
BIPOLAR DUAL			
LM 358,A	Low Power	8	N,D,J,H
LM 2904	Low Power (Temp. range: −40°C to +105°C)	8	N,D,J
LS 204	High Performance	8	D,H,N
LS 4558N	High Performance (Temp. range: 0°C to +70°C)	8	D,N
MC 1458	Standard	8	N,D,J,H
MC 4558	Wide Bandwidth (Temp. range: 0°C to +70°C −40°C to +105°C)	8	N,D,J,H
NE 532	Low Power (Temp. range: 0°C to +70°C)	8	N,D,J
TEB 1033	Active Filter (LS 204 Equivalent)	8	N,D
BIPOLAR QUAD			
LM 324,A	Standard	14	N,D,J,
LM 346	Programmable	16	N,D,J
LM 348	Quad UA 741	14	N,D,J
LM 2902	Standard (Temp. range: −40°C to +105°C)	14	N,D,J
LS 404	High Performance	14	D,N
MC 3403	Low Power	14	N,D,J
TEB 4033	Active Filter - (LS404 Equivalent)	14	N,D,J

Note: All OP-AMPs are available in 3 Temperature ranges (0°C to 70°C, −40°C to +105°C, −55°C to +125°C) unless otherwise specified.

THE OP AMP COMPROMISE

Hereunder you will find a very helpful tool: the ranking of some typical devices regarding 5 important parameters:

- BANDWIDTH
- SLEW RATE
- SUPPLY CURRENT
- INPUT BIAS
- NOISE

BANDWIDTH
GW_R (MHz)

0.1	1		2.5	4	5.5	50
TS27LX	TS27MX MC3403	UA741 LM324	TEBX033 MC1458	TL07X TL08X	MC4558	LM318

SLEWRATE
S_{VO} (V/μs)

0.04	0.4 - 0.8	1	2.2	5.5	16	70
TS27LX	LM324/UA741 MC3403/MC1458	TEBX033	MC4558	TS27X	TL07X TL08X	LM318

SUPPLY CURRENT
I_{CC} (mA/ampli)

5	2.3	1.7	1.4	0.7	0.5	0.15	0.01
LM318	MC1458	UA741	TL07X TL08X	MC4558 MC3403	LM324 TEBX033	TS27MX	TS27LX

INPUT BIAS CURRENT
I_{Ib} (nA)

160	80	50	20	0.3	1pA
LM318	UA741	TEBX033	LM324	TL0XX	TS27X TS27L/MX

NOISE
V_n (nV/$\sqrt{Hz}$)

70	38	30	18	10	8
TS27LX	TS27MX	TS27X	TL07X TL08X	MC3403 MC4558	TEBX033

COMPARATORS

Type	Description	Pins	Package D: Plastic micropackage H: Metal can J: Cerdip N: Plastic dual in line
CMOS DUAL			
TS 372	Low Power	8	N,D,J
CMOS QUAD			
TS 374	Low Power	14	N,D,J
BIPOLAR SINGLE			
LM 311	Standard	8	N,D,J,H
BIPOLAR DUAL			
LM 393,A	Low Power, Low Offset	8	N,D,J,H
LM 319	High Speed	14	N,D,J,H
LM 2903	Low Power, Low Offset (Temp. range: −40 to +105°C)	8	N,D,J
BIPOLAR QUAD			
LM 339,A	Low Power, Low Offset	14	N,D,J
LM 2901	Low Power, Low Offset (Temp. range: −40°C to +105°C)	14	N,D,J
MC 3302	Low Power, Low Offset (Temp. range: −40°C to +105°C)	14	N,D,J

Note: All comparators are available in 3 Temperature ranges: (0°C to 70°C, −40°C to +105°C, −55°C to +125°C)

VOLTAGE REGULATORS

STANDARD POSITIVE

I_O max (A)	Type	Regulated Output Voltage (V)												Precision %	Package
		5	6	7.5	8	8.5	9	10	12	15	18	20	24		
5	LM238K (*) LM338K	1.2V ← adjustable → 32V												4 4	TO-3 TO-3
3	LM223K LM323K	● ●												6 4	TO-3 TO-3
2	L78S00CV L78S00CT L78S00T (**)	● ● ●		● ● ●			● ● ●	● ● ●	● ● ●	● ● ●	● ● ●		● ● ●	4 4 4	TO-220 TO-3 TO-3
1.5	LM117K (**) LM217K (**) LM317K LM317T	1.2V ← adjustable → 37V												4 4 4 4	TO-3 TO-3 TO-3 TO-220
1	L7800CV L7800ABV (*) L7800ACV L7800CT L7800T (**)	● ● ● ● ●	● ● ● ● ●		● ● ● ● ●	● ● ●			● ● ● ● ●	● ● ● ● ●	● ● ● ● ●	● ● ● ● ●	● ● ● ● ●	4 2 2 4 4	TO-220 TO-220 TO-220 TO-3 TO-3
0-5	L78M00ABV (*) L78M00CV L78M00CX L78M00CS	● ● ● ●	● ● ● ●		● ● ● ●				● ● ● ●	● ● ● ●	● ● ● ●	● ● ● ●	● ● ● ●	2 4 4 4	TO-220 TO-220 SOT-82 SOT-194
0.15	LM723CD1 LM723CH LM723CJ LM723CN LM723J (**) LM723H (**)	2.0V ← adjustable → 37V												3 3 3 3 3 3	S0-14 TO-100 DIL-14C DIL-14P DIL-14C TO-100

(*) −40°C to 125°C (**) −55°C to 150°C

STANDARD NEGATIVE

I_O max (A)	Type	Regulated Output Voltage (V)										Precision %	Package
		5	5.2	6	8	12	15	18	20	22	24		
1.5	LM237K (*) LM337K LM337SP	1.2V ← adjustable → 32V										2 3 3	TO-3 TO-3 TO-220
1	L7900ACV L7900CV L7900CT	● ● ●	● ● ●	● ● ●	● ● ●	● ● ●	● ● ●	● ● ●	● ● ●	● ● ●	● ● ●	2 4 4	TO-220 TO-220 TO-3

(*) −40°C to 125°C (**) −55°C to 150°C

VOLTAGE REGULATORS (Continued)

LOW DROP

Type	Low Drop	Very Low Drop	Transient Protection				Reset	Short Circuit Protection	Reverse Voltage Protection	Output Voltage			
			±100	±80	±60	±40				5V	8.5V	10V	12V
L387A		●					●	●	●	●			
L4940/41		●				●		●	●	●			

PROPRIETARY

Type		I_O max (A)	Regulated Output Voltage (V)						Package
				5	8.5	10	12		
L296/P	(**)	4	5.1V ← adjustable → 40V						MULTIWATT 15
L4960	(**)	2.5	1V ← adjustable → 40V						HEPTAWATT
L200CH/CV **L200CT/T**		2	2.9V ← adjustable → 36V						PENTAWATT TO-3 (4 LEAD)
L4962	(**)	1.5	5V ← adjustable → 40V						POWERDIP 12+2+2
L4940				●					TO-220
L4941		1.0		●					TO-220
L387A		0.5		●					PENTAWATT
L4901A-2A	(*)			●					HEPTAWATT
L4903-4A	(*)			●					MINIDIP
L4905	(*)			●					HEPTAWATT

(*) Dual regulator (**) Switch-mode

VOLTAGE REGULATORS (Continued)

HIGH CURRENT SWITCHING			
Parameters	**Type**		
	L296/P	**L4960**	**L4962**
Voltage Reference (%)	±2	±4	±4
Output Voltage Range	V_{REF} to 40V	V_{REF} to 40V	V_{REF} to 40V
Output Current (A)	4.0	2.5	1.5
Internal Current Limiting	●	●	●
Soft Start	●	●	●
Inhibit Input	●		
Reset Output	●		
Crowbar Control	●		
Max. Oscillator Frequency (KHz)	200	120	120
Separate Oscillator Synch.	●		
Thermal Protection	●	●	●
Package	Multiwatt 15	Heptawatt	12+2+2

SPECIAL FUNCTIONS		
Type	**Description**	**Package**
TL7700A	Supply voltage supervisors designed for use as reset controllers in μP systems. During power-up the device test the supply voltage and keeps the reset outputs active as long as the supply voltage has non reached its nominal voltage value. — V_S = 3V to 18V — Temperature compensated voltage reference — Externally adjustable pulse width	MINIDIP

PWM CONTROLLERS

Parameters	Operating Temperature: −55 to 125°C				
	SG1524	SG1525A	SG1527A	UC1840	UC1842/1843/ 1844/1845
Voltage Reference (%)	±4	±1	±1	±1	±1
Soft Start		●	●	●	
PWM Latch		●	●	●	●
Under Voltage Lockout		●	●	●	●
Pulse by Pulse Current Limiting				●	●
Shutdown Terminal	●	●	●	●	
Output Current (A)	0.1	0.1 (0.4)	0.1 (0.4)	0.2	0.2 (1)
Feedforward				●	●
Max. Oscillator Frequency (KHz)	300	500	500	500	500
Dual Uncommitted Outputs	●				
Single Ended Output				●	●
Totem Pole Outputs		●	●		
Separate Oscillator Synch. Terminal		●	●		
Adjustable Deadtime Control		●	●	●	●
Latch Off or Continuous Retry Mode				●	
Low Current Start-Up				●	●

PWM CONTROLLERS

Parameters	Operating Temperature: −25 to 85°C				
	SG2524	SG2525A	SG2527A	UC2840	UC2842/2843/ 2844/2845
Voltage Reference (%)	±4	±1	±1	±1	±1
Soft Start		●	●	●	
PWM Latch		●	●	●	●
Under Voltage Lockout		●	●	●	●
Pulse by Pulse Current Limiting				●	●
Shutdown Terminal	●	●	●	●	
Output Current (A)	0.1	0.1 (0.4)	0.1 (0.4)	0.2	0.2 (1)
Feedforward				●	●
Max. Oscillator Frequency (KHz)	300	500	500	500	500
Dual Uncommitted Outputs	●				
Single Ended Output				●	●
Totem Pole Outputs		●	●		
Separate Oscillator Synch. Terminal		●	●		
Adjustable Deadtime Control		●	●	●	●
Latch Off or Continuous Retry Mode				●	
Low Current Start-Up				●	●

PWM CONTROLLERS

Parameters	Operating Temperature: 0 to 70°C				
	SG3524	SG3525A	SG3527A	UC3840	UC3842/3843/ 3844/3845
Voltage Reference (%)	±8	±2	±2	±2	±2
Soft Start		●	●	●	
PWM Latch		●	●	●	●
Under Voltage Lockout		●	●	●	●
Pulse by Pulse Current Limiting				●	●
Shutdown Terminal	●	●	●	●	●
Output Current (A)	0.1	0.1 (0.4)	0.1 (0.4)	0.2	0.2 (1)
Feedforward				●	●
Max. Oscillator Frequency (KHz)	300	500	500	500	500
Dual Uncommitted Outputs	●				
Single Ended Output				●	●
Totem Pole Outputs		●	●		
Separate Oscillator Synch. Terminal		●	●		
Adjustable Deadtime Control		●	●	●	●
Latch Off or Continuous Retry Mode				●	
Low Current Start-Up				●	●

DARLINGTON ARRAYS

Type	N.	V_{CEX}	I_O	Input	Configuration	Package
L601	8	90V	0.5A	General Purpose	● ⊣	PLASTIC DIP-16
L602	8	90V	0.4A	14-25V PMOS	● ⊣	
L603	8	90V	0.4A	5V TTL/CMOS	● ⊣	
L604	8	90V	0.4A	6-15V CMOS/PMOS	● ⊣	
L702B	4	90V	2A	5V TTL	●	
L702N	4	90V	2A	5V TTL	●	MULTIWATT 11
L7150	4	50V	1.5A	5V TTL/CMOS	● ⊣	MULTIWATT 15
L7152	4	50V	1.5A	6-15V CMOS/PMOS	● ⊣	
L7180	4	80V	1.5A	5V TTL/CMOS	● ⊣	
L7182	4	80V	1.5A	6-15V CMOS/PMOS	● ⊣	
ULN2001A/D	7	50V	0.5A	General Purpose	● ⊣	PLASTIC DIP-16 AND SO-16
ULN2002A/D	7	50V	0.5A	14-25V PMOS	● ⊣	
ULN2003A/D	7	50V	0.5A	5V TTL/CMOS	● ⊣	
ULN2004A/D	7	50V	0.5A	6-15V CMOS/PMOS	● ⊣	
ULQ2001R	7	50V	0.5A	General Purpose	● ⊣	CERAMIC DIP-16
ULQ2002R	7	50V	0.5A	14-25V PMOS	● ⊣	
ULQ2003R	7	50V	0.5A	5V TTL/CMOS	● ⊣	
ULQ2004R	7	50V	0.5A	6-15V CMOS/PMOS	● ⊣	

● = Common emitters. ■ = Isolated darlingtons.
⊣ = Integral suppression diodes. ▷ = Predriver stage.

DARLINGTON ARRAYS

Type	N.	V_{CEX}	I_O	Input	Configuration	Package
ULN2064B	4	50V	1.5A	5V TTL/CMOS	● ⊣▶⊢	PLASTIC DIP-16
ULN2065B	4	80V	1.5A	5V TTL/CMOS	● ⊣▶⊢	
ULN2066B	4	50V	1.5A	6-15V CMOS/PMOS	● ⊣▶⊢	
ULN2067B	4	80V	1.5A	6-15V CMOS/PMOS	● ⊣▶⊢	
ULN2068B	4	50V	1.5A	5V CMOS/TTL	▷ ● ⊣▶⊢	
ULN2069B	4	80V	1.5A	5V CMOS/TTL	▷ ● ⊣▶⊢	
ULN2070B	4	50V	1.5A	6-15V CMOS/PMOS	▷ ● ⊣▶⊢	
ULN2071B	4	80V	1.5A	6-15V CMOS/PMOS	▷ ● ⊣▶⊢	
ULN2074B	4	50V	1.5A	General Purpose	■	
ULN2075B	4	80V	1.5A	General Purpose	■	
ULN2076B	4	50V	1.5A	6-15V CMOS/PMOS	■	
ULN2077B	4	80V	1.5A	6-15V CMOS/PMOS	■	
ULN2801A	8	50V	0.5A	General Purpose	● ⊣▶⊢	PLASTIC DIP-18
ULN2802A	8	50V	0.5A	14-25V PMOS	● ⊣▶⊢	
ULN2803A	8	50V	0.5A	5V TTL/CMOS	● ⊣▶⊢	
ULN2804A	8	50V	0.5A	6-15V CMOS/PMOS	● ⊣▶⊢	
ULN2805A	8	50V	0.5A	High Output TTL	● ⊣▶⊢	

● = Common emitters.
⊣▶⊢ = Integral suppression diodes.
■ = Isolated darlingtons.
▷ = Predriver stage.

BIPOLAR TIMERS

Type	Description	Pins	Package D: Plastic micropackage H: Metal can J: Cerdip N: Plastic dual in line
NE 555	Single	8	N,D,J,H
NE 556	Dual	14	N,D,J

Note: Times are available in 3 temperature ranges (0°C to +70°C, −40°C to +105°C, −55°C to +125°C) unless otherwise specified.

CMOS TIMERS

Type	Description
TS555	Single } In development
TS556	Dual }

LINEAR DRIVERS

Type	Description	Package
L165	Power Op. Amplifier	PENTAWATT
L272	Dual Power Op. Amplifier	DIP-16
L272M	Dual Power Op. Amplifier	MINIDIP
L2720	Dual Power Op. Amplifier	DIP-16
L2722	Dula Power Op. Amplifier	MINIDIP

QUAD LINE DRIVERS/RECEIVERS

Type	Function	Temperature Range (°C)	Rise Time (ns)	Delay Time (ns)	Supply Current (mA)	Max Supply (V)	Package
MC1488 D	Driver	0 to 75	55	110/275	18	30	SO-14
MC1489 D MC1489 AD	Receivers	0 to 75	120 120	25 25	16 16	10	SO-14
MC1488 P	Driver	0 to 75	55	110/275	18	30	DIP-14
MC1489 AP MC1489 P	Receivers	0 to 75	120 120	25 25	16 16	10	DIP-14
MC1488 L	Driver	0 to 75	55	110/275	18	30	CERAMIC DIP-14
MC1489 AL MC1489 L	Receivers	0 to 75	120 120	25 25	16 10	10	CERAMIC DIP-14

DATA CONVERSION

Type	Accuracy	Temperature range (°C)	Package D: Plastic micropackage H: Metal can J: Cerdip N: Plastic dual in line
DAC0808 LCN **DAC0808 LCJ** **DAC0808 D1**	8 bit	0 to 75	DIP-16 CERAMIC DIP-16 SO-16
DAC0808 LJ		−55 to 125	CERAMIC DIP-16
DAC0807 LCN **DAC0807 LCJ** **DAC0807 D1**	7 bit	0 to 75	DIP-16 CERAMIC DIP-16 SO-16
DAC0806 LCN **DAC0806 LCJ** **DAC0806 D1**	6 bit	0 to 75	DIP-16 CERAMIC DIP-16 SO-16
AM6012 DC **AM6012 ADC**	12 bit	0 to 70	DIP-20
AM6012 D **AM6012 AD**	12 bit	0 to 70	SO-20L

MISCELLANEOUS

Type	Description	Pins	Package
LM 334	Adjustable Current Source (Temp. ranges: 0°C to +70°C, −25°C to +100°C, −55°C to +125°C)	3	Z
LM 335/A	Precision Temperature Sensor (Temp. ranges: −40°C to +100°C, −40°C to +125°C, −55°C to +150°C)	8,3	D,Z
LM 336/A/B	2.5V Voltage Reference (Temp. ranges: 0°C to +70°C −25°C to +85°C)	8,3	D,Z
L5832	Solenoid Controller Temp. Range: 0 to 70°C	16	DIP
L6221A/N	Quad Darlington Switch Temp. Range: 0 to 70°C	15/16	MULTIWATT, DIP
M8438A	LCD Driver Temp. Range: −40 to 85°C	40/44	DIP PLCC
M8439	LCD Driver Temp. Range: −40 to 85°C	40	DIP
UCN4801A	BIMOS/LATCH driver Temp. Ranges: −20 to 85°C	22	DIP

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
AM6012APC	AMD	AM6012APC
AM6012PC	AMD	AM6012PC
CA081AE	RCA	TL081ACN
CA081BE	RCA	TL081BCN
CA081E	RCA	TL081CN
CA082AE	RCA	TL082ACN
CA082BE	RCA	TL082BCN
CA082E	RCA	TL082CN
CA084AE	RCA	TL084ACN
CA084BE	RCA	TL084BCN
CA084E	RCA	TL084CN
CA124E	RCA	LM124N
CA139AF	RCA	LM139AJ
CA139E	RCA	LM139N
CA139F	RCA	LM139J
CA1458E	RCA	MC1458N
CA1558E	RCA	MC1558N
CA158E	RCA	LM158N
CA224E	RCA	LM224N
CA239AE	RCA	LM239AN
CA239AF	RCA	LM239AJ
CA239E	RCA	LM239N
CA239F	RCA	LM239J
CA258E	RCA	LM258N
CA2901E	RCA	LM2901N
CA2901F	RCA	LM2901J
CA2902E	RCA	LM2902N
CA2904E	RCA	LM2904N
CA301AE	RCA	LM301AN
CA311E	RCA	LM311N
CA324E	RCA	LM324N
CA3290E	RCA	LM393N
CA339AE	RCA	LM339AN
CA339AF	RCA	LM339AJ
CA339E	RCA	LM339N
CA339F	RCA	LM339J
CA358AE	RCA	LM358AN
CA358E	RCA	LM358N
CA555E	RCA	NE555N
CA741CE	RCA	UA741CN
CA741CT	RCA	UA741CH
CA741E	RCA	UA741EN
CA741T	RCA	UA741H
CA748CE	RCA	UA748CN
CA748CT	RCA	UA748CH
CA748T	RCA	UA748J
DAC0806LCJ	NATIONAL	DAC0806LCJ
DAC0806LCN	NATIONAL	DAC0806LCN
DAC0807LCJ	NATIONAL	DAC0807LCJ
DAC0807LCN	NATIONAL	DAC0807LCN
DAC0808LCJ	NATIONAL	DAC0808LCJ
DAC0808LCN	NATIONAL	DAC0808LCN
DAC0808LJ	NATIONAL	DAC0808LJ
DS1488J	NATIONAL	MC1488L
DS1488N	NATIONAL	MC1488P

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
DS1489AJ	NATIONAL	MC1489AL
DS1489AN	NATIONAL	MC1489AP
DS1489J	NATIONAL	MC1489L
DS1489N	NATIONAL	MC1489P
ITT552	ITT	ULN2001A
ITT554	ITT	ULN2002A
ITT556	ITT	ULN2003A
LF255M	NATIONAL	LF255D
LF255N	NATIONAL	LF255N
LF256M	NATIONAL	LF256D
LF256N	NATIONAL	LF256N
LF257M	NATIONAL	LF257D
LF257N	NATIONAL	LF257N
LF347J	NATIONAL	LF347J
LF347M	NATIONAL	LF347D
LF347N	MOTOROLA	LF347N
LF347N	NATIONAL	LF347N
LF351M	NATIONAL	LF351D
LF351N	MOTOROLA	LF351N
LF351N	NATIONAL	LF351N
LF353M	NATIONAL	LF353D
LF353N	MOTOROLA	LF353N
LF353N	NATIONAL	LF353N
LF355AM	NATIONAL	LF355AD
LF355AN	NATIONAL	LF355AN
LF355M	NATIONAL	LF355D
LF355N	MOTOROLA	LF355N
LF355N	NATIONAL	LF355N
LF356AM	NATIONAL	LF356AD
LF356AN	NATIONAL	LF356AN
LF356M	NATIONAL	LF356D
LF356N	MOTOROLA	LF356N
LF356N	NATIONAL	LF356N
LF357AM	NATIONAL	LF357AD
LF357M	NATIONAL	LF357D
LF357N	MOTOROLA	LF357N
LF357N	NATIONAL	LF357N
LM101AM	NATIONAL	LM101AD
LM111D	SIGNETICS	LM111D
LM117K	NATIONAL	LM117K
LM119D	SIGNETICS	LM119D
LM119F	SIGNETICS	LM119J
LM119J	NATIONAL	LM119J
LM124AJ	NATIONAL	LM124AJ
LM124AJ	TEXAS	LM124AJ
LM124D	SIGNETICS	LM124D
LM124F	SIGNETICS	LM124J
LM124J	MOTOROLA	LM124J
LM124J	NATIONAL	LM124J
LM124J	TEXAS	LM124J
LM124N	SIGNETICS	LM124N
LM1398AD	SIGNETICS	LM139AD
LM139AF	SIGNETICS	LM139AJ
LM139AJ	MOTOROLA	LM139AJ
LM139AJ	NATIONAL	LM139AJ

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
LM139AJ	TEXAS	LM139AJ
LM139D	SIGNETICS	LM139D
LM139F	SIGNETICS	LM139J
LM139J	MOTOROLA	LM139J
LM139J	NATIONAL	LM139J
LM139J	TEXAS	LM139J
LM139N	SIGNETICS	LM139N
LM1458M	NATIONAL	MC1458D
LM1458N	NATIONAL	MC1458N
LM146J	NATIONAL	LM146J
LM148J	MOTOROLA	LM148J
LM148J	NATIONAL	LM148J
LM148J	TEXAS	LM148J
LM158AJ	NATIONAL	LM158AJ
LM158AJG	TEXAS	LM158AJ
LM158F	SIGNETICS	LM158J
LM158J	MOTOROLA	LM158J
LM158J	NATIONAL	LM158J
LM158JG	TEXAS	LM158J
LM158N	SIGNETICS	LM158N
LM193AF	SIGNETICS	LM193AJ
LM193AJ	NATIONAL	LM193AJ
LM193AJG	TEXAS	LM193AJ
LM193D	SIGNETICS	LM193D
LM193J	NATIONAL	LM193J
LM193N	SIGNETICS	LM193N
LM201AD	MOTOROLA	LM201AD
LM201AD	TEXAS	LM201AD
LM201AM	NATIONAL	LM201AD
LM201AN	MOTOROLA	LM201AN
LM201AN	NATIONAL	LM201AN
LM201AP	TEXAS	LM201AN
LM211D	MOTOROLA	LM211D
LM211D	SIGNETICS	LM211D
LM211D	TEXAS	LM211D
LM211N	SIGNETICS	LM211N
LM211P	TEXAS	LM211N
LM219D	SIGNETICS	LM219D
LM219F	SIGNETICS	LM219J
LM219J	NATIONAL	LM219J
LM223K	MOTOROLA	LM223K
LM223K	STEEL NATIONAL	LM223K
LM224AD	TEXAS	LM224AD
LM224AJ	NATIONAL	LM224AJ
LM224AJ	TEXAS	LM224AJ
LM224AN	TEXAS	LM224AN
LM224D	MOTOROLA	LM224D
LM224D	SIGNETICS	LM224D
LM224D	TEXAS	LM224D
LM224F	SIGNETICS	LM224J
LM224J	MOTOROLA	LM224J
LM224J	NATIONAL	LM224J
LM224J	TEXAS	LM224J
LM224N	SIGNETICS	LM224N
LM224N	TEXAS	LM224N

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
LM237K	MOTOROLA	LM237K
LM237K	STEEL NATIONAL	LM237K
LM238K	STEEL NATIONAL	LM238K
LM239AD	SIGNETICS	LM239AD
LM239AD	TEXAS	LM239AD
LM239AF	SIGNETICS	LM239AJ
LM239AJ	MOTOROLA	LM239AJ
LM239AJ	NATIONAL	LM239AJ
LM239AJ	TEXAS	LM239AJ
LM239AN	SIGNETICS	LM239AN
LM239AN	TEXAS	LM239AN
LM239D	MOTOROLA	LM239D
LM239D	SIGNETICS	LM239D
LM239D	TEXAS	LM239D
LM239F	SIGNETICS	LM239J
LM239J	MOTOROLA	LM239J
LM239J	NATIONAL	LM239J
LM239J	TEXAS	LM239J
LM239N	SIGNETICS	LM239N
LM239N	TEXAS	LM239N
LM246J	NATIONAL	LM246J
LM248D	TEXAS	LM248D
LM248N	TEXAS	LM248N
LM258AJG	TEXAS	LM258AJ
LM258D	MOTOROLA	LM258D
LM258D	TEXAS	LM258D
LM258F	SIGNETICS	LM258J
LM258JG	TEXAS	LM258J
LM258N	SIGNETICS	LM258N
LM258P	TEXAS	LM258N
LM2901D	MOTOROLA	LM2901D
LM2901D	SIGNETICS	LM2901D
LM2901D	TEXAS	LM2901D
LM2901F	SIGNETICS	LM2901J
LM2901J	MOTOROLA	LM291J
LM2901J	NATIONAL	LM2901J
LM2901J	TEXAS	LM2901J
LM2901M	NATIONAL	LM2901D
LM2901N	MOTOROLA	LM2901N
LM2901N	NATIONAL	LM2901N
LM2901N	SIGNETICS	LM2901N
LM2901N	TEXAS	LM2901N
LM2902D	MOTOROLA	LM2902D
LM2902D	TEXAS	LM2902D
LM2902J	MOTOROLA	LM2902J
LM2902J	NATIONAL	LM2902J
LM2902J	TEXAS	LM2902J
LM2902M	NATIONAL	LM2902D
LM2902N	MOTOROLA	LM2902N
LM2902N	NATIONAL	LM2902N
LM2902N	TEXAS	LM2902N
LM2903D	MOTOROLA	LM2903D
LM2903D	TEXAS	LM2903D
LM2903F	SIGNETICS	LM2903J
LM2903JG	TEXAS	LM2903J

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
LM2903M	NATIONAL	LM2903D
LM2903N	MOTOROLA	LM2903N
LM2903N	NATIONAL	LM2903N
LM2903N	SIGNETICS	LM2903N
LM2903P	TEXAS	LM2903N
LM2904D	MOTOROLA	LM2904D
LM2904D	TEXAS	LM2904D
LM2904J	NATIONAL	LM2904J
LM2904JG	TEXAS	LM2904J
LM2904M	NATIONAL	LM2904D
LM2904N	MOTOROLA	LM2904N
LM2904N	NATIONAL	LM2904N
LM2904P	TEXAS	LM2904N
LM293AF	SIGNETICS	LM293AJ
LM293AJ	NATIONAL	LM293AJ
LM293AJG	TEXAS	LM293AJ
LM293D	TEXAS	LM293D
LM293F	SIGNETICS	LM293J
LM293J	NATIONAL	LM293J
LM293JG	TEXAS	LM293J
LM293N	NATIONAL	LM293N
LM293N	SIGNETICS	LM293N
LM301AD	MOTOROLA	LM301AD
LM301AD	TEXAS	LM301AD
LM301AJ	MOTOROLA	LM301AJ
LM301AJ	NATIONAL	LM301AJ
LM301AJG	TEXAS	LM301AJ
LM301AM	NATIONAL	LM301AD
LM301AN	MOTOROLA	LM301AN
LM301AN	NATIONAL	LM301AN
LM301AP	TEXAS	LM301AN
LM308AD	MOTOROLA	LM308AD
LM308AM	NATIONAL	LM308AD
LM308AN	MOTOROLA	LM308AN
LM308AN	NATIONAL	LM308AN
LM308D	MOTOROLA	LM308D
LM308M	NATIONAL	LM308D
LM308N	MOTOROLA	LM308N
LM308N	NATIONAL	LM308N
LM311D	MOTOROLA	LM311D
LM311D	SIGNETICS	LM311D
LM311D	TEXAS	LM311D
LM311F	SIGNETICS	LM311J
LM311J	MOTOROLA	LM311J
LM311J-8	NATIONAL	LM311J
LM311JG	TEXAS	LM311J
LM311M	NATIONAL	LM311D
LM311N	MOTOROLA	LM311N
LM311N	NATIONAL	LM311N
LM311N	SIGNETICS	LM311N
LM311P	TEXAS	LM311N
LM317K	NATIONAL	LM317K
LM317SP	THOMSON	LM317T
LM317T	NATIONAL	LM317T
LM318D	TEXAS	LM318D

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
LM318M	NATIONAL	LM318D
LM318N	NATIONAL	LM318N
LM318P	TEXAS	LM318N
LM319D	SIGNETICS	LM319D
LM319F	SIGNETICS	LM319J
LM319J	NATIONAL	LM319J
LM319M	NATIONAL	LM319D
LM319N	NATIONAL	LM319N
LM323K	MOTOROLA	LM323K
LM323K	STEEL NATIONAL	LM323K
LM324AD	TEXAS	LM324AD
LM324AJ	MOTOROLA	LM324AJ
LM324AJ	NATIONAL	LM324AJ
LM324AJ	TEXAS	LM324AJ
LM324AM	NATIONAL	LM324AD
LM324AN	NATIONAL	LM324AN
LM324AN	TEXAS	LM324AN
LM324D	MOTOROLA	LM324D
LM324D	SIGNETICS	LM324D
LM324D	TEXAS	LM324D
LM324F	SIGNETICS	LM324J
LM324J	MOTOROLA	LM324J
LM324J	NATIONAL	LM324J
LM324J	TEXAS	LM324J
LM324M	NATIONAL	LM324D
LM324N	MOTOROLA	LM324N
LM324N	NATIONAL	LM324N
LM324N	SIGNETICS	LM324N
LM324N	TEXAS	LM324N
LM3302D	TEXAS	MC3302D
LM3302J	NATIONAL	MC3302J
LM3302J	TEXAS	MC3302J
LM3302N	NATIONAL	MC3302N
LM3302N	TEXAS	MC3302N
LM3303N	NATIONAL	MC3303N
LM334Z	NATIONAL	LM334Z
LM335Z	NATIONAL	LM335Z
LM336BM	NATIONAL	LM336BD
LM336BZ	NATIONAL	LM336BZ
LM336M	NATIONAL	LM336D
LM336Z	NATIONAL	LM336Z
LM337K	MOTOROLA	LM337K
LM337K	STEEL NATIONAL	LM337K
LM337KC	TEXAS	LM337SP
LM337T	MOTOROLA	LM337SP
LM337T	NATIONAL	LM337SP
LM339AD	SIGNETICS	LM339AD
LM339AD	TEXAS	LM339AD
LM339AF	SIGNETICS	LM339AJ
LM339AJ	MOTOROLA	LM339AJ
LM339AJ	NATIONAL	LM339AJ
LM339AJ	TEXAS	LM339AJ
LM339AM	NATIONAL	LM339AD
LM339AN	MOTOROLA	LM339AN
LM339AN	NATIONAL	LM339AN

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
LM339AN	SIGNETICS	LM339AN
LM339AN	TEXAS	LM339AN
LM339D	MOTOROLA	LM339D
LM339D	SIGNETICS	LM339D
LM339D	TEXAS	LM339D
LM339F	SIGNETICS	LM339J
LM339J	NATIONAL	LM339J
LM339J	TEXAS	LM339J
LM339M	NATIONAL	LM339D
LM339N	MOTOROLA	LM339N
LM339N	NATIONAL	LM339N
LM339N	SIGNETICS	LM339N
LM339N	TEXAS	LM339N
LM3403J	NATIONAL	MC3403J
LM3403M	NATIONAL	MC3403D
LM3403N	NATIONAL	MC3403N
LM346J	NATIONAL	LM346J
LM346M	NATIONAL	LM346D
LM346N	NATIONAL	LM346N
LM348D	MOTOROLA	LM348D
LM348D	TEXAS	LM348D
LM348M	NATIONAL	LM348D
LM348N	MOTOROLA	LM348N
LM348N	NATIONAL	LM348N
LM348N	TEXAS	LM348N
LM3503J	NATIONAL	MC3503J
LM358AD	TEXAS	LM358AD
LM358AJG	TEXAS	LM358AJ
LM358AM	NATIONAL	LM358AD
LM358AN	NATIONAL	LM358AN
LM358AP	TEXAS	LM358AN
LM358D	MOTOROLA	LM358D
LM358D	SIGNETICS	LM358D
LM358D	TEXAS	LM358D
LM358F	SIGNETICS	LM358J
LM358J	MOTOROLA	LM358J
LM358J	NATIONAL	LM358J
LM358JG	TEXAS	LM358J
LM358M	NATIONAL	LM358D
LM358N	MOTOROLA	LM358N
LM358N	NATIONAL	LM358N
LM358N	SIGNETICS	LM358N
LM358P	TEXAS	LM358N
LM393AD	TEXAS	LM393AD
LM393AF	SIGNETICS	LM393AJ
LM393AJ	NATIONAL	LM393AJ
LM393AJG	TEXAS	LM393AJ
LM393AN	MOTOROLA	LM393AN
LM393AN	NATIONAL	LM393AN
LM393AN	SIGNETICS	LM393AN
LM393AP	TEXAS	LM393AN
LM393D	MOTOROLA	LM393D
LM393D	SIGNETICS	LM393D
LM393D	TEXAS	LM393D
LM393F	SIGNETICS	LM393J

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
LM393J	NATIONAL	LM393J
LM393JG	TEXAS	LM393J
LM393M	NATIONAL	LM393D
LM393N	MOTOROLA	LM393N
LM393N	NATIONAL	LM393N
LM393N	SIGNETICS	LM393N
LM393P	TEXAS	LM293N
LM393P	TEXAS	LM393N
LM555CJ	NATIONAL	NE555J
LM555CM	NATIONAL	NE555D
LM555CN	NATIONAL	NE555N
LM556CJ	NATIONAL	NE556J
LM556CM	NATIONAL	NE556D
LM556CN	NATIONAL	NE556N
LM556J	NATIONAL	SE556J
LM723CH	NATIONAL	LM723CH
LM723CJ	NATIONAL	LM723CD
LM723CM	NATIONAL	LM723CD
LM723CN	NATIONAL	LM723CN
LM723H	NATIONAL	LM723H
LM723J	NATIONAL	LM723J
LM741AH	NATIONAL	UA741AH
LM741AJ	NATIONAL	UA741AJ
LM741CH	NATIONAL	UA741CH
LM741CJ	NATIONAL	UA741CJ
LM741CM	NATIONAL	UA741CD
LM741CN	NATIONAL	UA741CN
LM741EH	NATIONAL	UA741EH
LM741EN	NATIONAL	UA741EN
LM741H	NATIONAL	UA741H
LM741J	NATIONAL	UA741J
LM748CH	NATIONAL	UA748CH
LM748CJ	NATIONAL	UA748CJ
LM748CN	NATIONAL	UA748MH
LM748J	NATIONAL	UA748J
LMC660AIN	NATIONAL	TS27M4BIN
LMC660CN	NATIONAL	TS27M4ACN
LM7805CK	NATIONAL	L7805CT
LM7805CT	NATIONAL	L7805CV
LM7812CK	NATIONAL	L7812CT
LM7812CT	NATIONAL	L7812CV
LM7815CK	NATIONAL	L7815CT
LM7815CT	NATIONAL	L7815CV
LM7905CK	NATIONAL	L7905CT
LM7905CT	NATIONAL	L7905CV
LM7912CK	NATIONAL	L7912CT
LM7912CT	NATIONAL	L7912CV
LM7915CK	NATIONAL	L7915CT
LM7915CT	NATIONAL	L7915CV
MC1408L6	MOTOROLA	DAC0806LCJ
MC1408L7	MOTOROLA	DAC0807LCJ
MC1408L8	MOTOROLA	DAC0808LCJ
MC1408P6	MOTOROLA	DAC0806LCN
MC1408P7	MOTOROLA	DAC0807LCN
MC1408P8	MOTOROLA	DAC0808LCN

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
MC1455D	MOTOROLA	NE555D
MC1455P1	MOTOROLA	NE555N
MC1455U	MOTOROLA	NE555J
MC1458D	MOTOROLA	MC1458D
MC1458D	SIGNETICS	MC1458D
MC1458D	TEXAS	MC1458D
MC1458FE	SIGNETICS	MC1458J
MC1458JG	TEXAS	MC1458J
MC1458N	SIGNETICS	MC1458N
MC1458P	TEXAS	MC1458N
MC1458P	MOTOROLA	MC1458N
MC1458U	MOTOROLA	MC1458J
MC1488F	PHIL.SIGN.	MC1488L
MC1488L	MOTOROLA	MC1488L
MC1488N	PHIL.SIGN.	MC1488P
MC1488P	MOTOROLA	MC1488P
MC1489AF	PHIL.SIGN.	MC1489AL
MC1489AL	MOTOROLA	MC1489AL
MC1489AN	PHIL.SIGN.	MC1489AP
MC1489AP	MOTOROLA	MC1489AP
MC1489F	PHIL.SIGN.	MC1489L
MC1489L	MOTOROLA	MC1489L
MC1489N	PHIL.SIGN.	MC1489P
MC1489P	MOTOROLA	MC1489P
MC1508L8	MOTOROLA	DAC0808LJ
MC1558D	SIGNETICS	MC1558D
MC1558FE	SIGNETICS	MC1558J
MC1558JG	TEXAS	MC1558J
MC1558N	SIGNETICS	MC1558N
MC1558U	MOTOROLA	MC1558J
MC1741CD	MOTOROLA	UA741CD
MC1741CG	MOTOROLA	UA741CH
MC1741CP1	MOTOROLA	UA741CN
MC1741CU	MOTOROLA	UA741CJ
MC1741G	MOTOROLA	UA741H
MC1741U	MOTOROLA	UA741J
MC1748CD	MOTOROLA	UA748CD
MC1748BCG	MOTOROLA	UA748CH
MC1748CP1	MOTOROLA	UA748CN
MC1748CU	MOTOROLA	UA748CJ
MC1748G	MOTOROLA	UA748MH
MC1748U	MOTOROLA	UA748J
MC1776CD	MOTOROLA	UA778CD
MC1776CG	MOTOROLA	UA778CH
MC1776CP1	MOTOROLA	UA776CN
MC1776G	MOTOROLA	UA77BMH
MC3302D	MOTOROLA	MC3302D
MC3302D	SIGNETICS	MC3302D
MC3302F	SIGNETICS	MC3302J
MC3302L	MOTOROLA	MC3302J
MC3302N	SIGNETICS	MC3302N
MC3302P	MOTOROLA	MC3302N
MC3303D	SIGNETICS	MC3303D
MC3303D	TEXAS	MC3303D
MC3303F	SIGNETICS	MC3303J

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
MC3303J	TEXAS	MC3303J
MC3303L	MOTOROLA	MC3303J
MC3303N	SIGNETICS	MC3303N
MC3303N	TEXAS	MC3303N
MC3303P	MOTOROLA	MC3303N
MC34001AP	MOTOROLA	MC34001AN
MC34001BP	MOTOROLA	MC34001BN
MC34001P	MOTOROLA	MC34001N
MC34002AP	MOTOROLA	MC34002AN
MC34002BP	MOTOROLA	MC34002BN
MC34002P	MOTOROLA	MC34002N
MC34004AP	MOTOROLA	MC34004AN
MC34004BP	MOTOROLA	MC34004BN
MC34004P	MOTOROLA	MC34004N
MC3403CF	SIGNETICS	MC3403J
MC3403CN	SIGNETICS	MC3403N
MC3403D	MOTOROLA	MC3403D
MC3403D	SIGNETICS	MC3403D
MC3403D	TEXAS	MC3403D
MC3403J	TEXAS	MC3403J
MC3403L	MOTOROLA	MC3403J
MC3403N	TEXAS	MC3403N
MC3403P	MOTOROLA	MC3403N
MC3456L	MOTOROLA	NE556J
MC3456P	MOTOROLA	NE556N
MC3503F	SIGNETICS	MC3503J
MC3503J	TEXAS	MC3503J
MC3503L	MOTOROLA	MC3503J
MC3556L	MOTOROLA	SE556J
MC4558CP1	MOTOROLA	MC4558CN
MC4558BCU	MOTOROLA	MC4558CJ
MC7805ACT	MOTOROLA	L7805ACV
MC7805CK	MOTOROLA	L7805CT
MC7805CT	MOTOROLA	L7805CV
MC7805K	MOTOROLA	L7805T
MC7806ACT	MOTOROLA	L7806ACV
MC7806CK	MOTOROLA	L7806CT
MC7806CT	MOTOROLA	L7806CV
MC7806K	MOTOROLA	L7806T
MC7808ACT	MOTOROLA	L7808ACV
MC7808CK	MOTOROLA	L7808CT
MC7808CT	MOTOROLA	L7808CV
MC7808K	MOTOROLA	L7808T
MC7812ACT	MOTOROLA	L7812ACV
MC7812CK	MOTOROLA	L7812CT
MC7812CT	MOTOROLA	L7812CV
MC7812K	MOTOROLA	L7812T
MC7815ACT	MOTOROLA	L7815ACV
MC7815CK	MOTOROLA	L7815CT
MC7815CT	MOTOROLA	L7815CV
MC7815K	MOTOROLA	L7815T
MC7818ACT	MOTOROLA	L7818ACV
MC7818CK	MOTOROLA	L7818CT
MC7818CT	MOTOROLA	L7818CV
MC7818K	MOTOROLA	L7818T

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
MC7824ACT	MOTOROLA	L7824ACV
MC7824CT	MOTOROLA	L7824CV
MC7824K	MOTOROLA	L7824T
MC78M05CT	MOTOROLA	L78M05CV
MC78M06CT	MOTOROLA	L78M06CV
MC78M08CT	MOTOROLA	L78M08CV
MC78M12CT	MOTOROLA	L78M12CV
MC78M15CT	MOTOROLA	L78M15CV
MC78M18CT	MOTOROLA	L78M18CV
MC78M24CT	MOTOROLA	L78M24CV
MC7905CK	MOTOROLA	L7905CT
MC7905CT	MOTOROLA	L7905CV
MC7908CK	MOTOROLA	L7908CT
MC7908CT	MOTOROLA	L7908CV
MC7912CK	MOTOROLA	L7912CT
MC7912CT	MOTOROLA	L7912CV
MC7915CK	MOTOROLA	L7915CT
MC7915CT	MOTOROLA	L7915CV
MC7918CK	MOTOROLA	L7918CT
MC7918CT	MOTOROLA	L7918CV
MC7924CK	MOTOROLA	L7924CT
MC7924CT	MOTOROLA	L7924CV
MC7952CK	MOTOROLA	L7952CT
MC7952CT	MOTOROLA	L7952CV
NE4558D	SIGNETICS	MC4558CD
NE4558F	SIGNETICS	MC4558CJ
NE4558N	SIGNETICS	MC4558CN
NE532D	SIGNETICS	NE532D
NE532F	SIGNETICS	NE532J
NE532N	SIGNETICS	NE532N
NE555D	SIGNETICS	NE555D
NE555D	TEXAS	NE555D
NE555F	SIGNETICS	NE555J
NE555JG	TEXAS	NE555J
NE555N	SIGNETICS	NE555N
NE555P	TEXAS	NE555N
NE556D	SIGNETICS	NE556D
NE556D	TEXAS	NE556D
NE556F	SIGNETICS	NE556J
NE556J	TEXAS	NE556J
NE556N	SIGNETICS	NE556N
NE556N	TEXAS	NE556N
NE5601N	PHIL.SIGN.	ULN2001A
NE5602N	PHIL.SIGN.	ULN2002A
NE5603N	PHIL.SIGN.	ULN2003A
NE5604N	PHIL.SIGN.	ULN2004A
PWM125AK	SILICONIX	SG1525AJ
PWM125BK	SILICONIX	SG2525AJ
PWM125CK	SILICONIX	SG3525AJ
RC1488DC	RAYTHEON	MC1488L
RC1489ADC	RAYTHEON	MC1489AL
RC1489DC	RAYTHEON	MC1489L
RC4558D	TEXAS	MC4558CD
RC4558JG	TEXAS	MC4558CJ
RC4558P	TEXAS	MC4558CN

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
RV4558P	TEXAS	MC4558IN
SA1458D	SIGNETICS	MC1458ID
SA1458N	SIGNETICS	MC1458IN
SA4558N	SIGNETICS	MC4558IN
SA532D	SIGNETICS	LM2904D
SA532FE	SIGNETICS	LM2904J
SA532N	SIGNETICS	LM2904N
SA534D	SIGNETICS	LM2902D
SA534F	SIGNETICS	LM2902J
SA534N	SIGNETICS	LM2902N
SA555D	TEXAS	SA555D
SA555JG	TEXAS	SA555J
SA555P	TEXAS	SA555N
SA556D	TEXAS	SA556D
SA556J	TEXAS	SA556J
SA556N	TEXAS	SA556N
SA741CN	SIGNETICS	UA741IN
SE555F	SIGNETICS	SE558J
SE556J	TEXAS	SE556J
SG1524J	SIL.GEN.	SG1524J
SG1525AJ	SIL.GEN.	SG1525AJ
SG1527AJ	SIL.GEN.	SG1527AJ
SG2001J	SIL.GEN.	ULQ2001R
SG2001N	SIL.GEN.	ULN2001A
SG2002J	SIL.GEN.	ULQ2002R
SG2002N	SIL.GEN.	ULN2002A
SG2003J	SIL.GEN.	ULQ2003R
SG2003N	SIL.GEN.	ULN2003A
SG2004J	SIL.GEN.	ULQ2004R
SG2004N	SIL.GEN.	ULN2004A
SG2524J	SIL.GEN.	SG2524J
SG2524N	SIL.GEN.	SG2524J
SG2525AJ	SIL.GEN.	SG2525AJ
SG2525AN	SIL.GEN.	SG2525AN
SG2527AJ	SIL.GEN.	SG2527AJ
SG2527AN	SIL.GEN.	SG2527AN
SG3524D	PHIL.SIGN.	SG3524D
SG3524J	SIL.GEN.	SG3524J
SG3524N	SIL.GEN.	SG3524N
SG3525AJ	SIL.GEN.	SG3525AJ
SG3525AN	SIL.GEN.	SG3525AN
SG3527AJ	SIL.GEN.	SG3527AJ
SG3527AN	SIL.GEN.	SG3527AN
SN75064NE	TEXAS	ULN2064B
SN75065NE	TEXAS	ULN2065B
SN75066NE	TEXAS	ULN2066B
SN75067NE	TEXAS	ULN2067B
SN75068NE	TEXAS	ULN2068B
SN75069NE	TEXAS	ULN2069B
SN75074NE	TEXAS	ULN2074B
SN75075NE	TEXAS	ULN2075B
SN75188J	TEXAS	MC1488L
SN75188N	TEXAS	MC1488P
SN75189AN	TEXAS	MC1489AP
SN75189AT	TEXAS	MC1489AL

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
SN75189J	TEXAS	MC1489L
SN75189N	TEXAS	MC1489P
TA7504P	TOSHIBA	UA741CN
TA75061P	TOSHIBA	TL061CN
TA75062F	TOSHIBA	TL062CD
TA75062P	TOSHIBA	TL062CN
TA75064F	TOSHIBA	TL064CD
TA75064P	TOSHIBA	TL064IN
TA75064P	TOSHIBA	TL064CN
TA7506P	TOSHIBA	LM301AN
TA75071F	TOSHIBA	TL071CD
TA75071P	TOSHIBA	TL071CN
TA75072F	TOSHIBA	TL072CD
TA75072P	TOSHIBA	TL072CN
TA75074F	TOSHIBA	TL074CD
TA75074P	TOSHIBA	TL074CN
TA75339F	TOSHIBA	LM2901D
TA75339P	TOSHIBA	LM2901N
TA75358CF	TOSHIBA	LM358D
TA75358CP	TOSHIBA	LM358N
TA75358F	TOSHIBA	LM2904D
TA75358P	TOSHIBA	LM2904N
TA75393F	TOSHIBA	LM2903D
TA75393P	TOSHIBA	LM2903N
TA7540P	TOSHIBA	UA776IN
TA75458F	TOSHIBA	MC1458D
TA75558F	TOSHIBA	MC4558CD
TA75558P	TOSHIBA	MC4558CN
TA7555F	TOSHIBA	NE555D
TA7555P	TOSHIBA	NE555N
TA75902F	TOSHIBA	LM2902D
TA75902P	TOSHIBA	LM2902N
TBA222	SIEMENS	UA741H
TBA222B	SIEMENS	UA741N
TBB741G	SIEMENS	UA741CD
TDA0200SP	THOMSON	L200CV
TL061ACD	TEXAS	TL061ACD
TL061ACP	TEXAS	TL061ACN
TL061BCD	TEXAS	TL061BCD
TL061BCP	TEXAS	TL061BCN
TL061CD	TEXAS	TL061CD
TL061CP	TEXAS	TL061CN
TL061ID	TEXAS	TL061ID
TL061IP	TEXAS	TL061IN
TL062ACP	TEXAS	TL062ACN
TL062ACPD	TEXAS	TL062ACD
TL062BCD	TEXAS	TL062BCD
TL062BCP	TEXAS	TL062BCN
TL062CD	TEXAS	TL062CD
TL062CP	TEXAS	TL062CN
TL062ID	TEXAS	TL062ID
TL062IP	TEXAS	TL062IN
TL064ACD	TEXAS	TL064ACD
TL064ACN	TEXAS	TL064ACN
TL064BCD	TEXAS	TL064BCD

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
TL064BCN	TEXAS	TL064BCN
TL064CD	TEXAS	TL064CD
TL064CN	TEXAS	TL064CN
TL064ID	TEXAS	TL064ID
TL064IN	TEXAS	TL064IN
TL070ACP	MOTOROLA	TL072ACN
TL071ACD	TEXAS	TL071ACD
TL071ACP	MOTOROLA	TL071ACN
TL071ACP	TEXAS	TL071ACN
TL071BCD	TEXAS	TL071BCD
TL071BCP	MOTOROLA	TL071BCN
TL071BCP	TEXAS	TL071BCN
TL071CD	TEXAS	TL071CD
TL071CP	MOTOROLA	TL071CN
TL071CP	TEXAS	TL071CN
TL071ID	TEXAS	TL071ID
TL071IP	TEXAS	TL071IN
TL072ACD	TEXAS	TL072ACD
TL072ACP	TEXAS	TL072ACN
TL072BCD	TEXAS	TL072BCD
TL072BCP	MOTOROLA	TL072BCN
TL072BCP	TEXAS	TL072BCN
TL072CD	TEXAS	TL072CD
TL072CP	MOTOROLA	TL072CN
TL072CP	TEXAS	TL072CN
TL072ID	TEXAS	TL072ID
TL072IP	TEXAS	TL072IN
TL074ACD	TEXAS	TL074ACD
TL074ACN	MOTOROLA	TL074ACN
TL074ACN	TEXAS	TL074ACN
TL074BCD	TEXAS	TL074BCD
TL074BCN	MOTOROLA	TL074BCN
TL074BCN	TEXAS	TL074BCN
TL074CD	TEXAS	TL074CD
TL074CN	MOTOROLA	TL074CN
TL074CN	TEXAS	TL074CN
TL074ID	TEXAS	TL074ID
TL074IN	TEXAS	TL074IN
TL081ACD	TEXAS	TL081ACD
TL081ACP	MOTOROLA	TL081ACN
TL081ACP	TEXAS	TL081ACN
TL081BCD	TEXAS	TL081BCD
TL081BCP	MOTOROLA	TL081BCN
TL081BCP	TEXAS	TL081BCN
TL081CD	TEXAS	TL081CD
TL081CP	MOTOROLA	TL081CN
TL081CP	TEXAS	TL081CN
TL081ID	TEXAS	TL081ID
TL081IP	TEXAS	TL081IN
TL082ACD	TEXAS	TL082ACD
TL082ACP	MOTOROLA	TL082ACN
TL082BCD	TEXAS	TL082BCD
TL082BCP	MOTOROLA	TL082BCN
TL082BCP	TEXAS	TL082BCN
TL082CD	TEXAS	TL082CD

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
TL082CP	MOTOROLA	TL082CN
TL082CP	MOTOROLA	TL082CN
TL082ID	TEXAS	TL082ID
TL082IP	TEXAS	TL082IN
TL084ACD	TEXAS	TL084ACD
TL084ACN	MOTOROLA	TL084ACN
TL084ACN	TEXAS	TL084ACN
TL084BCD	TEXAS	TL084BCD
TL084BCN	MOTOROLA	TL084BCN
TL084BCN	TEXAS	TL084BCN
TL084CD	TEXAS	TL084CD
TL084CN	MOTOROLA	TL084CN
TL084CN	TEXAS	TL084CN
TL084ID	TEXAS	TL084ID
TL084IJ	TEXAS	TL084IJ
TL084IN	TEXAS	TL084IN
TL7702ACP	TEXAS	TL7702ACP
TL7705ACP	TEXAS	TL7705ACP
TL7709ACP	TEXAS	TL7709ACP
TL7712ACP	TEXAS	TL7712ACP
TL7715ACP	TEXAS	TL7715ACP
TLC271ACD	TEXAS	TS271ACD
TLC271ACP	TEXAS	TS271ACN
TLC271AID	TEXAS	TS271AID
TLC271AIP	TEXAS	TS271AIN
TLC271BCD	TEXAS	TS271BCD
TLC271BCP	TEXAS	TS271BCN
TLC271BID	TEXAS	TS271BID
TLC271BIP	TEXAS	TS271BIN
TLC271CD	TEXAS	TS271CD
TLC271CP	TEXAS	TS271CN
TLC271ID	TEXAS	TS271ID
TLC271IP	TEXAS	TS271IN
TLC272ACD	TEXAS	TS272ACD
TLC272ACP	TEXAS	TS272ACN
TLC272AID	TEXAS	TS272AID
TLC272AIP	TEXAS	TS272AIN
TLC272BCD	TEXAS	TS272BCD
TLC272BCP	TEXAS	TS272BCN
TLC272BID	TEXAS	TS272BID
TLC272BIP	TEXAS	TS272BIN
TLC272CD	TEXAS	TS272CD
TLC272CP	TEXAS	TS272CN
TLC272ID	TEXAS	TS272ID
TLC272IP	TEXAS	TS272IN
TLC274ACD	TEXAS	TS274ACD
TLC274ACN	TEXAS	TS274ACN
TLC274AID	TEXAS	TS274AID
TLC274AIP	TEXAS	TS274AIN
TLC274BCD	TEXAS	TS274BCD
TLC274BCN	TEXAS	TS274BCN
TLC274BID	TEXAS	TS274BID
TLC274BIP	TEXAS	TS274BIN
TLC274CD	TEXAS	TS274CD
TLC274CN	TEXAS	TS274CN

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
TLC274ID	TEXAS	TS274ID
TLC274IN	TEXAS	TS274IN
TLC27L2ACD	TEXAS	TS27L2ACD
TLC27L2ACP	TEXAS	TS27L2ACN
TLC27L2AID	TEXAS	TS27L2AID
TLC27L2AIP	TEXAS	TS27L2AIN
TLC27L2BCD	TEXAS	TS27L2BCD
TLC27L2BCP	TEXAS	TS27L2BCN
TLC27L2BID	TEXAS	TS27L2BID
TLC27L2BIP	TEXAS	TS27L2BIN
TLC27L2CD	TEXAS	TS27L2CD
TLC27L2CP	TEXAS	TS27L2CN
TLC27L2ID	TEXAS	TS27L2ID
TLC27L2IP	TEXAS	TS27L2IN
TLC27L4ACD	TEXAS	TS27L4ACD
TLC27L4ACN	TEXAS	TS27L4ACN
TLC27L4AID	TEXAS	TS27L4AID
TLC27L4AIN	TEXAS	TS27L4AIN
TLC27L4BCD	TEXAS	TS27L4BCD
TLC27L4BCN	TEXAS	TS27L4BCN
TLC27L4BID	TEXAS	TS27L4BID
TLC27L4BIN	TEXAS	TS27L4BIN
TLC27L4CD	TEXAS	TS27L4CD
TLC27L4CN	TEXAS	TS27L4CN
TLC27L4ID	TEXAS	TS27L4ID
TLC27L4IN	TEXAS	TS27L4IN
TLC27M2ACD	TEXAS	TS27M2ACD
TLC27M2ACP	TEXAS	TS27M2ACN
TLC27M2AID	TEXAS	TS27M2AID
TLC27M2AIP	TEXAS	TS27M2AIN
TLC27M2BCD	TEXAS	TS27M2BCD
TLC27M2BCP	TEXAS	TS27M2BCN
TLC27M2BID	TEXAS	TS27M2BID
TLC27M2BIP	TEXAS	TS27M2BIN
TLC27M2CD	TEXAS	TS27M2CD
TLC27M2CP	TEXAS	TS27M2CN
TLC27M2ID	TEXAS	TS27M2ID
TLC27M2IP	TEXAS	TS27M2IN
TLC27M4ACD	TEXAS	TS27M4ACD
TLC27M4ACN	TEXAS	TS27M4ACN
TLC27M4AID	TEXAS	TS27M4AID
TLC27M4AIN	TEXAS	TS27M4AIN
TLC27M4BCD	TEXAS	TS27M4BCD
TLC27M4BCN	TEXAS	TS27M4BCN
TLC27M4BID	TEXAS	TS27M4BID
TLC27M4BIN	TEXAS	TS27M4BIN
TLC27M4CD	TEXAS	TS27M4CD
TLC27M4CN	TEXAS	TS27M4CN
TLC27M4ID	TEXAS	TS27M4ID
TLC27M4IN	TEXAS	TS27M4IN
TLC372CD	TEXAS	TS372CD
TLC372CP	TEXAS	TS372CN
TLC372ID	TEXAS	TS372ID
TLC372IP	TEXAS	TS372IN
TLC374CD	TEXAS	TS374CD

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
TLC374CN	TEXAS	TS374CN
TLC374ID	TEXAS	TS374ID
TLC374IN	TEXAS	TS374IN
UA124DM	FAIRCHILD	LM124J
UA139ADM	FAIRCHILD	LM139AJ
UA139DM	FAIRCHILD	LM139J
UA1458RC	FAIRCHILD	MC1458J
UA1458SC	FAIRCHILD	MC1458D
UA1458TC	FAIRCHILD	MC1458N
UA148DM	FAIRCHILD	LM148J
UA1558RM	FAIRCHILD	MC1558J
UA201TC	FAIRCHILD	LM201AN
UA224DV	FAIRCHILD	LM224J
UA224PV	FAIRCHILD	LM224N
UA239DV	FAIRCHILD	LM239J
UA239PV	FAIRCHILD	LM239N
UA239SV	FAIRCHILD	LM239D
UA2901DV	FAIRCHILD	LM2901J
UA2901PV	FAIRCHILD	LM2901N
UA2902PV	FAIRCHILD	LM2902N
UA301ASC	FAIRCHILD	LM301AD
UA301ATC	FAIRCHILD	LM301AN
UA308ASC	FAIRCHILD	LM308AD
UA308ATC	FAIRCHILD	LM308AN
UA308SC	FAIRCHILD	LM308D
UA308TC	FAIRCHILD	LM308N
UA311SC	FAIRCHILD	LM311D
UA311TC	FAIRCHILD	LM331N
UA324DC	FAIRCHILD	LM324J
UA324PC	FAIRCHILD	LM324N
UA324SC	FAIRCHILD	LM324D
UA3302DV	FAIRCHILD	MC3302J
UA3302PV	FAIRCHILD	MC3302N
UA3302SV	FAIRCHILD	MC3303D
UA3303DV	FAIRCHILD	MC3303J
UA3303PV	FAIRCHILD	MC3303N
UA339DC	FAIRCHILD	LM339J
UA339PC	FAIRCHILD	LM339N
UA339SC	FAIRCHILD	LM339D
UA3403DC	FAIRCHILD	MC3403J
UA3403PC	FAIRCHILD	MC3403N
UA3403SC	FAIRCHILD	MC3403D
UA348PC	FAIRCHILD	LM348N
UA3503DM	FAIRCHILD	MC3503J
UA555SC	FAIRCHILD	NE555D
UA555TC	FAIRCHILD	NE555N
UA556PC	FAIRCHILD	NE556N
UA723CFP	THOMSON	LM723CD
UA741AHM	FAIRCHILD	UA741AH
UA741ARM	FAIRCHILD	UA741AJ
UA741CD	SIGNETICS	UA741CD
UA741CD	TEXAS	UA741CD
UA741CFE	SIGNETICS	UA741CJ
UA741CJG	TEXAS	UA741CJ
UA741CN	SIGNETICS	UA741CN

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
UA741CP	TEXAS	UA741CN
UA741EHC	FAIRCHILD	UA741EH
UA741ETC	FAIRCHILD	UA741EN
UA741FE	SIGNETICS	UA741J
UA741HC	FAIRCHILD	UA741CH
UA741HM	FAIRCHILD	UA741H
UA741MJG	TEXAS	UA741J
UA741N	SIGNETICS	UA741N
UA741RC	FAIRCHILD	UA741CJ
UA741RM	FAIRCHILD	UA741CD
UA741TC	FAIRCHILD	UA741CN
UA748CD	TEXAS	UA748CD
UA748CJG	TEXAS	UA748CJ
UA748CP	TEXAS	UA748CN
UA748HC	FAIRCHILD	UA748CH
UA748HM	FAIRCHILD	UA748MH
UA748MJG	TEXAS	UA748J
UA748RC	FAIRCHILD	UA748CJ
UA748RM	FAIRCHILD	UA748J
UA748SC	FAIRCHILD	UA748CD
UA748TC	FAIRCHILD	UA748CN
UA771ASC	FAIRCHILD	TL071BCD
UA771ATC	FAIRCHILD	TL07BCN
UA771BSC	FAIRCHILD	TL071ACD
UA771BTC	FAIRCHILD	TL071ACN
UA771SC	FAIRCHILD	TL071CD
UA771TC	FAIRCHILD	TL071CN
UA772ASC	FAIRCHILD	TL072BCD
UA772ATC	FAIRCHILD	TL072BCN
UA772BSC	FAIRCHILD	TL072ACD
UA772BTC	FAIRCHILD	TL072ACN
UA772SC	FAIRCHILD	TL072CD
UA772TC	FAIRCHILD	TL072CN
UA774BPC	FAIRCHILD	TL072ACN
UA774DC	FAIRCHILD	TL074CJ
UA774PC	FAIRCHILD	TL074CN
UA774SC	FAIRCHILD	TL074CD
UA776HC	FAIRCHILD	UA776CH
UA776HM	FAIRCHILD	UA776MH
UA776SC	FAIRCHILD	UA776CD
UA776TC	FAIRCHILD	UA776CN
UC1840J	UNITRODE	UC1840J
UC1840N	UNITRODE	UC1840N
UC1842J	UNITRODE	UC1842J
UC1842N	UNITRODE	UC1842N
UC2840J	UNITRODE	UC2840J
UC2840N	UNITRODE	UC2840N
UC2842J	UNITRODE	UC2842J
UC2842N	UNITRODE	UC2842N
UC3840J	UNITRODE	UC3840J
UC3840N	UNITRODE	UC3840N
UC3842J	UNITRODE	UC3842J
UC3842N	UNITRODE	UC3842N
ULN2001A	SPRAGUE	ULN2001A
ULN2001AJ	TEXAS	ULQ2001R

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
ULN2001AN	TEXAS	ULN2001A
ULN2001F	PHIL.SIGN.	ULQ2001R
ULN2001N	PHIL.SING.	ULN2001A
ULN2002A	SPRAGUE	ULN2002A
ULN2002AJ	TEXAS	ULQ2002R
ULN2002AN	TEXAS	ULN2002A
ULN2002F	PHIL.SIGN.	ULQ2002R
ULN2002N	PHIL.SIGN.	ULN2002A
ULN2003A	SPRAGUE	ULN2003A
ULN2003AJ	TEXAS	ULQ2003R
ULN2003AN	TEXAS	ULN2003A
ULN2003F	PHIL.SIGN.	ULQ2003R
ULN2003N	PHIL.SIGN.	ULN2003A
ULN2004A	SPRAGUE	ULN2004A
ULN2004AJ	TEXAS	ULQ2004R
ULN2004AN	TEXAS	ULN2004A
ULN2004F	PHIL.SIGN.	ULQ2004R
ULN2004N	PHIL.SIGN.	ULN2004A
ULN2064B	SPRAGUE	ULN2064B
ULN2064NE	TEXAS	ULN2064B
ULN2065B	SPRAGUE	ULN2065B
ULN2065NE	TEXAS	ULN2065B
ULN2066B	SPRAGUE	ULN2066B
ULN2066NE	TEXAS	ULN2066B
ULN2067B	SPRAGUE	ULN2067B
ULN2067NE	TEXAS	ULN2067B
ULN2068B	SPRAGUE	ULN2068B
ULN2068NE	TEXAS	ULN2068B
ULN2069B	SPRAGUE	ULN2069B
ULN2069NE	TEXAS	ULN2069B
ULN2070B	SPRAGUE	ULN2070B
ULN2071B	SPRAGUE	ULN2071B
ULN2074B	SPRAGUE	ULN2074B
ULN2074NE	TEXAS	ULN2074B
ULN2075B	SPRAGUE	ULN2075B
ULN2075NE	TEXAS	ULN2075B
ULN2076B	SPRAGUE	ULN2076B
ULN2077B	SPRAGUE	ULN2077B
ULN2801A	SPRAGUE	ULN2801A
ULN2802A	SPRAGUE	ULN2802A
ULN2803A	SPRAGUE	ULN2803A
ULN2803N	TEXAS	ULN2803A
ULN2804A	SPRAGUE	ULN2804A
ULN2804N	TEXAS	ULN2804A
ULN2805A	SPRAGUE	ULN2805A
uA117KM	FAIRCHILD	LM117K
uA1488DC	FAIRCHILD	MC1488L
uA1488PC	FAIRCHILD	MC1488P
uA1489ADC	FAIRCHILD	MC1489AL
uA1489APC	FAIRCHILD	MC1489AP
uA1489DC	FAIRCHILD	MC1489L
uA1489PC	FAIRCHILD	MC1489P
uA723CDP	THOMSON	LM723CN
uA723CF	PHIL.SIGN.	LM723CJ
uA723CFP	THOMSON	LM723CD

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
uA723CH	THOMSON	LM723CH
uA723CJ	TEXAS	LM723CJ
uA723CN	PHIL.SIGN.	LM723CN
uA723DC	FAIRCHILD	LM723CJ
uA723DM	FAIRCHILD	LM723J
uA723F	PHIL.SIGN.	LM723J
uA723MDG	THOMSON	LM723J
uA723MH	THOMSON	LM723H
uA723MJN	TEXAS	LM723J
uA723PC	FAIRCHILD	LM723CN
uA7805CK	THOMSON	L7805CT
uA7805CKC	TEXAS	L7805CV
uA7805CSP	THOMSON	L7805CV
uA7805KC	FAIRCHILD	L7805CT
uA7805KM	FAIRCHILD	L7805T
uA7805UC	FAIRCHILD	L7805CV
uA7806CK	THOMSON	L7806CT
uA7806CKC	TEXAS	L7806CV
uA7806CSP	THOMSON	L7806CV
uA7806KC	FAIRCHILD	L7806CT
uA7806KM	FAIRCHILD	L7806T
uA7806UC	FAIRCHILD	L7806CV
uA7808CKC	TEXAS	L7808CV
uA7808KC	FAIRCHILD	L7808CT
uA7808KM	FAIRCHILD	L7808T
uA7808UC	FAIRCHILD	L7808CV
uA7812CK	THOMSON	L7812CT
uA7812CKC	TEXAS	L7812CV
uA7812CSP	THOMSON	L7812CV
uA7812KC	FAIRCHILD	L7812CT
uA7812KM	FAIRCHILD	L7812T
uA7812UC	FAIRCHILD	L7812CV
uA7815CK	THOMSON	L7815CT
uA7815CKC	TEXAS	L7815CV
uA7815CSP	THOMSON	L7815CV
uA7815KC	FAIRCHILD	L7815CT
uA7815KM	FAIRCHILD	L7815T
uA7815UC	FAIRCHILD	L7815CV
uA7818CK	THOMSON	L7818CT
uA7818CKC	TEXAS	L7818CV
uA7818CSP	THOMSON	L7818CV
uA7818KC	FAIRCHILD	L7818CT
uA7818KM	FAIRCHILD	L7818T
uA7818UC	FAIRCHILD	L7818CV
uA7824CK	THOMSON	L7824CT
uA7824CKC	TEXAS	L7824CV
uA7824CSP	THOMSON	L7824CV
uA7824KM	FAIRCHILD	L7824T
uA7824UC	FAIRCHILD	L7824CV
uA78M05CKC	TEXAS	L78M05CV
uA78M05UC	FAIRCHILD	L78M05CV
uA78M06CKC	TEXAS	L78M06CV
uA78M06UC	FAIRCHILD	L78M06CV
uA78M08CKC	TEXAS	L78M08CV
uA78M08UC	FAIRCHILD	L78M08CV

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
uA78M12CKC	TEXAS	L78M12CV
uA78M12UC	FAIRCHILD	L78M12CV
uA78M15CKC	TEXAS	L78M15CV
uA78M15UC	FAIRCHILD	L78M15CV
uA78M24CKC	TEXAS	L78M24CV
uA78M24UC	FAIRCHILD	L78MM24CV
uA78S05CK	THOMSON	L78S05CT
uA78S05CSP	THOMSON	L78S05CV
uA78S09CK	THOMSON	L78S09CT
uA78S09CSP	THOMSON	L78S09CV
uA78S12CK	THOMSON	L78S12CT
uA78S12CSP	THOMSON	L78S12CV
uA78S15CK	THOMSON	L78S15CT
uA78S15CSP	THOMSON	L78S15CV
uA7905CK	THOMSON	L7905CT
uA7905CKC	TEXAS	L7905CV
uA7905CSP	THOMSON	L7905CV
uA7905KC	FAIRCHILD	L7905CT
uA7905UC	FAIRCHILD	L7905CV
uA7908CKC	TEXAS	L7908CV
uA7908KC	FAIRCHILD	L7908CT
uA7908UC	FAIRCHILD	L7908CV
uA7912CK	THOMSON	L7912CT
uA7912CKC	TEXAS	L7912CV
uA7912CSP	THOMSON	L7912CV
uA7912KC	FAIRCHILD	L7912CT
uA7912UCF	FAIRCHILD	L7912CV
uA7915CK	THOMSON	L7915CT
uA7915CKC	TEXAS	L7915CV
uA7915CSP	THOMSON	L7915CV
uA7915KC	FAIRCHILD	L7915CT
uA7915UC	FAIRCHILD	L7915CV
uA7918CKC	TEXAS	L7918CV
uA7924CKC	TEXAS	L7924CV
uA7952CKC	TEXAS	L7952CV
uA9665DC	FAIRCHILD	ULQ2001R
uA9665PC	FAIRCHILD	ULN2001A
uA9666DC	FAIRCHILD	ULQ2002R
uA9666PC	FAIRCHILD	ULN2002A
uA9667DC	FAIRCHILD	ULQ2003R
uA9667PC	FAIRCHILD	ULN2003A
uA9668DC	FAIRCHILD	ULQ2004R
uA9668PC	FAIRCHILD	ULN2004A
UPC1458C	NEC	MC1458N
UPC1458G	NEC	MC1458D
UPC1555C	NEC	NE555N
UPC1558C	NEC	MC1558N
UPC156D	NEC	LM208N
UPC157C	NEC	LM201AN
UPC159D	NEC	LM318N
UPC251C	NEC	MC1458IN
UPC251G	NEC	MC1458ID
UPC271C	NEC	LM211N
UPC271G	NEC	LM211D
UPC272C	NEC	LM219N

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
UPC272D	NEC	LM219J
UPC272G	NEC	LM219D
UPC301AC	NEC	LM301AN
UPC311C	NEC	LM311N
UPC319G	NEC	LM319D
UPC324C	NEC	LM324N
UPC324G	NEC	LM324D
UPC339C	NEC	LM339N
UPC339G	NEC	LM339D
UPC3403C	NEC	MC3403N
UPC3403G	NEC	MC3403D
UPC356C	NEC	LF356N
UPC357C	NEC	LF357N
UPC358C	NEC	LM358N
UPC358G	NEC	LM358D
UPC393C	NEC	LM393N
UPC451C	NEC	LM224N
UPC451D	NEC	LM224J
UPC452C	NEC	MC3303N
UPC452G	NEC	MC3303D
UPC4558G	NEC	MC4558CD
UPC4558N	NEC	MC4558CN
UPC4741C	NEC	LM348N

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
FAIRCHILD		
uA117KM	FAIRCHILD	LM117K
UA124DM	FAIRCHILD	LM124J
UA139ADM	FAIRCHILD	LM139AJ
UA139DM	FAIRCHILD	LM139J
UA1458RC	FAIRCHILD	MC1458J
UA1458SC	FAIRCHILD	MC1458D
UA1458TC	FAIRCHILD	MC1458N
UA148DM	FAIRCHILD	LM148J
UA1558RM	FAIRCHILD	MC1558J
UA201TC	FAIRCHILD	LM201AN
UA224DV	FAIRCHILD	LM224J
UA224PV	FAIRCHILD	LM224N
UA239DV	FAIRCHILD	LM239J
UA239PV	FAIRCHILD	LM239N
UA239SV	FAIRCHILD	LM239D
UA2901DV	FAIRCHILD	LM2901J
UA2901PV	FAIRCHILD	LM2901N
UA2902PV	FAIRCHILD	LM2902N
UA301ASC	FAIRCHILD	LM301AD
UA301ATC	FAIRCHILD	LM301AN
UA308ASC	FAIRCHILD	LM308AD
UA308ATC	FAIRCHILD	LM308AN
UA308SC	FAIRCHILD	LM308D
UA308TC	FAIRCHILD	LM308N
UA311SC	FAIRCHILD	LM311D
UA311TC	FAIRCHILD	LM311N
UA324DC	FAIRCHILD	LM324J
UA324PC	FAIRCHILD	LM324N
UA324SC	FAIRCHILD	LM324D
UA3302DV	FAIRCHILD	MC3302J
UA3302PV	FAIRCHILD	MC3302N
UA3302SV	FAIRCHILD	MC3302D
UA3303DV	FAIRCHILD	MC3303J
UA3303PV	FAIRCHILD	MC3303N
UA339DC	FAIRCHILD	LM339J
UA330PC	FAIRCHILD	LM339N
UA339SC	FAIRCHILD	LM339D
UA3403DC	FAIRCHILD	MC3403J
UA3403PC	FAIRCHILD	MC3403N
UA3403SC	FAIRCHILD	MC3403D
UA348DC	FAIRCHILD	LM848J
UA348PC	FAIRCHILD	LM348N
UA3503DM	FAIRCHILD	MC3503J
UA555SC	FAIRCHILD	NE555D
UA555TC	FAIRCHILD	NE555N
UA556PC	FAIRCHILD	NE556N
uA723DC	FAIRCHILD	LM723CJ
uA723DM	FAIRCHILD	LM723J
uA723PC	FAIRCHILD	LM723CN
UA741AHM	FAIRCHILD	UA741AH
UA741ARM	FAIRCHILD	UA741AJ
UA741EHC	FAIRCHILD	UA741EH
UA741ETC	FAIRCHILD	UA741EN
UA741HC	FAIRCHILD	UA741CH
UA741HM	FAIRCHILD	UA741H
UA741RC	FAIRCHILD	UA741CJ
UA741RM	FAIRCHILD	UA741J
UA741SC	FAIRCHILD	UA741CD
UA741TC	FAIRCHILD	UA741CN
UA748HC	FAIRCHILD	UA748CH
UA748HM	FAIRCHILD	UA748MH
UA78RC	FAIRCHILD	UA748CJ
UA748RM	FAIRCHILD	UA748J
UA748SC	FAIRCHILD	UA748CD
UA748TC	FAIRCHILD	UA748CN
UA771ASC	FAIRCHILD	TL071BCD
UA771ATC	FAIRCHILD	TL071BCN
UA771BSC	FAIRCHILD	TL071ACD
UA771BTC	FAIRCHILD	TL071ACN
UA771SC	FAIRCHILD	TL071CD
UA771TC	FAIRCHILD	TL071CN
UA772ASC	FAIRCHILD	TL072BCD
UA772ATC	FAIRCHILD	TL072BCN
UA772BSC	FAIRCHILD	TL072ACD
UA772BTC	FAIRCHILD	TL072ACN
UA772SC	FAIRCHILD	TL072CD
UA772TC	FAIRCHILD	TL072CN
UA774BPC	FAIRCHILD	TL074ACN
UA774DC	FAIRCHILD	TL074CJ
UA774PC	FAIRCHILD	TL074CN
UA774SC	FAIRCHILD	TL074CD
UA776HC	FAIRCHILD	UA776CH
UA776HM	FAIRCHILD	UA776MH
UA776SC	FAIRCHILD	UA776CD
UA776TC	FAIRCHILD	UA776CN
uA7805KC	FAIRCHILD	L7805CT
uA7805KM	FAIRCHILD	L7805T
uA7805UC	FAIRCHILD	L7805CV
uA7806KC	FAIRCHILD	L7806CT
uA7806KM	FAIRCHILD	L7806T
uA7806UC	FAIRCHILD	L7806CV
uA7808KC	FAIRCHILD	L7808CT
uA7808KM	FAIRCHILD	L7808T
uA7808UC	FAIRCHILD	L7808CV
uA7812KC	FAIRCHILD	L7812CT
uA7812KM	FAIRCHILD	L7812T
uA7812UC	FAIRCHILD	L7812CV
uA7815KC	FAIRCHILD	L7815CT
uA7815KM	FAIRCHILD	L7815T
uA7815UC	FAIRCHILD	L7815CV
uA7818KC	FAIRCHILD	L7818CT
uA7818KM	FAIRCHILD	L7818T
uA7818UC	FAIRCHILD	L7818CV
uA7824KM	FAIRCHILD	L7824T
uA7824UC	FAIRCHILD	L7824CV
uA78M05UC	FAIRCHILD	L78M05CV
uA78M06UC	FAIRCHILD	L78M06CV
uA78M08UC	FAIRCHILD	L78M08CV

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
uA78M12UC	FAIRCHILD	L78M12CV
uA78M15UC	FAIRCHILD	L78M15CV
uA78M24UC	FAIRCHILD	L78M24CV
uA7905KC	FAIRCHILD	L7905CT
uA7905UC	FAIRCHILD	L7905CV
uA7908KC	FAIRCHILD	L7908CT
uA7908UC	FAIRCHILD	L7908CV
uA7912KC	FAIRCHILD	L7912CT
uA7912UC	FAIRCHILD	L7912CV
uA7915KC	FAIRCHILD	L7915CT
uA7915UC	FAIRCHILD	L7915CV
	MOTOROLA	
LM223K	MOTOROLA	LM223K
LM237K	MOTOROLA	LM237K
LM323K	MOTOROLA	LM323K
LM337K	MOTOROLA	LM337K
LM337T	MOTOROLA	LM337SP
LF347N	MOTOROLA	LF347N
LF351N	MOTOROLA	LF351N
LF353N	MOTOROLA	LF353N
LF355N	MOTOROLA	LF355N
LF356N	MOTOROLA	LF356N
LF357N	MOTOROLA	LF357N
LM124J	MOTOROLA	LM124J
LM139AJ	MOTOROLA	LM139AJ
LM139J	MOTOROLA	LM139J
LM148J	MOTOROLA	LM148J
LM158J	MOTOROLA	LM158J
LM201AD	MOTOROLA	LM201AD
LM201AN	MOTOROLA	LM201AN
LM211D	MOTOROLA	LM211D
LM224D	MOTOROLA	LM224D
LM224J	MOTOROLA	LM224J
LM239AJ	MOTOROLA	LM239J
LM239D	MOTOROLA	LM239D
LM239J	MOTOROLA	LM239J
LM258D	MOTOROLA	LM258D
LM2901D	MOTOROLA	LM2901D
LM2901J	MOTOROLA	LM2901J
LM2901N	MOTOROLA	LM2901N
LM2902D	MOTOROLA	LM2902D
LM2902J	MOTOROLA	LM2902J
LM2902N	MOTOROLA	LM2902J
LM2903D	MOTOROLA	LM2903D
LM2903N	MOTOROLA	LM2903N
LM2904D	MOTOROLA	LM2904D
LM2904N	MOTOROLA	LM2904N
LM301AD	MOTOROLA	LM301AD
LM301AJ	MOTOROLA	LM301AJ
LM301AN	MOTOROLA	LM301AN
LM301AD	MOTOROLA	LM308AD
LM308AN	MOTOROLA	LM308AN
LM308D	MOTOROLA	LM308D
LM308J	MOTOROLA	LM308J

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
LM308N	MOTOROLA	LM308N
LM311D	MOTOROLA	LM311D
LM311J	MOTOROLA	LM311J
LM311N	MOTOROLA	LM311N
LM324AJ	MOTOROLA	LM324AJ
LM324D	MOTOROLA	LM324D
LM324J	MOTOROLA	LM324J
LM324N	MOTOROLA	LM324N
LM339AJ	MOTOROLA	LM339AJ
LM339AN	MOTOROLA	LM339AN
LM339D	MOTOROLA	LM339D
LM339N	MOTOROLA	LM339N
LM348D	MOTOROLA	LM348D
LM348N	MOTOROLA	LM348N
LM358D	MOTOROLA	LM358D
LM358J	MOTOROLA	LM358J
LM358N	MOTOROLA	LM358N
LM393AN	MOTOROLA	LM393AN
LM393D	MOTOROLA	LM393D
LM393N	MOTOROLA	LM393N
MC1455D	MOTOROLA	N3555D
MC1455P1	MOTOROLA	NE555N
MC1455U	MOTOROLA	NE555J
MC1458D	MOTOROLA	MC1458D
MC1458P1	MOTOROLA	MC1458N
MC1458U	MOTOROLA	MC1458J
MC1558U	MOTOROLA	MC1558J
MC1741CD	MOTOROLA	UA741CD
MC1741CG	MOTOROLA	UA741CH
MC1741CP1	MOTOROLA	UA741CN
MC1741CU	MOTOROLA	UA741CJ
MC1741G	MOTOROLA	UA741H
MC1741U	MOTOROLA	UA741J
MC1748CD	MOTOROLA	UA748CD
MC1748CG	MOTOROLA	UA748CH
MC1748CP1	MOTOROLA	UA748CN
MC1748CU	MOTOROLA	UA748CJ
MC1748G	MOTOROLA	UA748MH
MC1748U	MOTOROLA	UA748J
MC1776CD	MOTOROLA	UA776CD
MC1776CG	MOTOROLA	UA776CH
MC1776CP1	MOTOROLA	UA776CN
MC1776G	MOTOROLA	UA776MH
MC3302D	MOTOROLA	MC3302D
MC3302L	MOTOROLA	MC3302J
MC3302P	MOTOROLA	MC3302N
MC3303L	MOTOROLA	MC3303J
MC3303P	MOTOROLA	MC3303N
MC34001AP	MOTOROLA	MC34001AN
MC34001BP	MOTOROLA	MC34001BN
MC34001P	MOTOROLA	MC34001N
MC34002AP	MOTOROLA	MC34002AN
MC34002BP	MOTOROLA	MC34002BN
MC34002P	MOTOROLA	MC34002N
MC34004AP	MOTOROLA	MC34004AN

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
MC34004BP	MOTOROLA	MC34004BN
MC34004P	MOTOROLA	MC34004N
MC3403D	MOTOROLA	MC3403D
MC3403L	MOTOROLA	MC3403J
MC3403P	MOTOROLA	MC3403N
MC3456L	MOTOROLA	NE556J
MC3456P	MOTOROLA	NE556N
MC3503L	MOTOROLA	MC3503J
MC3556L	MOTOROLA	SE556J
MC4558CP1	MOTOROLA	MC4558CN
MC4558CU	MOTOROLA	MC4558CJ
MC7805ACT	MOTOROLA	L7805ACV
MC7805CK	MOTOROLA	L7805CT
MC7805CT	MOTOROLA	L7805CV
MC7805K	MOTOROLA	L7805T
MC7606ACT	MOTOROLA	L7606ACV
MC7806CK	MOTOROLA	L78C6CT
MC7806CT	MOTOROLA	L7806CV
MC7806K	MOTOROLA	L7806T
MC7808ACT	MOTOROLA	L7808ACV
MC7808CK	MOTROLA	L7808CT
MC7808CT	MOTOROLA	L7808CV
MC7808K	MOTOROLA	L7808T
MC7812ACT	MOTOROLA	L7812ACV
MC7812CK	MOTOROLA	L7812CT
MC7812CT	MOTOROLA	L7812CV
MC7812K	MOTOROLA	L7812T
MC7815ACT	MOTOROLA	L7815ACV
MC7815CK	MOTOROLA	L7815CT
MC7815CT	MOTOROLA	L7815CV
MC7815K	MOTOROLA	L7815T
MC7818ACT	MOTOROLA	L7818ACV
MC7818CK	MOTOROLA	L7818CT
MC7818CT	MOTOROLA	L7818CV
MC7818K	MOTOROLA	L7818T
MC7824ACT	MOTOROLA	L7824ACV
MC7824ACT	MOTOROLA	L7824CV
MC7824K	MOTOROLA	L7824T
MC78M05CT	MOTOROLA	L78M05CV
MC78M08CT	MOTOROLA	L78M06CV
MC78M08CT	MOTOROLA	L78M08CV
MC78M12CT	MOTOROLA	L78M12CV
MC78M15CT	MOTOROLA	L78M15CV
MC78M18CT	MOTOROLA	L78M18CV
MC78M24CT	MOTOROLA	L78M24CV
MC7905CK	MOTOROLA	L7905CT
MC7905CT	MOTOROLA	L7905CV
MC7908CK	MOTOROLA	L7908CT
MC7908CT	MOTOROLA	L7908CV
MC7912CK	MOTOROLA	L7912CT
MC7912CT	MOTOROLA	L7912CV
MC7915CK	MOTOROLA	L7915CT
MC7915CT	MOTOROLA	L7915CV
MC7918CK	MOTOROLA	L7918CT
MC7918CT	MOTOROLA	L7918CV

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
MC7924CK	MOTOROLA	L7924CT
MC7924CT	MOTOROLA	L7924CV
MC7952CK	MOTOROLA	L7952CT
MC7952CT	MOTOROLA	L7952CV
TL070ACP	MOTOROLA	TL072ACN
TL071ACP	MOTOROLA	TL071ACN
TL071BCP	MOTOROLA	TL071BCN
TL071CP	MOTOROLA	TL071CN
TL072BCP	MOTOROLA	TL072BCN
TL072CP	MOTOROLA	TL072CN
TL074ACN	MOTOROLA	TL074ACN
TL074BCN	MOTOROLA	TL074BCN
TL074CJ	MOTOROLA	TL074CJ
TL074CN	MOTOROLA	TL074CN
TL081ACP	MOTOROLA	TL081ACN
TL081BCP	MOTOROLA	TL081BCN
TL081CP	MOTOROLA	TL081CN
TL082ACP	MOTOROLA	TL082ACN
TL082BCP	MOTOROLA	TL082BCN
TL082CP	MOTOROLA	TL082CN
TL084ACJ	MOTOROLA	TL084ACJ
TL084ACN	MOTOROLA	TL084ACN
TL084BCJ	MOTOROLA	TL084BCJ
TL084BCN	MOTOROLA	TL084BCN
TL084CJ	MOTOROLA	TL084CJ
TL084CN	MOTOROLA	TL84CN
	NATIONAL	
LM223K	NATIONAL	LM223K
LM237K	NATIONAL	LM237K
LM238K	NATIONAL	LM238K
LF255M	NATIONAL	LF255D
LF255N	NATIONAL	LF255N
LF256M	NATIONAL	LF256D
LF256N	NATIONAL	LF256N
LF257M	NATIONAL	LF257D
LF257N	NATIONAL	LF257N
LM317K	NATIONAL	LM317K
LM317T	NATIONAL	LM317T
LM323K	NATIONAL	LM323K
LM337K	NATIONAL	LM337K
LM337T	NATIONAL	LM337SP
LF347J	NATIONAL	LF347J
LF347M	NATIONAL	LF347D
LF347N	NATIONAL	LF347N
LF351M	NATIONAL	LF351D
LF351N	NATIONAL	LF351N
LF353M	NATIONAL	LF353D
LF353N	NATIONAL	LF353N
LF355AM	NATIONAL	LF355AD
LF355AN	NATIONAL	LF355AN
LF355M	NATIONAL	LF355D
LF355N	NATIONAL	LF355N
LF356AM	NATIONAL	LF356AD
LF356AN	NATIONAL	LF356AN

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
LF356M	NATIONAL	LF356D
LF356N	NATIONAL	LF356N
LF357AM	NATIONAL	LF357AD
LF357M	NATIONAL	LF357D
LF357N	NATIONAL	LF357N
LM101AM	NATIONAL	LM101AD
LM119J	NATIONAL	LM119J
LM124AJ	NATIONAL	LM124AJ
LM124J	NATIONAL	LM124J
LM139AJ	NATIONAL	LM139AJ
LM139J	NATIONAL	LM139J
LM1458M	NATIONAL	MC1458D
LM1458N	NATIONAL	MC1458N
LM146J	NATIONAL	LM146J
LM148J	NATIONAL	LM148J
LM158AJ	NATIONAL	LM158AJ
LM158J	NATIONAL	LM158J
LM193AJ	NATIONAL	LM193AJ
LM193J	NATIONAL	LM193J
LM201AM	NATIONAL	LM201AD
LM201AN	NATIONAL	LM201AN
LM219J	NATIONAL	LM219J
LM224AJ	NATIONAL	LM224AJ
LM224J	NATIONAL	LM224J
LM239AJ	NATIONAL	LM239AJ
LM239J	NATIONAL	LM239J
LM246J	NATIONAL	LM246J
LM2901J	NATIONAL	LM2901J
LM2901M	NATIONAL	LM2901D
LM2901N	NATIONAL	LM2901N
LM2902J	NATIONAL	LM2902J
LM2902M	NATIONAL	LM2902D
LM2902N	NATIONAL	LM2902N
LM2903M	NATIONAL	LM2903D
LM2903N	NATIONAL	LM2903N
LM2904J	NATIONAL	LM2904J
LM2904M	NATIONAL	LM2904D
LM2904N	NATIONAL	LM2904N
LM293AJ	NATIONAL	LM293AJ
LM293J	NATIONAL	LM293J
LM293N	NATIONAL	LM293N
LM301AJ	NATIONAL	LM301AJ
LM301AM	NATIONAL	LM301AN
LM301AN	NATIONAL	LM301AN
LM308AJ-8	NATIONAL	LM308AJ
LM308AM	NATIONAL	LM308AD
LM308AN	NATIONAL	LM308AN
LM308M	NATIONAL	LM308D
LM308N	NATIONAL	LM308N
LM311J-8	NATIONAL	LM311J
LM311M	NATIONAL	LM311D
LM311N	NATIONAL	LM311N
LM318M	NATIONAL	LM318D
LM318N	NATIONAL	LM318N

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
LM319J	NATIONAL	LM319J
LM319M	NATIONAL	LM319D
LM319N	NATIONAL	LM319N
LM324AJ	NATIONAL	LM324AJ
LM324AM	NATIONAL	LM324AD
LM324AN	NATIONAL	LM324AN
LM324J	NATIONAL	LM324J
LM324M	NATIONAL	LM324D
LM324N	NATIONAL	LM324N
LM3302J	NATIONAL	MC3302J
LM3302N	NATIONAL	MC3302N
LM3303N	NATIONAL	MC3303N
LM334Z	NATIONAL	LM334Z
LM335Z	NATIONAL	LM335Z
LM336BM	NATIONAL	LM336BD
LM336BZ	NATIONAL	LM336BZ
LM336M	NATIONAL	LM336D
LM336Z	NATIONAL	LM336Z
LM333AJ	NATIONAL	LM339AJ
LM339AM	NATIONAL	LM339AD
LM339AN	NATIONAL	LM339AN
LM339J	NATIONAL	LM339J
LM339M	NATIONAL	LM339D
LM339N	NATIONAL	LM339N
LM3403J	NATIONAL	MC3403J
LM3403M	NATIONAL	MC3403D
LM3403N	NATIONAL	MC3403N
LM346J	NATIONAL	LM346J
LM346M	NATIONAL	LM346D
LM346N	NATIONAL	LM346N
LM348M	NATIONAL	LM348D
LM348N	NATIONAL	LM348N
LM3503J	NATIONAL	MC3503J
LM358AM	NATIONAL	LM358AD
LM358AN	NATIONAL	LM358AN
LM358J	NATIONAL	LM358J
LM358M	NATIONAL	LM358D
LM358N	NATIONAL	LM358N
LM393AJ	NATIONAL	LM393AJ
LM393AN	NATIONAL	LM393AN
LM393J	NATIONAL	LM393J
LM393M	NATIONAL	LM393D
LM393N	NATIONAL	LM393N
LM555CJ	NATIONAL	NE555J
LM555CM	NATIONAL	NE555D
LM555CN	NATIONAL	NE555N
LM556CJ	NATIONAL	NE556J
LM556CM	NATIONAL	NE556D
LM556CN	NATIONAL	NE556N
LM556J	NATIONAL	SE556J
LM723CH	NATIONAL	LM723CH
LM723CJ	NATIONAL	LM723CD
LM723CM	NATIONAL	LM723CD
LM723CN	NATIONAL	LM723CN
LM723H	NATIONAL	LM723H

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
LM723J	NATIONAL	LM723J
LM741AH	NATIONAL	UA741AH
UM741AJ	NATIONAL	UA741AJ
LM741CH	NATIONAL	UA741CH
LM741CJ	NATIONAL	UA741CJ
LM741CM	NATIONAL	UA741CD
LM741CN	NATIONAL	UA741CN
LM741EH	NATIONAL	UA741EH
LM741EN	NATIONAL	UA741EN
LM741H	NATIONAL	UA741H
LM741J	NATIONAL	UA741J
LM748CH	NATIONAL	UA748CH
LM748CJ	NATIONAL	UA748CJ
LM748CN	NATIONAL	UA748CN
LM748H	NATIONAL	UA748MH
LM748J	NATIONAL	UA748J
LM7805CK	NATIONAL	L7805CT
LM7805CT	NATIONAL	L7805CV
LM7812CK	NATIONAL	L7812CT
LM7812CT	NATIONAL	L7812CV
LM7815CK	NATIONAL	L7815CT
LM7815CT	NATIONAL	L7815CV
LM7905CK	NATIONAL	L7905CT
LM7905CT	NATIONAL	L7905CV
LM7912CK	NATIONAL	L7912CT
LM7912CT	NATIONAL	L7912CV
LM7915CK	NATIONAL	L7915CT
LM7915CT	NATIONAL	L7915CV
LMC660AIN	NATIONAL	TS27M4BIN
LMC660CN	NATIONAL	TS27M4ACN
NEC		
UPC1458C	NEC	MC1458N
UPC1458G	NEC	MC1458D
UPC1555C	NEC	NE555N
UPC1558C	NEC	NC1558N
UPC156D	NEC	LM208N
UPC157C	NEC	LM201AN
UPC159D	NEC	LM318N
UPC251C	NEC	MC318N
UPC251G	NEC	MC1458IN
UPC251G	NEC	MC1458ID
UPC271C	NEC	LM211N
UPC271G	NEC	LM211D
UPC272C	NEC	LM219N
UPC272D	NEC	LM219J
UPC272G	NEC	LM219D
UPC301AC	NEC	LM301AN
UPC311C	NEC	LM311N
UPC319G	NEC	LM319D
UPC324C	NEC	LM324N
UPC324G	NEC	LM324D
UPC339C	NEC	LM339N
UPC339G	NEC	LM339D
UPC3403C	NEC	MC3403N

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
UPC3403G	NEC	MC3403D
UPC356C	NEC	LF356N
UPC357C	NEC	LF357N
UPC358C	NEC	LM358N
UPC358G	NEC	LM358D
UPC393C	NEC	LM393N
UPC451C	NEC	LM224N
UPC451D	NEC	LM224J
UPC452C	NEC	MC3303N
UPC452G	NEC	MC3303D
UPC4558G	NEC	MC4558CD
UPC4558N	NEC	MC4558CN
UPC4741C	NEC	LM348N
UPC4741G	NEC	LM348D
UPC741C	NEC	UA741CN
RCA		
CA081AE	RCA	TL081ACN
CA081BE	RCA	TL081BCN
CA081E	RCA	TL081CN
CA082AE	RCA	TL082ACN
CA082BE	RCA	TL082BCN
CA082E	RCA	TL082CN
CA08AE	RCA	TL084ACN
CA084BE	RCA	TL084BCN
CA084E	RCA	TL084CN
CA124E	RCA	LM124N
CA139AF	RCA	LM139AJ
CA139E	RCA	LM139N
CA139F	RCA	LM139J
CA1458E	RCA	MC1458N
CA1558E	RCA	MC1558N
CA158E	RCA	LM158N
CA224E	RCA	LM224N
CA239AE	RCA	LM239AN
CA239AF	RCA	LM239AJ
CA239E	RCA	LM239N
CA239F	RCA	LM239J
CA258E	RCA	LM258N
CA2901E	RCA	LM2901N
CA2901F	RCA	LM2901J
CA2902E	RCA	LM2902N
CA2904E	RCA	LM2904N
CA301AE	RCA	LM301AN
CA311E	RCA	LM311N
CA324E	RCA	LM324N
CA3290E	RCA	LM393N
CA339AE	RCA	LM339AN
CA339AF	RCA	LM339AJ
CA339E	RCA	LM339N
CA339F	RCA	LM339J
CA358AE	RCA	LM358AN
CA358E	RCA	LM358N
CA555E	RCA	NE555N
CA741CE	RCA	UA741CN

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
CA741CT	RCA	UA741CH
CA741E	RCA	UA741EN
CA741T	RCA	UA741H
CA748CE	RCA	UA748CN
CA748CT	RCA	UA748CH
CA748T	RCA	UA748J
SIEMENS		
TBA222	SIEMENS	UA741H
TBA222B	SIEMENS	UA741N
TBB741G	SIEMENS	UA741CD
SIGNETICS		
LM111D	SIGNETICS	LM111D
LM119D	SIGNETICS	LM119D
LM119F	SIGNETICS	LM119J
LM124D	SIGNETICS	LM124D
LM124F	SIGNETICS	LM124J
LM124N	SIGNETICS	LM124N
LM139AD	SIGNETICS	LM139AD
LM139AF	SIGNETICS	LM139AJ
LM139D	SIGNETICS	LM139D
LM139F	SIGNETICS	LM139J
LM139N	SIGNETICS	LM139N
LM158F	SIGNETICS	LM158J
LM158N	SIGNETICS	LM158N
LM193AF	SIGNETICS	LM193AJ
LM193D	SIGNETICS	LM193D
LM193N	SIGNETICS	LM193N
LM211D	SIGNETICS	LM211D
LM211N	SIGNETICS	LM211N
LM219D	SIGNETICS	LM219D
LM219F	SIGNETICS	LM219J
LM224D	SIGNETICS	LM224D
LM224F	SIGNETICS	LM224J
LM224N	SIGNETICS	LM224N
LM239D	SIGNETICS	LM239AD
LM239AF	SIGNETICS	LM239AJ
LM239AN	SIGNETICS	LM239AN
LM239D	SIGNETICS	LM239D
LM239F	SIGNETICS	LM239J
LM239N	SIGNETICS	LM239N
LM258F	SIGNETICS	LM258J
LM258N	SIGNETICS	LM258N
LM2901D	SIGNETICS	LM2901D
LM2901F	SIGNETICS	LM2901J
LM2901N	SIGNETICS	LM2901N
LM2903F	SIGNETICS	LM2903J
LM2903N	SIGNETICS	LM2903N
LM293AF	SIGNETICS	LM293AJ
LM293F	SIGNETICS	LM293J
LM293N	SIGNETICS	LM293N
LM311D	SIGNETICS	LM311D
LM311F	SIGNETICS	LM311J
LM311N	SIGNETICS	LM311N

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
LM319D	SIGNETICS	LM319D
LM319F	SIGNETICS	LM319J
LM324D	SIGNETICS	LM324D
LM324F	SIGNETICS	LM324J
LM324N	SIGNETICS	LM324N
LM339AD	SIGNETICS	LM339AD
LM339AF	SIGNETICS	LM339AJ
LM339AN	SIGNETICS	LM339AN
LM339D	SIGNETICS	LM339D
LM339F	SIGNETICS	LM339J
LM339N	SIGNETICS	LM339N
LM358D	SIGNETICS	LM358D
LM358F	SIGNETICS	LM358J
LM358N	SIGNETICS	LM358N
LM393AF	SIGNETICS	LM393AJ
LM393AN	SIGNETICS	LM393AN
LM393D	SIGNETICS	LM393D
LM393F	SIGNETICS	LM393J
LM393N	SIGNETICS	LM393N
MC1458D	SIGNETICS	MC1458D
MC1458FE	SIGNETICS	MC1458J
MC1458N	SIGNETICS	MC1458N
MC1558D	SIGNETICS	MC1558D
MC1558FE	SIGNETICS	MC1558J
MC1558N	SIGNETICS	MC1558N
MC3302D	SIGNETICS	MC3302D
MC3302F	SIGNETICS	MC3302J
MC3302N	SIGNETICS	MC3302N
MC3303D	SIGNETICS	MC3303D
MC3303F	SIGNETICS	MC3303J
MC3303N	SIGNETICS	MC3303N
MC3403CF	SIGNETICS	MC3403J
MC3403CN	SIGNETICS	MC3403N
MC3403D	SIGNETICS	MC3403D
MC3503F	SIGNETICS	MC3503J
NE4558D	SIGNETICS	MC4558CD
NE4558F	SIGNETICS	MC4558CJ
NE4558N	SIGNETICS	MC4558CN
NE532D	SIGNETICS	NE532D
NE532F	SIGNETICS	NE532J
NE532N	SIGNETICS	NE532N
NE555D	SIGNETICS	NE555D
NE555F	SIGNETICS	NE555J
NE555N	SIGNETICS	NE555N
NE556D	SIGNETICS	NE556D
NE556F	SIGNETICS	NE556J
NE556N	SIGNETICS	NE556N
SA1458D	SIGNETICS	MC1458ID
SA1458N	SIGNETICS	MC1458IN
SA4558D	SIGNETICS	MC4558ID
SA4558N	SIGNETICS	MC4558IN
SA532D	SIGNETICS	LM2904D
SA532FE	SIGNETICS	LM2904J
SA532N	SIGNETICS	LM2904N
SA534D	SIGNETICS	LM2902D

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
SA534F	SIGNETICS	LM2902J
SA534N	SIGNETICS	LM2902N
SA741CN	SIGNETICS	UA741IN
SE556F	SIGNETICS	SE556J
uA723CFP	SIGNETICS	LM723CJ
uA723CN	SIGNETICS	LM723CN
uA723F	SIGNETICS	LM723J
UA741CD	SIGNETICS	UA741CD
UA741CFE	SIGNETICS	UA741CJ
UA741CN	SIGNETICS	UA741CN
UA741FE	SIGNETICS	UA741J
UA741N	SIGNETICS	UA741N
	TEXAS	
LM124AJ	TEXAS	LM124AJ
LM124J	TEXAS	LM124J
LM139AJ	TEXAS	LM139AJ
LM139J	TEXAS	LM139J
LM14BJ	TEXAS	LM148J
LM158AJG	TEXAS	LM158AJ
LM158JG	TEXAS	LM158J
LM193AJG	TEXAS	LM193AJ
LM201AD	TEXAS	LM201AD
LM201AP	TEXAS	LM201AN
LM211D	TEXAS	LM211D
LM211P	TEXAS	LM211N
LM224AD	TEXAS	LM224AD
LM224AJ	TEXAS	LM224AJ
LM224AN	TEXAS	LM224AN
LM224D	TEXAS	LM224D
LM224J	TEXAS	LM224J
LM224N	TEXAS	LM224N
LM239AD	TEXAS	LM239AD
LM239AJ	TEXAS	LM239AJ
LM239AN	TEXAS	LM239AN
LM239D	TEXAS	LM239D
LM239J	TEXAS	LM239J
LM239N	TEXAS	LM239N
LM248D	TEXAS	LM248D
LM248N	TEXAS	LM248N
LM258AJG	TEXAS	LM258AJ
LM258D	TEXAS	LM258D
LM258JG	TEXAS	LM258J
LM258P	TEXAS	LM258N
LM2901D	TEXAS	LM2901D
LM2901J	TEXAS	LM2901J
LM2901N	TEXAS	LM2901N
LM2902D	TEXAS	LM2902D
LM2902J	TEXAS	LM2902J
LM2902N	TEXAS	LM2902N
LM2903D	TEXAS	LM2903D
LM2903JG	TEXAS	LM2903J
LM2903P	TEXAS	LM2903N
LM2904D	TEXAS	LM2904D
LM2904JG	TEXAS	LM2904J

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
LM2904P	TEXAS	LM2904N
LM293AJG	TEXAS	LM293AJ
LM293D	TEXAS	LM293D
LM293JG	TEXAS	LM293J
LM301AD	TEXAS	LM301AD
LM301AJG	TEXAS	LM301AJ
LM301AP	TEXAS	LM301AN
LM311D	TEXAS	LM311D
LM311JG	TEXAS	LM311J
LM311P	TEXAS	LM311N
LM318D	TEXAS	LM318D
LM318P	TEXAS	LM318N
LM324AD	TEXAS	LM324AD
LM324AJ	TEXAS	LM324AJ
LM324AN	TEXAS	LM324AN
LM324D	TEXAS	LM324D
LM324J	TEXAS	LM324J
LM324N	TEXAS	LM324N
LM3302D	TEXAS	MC3302D
LM3302J	TEXAS	MC3302J
LM3302N	TEXAS	MC3302N
LM337KC	TEXAS	LM337SP
LM339AD	TEXAS	LM339AD
LM339AJ	TEXAS	LM339AJ
LM339AN	TEXAS	LM339AN
LM339D	TEXAS	LM339D
LM339J	TEXAS	LM339J
LM339N	TEXAS	LM399N
LM348D	TEXAS	LM348D
LM348N	TEXAS	LM348N
LM358AD	TEXAS	LM358AD
LM358AJG	TEXAS	LM358AJ
LM358AP	TEXAS	LM358AN
LM358D	TEXAS	LM358D
LM358JG	TEXAS	LM358J
LM368P	TEXAS	LM368N
LM393AD	TEXAS	LM393AD
LM393AJG	TEXAS	LM393AJ
LM393AP	TEXAS	LM393AN
LM3930	TEXAS	LM393D
LM393JG	TEXAS	LM393J
LM393P	TEXAS	LM293N
LM393P	TEXAS	LM393N
MC1458D	TEXAS	MC1458D
MC1458JG	TEXAS	MC1458J
MC1458P	TEXAS	MC1458N
MC1558JG	TEXAS	MC1558J
MC3303D	TEXAS	MC3303D
MC3303J	TEXAS	MC3303J
MC3303N	TEXAS	MC3303N
MC3403D	TEXAS	MC3403D
MC3403J	TEXAS	MC3403J
MC3403N	TEXAS	MC3403N
MC3503J	TEXAS	MC3503J
NE555D	TEXAS	NE555D

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
NE555JG	TEXAS	NE555J
NE556P	TEXAS	NE555N
NE556D	TEXAS	NE556D
NE556J	TEXAS	NE556J
NE556N	TEXAS	NE556N
RCA558D	TEXAS	MC4558CD
RCA558JG	TEXAS	MC4558CJ
RC4558P	TEXAS	MC4558CN
RV4558D	TEXAS	MC4558ID
RV4558P	TEXAS	MC4558IN
SA655D	TEXAS	SA655D
SA555JG	TEXAS	SA555J
SA556P	TEXAS	SA556N
SA556D	TEXAS	SA556D
SA556J	TEXAS	SA556J
SA556N	TEXAS	SA556N
SE655JG	TEXAS	SE665J
SE556J	TEXAS	SE556J
TL061ACD	TEXAS	TL061ACD
TL061ACP	TEXAS	TL061ACN
TL061BCD	TEXAS	TL061BCD
TL061BCP	TEXAS	TL061BCN
TL061CD	TEXAS	TL061CD
TL061CP	TEXAS	TL061CN
TL061ID	TEXAS	TL061ID
TL061IP	TEXAS	TL061IN
TL062ACP	TEXAS	TL062ACN
TL062ACPD	TEXAS	TL062ACD
TL062BCD	TEXAS	TL062BCD
TL062BCP	TEXAS	TL062BCN
TL062CD	TEXAS	TL062CD
TL062CP	TEXAS	TL062CN
TL062ID	TEXAS	TL062ID
TL062IP	TEXAS	TL062IN
TL064ACD	TEXAS	TL064ACD
TL064ACN	TEXAS	TL064ACN
TL064BCD	TEXAS	TL0648CD
TL0648CN	TEXAS	TL0648CN
TL064CD	TEXAS	TL064CD
TL064CN	TEXAS	TL064CN
TL064ID	TEXAS	TL064ID
TL064IN	TEXAS	TL064IN
TL071ACD	TEXAS	TL071ACD
TL071ACP	TEXAS	TL071ACN
TL071BCD	TEXAS	TL071BCD
TL071BCP	TEXAS	TL071BCN
TL071CD	TEXAS	TL071CD
TL071CP	TEXAS	TL071CN
TL071ID	TEXAS	TL071ID
TL071IP	TEXAS	TL071IN
TL072ACD	TEXAS	TL072ACD
TL072ACP	TEXAS	TL072ACN
TL072BCD	TEXAS	TL072BCD
TL072BCP	TEXAS	TL072BCN
TL072CD	TEXAS	TL072CD

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
TL072CP	TEXAS	TL072CN
TL072ID	TEXAS	TL072ID
TL072IP	TEXAS	TL072IN
TL074ACD	TEXAS	TL074ACD
TL074ACN	TEXAS	TL074ACN
TL074BCD	TEXAS	TL074BCD
TL074BCN	TEXAS	TL074BCN
TL074CD	TEXAS	TL074CD
TL074CN	TEXAS	TL074CN
TL074ID	TEXAS	TL074ID
TL074IN	TEXAS	TL074IN
TL081ACD	TEXAS	TL081ACD
TL081ACP	TEXAS	TL081ACN
TL081BCD	TEXAS	TL081BCD
TL081BCP	TEXAS	TL081BCN
TL081CD	TEXAS	TL081CD
TL081CP	TEXAS	TL081CN
TL081ID	TEXAS	TL081ID
TL081ID	TEXAS	TL081IN
TL082ACD	TEXAS	TL082ACD
TL082BCD	TEXAS	TL082BCD
TL082BCP	TEXAS	TL082BCN
TL082CD	TEXAS	TL082CD
TL082CP	TEXAS	TL082CN
TL082ID	TEXAS	TL082ID
TL082IP	TEXAS	TL082IN
TL084ACD	TEXAS	TL084ACD
TL084ACN	TEXAS	TL084ACN
TL084BCD	TEXAS	TL084BCD
TL084BCN	TEXAS	TL084BCN
TL084CD	TEXAS	TL084CD
TL08CN	TEXAS	TL084CN
TL084ID	TEXAS	TL084ID
TL084IN	TEXAS	TL084IN
TLC271ACD	TEXAS	TS271ACD
TLC271ACP	TEXAS	TS271ACN
TLC271AID	TEXAS	TS271AID
TLC271AIP	TEXAS	TS271AIN
TLC271BCD	TEXAS	TS271BCD
TLC271BCP	TEXAS	TS271BCN
TLC271BID	TEXAS	TS271BID
TLC271BIP	TEXAS	TS271BIN
TLC271CD	TEXAS	TS271CD
TLC271CP	TEXAS	TS271CN
TLC271ID	TEXAS	TS271ID
TLC271IP	TEXAS	TS271IN
TLC272ACD	TEXAS	TS272ACD
TLC272ACP	TEXAS	TS272ACN
TLC272AID	TEXAS	TS272AID
TLC272AIP	TEXAS	TS272AIN
TLC272BCD	TEXAS	TS272BCD
TLC272BCP	TEXAS	TS272BCN
TLC272BID	TEXAS	TS272BID
TLC272BIP	TEXAS	TS272BIN
TLC272CD	TEXAS	TS272CD

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
TLC272CP	TEXAS	TS272CN
TLC272ID	TEXAS	TS272ID
TLC272IP	TEXAS	TS272IN
TLC274ACD	TEXAS	TS274ACD
TLC274ACN	TEXAS	TS274ACN
TLC274AID	TEXAS	TS274AID
TLC274AIP	TEXAS	TS274AIN
TLC274BCD	TEXAS	TS274BCD
TLC274BCN	TEXAS	TS274BCN
TLC274BID	TEXAS	TS274BID
TLC274BIP	TEXAS	TS274BIN
TLC274CD	TEXAS	TS274CD
TLC274CN	TEXAS	TS274CN
TLC274ID	TEXAS	TS274ID
TLC274IN	TEXAS	TS274IN
TLC27L2ACD	TEXAS	TS27L2ACD
TLC27L2ACP	TEXAS	TS27L2ACN
TLC27L2AID	TEXAS	TS27L2AID
TLC27L2AIP	TEXAS	TS27L2AIN
TLC27L2BCO	TEXAS	TS27L2BCD
TLC27L2BCP	TEXAS	TS27L2BCN
TLC27L2BID	TEXAS	TS27L2B1D
TLC27L2BIP	TEXAS	TS27L2BIN
TLC27L2CD	TEXAS	TS27L2CD
TLC27L2CP	TEXAS	TS27L2CN
TLC27L2D	TEXAS	TS27L2ID
TLC27L2IP	TEXAS	TS27L2IN
TLC27L4ACD	TEXAS	TS27L4ACD
TLC27L4ACN	TEXAS	TS27L4ACN
TLC27L4AID	TEXAS	TS27L4AID
TLC27L4AIN	TEXAS	TS27L4AIN
TLC27L4BCD	TEXAS	TS27L4BCD
TLC27L4BCN	TEXAS	TS27L4BCN
TLC27L4BID	TEXAS	TS27L4BID
TLC27L4BIN	TEXAS	TS27L4BIN
TLC27L4CD	TEXAS	TS27L4CD
TLC27L4CN	TEXAS	TS27L4CN
TLC27L4ID	TEXAS	TS27L4ID
TLC27L4IN	TEXAS	TS27L4IN
TLC27M2ACD	TEXAS	TS27M2ACD
TLC27M2ACP	TEXAS	TS27M2ACN
TLC27M2AID	TEXAS	TS27M2AID
TLC27M2AIP	TEXAS	TS27M2AIN
TLC27M2BCD	TEXAS	TS27M2BCN
TLC27M2BCP	TEXAS	TS27M2BCN
TLC27M2BID	TEXAS	TS27M2BID
TLC27M2BIP	TEXAS	TS27M2BIN
TLC27M2CD	TEXAS	TS27M2CD
TLC27M2CP	TEXAS	TS27M2CN
TLC27M2ID	TEXAS	TS27M2ID
TLC27M2IP	TEXAS	TS27M2IN
TLC27M4ACD	TEXAS	TS27M4ACD
TLC27M4ACN	TEXAS	TS27M4ACN
TLC27M4AID	TEXAS	TS27M4AID
TLC27M4AIN	TEXAS	TS27M4AIN
TLC27M4BCD	TEXAS	TS27M4BCD
TLC27M4BCN	TEXAS	TS27M4BCN
TLC27M4BID	TEXAS	TS27M4BID
TLC27M4BIN	TEXAS	TS27M4BIN
TLC27M4CD	TEXAS	TS27M4CD
TLC27M4CN	TEXAS	TS27M4CN
TLC27M4ID	TEXAS	TS27M4ID
TLC27M4IN	TEXAS	TS27M4IN
TLC372CD	TEXAS	TS372CD
TLC372CP	TEXAS	TS372CN
TLC372ID	TEXAS	TS372ID
TLC372IP	TEXAS	TS372IN
TLC374CD	TEXAS	TS374CD
TLC374CN	TEXAS	TS374CD
TLC374ID	TEXAS	TS374ID
TLC374IN	TEXAS	TS374IN
uA723CJ	TEXAS	LM723CJ
uA723MJN	TEXAS	LM723J
UA741CD	TEXAS	UA741CD
UA741CJG	TEXAS	UA741CJ
UA741CP	TEXAS	UA741CN
UA741MJG	TEXAS	UA741J
UA748CD	TEXAS	UA748CD
UA748CJG	TEXAS	UA748CJ
UA748CP	TEXAS	UA748CN
UA748MJG	TEXAS	UA748J
uA7805CKC	TEXAS	L7805CV
uA7806CKC	TEXAS	L7806CV
uA7806CKC	TEXAS	L7806CV
uA7808CKC	TEXAS	L7808CV
uA7812CKC	TEXAS	L7812CV
uA7815CKC	TEXAS	L7815CV
uA7818CKC	TEXAS	L7818CV
uA7824CKC	TEXAS	L7824CV
uA78M05CKC	TEXAS	L78M05CV
uA78M06CKC	TEXAS	L78M06CV
uA78M08CKC	TEXAS	L78M08CV
uA78M12CKC	TEXAS	L78M12CV
uA78M15CKC	TEXAS	L78M15CV
uA78M24CKC	TEXAS	L78M24CV
uA7905CKC	TEXAS	L7905CV
uA7908CKC	TEXAS	L7908CV
uA7912CKC	TEXAS	L7912CV
uA7915CKC	TEXAS	L7915CV
uA7918CKC	TEXAS	L7918CV
uA7924CKC	TEXAS	L7924CV
uA7952CKC	TEXAS	L7952CV
	THOMSON	
LM317SP	THOMSON	LM317T
uA723CFP	THOMSON	LM723CD
uA78S05CK	THOMSON	L78S05CT
uA78S05CSP	THOMSON	L78S05CV
uA78S09CK	THOMSON	L78S09CT
uA78S09CSP	THOMSON	L78S09CV

INDUSTRY STANDARD	SOURCE	NEAREST SGS-THOMSON TYPE
uA78S12CK	THOMSON	L78S12CT
uA78S12CSP	THOMSON	L78S12CV
uA78S15CK	THOMSON	L78S15CT
uA78S15CSP	THOMSON	L78S15CV
uA723CDP	THOMSON	LM723CN
uA723CFP	THOMSON	LM723CD
uA723CH	THOMSON	LM723CH
uA723MDG	THOMSON	LM723J
uA723MH	THOMSON	LM723H
uA7805CK	THOMSON	L7805CT
uA7805CSP	THOMSON	L7805CV
uA7806CK	THOMSON	L7806CT
uA7806CSP	THOMSON	L7806CV
uA7812CK	THOMSON	L7812CT
uA7812CSP	THOMSON	L7812CV
uA7815CK	THOMSON	L7815CT
uA7815CSP	THOMSON	L7815CV
uA7818CK	THOMSON	L7818CT
uA7818CSP	THOMSON	L7818CV
uA7824CK	THOMSON	L7824CT
uA7824CSP	THOMSON	L7824CV
uA7905CK	THOMSON	L7905CT
uA7905CSP	THOMSON	L7905CV
uA7912CK	THOMSON	L7912CT
uA7912CSP	THOMSON	L7912CV
uA7915CK	THOMSON	L7915CT
uA7915CSP	THOMSON	L7915CV
	TOSHIBA	
TA7504P	TOSHIBA	UA741CN
TA75061P	TOSHIBA	TL061CN
TA75062F	TOSHIBA	TL062CD
TA75062P	TOSHIBA	TL064CN
TA75064F	TOSHIBA	TL064CD
TA75064P	TOSHIBA	TL064IN
TA75064P	TOSHIBA	TL064CN
TA7506P	TOSHIBA	LM301AN
TA75071F	TOSHIBA	TL071CD
TA75071P	TOSHIBA	TL071CN
TA75072F	TOSHIBA	TL072CD
TA75072P	TOSHIBA	TL072CN
TA75074F	TOSHIBA	TL074CD
TA75074P	TOSHIBA	TL074CN
TA75339F	TOSHIBA	LM290ID
TA75339P	TOSHIBA	LM2901N
TA75358CF	TOSHIBA	LM358D
TA75358CP	TOSHIBA	LM358N
TA75358F	TOSHIBA	LM2904D
TA75358P	TOSHIBA	LM2904N
TA75393F	TOSHIBA	LM2903D
TA7539P	TOSHIBA	LM2903N
TA7540P	TOSHIBA	UA776IN
TA75458F	TOSHIBA	MC1458D
TA75558F	TOSHIBA	MC4558CD
TA75558P	TOSHIBA	MC4558CN
TA7555F	TOSHIBA	NE565D
TA7555P	TOSHIBA	NE555N
TA75902F	TOSHIBA	LM2902D
TA75902P	TOSHIBA	LM2902N

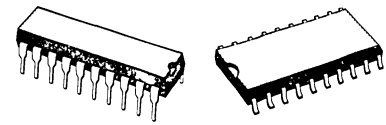
DATASHEETS

SGS-THOMSON MICROELECTRONICS

AM6012
AM6012A

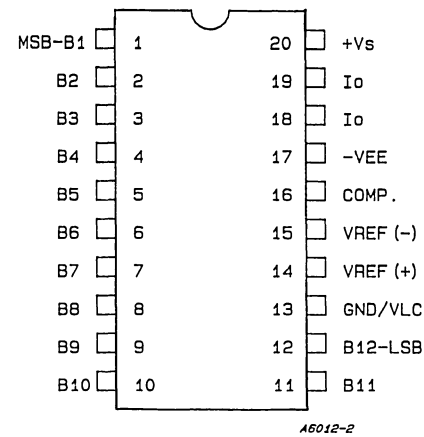
12-BIT HIGH SPEED D/A CONVERTERS

- ALL GRADES 12-BIT MONOTONIC OVER TEMPERATURE
- DIFFERENTAL NONLINEARITY TO ±0.012% (13 BITS) MAX OVER TEMPERATURE (A GRADES)
- 250ns TYPICAL SETTLING TIME
- FULL SCALE CURRENT 4mA
- HIGH SPEED MULTIPLYING CAPABILITY
- TTL/CMOS/ECL/HTL COMPATIBLE
- HIGH OUTPUT COMPLIANCE: −5V TO +10V
- COMPLEMENTARY CURRENT OUTPUTS
- LOW POWER CONSUMPTION: 230mW



DIP-20 Plastic (0.4) **SO-20L**

PIN CONNECTION



A6012-2

DESCRIPTION

The AM6012 is an industry standard monolithic 12-bit digital-to analog converter. Complementary current output and high speed multiplying capability make the AM6012 useful in a wide range of applications such as video displays, process control circuitry and fast A/D converters. The 6012 is the first D/A to achieve 12-bit differential linearity without the use of thin film resistors or active trimming. The 6012's unique circuit design insures monotonicity without the precision trimming associated with most other 12-bit DAC architectures. The AM6012 is packaged in a 20-pin plastic DIP and is SO-20L for surface mounting. Although tested and specified at ±15V, the AM6012 works well over a wide range of power supply voltages. Performance is essentially independent of supply voltage over the range of +5 volts, −12 volts to ±18 volts. The AM6012 series guarantees full 12-bit monotonicity for all grades and differential nonlinearity as high as 0.012% (13 bits) for the A grades and 0.025% (12 bits) for the standard grades over the entire temperature range.

Guaranteed monotonicity and low cost make the AM6012 an ideal choice for high volume applications requiring fine local resolution. Typical applications include printer graphics and video displays. These applications need a minimum of 12 bits of resolution, although conformance to an ideal straight line from zero to full scale is less important.

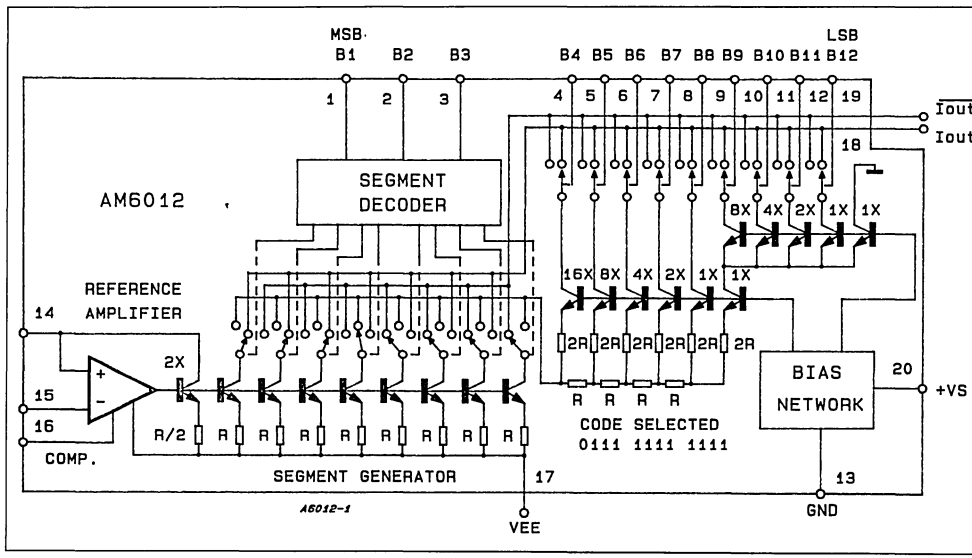
ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	0 to 70	°C
Storage Temperature	−65 to + 125	°C
Power Supply Voltage	±18	V
Logic Inputs	−5 to +18	V
Voltage at Current Outputs Pins	−8 to +12	V
Reference Inputs	$+V_S$ to $-V_{EE}$ ±18V max Differential	V
Reference Input Current	1.25	mA

CONNECTION DIAGRAM AND ORDERING INFORMATION

Type	Differential linearity (%)	Temperature Range (°C)	Package
AM6012PC	0.025	0 to 70	DIP.20
AM6012APC	0.012		
AM6012 D	0.025	0 to 70	SO.20L
AM6012 AD	0.012		

BLOCK DIAGRAM



THERMAL DATA

$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	100 °C/W

ELECTRICAL CHARACTERISTICS

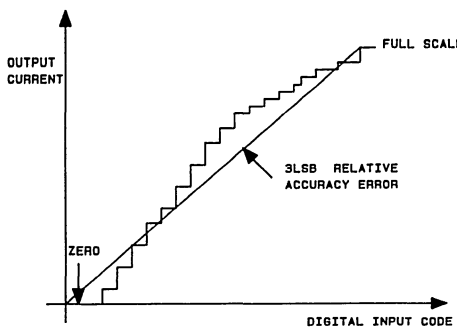
These specifications apply for $V_S = +15V$, $V_{EE} = -15V$, $I_{REF} = 1.0mA$, over the operating temperature range unless otherwise specified

Param.	Description	Test Conditions	AM6012A			AM6012			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
	Resolution		12	12	12	12	12	12	Bits
	Monotonicity		12	12	12	12	12	12	Bits
D.N.L.	Differential Nonlinearity	Deviation from ideal step size	—	—	±.012	—	—	±.025	%FS
			13	—	—	12	—	—	Bits
N.L.	Nonlinearity	Deviation from ideal straight line	—	—	±.05	—	—	±0.05	%FS
I_{FS}	Full Scale Current	$V_{REF} = 10.000V$ $R_{14} = R_{15} = 10.000k\Omega$ $T_A = 25°C$	3.967	3.999	4.031	3.935	3.999	4.063	mA
TCI_{FS}	Full Scale Temp.Co.		—	±5	±20	—	±10	±40	ppm°C
			—	±.0005	±.002		±.001	±.004	%FS°C
V_{OC}	Output Voltage Compliance	D.N.L. Specification guaranteed over compliance range $R_{OUT} > 10$ megohme typ.	−5	—	+10	−5	—	+10	V
I_{FSS}	Full Scale Symmetry	I_{FS}-I_{FS}	—	±0.2	±1.0	—	±0.4	±2.0	μA
I_{ZS}	Zero Scale Current		—	—	0.10	—	—	0.10	μA
I_S	Setting Time	To ±1/2 LSB, all bits ON or OFF, $T_A = 25°C$	—	250	500	—	250	500	nSec
t_{PLH} t_{PHL}	Propagation Delay - all bits	50% to 50%	—	25	50	—	25	50	nSec
C_{OUT}	Output Capacitance		—	20	—	—	20	—	pF
V_{IL}	Logic Input Levels — Logic "O"		—	—	0.8	—	—	0.8	V
V_{IH}	Logic Input Levels — Logic "1"		2.0	—	—	2.0	—	—	
I_{IN}	Logic Input Current	$V_{IN} = -5$ to $+18V$	—	—	40	—	—	40	μA
V_{IS}	Logic Input Swing	$V_{EE} = -15V$	−5	—	+18	−5	—	+18	V
I_{REF}	Reference Current Range		0.2	1.0	1.1	0.2	1.0	1.1	mA
I_{15}	Reference Bias Current		0	−0.5	−2.0	0	−0.5	−2.0	μA

ELECTRICAL CHARACTERISTICS (Continued)

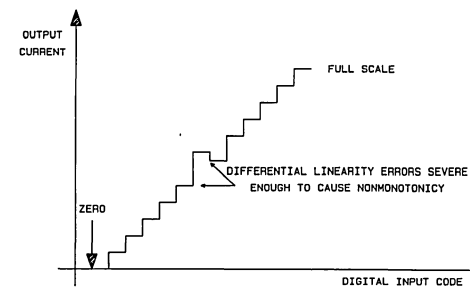
Param.	Description	Test Conditions	AM6012A			AM6012			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
di/dt	Reference Input Slew Rate	$R_{14(eq)} = 800\Omega$ CC = OpF	4.0	8.0	—	4.0	8.0	—	mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity	$V_S = (+13.5V$ to $+16.5V)$ $V_{EE} = -15V$	—	±.00005	±.001	—	±0.0005	±.001	%FS/%
$PSSI_{FS-}$		$V_{EE} = -13.5V$ to $-16.5V$ $V_S = +15V$	—	±.00025	±.001	—	±.00025	±.001	
V_S	Power Supply Range	$V_{OUT} = 0V$	4.5	—	18	4.5	—	18	V
V_{EE}			−18	—	−10.8	−18	—	−10.8	
I+	Power Supply Current	$V_S = +5V$, $V_{EE} = -15V$	—	5.7	8.5	—	5.7	8.5	mA
I−			—	−13.7	−18.0	−	−13.7	−18.0	
I+		$V_S = +15V$, $V_{EE} = -15V$		5.7	8.5	—	5.7	8.5	
I−			—	−13.7	−18.0	−	−13.7	−18.0	
P_D	Power Dissipation	$V_S = +5V$, $V_{EE} = -15V$	—	234	312	—	234	312	mW
		$V_S = +15V$, $V_{EE} = -15V$	—	291	397	—	291	397	

Fig. 1 - Relative Accuracy Error



A6012-10::DIS

Fig. 2 - Example of Nonmonotonic Behavior



A6012-10::LIB

APPLICATION INFORMATION

FUNCTIONAL DESCRIPTION

The segmented design of the AM6012, shown in the block diagram, insures that there are no significant differential nonlinearities in the transfer characteristic. The eight major carries of the most significant bits are not subject to the gross differential nonlinearities that can occasionally occur in an R-2R type DAC. This advantage is due to the fundamentally different way that the current is handled in an AM6012.

In a conventional R-2R type DAC, when the input code is increemented past a major carry, a current representing the new code is substituted for the sum of all the less significant bit currents that were previously on. To avoid any nonlinearities, the two total currents must be extremely well matched. In the case of the MSB major carry in a 12-bit DAC, the match must be better than one part in 2048 to maintain monotonicity. However, in the AM6012, a new current is never substituted for the sum of several smaller ones, but redirected through alternate channels and incremented one step at a time. For example, consider the MSB carry in an AM6012. In the initial state of 011111111111 as shown in the block diagram, the switches in the segment generator are set in such a way that currents I_0, I_1 and I_2 are steered directly into the noninverting output I_{OUT}. In addition, a portion of I_3 is directed through the 9-bit DAC that is controlled by the 9 least significant bits into I_{OUT}. With the 9LSBs set to "1", all of the I_3 current is directed to I_{OUT} except for the 1/512 that goes to ground through the right-most transistor in the 9-bit DAC. After the input word is changed to 100000000000, the segment decoder switch for I_3 will be all the way to the right, the switch for I_4 will be in the middle, and all the switches in the 9-bit DAC will be to the left. I_{OUT} will be composed of I_0, I_1, I_2 and I_3. None of I_4 will be directed into I_{OUT} until a higher code is reached. In other words, I_3 is now steered directly to I_{OUT} instead of being divided by a factor of 511/512 in the 9-bit DAC. Since no major current substitution occurs, there is less chance of a large nonlinearity at this transition than in a comparable R-2R DAC.

RELATIVE ACCURACY VS. DIFFERENTIAL NONLINEARITY

We defines relative accuracy as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn between the lowest code output voltage and the highest code output voltage) for any bit combination. Relative accuracy is often referred to as nonlinearity. The DAC transfer function shown in Figure 1 has a bow that results in a maximum relative accuracy error of 3LSB. This must be distinguished from a differential linearity error. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a ILSB change in digital input code.

For example, for a 4mA full scale output, a change of ILSB in digital input code should result in a 0.98μA change in the analog output current (ILSB = 4mA x 1/4096 = 0.98μA). If in actual use, however, a ILSB change in the input code results ina change of only 0.24μA (1/4LSB) in output current, the differential linearity error would be 0.74μA or 3/4LSB.

The AM6012 has very good differential linearity in spite of the porr relative accuracy. Conversely, the DAC of Figure 1 has very good relative accuracy but poor differential linearity. The anomaly in the middle of the transfer function is the result of a positive differential linearity error followed by a negative differential linearity error greater than 1LSB. A negative output step for an increase in digital input code is referred to as nonmonotonic behavior. In general, if a DAC has a differential linearity error specification greater than 1LSB, it may be nonmonotonic at one or more of the major carries. In most case the worst differential linearity error will occur at the MSB transition point.

As noted in the functional description, the 6012's unique design minimizes differential linearity errors at the transition points of the 3MSBs. This results in a tight specification on maximum differential nonlinearity over temperature. Differential linearity is verified on all AM6012s with 100% final testing. In many converter applications, uniform step size (or minimum differential linearity error) is more important than conformance to an ideal straight line. Twelve-bit onverters are usually needed for high resolution rather than high linearity as evidenced by the fact that few transducers are more linear than 0.1%. This is also true in video graphics, where the human eye has difficulty discerning nonlinearity of less than 5%. The AM6012 is especially well suited for these applications since it has inherently low differential linearity error.

APPLICATION INFORMATION (Continued)

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + I_{\overline{O}} = I_{FR}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 18 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 18 and turned on at pin 19. A decreasing logic count increase I_O as in a negative or inverter logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FR}; do not leave an unused output pin one.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 25V above V− and is independent of the positive supply. Negative compliance is +10V above V−.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The AM6012 operates over a wide range of power supply voltages from a total supply of 20V to 36V. When operating with V− supplies of −10V or less, $I_{REF} \leq 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range; consult the various figures fro guidance. For example, operation at −9V with $I_{REF} = 1mA$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the AM6012 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

TEMPERATURE PERFORMANCE

The nonlinearity and mononicity specifications of the AM6012 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is flight, typically ±10ppm/°C with zero scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full scale drift.

SETTLING TIME

The AM6012 is capable of extremely fast settling times, typically 250ns at $I_{REF} = 1.0mA$. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 25ns for each of the 12 bits. Settling time to within 1/2 LSB of the LSB is therefore 25ns, with each progressively larger bit taking successively longer. The MSB settles in 250ns, thus determining the overall settling time of 250ns. Settling to 10-bit accuracy requires about 90 to 130ms. The output capacitance of the AM6012 including the package is approximately 20pF; therefore, the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 0.5mA, with gradual increases for lower I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve $\pm 2\mu A$, therefore a 2.5kΩ load is needed to provide adequate drive for most oscilloscopes. At I_{REF} values of less than 0.5mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 011111111111 to 100000000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.1% of the final value, and thus settling times may be observed at lower values of I_{REF}.

AM6012 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be octained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference, and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.

APPLICATION INFORMATION (Continued)

REFERENCE AMPLIFIER SETUP

The AM6012 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{RF} = \frac{4095}{4096} \times 4 \times (I_{REF}) = 3.999\ I_{REF},$$

where $I_{REF} = I_{14}$

In positive reference applications, an external positive reference voltage forces current through R14 into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15. Reference current flows from ground through R14 into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R15 (nominally equal to R14) is used to cancel bias current errors. (Figure 3).
Bipolar references may be accommodated by offsetting V_{REF} or pin 15. The negative common-mode range of the reference amplifier is given by: $V_{CM}- = V-$ plus ($I_{REF} \times 3k\Omega$) plus 1.8V. The positive common-mode range is V+ less 1.23V.
When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R14 should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.
For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R14, or by using a potentiometer for R14.

MULTIPLYING OPERATION

The AM6012 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 1mA to 1μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 1.0mA.

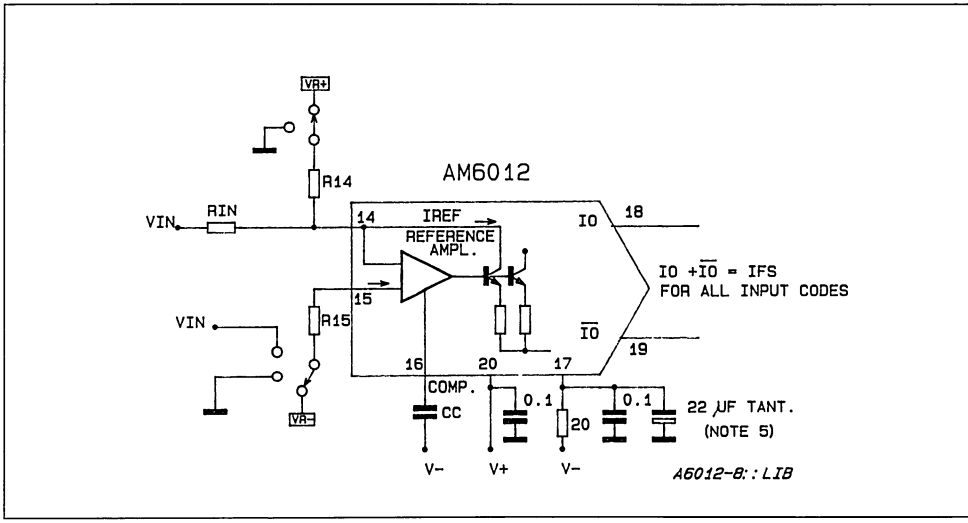
REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V−. The value of this capacitor depends on the impedance presented to pin 14. For R14 values of 1.0, 2.5 and 5 OkΩ; minimum values of C_C are 5, 12 and 25 pF. Larger values of R14 require proportionately increased values of C_C for proper phase margin (See Figure 4 and 5).
For fastest response to a pulse, low values of R14 enabling small C_C values should be used. If pin 14 is driven be a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall compensated which will decrease overall bandwidth and slew rate. For R14 = 1kΩ and C_C = 5pF, the reference amplifier slews at 4mA/ms enabling a transition from $I_{REF} = 0$ to I_{REF} = 1mA in 250ns.
Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff ($I_{REF} = 0$) condition. Full scale transition (0 to 1mA) occurs in 62.5ns when the equivalent impedance at pin 14 is 800Ω and $C_C = 0$. This yields a reference slew rate of 8mA/μs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The AM6012 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 40μA logic input current, and completely adjustable logic inputs may swing between −5 and +10V.
This enables direct interface with +15V CMOS logic, even when the AM6012 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 13, V_{LC}). For TTL interface, simply ground pin 13. When interfacing ECL, an $I_{REF} \leq$ 1mA is recommended. For interfacing other logic families, see block titled "Interfacing with Various Logic Families". For general setup of the logic control circuit, it should be noted that pin 13 will sink 1.1mA typical, external circuitry should be designed to accommodate this current (Figure 6).

Fig. 3 - Reference amplifier biasing



Reference Configuration	R_{14}	R_{15}	R_{IN}	C_C	I_{REF}
Positive Reference	V_{R+}	0V	N/C	.01µF	V_{R+}/R_{14}
Negative Reference	0V	V_{R-}	N/C	.01µF	$-V_{R-}/R_{14}$
Lo Impedance Bipolar Reference	V_{R+}	0V	V_{IN}	(Note 1)	$V_{R+}/R_{14}) + (V_{IN}/R_{IN})$ (Note 2)
Hi Impedance Bipolar Reference	V_{R+}	V_{IN}	N/C	(Note 1)	$(V_{R+} - V_{IN})/R_{14}$ (Note 3)
Pulsed Reference (Note 4)	V_{R+}	0V	V_{IN}	No Cap	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$

Notes:
1. The compensation capacitor a function of the impedance seen at the $+V_{REF}$ input and must be at least $5pF \times R_{14(eq)}$ in kΩ. For $R_{14} < 800\Omega$ no capacitor is necessary.
2. For negative values of V_{IN}, V_{R+}/R_{14} must be greater than $-V_{IN}$ Max/R_{IN} so that the amplifier is not turned off.
3. For positive values of V_{IN}, V_{R+} must be greater than V_{IN} Max so the amplifier is not turned off.
4. For pulsed operation, V_{R+} provides a DC offset and may be set to zero in some cases. The impedance at pin 14 should be 800Ω or less.
5. For optimum settling time, decouple V - with 20Ω and bypass with 22µF tantulum capacitor.
6. Reference current and reference resistor - there is a 1 to 4 schale factor between the reference current (I_{REF}) and the full scale output current (I_{FS}). If $V_{REF} = +10V$ and $I_{FS} = 4mA$, the value of the R_{14} is:

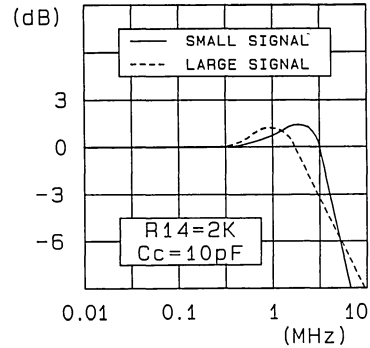
$$R_{14} = \frac{4 \times 10 \text{ Volt}}{4mA} = 10k\Omega \quad R_{14} = R_{15}$$

Fig. 4 - Minimum size compensation capacitor (I_{FS} = 4mA, I_{REF} = 1.0mA)

$R_{14(EQ)}$(KΩ)	C_C(pF)
›10	50
5	25
2	10
1	5
5	0

Note· A 0.01 μF capacitor is recommended for fixed reference operation.

Fig. 5 - Reference Amplifier Frequency response



A6012-11:: DI

Fig. 6 - Interfacing Circuits

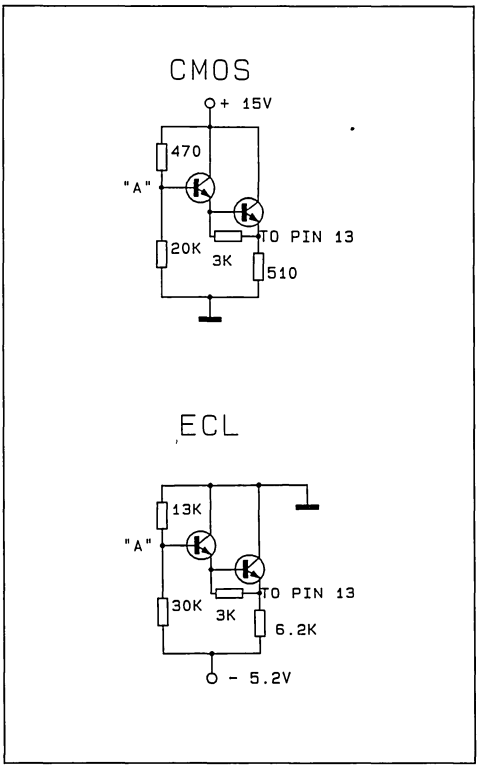


Fig. 7 - Accomodating Bipolar Reference

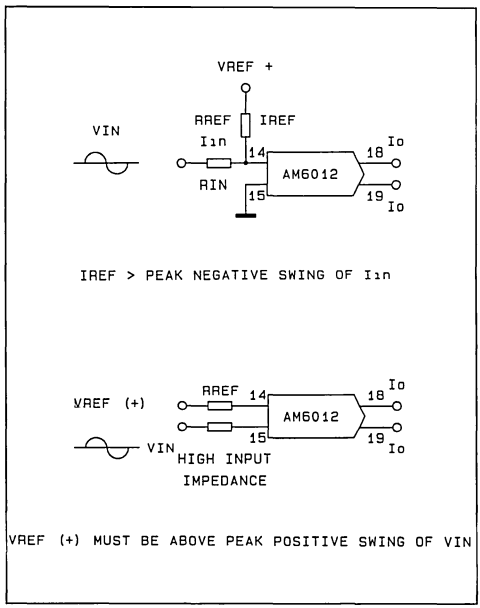
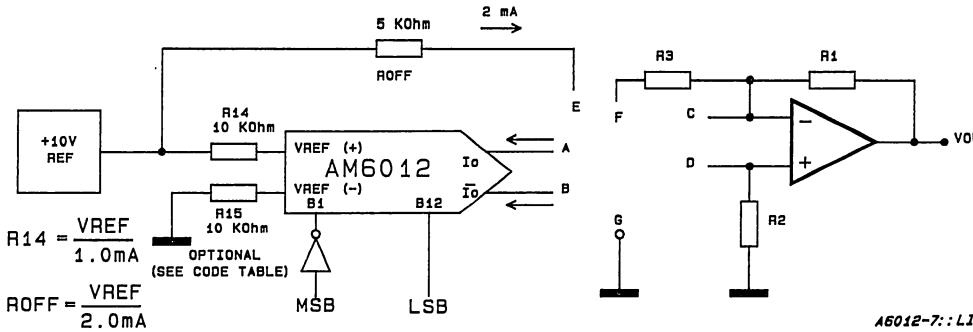


Fig. 8 - AM6012 Logic Inputs



Code Format		Connec.	Output Scale	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_0	$\overline{I_0}$	V_{OUT}
Unipolar	Straight bynary one polarity with true input code, true zero output.	a-c b-g R_1=R2=2 5K	Positive full scale Positive full scale-LSB Zero scale	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 0 0	3 999 3 998 000	000 001 3 999	9.9978 9 9951 0000
	Complementary binary one polarity with complementary input code, true zero output	a-g b-c R1=R2=2.5K	Positive full scale Positive full scale-LSB Zero scale	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 1 1	000 001 3 999	3 999 3 998 000	9 9976 9 9951 0000
Symmetrical Offset	Straight offset binary, offset half scale, sym-metrical about zero, no true zero output	a-c b-d f-0 R1=R3=2 5K R2=1 25K	Positive full scale Positive full scale-LSB (+) Zero scale (-) Zero scale Negative full scale-LSB Negative full scale	1 1 1 0 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 0 0 1 1 0	3 999 3 998 2 000 1 999 001 .000	000 001 1.999 2.000 3.998 3 999	9 9976 9 9927 0024 - 0024 -9 9927 -9.9976
	1's complement offset half scale symmetrical about zero, no true zero output MSB comple-mented (need inverter at B1)	a-c b-d f-g R1=R3=2.5K R2=1 25K	Positive full scale Positive full scale-LSB (+) Zero scale (-) Zero scale Negative full scale-LSB Negative full scale	0 0 0 1 1 1	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 0 0 1 1 0	3 999 3 998 2 000 1 999 .001 000	000 001 1 999 2 000 3 998 3.999	9 9976 9 9927 0024 -.0024 -9.9927 -9.9976
Offset with True Zero	Offset binary, offset half scale, true zero output	e-a-c b-g R1=R2=5K	Positive full scale Positive full scale-LSB +LSB Zero Scale -LSB Negative full scale+LSB Negative full scale	1 1 1 1 0 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 0 1 0 1 1 0	3.999 3.998 2.001 2 000 1 999 001 000	000 .001 1.998 1 999 2 000 3 998 3 999	9.9951 9.9902 .0049 000 - 0049 -9 9951 -10 000
	2's complement offset half scale true zero output MSB comple-mented (need inverter at B1)	e-a-c b-g R1=R2=5K	Positive full scale Positive full scale-LSB +1 LSB Zero scale -1 LSB Negative full scale+LSB Negative full scale	0 0 0 0 1 1 1	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 0 1 0 1 1 0	3.999 3.998 2 001 2.000 1 999 001 .000	.006 001 1 998 1 999 2 000 3 998 3 999	9.9951 9.9902 .0049 000 -0 049 -9 9951 -10 000

ADDITIONAL CODE MODIFICATIONS

1. Any of the offset binary codes may be complemented by reversing the output terminal pair.

Fig. 9 - Basic Negative Reference Operation

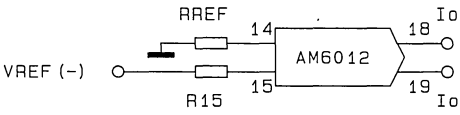


Fig. 10 - Recommended Full-scale Adjustment Circuit

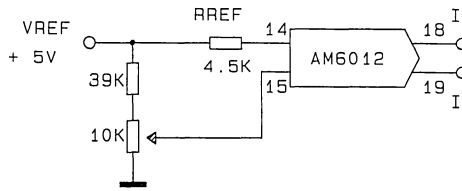


Fig. 11 - CRT Display Driver

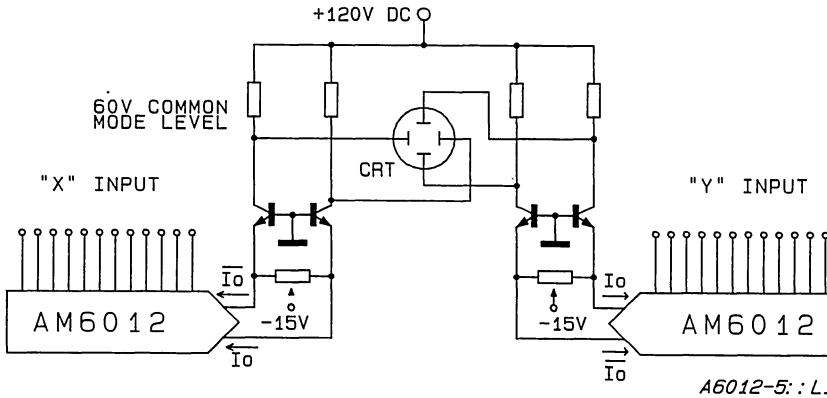


Fig. 12 - 12-BIT High-Speed A/D Converter

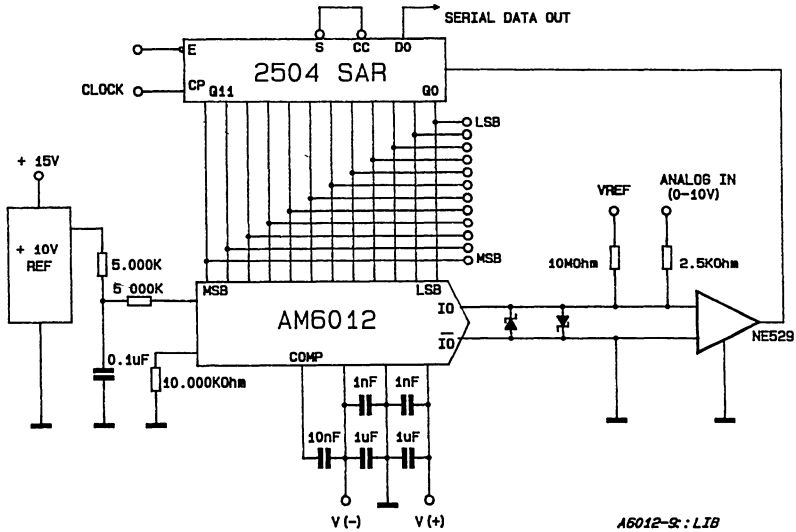


Fig. 13 - Interface with 8-bit Microprocessor Bus

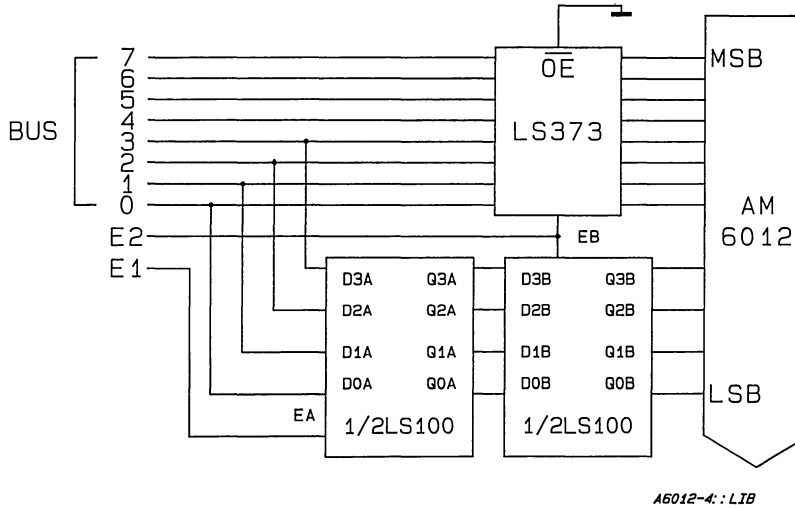
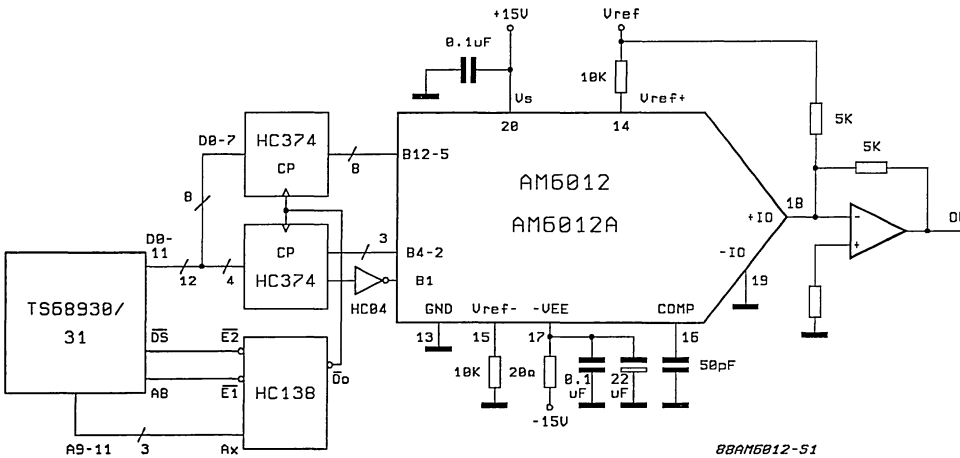
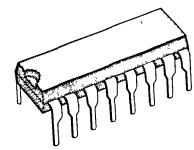


Fig. 14 - Interface with digital signal processor TS68930/31

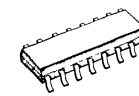


8-BIT D/A CONVERTERS

- RELATIVE ACCURACY: ±0.19% ERROR MAXIMUM (DAC0808)
- FULL SCALE CURRENT MATCH: ±1 LSB TYP
- 7 AND 6-BIT ACCURACY AVAILABLE (DAC0807, DAC0806)
- FAST SETTING TIME: 150 ns TYP
- NONINVERTING DIGITAL INPUTS ARE TTL AND CMOS COMPATIBLE
- HIGH SPEED MULTIPLYING INPUT SLEW RATE: 8 mA/μs
- POWER SUPPLY VOLTAGE RANGE: ±4.5V to ±18V
- LOW POWER CONSUMPTION: 33 mW @ ±5V

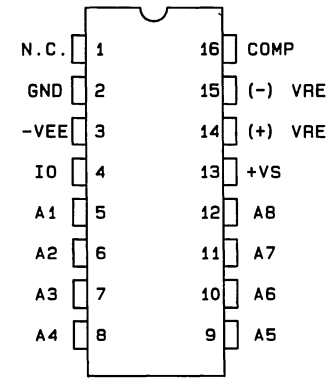


DIP-16 Plastic (0.25) and Ceramic



SO-16J

PIN CONNECTION



DAC0808-13

DESCRIPTION

The DAC0808 series is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 $I_{REF}/256$. Relative accuracies of better than 0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 series are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, or CMOS logic levels, and is a direct replacement for the MC1508/MC1408.

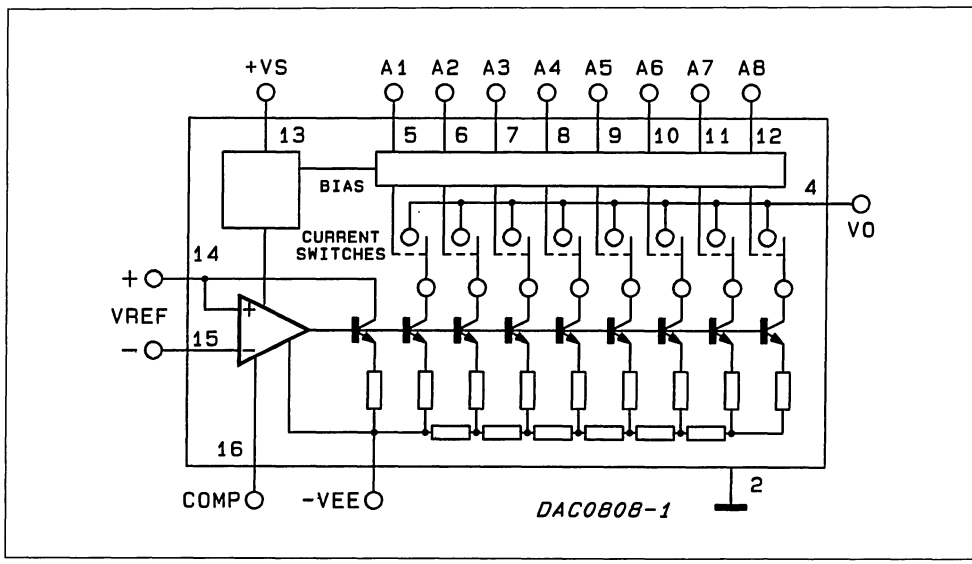
ABSOLUTE MAXIMUM RATINGS

Supply Voltage		
V_S	+18	V
V_{EE}	−18	V
Digital Input Voltage V5 − V12	−10 V to +18	V
Reference Current, I_{14}	5	mA
Reference Amplifier Inputs, V14, V15	V_{CC} , V_{EE}	
Operating Temperature Range		
DAC0808L	$-55°C \leq T_A \leq +125$	°C
DAC0808LC/D1	$0 \leq T_A \leq +75$	°C
Storage Temperature Range	−65°C to +150	°C

ORDERING INFORMATION

Accuracy	Temperature range	Plastic DIP-16	Ceramic DIP-16	SO-16
8 bit	0 to 75°C	DAC0808LCN	DAC0808LCJ	DAC0808D
7 bit	0 to 75°C	DAC0807LCN	DAC0807LCJ	DAC0807D
6 bit	0 to 75°C	DAC0806LCN	DAC0806LCJ	DAC0806D
8 bit	−55 to 125°C	—	DAC0808LJ	—

BLOCK DIAGRAM



THERMAL DATA

		Ceramic DIP-16	SO-16	Plastic DIP-16
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	150°C/W	120°C/W	100°C/W

ELECTRICAL CHARACTERISTICS

($V_S = 5V$, $V_{EE} = -15V$, $V_{REF}/R14 = 2$ mA, $T_A = T_{MIN}$ to T_{MAX} and all digital inputs at high logic level unless otherwise noted.)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
E_r	Relative Accuracy (Error Relative to Full Scale I_O)	*(Figure 10)*				%
	DAC0808L				±0.19	%
	DAC0807LC/D1 (Note 1)				±0.39	%
	DAC0806LC/D1 (Note 1)				±0.78	%
	Settling Time to Within 1/2 LSB (Includes t_{PLH})	$T_A = 25°C$ (Note 2) *(Figure 11)*		150		ns
t_{PLH} t_{PHL}	Propagation Delay Time	$T_A = 25°C$ *(Figure 11)*		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		ppm/°C
MSB	Digital Input Logic Levels	*(Figure 9)*				
V_{IH}	High Level, Logic "1"		2			V_{DC}
V_{IL}	Low Level, Logic "0"				0.8	V_{DC}
MSB	Digital Input Current	*(Figure 9)*				
	High Level	$V_{IH} = 5V$		0	0.040	mA
	Low Level	$V_{IL} = 0.8V$		−0.003	−0.8	mA
I_{15}	Reference Input Bias Current	*(Figure 3)*		−1	−3	μA
	Output Current Range	*(Figure 9)*				
		$V_{EE} = -5V$	0	2.0	2.1	mA
		$V_{EE} = -15V$, $T_A = 25°C$	0	2.0	4.2	mA
I_O	Output Current	$V_{REF} = 2.000V$. $R14 = 1000\Omega$				
		(Figure 9)	1.9	1.99	2.1	mA
	Output Current, All Bits Low	*(Figure 9)*		0	4	μA
	Output Voltage Compliance	$E_r \leq 0.19\%$, $T_A = 25°C$				
	$V_{EE} = -5V$				−0.55, +0.4	V
	V_{EE} Below −10V				−5.0 , +0.4	V
SRI_{REF}	Reference Current Siew Rate	*(Figure 14)*	4	8		mA/μs
	Output Current Power Supply Sensitivity	$-5V \leq V_{EE} \leq -16.5V$		0.05	2.7	μA/V
Power Supply Current (All Bits Low)		*(Figure 9)*				
I_S				2.3	22	mA
I_{EE}				−4.3	−13	
Power Supply Voltage Range		$T_A = 25°C$ *(Figure 9)*				
V_S			4.5	5.0	5.5	V
V_{EE}			−4.5	−15	−16.5	
	Power Dissipation					
	All Bits Low	$V_S = 5V. V_{EE} = -5V$		33	170	mW
		$V_S = 5V. V_{EE} = -15V$		106	305	mW
	All Bits High	$V_S = 15V. V_{EE} = -5V$		90		mW
		$V_S = 15V. V_{EE} = -15V$		160		mW

Note 1: All current switches are tested to guarantee at least 50% of rated current.
Note 2: All bits switched.
Note 3: Range control is not required.

Fig. 1 - Supply Current vs Temperature

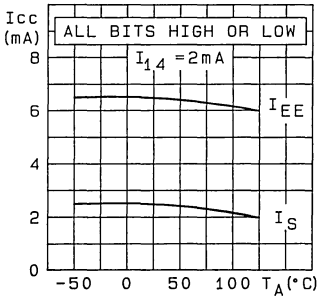


Fig. 2 - Supply Current vs Supply Voltage (V_{EE})

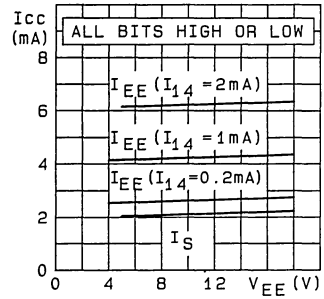


Fig. 3 - Supply Current vs Supply Voltage (V_S)

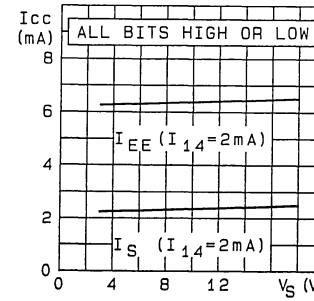


Fig. 4 - Logic Input Current vs Input Voltage

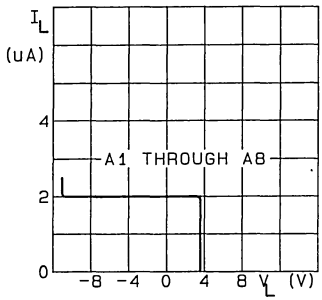


Fig. 5 - Bit Transfer Characteristics

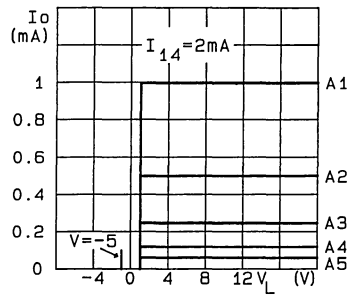


Fig. 6 - Output Voltage Compliance

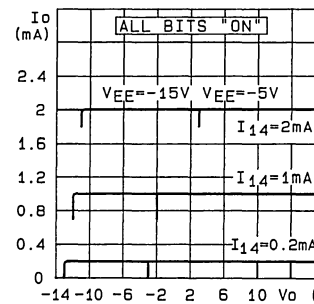


Fig. 7 - Output Voltage Compliance vs Temperature

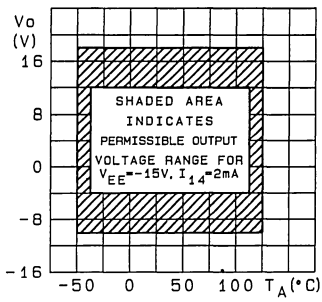
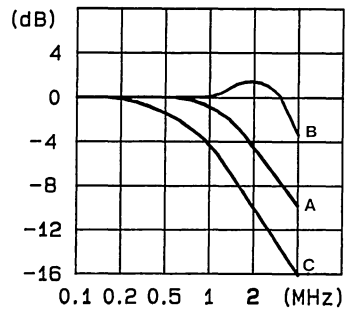


Fig. 8 - Frequency response



Unless otherwise specified: R14 = R15 = 1 kΩ, C = 15 pF, pin 16 to V_{EE}; R_L = 50Ω, pin 4 to ground.

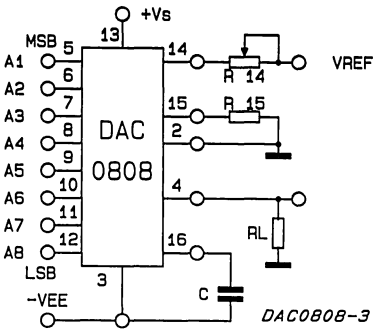
Curve A: Large Signal Bandwidth Method of *Figure 7*, V_{REF} = 2 Vp-p offset 1 V above ground

Curve B: Small Signal Bandwidth Method of *Figure 7*, R_L = 250Ω, V_{REF} = 50 mVp-p offset 200 mV above ground.

Curve C: Large and Small Signal Bandwidth Method of *Figure 9* (no op amp. R_L = 50Ω), R_S = 50Ω, V_{REF} = 2V, V_S = 100 mVp-p centered at 0V.

Test Circuits

FIGURE 9. Notation Definitions



The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$Io = K\left(\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right)$$

where $K \cong \frac{V_{REF}}{R14}$

and A_N = "1" if A_N is at high level
A_N = "0" if A_N is at low level

FIGURE 10. Relative Accuracy

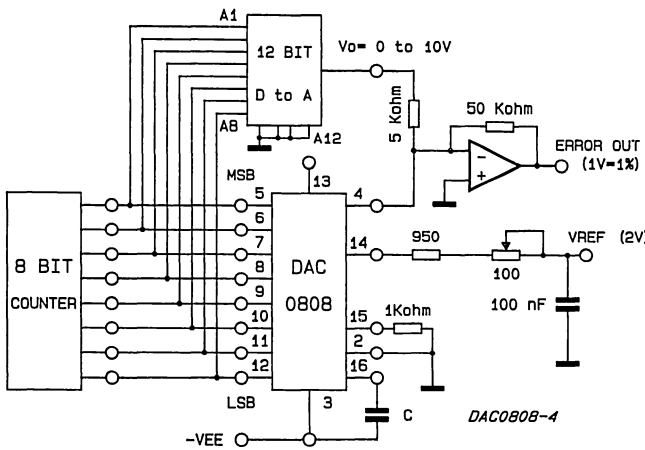
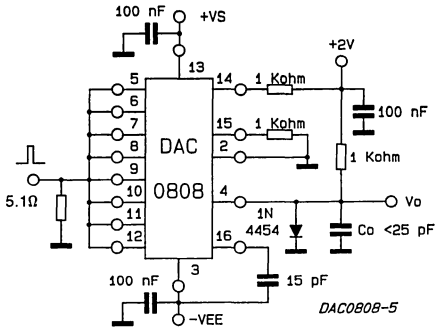


FIGURE 11. Transient Response and Settling Time



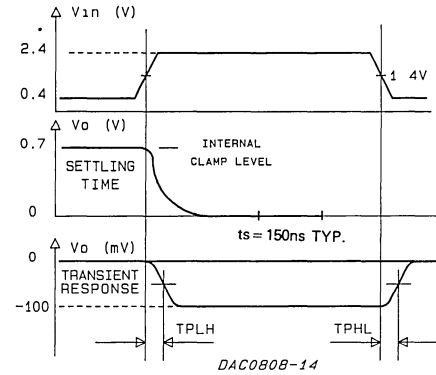


FIGURE 12. Positive V_{REF}

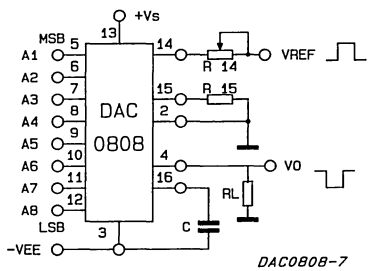


FIGURE 13. Negative V_{REF}

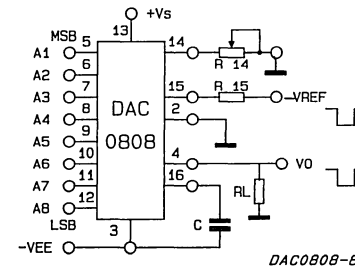
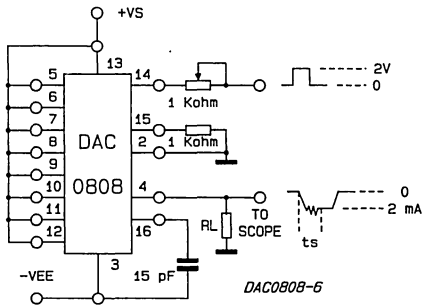


FIGURE 14. Reference Current Slew Rate Measurement



APPLICATION INFORMATION

CIRCUIT DESCRIPTION

The DAC0808 consists of a reference current amplifier, an R-2R ladder, and eight high-speed current switches. For many applications, only a reference resistor and reference voltage need be added.

The switches are noninverting in operation, therefore a high state on the input turns on the specified output current component. The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches. Nota that there is always a remainder current which is equal to the last significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992 mA for a 2.0 mA reference amplifier current if the NPN current source pair is perfectly matched.

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I_{14}, must always flow into pin 14, regardless of the set-up method or reference voltage polarity.

Connections for a positive voltage are shown in *Figure 12*. The reference voltage source supplies the full current I_{14}. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1, 2.5 and 5 kΩ, minimum capacitor values are 15,37 and 75 pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in *Figure 13*. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 3V above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a DC reference voltage is used, capacitive by pass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to 5V through another resistor and bypassing the junction of the 2 resistors with 0.1 μF to ground. For reference voltages greater than 5V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on pin 4 is restricted to a range of −0.6 to 0.5V when V_{EE} = −5V due to the current switching methods employed in the DAC0808.

The negative output voltage compliance of the DAC0808 is extended to −5V where the negative supply voltage is more negative than −10V. Using a full-scale current of 1.992 mA and load resistor of 2.5 kΩ between pin 4 and ground will yield a voltage output of 256 levels between 0 and −4.980V. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500Ω do not significantly affect performance, but a 2.5 kΩ load increases worst-case setting time to 1.2 μs (when all bits are switched ON). Refer to the subsequent text section on Settling Time for more details output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2 mA may be used only for negative supply voltages more negative than −7V, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current. The relative accuracy of the DAC0808 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC0808 has a very low full-scale current drift with temperature.

The DAC0808 series is guaranteed accurate to within ±1/2 LSB at a full-scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2 mA, with the loss of 1 LSB (8 μA) which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mis-match in the NPN current source pair. The accuracy test circuit is shown in *Figure 10*. The 12-bit converter is calibrated for a full-scale output current of 1.992 mA. This is an optional step since the DAC0808 accuracy is essentially the same between 1.5 and 2.5 mA.

Then the DAC0808 circuits' full-scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accuracy D-to-A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65,536, or ±0.00076%, which is much more accurate than the ±0.019% specification provided by the DAC0808.

MULTIPLYING ACCURACY

The DAC0808 may be used in the multiplying mode with 8-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16 μA to 4 mA, the additional error contributions are less than 1.6 μA. This is well within 8-bit accuracy when referred to full-scale.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the DAC0808 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a DC reference current is 0.5 to 4 mA.

SETTLING TIME

The "worst case" switching condition occurs when all bits are switched "on", which corresponds to a low-high transition for all bits. This time is typically 150 ns for settling to within ±1/2 LSB for 8-bit accuracy and 100 ns to 1/2 LSB for 7 and 6-bit accuracy. The turn off is typically under 100 ns. These timers apply when $R_L \leqslant 500$ ohms and $C_0 \leqslant 25$ pF.

The test circuit of Figure 11 requires a smaller voltage swing for the current switches due to internal voltage clamping in the DAC0808 A 1.0-kilohm load resistor from pin 4 to ground gives a typical settling time of 200 ns.
Thus, it is voltage swing and not the output RC time constant that determines setting time for most applications.
Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time.
Short leads, 100 μF supply bypassing for low frequencies, and minimum scope lead length are all mondatory.

PROGRAMMABLE GAIN AMPLIFIER OR DIGITAL ATTEPUATOR

When used in the multiplying mode can be applied as a digital attenuator. See Figure 15. One advantage of this technique is that if $R_S = 50$ ohms, no compensation capacitor is needed. The small and large signal band are now identical and are shown in Figure 8C.

The best frequency response is obtained by not allowing I_{14} to reach zero. However, the high impedance node, pin 16, is clamped to prevent saturation and insure fast recovery when the current through R14 goes to zero. R_S can be set for a ± 1.0 mA variation in relation to I_{14}. I_{14} can never be negative.
The output current is always unipolar. The quiescent dc output current level changes with the digital word which makes accoupling necessary.

CURRENT TO VOLTAGE CONVERSION

Voltage output of a larger magnitude are obtainable with the circuit of fig. 16 which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the DAC0808 ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and setting time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases over compensation may be desirable.
Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input. The LM301 can be used in a feedforwerd mode resulting in a full scale setting time on the order of 2.0 μs.

COMBINED OUTPUT AMPLIFIER AND VOLTAGE REFERENCE

For many of its applications the DAC0808 requires a reference voltage and an operational amplifier. Normally the operational amplifier is used as a current to voltage converter and its output need only go positive. With the popular LM723 voltage regulator both of these functions are provided in a single package with the added bonus of up to 150 mA output current. See Figure 17. The reference voltage is developed with respect to the negative voltage and appears as a common-mode signal to the reference amplifier in the D-to-A converter. This allows use of its amplifier as a classic current-to-voltage converter with the non-inverting input grounded.
Since ± 15V and $+5.0$V are normally available in a combination digital-to-analog system, only the -5.0 V need be developed. A resistor divider is sufficiently accurate since the allowable range on pin 5 is from -2.0 to -8.0 volts. The 5.0 kilohm pulldown resistor on the amplifier output is necessary for fast negative transitions.
Full scale output may be increasing R_O and raising the $+15$V supply voltage to 35 V maximum. The resistor divider should be altered to comply with the maximum limit of 40 volts across the LM723 C_O may be decreased to maintain the same R_O-C_O product if maximum speed is desired.

PROGRAMMABLE POWER SUPPLY

The circuit of figure 17 can be used as a digitally programmed power supply by the addition of thumb-wheel switches and a BCD-to-binary converter. The output voltage can be scaled in several ways, including 0 to $+25.5$ volts in 0.1 $-$volt increments, ± 10 mV.

PANEL METER READOUT

The DAC0808 can be used to read out the status of BCD or binary registers or counters a digital control system. The current output can be used to drive directly an analog panel meter. External meter shunts may be necessary if a meter of less than 20 mA full scale is used. Full scale calibration can be done by adjusting R14 or V_{ref} (see fig. 18).

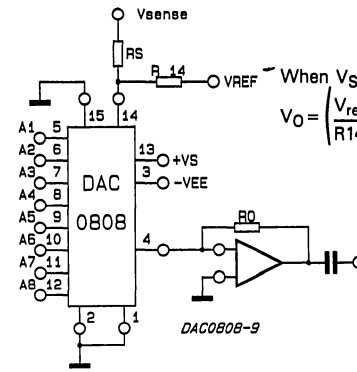
CHARACTER GENERATOR

In a character generation system fig. 19 one DAC0808 circuit uses a fixed reference voltage and its digital input defines the starting point for a stroke. The second converter circuit has a ramp input for the reference and its digital input defines the slope of the stroke. Note that this approach does not result in a 16-bit D-to-A converter (see Accuracy Section).

TWO-DIGIT BCD CONVERSION

Two 8-bit, D-to-A converters can be used to build a two digit BCD D-to-A or A-to-D converter (fig. 21). If both outputs feed the virtual ground of an operational amplifier, 10:1 current scaling can be achieved with a resistive current divider. If current output is desired, the units may be operated at full scale current levels of 4.0 mA and 0.4 mA with the outputs connected to sum the currents. The error of the D-to-A converter handling the least significant bits will be scaled down by a factor of ten and thus an DAC0806 may be used for the least significant word.

FIGURE 15. Programmable Gain Amplifier or Digital Attenuator Circuit



$$V_O = 10V \left(\frac{A1}{2} + \frac{A2}{4} + \cdots \frac{A8}{256} \right)$$

FIGURE 16.

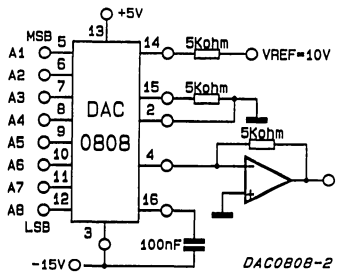


FIGURE 17. Combined output amplifier and voltage reference circuit

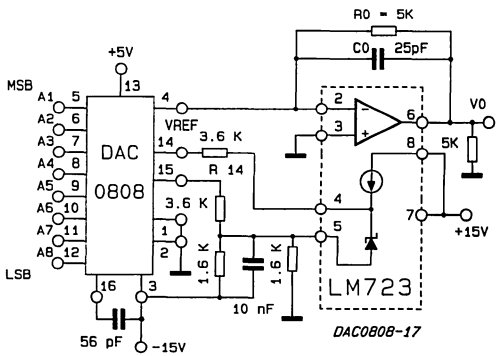
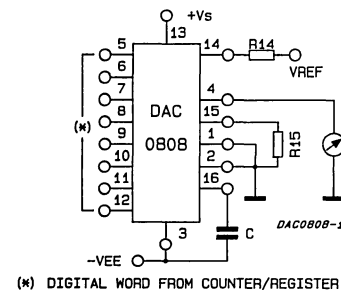
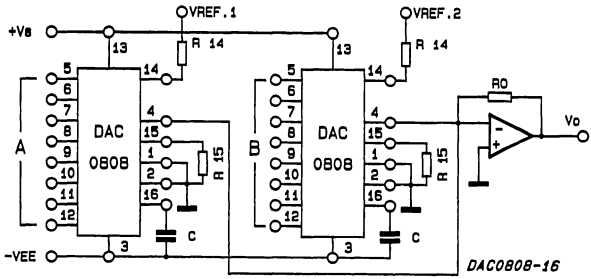


FIGURE 18. Panel meter readout circuit



(*) DIGITAL WORD FROM COUNTER/REGISTER

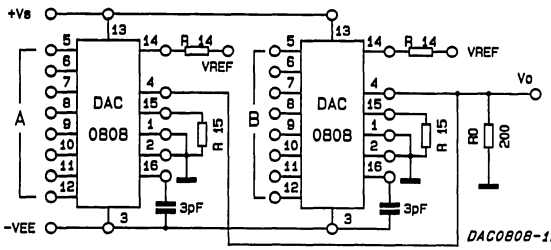
FIGURE 19. Digital summing and character generation



$$V_O = (I_{O1} + I_{O2})\, R_O$$

$$V_O = \left[\frac{V_{ref1}}{R14_1}\{A\} + \frac{V_{ref2}}{R14_2}\{B\}\right] R_O$$

FIGURE 20. Analog product of two digital words (High Speed Operation)



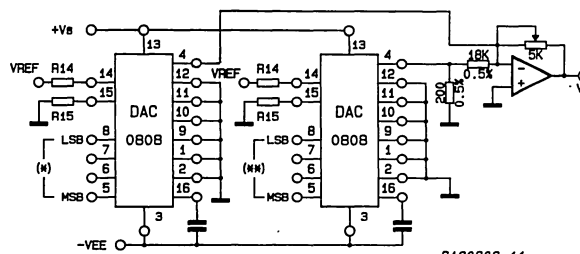
$$V_O = -I_{O1}\, R_O = \frac{V_{ref}}{R14_1}\{A\}\, R_O$$

$$I_{O2} = \frac{\{B\}\,|V_O|}{R14_2} = \frac{\{B\}}{R14_2}\left[R_O\left(\frac{V_{ref}}{R14_1}\right)\{A\}\right]$$

Since $R_O = R14_2$ and $K = \dfrac{V_{ref}}{R14_1}$

$$I_{O2} = K\{A\}\{B\}$$ K can be an analog variable

FIGURE 21. Two-digit BCD conversion



(*) MOST SIGNIFICANT BCD WORD
(**) LEAST SIGNIFICANT BCD WORD

SGS-THOMSON MICROELECTRONICS

TSFJ SERIES

MIXED ANALOG - DIGITAL BIPOLAR ARRAYS

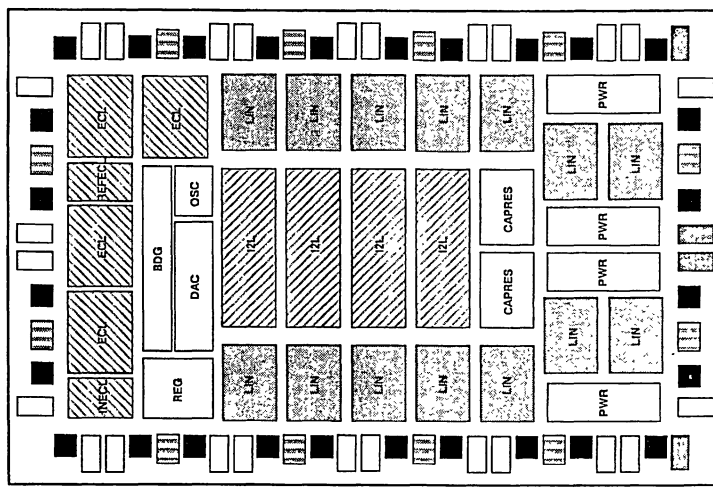
- ADVANCED BIPOLAR TECHNOLOGY :
  - NPN, F_T = 3GHz
  - 2 METAL LAYER
  - 100MHz, ECL FUNCTIONS
- FULL ESD PROTECTION
- POWER SUPPLY :
  MAXIMUM RATINGS = UP TO 15V
  OPERATING CONDITIONS = 3 TO 12V
- ANALOG - DIGITAL ARRAYS :
  - ANALOG TILES
  - ECL TILE FOR HIGH SPEED LOGIC
  - I2L CORE FOR LOW FREQUENCY RANDOM LOGIC
  - POWER TILE WITH 200mA CAPABILITY
- 5 ARRAYS AVAILABLE :
  J4, J6, J9, J13, J23 FROM 600 TO 3000 COMPONENTS
- CAD SOFTWARE SUPPORT :
  - ADS-PC (analog design system - PC)
  - FULLY INTEGRATED IN PC ENVIRONMENT
  - P-CAD* SOFTWARE, FOR SCHEMATIC CAPTURE, SIMULATION, AND LAYOUT
- OPERATING TEMPERATURE RANGE :
  COMMERCIAL : 0 TO 70C
  INDUSTRIAL : - 40 TO + 85C
  MILITARY : - 55 TO + 125C
- PACKAGE OPTIONS
  DIL : PLASTIC OR CERAMIC
  SMD : SO, PLCC, LCCC, QFP

USIC PRODUCTS DESCRIPTION

SGS-THOMSON Microelectronics introduces the mixed analog-digital arrays developped on a 3GHz process. Using the expertise in bipolar arrays, SGS-THOMSON has developped this new series to offer a product taking the leading edge of any technology :

- High speed process (NPN, F_T = 3GHz)
- Architecture with tile concept to improve the efficiency of the placement and routing
- 2 customized metal layers with 4 masks to personalize (contact, M1, via, M2)
- Complete CAD system on a PC from schematic capture up to the layout.

Figure 1 : Example of TSFJ13 architecture.



TSFJ ARCHITECTURE

TECHNOLOGY

TSFJ series developped by SGS-THOMSON is using an advanced bipolar process with high frequency performance (NPN, F_t = 3GHz). With a double metal layer the parasitic elements are minimized to improve the layout density and to increase the performances.

The process is very well suited for accurate analog bipolar design. The other key feature is introduced with the digital capability using either ECL functions or I2L ones.

Thanks to protection network placed on each input pad, the complete TSFJ series is protected against ESD parasitic effects.

TILE ARCHITECTURE

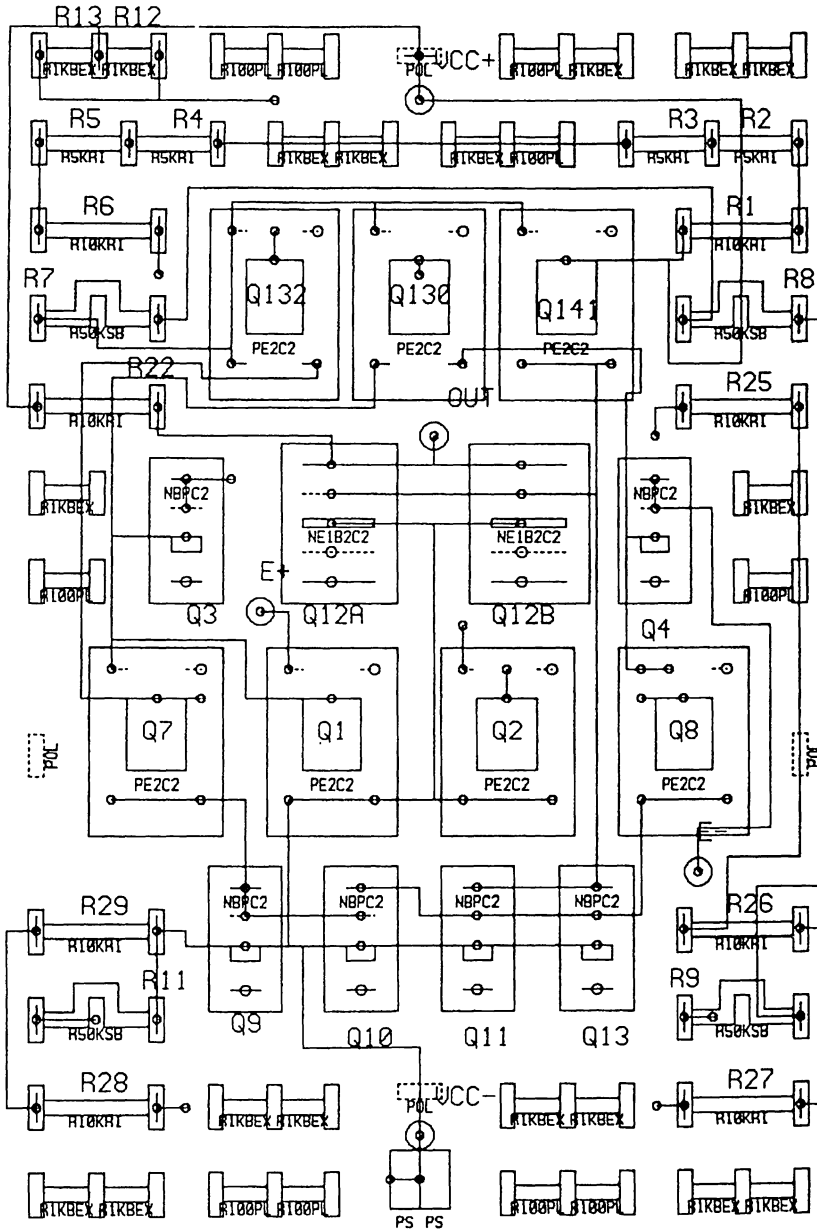
The TSFJ series has an architecture based on a tile concept in order to take advantage of efficient layout.

For SGS-THOMSON a tile is an optimized placement of basic components such as transistors, resistors, and capacitors, with no routing done in advance. When customisation is prepared, the designer optimized the routing of each tile according to his needs.

6 different types of tiles have been developped :

- LINEAR TILE, optimized for analog functions (op amps, comparators, ...)
  - 6 standard NPN (h_{FE} = 105, and I_c = 100A)
  - 2 low noise NPN
  - 7 lateral PNP (h_{FE} = 52, and I_c = 1A)
  - 44 resistances from 100 ohms to 50KΩ
- POWER TILE, optimized for power interface capability ;
  - 4 standard substrate PNP
  - 1 power substrate PNP (I_{KF} = 10mA)
  - 1 power NPN (I_{KF} = 314mA)
  - 1 medium power NPN (I_{KF} = 78mA)
  - 3 std NPN
- I2L LOGIC TILE, optimized to implement random logic using standard I2L functions (NAND, AND, NOR, OR, Flip-flop, ...)
  - row of I2L operators
- ECL LOGIC TILE, optimized for high speed logic up to 100MHz
  - equivalent to 1 D flip-flop or 5 NOR gates
- BUILT-IN FUNCTION TILES, a certain number of predefined tile have been created to fulfill some specific analog requests such as ;
  - 1 bandgap voltage reference
  - 1 oscillator (RC or quartz)
  - 1 voltage regulator
  - 1 R-2R resistor ladder for 6 bits DAC
- RESISTOR/CAPACITOR TILE, optimized for RC network or compensation capacitor purpose
  - 2.5pF and 7pF capacitor available

igure 2 : Example of a symbolic Linear Tile.



LINEAR TILE AFTER CMP139X LAYOUT E89TSFJ-02

Figure 3 : TSFJ Series : The Available Tiles.

Tiles	Nb Components	J04	J06	J09	J13	J23
ECL	86			4	4	5
I2L	9	6	15	18	36	54
HF	46			1	1	1
CAPRES	24			2	2	
REFECL	31			1	1	1
DAC	33			1	1	
R2R	46					1
LIN	59	6	8	10	14	24
RES	21	1	1			4
PWR	34	1	2	2	2	4
PWR1	34	1	2	2	2	4
BANDGAP	37	1	1	1	1	1
OSCIL	23	1	1	1	1	1
PROTECA	2	7	8	11	13	18
PROTECB	2	7	7	11	13	18
CAP1	1	4	6	8	8	10
CAP2	2	2	4	2	4	9
CAPAS	3		1			
DIODES	2	2	4	4	4	8
PUISS	3	1				
ALIM	40		1	1	1	2
	TOTAL :	600	919	1554	1964	3067

E88TSFJ-03

Figure 4 : TSFJ Series : The Transistors.

Components	J04	J06	J09	J13	J23
NPN 5mA	54	79	201	225	331
NPN 16mA	14	18	24	32	52
NPN 50mA	2	4	4	4	8
NPN 100mA	2	2	2	2	4
NPN 200mA	2	4	4	4	8
LATERAL PNP 60µA	50	68	83	111	184
SUBSTRATE PNP	8	16	16	16	32
SUBSTRATE PNP 10mA	2	4	4	4	8

E88TSFJ-04

Figure 5 : TSFJ Series : The Resistors.
(high values)

Components	J04	J06	J09	J13	J23
3KΩ RI	0	0	10	10	10
5KΩ RI	36	56	64	80	136
8KΩ RI	0	0	18	18	18
10KΩ RI	64	80	96	128	202
40KΩ RI	0	2	2	2	2
50KΩ RI	0	4	4	4	4
50KΩ SB	24	32	40	56	88
100KΩ SB	4	4	12	12	20

(medium and low values)

Components	J04	J06	J09	J13	J23
30Ω PL	9	17	17	17	33
100Ω PL	60	80	116	156	260
200Ω PL	0	0	16	16	20
300Ω PL	0	0	9	9	8
1KΩ BEX	130	182	398	470	720

E88TSFJ-05

ADS-PC : ANALOG DESIGN SYSTEM - PC

The TSFJ series is fully supported by a complete Computer Aided Design (CAD) system. The ADS-PC tool offers capabilities of schematic entry, analog and digital simulation and symbolic layout, using a standard software package from PCAD.
The ADS-PC software requires a low cost IBM PC AT3 or fully compatible with the following configuration :
- 640 KO RAM, coprocessor 80287
optional : 80386 and 80387 accelerator boards
2MB EMS board
- microsoft parallel mouse
- EGA graphic monitor
- 30 MO hard disk
- laser jet printer
Checkings and mask generation are implemented on DEC™ VAX™ computer systems.

SCHEMATIC GRAPHIC CAPTURE

PC-CAPS™ software, from P-CAD™, provides capture of schematic circuit diagram, allowing the circuit description in a hierarchical way* and using either macrocell from ST library or basic array components.
A database is generated (netlist extraction) for simulation and symbolic layout.

* (symbols can be created to represent schematic designs and can be used as components in higher-level schematic designs)

ANALOG SIMULATION

The analog simulation is performed using PSPICE™* software and the models library for basic components and macrocells. The result analysis is performed using graphic representation on listing edition.

* from MICROSIM

PSPICE input files are the net list from schematic capture, command file, configuration file and simulation environment (active device level description, technology worst cases...).

DIGITAL SIMULATION

PC-LOGS™, from P-CAD™, is a logic simulation program providing primitive symbols library and using commands interactively or in batch mode to set up and perform a simulation.

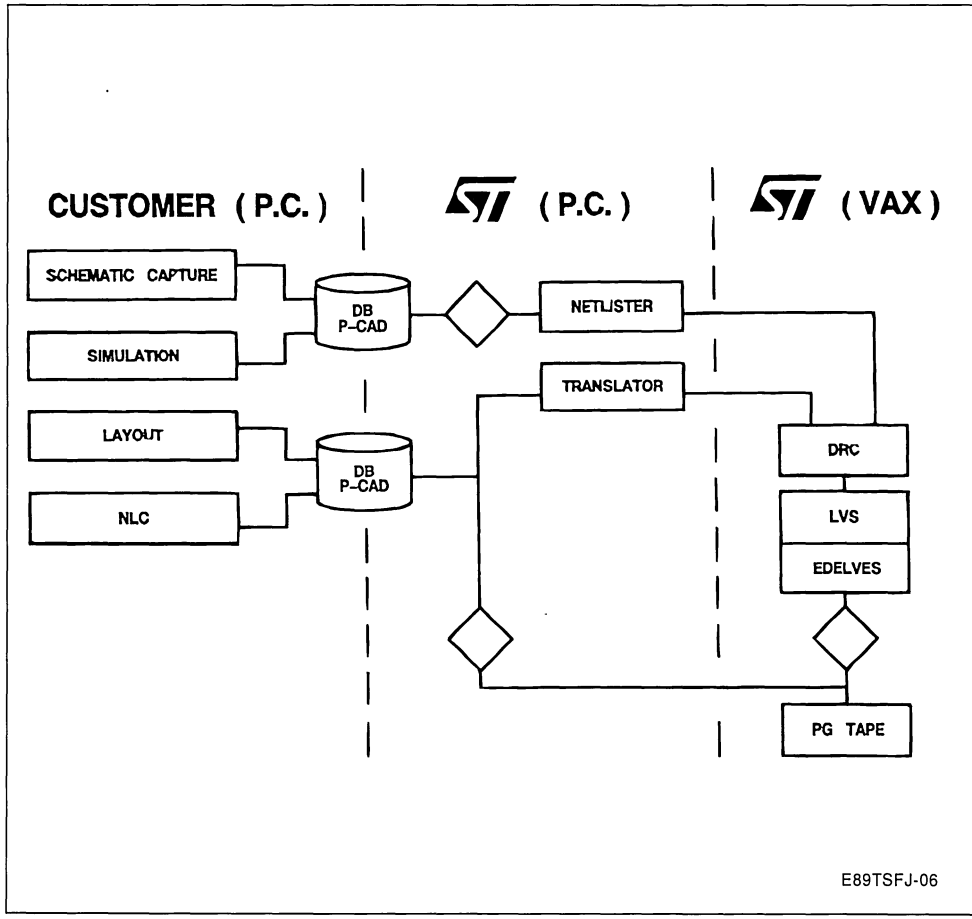
Simulation results can be displaid to the screen in graphic or tabular forms. PC-LOGS inputs are of two types : a verified netlist and user commands.

PLACEMENT AND ROUTING

PC-CARDS™, from P-CAD™, is built around an intelligent database that continually keeps track of components and connectivities.

The on-screen menu includes commands to draw, edit, move, delete, zoom in and out, view selected window.

Figure 6 : ADS - PC Design Flow.



CUSTOMER DESIGN INTERFACE

SGS-THOMSON has developped several interfaces for customers, giving them easy and flexible design approaches for TSFJ mixed analog/ digital bipolar arrays.

User can access ADS-PC system ;
- via the SGS-THOMSON Design centers
- via CAE workstations using a PC configuration and the P-CAD™ software package

According to all of these design possibilities, SGS-THOMSON defined 2 main customer interfaces. Next figure outlines these interfaces. Each interface delimits the responsabilities of customer and SGS-THOMSON during circuit development flow.

	Interface 2	Interface 3
Definition of Circuit Specifications	Customer	Customer
Electrical Description (analog + digital)	Customer	Customer
Test Procedure	Customer	Customer
Graphic Capture + Input Signal Entry	ST	Customer
Design Verification	ST	Customer
Simulation (analog + digital)	ST	Customer
Approval	Customer	Customer/ST
Place and Route	ST	Customer
Final Design Release	Customer	Customer/ST
Test Program Generation + Test Tooling	ST	ST
Mask Tooling	ST	ST
Prototype Manufacturing	ST	ST
Prototype Delivery	ST	ST

With interface 3, design can be done either at SGS-THOMSON Microelectronics design center facilities or at customer location.

ABSOLUTE MAXIMUM RATINGS (note 1) T_{amb} = 25°C, Voltage Referenced to V-

Symbol	Parameter	Value		Unit
		Min.	Max.	
V+	Supply Voltage	– 0.5	+ 15	V
T_{stg}	Storage Temperature (ceramic)	– 60	+ 150	°C
	Storage Temperature (plastic)	– 40	+ 125	°C

Note : 1. Stresses above those listed order "maximum rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these on any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS, Voltage Referenced to V-

Symbol	Parameter		Value			Unit
			Min.	Typ.	Max.	
V+	Operating Supply Voltage		3		12	V
T_{amb}	Operating Ambient Temperature	Military	– 55		+125	°C
		Industrial	– 40		+ 85	
		Commercial	0		+ 70	

DC GENERAL ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
	Resistors					
P_+	P_+ Diffusion	Resistor Value Range	30		420	Ω
		Absolute Accuracy			± 25	%
		Matching (note 1)			± 2	%
		Matching (note 2)			± 6	%
		Temperature Coefficient (1^{st} order)			0.12	%/°C
B_{ext}	Extrinsec Base Region	Resitor Value Range	270		5000	Ω
		Absolute Accuracy			± 15	%
		Matching (1)			± 2	%
		Matching (2)			± 6	%
		Temperature Coefficient (1^{st} order)			0.09	%/°C
R_I	Implanted Resitor	Resitor Value Range	5		50	KΩ
		Absolute Accuracy			± 15	%
		Matching (1)			± 2	%
		Matching (2)			± 6	%
		Temperature Coefficient (1^{st} order)			0.21	%/°C
B_{INT}	Intrinsec Base Region	Resitor Value Range	50		100	KΩ
		Absolute Accuracy			± 25	%
		Matching (1)			± 2	%
		Matching (2)			± 6	%
	Capacitors	Capacitor Value Range	2.5		7	pF
		Absolute Accuracy			± 20	%
V_+		Maximum Operating Voltage			20	V
N_{BPC1}		std NPN Transistor (note 3)				
V_{BCB0}	Breakdown Voltage	Collector-base	40			V
V_{BCE0}	Breakdown Voltage	Collector-emitter	18			V
V_{BCS0}	Breakdown Voltage	Collector-substrate	40			V
H_{FE}	Current Gain	@ I_c = 100µA		100		
I_{KF}	Knee Current			5.6		mA
NPWR		Power NPN Transistor (note 3)				
V_{BCB0}	Breakdown Voltage	Collector-base	40			V
V_{BCE0}	Breakdown Voltage	Collector-emitter	18			V
V_{BCS0}	Breakdown Voltage	Collector-substrate	40			V
H_{FE}	Current Gain	@ I_c = 10mA		140		
I_{KF}	Knee Current			314		mA

Notes=
1. matching between 2 resistors of the same value, closed to each other and with the same orientation on the die.
2. matching between 2 resistors of different values, close one from the other and with the same orientation on the die.
3. for more informations refer to the TSFJ user's manual.
4. voltage references are provided by an "ECL reference" macrocell (REFECL) built on a specific tile
5. input voltages could be supplied by a specific tile called HFECL.
6 output levels are not compatible with standard 10K, 100K ECL series.

DC GENERAL ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
PNPS		Substrate PNP Transistor (note 3)				
V_{BCB0}	Breakdown Voltage	Collector-base	40			V
V_{BCE0}	Breakdown Voltage	Collector-emitter	18			V
V_{BCS0}	Breakdown Voltage	Collector-substrate	40			V
H_{FE}	Current Gain	@ I_c = 1µA		160		
I_{KF}	Knee Current			40		µA
		ECL Cells (V_+ = 5V ± 10%)				
V_R	$V_{reference}$	Voltage Reference (note 4)		.97		V
V_{T1}	$V_{reference}$	Voltage Reference (note 4)		3.92		V
V_{T2}	$V_{reference}$	Voltage Reference (note 4)		3.20		V
V_{IL}	Input Voltage	(note 5)			3.6	V
V_{IH}	Input Voltage	(note 5)	4.3			V
V_{OL}	Output Voltage	(note 6)			3.6	V
V_{OH}	Output Voltage	(note 6)	4.3			V

Notes : 1. matching between 2 resistors of the same value, closed to each other and with the same orientation on the die.
2. matching between 2 resistors of different values, close one from the other and with the same orientation on the die.
3. for more informations refer to the TSFJ user's manual.
4. voltage references are provided by an "ECL reference" macrocell (REFECL) built on a specific tile.
5. input voltages could be supplied by a specific tile called HFECL.
6. output levels are not compatible with standard 10K, 100K ECL series.

DIGITAL LIBRARY AC ELECTRICAL CHARACTERISTICS ABSTRACT

(unless otherwise specified, T_{amb} = 25°C, typical process)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
		ECL CELLS				
V_S	Voltage Swing			600		mV
T_G	Toggle Frequency	D Type Flip-flop			100	MHz
t_{PLH}	Propagation Delay	NAND2, (FO = 1)		1.1		ns
t_{PHL}	Propagation Delay	NAND2, (FO = 1)		3.2		ns
		I2L CELLS (note 7)				
T_G	Toggle Frequency	D Type Flip-flop				
		@ Injection = 0.1µA			20	KHz
		@ Injection = 1µA			160	KHz
		@ Injection = 10µA			600	KHz

Note : 7. I2L cells have been caracterised between 0.1µA and 100µA.

ANALOG LIBRARY, AC ELECTRICAL CHARACTERISTICS ABSTRACT

(unless otherwise specified, T_{amb} = 25°C, typical process)

JOPA1 (programmable operationnal amplifier) $V_{CC} \pm 6V$, $I_{set} = 20\mu A$

Symbol	Parameter	Test Conditions	Typical Value	Unit
B	Unity Gain Bandwidth	RL = 5KΩ ; CL = 20pF	1	MHz
ϕM	Phase Margin	Av = 1 ; RL = 5KΩ ; CL = 20pF	60	
Svo	Slew Rate	Av = 1 ; RL = 5KΩ ; CL = 20pF	0.35	V/µs
Av	Open-loop Voltage Gain	RL = 5KΩ ; CL = 20pF	90	dB

JCOMP1 (programmable voltage comparator - LM139 type)

Symbol	Parameter	Test Conditions	Typical Value	Unit
tref	Large Signal Response Time	RL = 5KΩ ; CL = 2pF with Overdrive : 100mV	300	ms
tre	Small Signal Response Time	RL = 5KΩ ; CL = 2pF with Overdrive : 5mV	1	µs
AVD	Large Signal Voltage Gain		87	dB

HIGH FREQUENCY ANALOG BIPOLAR ARRAYS

The K09 array is manufactured using a very high frequency technology (Ft of NPN = 3GHz) which allows a 15V maximum supply operating voltage.

- TECHNOLOGY HF2C, 2 METAL LAYERS
- 1 METAL LAYER TO CUSTOMIZED
- 28 BONDING PADS (maximum)
- 188 NPN TRANSISTORS
- 28 PNP TRANSISTORS (placed in peripheral)
- 686 RESISTORS
- MAXIMUM SUPPLY VOLTAGE = 15V

DESCRIPTION

The K09 array is a prediffused bipolar array of components allowing the user to design his specific applications in a short cycle time and with a minimum risk of errors.

The K09 array from SGS-THOMSON Microelectronics is specially intended for use in video, telecommunication, instrumentation and other high frequency applications, but it could be used with benefit for low frequency applications.

Using kit parts for breadboard, the designer has the capability to validate the schematics in the final application environment.

ANALOG ARRAY :

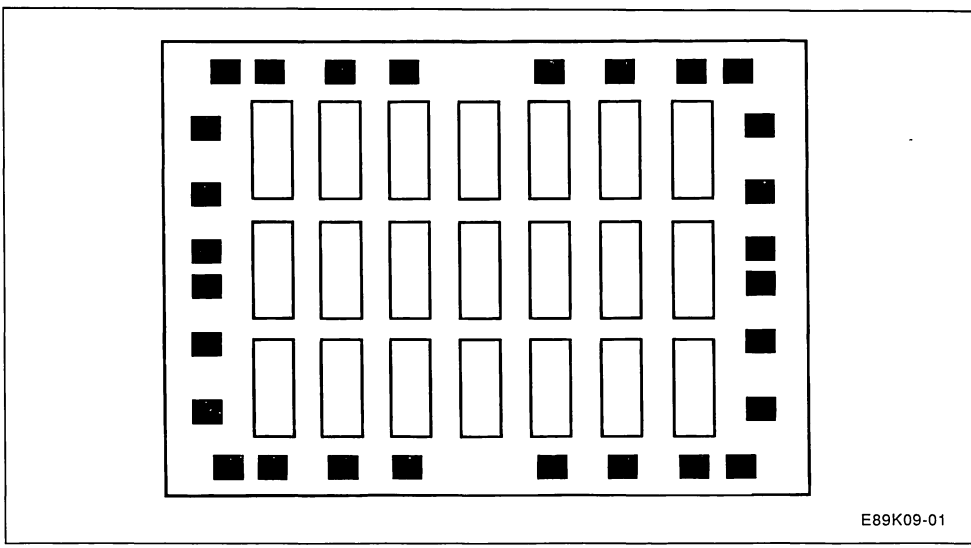
The structure of the K09 based on a regular matrix of 3 x 7 tiles, improves the efficiency of the layout.

Each tile contains :

- 6 QN1 type NPN transistors
- 2 QN2 type NPN transistors
- 100, 200, 400 and 800 P+ type resistors, 1K, 2K, 4K, 8K and 16K Pextrinsec base resistors.

2 independent resistor tubs allow to place 2 positive power supplies if required.

Figure 1 : K09 array architecture.



MAXIMUM VOLTAGE

Volts	NPN	PNP
Collector-base	25	25
Collector-emitter	15	15
Collector-substrate	25	
Base-substrate		25
Emitter-base	5.8	
Base-emitter		25

Resistor voltage = 20V maximum.
Capacitor voltage = ± 20V maximum.

ELECTRICAL CHARACTERISTICS

Current Gain (hFE)		Resistor Tolerances	Resistors Matching
NPN	110 (@.1mA < I < 1mA)	± 25%	Same Value Resistor = ± 2%
PNP	60 (@ I = 10µA)		
$(Ft)_{NPN}$	3GHz (@ I = 1mA)		Different Value Resistor = ± 5%
$(Ft)_{PNP}$	10MHz (@ I = 10µA)		

DEVICES MODELING

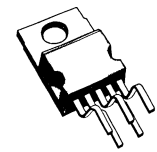
All basic components are available with SPICE models, for the 4 different kinds of transistors, the parameters are :

Symbol	Parameter	QN1	QN2	QN4	PNP	Unit
Is	Transport Saturation Current (10^{-16})	2.1	4.19	10.5	0.5	A
B_F	Ideal Maximum Forward Beta	136	136	136	73	
V_{AF}	Forward Early Voltage	35	35	35	41	V
I_{KF}	Knee Current	14.7	29.4	73.5	43.10^{-3}	mA
R_B	Zero Bias Resistance	292	146	58.4	190	Ω
R_{BM}	Minimum Base Resistance	56.5	28.2	11.3	61.3	Ω
R_E	Emitter Resistance	9.8	4.9	1.96	8.90	Ω
R_C	Collector Resistance	79.5	53.9	32.6	8	Ω

3A POWER OPERATIONAL AMPLIFIER

- OUTPUT CURRENT UP TO 3A
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGES
- SOA PROTECTION
- THERMAL PROTECTION
- ± 18V SUPPLY

The L165 is a monolithic integrated circuit in Pentawatt® package, intended for use as power operational amplifier in a wide range of applications, including servo amplifiers and power supplies. The high gain and high output power capability provide superior performance wherever an operational amplifier/power booster combination is required.



Pentawatt®

ORDER CODE : L165V

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 18	V
$V_5 - V_4$	Upper power transistor V_{CE}	36	V
$V_4 - V_3$	Lower power transistor V_{CE}	36	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 15	V
I_o	Peak output current (internally limited)	3.5	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	– 40 to 150	°C

APPLICATION CIRCUITS

Figure 1 : Gain > 10.

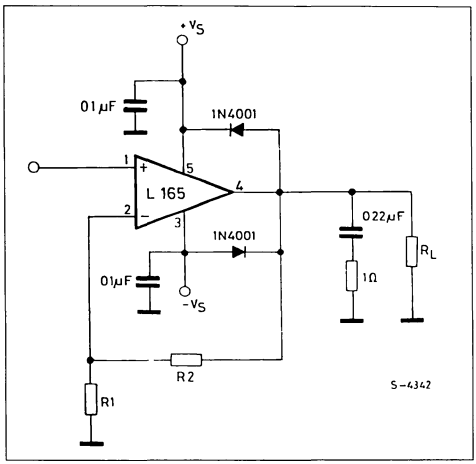
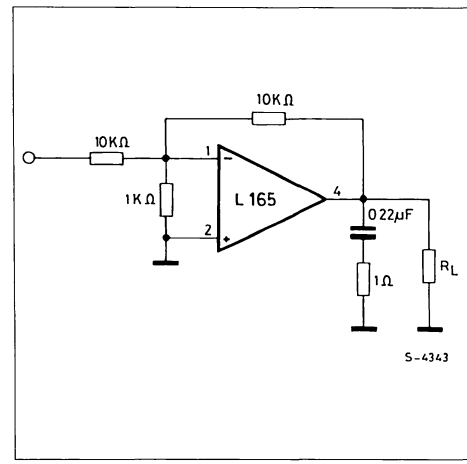
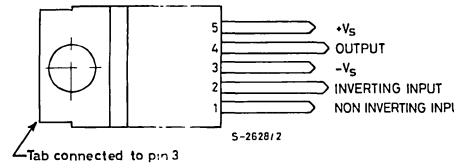


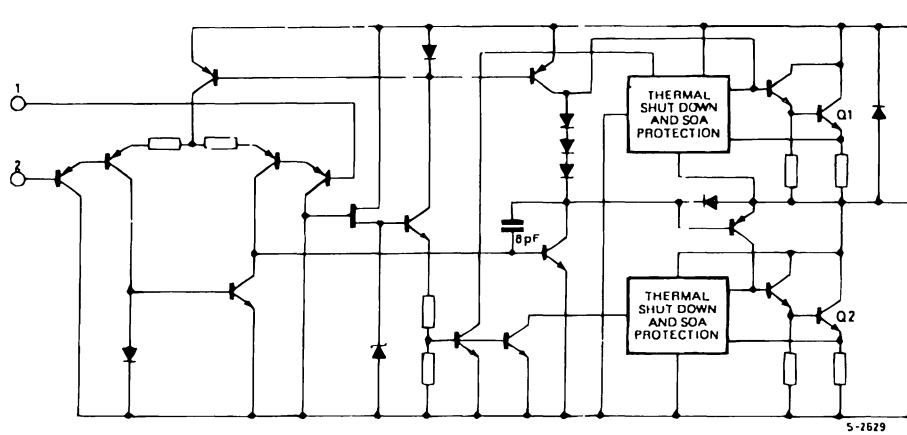
Figure 2 : Unity gain configuration.



CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (V_S = ± 15 V, T_j = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		± 6		± 18	V
I_d	Quiescent Drain Current	V_s = ± 18 V		40	60	mA
I_b	Input Bias Current			0.2	1	µA
V_{os}	Input Offset Voltage			± 2	± 10	mV
I_{os}	Input Offset Current			± 20	± 200	nA
SR	Slew-rate	G_v = 10		8		V/µs
		G_v = 1 (°)		6		
V_o	Output Voltage Swing	f = 1 kHz I_p = 0.3 A		27		V_{pp}
		f = 1 kHz I_p = 3 A		24		
		f = 10 kHz I_p = 0.3 A		27		V_{PP}
		f = 10 kHz I_p = 3 A		23		
R	Input Resistance (pin 1)	f = 1 KHz	100	500		KΩ
G_v	Voltage Gain (open loop)			80		dB
e_N	Input Noise Voltage	B = 10 to 10 000 Hz		2		µV
i_N	Input Noise Current			100		pA
CMR	Common-mode Rejection	R_g ≤ 10 KΩ G_v = 30 dB		70		dB
SVR	Supply Voltage Rejection	R_g = 22 KΩ G_v = 10		60	dB	dB
		V_{ripple} = 0.5 V_{rms} f_{ripple} = 100 Hz dBG_v = 100		40		dB
	Efficiency	f = 1 kHz I_p = 1.6 A ; P_o = 5 W		70		%
		R_L = 4 Ω I_p = 3 A ; P_o = 18 W		60		%
T_{sd}	Thermal Shut-down Case Temperature	P_{tot} = 12 W		110		°C
		P_{tot} = 6 W		130		

Figure 3 : Open loop frequency response.

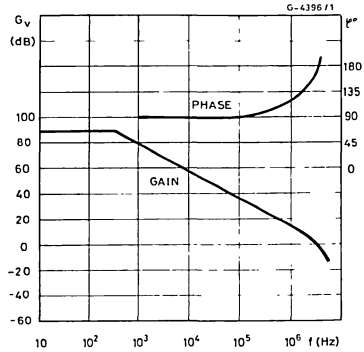


Figure 4 : Closed loop frequency response (circuit of figure 2).

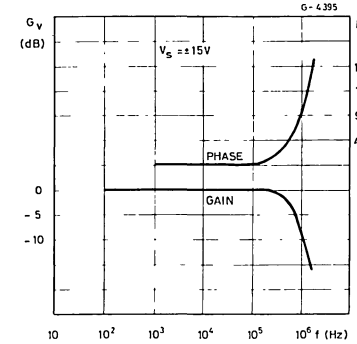


Figure 5 : Large signal frequency response.

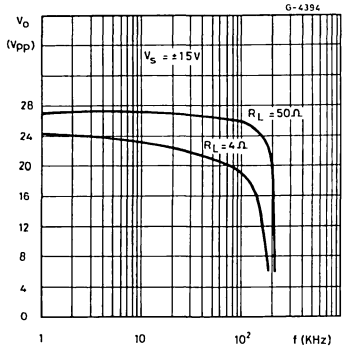


Figure 6 : Maximum output current vs. voltage [VCE] across each output transistor.

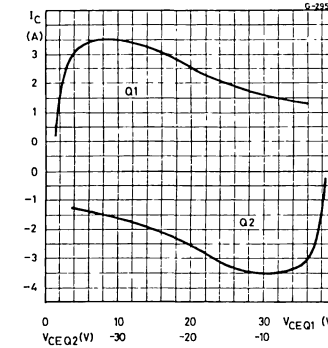


Figure 7 : Safe operating area and collector characteristics of the protected power transistor.

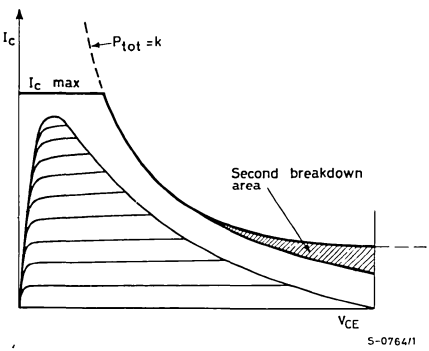


Figure 8 : Maximum allowable power dissipation vs. ambient temperature.

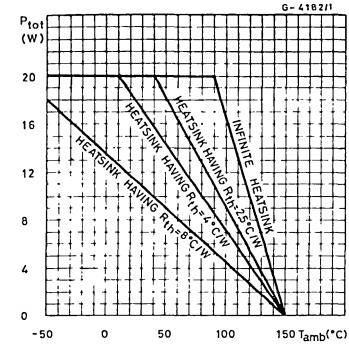
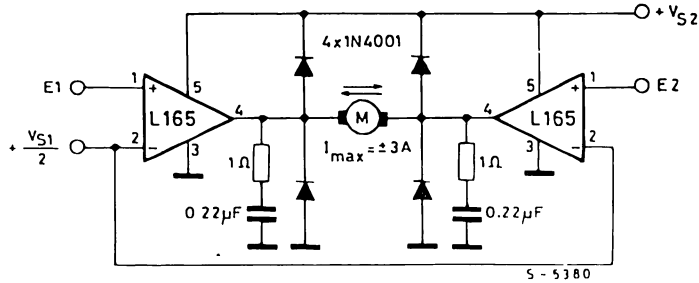
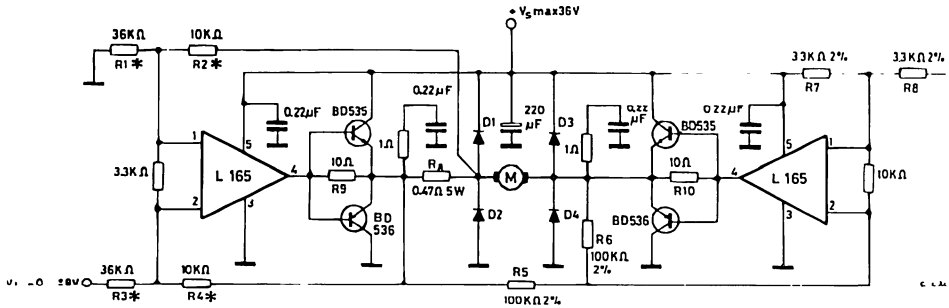


Figure 9 : Bidirectional DC motor control with TTL/CMOS/µP compatible inputs.



Must be $V_{S2} \geq V_{S1}$ E1, E2 = logic inputs
V_{S1} = logic supply voltage

Figure 10 : Motor current control circuit with external power transistors (I_{motor} > 3.5A).

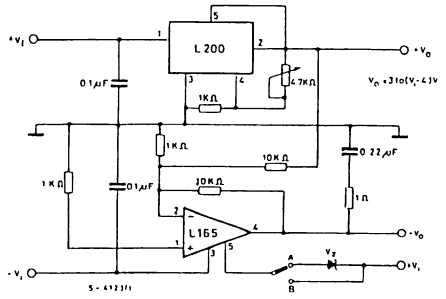


D1 to D4 : $V_F \leq 1.2$ @ I = 4A
trr ≤ 500 ns

Note : The input voltage level is compatible with L291 (5-BIT D/A converter).

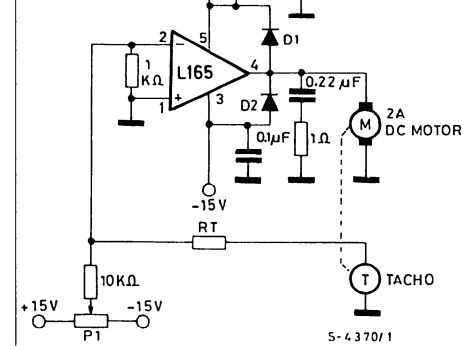
The transfer function is : $\frac{I_M}{V_i} = \frac{R4}{Rx\ R3}$

Figure 11 : High current tracking regulator.



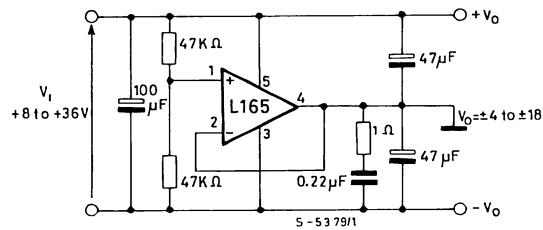
A for $\pm 18 \leq V_i \leq \pm 32$
Note · V_z must be chosen in order to verify
$2 V_i - V_z \leq 36V$
B for $V_i \leq \pm 18V$

Figure 12 : Bidirectional speed control of DC motor (Compensation networks not shown).



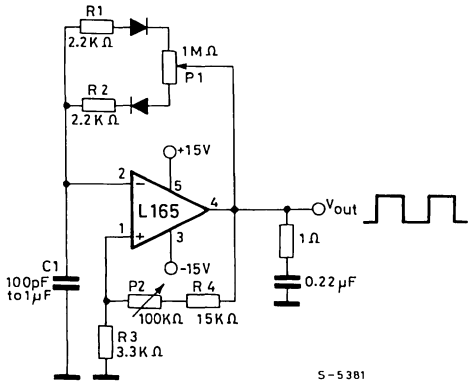
D1, D2 · VF ≤ 1.2V @ I = 2A
trr ≤ 500 ns

Figure 13 : Split power supply.



V_I +8 to +36V
$+V_O$
V_O=±4 to ±18 V
$-V_O$

Figure 14 : Power squarewave oscillator with independent adjustments for frequency and duty-cycle.



P1 : duty-cycle adjust

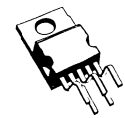
P2 : frequency adjust (f = 700 Hz with C1 = 10 nF, P2 = 100 KΩ, f = 25 Hz with C1 = 10 nF, P2 = 0)

ADJUSTABLE VOLTAGE AND CURRENT REGULATOR

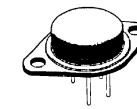
- ADJUSTABLE OUTPUT CURRENT UP TO 2 A (GUARANTEED UP TO T_j = 150 °C)
- ADJUSTABLE OUTPUT VOLTAGE DOWN TO 2.85 V
- INPUT OVERVOLTAGE PROTECTION (UP TO 60 V, 10 ms)
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR S.O.A. PROTECTION
- THERMAL OVERLOAD PROTECTION
- LOW BIAS CURRENT ON REGULATION PIN
- LOW STANDBY CURRENT DRAIN

DESCRIPTION

The L200 is a monolithic integrated circuit for voltage and current programmable regulation. It is available in Pentawatt® package or 4-lead TO-3 metal case. Current limiting, power limiting, thermal shutdown and input overvoltage protection (up to 60 V) make the L200 virtually blow-out proof. The L200 can be used to replace fixed voltage regulators when high output voltage precision is required and eliminates the need to stock a range of fixed voltage regulators.



Pentawatt®



TO–3 (4 lead)

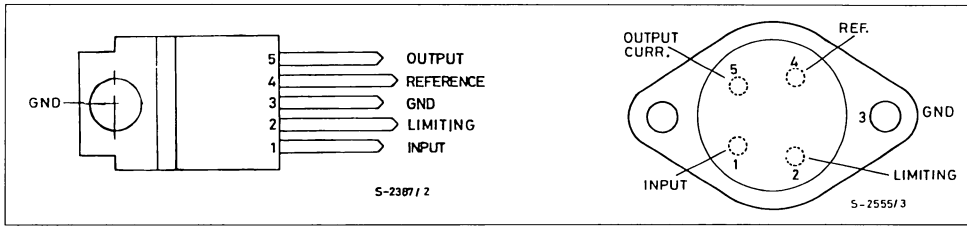
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage	40	V
V_i	Peak Input Voltage (10 ms)	60	V
ΔV_{i-o}	Dropout Voltage	32	V
I_o	Output Current	internally limited	
P_{tot}	Power Dissipation	internally limited	
T_{stg}	Storage Temperature	– 55 to 150	°C
T_{op}	Operating Junction Temperature for L200C	– 25 to 150	°C
	for L200	– 55 to 150	°C

THERMAL DATA

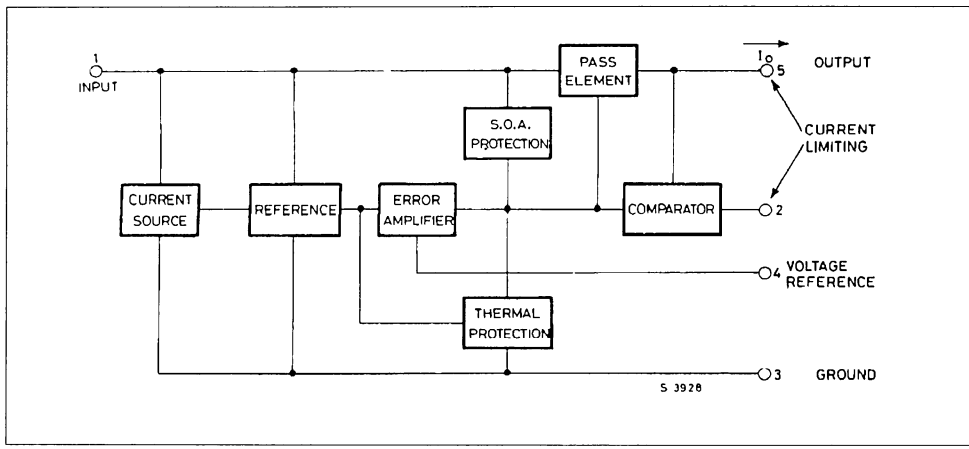
			TO–3	Pentawatt®
$R_{th\,j\text{-}case}$	Thermal Resistance Junction-case	Max	4 °C/W	3 °C/W
$R_{th\,j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	35 °C/W	50 °C/W

CONNECTION DIAGRAMS AND ORDER CODES (top views)



Type	Pentawatt®	TO–3
L200		L200 T
L200 C	L200 CH L200 CV	L200 CT

BLOCK DIAGRAM



APPLICATION CIRCUITS

Figure 1 : Programmable Voltage Regulator with Current Limiting.

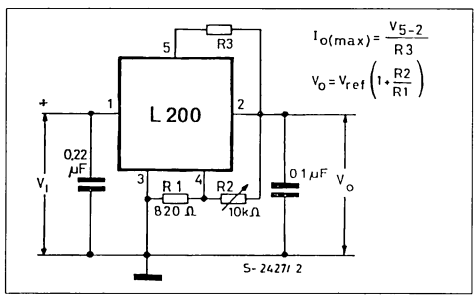
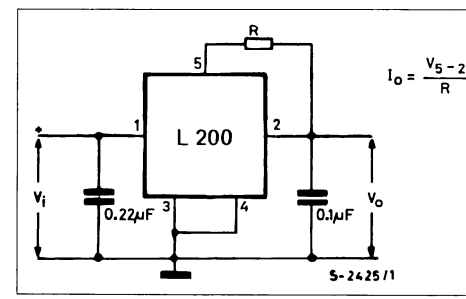
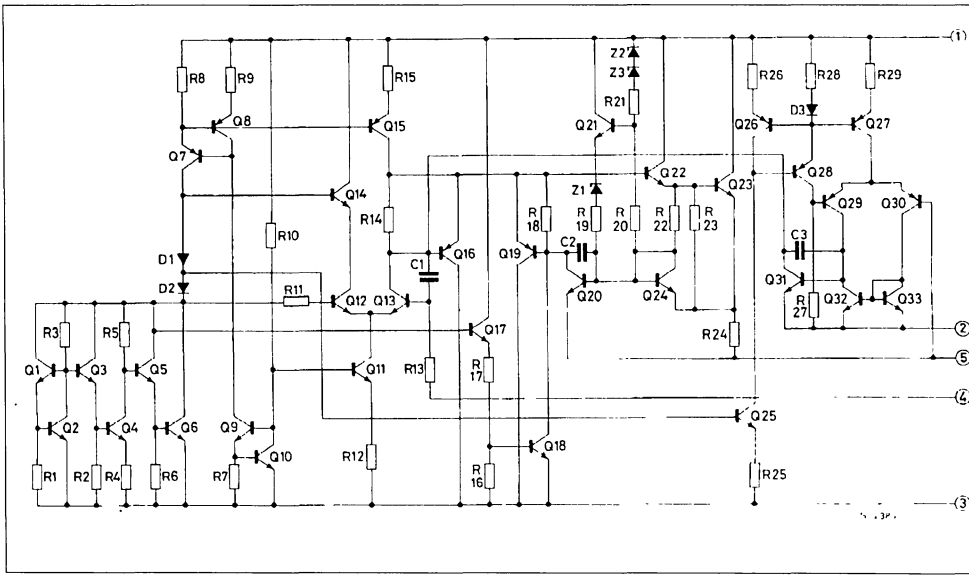


Figure 2 : Programmable Current Regulator.



SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
VOLTAGE REGULATION LOOP						
I_d	Quiescent Drain Current (pin 3)	V_i = 20 V		4.2	9.2	mA
e_N	Output Noise Voltage	$V_o = V_{ref}$ I_o = 10 mA B = 1 MHz		80		µV
V_o	Output Voltage Range	I_o = 10 mA	2.85		36	V
$\frac{\Delta V_o}{V_o}$	Voltage Load Regulation (note 1)	ΔI_o = 2 A ΔI_o = 1.5 A		0.15 0.1	1 0.9	% %
$\frac{\Delta V_i}{\Delta V_o}$	Line Regulation	V_o = 5 V V_i = 8 to 18 V	48	60		dB
SVR	Supply Voltage Rejection	V_o = 5 V I_o = 500 mA ΔV_i = 10 V_{pp} f = 100 Hz (note 2)	48	60		dB
ΔV_{i-o}	Droupout Voltage between Pins 1 and 5	I_o = 1.5 A $\Delta V_o \leq 2$ %		2	2 5	V
V_{ref}	Reference Voltage (pin 4)	V_i = 20 V I_o = 10 mA	2.64	2.77	2.86	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
ΔV_{ref}	Average Temperature Coefficient of Reference Voltage	V_i = 20 V I_o = 10 mA for T_j = – 25 to 125 °C for T_j = 125 to 150 °C		– 0.25 – 1.5		mV/°C mV/°C
I_4	Bias Current at Pin 4			3	10	µA
$\frac{\Delta I_4}{\Delta T \cdot I_4}$	Average Temperature Coefficient (pin 4)			– 0.5		%/°C
Z_o	Output Impedance	V_i = 10 V $V_o = V_{ref}$ I_o = 0.5 A f = 100 Hz		1.5		mΩ

CURRENT REGULATION LOOP

V_{SC}	Current Limit Sense Voltage between Pins 5 and 2	V_i = 10 V $V_o = V_{ref}$ I_5 = 100 mA	0 38	0.45	0 52	V
$\frac{\Delta V_{SC}}{\Delta T \cdot V_{SC}}$	Average Temperature Coefficient of V_{SC}			0.03		%/°C
$\frac{\Delta I_o}{I_o}$	Current Load Regulation	V_i = 10 V ΔV_o = 3 V I_o = 0.5 A I_o = 1 A I_o = 1.5 A		 1.4 1 0.9		 % % %
I_{SC}	Peak Short Circuit Current	$V_i - V_o$ = 14 V (pins 2 and 5 short circuited)			3.6	A

Note 1 A load step of 2 A can be applied provided that input-output differential voltage is lower than 20 V (see Figure 3)

Note 2 The same performance can be maintained at higher output levels if a bypassing capacitor is provided between pins 2 and 4.

Figure 3 : Typical Safe Operating Area Protection.

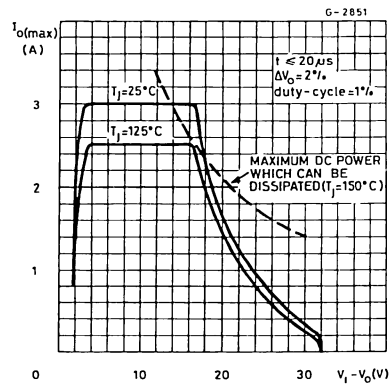


Figure 4 : Quiescent Current vs. Supply Voltage.

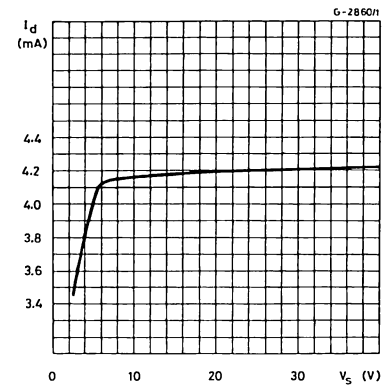


Figure 5 : Quiescent Current vs. Junction Voltage.

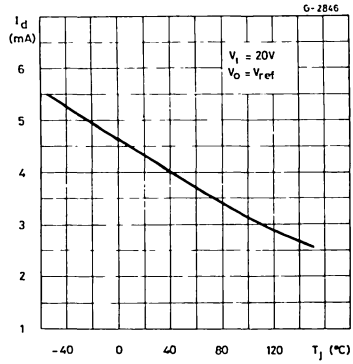


Figure 6 : Quiescent Current vs. Output Current.

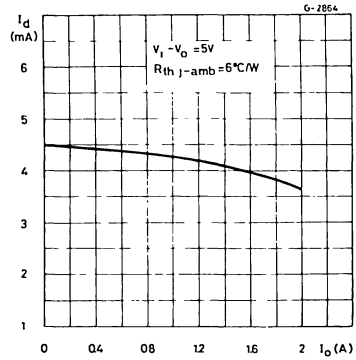


Figure 7 : Output Noise Voltage vs. Output Voltage.

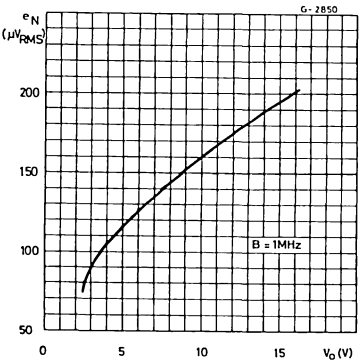


Figure 8 : Output Noise Voltage vs. Frequency.

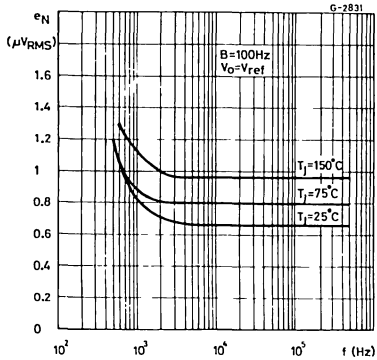


Figure 9 : Reference Voltage vs. Junction Temperature.

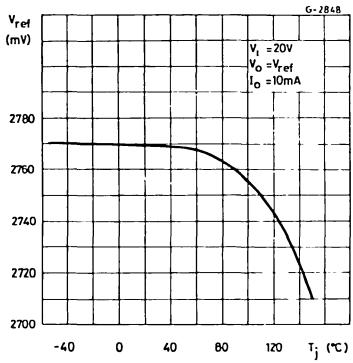


Figure 10 : Voltage Load Regulation vs. Junction Temperature.

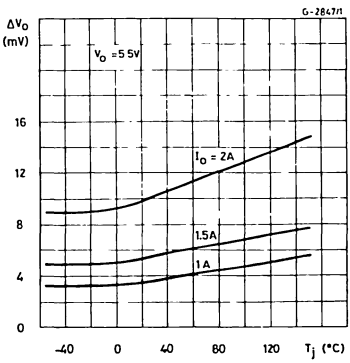


Figure 11 : Supply Voltage Rejection vs. Frequency.

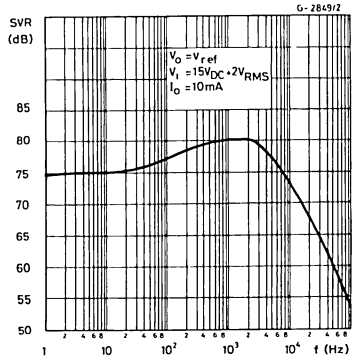


Figure 12 : Dropout Voltage vs. Junction Temperature.

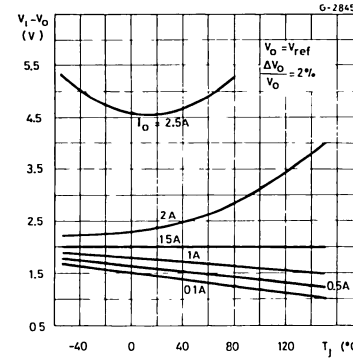


Figure 13 : Output Impedance vs. Frequency.

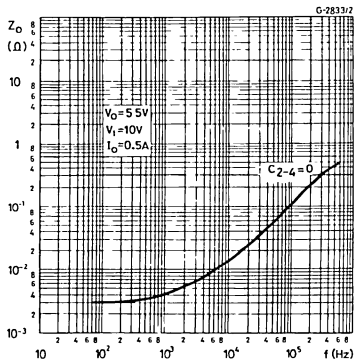


Figure 14 : Output Impedance vs. Output Current.

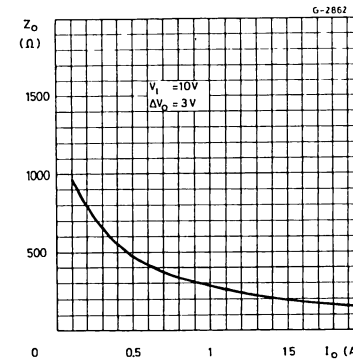


Figure 15 : Voltage Transient Response.

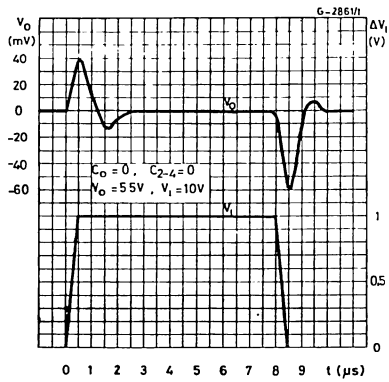


Figure 16 : Load Transient Response.

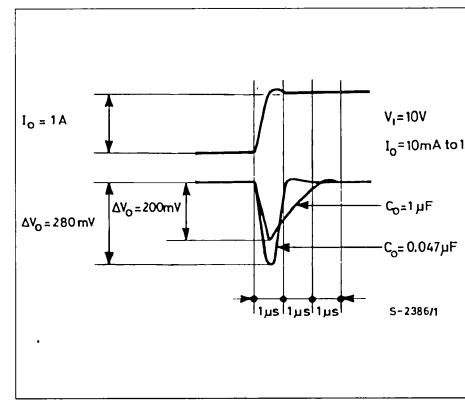


Figure 17 : Load Transient Response.

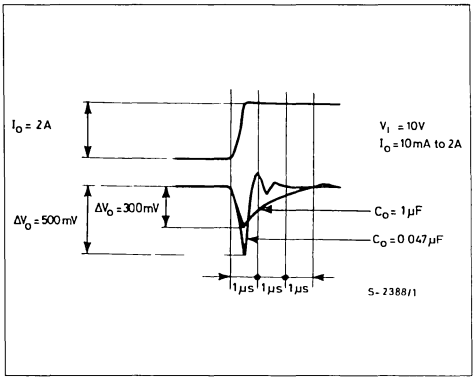
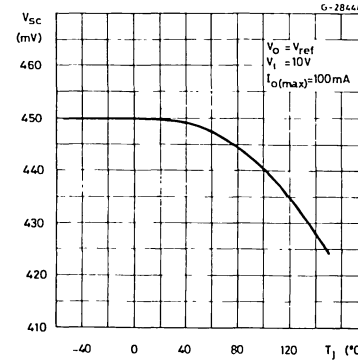


Figure 18 : Current Limit Sense Voltage vs. Junction Temperature.



APPLICATION CIRCUITS

Figure 19 : Programmable Voltage Regulator.

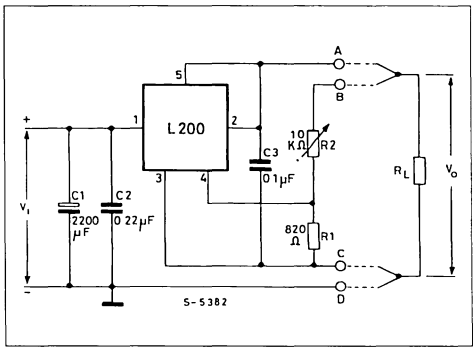


Figure 20 : P.C. Board and Components Layout of Figure 19.

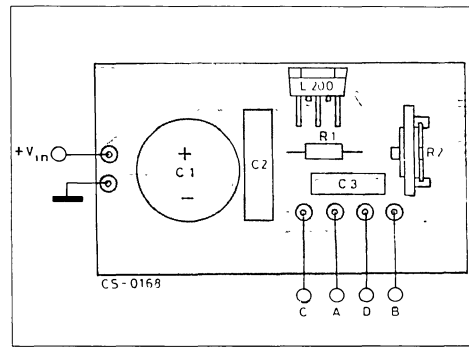


Figure 21 : High Current Voltage Regulator with Short Circuit Protection.

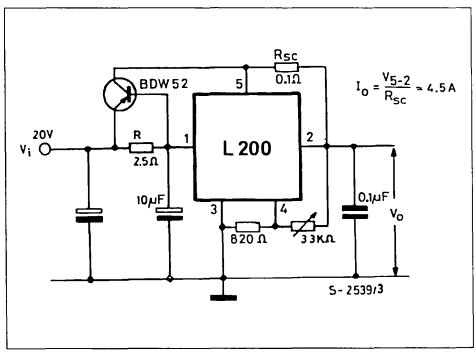


Figure 22 : Digitally Selected Regulator with Inhibit.

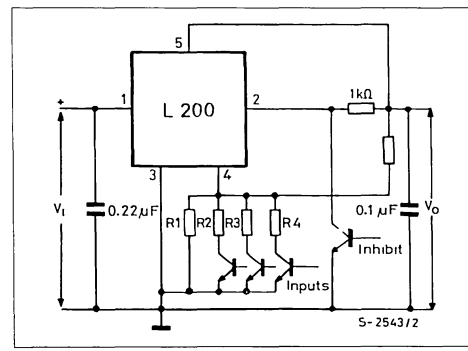
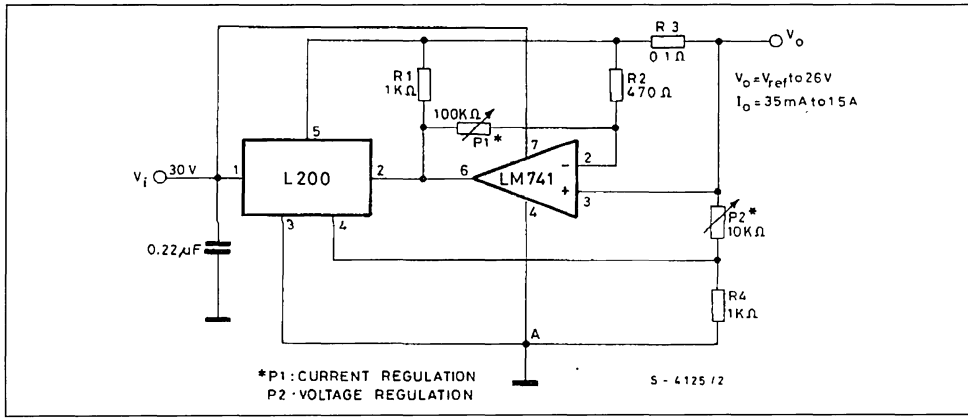


Figure 23 : Programmable Voltage and Current Regulator.



Note : Connecting point A to a negative voltage (for example – 3 V/10 mA) it is possible to extend the output voltage range down to 0 V and to obtain the current limiting down to this level (output short-circuit condition).

Figure 24 : High Current Regulator with NPN Pass Transistor.

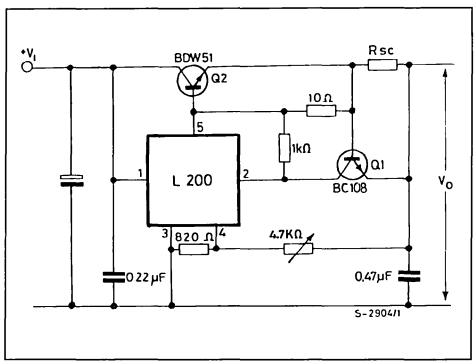
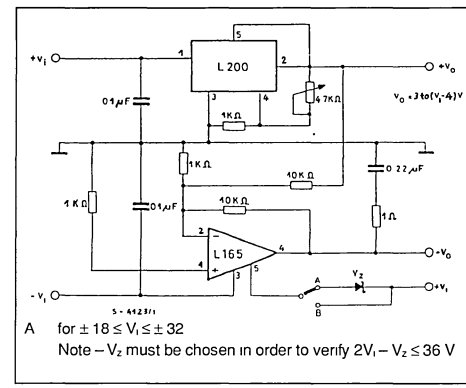


Figure 25 : High Current Tracking Regulator.



A for $\pm 18 \leq V_i \leq \pm 32$

Note – V_z must be chosen in order to verify $2V_i - V_z \leq 36$ V

Figure 26 : High Input and Output Voltage.

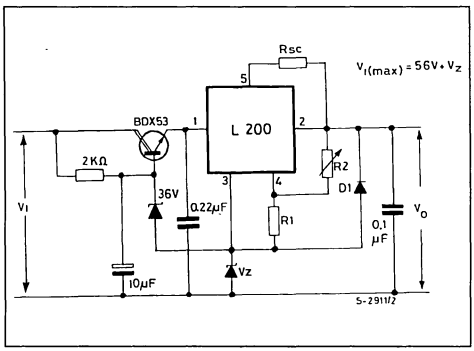
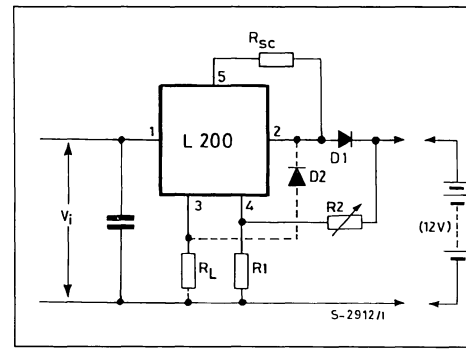


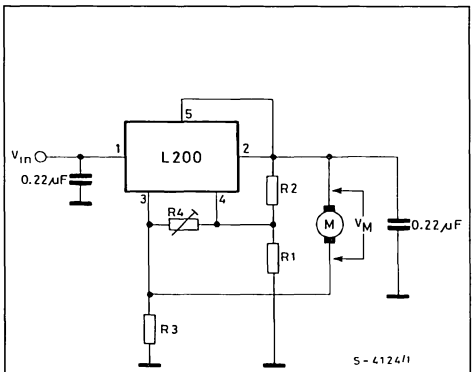
Figure 27 : Constant Current Battery Charger.



The resistors R_1 and R_2 determine the final charging voltage and R_{SC} the initial charging current D_1 prevents discharge of the battery throught the regulator.

The resistor R_L limits the reverse currents through the regulator (which should be 100 mA max) when the battery is accidentally reverse connected If R_L is in series with a bulb of 12 V/50 mA rating this will indicate incorrect connection

Figure 28 : 30 W Motor Speed Control.



$$R_3 = \frac{R_1}{R_2} \cdot R_M$$

$$V_M = V_{ref} \cdot (1 + \frac{R_2}{R_1})$$

Figure 29 : Low Turn on.

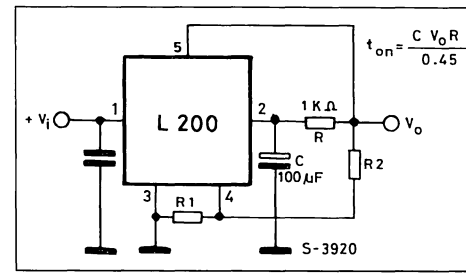
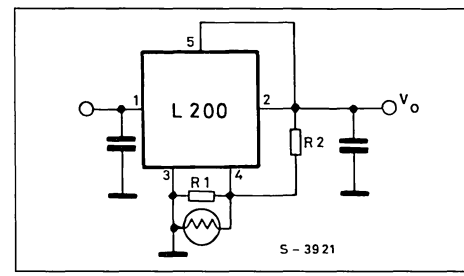


Figure 30 : Light Controller.

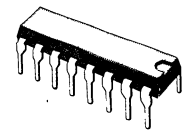


DUAL POWER OPERATIONAL AMPLIFIERS

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN

The L272 and L272M are monolithic integrated circuits in powerdip and minidip packages intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies, compact disc, VCR, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



Powerdip (8 + 8) **Minidip Plastic**

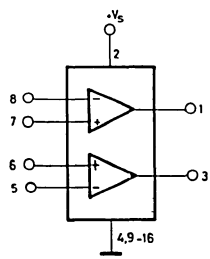
ORDERING NUMBERS:

L272 L272M

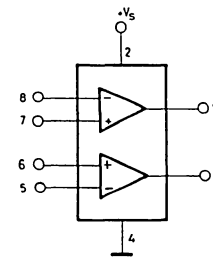
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at T_{amb} = 80°C **(L272)**, T_{amb} = 50°C **(L272M)**	1	W
	T_{case} = 75°C **(L272)**	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAM

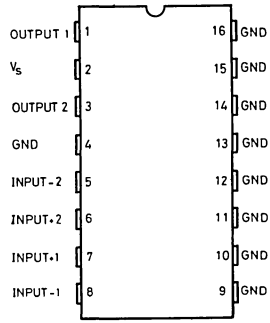


L272

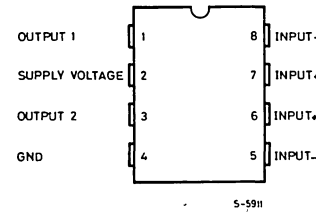


L272M

CONNECTION DIAGRAM
(Top view)

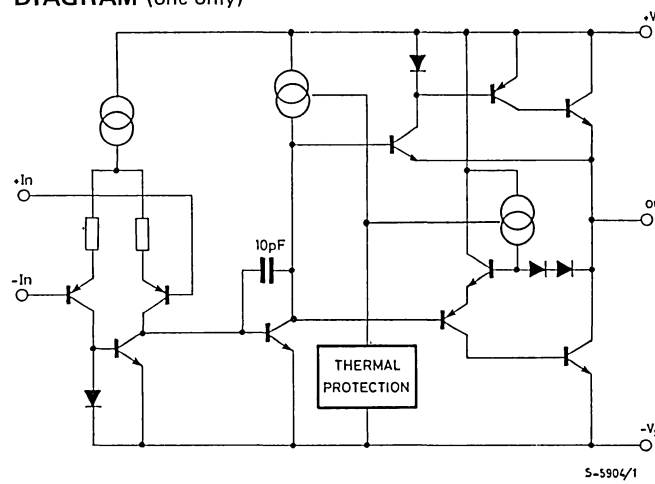


L272



L272M

SCHEMATIC DIAGRAM (one only)



THERMAL DATA

			Powerdip	Minidip
$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max	15°C/W	*70°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70°C/W	100°C/W

* Thermal resistance junction-pin 4

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			4		28	V
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$	V_s = 24V		8	12	mA
			V_s = 12V		7.5	11	mA
I_b	Input bias current				0.3	2.5	μA
V_{os}	Input offset voltage				15	60	mV
I_{os}	Input offset current				50	250	nA
SR	Slew rate				1		V/μs
B	Gain-bandwidth product				350		KHz
R_I	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		60	70		dB
		f = 1KHz			50		dB
e_N	Input noise voltage	B = 20KHz			10		μV
I_N	Input noise current	B = 20KHz			200		pA
CRR	Common Mode rejection	f = 1KHz		60	75		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	54	70 62 56		dB dB dB
V_o	Output voltage swing		I_p = 0.1A I_p = 0.5A	21	23 22.5		V V
C_s	Channel separation	f = 1KHz; R_L = 10Ω; G_v = 30dB	V_s = 24V V_s = ± 6V		60 60		dB dB
d	Distortion	f = 1KHz V_s = 24V	G_v = 30dB R_L = ∞		0.5		%
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

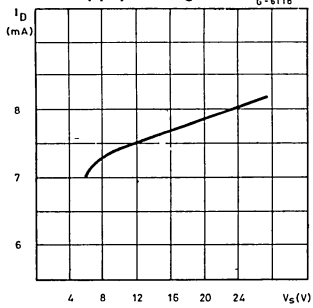


Fig. 2 - Quiescent drain current vs. temperature

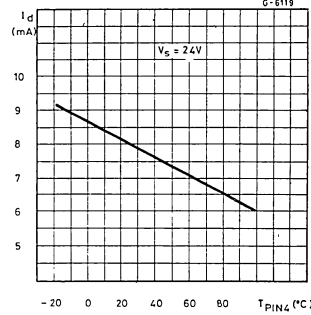


Fig. 3 - Open loop voltage gain

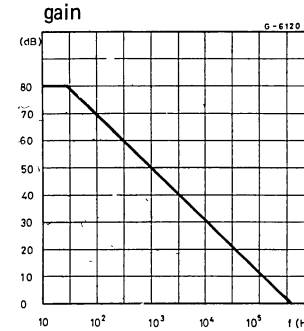


Fig. 4 - Output voltage swing vs. load current

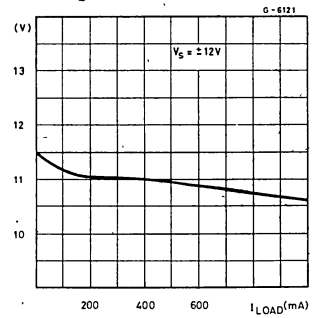


Fig. 5 - Output voltage swing vs. load current

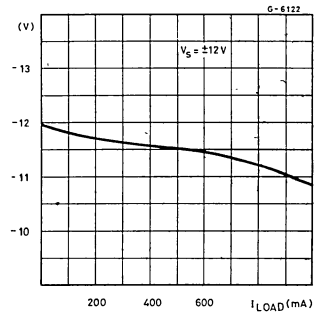


Fig. 6 - Supply voltage rejection vs. frequency

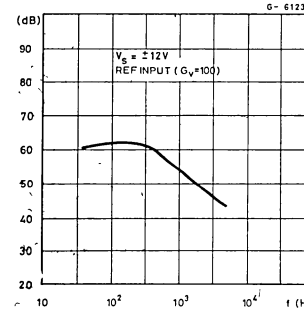


Fig. 7 - Channel separation vs. frequency

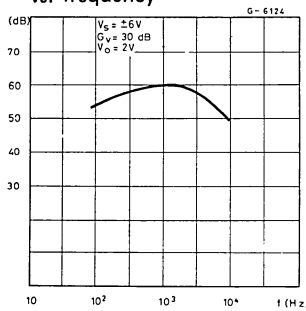
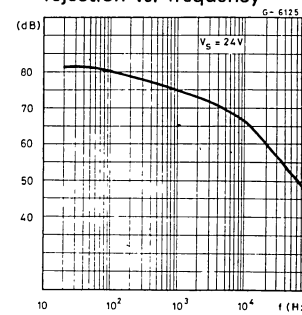


Fig. 8 - Common mode rejection vs. frequency



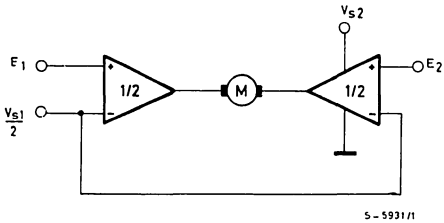
APPLICATION SUGGESTION

NOTE

In order to avoid possible instability occurring into final stage the usual suggestions for the linear power stages are useful, as or instance:

- layout accuracy;
- A 100nF capacitor corrected between supply pins and ground;
- boucherot cell (0.1 to 0.2μF +1Ω series) between outputs and ground or across the load.

Fig. 9 - Bidirectional DC motor control with μP compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} > V_{S1}$

E1, E2 = logic inputs

Fig. 10 - Servocontrol for compact-disc

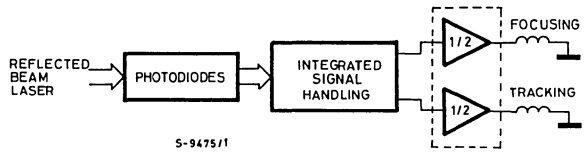


Fig. 11 - Capstan motor control in video recorders

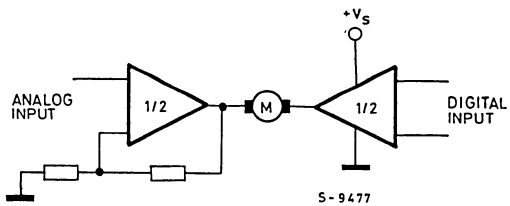
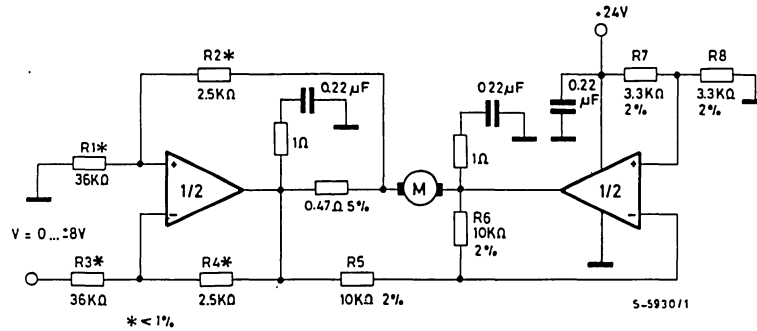


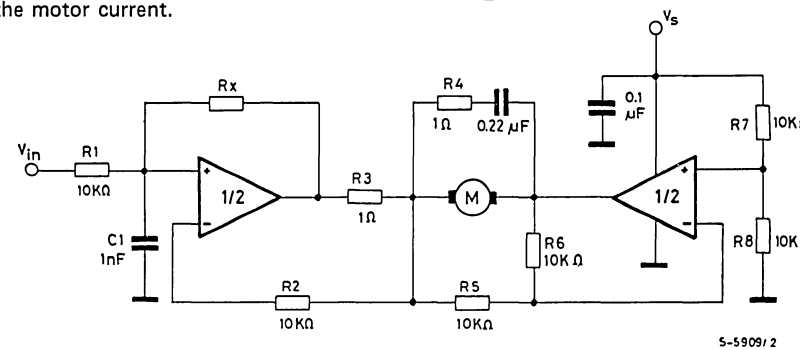
Fig. 12 - Motor current control circuit



Note: The input voltage level is compatible with L291 (5-BIT D/A converter)

Fig. 13 - Bidirectional speed control of DC motors.

For circuit stability ensure that $R_X > \frac{2R3 \circ R1}{R_M}$ where R_M = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2\left(V_I - \frac{V_s}{2}\right) + |R_o|.\ I_M$ where $|R_o| = \frac{2R3 \circ R1}{R_X}$ and I_M is the motor current.



HIGH CURRENT SWITCHING REGULATORS

- 4 A OUTPUT CURRENT
- 5.1 V TO 40 V OUTPUT VOLTAGE RANGE
- 0 TO 100 % DUTY CYCLE RANGE
- PRECISE (±2 %) ON-CHIP REFERENCE
- SWITCHING FREQUENCY UP TO 200 KHz
- VERY HIGH EFFICIENCY (UP TO 90 %)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- RESET OUTPUT
- EXTERNAL PROGRAMMABLE LIMITING CURRENT (L296P)
- CONTROL CIRCUIT FOR CROWBAR SCR
- INPUT FOR REMOTE INHIBIT AND SYNCHRONUS PWM
- THERMAL SHUTDOWN

DESCRIPTION

The L296 and L296P are stepdown power switching regulators delivering 4 A at a voltage variable from 5.1 V to 40 V.

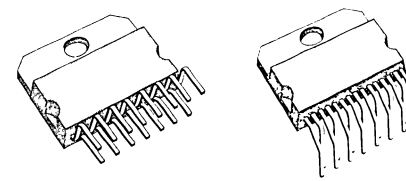
Features of the devices include soft start, remote inhibit, thermal protection, a reset output for microprocessors and a PWM comparator input for synchronization in multichip configurations.

The L296P incudes external programmable limiting current.

The L296 and L296P are mounted in a 15-lead Multiwatt® plastic power package and requires very few external components.

Efficient operation at switching frequencies up to 200 KHz allows a reduction in the size and cost of external filter components. A voltage sense input and SCR drive output are provided for optional crowbar overvoltage protection with an external SCR.

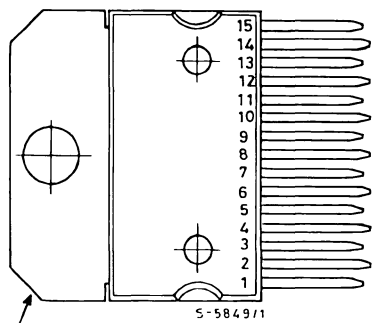
Multiwatt®
(15-lead)



ORDER CODES :

L296	L296HT
L296P	L296PHT

PIN CONNECTION (top view)



15	CROWBAR DRIVE
14	RESET OUTPUT
13	RESET DELAY
12	RESET INPUT
11	OSCILLATOR
10	FEEDBACK INPUT
9	FREQUENCY COMPENSATION
8	GROUND
7	SYNC. INPUT
6	INHIBIT INPUT
5	SOFT-START
4	CURRENT LIMIT
3	SUPPLY VOLTAGE
2	OUTPUT
1	CROWBAR INPUT

Tab connected to pin 8

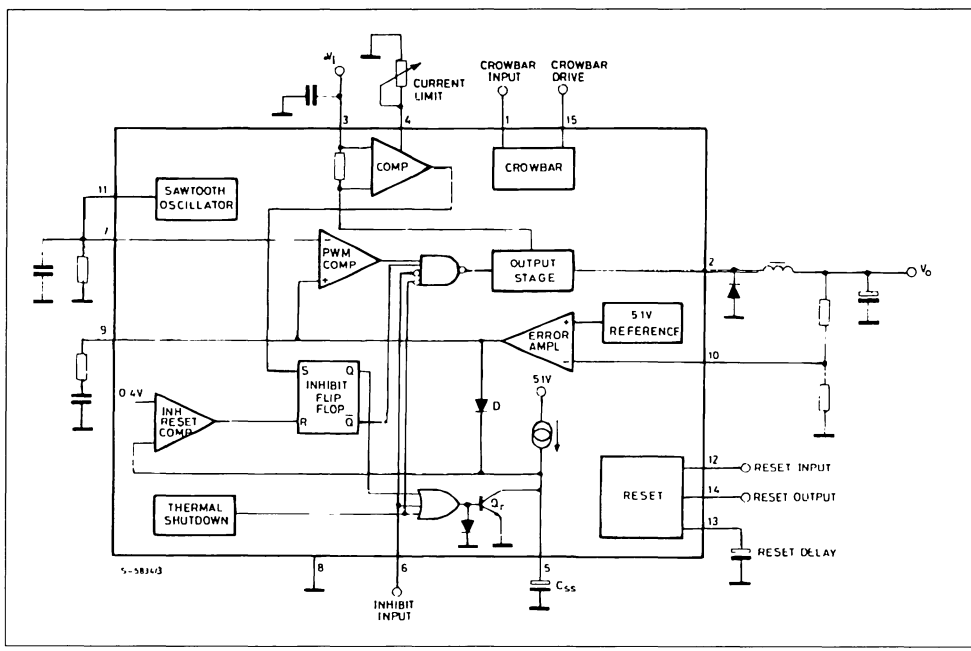
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_i	Input Voltage (pin 3)	50	V
$V_i - V_2$	Input to Output Voltage Difference	50	V
V_2	Output DC Voltage Output Peak Voltage at t = 0.1 µsec f = 200KHz	– 1 – 7	V V
V_1, V_{12}	Voltage at Pins 1, 12	10	V
V_{15}	Voltage at Pin 15	15	V
V_4, V_5, V_7, V_9, V_{13}	Voltage at Pins 4, 5, 7, 9 and 13	5.5	V
V_{10}, V_6	Voltage at Pins 10 and 6	7	V
V_{14}	Voltage at Pin 14 ($I_{14} \leq 1$ mA)	V_i	
I_9	Pin 9 Sink Current	1	mA
I_{11}	Pin 11 Source Current	20	mA
I_{14}	Pin 14 Sink Current ($V_{14} < 5$ V)	50	mA
P_{tot}	Power Dissipation at $T_{case} \leq 90$ °C	20	W
T_j, T_{stg}	Junction and Storage Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	35	°C/W

BLOCK DIAGRAM



PIN FUNCTIONS

N°	Name	Function
1	CROWBAR INPUT	Voltage Sense Input for Crowbar Overvoltage Protection. Normally connected to the feedback input thus triggering the SCR when V_{out} exceeds nominal by 20 %. May also monitor the input and a voltage divider can be added to increase the threshold. Connected to ground when SCR not used.
2	OUTPUT	Regulator Output.
3	SUPPLY VOLTAGE	Unrergulated Voltage Input. An internal Regulator Powers the L296s Internal Logic.
4	CURRENT LIMIT	A resistor connected between this terminal and ground sets the current limiter threshold. If this terminal is left unconnected the threshold is internally set (see electrical characteristics).
5	SOFT START	Soft Start Time Constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
6	INHIBIT INPUT	TTL – Level Remote Inhibit. A logic high level on this input disables the device.
7	SYNC INPUT	Multiple L296s are synchronized by connecting the pin 7 inputs together and omitting the oscillator RC network on all but one device.
8	GROUND	Common Ground Terminal.
9	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
10	FEEDBACK INPUT	The Feedback Terminal on the Regulation Loop. The output is connected directly to this terminal for 5.1 V operation ; it is connected via a divider for higher voltages.
11	OSCILLATOR	A parallel RC networki connected to this terminal determines the switching frequency. This pin must be connected to pin 7 input when the internal oscillator is used.
12	RESET INPUT	Input of the Reset Circuit. The threshold is roughly 5 V. It may be connected to the feedback point or via a divider to the input.
13	RESET DELAY	A capacitor connected between this terminal and ground determines the reset signal delay time.
14	RESET OUTPUT	Open collector reset signal output. This output is high when the supply is safe.
15	CROWBAR OUTPUT	SCR gate drive output of the crowbar circuit.

CIRCUIT OPERATION (refer to the block diagram)

The L296 and L296P are monolithic stepdown switching regulators providing output voltages from 5.1 V to 40 V and delivering 4 A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1 V on-chip reference (zener zap trimmed to ± 2 %). This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage. The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 9. Closing the loop directly gives an output voltage of 5.1 V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor Css and allowed to rise, linearly, as this capacitor is charged by a constant current source.

Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4 V. The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network.

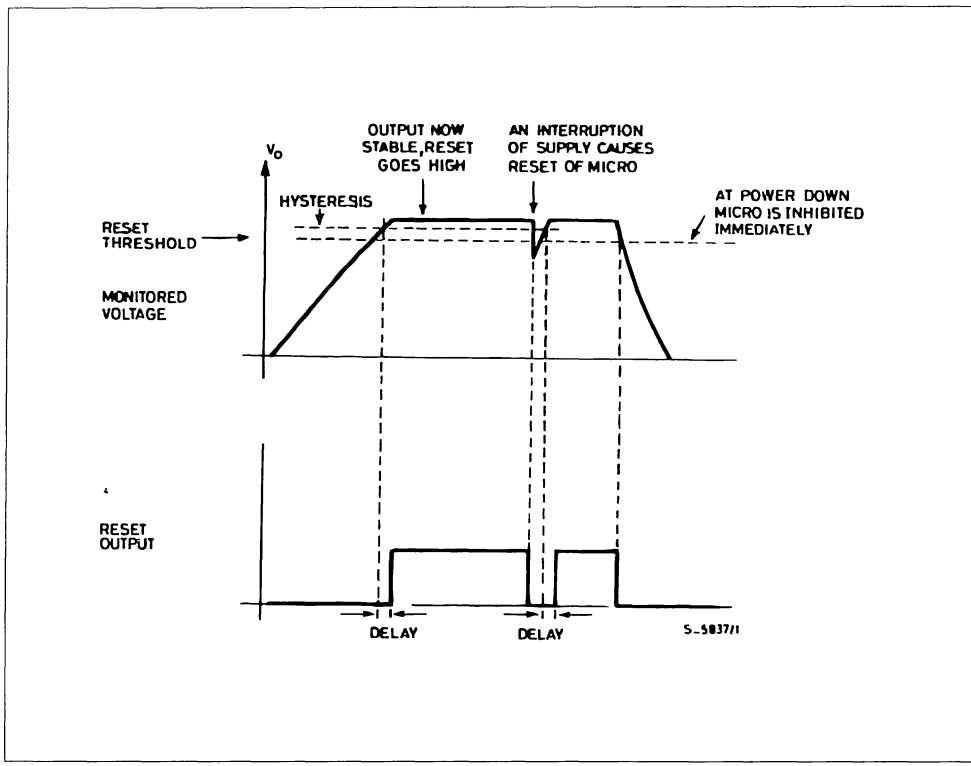
The reset circuit generates an output signal when the supply voltage exceeds a threshold programmed by an external divider. The reset signal is generated with a delay time programmed by an external capacitor. When the supply falls below the threshold the reset output goes low immediately. The reset output is an open collector.

The scrowbar circuit senses the output voltage and the crowbar output can provide a current of 100 mA to switch on an external SCR. This SCR is triggered when the output voltage exceeds the nominal by 20 %. There is no internal connection between the output and crowbar sense input therefore the crowbar can monitor either the input or the output.

A TTL - level inhibit input is provided for applications such as remote on/off control. This input is activated by high logic level and disables circuit operation. After an inhibit the L296 restarts under control of the soft start network.

The thermal overload circuit disables circuit operation when the junction temperature reaches about 150 °C and has hysteresis to prevent unstable conditions.

Figure 1 : Reset Output Waveforms.



CIRCUIT OPERATION (continued)

Figure 2 : Soft Start Waveforms.

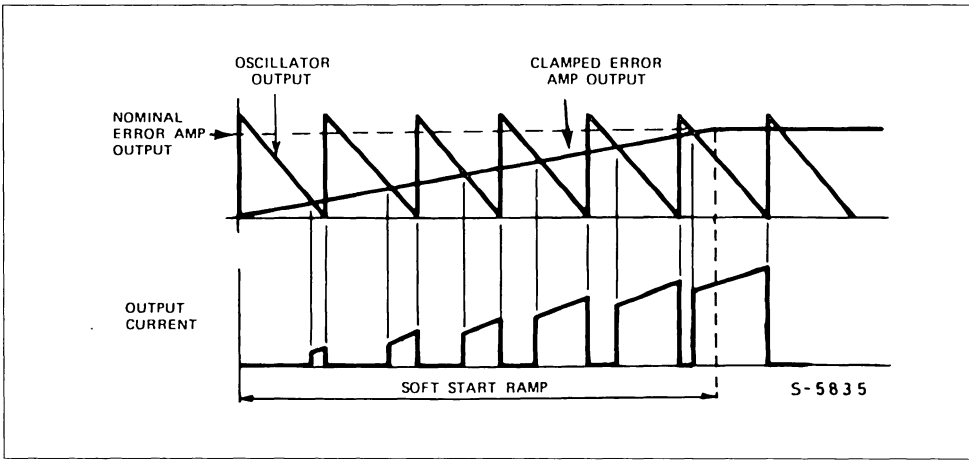
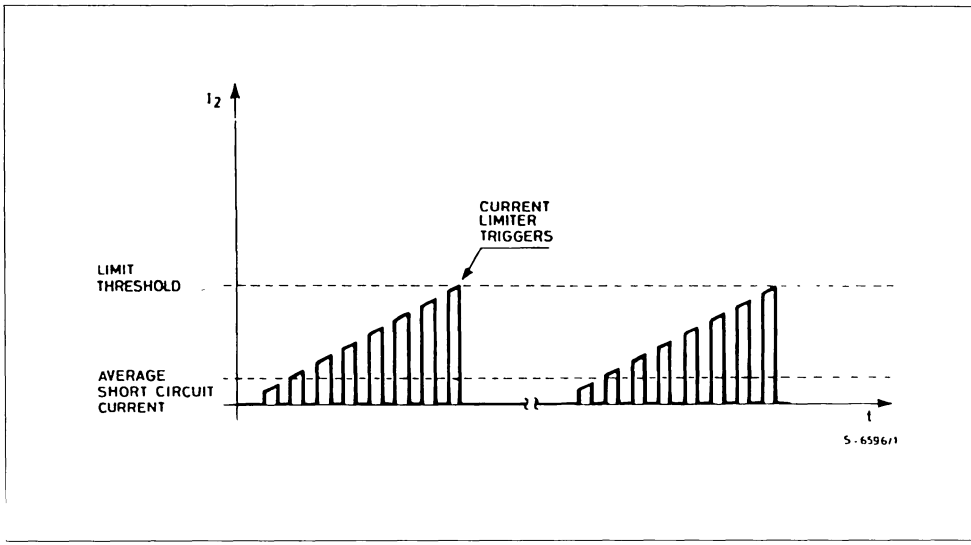


Figure 3 : Current Limiter Waveforms.



ELECTRICAL CHARACTERISTICS (refer to the test circuits T_j = 25 °C, V_i = 35 V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.

DYNAMIC CHARACTERISTICS (pin 6 to GND unless otherwise specified)

V_o	Output Voltage Range	V_i = 46 V I_o = 1 A	V_{ref}		40	V	4
V_i	Input Voltage Range	$V_o = V_{ref}$ to 36 V $I_o \leq 3$ A	9		46	V	4
V_i	Input Voltage Range	Note (1) $V_o = V_{REF}$ to 36 V I_o = 4 A			46	V	4
ΔV_o	Line Regulation	V_i =10 V to 40 V, $V_o = V_{ref}$, I_o = 2 A		15	50	mV	4
ΔV_o	Load Regulation	I_o = 2 A to 4 A		10	30	mV	4
		$V_o = V_{ref}$ I_o = 0.5 A to 4 A		15	45	mV	4
V_{ref}	Internal Reference Voltage (pin 10)	V_i = 9 V to 46 V I_o = 2 A	5	5.1	5.2	V	4
$\frac{\Delta V_{ref}}{\Delta T}$	Average Temperature Coefficient of Reference Voltage	T_j = 0 °C to 125 °C I_o = 2 A		0.4		mV/°C	
V_d	Dropout Voltage Between Pin 2 and Pin 3	I_o = 4 A		2	3.2	V	4
		I_o = 2 A		1.3	2.1	V	4
I_{2L}	Current Limiting Threshold (pin 2)	L296 Pin 4 Open V_i = 9 V to 40 V $V_o = V_{ref}$ to 36 V	4.5		7.5	A	4
		L296P Pin 4 Open	5		7	A	4
		V_i = 9 V to 40 V $V_o = V_{ref}$ R_{lim} = 22 KΩ	2.5		4.5	A	4
I_{SH}	Input Average Current	V_i = 46 V; Output Short-circuited		60	100	mA	4
η	Efficiency	I_o = 3 A $V_o = V_{ref}$		75		%	4
		V_o = 12 V		85		%	4
SVR	Supply Voltage Ripple Rejection	ΔV_i = 2 V_{rms} f_{ripple} = 100 Hz $V_o = V_{ref}$ I_o = 2 A	50	56		dB	4
f	Switching Frequency		85	100	115	KHz	4
$\frac{\Delta f}{\Delta V_i}$	Voltage Stability of Switching Frequency	V_i = 9 V to 46 V		0.5		%	4
$\frac{\Delta f}{\Delta T_j}$	Temperature Stability of Switching Frequency	T_j = 0 °C to 125 °C		1		%	4
f_{max}	Maximum Operating Switching Frequency	$V_o = V_{ref}$; I_o = 1 A	200			KHz	–
T_{sd}	Thermal Shutdown Junction Temperature	Note (2)	135	145		°C	–

DC CHARACTERISTICS

I_{3Q}	Quiescent Drain Current	V_i = 46 V V_7 = 0 V S1 : B S2 : B V_6 = 0 V		66	85	mA	6a
		V_6 = 3V		30	40	mA	6a
$-I_{2L}$	Output Leakage Current	V_i = 46 V, V_6 = 3 V, S1 : B, S2 : A, V_7 = 0 V			2	mA	6a

Note (1) : Using min. 7 A schottky diode
(2) : Guaranteed by design, not 100 % tested in production

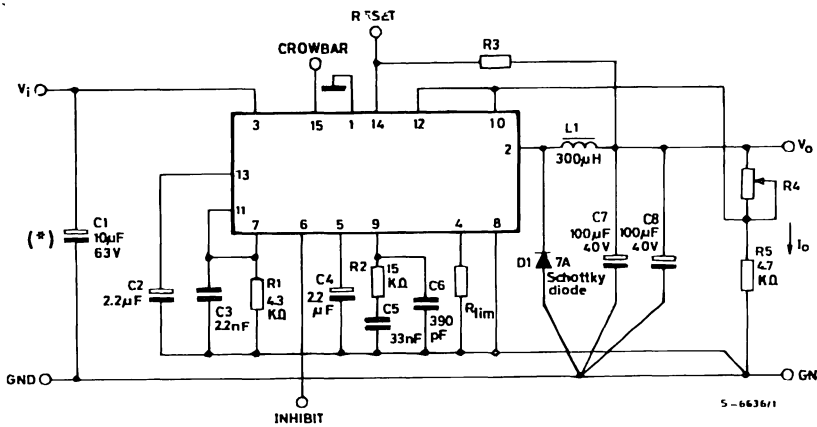
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
SOFT START								
$I_{5\,so}$	Source Current	$V_6 = 0$ V, $V_5 = 3$ V		80	130	150	µA	6b
$I_{5\,si}$	Sink Current	$V_6 = 3$ V, $V_5 = 3$ V		50	70	120	µA	6b
INHIBIT								
V_{6L}	Low Input Voltage	$V_i = 9$ V to 46 V	S1 : B S2 : B	− 0.3		0.8	V	6a
V_{6H}	High Input Voltage	$V_7 = 0$ V		2		5.5	V	6a
$-I_{6L}$	Input Current with Low Input Voltage	$V_i = 9$ V to 46 V	$V_6 = 0.8$ V			10	µA	6a
$-I_{6H}$	Input Current with High Input Voltage	$V_7 = 0$ V S1 : B S2 : B	$V_6 = 2$ V			3	µA	6a
ERROR AMPLIFIER								
V_{9H}	High Level Output Voltage	$V_{10} = 4.7$ V, $I_9 = 100$ µA, S1 : A, S2 : A		3.5			V	6c
V_{9L}	Low Level Output Voltage	$V_{10} = 5.3$ V, $I_9 = 100$ µA, S1 : A, S2 : E				0.5	V	6c
$I_{9\,si}$	Sink Output Current	$V_{10} = 5.3$ V,	S1 : A, S2 : B	100	150		µA	6c
$-I_{9\,so}$	Source Output Current	$V_{10} = 4.7$ V,	S1 : A, S2 : D	100	150		µA	6c
I_{10}	Input Bias Current	$V_{10} = 5.2$ V,	S1 : B		2	10	µA	6c
		$V_{10} = 6.4$ V,	S1 : B, L296P		2	10	µA	6c
G_v	DC Open Loop Gain	$V_9 = 1$ V to 3 V,	S1 : A, S2 : C	46	55		dB	6c
OSCILLATOR AND PWM COMPARATOR								
$-I_7$	Input Bias Current of PWM Comparator	$V_7 = 0.5$ V to 3.5 V				5	µA	6a
$-I_{11}$	Oscillator Source Current	$V_{11} = 2$ V,	S1 : A S2 : B	5				mA
RESET								
$V_{12\,R}$	Rising Threshold Voltage	$V_i = 9$ V to 46 V,	S1 : B, S2 : B	V_{ref} -150mV	V_{ref} -100mV	V_{ref} -50mV	V	6d
$V_{12\,F}$	Falling Threshold Voltage			4.75	V_{ref} -150mV	V_{ref} -100mV	V	6d
$V_{13\,D}$	Delay Thershold Voltage	$V_{12} = 5.3$ V,	S1 : A, S2 : B	4.3	4.5	4.7	V	6d
$V_{13\,H}$	Delay Threshold Voltage Hysteresis				100		mV	6d
$V_{14\,S}$	Output Saturation Voltage	$I_{14} = 16$ mA; $V_{12} = 4.7$ V; S1, S2 : B				0.4	V	6d
I_{12}	Input Bias Current	$V_{12} = 0$ V to V_{ref},	S1 : B, S2 : B		1	3	µA	6d
$-I_{13\,so}$	Delay Source Current	$V_{13} = 3$ V S1 : A S2 : B	$V_{12} = 5.3$ V	70	110	140	µA	6d
$I_{13\,si}$	Delay Sink Current		$V_{12} = 4.7$ V	10			mA	6d
I_{14}	Output Leakage Current	$V_i = 46$ V, $V_{12} = 5.3$ V,	S1 : B, S2 : A			100	µA	6d

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
CROWBAR								
V_1	Input Threshold Voltage	S1 : B		5.5	6	6.4	V	6b
V_{15}	Output Saturation Voltage	V_i = 9 V to 46 V, I_{15} = 5 mA	V_i = 5.4 V S1 : A		0.2	0.4	V	6b
I_1	Input Bias Current	V_1 = 6 V,	S1 : B			10	µA	6b
$-I_{15}$	Output Source Current	V_i = 9 V to 46 V, V_{15} = 2 V	V_1 = 6.5 V S1 : B	70	100		mA	6b

Figure 4 : Dynamic Test Circuit.



C7, C8 : EKR (ROE)
L1 · L = 300 µH at 8 A Core type · MAGNETICS 58930 - A2 MPP
N° turns : 43 Wire Gauge : 1 mm (18 AWG) COGEMA 946044
(*) Minimum suggested value (10 µF) to avoid oscillations Ripple consideration leads to typical value of 1000 µF or higher.

Figure 5 : PC. Board and Component Layout of the Circuit of Figure 4 (1:1 scale).

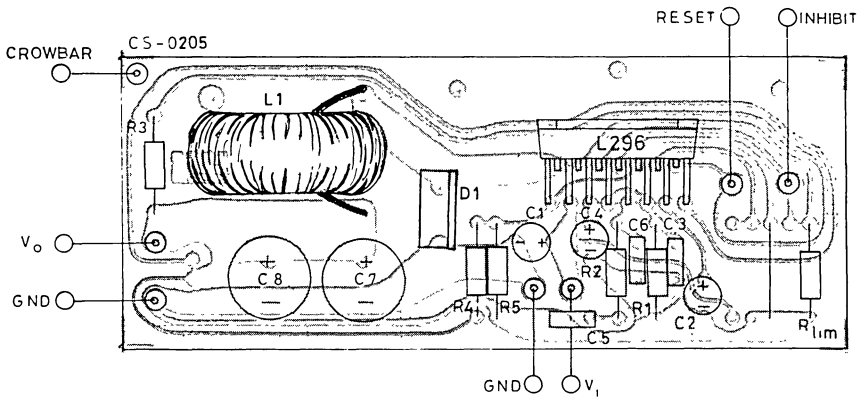


Figure 6 : DC Test Circuits.

Figure 6a.

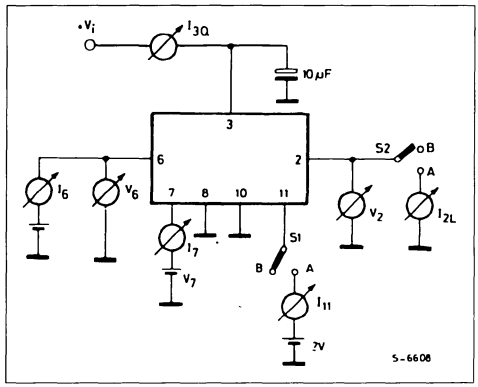


Figure 6b.

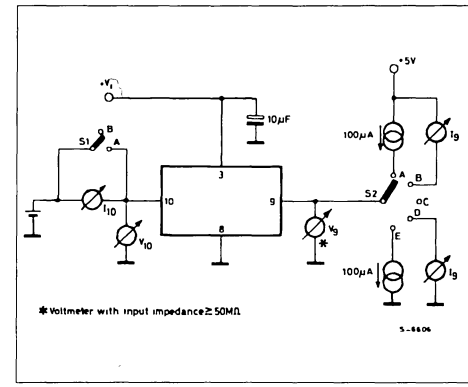


Figure 6c.

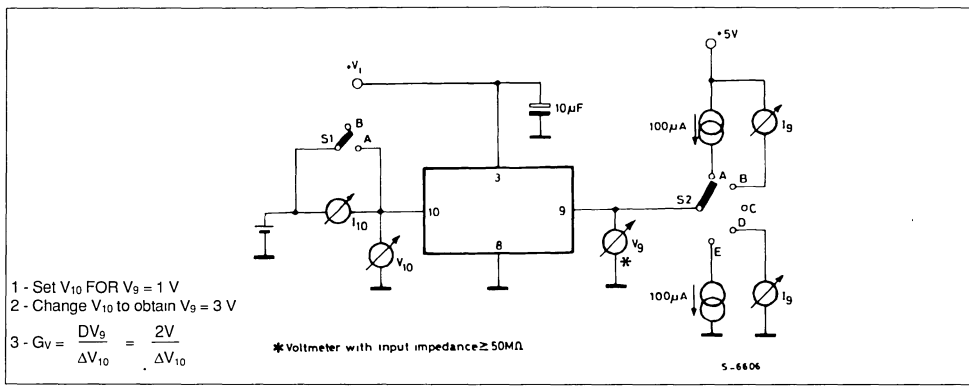


Figure 6d.

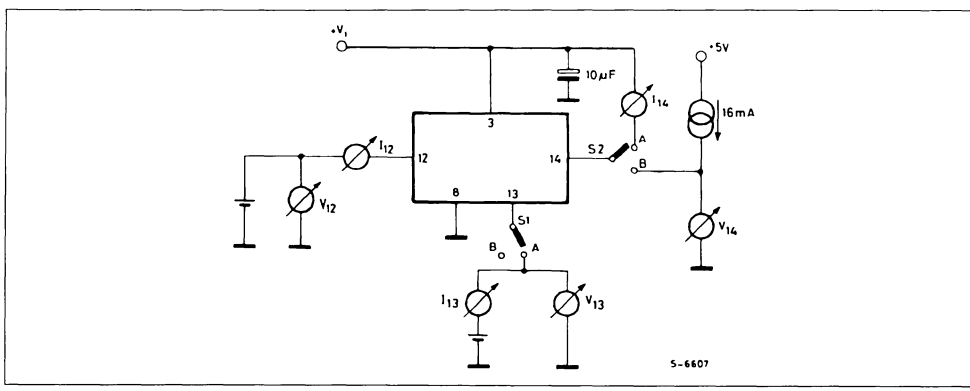


Figure 7 : Quienscent Drain Current vs. Supply Voltage (0 % Duty Cycle - see fig. 6a).

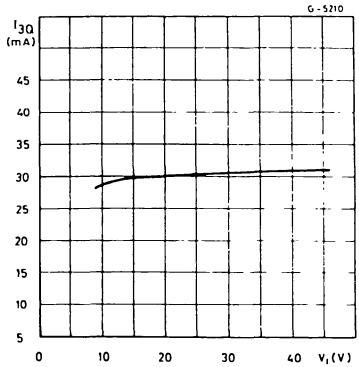


Figure 8 : Quienscent Drain Current vs. Supply Voltage (100 % Duty Cycle see fig. 6a).

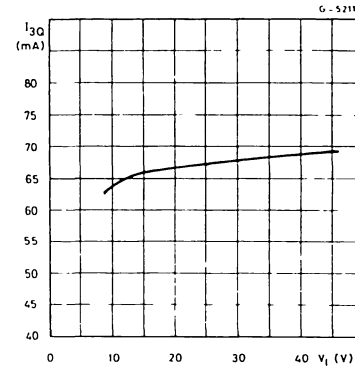


Figure 9 : Quiescent Drain Current vs. Junction Temperature (0 % Duty Cycle - see fig. 6a).

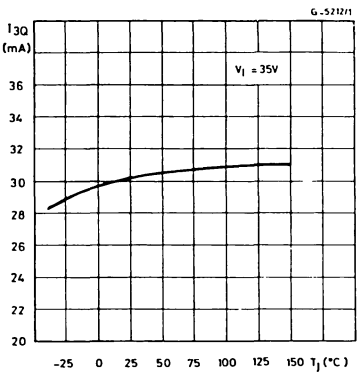


Figure 10 : Quiescent Drain Current vs. Junction Temperature (100 % Duty Cycle - see fig. 6a).

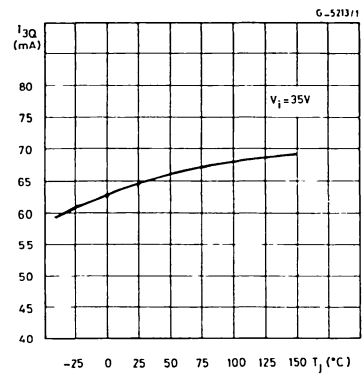


Figure 11 : Reference Voltage (pin 10) vs. V_I (see fig. 4).

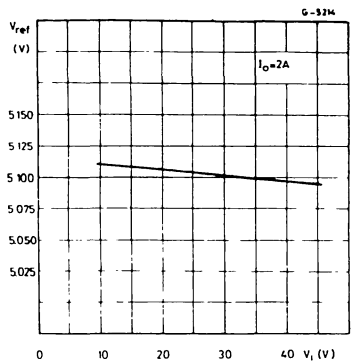


Figure 12 : Reference Voltage (pin 10) vs. Junction Temperature (see fig. 4).

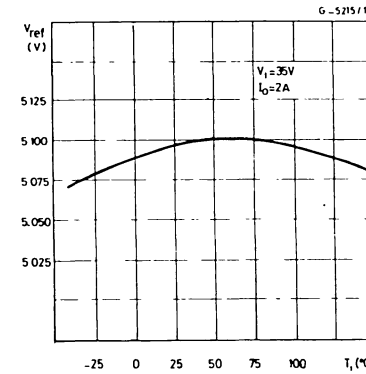


Figure 13 : Open Loop Frequency and Phase Response of Error Amplifier (see fig. 6c).

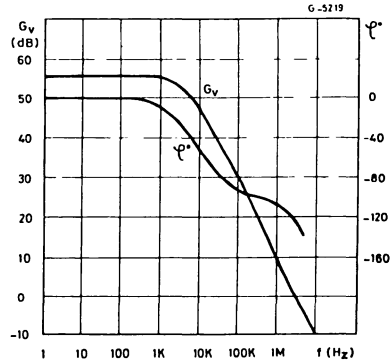


Figure 14 : Switching Frequency vs. Input Voltage (see fig. 4).

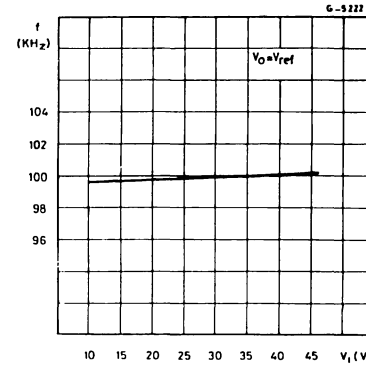


Figure 15 : Switching Frequency vs. Junction Temperature (see fig. 4).

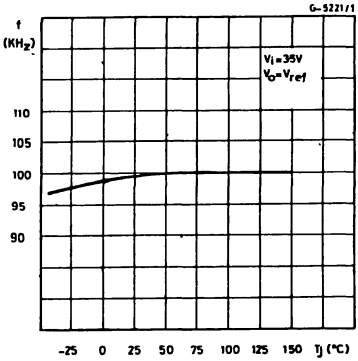


Figure 16 : Switching Frequency vs. R1 (see fig. 4).

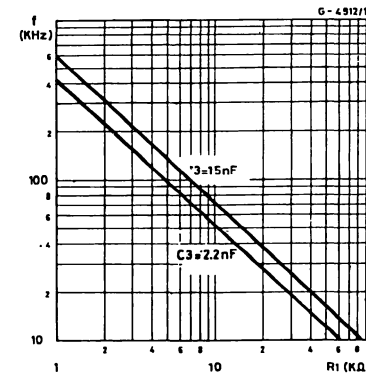


Figure 17 : Line Transient Response (see fig. 4).

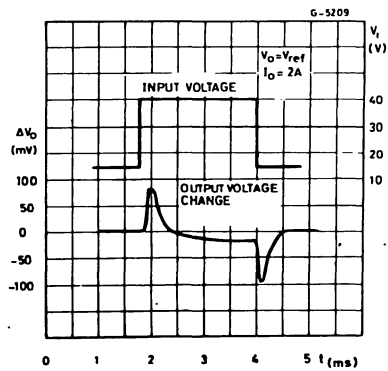


Figure 18 : Load Transient Response (see fig. 4).

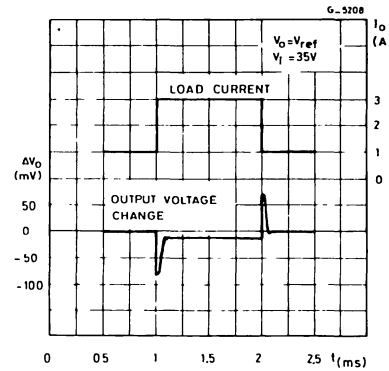


Figure 19 : Supply Voltage Ripple Rejection vs. Frequency (see fig. 4).

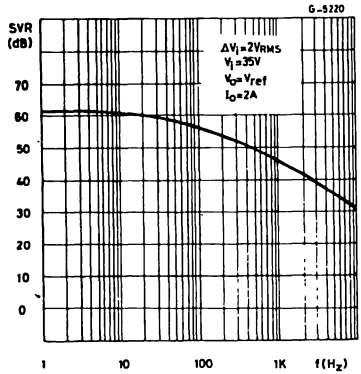


Figure 20 : Dropout Voltage Between Pin 3 and Pin 2 vs. Current at Pin 2.

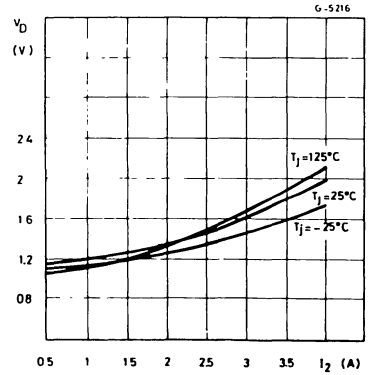


Figure 21 : Dropout Voltage Between Pin 3 and Pin 2 vs. Junction Temperature.

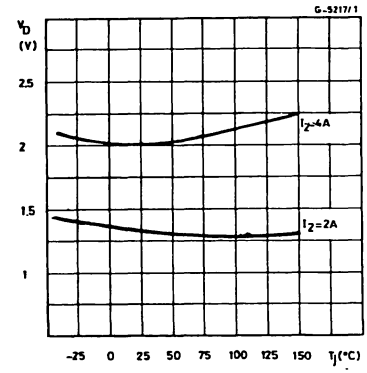


Figure 22 : Power Dissipation Derating Curve.

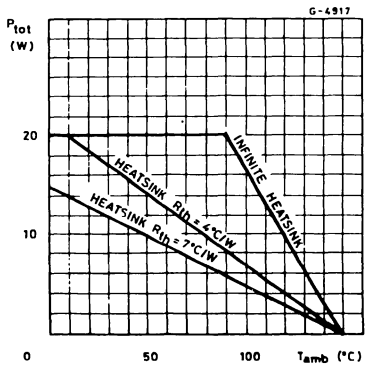


Figure 23 : Power Dissipation (device only) vs. Input Voltage.

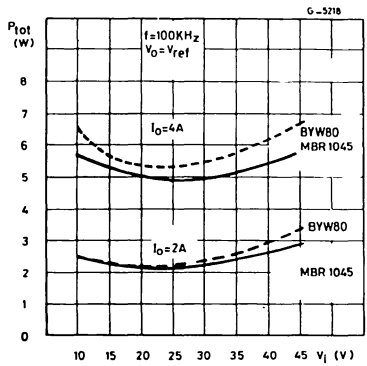


Figure 24 : Power Dissipation (device only) vs. Input voltage.

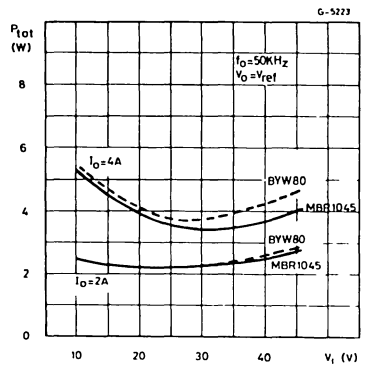


Figure 25 : Power Dissipation (device only) vs. Output Voltage (see fig. 4).

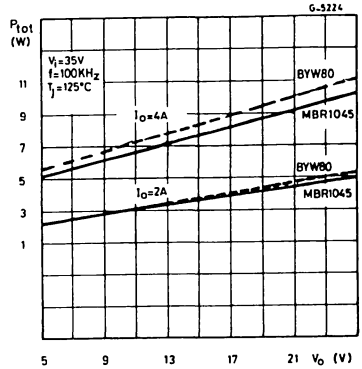


Figure 26 : Power Dissipation (device only) vs. Output Voltage (see fig. 4).

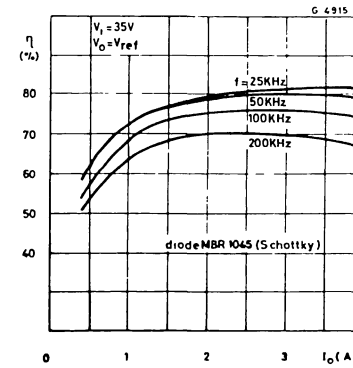


Figure 27 : Voltage and Current Waveforms at Pin 2 (see fig. 4).

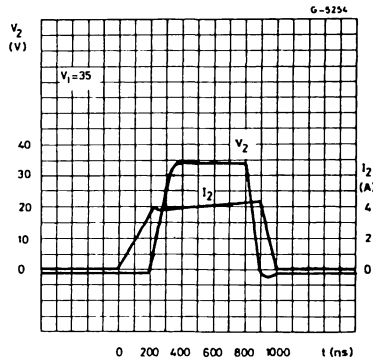


Figure 28 : Efficiency vs. Output Current.

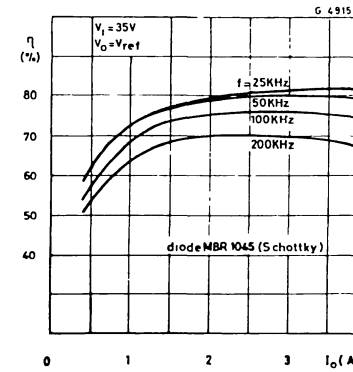


Figure 29 : Efficiency vs. Output Voltage.

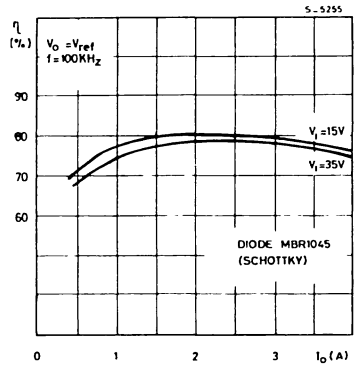


Figure 30 : Efficiency vs. Output Voltage.

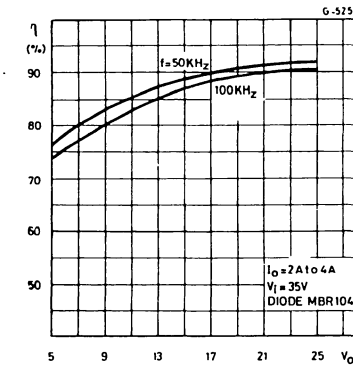


Figure 31 : Current Limiting Threshold vs. $R_{pin\,4}$ (L296P only).

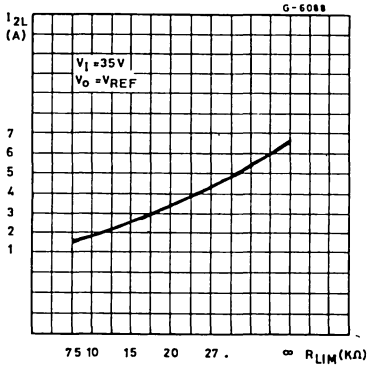


Figure 32 : Current Limiting Threshold vs. Junction Temperature.

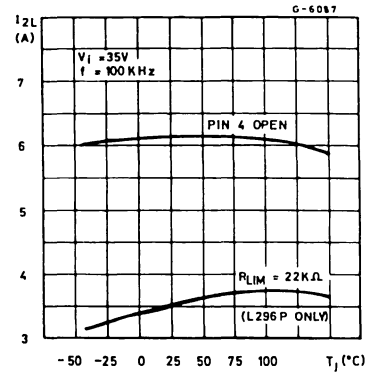
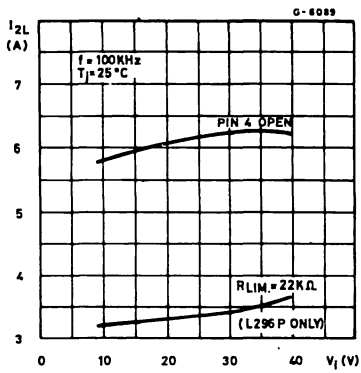
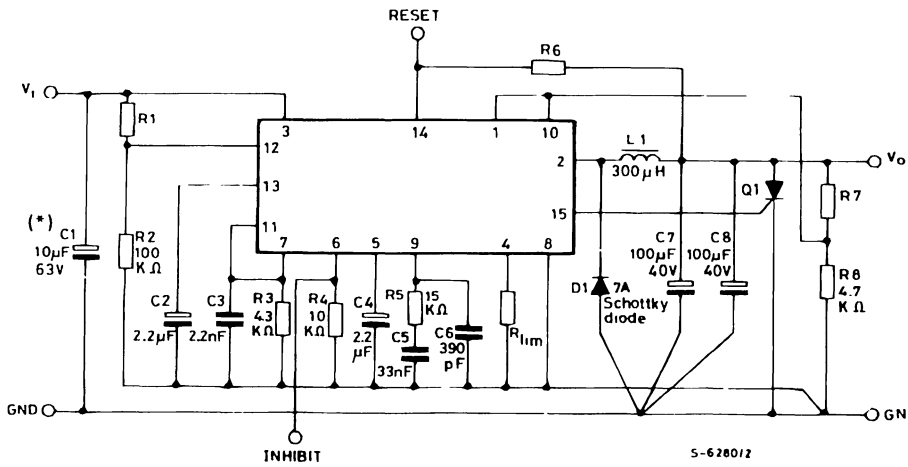


Figure 33 : Current Limiting Threshold vs. Supply Voltage.



APPLICATION INFORMATION

Figure 34 : Typical Application Circuit.



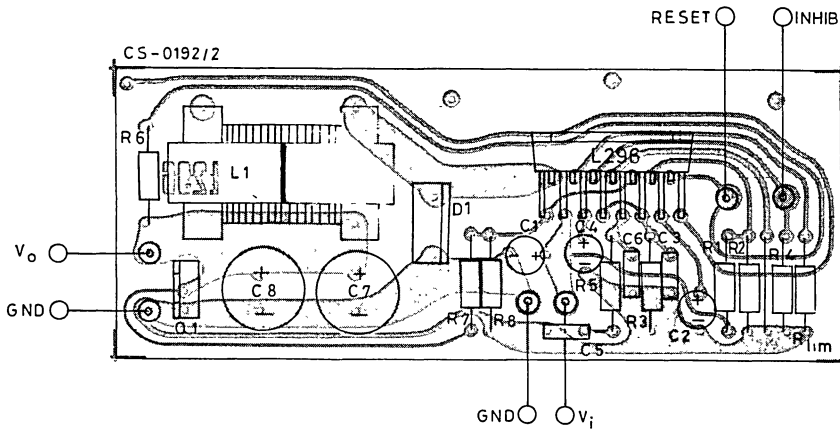
(*) Minimum value (10 µF) to avoid oscillations ; ripple consideration leads to typical value of 1000 µF or higher L1 : 58930 - MPP COGEMA 946044 ; GUP 20 COGEMA 946045

SUGGESTED INDUCTOR (L1)

Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 – A2MPP	43	1.0 mm	–
Thomson GUP 20 x 16 x 7	65	0.8 mm	1 mm
Siemens EC 35/17/10 (B6633& – G0500 – X127)	40	2 x 0.8 mm	–
VOGT 250 µH Toroidal Coil, Part Number 5730501800			

Resistor Values for Standard Output Voltages		
V_0	R8	R7
12 V	4.7 KΩ	6.2 KΩ
15 V	4.7 KΩ	9.1 KΩ
18 V	4.7 KΩ	12 KΩ
24 V	4.7 KΩ	18 KΩ

Figure 35 : P.C. Board and Component Layout of the Circuit of fig. 34 (1:1 scale).



SELECTION OF COMPONENT VALUES (see fig. 34)

Component	Recommended Value	Purpose	Allowed Rage Min.	Allowed Rage Max.	Notes
R1 R2	– 100 kΩ	Set Input Voltage Threshold for Reset.	–	220 kΩ	$R1/R2 = \frac{V_{I\,min}}{5} - 1$ If output voltage is sensed R1 and R2 may be limited and pin 12 connected to pin 10.
R3	4.3 kΩ	Sets Switching Frequency	1 kΩ	100 kΩ	
R4	10 kΩ	Pull-down Resistor		22 kΩ	May be omitted and pin 6 grounded if inhibit not used.
R5	15 kΩ	Frequency Compensation	10 kΩ		
R6		Collector Load For Reset Output	$\frac{V_o}{0.05\ A}$		Omitted if reset function not used.
R7 R8	– 4.7 kΩ	Divider to Set Output Voltage	– –	– 10 kΩ	$R7/R8 = \frac{V_o - V_{ref}}{V_{ref}} -$
R_{lim}	–	Sets Current Limit Level	7.5 kΩ		If R_{lim} is omitted and pin 4 left open the current limit is internally fixed.
C1	10 µF	Stability	2.2 µF		
C2	2.2 µF	Sets Reset Delay	–	–	Omitted if reset function not used.
C3	2.2 nF	Sets Switching Frequency	1 nF	3.3 nF	
C4	2.2 µF	Soft Start	1 µF	–	Also determines average short circuit current.
C5	33 nF	Frequency Compensation			
C6	390 pF	High Frequency Compensation	–	–	Not required for 5 V operation.
C7, C8 L1	100 µF 300 µH	Output Filter	– 100 µH	–	
Q1		Crowbar Protection			The SCR must be able to withstand the peak discharge current of the output capacitor and the short circuit current of the device.
D1		Recirculation Diode			7A Schottky or 35 ns t_{rr} Diode.

Figure 36 : A Minimal 5.1 V Fixed Regulator. Very Few Components are Required.

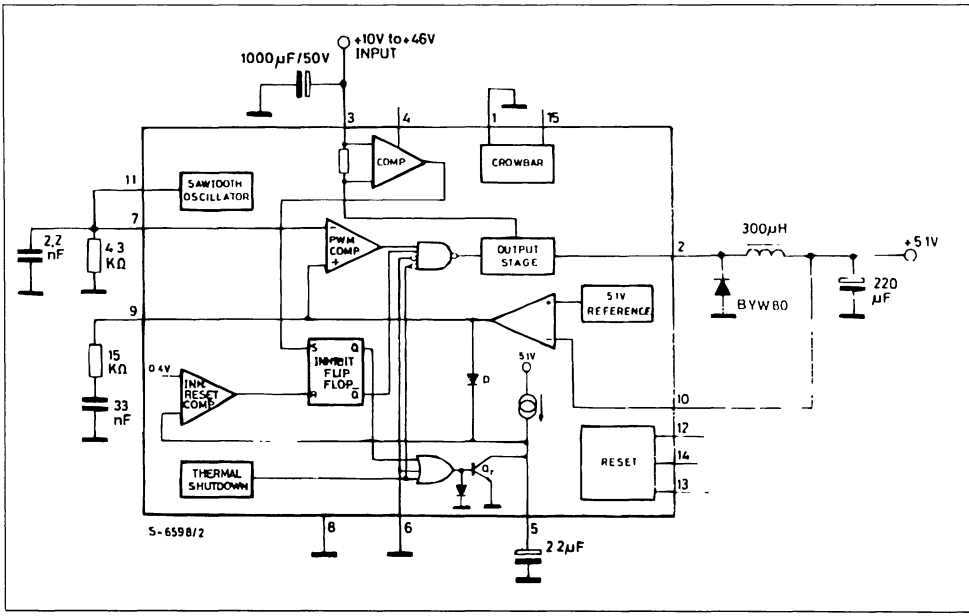


Figure 37 : 12 V/10 A Power Supply.

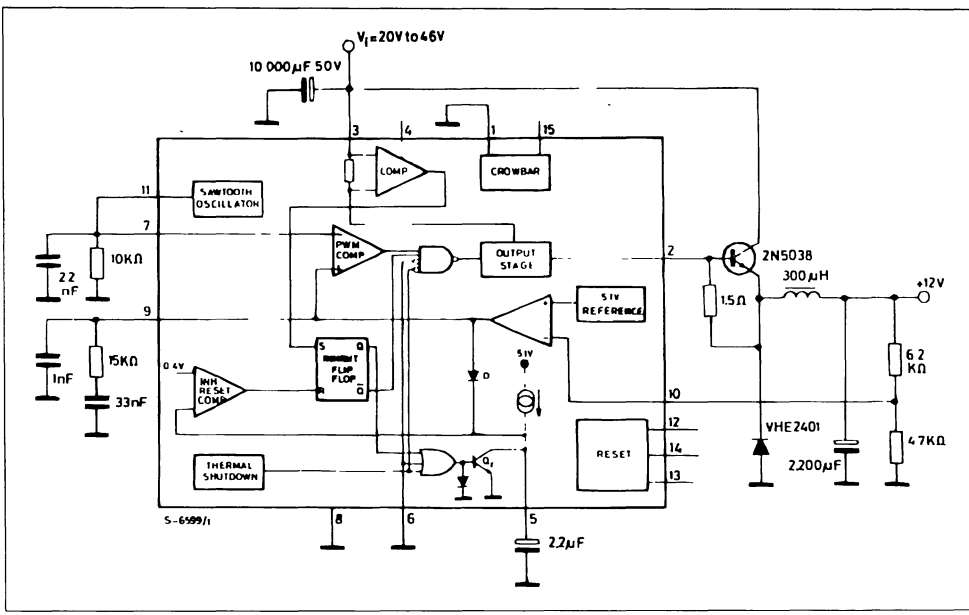
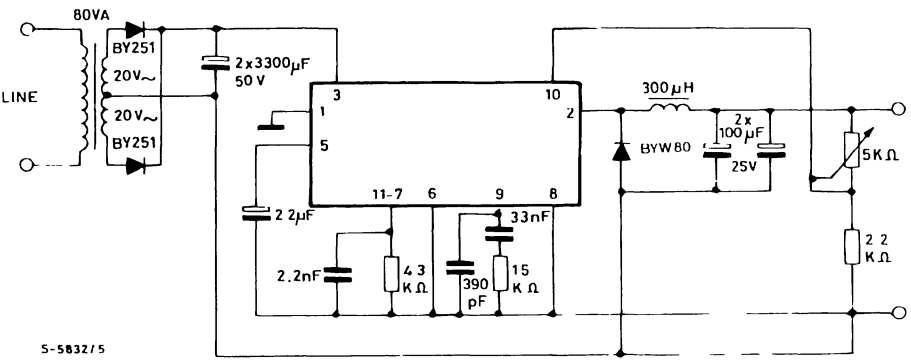
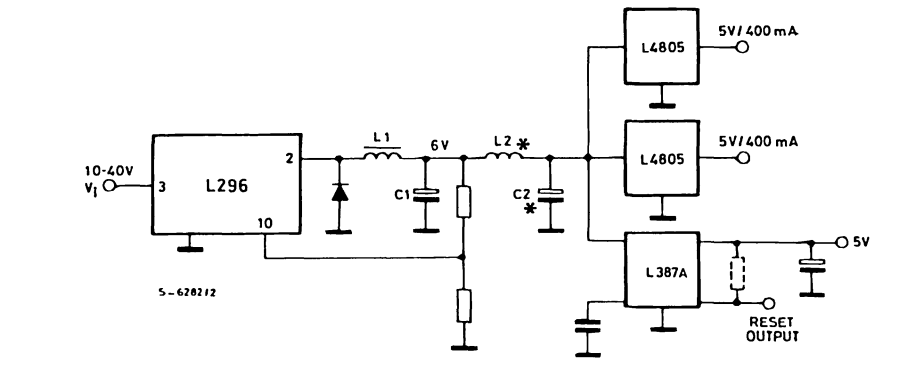


Figure 38 : Programmable Power Supply.



V_o = 5.1 to 15 V
I_o = 4 A max. (min load current = 100 mA)
ripple ≤ 20 mV
load regulation (1 A to 4 A) = 10 mV (V_o = 5.1 V)
line regulation (220 V ± 15 % and to I_o = 3 A) = 15 mV (V_o = 5.1 V)

Figure 39 : Preregulator for Distributed Supplies.



(*) L2 and C2 are necessary to reduce the switching frequency spikes

Figure 40 : In Multiple Supplies Several L296s can be Synchronized As Shown.

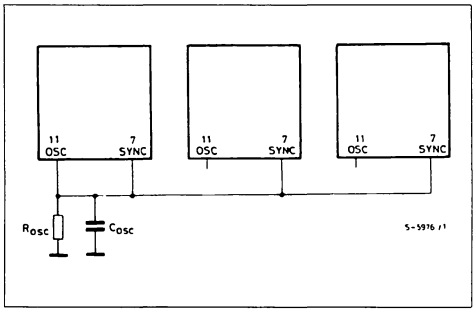


Figure 41 : Voltage Sensing for Remote Load.

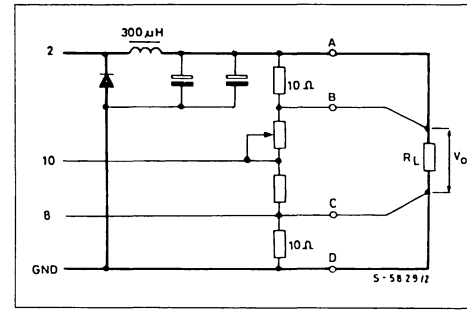


Figure 42 : A 5.1 V/15 V/24 V Multiple Supply. Note the Synchronization of the Three L296s.

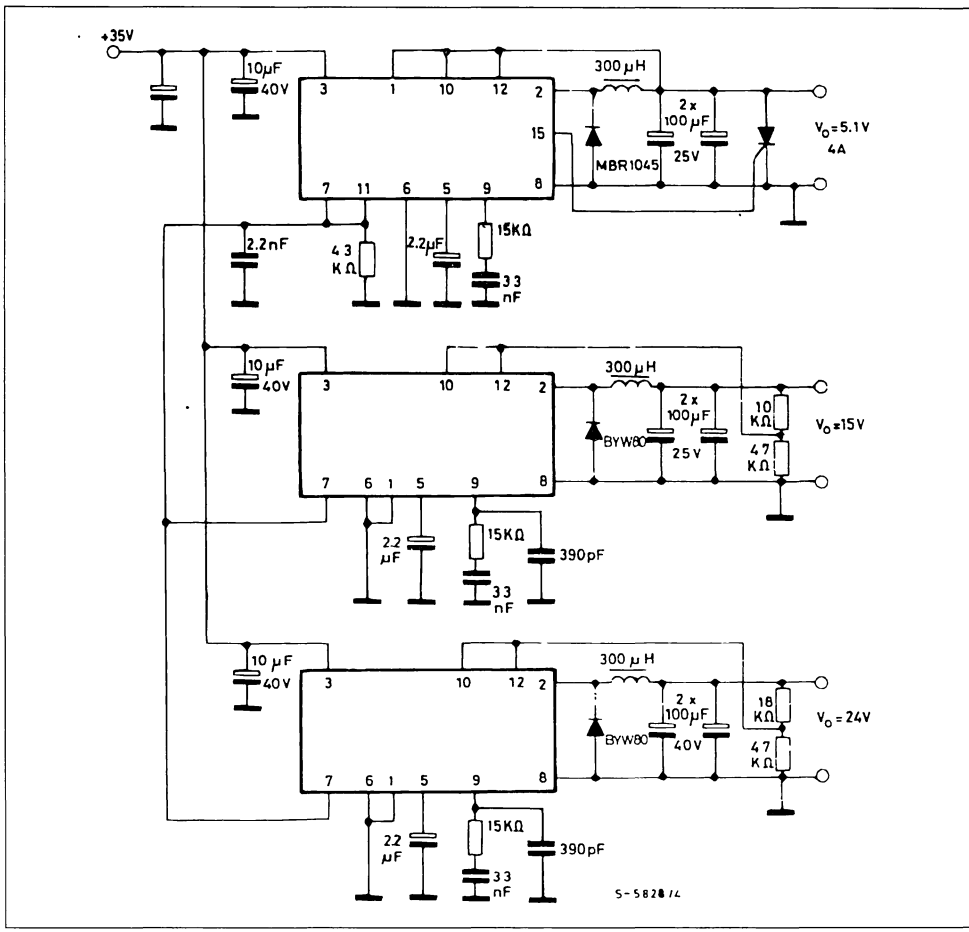
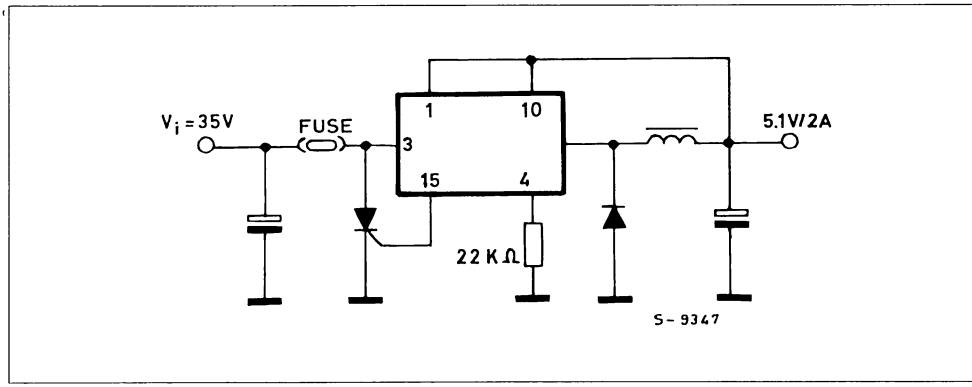


Figure 43 : 5.1 V/2 A Power Supply using External Limiting Current Resistor and Crowbar Protection on the Supply Voltage (L296P only).



SOFT-START AND REPETITIVE POWER-ON

When the device is repetitively powered-on, the soft-start capacitor, C_{SS}, must be discharged rapidly to ensure that each start is "soft". This can be achieved economically using the reset circuit, as shown in Fig. 44.

In this circuit the divider R1, R2 connected to pin 12 determines the minimum supply voltage, below which the open collector transistor at the pin 14 output discharges C_{SS}.

The approximate discharge times obtained with this circuit are :

C_{SS}	t_{DIS}
2.2 µF	200 µs
4.7 µF	300 µs
10 µF	600 µs

If these times are still too long, an external PNP transistor may be added, as shown in Fig. 45 ; with this circuit discharge times of a few microseconds may be obtained.

Figure 44.

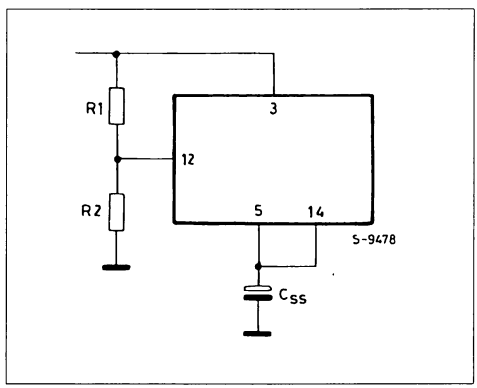
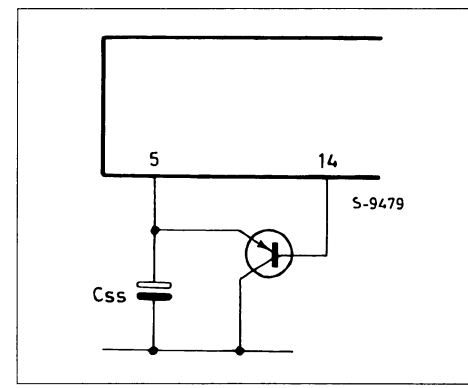


Figure 45.



HOW TO OBTAIN BOTH RESET AND POWER FAIL

Figure 46 illustrates how it is possible to obtain at the same time both the power fail and reset functions simply by adding one diode (D) and one resistor (R).

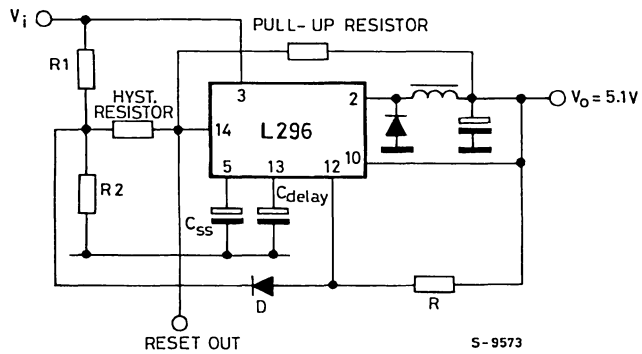
In this case the reset delay time (pin 13) can only start when the output voltage is $V_o \geq V_{REF}$ - 100 mV and the voltage across R2 is higher than 4.5 V.

With the hysteresis resistor it is possible to fix the input pin 12 hysteresis in order to increase immunity to the 100 Hz ripple present on the supply voltage.

Moreover, the power fail and reset delay time are automatically locked to the soft start. Soft start and delayed reset are thus two sequential functions.

The hysteresis resistor should be in the range of about 100 KΩ and the pull-up resistor of 1 to 2.2 KΩ.

Figure 46.



SGS-THOMSON MICROELECTRONICS

L387A

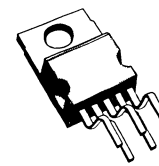
VERY LOW DROP 5V REGULATOR

- PRECISE OUTPUT VOLTAGE (5 V ± 4 %)
- VERY LOW DROPOUT VOLTAGE
- OUTPUT CURRENT IN EXCESS OF 500mA
- POWER-ON, POWER-OFF INFORMATION (RESET FUNCTION)
- HIGH NOISE IMMUNITY ON RESET DELAY CAPACITOR

L387A particularly suitable for microprocessor systems. This output provides a reset signal when power is applied (after an external programmable delay) and goes low when power is removed, inhibiting the microprocessor. An hysteresis on reset delay capacitor raises the immunity to the ground noise.

DESCRIPTION

The L387A is a very low drop voltage regulator in a Pentawatt® package specially designed to provide stabilized 5V supplies in consumer and industrial applications. Thanks to its very low input/output voltage drop this device is very useful in battery powered equipment, reducing consumption and prolonging battery life. A reset output makes the



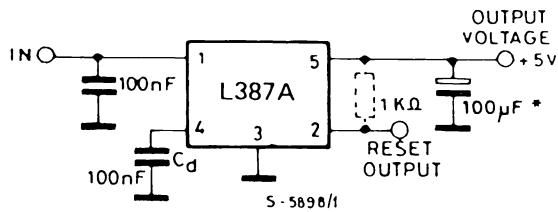
Pentawatt®

ORDER CODE : L387A

ABSOLUTE MAXIMUM RATINGS

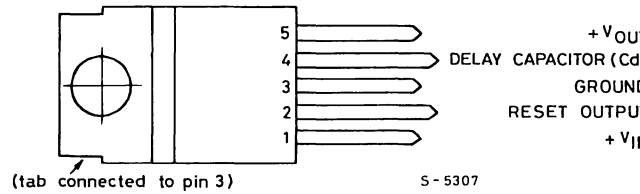
Symbol	Parameter	Value	Unit
V_i	Forward Input Voltage	35	V
T_{op}	Operating Temperature Range	– 40 to + 125	°C
T_{stg}, T_J	Storage and Junction Temperature	– 40 to + 150	°C

APPLICATION CIRCUIT

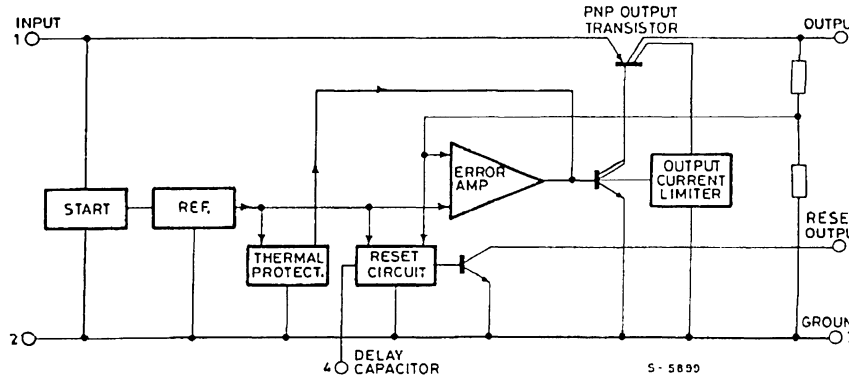


* Min 33 µF and max. ESR ≤ 3 Ω over temperature range.

CONNECTION DIAGRAM (top views)



BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	4	°C/W

ELECTRICAL CHARACTERISTICS (refer to the test circuit, V_i = 14.4 V, T_j = 25 °C, C_o = 100 µF; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 5 mA to 500 mA T_j = 25 °C – 40 ≤ T_j ≤ 125 °C	4.80 4.75	5.00 5.00	5.20 5.25	V
V_I	Operating Input Voltage	(*), Over Full T Range (– 40 to 125 °C) (see note **)			26	V
ΔV_o	Line Regulation	V_i = 6 V to 26 V I_o = 5 mA		5	50	mV
ΔV_o	Load Regulation	I_o = 5 mA to 500 mA		15	60	mV
$V_I - V_o$	Dropout Voltage	I_o = 350 mA I_o = 500 mA $V_O = V_{O\ NOM} - 100$ mV		0.40 0.60	0.65 0.8	V
I_q	Quiescent Current	I_o = 0 mA I_o = 150 mA I_o = 350 mA I_o = 500 mA		5 20 60 100	15 35 100 160	mA
		V_i = 6.2 V I_o = 500 mA		160	180	
$\frac{\Delta V_o}{\Delta T}$	Temperature Output Voltage Drift			– 0.5		mV/°C
SVR	Supply Voltage Rejection	I_o = 350 mA f = 120 Hz C_o = 100 µF V_i = 12 V ± 5 V_{pp}		60		dB
I_{SC}	Output Short Circuit Current			1.2	1.6	A
V_R	Reset Output Voltage	I_R = 3 mA 1 < V_o < 4.75 V I_R = 16 mA 1.5 < V_o < 4.75 V Over Full T (– 40 °C ≤ T_j ≤ 125 °C)			0.5 0.8	V
I_R	Reset Output Leakage Current	V_o in Regulation Over Full T Range			50	µA
t_d	Delay Time for Reset Output	Cd = 100 nF Over Full T Range		25		ms
$V_{RT\ (off)}$		V_o @ Reset out H to L Transition, Over Full T Range	4.75	V_o – 0.15		V
I_{C4}	Charging Current (current generator)	V_4 = 3 V	10	20	30	µA
$V_{RT\ (on)}$	Power on V_oThreshold	V_o @ Reset out L to H Transition , Over Full T Range		$V_{RT\ (off)}$ + 0.05 V	V_o – 0.04 V	V
V_4	Comparator Threshold (pin 4)	V_4 @ Reset out H to L Transition	3.2		3.9	V
		V_4 @ Reset out L to H Transition	3.7		4.3	V
V_H	Hysteresis Voltage	Over Full T Range		450		mV

(*) For a DC voltage 26 < V_I < 35 V the device is not operating.
(**) Design limits are guaranteed (but not 100 % production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Figure 1 : Dropout Voltage vs. Output Current.

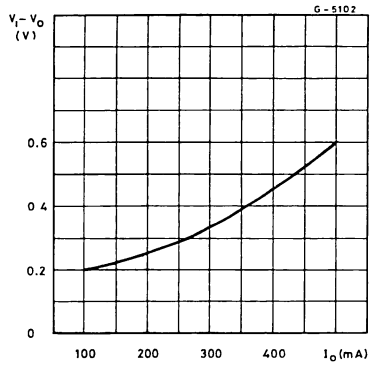


Figure 2 : Quiescent Current vs. Output Current.

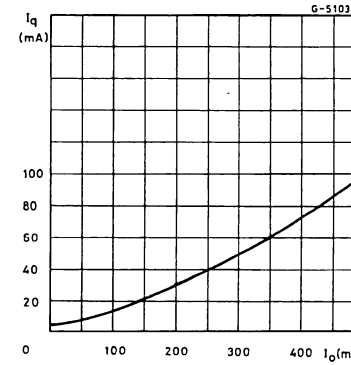
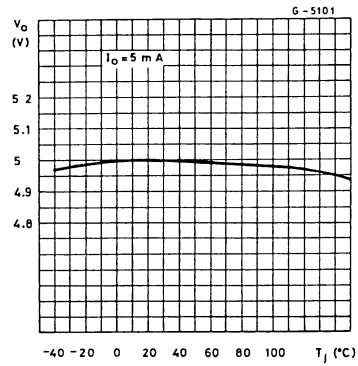


Figure 3 : Output Voltage vs. Temperature.



SGS-THOMSON MICROELECTRONICS

L601-L603
L602-L604

DARLINGTON ARRAYS

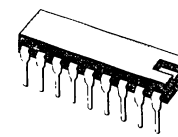
- EIGHT DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 400 mA PER DRIVER (500 mA PEAK)
- OUTPUT VOLTAGE 90 V ($V_{CE\ (sus)}$ = 70 V)
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL / CMOS / PMOS / DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

The four versions interface to all common logic families :

L601	General purpose
L602	14 - 25 V PMOS
L603	5 V TTL, CMOS
L604	6 - 15 V CMOS, PMOS

These versatile devices are useful for driving a wide range of loads, including solenoids, relays DC motors, LED displays, filament lamps, thermal printheads and high power buffers.

The L601, L602, L603 and L604 are supplied in 18 pin plastic DIP packages with a copper leadframe to reduce thermal resistance.



DIP-18
(Plastic)

ORDER CODES : L601C, L603B
L602B, L604B

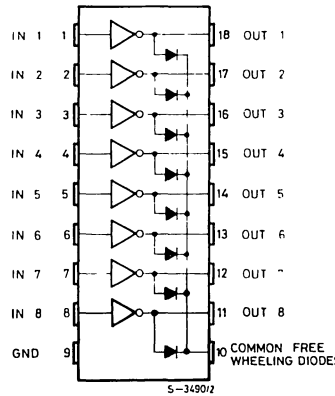
DESCRIPTION

The L601, L602, L603 and L604 are high voltage, high current darlington arrays each containing eight open collector darlington pairs with common emitters. Each channel is rated at 400 mA and can with stand peak currents of 500 mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

ABSOLUTE MAXIMUM RATINGS

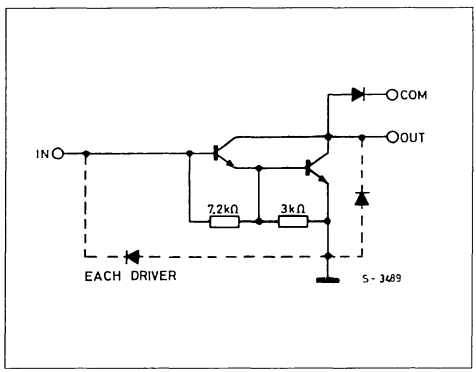
Symbol	Parameter	Value	Unit
V_{CEX}	Collector Emitter Voltage (input open)	90	V
I_C	Collector Current	0.4	A
I_C	Collector Peak Current	0.5	A
V_i	Input Voltage (for L602, L603 and L604)	30	V
I_i	Input Current (for L601 only)	25	mA
P_{tot}	Total Power Dissipation a T_{amb} = 25°C	1.8	W
T_{op}	Operating Junction Temperature	– 25 to 150	°C

PIN CONNECTIONS (top view)

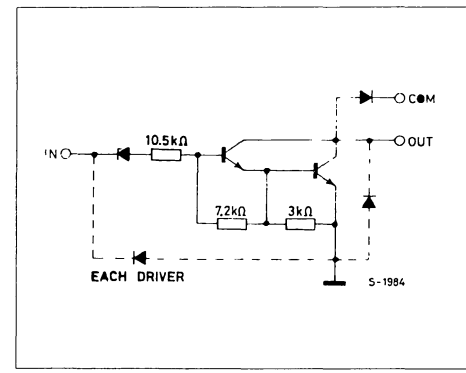


SCHEMATIC DIAGRAMS

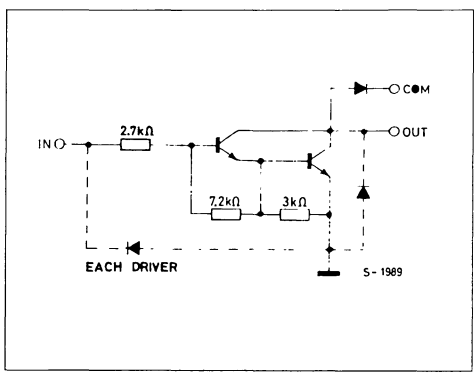
L601



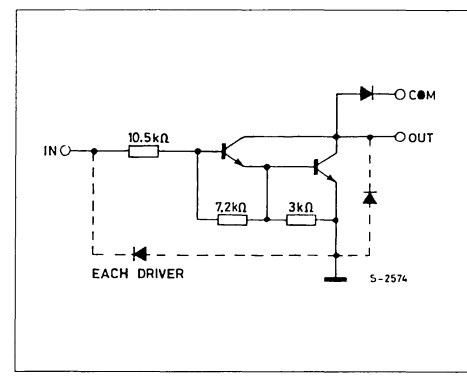
L602



L603



L604



THERMAL DATA

$R_{th\,j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	70	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

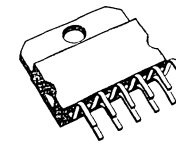
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CEX}	Output Leakage Current	V_{CE} = 90 V			10	µA
$V_{CE(sat)}$	Collector Emitter Saturation Voltage	I_C = 300 mA I_B = 500 µA I_C = 200 mA I_B = 350 µA I_C = 100 mA I_B = 250 µA			2 1.7 1.2	V V V
h_{FE}	DC Forward Current Gain (L601 only)	V_{CE} = 3 V I_C = 300 mA	1000			–
V_i	Minimum Input Voltage (ON condition)	V_{CE} = 3 V I_C = 300 mA for L602 for L603 for L604			 11.5 2.5 5	 V V V
V_i	Maximum Input Voltage (OFF condition)	V_{CE} = 90 V I_C = 25 µA for L601 for L602 for L603 for L604	 0.55 7 0.75 1			 V V V V
I_R	Clamp Diode Reverse Current	V_R = 90 V			50	µA
V_F	Clamp Diode Forward Voltage	I_F = 300 mA		2	2.4	V
t_{on}	Turn-on Delay	0.5 V_i to 0.5 V_o		0.4		µs
t_{off}	Turn-off Delay	0.5 V_i to 0.5 V_o		0.4		µs

SGS-THOMSON MICROELECTRONICS

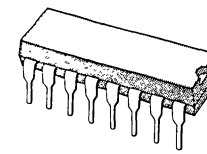
L702

2A QUAD DARLINGTON SWITCH

- SUSTAINING VOLTAGE : 70 V
- 2 A OUTPUT
- HIGH CURRENT GAIN
- IDEAL FOR DRIVING SOLENOIDS, DC MOTORS, STEPPER MOTORS, RELAYS, DISPLAYS, ETC.



Multiwatt-11



Powerdip 8 + 8

ORDER CODES : L702B - Powerdip
L702N - Multiwatt

DESCRIPTION

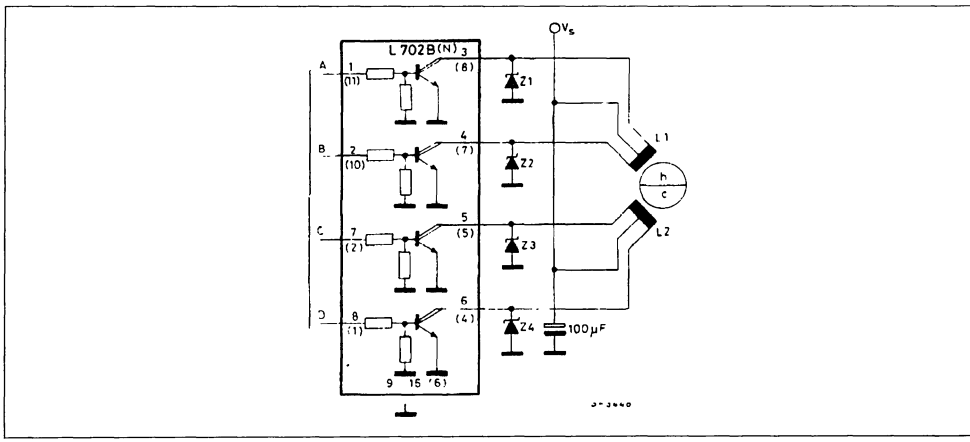
The L702 is a monolithic integrated circuit for high current and high voltage switching applications. It comprises four darlington transistors with common emitter and open collector suitable for current sinking applications mounted on the new POWERDIP and Multiwatt® packages.

This circuit reduces components, sizes and costs ; it can provide direct interface between low level logic and a variety of high current applications.

ABSOLUTE MAXIMUM RATINGS

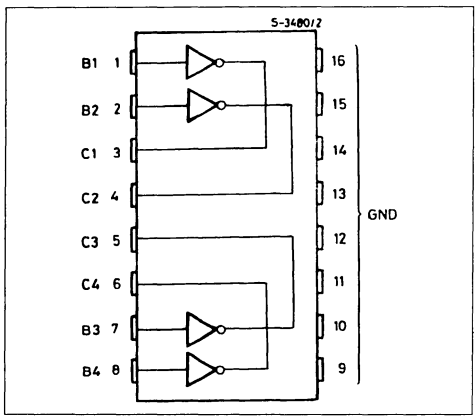
Symbol	Parameter		Value	Unit
V_{CEX}	Collector-emitter Voltage (input open)		90	V
V_i	Input Voltage		30	V
I_C	Collector Current		3	A
P_{tot}	Total Power Dissipation at T_{pin} 9 to 16 ≤ 90 °C	Powerdip	4	W
	Total Power Dissipation at T_{amb} ≤ 70 °C	Powerdip	1.1	W
	Total Power Dissipation at T_{case} ≤ 90 °C	Multiwatt	20	W
T_{stg}	Storage Temperature		– 55 to 150	°C
T_j	Operating Junction Temperature		– 25 to 150	°C

STEPPING MOTOR BUFFER

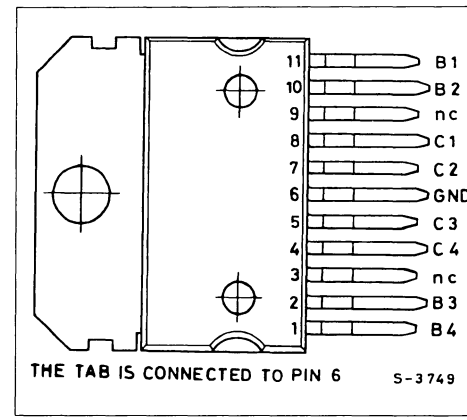


CONNECTION DIAGRAMS (top view)

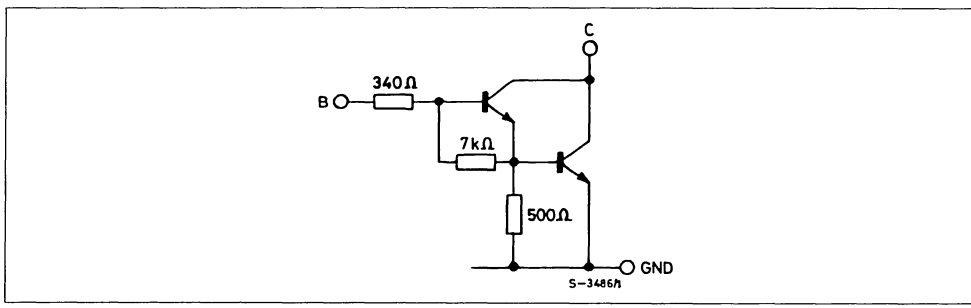
Powerdip



Multiwatt



SCHEMATIC DIAGRAM (each Darlington)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction Ambient	} Powerdip	Max	70	°C/W
$R_{th\ j\text{-}pins\ 9/16}$	Thermal Resistance Junction Pins 9 to 16		Max	14	°C/W
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Multiwatt	Max	3	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Symbol	Parameter		Test conditions		Min.	Typ.	Max.	Unit
I_{CEX}	Output Leakage Current		V_{CE} = 90 V			10	50	µA
$V_{CE(sust)}$	Collector Emitter (*) Sustaining Voltage		I_C = 100 mA		70			V
$V_{CE(sat)}$	Collector Emitter Saturation Voltage		I_C = 1.25 A I_i = 2 mA			1.3	1.9	V
h_{FE}	DC Forward Current Gain		I_C = 1 A V_{CE} = 3 V		1 000	4 000		
I_i	Input Current		V_i = 3.75 V V_i = 2.4 V Open Collector			7 3	11 6	mA mA
V_i	Input Voltage	Off Condition	V_{CE} = 70 V	$I_C \leq$ 0.1 mA			0.4	V
		On Condition	V_{CE} = 3 V	$I_C \geq$ 1 A	2.4			V
T_{on}	Turn On Time		V_s = 12 V			0.3		µs
T_{off}	Turn Off Time		R_L = 10 Ω			1		µs

Figure 1 : Switching Time.

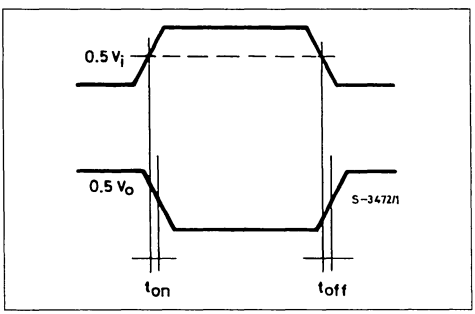


Figure 2 : t_{on} and t_{off} Test Circuit.

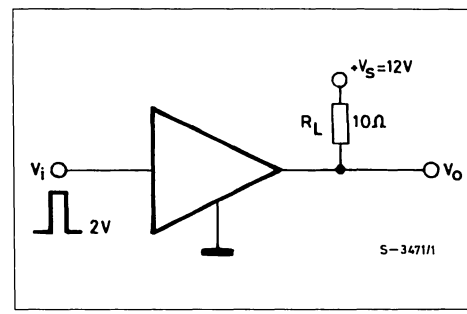


Figure 3 : Peak Collector Current vs. Duty Cycle and Number of Outputs (L702B only).

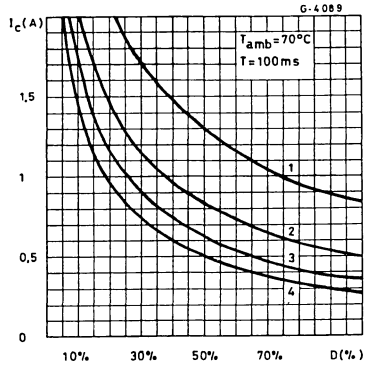


Figure 4 : Collector Emitter Saturation Voltage vs. Collector Current.

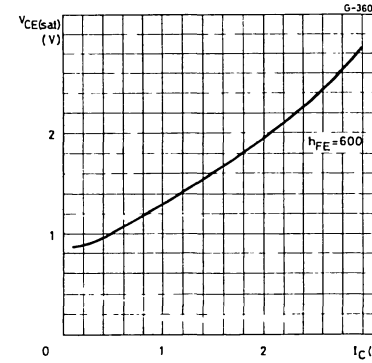


Figure 5 : Collector Current vs. Input Voltage.

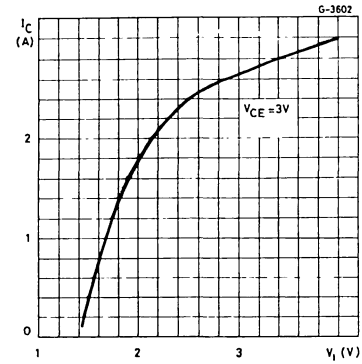


Figure 6 : Input Current vs. Input Voltage.

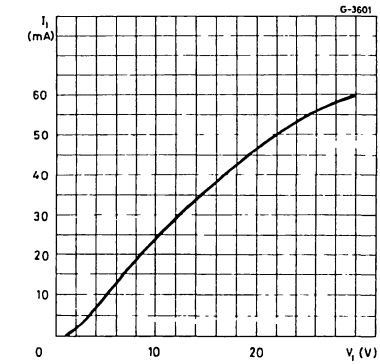


Figure 7 : Safe Operating Areas (L702B).

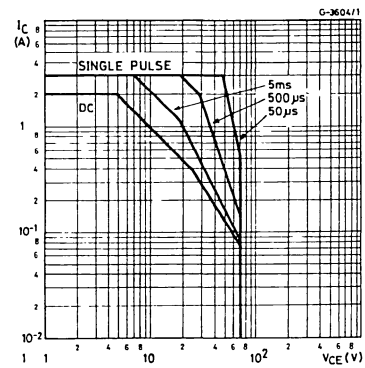
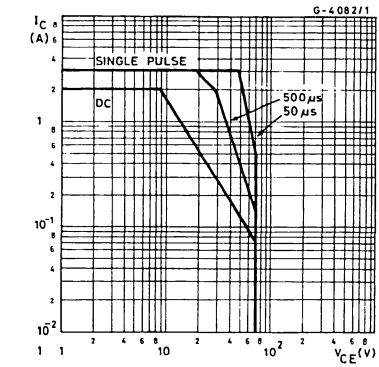


Figure 8 : Safe Operating Areas (L702N).



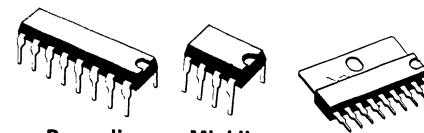
LOW DROP DUAL POWER OPERATIONAL AMPLIFIERS

PRELIMINARY DATA

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- LOW INPUT OFFSET VOLTAGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN
- CLAMP DIODE

The L2720, L2722 and L2724 are monolithic integrated circuits in powerdip, minidip and SIP-9 packages, intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies. They are particularly indicated for driving, inductive loads, as motor and finds applications in compact-disc VCR automotive, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



Powerdip (8 + 8) | **Minidip Plastic** | **SIP-9**

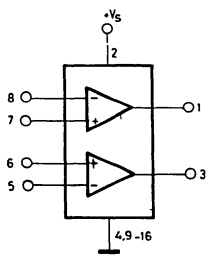
ORDERING NUMBERS:

L2720 L2722 L2724

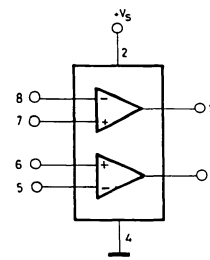
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
V_s	Peak supply voltage (50ms)	50	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at T_{amb} = 80°C (**L2720**), T_{amb} = 50°C (**L2722**)	1	W
	T_{case} = 75°C (**L2720**)	5	W
	T_{case} = 50°C (**L2724**)	10	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

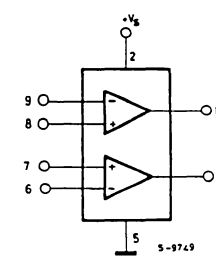
BLOCK DIAGRAMS



L2720

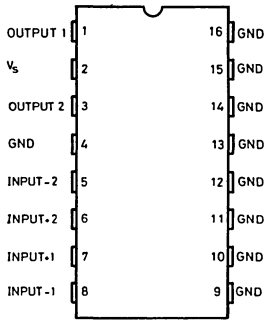


L2722

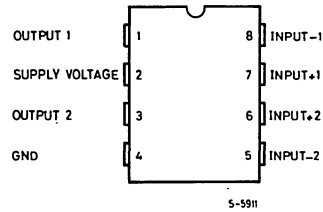


L2724

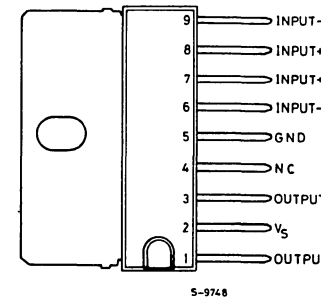
CONNECTION DIAGRAMS
(Top view)



L2720

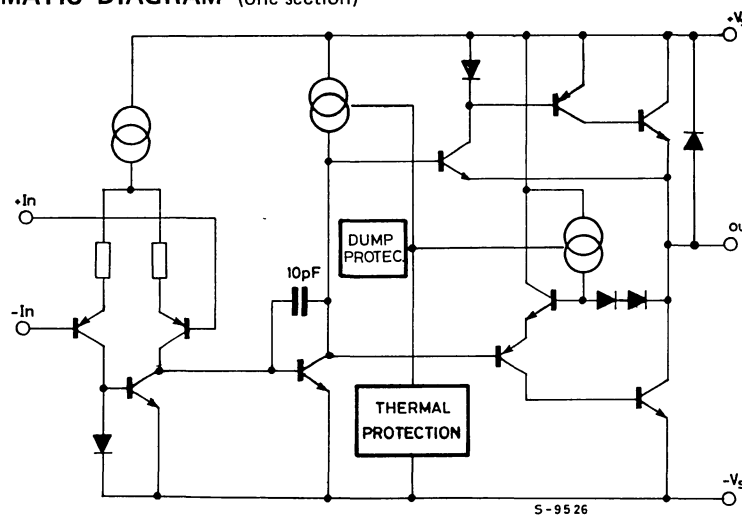


L2722



L2724

SCHEMATIC DIAGRAM (one section)



THERMAL DATA

			SIP-9	Powerdip	Minidip
$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max	10°C/W	15°C/W	*70°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-albient	max	70°C/W	70°C/W	100°C/W

* Thermal resistance junction-pin 4.

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Single supply voltage			4		28	V
V_s	Split supply voltage			± 2		± 14	V
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$	V_s = 24V		10	15	mA
			V_s = 8V		9	15	mA
I_b	Input bias current				0.2	1	µA
V_{os}	Input offset voltage					10	mV
I_{os}	Input offset current					100	nA
SR	Slew rate				2		V/µs
B	Gain-bandwidth product				1.2		MHz
R_i	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		70	80		dB
		f = 1KHz			60		dB
e_N	Input noise voltage	B = 22Hz to 22KHz			10		µV
I_N	Input noise current				200		pA
CMR	Common Mode rejection	f = 1KHz		66	84		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	60	70 75 80		dB dB dB
$V_{DROP\ (HIGH)}$		V_s = ±2.5V to ±12V	I_p = 100mA		0.7		V
			I_p = 500mA		1.0	1.5	V
$V_{DROP\ (LOW)}$			I_p = 100mA		0.3		V
			I_p = 500mA		0.5	1.0	V
C_s	Channel separation	f = 1KHz R_L = 10Ω G_v = 30dB	V_s = 24V V_s = 6V		60 60		dB
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

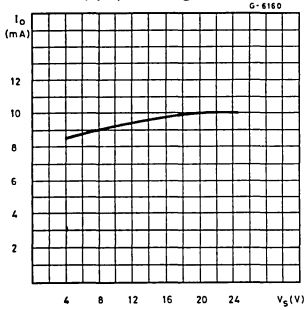


Fig. 2 - Open loop gain vs. frequency

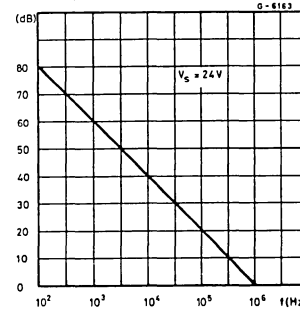


Fig. 3 - Common mode rejection vs. frequency

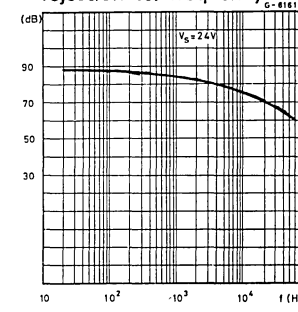


Fig. 4 - Output swing vs. load current (V_S = ± 5V)

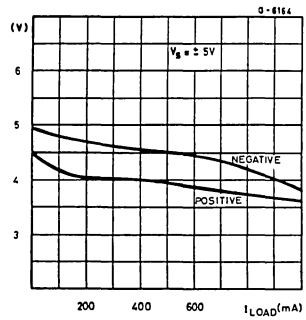


Fig. 5 - Output swing vs. load current (V_S = ± 12V)

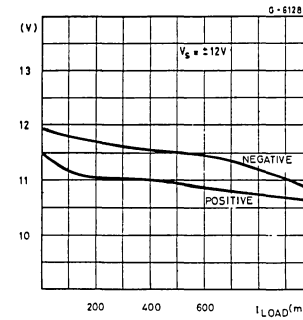


Fig. 6 - Supply voltage rejection vs. frequency

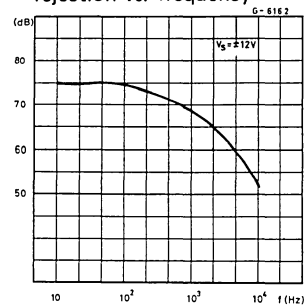
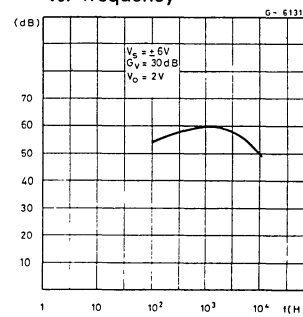


Fig. 7 - Channel separation vs. frequency

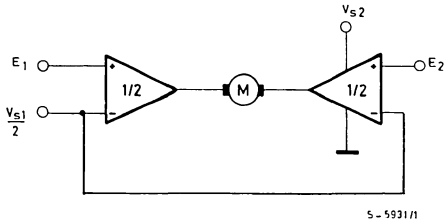


APPLICATION SUGGESTION

In order to avoid possible instability occurring into final stage the usual suggestions for the linear power stages are useful, as for instance:

- layout accuracy;
- A 100nF capacitor connected between supply pins and ground;
- boucherot cell (0.1 to 0.2 μF + 1Ω series) between outputs and ground or across the load. With single supply operation, a resistor (1KΩ) between the output and supply pin can be necessary for stability.

Fig. 8 - Bidirectional DC motor control with μP compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} > V_{S1}$

E1, E2 = logic inputs

Fig. 9 - Servocontrol for compact-disc

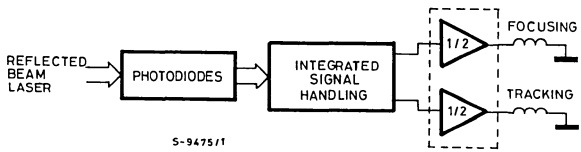


Fig. 10 - Capstan motor control in video recorders

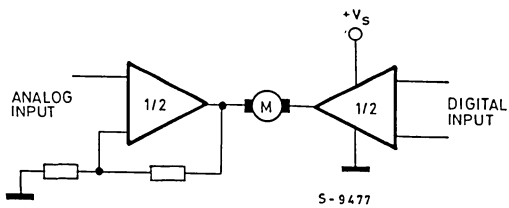
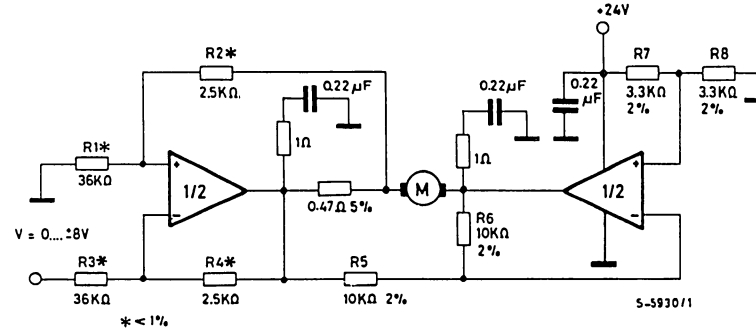


Fig. 11 - Motor current control circuit



Note: The input voltage level is compatible with L291 (5-BIT D/A converter)

Fig. 12 - Bidirectional speed control of DC motors.

For circuit stability ensure that $R_X > \frac{2R3 \circ R1}{R_M}$ where R_M = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2\left(V_I - \frac{V_s}{2}\right) + |R_o|. I_M$ where $|R_o| = \frac{2R \circ R1}{R_X}$ and I_M is the motor current.

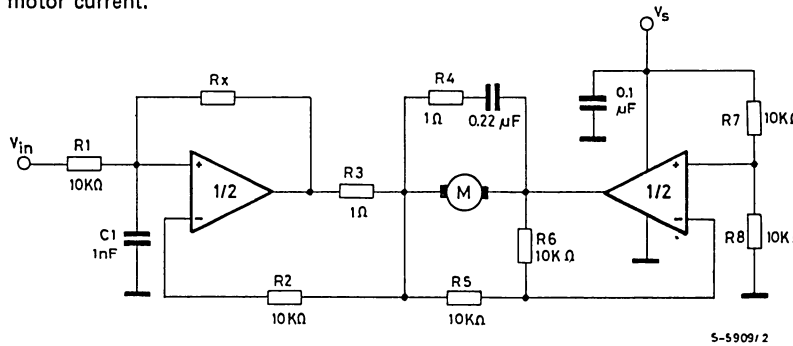
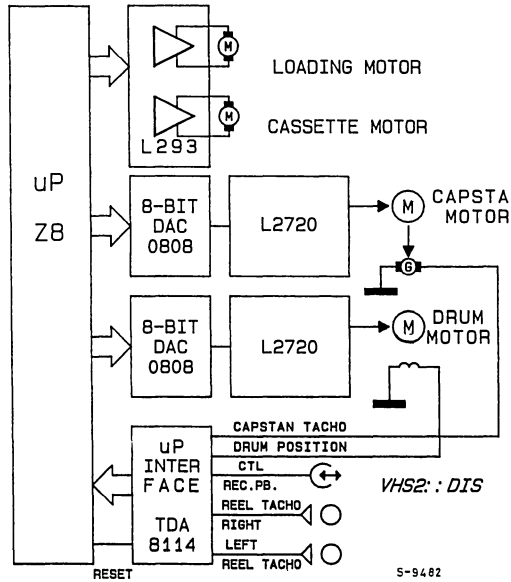


Fig. 13 - VHS-VCR Motor control circuit



SGS-THOMSON MICROELECTRONICS

L4901A

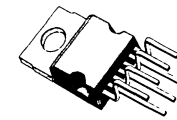
DUAL 5V REGULATOR WITH RESET

PRELIMINARY DATA

- OUTPUT CURRENTS: I_{01} = 400mA
  I_{02} = 400mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4901A is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.



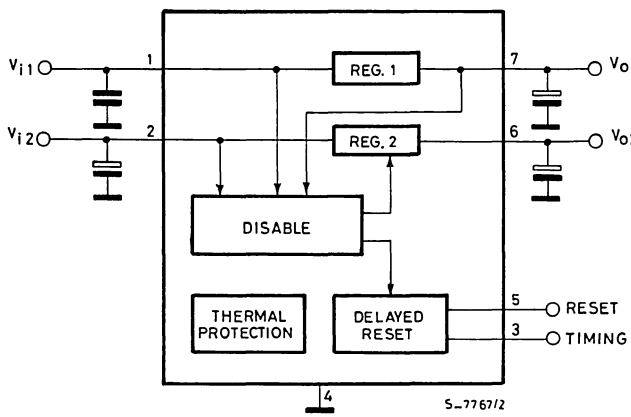
Heptawatt

ORDERING NUMBER: L4901A

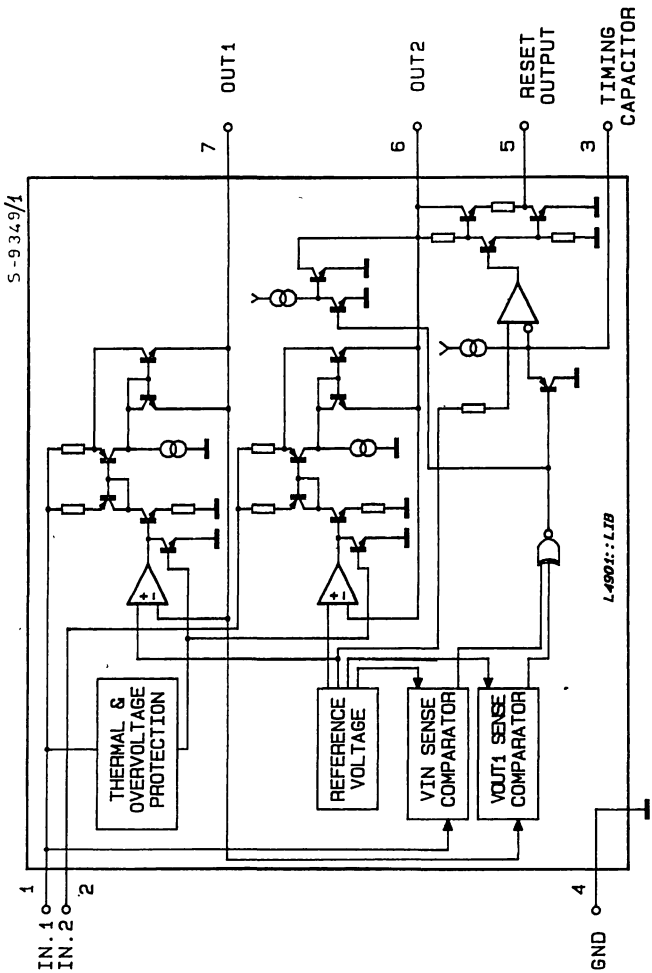
BSOLUTE MAXIMUM RATINGS

IN	DC input voltage	24	V
	Transient input overvoltage (t = 40 ms)	60	V
I_o	Output current	internally limited	
j	Storage and junction temperature	-40 to 150	°C

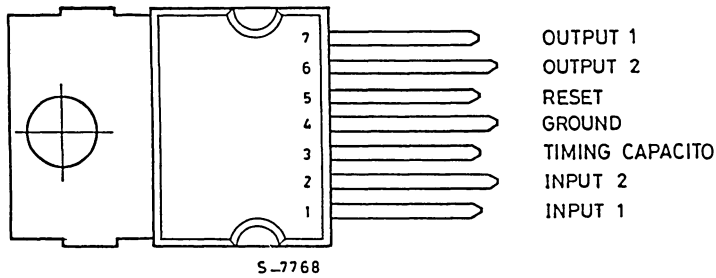
LOCK DIAGRAM



SCHEMATIC DIAGRAM



ONNECTION DIAGRAM
op view)



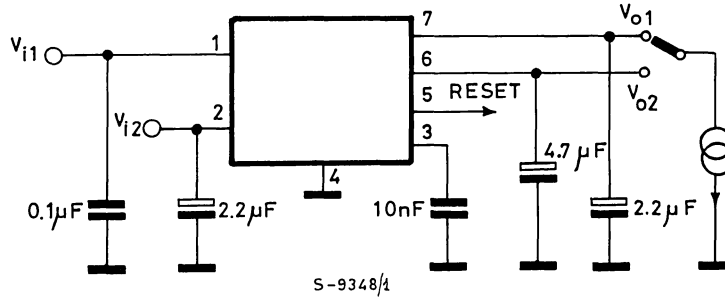
IN FUNCTIONS

NAME	FUNCTION
INPUT 1	Low quiescent current 400mA regulator input.
INPUT 2	400mA regulator input.
TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
GND	Common ground.
RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A}\right)$; t_{RD} (ms) = C_t (nF)
OUTPUT 2	5V - 400mA regulator output. Enabled if $V_O 1 > V_{RT}$ and $V_{IN2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
OUTPUT 1	5V - 400mA regulator output with low leakage (in switch-OFF condition).

HERMAL DATA

th j-case	Thermal resistance junction-case	max	4	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS ($V_{IN1} = V_{IN2} = 14,4V$, $T_{amb} = 25°C$ unless otherwise specified)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1	ΔV_{01} = -100mV	400			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq 3V$			1	µA
I_{02}	Output current 2	ΔV_{02} = -100mV	400			mA
V_{i01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 100mA I_{01} = 300mA		0.7 0.8 1.1	0.8 1 1.4	V V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.7	V
V_{ITH}	Input threshold voltage hyst.			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 18V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	5mA < I_{01} < 400mA		50	100	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 400mA		50	100	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V I_{02} = $I_{01} \leq$ 5mA		4.5 1.6	6.5 3.5	mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 $I_{01} \leq$ 5mA I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3	5	11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	-20°C ⩽ T_{amb} ⩽ 125°C		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	-20°C ⩽ T_{amb} ⩽ 125°C		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 100mA	50	84		dB
SVR2	Supply voltage rejection		50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4901A makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:

- an input overvoltage
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator;
- very low drop series regulator element utilizing current mirrors;

permit high output impedance and then very low leakage current error even in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{01}

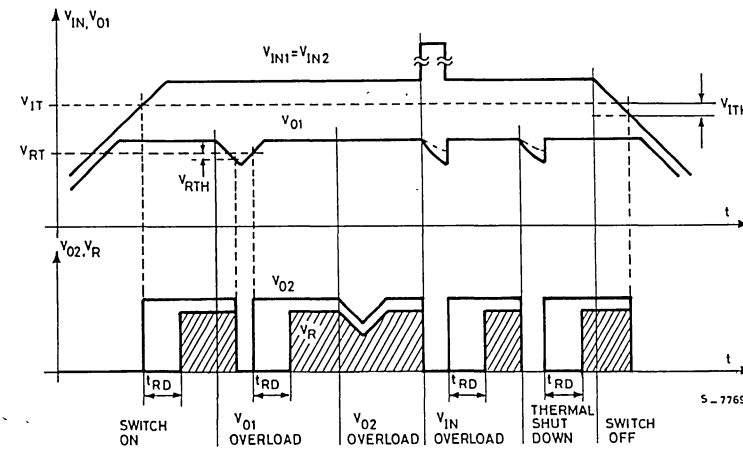
CIRCUIT OPERATION (continued)

regulator also features low consumption (0.6mA typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

Fig. 1



APPLICATION SUGGESTIONS

Fig. 2 shows an application circuit for a μP system typically used in trip computers or in car radios with programmable tuning.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Fig. 4 shows the L4901A with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type N-MOS μP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

The L4901A is also ideal for microcomputer systems using battery backup CMOS static RAMs. As shown in fig. 5 the reset output is used both to disable the μP and, through the address decoder M74HC138, to ensure that the RAMS are disabled as soon as the main supply starts to fall.

Another interesting application of the L4901A is in μP system with shadow memories. (see fig. 6)

When the input voltage goes below V_{IT}, the reset output enables the execution of a routine that saves the machine's state in the shadow RAM (xicor x 2201 for example).

Thanks to the low consumption of the Reg. 1 a 680μF capacitor on its input is sufficient to provide enough energy to complete the operation. The diode on the input guarantees the supply of the equipment even if a short circuit on V_1 occurs.

APPLICATION SUGGESTION (continued)

Fig. 2

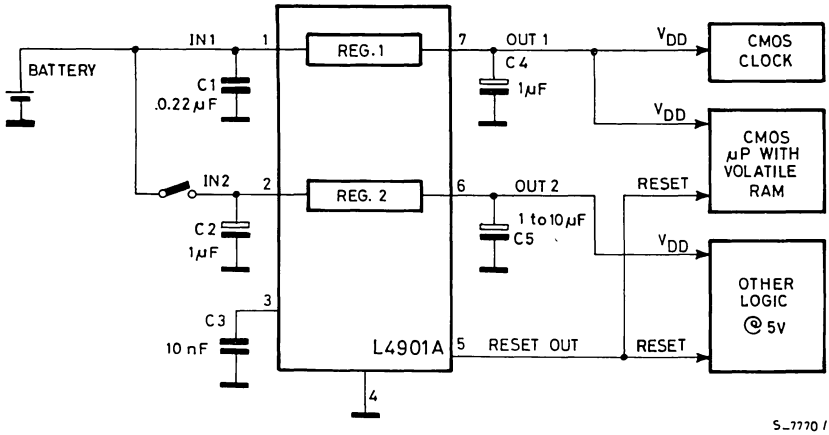
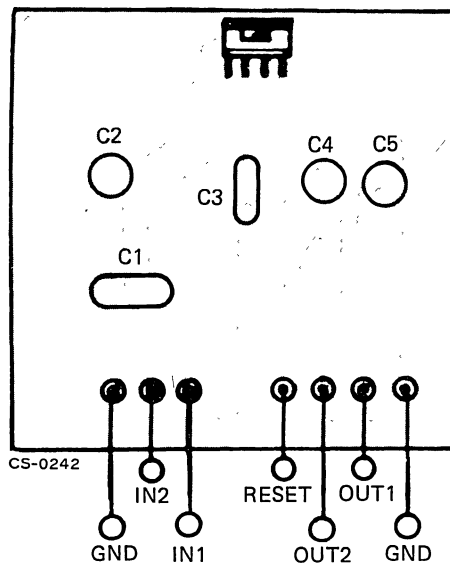


Fig. 3 - P.C. board component layout of fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 4

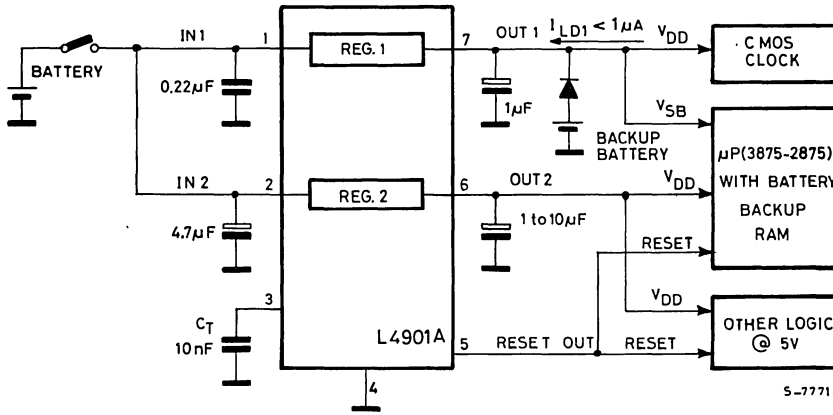
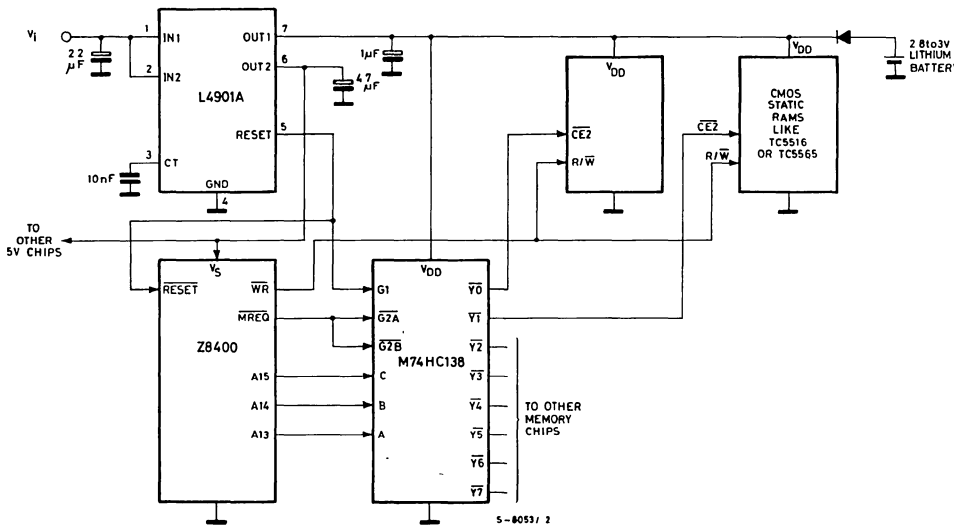


Fig. 5



APPLICATION SUGGESTION (continued)

Fig. 6

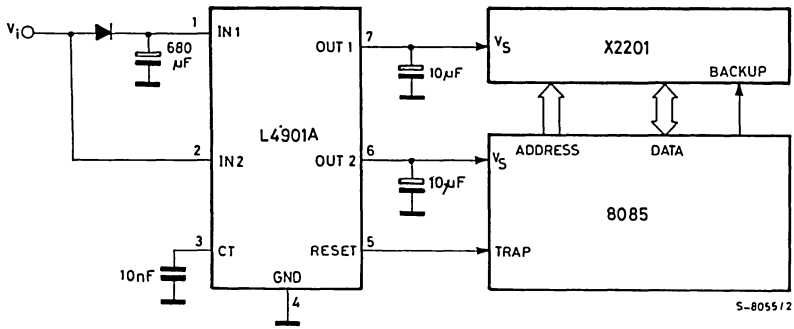


Fig. 7 - Quiescent current (Reg. 1) vs. output current

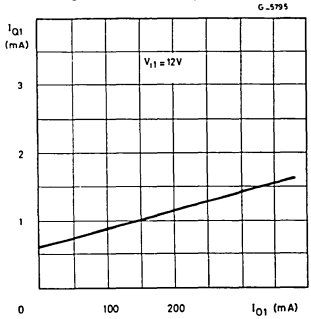


Fig. 8 - Quiescent current (Reg. 1) vs. input voltage

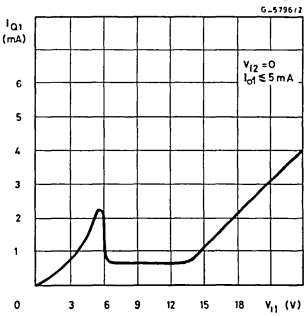


Fig. 9 - Total quiescent current vs. input voltage

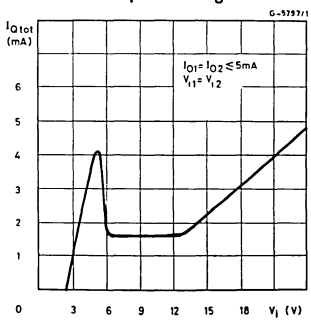


Fig. 10 - Regulator 1 output current and short circuit current vs. input voltage

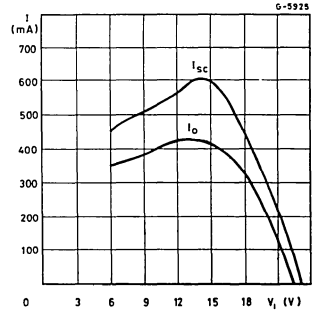


Fig. 11 - Regulator 2 output current and short circuit current vs. input voltage

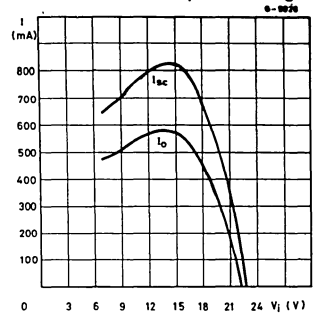
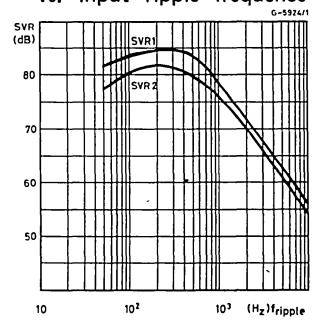


Fig. 12 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



SGS-THOMSON MICROELECTRONICS

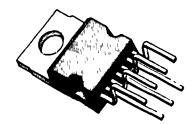
L4902A

DUAL 5V REGULATOR WITH RESET AND DISABLE

PRELIMINARY DATA

- DOUBLE BATTERY OPERATING
- OUTPUT CURRENTS: I_{01} = 300mA, I_{02} = 300mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- RESET OUTPUT NORMALLY HIGH
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4902A is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.
Reset and data save functions and remote switch on/off control can be realized.



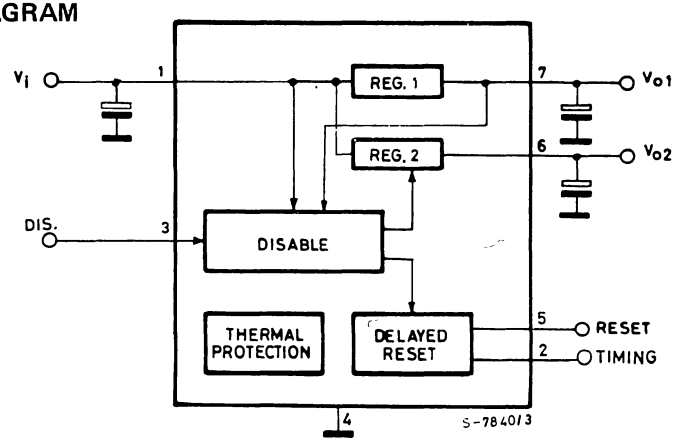
Heptawatt

ORDERING NUMBER: L4902A

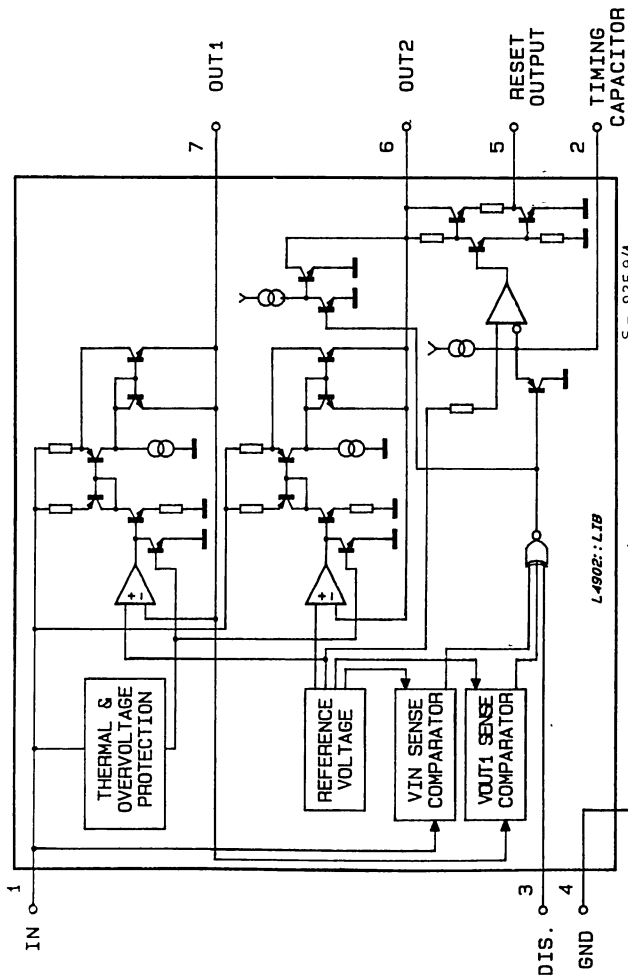
BSOLUTE MAXIMUM RATINGS

IN	DC input voltage	28	V
	Transient input overvoltage (t = 40 ms)	60	V
o	Output current	internally limited	
stg, T_j	Storage and junction temperature	-40 to 150	°C

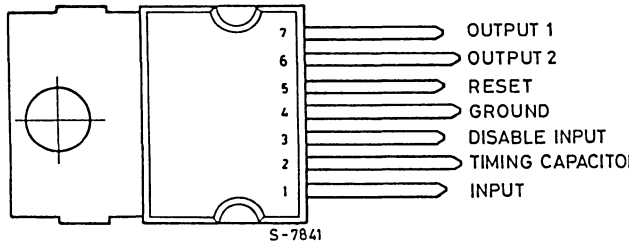
LOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



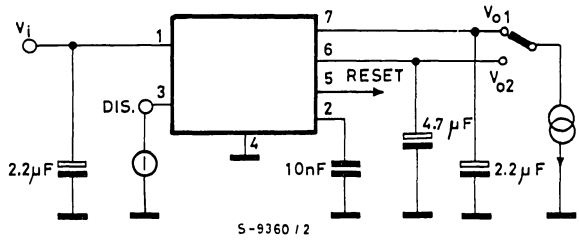
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Regulators common input.
2	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 5μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
3	V_{02} DISABLE INPUT	A high level ($> V_{DT}$) disable output Reg. 2.
4	GND	Common ground.
5	RESET OUTPUT	When pin 2 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A}\right)$; t_{RD} (ms) = C_t (nF).
6	OUTPUT 2	5V - 300mA regulator output. Enabled if $V_O 1 > V_{RT}$. DISABLE INPUT $< V_{DT}$ and $V_{IN} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	OUTPUT 1	5V - 300mA. Low leakage (in switch-OFF condition) output.

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (V_{IN} = 14.4V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_I	DC operating input voltage				24	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1 max.	ΔV_{01} = -100mV	300			mA
I_{LO1}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	µA
I_{02}	Output current 2 max.	ΔV_{02} = -100mV	300			mA
V_{I01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 100mA I_{01} = 300mA		0.7 0.8 1.1	0.8 1 1.4	V V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.7	V
V_{ITH}	Input threshold voltage hysteresis			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 24V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	5mA < I_{01} < 300mA		40	80	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 300mA		50	80	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V V_{02} LOW 7V < V_{IN} < 13V V_{02} HIGH I_{01} = $I_{02} \leq$ 5mA		4.5 2.7 1.6	6.5 4.5 3.5	mA mA mA
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -1mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3	5	11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
V_{DT}	V_{02} disable threshold voltage			1.25	2.4	V
I_D	V_{02} disable input current	$V_D \leq 0.4V$ $V_D \geq 2.4V$		-150 -30		μA μA
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R=0.5V I_o = 100mA	50	84		dB
SVR2	Supply voltage rejection		50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4902A makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with common inputs plus a reset output for the data save function and a Reg. 2 disable input.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:
- a high level ($> V_{DT}$) is applied on pin 3;
- an input overvoltage;
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:
- 5V internal reference without voltage divider between the output and the error comparator
- very low drop series regulator element utilizing current mirrors

permit high output impedance and then very low leakage current even in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery.

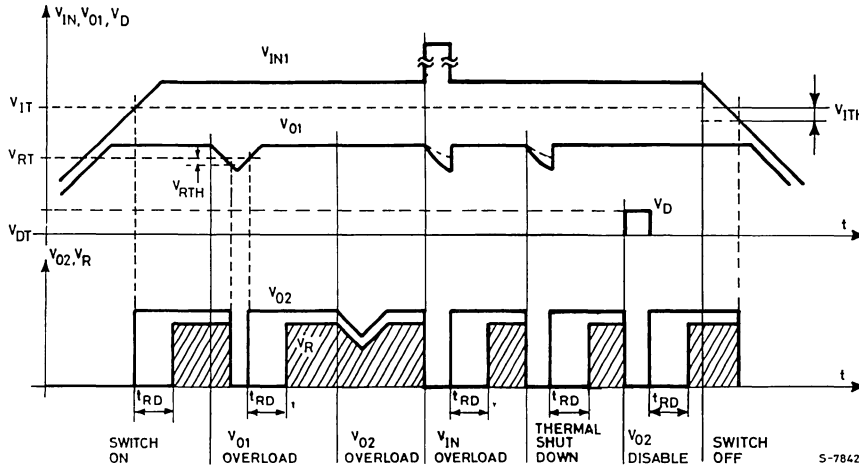
CIRCUIT OPERATION (continued)

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

The disable function can be used for remote on/off control of circuits connected to the V_{02} output.

Fig. 1



APPLICATION SUGGESTION

Fig. 2 illustrate how the L4902A's disable input may be used in a CMOS μComputer application.

The V_{01} regulator (low consumption) supply permanently a CMOS time of day clock and a CMOS μcomputer chip with volatile memory. V_{02} output, supplying non-essential circuits, is turned OFF under control of a μP unit.

Configurations of this type are used in products where the OFF switch is part of a keyboard scanned by a micro which operates continuously even in the OFF state.

Another application for the L4902A is supplying a shadow-ram microcomputer chip (SGS M38SH72 for exemple) where a fast NV memory is backed up on chip by a EEPROM when a low level on the reset output occurs.

By adding two CMOS-SCHMIDT-TRIGGER and few external components, also a watch dog function may be realized (see fig. 5). During normal operation the microsystem supplies a periodical pulse waveform; if an anomalous condition occours (in the program or in the system), the pulses will be absent and the disable input will be activated after a settling time determined by R1 C1. In this condition all the circuitry connected to V_{02} will be disabled, the system will be restarted with a new reset front.

The disable of V_{02} prevent spurious operation during microprocessor malfunctioning.

APPLICATION SUGGESTION (continued)

Fig. 2

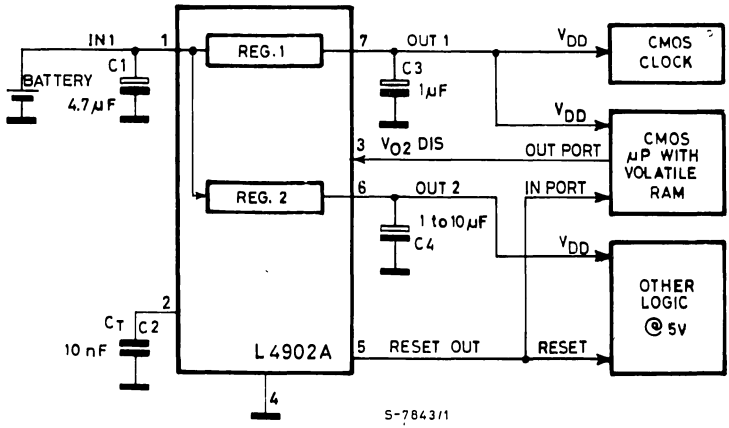
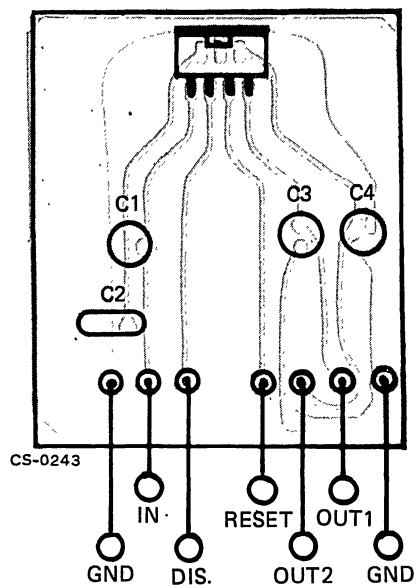


Fig. 3 - P.C. board and component layout of the circuit of Fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 4

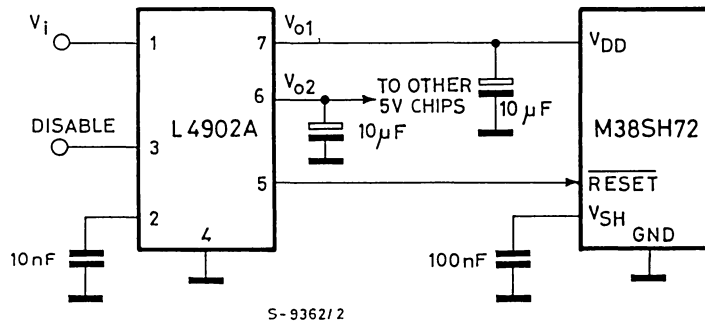
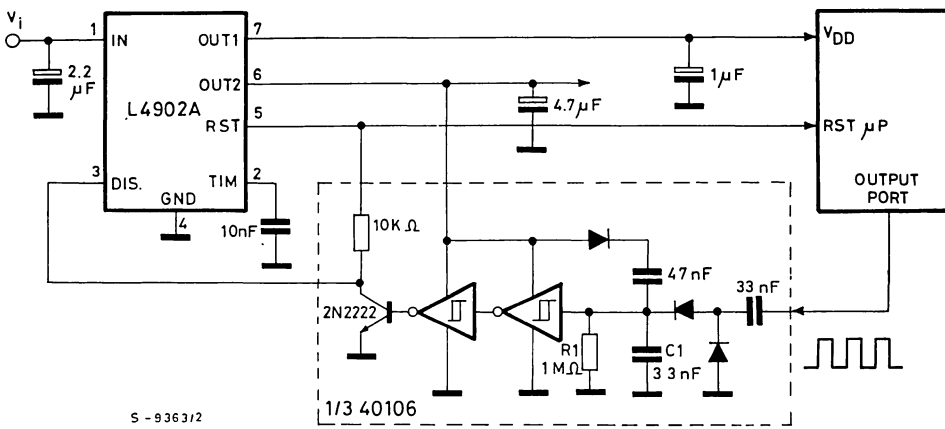


Fig. 5



APPLICATION SUGGESTION (continued)

Fig. 6 - Quiescent current vs. output current

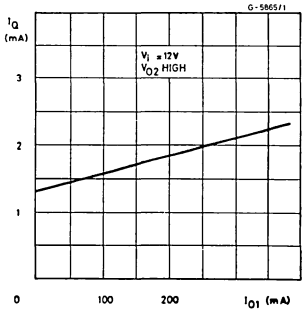


Fig. 7 - Quiescent current vs. input voltage

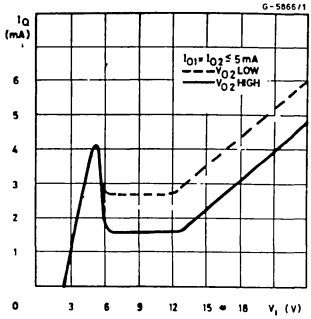
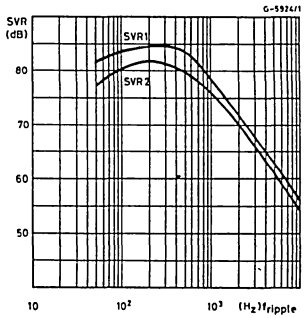


Fig. 8 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



SGS-THOMSON MICROELECTRONICS

L4903

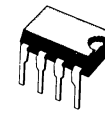
DUAL 5V REGULATOR WITH RESET AND DISABLE FUNCTIONS

PRELIMINARY DATA

- OUTPUT CURRENTS: I_{01} = 50mA, I_{02} = 100mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ±2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT NORMALLY LOW
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4903 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset, data save functions and remote switch on/off control can be realized.



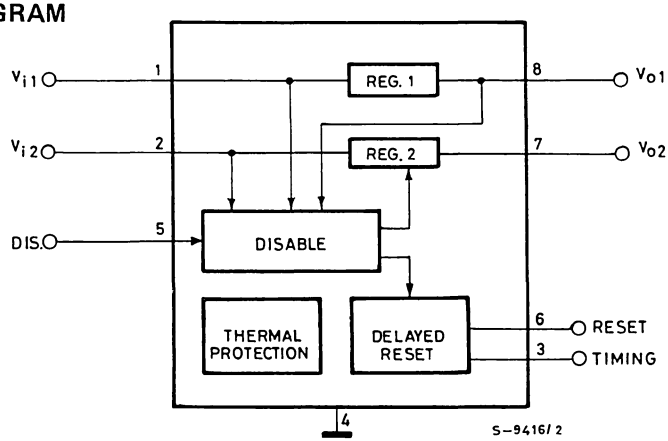
Minidip Plastic

ORDERING NUMBER: L4903

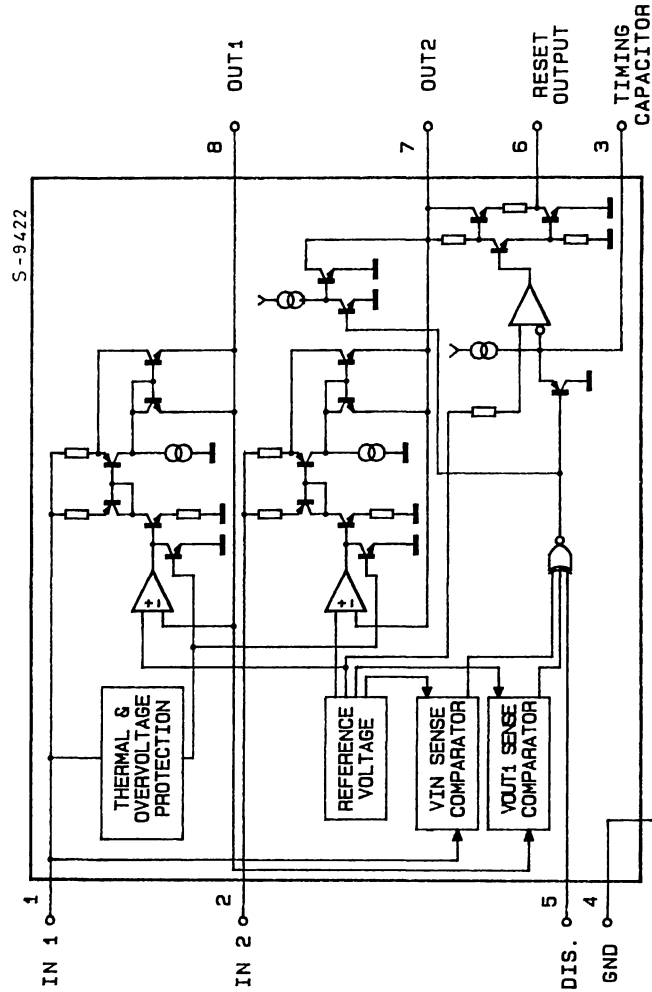
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
V_t	Transient input overvoltage (t = 40 ms)	60	V
P_{tot}	Power dissipation at T_{amb} = 50°C	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

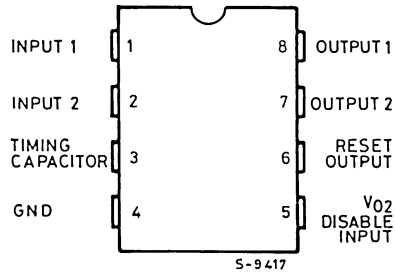
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



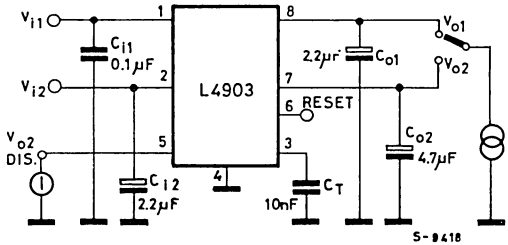
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 50mA regulator input.
2	INPUT 2	100mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	V_{02} DISABLE INPUT	A high level ($> V_{DT}$) disables output Reg. 2.
6	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched low. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A}\right)$; t_{RD} (ms) = C_t (nF).
7	OUTPUT 2	5V - 100mA regulator output. Enabled if V_O 1 $> V_{RT}$. DISABLE INPUT $< V_{DT}$ and $V_{IN\,2} > V_{IT}$. If Reg. 2 is switched OFF the C_{02} capacitor is discharged.
8	OUTPUT 1	5V - 50mA regulator output with low leakage in switch-OFF condition.

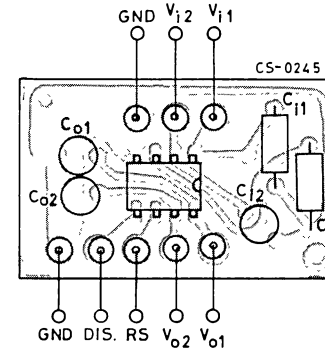
THERMAL DATA

$R_{th\,j\text{-}pin}$	Thermal resistance junction-pin 4	max	70	°C/W
$R_{th\,j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

TEST CIRCUIT



P.C. board and components layout of the test circuit (1 : 1 scale)



ELECTRICAL CHARACTERISTICS (V_{IN} = 14,4V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{01}	Output voltage 1	R load 1KΩ	4,95	5.05	5,15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1 max. (*)	ΔV_{01} = -100mV	50			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	µA
I_{02}	Output current 2 max. (*)	ΔV_{02} = -100mV	100			mA
V_{i01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 50mA		0.7 0.75	0.8 0.9	V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.7	V
V_{ITH}	Input threshold voltage hysteresis			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 18V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	V_{IN1} = 8V 5mA < I_{01} < 50mA		5	20	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 100mA		10	50	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V V_{02} LOW 7V < V_{IN} < 13V V_{02} HIGH I_{01} = $I_{02} \leq$ 5mA		4.5 2.7 1.6	6.5 4.5 3.5	mA mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 I_{01} < 5mA I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.4	4.7	V_{02}-0.2	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3	5	11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
V_{DT}	V_{02} disable threshold voltage			1.25	2.4	V
I_D	V_{02} disable input current	$V_D \leq 0.4V$ $V_D \geq 2.4V$		-150 30		μA μA
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 50mA	50	84		dB
SVR2	Supply voltage rejection	I_o = 100mA	50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current conditions.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4903 makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function and Reg. 2 disable input.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02} and V_R) switches on and the reset output (V_R) goes low after a programmable time T_{RD} (timing capacitor).

V_{02} is switched at low level and V_R at high level when one of the following conditions occurs:

- a high level ($> V_{DT}$) is applied on pin 5;
- an input overvoltage;
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator
- very low drop series regulator element utilizing current mirrors

permit high output impedance and then very low leakage current even in power down conditions.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery.

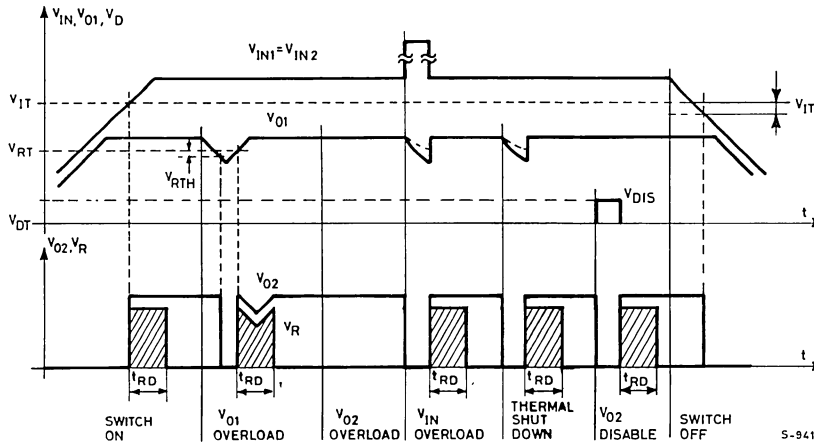
CIRCUIT OPERATION (continued)

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

The disable function can be used for remote on/off control of circuits connected to the V_{02} output.

Fig. 1



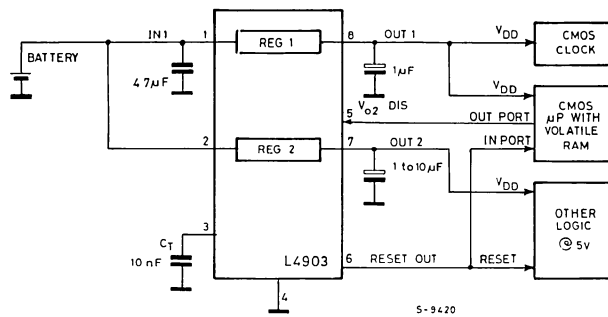
APPLICATION SUGGESTION

Fig. 2 illustrates how the L4903's disable input may be used in a CMOS μComputer application.

The V_{01} regulator (low consumption) supply permanently a CMOS time of day clock and a CMOS μcomputer chip with volatile memory. V_{02} output, supplying non-essential circuits, is turned OFF under control of a μP unit.

Configurations of this type are used in products where the OFF switch is part of a keyboard scanned by a micro which operates continuously even in the OFF state.

Fig. 2



APPLICATION SUGGESTIONS (continued)

Fig. 3 - Quiescent current (Reg. 1) vs. output current

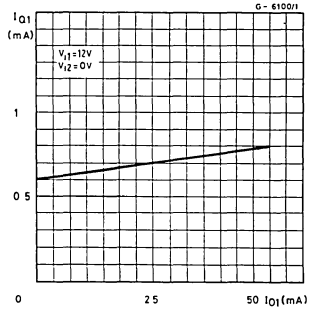


Fig. 4 - Quiescent current (Reg. 1) vs. input voltage

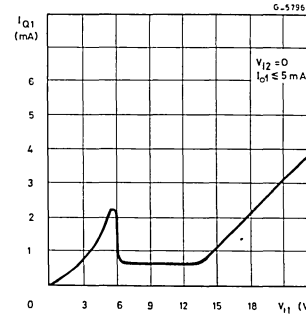


Fig. 5 - Total quiescent current vs. input voltage

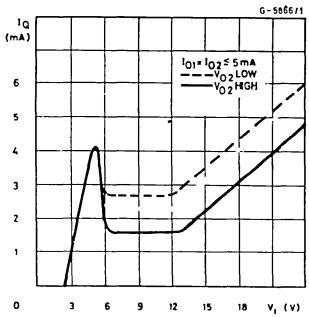
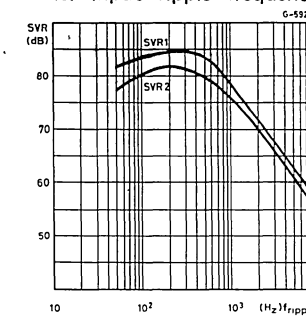


Fig. 6 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



SGS-THOMSON MICROELECTRONICS

L4904A

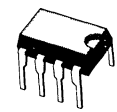
DUAL 5V REGULATOR WITH RESET

PRELIMINARY DATA

- OUTPUT CURRENTS: I_{01} = 50mA, I_{02} = 100mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT NORMALLY HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4904A is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.



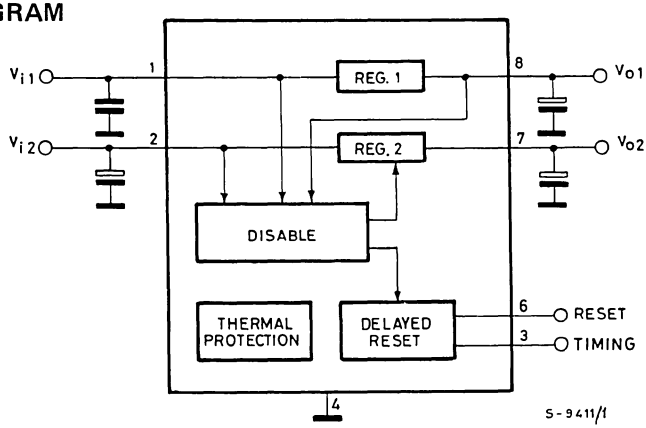
Minidip Plastic

ORDERING NUMBER: L4904A

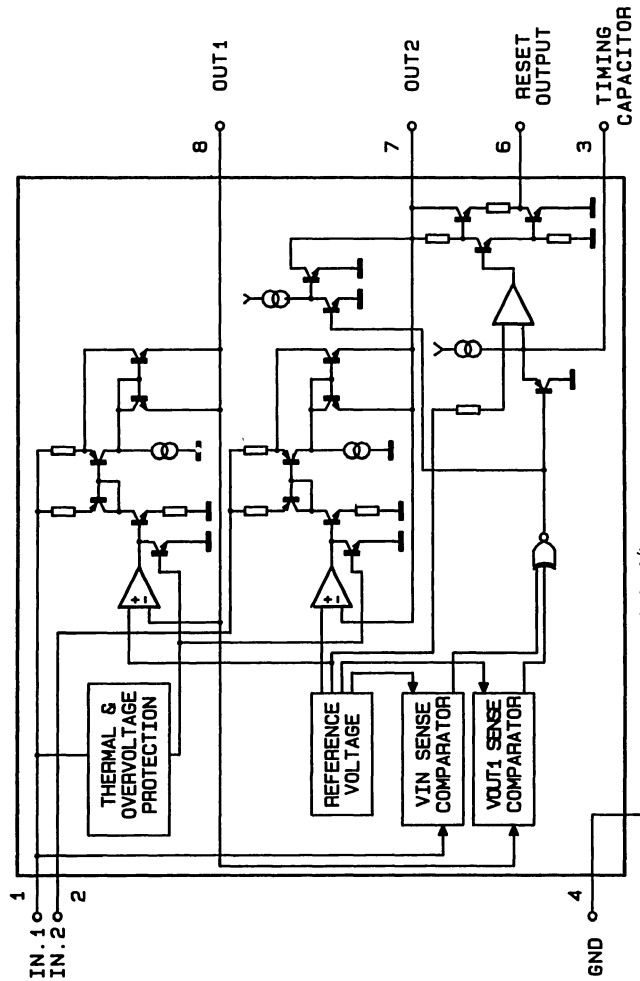
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
	Transient input overvoltage (t = 40 ms)	60	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation at T_{amb} = 50°C	1	W
T_j	Storage and junction temperature	-40 to 150	°C

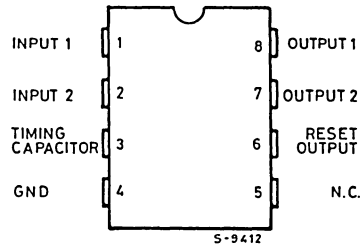
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



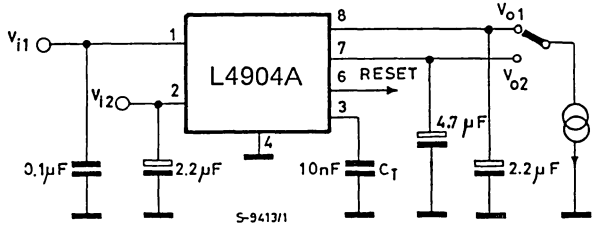
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 50mA regulator input.
2	INPUT 2	100mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
6	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \ (\frac{5V}{10\mu A})$; t_{RD} (ms) = C_t (nF).
7	OUTPUT 2	5V - 100mA regulator output. Enabled if $V_O 1 > V_{RT}$ and $V_{IN\,2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
8	OUTPUT 1	5V - 50mA regulator output with low leakage in switch-OFF condition.

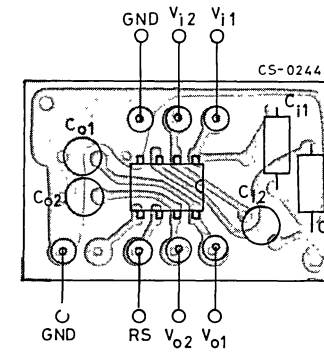
THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

TEST CIRCUIT



P.C. board and components layout of the test circuit (1 : 1 scale)



ELECTRICAL CHARACTERISTICS (V_{IN} = 14,4V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01} -0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1	ΔV_{01} = -100mV	50			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	µA
I_{02}	Output current 2	ΔV_{02} = -100mV	100			mA
V_{I01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 50mA		0.7 0.75	0.8 0.9	V V
V_{IT}	Input threshold voltage		V_{01} +1.2	6.4	V_{01} +1.7	V
V_{ITH}	Input threshold voltage hyst.			250		mV
ΔV_{01}	Line regulation	7V < V_{IN} < 18V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	
ΔV_{01}	Load regulation 1	V_{IN} = 8V 5mA < I_{01} < 50mA		5	20	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 100mA		10	50	
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V I_{02} = $I_{01} \leq$ 5mA		4.5 1.6	6.5 3.5	mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 $I_{01} \leq$ 5mA I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3		11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 125°C		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 125°C		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 50mA	50	84		dB
SVR2	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 100mA	50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4904A makes it very easy to supply such equipments; it provides two voltage regulators (booth 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:

- an input overvoltage
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator;
- very low drop series regulator element utilizing current mirrors;

permit high output impedance and then very low leakage current even in power down conditions.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{01} regulator also features low consumption (0.6mA

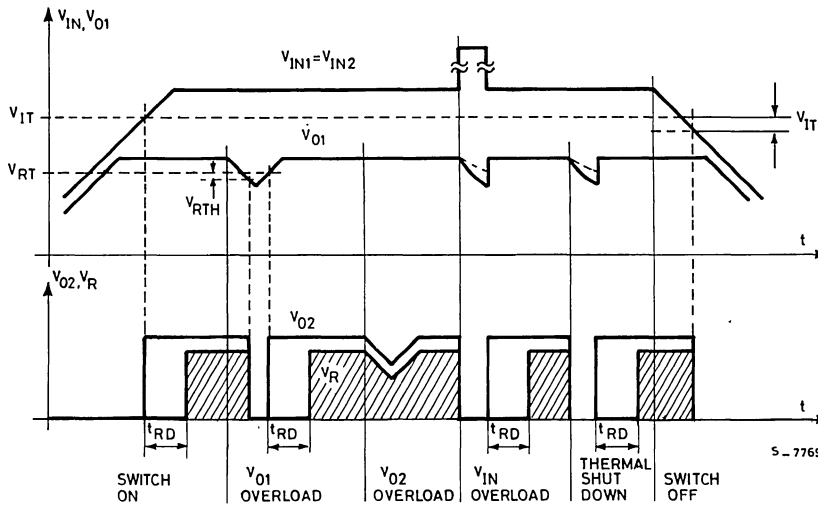
CIRCUIT OPERATION (continued)

typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5V circuits which may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

Fig. 1



APPLICATION SUGGESTIONS

Fig. 2 shows an application circuit for a μP system.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Fig. 3 shows the L4904A with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type C-MOS μP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

APPLICATION SUGGESTIONS (continued)

Application Circuits of a Microprocessor system (Fig. 2) or with data save battery (Fig. 3). The reset output provide delayed rising front at the turn-off of the regulator 2.

Fig. 2

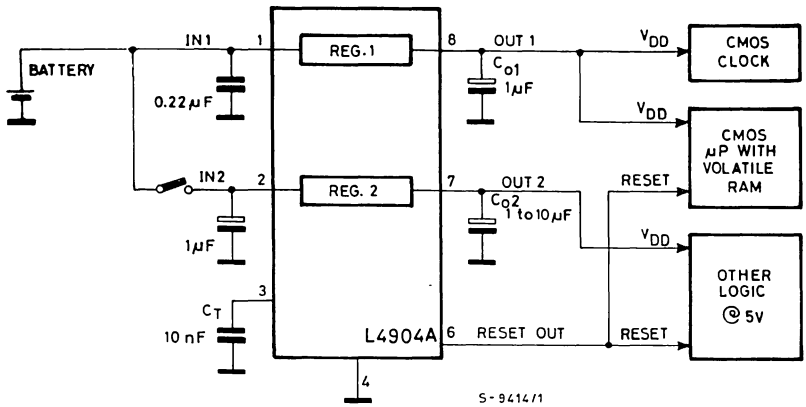
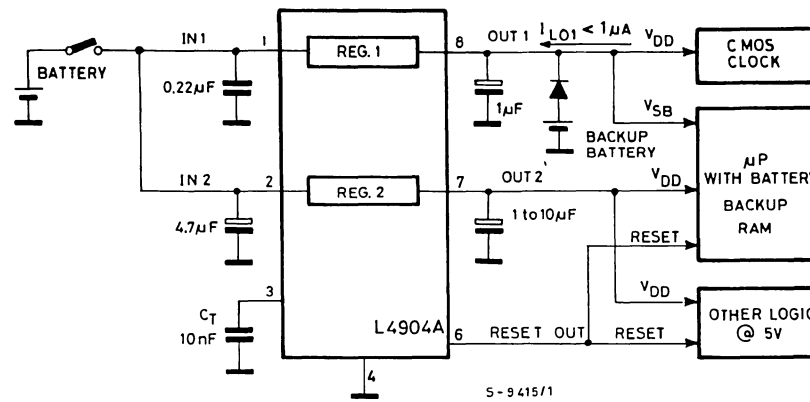


Fig. 3



APPLICATION SUGGESTIONS (continued)

Fig. 4 - Quiescent current (Reg. 1) vs. output current

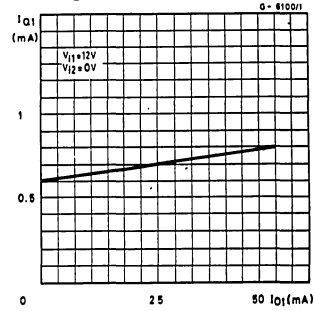


Fig. 5 - Quiescent current (Reg. 1) vs. input voltage

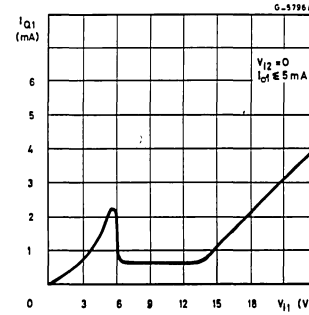


Fig. 6 - Total quiescent current vs. input voltage

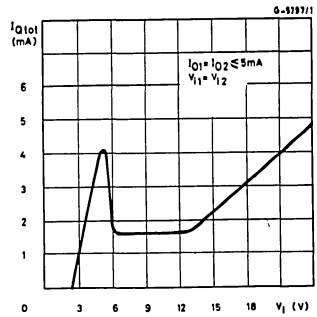
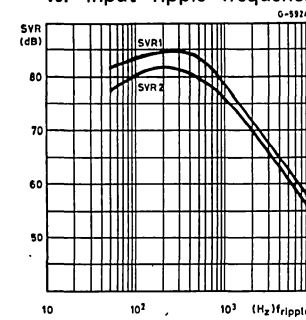


Fig. 7 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



SGS-THOMSON MICROELECTRONICS

L4905

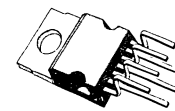
DUAL 5V REGULATOR WITH RESET

ADVANCE DATA

- DOUBLE BATTERY OPERATING
- OUTPUT CURRENTS: $I_{01} = 200mA$ $I_{02} = 300mA$
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 1%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCIENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4905 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.



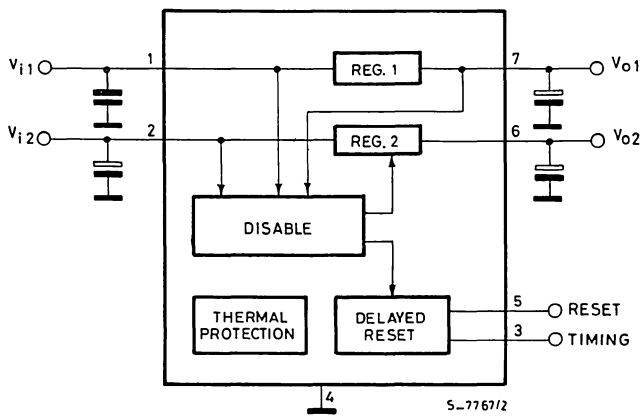
Heptawatt

ORDERING NUMBER: L4905

ABSOLUTE MAXIMUM RATINGS

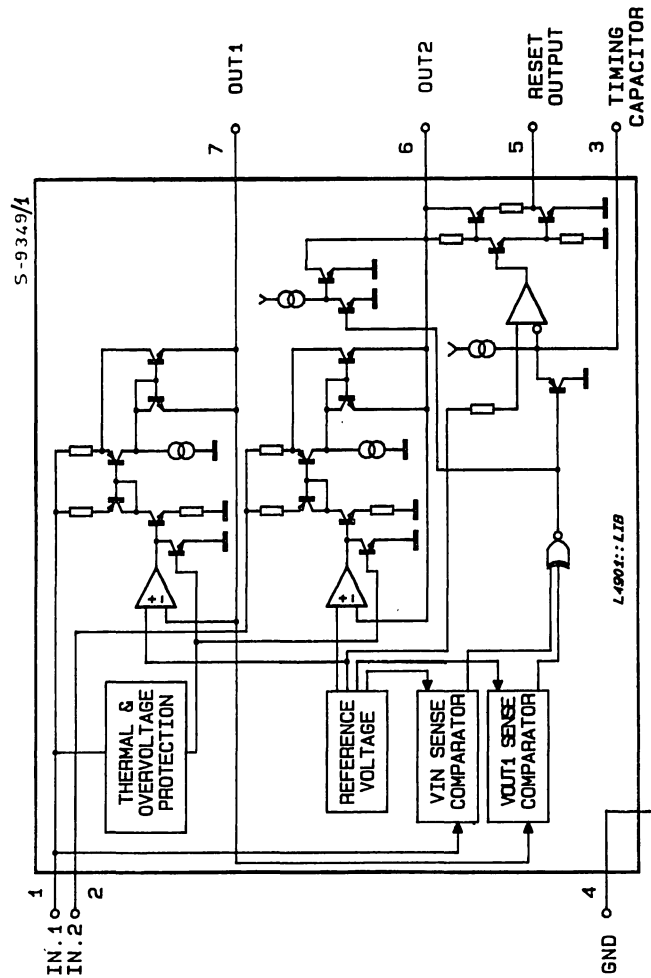
V_{IN}	DC input voltage	28	V
	Transient input overvoltage (t = 40 ms)	60	V
I_o	Output current	internally limited	
T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAM

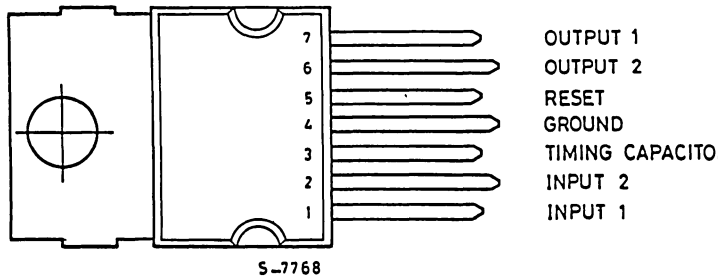


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



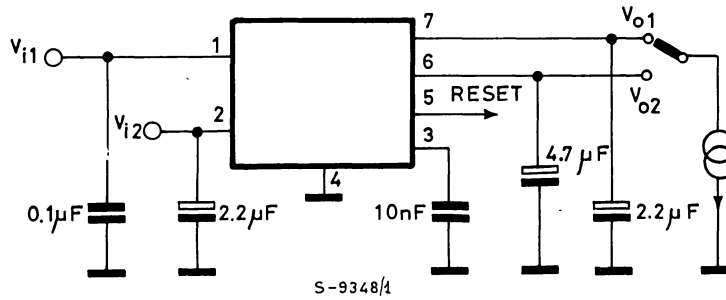
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 200mA regulator input.
2	INPUT 2	300mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A} \right)$; t_{RD} (ms) = C_t (nF)
6	OUTPUT 2	5V - 300mA regulator output. Enabled if $V_O 1 > V_{RT}$ and $V_{IN2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	OUTPUT 1	5V - 200mA regulator output with low leakage (in switch-OFF condition).

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS ($V_{IN1} = V_{IN2} = 14,4V$, $T_{amb} = 25°$ unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_I	DC operating input voltage				24	V
V_{01}	Output voltage 1	R load 1KΩ	5.0	5.05	5.1	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1	ΔV_{01} = -100mV	200			mA
I_{LO1}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	µA
I_{02}	Output current 2	ΔV_{02} = -100mV	300			mA
V_{i01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 100mA I_{01} = 200mA		0.7 0.8 1.05	0.8 1 1.3	V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.7	V
V_{ITH}	Input threshold voltage hyst.			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 24V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	5mA < I_{01} < 200mA		40	80	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 300mA		50	100	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V I_{02} = $I_{01} \leq$ 5mA		4.5 1.6	6.5 3.5	mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 $I_{01} \leq$ 5mA I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3	5	11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 125°C		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 125°C		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 100mA	54 50	84		dB
SVR2	Supply voltage rejection		50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4905 makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:

- an input overvoltage
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator;
- very low drop series regulator element utilizing current mirrors;
- permit high output impedance and then very low leakage current error even in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{01}

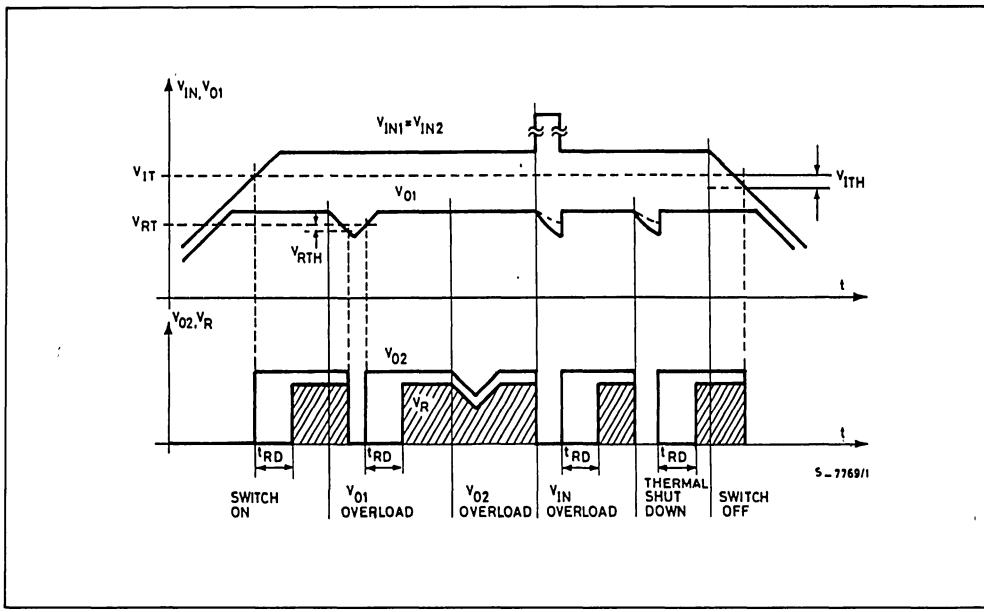
CIRCUIT OPERATION (continued)

regulator also features low consumption (0.6mA typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

Fig. 1



APPLICATION SUGGESTIONS

Fig. 2 shows an application circuit for a μP system typically used in trip computers or in car radios with programmable tuning.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Fig. 4 shows the L4905 with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type N-MOS μP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

APPLICATION SUGGESTION (continued)

Fig. 2

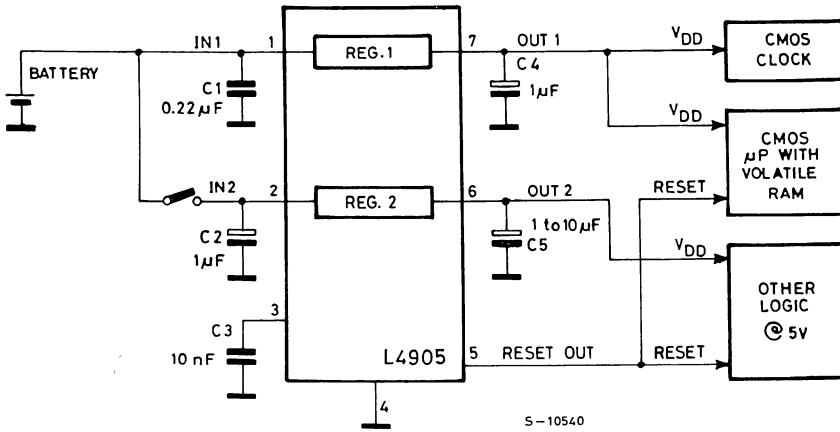
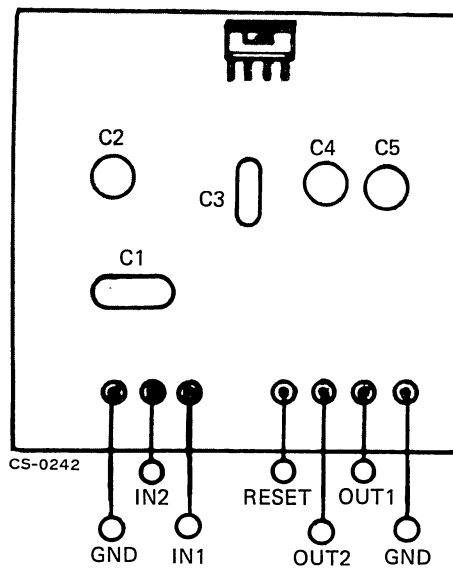


Fig. 3 - P.C. board component layout of fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 4

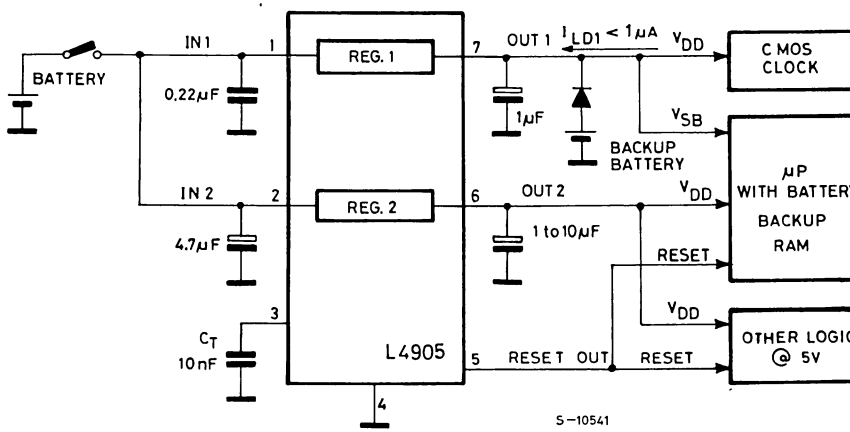


Fig. 5 - Quiescent current (Reg. 1) vs. output current

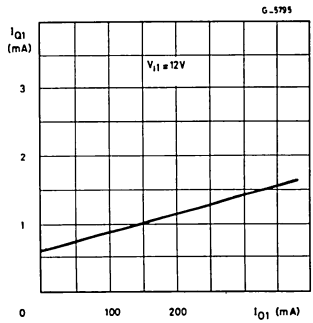


Fig. 6 - Quiescent current (Reg. 1) vs. input voltage

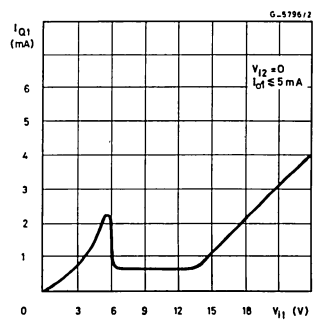
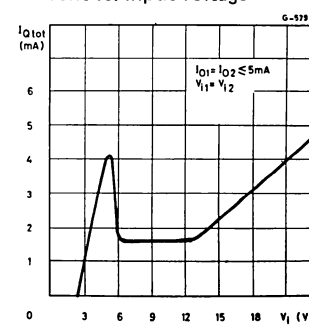


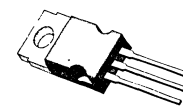
Fig. 7 - Total quiescent current vs. input voltage



VERY LOW DROP 1.5A REGULATORS

PRELIMINARY DATA

- PRECISE 5V, 8.5V, 10V, 12V OUTPUTS
- LOW DROPOUT VOLTAGE (500mV TYP AT 1.5A)
- VERY LOW QUIESCENT CURRENT
- THERMAL SHUTDOWN
- SHORT CIRCUIT PROTECTION
- REVERSE POLARITY PROTECTION

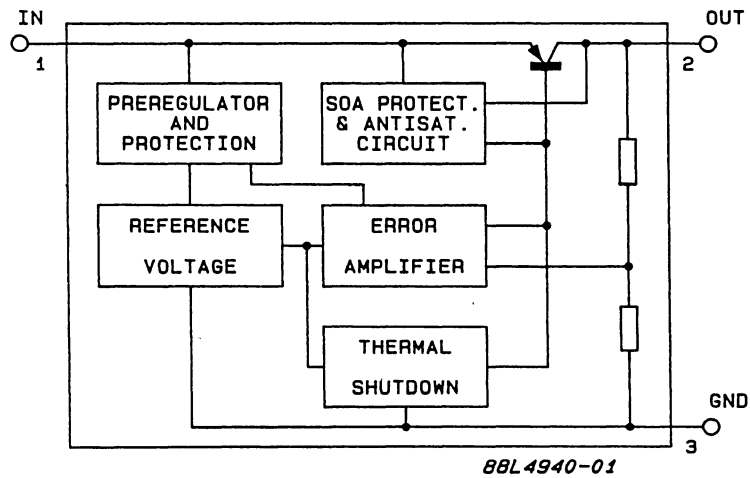


TO-220

INTRODUCTION

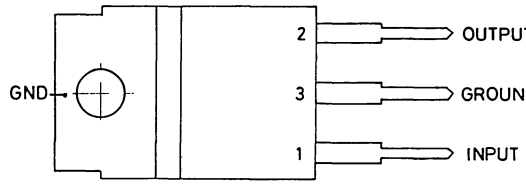
The L4940 series of three terminal positive regulators is available in TO-220 package and with several fixed output voltages, making it useful in a wide range of industrial and consumer applications. Thanks to its very low input/output voltage drop, these devices are particularly suitable for battery powered equipments, reducing consumption and prolonging battery life. Each type employs internal current limiting, antisaturation circuit, thermal shut-down and safe area protection.

BLOCK DIAGRAM



CONNECTION DIAGRAM AND ORDERING NUMBERS

(Top view)



S - 2568/1

ORDERING NUMBERS	OUTPUT VOLTAGE
L4940V5	5V
L4940V85	8.5V
L4940V10	10V
L4940V12	12V

ABSOLUTE MAXIMUM RATINGS

V_i	Forward input voltage			30	V
V_{IR}	Reverse input voltage	(V_O = 5V	R_O = 100Ω)	-15	V
		(V_O = 8.5V	R_O = 180Ω)		
		(V_O = 10V	R_O = 200Ω)		
		(V_O = 12V	R_O = 240Ω)		
I_O	Output current			Internally limited	
P_{tot}	Power dissipation			Internally limited	
T_j, T_{stg}	Junction and storage temperature			-40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50	°C/W

TEST CIRCUITS

Fig. 1 - DC Parameters

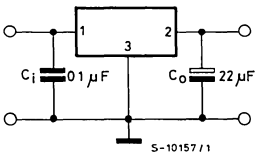


Fig. 2 - Load Regulation

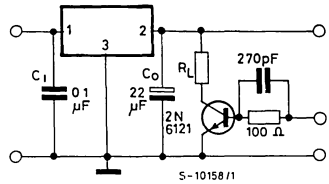
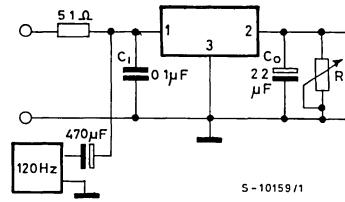


Fig. 3 - Ripple Rejection



ELECTRICAL CHARACTERISTICS (Refer to the test circuits $T_j = 25°C$, $C_i = 0.1\mu F$, $C_o = 22\mu F$, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
OUTPUT VOLTAGE				5			8.5		V
INPUT VOLTAGE (unless otherwise specified)				7			10.5		V
V_o	Output voltage	I_o = 0.5A	4.9	5	5.1	8.3	8.5	8.7	V
		I_o = 5 mA to 1.5A	4.8 (V_i= 6.5 to 16V)	5	5.2	8.15 (V_i= 10.2 to 16V)	8.5	8.85	V
V_i	Operating input voltage	I_o = 5 mA			17			17	V
ΔV_o	Line regulation	I_o = 5 mA		4 (V_i= 6V to 17V)	10		4 (V_i= 9.5 to 17V)	9	mV
ΔV_o	Load regulation	I_o = 5 mA to 1.5A		8	25		12	30	mV
		I_o = 0.5A to 1A		5	15		8	16	
I_Q	Quiescent current	I_o = 5 mA		5	8		4	8	mA
		I_o = 1.5 A		30 (V_i = 6.5V)	50		30 (V_i = 10.2V)	50	
ΔI_Q	Quiescent current change	I_o = 5 mA			3			2.5	mA
		I_o = 1.5 A			15 (V_i= 6.5 to 16V)			15 (V_i= 10.2 to 16V)	
V_d	Dropout voltage	I_o = 0.5A		200	400		200	400	mV
		I_o = 1.5A		500	900		500	900	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift			0.5			0.8		mV/°C
SVR	Supply voltage rejection	f = 120 Hz I_o = 1A	58	68		58	66		dB
I_{sc}	Short circuit current limit	V_i = 14V		2	2.7		2	2.7	A
				2.2 (V_i = 6.5V)	2.9		2.2 (V_i = 10.2V)	2.9	
Z_o	Output impedance	f = 1 KHz I_o = 0.5A		30			32		mΩ
e_N	Output noise	B = 100 Hz to 100 KHz		30			30		$\mu V/V_o$

ELECTRICAL CHARACTERISTICS (Refer to the test circuits $T_j = 25°C$, $C_i = 0.1\mu F$, $C_o = 22\mu F$, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
OUTPUT VOLTAGE				10			12		V
INPUT VOLTAGE (unless otherwise specified)				12			14		V
V_o	Output voltage	I_o = 0.5A	9.8	10	10.2	11.75	12	12.25	V
		I_o = 5 mA to 1.5A	9.6 (V_i= 11.7 to 16V)	10	10.4	11.5 (V_i= 13.8 to 17V)	12	12.5	
V_i	Operating input voltage	I_o = 5 mA			17			17	V
ΔV_o	Line regulation	I_o = 5 mA		3 (V_i = 11 to 17V	8		3 (V_i = 13 to 14V)	7	mV
ΔV_o	Load regulation	I_o = 5 mA to 1.5A		15	35		15	35	mV
		I_o = 0.5A to 1A		10	20		10	25	
I_Q	Quiescent current	I_o = 5 mA		4	8		4	8	mA
		I_o = 1.5A		30 (V_i = 11.7V)	50		30 (V_i = 13.8V)	50	
ΔI_Q	Quiescent current change	I_o = 5 mA			2			1.5	mA
		I_o = 1.5A			13 (V_i= 11.7 to 16V)			10 (V_i = 13.8V)	
V_d	Dropout voltage	I_o = 0.5A		200	400		200	400	mV
		I_o = 1.5A		500	900		500	900	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift			1			1.2		mV/°C
SVR	Supply voltage rejection	f = 120 Hz I_o = 1A	56	62		55	61		dB
I_{sc}	Short circuit current limit	V_i = 14V		2	2.7		2	2.7	A
		V_i = 11.7V		2.2	2.9		—	—	
Z_o	Output impedance	f = 1KHz I_o = 0.5A		36			40		mΩ
e_N	Output noise voltage	B = 100 Hz to 100 KHz		30			30		$\mu V/V_o$

Fig. 4 - Dropout voltage vs. output current

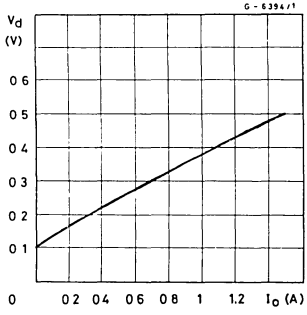


Fig. 5 - Dropout voltage vs. temperature

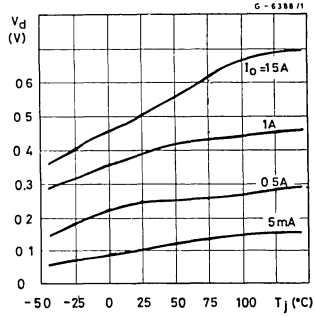


Fig. 6 - Output voltage vs. temperature (L4940V5)

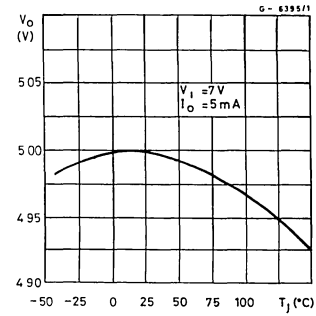


Fig. 7 - Output voltage vs. temperature (L4940V85)

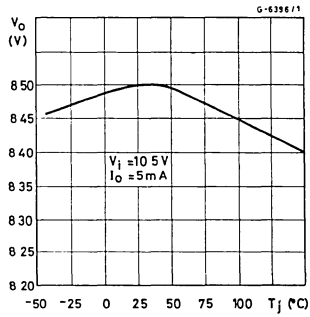


Fig. 8 - Output voltage vs. temperature (L4040V10)

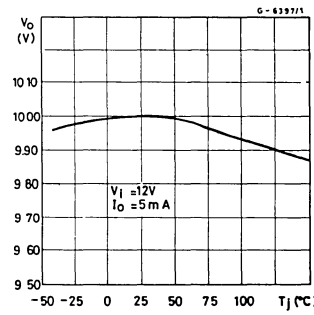


Fig. 9 - Output voltage vs. temperature (L4940V12)

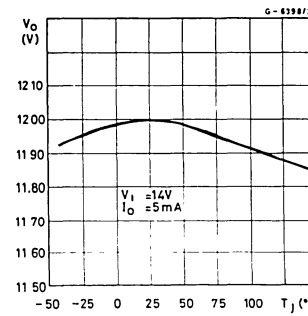


Fig. 10 - Quiescent current vs. temperature (L4940V5)

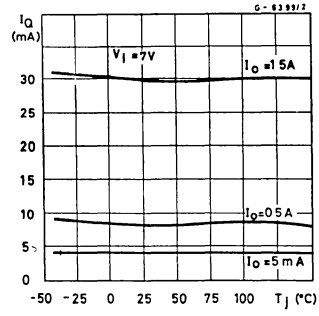


Fig. 11 - Quiescent current vs. input voltage (L4940V5)

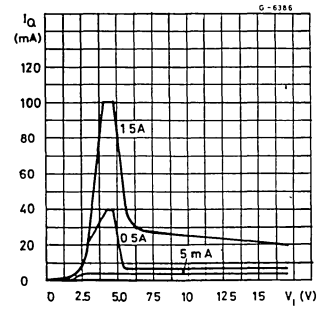


Fig. 12 - Quiescent current vs. output current (L4940V5)

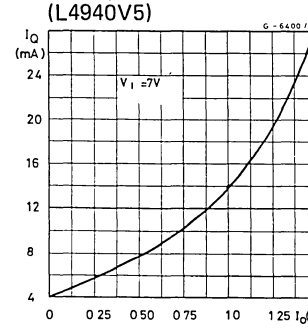


Fig. 13 - Short circuit current vs. temperature (L4940V5)

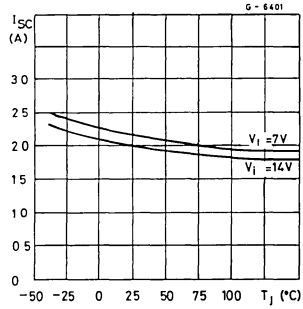


Fig. 14 - Peak output current vs. input/output differential voltage (L4940V5)

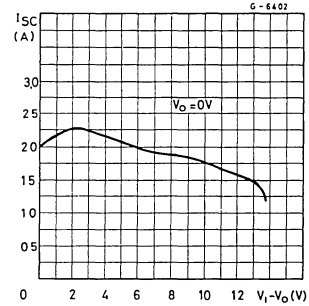


Fig. 15 - Low voltage behavior (L4940V5)

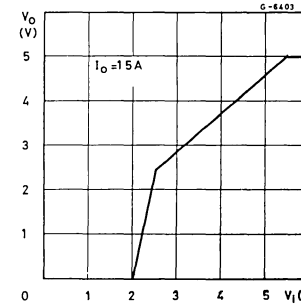


Fig. 16 - Low voltage behavior (L4940V85)

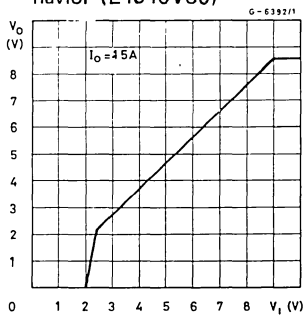


Fig. 17 - Low voltage behavior (L4940V10)

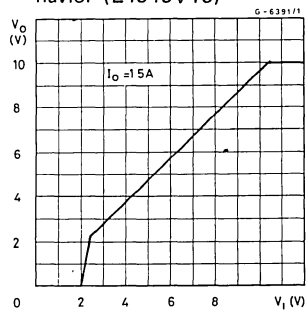


Fig. 18 - Low voltage behavior (L4940V12)

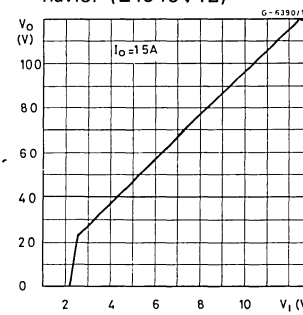


Fig. 19 - Supply voltage rejection vs. frequency (L4940V5)

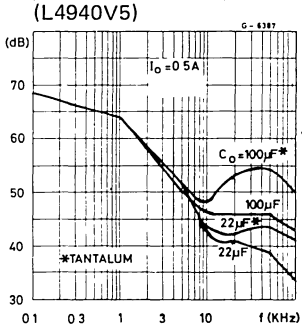


Fig. 20 - Supply voltage rejection vs. output current

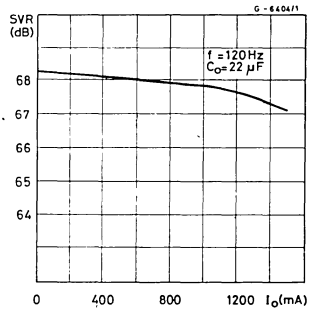


Fig. 21 - Load dump characteristics (L4940V5)

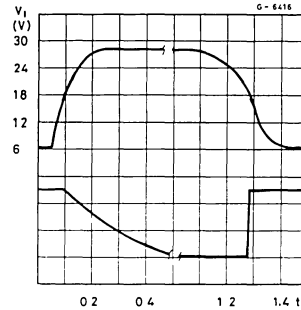


Fig. 22 - Line transient response (L4940V5)

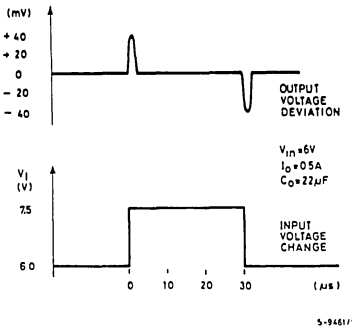


Fig. 23 - Load transient response

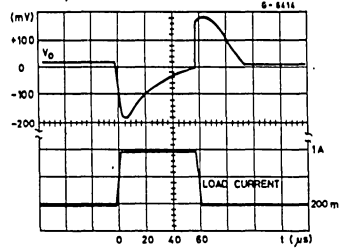


Fig. 24 - Total power dissipation

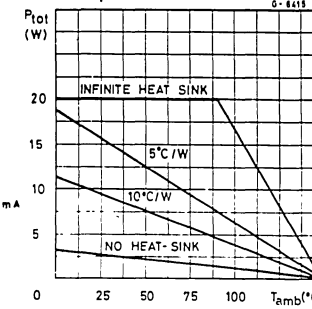


Fig. 25 - Distributed supply with on-card L4940 and L4941 low-drop regulators

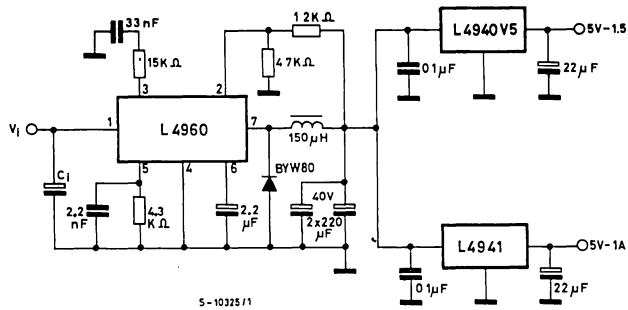
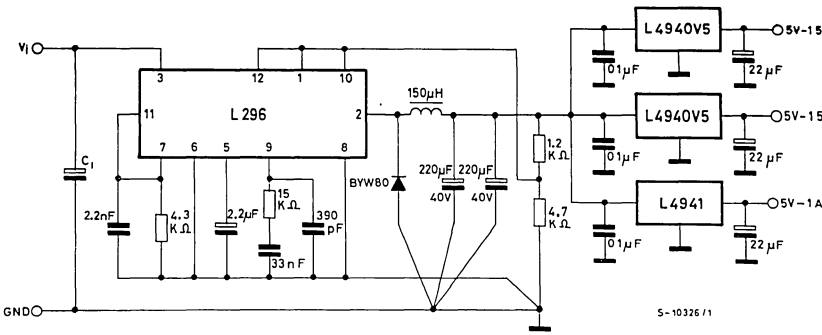


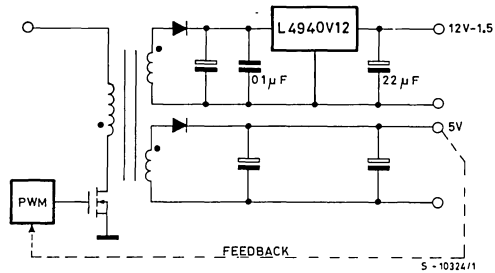
Fig. 26 - Distributed supply with on-card L4940 and L4941 low-drop regulators



ADVANTAGES OF THESE APPLICATIONS ARE:

- On card regulation with short circuit and thermal protection on each output.
- Very high total system efficiency due to the switching preregulation and very low-drop postregulations.

Fig. 27



ADVANTAGES OF THIS CONFIGURATION ARE:

- Very high regulation (line and load) on both the output voltages.
- 12V output short-circuit and thermally protected.
- Very high efficiency on the 12V output due to the very low drop regulator.

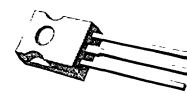
SGS-THOMSON MICROELECTRONICS

L4941 - 4941X

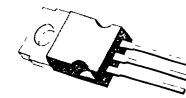
VERY LOW DROP 1A REGULATOR

PRELIMINARY DATA

- LOW DROPOUT VOLTAGE (450mV TYP AT 1A)
- VERY LOW QUIESCENT CURRENT
- THERMAL SHUTDOWN
- SHORT CIRCUIT PROTECTION
- REVERSE POLARITY PROTECTION



SOT-82



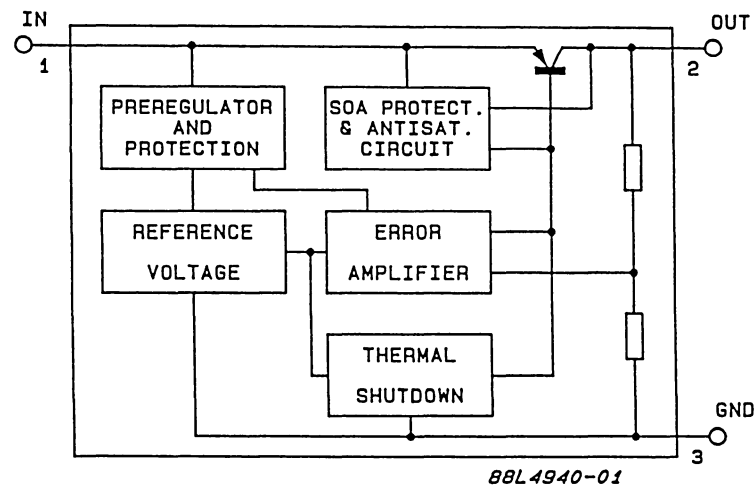
TO-220

ORDER CODE: L4941 (TO-220)
L4941X (SOT-82)

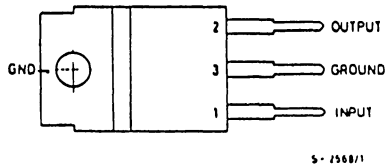
INTRODUCTION

The L4941/X is a three terminal 5V positive regulator available in TO-220 and SOT-82 packages; making it useful in a wide range of the industrial and consumer applications. Thanks to its very low input/output voltage drop, this device is particularly suitable for battery powered equipment, reducing consumption and prolonging battery life. It employes internal current limiting, antisaturation circuit, thermal shutdown and safe area protection.

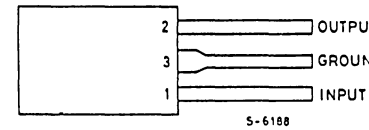
BLOCK DIAGRAM



PIN CONNECTIONS



TO-220



SOT-82

ABSOLUTE MAXIMUM RATINGS

V_I	Forward input voltage	30	V
V_{IR}	Reverse input voltage (R_O = 100Ω)	-15	V
I_O	Output current	Internally limited	
P_{tot}	Power dissipation	Internally limited	
T_j, T_{stg}	Junction and storage temperature	-40 to 150	°C

THERMAL DATA

			SOT-82	TO-220
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	8 °C/W	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100 °C/W	50 °C/W

TEST CIRCUITS

Fig. 1 - DC Parameters

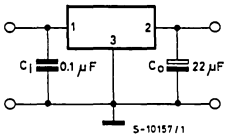


Fig. 2 - Load Regulation

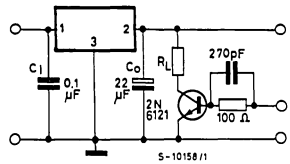
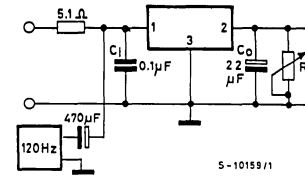


Fig. 3 - Ripple Rejection



ELECTRICAL CHARACTERISTICS (Refer to the test circuits $T_j = 25°C$, $C_I = 0.1\mu F$, $C_o = 22\mu F$, unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
OUTPUT VOLTAGE					5		
INPUT VOLTAGE (unless otherwise specified)					7		
V_o	Output voltage	I_o = 5mA to 1A V_I = 6V to 14V		4.8	5	5.2	V
V_I	Operating input voltage	I_o = 5mA				16	V
ΔV_o	Line regulation	V_I = 6V to 16V I_o = 5mA			5	20	mV
ΔV_o	Load regulation	I_o = 5mA to 1A I_o = 0.5A to 1A			8 5	20 15	mV
I_Q	Quiescent current	V_I = 6V	I_o = 5mA		4	8	mA
			I_o = 1A		20	40	
ΔI_Q	Quiescent current change	V_I = 6V to 14V	I_o = 5mA			3	mA
			I_o = 1A			-10	
V_d	Dropout voltage	I_o = 0.5A			250	450	mV
		I_o = 1A			450	700	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift				0.6		mV/°C
SVR	Supply voltage rejection	f = 120Hz I_o = 0.5A		58	68		dB
I_{sc}	Short circuit current limit	V_I = 14V			1.6	2.0	A
		V_I = 6V			1.8	2.2	
Z_o	Output impedance	f = 1KHz I_o = 0.5A			30		mΩ
e_N	Output noise voltage	B = 100Hz to 100KHz			30		$\mu V/V_o$

Fig. 4 - Dropout voltage vs. output current

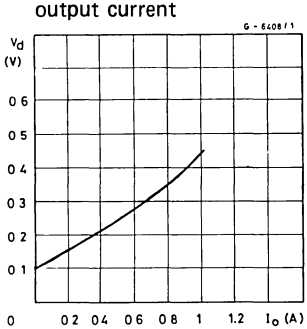


Fig. 5 - Dropout voltage vs. temperature

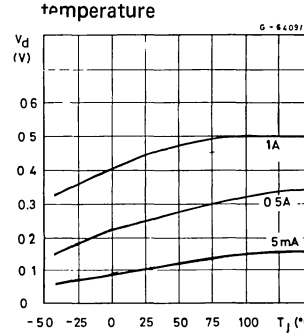


Fig. 6 - Output voltage vs. temperature

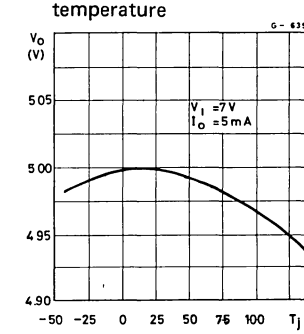


Fig. 7 - Quiescent current vs. temperature

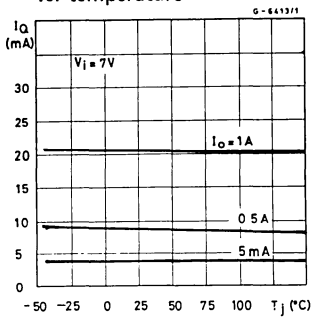


Fig. 8 - Quiescent current vs. input voltage

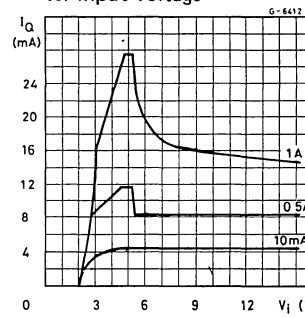


Fig. 9 - Quiescent current vs. output current

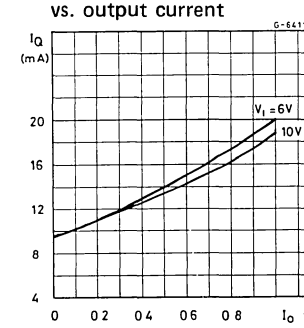


Fig. 10 - Short circuit current vs. temperature

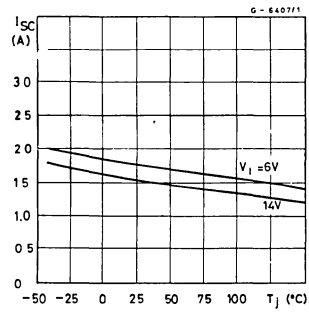


Fig. 11 - Peak output current vs. input/output differential voltage

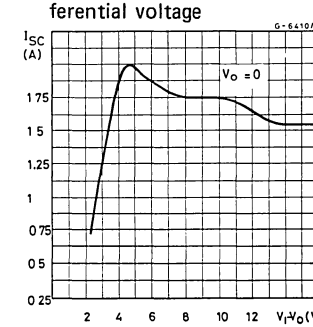


Fig. 12 - Low voltage behavior

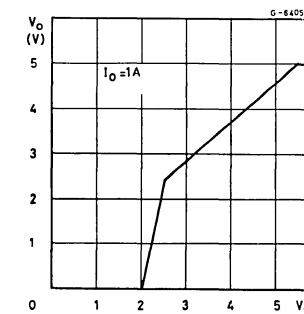


Fig. 13 - Supply voltage rejection vs. frequency

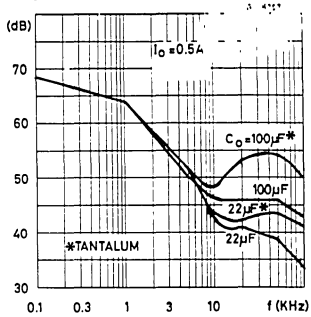


Fig. 14 - Supply voltage rejection vs. output current

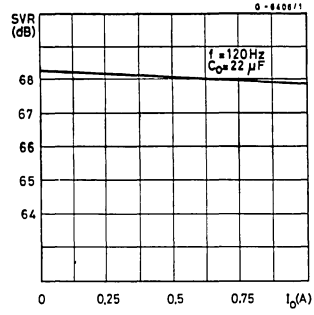


Fig. 15 - Load dump characteristics

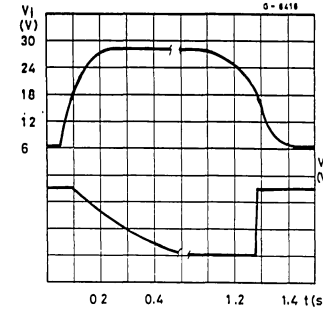


Fig. 16 - Line transient response

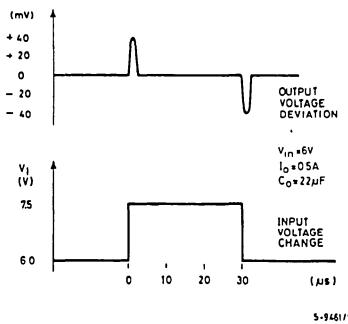


Fig. 17 - Load transunt response

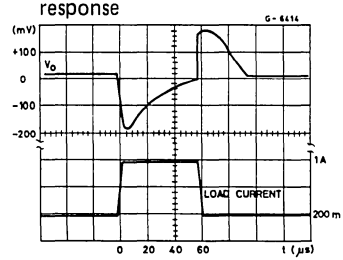


Fig. 18 - Totale power dissipation (TO-220)

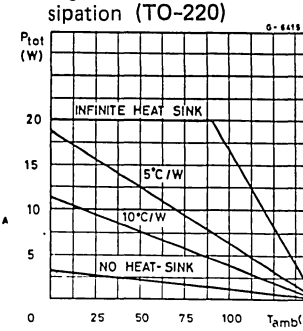
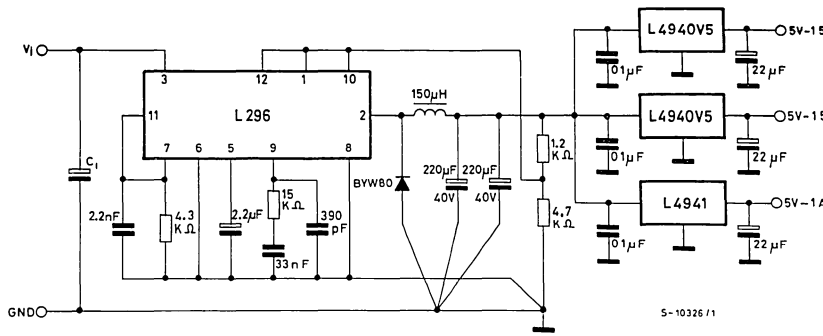


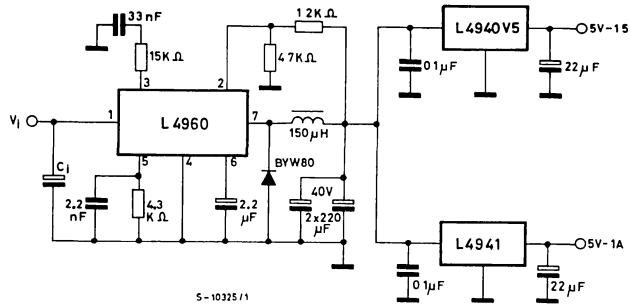
Fig. 19 - Distributed supply with on-card L4940 and L4941 low-drop regulators



ADVANTAGES OF THESE APPLICATIONS ARE:

- On card regulation with short circuit and thermal protection on each output.
- Very high total system efficiency due to the switching preregulation and very low-drop postregulations.

Fig. 20 - Distributed supply with on-card L4940 and L4941 low-drop regulators



2.5A POWER SWITCHING REGULATOR

PRELIMINARY DATA

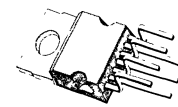
- 2.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- PRECISE (± 2%) ON-CHIP REFERENCE
- HIGH SWITCHING FREQUENCY
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- INTERNAL LIMITING CURRENT
- THERMAL SHUTDOWN

The L4960 is a monolithic power switching regulator delivering 2.5A at a voltage variable from 5V to 40V in step down configuration.

Features of the device include current limiting, soft start, thermal protection and 0 to 100% duty cycle for continuous operation mode.

The L4960 is mounted in a Heptawatt plastic power package and requires very few external componénts.

Efficient operation at switching frequencies up to 150KHz allows a reduction in the size and cost of external filter components.



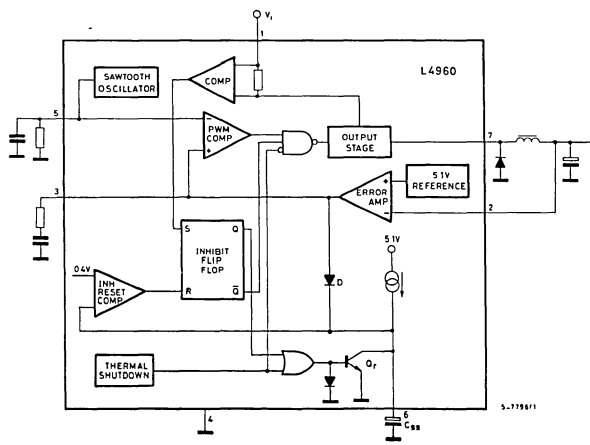
Heptawatt

ORDERING NUMBER: L4960 (Vertical)
L4960H (Horizontal)

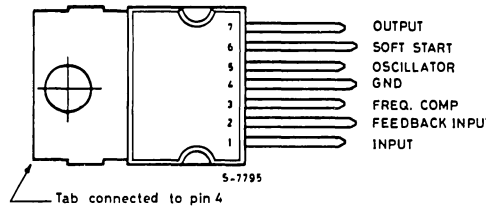
ABSOLUTE MAXIMUM RATINGS

V_1	Input voltage	50	V
$V_1 - V_7$	Input to output voltage difference	50	V
V_7	Negative output DC voltage	-1	V
	Negative output peak voltage at t = 0.1μs; f = 100KHz	-5	V
V_3, V_6	Voltage at pin 3 and 6	5.5	V
V_2	Voltage at pin 2	7	V
I_3	Pin 3 sink current	1	mA
I_5	Pin 5 source current	20	mA
P_{tot}	Power dissipation at $T_{case} \leqslant 90°C$	15	W
T_j, T_{stg}	Junction and storage temperature	-40 to 150	°C

BLOCK DIAGRAM



CONNECTION DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50	°C/W

PIN FUNCTIONS

N°	NAME	FUNCTION
1	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the internal logic.
2	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
3	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
4	GROUND	Common ground terminal.
5	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency.
6	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
7	OUTPUT	Regulator output.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_j = 25°C, V_i = 35V, unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS							
V_o	Output voltage range	V_i = 46V	I_o = 1A	V_{ref}		40	V
V_i	Input voltage range	V_o = V_{ref} to 36V	I_o = 2.5A	9		46	V
ΔV_o	Line regulation	V_i = 10V to 40V	V_o = V_{ref} I_o = 1A		15	50	mV
ΔV_o	Load regulation	V_o = V_{ref}	I_o = 0.5A to 2A		10	30	mV
V_{ref}	Internal reference voltage (pin 2)	V_i = 9V to 46V	I_o = 1A	5	5.1	5.2	V
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of refer. voltage	T_j = 0°C to 125°C I_o = 1A			0.4		mV/°C
V_d	Dropout voltage	I_o = 2A			1.4	3	V
I_{om}	Maximum operating load current	V_i = 9V to 46V V_o = V_{ref} to 36V		2.5			A
I_{7L}	Current limiting threshold (pin 7)	V_i = 9V to 46V V_o = V_{ref} to 36V		3		4.5	A
I_{SH}	Input average current	V_i = 46V; output short-circuit			30	60	mA
η	Efficiency	f = 100KHz	V_o = V_{ref}		75		%
		I_o = 2A	V_o = 12V		85		%
SVR	Supply voltage ripple rejection	ΔV_i = $2V_{rms}$ f_{ripple} = 100Hz V_o = V_{ref}	I_o = 1A	50	56		dB
f	Switching frequency			85	100	115	KHz
$\frac{\Delta f}{\Delta V_i}$	Voltage stability of switching frequency	V_i = 9V to 46V			0.5		%
$\frac{\Delta f}{\Delta T_j}$	Temperature stability of switching frequency	T_j = 0°C to 125°C			1		%
f_{max}	Maximum operating switching frequency	V_o = V_{ref}	I_o = 2A	120	150		KHz
T_{sd}	Thermal shutdown junction temperature				150		°C

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
DC CHARACTERISTICS							
I_{1Q}	Quiescent drain current	100% duty cycle pins 5 and 7 open	V_I = 46V		30	40	mA
		0% duty cycle			15	20	mA
$-I_{7L}$	Output leakage current	0% duty cycle				1	mA
SOFT START							
I_{6SO}	Source current			100	130	150	μA
I_{6SI}	Sink current			50	70	120	μA
ERROR AMPLIFIER							
V_{3H}	High level output voltage	V_2 = 4.7V	I_3 = 100μA	3.5			V
V_{3L}	Low level output voltage	V_2 = 5.3V	I_3 = 100μA			0.5	V
I_{3SI}	Sink output current	V_2 = 5.3V		100	150		μA
$-I_{3SO}$	Source output current	V_2 = 4.7V		100	150		μA
I_2	Input bias current	V_2 = 5.2V			2	10	μA
G_V	DC open loop gain	V_3 = 1V to 3V		46	55		dB
OSCILLATOR							
$-I_5$	Oscillator source current			5			mA

CIRCUIT OPERATION (refer to the block diagram)

The L4960 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 2.5A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2%).

This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.

The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 3. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{ss} and allowed to rise, linearly, as this capacitor is charged by a constant current source. Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V.

The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network. The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

Fig. 1 - Soft start waveforms

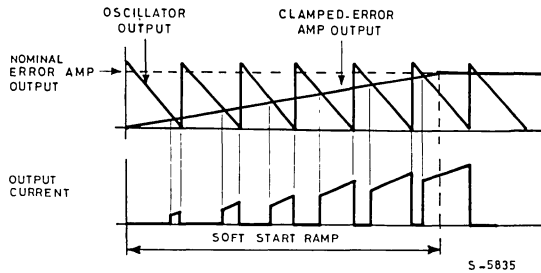


Fig. 2 - Current limiter waveforms

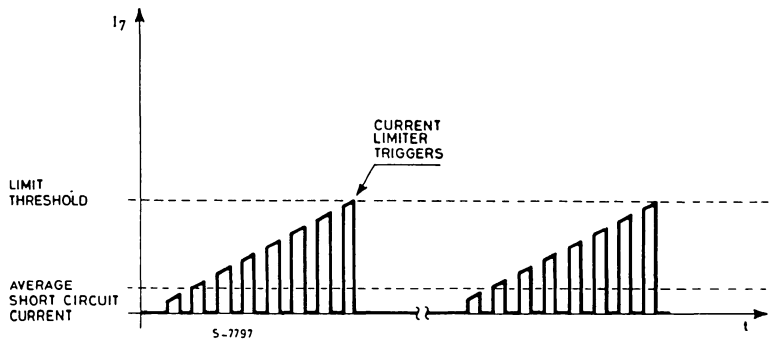
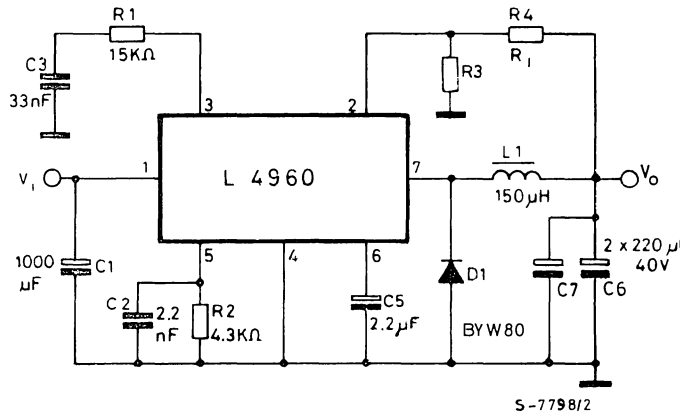


Fig. 3 - Test and application circuit



C6, C7: EKR (ROE)
L1 = 150μH at 5A (COGEMA 946042)
CORE TYPE: MAGNETICS 58206-A2 MPP
N° TURNS 45, WIRE GAUGE: 0.8mm (20 AWG)

Fig. 4 - Quiescent drain current vs. supply voltage (0% duty cycle)

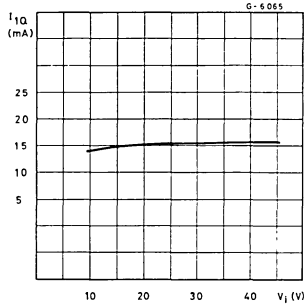


Fig. 5 - Quiescent drain current vs. supply voltage (100% duty cycle)

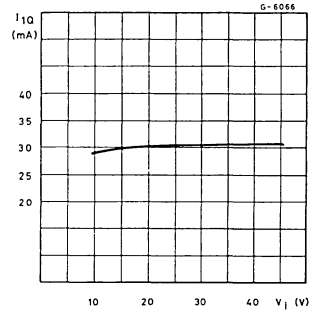


Fig. 6 - Quiescent drain current vs. junction temperature (0% duty cycle)

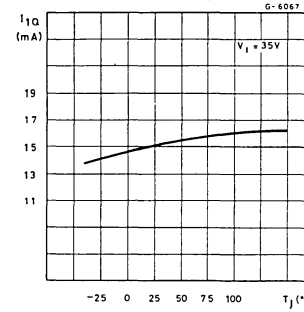


Fig. 7 - Quiescent drain current vs. junction temperature (100% duty cycle)

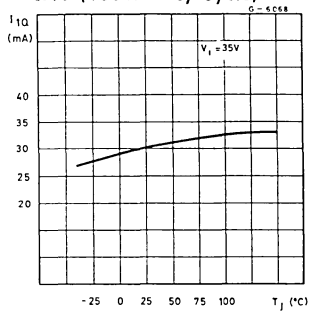


Fig. 8 - Reference voltage (pin 2) vs. V_I

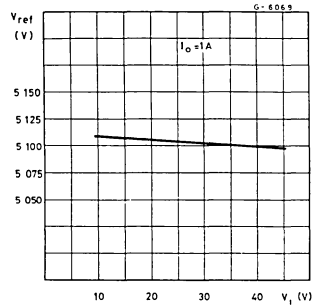


Fig. 9 - Reference voltage vs. junction temperature (pin 2)

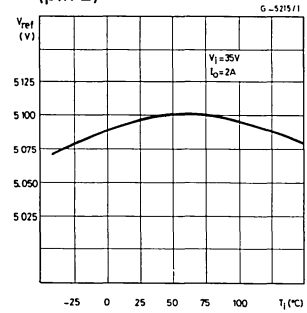


Fig. 10 - Open loop frequency and phase responde of error amplifier

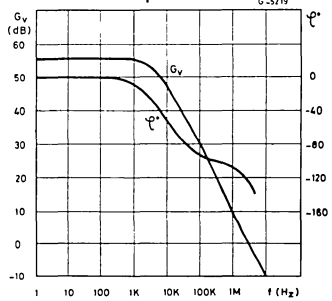


Fig. 11 - Switching frequency vs. input voltage

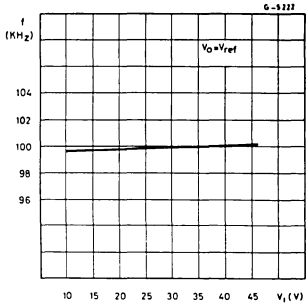


Fig. 12 - Switching frequency vs. junction temperature

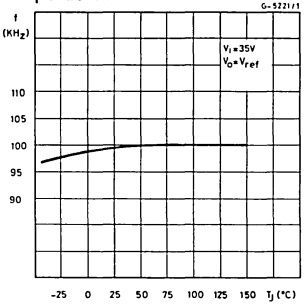


Fig. 13 - Switching frequency vs. R2 (see test circuit)

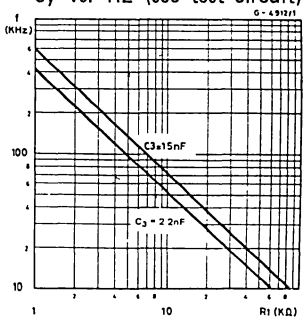


Fig. 14 - Line transient response

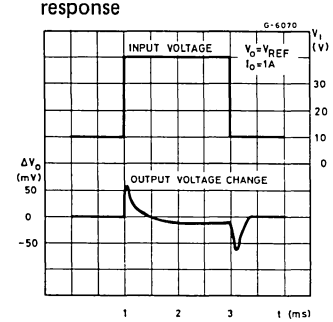


Fig. 15 - Load transient response

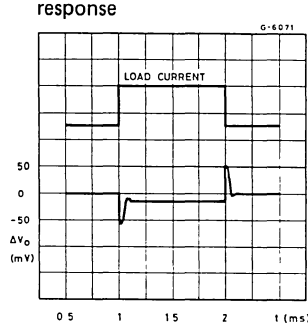


Fig. 16 - Supply voltage ripple rejection vs. frequency

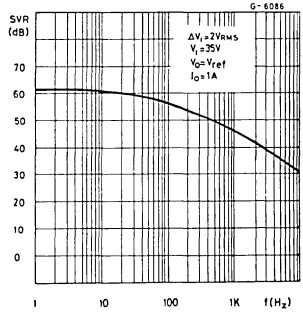


Fig. 17 - Dropout voltage between pin 1 and pin 7 vs. current at pin 7

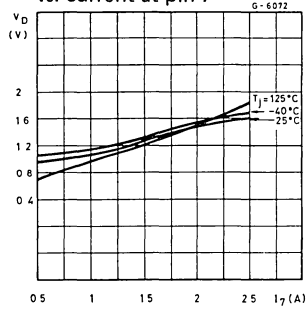


Fig. 18 - Dropout voltage between pin 1 and 7 vs. junction temperature

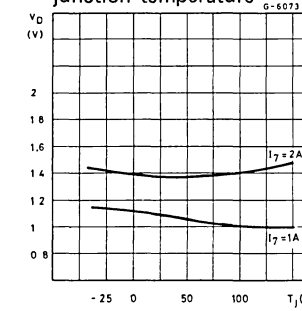


Fig. 19 - Power dissipation derating curve

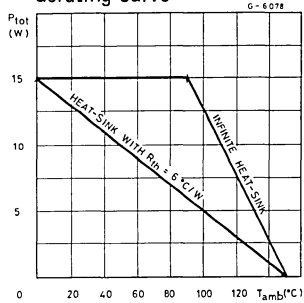


Fig. 20 - Efficiency vs. output current

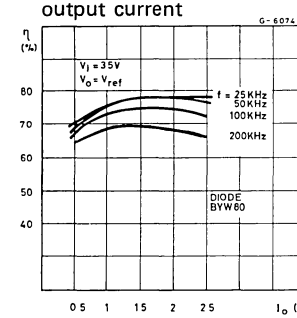


Fig. 21 - Efficiency vs. output current

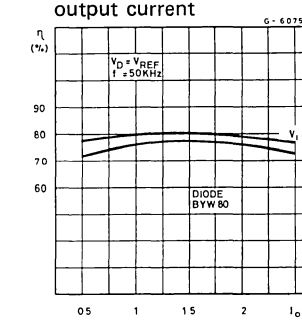


Fig. 22 - Efficiency vs. output current

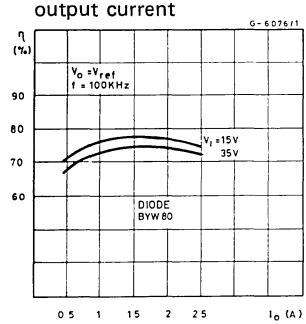
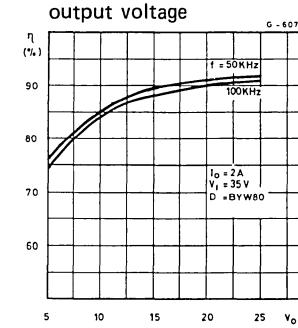
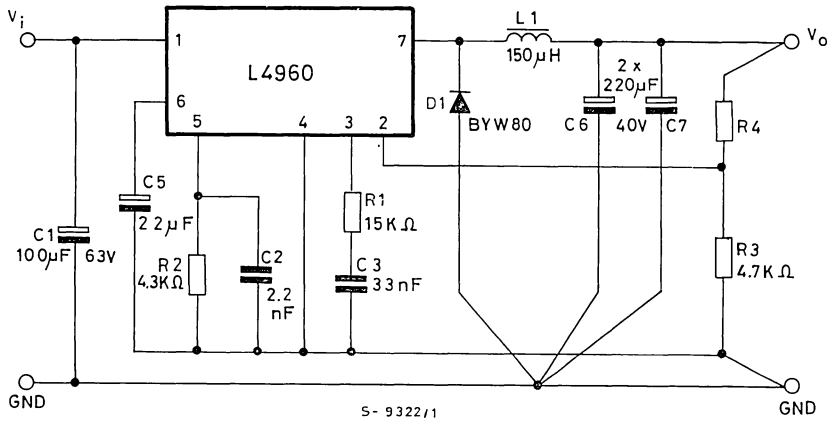


Fig. 23 - Efficiency vs. output voltage



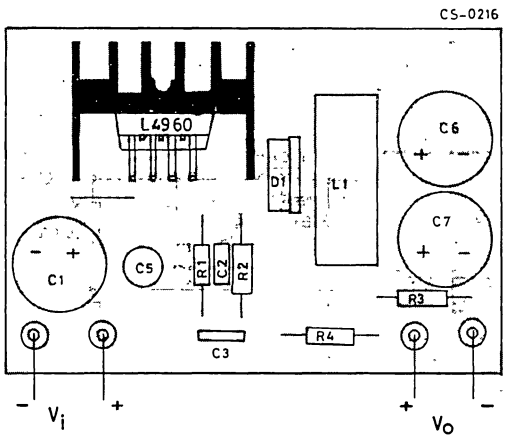
APPLICATION INFORMATION

Fig. 24 - Typical application circuit



C_1, C_6, C_7: EKR (ROE)
D_1: BYW80 OR 5A SCHOTTKY DIODE
SUGGESTED INDUCTOR: L_1 = 150µH at 5A
CORE TYPE: MAGNETICS 58206 - A2 - MPP
N° TURNS: 45, WIRE GAUGE: 0.8mm (20 AWG), COGEMA 946042
U15/GUP15: N° TURNS: 60, WIRE GAUGE: 0.8mm (20 AWG), AIR GAP: 1mm, COGEMA 969051.

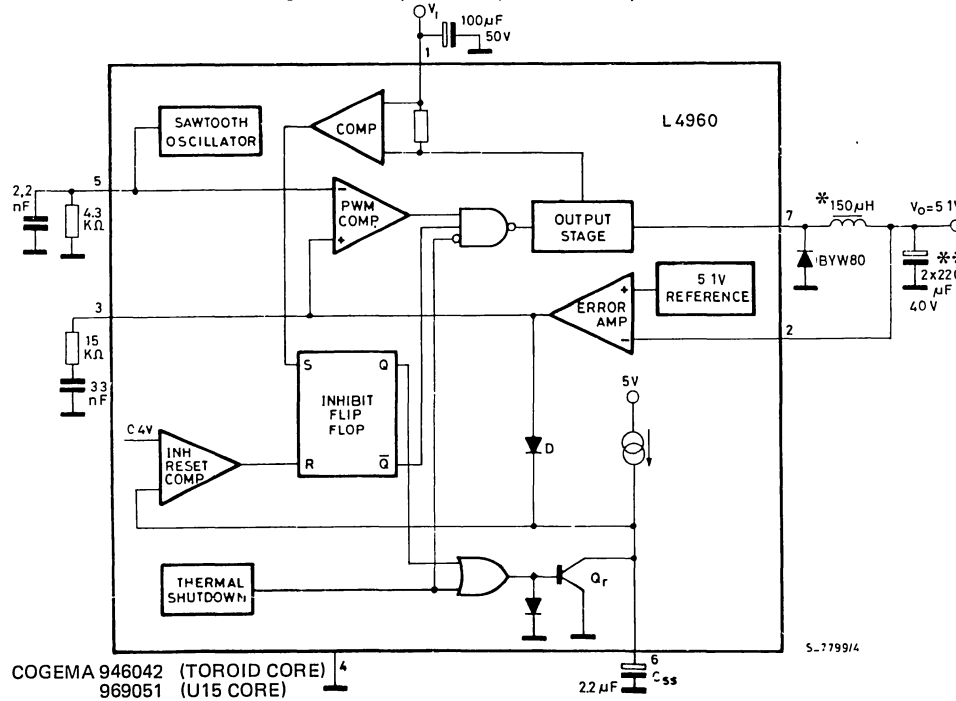
Fig. 25 - P.C. board and component layout of the Fig. 24 (1 : 1 scale)



Resistor values for standard output voltages		
V_o	R3	R4
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

APPLICATION INFORMATION (continued)

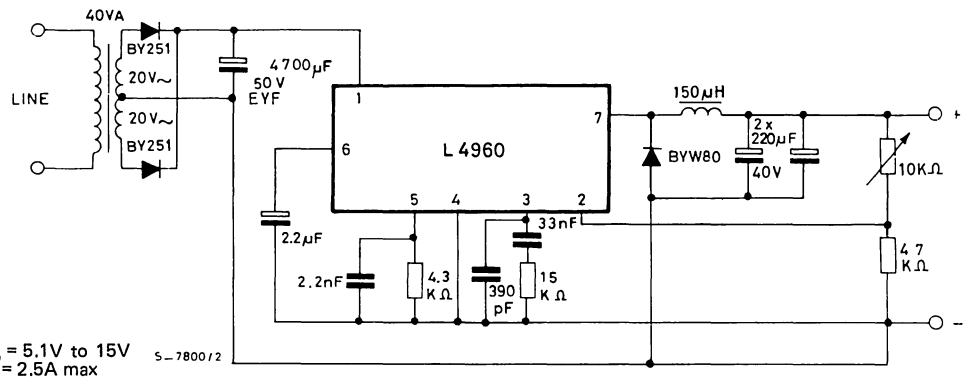
Fig. 26 - A minimal 5.1V fixed regulator; Very few component are required



* COGEMA 946042 (TOROID CORE)
969051 (U15 CORE)

** EKR (ROE)

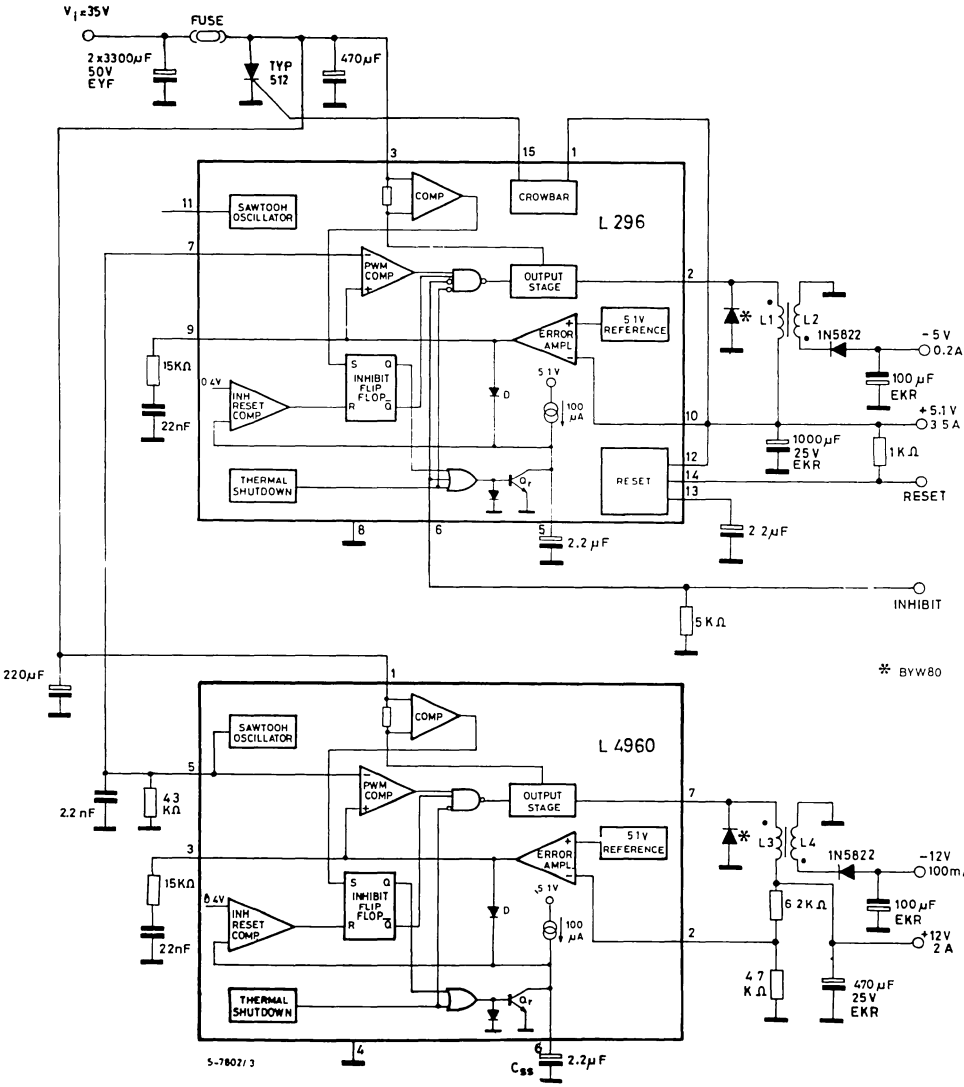
Fig. 27 - Programmable power supply



V_o = 5.1V to 15V
I_o = 2.5A max
Load regulation (1A to 2A) = 10mV (V_o = 5.1V)
Line regulation (220V ± 15% and to I_O = 1A) = 15mV (V_o = 5.1V)

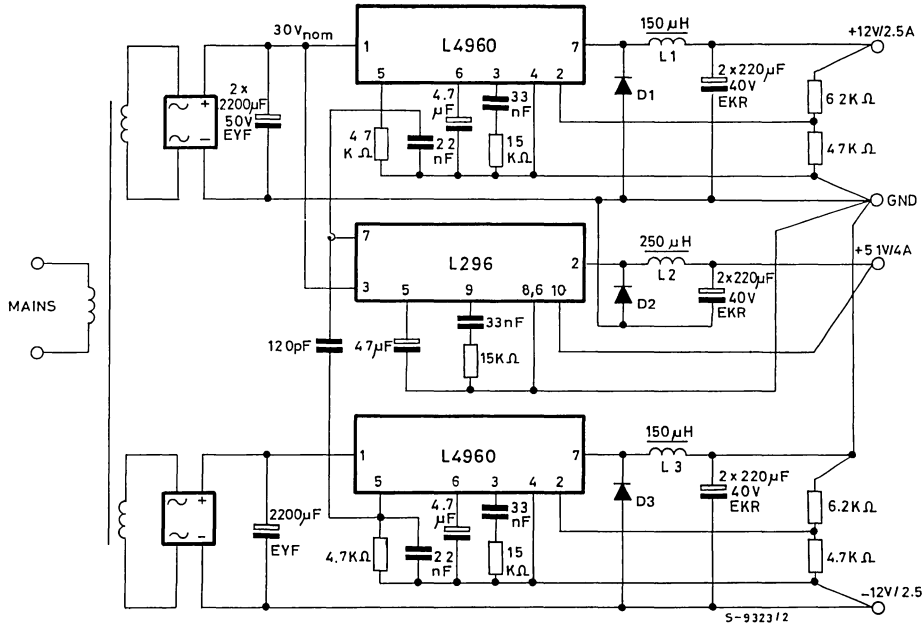
APPLICATION INFORMATION (continued)

Fig. 28 – Microcomputer supply with + 5.1V, -5V, +12V and -12V outputs



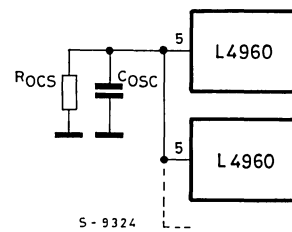
APPLICATION INFORMATION (continued)

Fig. 29 - DC-DC converter 5.1V/4A, ± 12V/2.5A; a suggestion how to synchronize a negative output



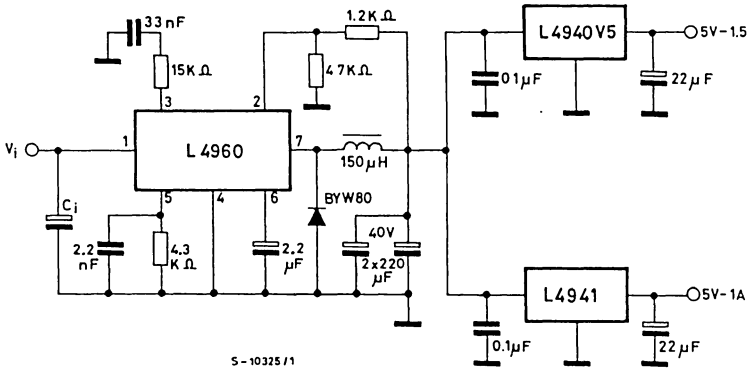
L1, L3 = COGEMA 946042 (969051)
L2 = COGEMA 946044 (946045)
D_1, D_2, D3 = BYW80

Fig. 30 - In multiple supplies several L4960s can be synchronized as shown



APPLICATION INFORMATION (continued)

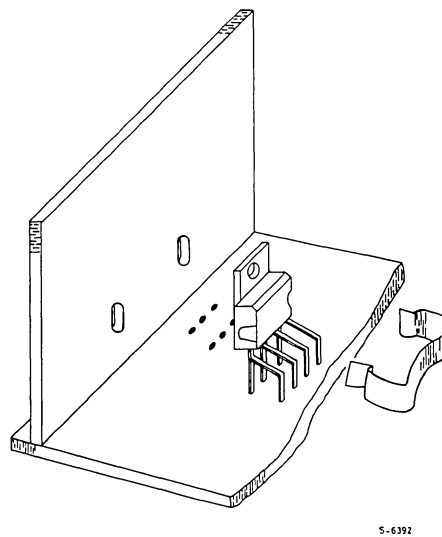
Fig. 31 - Regulator for distributed supplies



MOUNTING INSTRUCTION

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the Heptawatt package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact, no electrical isolation is needed between the two surfaces.

Fig. 32 - Mounting example



1.5A POWER SWITHING REGULATOR

PRELIMINARY DATA

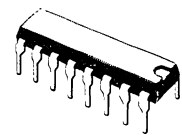
- 1.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- PRECISE (± 2 %) ON-CHIP REFERENCE
- HIGH SWITCHING FREQUENCY
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT-START
- INTERNAL LIMITING CURRENT
- THERMAL SHUTDOWN

The L4962 is a monolithic power switching regulator delivering 1.5A at a voltage veriable from 5V to 40V in step down configuration.

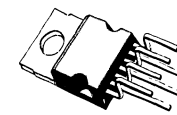
Features of device include current limiting, soft start, thermal protection and 0 to 100% duty cycle for continuous operating mode.

The L4962 is mounted in a 16-lead Powerdip plastic package and Heptawatt package and requires very few external components.

Efficient operation at switching frequencies up to 150KHz allows a reduction in the size and cost of external filter components.



Powerdip
(12 + 2 + 2)



Heptawatt

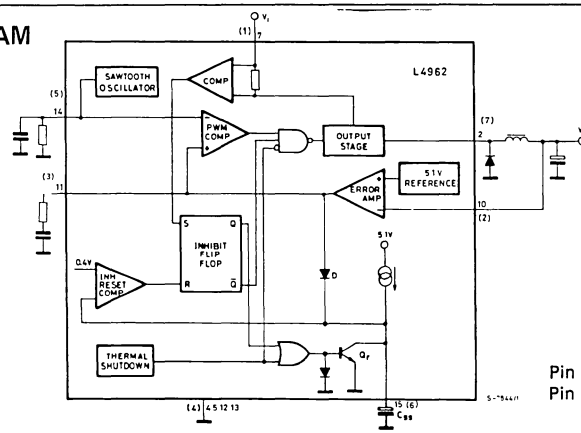
ORDERING NUMBER:

L4962 (12 + 2 + 2 Powerdip)
L4962E (Heptawatt)
L4962EH (Horizontal Heptawatt)

ABSOLUTE MAXIMUM RATINGS

V_7	Input voltage	50	V
$V_7 - V_2$	Input to output voltage difference	50	V
V_2	Negative output DC voltage	-1	V
	Output peak voltage at t = 0.1μs, f = 100KHz	-5	V
V_{11}, V_{15}	Voltage at pin 11, 15	5.5	V
V_{10}	Voltage at pin 10	7	V
I_{11}	Pin 11 sink current	1	mA
I_{14}	Pin 14 source current	20	mA
P_{tot}	Power dissipation at $T_{pins} \leqslant 90°C$ (Powerdip)	4.3	W
	$T_{case} \leqslant 90°C$ (Heptawatt)	15	W
T_j, T_{stg}	Junction and storage temperature	-40 to 150	°C

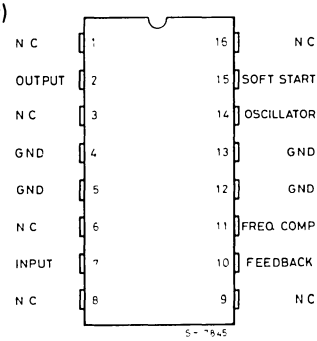
BLOCK DIAGRAM

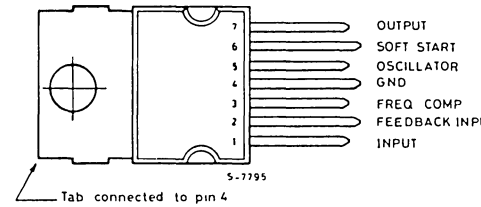


Pin X = Powerdip
Pin (X) = Heptawatt

CONNECTION DIAGRAMS

(Top view)





THERMAL DATA

			Heptawatt	Powerdip
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4°C/W	—
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	—	14°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50°C/W	80°C/W*

* Obtained with the GND pins soldered to printed circuit with minimized copper area.

PIN FUNCTIONS

HEPTAWATT	POWERDIP	NAME	FUNCTION
1	7	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the internal logic.
2	10	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
3	11	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
4	4, 5, 12, 13	GROUND	Common ground terminal.
5	14	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency. This pin must be connected to pin 7 input when the internal oscillator is used.
6	15	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. The capacitor also determines the average short circuit output current.
7	2	OUTPUT	Regulator output.
	1, 3, 6, 8, 9, 16		N.C.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_j = 25°C$, $V_I = 35V$, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS						
V_o	Output voltage range	$V_I = 46V$ $I_o = 1A$	V_{ref}		40	V
V_I	Input voltage range	$V_o = V_{ref}$ to 36V $I_o = 1.5A$	9		46	V
ΔV_o	Line regulation	$V_I = 10V$ to 40V $V_o = V_{ref}$ $I_o = 1A$		15	50	mV
ΔV_o	Load regulation	$V_o = V_{ref}$ $I_o = 0.5A$ to 1.5A		8	20	mV
V_{ref}	Internal reference voltage (pin 10)	$V_I = 9V$ to 46V $I_o = 1A$	5	5.1	5.2	V
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of refer. voltage	$T_j = 0°C$ to $125°C$ $I_o = 1A$		0.4		mV/°C
V_d	Dropout voltage	$I_o = 1.5A$		1.5	2	V
I_{om}	Maximum operating load current	$V_I = 9V$ to 46V $V_o = V_{ref}$ to 36V	1.5			A
I_{2L}	Current limiting threshold (pin 2)	$V_I = 9V$ to 46V $V_o = V_{ref}$ to 36V	2		3.3	A
I_{SH}	Input average current	$V_I = 46V$; output short-circuit		15	30	mA
η	Efficiency	f = 100KHz $V_o = V_{ref}$		70		%
		$I_o = 1A$ $V_o = 12V$		80		%
SVR	Supply voltage ripple rejection	$\Delta V_I = 2V_{rms}$ $f_{ripple} = 100Hz$ $V_o = V_{ref}$ $I_o = 1A$	50	56		dB
f	Switching frequency		85	100	115	KHz
$\frac{\Delta f}{\Delta V_I}$	Voltage stability of switching frequency	$V_I = 9V$ to 46V		0.5		%
$\frac{\Delta f}{\Delta T_j}$	Temperature stability of switching frequency	$T_j = 0°C$ to $125°C$		1		%
f_{max}	Maximum operating switching frequency	$V_o = V_{ref}$ $I_o = 1A$	120	150		KHz
T_{sd}	Thermal shutdown junction temperature			150		°C

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
DC CHARACTERISTICS							
I_{7Q}	Quiescent drain current	100% duty cycle pins 2 and 14 open	V_I = 46V		30	40	mA
		0% duty cycle			15	20	mA
$-I_{2L}$	Output leakage current	0% duty cycle				1	mA
SOFT START							
I_{15SO}	Source current			100	130	160	μA
I_{15SI}	Sink current			50	70	120	μA
ERROR AMPLIFIER							
V_{11H}	High level output voltage	V_{10} = 4.7V	I_{11} = 100μA	3.5			V
V_{11L}	Low level output voltage	V_{10} = 5.3V	I_{11} = 100μA			0.5	V
I_{11SI}	Sink output current	V_{10} = 5.3V		100	150		μA
$-I_{11SO}$	Source output current	V_{10} = 4.7V		100	150		μA
I_{10}	Input bias current	V_{10} = 5.2V			2	10	μA
G_V	DC open loop gain	V_{11} = 1V to 3V		46	55		dB
OSCILLATOR							
$-I_{14}$	Oscillator source current			5			mA

CIRCUIT OPERATION (refer to the block diagram)

The L4962 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 1.5A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2%).

This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.

The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 11. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{ss} and allowed to rise, linearly, as this capacitor is charged by a constant current source. Output overload protection is provided in the form of a current limiter. The load current is sensed by a internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V.

The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network. The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

Fig. 1 - Soft start waveforms

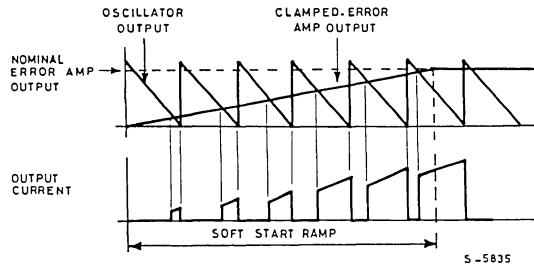


Fig. 2 - Current limiter waveforms

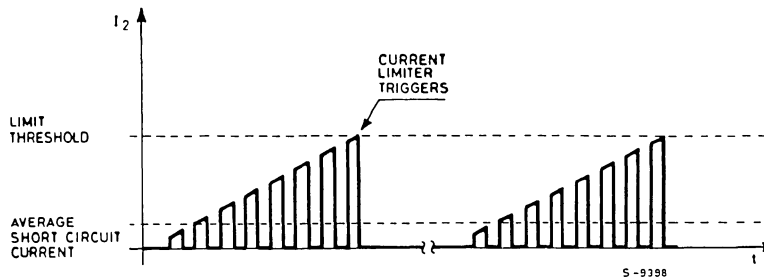
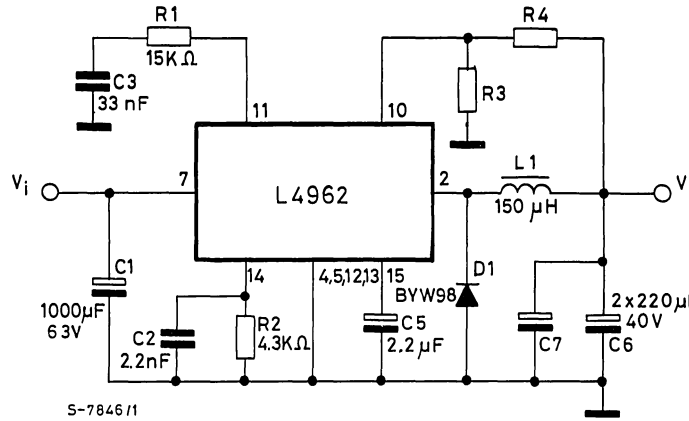


Fig. 3 - Test and application circuit (Powerdip)



1) D_1: BYW98 or 3A Schottky diode, 45V of VRRM;
2) L_1: CORE TYPE - MAGNETICS 58120 - A2 MPP
   N° TURNS 45, WIRE GAUGE: 0.8mm (20 AWG)
3) C_6, C_7: ROE, EKR 220μF 40V

Fig. 4 - Quiescent drain current vs. supply voltage (0% duty cycle)

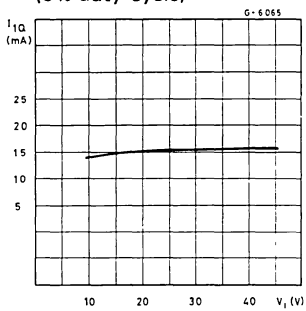


Fig. 5 - Quiescent drain current vs. supply voltage (100% duty cycle)

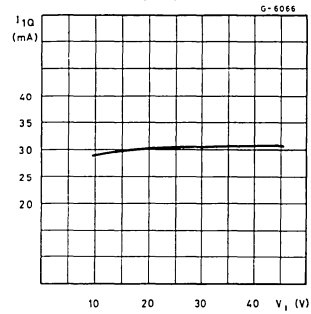


Fig. 6 - Quiescent drain current vs. junction temperature (0% duty cycle)

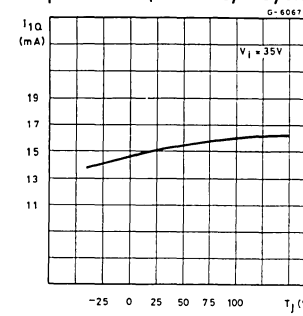


Fig. 7 - Quiescent drain current vs. junction temperature (100% duty cycle)

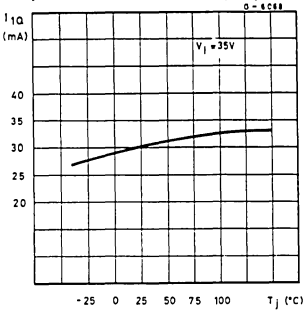


Fig. 8 - Reference voltage (pin 10) vs. V_I rdip) vs. V_I

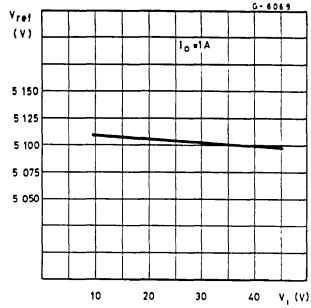


Fig. 9 - Reference voltage (pin 10) vs. junction temperature

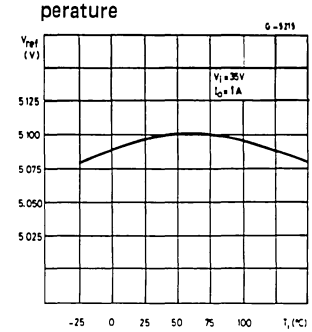


Fig. 10 - Open loop frequency and phase response of error amplifier

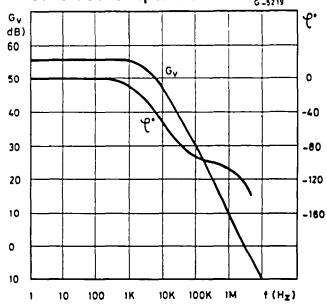


Fig. 11 - Switching frequency vs. input voltage

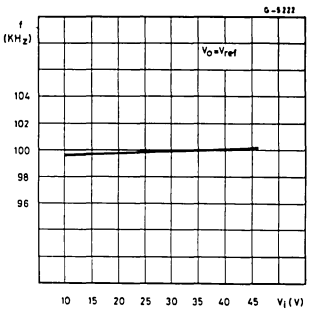


Fig. 12 - Switching frequency vs. junction temperature

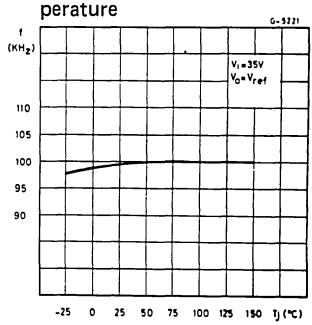


Fig. 13 - Switching frequency vs. R2 (see test circuit)

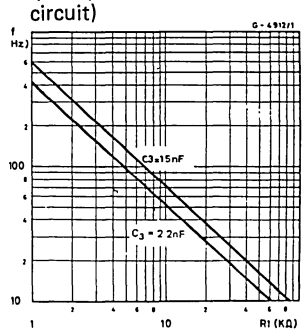


Fig. 14 - Line transient response

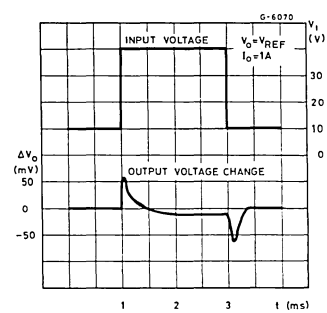


Fig. 15 - Load transient response

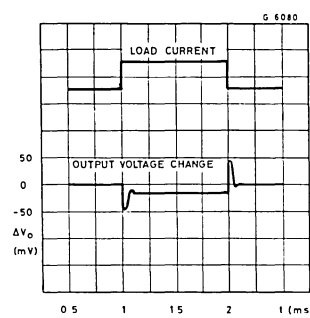


Fig. 16 - Supply voltage ripple rejection vs. frequency

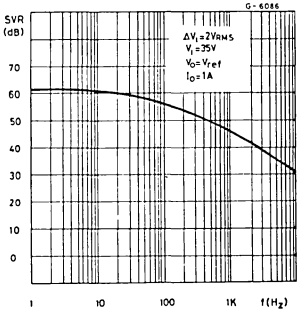


Fig. 17 - Dropout voltage between pin 7 and pin 2 vs. current at pin 2

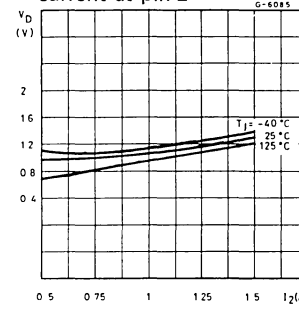


Fig. 18 - Dropout voltage between pin 7 and 2 vs. junction temperature

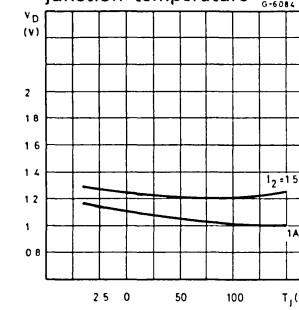


Fig. 19 - Efficiency vs. output current

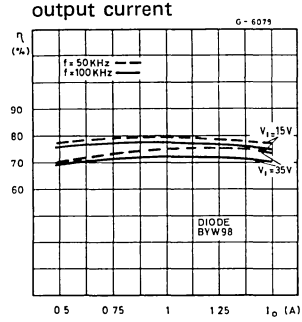


Fig. 20 - Efficiency vs. output current

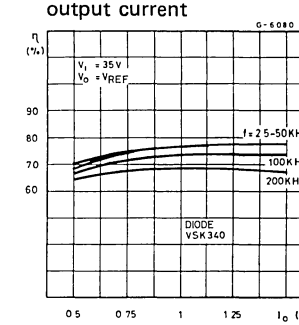


Fig. 21 - Efficiency vs. output current

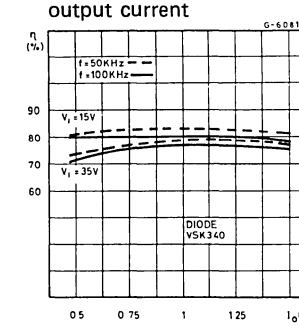


Fig. 22 - Efficiency vs. output voltage

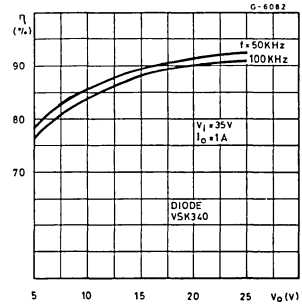


Fig. 23 - Efficiency vs. output voltage

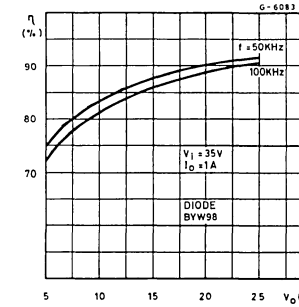
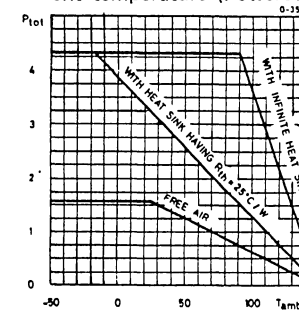
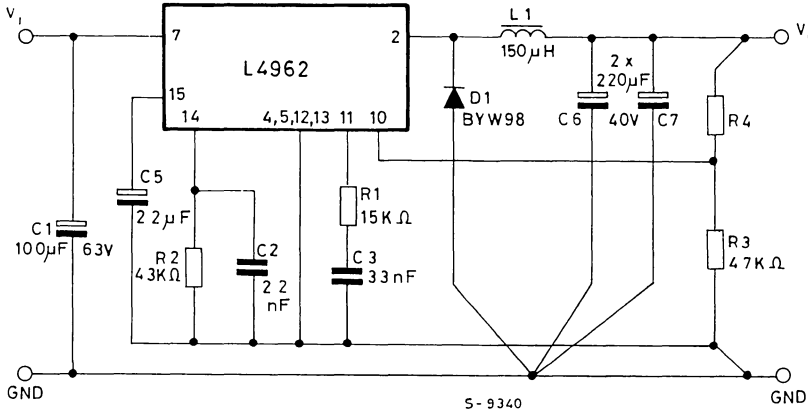


Fig. 24 - Maximum allowable power dissipation vs. ambient temperature (Powerdip)



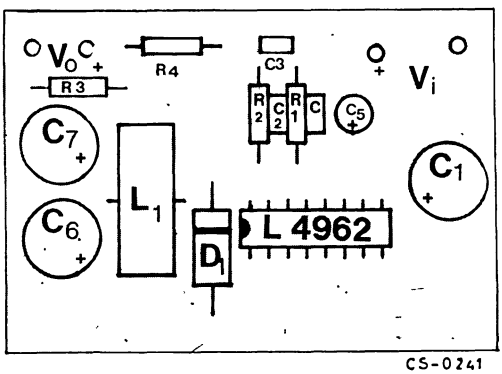
APPLICATION INFORMATION

Fig. 25 - Typical application circuit



C_1, C_6, C_7: EKR (ROE)
D_1: BYW98 OR VISK340 (SCHOTTKY)
SUGGESTED INDUCTORS (L_1): MAGNETICS 58120 - A2MPP - 45 TURNS - WIRE GAUGE 0.8mm (20AWG) - COGEMA 946043
OR U15, GUP15, 60 TURNS 1mm, AIR GAP 0.8mm (20AWG) - COGEMA 969051

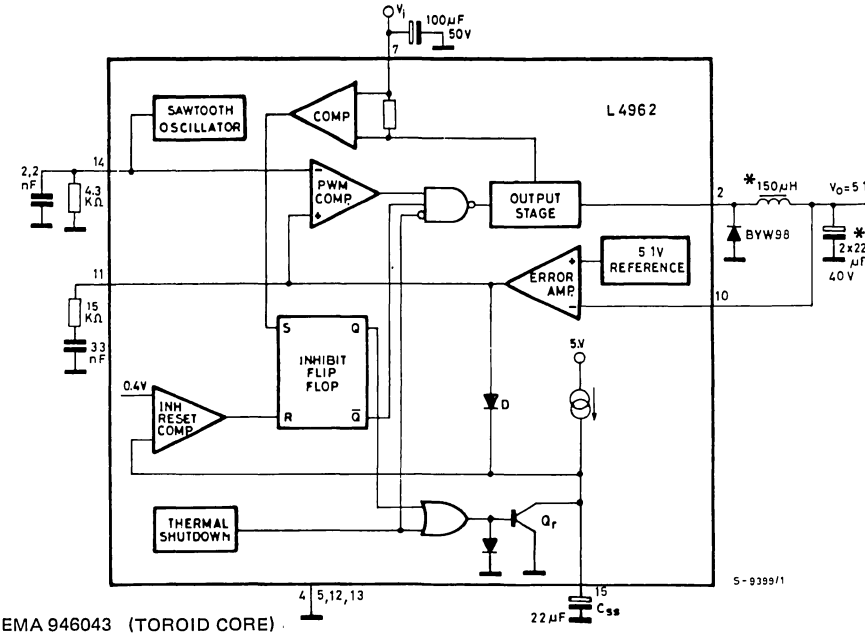
Fig. 26 - P.C. board and component layout of the circuit of Fig. 25 (1 : 1 scale)



Resistor values for standard output 7 voltages		
V_o	R3	R4
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

APPLICATION INFORMATION (continued)

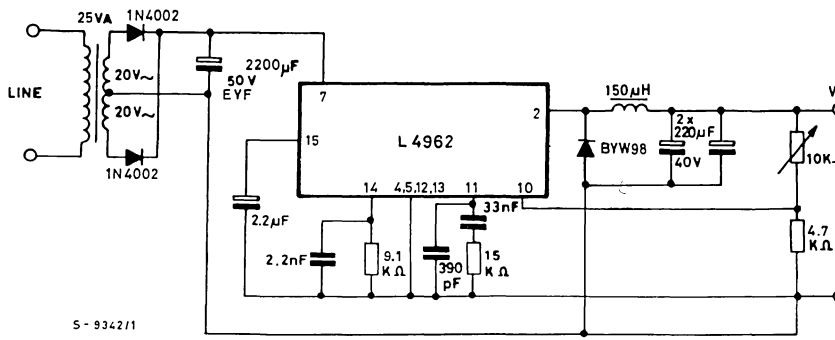
Fig. 27 - A minimal 5.1V fixed regulator; very few components are required



* COGEMA 946043 (TOROID CORE)
969051 (U15 CORE)

** EKR (ROE)

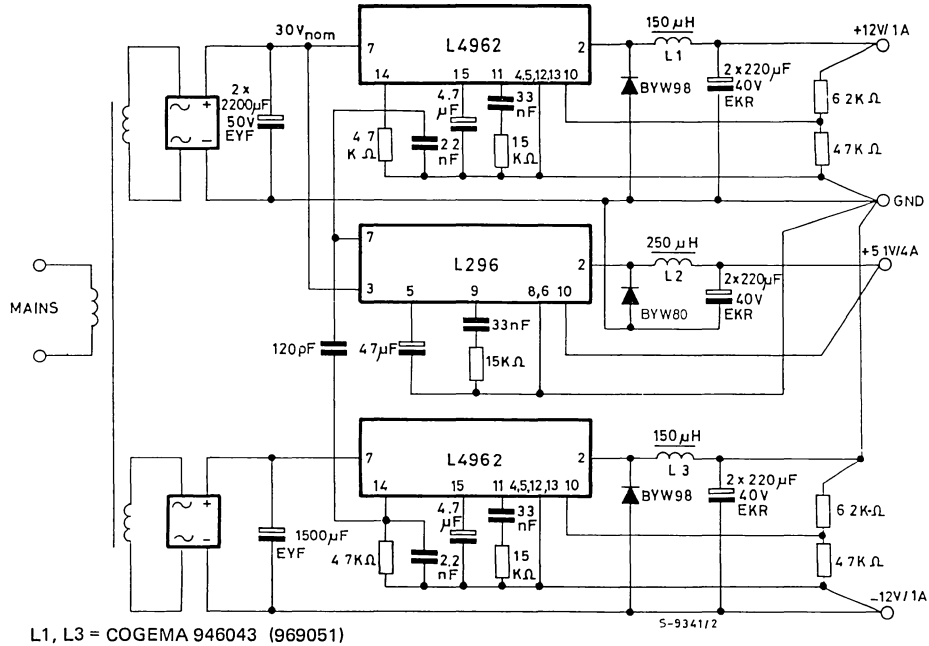
Fig. 28 - Programmable power supply



V_O = 5.1V to 15V
I_O = 1.5A max
Load regulation (0.5A to 1.5A) = 10mV (V_O = 5.1V)
Line regulation (220V ± 15% and to I_O = 1A) = 15mV (V_O = 5.1V)

APPLICATION INFORMATION (continued)

Fig. 29 - DC-DC converter 5.1V/4A, ± 12V/1A. A suggestion how to synchronize a negative output



L1, L3 = COGEMA 946043 (969051)
L2 = COGEMA 946044 (946045)

Fig. 30 - In multiple supplies several L4962s can be synchronized as shown

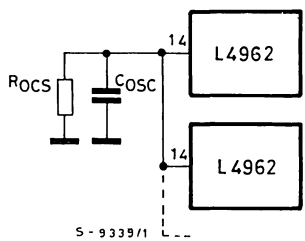
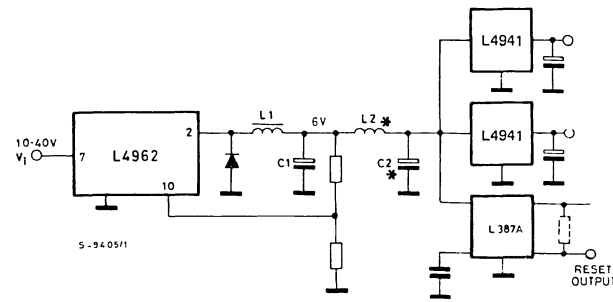


Fig. 31 - Preregulator for distributed supplies



* L2 and C2 are necessary to reduce the switching frequency spikes when linear regulators are remote from L4962

MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the L4962 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 32).
The diagram of figure 33 shows the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having the thickness of 35μ (1.4 mils). During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 32 - Example of P.C. board copper area which is used as heatsink

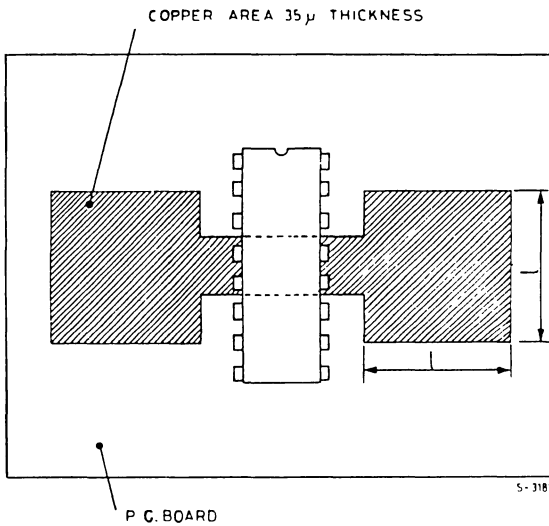
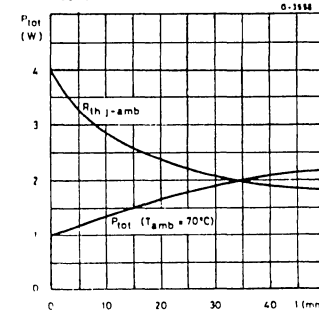


Fig. 33 - Maximum dissipable power and junction to ambient thermal resistance vs. side "ℓ"



SOLENOID CONTROLLER

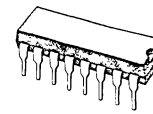
- DRIVES ONE OR TWO EXTERNAL DARLINGTONS
- DUAL AND SINGLE LEVEL CURRENT CONTROL
- SWITCHMODE CURRENT REGULATION
- ADJUSTABLE PEAK DURATION
- WIDE SUPPLY RANGE (4.75-46 V)
- TTL-COMPATIBLE LOGIC INPUTS
- THERMAL PROTECTION

DESCRIPTION

The L5832 Solenoid Controller is designed for use with one or two external darlington transistors in solenoid and relay driving applications.The device is controlled by two logic inputs and features switchmode regulation of the load current. A key feature of the L5832 is flexibility.

It can be used with a variety of darlingtons to match the requirements of the load and it allows both simple and two level current control Moreover, the drive waveshape can be adjusted by external components. Other features of the device include thermal shutdown, a supply voltage range of 4.75-46 V and TLL-compatible inputs.

The L5832 is supplied in a 12 + 2 + 2 – lead Powerdip package which use the four center pins to conduct heat to the PC board copper.



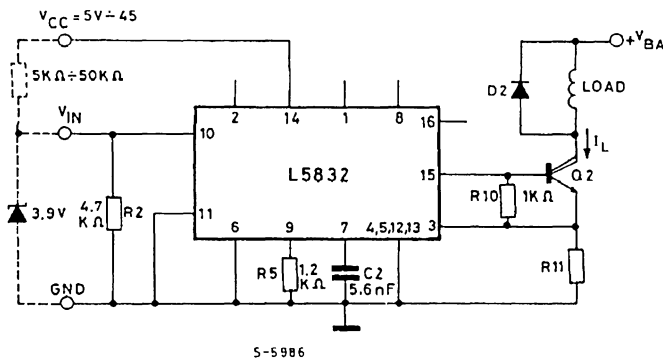
Powerdip
12 + 2 + 2

ORDER CODE : L5832

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	80	°C/W

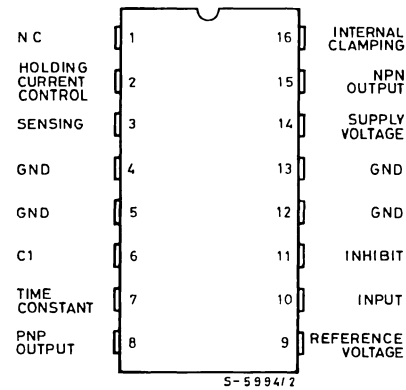
APPLICATION CIRCUIT USING ONE DARLINGTON



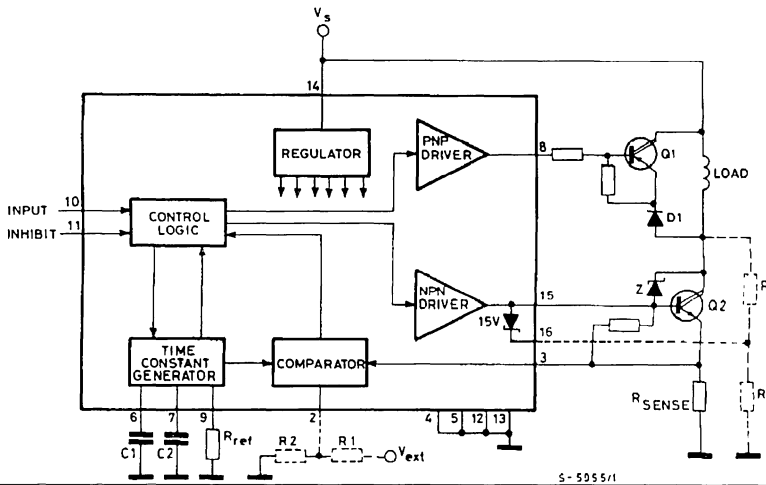
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage	46	V
V_8	Positive Transient Voltage at Pin 8	60	V
V_{en}	Enable Input Voltage (pin 11)	7	V
V_I	Input Voltage (pin 10)	7	V
V_R	External Reference Voltage (pin 2)	2	V
P_d	Power Dissipation (T_{case} = 80 °C)	5	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

CONNECTION DIAGRAM



BLOCK DIAGRAM



PIN FUNCTIONS

N°	Name	Function
1	NC	Not Connected. Must be left open circuit.
2	HOLDING CURRENT CONTROL	A voltage applied to this pin sets the holding current level. If left open circuit an internal 75 mV reference is used and $I_h = I_p/6$
3	SENSING	Connection for Load Current Sense Resistor. Value sets the maximum load current $I_p = 0\ 45/R_s$.
4	GROUND	Ground Connection. With pins 5, 12 and 13 conducts heat to printed circuit board copper.
5	GROUND	See Pin 4
6	C1	A capacitor connected between this pin and ground sets the duration of the current peak (t2 in fig.3). If left open, the switchmode control of the peak is suppressed. If grounded, the current does not fall to the holding level.
7	DISCHARGE TIME CONSTANT	A capacitor connected between this pin and ground sets the duration of t_{off} (fig.3). If grounded, switchmode control is suppressed.
8	PNP DRIVING OUTPUT	Current Drive Output for External PNP Darlington (for recirculation). $I = 35\ I_{ref}$
9	REFERENCE VOLTAGE	A resistor connected between this pin and ground sets the internal current reference, I_{ref}. The recommended value is 1.2kΩ, giving $I_{Ref} = 1$ mA.
10	INPUT	TTL - Compatible Input. A high level on this pin activates the output, driving the load.
11	INHIBIT	TTL - Compatible Inhibit Input. A high level on this input disables the output stages and logic circuitry, irrespective of the state of pin 10.
12	GROUND	See Pin 4
13	GROUND	See Pin 4
14	SUPPLY VOLTAGE	Supply Voltage Input
15	NPN DRIVING OUTPUT	Current Drive for External NPN Darlington (in series with the load). $I = 100\ I_{ref}$
16	INTERNAL CLAMPING	Internal Zener Clamp Avaible for Fast Turnoff.

ELECTRICAL CHARACTERISTICS ($V_{S\,(pin\ 14)}$ = 14 V , T_{amb} = 25 °C, R_{ref} = 1.2 KΩ, unless otherwise specified. Refer to Fig.2)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage (pin 14)			4.75		46	V
I_S	Quiescent Current (pin 14)	$V_{pin\ 10} = V_{pin\ 11}$ = Low State			21	40	mA
V_{in}	Input Voltage (pin 10)	Low State				0.8	V
V_{en}	Enable Input Voltage (pin 11)	High State		2.4			V
I_{in}	Input Current (pin 10)	Low State				100	µA
I_{en}	Enable Input Current (pin 11)	High State				10	µA
V_{ref}	Internal Reference Voltage (pin 9)			1.2	1 25	1.3	V
I_{ref}	Reference Current (pin 9)	$I_{ref} = V_{ref}/R_{ref}$ R_{ref} = 1.2 KΩ				1 300	µA
I_{pd}	Peak Duration Control Current (pin 6)	$I_{pd} = I_{ref}/8$		110	130	180	µA
t_{pd}	Peak Duration Time (pin 6)	$t_{pd} = C1\ V_{Th}/I_{pd}$ V_{th} = 1.4V C_1 = 4.7 nF			500		µs
I_{od}	Off Duration Control Current (pin 7)	$I_{od} = I_{ref}$ / 8		110	130	180	µA
t_{off}	Off Duration Time (pin 7)	$t_{od} = C2\ V_{th}/I_{od}$ V_{th} = 1.4V C2 = 4.7 nF			50		µs
I_{d1}	NPN Driving Current (pin 15)	I_{d1} = 100 I_{ref} (only present during charging phase)		80	100	130	mA
I_{d2}	PNP Driving Current (pin 8)	I_{d2} = 35 I_{ref}		28	35	48	mA
I_p	Peak Current (emitter of NPN Darlington)	I_p = 450 mV/R_{sens} R_{sens} = 0.1 Ω		4.2	4.5	4.8	A
V_h	Holding Current Control Voltage	$V_h = R_{sens}\ I_h$ I_h = Emitter Current of NPN Darlington	Pin 2 Floating	70	75	85	mV
			Pin 2 Externally Biased			2	V
R_{in}	Holding Current Control Input Impedance (Pin 2)			100	150	200	Ω
r	Peak to Hold Current Ratio	Pin 2 Floating		5.8	6	6.2	
			Pin 6 Shorted	0.97	1	1.03	
I_B	Sense Input Bias Current (Pin 3)					100	µA
V_{clamp}	Internal Clamping (Pin 16 to 15)	I = 200 µA		14	16	18	V
V_{dt}	Dump Protection Threshold Voltage (Pin 1)			28	32	34	V
R_{dt}	Dump Protection Threshold Input Impedance (Pin 1)			22	32	42	KΩ
	Thermal Drift of Reference Voltage				0.5		mV/°C

APPLICATION INFORMATION

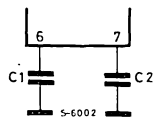
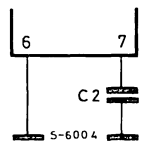
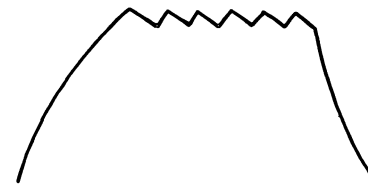
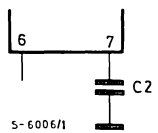
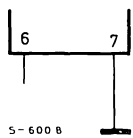
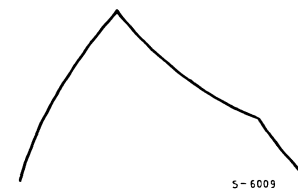
The L5832 solenoid controller is intended for use with one or two external darlington transistors to drive inductive loads such as solenoids, relays, electric valves and DC motors.

Controlled by a logic input and an inhibit input (both TTL compatible), the device drives the external darlington (s) to produce a load current waveform as shown in figure 3. This basic waveform shows that the device produces an initial current peak followed by a lower holding current. Both the peak and holding current levels are regulated by the L5832's switchmode circuitry .

The duration of the peak, the peak current level and holding current level can all be adjusted by external components.

Moreover, by omitting C1, C2 or both it is possible to realize single-level current control, a transitory peak followed by a regulated holding current or a simple peak (figure 1).

Figure 1 : Components Connected to Pins 6 and 7 Determine the Load Current Waveshape.

COMPONENTS ON PINS 6 AND 7	LOAD CURRENT WAVEFORM
	
	
	
	

The peak current level I_p, is set by the sensing resistor, R_{sens}, and is found from :

$$I_p = \frac{0.45}{R_{sens}}$$

The holding current level, I_h, is set by a voltage applied to pin 2. If this pin is left open circuit an internal reference of 75 mV supervenes and the holding current is given by :

$$I_h = \frac{I_p}{6}$$

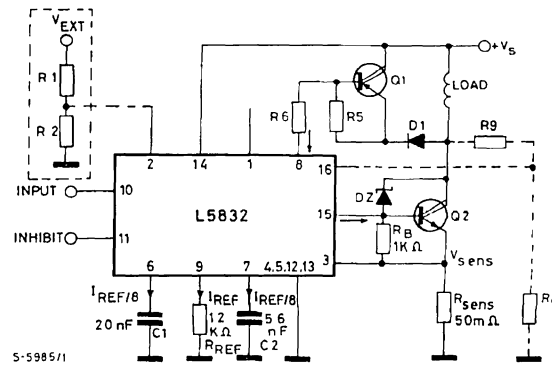
Alternatively, this level may be varied by adding a divider to pin 2 (R1, R2) and suitable values are found from :

$$\frac{I_{h\,max}}{I_p} = \frac{1}{0\,45\ V}\left(\frac{R2\ //\ R_{in}}{R1 + R2\ //\ R_n}\ Vext + \frac{R2\ //\ R_{in}}{Rx = R2\ //\ R_{in}}\ Vx\right)$$

where Vx = 3V, Rx = 5850Ω. R_{in} = 150Ω (R_{in} of pin 2) and V_{ext} is the external voltage applied to the divider.

Figure 2 : Application Circuit Showing all the Optional Components. In Particular it Illustrates how the Holding Current Level is Adjusted Independently of the Peak Current (with R1, R2, V_{ext}) and how the Internal Zener Clamp is Connected. This Circuit Produces the Waveforms Shown in Fig.3.

I_o (A)	Q1	Q2
4	BDX54	BDX53
8	BDW94	BDW93
12	BDV64	BDV65



The drive currents for the two darlingtons and the waveform time constants are all defined by a reference current, I_{ref}, which is defined in turn by a resistor between pin 9 and ground.

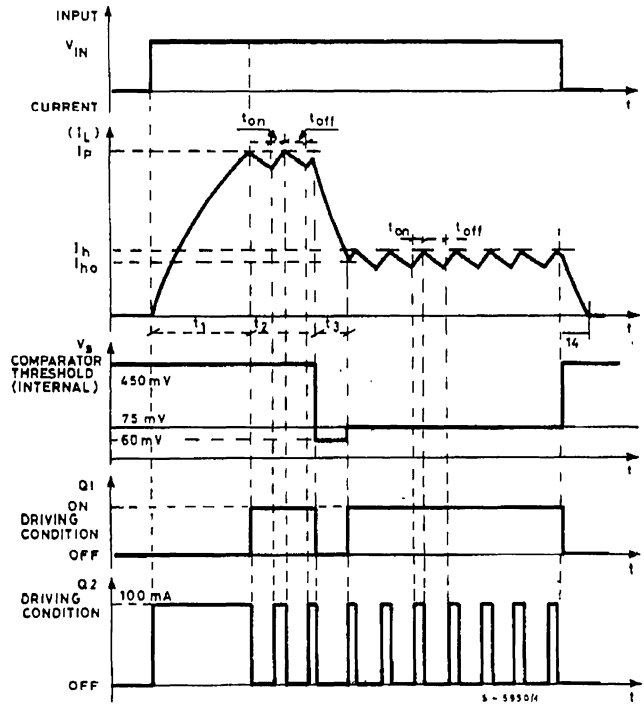
The recommended value for I_{ref} is 1 mA which is obtained with a 1.2 kΩ resistor. From I_{ref} the darlington drive currents are given by :

PNP : I = 35 I_{ref}
NPN : I = 100 I_{ref}

The duration of the high current level (t2 in figure 3) is set by a capacitor connected between pin 6 and ground.This capacitor, C1, is related to the duration, T, by :

$$C1 = \frac{I_{ref}\ T}{12}$$

Figure 3 : Waveforms of the Typical Application Circuit of Fig. 2.



The discharge time constant (t_{off} in figure 3) is set by a capacitor between pin 7 and ground and is found from :

$$t_{off} = \frac{12C2}{I_{ref}}$$

The t_{off} and t_{on} times are also related to the current ripple , ΔI :

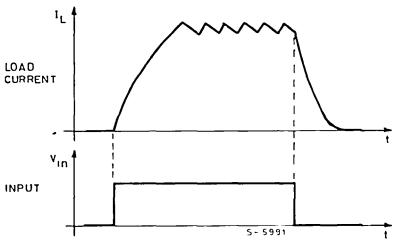
$$t_{off} = \frac{L\Delta I}{V_{off}} \quad \text{and } t_{on} = \frac{L\Delta I}{V_{on}}$$

where $V_{off} = V_{diode} + V_{CEQ1} + R_L I_L$
$V_{on} = V_s - V_{CEQ2} - V_{RS} - R_L I_L$
L = load inductance
R_L = load resistance
Δ I = load current ripple.

Note that t_{off} is the same for both the peak and holding currents.

Figure 4 : When Pin 6 in Grounded, as Shown here, the Load Current is Regulated at a Single Level.

I_o(A)	Q1	Q2
4	BDX54	BDX53
8	BDW94	BDW93
10	BDV64	BDV65



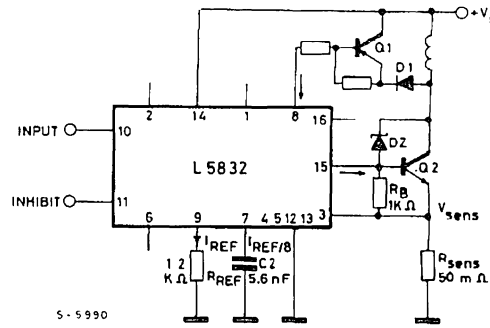
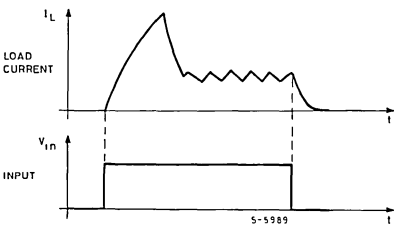


Figure 5 : In this Application Circuit, Pin 6 is Left Open to Give a Single Peak Followed by a Regulated Holding Current.

I_o(A)	Q1	Q2
4	BDX54	BDX53
8	BDX54	BDX53
16	BDW94	BDV65



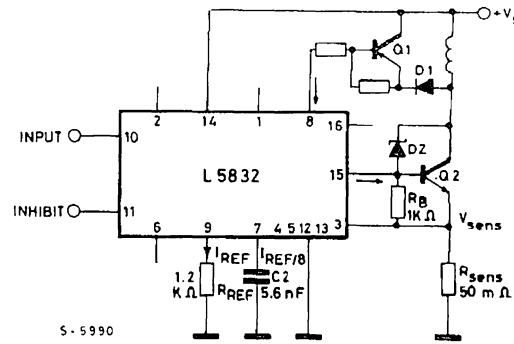
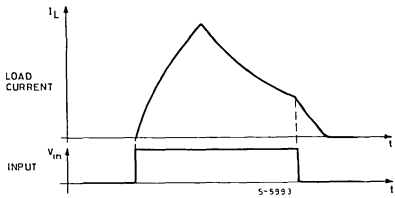
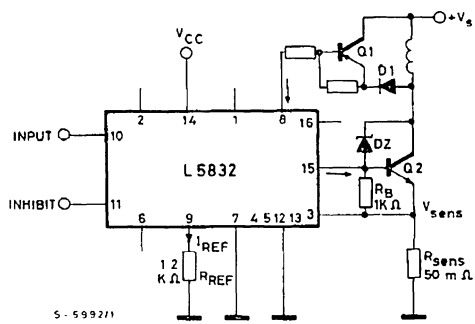


Figure 6 : Switchmode Control of the Current can be Suppressed Entirely by Leaving Pin 6 Open and Grounding Pin 7. The Peak Current is still Controlled.

I_o(A)	Q1	Q2
4	BDX54	BDX53
8	BDW94	BDW93
10	BDV64	BDV65





For fast turnoff an internal zener clamp is available on pin 16.
This is used with an external divider, R8 R9, as shown in figure 2. Suitable values can be found from :

$$V_{pin\ 16} \cong 15V + V_{BEQ2} + VRsense$$

$$V_{CQ2} \cong V_{pin16} \cdot \frac{R9 + R8}{R8}$$

(V_{CQ2} is the voltage at the collector of Q2).

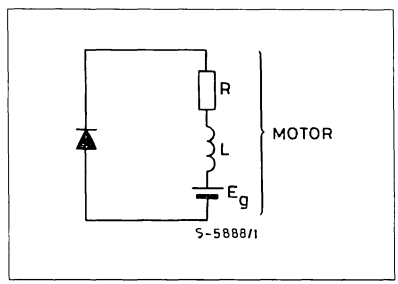
To ensure stability, a small capacitor (about 200 pF) must be connected between the base and collector of Q2 when pin 16 is used.

For the application circuit of figure 7 $t_{off} = 12C2/I_{ref}$, as before, and the current ripple is given by :

$$t_{off} = -\frac{L}{R} \cdot \frac{\ln(I_{LP} - \Delta I) \cdot R_L + V_L}{I_{LP} \cdot R_L + V_L}$$

where V_L is the voltage across the inductor during recirculation.

Note that if the load is a motor $V_L = Eg + V_D$.



Normally Δ I is a design parameter therefore C2 can be calculated directly from :

$$C2 = \frac{-I_{ref} \cdot L}{12\,R_L} \cdot \frac{\ln(I_{LP} - \Delta I)\,R_L + V_L}{I_{LP} \cdot R_L + V_L}$$

This application is particularly important because it allows the use of inductive loads with the lowest possible series resistance (compatible with constructional requirements) and therefore reduces notably the power dissipation.

For example, an electric valve driven from 24V which draws 2A has a series resistance of 12Ω and dissipates 48W . Using this circuit a valve with a 2Ω series resistance can be used and the power dissipation is :

$$Pd = R_L I_L^2 + V_D I_L(1-\delta) + V_{sat} \cdot I_L\,\delta + R_S I_L 2\delta$$

where R_L = resistance of valve = 2Ω
V_D = drop across diode, $V_D \cong 1V$
V_{sat} = saturation voltage of Q2, ≅ 1V
R_S = R11 = 220 mΩ
δ = duty cycle = 20 %

therefore :

$$Pd = 8 + 1.6 + 0.4 + 0.16 = 10.16W$$

This given two advantages : the size (and cost) of the valve is reduced and the drive current is reduced from 2A to about 0.4A.

The same consideration is also true for DC motors.

Figure 7 : Application Circuit Using Only one Darlington. The Resistor and Zener Shown Dotted Activate the Load when Power is Applied.

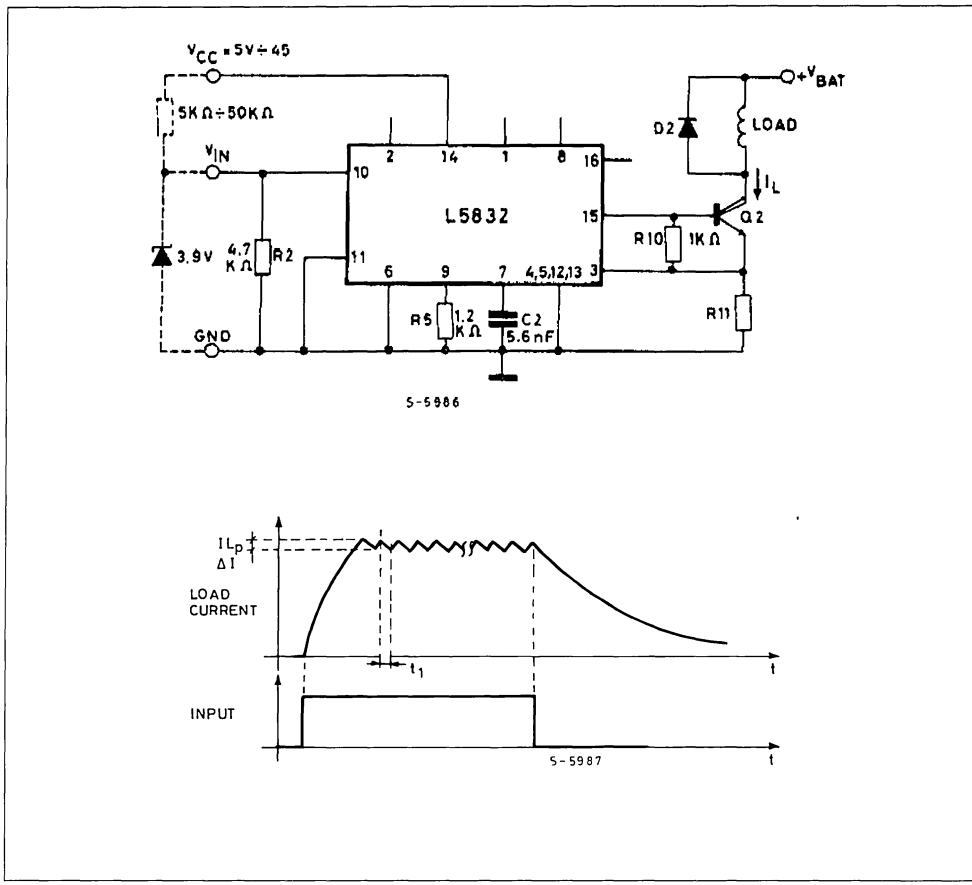


Figure 8: P.C. Board and Component Layout of the Circuit of Fig. 7 (1 : 1 Scale)

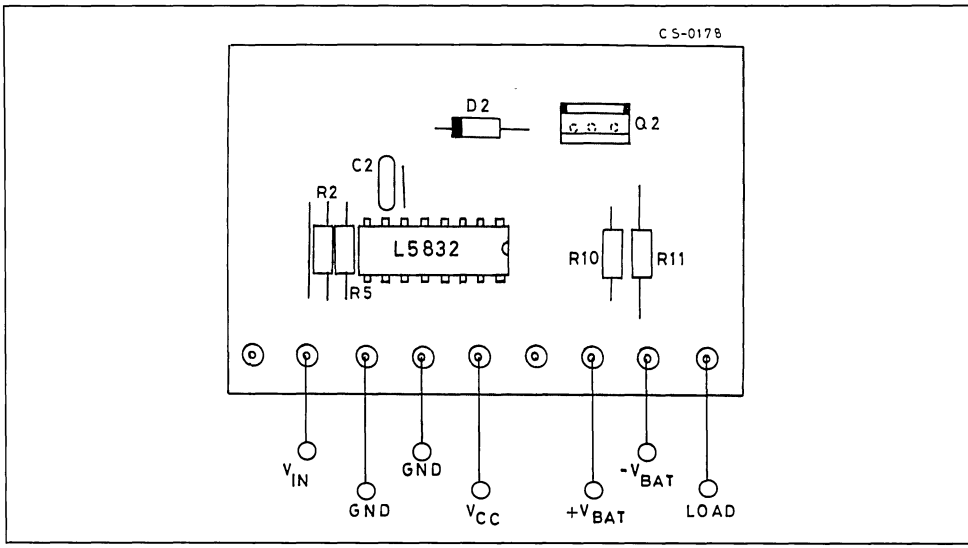
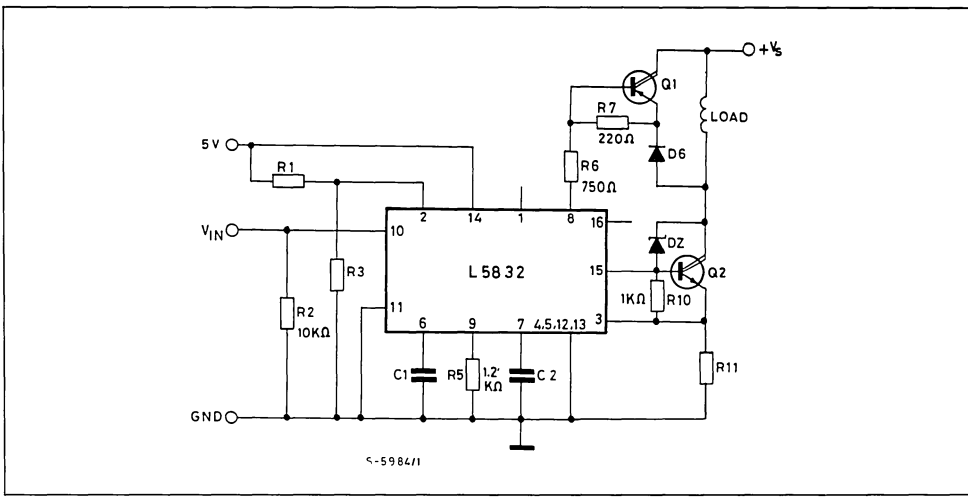


Figure 9: Application Circuit Showing how two Separate Supplies can be Used.



The application circuit of figure 9 is very similar to figure 2 except that it shows the use of two supplies-one for the control circuit, one for the power stage.

Chose R6 so that the voltage on pin 8 does not exceed 46V DC. This can be done simply bearing in mind that the pin 8 current is 35 I_{ref}.

R6 must not be too high if a very low supply voltage is used because:

$$V_{smin} = R6 \cdot 16 + 4.75$$

$$V_{smin} = 750 \cdot 35 \cdot 10^{-3} + 4.75 = 31V$$

The zener diode DZ can not exceed 62V because when Q1 is off and DZ triggered – the fast recirculation – the voltage on pin 8 may not exceed 60 V.

QUAD DARLINGTON SWITCH

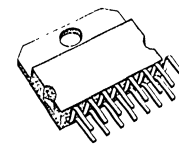
- FOUR NON INVERTING INPUTS WITH ENABLE
- OUTPUT VOLTAGE UP TO 50 V
- OUTPUT CURRENT UP TO 1.8 A
- VERY LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUTS
- INTEGRAL FAST RECIRCULATION DIODES

DESCRIPTION

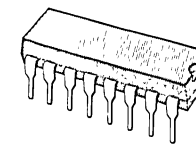
The L6221 monolithic quad darlington switch is designed for high current, high voltage switching applications. Each of the four switches is controlled by a logic input and all four are controlled by a common enable input. All inputs are TTL-compatible for direct connection to logic circuits.

Each switch consists of an open-collector darlington transistor plus a fast diode for switching applications with inductive device loads. The emitters of the four switches are commoned. Any number of inputs and outputs of the same device may be paralleled.

Two versions are available : the L6221A mounted in a Powerdip 12 + 2 + 2 package and the L6221N mounted in a 15--lead Multiwatt package.



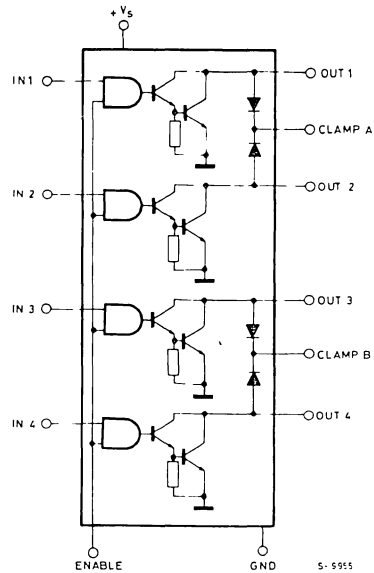
Multiwatt 15



Powerdip 12 + 2 + 2

ORDER CODES : L6221A
L6221N

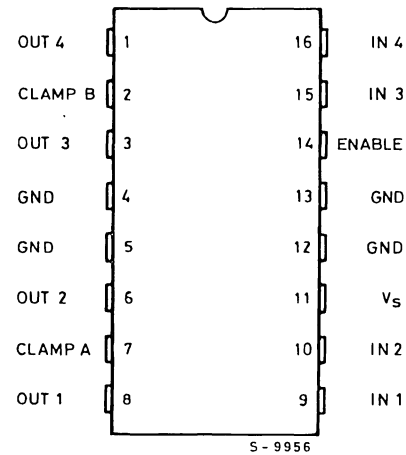
BLOCK DIAGRAM



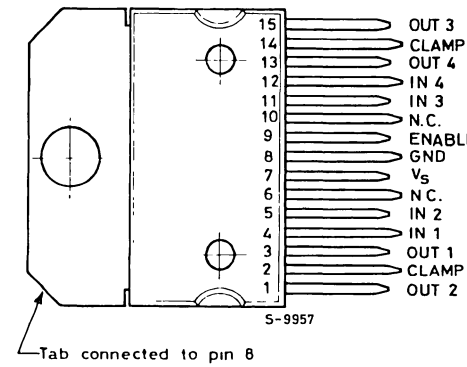
ABSOLUTE MAXIMUM RATINGS

V_o	Output Voltage	50	V
V_s	Logic Supply Voltage	7	V
V_{IN}, V_{EN}	Input Voltage, Enable Voltage	V_s	
I_C	Continuous Collector Current (for each channel)	1.8	A
I_C	Collector Peak Current (repetitive, duty cycle = 10 % t_{on} = 5 ms)	2.5	A
I_C	Collector Peak Current (non repetitive, t = 10 µs)	3.2	A
T_{op}	Operating Temperature Range (junction)	– 40 to + 150	°C
T_{stg}	Storage Temperature Range	– 55 to + 150	°C
I_{sub}	Output Substrate Current	350	mA
P_{tot}	Total Power Dissipation at T_{pins} = 90 °C (powerdip) at T_{case} = 90 °C (multiwatt) at T_{amb} = 70 °C (powerdip) at T_{amb} = 70 °C (multiwatt)	4.3 20 1 2.3	W W W W

PIN CONNECTIONS (top views)



L6221A (Powerdip)



L6221N (Multiwatt-15)

THERMAL DATA

			Powerdip	Multiwatt-15
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	14 °C/W	–
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	–	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80 °C/W	35 °C/W

TRUTH TABLE

Enable	Input	Power Out
H	H	ON
H	L	OFF
L	X	OFF

For each input : H = High level
L = Low level
X = Don't care

PIN FUNCTIONS (see block diagram)

Name	Function
IN 1	Input to Driver 1
IN 2	Input to Driver 2
OUT 1	Output of Driver 1
OUT 2	Output of Driver 2
CLAMP A	Diode Clamp to Driver 1 and Driver 2
IN 3	Input to Driver 3
IN 4	Input to Driver 4
OUT 3	Output of Driver 3
OUT 4	Output of Driver 4
CLAMP B	Diode Clamp to Driver 3 and Driver 4
ENABLE	Enable Input to All Drivers
V_S	Logic Supply Voltage
GND	Common Ground

ELECTRICAL CHARACTERISTICS Refer to the test circuit to Fig. 1 to Fig. 9
(VS = 5V, Tamb = 25 °C unless otherwise specified)

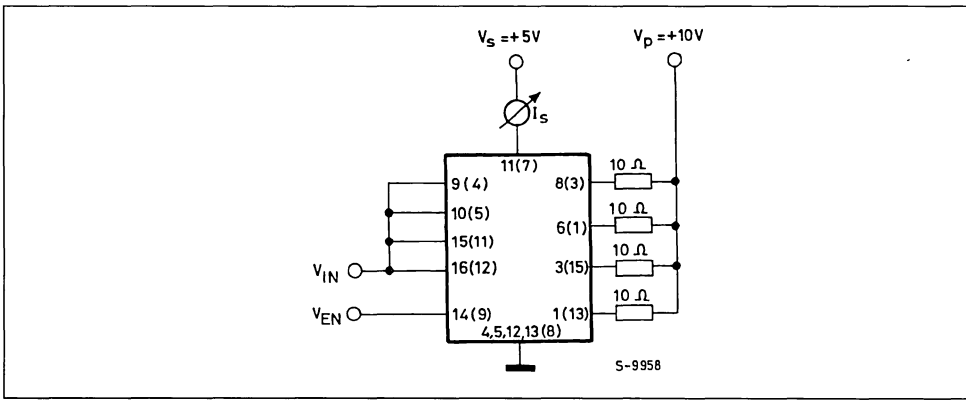
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Logic Supply Voltage		4.5		5.5	V
I_s	Logic Supply Current	All Outputs ON I_C = 0.7 A			20	m A
		All Outputs OFF			20	m A
$V_{CE(sus)}$	Output Sustaining Voltage	V_{IN} = V_{INL} V_{EN} = V_{ENH} I_C = 100 mA	46			V
I_{CEX}	Output Leakage Current	V_{CE} = 50V V_{EN} = V_{ENH} V_{IN} = V_{INL}			1	mA
$V_{CE(sat)}$	Collector Emitter Saturation Voltage (one input on ; all others inputs off.)	V_s = 4.5V V_{IN} = V_{INH} V_{EN} = V_{ENH} I_C = 0.6 A			1	V
		I_C = 1 A			1.2	V
		I_C = 1.8 A			1.6	V
V_{INL}, V_{ENL}	Input Low Voltage				0.8	V
I_{INL}, I_{ENL}	Input Low Current	V_{IN} = V_{INL} V_{EN} = V_{ENL}			− 100	µ A
V_{INL}, V_{ENH}	Input High Voltage		2.0			V
I_{INH} , I_{ENH}	Input High Current	V_{IN} = V_{INH} V_{EN} = V_{ENH}			± 10	µ A
I_R	Clamp Diode Leakage Current	V_R = 50 V V_{EN} = V_{ENH} V_{IN} = V_{INL}			100	µ A
V_F	Clamp Diode Forward Voltage	I_F = 1 A			1.6	V
		I_F = 1.8 A			2.0	V
$t_{d\ (on)}$	Turn on Delay Time	V_p = 5V R_L = 10Ω			2	µ s
$t_{d\ (off)}$	Turn off Delay Time	V_p = 5V R_L = 10Ω			5	µ s
ΔI_s	Logic Supply Current Variation	V_{IN} = 5V V_{EN} = 5V I_{out} = − 500 mA for Each Channel			150	m A

TEST CIRCUITS

(X) = Referred to Multiwatt package

X = Referred to Powerdip package

Figure 1 : Logic supply current.



Set V_{IN} = 4.5V, V_{EN} = 0 8V, or V_{IN} = 0 8V, V_{EN} = 4 5V, for I_S (all outputs off)
Set V_{IN} = 2V, V_{EN} = 2V, for I_S (all outputs on)

Figure 2 : Output Sustaining Voltage.

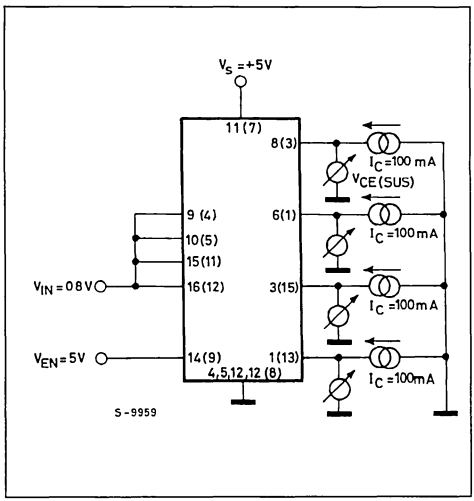


Figure 3 : Output Leakage Current.

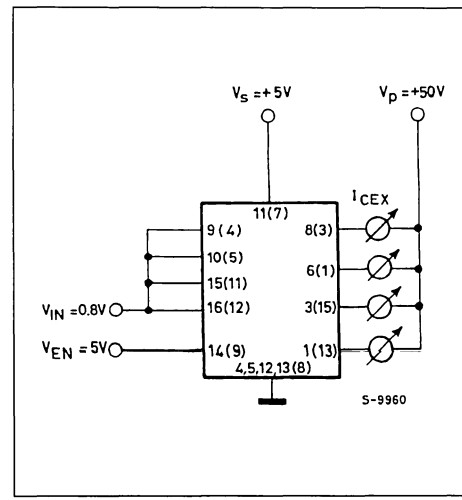


Figure 4 : Collector-emitter Saturation Voltage.

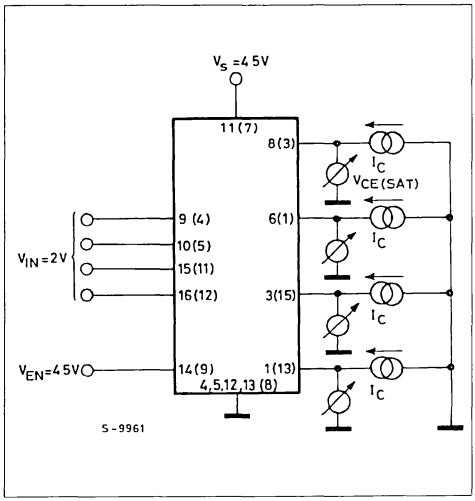
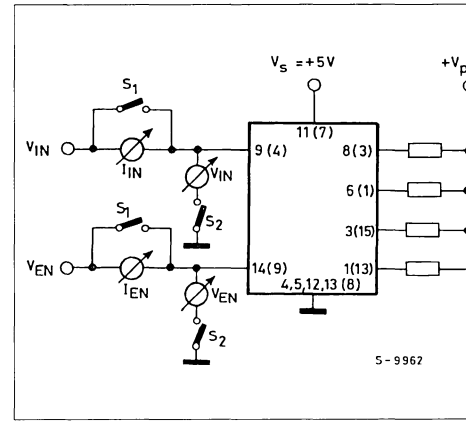


Figure 5 : Logic Input Characteristics.



Set S_1, S_2 open, V_{IN}, V_{EN} = 0.8V for I_{IN} L, I_{EN} L
Set S_1, S_2 open, V_{IN}, V_{EN} = 2V for I_{IN} H, I_{EN} H
Set S_1, S_2 close, V_{IN}, V_{EN} = 0.8V for V_{IN} L, V_{EN} L
Set S_1, S_2 close, V_{IN}, V_{EN} = 2V for V_{IN} H, V_{EN} H

Figure 6 : Clamp Diode Leakage Current.

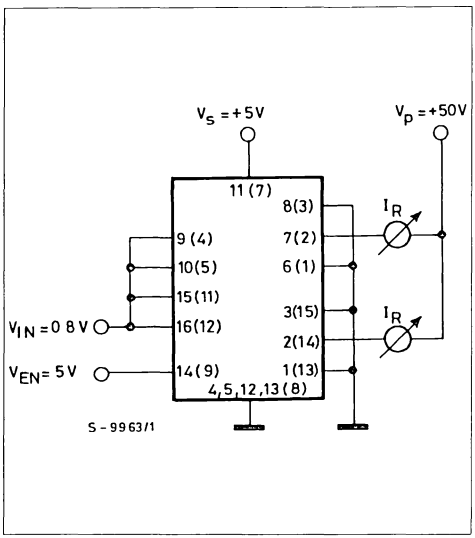


Figure 7 : Clamp Diode Forward Voltage.

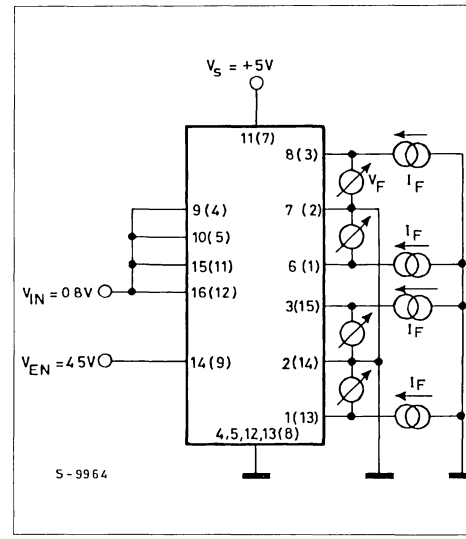


Figure 8 : Switching Times Test Circuit.

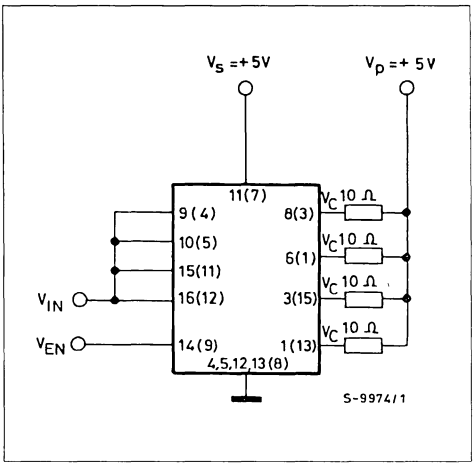


Figure 9 : Switching TImes Waveforms.

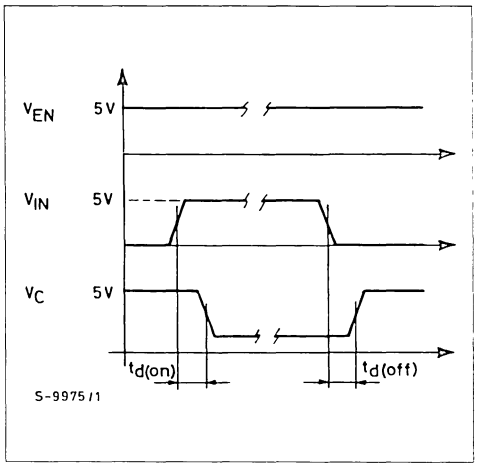


Figure 10 : Allowed Peak Collector Current vs. Duty Cycle for 1, 2, 3 or 4 Contemporary Working Outputs (L6221A).

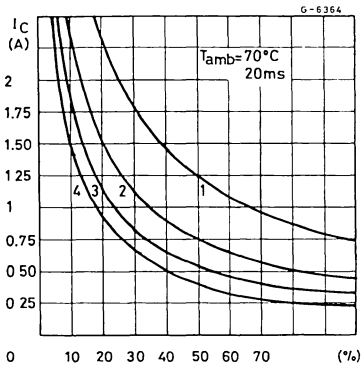


Figure 11 : Allowed Peak Collector Current vs. Duty Cycle for 1, 2, 3 or 4 Contemporary Working Outputs (L6221N).

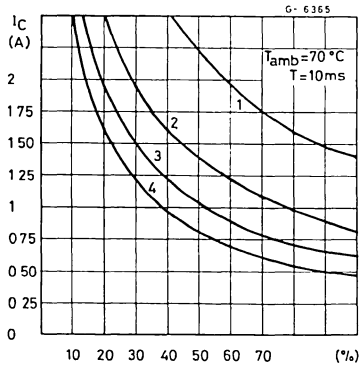


Figure 12 : Collector Saturation Voltage vs. Collector Current.

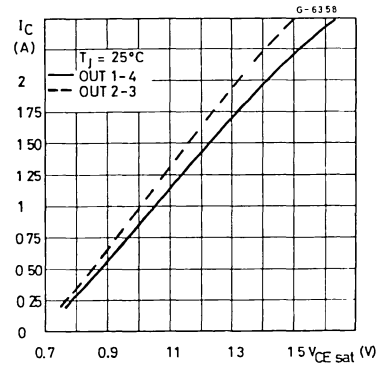


Figure 13 : Free-wheeling Diode Forward Voltage vs. Diode Current .

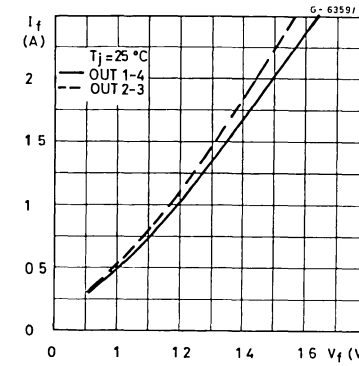


Figure 14 : Collector Saturation Voltage vs. Junction Temperature at I_C = 1A.

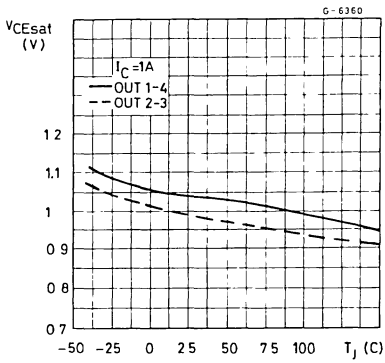


Figure 15 : Free-wheeling Diode Forward Voltage vs. Junction Temperature at I_F = 1A.

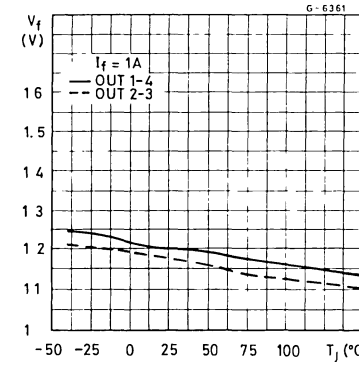


Figure 16 : Saturation Voltage vs. Junction Temperature at IC = 1.8A.

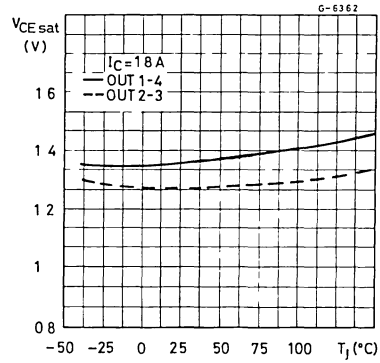


Figure 17 : Free-wheeling Diode Forward Voltage vs. Junction Temperature at If = 1.8A.

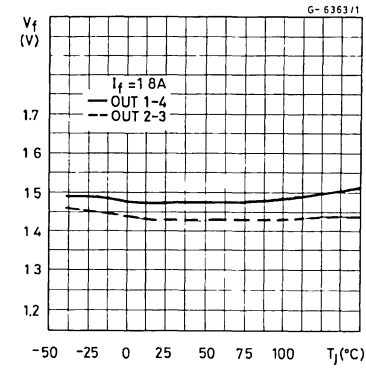
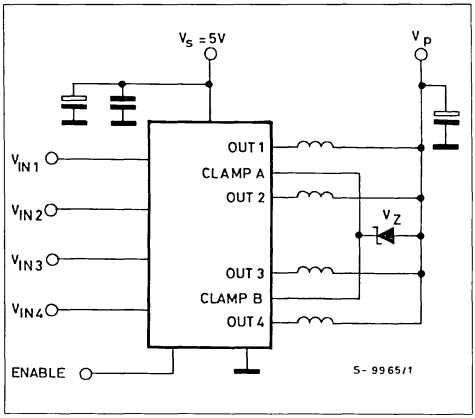


Figure 18.



APPLICATION INFORMATION

When inductive loads are driven by L6221A/N, a zener diode in series with the integral free-wheeling diodes increases the voltage across which energy stored in the load is discharged and therefore speeds the current decay (fig. 18).

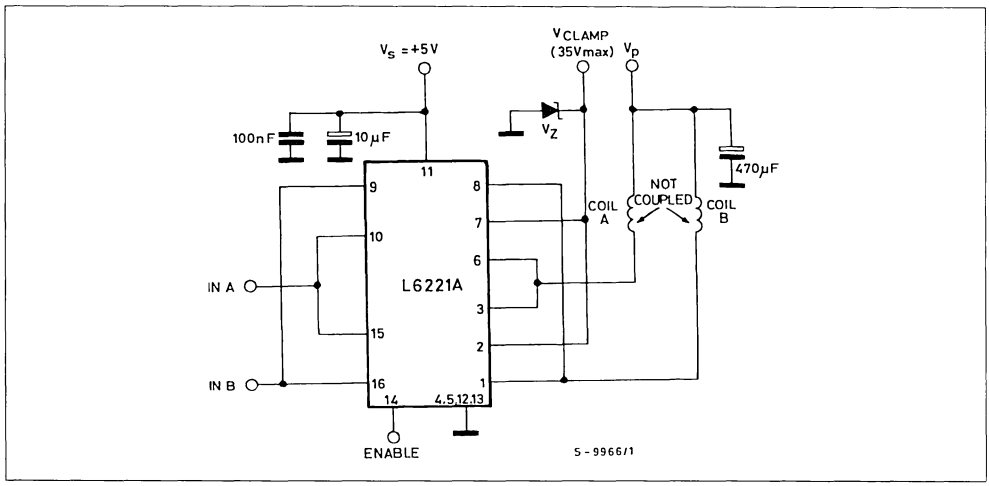
For reliability it is suggested that the zener is chosen so that $V_p + V_z < 35$ V.

The reasons for this are two fold :

1) The zener voltage changes in temperature and current.

2) The instantaneous power must be limited to avoid the reverse second breakdown.

Figure 19 : Driver for Solenoids up to 3A.



Some care must be taken to ensure that the collectors are placed close together to avoid different current partitioning at turn-off.

We suggest to put in parallel channel 1 and 4 and channel 2 and 3 as shown in figure 19 for the similar electrical characteristics of the logic section (turn-on and turn-off delay time) and the power stages (collector saturation voltage, free-wheeling diode forward voltage).

Figure 20 : Saturation Voltage vs. Collector Current.

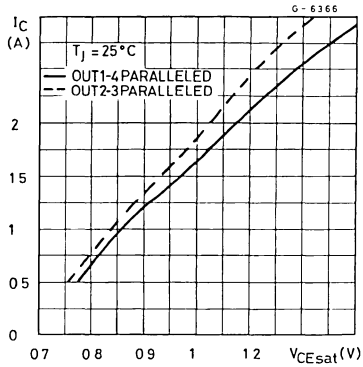


Figure 21 : Peak Collector Current vs. Duty Cycle for 1 or 2 Paralleled Outputs Driven (L6221A).

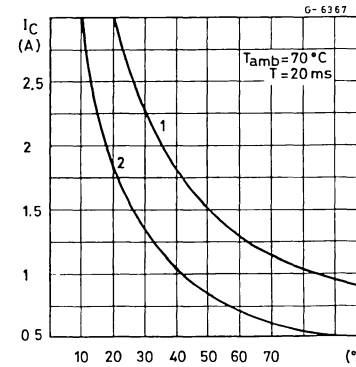
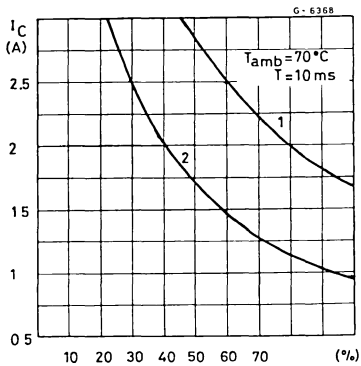


Figure 22 : Peak Collector Current vs. Duty Cycle for 1 or 2 Paralleled Outputs Driven (L6221N).



MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the L6221A can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 23) or to an external heatsink (Fig. 24).

The diagram of figure 25 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side " α" of two equal square copper areas having a thickness of 35µ (1.4 mils). During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 23 : Example of P.C. Board Copper Area Which is Used as Heatsink.

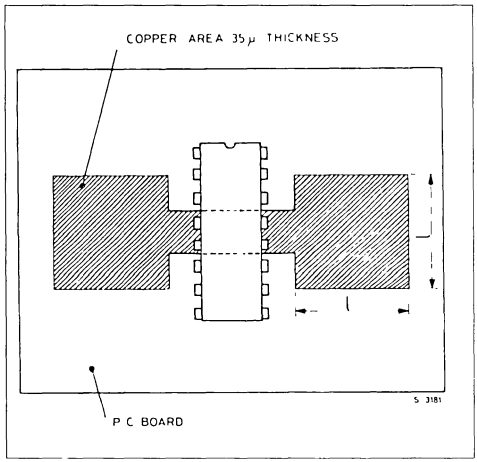


Figure 24 : External Heatsink Mounting Example.

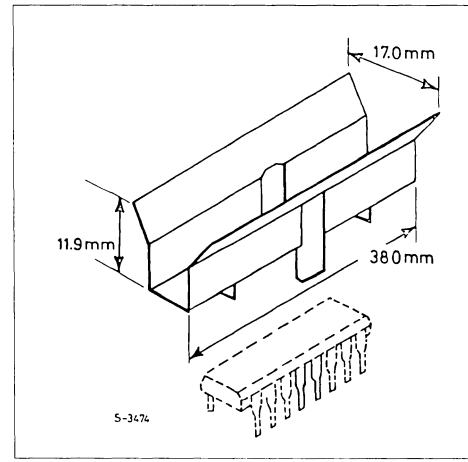


Figure 25 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side " α".

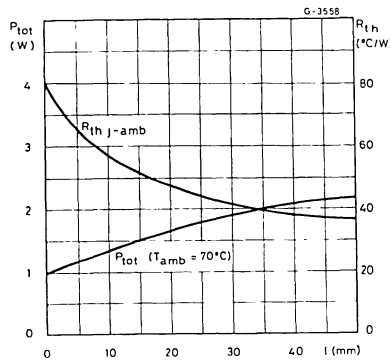
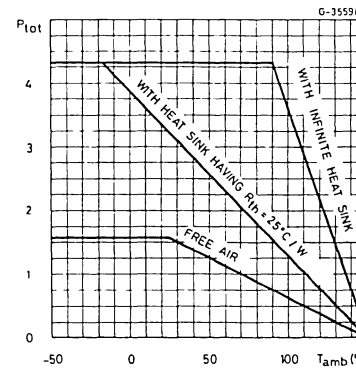


Figure 26 : Maximum Allowable Power Dissipation vs. Ambient Temperature.



QUAD TRANSISTOR SWITCH

- OUTPUT VOLTAGE TO 50 V
- OUTPUT CURRENT TO 1.2 A
- VERY LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUTS
- INTEGRAL SUPPRESSION DIODE

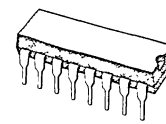
DESCRIPTION

The L6222 monolithic quad transistor switch is designed for high current, high voltage switching applications.

Each of the four switches is controlled by a logic input and all four are controlled by a common enable input. All inputs are TTL-compatible for direct connection to logic circuits. Each switch consists of an open-collector transistor plus a clamp diode for applications with inductive loads.

The emitters of the four switches are commoned. Any number of inputs and outputs of the same device may be paralleled.

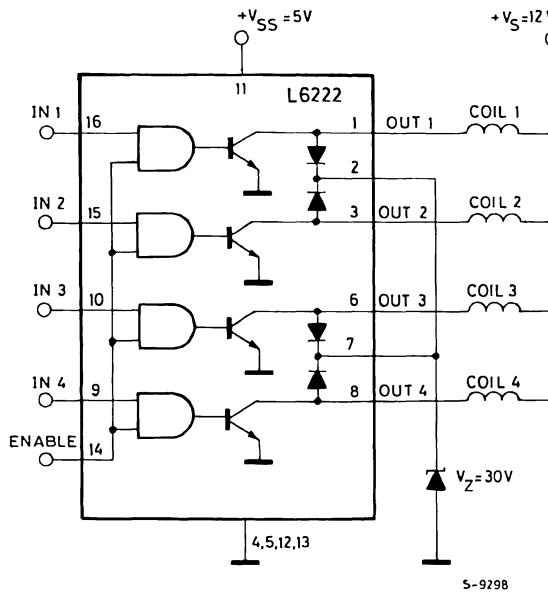
This device is intended to drive coils such as relays, solenoids, unipolar stepper motors, LED, etc.



Powerdip 12 + 2 + 2

ORDER CODE : L6222

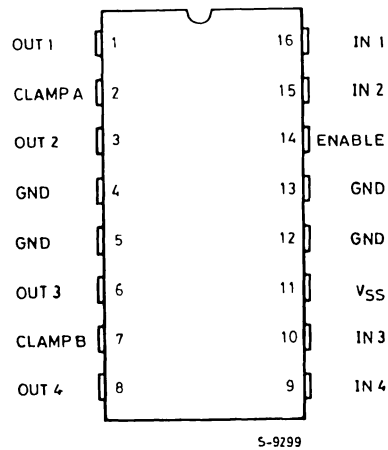
Figure 1 : Unipolar Stepper Motor Drive.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Output Voltage	50	V
V_{ss}	Logic Supply Voltage	7	V
V_{IN}	Input Voltage	15	V
I_C	Collector Current (PEAK)	1.2	A
T_{op}	Operating Temperature Range (junction)	– 40 to + 150	°C
T_{stg}	Storage Temperature Range	– 55 to + 150	°C

CONNECTION DIAGRAM (top view)



TRUTH TABLE

Enable	Input	Power Out
H	H	ON
H	L	OFF
L	X	OFF

For each input H = High level
L = Low level
X = Don't care

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	80	° C / W
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	14	° C / W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C, unless specified)

Symbol	Parameter	Test Conditions		Min.	Unit	Max.	Typ.
V_{SS}	Logic Supply Voltage			4.50		7	V
$V_{CE\ (sus)}$	Output Sustaining Voltage	V_{IN} = 0.8 V I_C = 100 mA		46			V
I_{CEX}	Output Leakage Current	V_{CE} = 50 V V_{IN} = 0.8 V				1	mA
$V_{CE\ (sat)}$	Collector Emitter Saturation Voltage	$V_{IN} \geq$ 2.0V	I_C = 0.1 A			0.2	V
			I_C = 0.4 A			0.5	
			I_C = 0.7 A			0.9	
V_{IL}	Input low Voltage					0.8	V
I_{IL}	Input Low Current	V_{IN} = 0.4 V				− 100	µA
V_{IH}	Input High Voltage			2.0			V
I_{IH}	Input High Current	$V_{IN} \geq$ 2.0 V				± 10	µA
I_S	Logic Supply Current	V_{SS} = 5 V	All Outputs ON I_C = 0.7 A		50	85	mA
			All Outputs OFF		8		mA
I_R	Clamp Diode Leakage Current	V_R = 50 V				100	µA
V_F	Clamp Diode Forward Voltage	I_F = 0.7 A				1.6	V
		I_F =1.2 A				2.0	

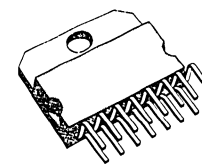
L7150
L7152

50 V QUAD DARLINGTON SWITCHES

- FOUR NPN DARLINGTONS WITH ISOLATED CONNECTIONS
- OUTPUT CURRENT TO 1.5 A EACH DARLINGTON
- MINIMUM BREAKDOWN 50 V
- MULTIWATT PACKAGE ALLOWS OPERATION AT 1.5 A, 50 V, 100 % DUTY CYCLE, ALL FOUR DEVICES ON
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR 5 V AND 6-15 V LOGIC FAMILIES

The L7150 has 350 input resistors and is compatible with TTL, DTL, LSTTL and 5 V CMOS logic. The L7152 has 3 KΩ input resistors for use with 6-15 V CMOS and PMOS logic.

These devices are suitable for driving a wide range of inductive and non-inductive loads including DC motors, stepper motors, solenoids, relays, lamps, multiplexed LEDs and heaters.



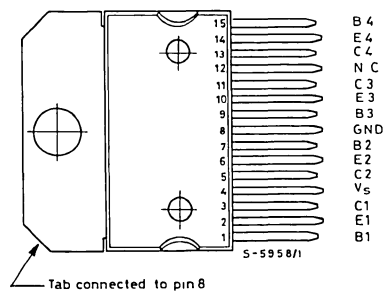
Multiwatt-15

ORDER CODES : L7150
L7152

DESCRIPTION

The L7150 and L7152 are 1.5 A quad darlington arrays mounted in the 15-lead Myltiwatt® plastic package. Each darlington is equipped with a suppression diode for inductive loads and all three terminals are isolated.

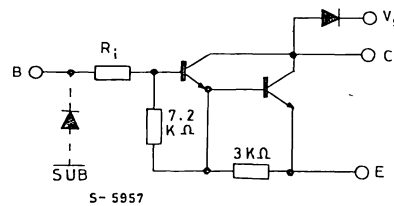
CONNECTION DIAGRAM (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CEX}	Output Voltage	50	V
I_o	Output Current	1.75	A
V_I	Input Voltage	30	V
I_B	Input Current	25	mA
P_{tot}	Power Dissipation (T_{case} = 75 °C)	25	W
T_{amb}	Operating Ambient Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

SCHEMATIC DIAGRAM



L7150 R_{IN} = 350Ω
L7152 R_{IN} = 3KΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Condtions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 50 V T_{amb} = 70°C V_{CE} = 50 V			100 500	µA µA	1
$V_{CER\ (sus)}$	Collector-emitter Sustaining Voltage*	I_C = 100 mA V_I = 0.4 V	35			V	2
$V_{CE\ (sat)}$	Collector-emitter Saturation Voltage	I_C = 500 mA I_B = 625 µA I_C = 750 mA I_B = 935 µA I_C = 1 A I_B = 1.25 mA I_C = 1.25 A I_B = 2 mA			**1.15** **1.3** **1.4** **1.5**	V V V V	3
$I_{I(on)}$	Input Current	for **L7150** V_I = 2.4 V for **L7150** V_I = 3.75 V for **L7152** V_I = 5 V for **L7152** V_I = 12 V	**1.4** **3.3** **0.6** **0.7**		4.3 9.6 1.8 5.2	mA mA mA mA	4
$V_{I(on)}$	Input Voltage	for **L7150** V_{CE} = 2 V I_C = 1 A V_{CE} = 2 V I_C = 1.5 A for **L7152** V_{CE} = 2 V I_C = 1 A V_{CE} = 2 V I_C = 1.5 A			 2 2.5 6.5 10	 V V V V	5
t_{PLH}	Turn-on Delay Time	0.5 V_I to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o			1.5	µs	

(*) $t_{(sus)}$ = 10 µs.

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	35	°C/W

TEST CIRCUIT

Figure 1.

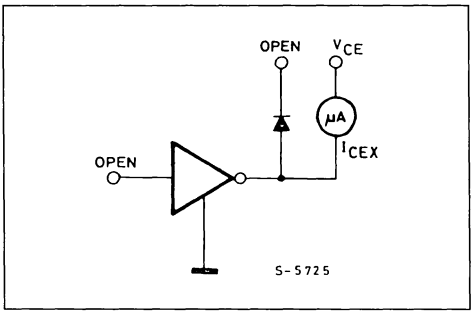


Figure 2.

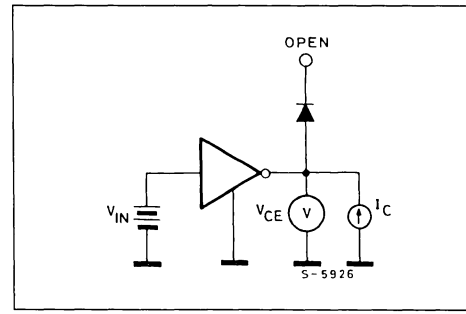


Figure 3.

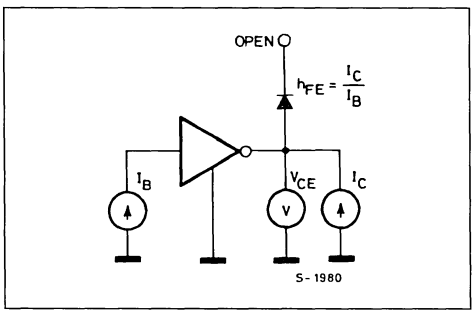


Figure 4.

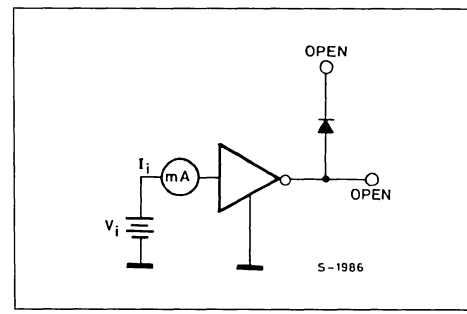
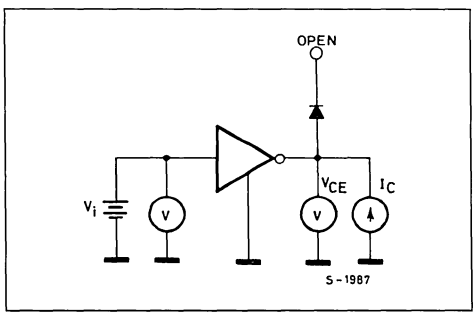


Figure 5.

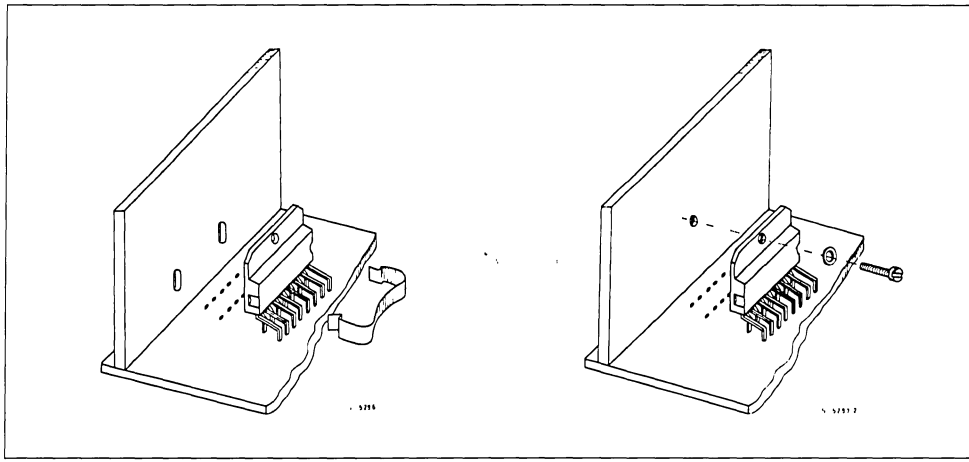


MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.

Thanks to the Multiwatt® package attaching the heatsink is very simple, a screw or compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact ; no electrical isolation is needed between the two surfaces.

Figure 6 : Mounting Example.

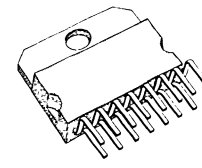


80 V QUAD DARLINGTON SWITCHES

- FOUR NPN DARLINGTONS WITH ISOLATED CONNECTIONS
- OUTPUT CURRENT TO 1.5 A EACH DARLINGTON
- MINIMUM BREAKDOWN 80 V
- MULTIWATT PACKAGE ALLOWS OPERATION AT 1.5 A, 80 V, 100 % DUTY CYCLE, ALL FOUR DEVICES ON
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR 5 V AND 6-15 V LOGIC FAMILIES

The L7180 has 350 Ω input resistors and is compatible with TTL, DTL, LSTTL and 5 V CMOS logic. The L7182 has 3 KΩ input resistors for use with 6-15 V CMOS and PMOS logic.

These devices are suitable for driving a wide range of inductive and non-inductive loads including DC motors, stepper motors, solenoids, relays, lamps, multiplexed LEDs and heaters.



Multiwatt 15

ORDER CODES : L7180
L7182

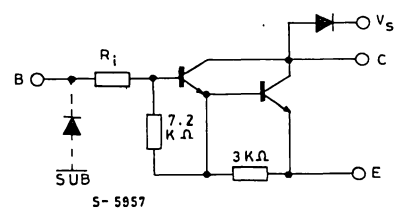
DESCRIPTION

The L7180 and L7182 are 1.5 A quad darlington arrays mounted in the 15-lead Multiwatt® plastic package. Each darlington is equipped with a suppression diode for inductive loads, and all three terminals are isolated.

ABSOLUTE MAXIMUM RATINGS

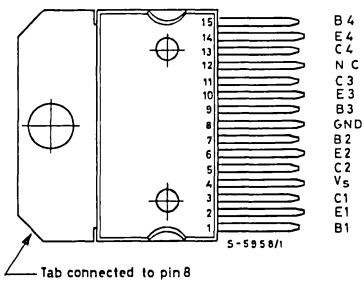
Symbol	Parameter	Test Conditions	Unit
V_{CEX}	Output Voltage	80	V
I_o	Output Current	1.75	A
V_i	Input Voltage	60	V
I_B	Input Current	25	mA
P_{tot}	Power Dissipation (T_{case} = 75 °C)	25	W
T_{amb}	Operating Ambient Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

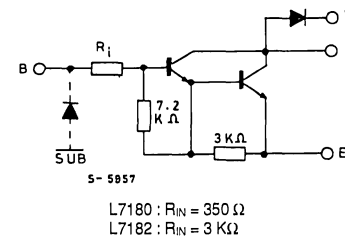
SCHEMATIC DIAGRAM



L7180 : R_{IN} = 350 Ω
L7182 : R_{IN} = 3 KΩ

CONNECTION AND SCHEMATIC DIAGRAMS (top view)





THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	35	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 80 V				100	µA	1
		V_{CE} = 80 V	T'_{amb} = 70 °C			500	µA	
$V_{CER(sus)}$	Collector-emitter Sustaining Voltage(*)	I_C = 50 mA	V_I = 0.4 V	50			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 500 mA	I_B = 625 µA			**1.15**	V	3
		I_C = 750 mA	I_B = 935 µA			**1.3**	V	
		I_C = 1 A	I_B = 1.25 mA			**1.4**	V	
		I_C = 1.5 A	I_B = 2.25 mA			**1.6**	V	
$I_{I(on)}$	Input Current	For **L7180**	V_I = 2.4 V	**1.4**		4.3	mA	4
		For **L7180**	V_I = 3.75 V	**3.3**		9.6	mA	
		For **L7182**	V_I = 5 V	**0.6**		1.8	mA	
		For **L7182**	V_I = 12 V	**1.7**		5.2	mA	
$V_{I(on)}$	Input Voltage	For **L7180**						5
		V_{CE} = 2 V	I_C = 1 A			2	V	
		V_{CE} = 2 V	I_C = 1.5 A			2.5	V	
		For **L7182**						
		V_{CE} = 2 V	I_C = 1 A			6.5	V	
		V_{CE} = 2 V	I_C = 1.5 A			10	V	
t_{PLH}	Turn-on Delay Time	0.5 V_I to 0.5 V_o				1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_I to 0.5 V_o				1.5	µs	

(*) $t_{(sus)}$ = 10 µs
Guaranteed by design ; not tested 100 %

TEST CIRCUITS

Figure 1.

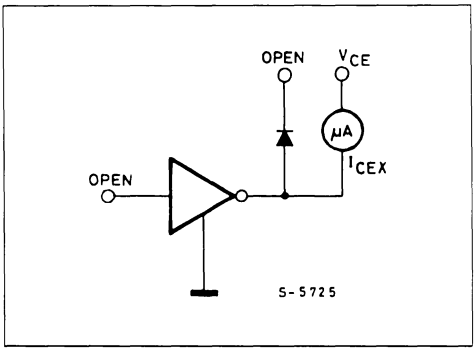


Figure 2.

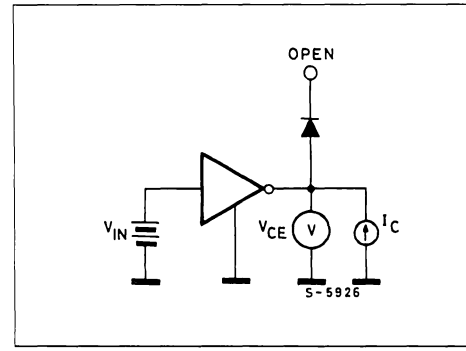


Figure 3.

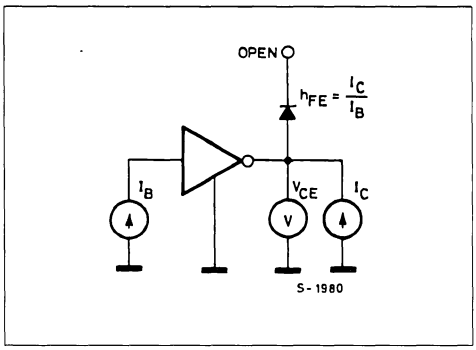


Figure 4.

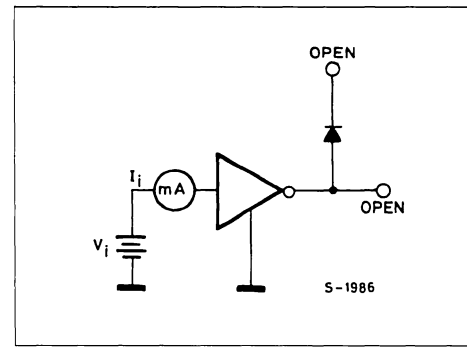
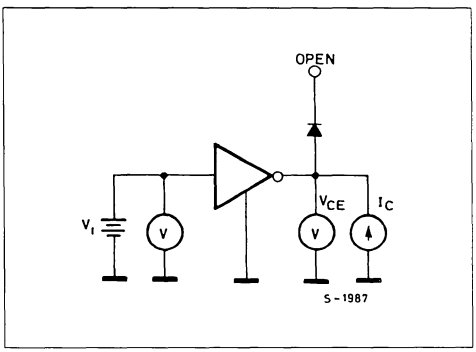


Figure 5.

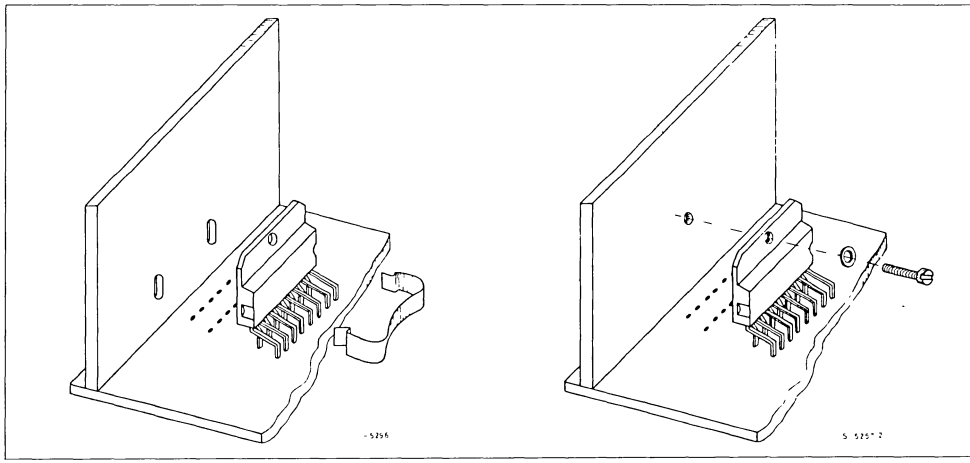


MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.

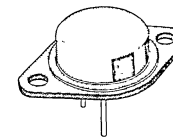
Thanks to the Multiwatt® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact ; no electrical isolation is needed between the two surfaces.

Figure 6 : Mounting Example.

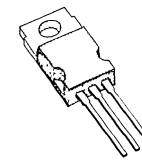


POSITIVE VOLTAGE REGULATORS

- OUTPUT CURRENT UP TO 1.5A
- OUTPUT VOLTAGES OF 5 ; 6 ; 8 ; 8.5 ; 12 ; 15 ; 18 ; 20 ; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION



TO-3

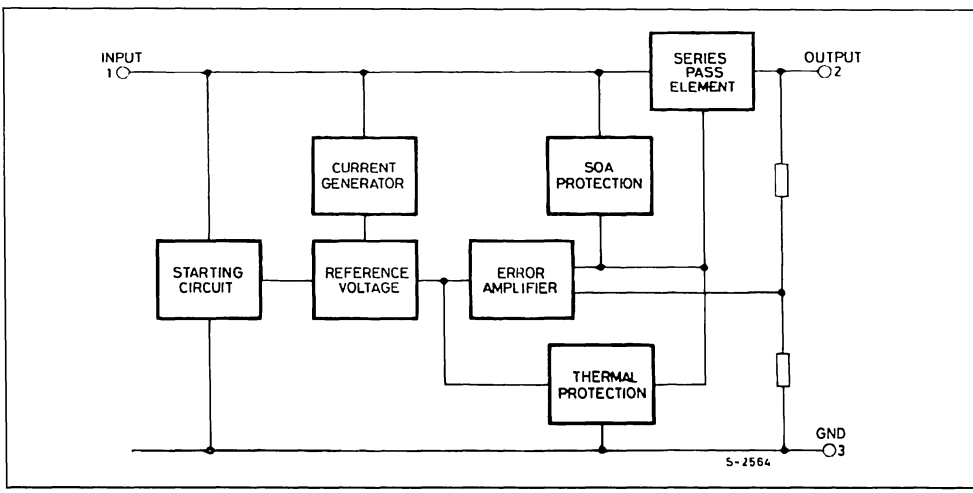


TO-220

DESCRIPTION

The L7800 series of three-terminal positive regulator is available in TO-220 and TO-3 packages and with several fixed output voltages making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

BLOCK DIAGRAM



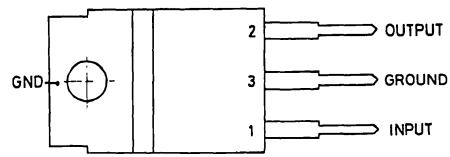
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage (for V_o = 5 to 18V) (for V_o = 20, 24V)	35 40	V V
I_o	Output Current	Internally limited	
P_{tot}	Power Dissipation	Internally limited	
T_{op}	Operating Junction Temperature (for **L7800**) (for **L7800C**)	– 55 to + 150 0 to + 150	°C °C
T_{stg}	Storage Temperature	– 65 to + 150	°C

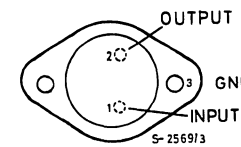
THERMAL DATA

Symbol	Parameter		TO-220	TO-3	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	4	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	50	35	°C/W

CONNECTION DIAGRAM AND ORDERING NUMBERS (top view)



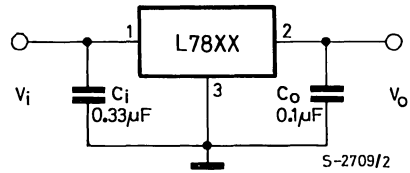
S - 2568/1



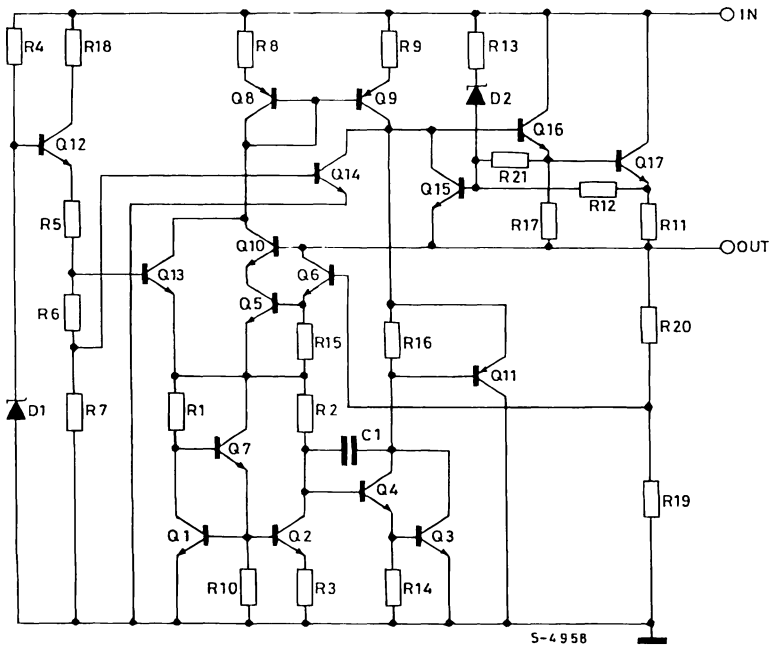
S- 2569/3

Type	TO-220	TO-3	Output Voltage
L7805		L7805T	5V
L7805C	L7805CV	L7805CT	5V
L7806		L7806T	6V
L7806C	L7806CV	L7806CT	6V
L7808		L7808T	8V
L7808C	L7808CV	L7808CT	8V
L7885C	L7885CV	L7885CT	8.5V
L7812		L7812T	12V
L7812C	L7812CV	L7812CT	12V
L7815		L7815T	15V
L7815C	L7815CV	L7815CT	15V
L7818		L7818T	18V
L7818C	L7818CV	L7818CT	18V
L7820		L7820T	20V
L7820C	L7820CV	L7820CT	20V
L7824		L7824T	24V
L7824C	L7824CV	L7824CT	24V

APPLICATION CIRCUIT



SCHEMATIC DIAGRAM



TEST CIRCUITS

Figure 1 : DC Parameters.

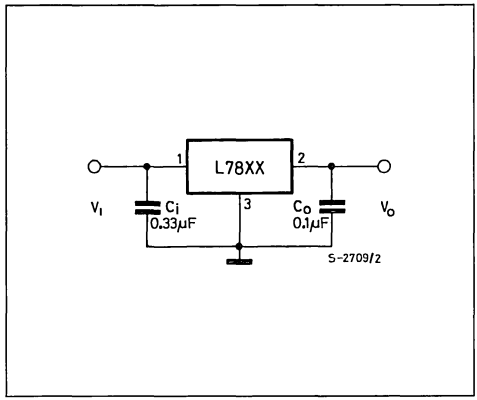


Figure 2 : Load Regulation.

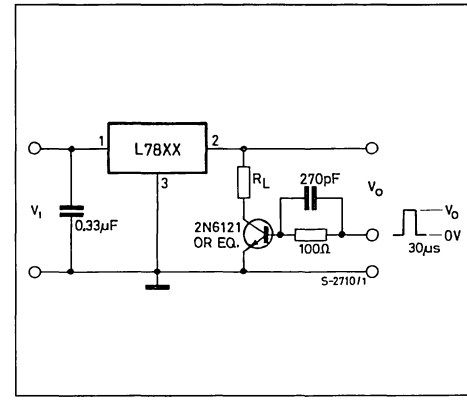
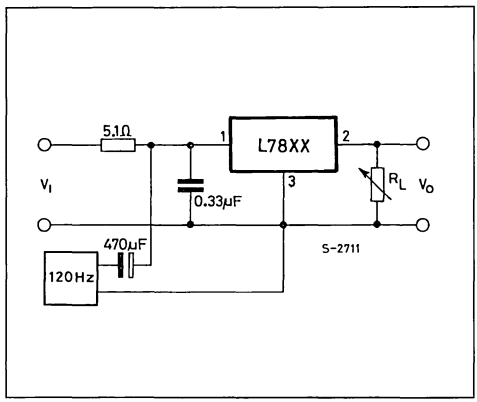


Figure 3 : Ripple Rejection.



ELECTRICAL CHARACTERISTICS FOR L7805 (refer to the test circuits, $T_j = -55$ to $150°C$ $V_i = 10V$, $I_o = 500mA$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	$T_j = 25°C$	4.8	5	5.2	V
V_o	Output Voltage	$I_o = 5mA$ to $1A$ $P_o \leq 15W$ $V_i = 8$ to $20V$	4.65	5	5.35	V
ΔV_o*	Line Regulation	$V_i = 7$ to $25V$ $T_j = 25°C$ $V_i = 8$ to $12V$ $T_j = 25°C$		3 1	50 25	mV mV
ΔV_o*	Load Regulation	$I_o = 5$ to $1500mA$ $T_j = 25°C$ $I_o = 250$ to $750mA$ $T_j = 25°C$			100 25	mV mV
I_d	Quiescent Current	$T_j = 25°C$			6	mA
ΔI_d	Quiescent Current Change	$I_o = 5$ to $1000mA$			0.5	mA
ΔI_d	Quiescent Current Change	$V_i = 8$ to $25V$			0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	$I_o = 5mA$		0.6		mV/°C
e_N	Output Noise Voltage	$B = 10Hz$ to $100KHz$ $T_j = 25°C$			40	$\mu V/V_o$
SVR	Supply Voltage Rejection	$V_i = 8$ to $18V$ $f = 120Hz$	68			dB
V_d	Dropout Voltage	$I_o = 1A$ $T_j = 25°C$		2	2.5	V
R_o	Output Resistance	$f = 1KHz$		17		mΩ
I_{sc}	Short Circuit Current	$V_i = 35V$ $T_j = 25°C$		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	$T_j = 25°C$	1.3	2.2	3.3	A

ELECTRICAL CHARACTERISTICS FOR L7806 (refer to the test circuits, $T_j = -55$ to $150°C$ $V_i = 11V$, $I_o = 500mA$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	$T_j = 25°C$	5.75	6	6.25	V
V_o	Output Voltage	$I_o = 5mA$ to $1A$ $P_o \leq 15W$ $V_i = 9$ to $21V$	5.65	6	6.35	V
ΔV_o*	Line Regulation	$V_i = 8$ to $25V$ $T_j = 25°C$ $V_i = 9$ to $13V$ $T_j = 25°C$			60 30	mV mV
ΔV_o*	Load Regulation	$I_o = 5$ to $1500mA$ $T_j = 25°C$ $I_o = 250$ to $750mA$ $T_j = 25°C$			100 30	mV mV
I_d	Quiescent Current	$T_j = 25°C$			6	mA
ΔI_d	Quiescent Current Change	$I_o = 5$ to $1000mA$			0.5	mA
ΔI_d	Quiescent Current Change	$V_i = 9$ to $25V$			0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	$I_o = 5mA$		0.7		mV/°C
e_N	Output Noise Voltage	$B = 10Hz$ to $100KHz$ $T_j = 25°C$			40	$\mu V/V_o$
SVR	Supply Voltage Rejection	$V_i = 9$ to $19V$ $f = 120Hz$	65			dB
V_d	Dropout Voltage	$I_o = 1A$ $T_j = 25°C$		2	2.5	V
R_o	Output Resistance	$f = 1KHz$		19		mΩ
I_{sc}	Short Circuit Current	$V_i = 35V$ $T_j = 25°C$		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	$T_j = 25°C$	1.3	2.2	3.3	A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7808 (refer to the test circuits, $T_j = -55$ to 150°C $V_i = 14V$, $I_o = 500mA$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	$T_j = 25°C$	7.7	8	8.3	V
V_o	Output Voltage	$I_o = 5mA$ to $1A$ $P_o \leq 15W$ $V_i = 11.5$ to $23V$	7.6	8	8.4	V
ΔV_o*	Line Regulation	$V_i = 10.5$ to $25V$ $T_j = 25°C$ $V_i = 11$ to $17V$ $T_j = 25°C$			80 40	mV mV
ΔV_o*	Load Regulation	$I_o = 5$ to $1500mA$ $T_j = 25°C$ $I_o = 250$ to $750mA$ $T_j = 25°C$			100 40	mV mV
I_d	Quiescent Current	$T_j = 25°C$			6	mA
ΔI_d	Quiescent Current Change	$I_o = 5$ to $1000mA$			0.5	mA
ΔI_d	Quiescent Current Change	$V_i = 11.5$ to $25V$			0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	$I_o = 5mA$		1		mV/°C
e_N	Output Noise Voltage	$B = 10Hz$ to $100KHz$ $T_j = 25°C$			40	$\mu V/V_o$
SVR	Supply Voltage Rejection	$V_i = 11.5$ to $21.5V$ $f = 120Hz$	62			dB
V_d	Dropout Voltage	$I_o = 1A$ $T_j = 25°C$		2	2.5	V
R_o	Output Resistance	$f = 1KHz$		16		mΩ
I_{sc}	Short Circuit Current	$V_i = 35V$ $T_j = 25°C$		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	$T_j = 25°C$	1.3	2.2	3.3	A

ELECTRICAL CHARACTERISTICS FOR L7812 (refer to the test circuits, $T_j = -55$ to 150°C $V_i = 19V$, $I_o = 500mA$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	$T_j = 25°C$	11.5	12	12.5	V
V_o	Output Voltage	$I_o = 5mA$ to $1A$ $P_o \leq 15W$ $V_i = 15.5$ to $27V$	11.4	12	12.6	V
ΔV_o*	Line Regulation	$V_i = 14.5$ to $30V$ $T_j = 25°C$ $V_i = 16$ to $22V$ $T_j = 25°C$			120 60	mV mV
ΔV_o*	Load Regulation	$I_o = 5$ to $1500mA$ $T_j = 25°C$ $I_o = 250$ to $750mA$ $T_j = 25°C$			120 60	mV mV
I_d	Quiescent Current	$T_j = 25°C$			6	mA
ΔI_d	Quiescent Current Change	$I_o = 5$ to $1000mA$			0.5	mA
ΔI_d	Quiescent Current Change	$V_i = 15$ to $30V$			0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	$I_o = 5mA$		1.5		mV/°C
e_N	Output Noise Voltage	$B = 10Hz$ to $100KHz$ $T_j = 25°C$			40	$\mu V/V_o$
SVR	Supply Voltage Rejection	$V_i = 15$ to $25V$ $f = 120Hz$	61			dB
V_d	Dropout Voltage	$I_o = 1A$ $T_j = 25°C$		2	2.5	V
R_o	Output Resistance	$f = 1KHz$		18		mΩ
I_{sc}	Short Circuit Current	$V_i = 35V$ $T_j = 25°C$		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	$T_j = 25°C$	1.3	2.2	3.3	A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7815 (refer to the test circuits, $T_j = -55$ to $150°C$
$V_i = 23V$, $I_o = 500mA$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$ unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_o	Output Voltage	$T_j = 25°C$		14.4	15	15.6	V
V_o	Output Voltage	$I_o = 5mA$ to $1A$ $V_i = 18.5$ to $30V$	$P_o \leq 15W$	14.25	15	15.75	V
ΔV_o*	Line Regulation	$V_i = 17.5$ to $30V$ $V_i = 20$ to $26V$	$T_j = 25°C$ $T_j = 25°C$			150 75	mV mV
ΔV_o*	Load Regulation	$I_o = 5$ to $1500mA$ $I_o = 250$ to $750mA$	$T_j = 25°C$ $T_j = 25°C$			150 75	mV mV
I_d	Quiescent Current	$T_j = 25°C$				6	mA
ΔI_d	Quiescent Current Change	$I_o = 5$ to $1000mA$				0.5	mA
ΔI_d	Quiescent Current Change	$V_i = 18.5$ to $30V$				0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	$I_o = 5mA$			1.8		mV/°C
e_N	Output Noise Voltage	$B = 10Hz$ to $100KHz$	$T_j = 25°C$		40		$\mu V/V_o$
SVR	Supply Voltage Rejection	$V_i = 18.5$ to $28.5V$	$f = 120Hz$	60			dB
V_d	Dropout Voltage	$I_o = 1A$	$T_j = 25°C$		2	2.5	V
R_o	Output Resistance	$f = 1KHz$			19		mΩ
I_{sc}	Short Circuit Current	$V_i = 35V$	$T_j = 25°C$		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	$T_j = 25°C$		1.3	2.2	3.3	A

ELECTRICAL CHARACTERISTICS FOR L7818 (refer to the test circuits, $T_j = -55$ to $150°C$
$V_i = 26V$, $I_o = 500mA$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$ unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_o	Output Voltage	$T_j = 25°C$		17.3	18	18.7	V
V_o	Output Voltage	$I_o = 5mA$ to $1A$ $V_i = 22$ to $33V$	$P_o \leq 15W$	17.1	18	18.9	V
ΔV_o*	Line Regulation	$V_i = 21$ to $33V$ $V_i = 24$ to $30V$	$T_j = 25°C$ $T_j = 25°C$			180 90	mV mV
ΔV_o*	Load Regulation	$I_o = 5$ to $1500mA$ $I_o = 250$ to $750mA$	$T_j = 25°C$ $T_j = 25°C$			180 90	mV mV
I_d	Quiescent Current	$T_j = 25°C$				6	mA
ΔI_d	Quiescent Current Change	$I_o = 5$ to $1000mA$				0.5	mA
ΔI_d	Quiescent Current Change	$V_i = 22$ to $33V$				0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	$I_o = 5mA$			2.3		mV/°C
e_N	Output Noise Voltage	$B = 10Hz$ to $100KHz$	$T_j = 25°C$		40		$\mu V/V_o$
SVR	Supply Voltage Rejection	$V_i = 22$ to $32V$	$f = 120Hz$	59			dB
V_d	Dropout Voltage	$I_o = 1A$	$T_j = 25°C$		2	2.5	V
R_o	Output Resistance	$f = 1KHz$			22		mΩ
I_{sc}	Short Circuit Current	$V_i = 35V$	$T_j = 25°C$		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	$T_j = 25°C$		1.3	2.2	3.3	A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7820 (refer to the test circuits, $T_j = -55$ to $150°C$ $V_i = 28V$, $I_o = 500mA$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$ unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_o	Output Voltage	$T_j = 25°C$		19.2	20	20.8	V
V_o	Output Voltage	$I_o = 5mA$ to $1A$ $V_i = 24$ to $35V$	$P_o \leq 15W$	19	20	21	V
ΔV_o*	Line Regulation	$V_i = 22.5$ to $35V$ $V_i = 26$ to $32V$	$T_j = 25°C$ $T_j = 25°C$			200 100	mV mV
ΔV_o*	Load Regulation	$I_o = 5$ to $1500mA$ $I_o = 250$ to $750mA$	$T_j = 25°C$ $T_j = 25°C$			200 100	mV mV
I_d	Quiescent Current	$T_j = 25°C$				6	mA
ΔI_d	Quiescent Current Change	$I_o = 5$ to $1000mA$				0.5	mA
ΔI_d	Quiescent Current Change	$V_i = 24$ to $35V$				0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	$I_o = 5mA$			2.5		mV/°C
e_N	Output Noise Voltage	$B = 10Hz$ to $100KHz$	$T_j = 25°C$		40		$\mu V/V_o$
SVR	Supply Voltage Rejection	$V_i = 24$ to $35V$	$f = 120Hz$	58			dB
V_d	Dropout Voltage	$I_o = 1A$	$T_j = 25°C$		2	2.5	V
R_o	Output Resistance	$f = 1KHz$			24		mΩ
I_{sc}	Short Circuit Current	$V_i = 35V$	$T_j = 25°C$		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	$T_j = 25°C$		1.3	2.2	3.3	A

ELECTRICAL CHARACTERISTICS FOR L7824 (refer to the test circuits, $T_j = -55$ to $150°C$ $V_i = 33V$, $I_o = 500mA$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$ unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_o	Output Voltage	$T_j = 25°C$		23	24	25	V
V_o	Output Voltage	$I_o = 5mA$ to $1A$ $V_i = 28$ to $38V$	$P_o \leq 15W$	22.8	24	25.2	V
ΔV_o*	Line Regulation	$V_i = 27$ to $38V$ $V_i = 30$ to $36V$	$T_j = 25°C$ $T_j = 25°C$			240 120	mV mV
ΔV_o*	Load Regulation	$I_o = 5$ to $1500mA$ $I_o = 250$ to $750mA$	$T_j = 25°C$ $T_j = 25°C$			240 120	mV mV
I_d	Quiescent Current	$T_j = 25°C$				6	mA
ΔI_d	Quiescent Current Change	$I_o = 5$ to $1000mA$				0.5	mA
ΔI_d	Quiescent Current Change	$V_i = 28$ to $38V$				0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	$I_o = 5mA$			3		mV/°C
e_N	Output Noise Voltage	$B = 10Hz$ to $100KHz$	$T_j = 25°C$		40		$\mu V/V_o$
SVR	Supply Voltage Rejection	$V_i = 28$ to $38V$	$f = 120Hz$	56			dB
V_d	Dropout Voltage	$I_o = 1A$	$T_j = 25°C$		2	2.5	V
R_o	Output Resistance	$f = 1KHz$			28		mΩ
I_{sc}	Short Circuit Current	$V_i = 35V$	$T_j = 25°C$		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	$T_j = 25°C$		1.3	2.2	3.3	A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7805C (refer to the test circuits, T_j = 0 to 125°C V_i = 10V, I_o = 500mA, C_i = 0.33µF, C_o = 0.1µF unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C		4.8	5	5.2	V
V_o	Output Voltage	I_o = 5mA to 1A V_i = 7 to 20V	$P_o \leq$ 15W	4.75	5	5.25	V
ΔV_o*	Line Regulation	V_i = 7 to 25V V_i = 8 to 12V	T_j = 25°C T_j = 25°C		3 1	100 50	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA I_o = 250 to 750mA	T_j = 25°C T_j = 25°C			100 50	mV mV
I_d	Quiescent Current	T_j = 25°C				8	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA				0.5	mA
ΔI_d	Quiescent Current Change	V_i = 7 to 25V				1.3	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA			– 1.1		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz	T_j = 25°C		40		µV/V_o
SVR	Supply Voltage Rejection	V_i = 8 to 18V	f = 120Hz	62			dB
V_d	Dropout Voltage	I_o = 1A	T_j = 25°C		2		V
R_o	Output Resistance	f = 1KHz			17		mΩ
I_{sc}	Short Circuit Current	V_i = 35V	T_j = 25°C		750		mA
I_{scp}	Short Circuit Peak Current	T_j = 25°C			2.2		A

ELECTRICAL CHARACTERISTICS FOR L7806C (refer to the test circuits, T_j = 0 to 125°C V_i = 11V, I_o = 500mA, C_i = 0.33µF, C_o = 0.1µF unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C		5.75	6	6.25	V
V_o	Output Voltage	I_o = 5mA to 1A V_i = 8 to 21V	$P_o \leq$ 15W	5.7	6	6.3	V
ΔV_o*	Line Regulation	V_i = 8 to 25V V_i = 9 to 13V	T_j = 25°C T_j = 25°C			120 60	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA I_o = 250 to 750mA	T_j = 25°C T_j = 25°C			120 60	mV mV
I_d	Quiescent Current	T_j = 25°C				8	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA				0.5	mA
ΔI_d	Quiescent Current Change	V_i = 8 to 25V				1.3	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA			– 0.8		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz	T_j = 25°C		45		µV/V_o
SVR	Supply Voltage Rejection	V_i = 9 to 19V	f = 120Hz	59			dB
V_d	Dropout Voltage	I_o = 1A	T_j = 25°C		2		V
R_o	Output Resistance	f = 1KHz			19		mΩ
I_{sc}	Short Circuit Current	V_i = 35V	T_j = 25°C		550		mA
I_{scp}	Short Circuit Peak Current	T_j = 25°C			2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7808C (refer to the test circuits, T_j = 0 to 125°C V_i = 14V, I_o = 500mA, C_i = 0.33µF, C_o = 0.1µF unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C		7.7	8	8.3	V
V_o	Output Voltage	I_o = 5mA to 1A V_i = 10.5 to 25V	$P_o \leq$ 15W	7.6	8	8.4	V
ΔV_o*	Line Regulation	V_i = 10.5 to 25V V_i = 11 to 17V	T_j = 25°C T_j = 25°C			160 80	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA I_o = 250 to 750mA	T_j = 25°C T_j = 25°C			160 80	mV mV
I_d	Quiescent Current	T_j = 25°C				8	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA				0.5	mA
ΔI_d	Quiescent Current Change	V_i = 10.5 to 25V				1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA			– 0.8		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz	T_j = 25°C		52		µV/V_o
SVR	Supply Voltage Rejection	V_i = 11.5 to 21.5V	f = 120Hz	56			dB
V_d	Dropout Voltage	I_o = 1A	T_j = 25°C		2		V
R_o	Output Resistance	f = 1KHz			16		mΩ
I_{sc}	Short Circuit Current	V_i = 35V	T_j = 25°C		450		mA
I_{scp}	Short Circuit Peak Current	T_j = 25°C			2.2		A

ELECTRICAL CHARACTERISTICS FOR L7885C (refer to the test circuits, T_j = 0 to 125°C V_i = 14.5V, I_o = 500mA, C_i = 0.33µF, C_o = 0.1µF unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C		8.2	8.5	8.8	V
V_o	Output Voltage	I_o = 5mA to 1A V_i = 11 to 26V	$P_o \leq$ 15W	8.1	8.5	8.9	V
ΔV_o*	Line Regulation	V_i = 11 to 27V V_i = 11.5 to 17.5V	T_j = 25°C T_j = 25°C			160 80	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA I_o = 250 to 750mA	T_j = 25°C T_j = 25°C			160 80	mV mV
I_d	Quiescent Current	T_j = 25°C				8	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA				0.5	mA
ΔI_d	Quiescent Current Change	V_i = 11 to 27V				1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA			– 0.8		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz	T_j = 25°C		55		µV/V_o
SVR	Supply Voltage Rejection	V_i = 12 to 22V	f = 120Hz	56			dB
V_d	Dropout Voltage	I_o = 1A	T_j = 25°C		2		V
R_o	Output Resistance	f = 1KHz			16		mΩ
I_{sc}	Short Circuit Current	V_i = 35V	T_j = 25°C		450		mA
I_{scp}	Short Circuit Peak Current	T_j = 25°C			2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7812C (refer to the test circuits, T_j = 0 to 125°C V_i = 19V, I_o = 500mA, C_i = 0.33µF, C_o = 0.1µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C	11.5	12	12.5	V
V_o	Output Voltage	I_o = 5mA to 1A $P_o \leq$ 15W V_i = 14.5 to 27V	11.4	12	12.6	V
ΔV_o*	Line Regulation	V_i = 14.5 to 30V T_j = 25°C V_i = 16 to 22V T_j = 25°C			240 120	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA T_j = 25°C I_o = 250 to 750mA T_j = 25°C			240 120	mV mV
I_d	Quiescent Current	T_j = 25°C			8	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 14.5 to 30V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA		– 1		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25°C		75		µV/V_o
SVR	Supply Voltage Rejection	V_i = 15 to 25V f = 120Hz	55			dB
V_d	Dropout Voltage	I_o = 1A T_j = 25°C		2		V
R_o	Output Resistance	f = 1KHz		18		mΩ
I_{sc}	Short Circuit Current	V_i = 35V T_j = 25°C		350		mA
I_{scp}	Short Circuit Peak Current	T_j = 25°C		2.2		A

ELECTRICAL CHARACTERISTICS FOR L7815C (refer to the test circuits, T_j = 0 to 125°C V_i = 23V, I_o = 500mA, C_i = 0.33µF, C_o = 0.1µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C	14.4	15	15.6	V
V_o	Output Voltage	I_o = 5mA to 1A $P_o \leq$ 15W V_i = 17.5 to 30V	14.25	15	15.75	V
ΔV_o*	Line Regulation	V_i = 17.5 to 30V T_j = 25°C V_i = 20 to 26V T_j = 25°C			300 150	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA T_j = 25°C I_o = 250 to 750mA T_j = 25°C			300 150	mV mV
I_d	Quiescent Current	T_j = 25°C			8	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 17.5 to 30V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA		– 1		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25°C		90		µV/V_o
SVR	Supply Voltage Rejection	V_i = 18.5 to 28.5V f = 120Hz	54			dB
V_d	Dropout Voltage	I_o = 1A T_j = 25°C		2		V
R_o	Output Resistance	f = 1KHz		19		mΩ
I_{sc}	Short Circuit Current	V_i = 35V T_j = 25°C		230		mA
I_{scp}	Short Circuit Peak Current	T_j = 25°C		2.1		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7818C (refer to the test circuits, T_j = 0 to 125°C V_i = 26V, I_o = 500mA, C_i = 0.33µF, C_o = 0.1µF unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C		17.3	18	18.7	V
V_o	Output Voltage	I_o = 5mA to 1A V_i = 21 to 33V	$P_o \leq$ 15W	17.1	18	18.9	V
ΔV_o*	Line Regulation	V_i = 21 to 33V V_i = 24 to 30V	T_j = 25°C T_j = 25°C			360 180	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA I_o = 250 to 750mA	T_j = 25°C T_j = 25°C			360 180	mV mV
I_d	Quiescent Current	T_j = 25°C				8	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA				0.5	mA
ΔI_d	Quiescent Current Change	V_i = 21 to 33V				1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA			– 1		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz	T_j = 25°C		110		µV/V_o
SVR	Supply Voltage Rejection	V_i = 22 to 32V	f = 120Hz	53			dB
V_d	Dropout Voltage	I_o = 1A	T_j = 25°C		2		V
R_o	Output Resistance	f = 1KHz			22		mΩ
I_{sc}	Short Circuit Current	V_i = 35V	T_j = 25°C		200		mA
I_{scp}	Short Circuit Peak Current	T_j = 25°C			2.1		A

ELECTRICAL CHARACTERISTICS FOR L7820C (refer to the test circuits, T_j = 0 to 125°C V_i = 28V, I_o = 500mA, C_i = 0.33µF, C_o = 0.1µF unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C		19.2	20	20.8	V
V_o	Output Voltage	I_o = 5mA to 1A V_i = 23 to 35V	$P_o \leq$ 15W	19	20	21	V
ΔV_o*	Line Regulation	V_i = 22.5 to 35V V_i = 26 to 32V	T_j = 25°C T_j = 25°C			400 200	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA I_o = 250 to 750mA	T_j = 25°C T_j = 25°C			400 200	mV mV
I_d	Quiescent Current	T_j = 25°C				8	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA				0.5	mA
ΔI_d	Quiescent Current Change	V_i = 23 to 35V				1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA			– 1		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz	T_j = 25°C		150		µV/V_o
SVR	Supply Voltage Rejection	V_i = 24 to 35V	f = 120Hz	52			dB
V_d	Dropout Voltage	I_o = 1A	T_j = 25°C		2		V
R_o	Output Resistance	f = 1KHz			24		mΩ
I_{sc}	Short Circuit Current	V_i = 35V	T_j = 25°C		180		mA
I_{scp}	Short Circuit Peak Current	T_j = 25°C			2.2		A

* Load and line regulation are specified at constant junction temperature Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7824C (refer to the test circuits, T_j = 0 to 125°C V_i = 33V, I_o = 500mA, C_i = 0.33µF, C_o = 0.1µF unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C		23	24	25	V
V_o	Output Voltage	I_o = 5mA to 1A V_i = 27 to 38V	$P_o \leq$ 15W	22.8	24	25.2	V
ΔV_o*	Line Regulation	V_i = 27 to 38V V_i = 30 to 36V	T_j = 25°C T_j = 25°C			480 240	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA I_o = 250 to 750mA	T_j = 25°C T_j = 25°C			480 240	mV mV
I_d	Quiescent Current	T_j = 25°C				8	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA				0.5	mA
ΔI_d	Quiescent Current Change	V_i = 27 to 38V				1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA			– 1.5		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz	T_j = 25°C		170		µV/V_o
SVR	Supply Voltage Rejection	V_i = 28 to 38V	f = 120Hz	50			dB
V_d	Dropout Voltage	I_o = 1A	T_j = 25°C		2		V
R_o	Output Resistance	f = 1KHz			28		mΩ
I_{sc}	Short Circuit Current	V_i = 35V	T_j = 25°C		150		mA
I_{scp}	Short Circuit Peak Current	T_j = 25°C			2.1		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

Figure 4 : Dropout Voltage vs. Junction Temperature.

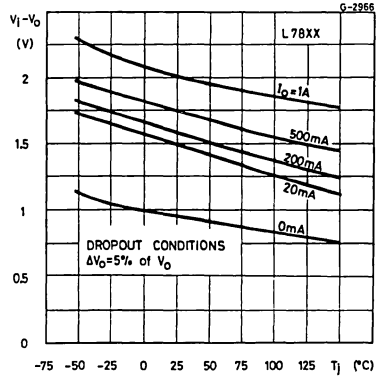


Figure 5 : Peak Output Current vs. Input/output Differential Voltage.

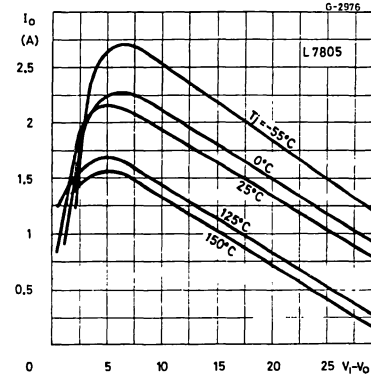


Figure 6 : Supply Voltage Rejection vs. Frequency.

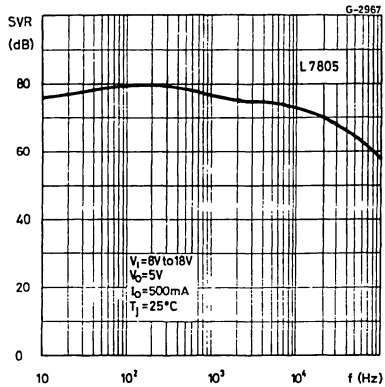


Figure 7 : Output Voltage vs. Junction Temperature.

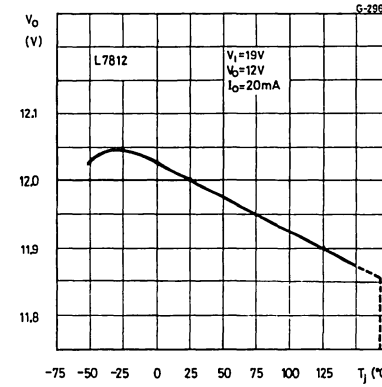


Figure 8 : Output Impedance vs. Frequency.

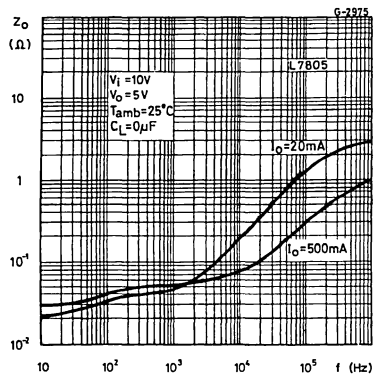


Figure 9 : Quiescent Current vs. Junction Temperature.

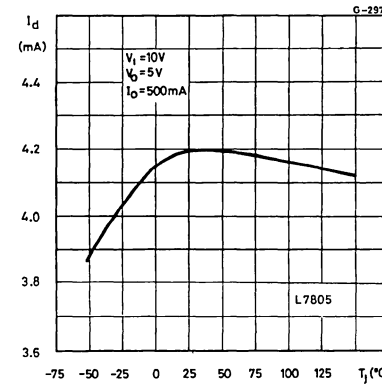


Figure 10 : Load Transient Response.

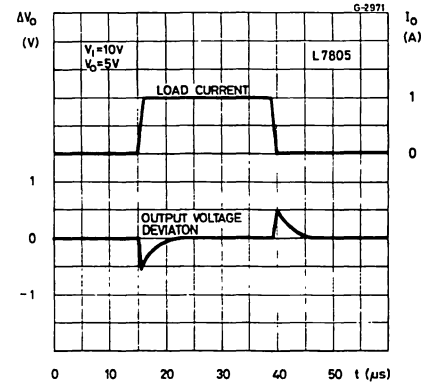


Figure 11 : Line Transient Response.

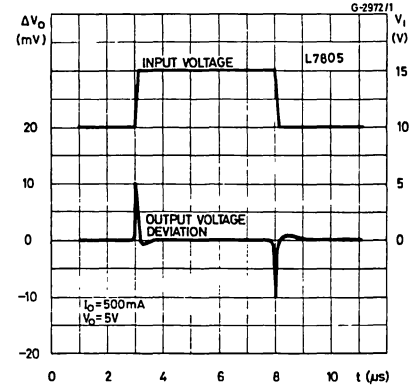


Figure 12 : Quiescent Current vs. Input Voltage.

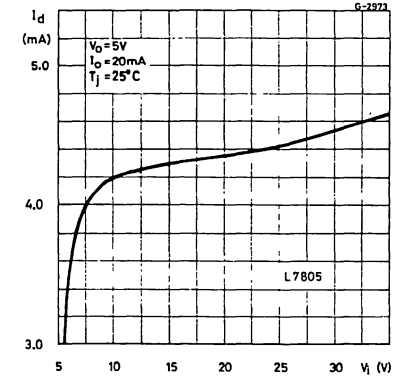


Figure 13 : Fixed Output Regulator.

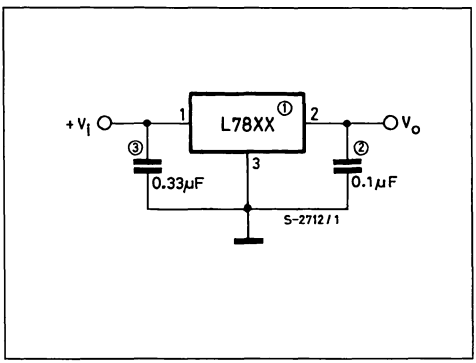
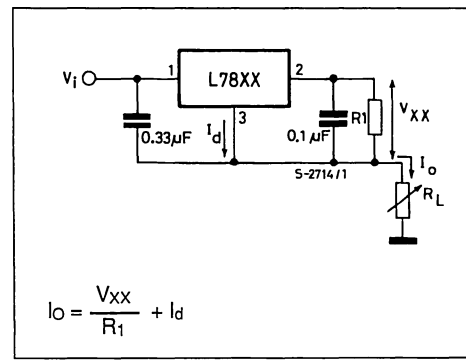
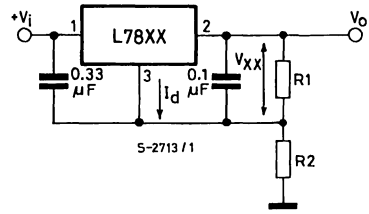


Figure 14 : Current Regulator.



Notes : 1. To specify an output voltage, substitute voltage value for "XX".
2. Although no output capacitor is needed for stability, it does improve transient response.
3. Required if regulator is located an appreciable distance from power supply filter.

Figure 15 : Circuit for Increasing Output Voltage.



$I_{R1} \geq 5\ I_d$

$$V_O = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + I_d R_2$$

Figure 16 : Adjustable Output Regulator (7 to 30V).

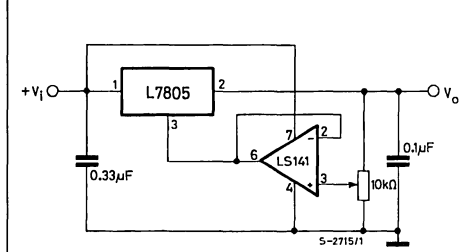
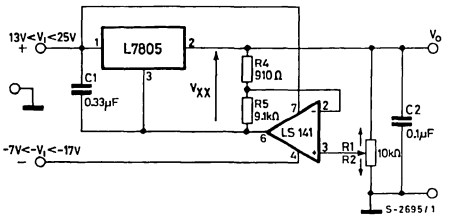
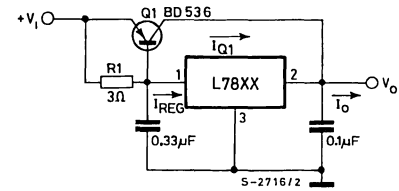


Figure 17 : 0.5 to 10V Regulator.



$$V_O = V_{XX}\frac{R_4}{R_1}$$

Figure 18 : High Current Voltage Regulator.



$$R_1 = \frac{V_{BEQ1}}{I_{REQ} - \frac{I_{Q1}}{\beta_{Q_1}}}$$

$$I_O = I_{REG} + Q_1\left[I_{REG} - \frac{V_{BEQ1}}{R_1}\right]$$

Figure 19 : High Output Current with Short Circuit Protection.

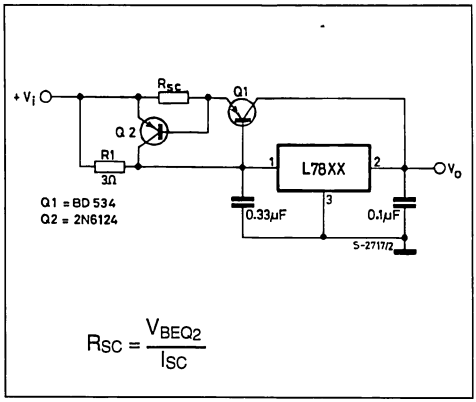


Figure 20 : Tracking Voltage Regulator.

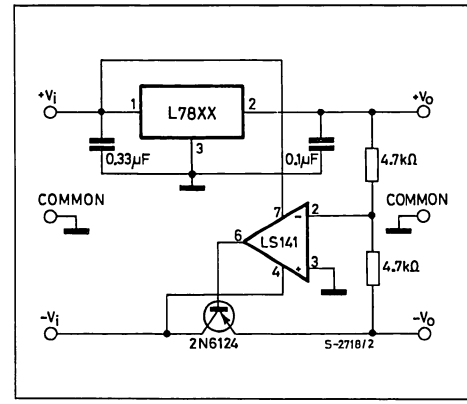
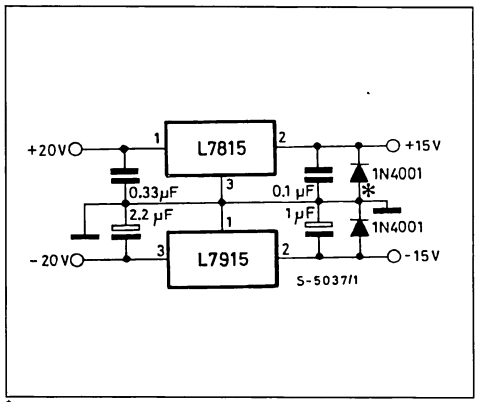


Figure 21 : Split Power Supply (± 15V – 1A).



* Against potential latch-up problems.

Figure 22 : Negative Output Voltage Circuit.

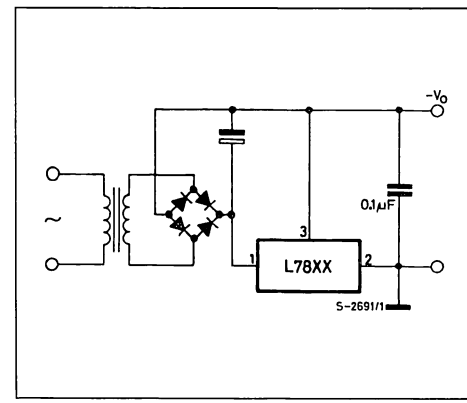


Figure 23 : Switching Regulator.

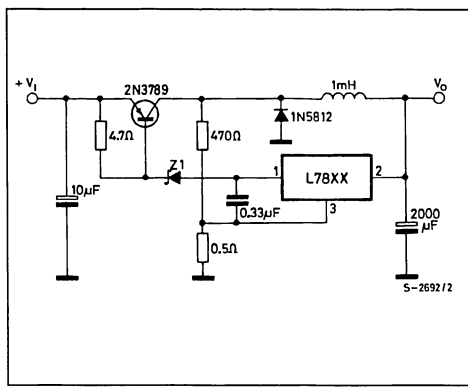


Figure 24 : High Input Voltage Circuit.

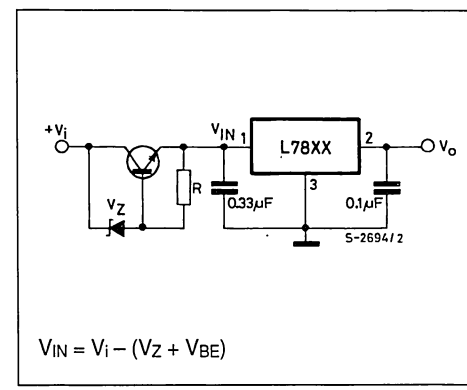


Figure 25 : High Input Voltage Circuit.

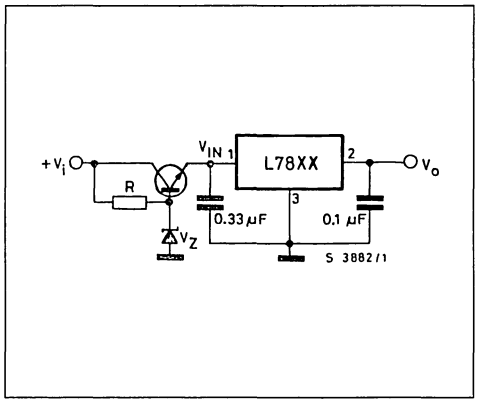


Figure 26 : High Output Voltage Regulator.

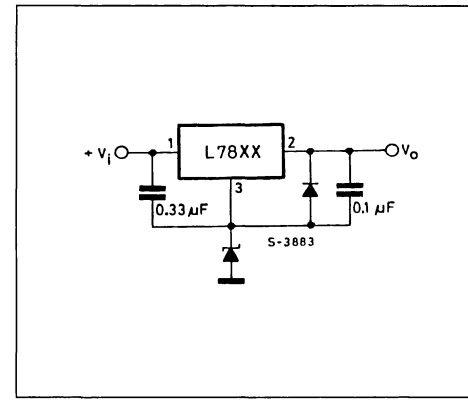


Figure 27 : High Input and Output Voltage.

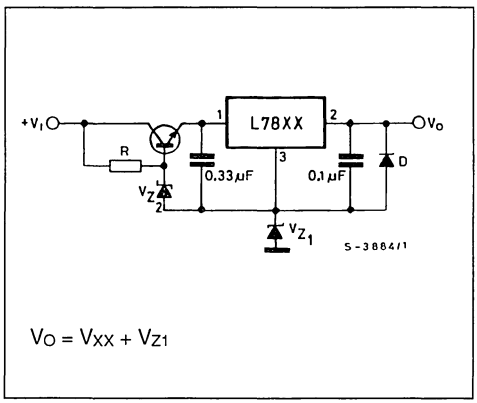


Figure 28 : Reducing Power Dissipation with Dropping Resistor.

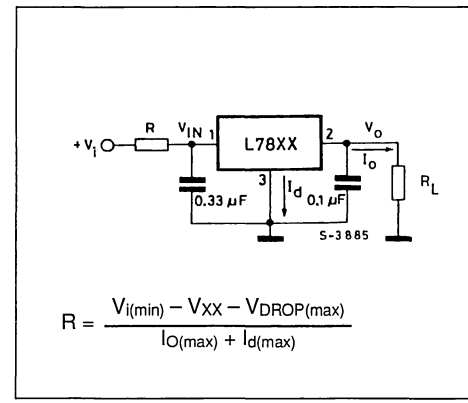


Figure 29 : Remote Shutdown.

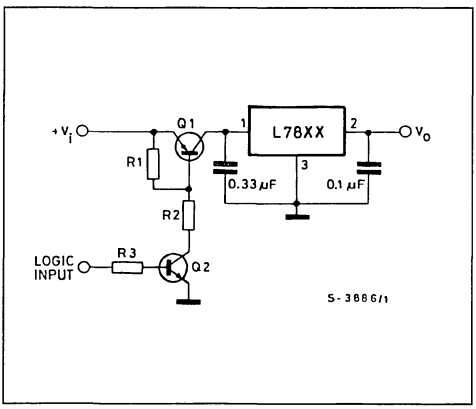
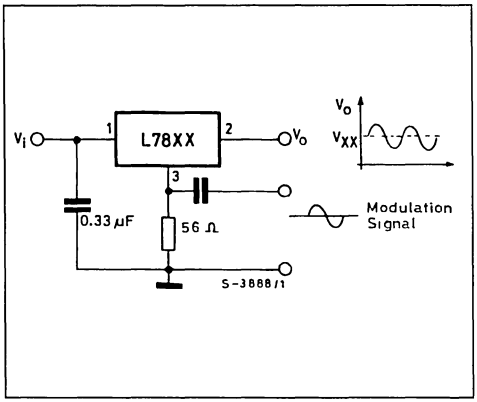
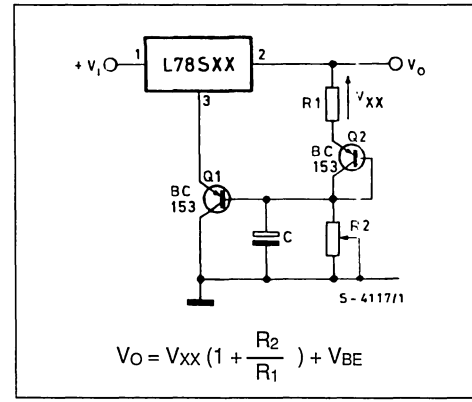


Figure 30 : Power AM Modulator (unity voltage gain, Io ≤ 1A).



Note : The circuit performs well up to 100KHz.

Figure 31 : Adjustable Output Voltage with Temperature Compensation.



$$V_O = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + V_{BE}$$

Note : Q_2 is connected as a diode in order to compensate the variation of the Q_1 V_{BE} with the temperature. C allows a slow rise-time of the V_O

Figure 32 : Light Controllers ($V_{O\,min} = V_{XX} + V_{BE}$).

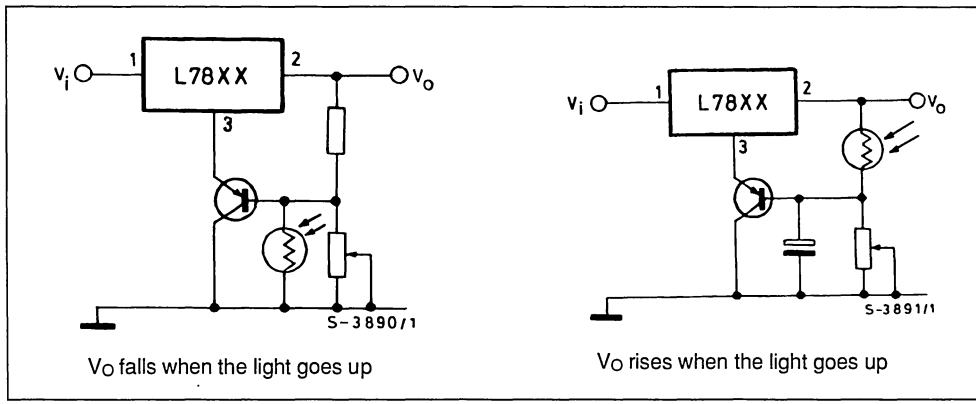
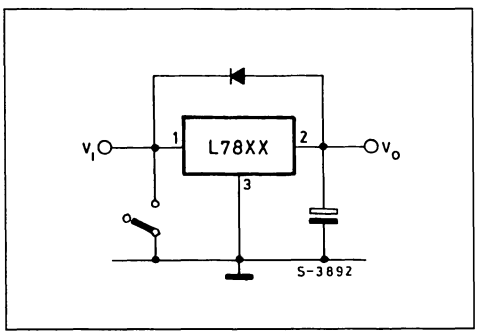


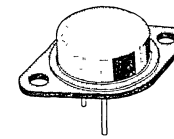
Figure 33 : Protection against Input Short-circuit with High Capacitance Loads.



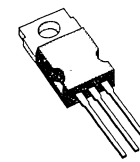
Applications with high capacitance loads and an output voltage greater than 6 volts need an external diode (see fig 33) to protect the device against input short circuit. In this case the input voltage falls rapidly while the output voltage decreases showly. The capacitance discharges by means of the Base-Emitter junction of the series pass transistor in the regulator. If the energy is sufficiently high, the tran-sistor may be destroyed. The external diode by-passes the current from the IC to ground.

PRECISION 1A REGULATORS

- OUTPUT CURRENT IN EXCESS OF 1A
- OUTPUT VOLTAGES OF 5; 6; 8; 12; 15; 18; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION
- 2% OUTPUT VOLTAGE TOLERANCE
- GUARANTEED IN EXTENDED TEMPERATURE RANGES



TO-3

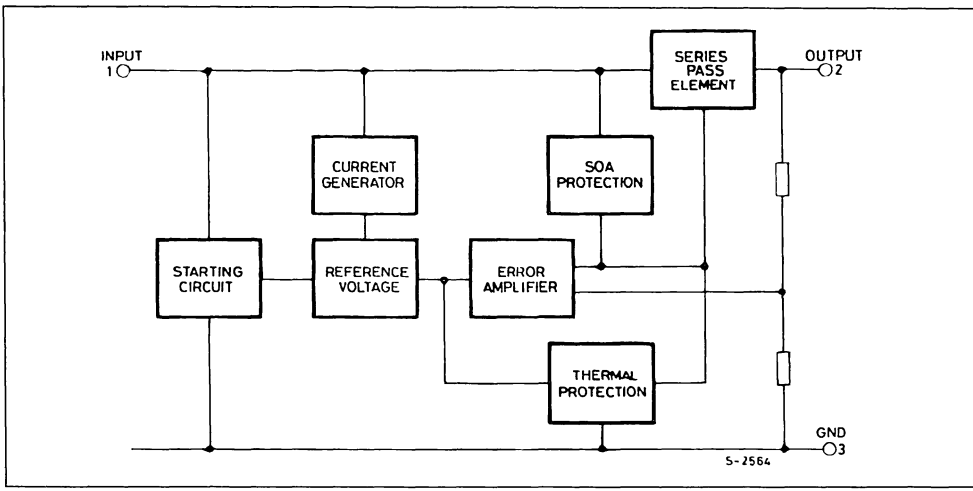


TO-220

DESCRIPTION

The L7800A series of three-terminal positive regulators is available in TO-220 and TO-3 packages and with several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

BLOCK DIAGRAM



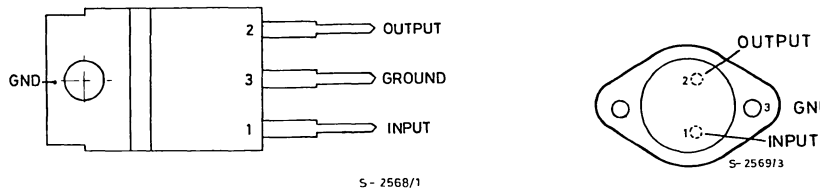
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage (for V_o = 5 to 18V) (for V_o = 24V)	35 40	V V
I_o	Output Current	Internally limited	
P_{tot}	Power Dissipation	Internally limited	
T_j	Operating Junction Temperature for L7800AC for L7800AB	0 to 125 – 40 to 125	°C °C
T_{stg}	Storage Temperature	– 65 to + 150	°C

THERMAL DATA

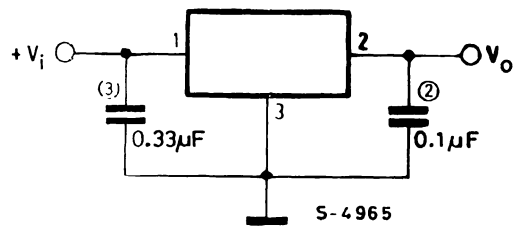
Symbol	Parameter		TO-220	TO-3	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	4	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	50	35	°C/W

CONNECTION DIAGRAM AND ORDERING NUMBERS (top view)

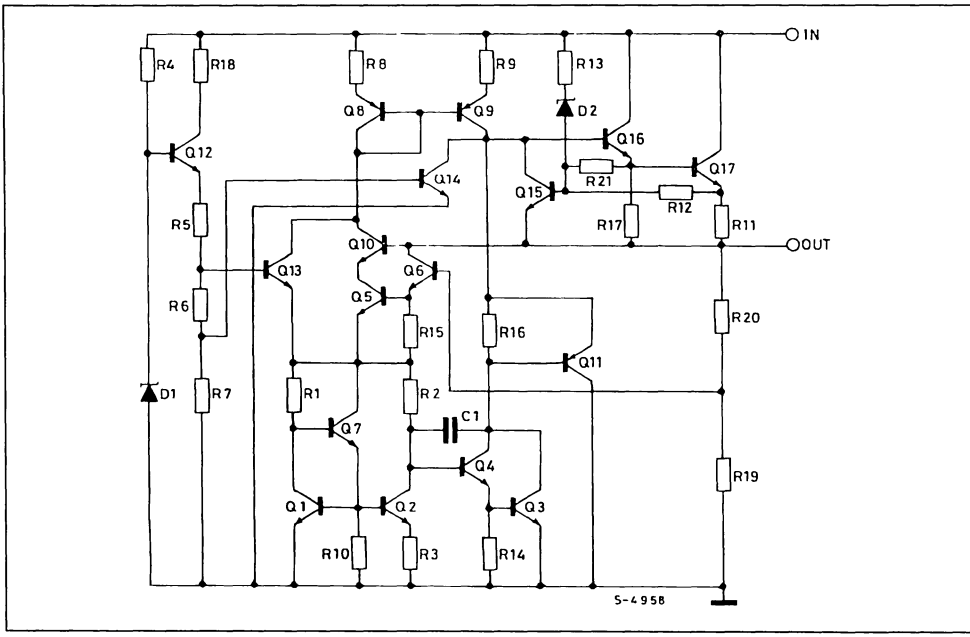


Ordering Numbers			Output Voltage
T_j = – 40 to 125°C	T_j = 0 to 125°C		
TO-220	TO-220	TO-3	
L7805ABV	L7805ACV	L7805ACT	5V
L7806ABV	L7806ACV	L7806ACT	6V
L7808ABV	L7808ACV	L7808ACT	8V
L7812ABV	L7812ACV	L7812ACT	12V
L7815ABV	L7815ACV	L7815ACT	15V
L7818ABV	L7818ACV	L7818ACT	18V
L7824ABV	L7824ACV	L7824ACT	24V

TYPICAL APPLICATION



SCHEMATIC DIAGRAM



TEST CIRCUITS

Figure 1 : DC Parameters.

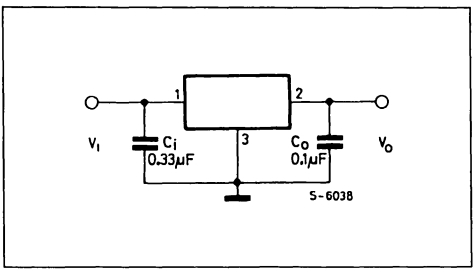


Figure 2 : Load Regulation.

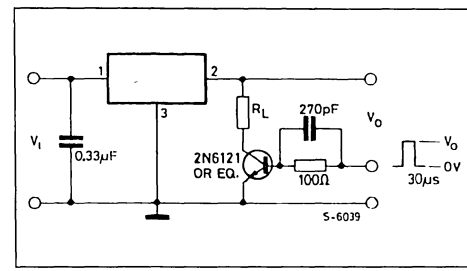
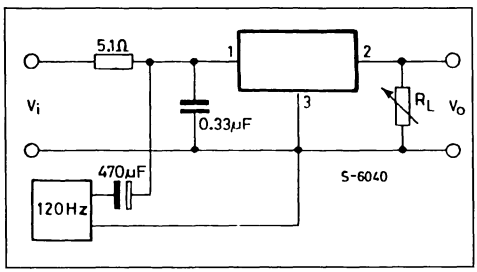


Figure 3 : Ripple Rejection.



ELECTRICAL CHARACTERISTICS L7805A (V_i = 10V, I_o = 1A, T_j = 0 to 125°C (L7805AC), T_j = – 40 to 125°C (L7805AB) unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C	4.9	5	5.1	V
V_o	Output Voltage	I_o = 5mA to 1A, $P_o \leq$ 15W V_i = 7.5 to 20V	4.8	5	5.2	V
ΔV_o*	Line Regulation	V_i = 7.5 to 25V, I_o = 500mA V_i = 8 to 12V		7 10	50 50	mV mV
		V_i = 8 to 12V, T_j = 25°C V_i = 7.3 to 20V, T_j = 25°C		2 7	25 50	mV mV
ΔV_o*	Load Regulation	I_o = 5mA to 1A I_o = 5mA to 1.5A, T_j = 25°C I_o = 250 to 750mA		25 25 8	100 100 50	mV mV mV
I_d	Quiescent Current	T_j = 25°C		4.3	6 6	mA mA
ΔI_d	Quiescent Current Change	V_i = 8 to 25V, I_o = 500mA V_i = 7.5 to 20V, T_j = 25°C I_o = 5mA to 1A			0.8 0.8 0.5	mA mA mA
SVR	Supply Voltage Rejection	V_i = 8 to 18V, f = 120Hz I_o = 500mA		68		dB
V_d	Dropout Voltage	I_o = 1A T_j = 25°C		2		V
e_N	Output Noise Voltage	f = 10Hz to 100KHz, T_j = 25°C		10		$\mu V/V_o$
R_o	Output Resistance	f = 1KHz		17		mΩ
I_{sc}	Short Circuit Current	T_{amb} = 25°C V_i = 35V		0.2		A
I_{scp}	Short Circuit Peak Current	T_j = 25°C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift			– 1.1		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS L7806A (V_I = 11V, I_O = 1A, T_J = 0 to 125°C (L7806AC), T_J = – 40 to 125°C (L7806AB) ; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_O	Output Voltage	T_J = 25°C	5.88	6	6.12	V
V_O	Output Voltage	I_O = 5mA to 1A, $P_O \leq$ 15W V_I = 8.6 to 21V	5.76	6	6.24	V
ΔV_O*	Line Regulation	V_I = 8.6 to 25V, I_O = 500mA V_I = 9 to 13V		9 11	60 60	mV mV
		V_I = 9 to 13V, T_J = 25°C V_I = 8.3 to 21V, T_J = 25°C		3 9	30 60	mV mV
ΔV_O*	Load Regulation	I_O = 5mA to 1A I_O = 5mA to 1.5A, T_J = 25°C I_O = 250 to 750mA		43 43 16	100 100 50	mV mV mV
I_d	Quiescent Current	T_J = 25°C		4.3	6 6	mA mA
ΔI_d	Quiescent Current Change	V_I = 9 to 25V, I_O = 500mA V_I = 8.6 to 21V, T_J = 25°C I_O = 5mA to 1A			0.8 0.8 0.5	mA mA mA
SVR	Supply Voltage Rejection	V_I = 9 to 19V, f = 120Hz I_O = 500mA		65		dB
V_d	Dropout Voltage	I_O = 1A T_J = 25°C		2		V
e_N	Output Noise Voltage	T_J = 25°C, f = 10Hz to 100KHz		10		$\mu V/V_O$
R_O	Output Resistance	f = 1KHz		17		mΩ
I_{sc}	Short Circuit Current	T_{amb} = 25°C V_I = 35V		0.2		A
I_{scp}	Short Circuit Peak Current	T_J = 25°C		2.2		A
$\frac{\Delta V_O}{\Delta T}$	Output Voltage Drift			– 0.8		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS L7808A (V_i = 14V, I_o = 1A, T_j = 0 to 125°C (L7808AC), T_j = – 40 to 125°C (L7808AB), unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C	7.84	8	8.16	V
V_o	Output Voltage	I_o = 5mA to 1A, $P_o \leq$ 15W V_i = 10.6 to 23V	7.7	8	8.3	V
ΔV_o*	Line Regulation	V_i = 10.6 to 25V, I_o = 500mA V_i = 11 to 17V		12 15	80 80	mV mV
		V_i = 11 to 17V, T_j = 25°C V_i = 10.4 to 23V, T_j = 25°C		5 12	40 80	mV mV
ΔV_o*	Load Regulation	I_o = 5mA to 1A I_o = 5mA to 1.5A, T_j = 25°C I_o = 250 to 750mA		45 45 16	100 100 50	mV mV mV
I_d	Quiescent Current	T_j = 25°C		4.3	6 6	mA mA
ΔI_d	Quiescent Current Change	V_i = 11 to 25V, I_o = 500mA V_i = 10.6 to 23V, T_j = 25°C I_o = 5mA to 1A			0.8 0.8 0.5	mA mA mA
SVR	Supply Voltage Rejection	V_i = 11.5 to 21.5V, f = 120Hz I_o = 500mA		62		dB
V_d	Dropout Voltage	I_o = 1A T_j = 25°C		2		V
e_N	Output Noise Voltage	T_j = 25°C, f = 10Hz to 100KHz		10		$\mu V/V_o$
R_o	Output Resistance	f = 1KHz		18		mΩ
I_{sc}	Short Circuit Current	T_{amb} = 25°C V_i = 35V		0.2		A
I_{scp}	Short Circuit Peak Current	T_j = 25°C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift			– 0.8		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS L7812A (V_i = 19V, I_o = 1A, T_j = 0 to 125°C (L7812AC), T_j = – 40 to 125°C (L7812AB), unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C	11.75	12	12.25	V
V_o	Output Voltage	I_o = 5mA to 1A, $P_o \leq$ 15W V_i = 14.8 to 27V	11.5	12	12.5	V
ΔV_o*	Line Regulation	V_i = 14.8 to 30V, I_o = 500mA V_i = 16 to 22V		13 16	120 120	mV mV
		V_i = 16 to 22V, T_j = 25°C V_i = 14.5 to 27V, T_j = 25°C		6 13	60 120	mV mV
ΔV_o*	Load Regulation	I_o = 5mA to 1A I_o = 5mA to 1.5A, T_j = 25°C I_o = 250 to 750mA		46 46 17	100 100 50	mV mV mV
I_d	Quiescent Current	T_j = 25°C		4.4	6 6	mA mA
ΔI_d	Quiescent Current Change	V_i = 15 to 30V, I_o = 500mA V_i = 14.8 to 27V, T_j = 25°C I_o = 5mA to 1A			0.8 0.8 0.5	mA mA mA
SVR	Supply Voltage Rejection	V_i = 15 to 25V, f = 120Hz I_o = 500mA		60		dB
V_d	Dropout Voltage	I_o = 1A T_j = 25°C		2		V
e_N	Output Noise Voltage	T_j = 25°C, f = 10Hz to 100KHz		10		$\mu V/V_o$
R_o	Output Resistance	f = 1KHz		18		mΩ
I_{sc}	Short Circuit Current	T_{amb} = 25°C V_i = 35V		0.2		A
I_{scp}	Short Circuit Peak Current	T_j = 25°C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift			– 1		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS L7815A (V_I = 23V, I_O = 1A, T_J = 0 to 125°C (L7815AC), T_J = – 40 to 125°C (L7815AB), unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_O	Output Voltage	T_J = 25°C	14.7	15	15.3	V
V_O	Output Voltage	I_O = 5mA to 1A, $P_O \leq$ 15W V_I = 17.9 to 30V	14.4	15	15.6	V
ΔV_O*	Line Regulation	V_I = 17.9 to 30V, I_O = 500mA V_I = 20 to 26V		13 16	150 150	mV mV
		V_I = 20 to 26V, T_J = 25°C V_I = 17.5 to 30V, T_J = 25°C		6 13	75 150	mV mV
ΔV_O*	Load Regulation	I_O = 5mA to 1A I_O = 5mA to 1.5A, T_J = 25°C I_O = 250 to 750mA		52 52 20	100 100 50	mV mV mV
I_d	Quiescent Current	T_J = 25°C		4.4	6 6	mA mA
ΔI_d	Quiescent Current Change	V_I = 17.5 to 30V, I_O = 500mA V_I = 17.5 to 30V, T_J = 25°C I_O = 5mA to 1A			0.8 0.8 0.5	mA mA mA
SVR	Supply Voltage Rejection	V_I = 18.5 to 28.5V, f = 120Hz I_O = 500mA		58		dB
V_d	Dropout Voltage	I_O = 1A T_J = 25°C		2		V
e_N	Output Noise Voltage	T_J = 25°C, f = 10Hz to 100KHz		10		$\mu V/V_O$
R_O	Output Resistance	f = 1KHz		19		mΩ
I_{sc}	Short Circuit Current	T_{amb} = 25°C V_I = 35V		0.2		A
I_{scp}	Short Circuit Peak Current	T_J = 25°C		2.2		A
$\frac{\Delta V_O}{\Delta T}$	Output Voltage Drift			– 1		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS L7818A (V_i = 27V, I_o = 1A, T_j = 0 to 125°C (L7818AC), T_j = – 40 to 125°C (L7818AB), unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C	17.64	18	18.36	V
V_o	Output Voltage	I_o = 5mA to 1A, $P_o \leq$ 15W V_i = 21 to 33V	17.3	18	18.7	V
ΔV_o*	Line Regulation	V_i = 21 to 33V, I_o = 500mA V_i = 24 to 30V		25 28	180 180	mV mV
		V_i = 24 to 30V, T_j = 25°C V_i = 20.6 to 33V, T_j = 25°C		10 25	90 180	mV mV
ΔV_o*	Load Regulation	I_o = 5mA to 1A I_o = 5mA to 1.5A, T_j = 25°C I_o = 250 to 750mA		55 55 22	100 100 50	mV mV mV
I_d	Quiescent Current	T_j = 25°C		4.5	6 6	mA mA
ΔI_d	Quiescent Current Change	V_i = 21 to 33V, I_o = 500mA V_i = 21 to 33V, T_j = 25°C I_o = 5mA to 1A			0.8 0.8 0.5	mA mA mA
SVR	Supply Voltage Rejection	V_i = 22 to 32V, f = 120Hz I_o = 500mA		57		dB
V_d	Dropout Voltage	I_o = 1A T_j = 25°C		2		V
e_N	Output Noise Voltage	T_j = 25°C, f = 10Hz to 100KHz		10		$\mu V/V_o$
R_o	Output Resistance	f = 1KHz		19		mΩ
I_{sc}	Short Circuit Current	T_{amb} = 25°C V_i = 35V		0.2		A
I_{scp}	Short Circuit Peak Current	T_j = 25°C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift			– 1		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS L7824A (V_I = 33V, I_O = 1A, T_j = 0 to 125°C (L7824AC), T_j = – 40 to 125°C (L7824AB), unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_O	Output Voltage	T_j = 25°C	23.5	24	24.5	V
V_O	Output Voltage	I_O = 5mA to 1A, $P_O \leq$ 15W V_I = 27.3 to 38V	23	24	25	V
ΔV_O*	Line Regulation	V_I = 27 to 38V, I_O = 500mA V_I = 30 to 36V		31 35	240 240	mV mV
		V_I = 30 to 36V, T_j = 25°C V_I = 26.7 to 38V, T_j = 25°C		14 31	120 240	mV mV
ΔV_O*	Load Regulation	I_O = 5mA to 1A I_O = 5mA to 1.5A, T_j = 25°C I_O = 250 to 750mA		60 60 25	100 100 50	mV mV mV
I_d	Quiescent Current	T_j = 25°C		4.6	6 6	mA mA
ΔI_d	Quiescent Current Change	V_I = 27.3 to 38V, I_O = 500mA V_I = 27.3 to 38V, T_j = 25°C I_O = 5mA to 1A			0.8 0.8 0.5	mA mA mA
SVR	Supply Voltage Rejection	V_I = 28 to 38V, f = 120Hz I_O = 500mA		54		dB
V_d	Dropout Voltage	I_O = 1A T_j = 25°C		2		V
e_N	Output Noise Voltage	T_j = 25°C, f = 10Hz to 100KHz		10		$\mu V/V_O$
R_O	Output Resistance	f = 1KHz		20		mΩ
I_{sc}	Short Circuit Current	T_{amb} = 25°C V_I = 35V		0.2		A
I_{scp}	Short Circuit Peak Current	T_j = 25°C		2.2		A
$\frac{\Delta V_O}{\Delta T}$	Output Voltage Drift			– 1.5		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

The L7800A Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33µF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Figure 4 : Current Regulator.

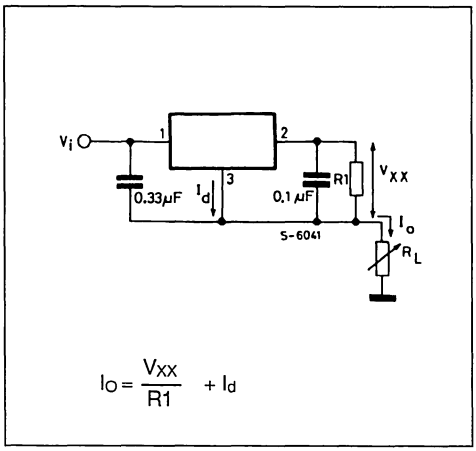
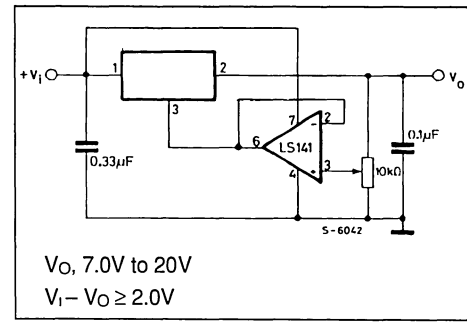


Figure 5 : Adjustable Output Regulator.



The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0V greater than the regulator voltage.

Figure 6 : Current Boost Regulator.

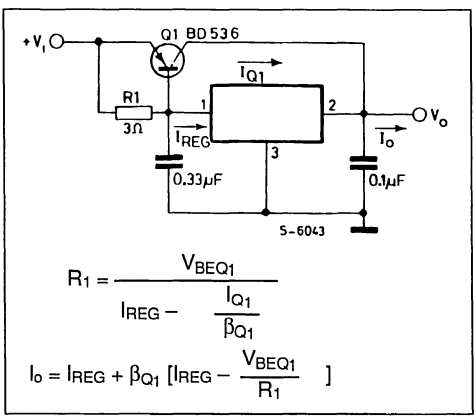
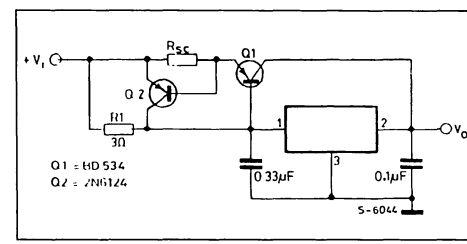


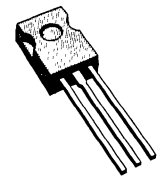
Figure 7 : Short-circuit Protection.



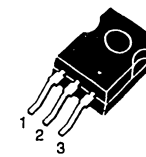
The circuit of figure 6 can be modified to provide supply protection against short circuit by adding a short-circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a four-ampere plastic power transistor is specified.

POSITIVE VOLTAGE REGULATORS

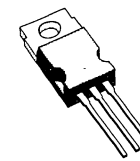
- OUTPUT CURRENT TO 0.5A
- OUTPUT VOLTAGES OF 5 ; 6 ; 8 ; 12 ; 15 ; 18 ; 20 ; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION



SOT-82



SOT-194

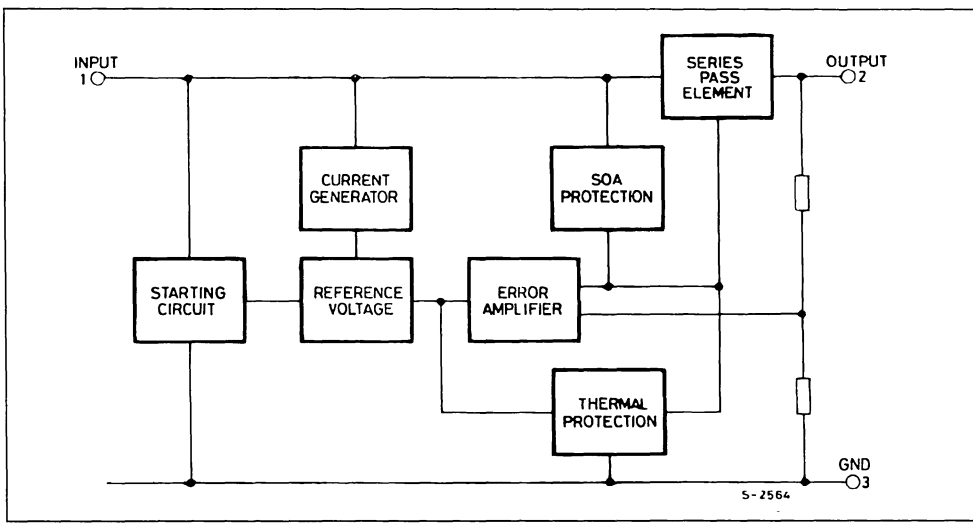


TO-220

DESCRIPTION

The L78M00 series of three-terminal positive regulators is available in TO-220 and SOT-82 packages and with several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 0.5A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

BLOCK DIAGRAM



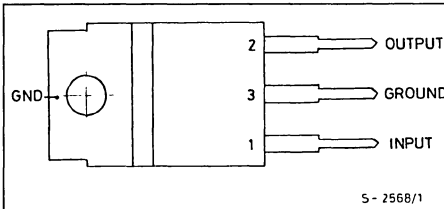
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage (for V_o = 5 to 18V) (for V_o = 20, 24V)	35 40	V V
I_o	Output Current	Internally limited	
P_{tot}	Power Dissipation	Internally limited	
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_{op}	Operating Junction Temperature	0 to + 150	°C

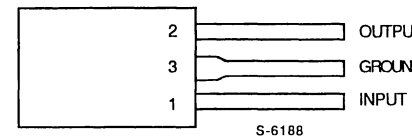
THERMAL DATA

Symbol	Parameter		SOT-82 SOT-194	TO-220	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	8	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	50	°C/W

CONNECTION DIAGRAM AND ORDERING NUMBERS (top view)



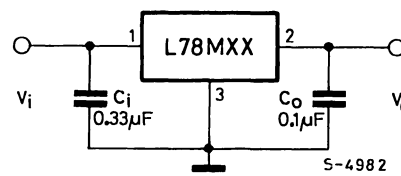
TO-220



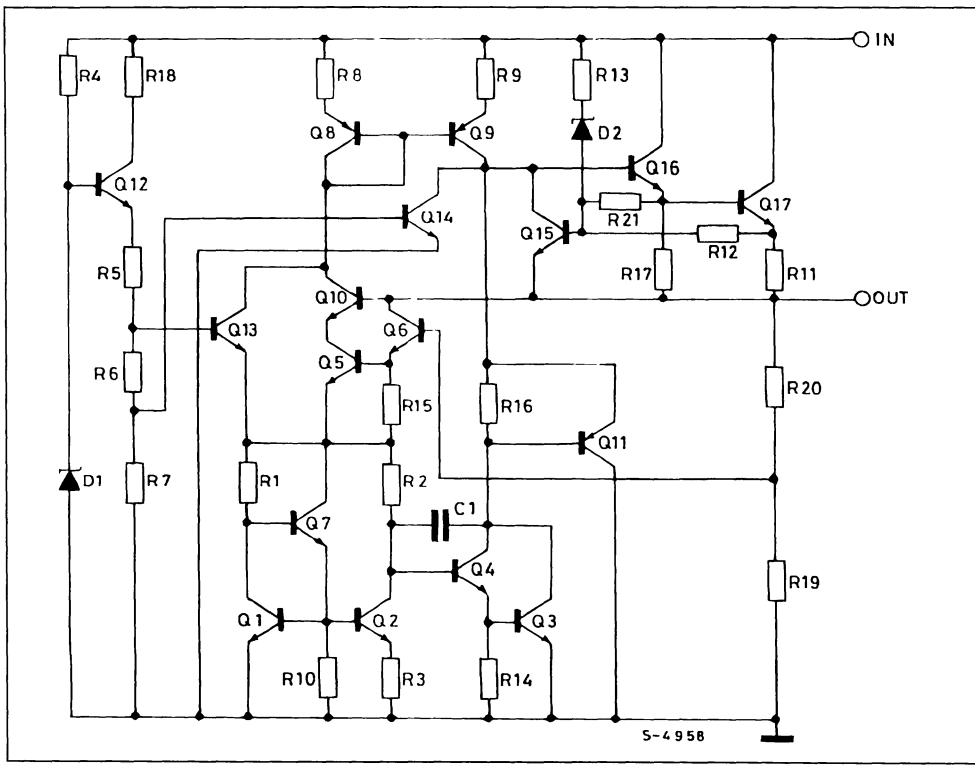
SOT82/194

Order Codes			Output Voltage
TO-220	SOT-82	SOT-194	
L78M05CV	L78M05CX	L78M05CS	5V
L78M06CV	L78M06CX	L78M06CS	6V
L78M08CV	L78M08CX	L78M08CS	8V
L78M12CV	L78M12CX	L78M12CS	12V
L78M15CV	L78M15CX	L78M15CS	15V
L78M18CV	L78M18CX	L78M18CS	18V
L78M20CV	L78M20CX	L78M20CS	20V
L78M24CV	L78M24CX	L78M24CS	24V

APPLICATION CIRCUIT



SCHEMATIC DIAGRAM



TEST CIRCUITS

Figure 1 : DC Parameters.

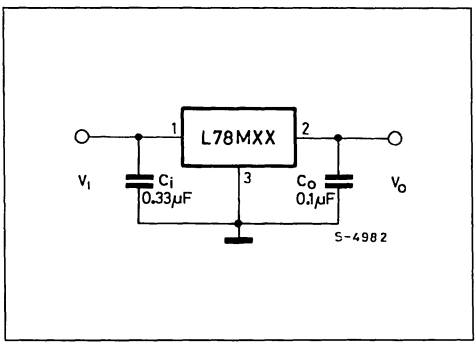


Figure 2 : Load Regulation.

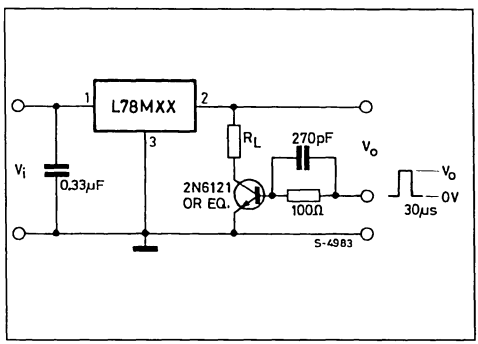
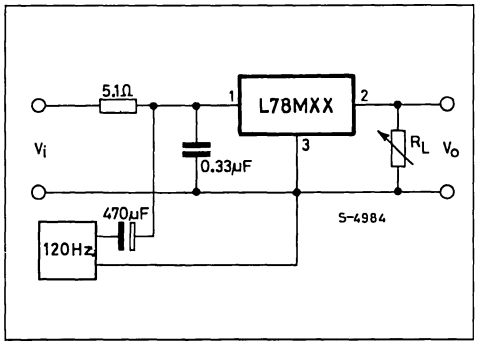


Figure 3 : Ripple Rejection.



ELECTRICAL CHARACTERISTICS L78M00C (Refer to the test circuits, T_j = 25°C, I_o = 350mA unless otherwise specified, C_i = 0.33µF, C_o = 0.1µF)

Output Voltage			5			6			8			12			Unit
Input Voltage (Unless otherwise specified)			10			11			14			19			
Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output Voltage		4.8	5	5.2	5.75	6	6.25	7.7	8	8.3	11.5	12	12.5	V
		I_o = 5 to 350mA	4.75	5	5.25	5.7	6	6.3	7.6	8	8.4	11.4	12	12.6	
			(V_i = 7 to 20V)			(V_i = 8 to 21V)			(V_i = 10.5 to 23V)			(V_i = 14 5 to 27V)			
ΔV_o	Line Regulation	I_o = 200mA			100			100			100			100	mV
					(V_i = 7 to 25V)			(V_i = 8 to 25V)			(V_i = 10.5 to 25V)			(V_i = 14.5 to 30V)	
					50			50			50			50	
					(V_i = 8 to 25V)			(V_i = 9 to 25V)			(V_i = 11 to 25V)			(V_i = 16 to 30V)	
ΔV_o	Load Regulation	I_o = 5mA to 0.5A			100			120			160			240	mV
		I_o = 5mA to 200mA			50			60			80			120	
I_d	Quiescent Current				6			6			6			6	mA
ΔI_d	Quiescent Current Change	I_o = 5mA to 350mA			0.5			0.5			0.5			0.5	mA
		I_o = 200mA			0.8			0.8			0.8			0.8	
			(V_i = 8 to 25V)			(V_i = 9 to 25V)			(V_i = 10 5 to 25V)			(V_i = 14.5 to 30V)			
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA T_j = 0 to 125°C		– 0.5			– 0.5			– 0.5			– 1.0		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz		40			45			52			75		µV
SVR	Supply Voltage Rejection	f = 120Hz I_o = 300mA	62 (V_i = 8 to 18V)			59 (V_i = 9 to 19V)			56 (V_i = 11 5 to 21 5V)			55 (V_i = 15 to 25V)			dB
V_d	Dropout Voltage			2			2			2			2		V
I_{sc}	Short Circuit Current	V_i = 35V		300			270			250			240		mA
I_{scp}	Short Circ. Peak Current			700			700			700			700		mA

ELECTRICAL CHARACTERISTICS L78M00C (continued)

Output Voltage			15			18			20			24			Unit
Input Voltage (Unless otherwise specified)			23			26			29			33			
Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output Voltage		14 4	15	15.6	17 3	18	18.7	19 2	20	20 8	23	24	25	V
		I_o = 5 to 350mA	14 25 (V_I = 17.5 to 30V)	15	15.75	17.1 (V_I = 20.5 to 33V)	18	18.9	19 (V_I = 23 to 35V)	20	21	22.8 (V_I = 27 to 38V)	24	25.2	
ΔV_o	Line Regulation	I_o = 200mA			100 (V_I = 17.5 to 30V)			100 (V_I = 21 to 33V)			100 (V_I = 23 to 35V)			100 (V_I = 27 to 38V)	mV
					50 (V_I = 20 to 30V)			50 (V_I = 24 to 33V)			50 (V_I = 24 to 35V)			50 (V_I = 28 to 38V)	
ΔV_o	Load Regulation	I_o = 5mA to 0 5A			300			360			400			480	mV
		I_o = 5mA to 200mA			150			180			200			240	
I_d	Quiescent Current				6			6			6			6	mA
ΔI_d	Quiescent Current Change	I_o = 5mA to 350mA			0 5			0 5			0.5			0 5	mA
		I_o = 200mA			0 8 (V_I = 17 5 to 30V)			0 8 (V_I = 21 to 33V)			0 8 (V_I = 23 to 35V)			0.8 (V_I = 27 to 38V)	
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA T_{amb} = 0 to 125°C		– 1			– 1 1			– 1 1			– 1 2		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz		90			100			110			170		µV
SVR	Supply Voltage Rejection	f = 120Hz I_o = 300mA	54 (V_I = 18 5 to 28 5V)			53 (V_I = 22 to 32V)			53 (V_I = 24 to 34V)			50 (V_I = 28 to 38V)			dB
V_d	Dropout Voltage			2			2			2			2		V
I_{sc}	Short Circuit Current	V_I = 35V		240			240			240			240		mA
I_{scp}	Short Circ Peak Current			700			700			700			700		mA

Figure 4 : Dropout Voltage vs. Junction Temperature.

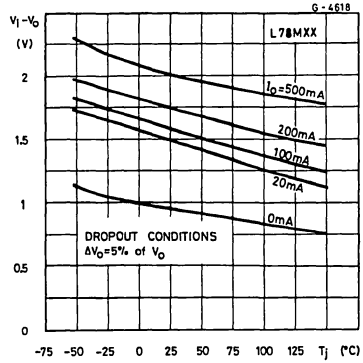


Figure 5 : Dropout Characteristics.

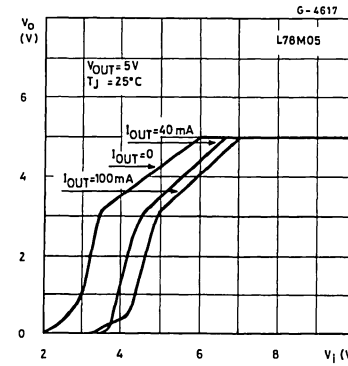


Figure 6 : Peak Output Current vs. Input-Output Differential Voltage.

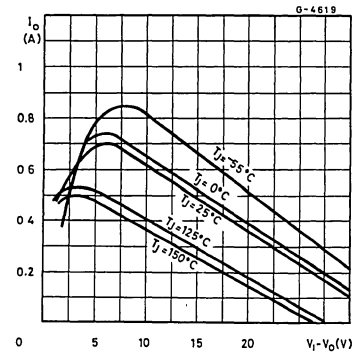


Figure 7 : Output Voltage vs. Junction Temperature.

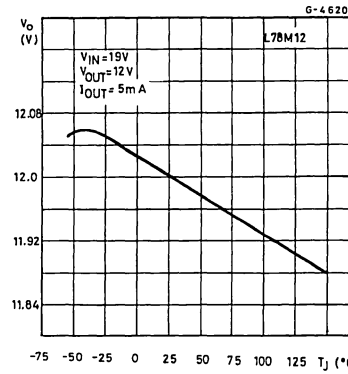


Figure 8 : Supply Voltage Rejection vs. Frequency.

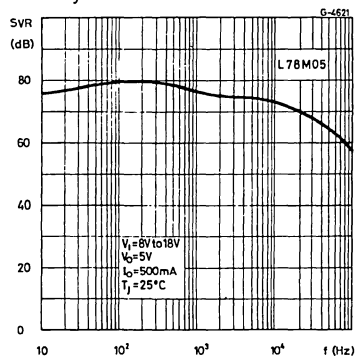


Figure 9 : Quiescent Current vs. Junction Temperature.

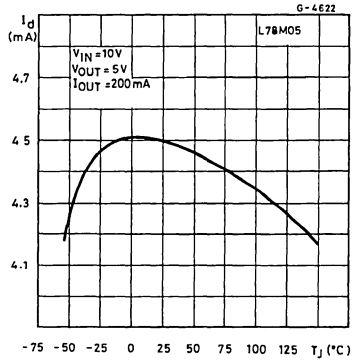


Figure 10 : Load Transient Response.

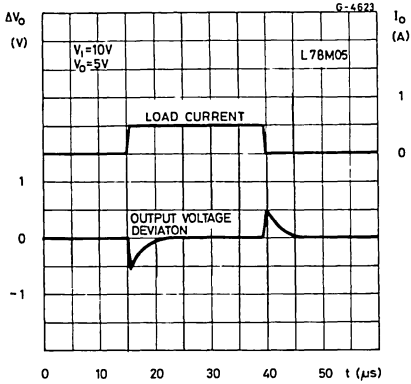


Figure 11 : Line Transient Response.

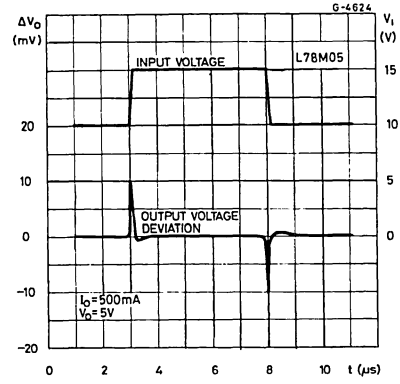


Figure 12 : Quiescent Current vs. Input Voltage.

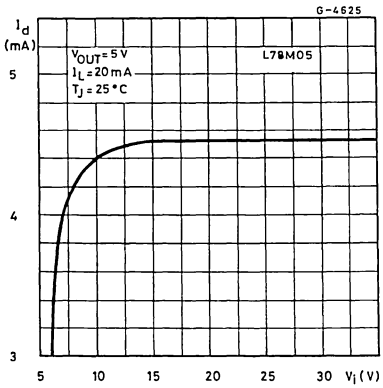
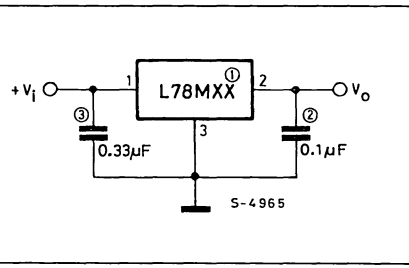
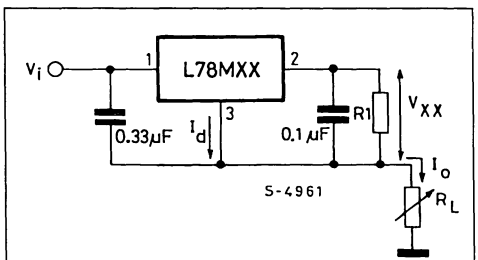


Figure 13 : Fixed Output Regulator.



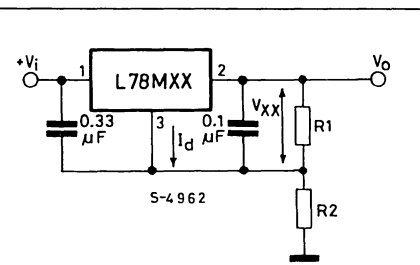
Notes :
1. To specify an output voltage, substitute voltage value for "XX".
2. Although no output capacitor is needed for stability, it does improve transient response.
3. Required if regulator is located an appreciable distance from power supply filter.

Figure 14 : Constant Current Regulator.



$$I_O = \frac{V_{XX}}{R_1} + I_d$$

Figure 15 : Circuit for Increasing Output Voltage.



$$I_{R1} \geq 5\ I_d$$

$$V_O = V_{XX}\ (1 + \frac{R_2}{R_1}) + I_d R_2$$

Figure 16 : Adjustable Output Regulator (7 to 30V).

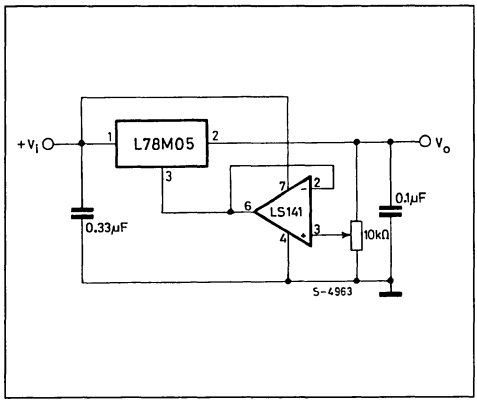


Figure 17 : 0.5 to 10V Regulator.

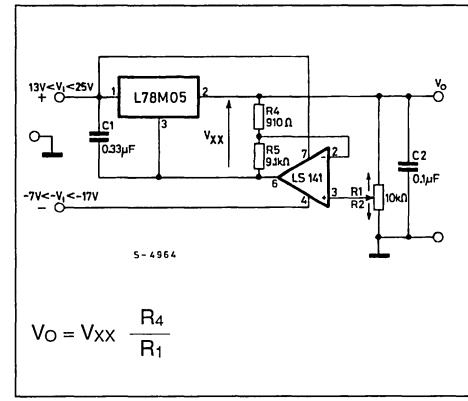


Figure 18 : High Current Voltage Regulator.

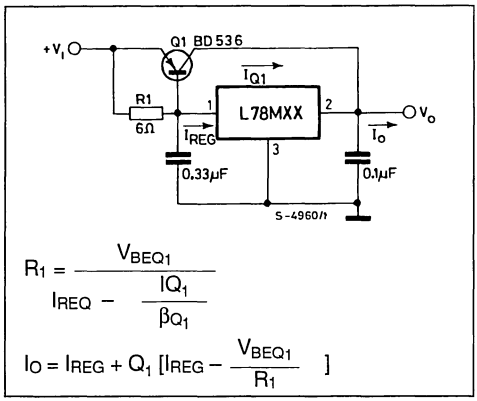


Figure 19 : High Output Current with Short Circuit Protection.

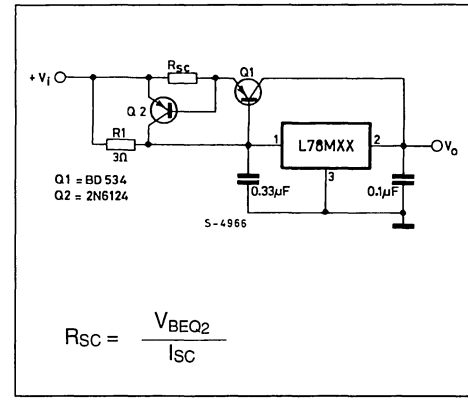


Figure 20 : Tracking Voltage Regulator.

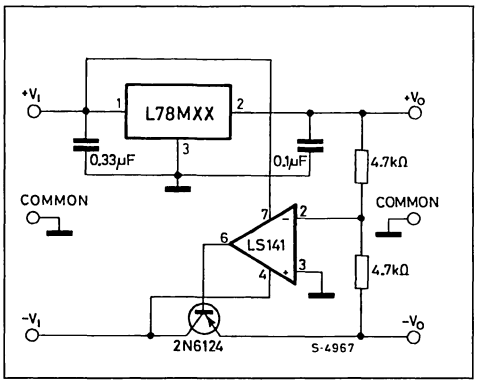


Figure 21 : High Input Voltage Circuit.

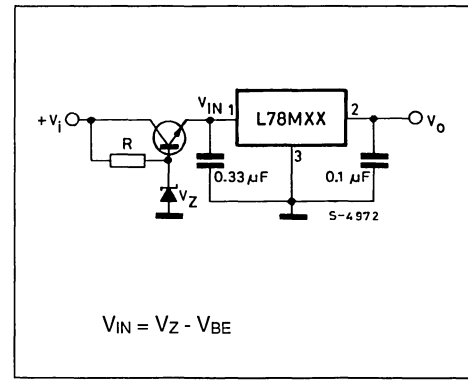
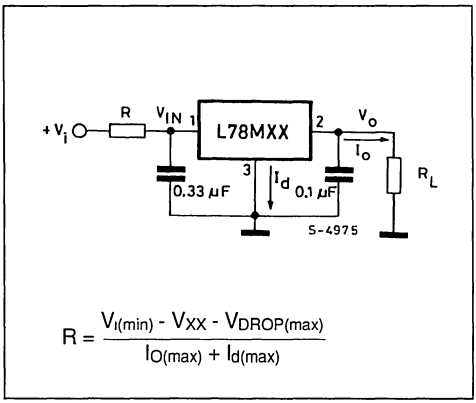
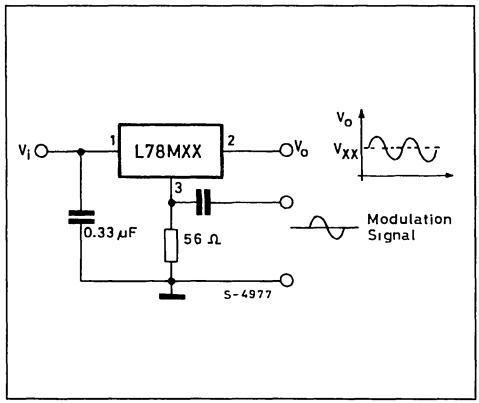


Figure 22 : Reducing Power Dissipation with Dropping Resistor.



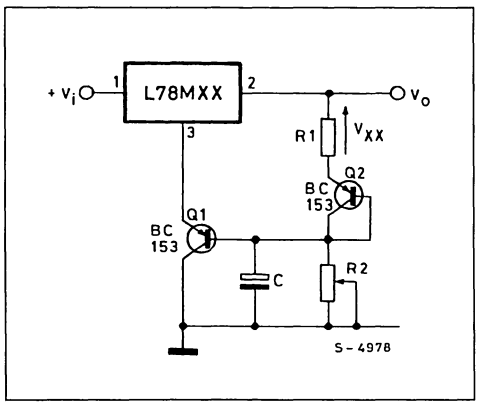
$$R = \frac{V_{I(min)} - V_{XX} - V_{DROP(max)}}{I_{O(max)} + I_{d(max)}}$$

Figure 23 : Power AM Modulator (unity voltage gain, Io ≤ 0.5).



Note : The circuit performs well up to 100KHz

Figure 24 : Adjustable Output Voltage with Temperature Compensation.



Note : Q_2 is connected as a diode in order to compensate the variation of the Q_1 V_{BE} with the temperature. C allows a slow rise-time of the V_O

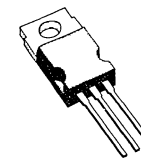
$$V_O = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + V_{BE}$$

SGS-THOMSON MICROELECTRONICS

L78M00AB SERIES

PRECISION 500mA REGULATORS

- OUTPUT CURRENT UP TO 0.5A
- OUTPUT VOLTAGES OF 5 ; 6 ; 8 ; 12 ; 15 ; 18 ; 20 ; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTORS SOA PROTECTION
- ± 2% OUTPUT VOLTAGE TOLERANCE
- GUARANTEED IN EXTENDED TEMPERATURE RANGES

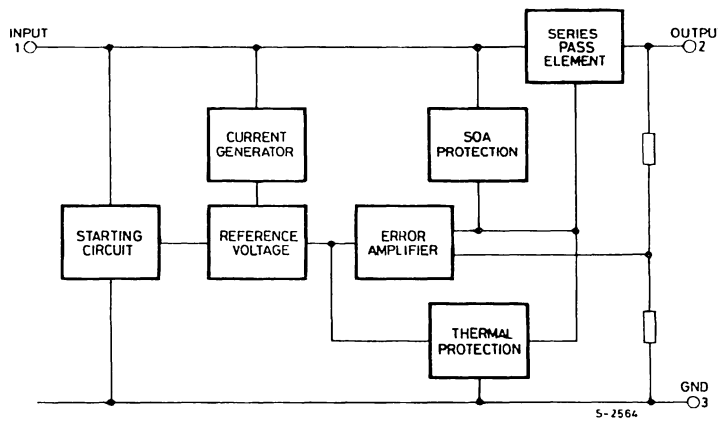


TO-220

DESCRIPTION

The L78M00AB series of three-therminal positive regulators is available in TO-220 package and with several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 0.5A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

BLOCK DIAGRAM



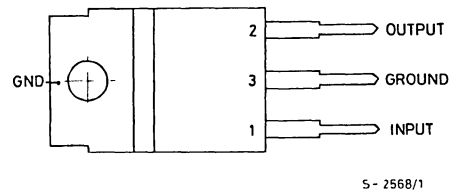
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage (for V_o = 5 to 18V) (for V_o = 20, 24V)	35 40	V V
I_o	Output Current	Internally limited	
P_{tot}	Power Dissipation	Internally limited	
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_j	Operating Junction Temperature	– 40 to 125	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	50	°C/W

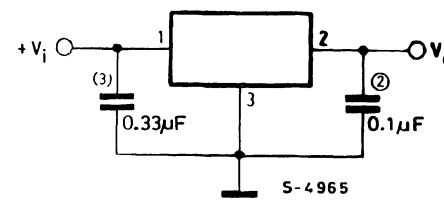
CONNECTION DIAGRAM AND ORDER CODES (top view)



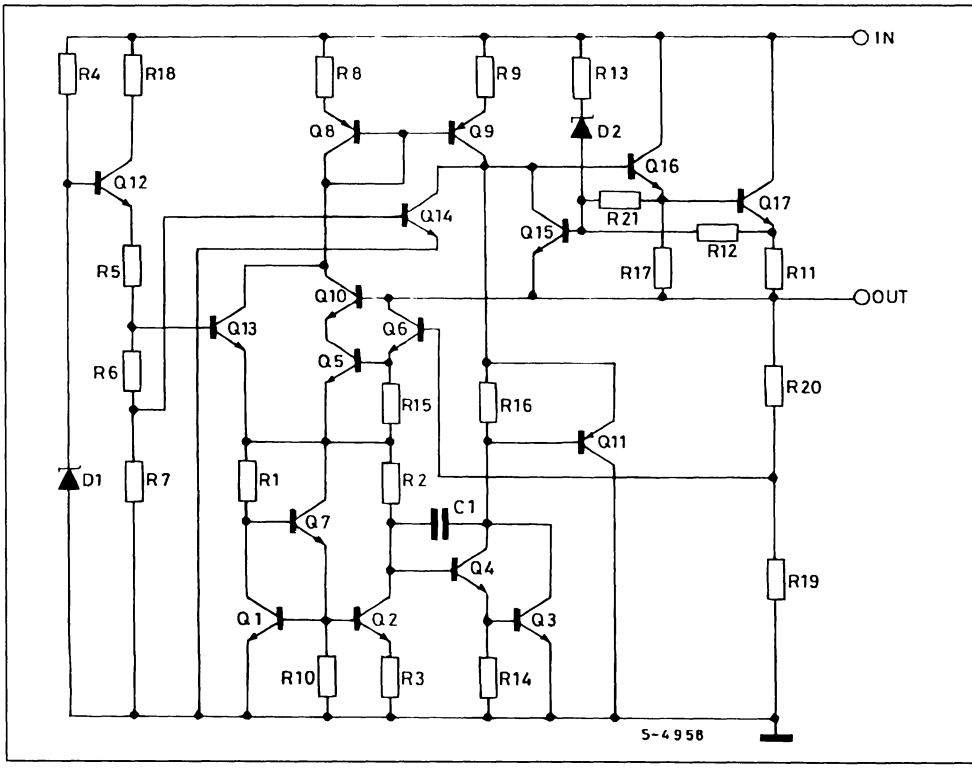
TO-220

Codes	Output Voltage
L78M05ABV	5V
L78M06ABV	6V
L78M08ABV	8V
L78M12ABV	12V
L78M15ABV	15V
L78M18ABV	18V
L78M20ABV	20V
L78M24ABV	24V

APPLICATION CIRCUIT



SCHEMATIC DIAGRAM



TEST CIRCUITS

Figure 1 : DC Parameters.

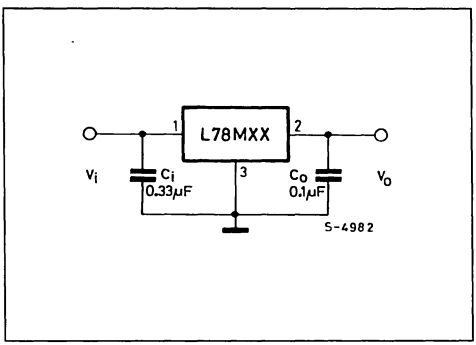


Figure 2 : Load Regulation.

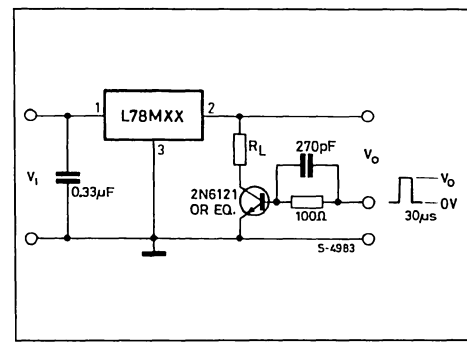
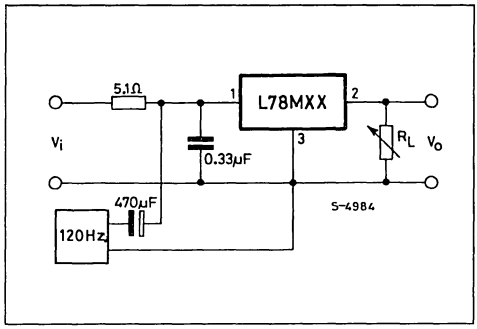


Figure 3 : Ripple Rejection.



ELECTRICAL CHARACTERISTICS L78M00AB (Refer to the test circuits, $T_j = -40$ to 125°C, I_o = 350mA unless otherwise specified, C_i = 0.33µF, C_o = 0.1µF)

Output Voltage			5			6			8			12			Unit
Input Voltage (unless otherwise specified)			10			11			14			19			
Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output Voltage	T_j = 25°C	4.9	5	5.1	5.88	6	6 12	7.84	8	8.16	11.75	12	12.25	V
		I_o = 5 to 350mA	4 8 (V_i = 7 to 20V)	5	5.2	5.75 (V_i = 8 to 21V)	6	6.3	7.7 (V_i = 10.5 to 23V)	8	8.3	11.5 (V_i = 14.5 to 27V)	12	12.5	
ΔV_o	Line Regulation	I_o = 200mA T_j = 25°C		100 (V_i = 7 to 25V)			100 (V_i = 8 to 25V)			100 (V_i = 10.5 to 25V)			100 (V_i = 14.5 to 30V)		mV
				30 (V_i = 8 to 25V)			30 (V_i = 9 to 25V)			30 (V_i = 11 to 25V)			30 (V_i = 16 to 30V)		
ΔV_o	Load Regulation	I_o = 5mA to 0.5A T_j = 25°C		100			120			160			240		mV
		I_o = 5mA to 200mA		50			60			80			120		
I_d	Quiescent Current	T_j = 25°C		6			6			6			6		mA
ΔI_d	Quiescent Current Change	I_o = 5mA to 350mA		0.5			0.5			0.5			0.5		mA
		I_o = 200mA		0 8 (V_i = 8 to 25V)			0.8 (V_i = 9 to 25V)			0 8 (V_i = 10.5 to 25V)			0.8 (V_i = 14.5 to 30V)		
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA		– 0.5			– 0 5			– 0.5			– 1.0		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25°C		40			45			52			75		µV
SVR	Supply Voltage Rejection	f = 120Hz I_o = 300mA T_j = 25°C	62 (V_i = 8 to 18V)			59 (V_i = 9 to 19V)			56 (V_i = 11 5 to 21.5V)			55 (V_i = 15 to 25V)			dB
V_d	Dropout Voltage	T_j = 25°C		2			2			2			2		V
I_{sc}	Short Circuit Current	V_i = 35V T_j = 25°C		300			270			250			240		mA
I_{scp}	Short Circ. Peak Current	T_j = 25°C		700			700			700			700		mA

ELECTRICAL CHARACTERISTICS L78M00AB (continued)

Output Voltage			15			18			20			24			Unit
Input Voltage (unless otherwise specified)			23			26			29			33			
Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output Voltage	T_j = 25°C	14.7	15	15.3	17.64	18	18.36	19.6	20	20.4	23.5	24	24.5	V
		I_o = 5 to 350mA	14.4	15	15.6 (V_i = 17.5 to 30V)	17.3	18	18.7 (V_i = 20.5 to 33V)	19.2	20	20.8 (V_i = 23 to 35V)	23	24	25 (V_i = 27 to 38V)	
ΔV_o	Line Regulation	I_o = 200mA T_j = 25°C			100 (V_i = 17.5 to 30V)			100 (V_i = 21 to 33V)			100 (V_i = 23 to 35V)			100 (V_i = 27 to 38V)	mV
					30 (V_i = 20 to 30V)			30 (V_i = 24 to 33V)			30 (V_i = 24 to 35V)			30 (V_i = 28 to 38V)	
ΔV_o	Load Regulation	I_o = 5mA to 0.5A T_j = 25°C			300			360			400			480	mV
		I_o = 5mA to 200mA			150			180			200			240	
I_d	Quiescent Current				6			6			6			6	mA
ΔI_d	Quiescent Current Change	I_o = 5mA to 350mA			0.5			0.5			0.5			0.5	mA
		I_o = 200mA			0.8 (V_i = 17.5 to 30V)			0.8 (V_i = 21 to 33V)			0.8 (V_i = 23 to 35V)			0.8 (V_i = 27 to 38V)	
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA		– 1			– 1.1			– 1.1			– 1.2		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25°C		90			100			110			170		µV
SVR	Supply Voltage Rejection	f = 120Hz I_o = 300mA T_j = 25°C	54 (V_i = 18.5 to 28.5V)			53 (V_i = 22 to 32V)			53 (V_i = 24 to 34V)			50 (V_i = 28 to 38V)			dB
V_d	Dropout Voltage	T_j = 25°C		2			2			2			2		V
I_{sc}	Short Circuit Current	V_i = 35V T_j = 25°C		240			240			240			240		mA
I_{scp}	Short Circ. Peak Current	T_j = 25°C		700			700			700			700		mA

Figure 4 : Dropout Voltage vs. Junction Temperature.

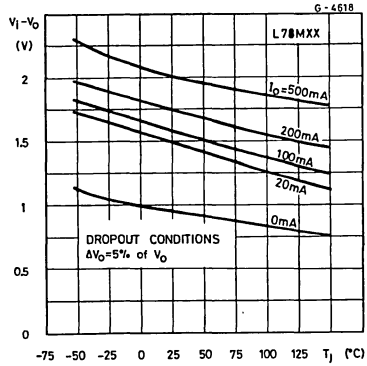


Figure 5 : Dropout Characteristics.

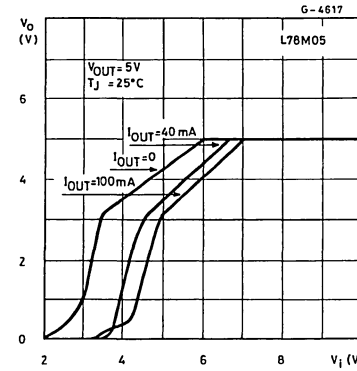


Figure 6 : Peak Output Current vs. Input-Output Differential Voltage.

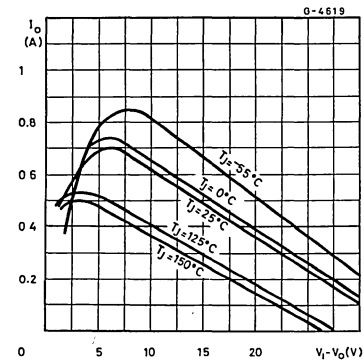


Figure 7 : Output Voltage vs. Junction Temperature.

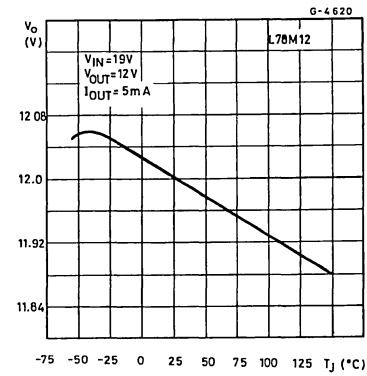


Figure 8 : Supply Voltage Rejection vs. Frequency.

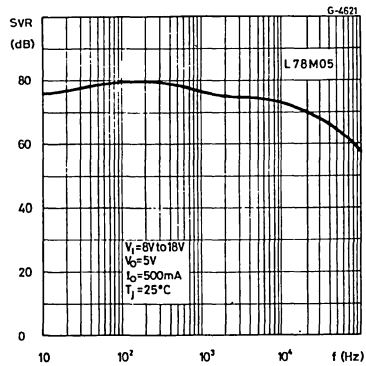


Figure 9 : Quiescent Current vs. Junction Temperature.

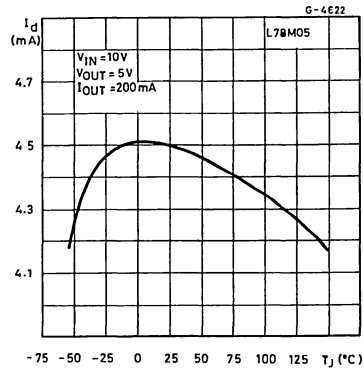


Figure 10 : Load Transient Response.

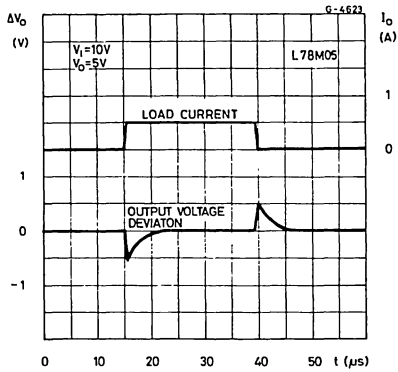


Figure 11 : Line Transient Response.

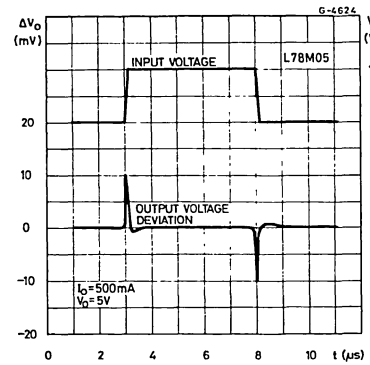
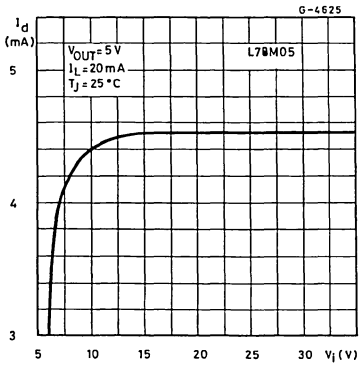


Figure 12 : Quiescent Current vs. Input Voltage.



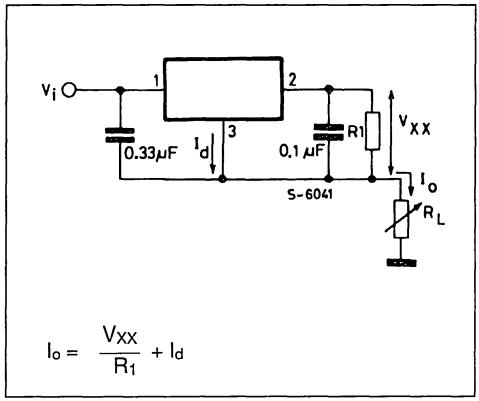
APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

The L78M00AB Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit as the voltage across the pass transistor is increased.

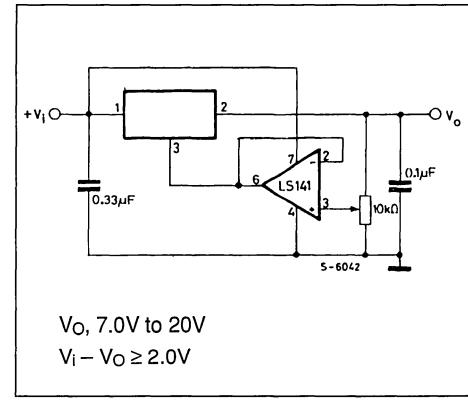
In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Figure 13 : Current Regulator.



$$I_o = \frac{V_{XX}}{R_1} + I_d$$

Figure 14 : Adjustable Output Regulator.

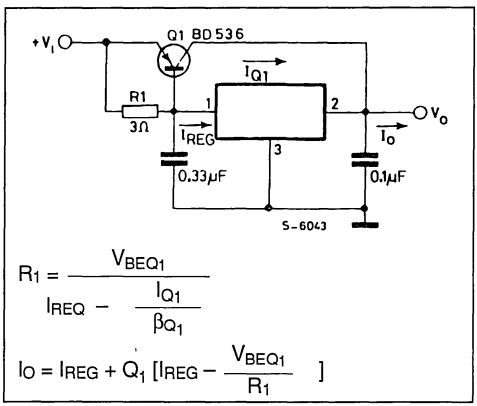


V_O, 7.0V to 20V

$V_i - V_O \geq 2.0V$

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0V greater than the regulator voltage.

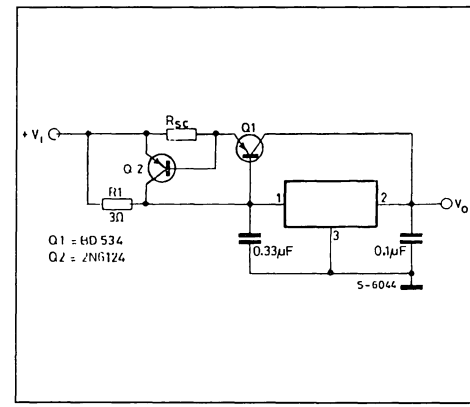
Figure 15 : Current Boost Regulator.



$$R_1 = \frac{V_{BEQ1}}{I_{REG} - \frac{I_{Q1}}{\beta_{Q1}}}$$

$$I_O = I_{REG} + Q_1 \left[I_{REG} - \frac{V_{BEQ1}}{R_1} \right]$$

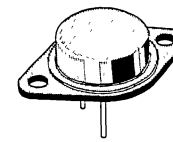
Figure 16 : Short-circuit Protection.



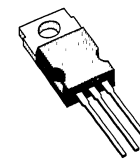
The circuit of figure 6 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a four-ampere plastic power transistor is specified.

2A POSITIVE VOLTAGE REGULATORS

- OUTPUT CURRENT TO 2A
- OUTPUT VOLTAGES OF 5 ; 7.5 ; 9 ; 10 ; 12 ; 15 ; 18 ; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION



TO-3

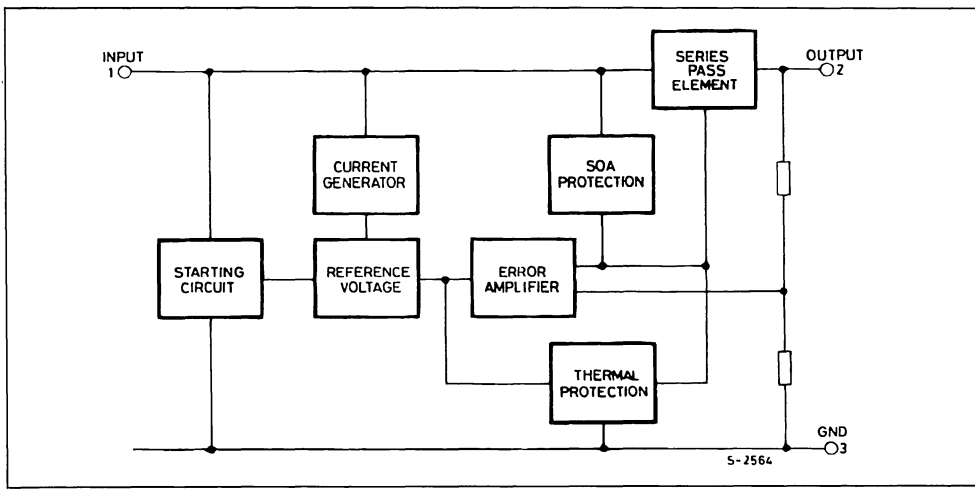


TO-220

DESCRIPTION

The L78S00 series of three-terminal positive regulators is available in TO-220 and TO-3 packages and with several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 2A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

BLOCK DIAGRAM



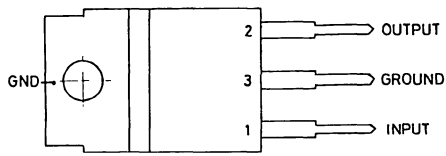
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	DC Input Voltage (for V_o = 5 to 18V) (for V_o = 24V)	35 40	V V
I_o	Output Current	Internally limited	
P_{tot}	Power Dissipation	Internally limited	
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_{op}	Operating Junction Temperature (for **L78S00**) (for **L78S00C**)	– 55 to + 150 0 to + 150	°C °C

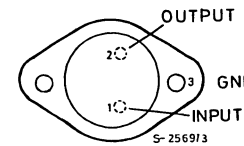
THERMAL DATA

			TO-220	TO-3	
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	4	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	50	35	°C/W

CONNECTION DIAGRAMS AND ORDERING NUMBERS (top views)



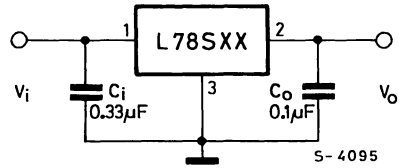
S - 2568/1



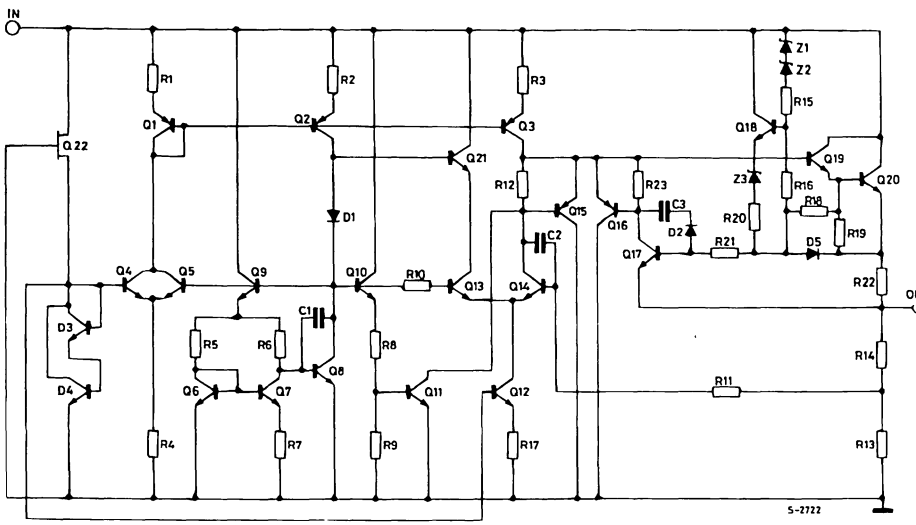
S- 2569/3

Type	TO-220	TO-3	Output Voltage
L78S05		L78S05T	5V
L78S05C	L78S05CV	L78S05CT	5V
L78S75		L78S75T	7.5V
L78S75C	L78S75CV	L78S75CT	7.5V
L78S09		L78S09T	9V
L78S09C	L78S09CV	L78S09CT	9V
L78S10		L78S10T	10V
L78S10C	L78S10CV	L78S10CT	10V
L78S12		L78S12T	12V
L78S12C	L78S12CV	L78S12CT	12V
L78S15		L78S15T	15V
L78S15C	L78S15CV	L78S15CT	15V
L78S18		L78S18T	18V
L78S18C	L78S18CV	L78S18CT	18V
L78S24		L78S24T	24V
L78S24C	L78S24CV	L78S24CT	24V

APPLICATION CIRCUIT



SCHEMATIC DIAGRAM



TEST CIRCUITS

Figure 1 : DC Parameters.

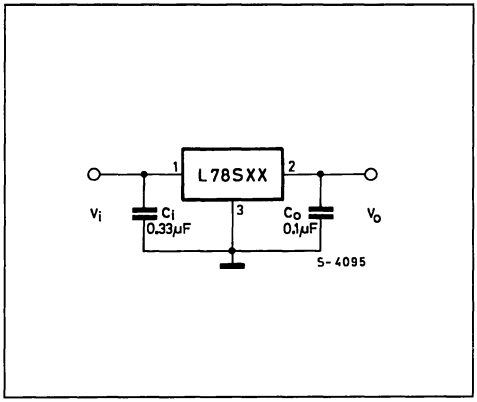


Figure 2 : Load Regulation.

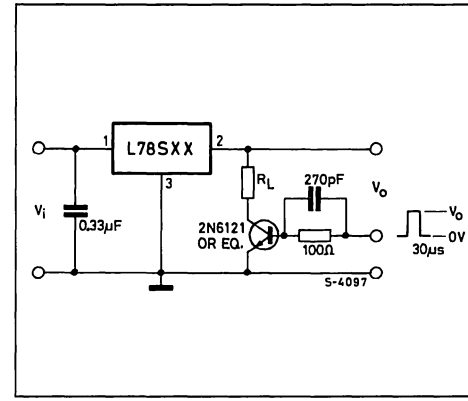
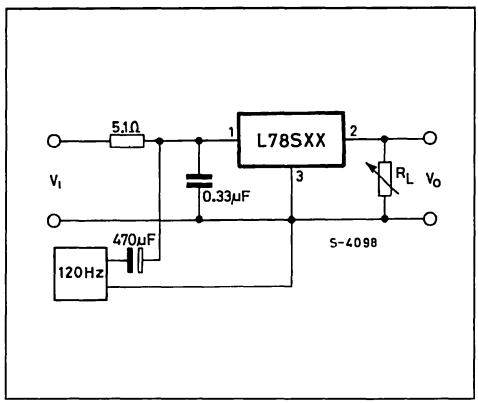


Figure 3 : Ripple Rejection.



ELECTRICAL CHARACTERISTICS L78S00

(Refer to the test circuits, T_j = 25°C, I_o = 500mA unless otherwise specified)

Output Voltage			5			7.5			9			10			Unit
Input Voltage (unless otherwise specified)			10			12.5			14			15			
Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output Voltage		4.8	5	5.2	7.15	7.5	7.9	8.65	9	9.35	9.5	10	10.5	V
		I_o = 1A	4.75	5	5.25 (V_i = 7V)	7.1	7.5	7.95 (V_i = 9.5V)	8.6	9	9.4 (V_i = 11V)	9.4	10	10.6 (V_i = 12.5V)	
ΔV_o	Line Regulation				100 (V_i = 7 to 25V)			120 (V_i = 9.5 to 25V)			130 (V_i = 11 to 25V)			200 (V_i = 12.5 to 30V)	mV
					50 (V_i = 8 to 12V)			60 (V_i = 10.5 to 20V)			65 (V_i = 11 to 20V)			100 (V_i = 14 to 22V)	
ΔV_o	Load Regulation	I_o = 20mA to 2A			100			120			130			150	mV
I_d	Quiescent Current				8			8			8			8	mA
ΔI_d	Quiescent Current Change	I_o = 20mA to 1A			0.5			0.5			0.5			0.5	mA
		I_o = 20mA			1.3 (Vi = 7 to 25V)			1.3 (V_i = 9.5 to 25V)			1.3 (V_i = 11 to 25V)			1 (V_i = 12.5 to 30V)	
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA T_j = − 55 to 150°C		− 1.1			− 0.8			− 1			− 1		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz		40			52			60			65		µV
SVR	Supply Voltage Rejection	f = 120Hz	60			54			53			53			dB
V_i	Operating Input Voltage	$I_o \leq$ 1.5A	8			10.5			12			13			V
R_o	Output Resistance	f = 1KHz		17			16			17			17		mΩ
I_{sc}	Short Circuit Current	V_i = 27V		500			500			500			500		mA
I_{scp}	Short Circ. Peak Current				4			4			4			4	A

ELECTRICAL CHARACTERISTICS L78S00 (continued)

Output Voltage			12			15			18			24			Unit
Input Voltage (unless otherwise specified)			19			23			26			33			
Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output Voltage		11.5	12	12.5	14.4	15	15.6	17.1	18	18.9	23	24	25	V
		I_o = 1A	11.4	12	12.6 (V_i = 14.5V)	14.25	15	15.75 (V_i = 17.5V)	17	18	19 (V_i = 20.5V)	22.8	24	25.2 (V_i = 27V)	
ΔV_o	Line Regulation				240 (V_i = 14.5 to 30V)			300 (V_i = 17.5 to 30V)			360 (V_i = 20.5 to 30V)			480 (V_i = 27 to 38V)	mV
					120 (V_i = 16 to 22V)			150 (V_i = 20 to 26V)			180 (V_i = 22 to 28V)			240 (V_i = 30 to 36V)	
ΔV_o	Load Regulation	I_o = 20mA to 2A			160			180			200			250	mV
I_d	Quiescent Current				8			8			8			8	mA
ΔI_d	Quiescent Current Change	I_o = 20mA to 1A			0.5			0.5			0.5			0.5	mA
		I_o = 20mA			1 (V_i = 14.5 to 30V)			1 (V_i = 17.5 to 30V)			1 (V_i = 22 to 33V)			1 (V_i = 28 to 38V)	
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA T_{amb} = 0 to 70°C		– 1			– 1			– 1			– 1.5		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz		75			90			110			170		μV
SVR	Supply Voltage Rejection	f = 120Hz	53			52			49			48			dB
V_i	Operating Input Voltage	$I_o \leq$ 1.5A	15			18			21			27			V
R_o	Output Resistance	f = 1KHz		18			19			22			23		mΩ
I_{sc}	Short Circuit Current	V_i = 27V		500			500			500			500		mA
I_{scp}	Short Circ Peak Current				4			4			4			4	A

ELECTRICAL CHARACTERISTICS L78S00C

(Refer to the test circuits, T_j = 25°C, I_o = 500mA unless otherwise specified)

Output Voltage			5			7.5			9			10			Unit
Input Voltage (unless otherwise specified)			10			12.5			14			15			
Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output Voltage		4.8	5	5.2	7.15	7.5	7.9	8.65	9	9.35	9.5	10	10.5	V
		I_o = 1A	4.75	5	5.25 (V_i = 7V)	7.1	7.5	7.95 (V_i = 9.5V)	8.6	9	9.4 (V_i = 11V)	9.4	10	10.6 (V_i = 12.5V)	
ΔV_o	Line Regulation				100 (V_i = 7 to 25V)			120 (V_i = 9.5 to 25V)			130 (V_i = 11 to 25V)			200 (V_i = 12.5 to 30V)	mV
					50 (V_i = 8 to 12V)			60 (V_i = 10.5 to 20V)			65 (V_i = 11 to 20V)			100 (V_i = 14 to 22V)	
ΔV_o	Load Regulation	I_o = 20mA to 1.5A I_o = 2A			100 80			140 100			170 100			240 150	mV
I_d	Quiescent Current				8			8			8			8	mA
ΔI_d	Quiescent Current Change	I_o = 20mA to 1A			0.5			0.5			0.5			0.5	mA
		I_o = 20mA			1.3 (V_i = 7 to 25V)			1.3 (V_i = 9.5 to 25V)			1.3 (V_i = 11 to 25V)			1.0 (V_i = 12.5 to 30V)	
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA T_{amb} = 0 to 70°C		− 1.1			− 0.8			− 1			− 1		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz		40			52			60			65		µV
SVR	Supply Voltage Rejection	f = 120Hz	54			48			47			47			dB
V_i	Operating Input Voltage	$I_o \leq$ 1.5A	8			10.5			12			13			V
R_o	Output Resistance	f = 1KHz		17			16			17			17		mΩ
I_{sc}	Short Circuit Current	V_i = 27V		500			500			500			500		mA
I_{scp}	Short Circ. Peak Current				4			4			4			4	A

ELECTRICAL CHARACTERISTICS L78S00C (continued)

Output Voltage			12			15			18			24			Unit
Input Voltage (unless otherwise specified)			19			23			26			33			
Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output Voltage		11.5	12	12.5	14.4	15	15.6	17.1	18	18.9	23	24	25	V
		I_o = 1A	11 4	12	12.6 (V_I = 14.5V)	14.25	15	15.75 (V_I = 17.5V)	17	18	19 (V_I = 20 5V)	22 8	24	25.2 (V_I = 27V)	
ΔV_o	Line Regulation				240 (V_I = 14.5 to 30V)			300 (V_I = 17.5 to 30V)			360 (V_I = 20.5 to 30V)			480 (V_I = 27 to 38V)	mV
					120 (V_I = 16 to 22V)			150 (V_I = 20 to 26V)			180 (V_I = 22 to 28V)			240 (V_I = 30 to 36V)	
ΔV_o	Load Regulation	I_o = 20mA to 1.5A			240			300			360			480	mV
		I_o = 2A			150			150			200			300	
I_d	Quiescent Current				8			8			8			8	mA
ΔI_d	Quiescent Current Change	I_o = 20mA to 1A			0.5			0.5			0.5			0.5	mA
		I_o = 20mA			1.0 (V_I = 14.5 to 30V)			1.0 (V_I = 17.5 to 30V)			1.0 (V_I = 20.5 to 30V)			1.0 (V_I = 27 to 38V)	
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA T_{amb} = 0 to 70°C		– 1			– 1			– 1			– 1.5		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz		75			90			110			170		µV
SVR	Supply Voltage Rejection	f = 120Hz	47			46			43			42			dB
V_i	Operating Input Voltage	$I_o \leq$ 1.5A	15			18			21			27			V
R_o	Output Resistance	f = 1KHz		18			19			22			28		mΩ
I_{sc}	Short Circuit Current	V_I = 27V		500			500			500			500		mA
I_{scp}	Short Circ. Peak Current				4			4			4			4	A

Figure 4 : Dropout Voltage vs. Junction Temperature.

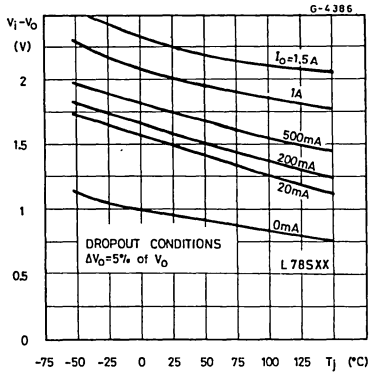


Figure 5 : Peak Output Current vs. Input/Output Differential Voltage.

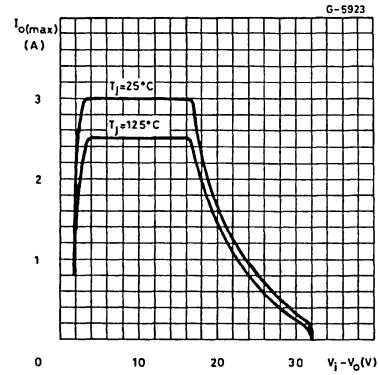


Figure 6 : Supply Voltage Rejection vs. Frequency.

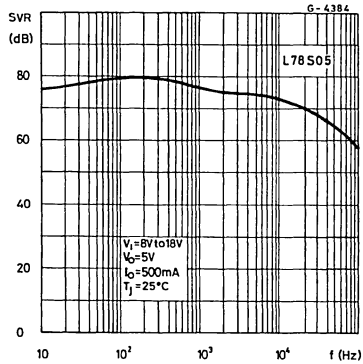


Figure 7 : Output Voltage vs. Junction Temperature.

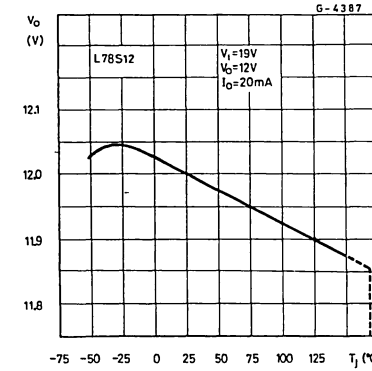


Figure 8 : Output Impedance vs. Frequency.

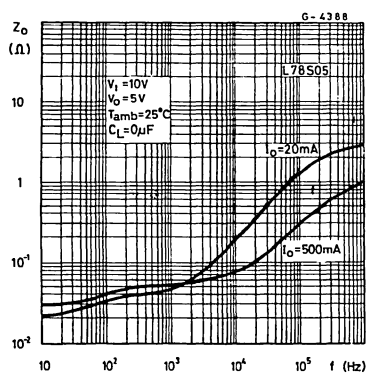


Figure 9 : Quiescent Current vs. Junction Temperature.

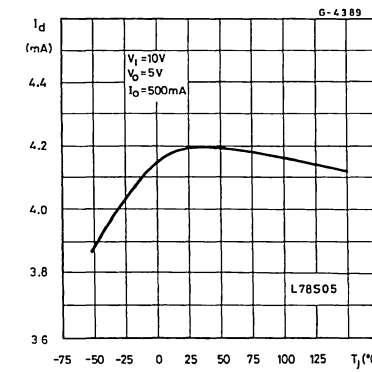


Figure 10 : Load Transient Response.

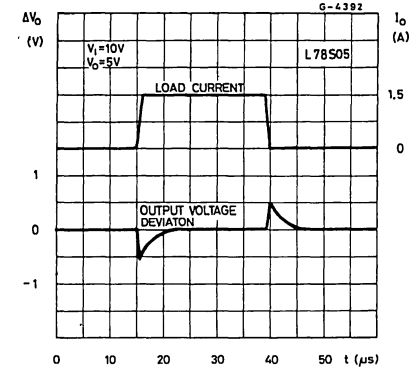


Figure 11 : Line Transient Response.

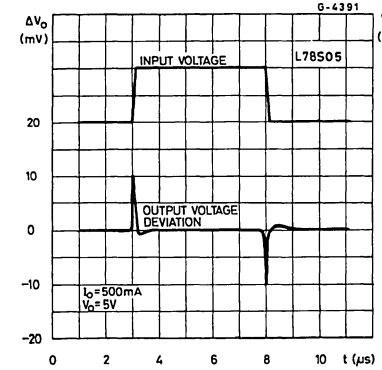


Figure 12 : Quiescent Current vs. Input Voltage.

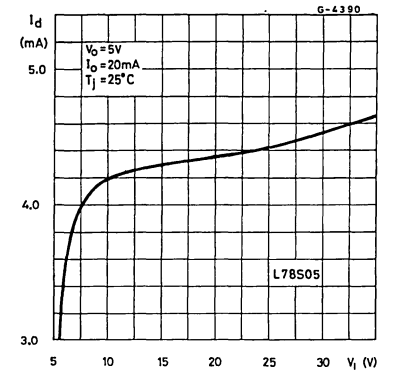


Figure 13 : Fixed Output Regulator.

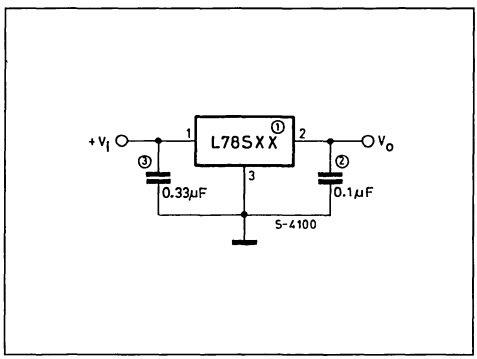
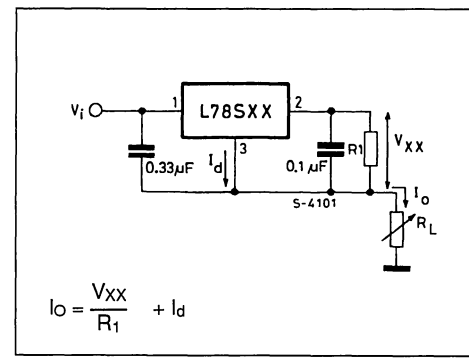
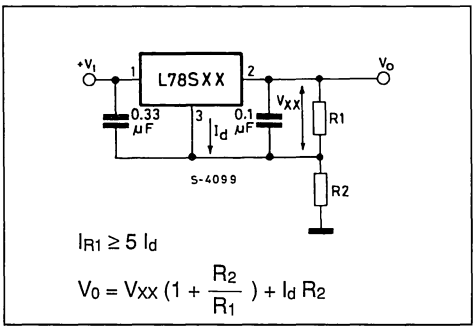


Figure 14 : Constant Current Regulator.



Notes : 1. To specify an output voltage, substitute voltage value for "XX".
2. Although no output capacitor is needed for stability, it does improve transient response.
3. Required if regulator is located an appreciable distance from power supply filter.

Figure 15 : Circuit for Increasing Output Voltage.



$I_{R1} \geq 5\ I_d$

$$V_O = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + I_d R_2$$

Figure 16 : Adjustable Output Regulator (7 to 30V).

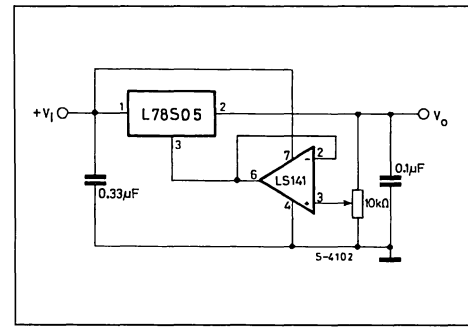
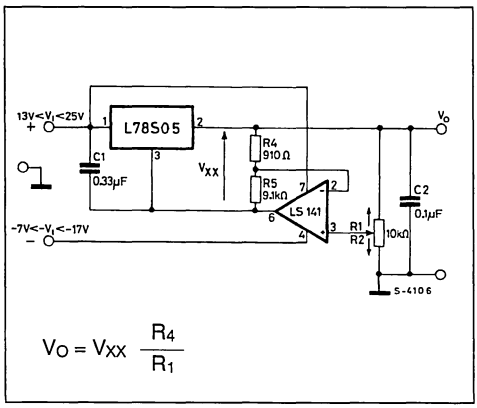
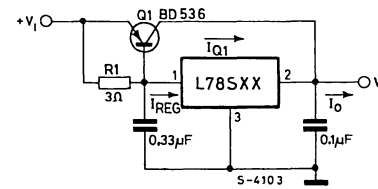


Figure 17 : 0.5 to 10V Regulator.



$$V_O = V_{XX}\frac{R_4}{R_1}$$

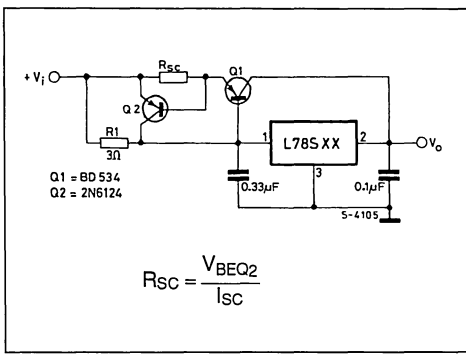
Figure 18 : High Current Voltage Regulator.



$$R_1 = \frac{V_{BEQ1}}{I_{REQ} - \frac{I_{Q1}}{\beta_{Q1}}}$$

$$I_O = I_{REG} + Q_1\left[I_{REG} - \frac{V_{BEQ1}}{R_1}\right]$$

Figure 19 : High Output Current with Short Circuit Protection.



$$R_{SC} = \frac{V_{BEQ2}}{I_{SC}}$$

Figure 20 : Tracking Voltage Regulator.

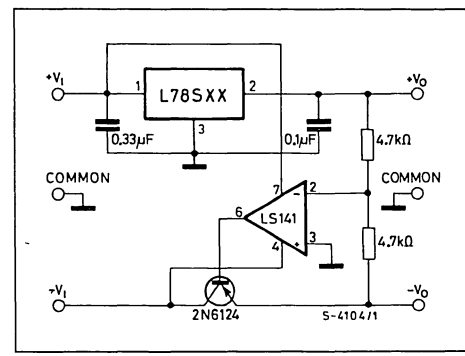
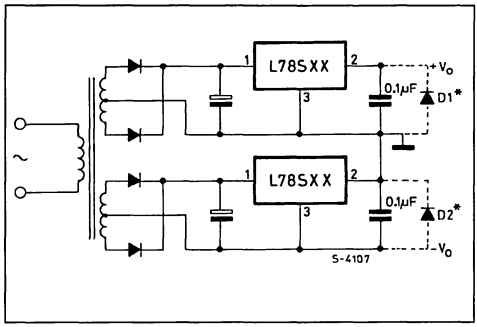


Figure 21 : Positive and Negative Regulator.



(*) D_1 and D_2 are necessary if the load is connected between + V_o and – V_o.

Figure 22 : Negative Output Voltage Circuit.

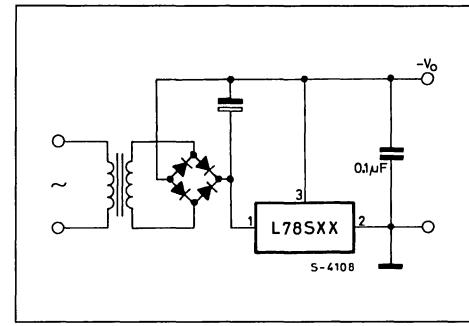


Figure 23 : Switching Regulator.

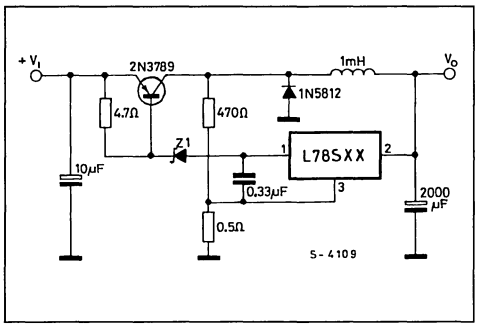
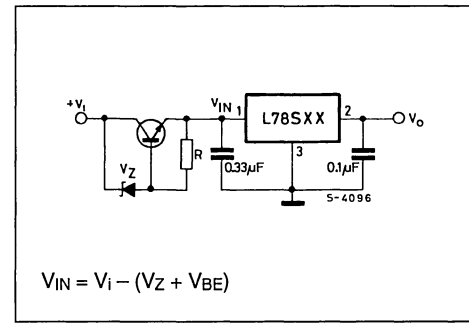
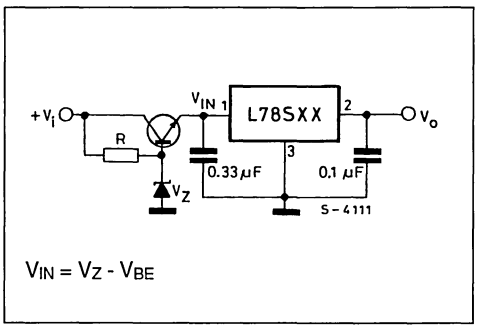


Figure 24 : High Input Voltage Circuit.



$V_{IN} = V_i - (V_Z + V_{BE})$

Figure 25 : High Input Voltage Circuit.



$V_{IN} = V_Z - V_{BE}$

Figure 26 : High Output VoltageRegulator.

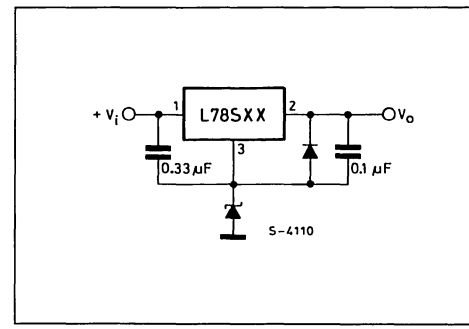
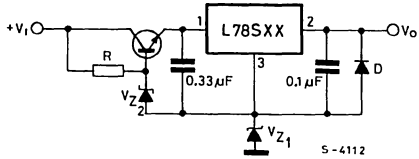
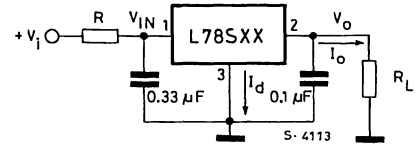


Figure 27 : High Input and Output Voltage.



$V_O = V_{XX} + V_{Z1}$

Figure 28 : Reducing Power Dissipation with Dropping Resistor.



$$R = \frac{V_{i(min)} - V_{XX} - V_{DROP(max)}}{I_{O(max)} + I_{d(max)}}$$

Figure 29 : Remote Shutdown.

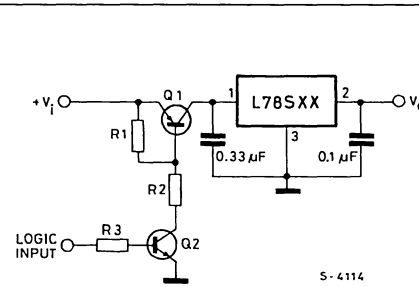
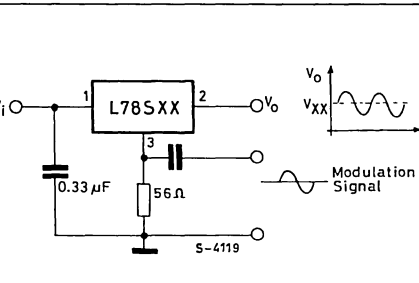
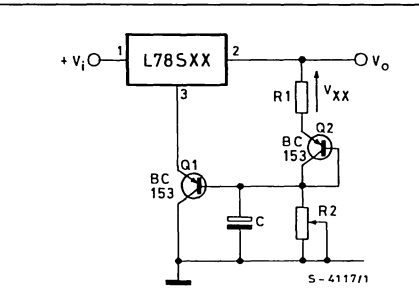


Figure 30 : Power AM Modulator (unity voltage gain, Io ≤ 1A).



Note : The circuit performs well up to 100KHz.

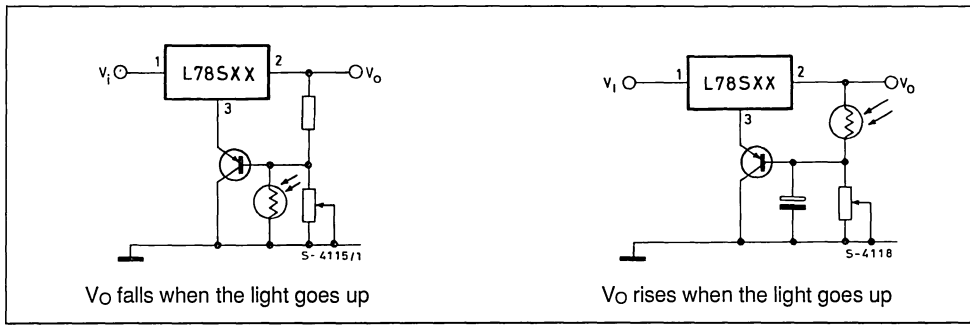
Figure 31 : Adjustable Output Voltage with Temperature Compensation.



$$V_O = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + V_{BE}$$

Note : Q_2 is connected as a diode in order to compensate the variation of the Q_1 V_{BE} with the temperature. C allows a slow rise-time of the V_O

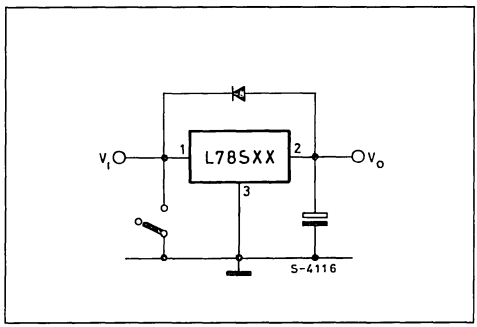
Figure 32 : Light Controllers ($V_{o\,min} = V_{xx} + V_{BE}$).



V_O falls when the light goes up

V_O rises when the light goes up

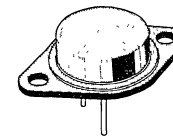
Figure 33 : Protection against Input Short-circuit with High Capacitance Loads.



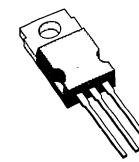
Applications with high capacitance loads and an output voltage greater than 6 volts need an external diode (see fig. 33) to protect the device against input short circuit. In this case the input voltage falls rapidly while the output voltage decreases showly. The capacitance discharges by means of the Base-Emitter junction of the series pass transistor in the regulator. If the energy is sufficiently high, the transistor may be destroyed. The external diode bypasses the current from the IC to ground.

NEGATIVE VOLTAGE REGULATORS

- OUTPUT CURRENT UP TO 1.5A
- OUTPUT VOLTAGES OF – 5 ; – 5.2 ; – 8 ; – 12 ; – 15 ; –18 ; – 20 ; – 22 ; – 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION



TO-3



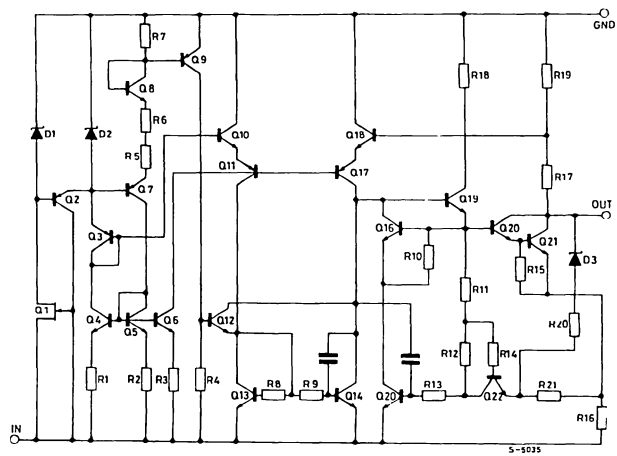
TO-220

DESCRIPTION

The L7900 series of three-terminal negative regulators is available in TO-220 and TO-3 packages and with several output voltages. They can provide local on-card regulation, eliminating the distribution problems associated with single point regulation ; furthermore, having the same voltage options as the L7800 positive standard series, they are particularly suited for split power supplies. In addition, the –5.2V is also available for ECL system.

If adeguate heatsinking is provided, the L7900 series can deliver an output current in excess of 1.5A. Although designed primarly as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

SCHEMATIC DIAGRAM



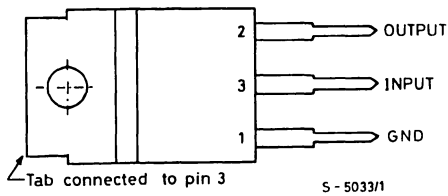
ABSOLUTE MAXIMUM RATINGS

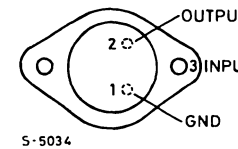
Symbol	Parameter	Value	Unit
V_i	DC Input Voltage (for V_o = – 5 to – 18V) (for V_o = – 20, – 24V)	– 35 – 40	V V
I_o	Output Current	Internally limited	
P_{tot}	Total Power Dissipation	Internally limited	
T_{op}	Operating Junction Temperature	0 to + 150	°C
T_{stg}	Storage Temperature	– 65 to + 150	°C

THERMAL DATA

			TO-220	TO-3	
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	4	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	50	35	°C/W

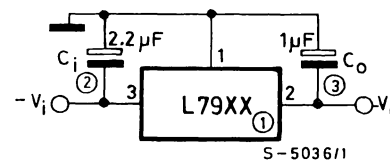
CONNECTION DIAGRAM AND ORDERING NUMBERS (top views)





Type	TO-220	TO-3	Output Voltage
L7905C	L7905CV	L7905CT	– 5V
L7952C	L7952CV	L7952CT	– 5.2V
L7908C	L7908CV	L7908CT	– 8V
L7912C	L7912CV	L7912CT	– 12V
L7915C	L7915CV	L7915CT	– 15V
L7918C	L7918CV	L7918CT	– 18V
L7920C	L7920CV	L7920CT	– 20V
L7922C	L7922CV	L7922CT	– 22V
L7924C	L7924CV	L7924CT	– 24V

APPLICATION CIRCUIT



ELECTRICAL CHARACTERISTICS FOR L7905C (refer to the test circuits, T_j = 0 to 150°C V_i = – 10V, I_o = 500mA, C_i = 2.2µF, C_o = 1µF unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C		– 4.8	– 5	– 5.2	V
V_o	Output Voltage	I_o = – 5mA to – 1A V_i = – 8 to – 20V	$P_o \leq$ 15W	– 4.75	– 5	– 5.25	V
ΔV_o*	Line Regulation	V_i = – 7 to – 25V V_i = – 8 to – 12V	T_j = 25°C T_j = 25°C			100 50	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA I_o = 250 to 750mA	T_j = 25°C T_j = 25°C			100 50	mV mV
I_d	Quiescent Current	T_j = 25°C				2	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA				0.5	mA
ΔI_d	Quiescent Current Change	V_i = – 8 to – 25V				1.3	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA			– 0.4		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz	T_j = 25°C		100		µV/V_o
SVR	Supply Voltage Rejection	ΔV_i = 10V	f = 120Hz	54	60		dB
V_d	Dropout Voltage	I_o = 1A ΔV_o = 100mV	T_j = 25°C		2		V
I_{sc}	Short Circuit Current				2.1		A
I_{scp}	Short Circuit Peak Current	T_j = 25°C			2.5		A

ELECTRICAL CHARACTERISTICS FOR L7952C (refer to the test circuits, T_j = 0 to 150°C V_i = – 10V, I_o = 500mA, C_i = 2.2µF, C_o = 1µF unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C		– 5	– 5.2	– 5.4	V
V_o	Output Voltage	I_o = – 5mA to – 1A V_i = – 9 to – 21V	$P_o \leq$ 15W	– 4.95	– 5.2	– 5.45	V
ΔV_o*	Line Regulation	V_i = – 8 to – 25V V_i = – 9 to – 13V	T_j = 25°C T_j = 25°C			105 52	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA I_o = 250 to 750mA	T_j = 25°C T_j = 25°C			105 52	mV mV
I_d	Quiescent Current	T_j = 25°C				2	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA				0.5	mA
ΔI_d	Quiescent Current Change	V_i = – 9 to – 25V				1.3	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA			– 0.5		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz	T_j = 25°C		125		µV/V_o
SVR	Supply Voltage Rejection	ΔV_i = 10V	f = 120Hz	54	60		dB
V_d	Dropout Voltage	I_o = 1A ΔV_o = 100mV	T_j = 25°C		1.8		V
I_{sc}	Short Circuit Current				2		A
I_{scp}	Short Circuit Peak Current	T_j = 25°C			2.5		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7908C (refer to the test circuits, T_j = 0 to 150°C V_i = – 14V, I_o = 500mA, C_i = 2.2µF, C_o = 1µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C	– 7.7	– 8	– 8.3	V
V_o	Output Voltage	I_o = – 5mA to – 1A $P_o \leq$ 15W V_i = – 11.5 to – 23V	– 7.6	– 8	– 8.4	V
ΔV_o*	Line Regulation	V_i = – 10.5 to – 25V T_j = 25°C V_i = – 11 to – 17V T_j = 25°C			160 80	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA T_j = 25°C I_o = 250 to 750mA T_j = 25°C			160 80	mV mV
I_d	Quiescent Current	T_j = 25°C			2	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = – 11.5 to – 25V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA		– 0.6		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25°C		175		µV/V_o
SVR	Supply Voltage Rejection	ΔV_i = 10V f = 120Hz	54	60		dB
V_d	Dropout Voltage	I_o = 1A T_j = 25°C ΔV_o = 100mV		1.1		V
I_{sc}	Short Circuit Current			1.5		A
I_{scp}	Short Circuit Peak Current	T_j = 25°C		2.5		A

ELECTRICAL CHARACTERISTICS FOR L7912C (refer to the test circuits, T_j = 0 to 150°C V_i = – 19V, I_o = 500mA, C_i = 2.2µF, C_o = 1µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C	– 11.5	– 12	– 12.5	V
V_o	Output Voltage	I_o = – 5mA to – 1A $P_o \leq$ 15W V_i = – 5.5 to – 27V	– 11.4	– 12	– 12.6	V
ΔV_o*	Line Regulation	V_i = – 14.5 to – 30V T_j = 25°C V_i = – 16 to – 22V T_j = 25°C			240 120	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA T_j = 25°C I_o = 250 to 750mA T_j = 25°C			240 120	mV mV
I_d	Quiescent Current	T_j = 25°C			3	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = – 15 to – 30V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA		– 0.8		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25°C		200		µV/V_o
SVR	Supply Voltage Rejection	ΔV_i = 10V f = 120Hz	54	60		dB
V_d	Dropout Voltage	I_o = 1A T_j = 25°C ΔV_o = 100mV		1.1		V
I_{sc}	Short Circuit Current			1.5		A
I_{scp}	Short Circuit Peak Current	T_j = 25°C		2.5		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7915C (refer to the test circuits, T_j = 0 to 150°C V_i = – 23V, I_o = 500mA, C_i = 2.2µF, C_o = 1µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C	– 14.4	– 15	– 15.6	V
V_o	Output Voltage	I_o = – 5mA to – 1A $P_o \leq$ 15W V_i = – 18.5 to – 30V	– 14.3	– 15	– 15.7	V
ΔV_o*	Line Regulation	V_i = – 17.5 to – 30V T_j = 25°C V_i = – 20 to – 26V T_j = 25°C			300 150	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA T_j = 25°C I_o = 250 to 750mA T_j = 25°C			300 150	mV mV
I_d	Quiescent Current	T_j = 25°C			3	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = – 18.5 to – 30V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA		– 0.9		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25°C		250		µV/V_o
SVR	Supply Voltage Rejection	ΔV_i = 10V f = 120Hz	54	60		dB
V_d	Dropout Voltage	I_o = 1A T_j = 25°C ΔV_o = 100mV		1.1		V
I_{sc}	Short Circuit Current			1.3		A
I_{scp}	Short Circuit Peak Current	T_j = 25°C		2.2		A

ELECTRICAL CHARACTERISTICS FOR L7918C (refer to the test circuits, T_j = 0 to 150°C V_i = – 27V, I_o = 500mA, C_i = 2.2µF, C_o = 1µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C	– 17.3	– 18	– 18.7	V
V_o	Output Voltage	I_o = – 5mA to – 1A $P_o \leq$ 15W V_i = – 22 to – 33V	– 17.1	– 18	– 18.9	V
ΔV_o*	Line Regulation	V_i = – 21 to – 33V T_j = 25°C V_i = – 24 to – 30V T_j = 25°C			360 180	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA T_j = 25°C I_o = 250 to 750mA T_j = 25°C			360 180	mV mV
I_d	Quiescent Current	T_j = 25°C			3	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = – 22 to – 33V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA		– 1		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25°C		300		µV/V_o
SVR	Supply Voltage Rejection	ΔV_i = 10V f = 120Hz	54	60		dB
V_d	Dropout Voltage	I_o = 1A T_j = 25°C ΔV_o = 100mV		1.1		V
I_{sc}	Short Circuit Current			1.1		A
I_{scp}	Short Circuit Peak Current	T_j = 25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7920C (refer to the test circuits, T_j = 0 to 150°C V_i = – 29V, I_o = 500mA, C_i = 2.2µF, C_o = 1µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C	– 19.2	– 20	– 20.8	V
V_o	Output Voltage	I_o = – 5mA to – 1A $P_o \leq$ 15W V_i = – 24 to – 35V	– 19	– 20	– 21	V
ΔV_o*	Line Regulation	V_i = – 23 to – 35V T_j = 25°C V_i = – 26 to – 32V T_j = 25°C			400 200	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA T_j = 25°C I_o = 250 to 750mA T_j = 25°C			400 200	mV mV
I_d	Quiescent Current	T_j = 25°C			3	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = – 24 to – 35V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA		– 1.1		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25°C		350		µV/V_o
SVR	Supply Voltage Rejection	ΔV_i = 10V f = 120Hz	54	60		dB
V_d	Dropout Voltage	I_o = 1A T_j = 25°C ΔV_o = 100mV		1.1		V
I_{sc}	Short Circuit Current			0.9		A
I_{scp}	Short Circuit Peak Current	T_j = 25°C		2.2		A

ELECTRICAL CHARACTERISTICS FOR L7922C (refer to the test circuits, T_j = 0 to 150°C V_i = – 31V, I_o = 500mA, C_i = 2.2µF, C_o = 1µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C	– 21.1	– 22	– 22.9	V
V_o	Output Voltage	I_o = – 5mA to – 1A $P_o \leq$ 15W V_i = – 26 to – 37V	– 20.9	– 22	– 23.1	V
ΔV_o*	Line Regulation	V_i = – 25 to – 37V T_j = 25°C V_i = – 28 to – 34V T_j = 25°C			440 220	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA T_j = 25°C I_o = 250 to 750mA T_j = 25°C			440 220	mV mV
I_d	Quiescent Current	T_j = 25°C			3	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = – 26 to – 37V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA		– 1.1		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25°C		375		µV/V_o
SVR	Supply Voltage Rejection	ΔV_i = 10V f = 120Hz	54	60		dB
V_d	Dropout Voltage	I_o = 1A T_j = 25°C ΔV_o = 100mV		1.1		V
I_{sc}	Short Circuit Current			1.1		A
I_{scp}	Short Circuit Peak Current	T_j = 25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

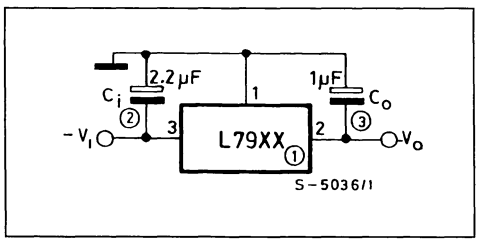
ELECTRICAL CHARACTERISTICS FOR L7924C (refer to the test circuits, T_j = 0 to 150°C V_i = – 33V, I_o = 500mA, C_i = 2.2µF, C_o = 1µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C	– 23	– 24	– 25	V
V_o	Output Voltage	I_o = – 5mA to – 1A $P_o \leq$ 15W V_i = – 27 to – 38V	– 22.8	– 24	– 25.2	V
ΔV_o*	Line Regulation	V_i = – 27 to – 38V T_j = 25°C V_i = – 30 to – 36V T_j = 25°C			480 240	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA T_j = 25°C I_o = 250 to 750mA T_j = 25°C			480 240	mV mV
I_d	Quiescent Current	T_j = 25°C			3	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = – 27 to – 38V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA		– 1		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25°C		400		µV/V_o
SVR	Supply Voltage Rejection	ΔV_i = 10V f = 120Hz	54	60		dB
V_d	Dropout Voltage	I_o = 1A T_j = 25°C ΔV_o = 100mV		1.1		V
I_{sc}	Short Circuit Current			1.1		A
I_{scp}	Short Circuit Peak Current	T_j = 25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

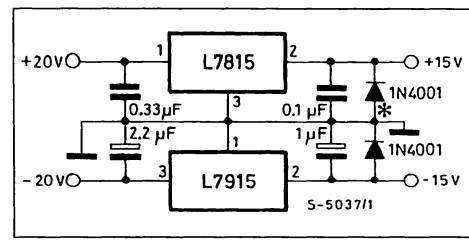
APPLICATION INFORMATION

Figure 1 : Fixed Output Regulator.



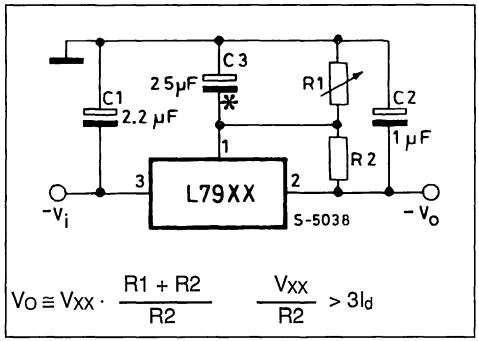
Notes : 1. To specify an output voltage, substitute voltage value for "XX".
2. Required for stability. For value given, capacitor must be solid tantalum. If aluminium electrolitics are used, at least ten times value should be selected. C_i is required if regulator is located an appreciable distance from power supply filter.
3. To improve transient response. If large capacitors are used, a high current diode from input to output (1N4001 or similar) should be introduced to protect the device from momentary input short circuit.

Figure 2 : Split Power Supply (± 15V/1A).



* Against potential latch-up problems.

Figure 3 : Circuit for Increasing Output Voltage.



* C3 Optional for improved transient response and ripple rejection.

Figure 4 : High Current Negative Regulator (– 5V/4A with 5A current limiting).

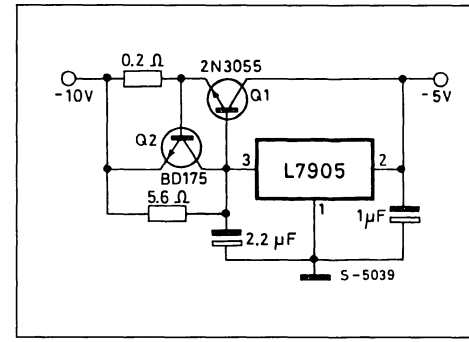
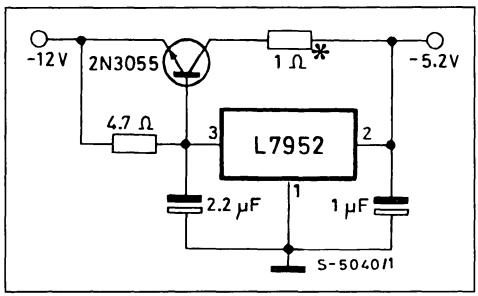


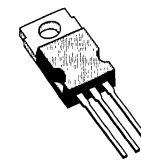
Figure 5 : Typical ECL System Power Supply (– 5.2V/4A).



* Optional dropping resistor to reduce the power dissipated in the boost transistor.

± 2% NEGATIVE VOLTAGE REGULATORS

- OUTPUT CURRENT UP TO 1.5A
- OUTPUT VOLTAGES OF – 5 ; – 5.2 ; – 8 ; –12 ; –15 ; – 18 ; – 20 ; – 22 ; – 24V
- THERMAL CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION



TO-220

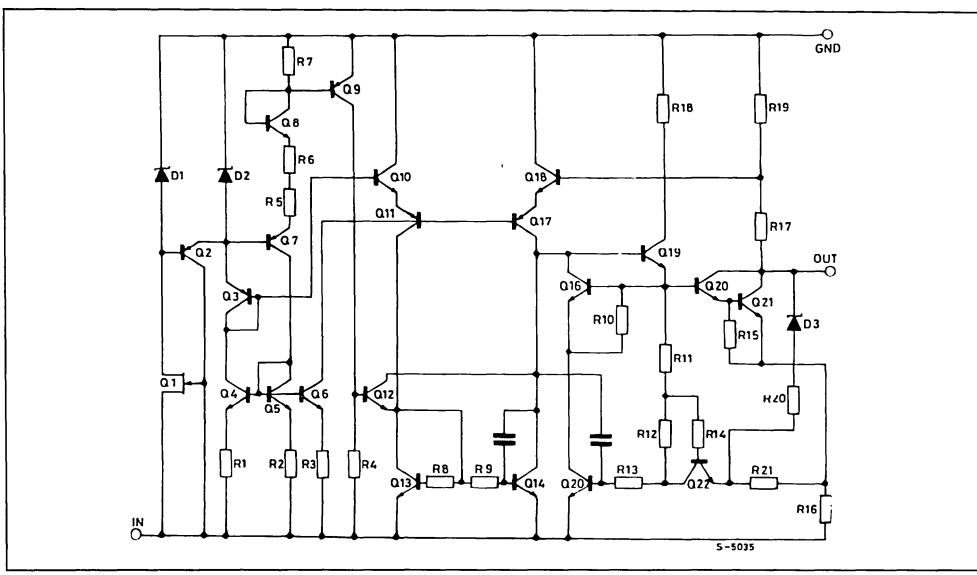
DESCRIPTION

The L7900AC series of three-terminal negative regulators is available in TO-220 package and with several output voltage. They can provide local on-card regulation, eliminating the distribution problems associated with single point regulation ; furthermore, having the same voltage options as the L7800 positive standard series, they are particularly suited for split power supplies.

In addition, the -5.2V is also available for ECL system.

If adeguate heatsinking is provided, the L7900AC series can deliver an output current in excess of 1.5A. Although designed primarly as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

SCHEMATIC DIAGRAM



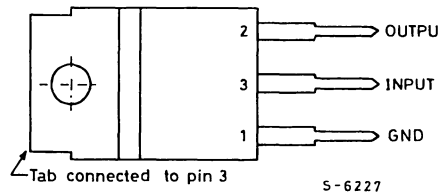
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage (for V_o = – 5 to – 18V) (for V_o = – 20, – 24V)	– 35 – 40	V V
I_o	Output Current	Internally limited	
P_{tot}	Total Power Dissipation	Internally limited	
T_{op}	Operating Junction Temperature	0 to + 150	°C
T_{stg}	Storage Temperature	– 65 to + 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	50	°C/W

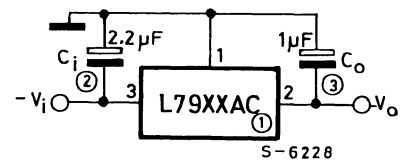
CONNECTION DIAGRAM AND ORDERING NUMBERS (top views)



TO-220

OrderingNumbers	OutputVoltage
L7905ACV	– 5V
L7952ACV	– 5.2V
L7908ACV	– 8V
L7912ACV	– 12V
L7915ACV	– 15V
L7918ACV	– 18V
L7920ACV	– 20V
L7922ACV	– 22V
L7924ACV	– 24V

APPLICATION CIRCUIT



ELECTRICAL CHARACTERISTICS FOR L7905AC (refer to the test circuits, T_j = 0 to 150°C V_i = – 10V, I_o = 500mA, C_i = 2.2µF, C_o = 1µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C	– 4.9	– 5	– 5.1	V
V_o	Output Voltage	I_o = – 5mA to – 1A $P_o \leq$ 15W V_i = – 8 to – 20V	– 4.8	– 5	– 5.2	V
ΔV_o*	Line Regulation	V_i = – 7 to – 25V T_j = 25°C V_i = – 8 to – 12V T_j = 25°C			100 50	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA T_j = 25°C I_o = 250 to 750mA T_j = 25°C			100 50	mV mV
I_d	Quiescent Current	T_j = 25°C			2	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = – 8 to – 25V			1.3	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA		– 0.4		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25°C		100		µV/V_o
SVR	Supply Voltage Rejection	ΔV_i = 10V f = 120Hz	54	60		dB
V_d	Dropout Voltage	I_o = 1A T_j = 25°C ΔV_o = 100mV		2		V
I_{sc}	Short Circuit Current			2.1		A
I_{scp}	Short Circuit Peak Current	T_j = 25°C		2.5		A

ELECTRICAL CHARACTERISTICS FOR L7952AC (refer to the test circuits, T_j = 0 to 150°C V_i = – 10V, I_o = 500mA, C_i = 2.2µF, C_o = 1µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C	– 5.1	– 5.2	– 5.3	V
V_o	Output Voltage	I_o = – 5mA to – 1A $P_o \leq$ 15W V_i = – 9 to – 21V	– 5	– 5.2	– 5.4	V
ΔV_o*	Line Regulation	V_i = – 8 to – 25V T_j = 25°C V_i = – 9 to – 13V T_j = 25°C			105 52	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA T_j = 25°C I_o = 250 to 750mA T_j = 25°C			105 52	mV mV
I_d	Quiescent Current	T_j = 25°C			2	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = – 9 to – 25V			1.3	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA		– 0.5		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25°C		125		µV/V_o
SVR	Supply Voltage Rejection	ΔV_i = 10V f = 120Hz	54	60		dB
V_d	Dropout Voltage	I_o = 1A T_j = 25°C ΔV_o = 100mV		1.8		V
I_{sc}	Short Circuit Current			2		A
I_{scp}	Short Circuit Peak Current	T_j = 25°C		2.5		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7908AC (refer to the test circuits, T_j = 0 to 150°C V_i = – 14V, I_o = 500mA, C_i = 2.2µF, C_o = 1µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C	– 7.84	– 8	– 8.16	V
V_o	Output Voltage	I_o = – 5mA to – 1A $P_o \leq$ 15W V_i = – 11.5 to – 23V	– 7.7	– 8	– 8.3	V
ΔV_o*	Line Regulation	V_i = – 10.5 to – 25V T_j = 25°C V_i = – 11 to – 17V T_j = 25°C			160 80	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA T_j = 25°C I_o = 250 to 750mA T_j = 25°C			160 80	mV mV
I_d	Quiescent Current	T_j = 25°C			2	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = – 11.5 to – 25V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA		– 0.6		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25°C		175		µV/V_o
SVR	Supply Voltage Rejection	ΔV_i = 10V f = 120Hz	54	60		dB
V_d	Dropout Voltage	I_o = 1A T_j = 25°C ΔV_o = 100mV		1.1		V
I_{sc}	Short Circuit Current			1.5		A
I_{scp}	Short Circuit Peak Current	T_j = 25°C		2.5		A

ELECTRICAL CHARACTERISTICS FOR L7912AC (refer to the test circuits, T_j = 0 to 150°C V_i = – 19V, I_o = 500mA, C_i = 2.2µF, C_o = 1µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C	– 11.75	– 12	– 12.75	V
V_o	Output Voltage	I_o = – 5mA to – 1A $P_o \leq$ 15W V_i = – 5.5 to – 27V	– 11.5	– 12	– 12.5	V
ΔV_o*	Line Regulation	V_i = – 14.5 to – 30V T_j = 25°C V_i = – 16 to – 22V T_j = 25°C			240 120	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA T_j = 25°C I_o = 250 to 750mA T_j = 25°C			240 120	mV mV
I_d	Quiescent Current	T_j = 25°C			3	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = – 15 to – 30V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA		– 0.8		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25°C		200		µV/V_o
SVR	Supply Voltage Rejection	ΔV_i = 10V f = 120Hz	54	60		dB
V_d	Dropout Voltage	I_o = 1A T_j = 25°C ΔV_o = 100mV		1.1		V
I_{sc}	Short Circuit Current			1.5		A
I_{scp}	Short Circuit Peak Current	T_j = 25°C		2.5		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7915AC (refer to the test circuits, T_j = 0 to 150°C V_i = – 23V, I_o = 500mA, C_i = 2.2µF, C_o = 1µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C	– 14.7	– 15	– 15.3	V
V_o	Output Voltage	I_o = – 5mA to – 1A $P_o \leq$ 15W V_i = – 18.5 to – 30V	– 14.4	– 15	– 15.6	V
ΔV_o*	Line Regulation	V_i = – 17.5 to – 30V T_j = 25°C V_i = – 20 to – 26V T_j = 25°C			300 150	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA T_j = 25°C I_o = 250 to 750mA T_j = 25°C			300 150	mV mV
I_d	Quiescent Current	T_j = 25°C			3	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = – 18.5 to – 30V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA		– 0.9		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25°C		250		µV/V_o
SVR	Supply Voltage Rejection	ΔV_i = 10V f = 120Hz	54	60		dB
V_d	Dropout Voltage	I_o = 1A T_j = 25°C ΔV_o = 100mV		1.1		V
I_{sc}	Short Circuit Current			1.3		A
I_{scp}	Short Circuit Peak Current	T_j = 25°C		2.2		A

ELECTRICAL CHARACTERISTICS FOR L7918AC (refer to the test circuits, T_j = 0 to 150°C V_i = – 27V, I_o = 500mA, C_i = 2.2µF, C_o = 1µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C	– 17.64	– 18	– 18.36	V
V_o	Output Voltage	I_o = – 5mA to – 1A $P_o \leq$ 15W V_i = – 22 to – 33V	– 17.3	– 18	– 18.7	V
ΔV_o*	Line Regulation	V_i = – 21 to – 33V T_j = 25°C V_i = – 24 to – 30V T_j = 25°C			360 180	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA T_j = 25°C I_o = 250 to 750mA T_j = 25°C			360 180	mV mV
I_d	Quiescent Current	T_j = 25°C			3	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = – 22 to – 33V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA		– 1		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25°C		300		µV/V_o
SVR	Supply Voltage Rejection	ΔV_i = 10V f = 120Hz	54	60		dB
V_d	Dropout Voltage	I_o = 1A T_j = 25°C ΔV_o = 100mV		1.1		V
I_{sc}	Short Circuit Current			1.1		A
I_{scp}	Short Circuit Peak Current	T_j = 25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7920AC (refer to the test circuits, T_j = 0 to 150°C V_i = – 29V, I_o = 500mA, C_i = 2.2µF, C_o = 1µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C	– 19.6	– 20	– 20.4	V
V_o	Output Voltage	I_o = – 5mA to – 1A $P_o \leq$ 15W V_i = – 24 to – 35V	– 19.2	– 20	– 20.8	V
ΔV_o*	Line Regulation	V_i = – 23 to – 35V T_j = 25°C V_i = – 26 to – 32V T_j = 25°C			400 200	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA T_j = 25°C I_o = 250 to 750mA T_j = 25°C			400 200	mV mV
I_d	Quiescent Current	T_j = 25°C			3	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = – 24 to – 35V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA		– 1.1		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25°C		350		µV/V_o
SVR	Supply Voltage Rejection	ΔV_i = 10V f = 120Hz	54	60		dB
V_d	Dropout Voltage	I_o = 1A T_j = 25°C ΔV_o = 100mV		1.1		V
I_{sc}	Short Circuit Current			0.9		A
I_{scp}	Short Circuit Peak Current	T_j = 25°C		2.2		A

ELECTRICAL CHARACTERISTICS FOR L7922AC (refer to the test circuits, T_j = 0 to 150°C V_i = – 31V, I_o = 500mA, C_i = 2.2µF, C_o = 1µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C	– 21.5	– 22	– 22.5	V
V_o	Output Voltage	I_o = – 5mA to – 1A $P_o \leq$ 15W V_i = – 26 to – 37V	– 21.1	– 22	– 22.9	V
ΔV_o*	Line Regulation	V_i = – 25 to – 37V T_j = 25°C V_i = – 28 to – 34V T_j = 25°C			440 220	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA T_j = 25°C I_o = 250 to 750mA T_j = 25°C			440 220	mV mV
I_d	Quiescent Current	T_j = 25°C			3	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = – 26 to – 37V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA		– 1.1		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25°C		375		µV/V_o
SVR	Supply Voltage Rejection	ΔV_i = 10V f = 120Hz	54	60		dB
V_d	Dropout Voltage	I_o = 1A T_j = 25°C ΔV_o = 100mV		1.1		V
I_{sc}	Short Circuit Current			1.1		A
I_{scp}	Short Circuit Peak Current	T_j = 25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

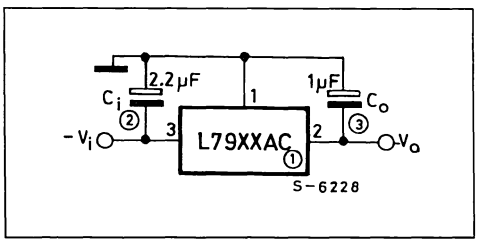
ELECTRICAL CHARACTERISTICS FOR L7924AC (refer to the test circuits, T_j = 0 to 150°C V_i = – 33V, I_o = 500mA, C_i = 2.2µF, C_o = 1µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C	– 23.5	– 24	– 24.5	V
V_o	Output Voltage	I_o = – 5mA to – 1A $P_o \leq$ 15W V_i = – 27 to – 38V	– 23	– 24	– 25	V
ΔV_o*	Line Regulation	V_i = – 27 to – 38V T_j = 25°C V_i = – 30 to – 36V T_j = 25°C			480 240	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500mA T_j = 25°C I_o = 250 to 750mA T_j = 25°C			480 240	mV mV
I_d	Quiescent Current	T_j = 25°C			3	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = – 27 to – 38V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5mA		– 1		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25°C		400		µV/V_o
SVR	Supply Voltage Rejection	ΔV_i = 10V f = 120Hz	54	60		dB
V_d	Dropout Voltage	I_o = 1A T_j = 25°C ΔV_o = 100mV		1.1		V
I_{sc}	Short Circuit Current			1.1		A
I_{scp}	Short Circuit Peak Current	T_j = 25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

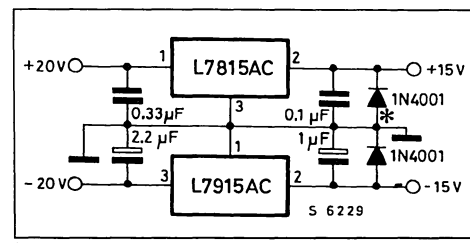
APPLICATION INFORMATION

Figure 1 : Fixed Output Regulator.



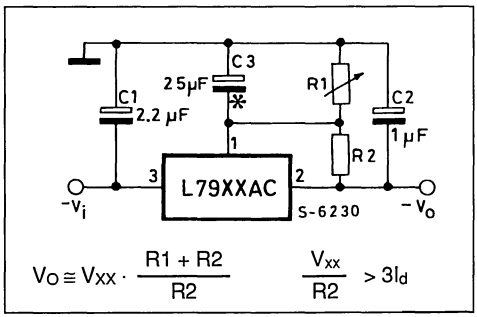
Notes : 1. To specify an output voltage, substitute voltage value for "XX".
2. Required for stability. For value given, capacitor must be solid tantalum. If aluminium electrolitics are used, at least ten times value shown should be selected, C_i is required if regulator is located an appreciable distance from power supply filter.
3. To improve transient response. If large capacitors are used, a high current diode from input to output (1N4001 or similar) should be introduced to protect the device from momentary input short circuit.

Figure 2 : Split Power Supply (± 15V/1A).



* Against potential latch-up problems.

Figure 3 : Circuit for Increasing Output Voltage.



* C3 optional for improved transient response and ripple rejection.

Figure 4 : High Current Negative Regulator (– 5V/4A with 5A current limiting).

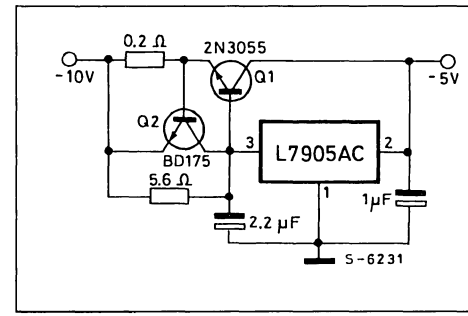
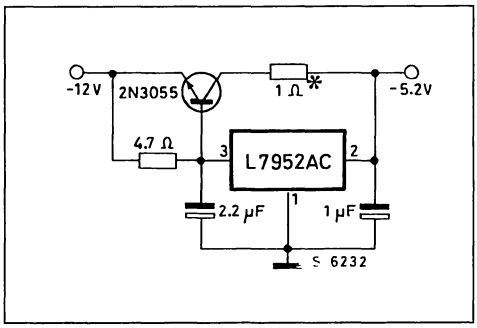


Figure 5 : Typical ECL System Power Supply (– 5.2V/4A).

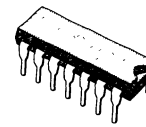


* Optional dropping resistor to reduce the power dissipated in the boost transistor.

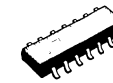
LF147/A/B
LF247/A/B
LF347/A/B

J–FET INPUT QUAD OP–AMPs

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J–FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 13 V/µs (typ)



N
DIP14
(Plastic package)



D
SO14
(Plastic micropackage)

J SUFFIX
(Cerdip package)

GC
LCC20
(Tricecop LCC)

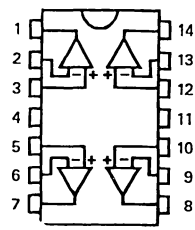
DESCRIPTION

These circuits are high speed J–FET input quad operational amplifiers incorporating well matched, high voltage J–FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

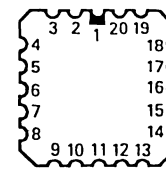
PIN CONNECTIONS (Top views)

DIP14/CERDIP14
SO14



1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^{+}
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - Output 3
9 - Inverting input 3
10 - Non-Inverting input 3
11 - V_{CC}^{-}
12 - Non-Inverting input 4
13 - Inverting input 4
14 - Output 4

LCC20



1 - NC
2 - Output 1
3 - Inverting input 1
4 - Non-inverting input 1
5 - NC
6 - V_{CC}^{-}
7 - NC
8 - Non-inverting input 2
9 - Inverting input 2
10 - Output 2
11 - NC
12 - Output 3
13 - Inverting input 3
14 - Non-inverting input 3
15 - NC
16 - V_{CC}^{+}
17 - NC
18 - Non-inverting input 4
19 - Inverting input 4
20 - Output 4

ORDER CODES

Part Number	Temperature	Package
LF147GC	– 55 °C to + 125 °C	LCC
LF147AGC	– 55 °C to + 125 °C	LCC
LF147BGC	– 55 °C to + 125 °C	LCC
LF147J	– 55 °C to + 125 °C	CERDIP
LF147AJ	– 55 °C to + 125 °C	CERDIP
LF147BJ	– 55 °C to + 125 °C	CERDIP
LF247N	– 40 °C to + 105 °C	DIP14
LF247AN	– 40 °C to + 105 °C	DIP14
LF247BN	– 40 °C to + 105 °C	DIP14
LF247D	– 40 °C to + 105 °C	SO14
LF247AD	– 40 °C to + 105 °C	SO14
LF247BD	– 40 °C to + 105 °C	SO14
LF347N	0 °C to + 70 °C	DIP14
LF347AN	0 °C to + 70 °C	DIP14
LF347BN	0 °C to + 70 °C	DIP14
LF347D	0 °C to + 70 °C	SO14
LF347AD	0 °C to + 70 °C	SO14
LF347BD	0 °C to + 70 °C	SO14

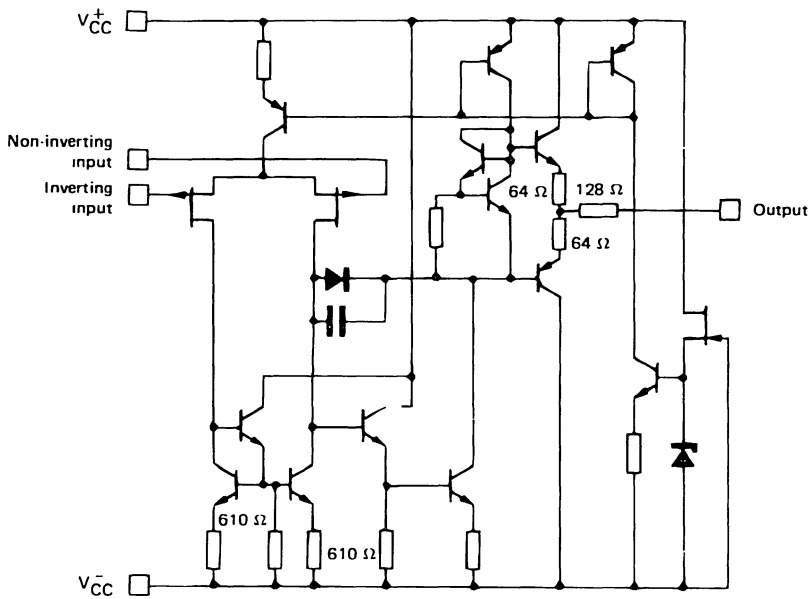
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	± 18	V
V_i	Input Voltage (note 3)	± 15	V
V_{CC}	Diff. Input Voltage (note 2)	± 30	V
P_{tot}	Power Dissipation	680	mW
	Output Short-circuit Duration (note 4)	Infinite	
T_{oper}	Operating Free Air Temperature Range		°C
	LF347, A, B	0 to 70	
	LF247, A, B	– 40 to 105	
	LF147, A, B	– 55 to 125	
T_{stg}	Storage Temperature Range	– 65 to 150	°C

Notes : 1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC} and V_{CC}.

2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

SCHEMATIC (each amplifier)



1/4 LF 347

E88LF347-01

Case	Outputs	Inverting Inputs	Non-inverting Inputs	V_{CC}^+	V_{CC}^-	N.C.
DIP14 SO14 CERDIP14	1, 7, 14, 8	2, 6, 13, 9	3, 5, 12, 10	4	11	
LCC20	2, 10, 12, 20	3, 9, 13, 19	4, 8, 14, 18	6	16	*

* **LCC20** : Other pins are not connected.

ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 15$ V (unless otherwise specified)
LF147, LF147B, LF147A $-55 \leq T_{amb} \leq +125$ °C
LF247, LF247B, LF247A $-40 \leq T_{amb} \leq +105$ °C
LF247, LF247B, LF247A $0 \leq T_{amb} \leq +70$ °C

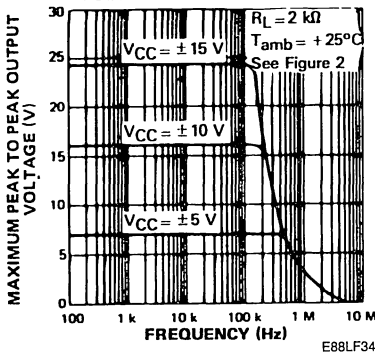
Symbol	Parameter	LF147A, B LF247A, B LF347A, B			LF147 LF247 LF347			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage							mV
	$T_{amb} = 25$ °C ($R_S < 10$ kΩ)					3	8	
	LF147B, LF247B, LF347B		3	5				
	LF147A, LF247A, LF347A		1	2				
	$T_{min} \leq T_{amb} \leq T_{max}$						13	
	LF147B, LF247B, LF347B			9				
	LF147A, LF247A, LF347A			5				
DV_{io}	Input Offset Voltage Drift		10			10		µV/°C
I_{io}	Input Offset Current *							
	$T_{amb} = 25$ °C		5	50		5	50	pA
	$T_{min} \leq T_{amb} \leq T_{max}$			4			4	nA
I_{ib}	Input Bias Current *							
	$T_{amb} = 25$ °C		30	200		30	200	pA
	$T_{min} \leq T_{amb} \leq T_{max}$			20			20	nA
A_{vd}	Large Signal Voltage Gain							V/mV
	($R_L > 2$ kΩ, $V_o = \pm 10$ V)							
	$T_{amb} = 25$ °C	50	200		50	200		
	$T_{min} \leq T_{amb} \leq T_{max}$	25			25			
SVR	Supply Voltage Rejection Ratio							dB
	($R_S < 10$ kΩ)							
	$T_{amb} = 25$ °C	80	86		80	86		
	$T_{min} \leq T_{amb} \leq T_{max}$	80			80			
I_{cc}	Supply Current, per Amp, no Load							mA
	$T_{amb} = 25$ °C		1.4	2.5		1.4	2.5	
	$T_{min} \leq T_{amb} \leq T_{max}$			2.5			2.5	
V_i	Input Voltage Range							V
	$T_{amb} = 25$ °C	−11		+11	−11		+11	
	$T_{min} \leq T_{amb} \leq T_{max}$							
CMR	Common Mode Rejection Ratio							dB
	($R_S < 10$ kΩ)							
	$T_{amb} = 25$ °C	80	86		70	86		
	$T_{min} \leq T_{amb} \leq T_{max}$	80			70			
I_{os}	Output Short-circuit Current							mA
	$T_{amb} = 25$ °C	10	40	60	10	40	60	
	$T_{min} \leq T_{amb} \leq T_{max}$	10		60	10		60	
$\pm V_{opp}$	Output Voltage Swing							V
	$T_{amb} = 25$ °C $R_L \geq 2$ kΩ	11	12		11	12		
	$R_L \geq 10$ kΩ	12	13.5		12	13.5		
	$T_{min} \leq T_{amb} \leq T_{max}$ $R_L \geq 2$ kΩ	11			11			
	$R_L \geq 10$ kΩ	12			12			
S_{vo}	Slew-rate ($V_i = 10$ V, $R_L = 2$ kΩ)							V/µs
	$C_L \leq 100$ pF, $T_{amb} = 25$ °C, unity gain	12	16		12	16		

* The input bias currents are junction leakage currents wich approximatvely double for every 10 °C increase in the junction temperature.

ELECTRICAL CHARACTERISTICS (continued)

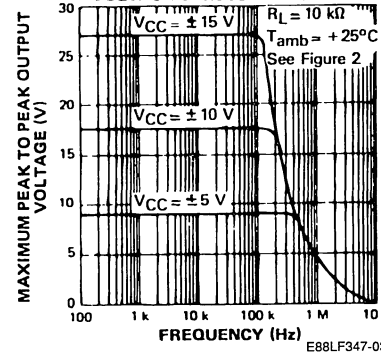
Symbol	Parameter	LF147A, B LF247A, B LF347A, B			LF147 LF247 LF347			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_r	Rise Time (V_i = 20 mV, R_L = 2 kΩ) C_L = 100 pF, T_{amb} = 25 °C, unity gain		0.1			0.1		µs
K_{ov}	Overshoot (V_i = 20 mV, R_L = 2 kΩ $C_L \leq$ 100 pF, T_{amb} = 25 °C, unity gain)		10			10		%
GBP	Gain Bandwidth Product (f = 100 kHz, T_{amb} = 25 °C V_{in} = 10 mV, R_L = 2 kΩ, C_L = 100 pF)	3.3	4.0	5.0	3.3	4.0	5.0	MHz
R_i	Input Resistance (T_{amb} = 25 °C)		10^{12}			10^{12}		Ω
THD	Total Harmonic Distortion (f = 1 kHz, A_v= 20 dB, R_L = 2 kΩ $C_L \leq$ 100 pF, T_{amb} = 25 °C, V_o = 2 V_{pp})		0.01			0.01		%
V_n	Equivalent Input Noise Voltage (f = 1 kHz, R_g = 100 Ω)		15			15		nV/√Hz
Øm	Phase Margin		45			45		Degrees
V_{o1}/V_{o2}	Channel Separation A_{vd} = 100, T_{amb} = 25 °C		120			120		dB

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



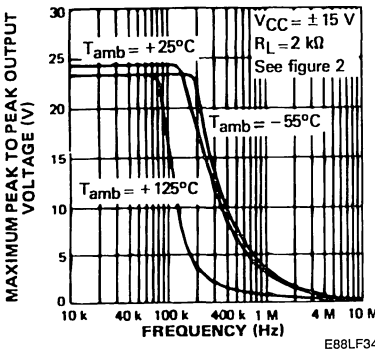
E88LF347-02

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



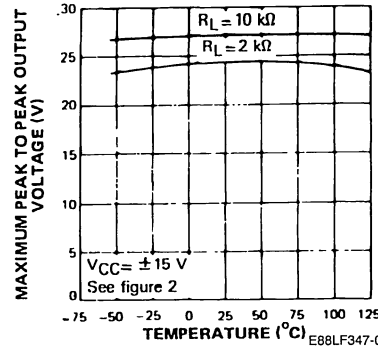
E88LF347-03

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



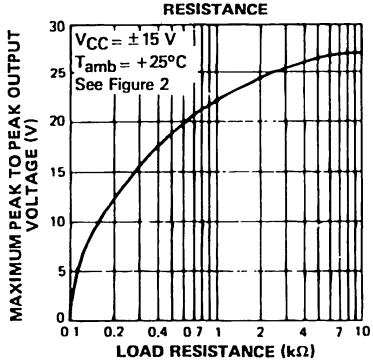
E88LF347-04

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREE-AIR TEMP.



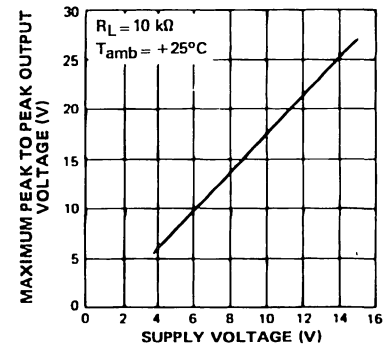
E88LF347-05

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



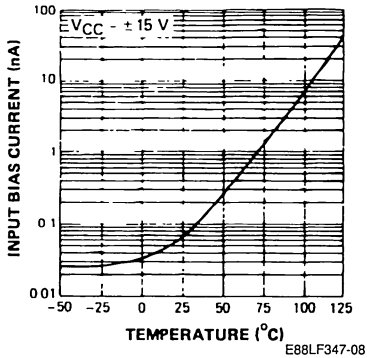
E88LF347-06

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



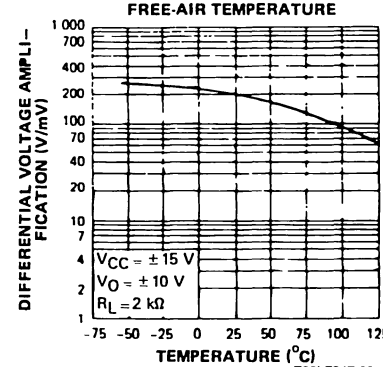
E88LF347-07

INPUT BIAS CURRENT VERSUS FREE-AIR TEMPERATURE



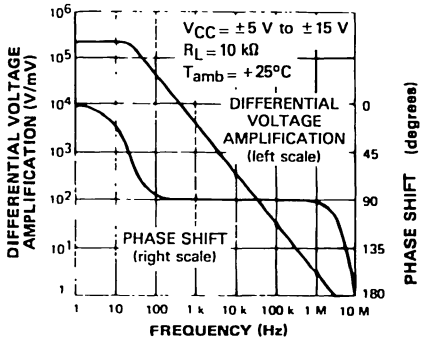
E88LF347-08

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE-AIR TEMPERATURE



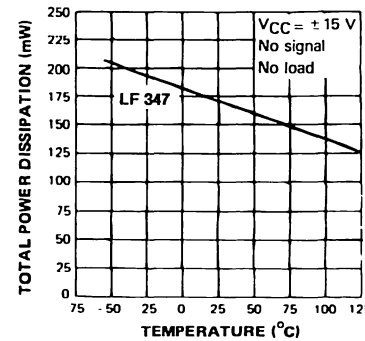
E88LF347-09

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



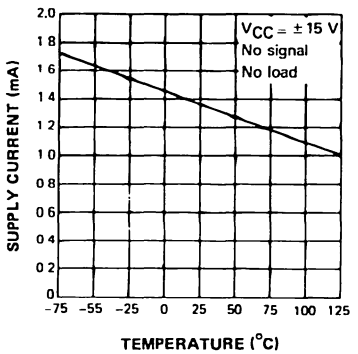
E88LF347-10

TOTAL POWER DISSIPATION VERSUS FREE-AIR TEMPERATURE



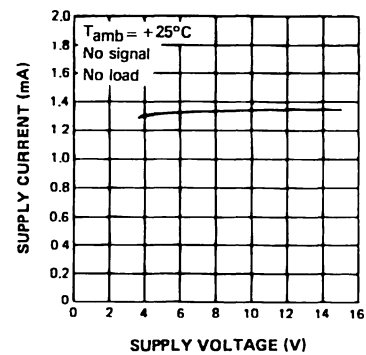
E88LF347-11

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE-AIR TEMPERATURE



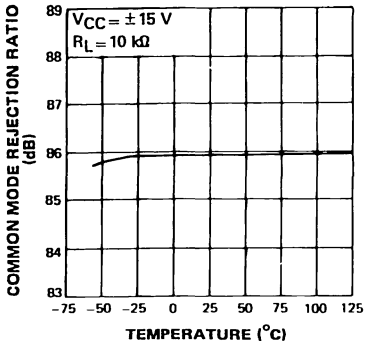
E88LF347-12

SUPPLY CURRENT PER AMPLIFIER VERSUS SUPPLY VOLTAGE



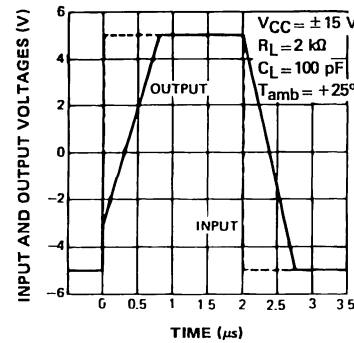
E88LF347-13

COMMON MODE REJECTION RATIO VERSUS FREE-AIR TEMPERATURE



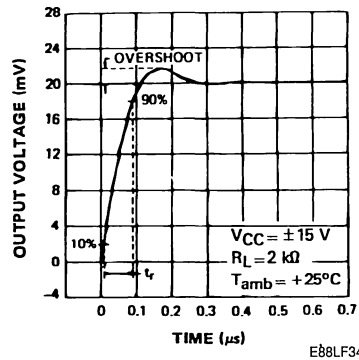
E88LF347-14

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



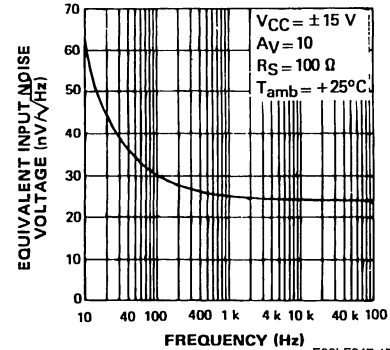
E88LF347-15

OUTPUT VOLTAGE VERSUS TIME



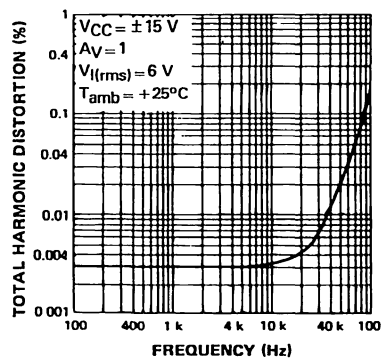
E88LF347-16

EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



E88LF347-17

TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



E88LF347-18

PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage Follower.

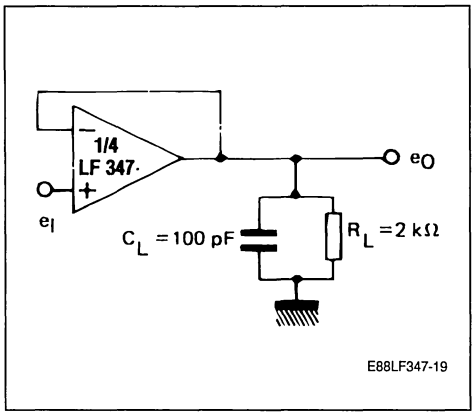
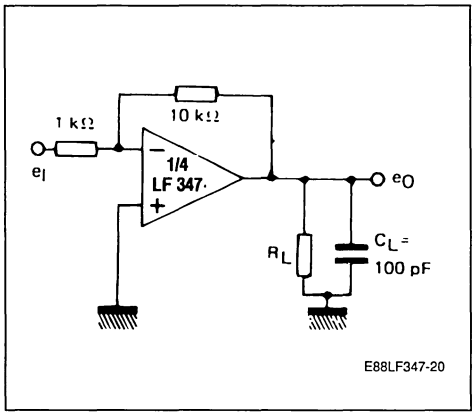
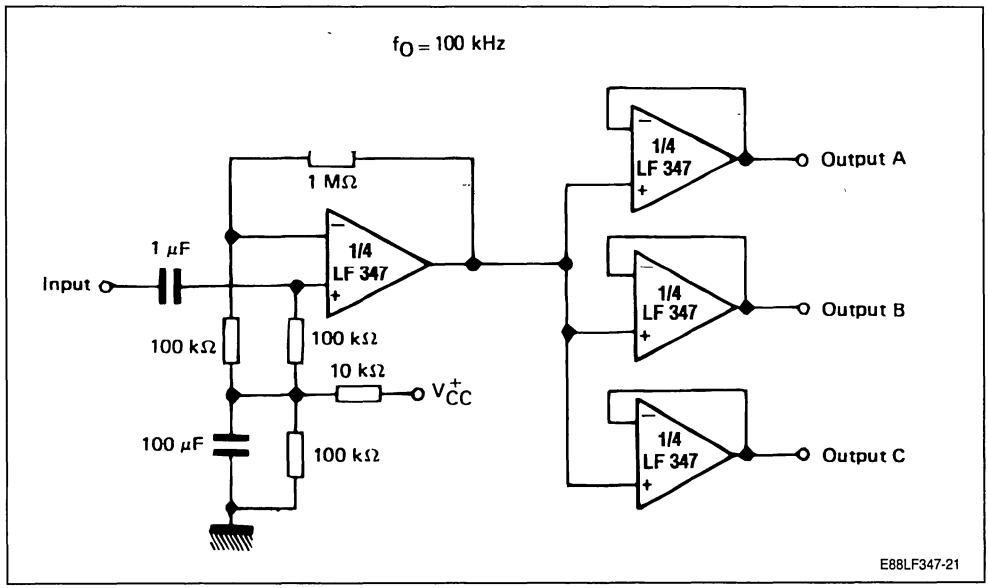


Figure 2 : Gain-of-10 Inverting Amplifier.



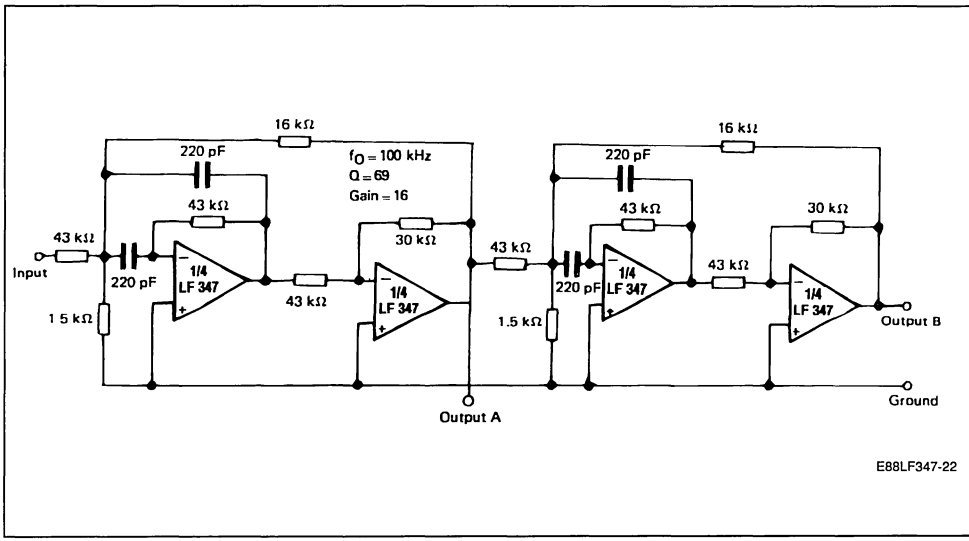
AUDIO DISTRIBUTION AMPLIFIER (f_o = 100 KHz)

Figure 3 : Voltage Follower.

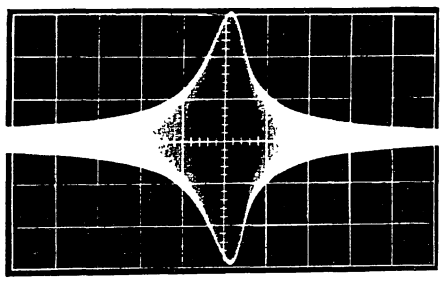


TYPICAL APPLICATION

POSITIVE FEEDBACK BANDPASS FILTER



OUTPUT A

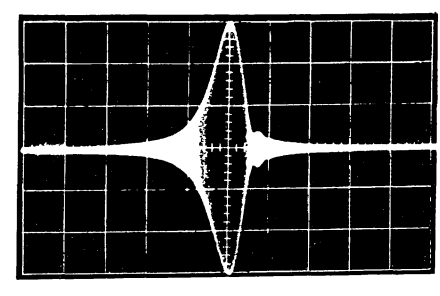


E88LF347-23

SECOND ORDER BANDPASS FILTER

f_o = 100 KHz ; Q = 30 ; Gain = 4

OUTPUT B



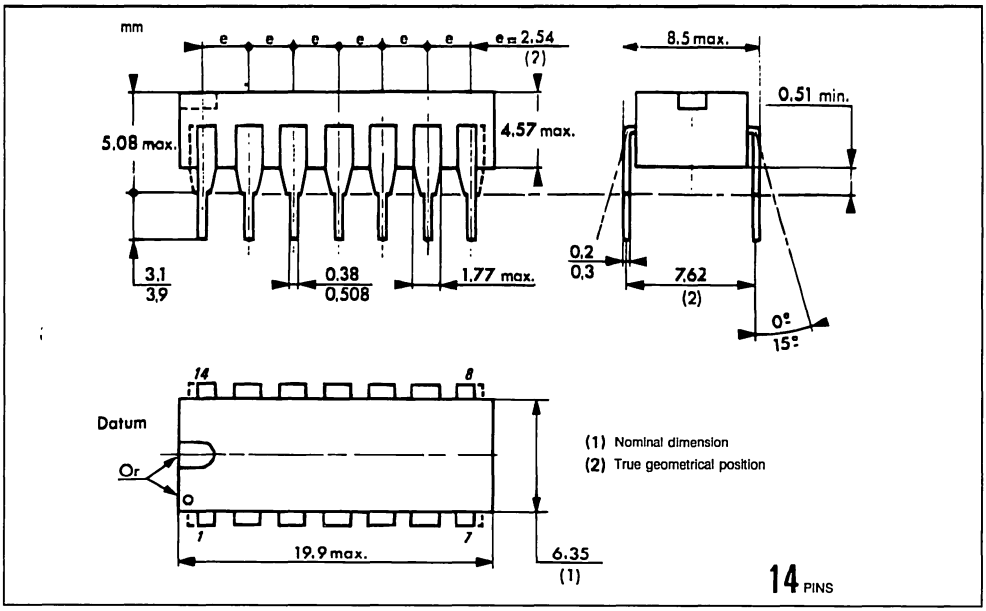
E88LF347-24

CASCADED BANDPASS FILTER

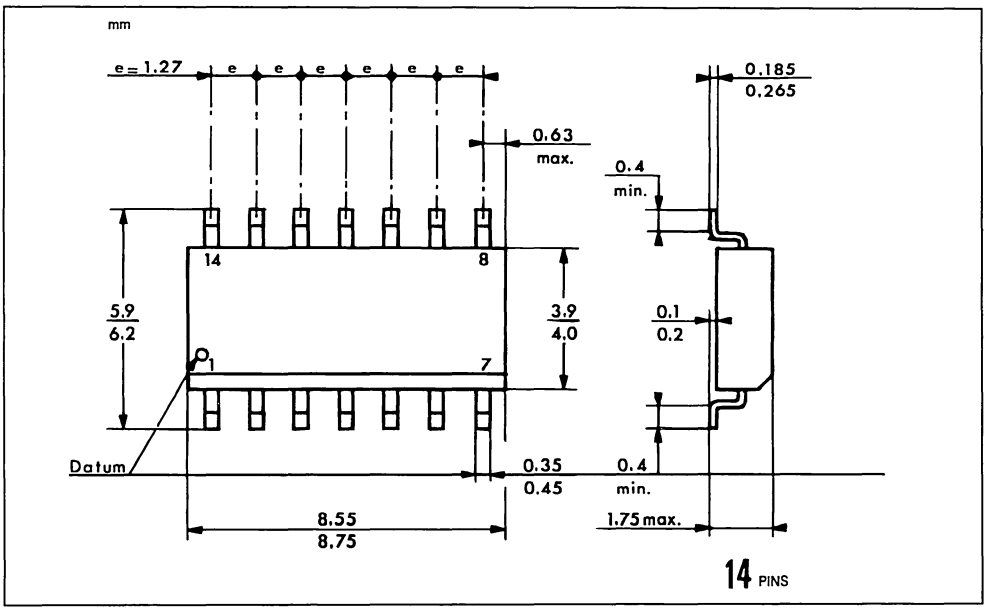
f_o = 100 KHz ; Q = 69 ; Gain = 16

PACKAGE MECHANICAL DATA

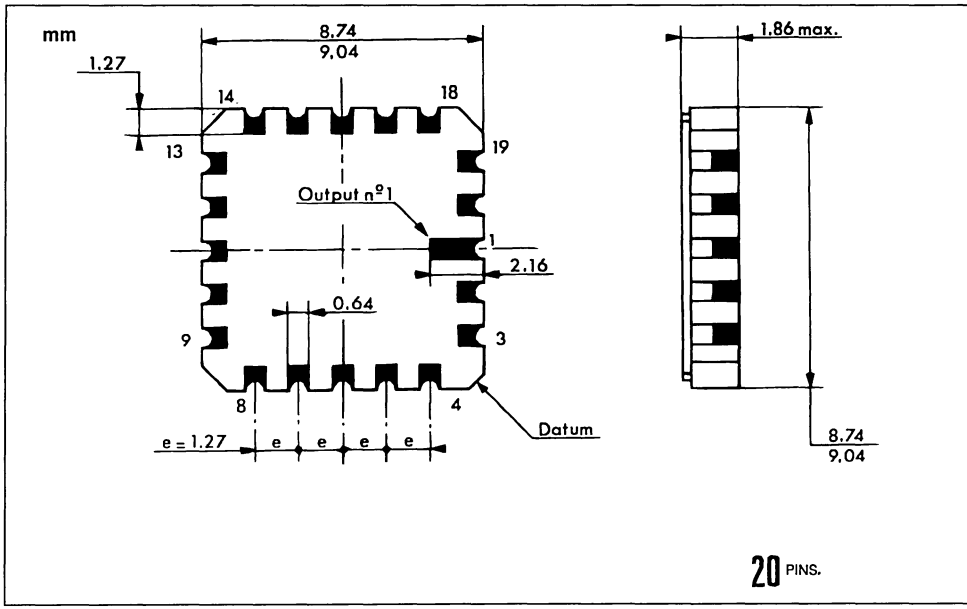
14 PINS – PLASTIC DIP OR CERDIP



14 PINS – PLASTIC MICROPACKAGE SO



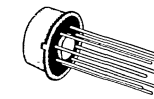
20 PINS – TRICECOP (LCC)



J–FET INPUT SINGLE OP–AMPs

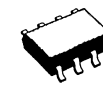
- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J–FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 13 V/µs (typ)

N
DIP8
(Plastic package)



H
TO99
(Metal can)

GC
LCC20
(Tricecop LCC)



D
SO8
(Plastic micropackage)

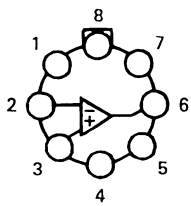
DESCRIPTION

These circuits are high speed J–FET input single operational amplifiers incorporating well matched, high voltage J–FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

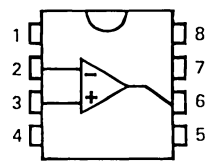
PIN CONNECTIONS (Top views)

TO99

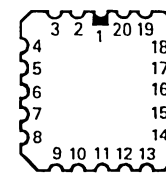


1 - Balance
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - Balance
6 - Output
7 - V_{CC}^+
8 - NC

DIP8
SO8



LCC20



1 - NC
2 - Balance
3 - NC
4 - NC
5 - Inverting input
6 - NC
7 - Non-inverting input
8 - NC
9 - NC
10 - V_{CC}^-
11 - NC
12 - Balance
13 - NC
14 - NC
15 - Output
16 - NC
17 - V_{CC}^+
18 - NC
19 - NC
20 - NC

ORDER CODES

Part Number	Temperature	Package
LF151GC	– 55 °C to + 125 °C	LCC
LF151AGC	– 55 °C to + 125 °C	LCC
LF151BGC	– 55 °C to + 125 °C	LCC
LF151H	– 55 °C to + 125 °C	METAL CAN
LF151AH	– 55 °C to + 125 °C	METAL CAN
LF151BH	– 55 °C to + 125 °C	METAL CAN
LF251N	– 40 °C to + 105 °C	DIP8
LF251AN	– 40 °C to + 105 °C	DIP8
LF251BN	– 40 °C to + 105 °C	DIP8
LF251D	– 40 °C to + 105 °C	SO8
LF251AD	– 40 °C to + 105 °C	SO8
LF251BD	– 40 °C to + 105 °C	SO8
LF351N	0 °C to + 70 °C	DIP8
LF351AN	0 °C to + 70 °C	DIP8
LF351BN	0 °C to + 70 °C	DIP8
LF351D	0 °C to + 70 °C	SO8
LF351AD	0 °C to + 70 °C	SO8
LF351BD	0 °C to + 70 °C	SO8

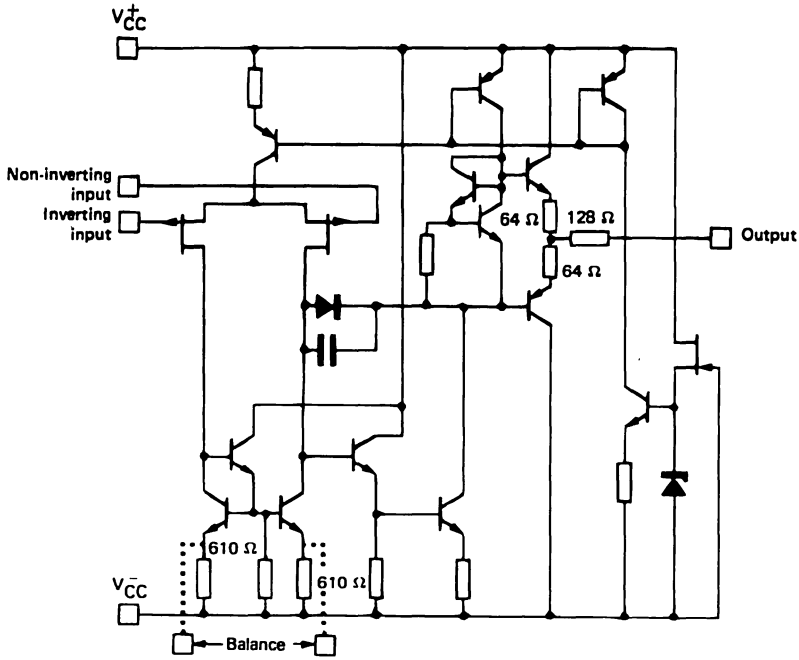
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	± 18	V
V_i	Input Voltage (note 3)	± 15	V
V_{CC}	Diff. Input Voltage (note 2)	± 30	V
P_{tot}	Power Dissipation	680	mW
	Output Short-circuit Duration (note 4)	Infinite	
T_{oper}	Operating Free Air Temperature Range		°C
	LF351, A, B	0 to 70	
	LF251, A, B	– 40 to 105	
	LF151, A, B	– 55 to 125	
T_{stg}	Storage Temperature Range	– 65 to 150	°C

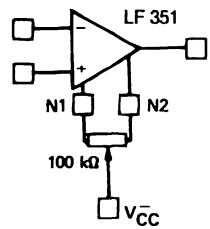
Notes : 1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC} and V_{CC}.

2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

SCHEMATIC DIAGRAM



INPUT OFFSET VOLTAGE NULL CIRCUITS



E88LF151-01

Case	Balance	Inverting Input	Non-inverting Input	Output	V_{CC}^+	V_{CC}^-	N.C.
DIP8 SO8 TO99	1, 5	2	3	6	7	4	8
LCC20	2, 12	5	7	15	17	10	*

* **LCC20** : Other pins are not connected.

ELECTRICAL CHARACTERISTICS

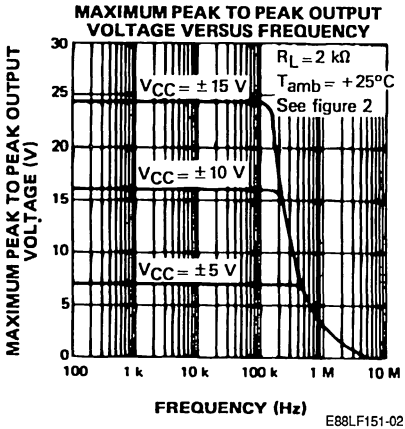
$V_{CC} = \pm 15$ V (unless otherwise specified)
LF151, LF151A, LF151B $-55 \leq T_{amb} \leq +125$ °C
LF251, LF251A, LF251B $-40 \leq T_{amb} \leq +105$ °C
LF351, LF351A, LF351B $0 \leq T_{amb} \leq +70$ °C

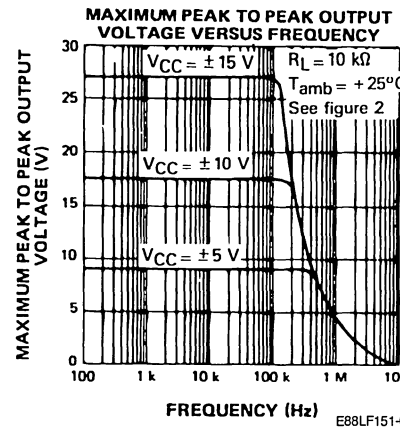
Symbol	Parameter		LF151A, B LF251A, B LF351A, B			LF151 LF251 LF351			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($R_S < 10$ kΩ)								mV
	$T_{amb} = 25$ °C	LF151B, LF251B, LF351B	3	5			3	8	
		LF151A, LF251A, LF351A	1	2					
	$T_{min} \leq T_{amb} \leq T_{max}$	LF151B, LF251B, LF351B		9				13	
		LF151A, LF251A, LF351A		5					
DV_{io}	Input Offset Voltage Drift			10			10		µV/°C
I_{io}	Input Offset Current *								
	$T_{amb} = 25$ °C			5	50		5	50	pA
	$T_{min} \leq T_{amb} \leq T_{max}$				4			4	nA
I_{ib}	Input Bias Current *								
	$T_{amb} = 25$ °C			20	200		20	200	pA
	$T_{min} \leq T_{amb} \leq T_{max}$				20			20	nA
A_{vd}	Large Signal Voltage Gain ($R_L > 2$ kΩ, $V_o = \pm 10$ V)								V/mV
	$T_{amb} = 25$ °C		50	200		50	200		
	$T_{min} \leq T_{amb} \leq T_{max}$		25			25			
SVR	Supply Voltage Rejection Ratio ($R_S < 10$ kΩ)								dB
	$T_{amb} = 25$ °C		80	86		80	86		
	$T_{min} \leq T_{amb} \leq T_{max}$		80			80			
Icc	Supply Current, no Load								mA
	$T_{amb} = 25$ °C			1.4	2.5		1.4	2.5	
	$T_{min} \leq T_{amb} \leq T_{max}$				2.5			2.5	
V_i	Input Voltage Range								V
	$T_{amb} = 25$ °C		−11		+11	−11		+11	
	$T_{min} \leq T_{amb} \leq T_{max}$								
CMR	Common Mode Rejection Ratio ($R_S < 10$ kΩ)								dB
	$T_{amb} = 25$ °C		80	86		70	86		
	$T_{min} \leq T_{amb} \leq T_{max}$		80			70			
I_{os}	Output Short-circuit Current								mA
	$T_{amb} = 25$ °C		10	40	60	10	40	60	
	$T_{min} \leq T_{amb} \leq T_{max}$		10		60	10		60	
$\pm V_{opp}$	Output Voltage Swing								V
	$T_{amb} = 25$ °C	$R_L \geq 2$ kΩ	11	12		11	12		
		$R_L \geq 10$ kΩ	12	13.5		12	13.5		
	$T_{min} \leq T_{amb} \leq T_{max}$	$R_L \geq 2$ kΩ	11			11			
		$R_L \geq 10$ kΩ	12			12			
S_{vo}	Slew-rate ($V_i = 10$ V, $R_L = 2$ kΩ)								V/µs
	$C_L \leq 100$ pF, $T_{amb} = 25$ °C, unity gain)		12	16		12	16		

* The input bias currents are junction leakage currents wich approximatively double for every 10 °C increase in the junction temperature.

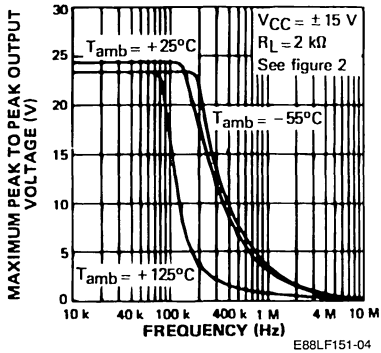
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	LF151A, B LF251A, B LF351A, B			LF151 LF251 LF351			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_r	Rise Time (V_I = 20 mV, R_L = 2 kΩ) C_L = 100 pF, T_{amb} = 25 °C, unity Gain		0.1			0.1		µs
K_{ov}	Overshoot (V_I = 20 mV, R_L = 2 kΩ $C_L \leq$ 100 pF, T_{amb} = 25 °C, unity gain)		10			10		%
GBP	Gain Bandwidth Product (f = 100 kHz, Tamb = 25 °C V_{in} = 10 mV, R_L = 2 kΩ, C_L = 100 pF)	3.3	4.0	5.0	3.3	4.0	5.0	MHz
R_I	Input Resistance (T_{amb} = 25 °C)		10^{12}			10^{12}		Ω
THD	Total Harmonic Distortion (f = 1 kHz, A_v = 20 dB, R_L = 2 kΩ $C_L \leq$ 100 pF, T_{amb} = 25 °C, V_o = 2 V_{pp})		0.01			0.01		%
V_n	Equivalent Input Noise Voltage (f = 1 kHz, R_g = 100 Ω)		15			15		nV/√Hz
∅m	Phase Margin		45			45		Degrees



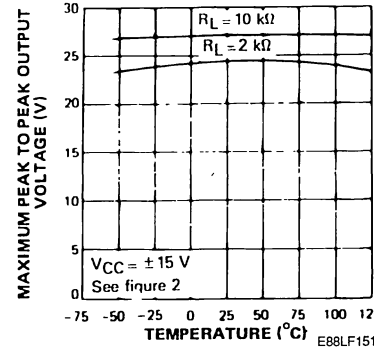


MAXIMUM PEAK TO PEAK OUPUT VOLTAGE VERSUS FREE-AIR TEMP.



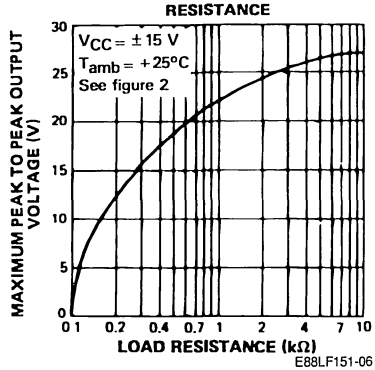
E88LF151-04

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



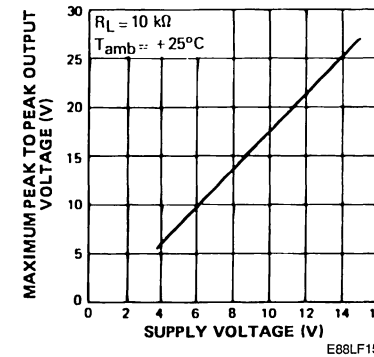
E88LF151-05

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



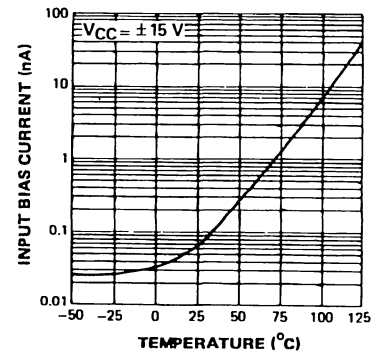
E88LF151-06

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



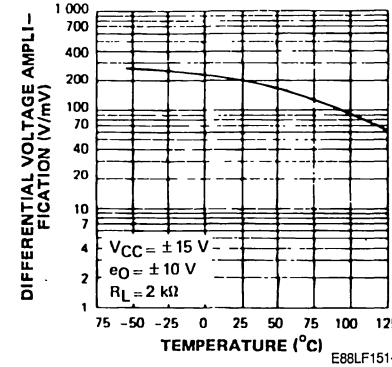
E88LF151-07

INPUT BIAS CURRENT VERSUS FREE-AIR TEMPERATURE



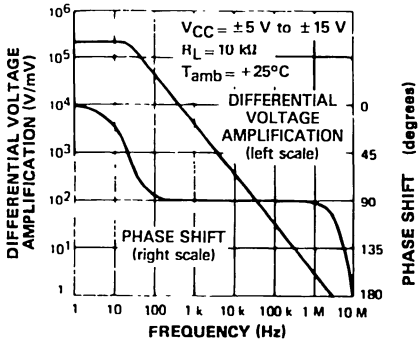
E88LF151-08

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE-AIR TEMPERATURE



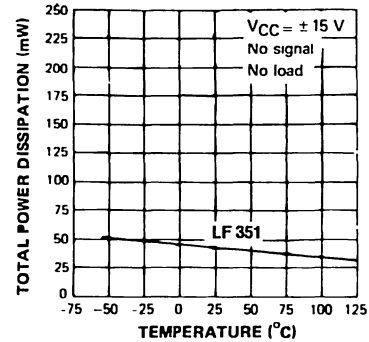
E88LF151-09

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



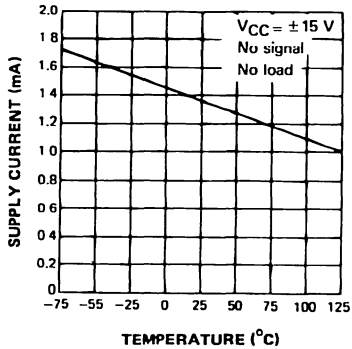
E88LF151-10

TOTAL POWER DISSIPATION VERSUS FREE-AIR TEMPERATURE



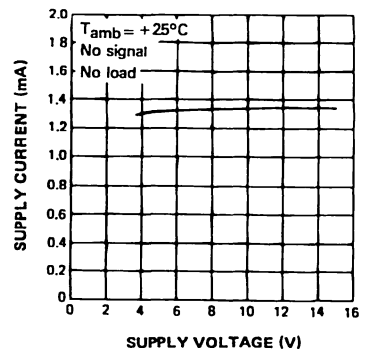
E88LF151-11

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE-AIR TEMPERATURE



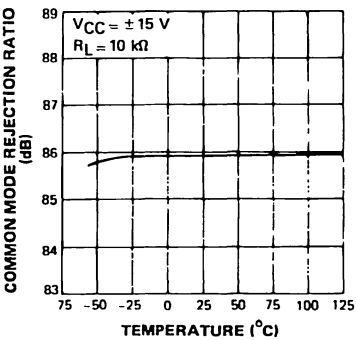
E88LF151-12

SUPPLY CURRENT PER AMPLIFIER VERSUS SUPPLY VOLTAGE



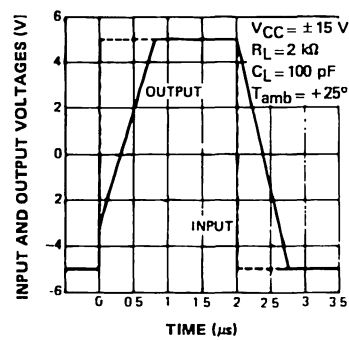
E88LF151-13

COMMON MODE REJECTION RATIO VERSUS FREE-AIR TEMPERATURE



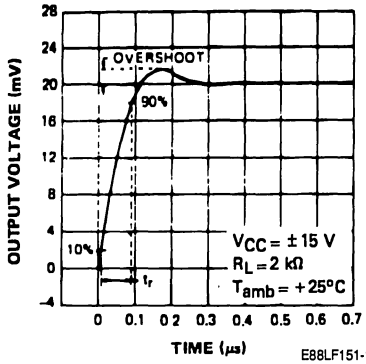
E88LF151-14

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



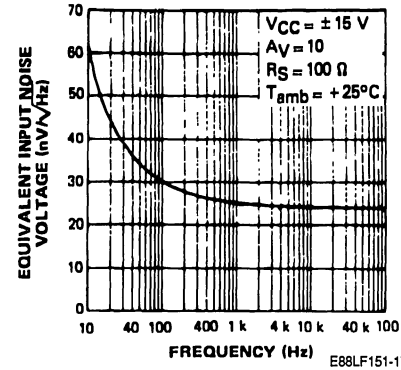
E88LF151-15

OUTPUT VOLTAGE VERSUS TIME



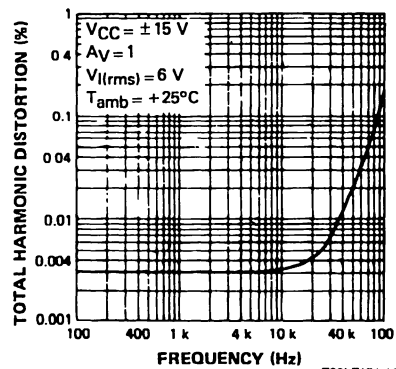
E88LF151-16

EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



E88LF151-17

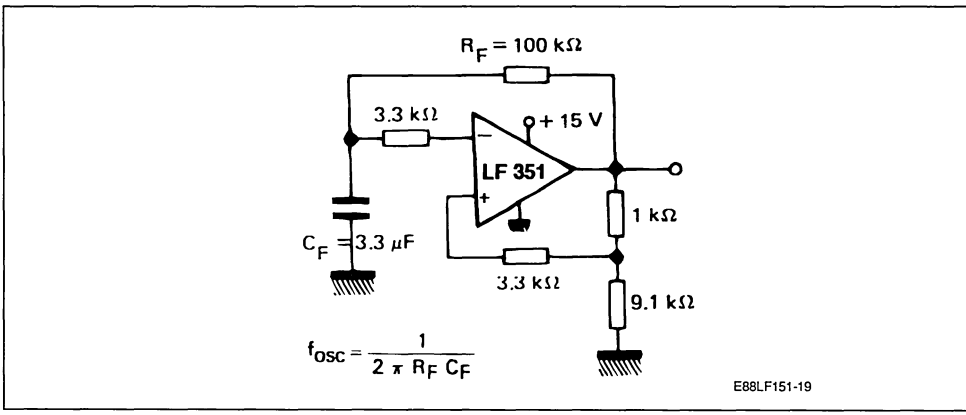
TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



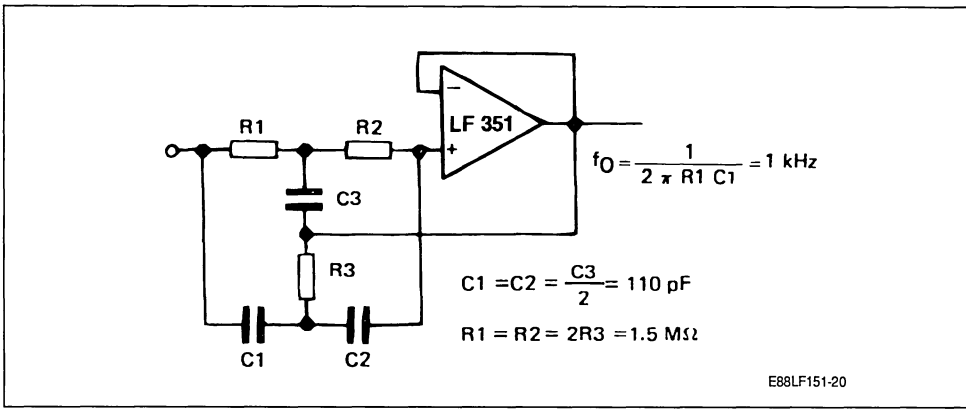
E88LF151-18

TYPICAL APPLICATIONS

(0.5 Hz) SQUARE WAVE OSCILLATOR



HIGH Q NOTCH FILTER



PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage Follower.

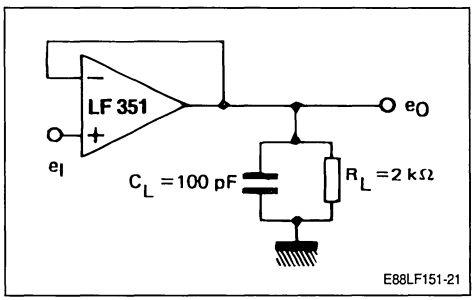
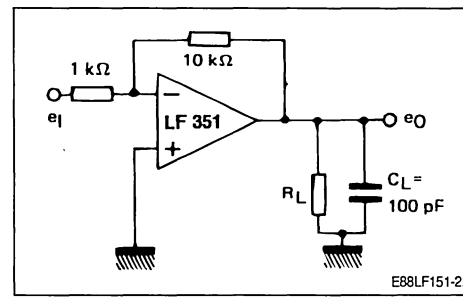
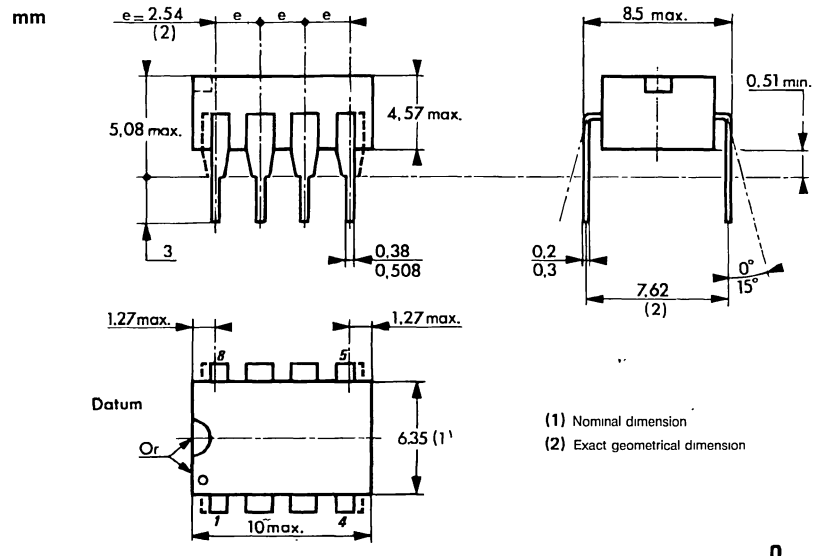


Figure 2 : Gain-of-10 Inverting Amplifier.

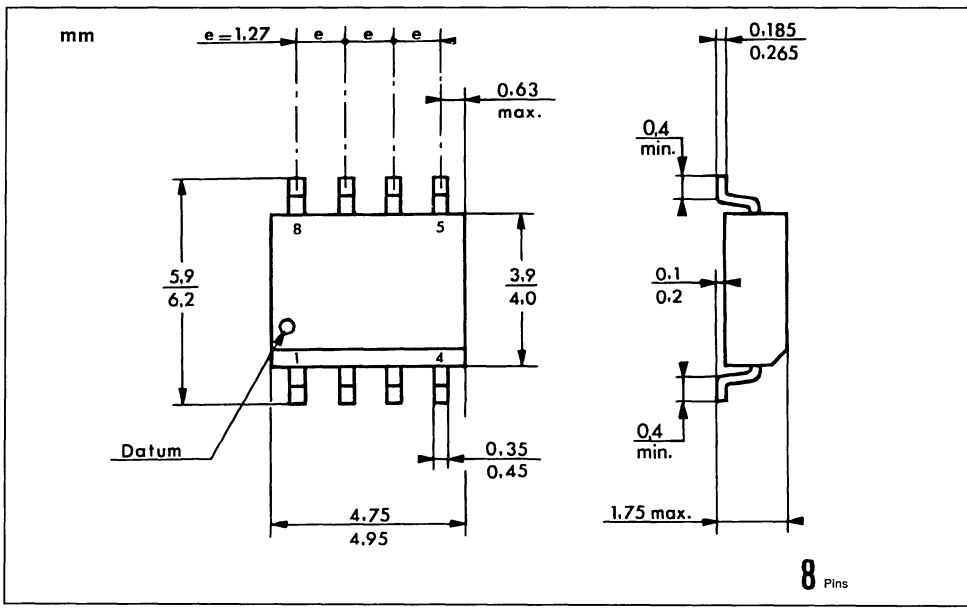


PACKAGE MECHANICAL DATA

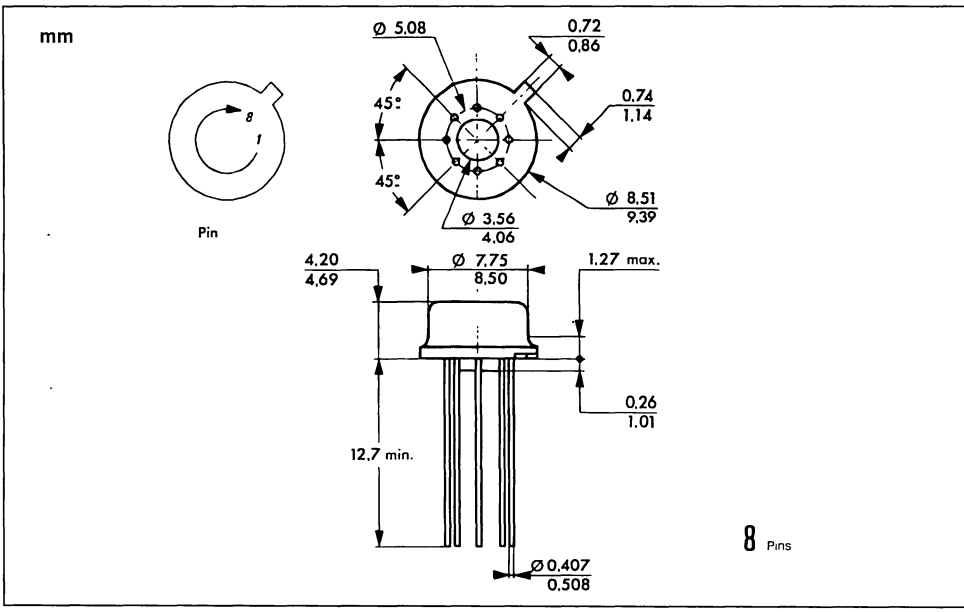
8 PINS – PLASTIC DIP



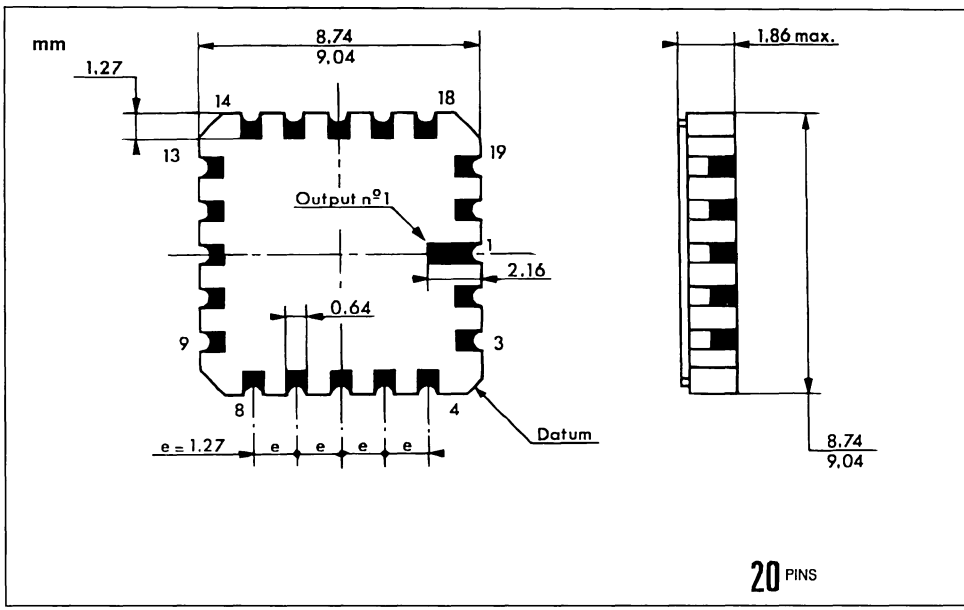
8 PINS – PLASTIC MICROPACKAGE (SO)



TO99 – METAL CAN

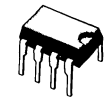


20 PINS – TRICECOP (LCC)

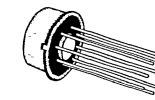


J–FET INPUT DUAL OP–AMPs

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J–FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 13 V/µs (typ)

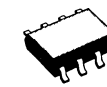


N
DIP8
(Plastic package)



H
TO99
(Metal can)

GC
LCC20
(Tricecop LCC)



D
SO8
(Plastic micropackage)

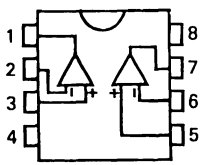
DESCRIPTION

The LF353 - 353A - 353B are high speed J–FET input dual operational amplifiers incorporating well matched, high voltage J–FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

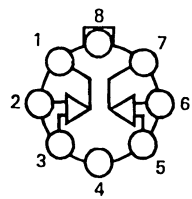
PIN CONNECTIONS (Top views)

DIP8
SO8

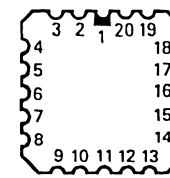


1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

TO99



LCC20



1 - NC
2 - Output 1
3 - NC
4 - NC
5 - Inverting input 1
6 - NC
7 - Non-inverting input 1
8 - NC
9 - NC
10 - V_{CC}^-
11 - NC
12 - Non-inverting input 2
13 - NC
14 - NC
15 - Inverting input 2
16 - NC
17 - Output 2
18 - NC
19 - NC
20 - V_{CC}^+

ORDER CODES

Part Number	Temperature	Package
LF153GC	– 55 °C to + 125 °C	LCC
LF153AGC	– 55 °C to + 125 °C	LCC
LF153BGC	– 55 °C to + 125 °C	LCC
LF153H	– 55 °C to + 125 °C	METAL CAN
LF153AH	– 55 °C to + 125 °C	METAL CAN
LF153BH	– 55 °C to + 125 °C	METAL CAN
LF253N	– 40 °C to + 105 °C	DIP8
LF253AN	– 40 °C to + 105 °C	DIP8
LF253BN	– 40 °C to + 105 °C	DIP8
LF253D	– 40 °C to + 105 °C	SO8
LF253AD	– 40 °C to + 105 °C	SO8
LF253BD	– 40 °C to + 105 °C	SO8
LF353N	0 °C to + 70 °C	DIP8
LF353AN	0 °C to + 70 °C	DIP8
LF353BN	0 °C to + 70 °C	DIP8
LF353D	0 °C to + 70 °C	SO8
LF353AD	0 °C to + 70 °C	SO8
LF353BD	0 °C to + 70 °C	SO8

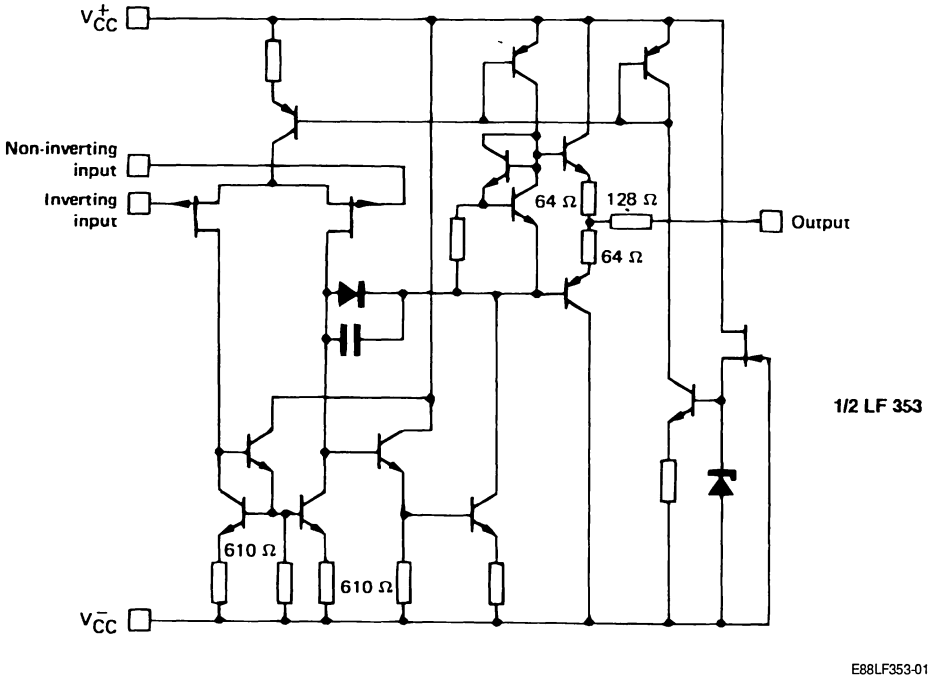
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	± 18	V
V_i	Input Voltage (note 3)	± 15	V
V_{CC}	Diff. Input Voltage (note 2)	± 30	V
P_{tot}	Power Dissipation	680	mW
	Output Short-circuit Duration (note 4)	Infinite	
T_{oper}	Operating Free Air Temperature Range		°C
	LF353, A, B	0 to 70	
	LF253, A, B	– 40 to 105	
	LF153, A, B	– 55 to 125	
T_{stg}	Storage Temperature Range	– 65 to 150	°C

Notes : 1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.

2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

SCHEMATIC DIAGRAM



Case	Outputs	Non-inverting Inputs	Inverting Inputs	V_{CC}^{+}	V_{CC}^{-}	N.C.
DIP8 SO8 TO99	1, 7	3, 5	2, 6	4	8	
LCC20	2, 17	7, 12	5, 15	10	20	*

* **LCC20** : Other pins are not connected.

ELECTRICAL CHARACTERISTICS

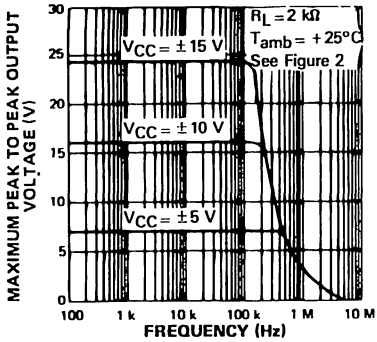
Vcc = ± 15 V (unless otherwise specified)
LF153, LF153A, LF153B $-55 \leq T_{amb} \leq +125$ °C
LF253, LF153A, LF253B $-40 \leq T_{amb} \leq +105$ °C
LF353, LF153A, LF353B $0 \leq T_{amb} \leq +70$ °C

Symbol	Parameter	LF153A, B LF253A, B LF353A, B			LF153 LF253 LF353			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage							mV
	T_{amb} = 25 °C (R_s < 10 kΩ)							
	LF153B, LF253B, LF353B	3	5			3	8	
	LF153A, LF253A, LF353A	1	2					
	$T_{min} \leq T_{amb} \leq T_{max}$							
	LF153B, LF253B, LF353B		9				13	
	LF153A, LF253A, LF353A		5					
DV_{io}	Input Offset Voltage Drift		10			10		µV/°C
I_{io}	Input Offset Current *							
	T_{amb} = 25 °C		5	50		5	50	pA
	$T_{min} \leq T_{amb} \leq T_{max}$			4			4	nA
I_{ib}	Input Bias Current *							
	T_{amb} = 25 °C		20	200		20	200	pA
	$T_{min} \leq T_{amb} \leq T_{max}$			20			20	nA
A_{vd}	Large Signal Voltage Gain							V/mV
	(R_L > 2 kΩ, V_o = ± 10 V)							
	T_{amb} = 25 °C	50	200		50	200		
	$T_{min} \leq T_{amb} \leq T_{max}$	25			25			
SVR	Supply voltage Rejection Ratio							dB
	(R_s < 10 kΩ)							
	T_{amb} = 25 °C	80	86		80	86		
	$T_{min} \leq T_{amb} \leq T_{max}$	80			80			
I_{cc}	Supply Current, per Amp, no Load							mA
	T_{amb} = 25 °C		1.4	2.5		1.4	2.5	
	$T_{min} \leq T_{amb} \leq T_{max}$			2.5			2.5	
V_i	Input Voltage Range							V
	T_{amb} = 25 °C	− 11		+ 11	− 11		+ 11	
	$T_{min} \leq T_{amb} \leq T_{max}$							
CMR	Common Mode Rejection Ratio							dB
	(R_s < 10 kΩ)							
	T_{amb} = 25 °C	80	86		70	86		
	$T_{min} \leq T_{amb} \leq T_{max}$	80			70			
I_{os}	Output Short-circuit Current							mA
	T_{amb} = 25 °C	10	40	60	10	40	60	
	$T_{min} \leq T_{amb} \leq T_{max}$	10		60	10		60	
± V_{opp}	Output Voltage Swing							V
	T_{amb} = 25 °C $R_L \geq$ 2 kΩ	11	12		11	12		
	$R_L \geq$ 10 kΩ	12	13.5		12	13.5		
	$T_{min} \leq T_{amb} \leq T_{max}$ $R_L \geq$ 2 kΩ	11			11			
	$R_L \geq$ 10 kΩ	12			12			
S_{vo}	Slew-rate (V_i = 10 V, R_L = 2 kΩ)							V/µs
	$C_L \leq$ 100 pF, T_{amb} = 25 °C, unity gain)	12	16		12	16		

ELECTRICAL CHARACTERISTICS (continued)

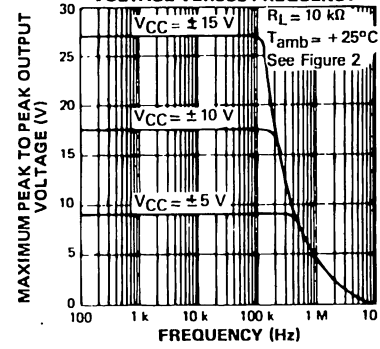
Symbol	Parameter	LF153A, B LF253A, B LF353A, B			LF153 LF253 LF353			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_r	Rise Time (V_I = 20 mV, R_L = 2 kΩ) C_L = 100pF, T_{amb} = 25 °C, unity Gain		0.1			0.1		µs
K_{ov}	Overshoot (V_I = 20 mV, R_L = 2 kΩ C_L ≤ 100 pF, T_{amb} = 25 °C, unity gain)		10			10		%
GBP	Gain Bandwidth Product (f = 100 kHz, T_{amb} = 25 °C V_{in} = 10 mV, R_L = 2 kΩ, C_L = 100 pF)	3.3	4.0	5.0	3.3	4.0	5.0	MHz
R_I	Input Resistance (T_{amb} = 25 °C)		10^{12}			10^{12}		Ω
THD	Total Harmonic Distortion (f = 1 kHz, A_v= 20 dB, R_L = 2 kΩ C_L < 100 pF, T_{amb} = 25 °C, V_o = 2 V_{pp})		0.01			0.01		%
V_n	Equivalent Input Noise Voltage (f = 1 kHz, R_g = 100 Ω)		15			15		$nV/\sqrt{Hz}$
∅m	Phase Margin		45			45		Degrees
V_{o1}/V_{o2}	Channel Separation A_{vd} = 100, T_{amb} = 25 °C		120			120		dB

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



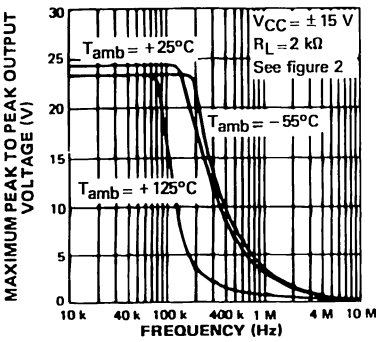
E88LF353-02

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



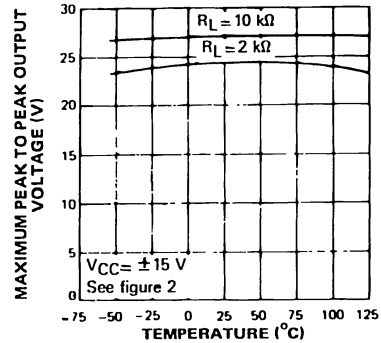
E88LF353-03

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



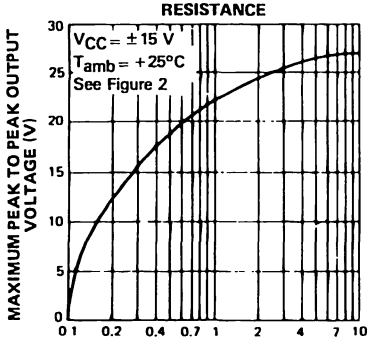
E88LF353-04

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREE-AIR TEMP.



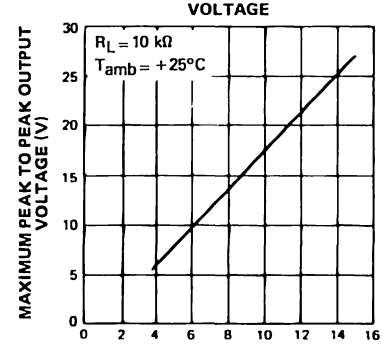
E88LF353-05

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



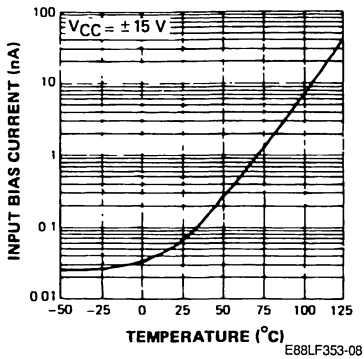
E88LF353-06

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



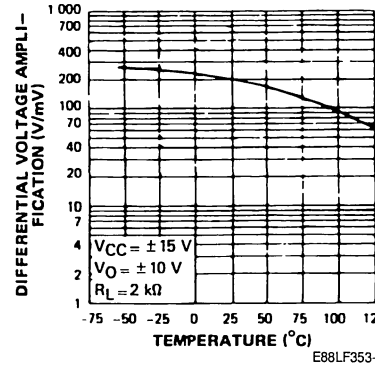
E88LF353-07

INPUT BIAS CURRENT VERSUS FREE-AIR TEMPERATURE



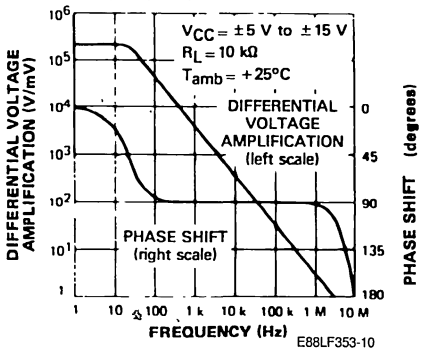
E88LF353-08

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE-AIR TEMPERATURE



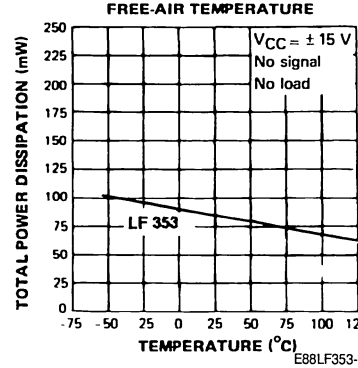
E88LF353-09

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



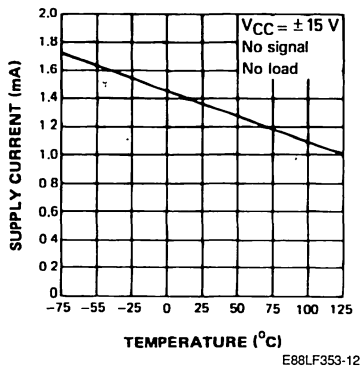
E88LF353-10

TOTAL POWER DISSIPATION VERSUS FREE-AIR TEMPERATURE



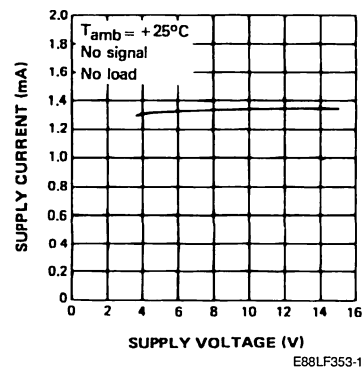
E88LF353-11

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE-AIR TEMPERATURE



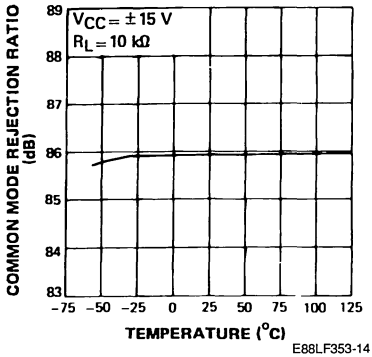
E88LF353-12

SUPPLY CURRENT PER AMPLIFIER VERSUS SUPPLY VOLTAGE



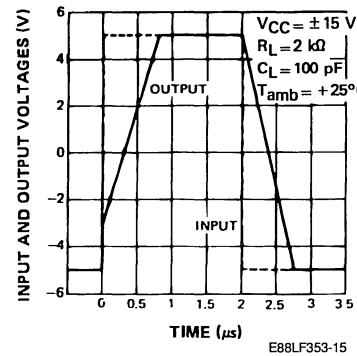
E88LF353-13

COMMON MODE REJECTION RATIO VERSUS FREE-AIR TEMPERATURE



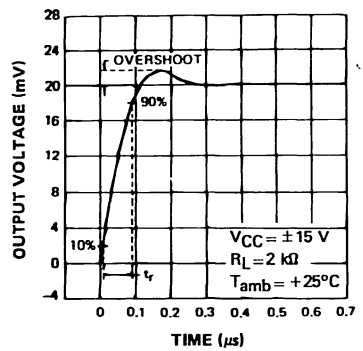
E88LF353-14

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



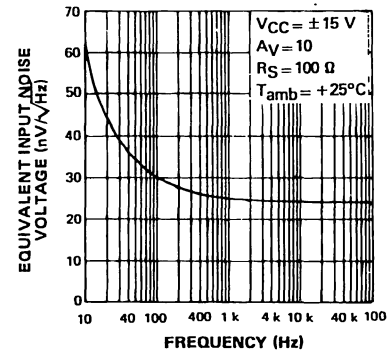
E88LF353-15

OUTPUT VOLTAGE VERSUS TIME



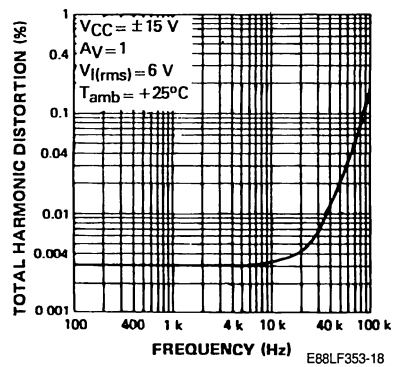
E88LF353-16

EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



E88LF353-17

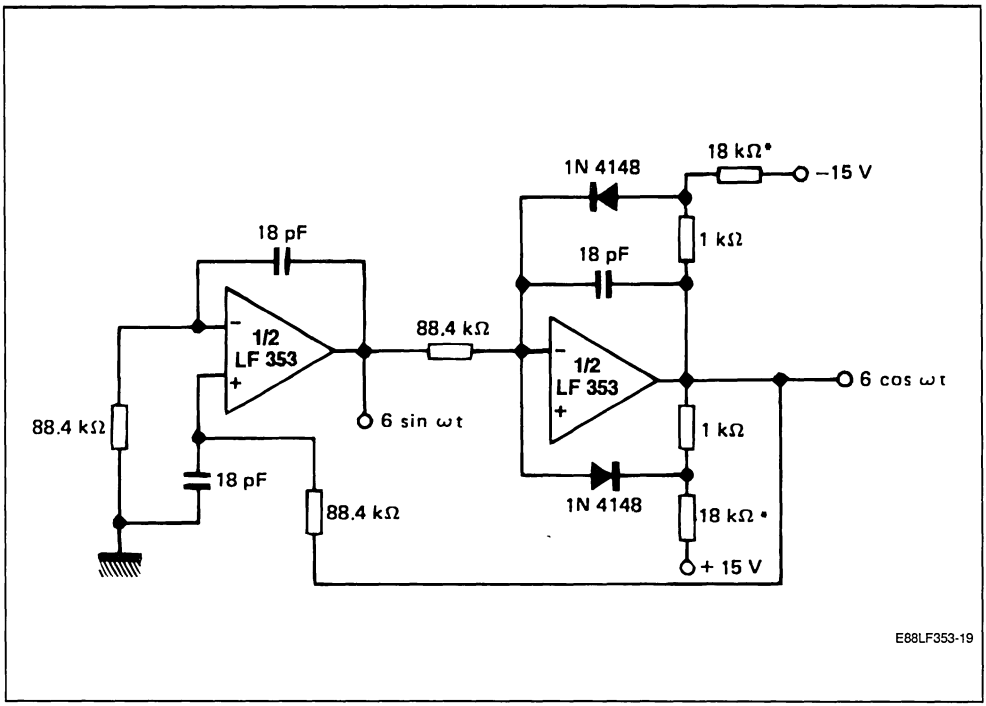
TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



E88LF353-18

TYPICAL APPLICATION

QUADRATURE OSCILLATOR



* These resistor values may be adjusted for a symmetrical output.

PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage Follower.

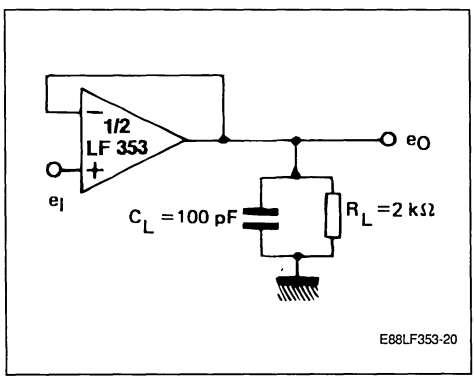
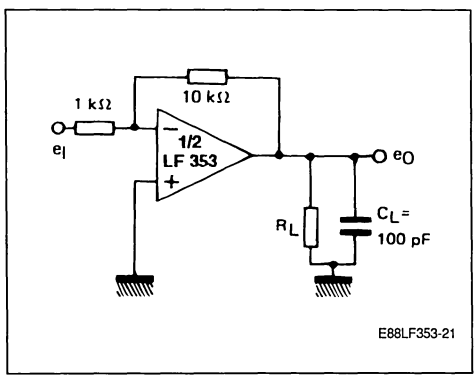
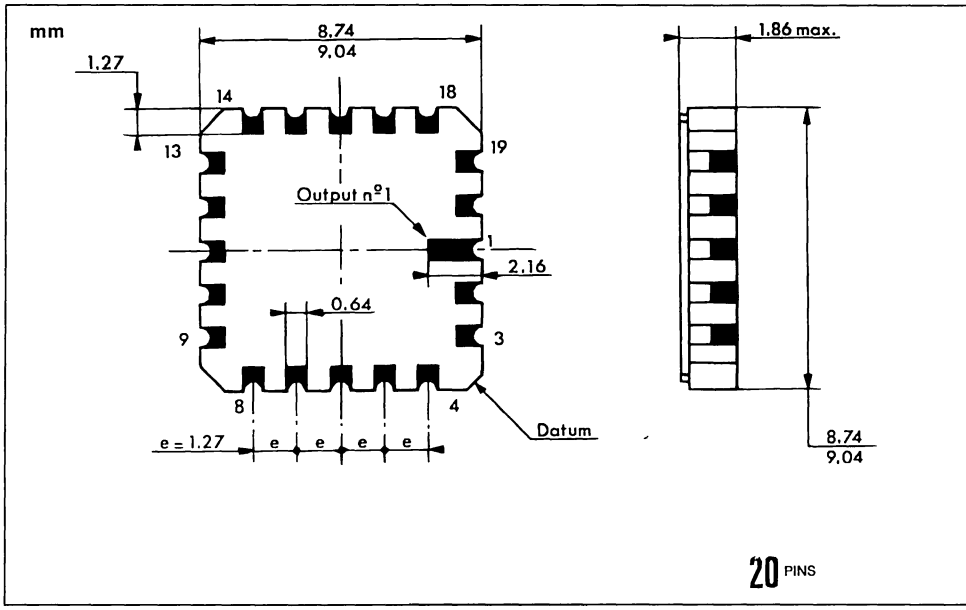


Figure 2 : Gain-of-10 Inverting Amplifier.

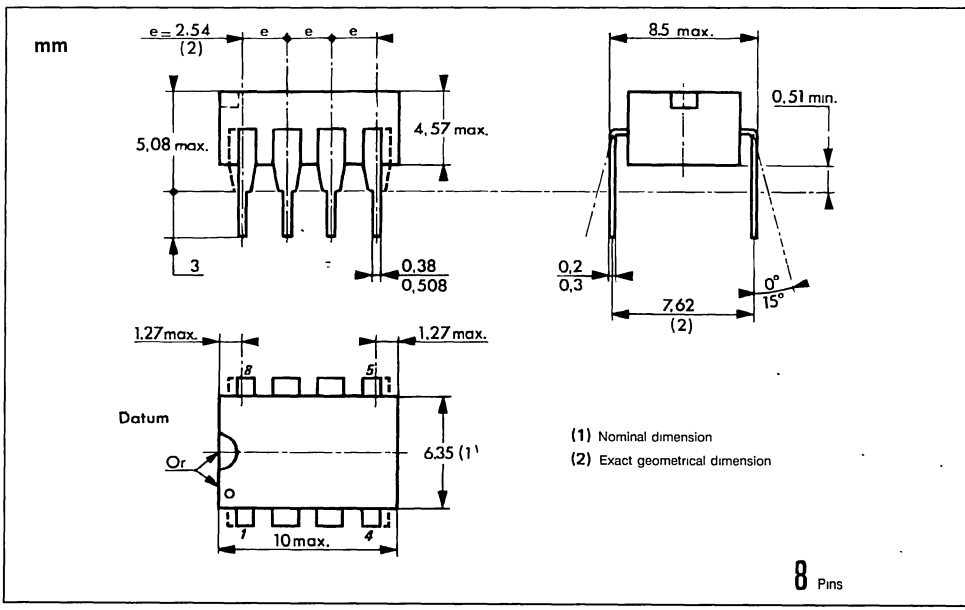


PACKAGE MECHANICAL DATA

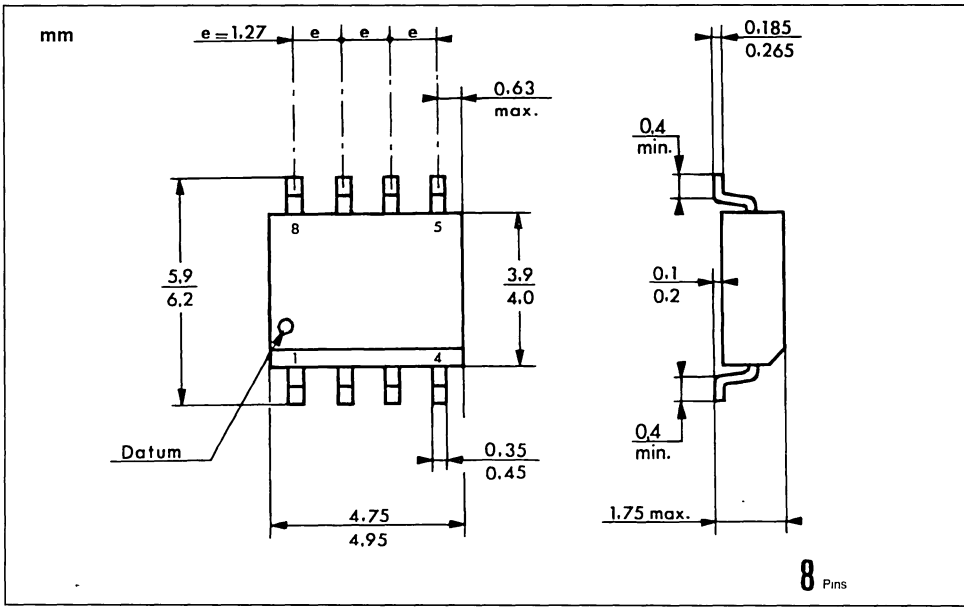
20 PINS – TRICECOP (LCC)



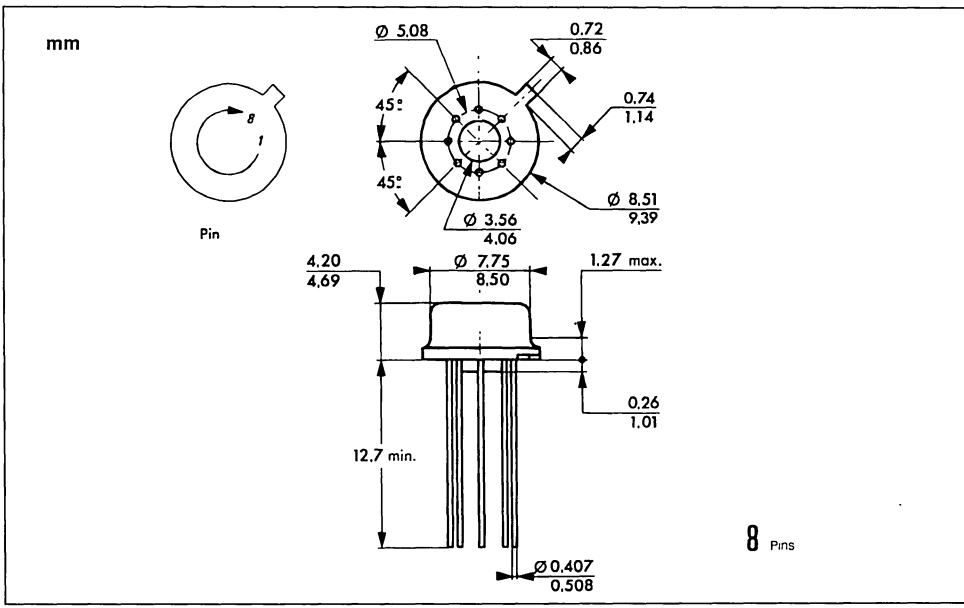
8 PINS – PLASTIC DIP



8 PINS – PLASTIC MICROPACKAGE (SO)



TO99 – METAL CAN



SGS-THOMSON MICROELECTRONICS

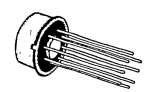
LF155
LF156-LF157

J–FET INPUT SINGLE OPERATIONAL AMPLIFIERS

- REPLACE HYBRID AND MODULE FET OP AMPs. RUGGED J-FETs ALLOW BLOW-OUT FREE HANDLING COMPARED WITH MOSFET INPUT DEVICES
- EXCELLENT FOR LOW NOISE APPLICATIONS USING EITHER HIGH OR LOW SOURCE IMPEDANCE VERY LOW I/F CORNER
- OFFSET VOLTAGE ADJUST DOES NOT DEGRADE DRIFT OR COMMON-MODE REJECTION AS IN MOST MONOLITHIC AMPLIFIERS
- NEW OUTPUT STAGE ALLOWS USE OF LARGE CAPACITIVE LOADS (10 000 pF) WITHOUT STABILITY PROBLEMS
- INTERNAL COMPENSATION AND LARGE DIFFERENTIAL INPUT VOLTAGE CAPABILITY

TYPICAL APPLICATIONS

- PRECISION HIGH SPEED INTEGRATORS
- FAST D/A AND A/D CONVERTERS
- HIGH IMPEDANCE BUFFERS
- WIDEBAND, LOW NOISE, LOW DRIFT AMPLIFIERS
- LOGARITHMIC AMPIFIERS
- PHOTOCELL AMPLIFIES
- SAMPLE AND HOLD CIRCUITS



H
TO-99
(Metal can)

N
DIP8
(Plastic package)

GC
LCC20
(Tricecop - LCC)

D
SO8
(Plastic micropackage)

DESCRIPTION

These circuits are monolithic J-FET input operational amplifiers incorporating well matched high voltage J-FETs on the same chip with standard bipolar transistors.
These amplifiers feature low input bias and offset currents, low input offset voltage and input offset voltage drift, coupled with offset adjust which does not degrade drift or common-jode rejection.
The devices are also designed for high, slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low I/f noise corner.

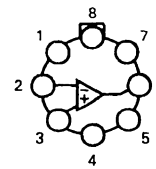
ORDER CODES

Part Number	Temperature Range	Package			
		N	D	H	GC
LF355,/LF356, LF357, LF255/LF256 LF257	0 °C to + 70 °C	•	•		
	– 40 °C to + 105 °C	•	•		
LF155/LF156 LF157	– 55 °C to + 125 °C	•		•	•

Note : Hi-Rel versions available
Examples : LF355 N, LF155 H

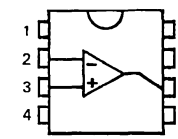
PIN CONNECTIONS (Top views)

TO-99



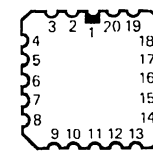
1 - Offset null
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-

DIP8
SO8



5 - Offset null
6 - Output
7 - V_{CC}^+
8 - NC

LCC20

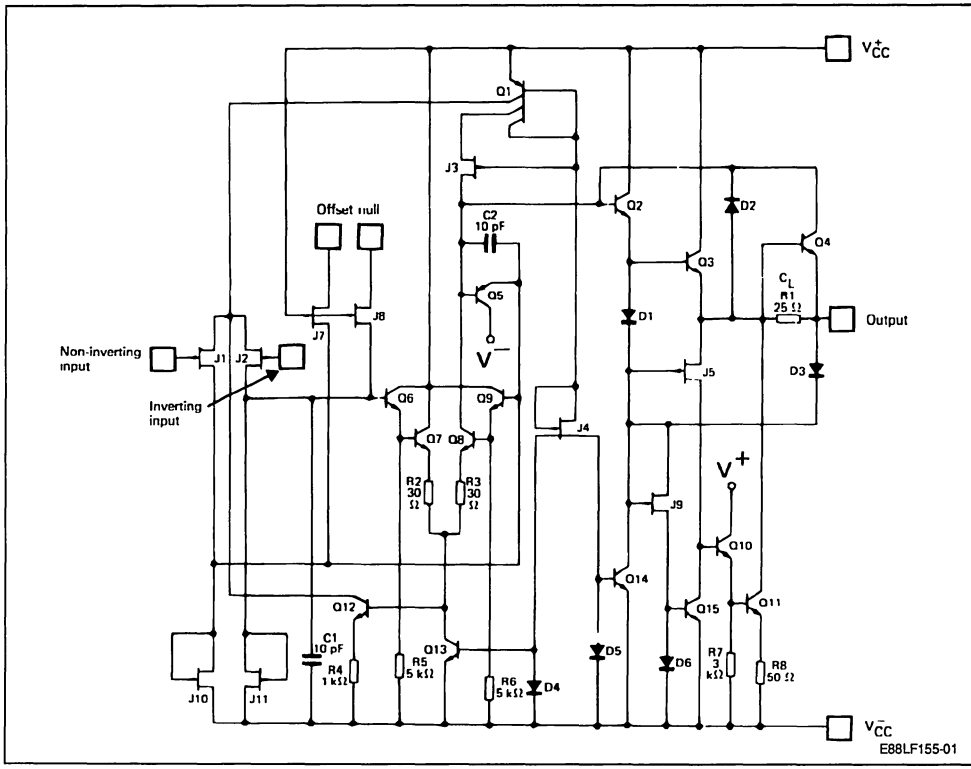


1 - NC
2 - Offset null
3 - NC
4 - NC
5 - Inverting input
6 - NC
7 - Non-inverting input
8 - NC
9 - NC
10 - V_{CC}^-
11 - NC
12 - Offset null
13 - NC
14 - NC
15 - Output
16 - NC
17 - V_{CC}^+
18 - NC
19 - NC
20 - NC

MAXIMUM RATINGS

Symbol	Parameter	LF355, A LF356, A LF357, A	LF255 LF256 LF257	LF155, A LF156, A LF157, A	Unit
V_{CC}	Supply Voltage	± 18	± 22	± 22	V
V_{ID}	Differential Input Voltage	± 30	± 40	± 40	V
V_I	Input Voltage (note 2)	± 16	± 20	± 20	V
	Output Short-circuit Duration	Continuous	Continuous	Continuous	
P_{tot}	Power Dissipation	500	570	670	mW
T_{oper}	Operating Free-air, Temperature Range	0 to + 70	− 40 to + 105	− 55 to + 125	°C
T_{stg}	Storage Temperature Range	− 65 to + 150	− 65 to + 150	− 65 to + 150	°C

SCHEMATIC DIAGRAM



Case	Offset Null	Inverting Input	Non-inverting Input	V_{CC}^-	V_{CC}^+	Output	N.C.
DIP8 SO8	1, 5	2	3	4	7	6	8
LCC20	2, 12	5	7	10	17	15	*

* **LCC20** : Other pins are not connected.

ELECTRICAL CHARACTERISTICS

LF155, LF156, LF157 : $-55\,°C \le T_{amb} \le +125\,°C$, $\pm 15V \le V_{CC} \le \pm 20V$ (note 3)
LF155A, LF156A, LF157A : $-55\,°C \le T_{amb} \le +125\,°C$, $\pm 15V \le V_{CC} \le \pm 20V$ (note 3)
LF255, LF256, LF257 : $-40\,°C \le T_{amb} \le +105\,°C$, $\pm 15V \le V_{CC} \le \pm 20V$ (note 3)
(Unless otherwise specified).

Symbol	Parameter	LF155, LF156, LF157 LF255, LF256, LF257			LF155A, 156A, 157A			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage (R_S = 50 Ω) T_{amb} = + 25 °C $T_{min} \le T_{amb} \le T_{max}$ LF155, LF156, LF157 LF255, LF256, LF257		3	5 7 6.5		1	2 2.5	mV
I_{IO}	Input Offset Current (note 5) T_j = + 25 °C $T_j \le T_{max}$ LF155, LF156, LF157 LF255, LF156, LF257		3	20 20 1		3	10 10	pA nA
I_{IB}	Input Bias Current (note 5) T_j = + 25 ° C $T_j \le T_{max}$ LF155, LF156, LF157 LF255, LF256, LF257		30	100 50 5		30	50 25	pA nA
A_{VD}	Large Signal Voltage Gain (V_{CC} = ± 15 V, V_{OPP} = ± 10 V, R_L = 20 KΩ) T_{amb} = + 25 °C $T_{min} \le T_{amb} \le T_{max}$	 50 25	 200		 50 25	 200		V/mV
SVR	Supply Voltage Rejection Ratio (note 6)	85	100		85	100		dB
I_{CC}	Supply Current (V_{CC} = ± 15 V, T_{amb} = + 25 °C) LF155, LF255 LF156, LF256 LF157, LF257		 2 5 5	 4 7 7		 2 5 5	 4 7 7	mA
αV_{ID}	Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω) - Note 4		5			3	5	µV/°C
$\alpha V_{IO}/V_{IO}$	Change in Average Temperature Coefficient with V_{IO} adjust R_S = 50 Ω		0.5			0.5		µV/°C per mV
V_I	Input Voltage Range (V_{CC} = ± 15 V)	± 11	± 15.1 − 12		± 11	± 15.1 − 12		V
CMR	Common-mode Rejection Ratio	85	100		85	100		dB
V_{OPP}	Output Voltage Swing (V_{CC} = ± 15 V) R_L = 10 KΩ R_L = 2 KΩ	 ± 12 ± 10	 ± 13 ± 12		 ± 12 ± 10	 ± 13 ± 12		V
GB_p	Gain-bandwidth Product (V_{CC} = + 15 V, T_{amb} = + 25 °C) LF155, LF255 LF156, LF256 LF157, LF257		2.5 5 20		 4 15	2.5 4.5 20		MHz
S_{VO}	Slew Rate (V_{CC} = ± 15 V, T_{amb} = + 25 °C) A_V = 1 LF155, LF255 LF156, LF256 A_V = 5 LF157, LF257	 7.5 30	5 12 50		3 10 40	5 12 50		V/µs
R_I	Input Resistance (T_j = + 25 °C)		10^{12}			10^{12}		Ω
C_I	Input Capacitance (V_{CC} = ±15 V, T_{amb} = + 25 °C)		3			3		pF
V_n	Equivalent Input Noise Voltage (V_{CC} = ± 15 V, T_{amb} = + 25°C, R_S = 100 Ω) f = 1000 Hz LF155 LF255 LF156, LF157 LF256, LF257 f = 100 Hz LF155 LF255 LF156, LF157 LF256, LF257		 25 20 12 15 20 25 12 15			 20 15 25 15		nV/√Hz
I_n	Equivalent Input Noise Current (V_{CC} = ± 15 V, T_{amb} = + 25 °C, f = 100 Hz or f = 1000 Hz)		0.01			0.01		pA/√Hz
t_s	Settling Time (V_{CC} = ± 15 V, T_{amb} = + 25 °C) - Note 7 LF155, LF255 LF156, LF256 LF157, LF257		 4			 1.5 4		1.5

ELECTRICAL CHARACTERISTICS

LF355, LF356, LF357 : $0\ ^\circ C \le T_{amb} \le +70\ ^\circ C$, $V_{CC} = \pm 15V$
LF355A, LF356A, LF357A : $0\ ^\circ C \le T_{amb} \le +70\ ^\circ C$, $\pm 15V \le V_{CC} \le \pm 18V$ (note 3)
(Unless otherwise specified).

Symbol	Parameter	LF355, LF356, LF357			LF355A, 356A, 357A			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage (R_S = 50 Ω) T_{amb} = + 25 °C $T_{min} \le T_{amb} \le T_{max}$		3	10 13		1	2 2.3	mV
I_{IO}	Input Offset Current (note 5) T_j = + 25 °C $T_j \le$ + 70 °C		3	50 2		3	10 1	pA nA
I_{IB}	Input Bias Current (note 5) T_j = + 25 °C T_j = + 70 °C		30	200 8		30	50 5	pA nA
A_{VD}	Large Signal Voltage Gain (V_{CC} = ± 15 V, V_{OPP} = ± 10 V, R_L = 2 KΩ) T_{amb} = + 25 °C $T_{min} \le T_{amb} \le T_{max}$	 25 15	 200		 50 25	 200		V/mV
SVR	Supply Voltage Rejection Ratio (note 6)	80	100		85	100		dB
I_{CC}	Supply Current (V_{CC} = ± 15 V, T_{amb} = + 25 °C) LF355 LF356, LF357		2 5	4 10		2 5	4 10	mA
αV_{IO}	Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω) - Note 4		5			3	5	µV/°C
$\alpha V_{IO}/V_{IO}$	Change in Average Temperature Coefficient with V_{IO} Adjust R_S = 50 Ω		0.5			0.5		µV/°C per mV
V_I	Input Voltage Range (V_{CC} = ± 15 V)	± 10	± 15.1 − 12		± 11	± 15.1 − 12		V
CMR	Common-mode Rejection Ratio	85	100		85	100		dB
V_{OPP}	Output Voltage Swing (V_{CC} = ± 15 V) R_L = 10 KΩ R_L = 2 KΩ	 ± 12 ± 10	 ± 13 ± 12		 ± 12 ± 10	 ± 13 ± 12		V
GB_p	Gain-bandwidth Product (V_{CC} = ± 15 V, T_{amb} = + 25 °C) LF355 LF356 LF357		 2.5 5 20		 4 15	 2.5 4.5 20		MHz
S_{VO}	Slew Rate (V_{CC} = ± 15 V, T_{amb} = + 25 °C) A_V = 1 LF355 LF356 A_V = 5 LF357		 5 12 50		 3 10 40	 5 12 50		V/µs
R_I	Input Resistance (T_j = + 25 °C)		10^{12}			10^{12}		Ω
C_I	Input Capacitance (V_{CC} = ± 15 V, T_{amb} = + 25 °C)		3			3		pF
V_n	Equivalent Input Noise Voltage (V_{CC} = ± 15 V, T_{amb} = + 25 °C, R_S = 100Ω) f = 1000 Hz LF355 LF356, LF357 f = 100 Hz LF355 LF356, LF357		 20 12 25 15			 20 12 25 15		nV/√Hz
I_n	Equivalent Input Noise Current (V_{CC} = ± 15 V, T_{amb} = + 25 °C, f = 100 Hz or f = 1000 Hz)		0.01			0.01		pA/√Hz
t_s	Settling Time (V_{CC} = ± 15 V , T_{amb} = + 25 °C) Note 7 LF355 LF356, LF357		 4 1.5			 4 1.5		µs

Notes : 1. The CB package must be derated based on a thermal resistance of 150 °C/W junction ambient or 45 °C/W junction to case ; for the DIP package, the device must be derated based on thermal resistance of 175 °C/W junction to ambient.
2. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
3. For the LF155, A, LF156, A, LF157, A these specifications apply for $\pm 15 \le V_{CC} \le \pm 20$ V, $-55\ ^\circ C \le T_{amb} \le +125\ ^\circ C$ and $T_{high} = +125\ ^\circ C$ unless otherwise stated.
For the LF255, A, LF256, A, LF257, A these specifications apply for ± 15 V $\le V_{CC} \le \pm 20$ V, $-40\ ^\circ C \le T_{amb} \le +105\ ^\circ C$ and $T_{high} = +105\ ^\circ C$ unless otherwise stated.
For the LF355, A, LF356, A, LF357, A these specifications apply for ± 15 V $\le VCC \le \pm 20$ V, $0\ ^\circ C \le T_{amb} \le +70\ ^\circ C$ and $T_{high} = +70\ ^\circ C$, unless otherwise stated.

Notes : 4. The temperature coefficient of the adjusted input offset voltage changes only a small amount (0.5 µV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

5. The input bias currents are junction leakage currents which approximately double for every 10 °C increase in the junction temperature T_j Due to limited production test time, the input bias current measured is correlated to junction temperature.
In a normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, $Ptot \cdot T_j = T_{amb} + R_{th(j-a)} \times P_{tot}$ where $R_{th(j-a)}$ is the thermal resistance from junction to ambient Use of a heatsink is recommended if input currents are to be kept to a minimum.

6. Supply voltage rejection is measured for both supply magnitudes increasing or decreasing simultaneous, in accordance with common practice.

7. Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155, LF156 series. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01 % of its final value from the time a 10 V step input is applied to the inverter. For the LF157 series $A_V = -5$, the feedback resistor from output to input is 2 kΩ and the output step is 10 V.

APPLICATION HINTS

The LF155, LF156, LF157 series are op amps with J-FET input devices. These JFETs have large reverse breakdown voltages from gate to source or drain eliminating the need of clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase of input currents. The maximum differential input voltage is independent of the supply voltage. However, neither of the negative input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive suplly can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently metalled backwards in a socket as an unilimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

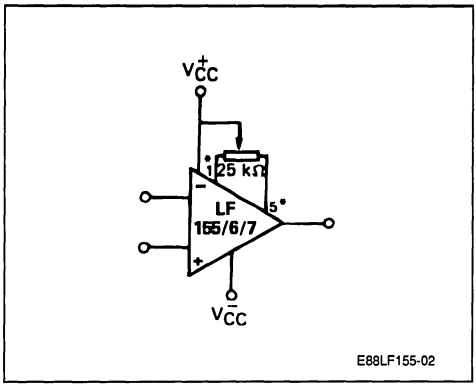
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltages.

As with most amplifiers, care should be taken with lead dress, components placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimiz "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six time the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of that added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

TYPICAL CIRCUITS

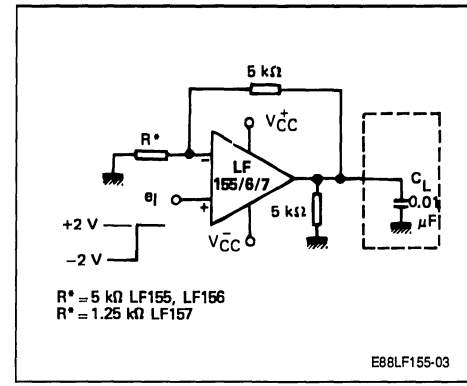
V_{IO} ADJUSTMENT



V_{IO} is adjusted with a 25 kΩ potentiometer. The potentiometer wiper is connected to V_{CC}^+.

* CB-11, CB-98 pin configuration.

DRIVING CAPACITIVE LOADS



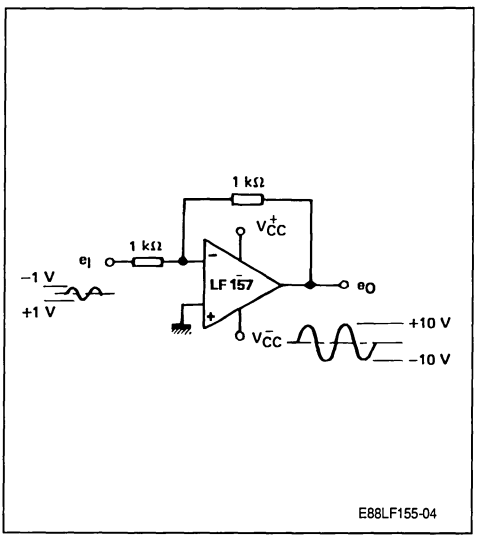
Due to a unique output stage design these amplifiers have the ability to drive large capacitive loads ans still maintain stability.

$C_{L(max)} = 0.01\ \mu F$

Overshoot ≤ 20%

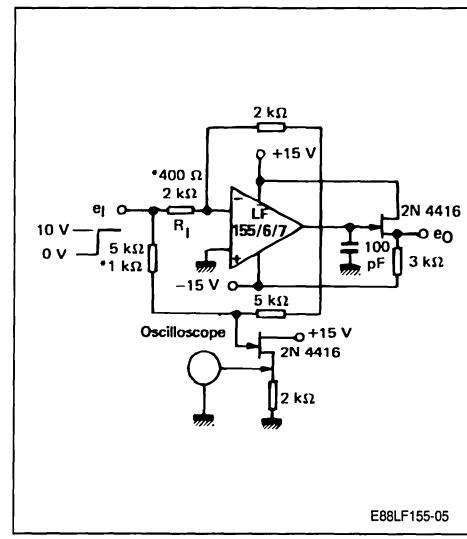
Settling time (t_s) = 5 µs

LARGE POWER BW AMPLIFIER



For distortion < 1% and a 20 V_{PP} V_O swing, power bandwidth is : 500 kHz.

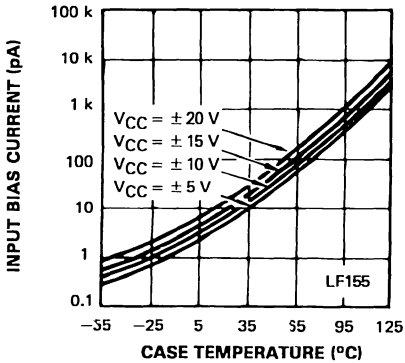
SETTLING TIME TEST CIRCUIT



Settling time is tested with the LF155, LF156 connected as unity gain converter R_I = 2 kΩ and LF157 connected for $A_V = -5$, R_I = 0.4 kΩ.

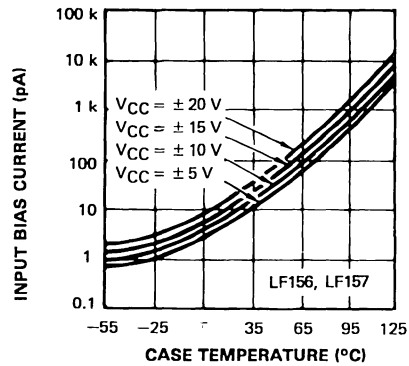
TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT



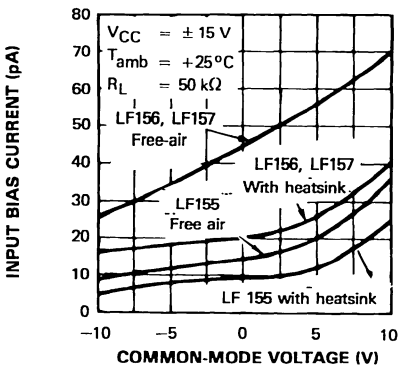
E88LF155-06

INPUT BIAS CURRENT



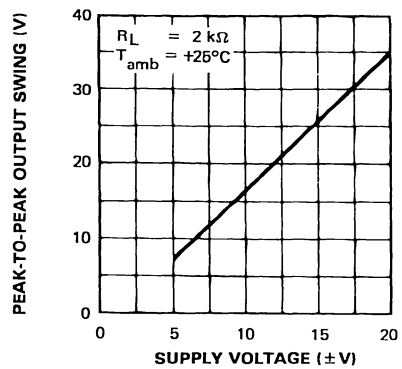
E88LF155-07

INPUT BIAS CURRENT



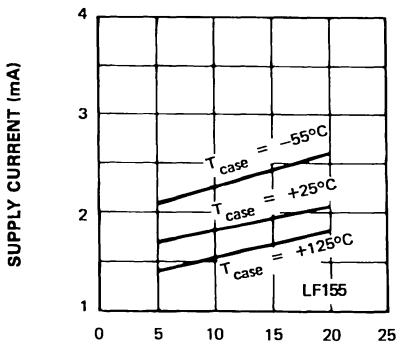
E88LF155-08

VOLTAGE SWING



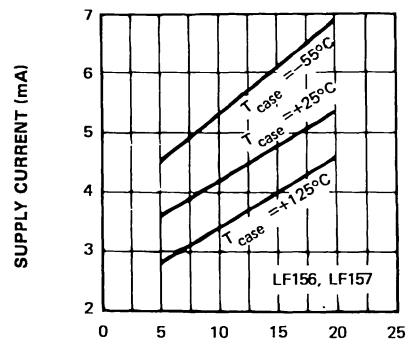
E88LF155-09

SUPPLY CURRENT



E88LF155-10

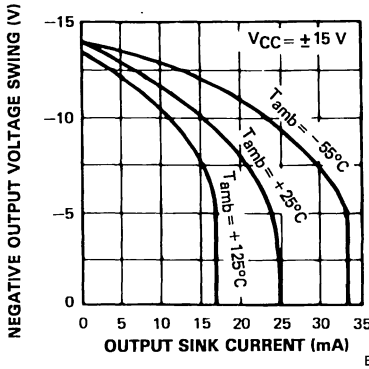
SUPPLY CURRENT



E88LF155-11

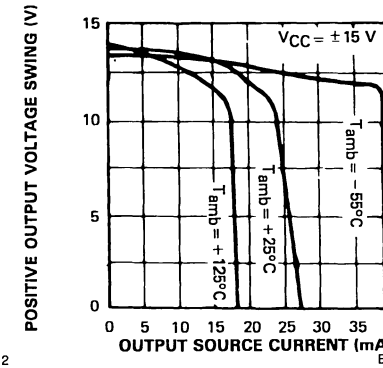
TYPICAL CHARACTERISTICS (continued)

MAXIMUM NEGATIVE CURRENT



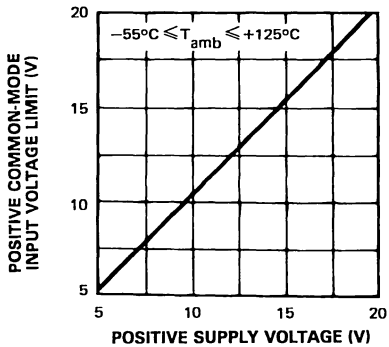
E88LF155-12

MAXIMUM POSITIVE CURRENT



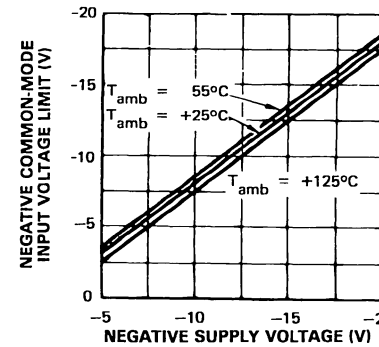
E88LF155-13

MAXIMUM POSITIVE COMMON-MODE INPUT VOLTAGE



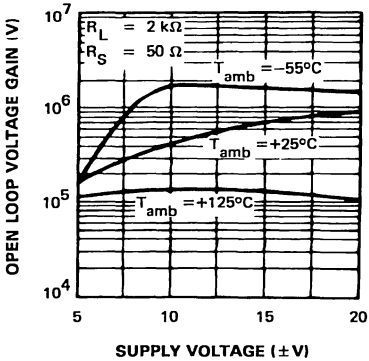
E88LF155-14

MAXIMUM NEGATIVE COMMON-MODE INPUT VOLTAGE



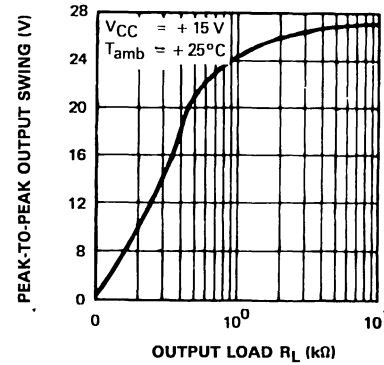
E88LF155-15

OPEN LOOP VOLTAGE GAIN



E88LF155-16

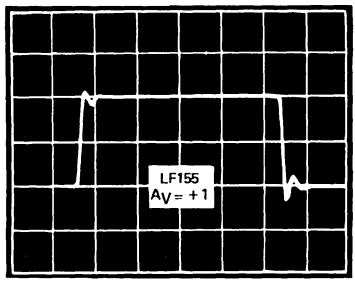
OUTPUT VOLTAGE SWING



E88LF155-17

TYPICAL CHARACTERISTICS (continued)

SMALL SIGNAL PULSE RESPONSE

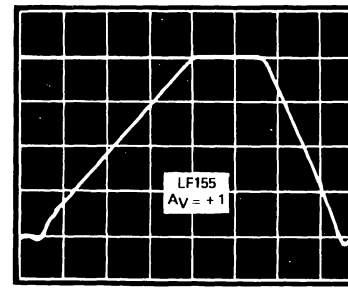


OUTPUT VOLTAGE SWING (60 mV/DIV)

TIME (0.5 μs/DIV)

E88LF155-18

LARGE SIGNAL PULSE RESPONSE

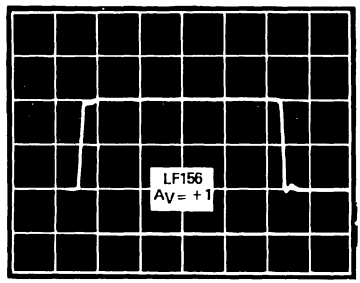


OUTPUT VOLTAGE SWING (5 V/DIV)

TIME (1 μs/DIV)

E88LF155-19

SMALL SIGNAL PULSE RESPONSE

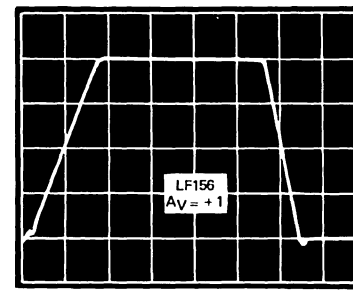


OUTPUT VOLTAGE SWING (60 mV/DIV)

TIME (0.5 μs/DIV)

E88LF155-20

LARGE SIGNAL PULSE RESPONSE

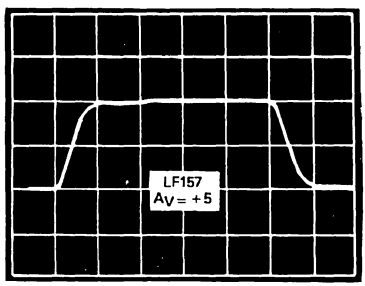


OUTPUT VOLTAGE SWING (5 V/DIV)

TIME (1 μs/DIV)

E88LF155-21

SMALL SIGNAL PULSE RESPONSE

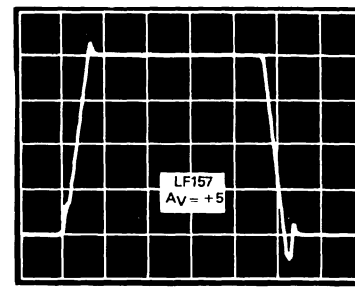


OUTPUT VOLTAGE SWING (50 mV/DIV)

TIME (0.1 μs/DIV)

E88LF155-22

LARGE SIGNAL PULSE RESPONSE



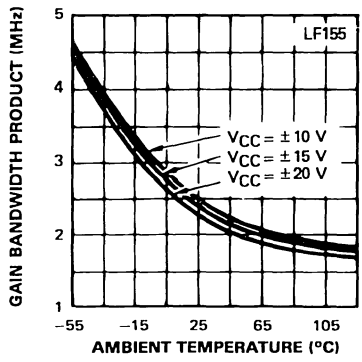
OUTPUT VOLTAGE SWING (5 V/DIV)

TIME (0.5 μs/DIV)

E88LF155-23

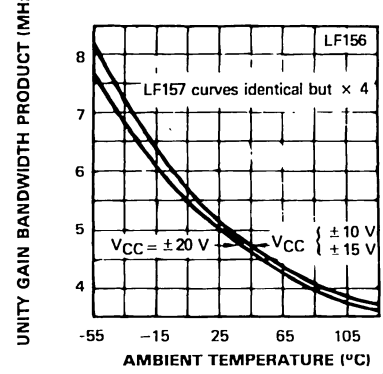
TYPICAL CHARACTERISTICS (continued)

GAIN BANDWIDTH PRODUCT



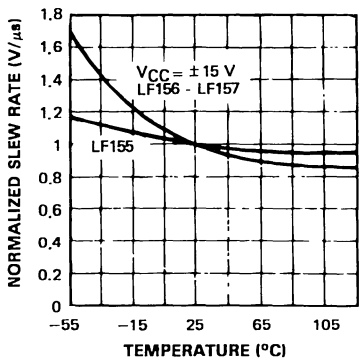
E88LF155-24

GAIN BANDWIDTH PRODUCT



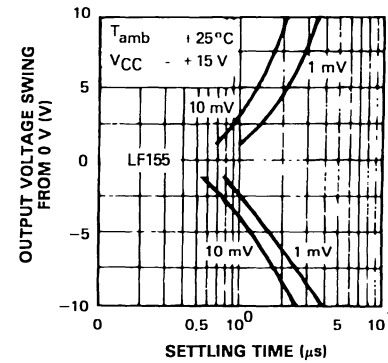
E88LF155-25

NORMALIZED SLEW RATE



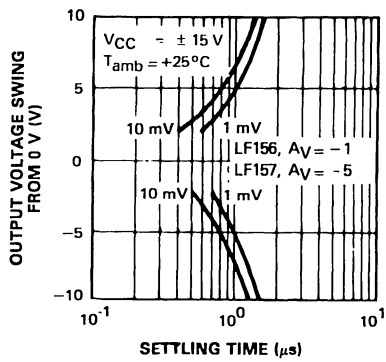
E88LF155-26

INVERTER SETTLING TIME



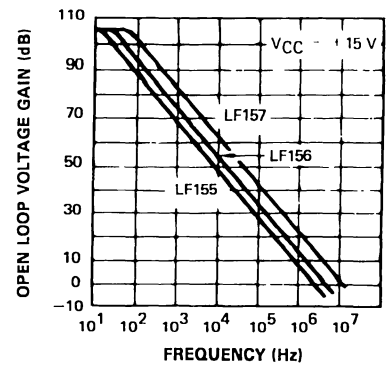
E88LF155-27

INVERTER SETTLING TIME



E88LF155-28

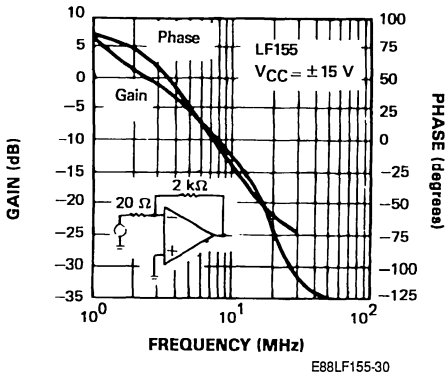
OPEN LOOP FREQUENCY RESPONSE



E88LF155-29

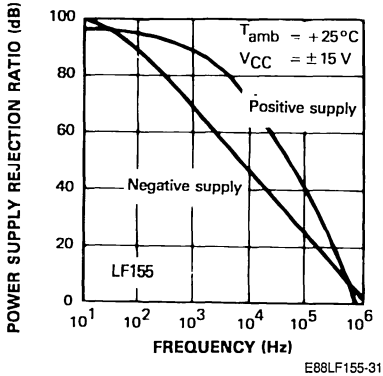
TYPICAL CHARACTERISTICS (continued)

BODE PLOT



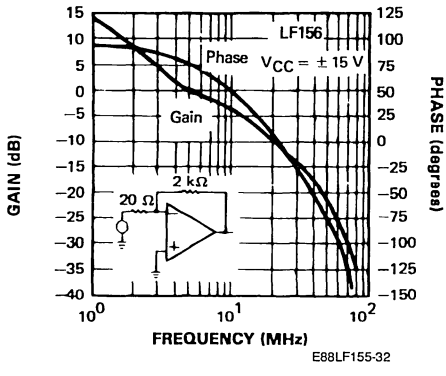
E88LF155-30

POWER SUPPLY REJECTION RATIO



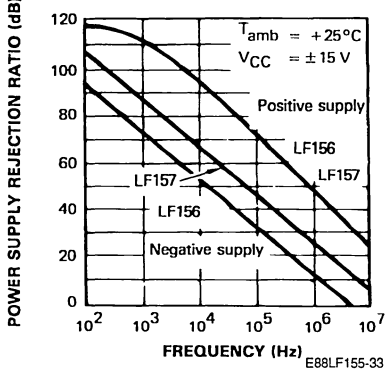
E88LF155-31

BODE PLOT



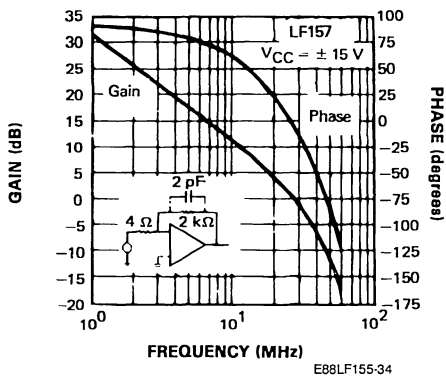
E88LF155-32

POWER SUPPLY REJECTION RATIO



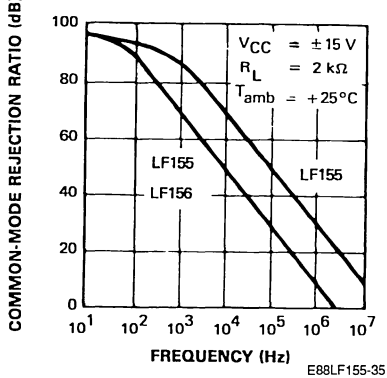
E88LF155-33

BODE PLOT



E88LF155-34

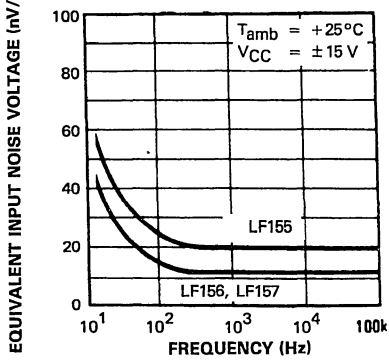
COMMON-MODE REJECTION RATIO



E88LF155-35

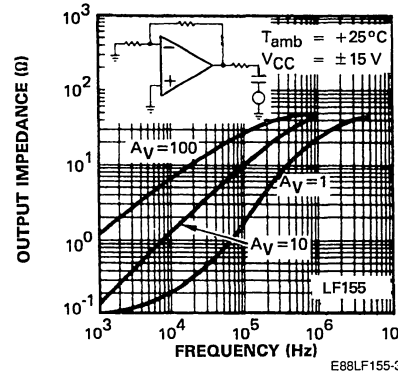
TYPICAL CHARACTERISTICS (continued)

EQUIVALENT INPUT NOISE VOLTAGE (EXPANDED SCALE)



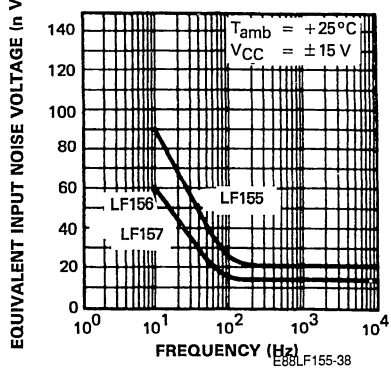
E88LF155-36

OUTPUT IMPEDANCE



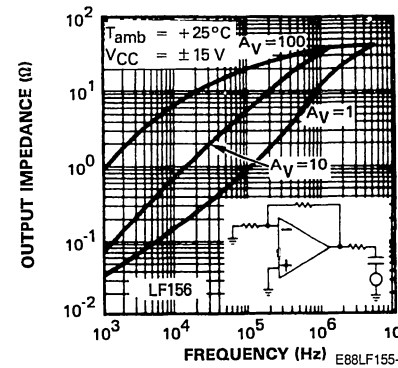
E88LF155-37

EQUIVALENT INPUT NOISE VOLTAGE



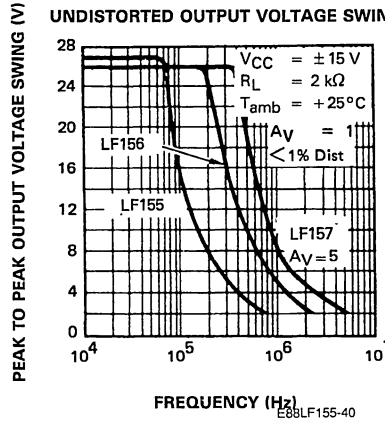
E88LF155-38

OUTPUT IMPEDANCE



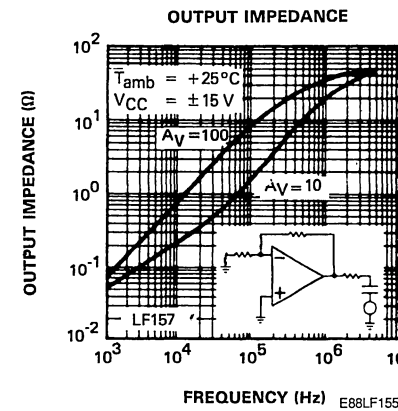
E88LF155-39

UNDISTORTED OUTPUT VOLTAGE SWING



E88LF155-40

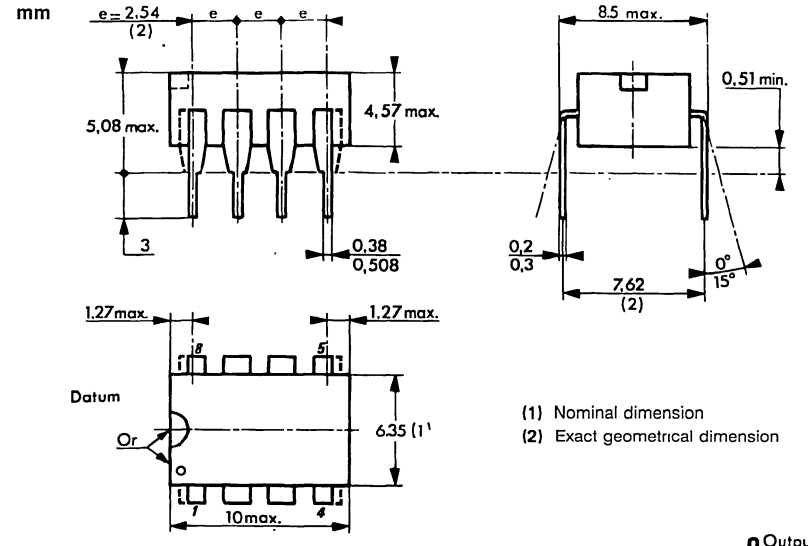
OUTPUT IMPEDANCE



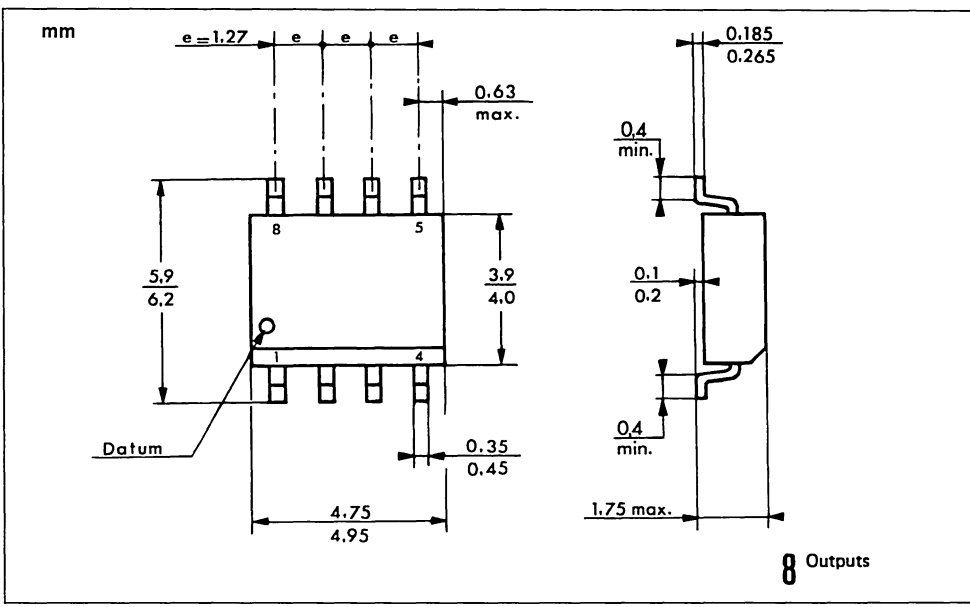
E88LF155-41

PACKAGE MECHANICAL DATA

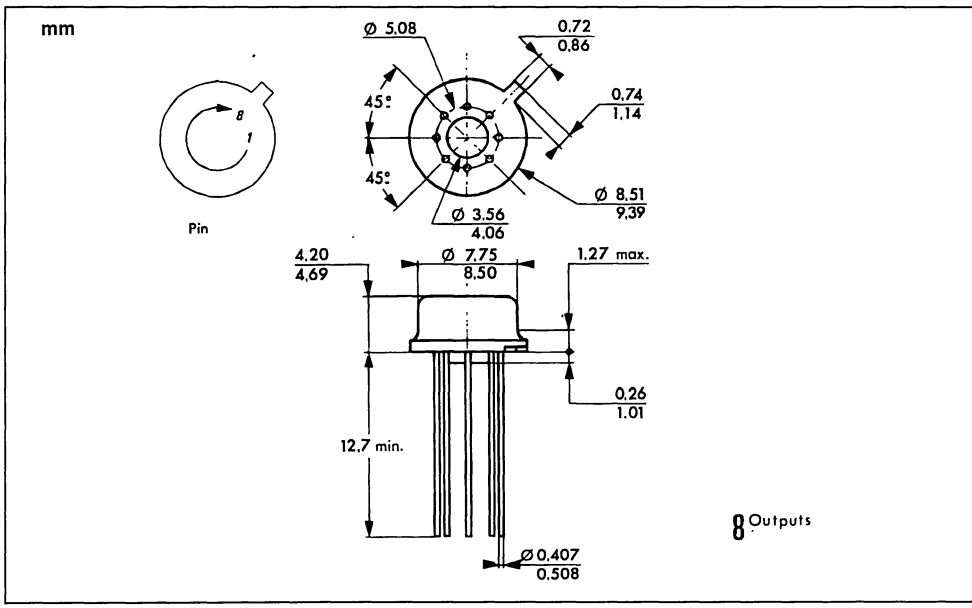
8 PINS – PLASTIC DIP



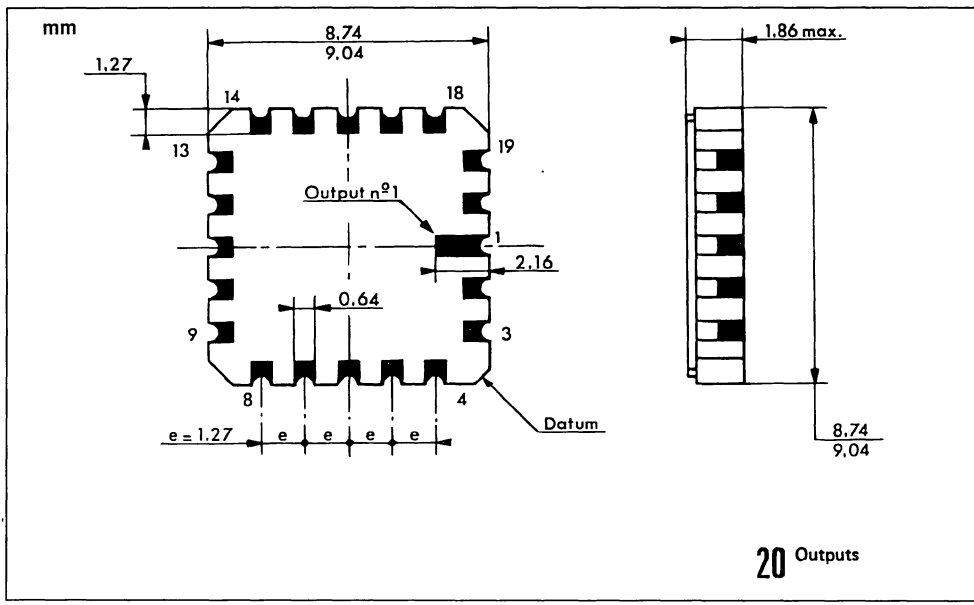
8 PINS – PLASTIC MICROPACKAGE (SO)



T0-99 – METAL CAN



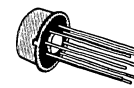
20 PINS – TRICECOP (LCC)



LM101A-LM201A LM301A

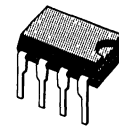
SINGLE OPERATIONAL AMPLIFIERS

	LM101A LM201A	LM301A
■ INPUT OFFSET VOLTAGE	0.2 mV	2 mV
■ INPUT BIAS CURRENT	25 nA	70 nA
■ INPUT OFFSET CURRENT	1.5 nA	2 nA
■ SLEW RATE AS INVERTING AMPLIFIER	10 V/µs	10 V/µs



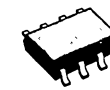
H
TO99
(Metal Can)

GC
LCC20
(Tricecop (LCC))



N
DIP8
(Plastic Package)

J
CERDIP8
(Cerdip Package)



D
SO8
(Plastic Micropackage)

DESCRIPTION

The LM101A is a general-purpose operational amplifier. This amplifier offers many features : supply voltages from ± 5 V to ± 20 V, low current drain, overload protection on the input and output, no latch-up when the common-mode range is exceeded, freedom from oscillations and compensation with a single 30 pF capacitor. It has advantages over internally compensated amplifiers in that the compensation can be tailored to the particular application : slew rates of 10 V/µs and bandwidths of 3.5 MHz can be easily achieved. In addition, the circuit can be used as a comparator with differential inputs up to ± 30 V. The output can be clamped at any desired level to make it compatible with logic circuits.

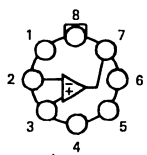
ORDER CODES

Part Number	Temperature Range	Package				
		H	N	J	GC	D
LM101A	– 55 to + 125 °C	•		•	•	
LM201A	– 40 to + 105 °C	•	•	•		
LM301A	0 to + 70 °C	•	•	•		•

Note : Hi-Rel Versions Available
Examples : LM101AH, LM201AN

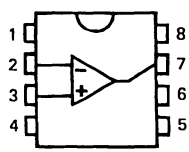
PIN CONNECTIONS (top views)

TO99



1 - Balance compensation 1
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}

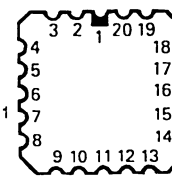
DIP8/CERDIP8
SO8



5 - Balance
6 - Output
7 - V_{CC}
8 - Compensation 2

1 - NC
2 - Balance compensation 1
3 - NC
4 - NC
5 - Inverting input
6 - NC
7 - Non-inverting input
8 - NC
9 - NC
10 - V_{CC}

LCC20



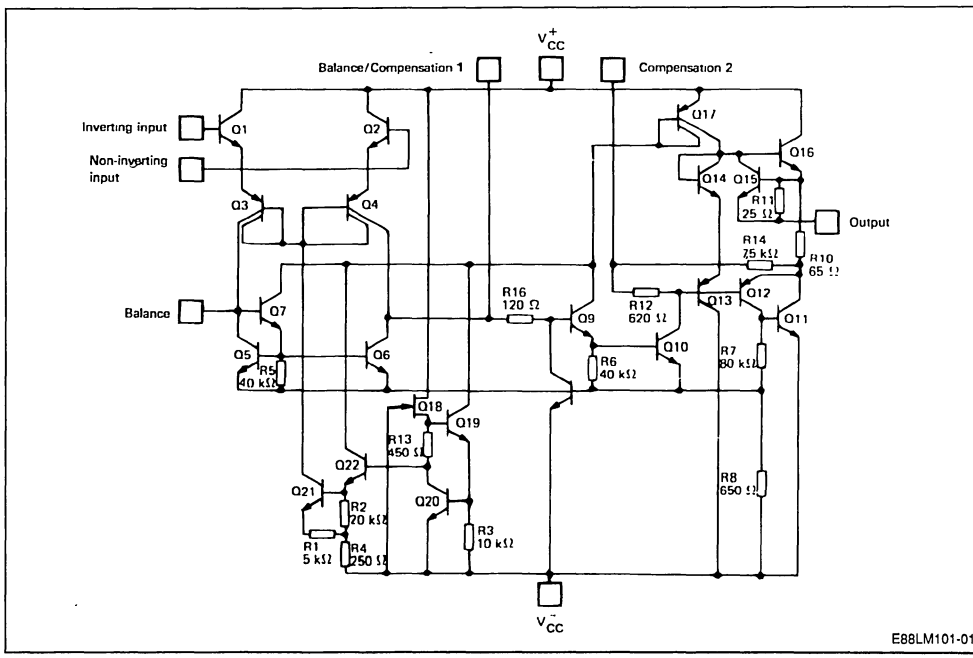
E88LM101-33

11 - NC
12 - Balance
13 - NC
14 - NC
15 - Output
16 - NC
17 - V_{CC}
18 - NC
19 - NC
20 - Compensation 2

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value			Unit
			LM101A	LM201A	LM301A	
V_{CC}	Supply Voltage		± 22	± 22	± 22	V
V_{ID}	Differential Input Voltage		± 30	± 30	± 30	V
V_I	Input Voltage		± 15	± 15	± 15	V
	Output Short-circuit Duration		Indefinite for T_{amb} = + 70 °C		Indefinite for T_{amb} = +55 °C	
P_{tot}	Power Dissipation	N.J.H. Suffix	500	500	500	mW
		GC Suffix	665			
		D Suffix		300	300	
T_{oper}	Operating Free-air Temperature Range		– 55 to + 125	– 40 to + 105	0 to + 70	°C
T_{stg}	Storage Temperature Range		– 65 to + 150	– 65 to + 150	– 65 to + 150	°C

SCHEMATIC DIAGRAM



Case	Balance/ Comp. 1	Inverting Input	Non-Inverting Input	$V_{\bar{C}C}$	$V_{\bar{C}C}$	Output	Balance	Comp. 2
TO99	1	2	3	4	7	6	5	8
DIP8 CERDIP8 SO8	1	2	3	4	7	6	5	8
LCC20*	2	5	7	10	17	15	12	20

* **LCC20 :** Other pins not connected.

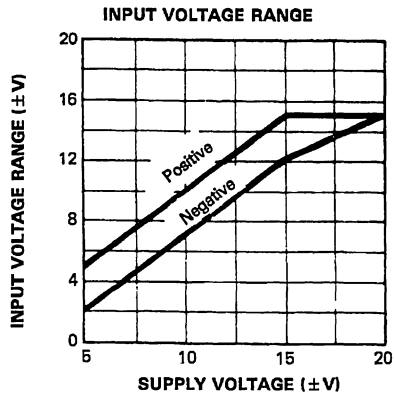
ELECTRICAL CHARACTERISTICS

LM301A : $0\,°C < T_{amb} < +\ 70\,°C, \pm 5\ V \leq V_{CC} \leq \pm 20\ V$, C1 = 30 pF
LM201A : $-40\,°C < T_{amb} < +\ 105\,°C, \pm 5\ V \leq V_{CC} \leq \pm 20\ V$, C1 = 30 pF
LM101A : $-55\,°C < T_{amb} < +\ 125\,°C, \pm 5\ V \leq V_{CC} \leq \pm 20\ V$, C1 = 30 pF
* => $V_{CC} = \pm 15\ V$
(unless otherwise specified)

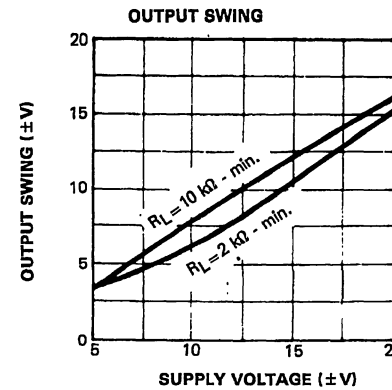
Symbol	Parameter	LM101A/LM201A			LM301A			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage ($R_S \leq 10\ k\Omega$) $T_{amb} = 25\,°C$ $T_{min} \leq T_{amb} \leq T_{max}$		0.2	1 3		2	5 6	mV
I_{IB}	Input Bias Current $T_{amb} = 25\,°C$ $T_{min} \leq T_{amb} \leq T_{max}$		25	75 100		70	100 200	nA
I_{IO}	Input Offset Current $T_{amb} = 25\,°C$ $T_{min} \leq T_{amb} \leq T_{max}$		1.5	10 20		2	20 40	nA
A_{VD}	Large Signal Voltage Gain * ($V_O = \pm\ 10\ V$, $R_L = 2\ k\Omega$) $T_{amb} = 25\,°C$ $T_{min} \leq T_{amb} \leq T_{max}$	 50 25	 100		 50 25	 100		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S \leq 10\ k\Omega$) $T_{amb} = 25\,°C$ $T_{min} \leq T_{amb} \leq T_{max}$	 80 80	 96		 80 80	 96		dB
I_{CC}	Supply Current no Load $T_{amb} = 25\,°C$ $T_{min} \leq T_{amb} \leq T_{max}$		1.8	3 3		1.8	3 3	mA
V_I	Input Voltage Range ($V_{CC} = \pm\ 20\ V$) $T_{amb} = 25\,°C$ $T_{min} \leq T_{amb} \leq T_{max}$	 − 15 − 15		 + 15 + 15	 − 15 − 15		 + 15 + 15	V
CMR	Common Mode Rejection Ratio ($R_S \leq 10\ k\Omega$) $T_{amb} = 25\,°C$ $T_{min} \leq T_{amb} \leq T_{max}$	 80 80	 96		 80 80	 96		dB
I_{OS}	Output Short-circuit Current * $T_{amb} = 25\,°C$	 10	 30	 50	 10	 30	 50	mA
$\pm V_{OPP}$	Output Voltage Swing * $T_{amb} = 25\,°C$ $R_L = 10\ k\Omega$ $R_L = 2\ k\Omega$ $T_{min} < T_{amb} < T_{max}$ $R_L = 10\ k\Omega$ $R_L = 2\ k\Omega$	 12 10 12 10	 14 13		 12 10 12 10	 14 13		V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	LM101A/LM201A			LM301A			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
S_{VO}	Slew Rate (V_I = ± 10 V, R_L = 2 kΩ, C_L < 100 pF, T_{amb} = 25 °C, unity gain) * (note 1)	0.25	0.5		0.25	0.5		V/µs
t_r	Rise Time (V_I = ± 20 mV, R_L = 2 kΩ, C_L ≤ 100 pF, T_{amb} = 25 °C, unity gain) *		0.3			0.3		µs
K_{OV}	Overshoot (V_I = 20 mV, R_L = 2 kΩ, C_L ≤ 100 pF, T_{amb} = 25 °C, unity gain)		5			5		%
Z_I	Input Impedance, T_{amb} = 25 °C *	1.5	4		1.5	4		MΩ
R_O	Output Resistance, T_{amb} = 25 °C *		75			75		Ω
GBP	Gain Bandwidth Product * (V_I = 10 mV, R_L = 2 KΩ, C_L ≤ 100 pF, f = 100 kHz, T_{amb} = 25 °C)	0.5	1	1.6	0.5	1	1.6	MHz
THD	Total Harmonic Distortion * (f = 1 kHz, A_V = 20 dB, R_L = 2 kΩ, V_O = 2 V_{PP} C_L ≤ 100 pF, T_{amb} = 25 °C)		0.015			0.015		%
V_n	Equivalent Input Noise Voltage (f = 1 kHz, R_g = 100 Ω) *		25			25		nV/√Hz
DV_{IO}	Input Offset Voltage Drift T_{min} ≤ T_{amb} ≤ T_{max}		3	15		6	30	µV/°C
DI_{IO}	Input Offset Current Drift 25 °C ≤ T_{amb} ≤ T_{max} T_{min} ≤ T_{amb} ≤ 25 °C		10 20	100 200		10 20	100 200	pA/°C

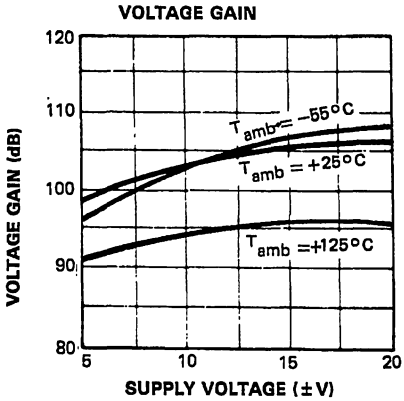


E88LM101-02

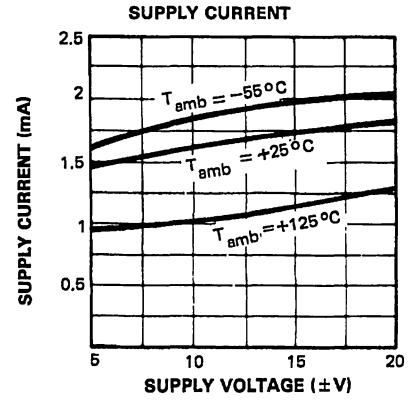


E88LM101-03

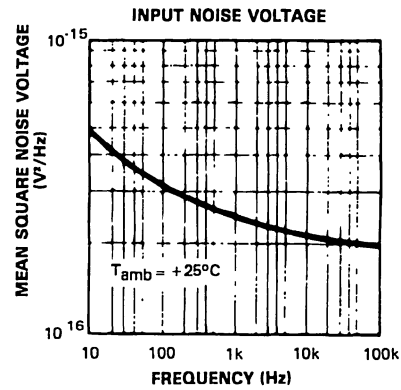
Note : 1. May be improved up to 10V/µs in inverting amplifier configuration (see basic diagram).



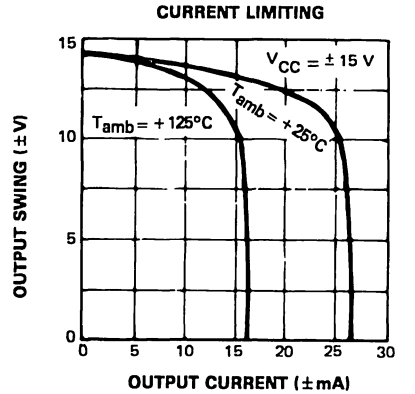
E88LM101-04



E88LM101-05

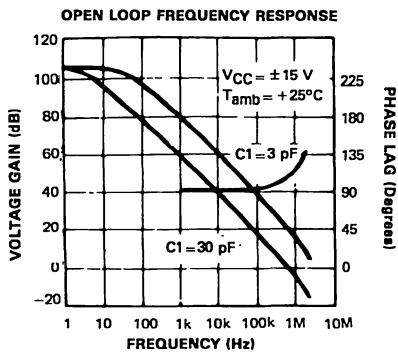


E88LM101-06



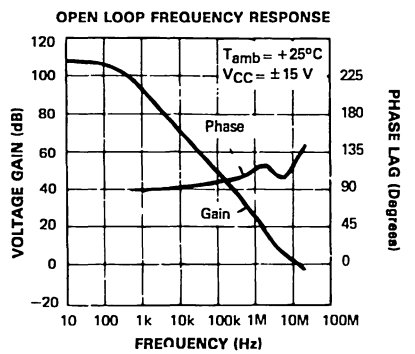
E88LM101-07

SINGLE POLE COMPENSATION



E88LM101-08

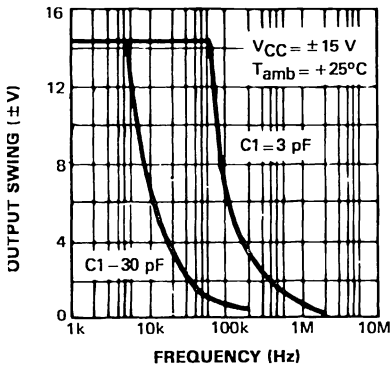
FEED FORWARD COMPENSATION



E88LM101-09

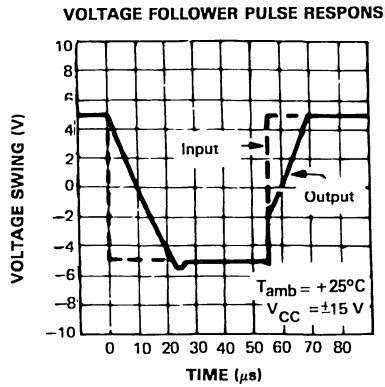
SINGLE POLE COMPENSATION

LARGE SIGNAL FREQUENCY RESPONSE



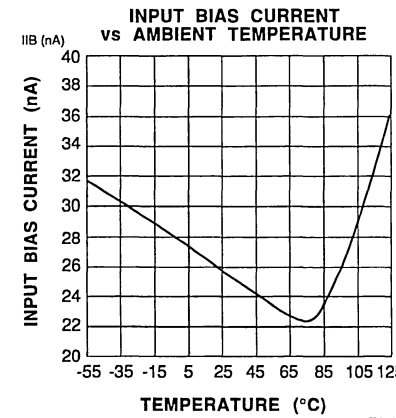
E88LM101-10

VOLTAGE FOLLOWER PULSE RESPONSE



E88LM101-12

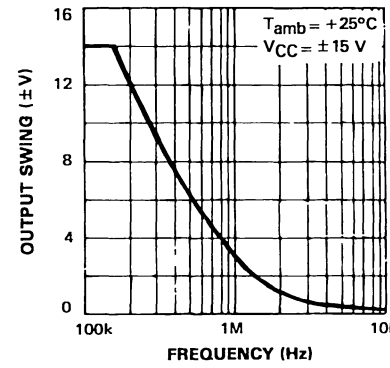
INPUT BIAS CURRENT VS AMBIENT TEMPERATURE



E88LM101-14

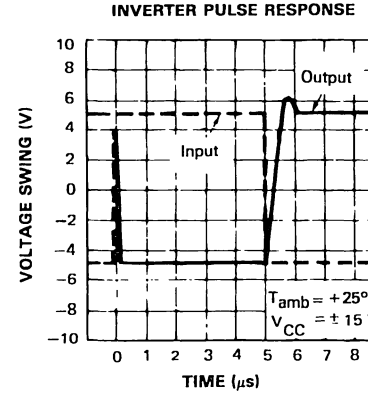
FEED FORWARD COMPENSATION

LARGE SIGNAL FREQUENCY RESPONSE



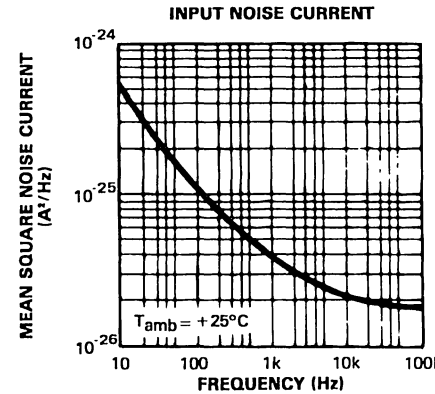
E88LM101-11

INVERTER PULSE RESPONSE



E88LM101-13

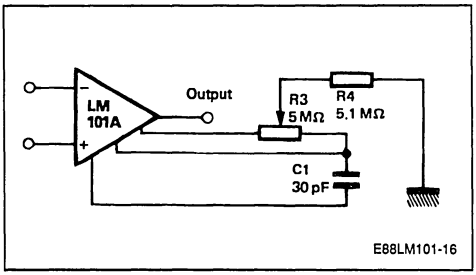
INPUT NOISE CURRENT



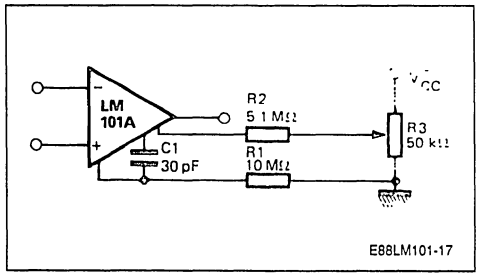
E88LM101-15

BASIC DIAGRAMS

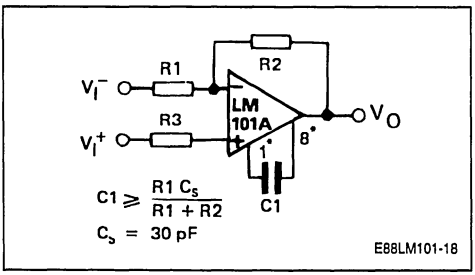
BALANCING CIRCUIT



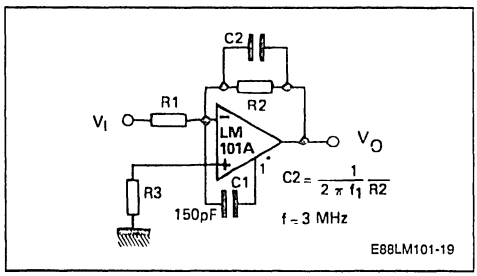
ALTERNATE BALANCING CIRCUIT



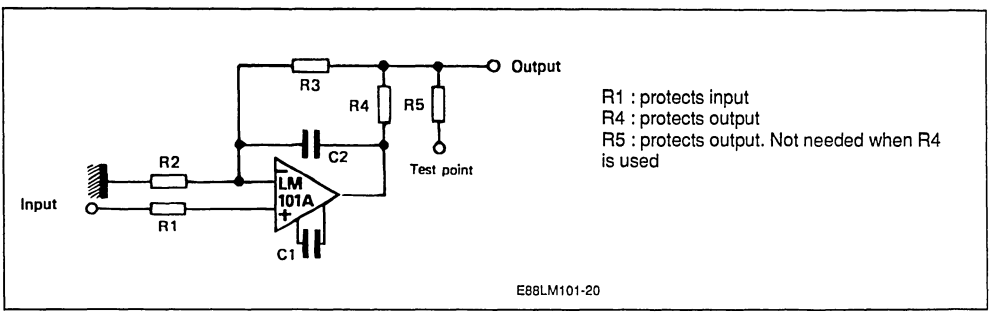
SINGLE POLE COMPENSATION



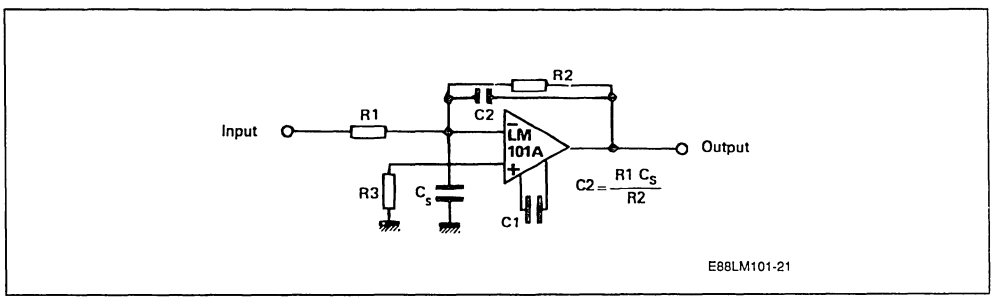
FEEDFORWARD COMPENSATION



PROTECTING AGAINST GROSS FAULT CONDITIONS

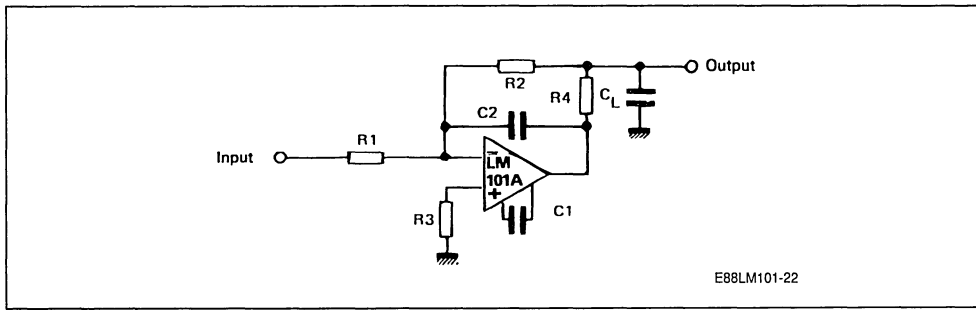


COMPENSATING FOR STRAY INPUT CAPACITANCES OR LARGE FEEDBACK RESISTOR

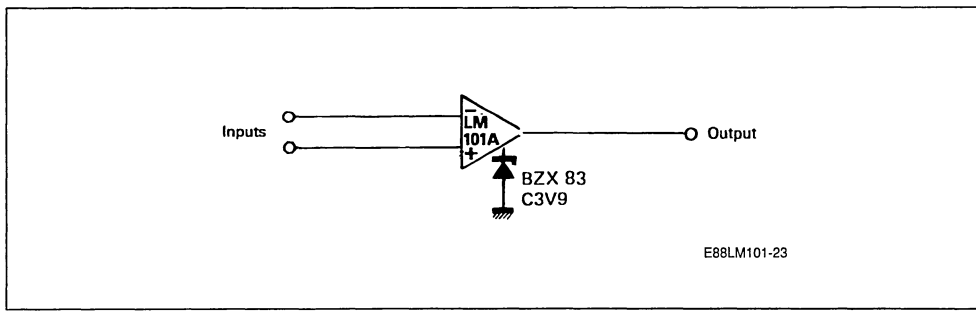


BASIC DIAGRAMS (continued)

ISOLATING LARGE CAPACITIVE LOADS

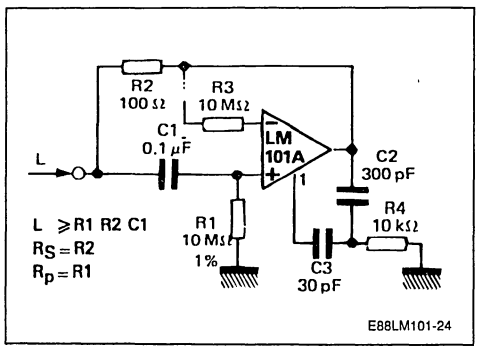


VOLTAGE COMPARATOR FOR DRIVING RTL LOGIC OR HIGH CURRENT DRIVER

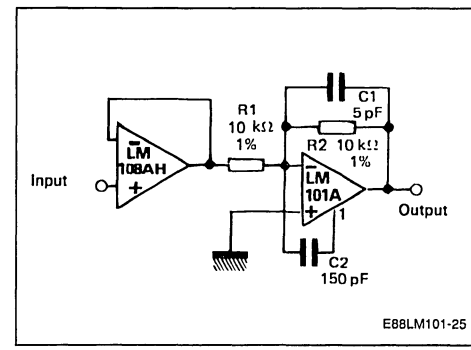


TYPICAL APPLICATIONS

SIMULATED INDUCTOR

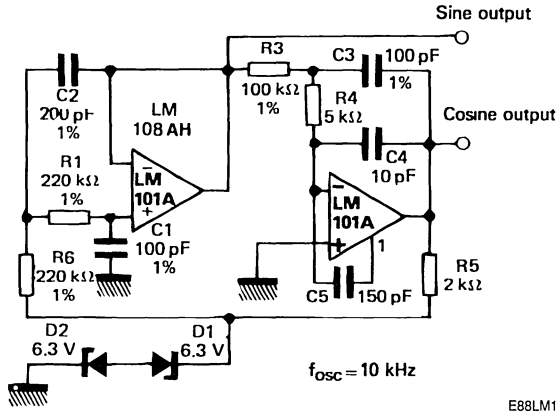


FAST INVERTING AMPLIFIER WITH HIGH INPUT IMPEDANCE



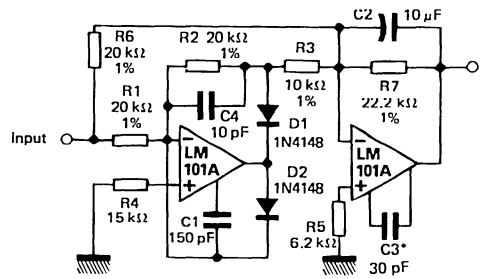
TYPICAL APPLICATIONS (continued)

SINE WAVE OSCILLATOR



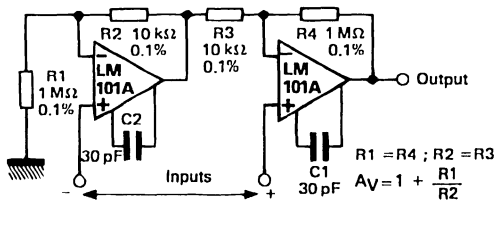
E88LM101-26

FAST AC/DC CONVERTER



E88LM101-27

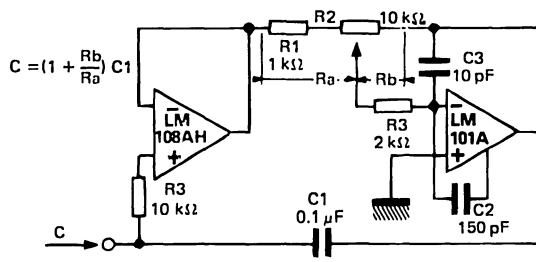
INSTRUMENTATION AMPLIFIER



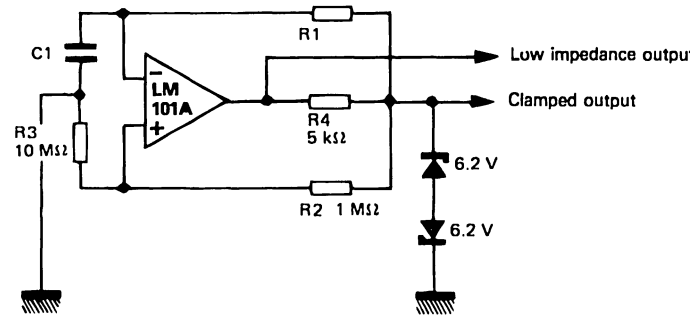
E88LM101-28

TYPICAL APPLICATIONS (continued)

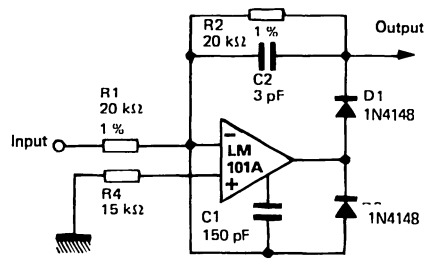
VARIABLE CAPACITANCE MULTIPLIER



LOW FREQUENCY SQUARE WAVE GENERATOR

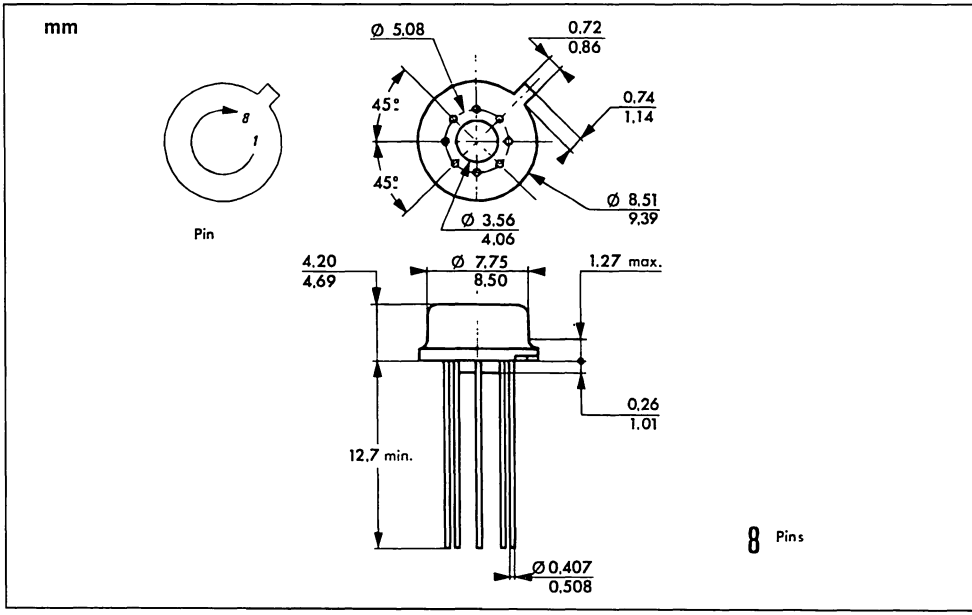


FAST HALF WAVE RECTIFIER

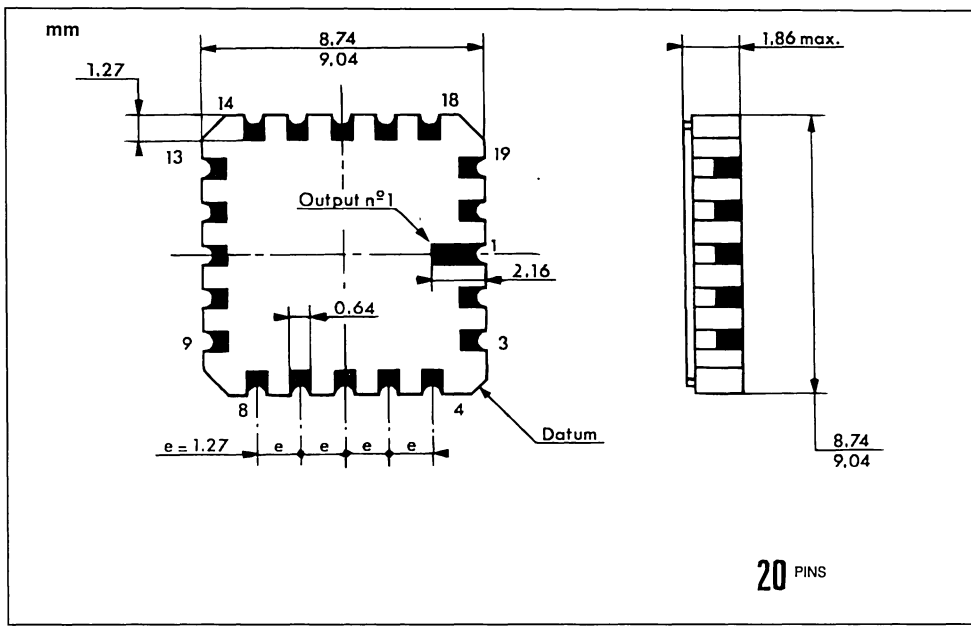


PACKAGE MECHANICAL DATA

8 PINS – METAL CAN TO99

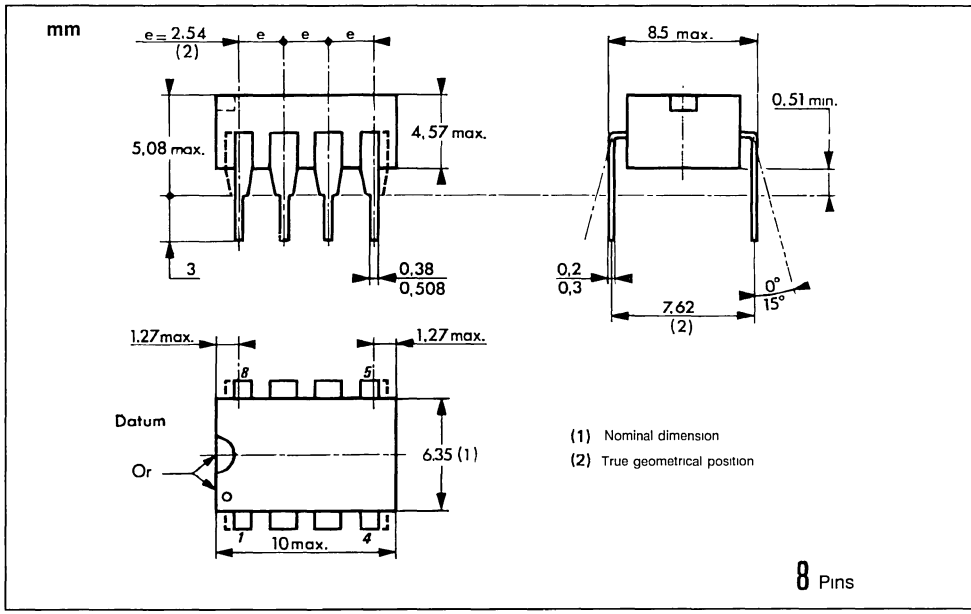


20 PINS – TRICECOP (LCC)

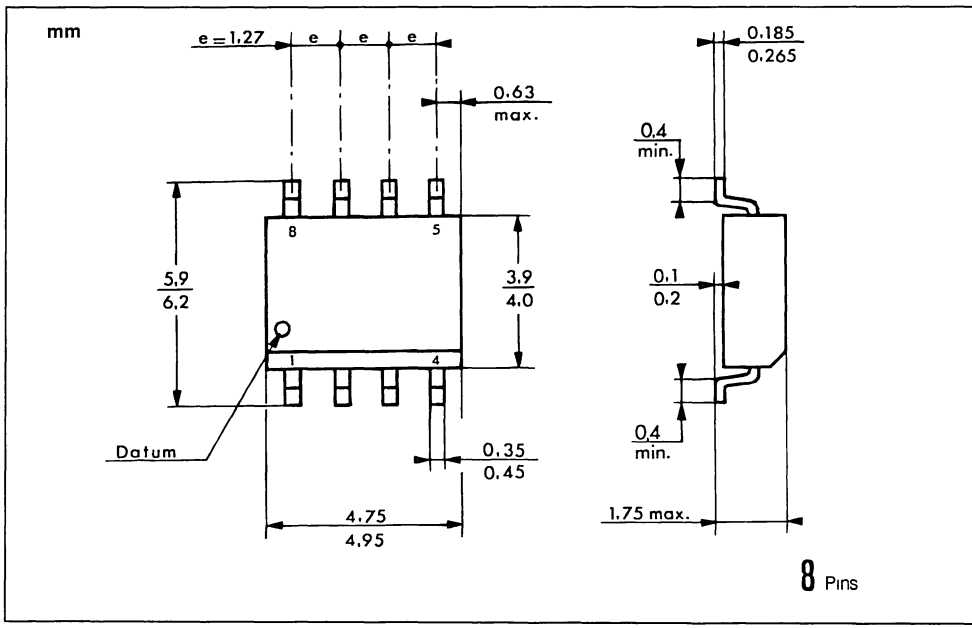


PACKAGE MECHANICAL DATA (continued)

8 PINS – PLASTIC DIP OR CERDIP



8 PINS – PLASTIC MICROPACKAGE (SO)

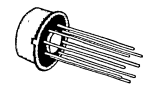


LM108,A-LM208,A LM308,A

PRECISION SINGLE OPERATIONAL AMPLIFIERS

Outstanding characteristics of LM108A :

- INPUT OFFSET VOLTAGE : 0.5 mV MAXIMUM
- INPUT BIAS CURRENT : 3 nA MAXIMUM OVER FULL TEMPERATURE RANGE
- INPUT OFFSET CURRENT : 0.4 nA MAXIMUM OVER FULL TEMPERATURE RANGE
- POWER SUPPLY CURRENT : 600 µA MAXIMUM
- GUARANTEED DRIFT CHARACTERISTICS
- SLEW RATE OF 10 V/µs AS INVERTING AMPLIFIER

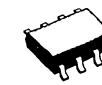


H
TO99
(Metal Can)

GC
LCC20
(Tricecop (LCC))

N
DIP8
(Plastic Package)

J
CERDIP8
(Cerdip Package)



D
SO8
(Plastic Micropackage)

DESCRIPTION

The LM108,A is a precision operational amplifier having specifications a factor ten better than FET amplifiers over a – 55 °C to + 125 °C temperature range. Selected units are available with offset voltages less than 1 mV and drifts less than 5 µV/°C. This makes it possible to eliminate offset adjustments, in most cases.

The device operates with supply voltages from ± 2 V to ± 20 V (LM308 : ± 2 V to ± 15 V) and has sufficient supply rejection to use unregulated supplies. Although the circuit is interchangeable with and uses the same compensation as the LM101A, an alternate compensation scheme can be used to make it particularly insensitive to power supply noise and to make supply bypass capacitors unnecessary.

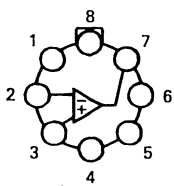
ORDER CODES

Part Number	Temperature Range	Package				
		H	J	N	GC	D
LM108,A	– 55 to + 125 °C	•	•		•	
LM208,A	– 40 to + 105 °C	•		•		•
LM308,A	0 to + 70 °C	•		•		•

Note : Hi-Rel Versions Available
Examples : LM108H, LM108AH, LM308N

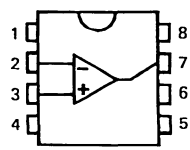
PIN CONNECTIONS (top views)

TO99



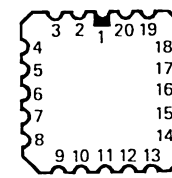
1 - Frequency compensation
2 - Inverting input
3 - Non-inverting input
4 - V^-_{CC}

DIP8
CERDIP8
SO8



5 - NC
6 - Output
7 - V^+_{CC}
8 - Frequency compensation

LCC20



1 - NC
2 - Frequency compensation
3 - NC
4 - NC
5 - Inverting input
6 - NC
7 - Non-inverting input
8 - NC
9 - NC
10 - V^-_{CC}

11 - NC
12 - NC
13 - NC
14 - NC
15 - Output
16 - NC
17 - V^+_{CC}
18 - NC
19 - NC
20 - Frequency compensation

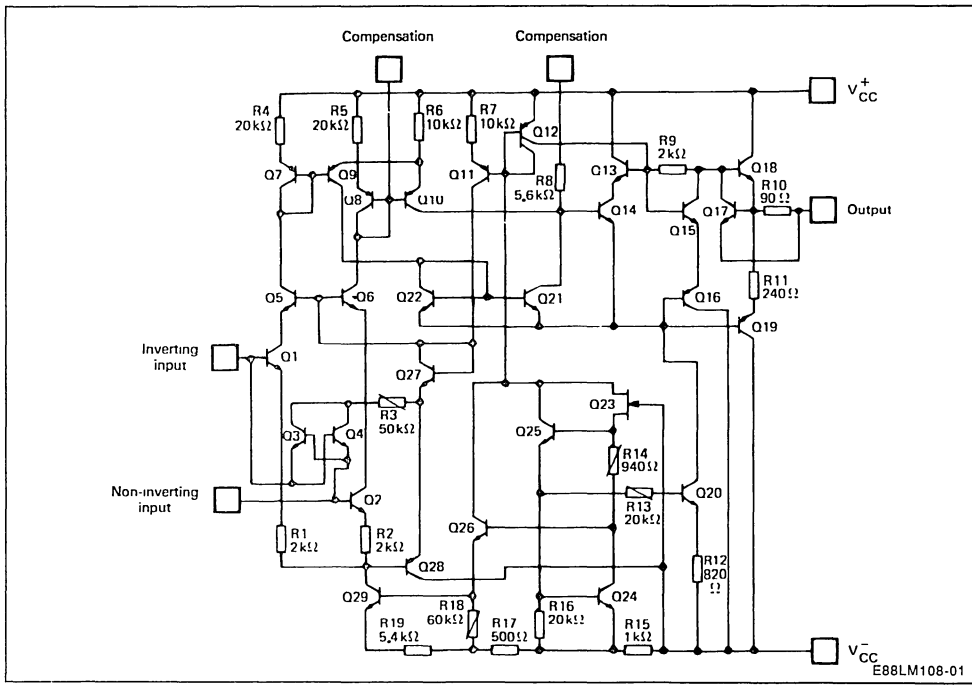
E88LM108-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM108, A	LM208, A	LM308, A	Unit
V_{CC}	Supply Voltage	± 22	± 22	± 22	V
V_I	Input Voltage (note 2)	± 15	± 15	± 15	V
I_{IO}	Input Offset Current (note 1)	± 10	± 10	± 10	mA
P_{tot}	Power Dissipation LM108GC, LM108AGC	500 665	500	500	mW
	Output Short-circuit Duration	Indefinite	Indefinite	Indefinite	
T_{oper}	Operating Free-air Temperature Range	– 55 to + 125	– 40 to + 105	0 to + 70	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	– 65 to + 150	– 65 to + 125	°C

Notes : 1. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1 V is applied between the inputs unless some limiting resistance is used.
2. For supply voltages less than ± 15 V, the absolute maximum input voltage is equel to the supply voltage.

SCHEMATIC DIAGRAM



Case	Frequency Compens.	Inverting Input	Non-inverting Input	V_{CC}^-	V_{CC}^+	Output	N.C.
TO99/SO8 DIP CERDIP	1, 8	2	3	4	7	6	5
LCC20	2, 20	5	7	10	17	15	*

* LCC 20 : Other pins are not connected.

ELECTRICAL CHARACTERISTICS

LM308A : $0\,°C \le T_{amb} < +\,70\,°C$ $C_1 = 33$ pF $\pm 5 < V_{CC} < \pm 20$ V
LM208A : $-40\,°C \le T_{amb} < +\,105\,°C$ $C_1 = 33$ pF $\pm 5 < V_{CC} < \pm 20$ V
LM108A : $-55\,°C \le T_{amb} < +\,125\,°C$ $C_1 = 33$ pF $\pm 5 < V_{CC} < \pm 20$ V
* => $V_{CC} = \pm 15$ V

Symbol	Parameter	LM108A / LM208A LM308A			Unit
		Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage $R_S \le 10$ kΩ $T_{amb} = 25$ °C $T_{min} \le T_{amb} \le T_{max}$		0.3	0.5 0.75	mV
I_{IO}	Input Offset Current $T_{amb} = 25$ °C $T_{min} \le T_{amb} \le T_{max}$		0.05	0.2 0.4	nA
I_{IB}	Input Bias Current $T_{amb} = 25$ °C LM108A - 208A LM308A $T_{min} \le T_{amb} \le T_{max}$ LM108A - 208A LM308A		0.6	2 4 3 7	nA
A_{VD}	Large Signal Voltage Gain * ($V_O = \pm 10$ V, $R_L = 2$ kΩ) $T_{amb} = 25$ °C $T_{min} \le T_{amb} \le T_{max}$	 80 60	 300		V/mV
S_{VR}	Supply Voltage Rejection Ratio ($R_S \le 10$ KΩ) $T_{amb} = 25$ °C $T_{min} \le T_{amb} \le T_{max}$	 96 96	 110		dB
I_{CC}	Supply Current, no Load $T_{amb} = 25$ °C $T_{min} \le T_{amb} \le T_{max}$		0.3	0.6 0.6	mA
V_I	Input Voltage Range * $T_{amb} = 25$ °C $T_{min} \le T_{amb} \le T_{max}$	 − 14 − 14		 + 14 + 14	V
CMR	Common-mode Rejection Ratio ($R_S \le 10$ kΩ) $T_{amb} = 25$ °C $T_{min} \le T_{amb} \le T_{max}$	 96 96	 110		dB
I_{OS}	Output Short-circuit Current * $T_{amb} = 25$ °C	 3	 10	 20	mA
$\pm V_{OPP}$	Output Voltage Swing * $T_{amb} = 25$ °C $R_L = 10$ KΩ $T_{min} \le T_{amb} \le T_{max}$ $R_L = 10$ KΩ	 13 13	 14		V
S_{VO}	Slew-rate ($V_I = \pm 10$ V, $R_L = 2$ kΩ, $C_L \le 100$ pF, $T_{amb} = 25$ °C, * unity Gain)		0.15		V/µs

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter		LM108A / LM208A LM308A			Unit
			Min.	Typ.	Max.	
t_r	Rise Time (V_I = ± 20 mV, R_L = 2 kΩ, C_L ≤ 100 pF, T_{amb} = 25 °C, unity gain)	*		0.7		µs
K_{OV}	Overshoot (V_I = 20 mV, R_L = 2 kΩ) C_L ≤ 100 pF, T_{amb} = 25 °C, unity gain)			10		%
R_I	Input Resistance, T_{amb} = 25 °C	*	30	70		MΩ
GBP	Gain Bandwidth Product (V_I = 10 mV, R_L = 2 kΩ, C_L ≤ 100 pF) (f = 100 KHz, T_{amb} = 25 °C)	*	 0.3	 0.8	 1.2	MHz
THD	Total Harmonic Distortion (f = 1 KHz, A_V = 20 dB, R_L = 2 kΩ, V_O = 2 V_{PP}, C_L ≤ 100 pF, T_{amb} = 25 °C)	*		 0.12		%
V_n	Equivalent Input Noise Voltage (f = 1 KHz, R_g = 100 Ω)	*		 20		$nV/\sqrt{Hz}$
DV_{IO}	Input Offset Voltage Drift $T_{min} \leq T_{amb} \leq T_{max}$			 1	 5	µV/°C
DI_{IO}	Input Offset Current Drift $T_{min} \leq T_{amb} \leq$ 25 °C			 0.5	 2.5	pA/°C

ELECTRICAL CHARACTERISTICS

LM308 : $0 \leq T_{amb} \leq +70$ °C $\quad \pm 5 \leq V_{CC} \leq \pm 20$ V
LM208 : $-40 \leq T_{amb} \leq +105$ °C $\quad \pm 5 \leq V_{CC} \leq \pm 20$ V
LM108 : $-55 \leq T_{amb} \leq +125$ °C $\quad \pm 5 \leq V_{CC} \leq \pm 20$ V

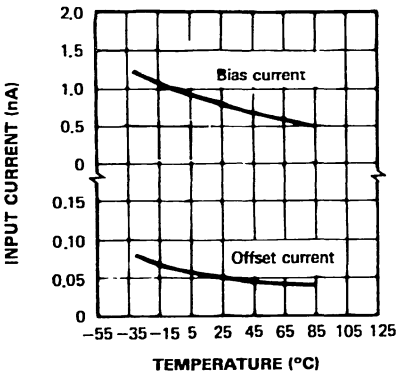
* = ≥ V_{CC} = ± 15 V

Symbol	Parameter	LM108 – LM208			LM308			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage R_S ≤ 10 kΩ T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		0.7	 2 3		2	 5 7	mV
I_{IO}	Input Offset Current T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		0.05	0.2 0.4		0.05	0.2 0.4	nA
I_{IB}	Input Bias Current T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		0.6	 2 3		0.6	 4 7	nA
A_{VD}	Large Signal Voltage Gain * (V_O = ± 10 V, R_L = 2 kΩ) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 50 25	 300		 50 25	 300		V/mV
S_{VR}	Supply Voltage Rejection Ratio (R_S ≤ 10 kΩ) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 80 80	 96		 80 80	 96		dB
I_{CC}	Supply Current, no Load T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		0.3	0.6 0.6		0.3	0.6 0.6	mA

ELECTRICAL CHARACTERISTICS (continued)

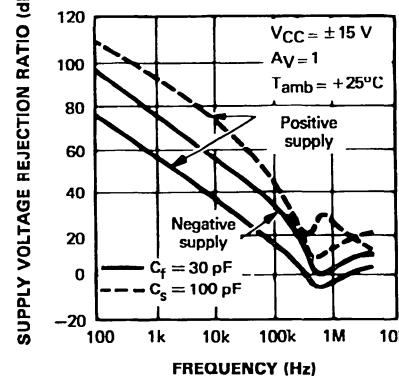
Symbol	Parameter		LM108 – LM208			LM308			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_I	Input Voltage Range T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	*	 – 14 – 14		 + 14 + 14	 – 14 – 14		 + 14 + 14	V
CMR	Common-mode Rejection Ratio ($R_S \leq 10$ kΩ) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		 80 80	 100		 80 80	 100		dB
I_{OS}	Output Short-circuit Current T_{amb} = 25 °C	*	 3	 10	 20	 3	 10	 20	mA
± V_{OPP}	Output Voltage Swing T_{amb} = 25 °C R_L = 10 kΩ $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 10 kΩ	*	 13 13	 14		 13 13	 14		V
S_{VO}	Slew-rate (V_I = ± 10 V, R_L = 2 kΩ, $C_L \leq 100$ pF, T_{amb} = 25 °C, unity gain)	*		 0.15			 0.15		V/µs
t_r	Rise Time (V_I = ± 20 mV, R_L = 2 kΩ, $C_L \leq 100$ pF, T_{amb} = 25 °C, unity gain)	*		 0.7			 0.7		µs
K_{OV}	Overshoot (V_I = 20 mV, R_L = 2 kΩ, $C_L \leq 100$ pF, T_{amb} = 25 °C, unity gain)			 10			 10		%
R_I	Input Resistance, T_{amb} = 25 °C	*	30	70		10	40		MΩ
GBP	Gain Bandwidth Product (V_I = 10 mV, R_L = 2 kΩ, $C_L \leq 100$ pF) (f = 100 kHz, T_{amb} = 25 °C)	*	 0.3	 0.8	 1.2	 0.3	 0.8	 1.2	MHz
THD	Total Harmonic Distortion (f = 1 kHz, A_V = 20 dB, R_L = 2 kΩ, V_O = 2 V_{PP}, $C_L \leq 100$ pF, T_{amb} = 25 °C)	*		 0.12			 0.12		%
V_n	Equivalent Input Noise Voltage (f = 1 kHz, R_g = 100 Ω)	*		 20			 20		nV/√Hz
DV_{IO}	Input Offset Voltage Drift $T_{min} \leq T_{amb} \leq T_{max}$			 3	 15		 6	 30	µV/°C
DI_{IO}	Input Offset Current Drift $T_{min} \leq T_{amb} \leq 25$ °C			 0.5	 2.5		 2	 10	pA/°C

INPUT CURRENTS (Note 3)



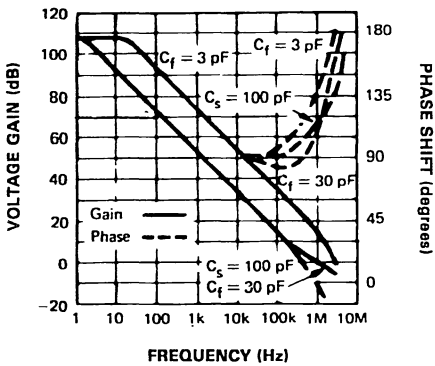
E88LM108-03

POWER SUPPLY REJECTION RATIO



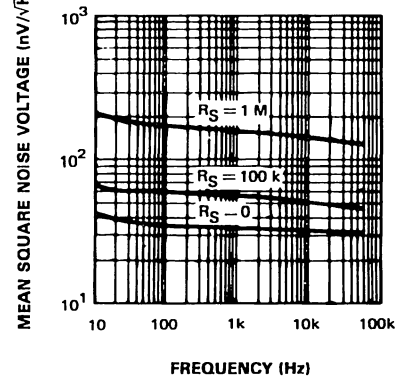
E88LM108-05

OPEN LOOP FREQUENCY RESPONSE



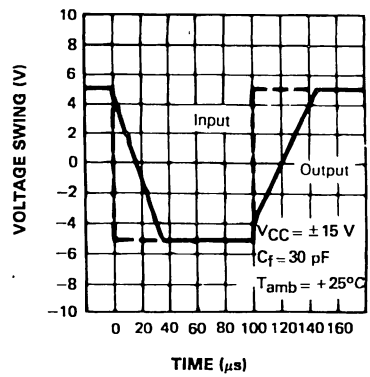
E88LM108-06

INPUT NOISE VOLTAGE



E88LM108-07

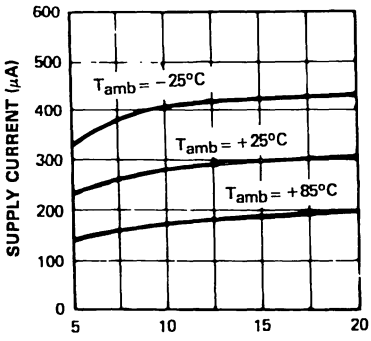
VOLTAGE FOLLOWER PULSE RESPONSE



E88LM108-08

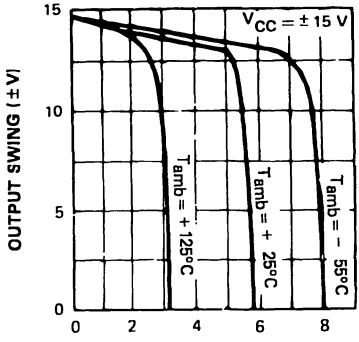
Note : 3. **LM108A :** − 55 °C ≤ T_{amb} ≤ + 125 °C, ± 5 V ≤ V_{CC} ≤ ± 20 V.
LM208A : − 40 °C ≤ T_{amb} ≤ + 105 °C, ± 5 V ≤ V_{CC} ≤ ± 20 V.

SUPPLY CURRENT



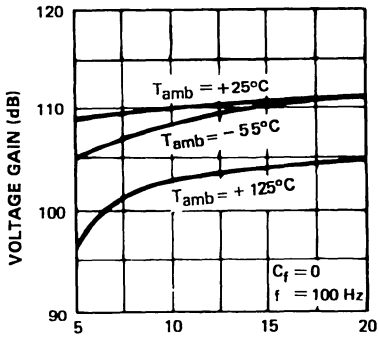
E88LM108-11

OUTPUT SWING



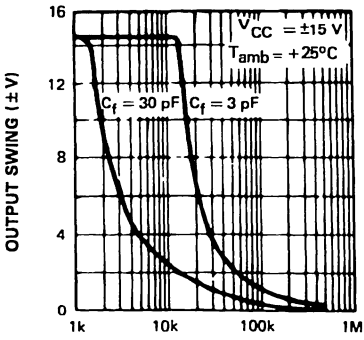
E88LM108-12

VOLTAGE GAIN



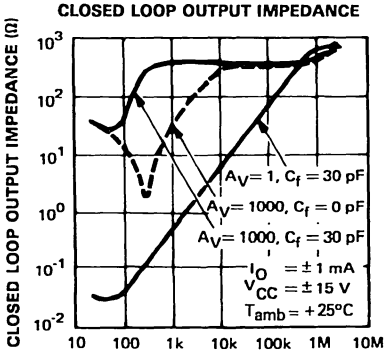
E88LM108-18

LARGE SIGNAL FREQUENCY RESPONSE



E88LM108-20

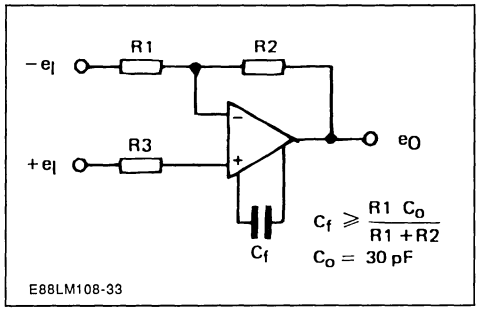
CLOSED LOOP OUTPUT IMPEDANCE



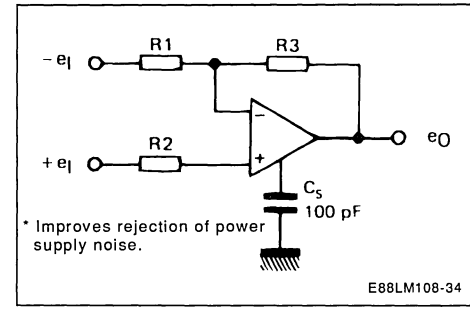
E88LM108-21

BASIC DIAGRAMS

STANDARD COMPENSATION CIRCUIT

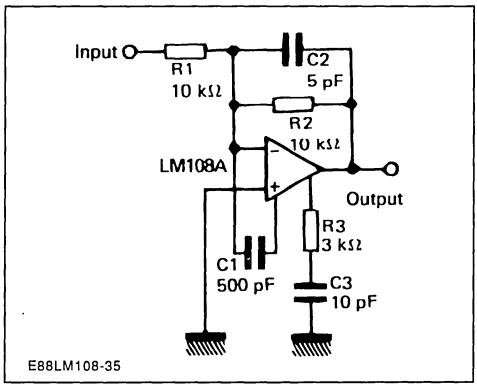


ALTERNATE FREQUENCY COMPENSATION

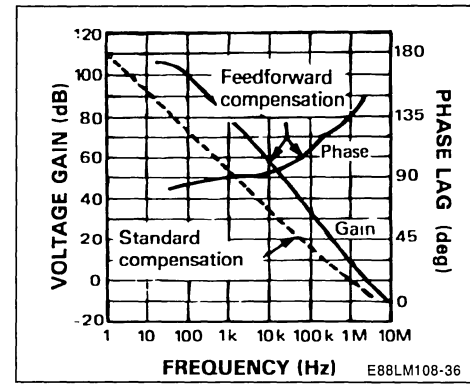


TYPICAL APPLICATIONS

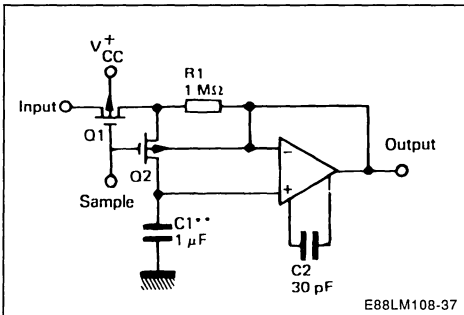
STANDARD FEEDFORWARD



OPEN LOOP VOLTAGE GAIN

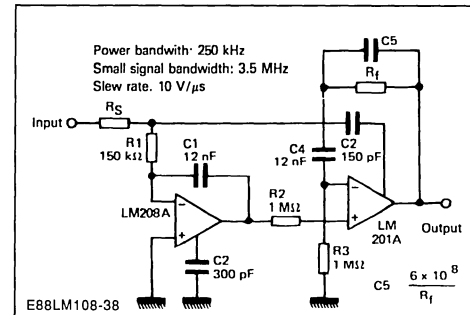


FEEDFORWARD COMPENSATION FOR DECOUPLING LOAD CAPACITANCE



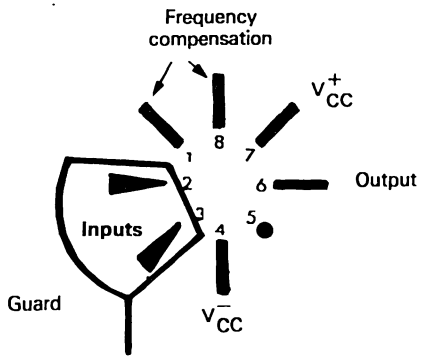
* Worst case drift less than 2.5 mV/sec.
** Teflon, polyethylène or polycarbonate dielectric capacitor.

SAMPLE AND HOLD



In addition to increasing speed the LM201A raises high and low frequency gain and eliminates thermal feedback.

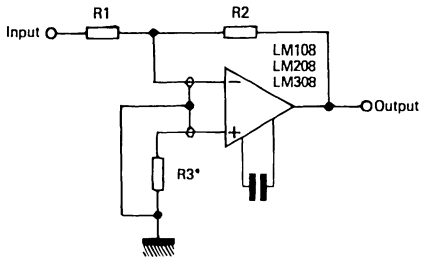
CB-11 METAL CAN (top view)



E88LM108-40

Pin 4 connected to case

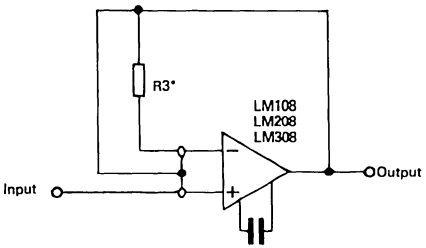
INVERTING AMPLIFIER



E88LM108-40

* Used to compensate for large source resistances.

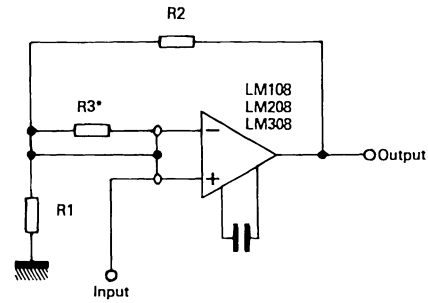
FOLLOWING AMPLIFIER



E88LM108-40

* Used to compensate for large source resistances.

NON-INVERTING AMPLIFIER



E88LM108-40

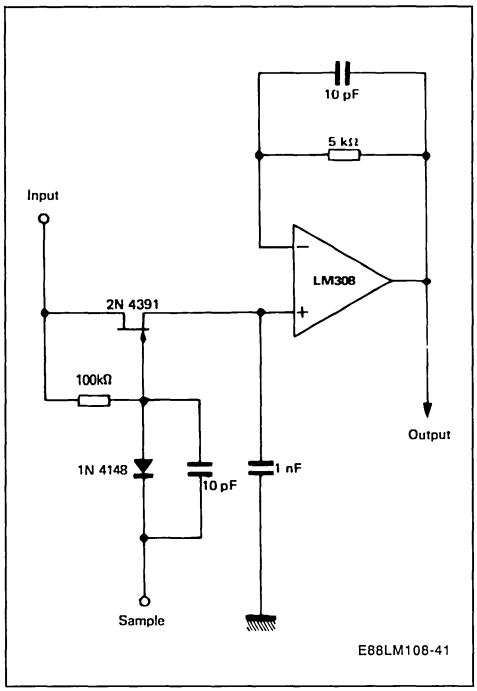
* Used to compensate for large source resistances.

INPUT GUARDING

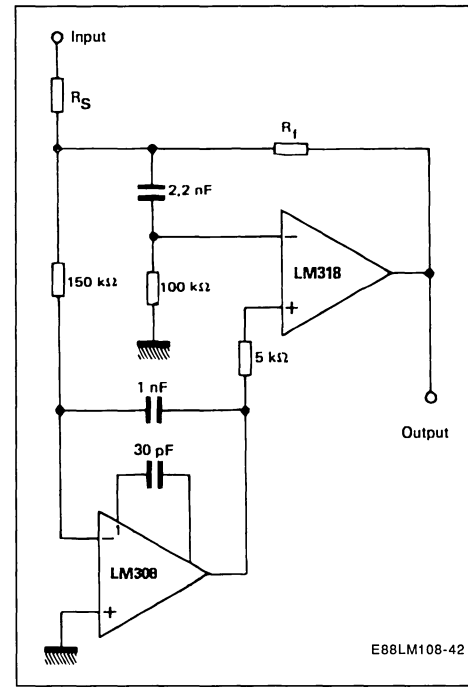
Leakage currents are on the verge of causing trouble at + 125 °C. The standard pin configuration of most IC op amps has the input pins adjacent to pins which are the supply potentials. Therefore, it is advisable to employ guarding to reduce the voltage difference between the inputs and adjacent metal runs. A ten-lead pin circle is used, and the leads of the IC are formed so that the holes adjacent to the inputs are vacant when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at the same potential as the inputs.

TYPICAL APPLICATION DIAGRAMS

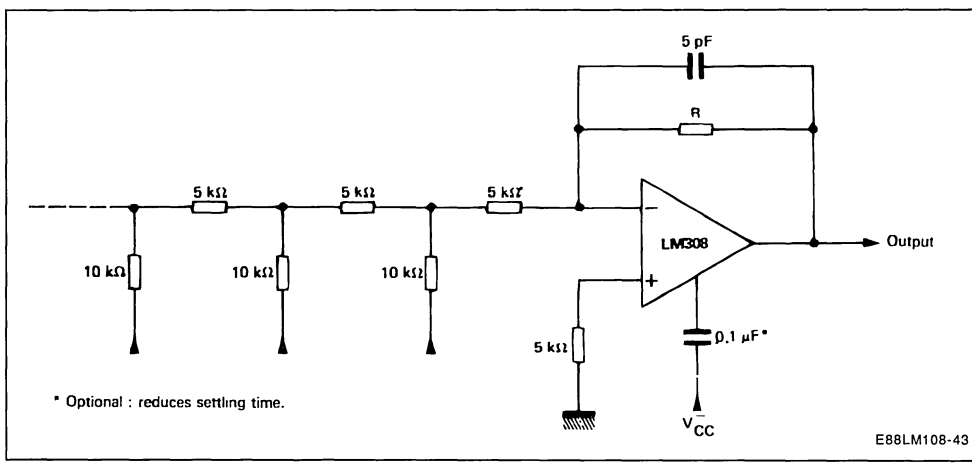
FAST SAMPLE AND HOLD



FAST SUMMING AMPLIFIER WITH LOW INPUT CURRENT

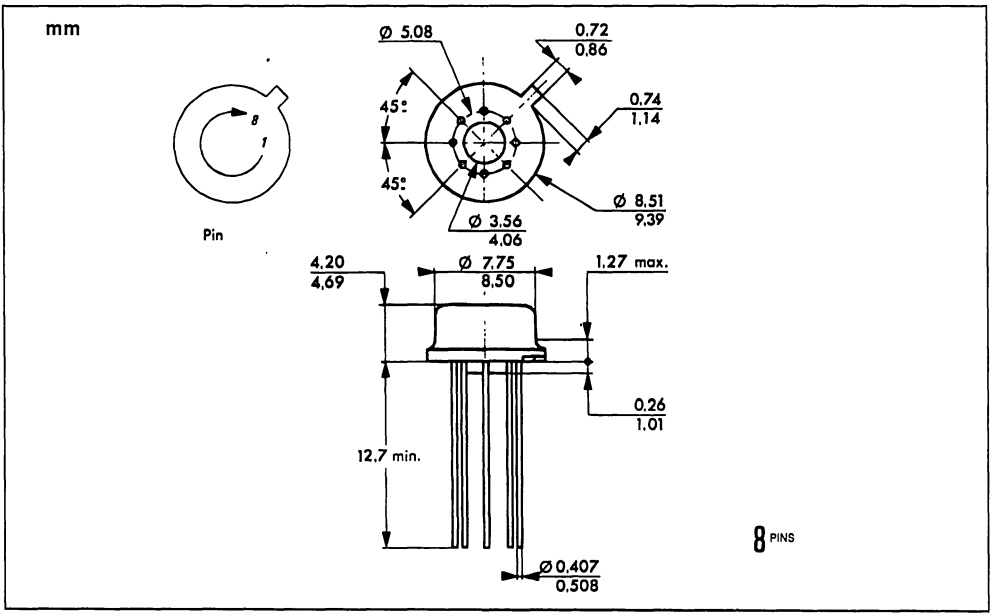


D/A CONVERTER USING LADDER NETWORK

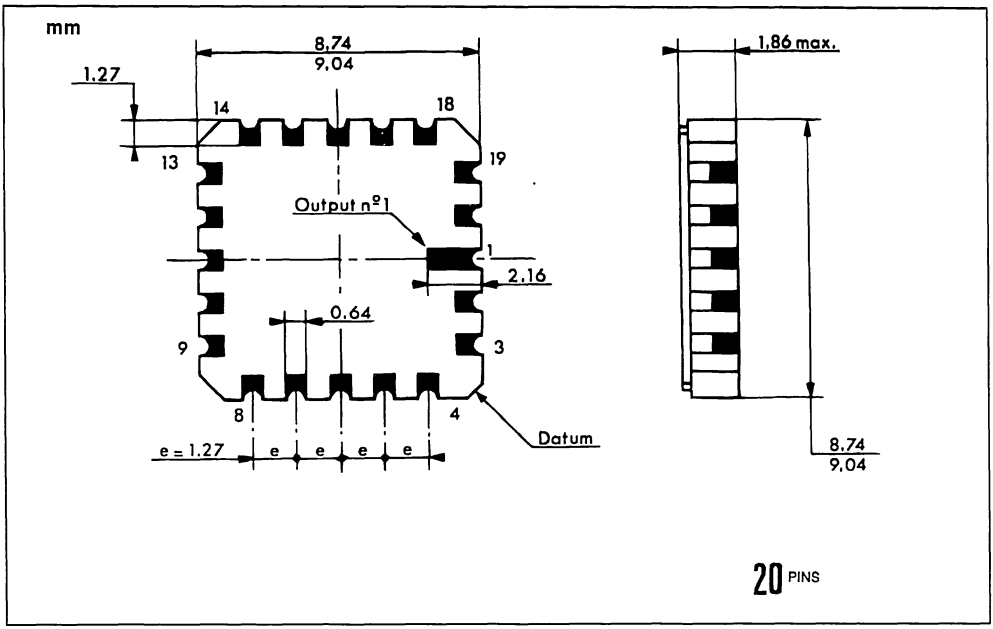


MECHANICAL DATA

8 PINS – TO99 – METAL CAN

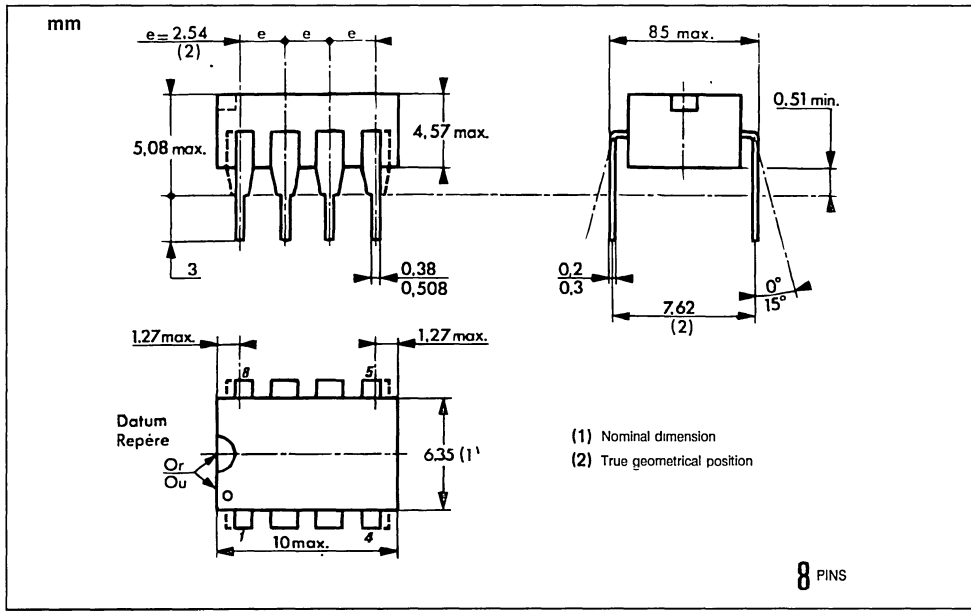


20 PINS – TRICECOP (LCC)

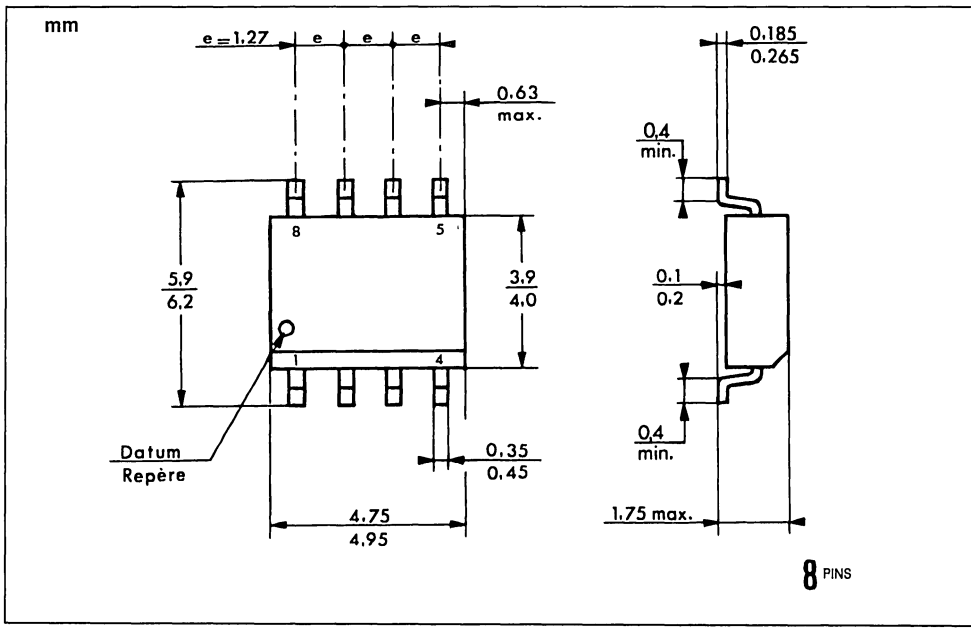


MECHANICAL DATA (continued)

8 PINS – PLASTIC DIP OR CERDIP



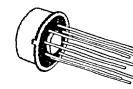
8 PINS – PLASTIC MICROPACKAGE SO



LM111-LM211 LM311

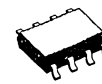
VOLTAGE COMPARATORS

- MAXIMUM INPUT CURRENT : 150 nA
- MAXIMUM OFFSET CURRENT : 20 nA
- DIFFERENTIAL INPUT VOLTAGE RANGE : ± 30 V
- POWER CONSUMPTION : 135 mW AT ± 15 V
- SUPPLY VOLTAGE : + 5 V TO ± 15 V
- OUTPUT CURRENT : 50 mA



H
TO-99
(Metal Can)

N
DIP8
(Plastic Package)
J
CERDIP8
(Cerdip Package)



D
SO8
(Plastic Micropackage)

GC
LCC20
(Tricecop (LCC))

DESCRIPTION

The LM111, LM211 and LM311 are voltage comparators that have low input currents.

They are also designed to operate over a wide range of supply voltages : from standard ± 15 V operational amplifier supplies down to the single + 5 V supply used for IC logic.

Their output is compatible with RTL-DTL and TTL as well as MOS circuits and can switch voltages up to + 50 V at output currents as high as 50 mA.

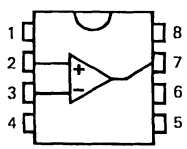
ORDER CODES

Part Number	Temperature Range	Package				
		H	N	J	D	GC
LM111	– 55 to + 125 °C	•		•		•
LM211	– 40 to + 105 °C	•	•		•	
LM311	0 to + 70 °C	•	•	•	•	

Note : Hi-Rel Versions Available
Examples : LM111H, LM111J

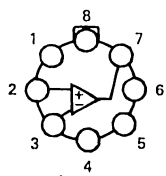
PIN CONNECTIONS (top views)

DIP8
CERDIP8
SO8



1 - Ground
2 - Non-inverting input
3 - Inverting input
4 - V_{CC}^-

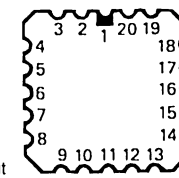
TO-99



5 - Balance
6 - Strobe/balance
7 - Output
8 - V_{CC}^+

1 - NC
2 - Ground
3 - NC
4 - NC
5 - Non-inverting input
6 - NC
7 - Inverting input
8 - NC
9 - NC
10 - V_{CC}^-

LCC20



11 - NC
12 - Balance
13 - NC
14 - NC
15 - Balance/Strobe
16 - NC
17 - Output
18 - NC
19 - NC
20 - V_{CC}^+

ABSOLUTE MAXIMUM RATINGS

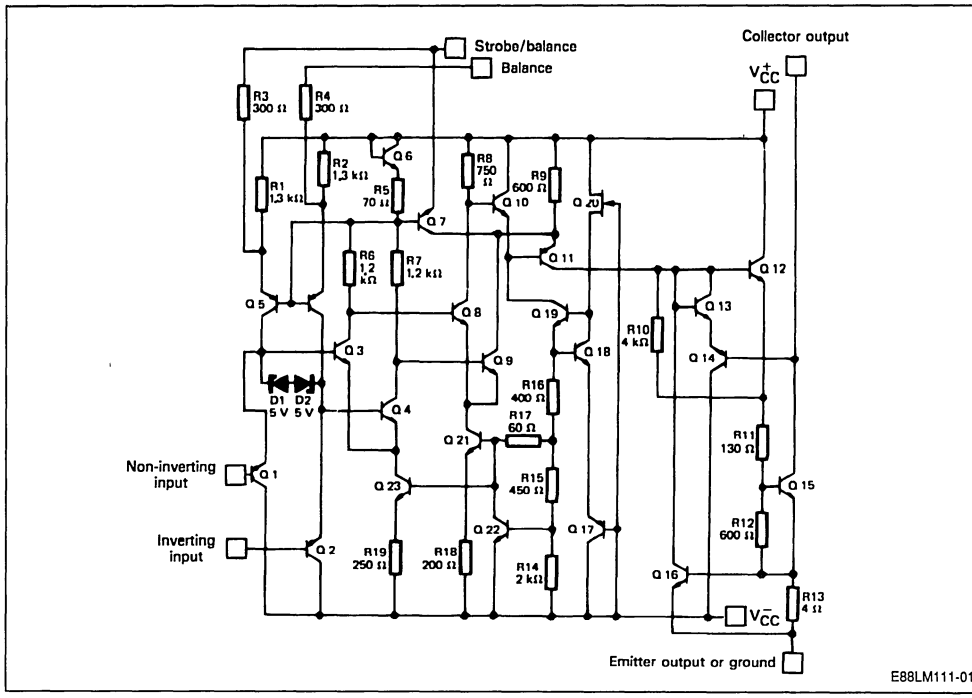
Symbol	Parameter	LM111	LM211	LM311	Unit
V_{CC}	Supply Voltage	36	36	36	V
V_{ID}	Differential Input Voltage	± 30	± 30	± 30	V
V_I	Input Voltage – (note 1)	± 15	± 15	± 15	V
P_{tot}	Power Dissipation LM311D-LM211D Other Versions	 500	 500	 300 500	mW
T_{oper}	Operating Free-air Temperature Range	– 55 to + 125	– 40 to + 105	0 to + 70	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	– 65 to + 150	– 65 to + 150	°C
$V_{(1-4)}$	Ground to Negative Supply Voltage	30	30	30	V
$V_{(7-4)}$	Output to Negative Supply Voltage	50	50	40	V

Output short-circuit duration : 10 s
Voltage at strobe pin : $V_{\bar{C}C}$ – 5 V

Maximum junction temperature **LM111** : + 150 °C
LM211 : + 150 °C
LM311 : + 150 °C

Note : 1. This rating applies for ± 15 V supplies. The positive input voltage limit is 30 V above the negative. The negative input voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.

SCHEMATIC DIAGRAM



Case	GND	Non-inverting Input	Inverting Input	$V_{\bar{C}C}$	Balance	Strobe/ Balance	Output	$V_{\bar{C}C}$	N.C.
TO–99 / DIP8 CERDIP8 / SO8	1	2	3	4	5	6	7	8	
LCC20	2	5	7	10	12	15	17	20	*

*** LCC20 :** Other pins are not connected.

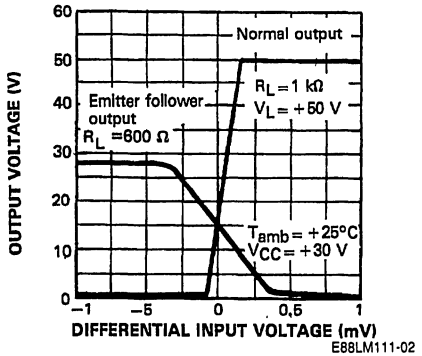
ELECTRICAL CHARACTERISTICS

LM111: $-55\ °C \le T_{amb} \le +125\ °C$, $V_{CC} = \pm 15\ V$
LM211: $-40\ °C \le T_{amb} \le +105\ °C$, $V_{CC} = \pm 15\ V$
LM311: $0\ °C \le T_{amb} \le +70\ °C$, $V_{CC} = \pm 15\ V$
(unless otherwise specified)

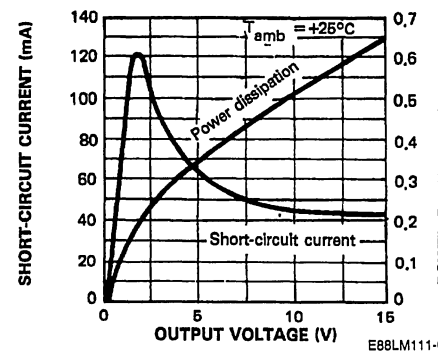
Symbol	Parameter	LM111/LM211			LM311			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage ($R_S \le 50\ k\Omega$) – (note 2)							mV
	$T_{min} \le T_{amb} \le T_{max}$			4			10	
	$T_{amb} = +25\ °C$		0.7	3		2	7.5	
I_{IO}	Input Offset Current – (note 2)							nA
	$T_{min} \le T_{amb} \le T_{max}$			20			70	
	$T_{amb} = +25\ °C$		4	10		6	50	
I_{IB}	Input Bias Current – (note 2)							nA
	$T_{min} \le T_{amb} \le T_{max}$			150			300	
	$T_{amb} = +25\ °C$		60	100		100	250	
A_{VD}	Large Signal Voltage Gain ($T_{amb} = +25\ °C$)	40	200		40	200		V/mV
	Supply Currents ($T_{amb} = 25\ °C$)							mA
I_{CC}^{+}	Positive		5.1	6		5.1	7.5	
I_{CC}^{-}	Negative		4.1	5		4.1	5	
V_I	Input Voltage Range		± 14			± 14		V
V_{OL}	Low Level Output Voltage							V
	$T_{min} \le T_{amb} \le T_{max}$							
	$V_{CC}^{+} \ge +4.5\ V$, $V_{CC}^{-} = 0$,							
	$I_{sink} = 8\ mA$, $V_I \le -6\ mV$		0.23	0.4				
	$V_I \le -10\ mV$					0.23	0.4	
	$T_{amb} = +25\ °C$, $I_O = 50\ mA$, $V_I \le -5\ mV$		0.75	1.5				
	$V_I \le -10\ mV$					0.75	1.5	
I_{OH}	High Level Output Current							
	$T_{min} \le T_{amb} \le T_{max}$, $V_I \ge +5\ mV$, $V_O = +35\ V$		0.1	0.5				µA
	$T_{amb} = +25\ °C$, $V_I \ge +5\ mV$, $V_O = +35\ V$		0.2	10				nA
	$V_I \ge +10\ mV$, $V_O = +35\ V$					0.2	50	nA
I_{strobe}	Strobe Current ($T_{amb} = +25\ °C$)		3			3		mA
t_{re}	Response Time ($T_{amb} = +25\ °C$) – (note 3)		200			200		ns

Notes : 2. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single + 5 V supply up to ± 15 V supplies.
The offset voltages and offset currents given are the maximum values required to drive the output down to + 1 V or up to + 14 V with a 1 mA load current. Thus, these parameters define an error band and take into account the worst-case of voltage gain and input impedance.
3. The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

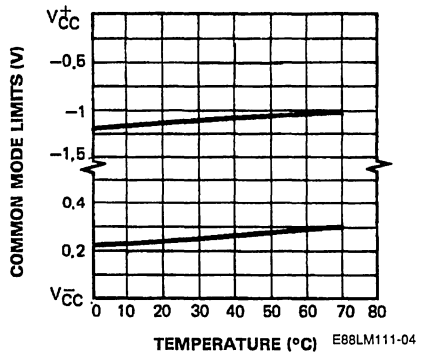
TRANSFER CHARACTERISTICS



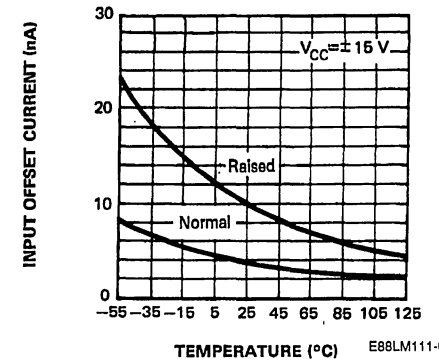
OUTPUT LIMITING CHARACTERISTICS



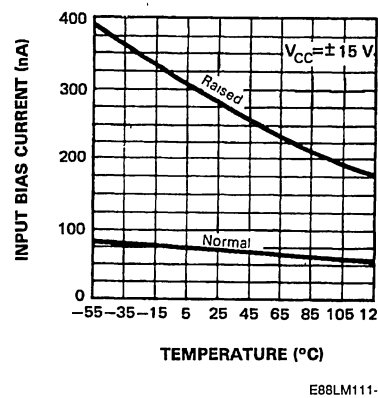
COMMON MODE LIMITS



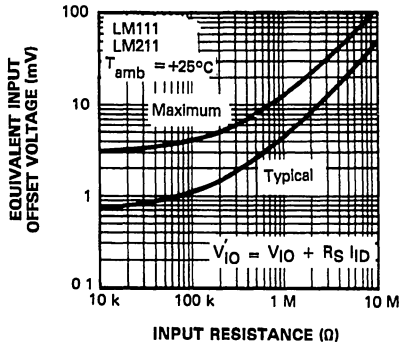
INPUT OFFSET CURRENT



INPUT BIAS CURRENT

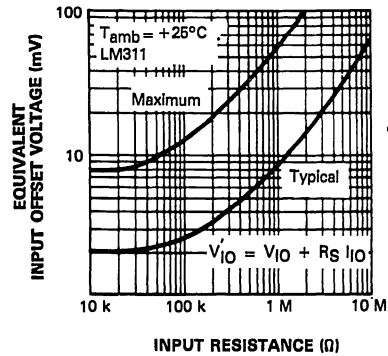


EQUIVALENT INPUT OFFSET ERROR



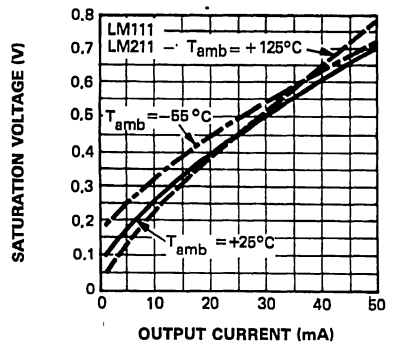
E88LM111-07

EQUIVALENT INPUT OFFSET ERROR



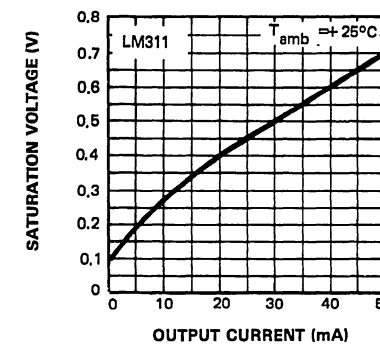
E88LM111-08

LOW LEVEL OUTPUT SATURATION VOLTAGE



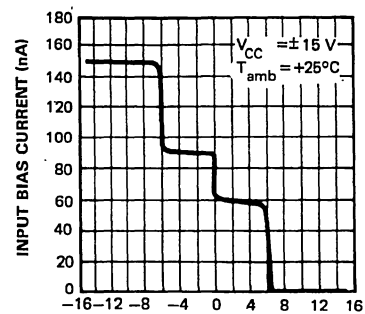
E88LM111-09

LOW LEVEL OUTPUT SATURATION VOLTAGE



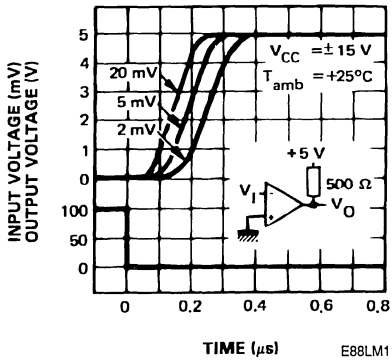
E88LM111-10

INPUT CHARACTERISTICS



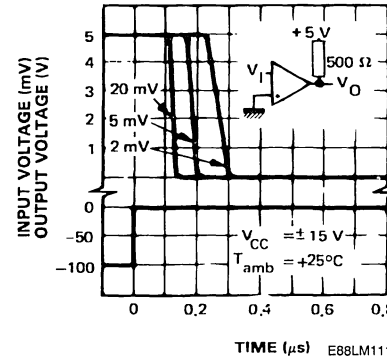
E88LM111-11

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



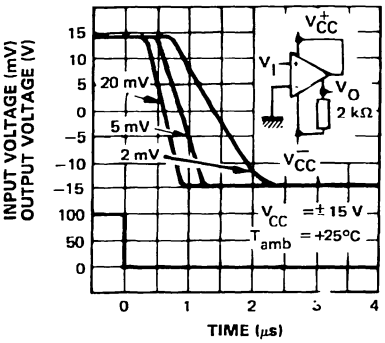
E88LM111-12

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



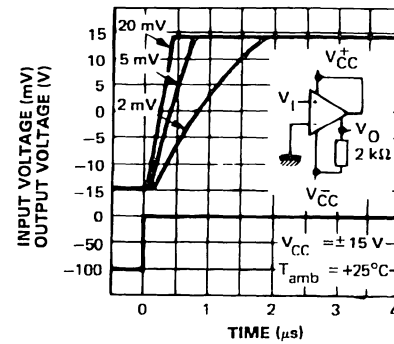
E88LM111-13

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



E88LM111-14

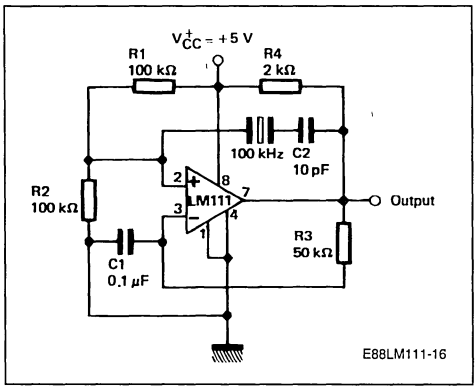
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



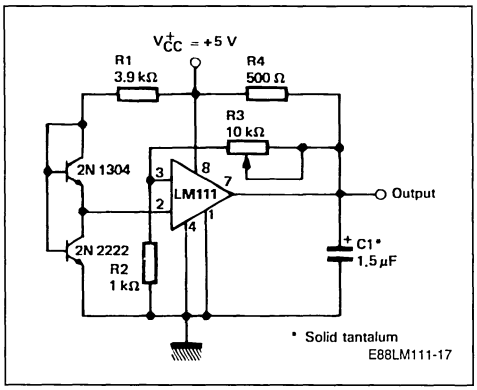
E88LM111-15

TYPICAL APPLICATIONS

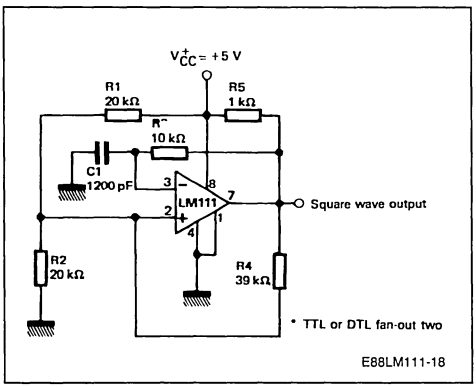
CRYSTAL OSCILLATOR



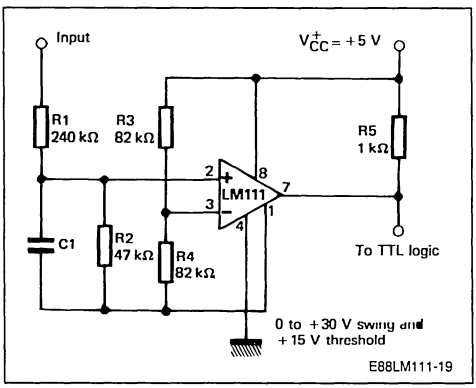
LOW VOLTAGE ADJUSTABLE REFERENCE SUPPLY



100 kHz FREE RUNNING MULTIVIBRATOR

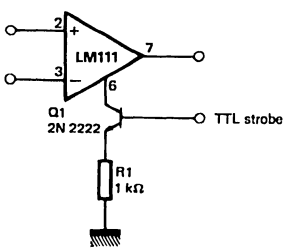


TTL INTERFACE WITH HIGH LEVEL LOGIC

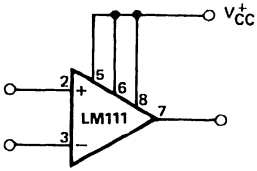


AUXILIARY CIRCUITS

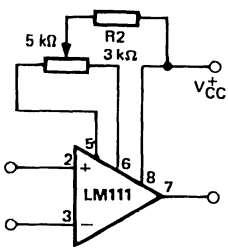
STROBE



INCREASING INPUT STAGE CURRENT

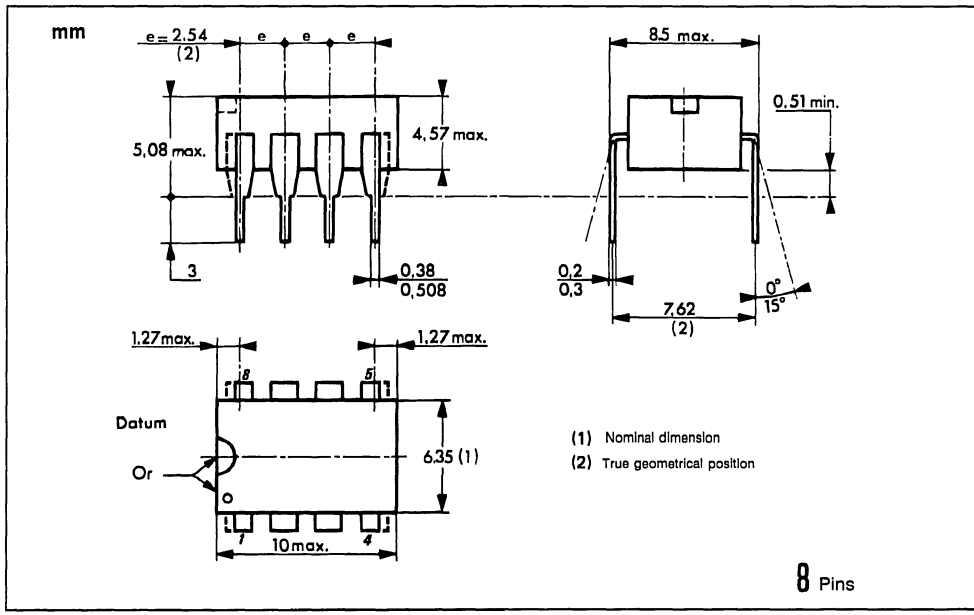


OFFSET BALANCING

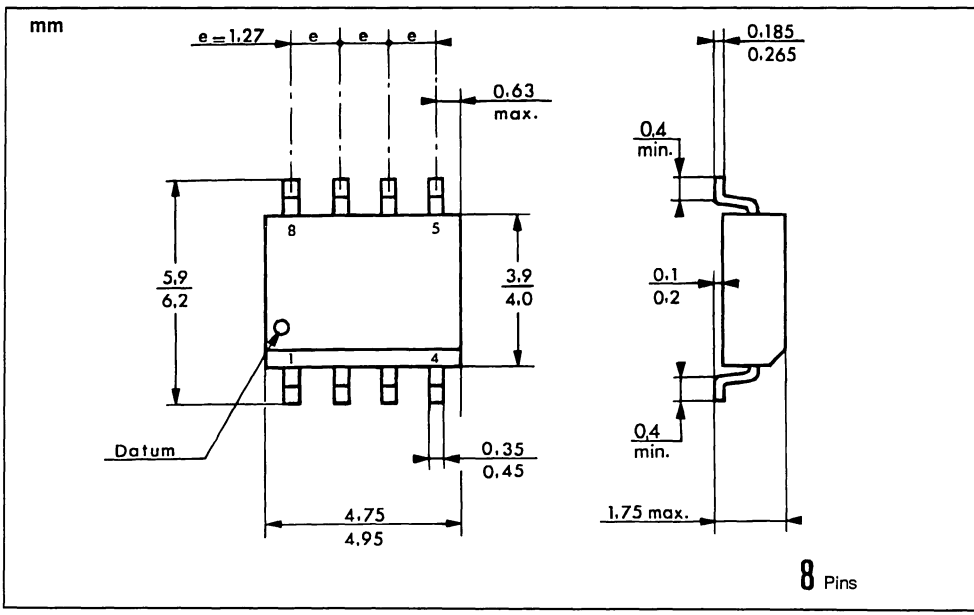


PACKAGE MECHANICAL DATA

8 PINS – PLASTIC DIP OR CERDIP

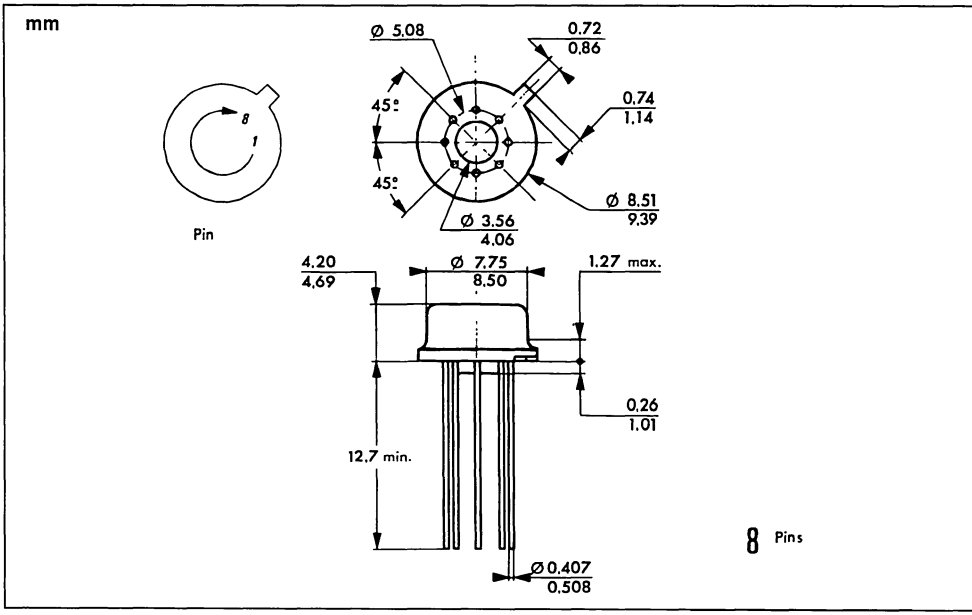


8 PINS – PLASTIC MICROPACKAGE (SO)

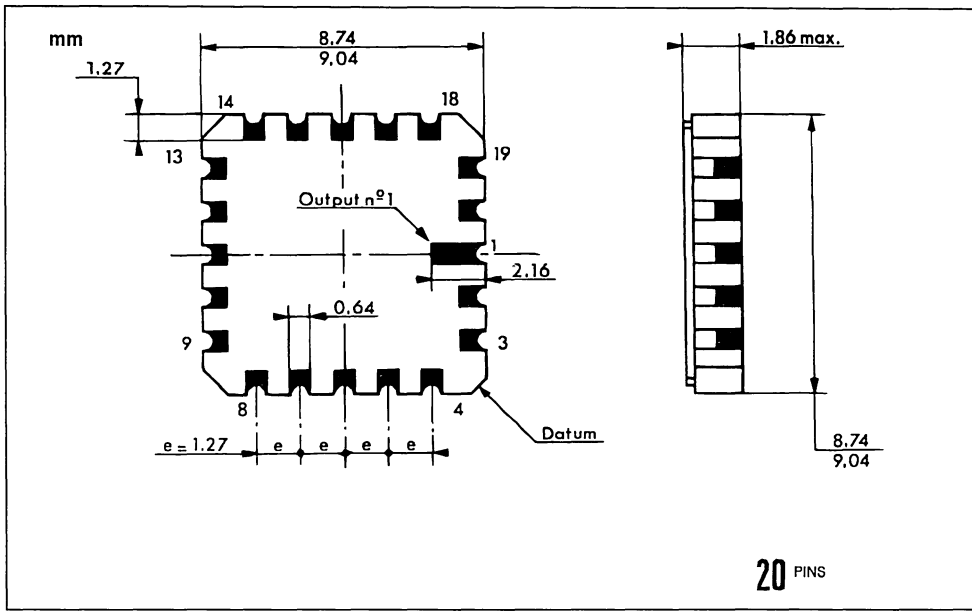


PACKAGE MECHANICAL DATA (continued)

8 PINS – METAL CAN TO99



20 PINS – TRICECOP (LCC)

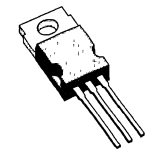


SGS-THOMSON MICROELECTRONICS

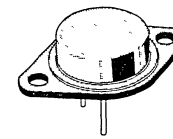
LM117/217 LM317

1.2V TO 37V ADJUSTABLE VOLTAGE REGULATOR

- OUTPUT VOLTAGE RANGE : 1.2 TO 37V
- OUTPUT CURRENT IN EXCESS OF 1.5A
- 0.1% LINE AND LOAD REGULATION
- FLOATING OPERATION FOR HIGH VOLTAGES
- COMPLETE SERIES OF PROTECTIONS : CURRENT LIMITING, THERMAL SHUTDOWN AND SOA CONTROL



TO-220



TO-3

DESCRIPTION

The LM117/LM217/LM317 are monolithic integrated circuit in TO-220 and TO-3 packages intended for use as positive adjustable voltage regulators.

They are designed to supply more than 1.5A of load current with an output voltage adjustable over a 1.2 to 37V range.

The nominal output voltage is selected by means of only a resistive divider, making the device exceptionally easy to use and eliminating the stocking of many fixed regulators.

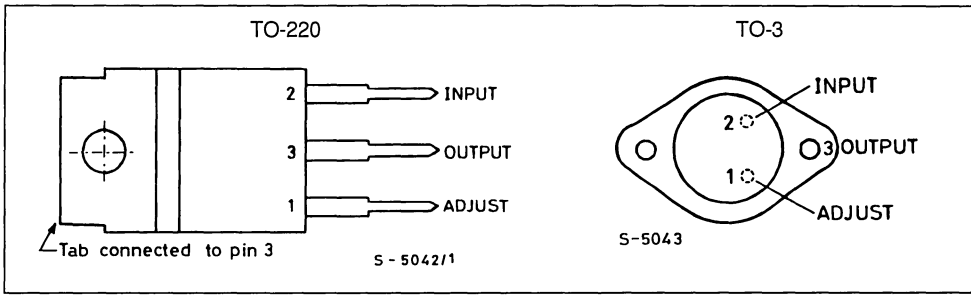
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{I-O}	Input-output Differential Voltage	40	V
I_O	Output Current	Internally Limited	
T_{op}	Operating Junction Temperature for : LM117 LM217 LM317	– 55 to 150 – 25 to 150 0 to 125	°C °C °C
P_{tot}	Power Dissipation	Internally limited	
T_{stg}	Storage Temperature	– 65 to 150	°C

THERMAL DATA

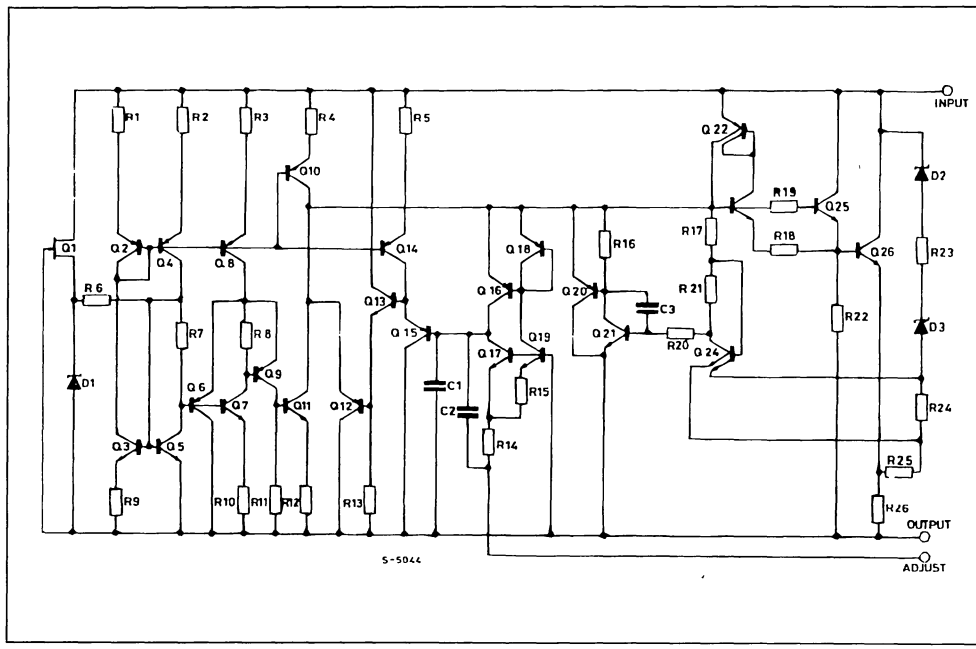
			TO-3	TO-220	
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	4	4	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	35	50	°C/W

PIN CONNECTION

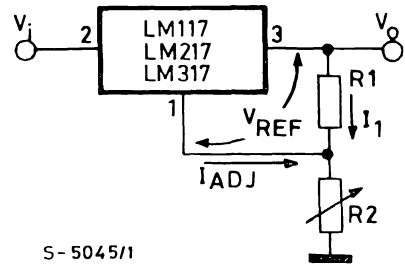


Type	TO-220	TO-3
LM117		LM117K
LM217	LM217T	LM217K
LM317	LM317T	LM317K

SCHEMATIC DIAGRAM



Basic adjustable regulator.



ELECTRICAL CHARACTERISTICS (V_i-V_o = 5V, I_o = 500mA, unless otherwise specified)

Symbol	Parameter	Test Conditions		LM117/LM217			LM317			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
ΔV_o	Line Regulation	V_i-V_o = 3 to 40V	T_j = 25°C		0.01	0.02		0.01	0.04	%/V
					0.02	0.05		0.02	0.07	
ΔV_o	Load Regulation	$V_o \leq 5V$ I_o = 10mA to 1.5A	T_j = 25°C		5	15		5	25	mV
					20	50		20	70	
		$V_o \geq 5V$ I_o = 10mA to 1.5A	T_j = 25°C		0.1	0.3		0.1	0.5	%
					0.3	1		0.3	1.5	
I_{ADJ}	Adjustment Pin Current				50	100		50	100	µA
ΔI_{ADJ}	Adjustment Pin Current	V_i-V_o = 2.5 to 40V I_o = 10mA to 1.5A			0.2	5		0.2	5	µA
V_{REF}	Reference Voltage (between pin 3 and pin 1)	V_i-V_o = 3 to 40V I_o = 10mA to 1.5A		1.2	1.25	1.3	1.2	1.25	1.3	V
$\frac{\Delta V_o}{V_o}$	Output Voltage Temperature Stability				1			1		%
$I_{o\,min}$	Minimum Load Current	V_i-V_o = 40V			3.5	5		3.5	10	mA
$I_{o\,max}$	Maximum Load Current	V_i-$V_o \leq 15V$		1.5	2.2		1.5	2.2		A
		V_i-V_o = 40V			0.4			0.4		
e_N	Output Noise (percentage of V_o)	T_j = 25°C, 10Hz to 10KHz			0.003			0.003		%
SVR	Supply Voltage Rejection (*)	T_j = 25°C f = 120Hz	C_{ADJ} = 0		65			65		dB
			C_{ADJ} = 10µF	66	80		66	80		

(*) CADJ is connected between pin 1 and ground

Note : Unless otherwise specified the above specs, apply over the following conditions LM 117 T_j = – 55 to 150°C ; LM 217 T_j = – 25 to 150°C , LM 317 T_j = 0 to 125°C.

Figure 1 : Output Current vs. Input-output Differential Voltage.

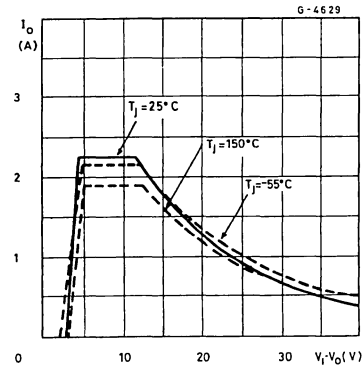


Figure 2 : Dropout Voltage vs. Junction Temperature.

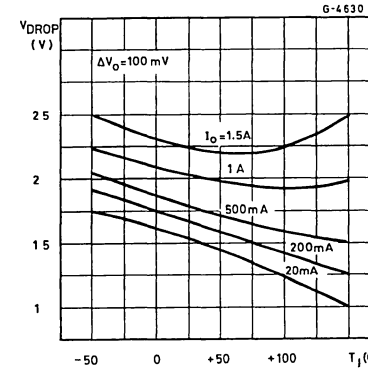


Figure 3 : Reference Voltage vs. Junction Temperature.

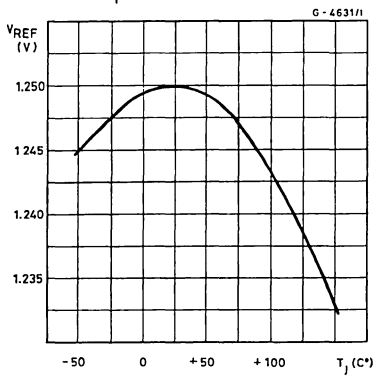
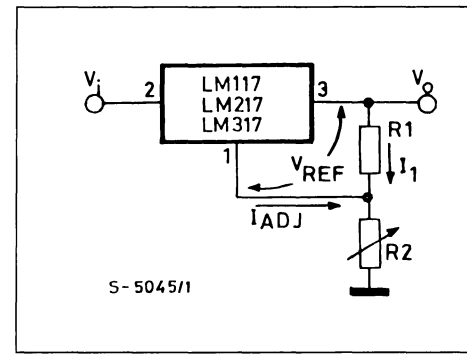


Figure 4 : Basic Adjustable Regulator.



APPLICATION INFORMATION

The LM117/LM217/LM317 provides an internal reference voltage of 1.25V between the output and adjustments terminals. This is used to set a constant current flow across an external resistor divider (see fig. 4), giving an output voltage V_O of :

$$V_O = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,R2$$

The device was designed to minimize the term I_{ADJ} (100µA max) and to maintain it very constant with line and load changes. Usually, the error term $I_{ADJ} \cdot R_2$ can be neglected. To obtain the previous requirement, all the regulator quiescent current is returned to the output terminal, imposing a minimum load current condition. If the load is insufficient, the output voltage will rise.

Since the LM117/LM217/LM317 is a floating regulator and "sees" only the input-to-output differential voltage, supplies of very high voltage with respect to ground can be regulated as long as the maximum input-to-output differential is not exceeded. Furthermore, programmable regulator are easily obtainable and, by connecting a fixed resistor between the adjustment and output, the device can be used as a precision current regulator.

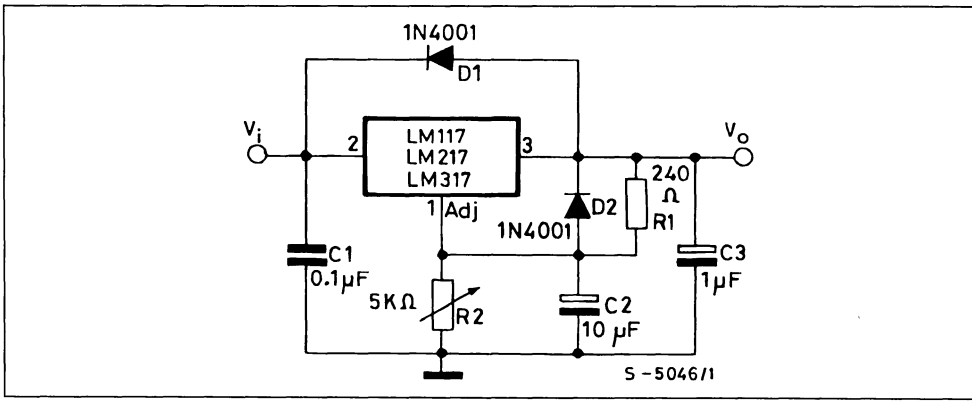
In order to optimise the load regulation, the current set resistor R1 (see fig. 4) should be tied as close as possible to the regulator, while the ground terminal of R2 should be near the ground of the load to provide remote ground sensing.

No external capacitors are required, but performance may be improved with added capacitance as follows :

- An input bypass capacitor of 0.1µF
- An adjustment terminal to ground 10µF capacitor to improve the ripple rejection of about 15dB (C_{ADJ})
- An 1µF tantalum capacitor on the output to improve transient response.

In additional to external capacitors, it is good practice to add protection diodes, as shown in fig. 5.

Figure 5 : Voltage Regulator with Protection Diodes.



D1 protects the device against input short circuit, while D2 protects against output short circuit for capacitors discharging.

Figure 6 : Slow Turn-on 15V Regulator.

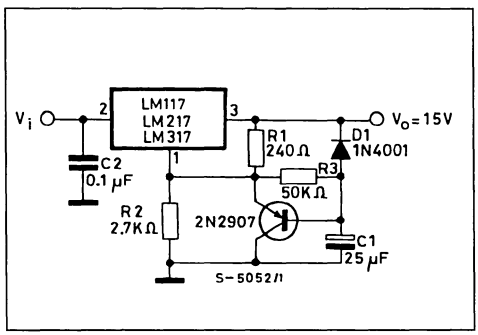


Figure 7 : Current Regulator.

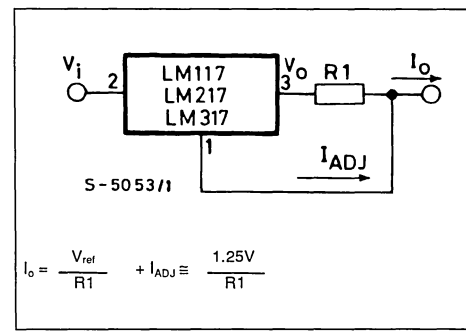


Figure 8 : 5V Electronic Shut-down Regulator.

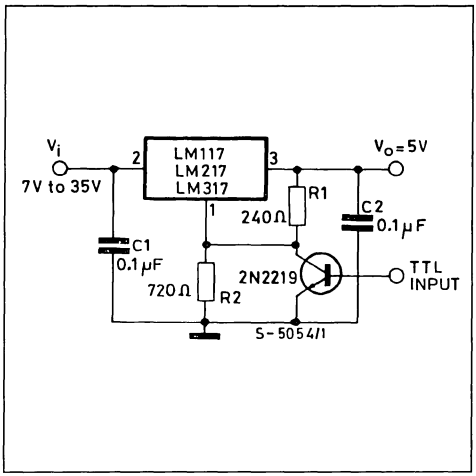


Figure 9 : Digitally Selected Outputs.

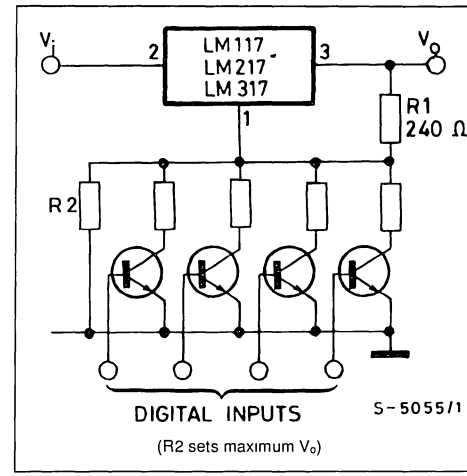
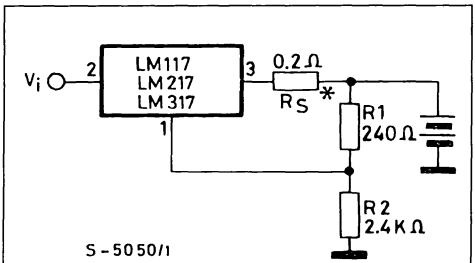


Figure 10 : Battery Charger (12V).

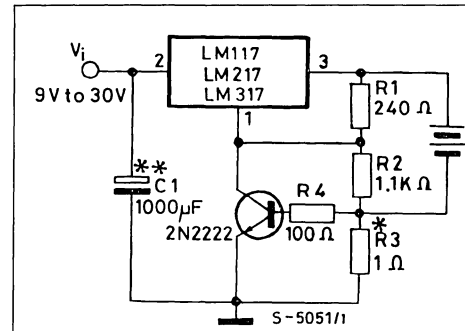


* R_S sets output impedance of charger

$$Z_O = R_S \left(1 + \frac{R2}{R1}\right)$$

Use of R_S allows low charging rates with fully charged battery

Figure 11 : Current Limited 6V Charger.

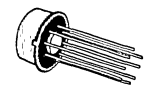


* R3 sets peak current (0.6A for 1Ω).
** C1 recommended to filter out input transients.

LM118-LM218 LM318

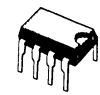
SINGLE OPERATIONAL AMPLIFIERS

- INPUT OFFSET VOLTAGE :
  - 4 mV MAX. LM118 – LM218
  - 10 mV MAX. LM318
- INPUT BIAS CURRENT :
  - 250 nA MAX.
- INPUT OFFSET CURRENT :
  - 50 nA MAX.
- SLEW RATE OF 150 V/µs AS INVERTING AMPLIFIER

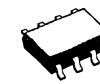


H
TO-99
(Metal Can)

GC
LCC20
(Tricecop (LCC))



N
DIP8
(Plastic Package)
J
CERDIP8
(Cerdip Package)



D
SO8
(Plastic Micropackage)

DESCRIPTION

The LM118, LM218 and LM318 are precision high speed operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature internal frequency compensation and a factor of ten increase in speed over general purpose devices.

Although, no external frequency compensation components are needed for operation, feedforward compensation may be used to further increase the speed. For inverting applications, feedforward compensation will boost the slew rate to over 150 V/µs and almost double the bandwidth. However, for non-inverting or differential applications feedforward cannot be used.

The high speed and fast settling time of these op amps make them useful in A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers.

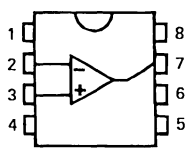
ORDER CODES

Part Number	Temperature Range	Package				
		H	N	J	GC	D
LM118	– 55 to + 125 °C	•		•	•	
LM218	– 40 to + 105 °C	•	•			•
LM318	0 to + 70 °C	•	•			•

Note : Hi-Rel Versions Available
Examples : LM118J, LM218H

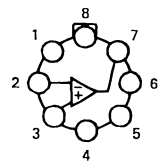
PIN CONNECTIONS

TO-99



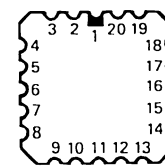
1 - Balance/Compensation 1
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-

DIP8/CERDIP8/ SO8



5 - Balance/Compensation 3
6 - Output
7 - V_{CC}^+

LCC 20



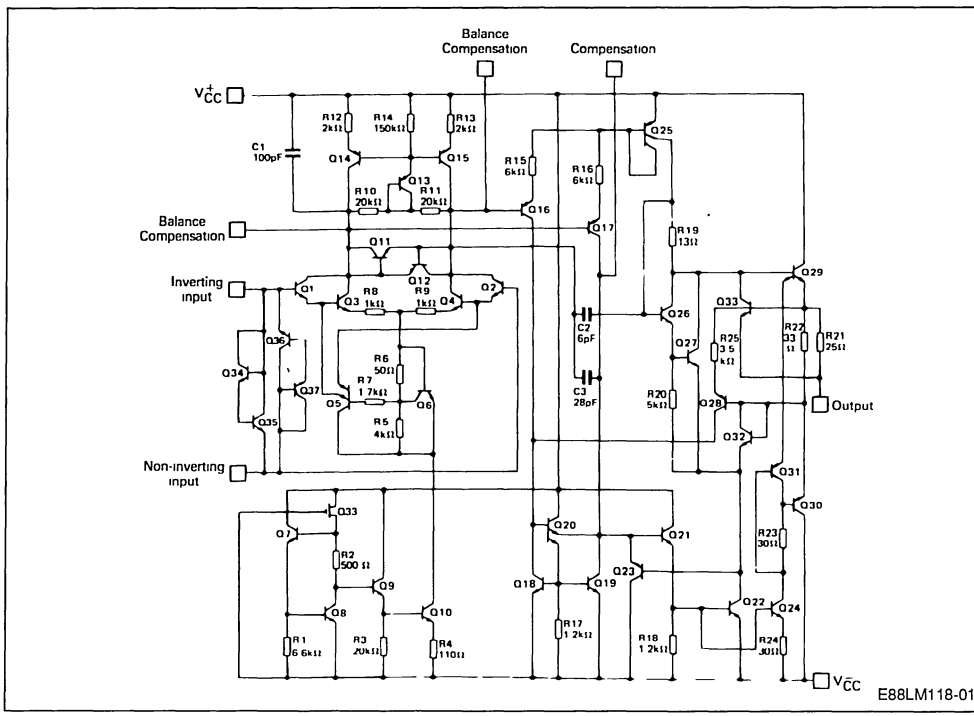
1 - NC
2 - Balance/Compensation 1
3 - NC
4 - NC
5 - Inverting input
6 - NC
7 - Non-inverting input
8 - NC
9 - NC
10 - V_{CC}^-
11 - NC
12 - Balance/Compensation 3
13 - NC
14 - NC
15 - Output
16 - NC
17 - V_{CC}^+
18 - NC
19 - NC
20 - Compensation 2

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM118	LM218	LM318	Unit
V_{CC}	Supply Voltage	± 20	± 20	± 20	V
V_I	Input Voltage (note 1)	± 15	± 15	± 15	V
I_{ID}	Differential Input Current (note 2)	± 10	± 10	± 10	mA
	Output Short-circuit Duration	Indefinite	Indefinite	Indefinite	
P_{tot}	Power Dissipation LM318D All other Versions	 500	 500	300 500	mW
T_{oper}	Operating Free-air Temperature Range	− 55 to + 125	− 40 to + 105	0 to + 70	°C
T_{stg}	Storage Temperature Range	− 65 to + 150	− 65 to + 150	− 65 to + 150	°C

Notes : 1. For supply voltage less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage
2. The inputs are shunted with shunt diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1 V is applied between the inputs unless some limiting resistance is used.

SCHEMATIC DIAGRAM



Case	Balance Compensation	Inverting Input	Non-inverting Input	V_{CC}^-	V_{CC}^+	Output	Compensation	N.C.
TO99/DIP8 CERDIP8/SO8	1, 5	2	3	4	7	6	8	
LCC20	2, 12	5	7	10	17	15	20	•

*** LCC20 :** Other pins are not connected.

ELECTRICAL CHARACTERISTICS

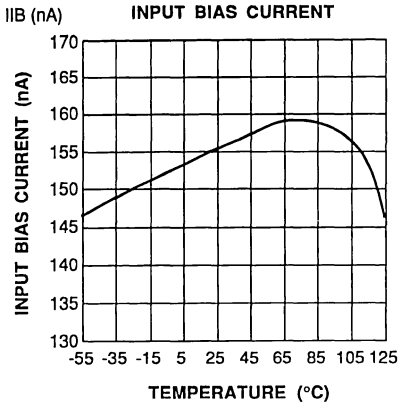
LM318 : $0 \leq T_{amb} \leq +70$ °C $\pm 5\ V \leq V_{CC} \leq \pm 20\ V$ $C_1 = 30$ pF
LM218 : $-40 \leq T_{amb} \leq +105$ °C $\pm 5\ V \leq V_{CC} \leq \pm 20\ V$ $C_1 = 30$ pF
LM118 : $-55 \leq T_{amb} \leq +125$ °C $\pm 5\ V \leq V_{CC} \leq \pm 20\ V$ $C_1 = 30$ pF
* => $V_{CC} = \pm 15$ V
(unless otherwise specified)

Symbol	Parameter	LM118, LM218			LM318			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage $R_S \leq 10$ kΩ $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$		2	4 6		2	10 15	mV
I_{IB}	Input Bias Current $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$		160	250 500		160	250 500	nA
I_{IO}	Input Offset Current $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$		6	50 100		6	50 100	nA
A_{VD}	Large Signal Voltage Gain * ($V_O = \pm 10$ V, $R_L \geq 2$ kΩ) $T_{amb} = 25$ °C $T_{min} < T_{amb} \leq T_{max}$	 50 25	 200		 50 25	 200		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S \leq 10$ kΩ) $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$	 70 70	 97		 70 70	 97		dB
I_{CC}	Supply Current, no Load $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$		5	8 15		5	10 15	mA
V_I	Input Voltage Range * $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$	− 11.5 − 11.5		11.5 11.5	− 11.5 − 11.5		11.5 11.5	V
CMR	Common Mode rejection Ratio * ($R_S \leq 10$ kΩ) $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$	 80 80	 105		 80 80	 105		dB
I_{OS}	Output Short-circuit Current * $T_{amb} = 25$ °C	10	30	60	10	30	60	mA
$\pm V_{OPP}$	Output Voltage Swing * $T_{amb} = 25$ °C $R_L = 2$ kΩ $T_{min} \leq T_{amb} \leq T_{max}$	12 12	13		12 12	13		V
S_{VO}	Slew-rate ($V_I = \pm 10$ V, $R_L = 2$ kΩ, $C_L \leq 100$ pF, * $T_{amb} = 25$ °C, unity gain) (note 3)	50	70		50	70		V/μs
Z_I	Input Impedance, $T_{amb} = 25$ °C *	1	3		1	3		MΩ

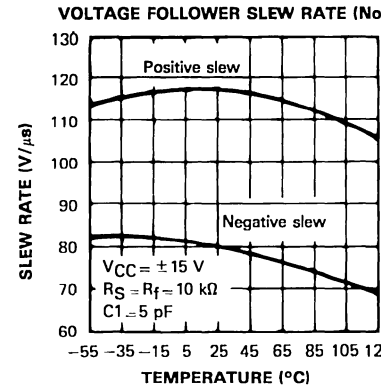
Note : 3 May be improved up to 150 V/μs in inverting amplifier configuration (see typical application)

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	LM118, LM218			LM318			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
GBP	Gain Bandwidth Product * (V_I = 10 mV, R_L = 2 kΩ, C_L ≤ 100 pF, f = 100 kHz, T_{amb} = 25 °C)		50			50		MHz
THD	Total Harmonic Distortion * (f = 1 kHz, A_V = 20 dB, R_L = 2 kΩ, V_O = 2 V_{PP}, C_L ≤ 100 pF, T_{amb} = 25 °C)		.008			.008		%
V_n	Equivalent Input Noise Voltage * (f = 1 kHz, Rg = 100 Ω)		17			17		nV/√Hz



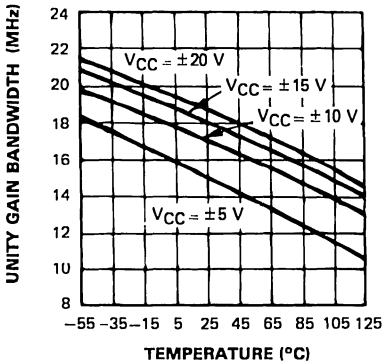
E88LM118-02



E88LM118-03

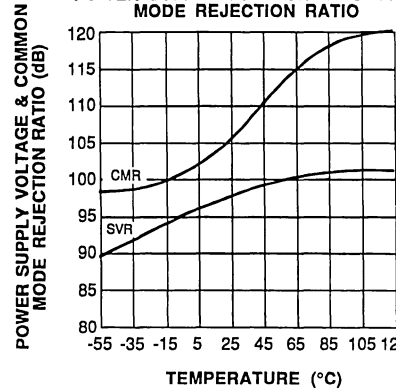
Note : 5. **LM118 :** − 55 °C ≤ T_{amb} ≤ + 125 °C, ± 5 V ≤ V_{CC} ≤ ± 20 V
LM218 : − 40 °C ≤ T_{amb} ≤ + 105 °C, ± 5 V ≤ V_{CC} ≤ ± 20 V
LM318 : − 0 °C ≤ T_{amb} ≤ + 70 °C, ± 5 V ≤ V_{CC} ≤ ± 20 V

UNITY GAIN BANDWIDTH (GAIN : 1) (Note 5)



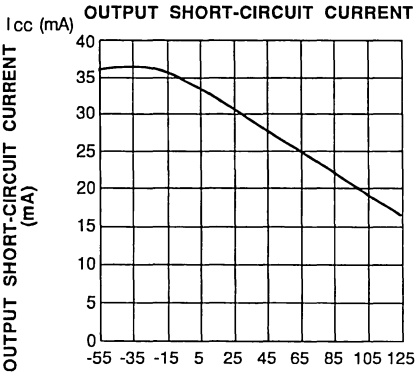
E88LM118-04

POWER SUPPLY VOLTAGE & COMMON MODE REJECTION RATIO



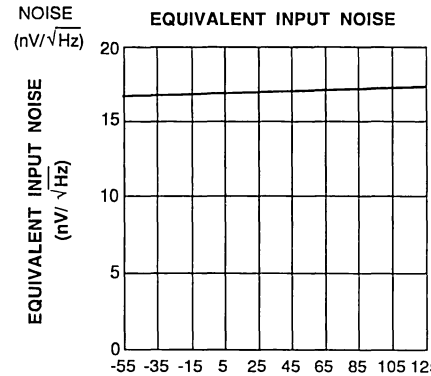
E88LM118-38

OUTPUT SHORT-CIRCUIT CURRENT



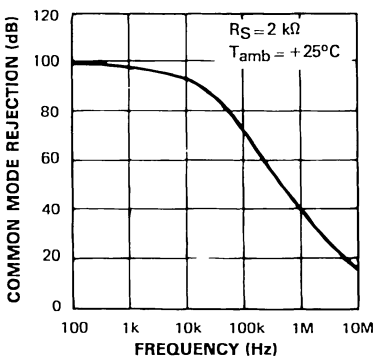
E88LM118-37

EQUIVALENT INPUT NOISE



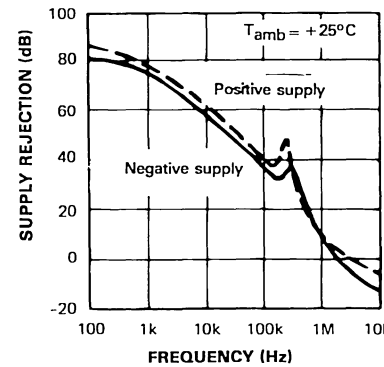
E88LM118-36

COMMON MODE REJECTION

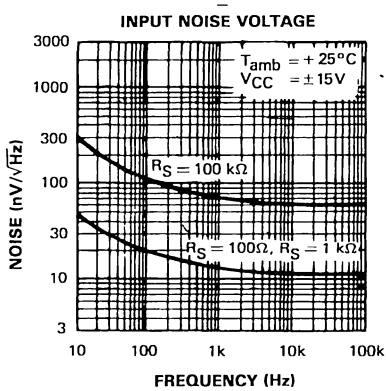


E88LM118-05

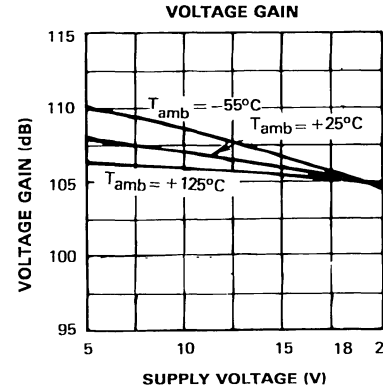
POWER SUPPLY REJECTION



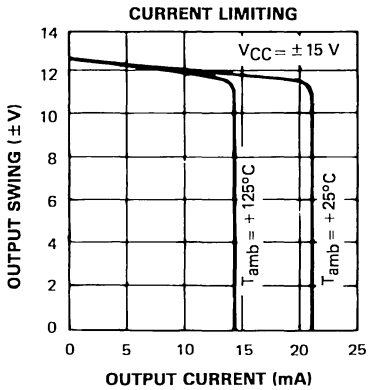
E88LM118-06



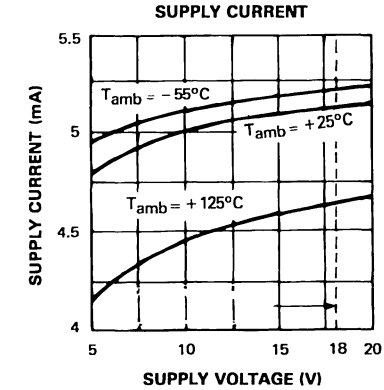
E88LM118-07



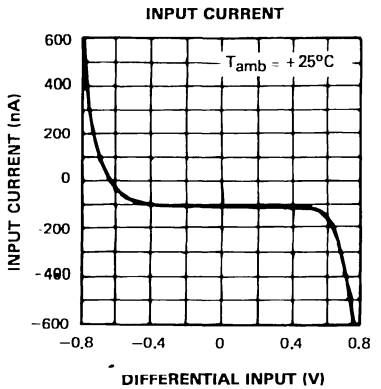
E88LM118-08



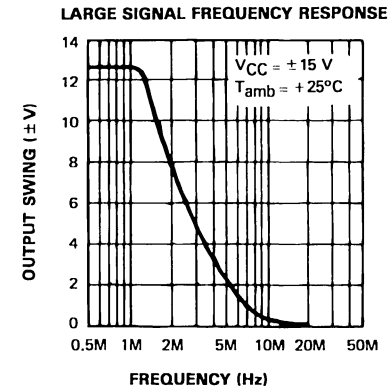
E88LM118-09



E88LM118-14

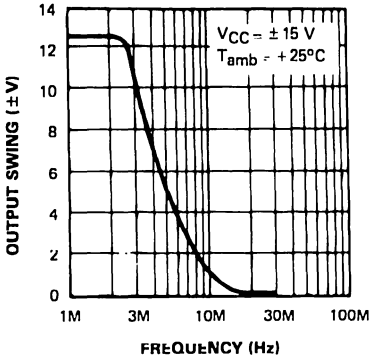


E88LM118-15



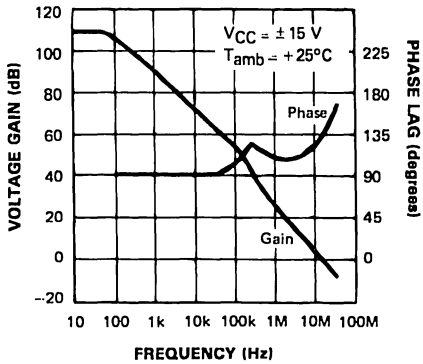
E88LM118-20

LARGE SIGNAL FREQUENCY RESPONSE*



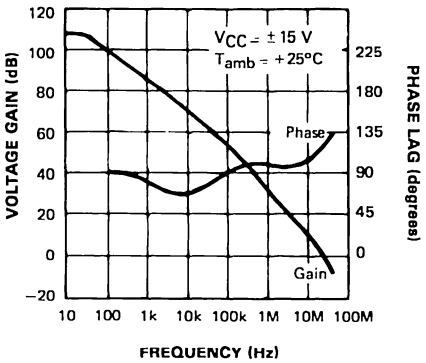
E88LM118-21

OPEN LOOP FREQUENCY RESPONSE



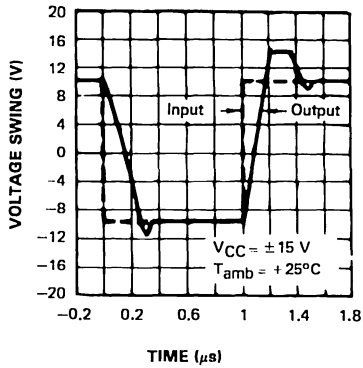
E88LM118-22

OPEN LOOP FREQUENCY RESPONSE*



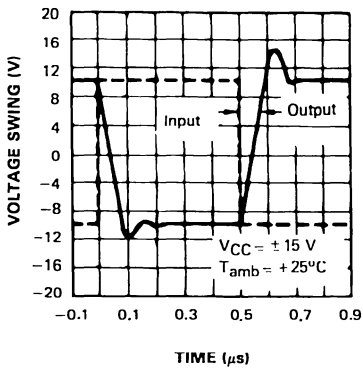
E88LM118-23

VOLTAGE FOLLOWER PULSE RESPONSE



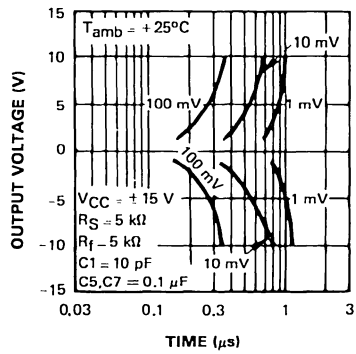
E88LM118-24

INVERTER PULSE RESPONSE*



E88LM118-25

INVERTER SETTLING TIME

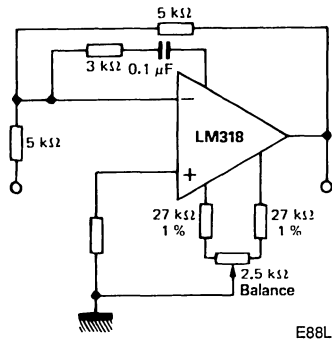


E88LM118-26

* With feedforward compensation

BASIC DIAGRAMS

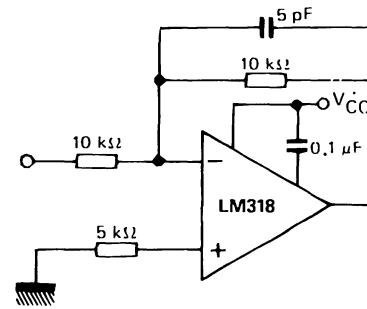
FEEDFORWARD COMPENSATION FOR GREATER INVERTING SLEW RATE*



E88LM118-28

* Slew rate typically 150 V/µs.

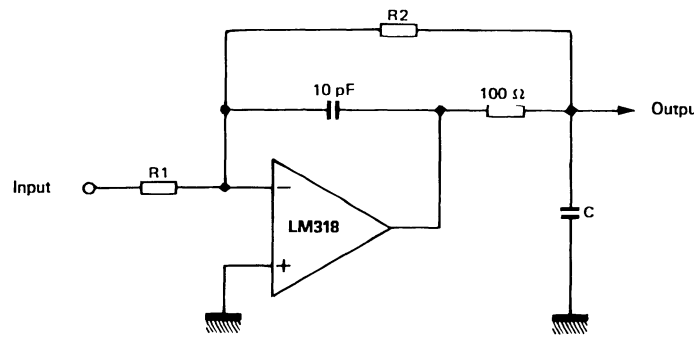
COMPENSATION FOR MINIMUM SETTLING TIME*



E88LM118-29

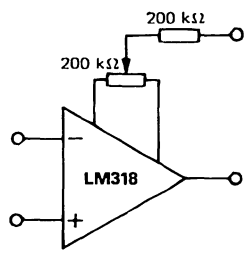
* Slew and settling time to 0.1 % for a 10 V step change is 800 ns

ISOLATING LARGE CAPACITIVE LOADS



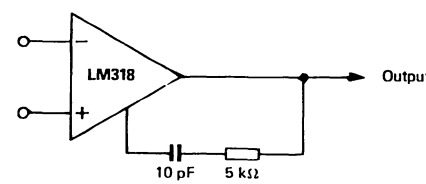
E88LM118-30

OFFSET BALANCING



E88LM118-31

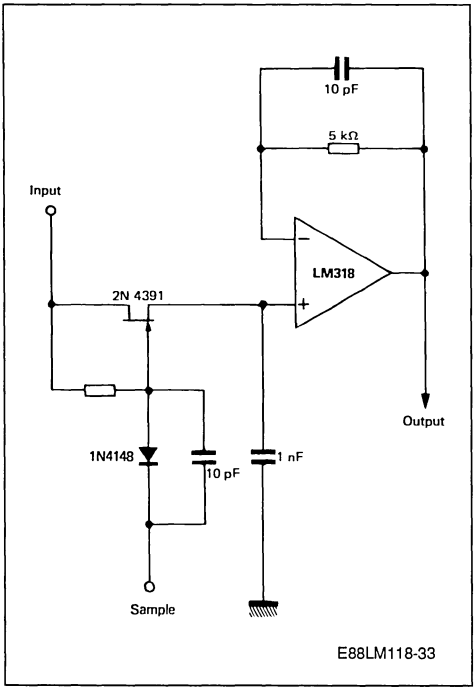
OVERCOMPENSATION



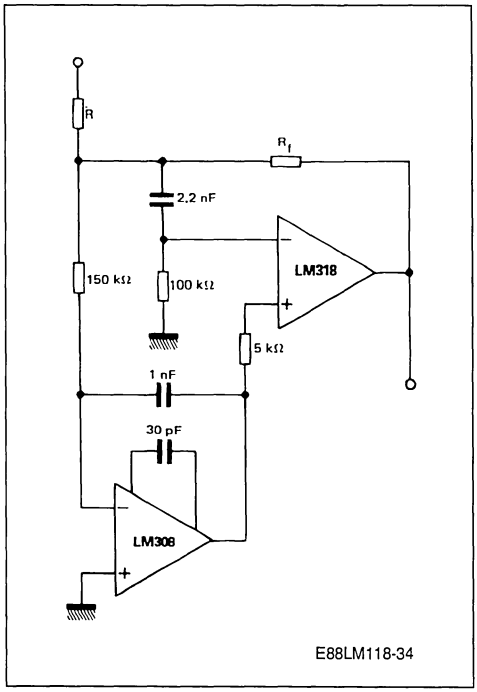
E88LM118-32

TYPICAL APPLICATION DIAGRAM

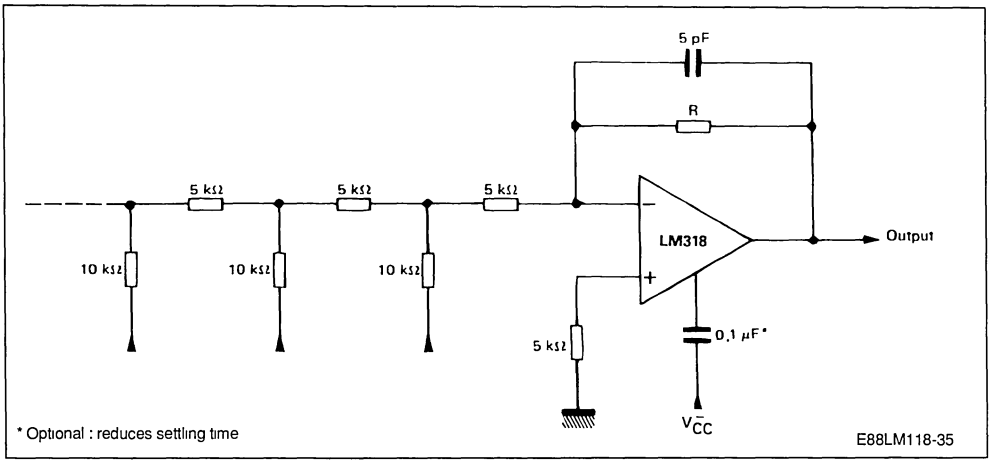
FAST SAMPLE AND HOLD



FAST SUMMING AMPLIFIER WITH LOW INPUT CURRENT

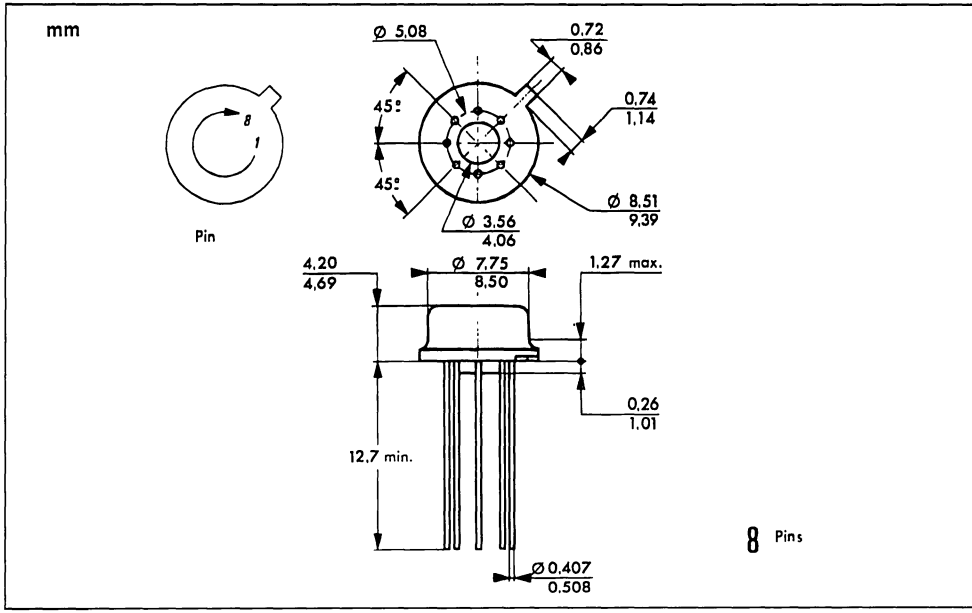


D/A CONVERTER USING LADDER NETWORK

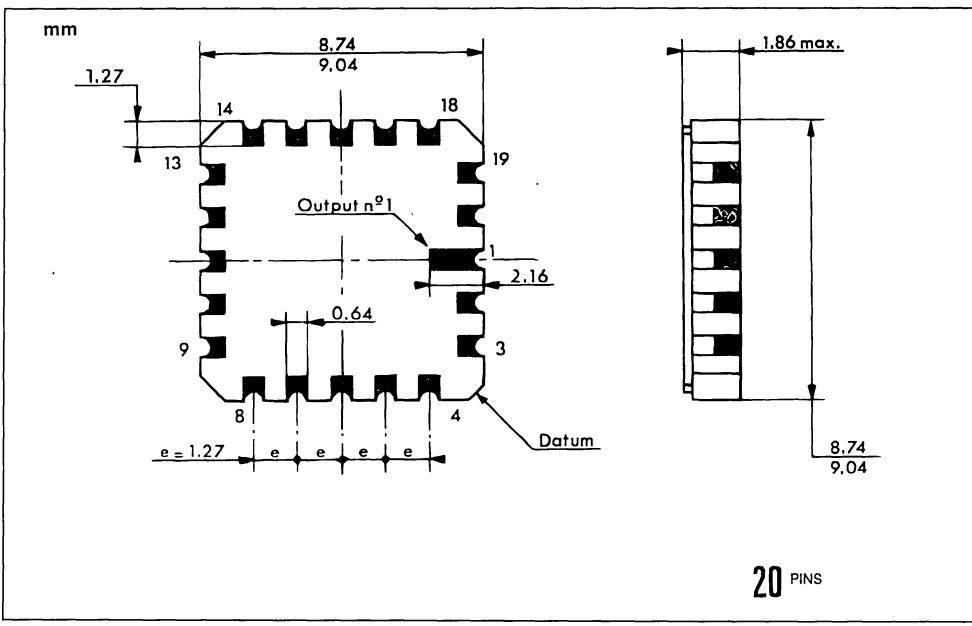


PACKAGE MECHANICAL DATA

8 PINS – TO-99 – METAL CAN

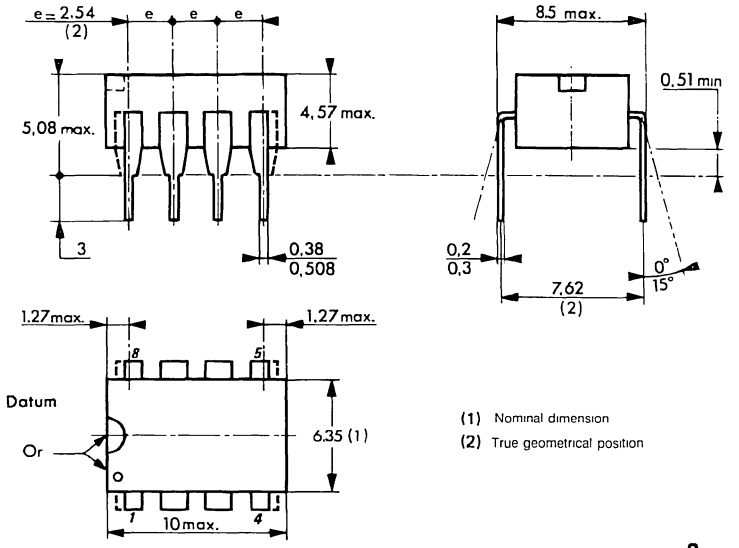


20 PINS – TRICECOP (LCC)

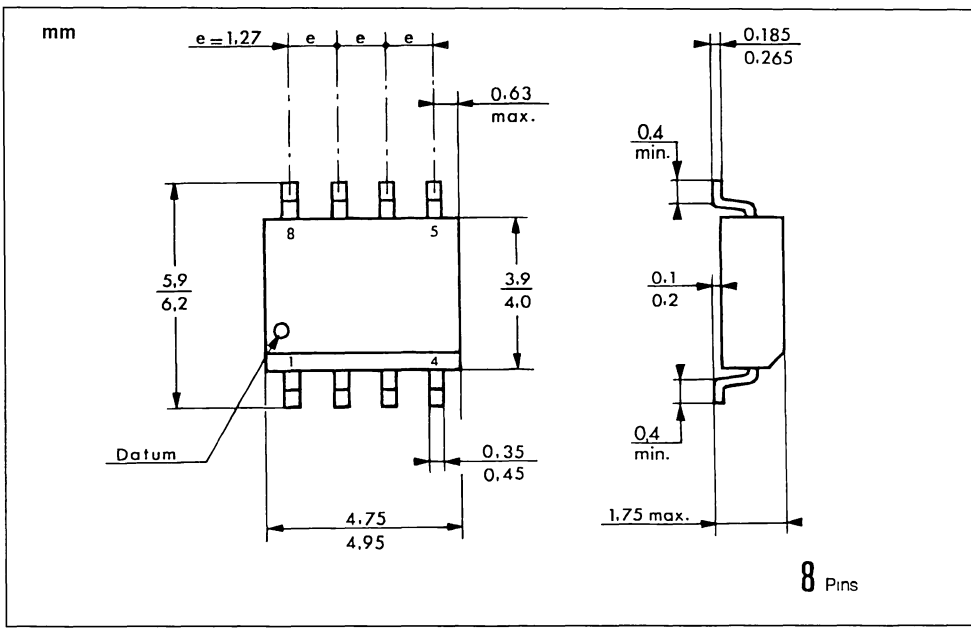


PACKAGE MECHANICAL DATA (continued)

8 PINS – PLASTIC DIP OR CERDIP



8 PINS – PLASTIC MICROPACKAGE (SO)

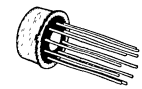


SGS-THOMSON MICROELECTRONICS

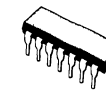
LM119 - LM219 LM319

HIGH SPEED DUAL COMPARATORS

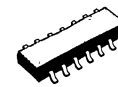
- TWO INDEPENDENT COMPARATORS
- OPERATION FROM A SINGLE + 5 V SUPPLY
- TYPICALLY 80 ns RESPONSE TIME AT ± 15 V
- MINIMUM FAN-OUT OF 2 EACH SIDE
- MAXIMUM INPUT CURRENT OF 1 µA OVER OPERATING TEMPERATURE RANGE
- INPUTS AND OUTPUTS CAN BE ISOLATED FROM SYSTEM GROUND
- HIGH COMMON-MODE SLEW RATE



H
TO-100
(Metal Can)



N
DIP14
(Plastic Package)
J
CERDIP14
(Cerdip Package)



D
SO14
(Plastic Micropackage)

GC
LCC20
(Tricecop (LCC))

DESCRIPTION

These products are precision high speed dual comparators designed to operate over a wide range of supply voltages down to a single 5 V logic supply and ground and have low input currents and high gains.

The open collector of the output stage makes compatible with TTL as well as capable of driving lamps and relays at currents up to 25 mA.

Although designed primarily for applications requiring operation from digital logic supplies, are fully specified for power supplies up to 15 V.

They feature faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the much more versatile.

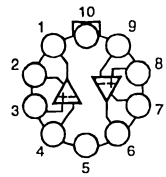
ORDER CODES

Part Number	Temperature Range	Package				
		H	N	J	D	GC
LM119	– 55 to + 125 °C	•		•		•
LM219	– 40 to + 105 °C	•	•	•	•	
LM319	0 to + 70 °C	•	•	•	•	

Note : Hi-Rel Versions Available.
Examples : LM119H, LM219N.

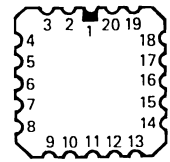
PIN CONNECTIONS (top views)

TO100



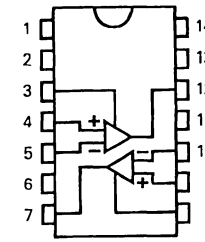
1 - Output 1
2 - Ground 1
3 - Non-inverting input 1
4 - Inverting input 1
5 - V_{CC}^-
6 - Output 2
7 - Ground 2
8 - Non-inverting input 2
9 - Inverting input 2
10 - V_{CC}^+

LCC20



1 - NC
2 - NC
3 - NC
4 - Ground 1
5 - NC
6 - Non-inverting input 1
7 - NC
8 - Inverting input 1
9 - V_{CC}^-
10 - Output 2
11 - NC
12 - Ground 2
13 - Non-inverting input2
14 - Inverting input 2
15 - NC
16 - V_{CC}^+
17 - NC
18 - Output 1
19 - NC
20 - NC

DIP14/CERDIP14
SO14



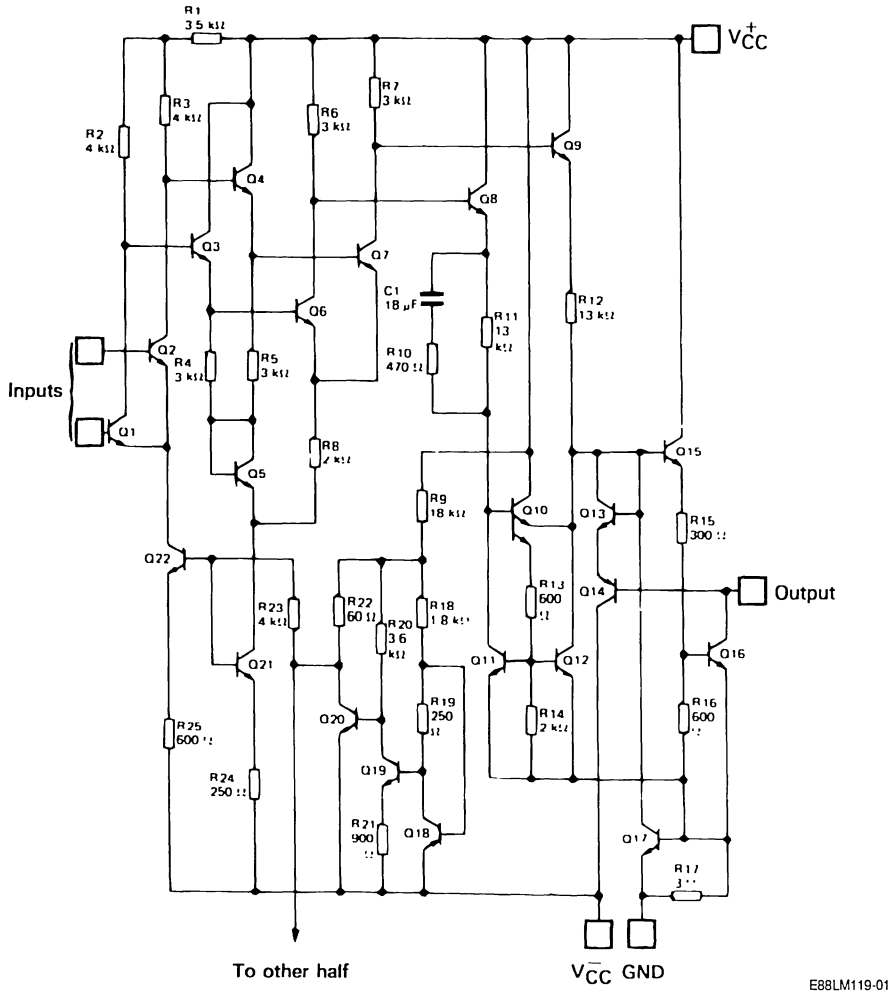
1 - NC
2 - NC
3 - Ground 1
4 - Non-inverting input 1
5 - Inverting input 1
6 - V_{CC}^-
7 - Output 2
8 - Ground 2
9 - Non- inverting input 2
10 - Inverting input 2
11 - V_{CC}^+
12 - Output 1
13 - NC
14 - NC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM119	LM219	LM319	Unit
$V_O - V_{CC}^-$	Output to Negative Supply Voltage	36	36	36	V
V_{CC}^-	Negative Supply Voltage	25	25	25	V
V_{CC}^+	Positive Supply Voltage	18	18	18	V
V_{ID}	Differential Input Voltage	± 5	± 5	± 5	V
V_I	Input Voltage – (note 1)	± 15	± 15	± 15	V
P_{tot}	Power Dissipation – (note 2)	500	500	500	mW
T_{oper}	Operating Free-air Temperature Range	– 55 to + 125	– 40 to + 105	0 to + 70	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	– 65 to + 150	– 65 to + 150	°C

* All potentials referenced to ground unless otherwise specified.

SCHEMATIC DIAGRAM



CASE	Outputs	Inverting Inputs	Non-inverting Inputs	GND	V_{CC}^+	V_{CC}^-	N.C.
TO100	1, 6	4, 9	3, 8	2, 7	10	5	–
DIP14/ CERDIP14/ SO14	7, 12	5, 10	4, 9	3, 8	11	6	1, 2, 13, 14
LCC20	10, 18	8, 14	6, 13	4, 12	16	9	*

* LCC20 : Other pins are not connected.

ELECTRICAL CHARACTERISTICS

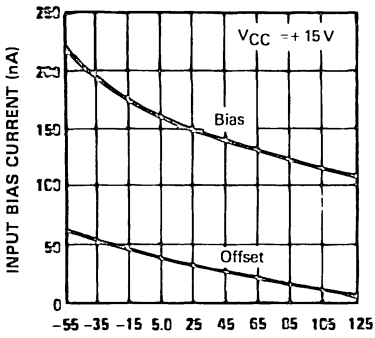
LM119 : – 55 °C ≤ T_{amb} ≤ + 125 °C, V_{CC} = ± 15 V
LM219 : – 40 °C ≤ T_{amb} ≤ + 105 °C, V_{CC} = ± 15 V
LM319 : 0 °C ≤ T_{amb} ≤ + 70 °C, V_{CC} = ± 15 V
(unless otherwise specified)

Symbol	Parameter	LM119, LM219			LM319			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage (R_S ≤ 5 kΩ) – (note 3)							mV
	T_{amb} = + 25 °C	–	0.7	4	–	2	8	
	T_{min} ≤ T_{amb} ≤ T_{max}	–	–	7	–	–	10	
I_{IO}	Input Offset Current – (note 3)							nA
	T_{amb} = + 25 °C	–	30	75	–	80	200	
	T_{min} ≤ T_{amb} ≤ T_{max}	–	–	100	–	–	300	
I_{IB}	Input Bias Current – (note 3)							nA
	T_{amb} = + 25 °C	–	150	500	–	250	1000	
	T_{min} ≤ T_{amb} ≤ T_{max}	–	–	1000	–	–	1200	
A_{VD}	Large Signal Voltage Gain (T_{amb} = + 25 °C)	10	40	–	8	40	–	V/mV
I_{CC}^{+}	Positive Supply Current							mA
	T_{amb} = + 25 °C, V_{CC} = ± 15 V	–	8	11.5	–	8	12.5	
	T_{min} ≤ T_{amb} ≤ T_{max}, V_{CC}^{+} = + 5 V, V_{CC}^{-} = 0 V	–	4.3	–	–	4.3	–	
I_{CC}^{-}	Negative Supply Current (T_{amb} = + 25 °C)	–	3	4.5	–	3	5	mA
V_I	Input Voltage Range	–	± 13	–	–	± 13	–	V
	(V_{CC}^{+} = + 5 V, V_{CC}^{-} = 0 V)	1	–	3	1	–	3	
V_{ID}	Differential Input Voltage	–	–	± 5	–	–	± 5	V
V_{OL}	Low Level Output Voltage							V
	T_{amb} = + 25 °C, I_O = 25 mA							
	V_I < – 5 mV	–	0.75	1.5	–	–	–	
	V_I < – 10 mV	–	–	–	–	0.75	1.5	
	0 °C ≤ T_{amb} ≤ T_{max}	–	–	0.6	–	–	–	
	V_{CC}^{+} > + 4.5 V, V_{CC}^{-} = 0 V, V_I < – 6 mV,							
	$I_{O(sink)}$ < 3.2 mA	–	0.23	0.4	–	–	–	
	T_{min} ≤ T_{amb} ≤ T_{max}							
	V_{CC}^{+} > + 4.5 V, V_{CC}^{-} = 0 V, V_I < – 10 mV,							
	$I_{O(sink)}$ < 3.2 mA	–	–	–	–	0.3	0.4	
I_{OH}	High Level Output Current (V_O = + 35 V)							µA
	T_{amb} = + 25 °C, V_I > + 5 mV	–	0.2	2	–	–	–	
	V_I > + 10 mV	–	–	–	–	0.2	10	
	T_{min} ≤ T_{amb} ≤ T_{max}, V_I > 5 mV	–	1	10	–	–	–	
t_{re}	Rise Time (T_{amb} = + 25 °C) – (note 4)	–	80	–	–	80	–	ns

Notes : 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage
2. TO100 · $R_{th(j-a)}$ = 160 °C/W, $R_{th(j-c)}$ = 45 °C/W
DIP14 · $R_{th(j-a)}$ = 150 °C/W
SO14 $R_{th(j-a)}$ = 250 °C/W
3 These specifications apply for V_{CC} = ± 15 V, unless otherwise stated The offset voltage, offset current and bias current specifications apply for any supply voltage from a single + 5 V supply up to ± 15 V supplies
The offset voltages and offset current given are the maximum values required to drive the output down to 1 V or up to + 14 V with a 1 mA load current
Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
4. The response time specified is for a 100 mV input step with 5 mV overdrive.

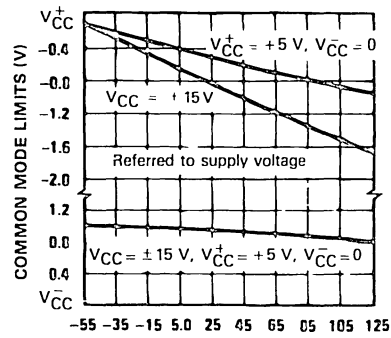
LM119-LM219

INPUT BIAS CURRENTS



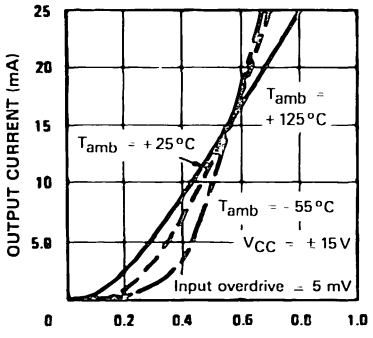
E88LM119-02

COMMON MODE LIMITS



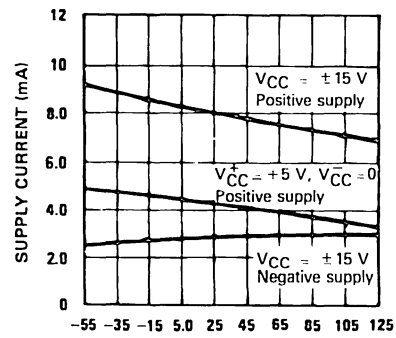
E88LM119-03

OUTPUT SATURATION VOLTAGE



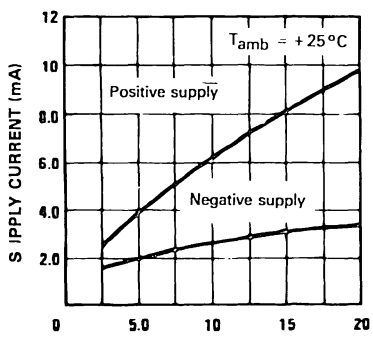
E88LM119-04

SUPPLY CURRENT



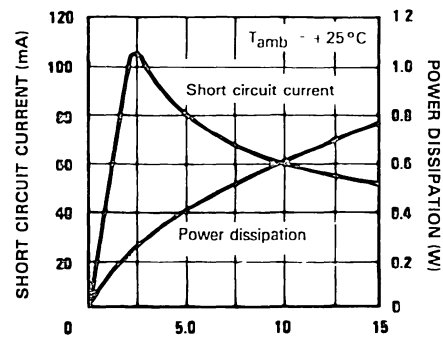
E88LM119-05

SUPPLY CURRENT



E88LM119-06

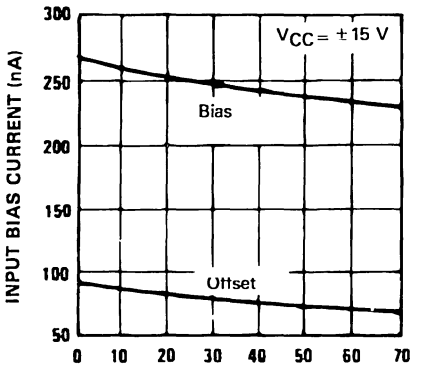
OUTPUT LIMITING CHARACTERISTICS



E88LM119-07

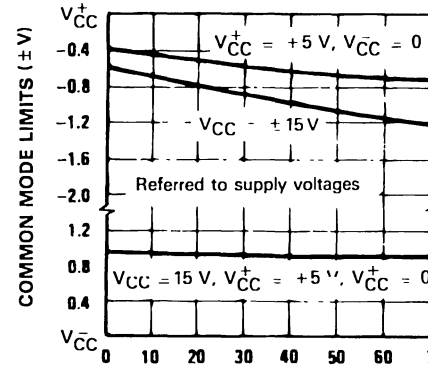
LM319

INPUT BIAS CURRENTS



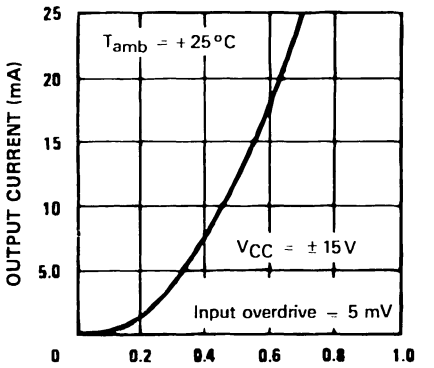
E88LM119-08

COMMON MODE LIMITS



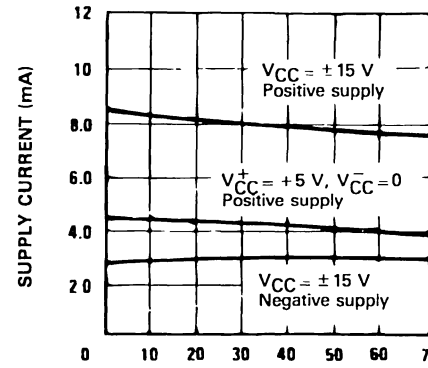
E88LM119-09

OUTPUT SATURATION VOLTAGE



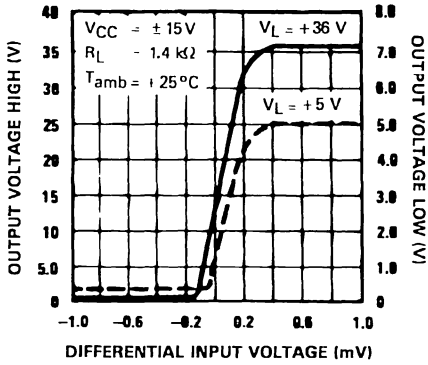
E88LM119-10

SUPPLY CURRENT



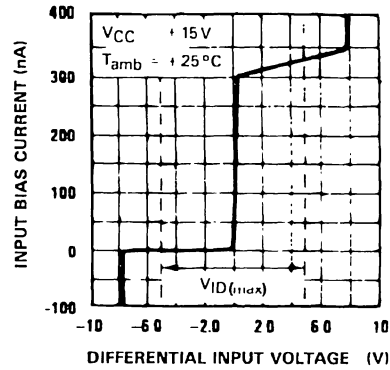
E88LM119-11

TRANSFER FUNCTION



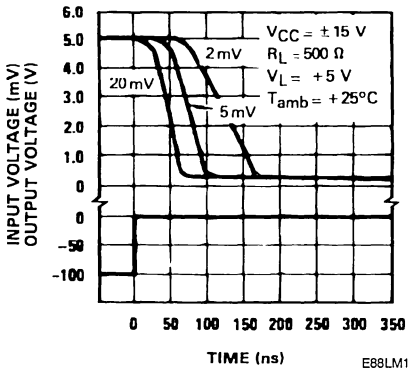
E88LM119-12

INPUT CHARACTERISTICS



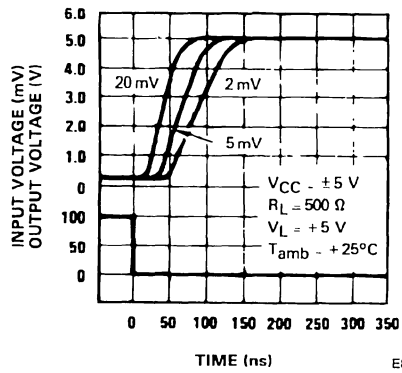
E88LM119-13

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



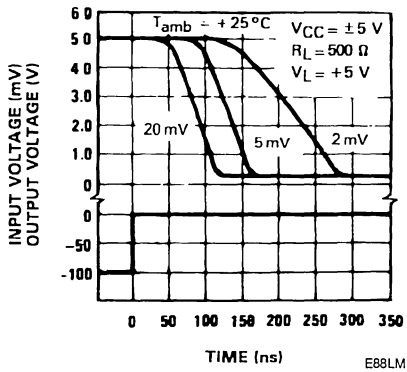
E88LM119-15

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



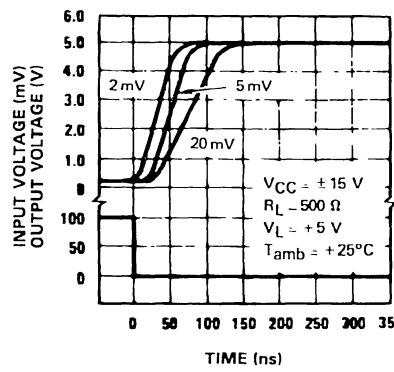
E88LM119-15

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



E88LM119-16

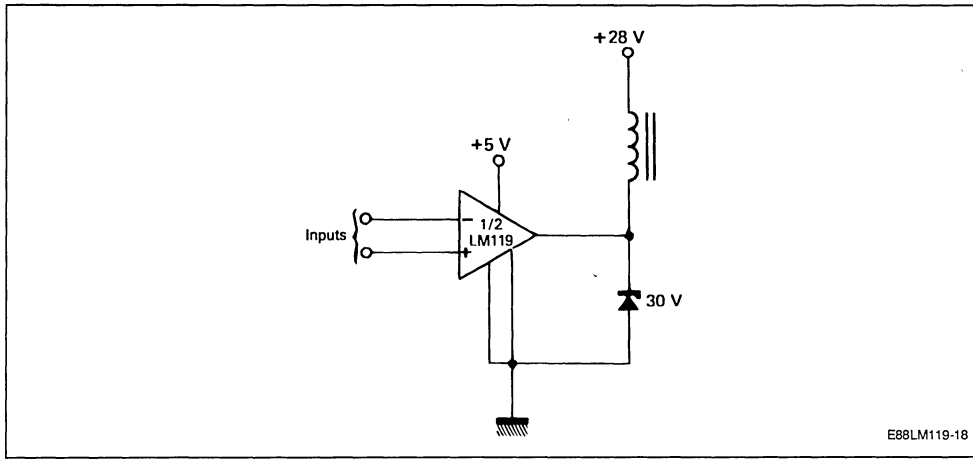
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



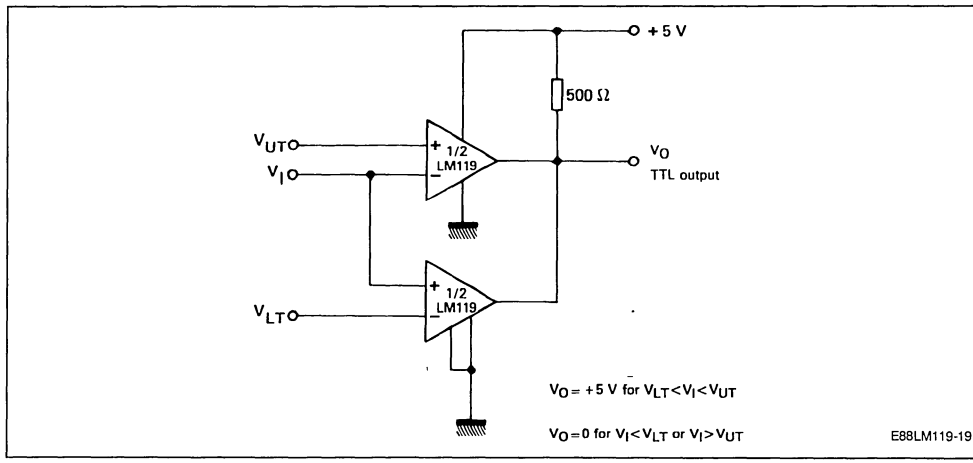
E88LM119-17

TYPICAL APPLICATION DIAGRAMS

RELAY DRIVER

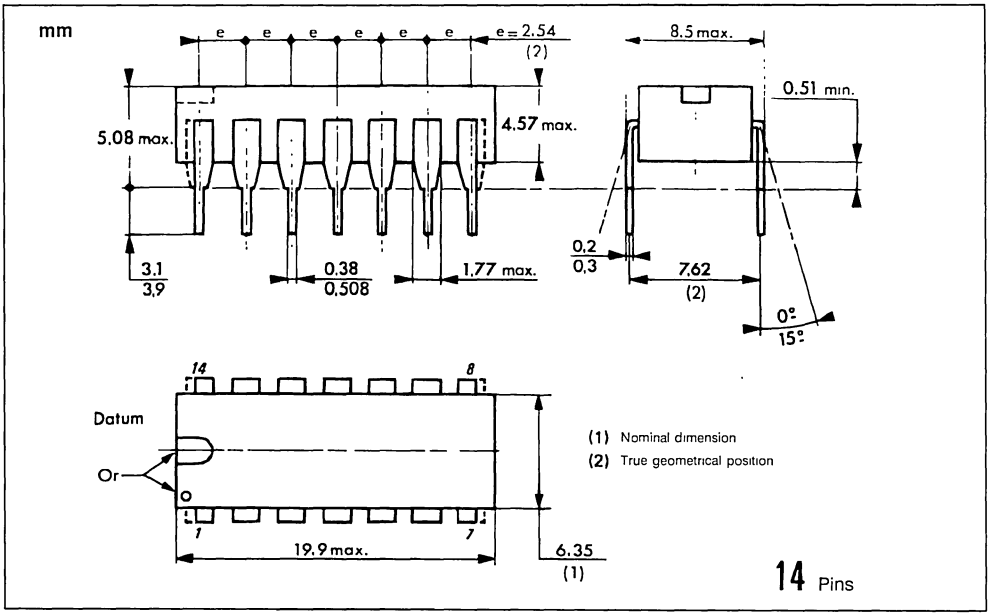


WINDOW DETECTOR

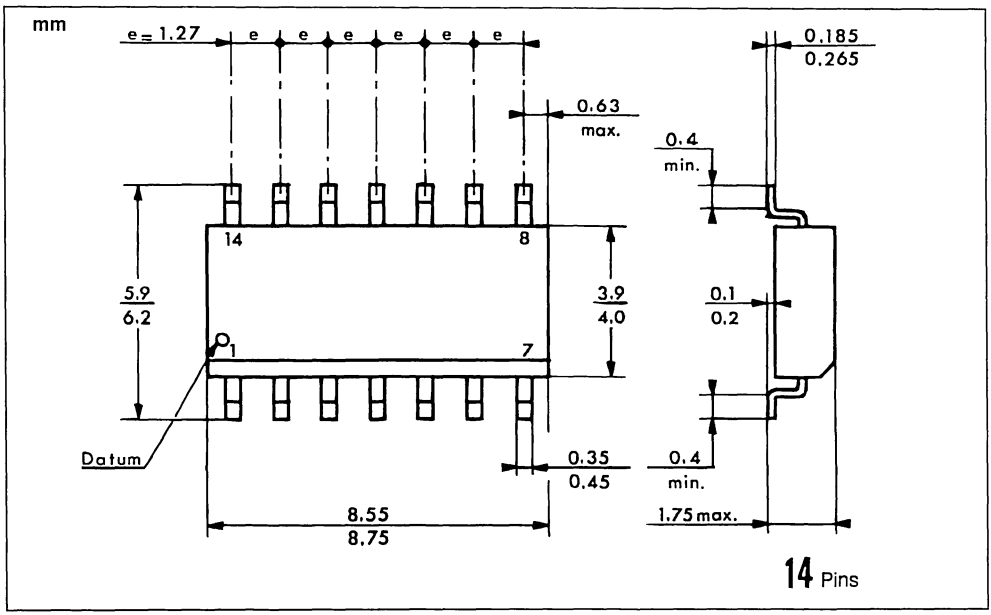


PACKAGE MECHANICAL DATA

14 PINS – PLASTIC DIP OR CERDIP

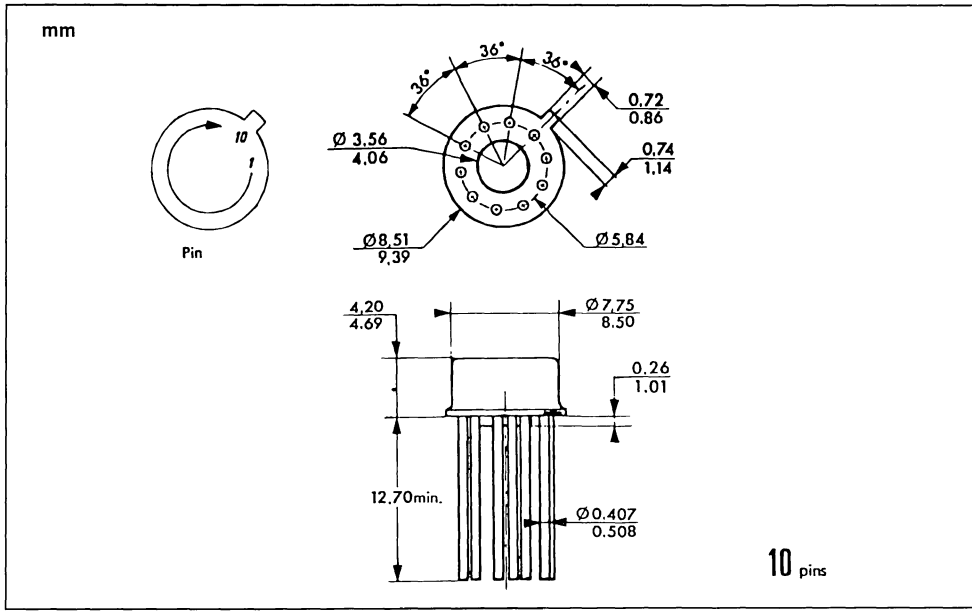


14 PINS – PLASTIC MICROPACKAGE (SO)

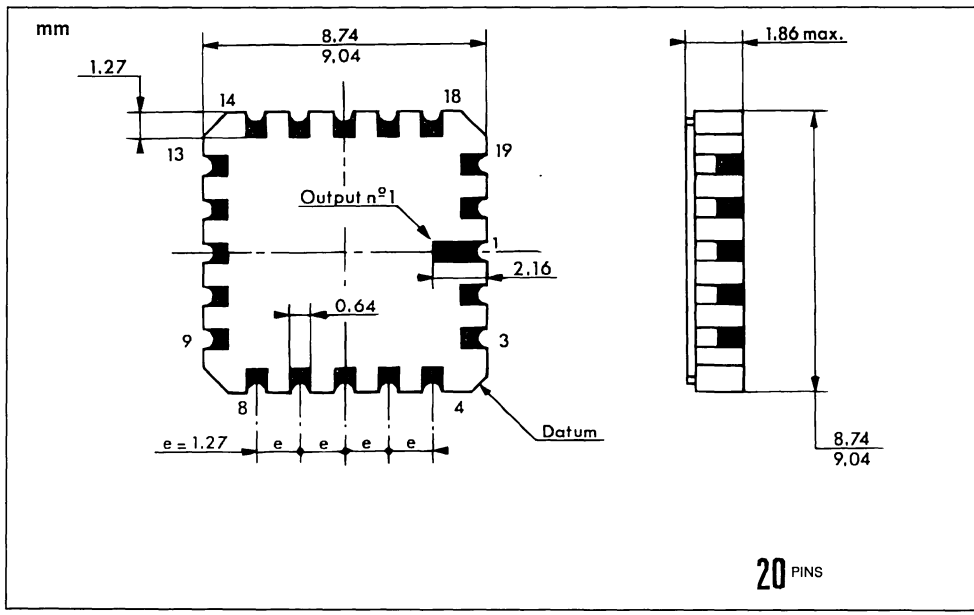


PACKAGE MECHANICAL DATA (continued)

10 PINS – METAL CAN TO100



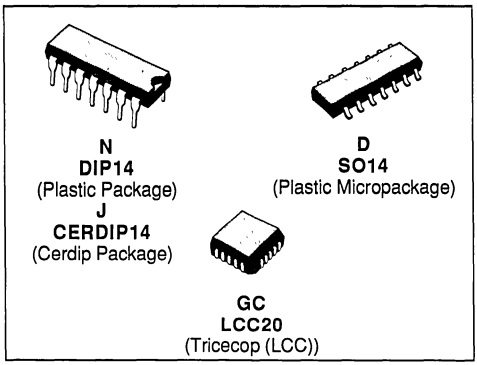
20 PINS – TRICECOP (LCC)



LM124,A-LM224,A LM324,A-LM2902

LOW POWER QUAD OPERATIONAL AMPLIFIERS

- LARGE VOLTAGE GAIN : 100 dB
- VERY LOW SUPPLY CURRENT/AMPLI : 375 µA
- LOW INPUT BIAS CURRENT : 20 nA
- LOW INPUT OFFSET VOLTAGE : 2 mV
- LOW INPUT OFFSET CURRENT : 2 nA
- WIDE POWER SUPPLY RANGE :
  - SINGLE SUPPLY : + 3 V TO + 30 V
  - DUAL SUPPLIES : ± 1.5 V TO ± 15 V



DESCRIPTION

These circuits consist of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically for automotive and industrial control systems. They operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

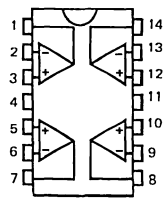
ORDER CODES

Part Number	Temperature Range	Package			
		N	J	GC	D
LM124,A	– 55 °C to + 125 °C	•	•	•	•
LM224,A	– 40 °C to + 105 °C	•	•		•
LM324,A	0 °C to + 70 °C	•	•		•
LM2902	– 40 °C to + 105 °C	•	•		•

Note : Hi-Rel Versions Available
Examples : LM124J, LM124GC, LM224N

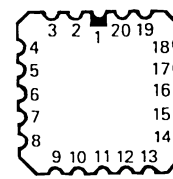
PIN CONNECTIONS (top views)

DIP14/CERDIP14
SO14



1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^+
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - Output 3
9 - Inverting input 3
10 - Non-inverting input 3
11 - V_{CC}^-
12 - Non inverting input 4
13 - Inverting input 4
14 - Output 4

LCC20

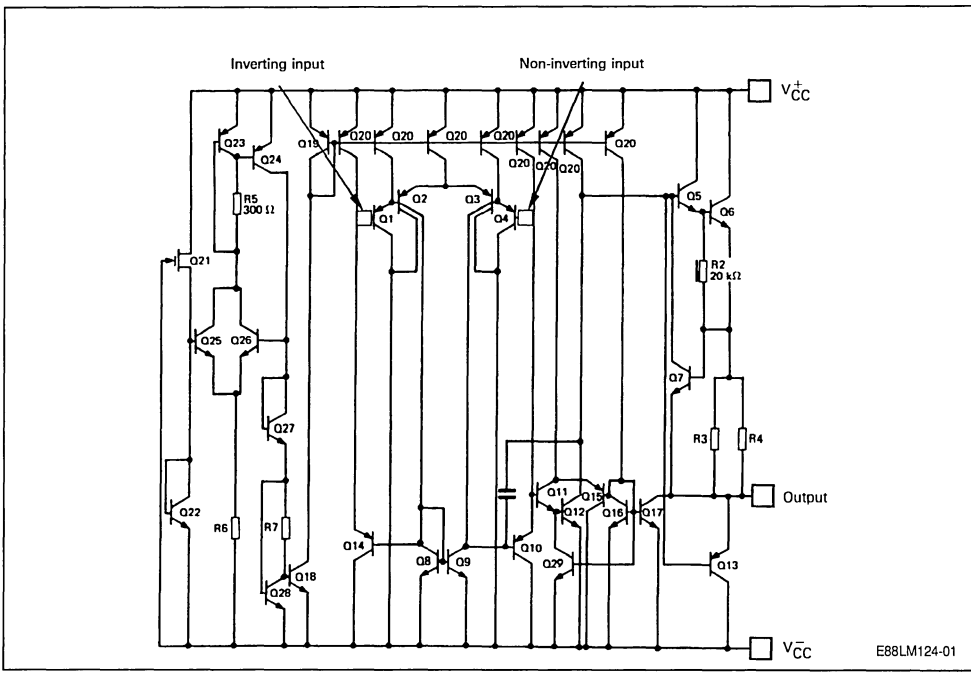


1 - NC
2 - Output 1
3 - Inverting input 1
4 - Non-inverting input 1
5 - NC
6 - V_{CC}^+
7 - NC
8 - Non-inverting input 2
9 - Inverting input 2
10 - Output 2
11 - NC
12 - Output 3
13 - Inverting input 3
14 - Non-inverting input 3
15 - NC
16 - V_{CC}^-
17 - NC
18 - Non-inverting input 4
19 - Inverting input 4
20 - Output 4

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM124,A	LM224,A 2902	LM324,A	Unit
V_{cc}	Supply Voltage	± 16 or 32			V
V_i	Input Voltage	– 0.3 to + 32			V
V_{id}	Differential Input Voltage	+ 32	+ 32	+ 32	V
P_{tot}	Power Dissipation N, J Suffix GC Suffix D Suffix	500 665	500 400	500 400	mW
	Output Short-circuit Duration	Indefinite			
I_{id}	Input Current – (note 6)	50	50	50	mA
T_{oper}	Operating Free Air Temperature Range	– 55 to + 125	– 40 to + 105	0 to + 70	°C
T_{stg}	Storage Temperature Range	– 65 to 150	– 65 to 150	– 65 to 150	°C

SCHEMATIC DIAGRAM (1/4 LM124)



Case	Inverting Inputs	Non-inverting Inputs	V_{CC}^-	V_{CC}^+	Outputs	N.C.
DIP14 CERDIP14 SO14	2, 6, 9, 13	3, 5, 10, 12	11	4	1, 7, 8, 14	
LCC20	3, 9, 13, 19	4, 8, 14, 18	16	6	1, 2, 12, 20	*

* **LCC20 :** Other pins are not connected.

ELECTRICAL CHARACTERISTICS

V_{CC}^{+} = + 5 V, V_{CC}^{-} = Ground, V_O = 1.4 V
LM324, A : $0 \leq T_{amb} \leq +70$ °C
LM224, A LM2902 : $-40 \leq T_{amb} \leq +105$ °C
LM124, A : $-55 \leq T_{amb} \leq +125$ °C
(unless otherwise specified)

Symbol	Parameter		LM124A, 224A 324A			LM124, 224 324, 2902			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage (note 3)								mV
	T_{amb} = + 25 °C			2	3		2	5	
	$T_{min} \leq T_{amb} \leq T_{max}$				5			7	
I_{IO}	Input Offset Current								nA
	T_{amb} = + 25 °C			2	20		2	20	
	$T_{min} \leq T_{amb} \leq T_{max}$				40			40	
I_{IB}	Input Bias Current (note 2)								nA
	T_{amb} = + 25 °C			20	100		20	100	
	$T_{min} \leq T_{amb} \leq T_{max}$				200			200	
A_{VD}	Large Signal Voltage Gain								V/mV
	(V_{CC}^{+} = + 15 V, R_L = 2 kΩ)								
	(V_O = 1.4 V to 11.4 V)								
	T_{amb} = + 25 °C		50	100		50	100		
	$T_{min} \leq T_{amb} \leq T_{max}$		25			25			
S_{VR}	Supply Voltage Rejection Ratio ($R_S \leq 10$ kΩ)								dB
	T_{amb} = + 25 °C		65	110		65	110		
	$T_{min} \leq T_{amb} \leq T_{max}$		65			65			
I_{CC}	Supply Current, all Amp, no Load								mA
	T_{amb} = + 25 °C	V_{CC} = + 5 V		0.7	1.2		0.7	1.2	
		V_{CC} = + 30 V		1.5	3		1.5	3	
	$T_{min} \leq T_{amb} \leq T_{max}$	V_{CC} = + 5 V		0.8	1.2		0.8	1.2	
		V_{CC} = + 30 V		1.5	3		1.5	3	
V_I	Input Voltage Range (note 4)								V
	T_{amb} = + 25 °C	V_{CC} = + 30 V	0		V_{CC} − 1.5	0		V_{CC} − 1.5	
	$T_{min} \leq T_{amb} \leq T_{max}$		0		V_{CC} − 2	0		V_{CC} − 2	
CMR	Common-mode Rejection Ratio ($R_S \leq 10$ kΩ)								dB
	T_{amb} = + 25 °C		70	80		70	80		
	$T_{min} \leq T_{amb} \leq T_{max}$		60			60			
I_O	Output Short-circuit Current								mA
	(V_I^{+} = + 1 V, V_I^{-} = 0 V, V_{CC} = + 15 V)								
	T_{amb} = + 25 °C		20	40	60	20	40	60	
	$T_{min} \leq T_{amb} \leq T_{max}$		10			10			
I_{sink}	Output Current Sink								
	(V_I^{+} = − 1 V, V_I^{-} = 0 V)								
	V_{CC} = + 15 V	T_{amb} = + 25 °C	10	20		10	20		mA
		$T_{min} \leq T_{amb} \leq T_{max}$	10			10			
	V_O = + 0.2 V	T_{amb} = + 25 °C	12	50		12	50		µA
		$T_{min} \leq T_{amb} \leq T_{max}$	12			12			
V_{OPP}	Output Voltage Swing								V
	T_{amb} = + 25 °C	$R_L \geq 2$ kΩ	0		V_{CC} − 1.5	0		V_{CC} − 1.5	
	$T_{min} \leq T_{amb} \leq T_{max}$	$R_L \geq 2$ kΩ	0		V_{CC} − 2	0		V_{CC} − 2	

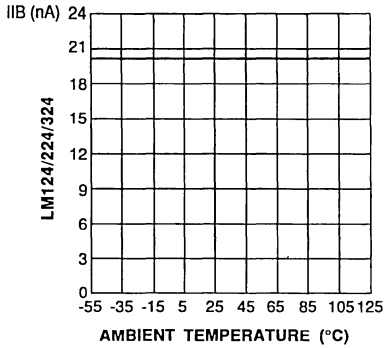
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	LM124A, 224A 324A			LM124, 224 324, 2902			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	High Level Output Voltage (V_{CC} = + 30 V)							V
	T_{amb} = + 25 °C R_L = 2 kΩ	26	27		26	27		
	$T_{min} \leq T_{amb} \leq T_{max}$	26			26			
	T_{amb} = + 25 °C R_L = 10 kΩ	27	28		27	28		
	$T_{min} \leq T_{amb} \leq T_{max}$	27			27			
V_{OL}	Low Level Output Voltage ($R_L \leq$ 10 kΩ)							V
	T_{amb} = + 25 °C	5	20			5	20	
	$T_{min} \leq T_{amb} \leq T_{max}$		20				20	
S_{VO}	Slew-rate (V_I = 0.5 to 3 V, R_L = 2 kΩ CL < 100 pF, T_{amb} = + 25 °C, unity gain V_{CC} = 15 V)	0.2	0.4		0.2	0.4		V/µs
GBP	Gain Bandwidth Product, V_{CC} = 30 V (f = 100 kHz, T_{amb} = + 25 °C, V_{IN} = 10 mV R_L = 2 kΩ, CL = 100 pF)	0.7	1.3	1.8	0.7	1.3	1.8	MHz
THD	Total Harmonic Distortion (f = 1 kHz, A_V = 20 dB, R_L = 2 kΩ, V_O = 2 V_{pp} CL < 100 pF, T_{amb} = + 25 °C, V_{CC} = 30 V)		0.015			0.015		%
V_n	Equivalent Input Noise Voltage (f = 1 kHz, R_g = 100 Ω, V_{CC} = 30 V)		40			40		nV/√Hz
DV_{io}	Average Temperature Coefficient of Input Offset Voltage $T_{min} \leq T_{amb} \leq T_{max}$		7	30		7	30	µV/°C
DI_{IO}	Average Temperature Coeff. of Input Offset Current $T_{min} \leq T_{amb} \leq T_{max}$		10	300		10	300	pA/°C
V_O1/V_O2	Channel Separation (note 5) 1 kHz ≤ f ≤ 20 kHz		120			120		dB

Notes : 1. Short-circuits from the output to V_{CC} can cause excessive heating if V_{CC} > 15 V. The maximum output current is approximatively 40 mA independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.

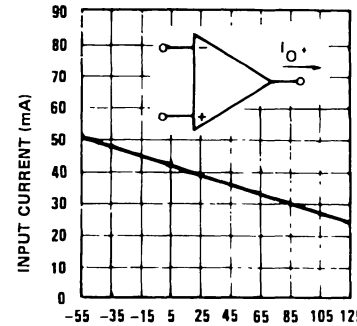
2. The direction of the input current is out of the IC. This current is essentialy constant, independent of the state of the output so no loading change exists on the input lines.
3. V_o = 1.4 V, R_S = 0, 5 V < V_{CC} < 30 V, 0 < V_i < V_{CC} – 1.5 V.
4. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC} – 1.5 V, but either or both inputs can go to + 32 V without damage.
5. Due to the proximity of external components insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequences.
6. This input only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the Op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time duration than an input is driven negative.
   This is not destructive and normal output will set up again for input voltage higher than – 0.3 V.

INPUT BIAS CURRENT
vs AMBIENT TEMPERATURE



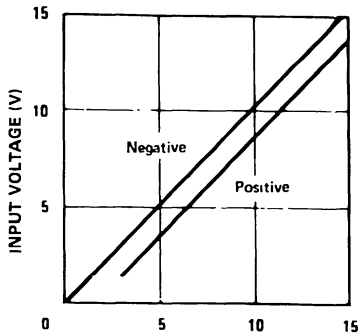
E88LM124-02

CURRENT LIMITING (Note 8)



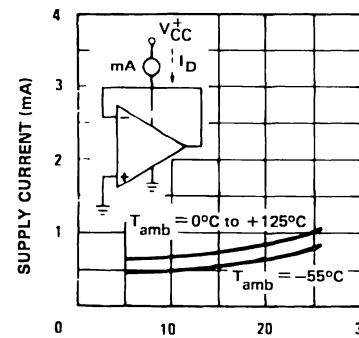
E88LM124-03

INPUT VOLTAGE RANGE



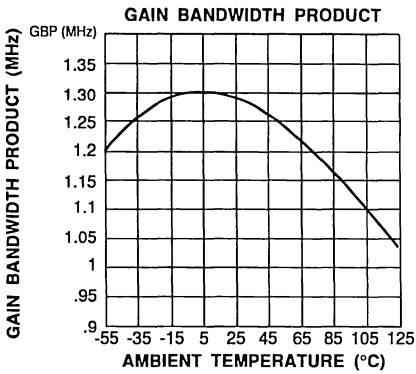
E88LM124-04

SUPPLY CURRENT



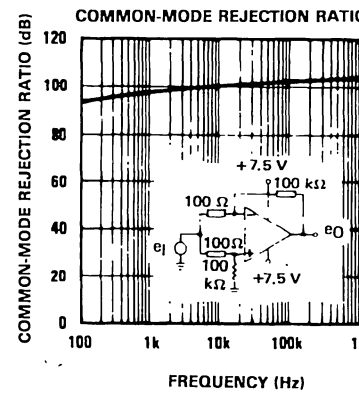
E88LM124-05

GAIN BANDWIDTH PRODUCT



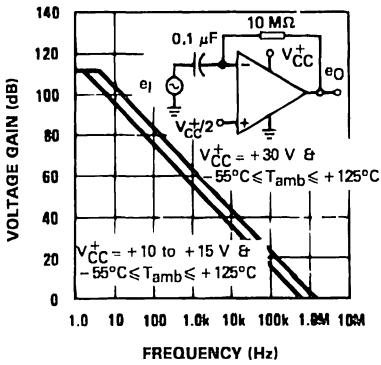
E88LM124-06

COMMON-MODE REJECTION RATIO



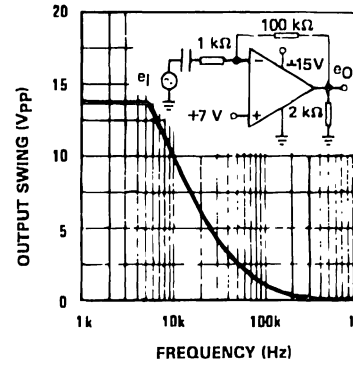
E88LM124-07

OPEN LOOP FREQUENCY RESPONSE



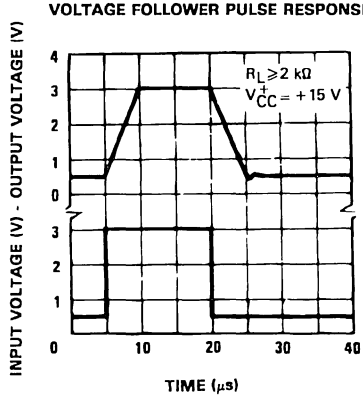
E88LM124-08

LARGE SIGNAL FREQUENCY RESPONSE



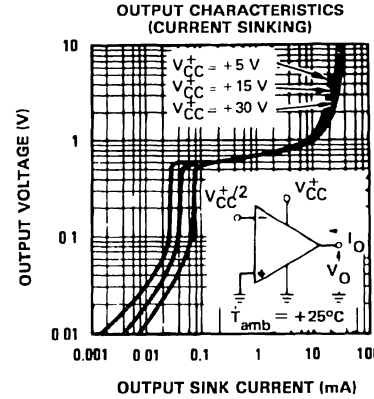
E88LM124-09

VOLTAGE FOLLOWER PULSE RESPONSE



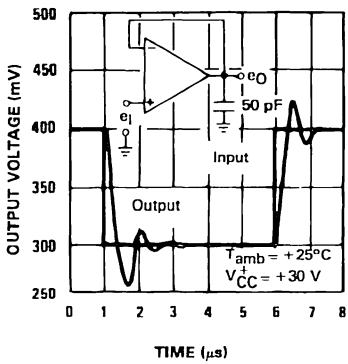
E88LM124-10

OUTPUT CHARACTERISTICS (CURRENT SINKING)



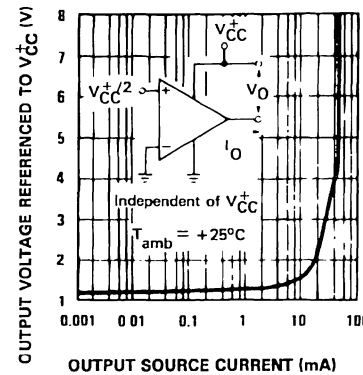
E88LM124-11

VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)



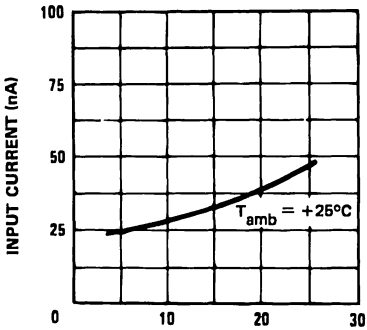
E88LM124-12

OUTPUT CHARACTERISTICS (CURRENT SOURCING)



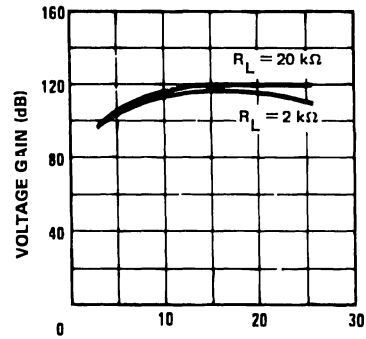
E88LM124-13

INPUT CURRENT



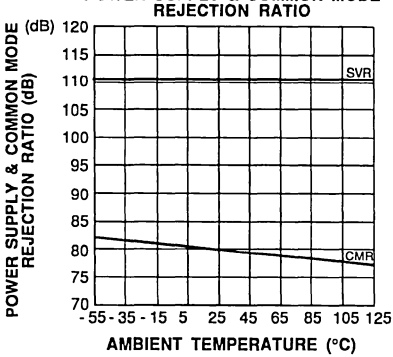
E88LM124-14

VOLTAGE GAIN



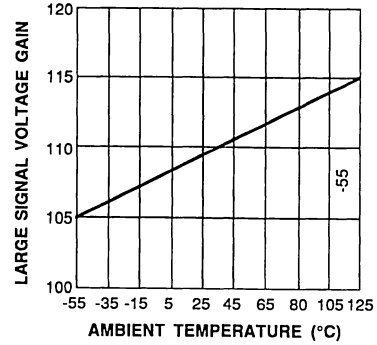
E88LM124-15

POWER SUPPLY & COMMON MODE REJECTION RATIO



E88LM124-16

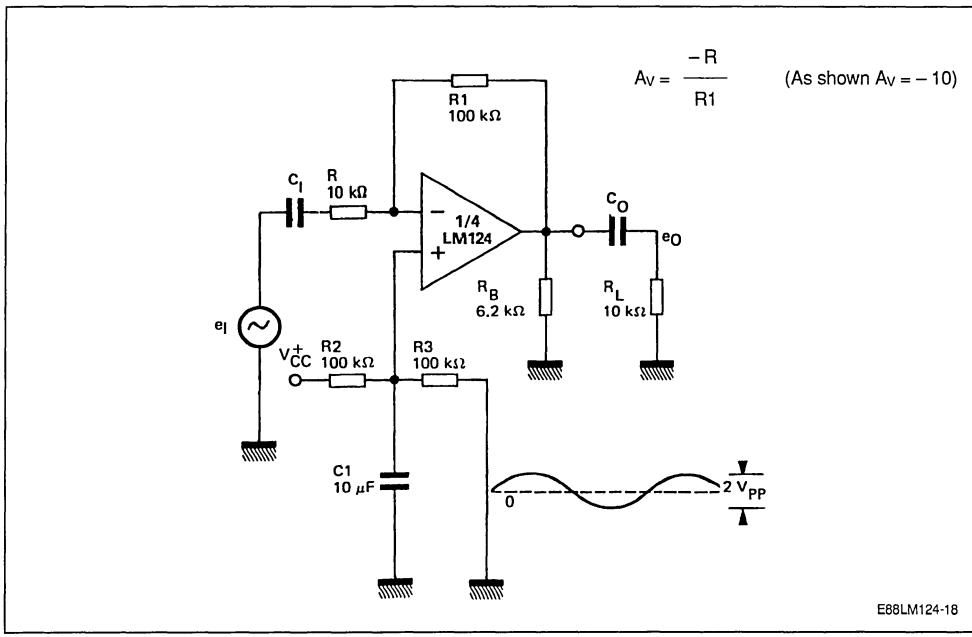
LARGE SIGNAL VOLTAGE GAIN



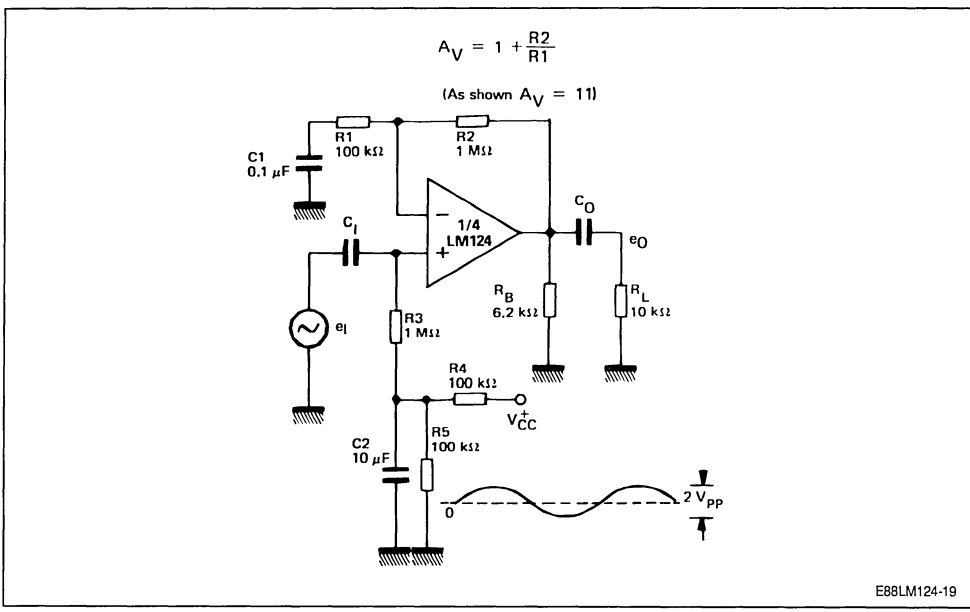
E88LM124-17

TYPICAL SINGLE - SUPPLY APPLICATIONS

AC COUPLED INVERTING AMPLIFIER

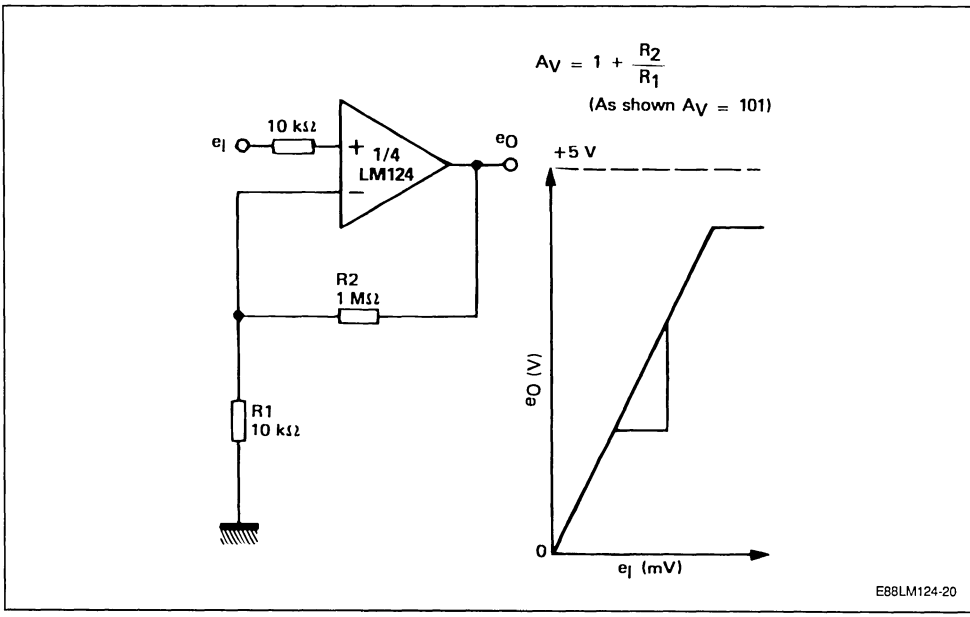


AC COUPLED NON-INVERTING AMPLIFIER

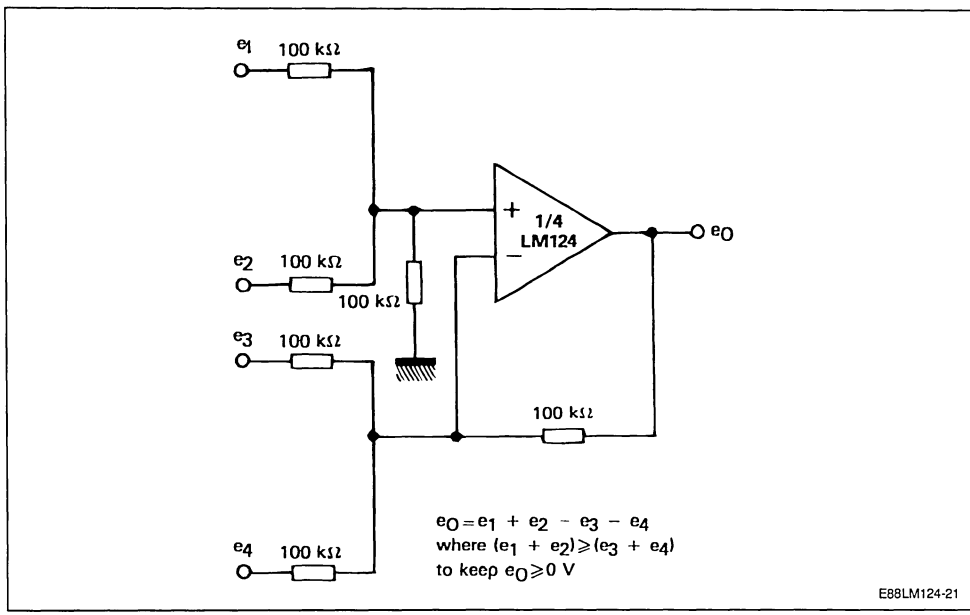


TYPICAL SINGLE - SUPPLY APPLICATIONS (continued)

NON-INVERTING DC GAIN



DC SUMMING AMPLIFIER



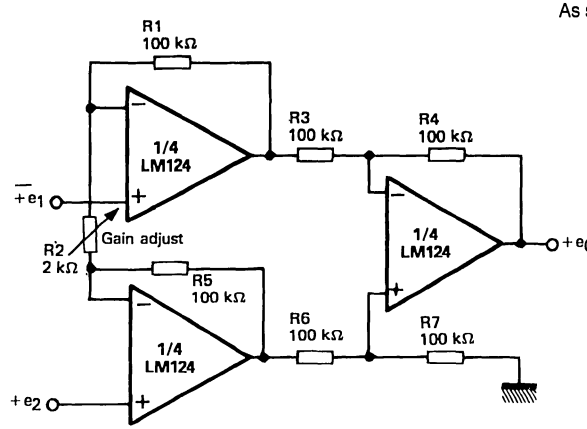
TYPICAL SINGLE SUPPLY APPLICATIONS (continued)

HIGH INPUT Z ADJUSTABLE GAIN DC INSTRUMENTATION AMPLIFIER

If $R_1 = R_5$ and $R_3 = R_4 = R_6 = R_7$

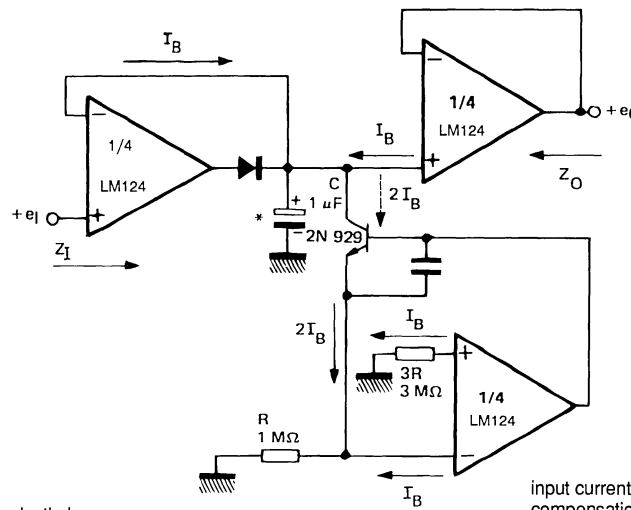
$$e_O = \left(1 + \frac{2R_1}{R_2}\right)(e_2 - e_1)$$

As shown $e_O = 101\,(e_2 - e_1)$



E88LM124-22

LOW DRIFT PEAK DETECTOR



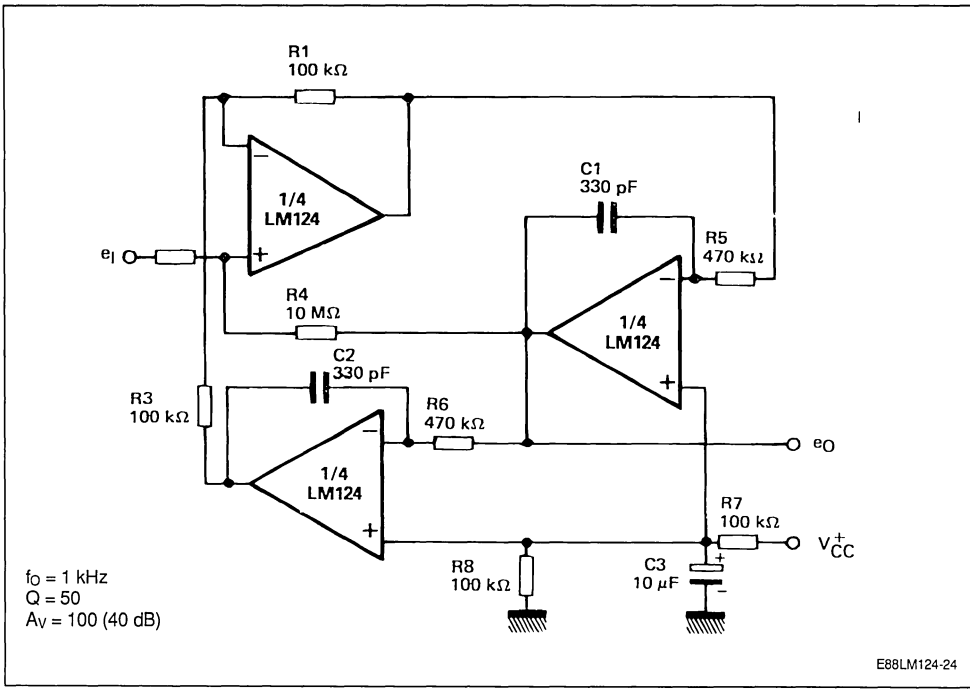
input current compensation

* Polycarbonate or polyethylene

E88LM124-23

TYPICAL SINGLE SUPPLY APPLICATIONS (continued)

ACTIVE BANDPASS FILTER



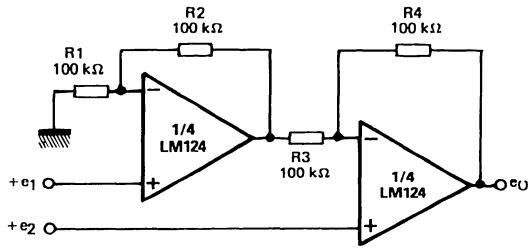
TYPICAL SINGLE SUPPLY APPLICATIONS (continued)

HIGH INPUT Z, DC DIFFERENTIAL AMPLIFIER

For $\frac{R_1}{R_2} = \frac{R_4}{R_3}$ (CMRR depends on this resistor ratio match)

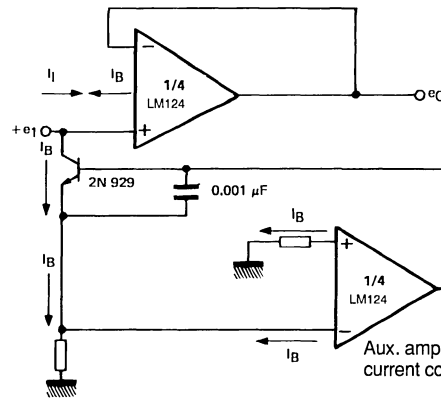
$e_O = \left(1 + \frac{R_4}{R_3}\right)(e_2 - e_1)$

As shown $e_O = 2(e_2 - e_1)$



E88LM124-25

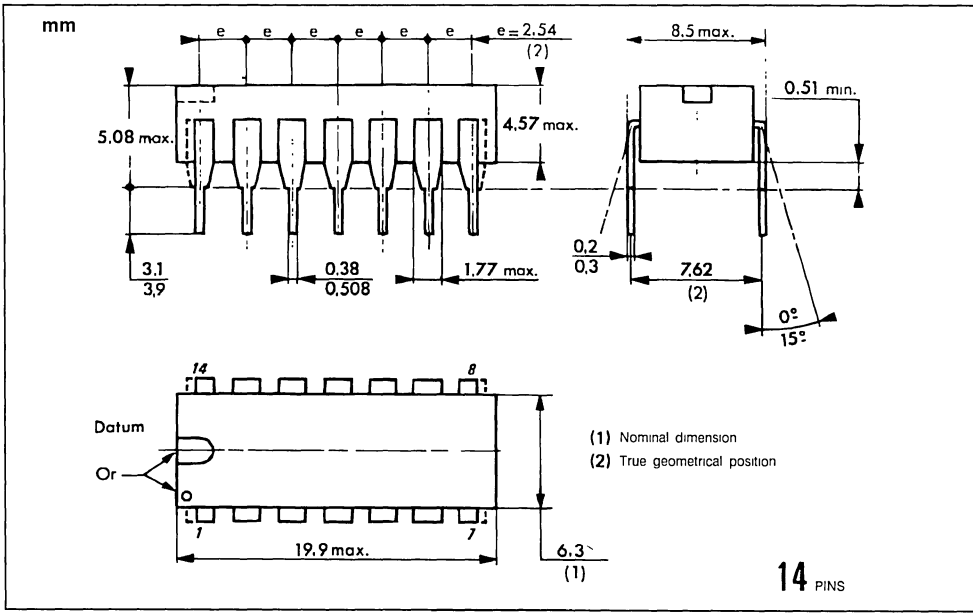
USING SYMMETRICAL AMPLIFIERS TO REDUCE INPUT CURRENT (GENERAL CONCEPT)



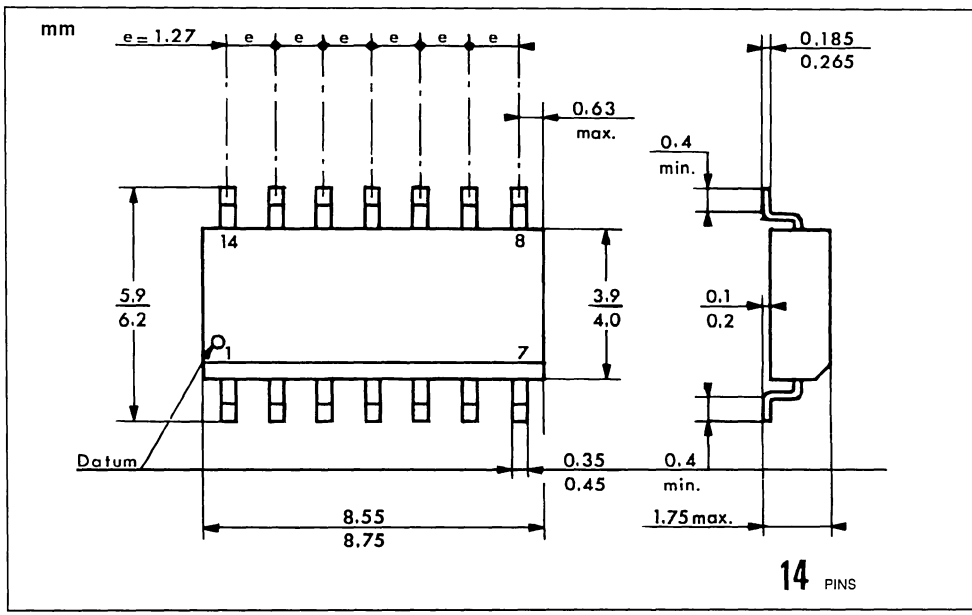
E88LM124-26

PACKAGE MECHANICAL DATA

14 PINS – N SUFFIX – PLASTIC PACKAGE – J SUFFIX – CERDIP PACKAGE

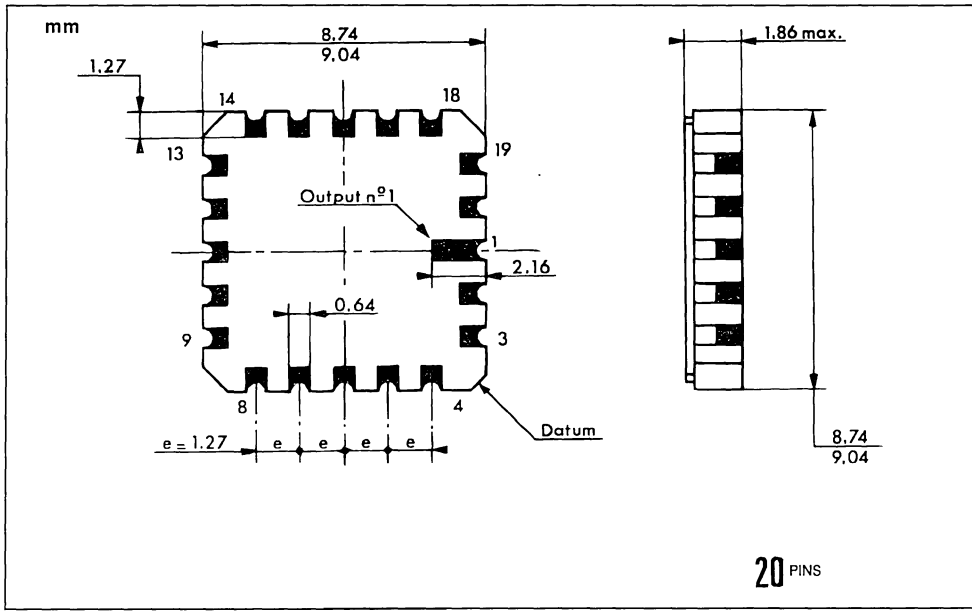


14 PINS – D SUFFIX – PLASTIC MICROPACKAGE.



PACKAGE MECHANICAL DATA (continued)

20 PINS – GC SUFFIX – TRICECOP (LCC)



SGS-THOMSON MICROELECTRONICS

LM134
LM234-LM334

THREE TERMINAL ADJUSTABLE CURRENT SOURCES

- OPERATES from 1 V to 40 V
- 0.02 % V CURRENT REGULATION
- PROGRAMMABLE from 1 μA to 10 mA
- ± 3 % INITIAL ACCURATY

DESCRIPTION

The LM134/LM234/LM334 are 3-terminal adjustable current sources characterized by :

- an operating current range of 10000 : 1
- an excellent current regulation
- a wide dynamic voltage range of 1 V to 40 V

The current is determined by an external resistor without requiring other external components.

Reverse voltages of up to 20 V will only draw a current of several microamperes. This enables the circuit to operate as a rectifier and as a source of current in a.c. applications.

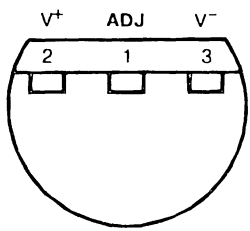
For the LM134/LM234/LM334, the voltage on the control pin is 64 mV at + 25 °C and is directly proportional to the absolute temperature (°K). The simplest external resistor connection generates a current with ≈ 0.33 %/°C temperature dependence. Zero drift can be obtained by adding an additional resistor and a diode to the external circuit.

Z
TO92
(Plastic Package)

(order code at the end of the Datasheet)

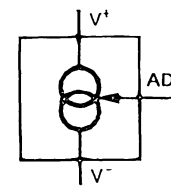
PIN CONNECTION

(bottom view)



E88LM134-01

BLOCK DIAGRAM



E88LM134-02

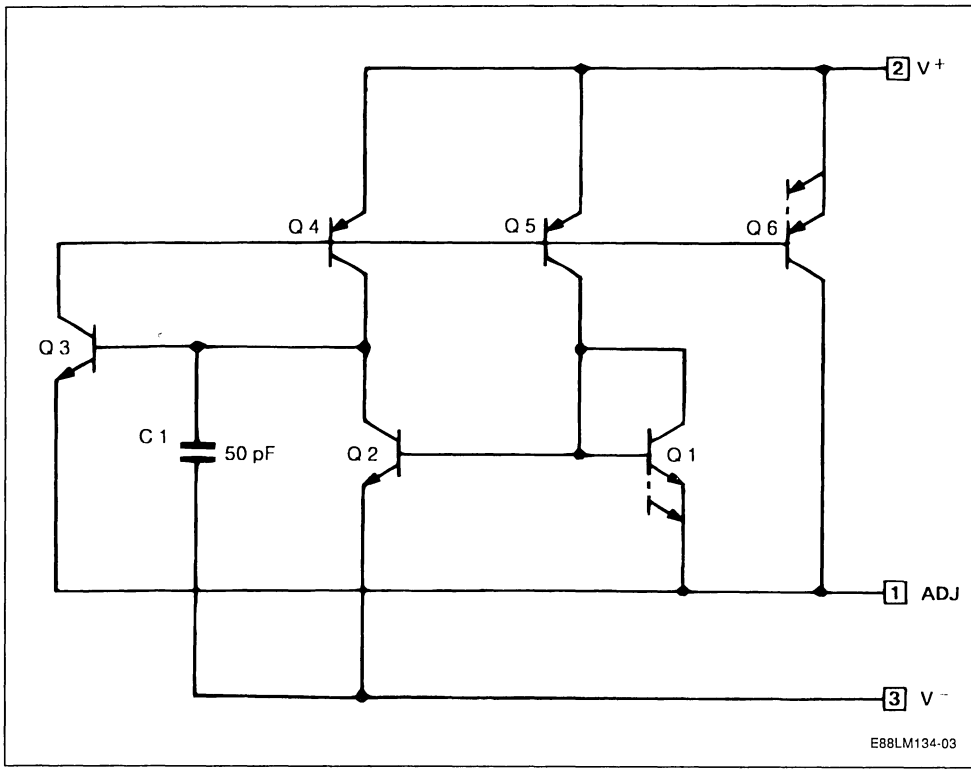
ABSOLUTE MAXIMUM RATING

Symbol	Parameter	LM134, LM234	LM334	Unit
	Voltage V^+ to V^-			V
	Forward	40	30	
	Reverse	20	20	
V^-_{ADJ}	ADJ Pin to V^- Voltage	5	5	V
I_{SET}	Set Current	10	10	mA
P_{tot}	Power Dissipation	400	400	mW
T_{stg}	Storage Temperature Range	– 65 to + 150		°C
T_{oper}	Operating Free-air Temperature Range			°C
	LM134	– 55 to + 125		
	LM234	– 25 to + 100		
	LM334	0 to + 70		

THERMAL DATA

$R_{th(j-c)}$	Maximum Junction-case Thermal Resistance	60	°C/W
$R_{th(j-a)}$	Maximum Junction-ambient Thermal Resistance	200	°C/W

SCHEMATIC DIAGAM



ELECTRICAL CHARACTERISTICS

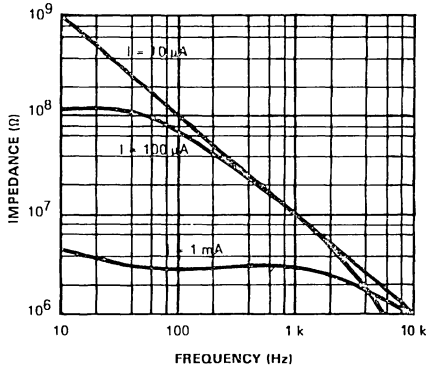
T_j = + 25 °C with pulse testing so that junction temperature does not change during testing.
(unless otherwise specified)

Parameter	LM134 - LM234			LM334			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Set Current Error (V^+ = + 25 V) - Note 1							%
10 µA ≤ I_{SET} ≤ 1 mA			3			6	
1 mA ≤ I_{SET} ≤ 5 mA			5			8	
2 µA ≤ I_{SET} ≤ 10 µA			8			12	
Ratio of Set Current to V^- Current							
10 µA ≤ I_{SET} ≤ 1 mA	14	18	23	14	18	26	
1 mA ≤ I_{SET} ≤ 5 mA		14			14		
2 µA ≤ I_{SET} ≤ 10 µA		14			14		
Minimum Operating Voltage							V
2 µA ≤ I_{SET} ≤ 100 µA		0.8			0.8		
100 µA ≤ I_{SET} ≤ 1 mA		0.9			0.9		
1 mA ≤ I_{SET} ≤ 5 mA		1			1		
Average change in set current with input voltage							% / V
2 µA ≤ I_{SET} ≤ 1 mA							
+ 1.5 V ≤ V^+ ≤ + 5 V		0.02	0.05		0.02	0.1	
+ 5 V ≤ V^+ ≤ + 40 V		0.01	0.03		0.01	0.05	
1 mA ≤ I_{SET} ≤ 5 mA							
+ 1.5 V ≤ V^+ ≤ + 5 V		0.03			0.03		
+ 5 V ≤ V^+ ≤ + 40 V		0.02			0.02		
Temperature Dependence of set current - (note 2)							
(25 µA ≤ I_{SET} ≤ 1 mA)	0.96 T	T	1.04 T	0.96 T	T	1.04 T	
Effective Shunt Capacitance		15			15		pF

Notes : 1 Set current is the current flowing into theV^+ pin. It is determined by the following formula I_{set} = 67.7 mV/R_{set} (T_j = + 25 °C).
Set current error is expressed as a percent deviation from this amount.

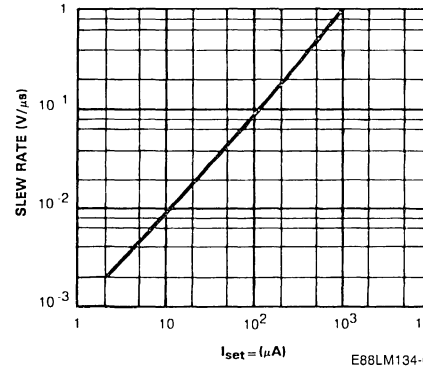
2. I_{set} is directly proportional to absolute temperature (°K) I_{set} at any temperature can be calculated from I_{set} = I_O (T/T_O) where I_O is Iset measured at T_O (°K).

OUTPUT IMPEDANCE



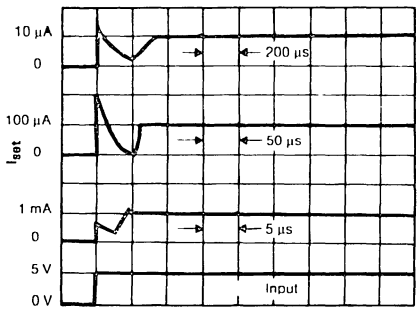
E88LM134-04

MAXIMUM SLEW RATE FOR LINEAR OPERATION



E88LM134-05

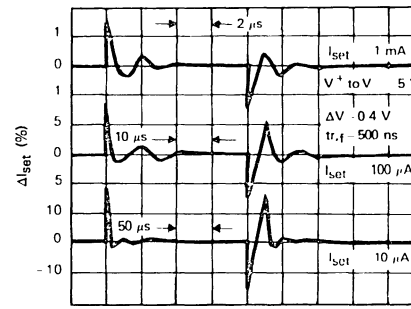
START UP



TIME (SCALE CHANGES AT EACH CURRENT LEVEL).

E88LM134-06

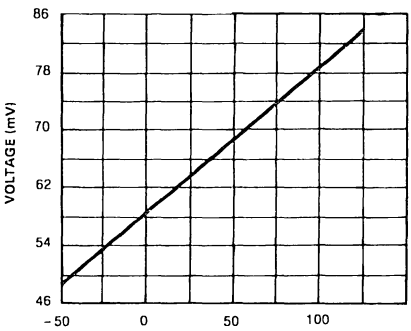
TRANSIENT RESPONSE



TIME (SCALE CHANGES AT EACH CURRENT LEVEL)

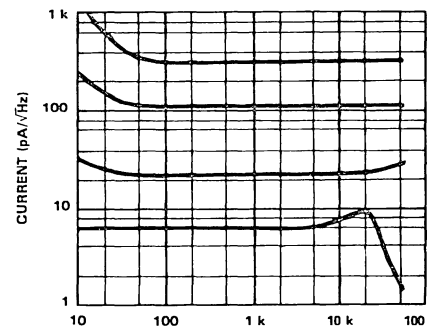
E88LM134-07

VOLTAGE ACROSS R_{set}



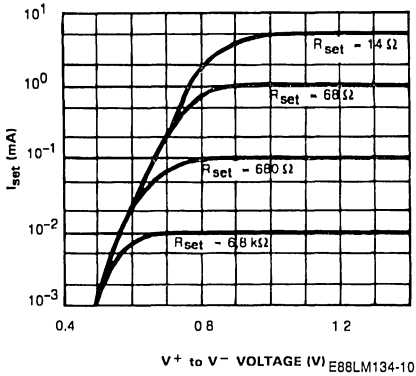
E88LM134-08

CURRENT NOISE



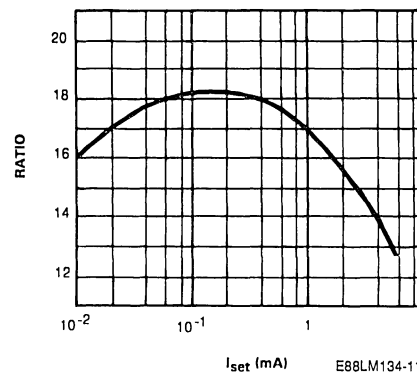
E88LM134-09

TURN-ON VOLTAGE



E88LM134-10

RATIO OF I_{set} to V⁻ CURRENT



E88LM134-11

APPLICATION HINTS

SLEW RATE

At slew rates above a threshold (see curve) the LM134, LM234, LM334 can have a non-linear current characteristic. The slew rate at which this takes place is directly proportional to I_{set}. At I_{set} = 10 µA, dv/dt max. = 0.01 V/µS ; at I_{set} = 1 mA, dv/dt max. = 1 V/µS. Slew rates of more than 1 V/µS do not damage the circuit nor do they produce high currents.

THERMAL EFFECTS

Internal heating can have a significant effect on current regulation for an I_{set} above 100 µA. For example, each increase of 1 V in the voltage across the LM134 at I_{set} = 1 mA will increase the junction temperature by ≈ 0.4 °C (in still air). The output current (I_{set}) has a temperature coefficient of about 0.33 %/°C. Thus the change in current due to the increase in temperature will be (0.4) (0.33) = 0.132 %. This is a degradation of 10 : 1 in regulation versus the true electrical effects. Thermal effects should be taken into account when d.c. regulation is critical and I_{set} is higher than 100 µA. The dissipation of the connections of CB-97 package can reduce this thermal effect by a coefficient of more than 3.

SHUNT CAPACITANCE

In certain applications, the 15 pF value for the shunt capacitance should be reduced :
- because of loading problems,
- because of limitation of the output impedance of the current source in a.c. applications. This reduction of the capacitance can be easily carried out by adding a FET as indicated in the typical applications. The value of this capacitance can be reduced by at least 3 pF and regulation can be improved by an order of magnitude without any modification of the d.c. characteristics (except for the minimum input voltage).

NOISE

The current noise produced by LM134, LM234, LM334 is about 4 times that of a transistor. If the LM134, LM234, LM334 is utilized as an active load for a transistor amplifier, the noise at the input will increase by about 12 dB. In most cases this is acceptable, and a single amplifier can be built with a voltage gain higher than 2 000.

LEAD RESISTANCE

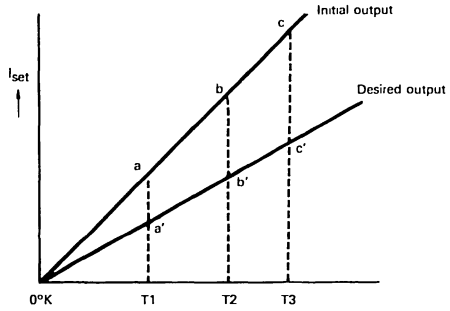
The sense voltage which determines the current of the LM134, LM234, LM334, is less than 100 mV. At this level, the effects of the thermocouple and the connection resistance should be reduced by locating the current setting resistor close to the device. Do not use sockets for the ICs. A contact resistance of 0.7 Ω is sufficient to decrease the output current by 1 % at the 1 mA level.

SENSING TEMPERATURE

The LM134, LM234, LM334 are excellent remote controlled temperature sensors because their operation as sources of current preserves their accuracy even in the case of long connecting wires. The output current is directly proportional to the absolute temperature in degrees Kelvin according to the following equation.

$$I_{set} = \frac{(227\ \mu V/°K)\ (T)}{R_{set}}$$

The calibration of the LM134, LM234, LM334 is simplified by the fact that most of the initial accuracy is due to gain limitation (slope error) and not an offset. Gain adjustment is a one point trim because the output of the device extrapolates to zero at 0 °K.

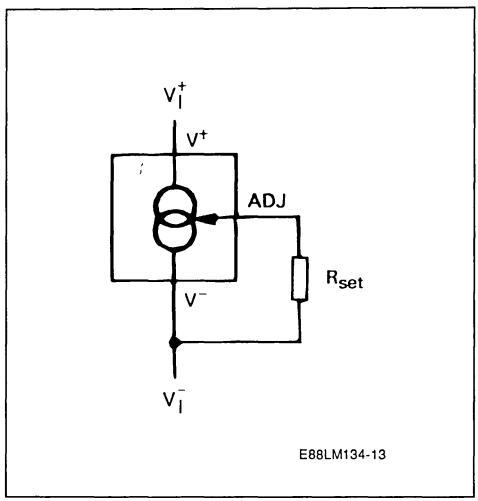


E88LM134-12

This particularity of the LM134, LM234, LM334 is illustrated in the above diagram. Line abc represents the sensor current before adjustment and line a'b'c' represents the desired output. An adjustment of the gain provided at T2 will move the output from b to b' and will correct the slope at the same time so that the output at T1 and T3 will be correct. This gain adjustment can be carried out by means of R_{set} or the load resistor utilized in the circuit. After adjustment, the slope error should be less than 1 %. A low temperature coefficient for R_{set} is necessary to keep this accuracy. A 33 ppm/°C temperature drift of R_{set} will give an error of 1 % on the slope because the resistance follows the same temperature variations as the LM134, LM234, LM334. Three wires are required to isolate R_{set} from the LM134, LM234, LM334. Since this solution is not recommended. Metal-film resistors with a drift less than 20 ppm/°C are now available. Wirewound resistors can be utilized when very high stability is required.

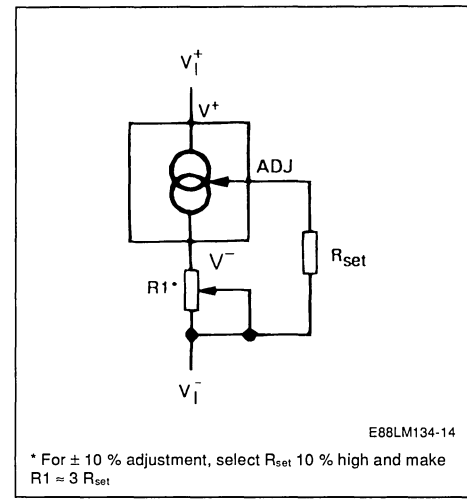
TYPICAL APPLICATIONS

Figure 1 : Basic 2-terminal Current Source.



E88LM134-13

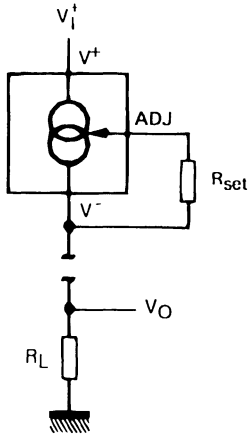
Figure 2 : Alternate Triming Technique.



E88LM134-14

* For ± 10 % adjustment, select R_{set} 10 % high and make R1 ≈ 3 R_{set}

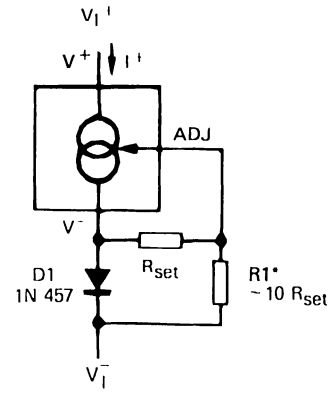
Figure 3 : Terminating Remote Sensor for Voltage Output.



$V_O = (I_{set})(R_L) = 10\ mV/°K$
$R_{set} = 230\ \Omega$
$R_L = 10\ k\Omega$

E88LM134-15

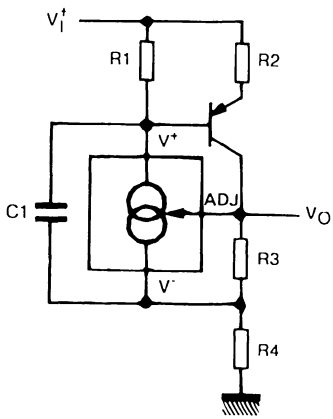
Figure 4 : Zero Temperature Coefficient Current Source.



E88LM134-16

* For ± 10 % adjustment, select R_{set} 10 % high and make $R1 \approx 3\ R_{set}$

Figure 5 : Low Output Impedance Thermometer.



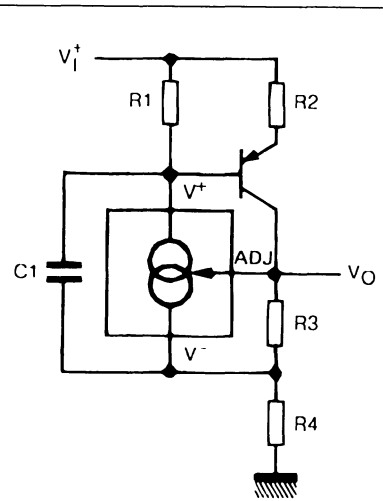
R1 = 230 Ω, 1 %
R2 = 10 kΩ, 1%
R3 = 600 Ω

$V_O = 10\ mV/°C$
$Z_O \leq 100\ \Omega$

E88LM134-17

* Output impedance of the LM134, LM234, LM334 at the "ADJ" pin is approximately $\frac{-R_O\ \Omega}{16}$ where R_O is the equivalent external resistance connected to the V^- pin. This negative resistance can be reduced by a factor of 5 or more by inserting an equivalent resistor in series with the output.

Figure 6 : Low Output Impedance Thermometer.



R1 = 15 kΩ
R2 = 300 Ω
R3 = 100 Ω
R4 = 4.5 kΩ
C1 = 2.2 nF
$V_O = 10\ mV/°C$
$Z_O \leq 2\ \Omega$

E88LM134-18

Figure 7 : Micropower Bias.

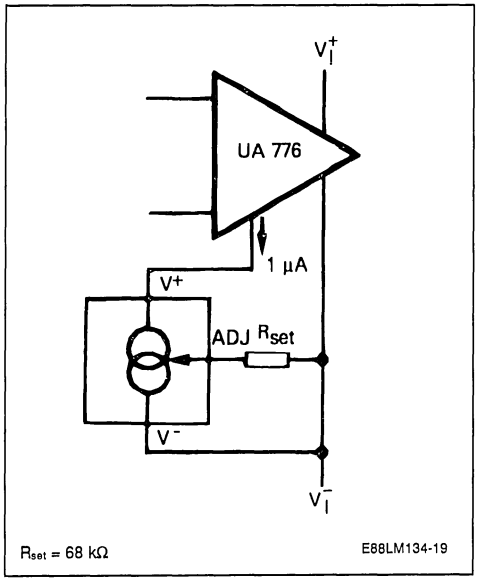


Figure 8 : Low Input Voltage Reference Driver.

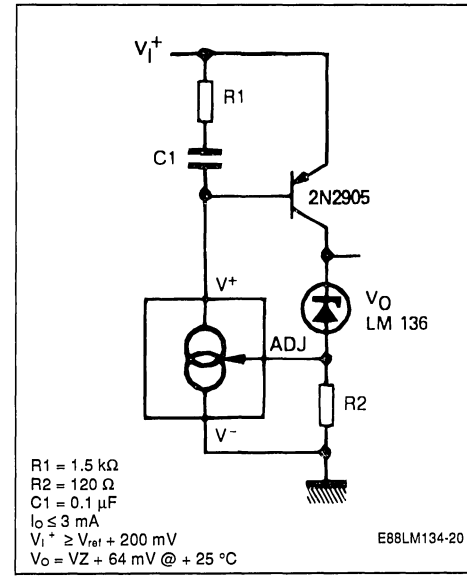
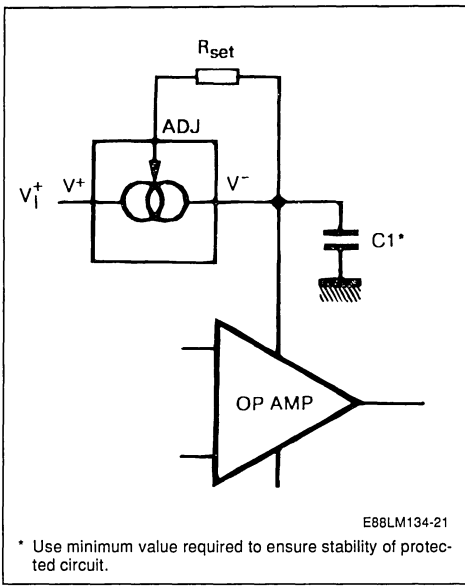
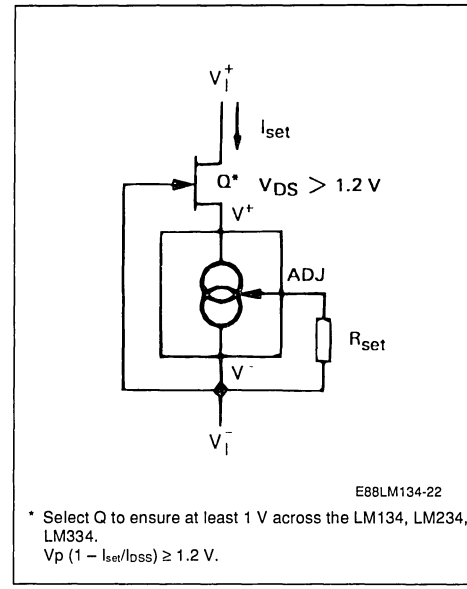


Figure 9 : In-line Current Limiter.



* Use minimum value required to ensure stability of protected circuit.

Figure 10 : Fet cascading for low capacitance.



* Select Q to ensure at least 1 V across the LM134, LM234, LM334.
$V_P (1 - I_{set}/I_{DSS}) \geq 1.2$ V.

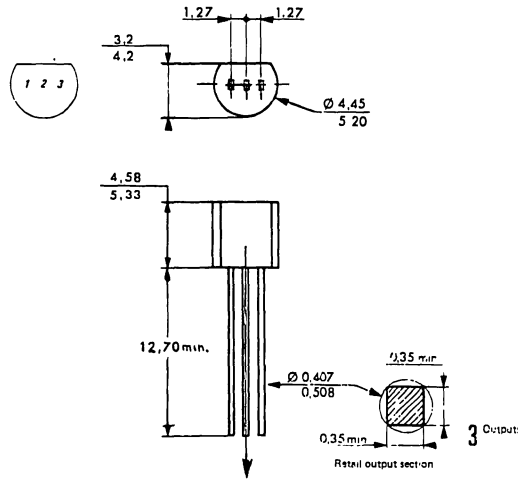
ORDER CODES

Part Number	Temperature Range	Package
		Z
LM134	– 55 °C to + 125 °C	•
LM234	– 25 °C to + 100 °C	•
LM334	0 °C to + 70 °C	•
Example : LM134Z		

PACKAGE MECHANICAL DATA

3 PINS - PLASTIC PACKAGE TO92

mm

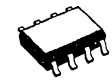


SGS-THOMSON MICROELECTRONICS

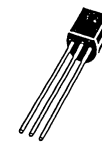
LM135
LM235-LM335,A

PRECISION TEMPERATURE SENSORS

- DIRECTLY CALIBRATED IN °K
- 1 °C INITIAL ACCURACY
- OPERATES FROM 400 µA TO 5 mA
- LESS THAN 1 Ω DYNAMIC IMPEDANCE



D
SO8
(Plastic Micropackage)



Z
TO92
(Plastic Package)

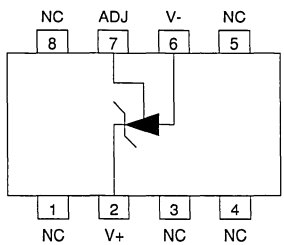
(order codes at the end of the Datasheet)

DESCRIPTION

The LM135, LM235, LM335 are precision temperature sensors which can be easily calibrated. They operate as a 2-terminal Zener and the breakdown voltage is directly proportional to the absolute temperature at 10 mV/°K. The circuit has a dynamic impedance of less than 1 Ω and operates within a range of current from 400 µA to 5 mA without alteration of its characteristics. Calibrated at + 25 °C, the LM135, LM235, LM335 have a typical error of less than 1 °C over a 100 °C temperature range. Unlike other sensors, the LM135, LM235, LM335 have a linear output.

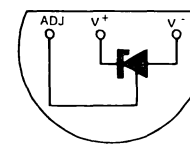
PIN CONNECTION

SO8
Top view



E88LM135-01

TO92
bottom view



E88LM135-02

ABSOLUTE MAXIMUM RATINGS

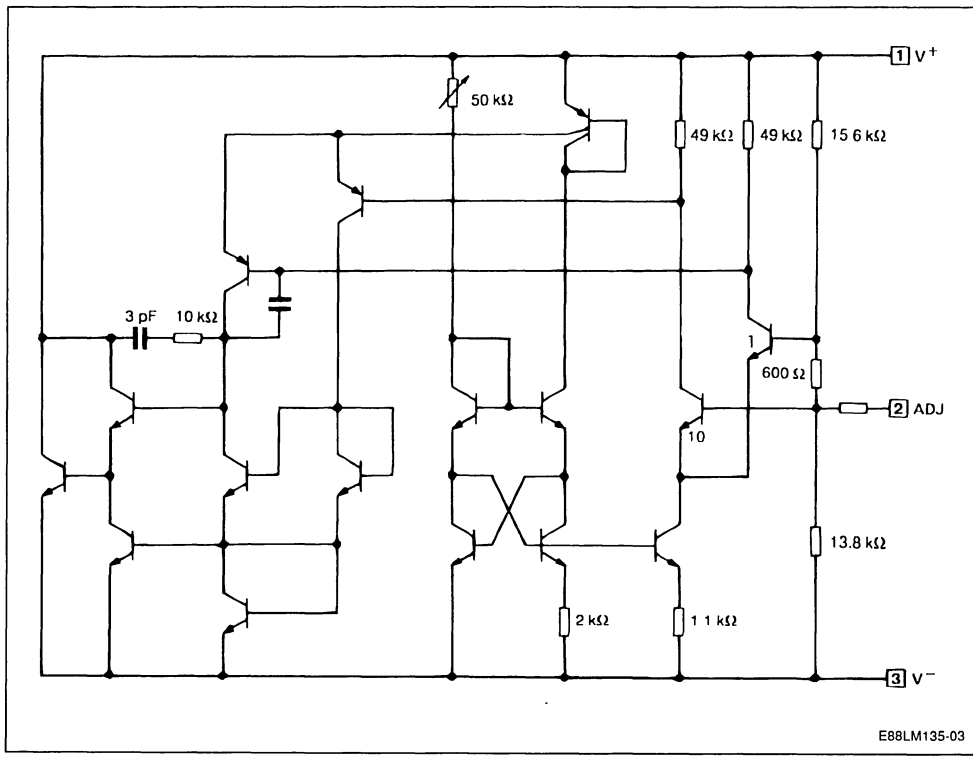
Symbol	Parameter	LM135	LM235	LM335, A	Unit
	Current				mA
I_R	Reverse	15	15	15	
I_F	Foward	10	10	10	
T_{oper}	Operating Free-air Temperature Range (note 1)				°C
	Continuous	− 55 to + 150	− 40 to + 125	− 40 to + 100	
	Intermittent	+ 150 to + 200	+ 125 to + 150	+ 100 to + 125	
T_{stg}	Storage Temperature Range	− 65 to + 150	− 65 to + 150	− 65 to + 150	°C

Note : 1. $T_j \leq 150$ °C.

THERMAL DATA

$R_{th(j-c)}$	Maximum Junction-case Thermal Resistance	60	°C/W
$R_{th(j-a)}$	Maximum Junction-ambient Thermal Resistance	170	°C/W

SCHEMATIC DIAGRAM



TEMPERATURE ACCURACY

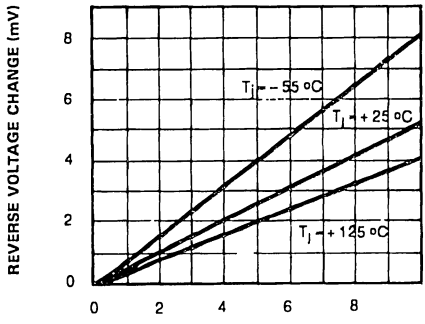
Symbol	Parameter	LM135 - LM235 LM335A			LM335			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
	Operating Output Voltage (T_{case} = + 25 °C, I_R = 1 mA)	2.95	2.98	3.01	2.92	2 98	3.04	V
	Uncalibrated Temperature Error (I_R = 1 mA) T_{case} = + 25 °C $T_{(min)} < T_{case} < T_{(max)}$		 1 2	 3 5		 2 4	 6 9	°C
	Temperature Error with 25 °C Calibration ($T_{(min)} < T_{case} < T_{(max)}$, I_R = 1 mA) LM135 - LM235 LM335 LM335A		 0.5 0.5	 1.5 1		 1	 2	°C
	Calibrated Error at External Temperature $T_{case} = T_{(max)}$ (intermittent)		2			2		°C
	Non-linearity (I_R = 1 mA) LM135 - LM235 LM335 LM335A		 0.3 0.3	 1 1.5		 0.3	 1.5	°C

ELECTRICAL CHARACTERISTICS (note 1)

Symbol	Parameter	LM135 - LM235			LM335, A			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
	Operating output voltage change with current (400 µA < I_R < 5 mA at constant temperature).		2.5	10		3	14	mV
	Dynamic Impedance (I_R = 1 mA)		0.5			0.6		Ω
	Output Voltage Temperature Drift		+ 10			+ 10		mV/°C
	Time Constant Still Air Air 0.5 m/s Stirred Oil		 80 10 1			 80 10 1		s
	Time Stability (T_{case} = + 125 °C)		0.2			0.2		°C/kh

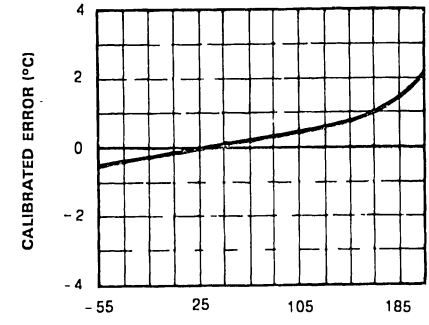
Note : 1. Accuracy measurements are made in a well-stirred oil bath For other conditions, self heating must be considered

REVERSE VOLTAGE CHANGE



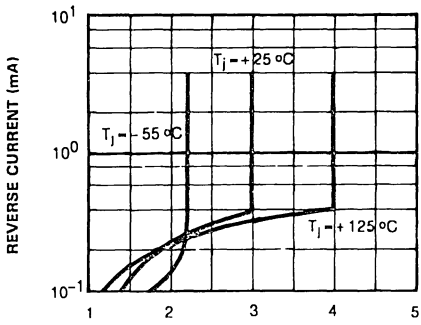
E88LM135-04

CALIBRATED ERROR



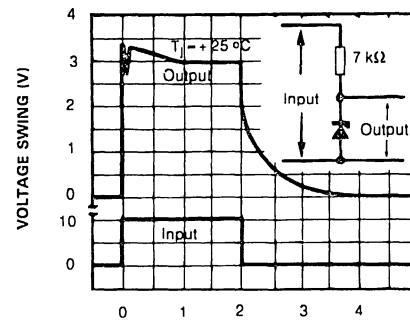
E88LM135-05

REVERSE CHARACTERISTICS



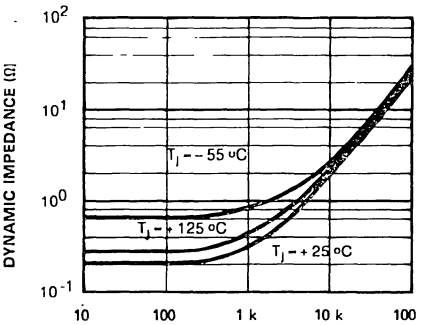
E88LM135-06

RESPONSE TIME



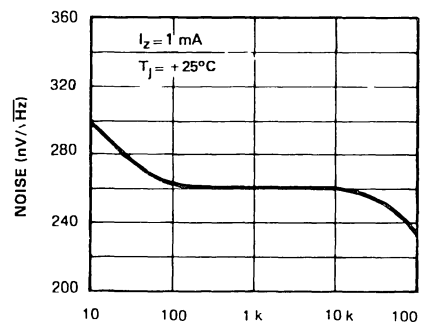
E88LM135-07

DYNAMIC IMPEDANCE



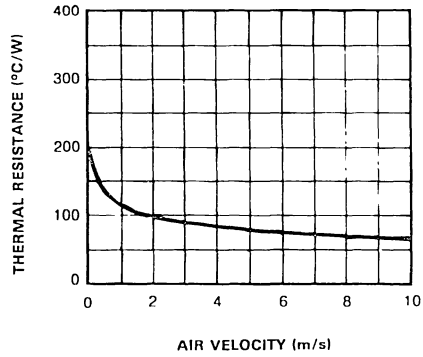
E88LM135-08

NOISE VOLTAGE



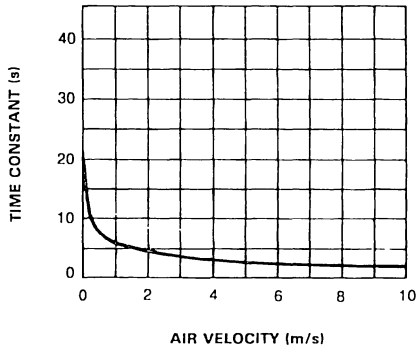
E88LM135-09

THERMAL RESISTANCE JUNCTION TO AIR



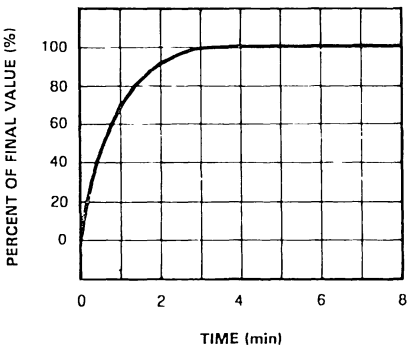
E88LM135-10

THERMAL TIME CONSTANT



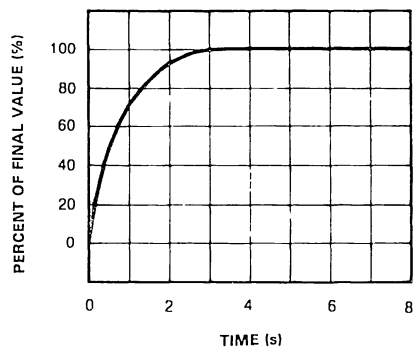
E88LM135-11

THERMAL RESPONSE IN STILL AIR



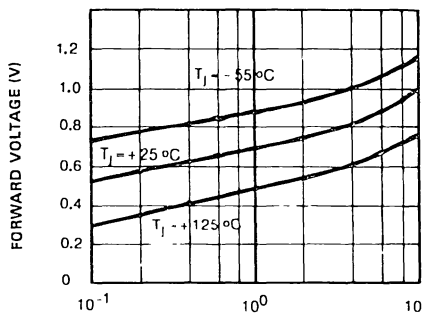
E88LM135-12

THERMAL RESPONSE IN STIRRED OIL BATH



E88LM135-13

FORWARD CHARACTERICS



E88LM135-14

APPLICATION HINTS

There is an easy method of calibrating the device for higher accuracies (see typical applications).

The single point calibration works because the output of the LM135, LM235, LM335 is proportional to the absolute temperature with the extrapolated output of sensor going to 0 V at 0 °K (– 273.15 °C). Errors in output voltage versus temperature are only slope. Thus a calibration of the slope at one temperature corrects errors at all temperatures.

The output of the circuit (calibrated or not) can be given by the equation :

$$V_{OT} = VO_{T_O} \times \frac{T}{T_O}$$

where T is the unknown temperature and T_O is the reference temperature (in °K).

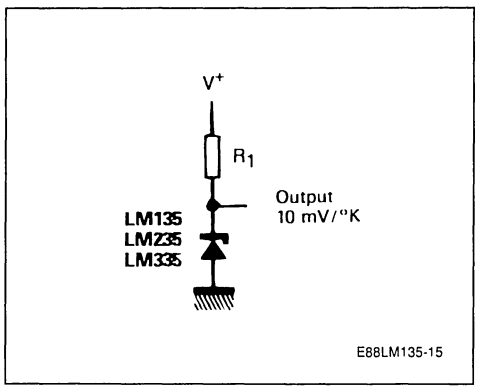
Nominally the output is calibrated at 10 mV/°K.

Precautions should be taken to ensure good sensing accuracy. As in the case of all temperatures sensors, self heating can decrease accuracy. The LM135, LM235, LM335 should operate with a low current, but sufficient to drive the sensor and its calibration circuit to their maximum operating temperature.

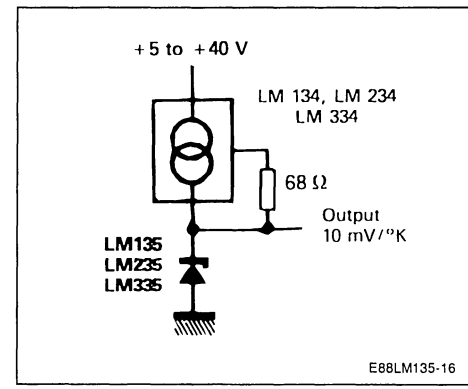
If the sensor is used in surroundings where the thermal resistane is constant, the errors due to self heating can be externally calibrated. This is possible if the circuit is biased with a temperature stable current. Heating will then be proportional to zener voltage and therefore temperature. In this way the error due to self heating is proportional to the absolute temperature as scale factor errors.

TYPICAL APPLICATIONS

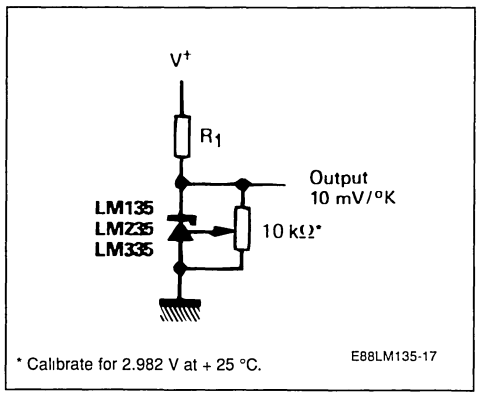
Basic Temperature Sensor.



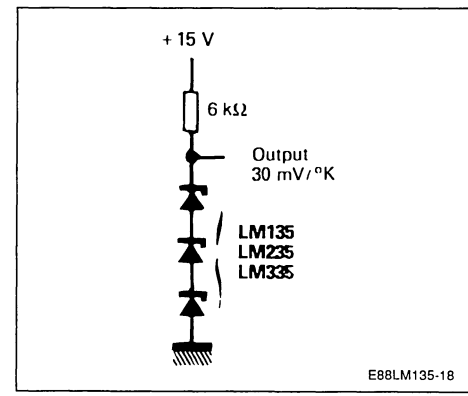
Wide Operating Supply.



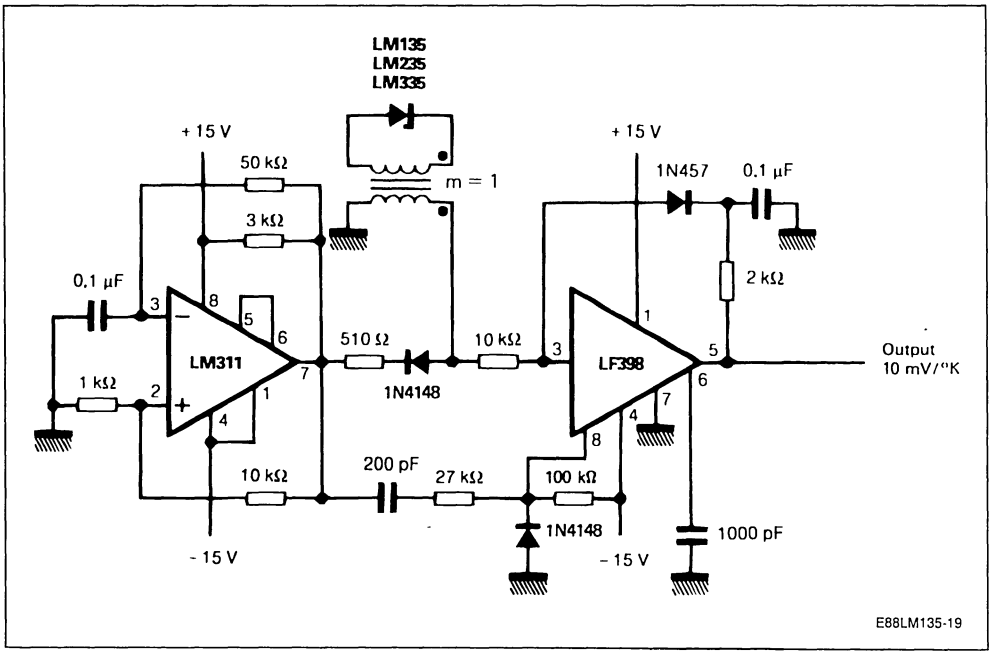
Calibrated Sensor.



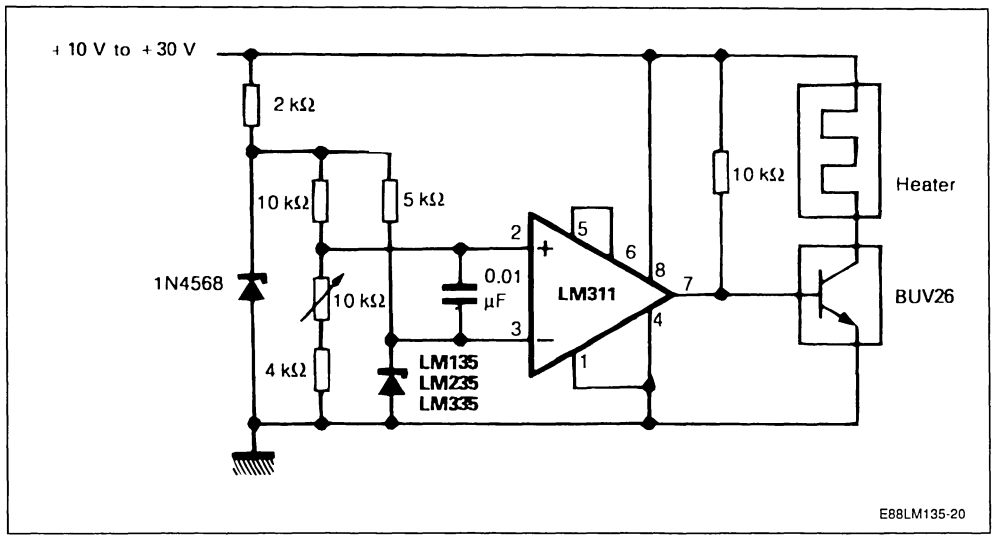
Average Temperature Sensing.



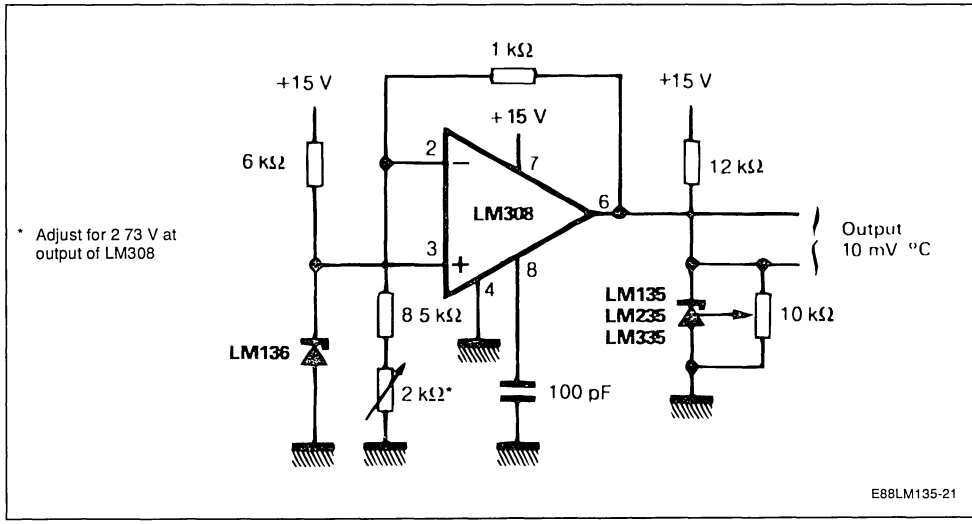
Isolated Temperature Sensor.



Simple Temperature Controller.

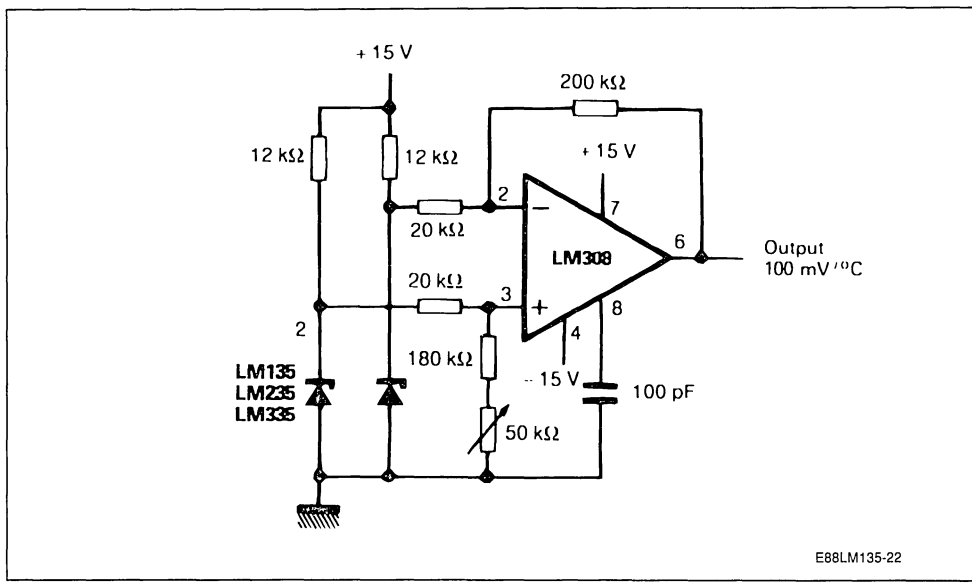


Centigrade Thermometer.



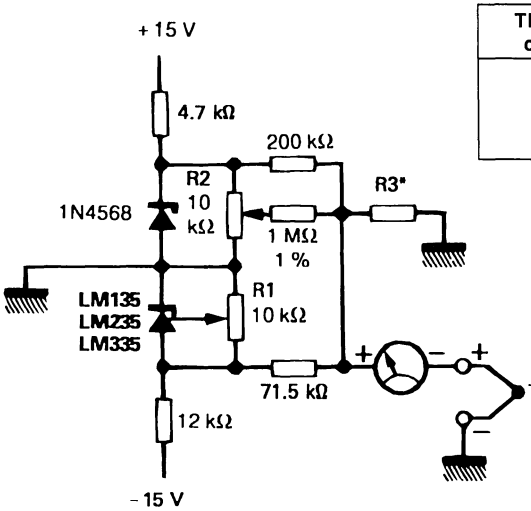
* Adjust for 2 73 V at output of LM308

Differential Temperature Sensor.



THERMOCOUPLE COLD JUNCTION COMPENSATION

Compensation for Grounded Thermocouple.



Thermo-couple	R3	Seebeck Coefficient
J	377 Ω	52.3 µV/°C
T	308 Ω	42.8 µV/°C
K	293 Ω	40.8 µV/°C
S	45.8 Ω	6.4 µV/°C

Adjustments : compensates for both sensor and resistor tolerances.
1. Short 1N4568.
2. Adjust R1 for SEEBECK coefficient ambient temperature (in degrees K) R3.
3. Short LM135 and adjust R2 for voltage across R3 correspon-ding to thermocouple type.
   J 14.32 mV K 11.17 mV
   T 11.79 mV S 1.768 mV

* Select R3 for proper thermocouple type.

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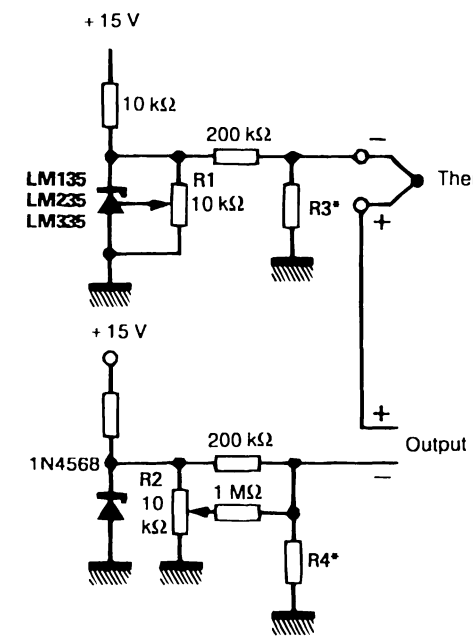
Single Power Supply Cold Junction Compensation.



Thermo-couple	R3	R4	Seebeck Coefficient
J	1.05 kΩ	365 Ω	52.3 µV/°C
T	856 Ω	315 Ω	42.8 µV/°C
K	816 Ω	300 Ω	40.8 µV/°C
S	128 Ω	46.3 Ω	6.4 µV/°C

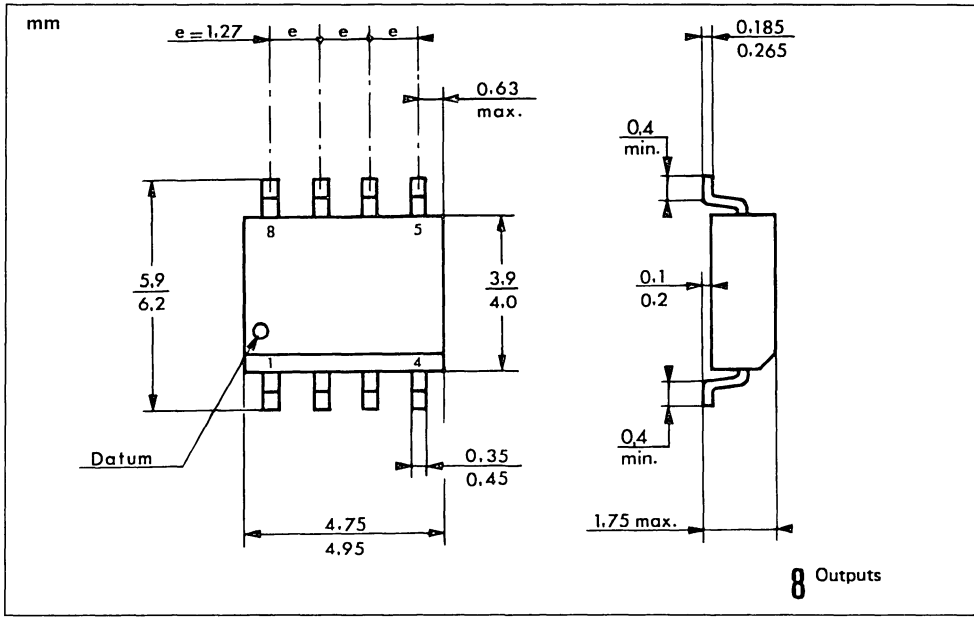
Adjustments :
1. Adjust R1 for the voltage across R3 equal to the SEEBECK coefficient times ambient temperature in degrees Kelvin.
2. Adjust R2 for voltage across R4 correspon-ding to thermocouple.
   J 14.32 mV K 11.17 mV
   T 11.79 mV S 1.768 mV

* Select R3 and R4 for proper thermocouple type.

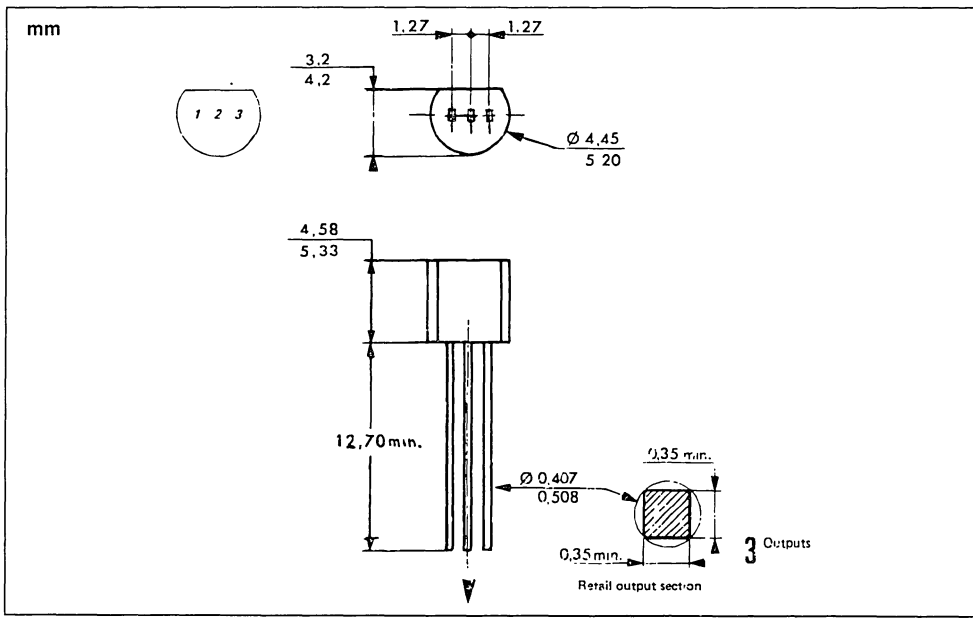
E88LM135-24

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC MICROPACKAGE (SO)



3 PINS - PLASTIC PACKAGE TO92

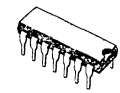


ORDER CODES

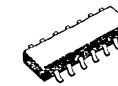
Part number	TemperatureRange		Package
	Continuous	Intermittent	
LM135Z	– 55 °C to + 150 °C	+ 150 °C to + 200 °C	TO92
LM235Z	– 40 °C to + 125 °C	+ 125 °C to + 150 °C	TO92
LM235D	– 40 °C to + 125 °C	+ 125 °C to + 150 °C	SO8
LM335Z	– 40 °C to + 100 °C	+ 100 °C to + 125 °C	TO92
LM335D	– 40 °C to + 100 °C	+ 100 °C to + 125 °C	SO8
LM335AZ	– 40 °C to + 100 °C	+ 100 °C to + 125 °C	TO92
LM335AD	– 40 °C to + 100 °C	+ 100 °C to + 125 °C	SO8

LOW POWER LOW OFFSET VOLTAGE QUAD COMPARATORS

- WIDE SINGLE SUPPLY VOLTAGE RANGE OR DUAL SUPPLIES FOR ALL DEVICES : + 2 V TO + 36 V OR ± 1 V TO ± 18 V
- VERY LOW SUPPLY CURRENT DRAIN (0.8 mA) INDEPENDENT OF SUPPLY VOLTAGE (1 mW/comparator at + 5 V)
- LOW INPUT BIAS CURRENT : 25 nA TYP
- LOW INPUT OFFSET CURRENT : ± 5 nA TYP
- LOW INPUT OFFSET VOLTAGE : ± 1 mV TYP
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND
- LOW OUTPUT SATURATION VOLTAGE : 250 mV TYP. (I_O = 4 mA)
- DIFFERENTIAL INPUT VOLTAGE RANGE TO THE SUPPLY VOLTAGE
- TTL COMPATIBLE OUTPUTS



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

J
CERDIP14
(Cerdip Package)

GC
LCC20
(Tricecop (LCC))

DESCRIPTION

These devices consist of four independent precision voltage comparators with an offset voltage specifications as low as 2 mV max for LM339A, LM239A and LM139A. All these comparators were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible.

These comparators also have a unique characteristic in that the input common-mode voltage range includes ground even through operated from a single power supply voltage.

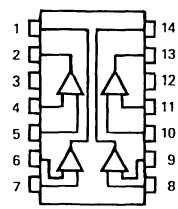
ORDER CODES

Part Number	Temperature Range	Package			
		N	J	GC	D
LM139,A	– 55 to + 125 °C	•	•		•
LM239,A	– 40 to + 105 °C	•	•		•
LM339,A	0 to + 70 °C	•	•	•	•
LM2901	– 40 to + 105 °C	•	•	•	•
MC3302	– 40 to + 105 °C	•	•		•

Note : Hi-Rel Versions Available
Examples : LM139GC, LM139AN, LM2901D

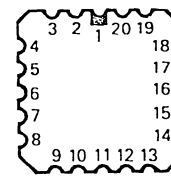
PIN CONNECTIONS (top views)

DIP14 / CERDIP14
SO14



1 - Output 2
2 - Output 1
3 - V_{CC}
4 - Inverting input 1
5 - Non-inverting input 1
6 - Inverting input 2
7 - Non-inverting 2
8 - Inverting input 3
9 - Non-inverting input 3
10 - Inverting input 4
11 - Non-inverting input 4
12 - V_{CC}
13 - Output 4
14 - Output 3

LCC20



E88LM139-01

1 - NC
2 - Output 2
3 - Output 1
4 - V_{CC}
5 - NC
6 - Inverting input 1
7 - NC
8 - Non-inverting input 1
9 - Inverting input 2
10 - Non-inverting input 2
11 - NC
12 - Inverting input 3
13 - Non-inverting input 3
14 - Inverting input 4
15 - NC
16 - Non-inverting input 4
17 - NC
18 - V_{CC}
19 - Output 4
20 - Output 3

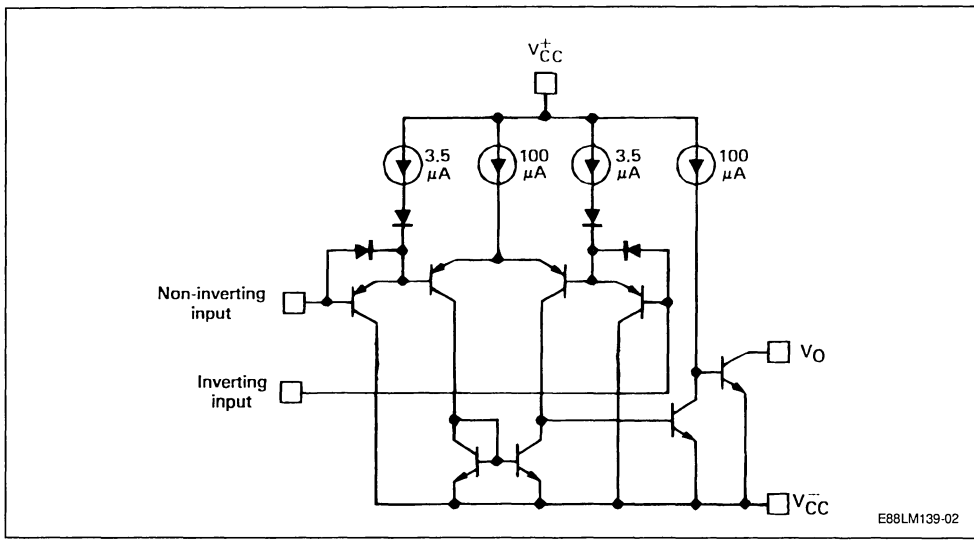
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM139, A LM239, A	LM339, A	LM2901 MC3302	Unit
V_{CC}	Supply Voltage	± 18 to 36	± 18 to 36	± 18 to 36	V
V_{ID}	Differential Input Voltage	36	36	36	V
V_I	Input Voltage	– 0.3 to + 36	– 0.3 to + 36	– 0.3 to + 36	V
	Output Short-circuit to Ground – (note 2)	Continuous	Continuous	Continuous	
P_{tot}	Power Dissipation – (note 1) LM139GC	570 665	570	570	mW
T_{oper}	Operating Free-air Temperature Range LM239, A	– 55 to + 125 – 40 to + 105	0 to + 70	– 40 to + 105	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	– 65 to + 150	– 65 to + 150	°C

Notes : 1. Short-circuit from the output to V_{CC}^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA, independent of the magnitude of V_{CC}.

2. For operating at high temperatures, the LM139, LM139A, LM2901 and MC3302 must be derated based on a + 125 °C max junction temperature and a thermal resistance of 175 °C/W which applies for the device soldered on a printed circuit board, operating in a still air ambient. The LM139 and LM139A must be derated based on a + 150 °C max junction temperature.
$R_{th(j-a)}$ = 250 °C/W. Devices bonded on a 6 x 3 x 0.15 cm glass-epoxy substrate with 30 mm^2 of 35 µm thick copper.

SCHEMATIC DIAGRAM (1/4 LM139)



Case	Outputs	Inverting Inputs	Non–inverting Inputs	V_{CC}^-	V_{CC}^+	N.C.
DIP14 CERDIP14 SO14	1, 2, 13, 14	4, 6, 8, 10	5, 7, 9, 11	12	3	
LCC20	2, 3, 19, 20	6, 9, 12, 14	8, 10, 13, 16	18	4	*

* **LCC20** : Other pins are not connected

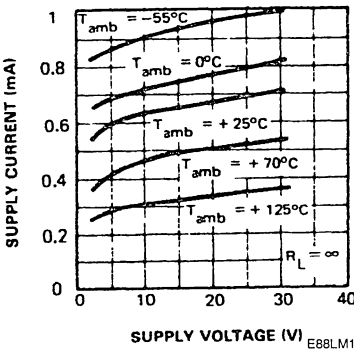
ELECTRICAL CHARACTERISTICS

LM139, A : $-55\,°C < T_{amb} < +125\,°C$
LM239, A, LM2901, MC3302 : $-40\,°C < T_{amb} < +105\,°C$
LM339, A : $0\,°C < T_{amb} < +70\,°C$
(unless otherwise specified) $V_{CC}^{+} = +5\ V$; $V_{CC}^{-} = GND$

Symbol	Parameter	LM139A - LM239A LM339A			LM139 - LM239 LM339 - LM2901 MC3302			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage – (note 3) $T_{amb} = +25\,°C$ $T_{min} \le T_{amb} \le T_{max}$		1	2 4		1	5 9	mV
I_{IO}	Input Offset Current $T_{amb} = +25\,°C$ $T_{min} \le T_{amb} \le T_{max}$		3	25 100		5	50 150	nA
I_{IB}	Input Bias Current (I_I^+ or I_I^-) $T_{amb} = +25\,°C$ – (note 4) $T_{min} \le T_{amb} \le T_{max}$		25	100 300		25	250 400	nA
A_{VD}	Large Signal Voltage Gain $V_{CC}^{+} = +15\ V$, $T_{amb} = +25\,°C$, $R_L \ge 15\ k\Omega$	50	200		25	200		V/mV
I_{CC}	Supply Current, RL = ∞, $T_{amb} = +25\,°C$ (all comparators)		0.8	2		0.8	2	mA
V_I	Input Common-mode Voltage Range (note 5) $T_{amb} = +25\,°C$ $T_{min} \le T_{amb} \le T_{max}$	0 0		$V_{CC}^{+} - 1.5$ $V_{CC}^{+} - 2$	0 0		$V_{CC}^{+} - 1.5$ $V_{CC}^{+} - 2$	V
V_{ID}	Differential Input Voltage ($V_I^+ = 0$, or $V_I^- = 0$, if used) (note 7)			V_{CC}^{+}			V_{CC}^{+}	V
V_{OL}	Low Level Output Voltage ($V_I^- \ge 1\ V$, $V_I^+ = 0\ V$, $I_{sink} \le 4\ mA$) $T_{amb} = +25\,°C$ $T_{min} \le T_{amb} \le T_{max}$		250	400 700		250	400 700	mV
I_{OH}	High Level Output Current ($V_I^+ \ge 1\ V$, $V_I^- = 0\ V$) $T_{amb} = +25\,°C$, $V_O = +5\ V$ $T_{min} \le T_{amb} \le T_{max}$, $V_O = +30\ V$		0.1	 1		0.1	 1	nA µA
$I_{O(sink)}$	Output Sink Current ($V_I^- \ge 1\ V$, $T_{amb} = +25\,°C$, $V_I^+ = 0\ V$, $V_O \le +1.5\ V$)	6	16		6	16		mA
t_{re}	Response Time – (note 6) ($V_L = +5\ V$, $R_L = 5100\ \Omega$, $V_{(ref)} = +1.4\ V$, $T_{amb} = +25\,°C$)		1.3			1.3		µs
t_{rel}	Large Signal Response Time ($V_L = 5\ V$, e_I = TTL, $V_{(ref)} = +1.4\ V$, $T_{amb} = +25\,°C$)		300			300		ns

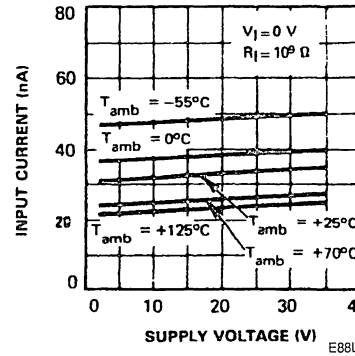
Notes : 3 At output switch point, $V_O \approx 1.4\ V$, $R_S = 0$ with $V_{CC} = 5\ V$, and over the full input common-mode range (0 V to $V_{CC} - 1.5\ V$).
4. The direction of the input current is out of the IC due to the PNP input stage This current is essentially constant, independent of the state of the output, so no loading charge exists on the reference of input lines.
5. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V The upper end of the common-mode voltage range is $V_{CC} - 1.5\ V$, but either or both inputs can go to +30 V without damage
6. The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained
7. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than – 0.3 V (or 0.3 V bellow the negative power supply, if used).

SUPPLY CURRENT



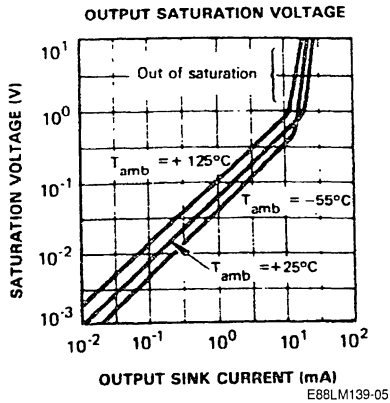
E88LM139-03

INPUT CURRENT



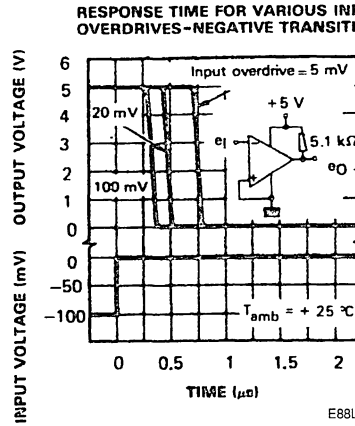
E88LM139-04

OUTPUT SATURATION VOLTAGE



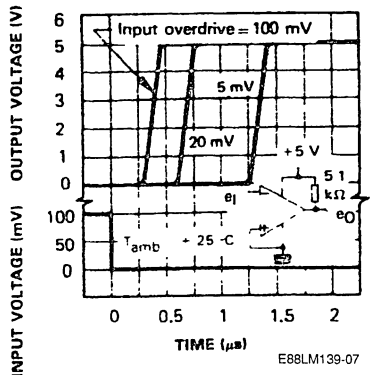
E88LM139-05

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES-NEGATIVE TRANSITION



E88LM139-06

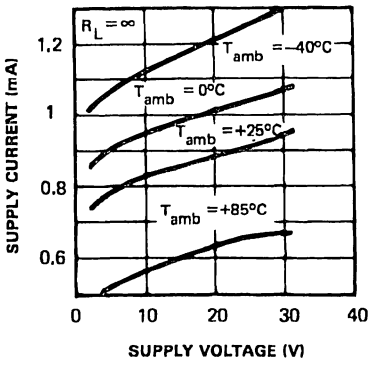
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES - POSITIVE TRANSITION



E88LM139-07

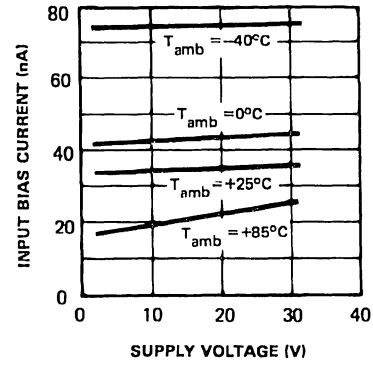
LM239,A
LM2901-MC3302

SUPPLY CURRENT



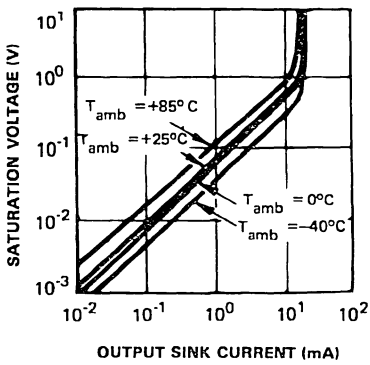
E88LM139-08

SUPPLY CURRENT



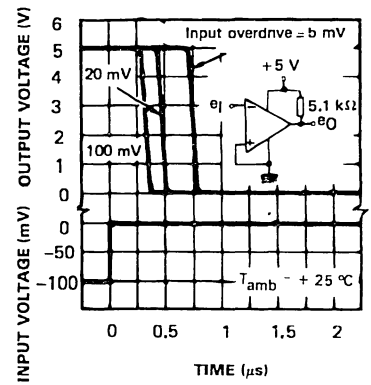
E88LM139-09

OUTPUT SATURATION VOLTAGE



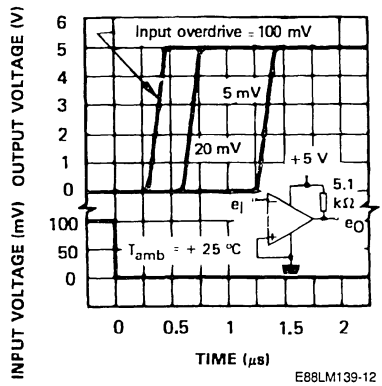
E88LM139-10

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES-NEGATIVE TRANSITION



E88LM139-11

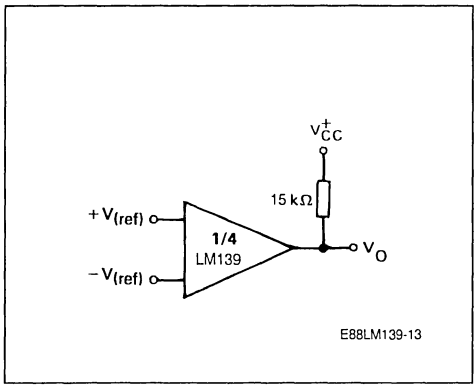
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES - POSITIVE TRANSITION



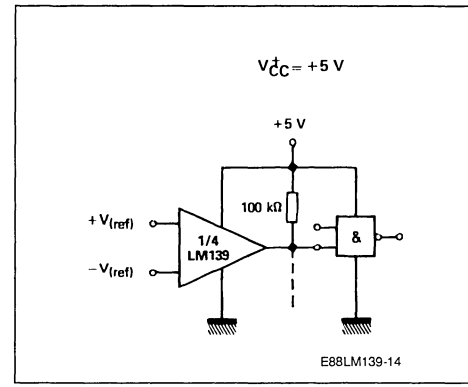
E88LM139-12

TYPICAL APPLICATIONS V_{CC}^{+} = + 5 V

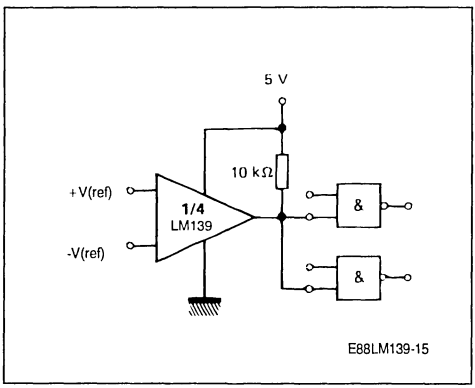
BASIC COMPARATOR



DRIVING CMOS

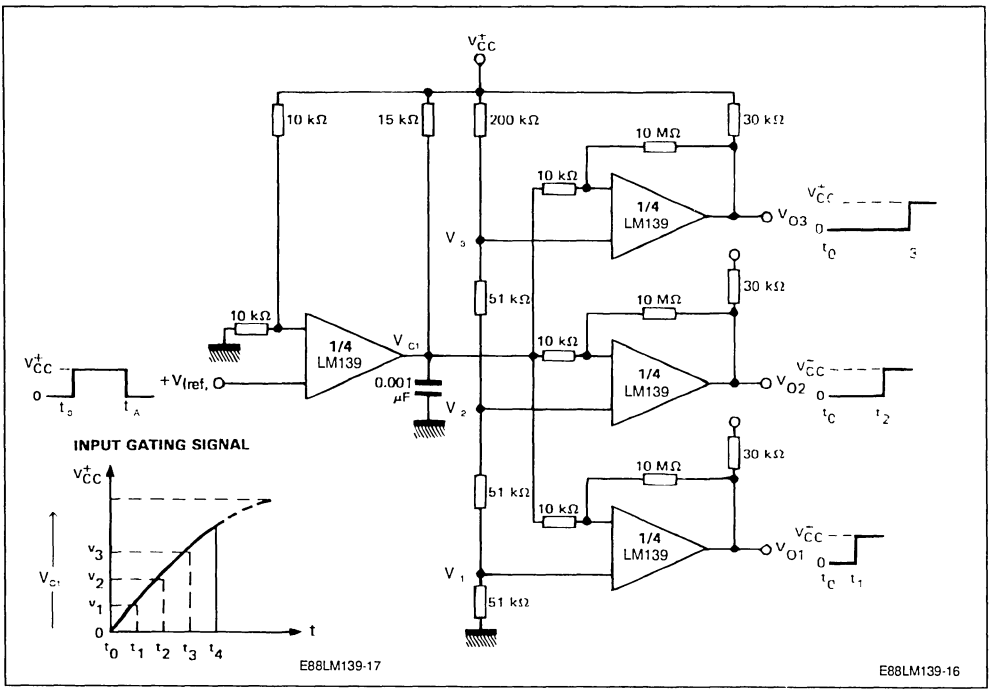


DRIVING TTL

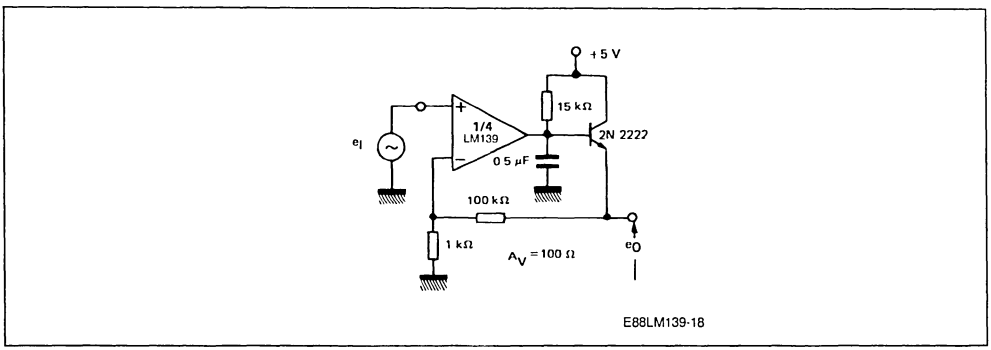


TYPICAL APPLICATIONS (continued)

TIME DELAY GENERATOR

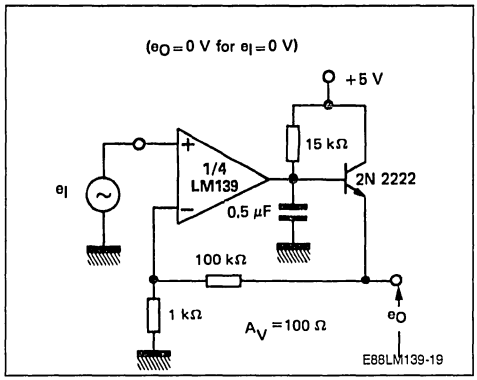


LOW FREQUENCY OP AMP

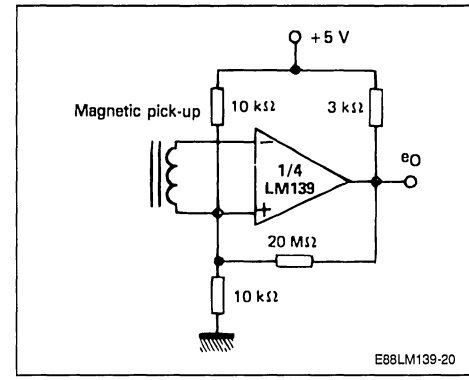


TYPICAL APPLICATIONS (continued)

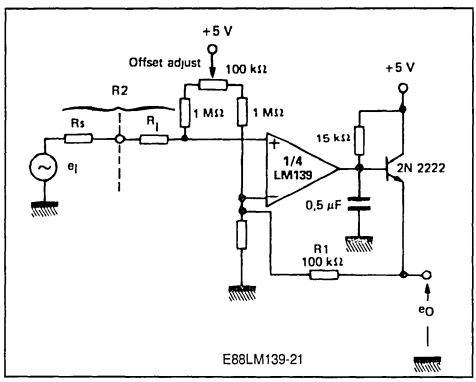
LOW FREQUENCY OP AMP



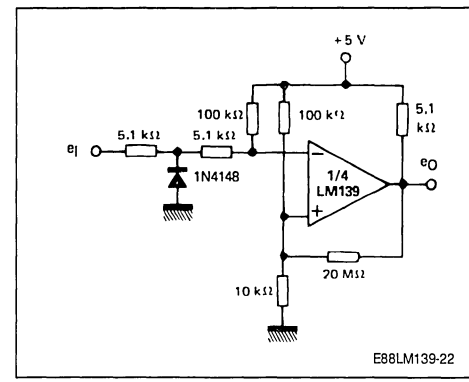
TRANSDUCER AMPLIFIER



LOW FREQUENCY OP AMP WITH OFFSET ADJUST

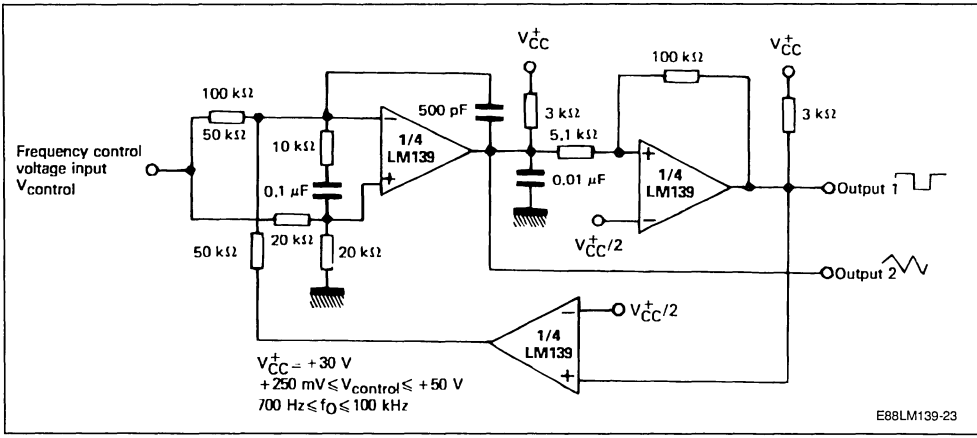


ZERO CROSSING DETECTOR (single power supply)

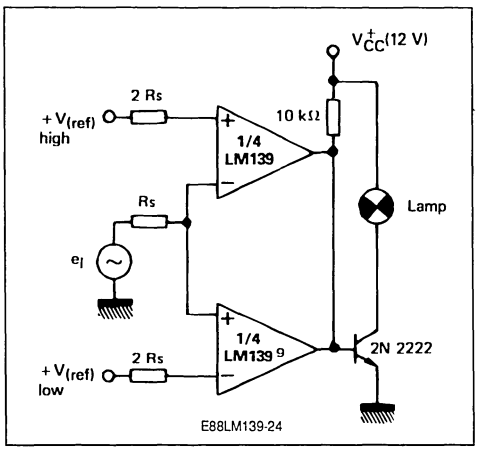


TYPICAL APPLICATIONS (continued)

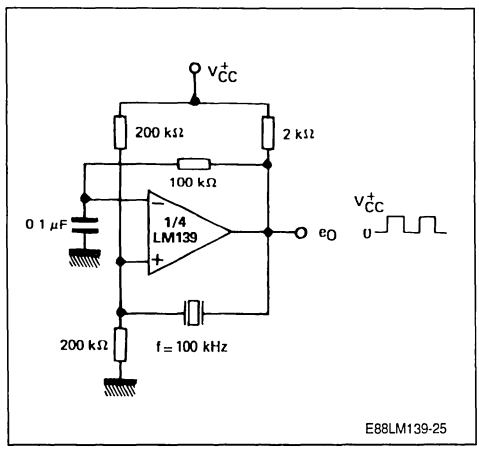
TWO-DECADE HIGH-FREQUENCY VCO



LIMIT COMPARATOR

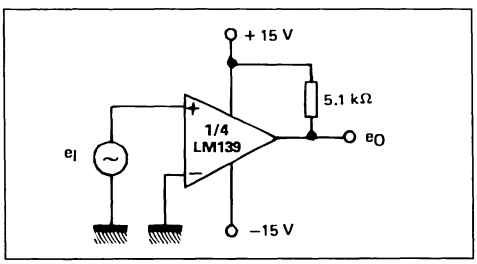


CRYSTAL CONTROLLED OSCILLATOR

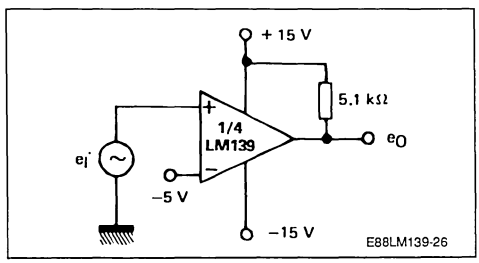


SPLIT-SUPPLY APPLICATIONS

ZERO CROSSING DETECTOR

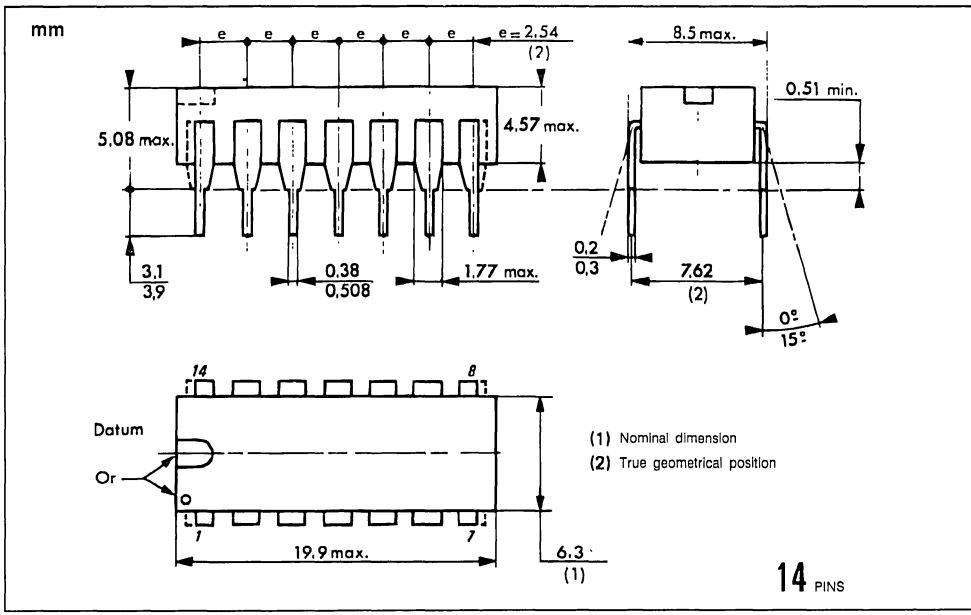


COMPARATOR WITH A NEGATIVE REFERENCE

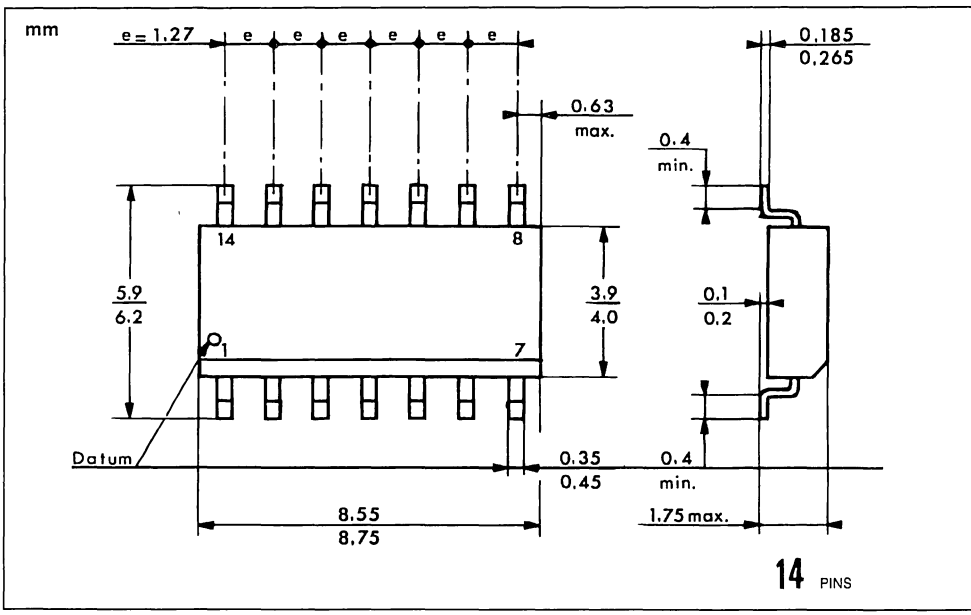


PACKAGE MECHANICAL DATA

14 PINS – PLASTIC DIP OR CERDIP

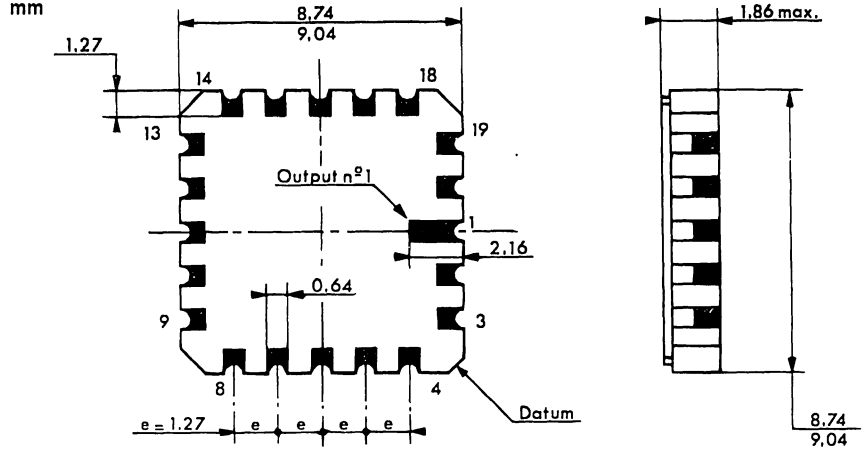


14 PINS – PLASTIC MICROPACKAGE (SO)



PACKAGE MECHANICAL DATA (continued)

20 PINS – TRICECOP (LCC)



SGS-THOMSON MICROELECTRONICS

LM146
LM246-LM346

PROGRAMMABLE QUAD OPERATIONAL AMPLIFIERS

- PROGRAMMABLE ELECTRICAL CHARACTERISTICS
- BATTERY POWERED OPERATION
- LOW SUPPLY CURRENT (250 µA/amplifier)
- GAIN-BANDWIDTH PRODUCT : 1 MHz
- LARGE DC VOLTAGE GAIN : 120 dB
- LOW NOISE VOLTAGE : 28 nV/√Hz
- WIDE POWER SUPPLY RANGE : ± 1.5 V TO ± 22 V
- CLASSE AB OUTPUT STAGE. NO CROSS-OVER DISTORTION
- OVERLOAD PROTECTION FOR INPUTS AND OUTPUTS

DESCRIPTION

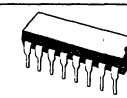
The LM346 consists of four independent, high gain, internally compensated, low power programmable amplifiers. Two external resistors (R_{set}) allow the user to program the gain-bandwith product, slew rate, supply current, input bias current, input offset current and input noise. For example the user can trade-off supply current for bandwidth or optimize noise figure for a given source resistance. In a similar way other amplifier characteristics can be tailored to the application.

Except for the two programming pins at the end of the package the LM346 pin out is the same as the LM324 and LM348.

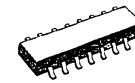
PROGRAMMING EQUATIONS :

Total supply current = 1 mA (I_{set} = 10 µA)
Gain-bandwith product = 1 MHz (I_{set} = 10 µA)
Slew rate = 0.5 V/µs (I_{set} = 10 µA)
Input bias current ≈ 30 nA (I_{set} = 10 µA)
I_{set} = current into pin 8 and pin 9 (see schematic diagram)

$$I_{set} = \frac{V_{cc}^{+} - V_{cc}^{-} - 0.6\ V}{R_{set}}$$



N – DIP16 – (Plastic Package)
J – CERDIP16 – (Cerdip Package)



D
SO16
(Plastic Micropackage)

GC
LCC20
(Tricecop (LCC))

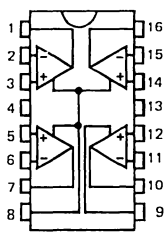
ORDER CODES

Part Number	Temperature Range	Package			
		N	J	D	GC
LM146	– 55 °C to + 125 °C		•		•
LM246	– 40 °C to + 105 °C	•	•	•	
LM346	0 °C to + 70 °C	•	•	•	

Note : Hi-rel Versions Available
Examples : LM146J, LM246N

PIN CONNECTIONS (top views)

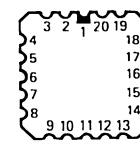
DIP16 / CERDIP16
SO16



1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{cc}^{-}
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - Set
9 - Set
10 - Output 3
11 - Inverting input 3
12 - Non-inverting input 3
13 - V_{cc}^{+}
14 - Non-inverting input 4
15 - Inverting input 4
16 - Output 4

E88LM146-01

LCC20



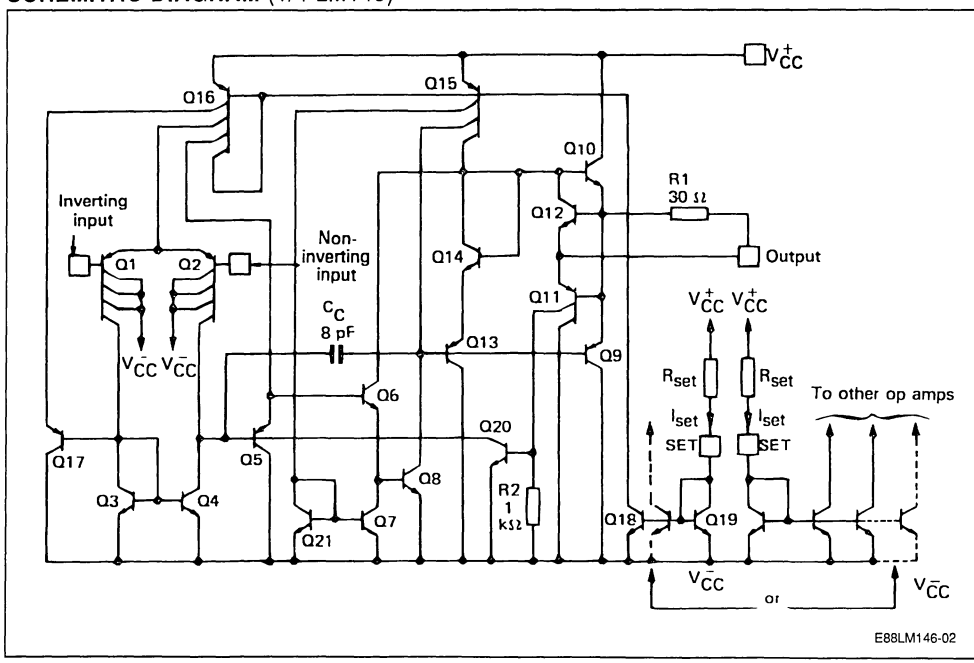
1 - NC
2 - Output 1
3 - Inverting input 1
4 - Non-inverting input 1
5 - V_{cc}^{-}
6 - NC
7 - Non-inverting input 2
8 - Inverting input 2
9 - Output 2
10 - Set 1, 2, 4
11 - NC
12 - Set 3
13 - Output 3
14 - Inverting input 3
15 - Non-inverting input 3
16 - NC
17 - V_{cc}^{+}
18 - Non-inverting input 4
19 - Inverting input 4
20 - Output 4

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM146	LM246	LM346	Unit
V_{CC}	Supply Voltage	± 22	± 22	± 22	V
V_I	Input Voltage (note 1)	± 15	± 15	± 15	V
V_{ID}	Differential Input Voltage	± 30	± 30	± 30	V
	Output Short-circuit Duration (note 2)	Indefinite	Indefinite	Indefinite	
P_{tot}	Power Dissipation N/D Suffix		500	500	mW
	GC Suffix	665			
	J Suffix	900	900	900	
T_{oper}	Operating Free-air Temperature Range	− 55 to + 125	− 40 to + 105	0 to + 70	°C
T_{stg}	Storage Temperature Range	− 65 to + 150	− 65 to + 150	− 65 to + 150	°C

Notes : 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Any of the amplifier outputs can be shorted to ground indefinitly ; however more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

SCHEMATIC DIAGRAM (1/4 LM146)



Case	Inverting Inputs	Non-inverting Inputs	V_{CC}^-	V_{CC}^+	Outputs	Set	N.C.
DIP16 CERDIP16 SO16	3, 5, 12, 14	2, 6, 11, 15	13	4	1, 7, 10, 16	8, 9	
LCC 20	3, 8, 14, 19	4, 7, 15, 18	17	5	2, 9, 13, 20	10, 12	*

* **LCC20 :** Other pins are not connected.

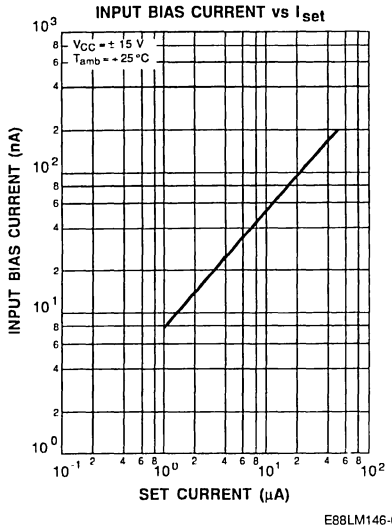
ELECTRICAL CHARACTERISTICS

LM346 : $0\ °C \le T_{amb} \le +\ 70\ °C$, $V_{CC} = \pm 15$ V, $I_{set} = 10\ \mu A$
LM246 : $-40\ °C \le T_{amb} \le +105\ °C$, $V_{CC} = \pm 15$ V, $I_{set} = 10\ \mu A$
LM146 : $-55\ °C \le T_{amb} \le +125\ °C$, $V_{CC} = \pm 15$ V, $I_{set} = 10\ \mu A$

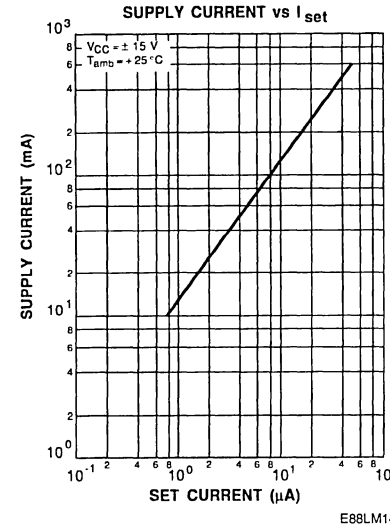
Symbol	Parameter	LM146-LM246-LM346			Unit
		Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage ($R_S \le 10$ kΩ) $T_{amb} = 25$ °C $T_{min} \le T_{amb} \le T_{max}$		0.5	3 5	mV
I_{IO}	Input Offset Current $T_{amb} = 25$ °C $T_{min} \le T_{amb} \le T_{max}$		2	20 25	nA
I_{IB}	Input Bias Current $T_{amb} = 25$ °C $T_{min} \le T_{amb} \le T_{max}$		30	100 100	nA
A_{vd}	Large Signal Voltage Gain ($V_o = \pm 10$ V, $R_L = 10$ kΩ) $T_{amb} = 25$ °C $T_{min} \le T_{amb} \le T_{max}$	 100 50	 1000		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S \le 10$ kΩ) $T_{amb} = 25$ °C $T_{min} \le T_{amb} \le T_{max}$	 80 80	 110		dB
I_{CC}	Supply Current, all Amp, no Load $T_{amb} = 25$ °C $T_{min} \le T_{amb} \le T_{max}$		1	2 2	mA
V_I	Input Voltage Range $T_{amb} = 25$ °C $T_{min} \le T_{amb} \le T_{max}$	 −13.5 −13.5		 +13.5 +13.5	V
CMR	Common Mode Rejection Ratio ($R_S \le 10$ kΩ) $T_{amb} = 25$ °C $T_{min} \le T_{amb} \le T_{max}$	 80 70	 110		dB
I_{OS}	Output Short-circuit Current $T_{amb} = 25$ °C $T_{min} \le T_{amb} \le T_{max}$	 10 4	 20	 30 35	mA
$\pm V_{opp}$	Output Voltage Swing $T_{amb} = 25$ °C $R_L = 10$ kΩ $T_{min} \le T_{amb} \le T_{max}$ $R_L = 10$ kΩ	 12 12	 14		V
S_{vo}	Slew-rate ($V_I = \pm 10$ V, $R_L = 10$ kΩ, $C_L \le 100$ pF, $T_{amb} = 25$ °C, Unity Gain)	0.3	0.5		V/μs
R_I	Input Resistance, $T_{amb} = 25$ °C		1		MΩ
C_I	Input Capacitance, $T_{amb} = 25$ °C		2		pF

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	LM146-LM246-LM346			Unit
		Min.	Typ.	Max.	
V_{o1}/V_{o2}	Channel Separation ($R_L \geq 10$ KΩ) ($V_o = 12\ V_{pp}$)		120		dB
GPB	Gain Bandwidth Product ($V_i = 10$ mV, $R_L = 10$ KΩ, $C_L \leq 100$ pF f = 100 KHz, $T_{amb} = 25$ °C)	0.8	1	1.6	MHz
THD	Total Harmonic Distortion (f = 1 KHz, $A_v = 20$ dB, $R_L = 10$ KΩ $C_L \leq 100$ pF, $T_{amb} = 25$ °C, $V_o = 2\ V_{pp}$)		0.015		%
V_n	Equivalent Input Noise Voltage (f = 1 KHz $R_g = 100\ \Omega$)		28		$nV/\sqrt{Hz}$

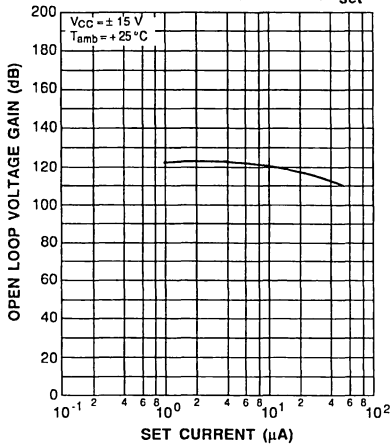


E88LM146-03



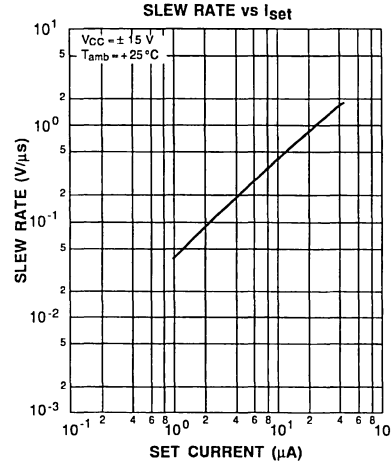
E88LM146-04

OPEN LOOP VOLTAGE GAIN vs I_{set}



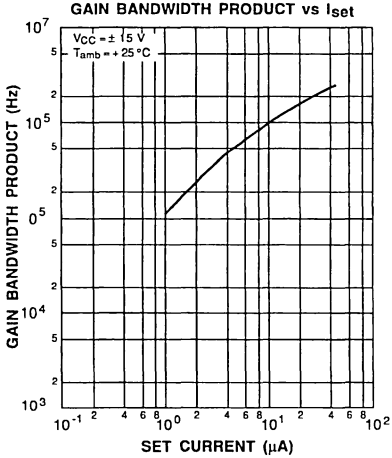
E88LM146-05

SLEW RATE vs I_{set}



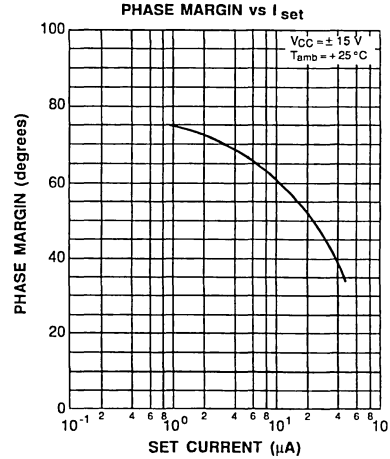
E88LM146-06

GAIN BANDWIDTH PRODUCT vs I_{set}



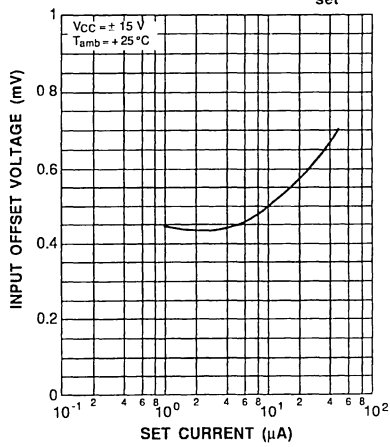
E88LM146-07

PHASE MARGIN vs I_{set}



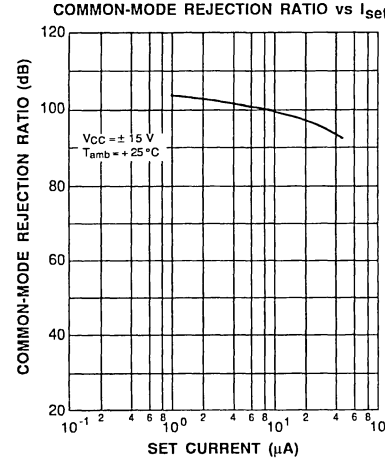
E88LM146-08

INPUT OFFSET VOLTAGE vs I_{set}



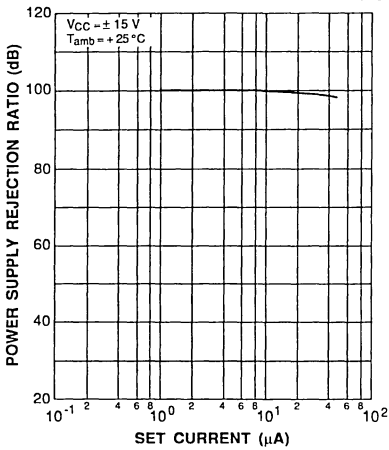
E88LM146-09

COMMON-MODE REJECTION RATIO vs I_{set}



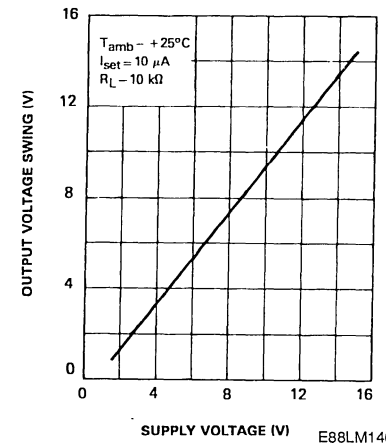
E88LM146-10

POWER SUPPLY REJECTION RATIO vs I_{set}



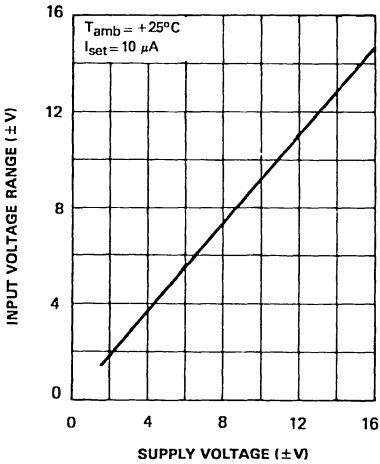
E88LM146-11

OUTPUT VOLTAGE SWING



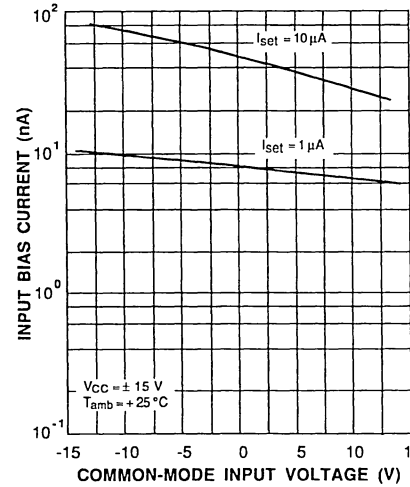
E88LM146-12

INPUT VOLTAGE RANGE



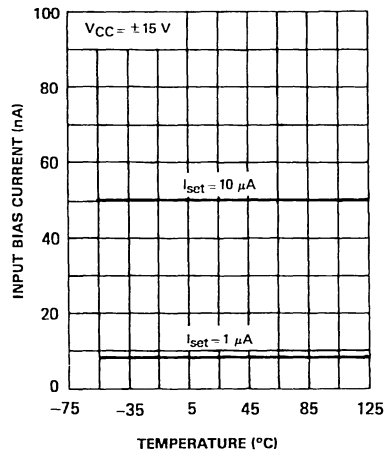
E88LM146-13

INPUT BIAS CURRENT



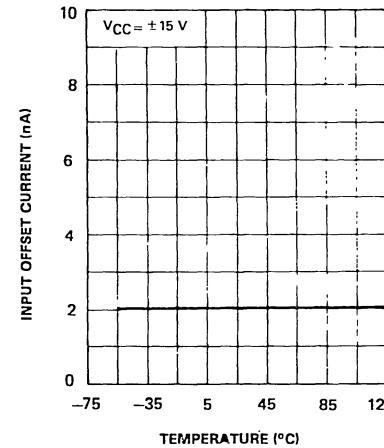
E88LM146-14

INPUT BIAS CURRENT vs TEMPERATURE



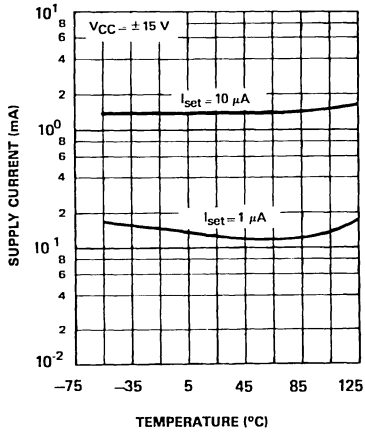
E88LM146-15

INPUT OFFSET CURRENT vs TEMPERATURE



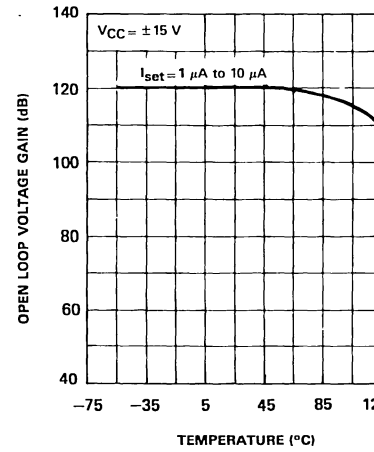
E88LM146-16

SUPPLY CURRENT vs TEMPERATURE



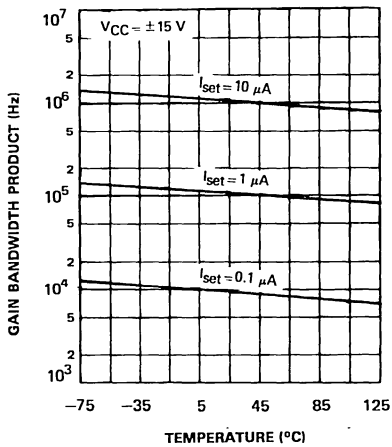
E88LM146-17

OPEN LOOP VOLTAGE GAIN vs TEMPERATURE



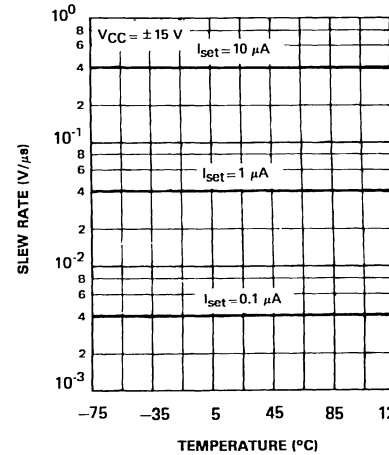
E88LM146-18

GAIN BANDWIDTH PRODUCT vs TEMPERATURE



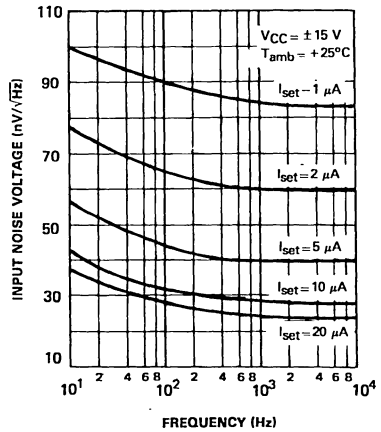
E88LM146-19

SLEW RATE vs TEMPERATURE



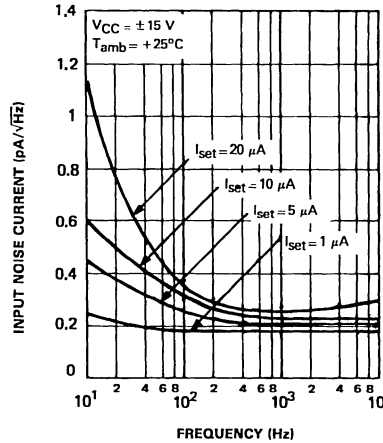
E88LM146-20

INPUT NOISE VOLTAGE vs FREQUENCY



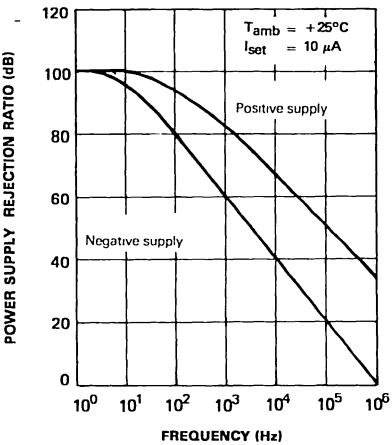
E88LM146-21

INPUT NOISE CURRENT vs FREQUENCY



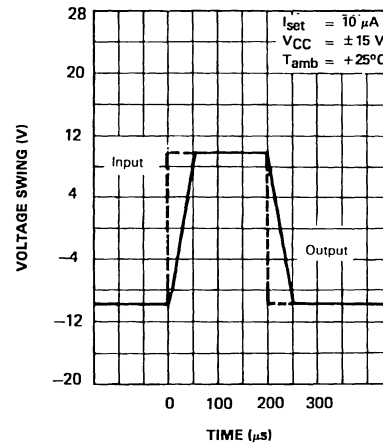
E88LM146-22

POWER SUPPLY REJECTION RATIO

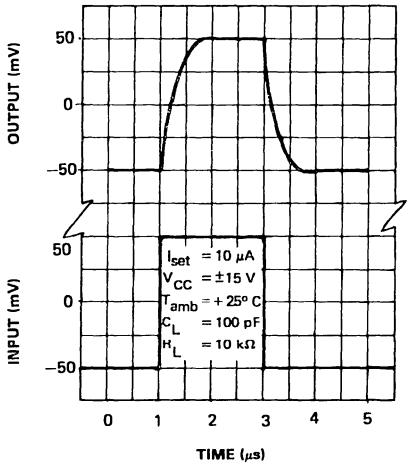


E88LM146-23

VOLTAGE FOLLOWER PULSE RESPONSE

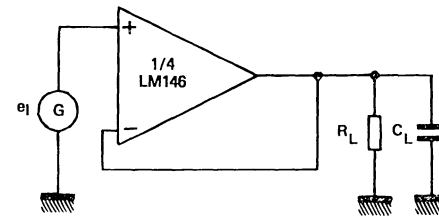


E88LM146-24



E88LM146-25

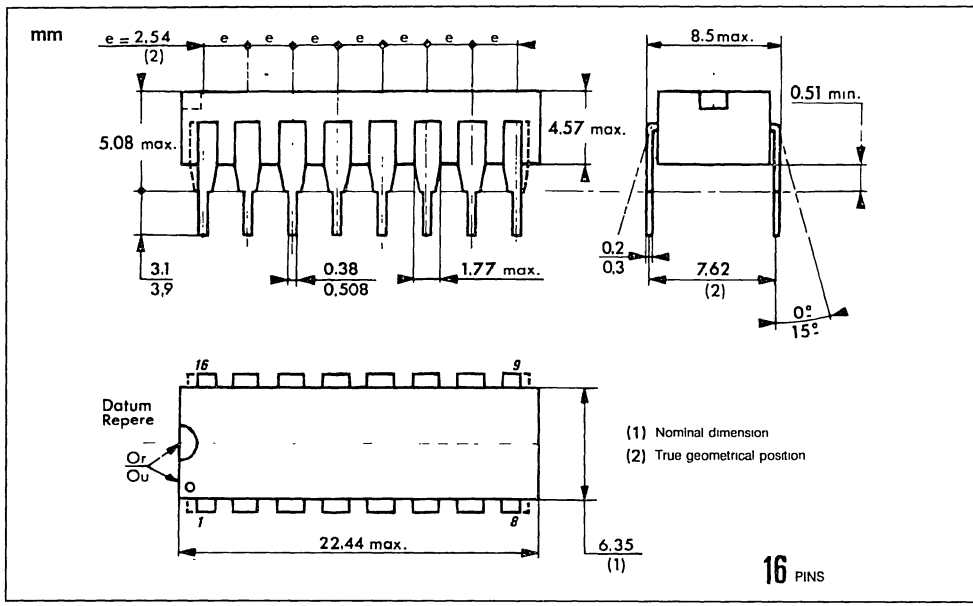
TRANSIENT RESPONSE TEST CIRCUIT



E88LM146-26

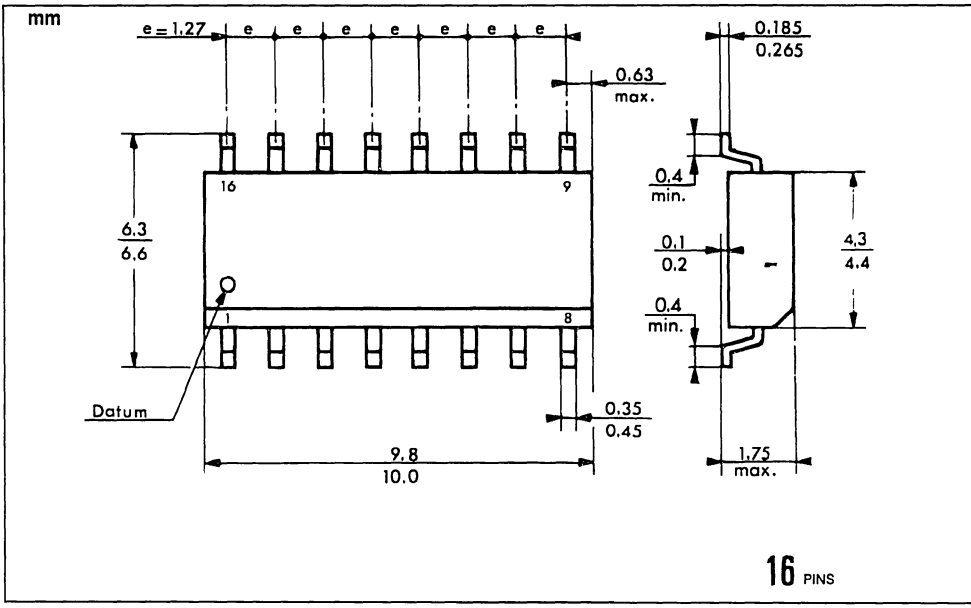
PACKAGE MECHANICAL DATA

16 PINS – PLASTIC DIP OR CERDIP

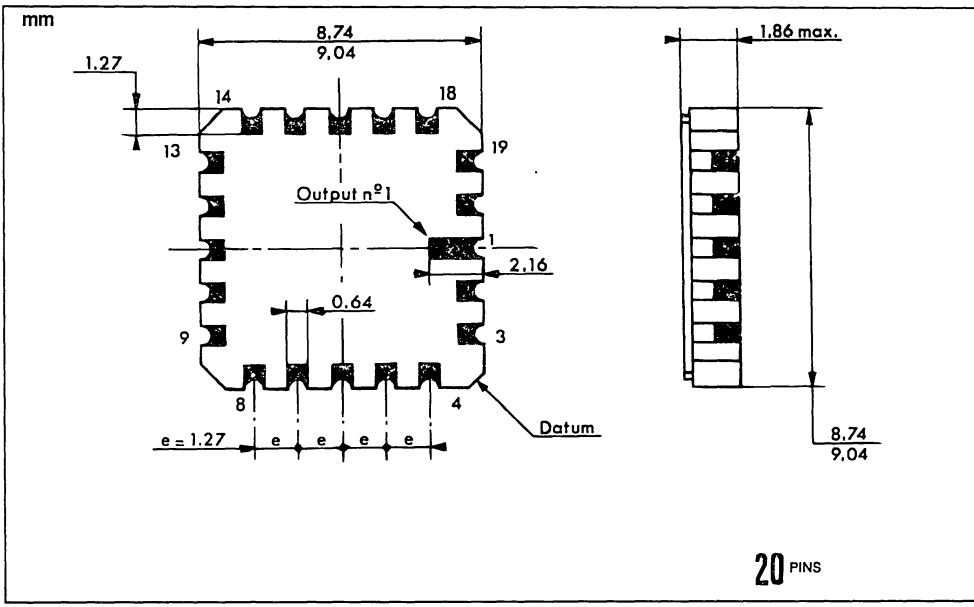


PACKAGE MECHANICAL DATA (continued)

16 PINS – PLASTIC MICROPACKAGE (SO)



20 PINS – TRICECOP (LCC)

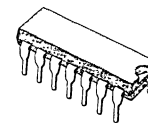


SGS-THOMSON MICROELECTRONICS

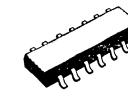
LM148-LM248 LM348

DIFFERENTIAL INPUT QUAD OP-AMPs

- LOW SUPPLY CURRENT : 0.53 mA/AMPLIFIER
- CLASS AB OUTPUT STAGE : NO CROSSOVER DISTORTION
- PIN COMPATIBLE WITH LM124
- LOW INPUT OFFSET VOLTAGE : 1 mV
- LOW INPUT OFFSET CURRENT : 2 nA
- LOW INPUT BIAS CURRENT : 30 nA
- GAIN BANDWIDTH PRODUCT : 1.3 MHz
- HIGH DEGREE OF ISOLATION BETWEEN AMPLIFIERS : 120 dB
- OVERLOAD PROTECTION FOR INPUTS AND OUTPUTS



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

J
CERDIP14
(Cerdip Package)

GC
LCC20
(Tricecop (LCC))

DESCRIPTION

The LM148 consists of four independent, high gain internally compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar UA741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a single UA741 type op amp. Other features include input offset current and input bias current which are much less than those of a standard UA741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.

The LM148 can be used anywhere multiple UA741 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

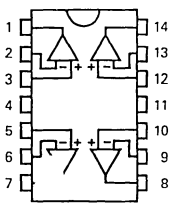
ORDER CODES

Part Number	Temperature Range	Package			
		N	J	GC	D
LM148	– 55 °C to + 125 °C		•	•	
LM248	– 40 °C to + 105 °C	•		•	•
LM348	0 °C to + 70 °C	•			•

Note : Hi-Rel Versions Available
Examples : LM148J, LM349D

PIN CONNECTIONS (top views)

DIP14/CERDIP14
SO14



1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{cc}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - Output 3
9 - Inverting input 3
10 - Non-inverting input 3
11 - V_{cc}^+
12 - Non-inverting input 4
13 - Inverting input 4
14 - Output 4

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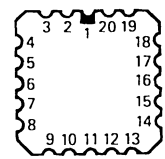
LCC20



1 - NC
2 - Output 1
3 - Inverting input 1
4 - Non-inverting input 1
5 - NC
6 - V_{cc}^-
7 - NC
8 - Non-inverting input 2
9 - Inverting input 2
10 - Output 2
11 - NC
12 - Output 3
13 - Inverting input 3
14 - Non-inverting input 3
15 - NC
16 - V_{cc}^+
17 - NC
18 - Non-inverting input 4
19 - Inverting input 4
20 - Output 4

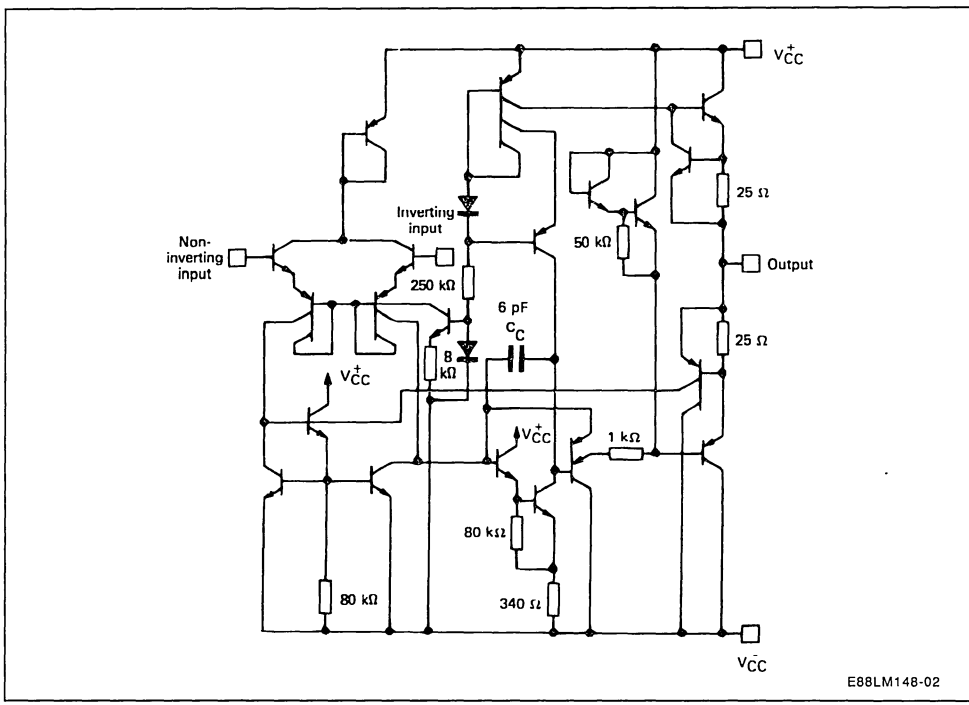
E88LM148-01

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM148	LM248	LM348	Unit
V_{CC}	Supply Voltage	± 22	± 22	± 22	V
V_{ID}	Differential Input Voltage	± 44	± 44	± 44	V
V_I	Input Voltage (note 1)	± 22	± 22	± 22	V
P_{tot}	Power Dissipation	500	500	500	mW
	Output Short-circuit Duration (note 2)	Indefinite	Indefinite	Indefinite	
T_{oper}	Operating Free-air Temperature Range	– 55 to + 125	– 40 to + 105	0 to + 70	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	– 65 to + 150	– 65 to + 150	°C

Notes : 1. For supply voltage less than maximum value, the absolute maximum input voltage is equal to the supply vol-tage.
2. Any of the amplifier outputs can be shorted to ground indefinitely ; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

SCHEMATIC DIAGRAM



Case	Outputs	Inverting Inputs	Non-inverting Inputs	V_{CC}^+	V_{CC}^-	N.C.
DIP14 CERDIP14/SO14	1, 7, 8, 14	2, 6, 9, 13	3, 5, 10, 12	4	11	
LCC20	2, 10, 12, 20	3, 9, 13, 19	4, 8, 14, 18	6	16	*

* **LCC20** : Other pins are not connected.

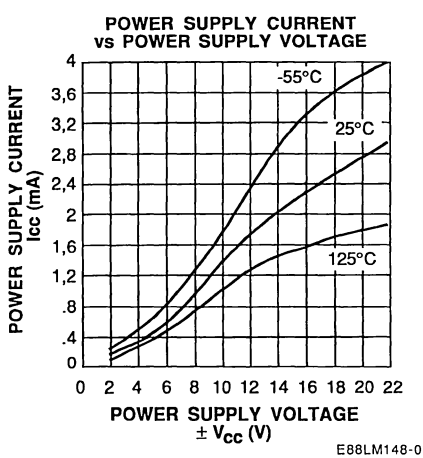
ELECTRICAL CHARACTERISTICS

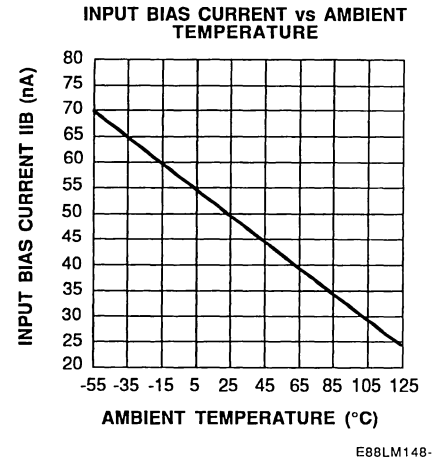
LM148 : $-55\,°C \le T_{amb} \le +125\,°C$, $V_{CC} = \pm 15\,V$
LM248 : $-40\,°C \le T_{amb} \le +105\,°C$, $V_{CC} = \pm 15\,V$
LM348 : $0\,°C \le T_{amb} \le +70\,°C$, $V_{CC} = \pm 15\,V$
(unless otherwise specified)

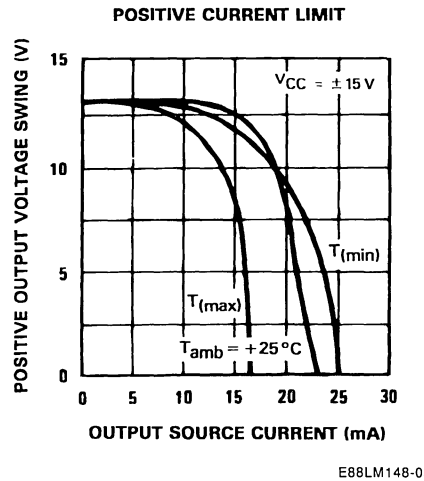
Symbol	Parameter	LM148/248/348			Unit
		Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage $R_S \le 10\,k\Omega$ $T_{amb} = +25\,°C$ $T_{min} \le T_{amb} \le T_{max}$		1	5 6	mV
I_{IO}	Input Offset Current $T_{amb} = +25\,°C$ $T_{min} \le T_{amb} \le T_{max}$		2	20 40	nA
I_{IB}	Input Bias Current $T_{amb} = +25\,°C$ $T_{min} \le T_{amb} \le T_{max}$		30	100 200	nA
A_{VD}	Large Signal Voltage Gain ($V_O = \pm 10\,V$, $R_L \ge 2\,k\Omega$) $T_{amb} = +25\,°C$ $T_{min} \le T_{amb} \le T_{max}$	 50 25	160		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S \le 10\,k\Omega$) $T_{amb} = +25\,°C$ $T_{min} \le T_{amb} \le T_{max}$	 77 77	100		dB
I_{CC}	Supply Current, all Amp, no Load $T_{amb} = +25\,°C$ $T_{min} \le T_{amb} \le T_{max}$		2.1	3.6 4.8	mA
V_I	Input Voltage Range $T_{amb} = +25\,°C$ $T_{min} \le T_{amb} \le T_{max}$	 −12 −12		 +12 +12	V
CMR	Common-mode Rejection Ratio ($R_S \le 10\,k\Omega$) $T_{amb} = +25\,°C$ $T_{min} \le T_{amb} \le T_{max}$	 70 70	110		dB
I_{OS}	Output Short-circuit Current $T_{amb} = +25\,°C$	 10	25	35	mA
$\pm V_{OPP}$	Output Voltage Swing $T_{amb} = +25\,°C$ $R_L = 10\,k\Omega$ $R_L = 2\,k\Omega$ $T_{min} \le T_{amb} \le T_{max}$ $R_L = 10\,k\Omega$ $R_L = 2\,k\Omega$	 12 10 12 10	 13 12		V
S_{VO}	Slew Rate ($V_i = \pm 10\,V$, $R_L = 2\,k\Omega$, $C_L \le 100\,pF$, $T_{amb} = +25\,°C$, unity gain)	 0.25	 0.5		V/µs
t_r	Rise Time ($V_i = \pm 20\,mV$, $R_L = 2\,k\Omega$, $C_L \le 100\,pF$, $T_{amb} = +25\,°C$, unity gain)		 0.3		µs
K_{ov}	Overshoot ($V_i = \pm 20\,mV$, $R_L = 2\,k\Omega$, $C_L \le 100\,pF$, $T_{amb} = +25\,°C$, unity gain)		 5		%
R_I	Input Resistance, $T_{amb} = +25\,°C$	0.8	2.5		MΩ
GPB	Gain-bandwidth Product ($V_i = \pm 10\,mV$, $R_L = 2\,k\Omega$, $C_L \le 100\,pF$, $f = 100\,KHz$, $T_{amb} = +25\,°C$)	 0.7	 1.3	 1.6	MHz

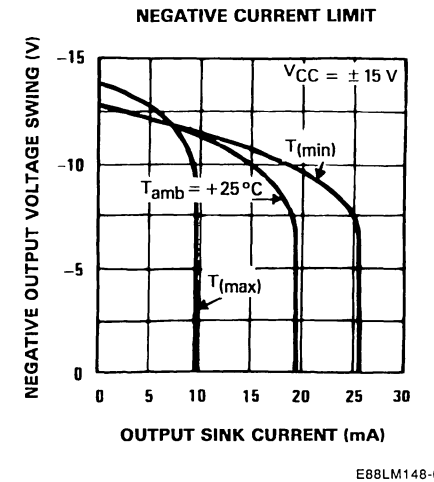
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	LM148/248/348			Unit
		Min.	Typ.	Max.	
THD	Total Harmonic Distortion ($f = 1$ KHz, $A_v = 20$ dB, $R_L = 2$ kΩ, $V_O = 2\ V_{PP}$, $C_L \leq 100$ pF, $T_{amb} = +25$ °C)		0.08		%
V_n	Equivalent Input Noise Voltage ($f = 1$ kHz, $R_G = 100\ \Omega$)		40		$nV/\sqrt{Hz}$
V_{01}/V_{02}	Channel Separation		120		dB

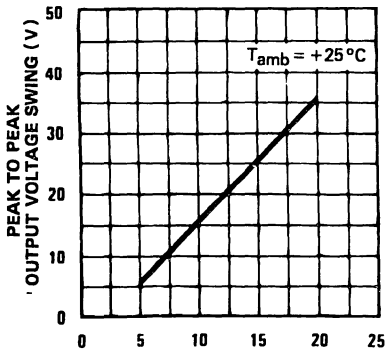






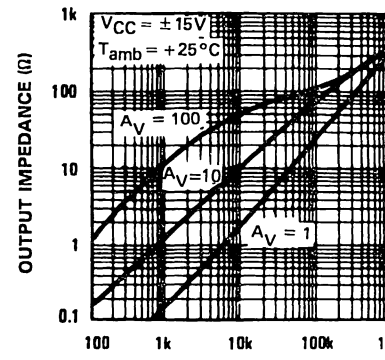


OUTPUT VOLTAGE SWING



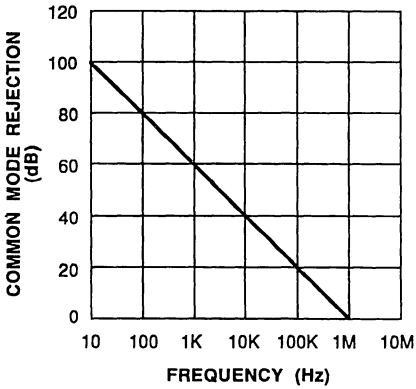
E88LM148-07

OUTPUT IMPEDANCE



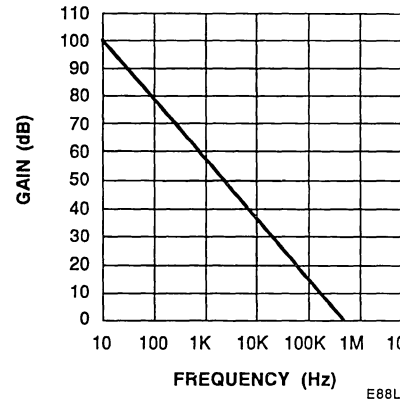
E88LM148-08

COMMON MODE REJECTION RATIO vs FREQUENCY



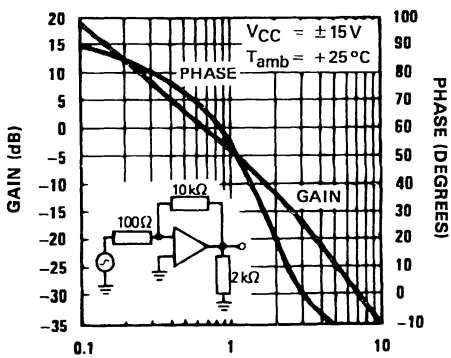
E88LM148-09

OPEN LOOP FREQUENCY RESPONSE



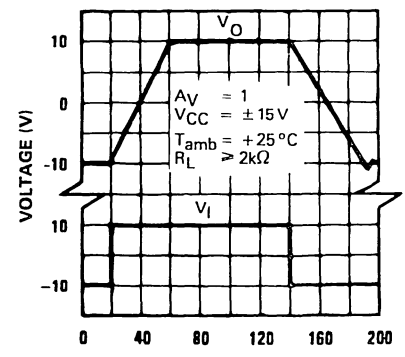
E88LM148-10

BODE PLOT (LM148)



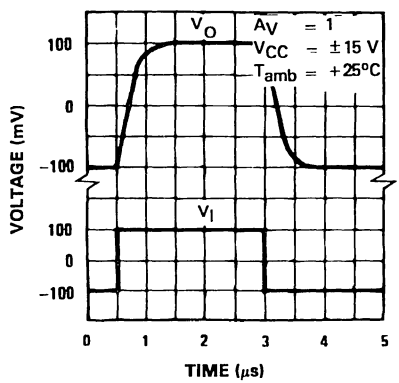
E88LM148-13

LARGE SIGNAL PULSE RESPONSE (LM148)



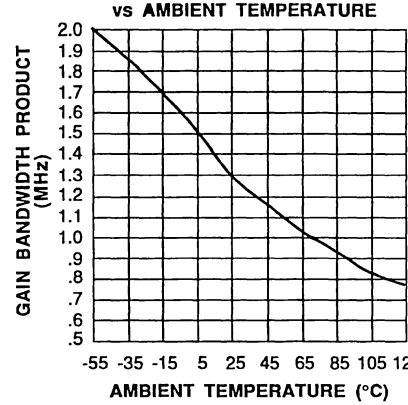
E88LM148-14

SMALL SIGNAL PULSE RESPONSE (LM148)



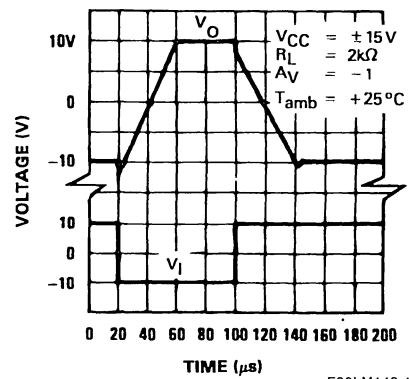
E88LM148-15

GAIN BANDWIDTH PRODUCT vs AMBIENT TEMPERATURE



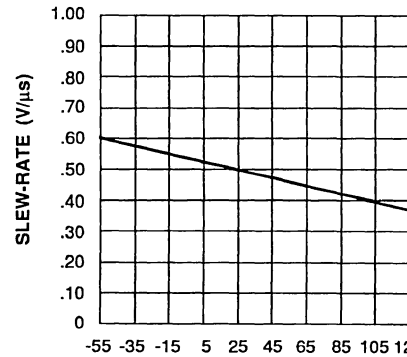
E88LM148-17

INVERTING LARGE SIGNAL PULSE RESPONSE (LM148)



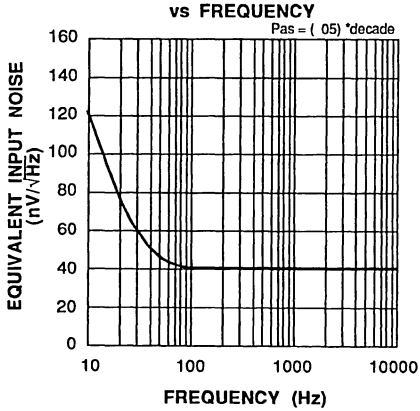
E88LM148-19

SLEW-RATE vs TEMPERATURE



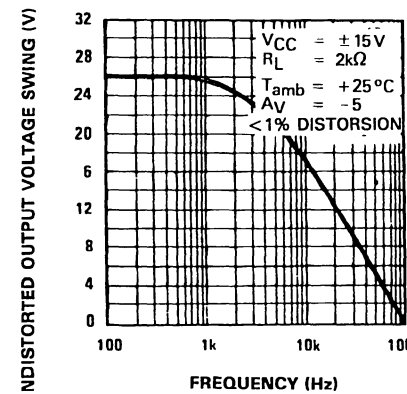
E88LM148-20

EQUIVALENT INPUT NOISE vs FREQUENCY



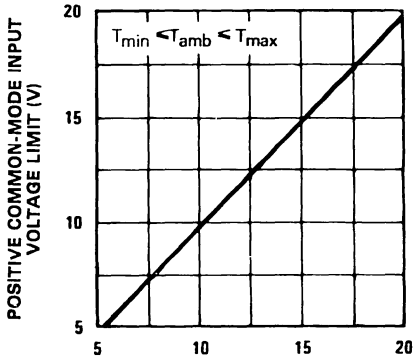
E88LM148-21

UNDISTORTED OUTPUT VOLTAGE SWING



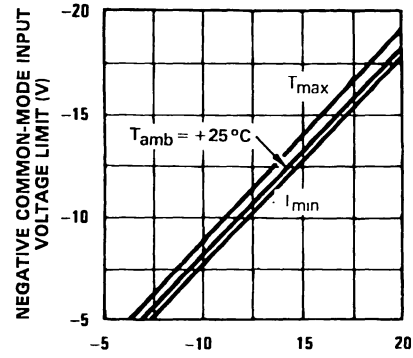
E88LM148-22

POSITIVE COMMON-MODE INPUT VOLTAGE LIMIT



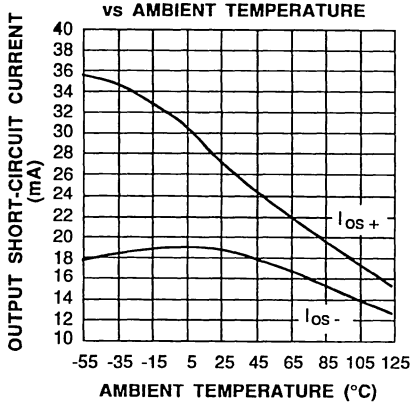
E88LM148-23

NEGATIVE COMMON-MODE INPUT VOLTAGE LIMIT



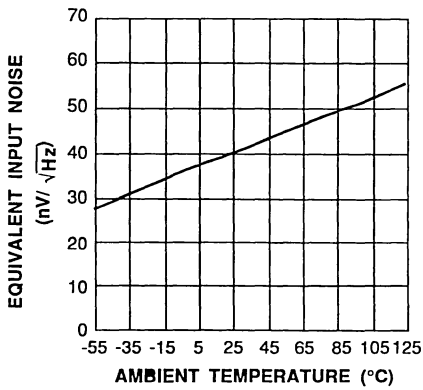
E88LM148-24

OUTPUT SHORT-CIRCUIT CURRENT vs AMBIENT TEMPERATURE



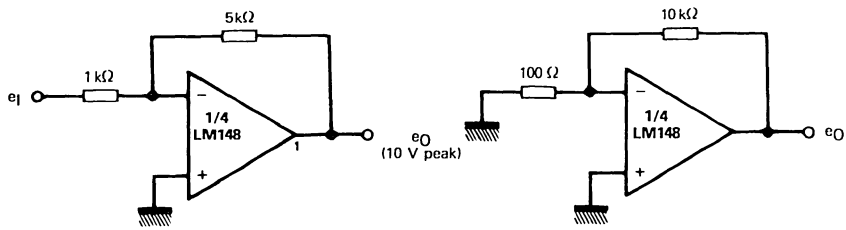
E88LM148-26

EQUIVALENT INPUT NOISE vs AMBIENT TEMPERATURE



E88LM148-27

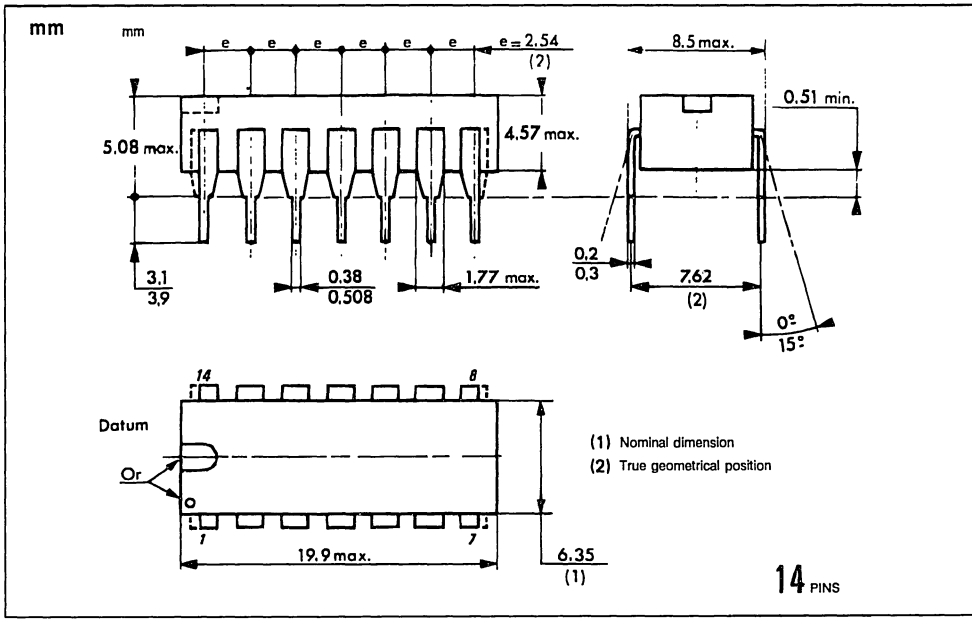
TEST CIRCUITS



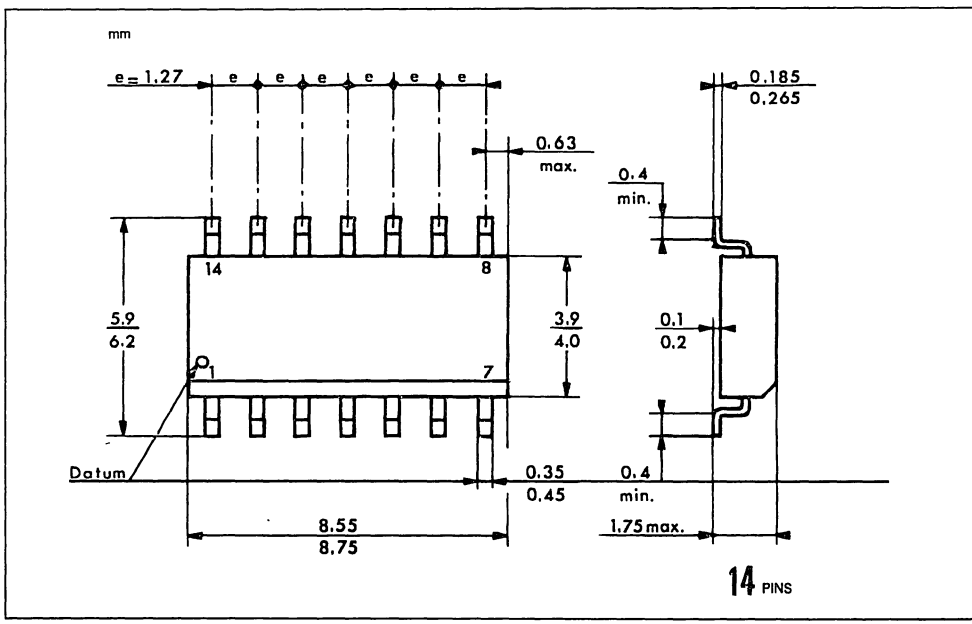
E88LM148-25

PACKAGE MECHANICAL DATA

14 PINS – PLASTIC DIP OR CERDIP

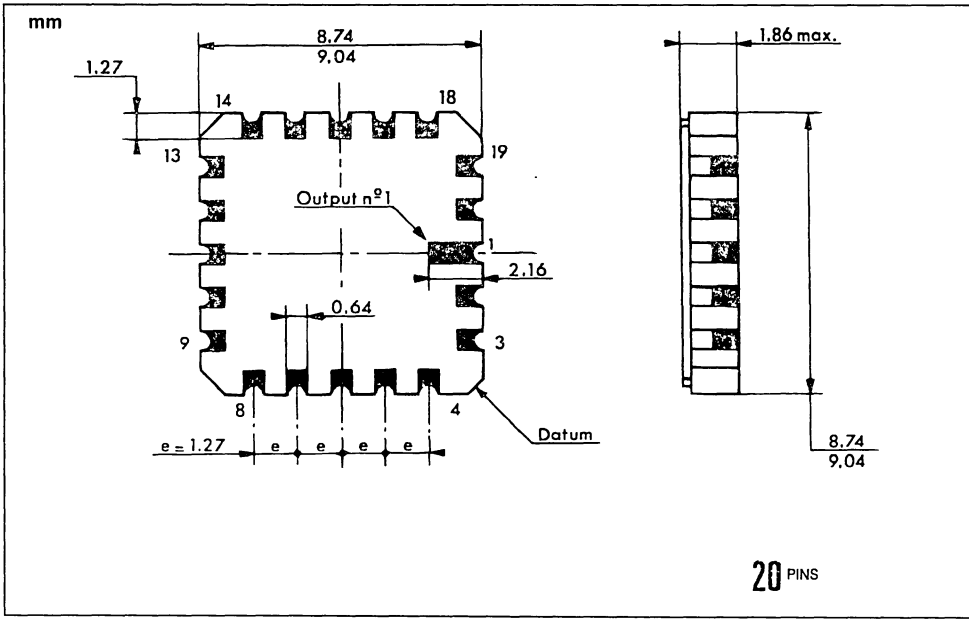


14 PINS - PLASTIC MICROPACKAGE (SO)



PACKAGE MECHANICAL DATA (continued)

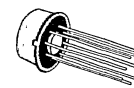
20 PINS - TRICECOP (LCC)



LM158,A-LM258,A LM358,A-LM2904-NE532

LOW POWER DUAL OPERATIONAL AMPLIFIERS

- INTERNALLY FREQUENCY COMPENSATED.
- LARGE DC VOLTAGE GAIN : 100 dB
- WIDE BANDWIDTH (unity gain) : 1.1 MHz (temperature compensated)
- VERY LOW SUPPLY CURRENT/AMPLI (500 µA) - ESSENTIALLY INDEPENDENT OF SUPPLY VOLTAGE
- LOW INPUT BIAS CURRENT : 20 nA (temperature compensated)
- LOW INPUT OFFSET VOLTAGE : 2 mV
- LOW INPUT OFFSET CURRENT : 2 nA
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND
- DIFFERENTIAL INPUT VOLTAGE RANGE EQUAL TO THE POWER SUPPLY VOLTAGE
- LARGE OUTPUT VOLTAGE SWING 0 V TO (V_{CC} – 1.5 V)



H
TO99
(Metal Can)

D
SO8
(Plastic Micropackage)

N
DIP8
(Plastic Package)
J
CERDIP8
(Cerdip Package)

GC
LCC20
(Tricecop (LCC))

DESCRIPTION

These circuits consist of two independent, high gain, internally frequency compensated which were designed specifically to operate from a single power supply over a wide range of voltages. The low power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op-amp circuits which now can be more easily implemented in single power supply systems. For example, these circuits can be directly operated off the standard + 5 V power supply voltage which is used in logic systems and will easily provide the required interface electronics without requiring any additional power supply.

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even through operated from only a single power supply voltage.

The gain-bandwidth product is temperature compensated.

The input bias current is temperature compensated.

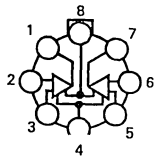
ORDER CODES

Part Number	Temperature Range	Package				
		H	N	J	GC	D
LM158, A	– 55 °C to + 125 °C	•	•	•	•	•
LM258, A	– 40 °C to + 105 °C	•	•	•		•
LM358, A	0 °C to + 70 °C	•	•	•		•
NE532	0 °C to + 70 °C		•	•		•
LM2904	– 40 °C to + 105 °C		•	•		•

Note : Hi-Rel Versions Available
Examples : LM158H, LM258N, LM2904D.

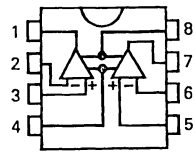
PIN CONNECTIONS (top views)

TO99



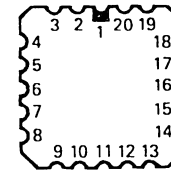
1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - Ground

DIP8
CERDIP8
SO8



5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}

LCC20



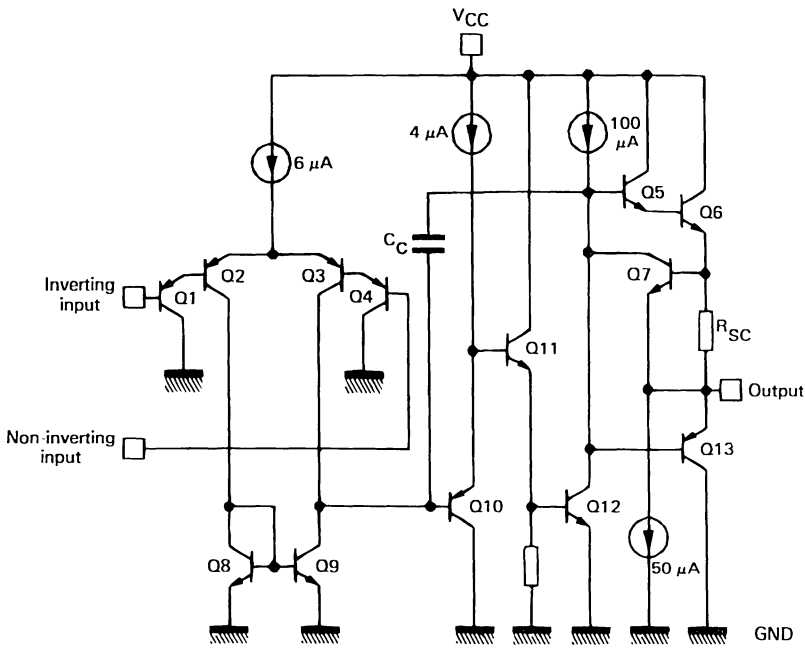
1 - NC
2 - Output 1
3 - NC
4 - NC
5 - Inverting input 1
6 - NC
7 - Non-inverting input 1
8 - NC
9 - NC
10 - Ground
11 - NC
12 - Non-inverting input 2
13 - NC
14 - NC
15 - Inverting input 2
16 - NC
17 - Output 2
18 - NC
19 - NC
20 - V_{CC}

E88LM158-01

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM158, A	LM258, A LM2904	LM358, A NE532	Unit
V_{CC}	Supply Voltage	+ 32	+ 32	+ 32	V
V_I	Input Voltage	– 0.3 to + 32	– 0.3 to + 32	– 0.3 to + 32	V
V_{ID}	Differential Input Voltage	+ 32	+ 32	+ 32	V
	Output Short-circuit Duration (note 2)	Indefinite	Indefinite	Indefinite	
P_{tot}	Power Dissipation LM158GC	500 665	500	500	mW
I_{ID}	Input Current (note 1)	50	50	50	mA
T_{oper}	Operating Free-air Temperature Range	– 55 to + 125	– 40 to + 105	0 to + 70	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	– 65 to + 150	– 65 to + 150	°C

SCHEMATIC DIAGRAM (1/2 LM158)



– Single Supply 3 V to 30 V
– Dual supplies ± 1.5 V to ± 15 V

E88LM158-02

CASE	Inverting Inputs	Non-inverting Inputs	GND	V_{CC}	Outputs	N.C.
TO99 - DIP8 - CERDIP8 - SO8	2-6	3-5	4	8	1-7	
LCC20	5-15	7-12	10	20	2-17	*

* **LCC20 :** Other pins are not connected.

ELECTRICAL CHARACTERISTICS

V_{CC}^{+} = + 5 V, V_{CC}^{-} = Ground, V_O = 1.4 V
(unless otherwise specified)

LM358,A/NE532 : $0 \leq T_{amb} \leq +70$ °C
LM258,A/LM2904 : $-40 \leq T_{amb} \leq +105$ °C
LM158,A : $-55 \leq T_{amb} \leq +125$ °C

Symbol	Parameter	LM158A, LM258A LM358A			LM158, LM258 LM358, LM2904 NE532			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage (note 3) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		1	2 4		2	5 7	mV
I_{IO}	Input Offset Current T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		2	10 30		2	20 40	nA
I_{IB}	Input Bias Current (note 4) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		20	50 100		20	100 200	nA
A_{VD}	Large Signal Voltage Gain (V_{CC} = + 15 V, $R_L \geq 2$ kΩ) (V_O = 1.4 V to 11.4 V) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 50 25	 100		 50 25	 100		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S \leq 10$ KΩ) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 65 65	 100		 65 65	 100		dB
I_{CC}	Supply Current, all Amp, no Load T_{amb} = 25 °C, V_{CC} = + 5 V T_{amb} = 25 °C, V_{CC} = + 30 V $T_{min} \leq T_{amb} \leq T_{max}$		0.7 1	1.2 2 2		0.7 1	1.2 2 2	mA
V_I	Input Voltage Range (note 6) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	0 0		V_{CC}^{+} − 1.5 V_{CC}^{+} − 2	0 0		V_{CC}^{+} − 1.5 V_{CC}^{+} − 2	V
CMR	Common-mode Rejection Ratio (R_S < 10 kΩ) (note 3) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 70 60	 85		 70 60	 85		dB
I_O	Output Short-circuit Current (V_I^+ = + 1 V, V_I = 0 V) T_{amb} = 25 °C, V_{CC} = + 15 V (note 2) $T_{min} \leq T_{amb} \leq T_{max}$	 20 10	 40	 60	 20 10	 40	 60	mA
I_{sink}	Output Current Sink (V_I^+ = - 1 V, V_I = 0 V) V_{CC} = + 15 V, T_{amb} = + 25 °C $T_{min} \leq T_{amb} \leq T_{max}$ V_O = + 0.2 V, T_{amb} = + 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 10 10 12 12	 20 50	 	 10 10 12 12	 20 50	 	 mA µA

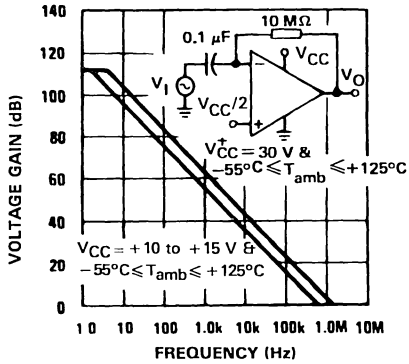
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter		LM158A, LM258A LM358A			LM158, LM258 LM358, LM2904 NE532			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OPP}	Output Voltage Swing								V
	T_{amb} = 25 °C	$R_L \geq 2$ kΩ	0		$V_{CC}^+ - 1.5$	0		$V_{CC}^+ - 1.5$	
	$T_{min} \leq T_{amb} \leq T_{max}$	$R_L \geq 10$ kΩ	0		$V_{CC}^+ - 2$	0		$V_{CC}^+ - 2$	
V_{OH}	High Level Output Voltage								V
	(V_{CC}^+ = 30 V)								
	T_{amb} = 25 °C	R_L = 2 kΩ	26	27		26	27		
	$T_{min} \leq T_{amb} \leq T_{max}$		26			26			
	T_{amb} = 25 °C	R_L = 10 kΩ	27	28		27	28		
	$T_{min} \leq T_{amb} \leq T_{max}$		27			27			
V_{OL}	Low Level Output Voltage								mV
	($R_L \geq 10$ kΩ)								
	T_{amb} = 25 °C			5	20		5	20	
	$T_{min} \leq T_{amb} \leq T_{max}$				20			20	
S_{VO}	Slew-rate (V_I = 0.5 to 3 V, R_L = 2 kΩ								V/µs
	$C_L \leq 100$ pF, T_{amb} = 25 °C, unity gain)								
	V_{CC} = 15 V		0.3	0.6		0.3	0.6		
GBP	Gain Bandwidth Product								MHz
	(f = 100 kHz, T_{amb} = 25 °C, V_{CC} = 30 V								
	V_{IN} = 10 mV, R_L = 2 kΩ, C_L = 100 pF)		0.7	1.1	1.6	0.7	1.1	1.6	
THD	Total Harmonic Distortion								%
	(f = 1 kHz, A_V = 20 dB, R_L = 2 kΩ, V_{CC} = 30 V								
	$C_L \leq 100$ pF, T_{amb} = 25 °C, V_O = 2 V_{PP})			0.02			0.02		
V_n	Equivalent Input Noise voltage								nV/√Hz
	(f = 1 kHz, R_g = 100 Ω, V_{CC} = 30 V)			55			55		
DV_{io}	Input Offset Voltage Drift								µV/°C
	$T_{min} \leq T_{amb} \leq T_{max}$			7	30		7	30	
DI_{io}	Input Offset Current Drift								pA/°C
	$T_{min} \leq T_{amb} \leq$ 25 °C			10	300		10	300	
V_{O1}/V_{O2}	Channel Separation (note 5)								dB
	1 kHz ≤ f ≤ 20 kHz			120			120		

Notes : 1. This input only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diode clamps.
In addition to this diode action, there is also NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the Op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative.
This is not destructive and normal output will set up again for input voltage higher than – 0.3V.

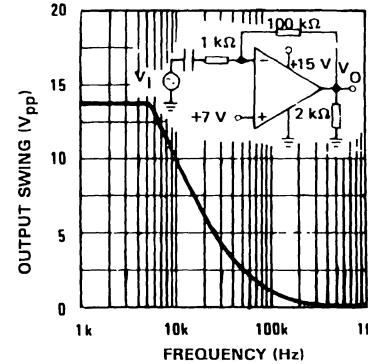
2. Short-circuits from the output to V_{CC} can cause excessive heating if V_{CC} > 15V. The maximum output current is approximatively 40mA independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.
3. V_O = 1.4V, R_S = 0, 5V < V_{CC} < 30V, 0 < V_I < V_{CC} – 1.5V.
4. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
5. Due to the proximity of external components insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequences.
6. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0 3V. The upper end of the common-mode voltage range is V_{CC} – 1.5V.
But either or both inputs can go to + 32V without damage.

OPEN LOOP FREQUENCY RESPONSE (Note 3)



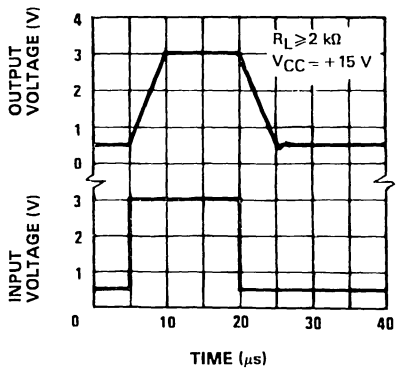
E88LM158-03

LARGE SIGNAL FREQUENCY RESPONSE



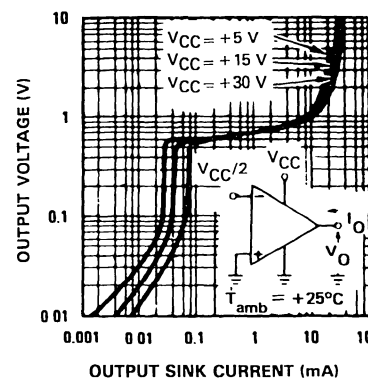
E88LM158-04

VOLTAGE FOLLOWER PULSE RESPONSE



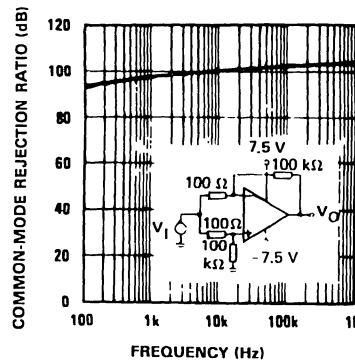
E88LM158-05

OUTPUT CHARACTERISTICS



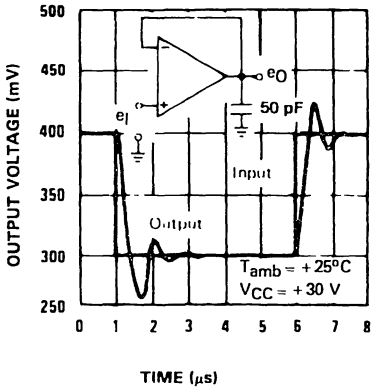
E88LM158-06

COMMON-MODE REJECTION RATIO



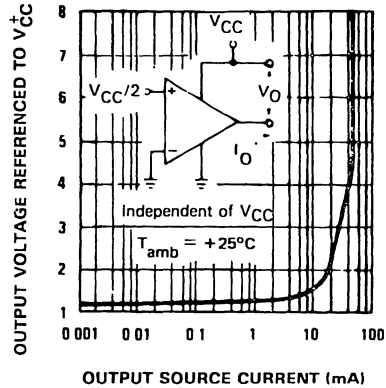
E88LM158-07

VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)



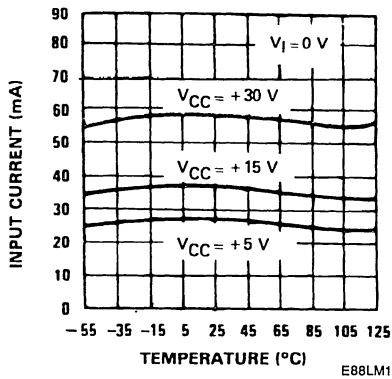
E88LM158-08

OUTPUT CHARACTERISTICS



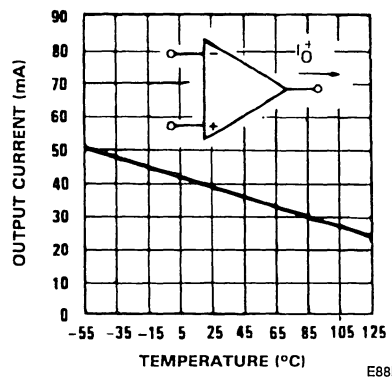
E88LM158-09

INPUT CURRENT (Note 1)



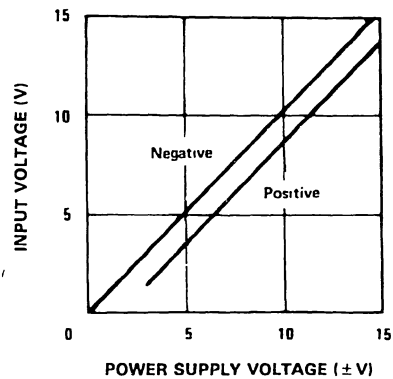
E88LM158-10

CURRENT LIMITING (Note 1)



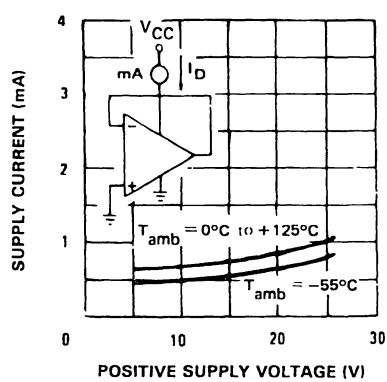
E88LM158-11

INPUT VOLTAGE RANGE



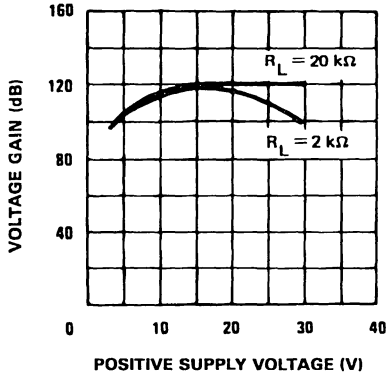
E88LM158-12

SUPPLY CURRENT



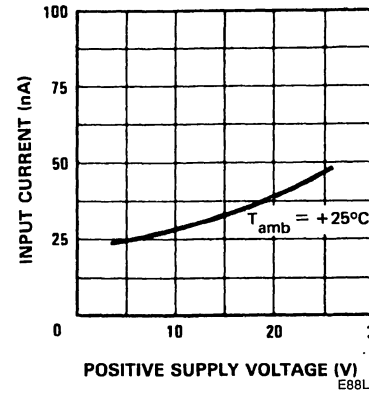
E88LM158-13

VOLTAGE GAIN



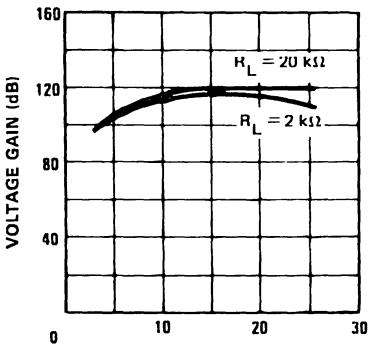
E88LM158-14

INPUT CURRENT



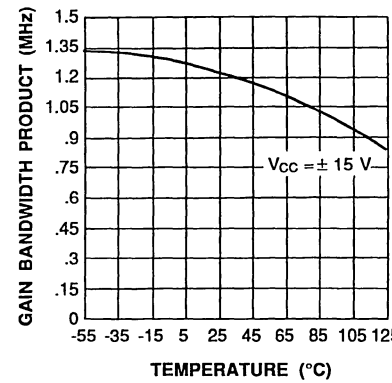
E88LM158-15

VOLTAGE GAIN



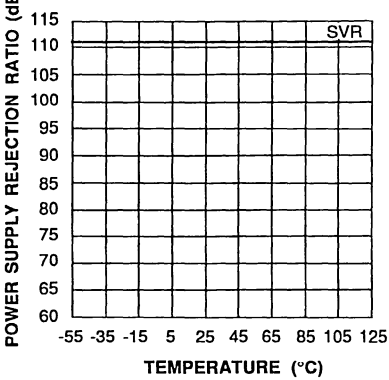
E88LM158-16

GAIN BANDWIDTH PRODUCT



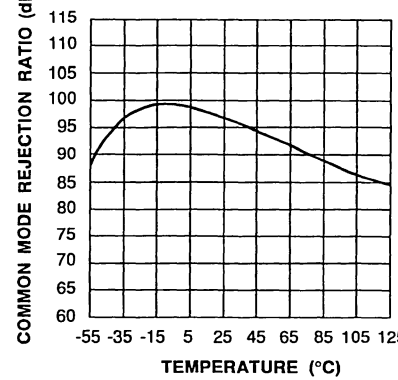
E88LM158-17

POWER SUPPLY REJECTION RATIO



E88LM158-18

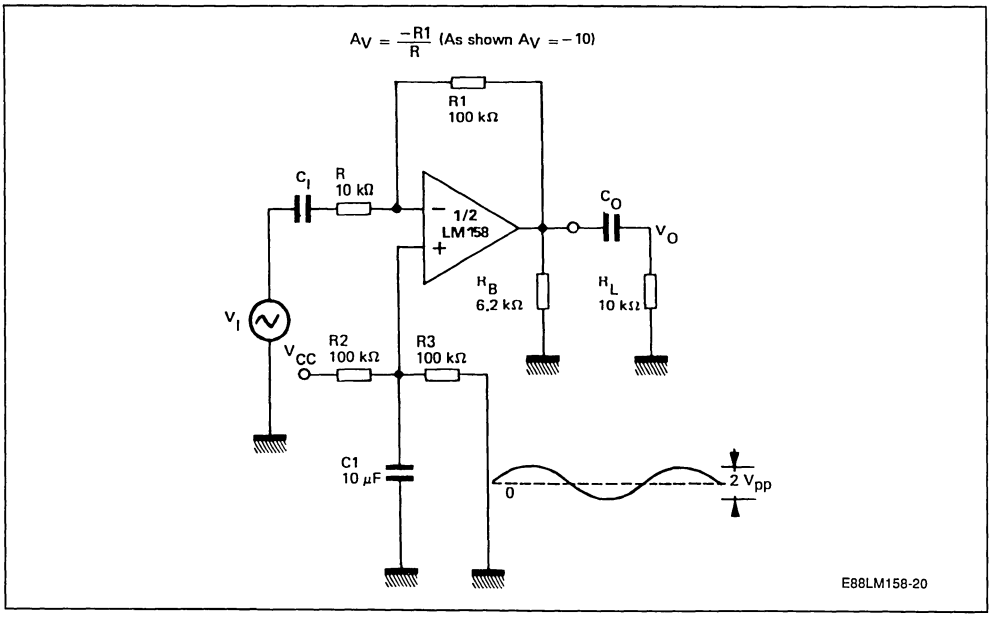
COMMON MODE REJECTION RATIO



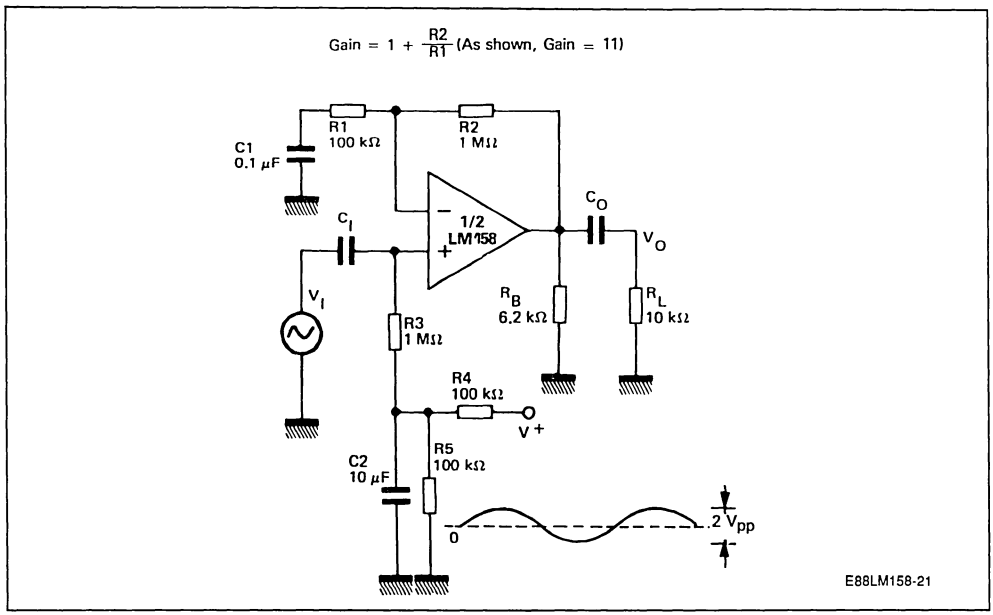
E88LM158-19

TYPICAL APPLICATIONS (single supply voltage) V_{CC} = + 5 V_{DC}

AC COUPLED INVERTING AMPLIFIER

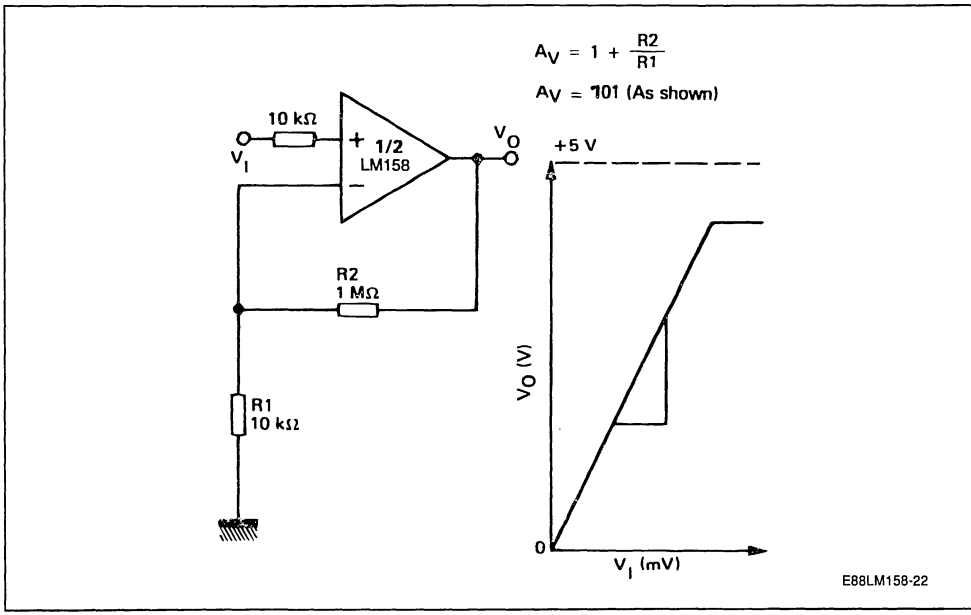


AC COUPLED NON INVERTING AMPLIFIER

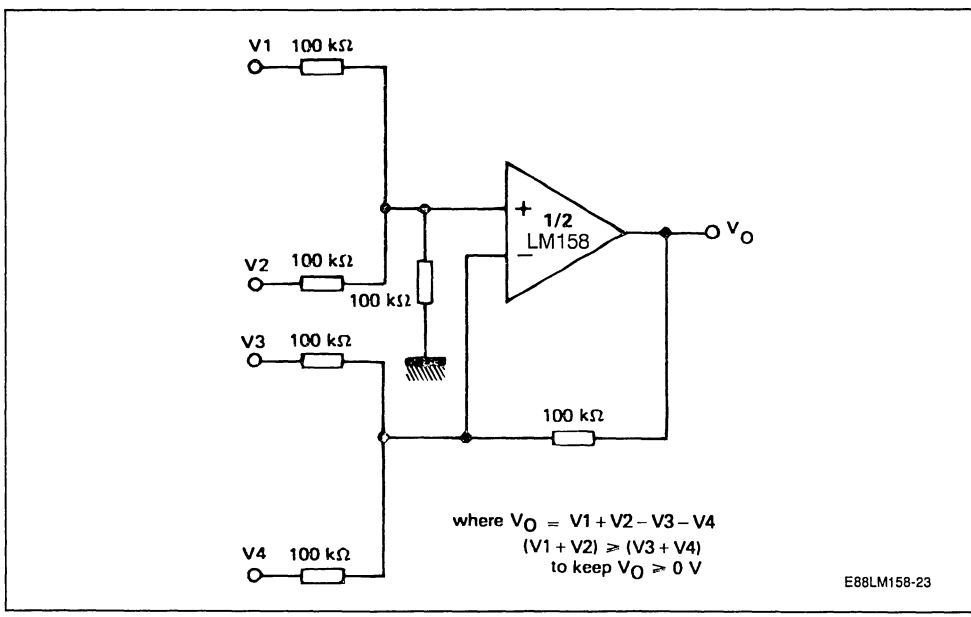


TYPICAL APPLICATIONS (single supply voltage) V_{CC} = + 5 V_{DC} (continued)

NON INVERTING DC AMPLIFIER

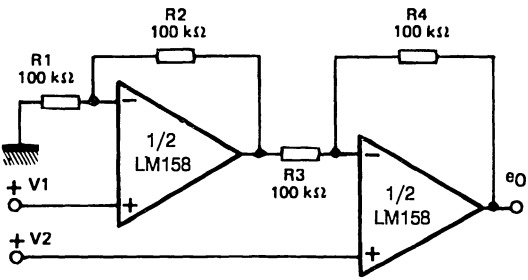


DC SUMMING AMPLIFIER



TYPICAL APPLICATIONS (single supply voltage) V_{CC} = + 5 V_{DC} (continued)

HIGH INPUT IMPEDANCE, DC DIFFERENTIAL AMPLIFIER



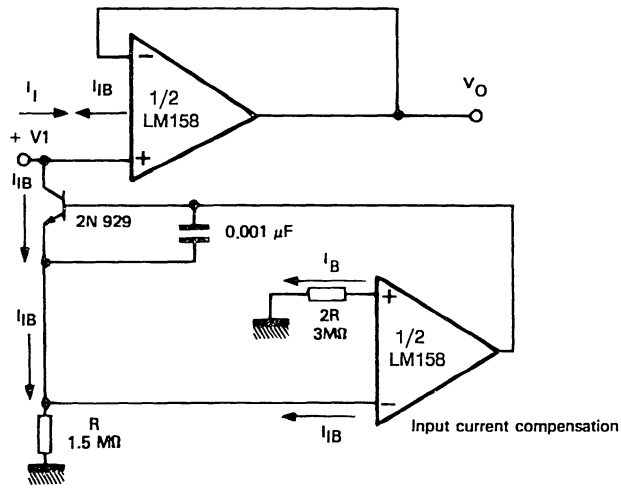
for $\frac{R1}{R2}=\frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$V_O=(1+\frac{R4}{R3})(V2-V1)$

As shown : $V_O=2(V2-V1)$

E88LM158-24

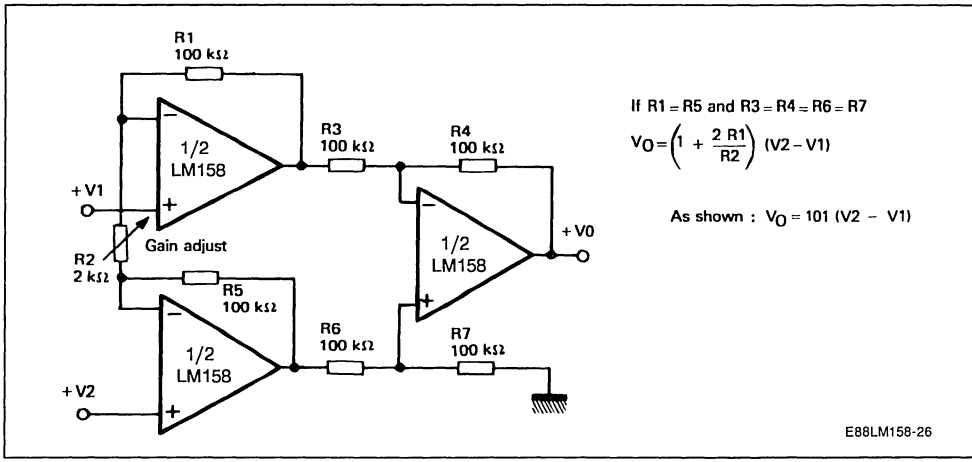
USING SYMMETRICAL AMPLIFIERS TO REDUCE INPUT CURRENT (general concept)



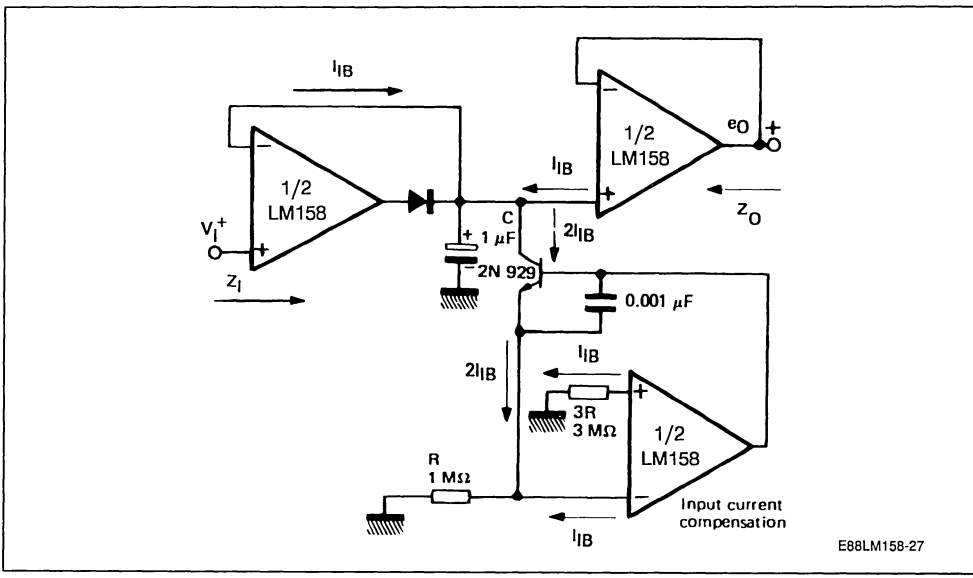
E88LM158-25

TYPICAL APPLICATIONS (single supply voltage) V_{CC} = + 5 V_{DC} (continued)

HIGH INPUT Z ADJUSTABLE-GAIN DC INSTRUMENTATION AMPLIFIER

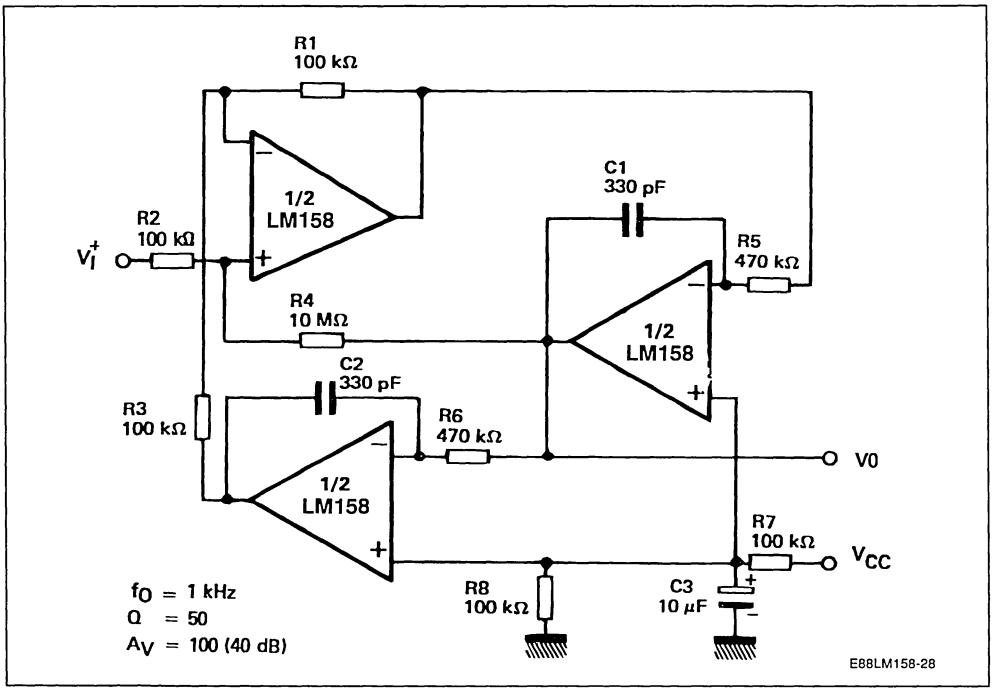


LOW DRIFT PEAK DETECTOR



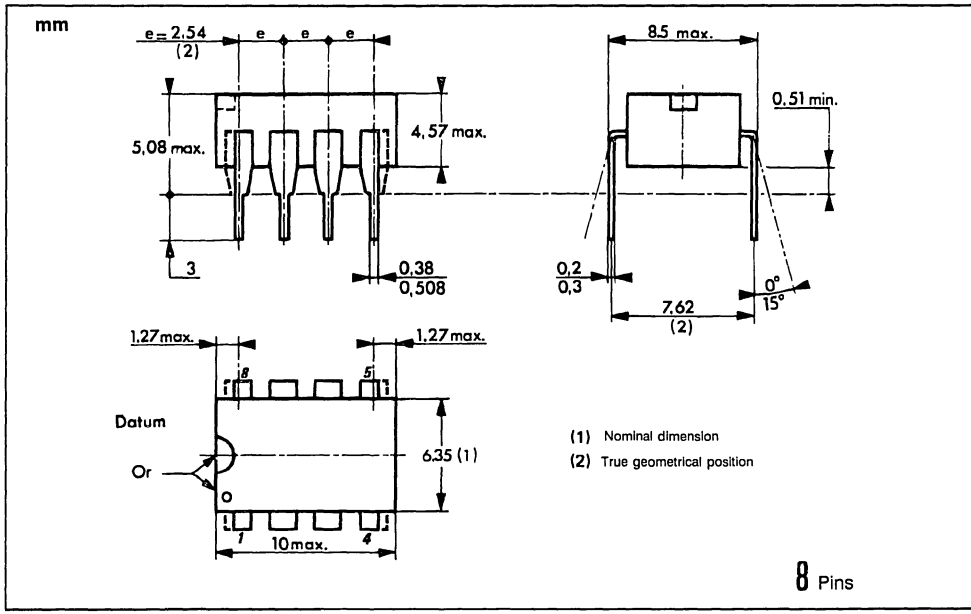
TYPICAL APPLICATIONS (single supply voltage) V_{CC} = + 5 V_{DC} (continued)

ACTIVE BAND-PASS FILTER

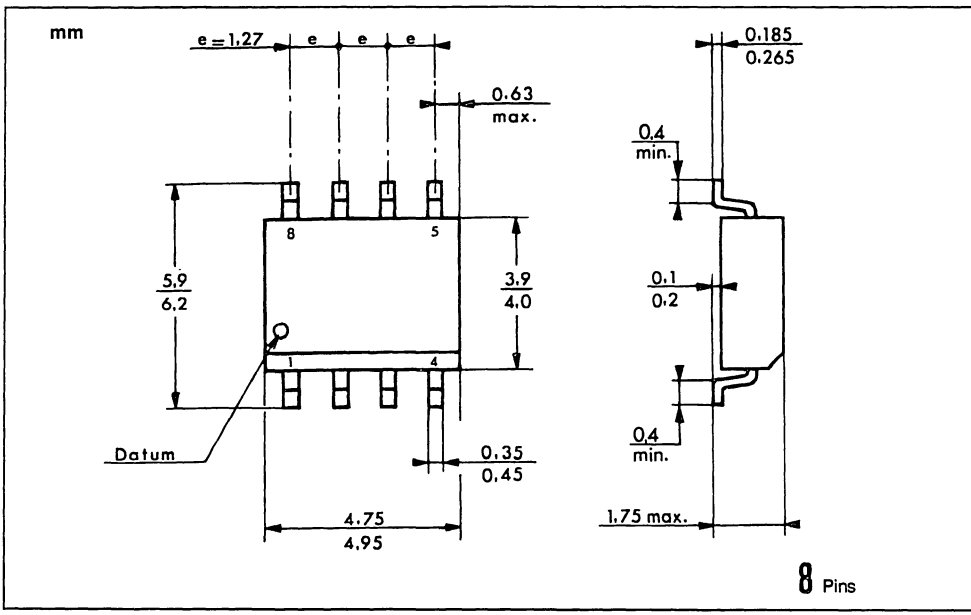


PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP OR CERDIP

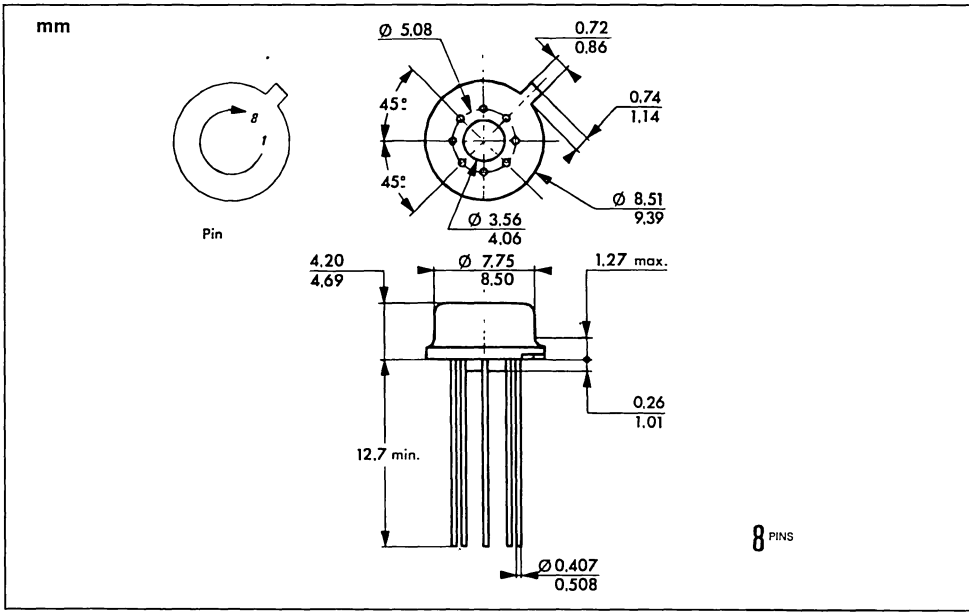


8 PINS – PLASTIC MICROPACKAGE (SO)

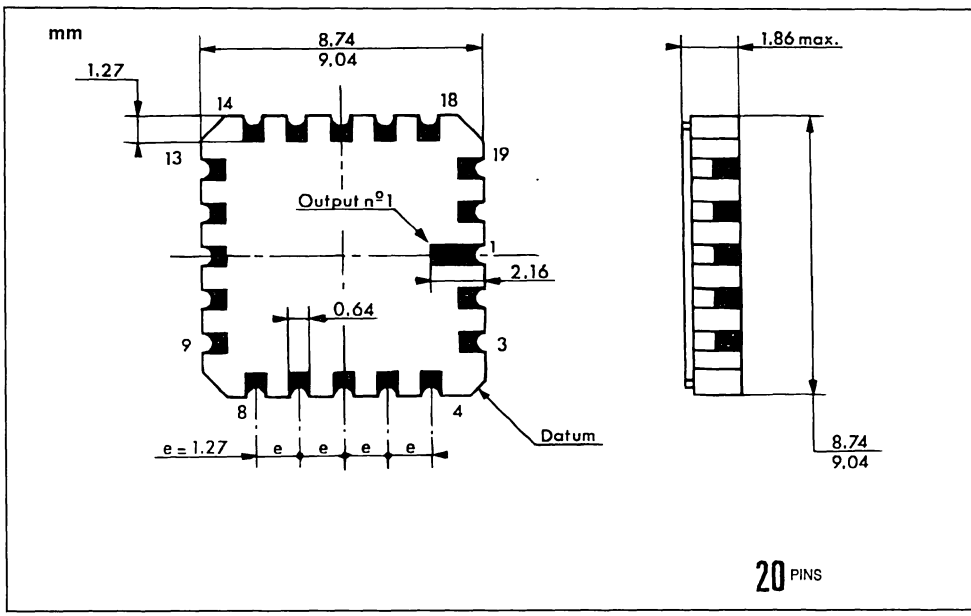


PACKAGE MECHANICAL DATA (continued)

8 PINS – METAL CAN - TO99



20 PINS – TRICECOP (LCC)

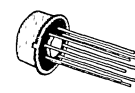


SGS-THOMSON MICROELECTRONICS

LM193,A-LM293,A LM393,A-LM2903

LOW POWER LOW OFFSET VOLTAGE DUAL COMPARATORS

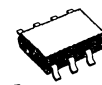
- WIDE SINGLE SUPPLY VOLTAGE RANGE OR DUAL SUPPLIES + 2 V TO + 36 V OR ± 1 V TO ± 18 V
- VERY LOW SUPPLY CURRENT DRAIN (0.4 mA) INDEPENDENT OF SUPPLY VOLTAGE (1 mW/comparator at + 5 V)
- LOW INPUT BIAS CURRENT : 25 nA TYP
- LOW INPUT OFFSET CURRENT : ± 5 nA TYP
- LOW INPUT OFFSET VOLTAGE : ± 1 mV TYP
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND
- LOW OUTPUT SATURATION VOLTAGE : 250 mV TYP. (I_O = 4 mA)
- DIFFERENTIAL INPUT VOLTAGE RANGE TO THE SUPPLY VOLTAGE
- TTL, DTL, ECL, MOS, CMOS COMPATIBLE OUTPUTS



H
TO99
(Metal Can)

N
DIP8
(Plastic Package)

J
CERDIP8
(Cerdip Package)



D
SO8
(Plastic Micropackage)

GC
LCC20
Tricecop (LCC)

DESCRIPTION

These devices consist of two independent precision voltage comparators with an offset voltage specifications as low as 2 mV max for LM393A, LM293A and LM193A.

All these comparators were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible.

These comparators also have a unique characteristics in that the input common-mode voltage range includes ground even through operated from a single power supply voltage.

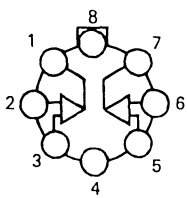
ORDER CODES

Part Number	Temperature Range	Package				
		H	N	D	GC	J
LM193,A	– 55 to + 125 °C	•	•	•	•	•
LM293,A	– 40 to + 105 °C	•	•	•		•
LM393,A	0 to + 70 °C	•	•	•		•
LM2903	– 40 to + 105 °C		•	•		•

Note : Hi-Rel Versions Available
Examples : LM193H, LM393D

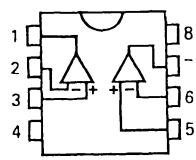
PIN CONNECTIONS (top views)

TO99



1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-

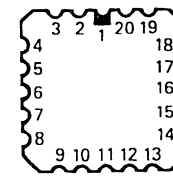
DIP8
CERDIP8
SO8



5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

1 - NC
2 - Output 1
3 - NC
4 - NC
5 - Inverting input 1
6 - NC
7 - Non-inverting input 1
8 - NC
9 - NC
10 - V_{CC}^-

LCC20



11 - NC
12 - Non inverting input 2
13 - NC
14 - NC
15 - Inverting input 2
16 - NC
17 - Output 2
18 - NC
19 - NC
20 - V_{CC}^+

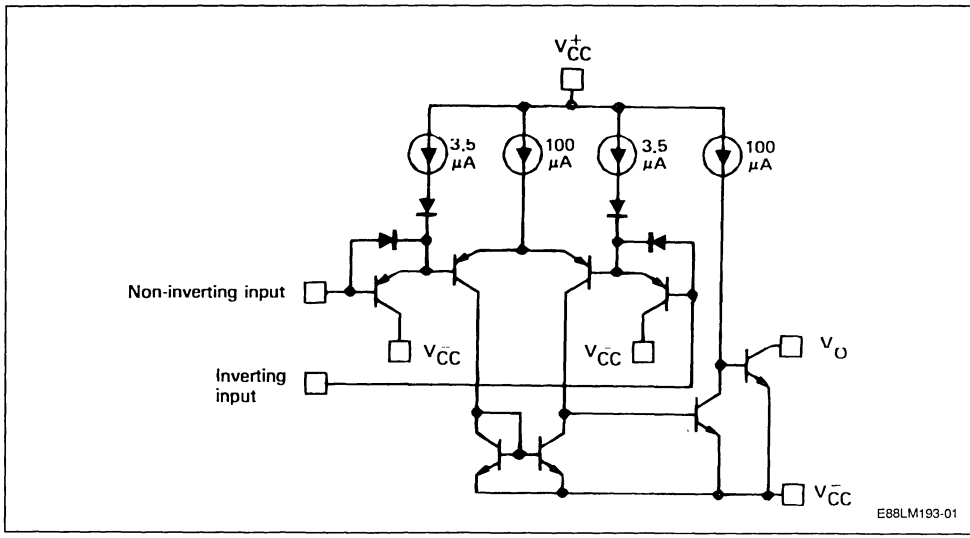
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM193, A	LM293, A	LM393, A LM2903	Unit
V_{CC}	Supply Voltage	± 18 to 36	± 18 to 36	± 18 to 36	V
V_{ID}	Differential Input Voltage	36	36	36	V
V_I	Input Voltage	– 0.3 to + 36	– 0.3 to + 36	– 0.3 to + 36	V
	Output Short-circuit to Ground – (note 2)	Continuous	Continuous	Continuous	
P_{tot}	Power Dissipation – (note 1) LM393AH	830	830	570 830	mW
T_{oper}	Operating Free-air Temperature Range LM2903	– 55 to + 125	– 25 to + 85	0 to + 70 – 40 to + 105	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	– 65 to + 150	– 65 to + 150	°C

Notes : 1. For operating at high temperatures the LM393, LM393A, LM2903 must be derated based on a + 125 °C max junction temperature and a thermal resistance of 175 °C/W which applies for the devices soldered on a printed circuit board, operating in a still air ambient. The LM393, LM393A, LM293 and LM293A must be derated based on a + 150 °C max junction temperature.

2. Short-circuit from the output to V_{CC} can cause excessive heating and eventual destruction The maximum output current is approximately 20 mA, independent of the magnitude of V_{CC}.

SCHEMATIC DIAGRAM (1/2 LM193)



CASE	Outputs	Inverting Inputs	Non-inverting Inputs	V_{CC}^-	V_{CC}^+	N.C.
TO99 SO8 DIP8	1, 7	3, 5	2, 6	4	8	–
LCC20	2, 17	7, 12	5, 15	10	20	*

* LCC20 : Other pins are not connected.

ELECTRICAL CHARACTERISTICS

LM393A / LM393 : $0\,°C \le T_{amb} \le +\ 70\,°C$
LM293A / LM293 / LM2903 : $-40\,°C \le T_{amb} \le +\ 105\,°C$
LM193A / LM193 : $-55\,°C \le T_{amb} \le +\ 125\,°C$
* = $\ge V_{CC}^{+} = +\ 5$ V, V_{CC}^{-} = GND
(unless otherwise specified)

Symbol	Parameter	LM193A - LM293A LM393A			LM193 - LM293 LM393 - LM2903			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage – (note 3) T_{amb} = + 25 °C $T_{min} \le T_{amb} \le T_{max}$		1	2 4		1	5 9	mV
I_{IB}	Input Bias Current – (note 4) T_{amb} = + 25 °C $T_{min} \le T_{amb} \le T_{max}$		25	100 300		25	250 400	nA
I_{IO}	Input Offset Current T_{amb} = + 25 °C $T_{min} \le T_{amb} \le T_{max}$		3	25 100		5	50 150	nA
A_{VD}	Large Signal Voltage Gain (V_{CC}^{+} = + 15 V, V_a = + 10 V, $R_L \ge 15\ k\Omega$) T_{amb} = + 25 °C	50	200		25	200		V/mV
I_{CC}	Supply Current, no Load (all comparators) T_{amb} = 25 °C V_{CC}^{+} = 30 V		0.4 1	1 2.5		0.4 1	1 2.5	mA
V_I	Input Voltage Range – (note 5) T_{amb} = + 25 °C $T_{min} \le T_{amb} \le T_{max}$	0 0		V_{CC}^{+} – 1.5 V_{CC}^{+} – 2	0 0		V_{CC}^{+} – 1.5 V_{CC}^{+} – 2	V
V_{ID}	Differential Input Voltage (V_I^{+} = 0 V or if used V_I^{-} = 0 V) – (note 7)			V_{CC}^{+}			V_{CC}^{+}	V
I_{OS}	Output Sink Current V_I^{+} = 0 V, $V_I^{-} \ge 1$ V, $V_O \le +\ 1.5$ V T_{amb} = 25 °C	6	16		6	16		mA
V_{OL}	Low Level Output Voltage $V_I^{-} \ge = 1$ V, V_I^{+} = 0 V, $I_{OS} \le = 4$ mA T_{amb} = 25 °C $T_{min} \le T_{amb} \le T_{max}$		250	400 700		250	400 700	mV
I_{OH}	High Level Output Current $V_I^{+} \ge 1$ V, V_I^{-} = 0 V T_{amb} = 25 °C, V_O = + 5 V $T_{min} \le T_{amb} \le T_{max}$, V_O = + 30 V		0.1	 1000		0.1	 1000	nA

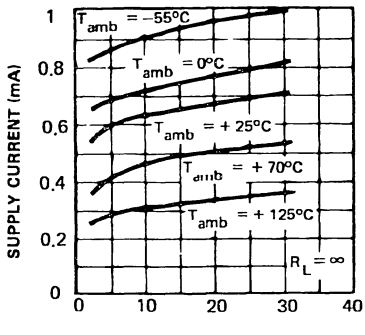
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	LM193A - LM293A LM393A			LM193 - LM293 LM393 - LM2903			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{re}	Response Time V_L = + 5 V, R_L = 5.1 kΩ – (note 6) T_{amb} = 25 °C		1.3			1.3		µs
t_{rel}	Large Signal Response Time e_i = TTL, V_{re} = + 1.4 V, V_L = + 5 V T_{amb} = 25 °C		300			300		ns

Notes : 3. At output switch point, $V_O \approx$ 1.4 V, R_S = 0 with V_{CC} from 5 V to 30 V the full input common-mode range (0 V to V_{CC} - 1.5 V).
4. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading charge exists on the reference or input lines.
5. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC} – 1.5 V, but either or both inputs can go to + 30 V without damage.
6. The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained.
7. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range the comparator will provide a proper output state. The low input voltage state must not be less than – 0.3 V (or 0.3 V below the negative power supply, if used).

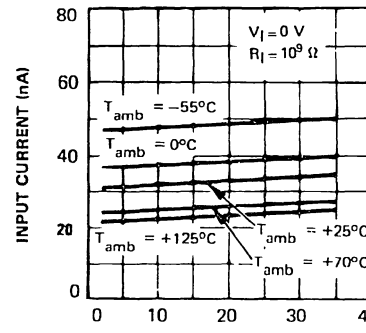
LM193,A - LM393,A

SUPPLY CURRENT



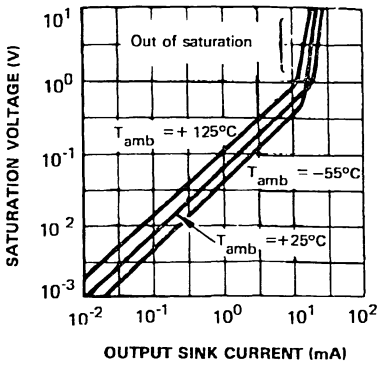
E88LM193-02

INPUT CURRENT



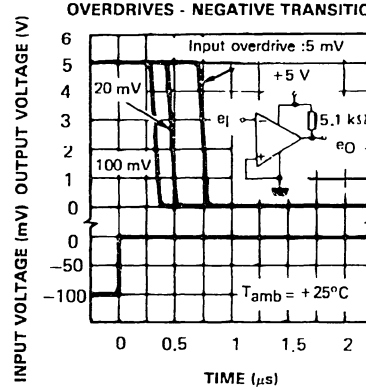
E88LM193-03

OUTPUT SATURATION VOLTAGE



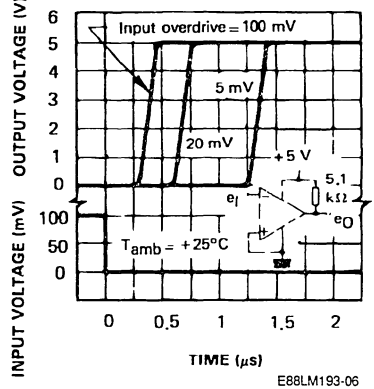
E88LM193-04

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES - NEGATIVE TRANSITION



E88LM193-05

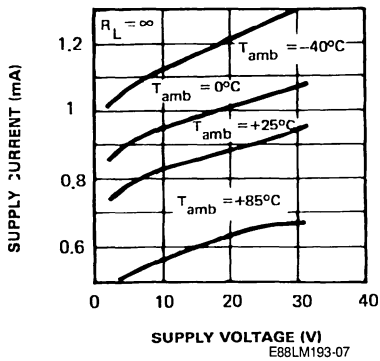
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES - POSITIVE TRANSITION



E88LM193-06

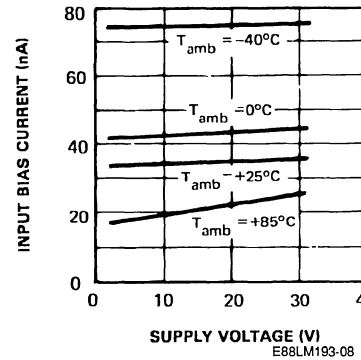
LM293,A - LM2903

SUPPLY CURRENT



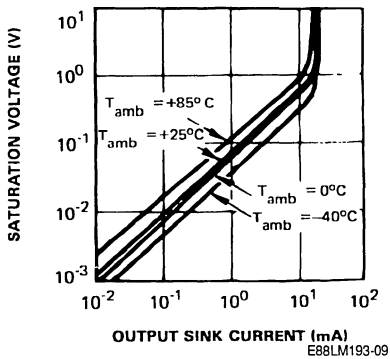
E88LM193-07

INPUT CURRENT



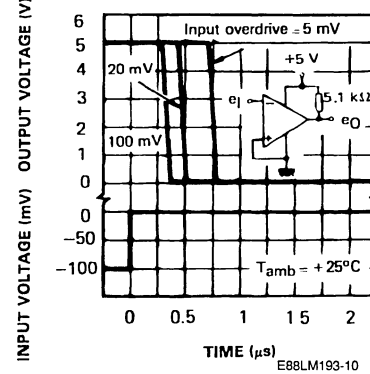
E88LM193-08

OUTPUT SATURATION VOLTAGE



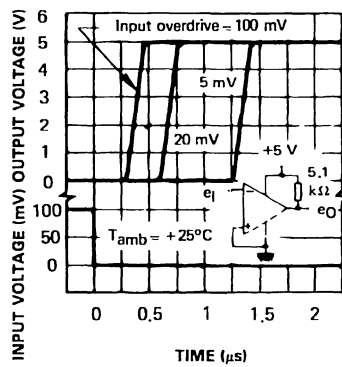
E88LM193-09

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES - NEGATIVE TRANSITION



E88LM193-10

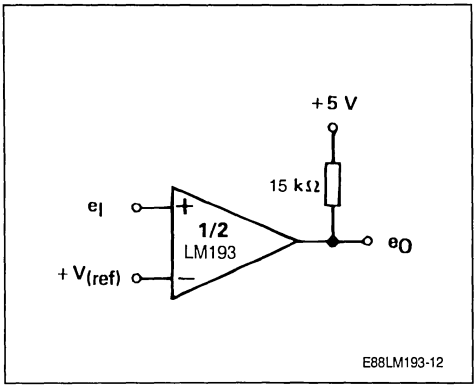
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES - POSITIVE TRANSITION



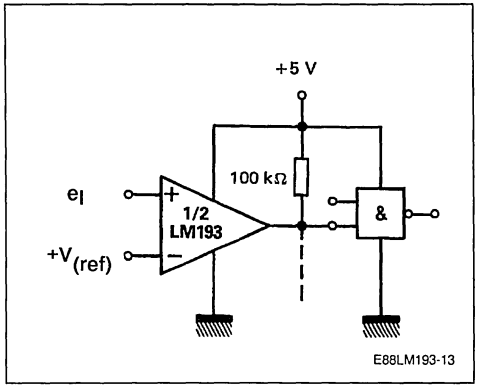
E88LM193-11

TYPICAL APPLICATIONS

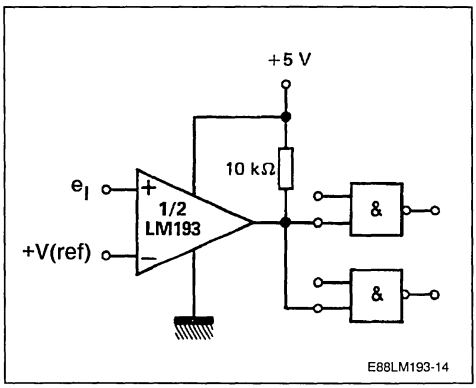
BASIC COMPARATOR



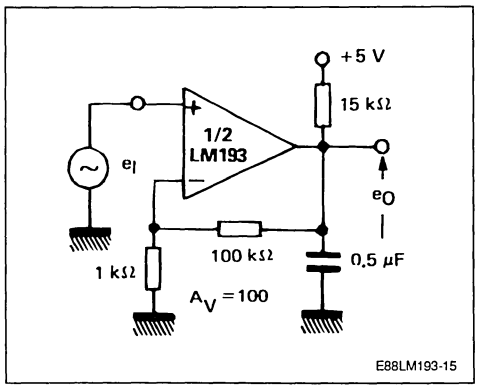
DRIVING CMOS



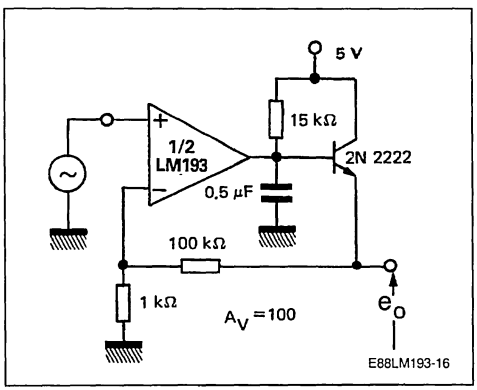
DRIVING TTL



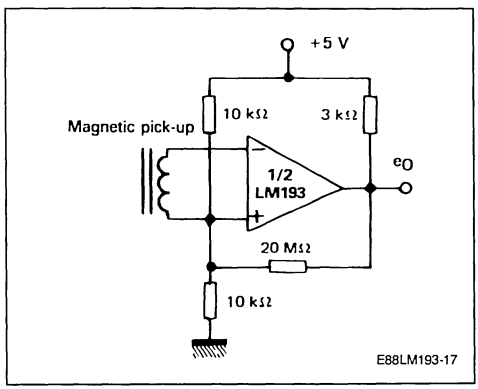
LOW FREQUENCY OP AMP



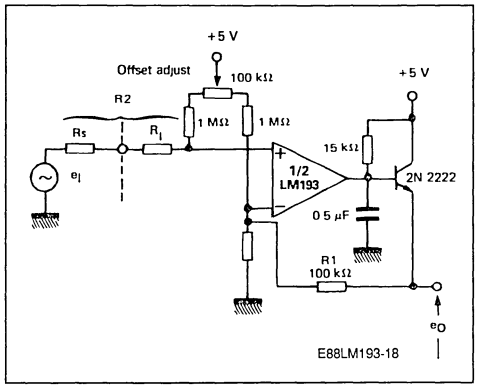
LOW FREQUENCY OP AMP



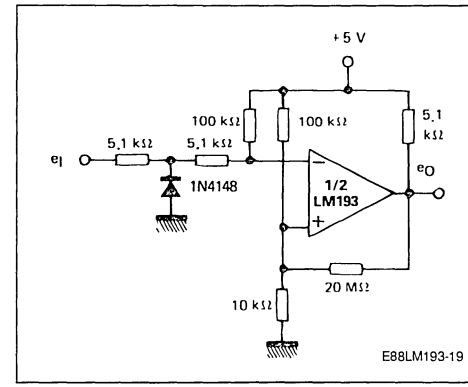
TRANSDUCER AMPLIFIER



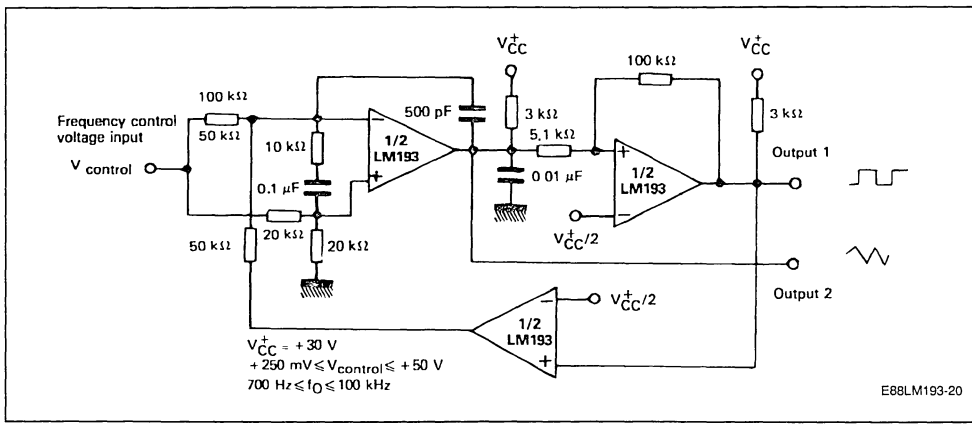
LOW FREQUENCY OP AMP WITH OFFSET ADJUST



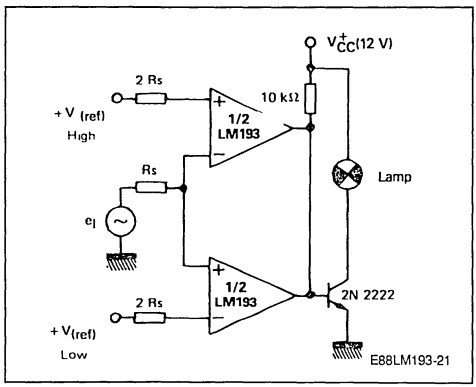
ZERO CROSSING DETECTOR (SINGLE POWER SUPPLY)



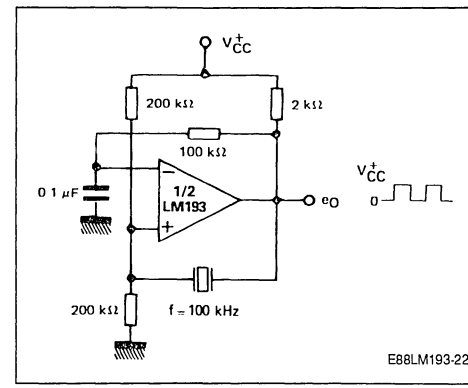
TWO DECADES HIGH FREQUENCY VCO



LIMIT COMPARATOR

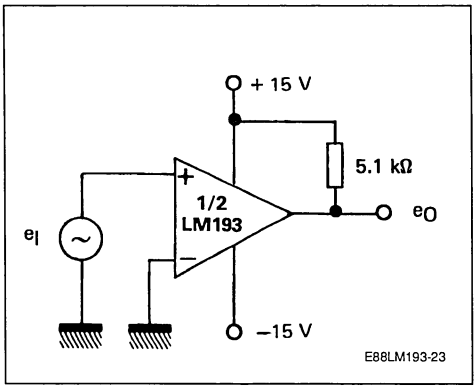


CRYSTAL CONTROLLED OSCILLATOR

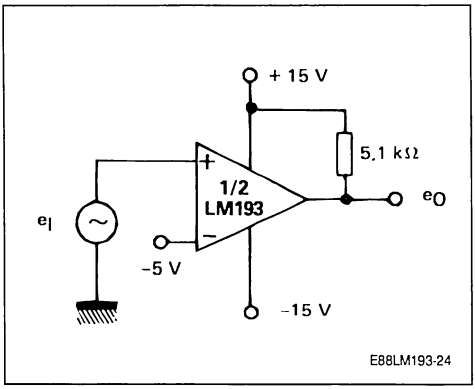


SPLIT-SUPPLY APPLICATIONS

ZERO CROSSING DETECTOR

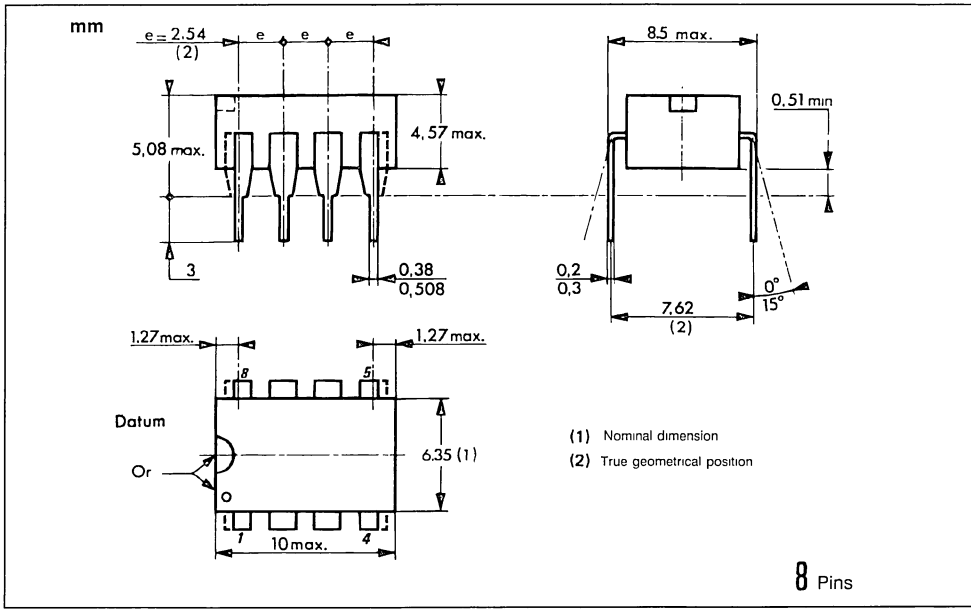


COMPARATOR WITH A NEGATIVE REFERENCE

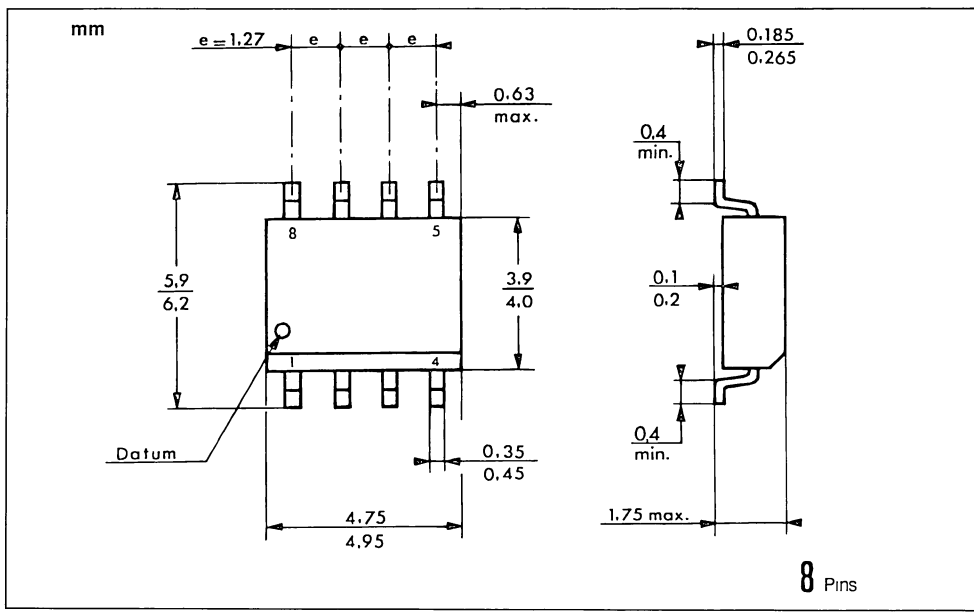


PACKAGE MECHANICAL DATA

8 PINS – PLASTIC DIP

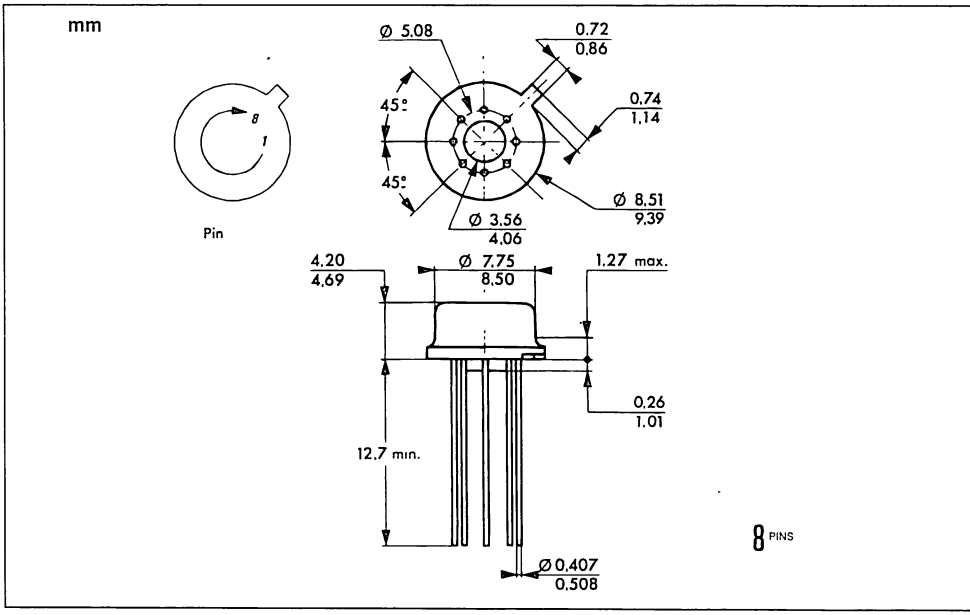


8 PINS – PLASTIC MICROPACKAGE (SO)

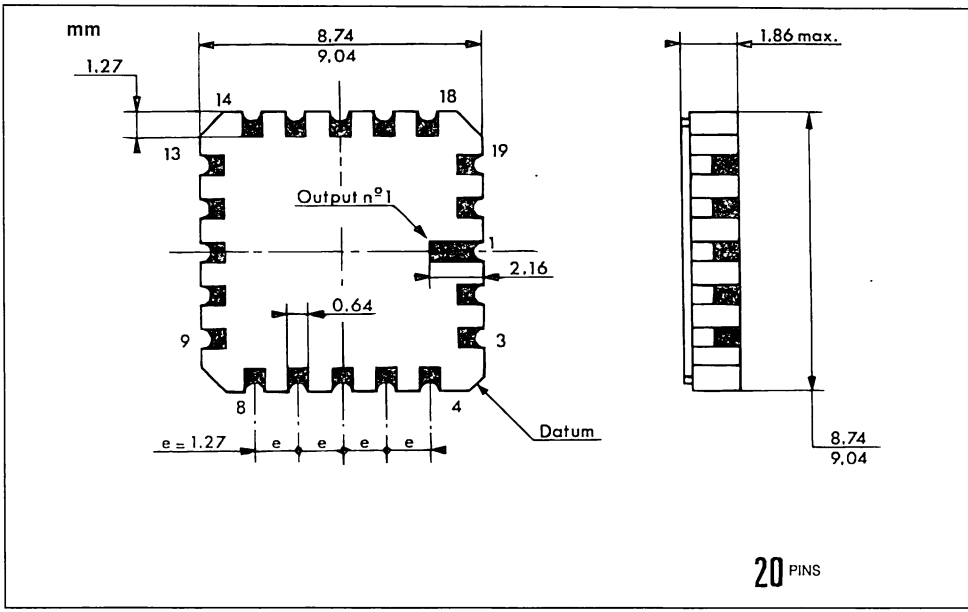


PACKAGE MECHANICAL DATA (continued)

8 PINS – METAL CAN TO99

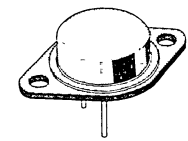


20 PINS – TRICECOP (LCC)



THREE-TERMINAL 5-VOLT REGULATORS

- FIXED VOLTAGE REGULATOR REQUIRES NO EXTERNAL COMPONENT FOR ADJUSTING
- CAN PROVIDE OTHER VALUES OF REGULATED VOLTAGES ABOVE 5V USING SEPARATE, BIAS RESISTORS
- SPECIFIED TO BE COMPATIBLE, WORST CASE, WITH TTL AND DTL



TO-3

DESCRIPTION

The LM209 and LM309 are 5V regulators. They are designed for local regulation on digital logic cards.

The available output current is greater than 1A.

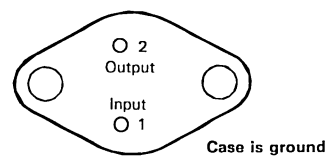
These regulators are essentially blow-out proof. Current limiting is included and thermal shut down is provided to keep the ICs from overheating. If internal dissipation becomes too great, the regulator will shut down to prevent excessive heating.

ORDER CODES

Part Number	Temperature Range
LM209	– 25°C to + 150°C
LM309	0°C to + 125°C

PIN CONNECTION (bottom view)

TO-3



Case is ground

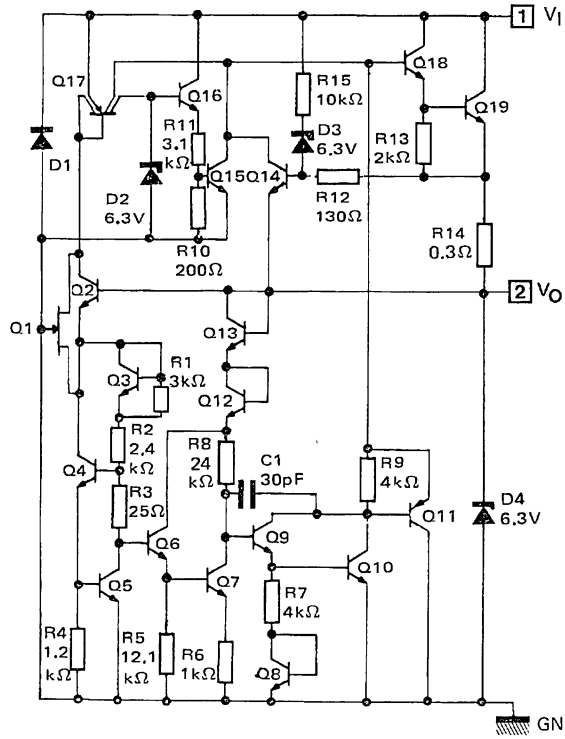
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_I	Input Voltage		35	V
P_D	Internal Power Dissipation		Internally Limited	W
I_{OS}	Short-circuit Output Current		Internally Limited	A
T_{oper}	Operating Free-air Temperature Range	LM209 LM309	– 25 to + 150 0 to + 125	°C
T_{stg}	Storage Temperature Range		– 65 to + 150	°C

THERMAL CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{th(j-c)}$	Junction-case Thermal Resistance			4	°C/W
$R_{th(j-a)}$	Junction-ambient Thermal Resistance		35		°C/W

SCHEMATIC DIAGRAM



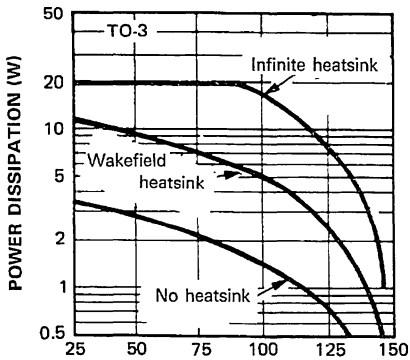
Case	V_I	V_O	GND
TO-3	1	2	Case

ELECTRICAL CHARACTERISTICS

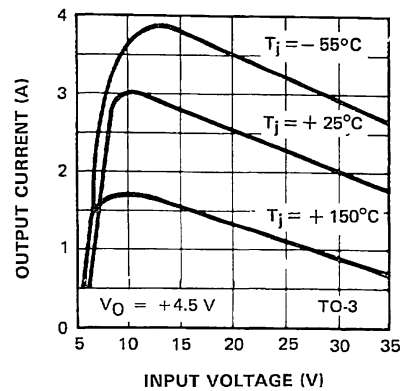
LM209 : $-25°C \leq T_j \leq +150°C$
LM309 : $0°C \leq T_j \leq +150°C$
$V_I = +10V$, $I_O = 0.5A$
(unless otherwise specified)

Symbol	Parameter	LM209			LM309			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_O	Output Voltage Range							V
	$T_j = +25°C$	4.7	5.05	5.3	4.8	5.05	5.2	
	$T_{min} \leq T_{amb} \leq T_{max}$							
	$+7V \leq V_I \leq +25V$, $5mA \leq I_O \leq 1A$, $P < 20W$	4.6		5.4	4.75		5.25	
K_{VI}	Line Regulation ($+7V \leq V_I \leq +25V$, $T_j = +25°C$)		4	50		4	50	mV
K_{VO}	Load Regulation ($T_j = +25°C$)							mV
	$5mA \leq I_O \leq 1.5A$		50	100		50	100	
I_{IB}	Quiescent Current ($+7V \leq V_I \leq +25V$)		5.2	10		5.2	10	mA
ΔI_{IB}	Quiescent Current Deviation							mA
	$+7V \leq V_I \leq +25V$			0.5			0.5	
	$5mA \leq I_O \leq 1A$ CB-19			0.8			0.8	
V_{NO}	Output Noise Voltage ($T_{amb} = +25°C$, $10Hz \leq f \leq 100kHz$)			40			40	µV
K_{VH}	Long Term Stability			10			20	mV

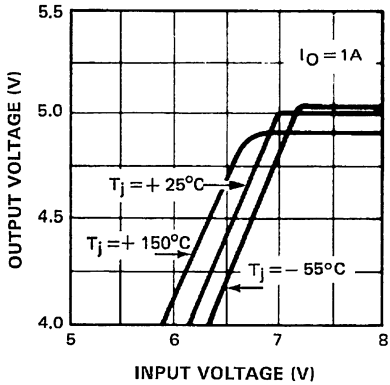
MAXIMUM AVERAGE POWER DISSIPATION



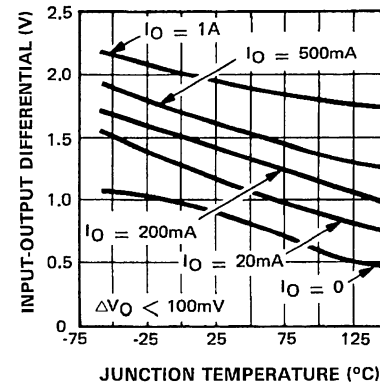
PEAK OUTPUT CURRENT



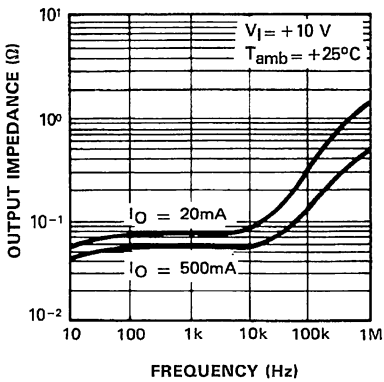
DROPOUT CHARACTERISTICS



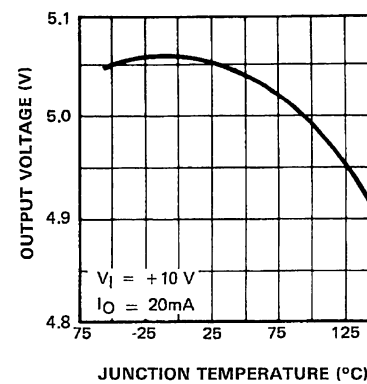
DROPOUT VOLTAGE



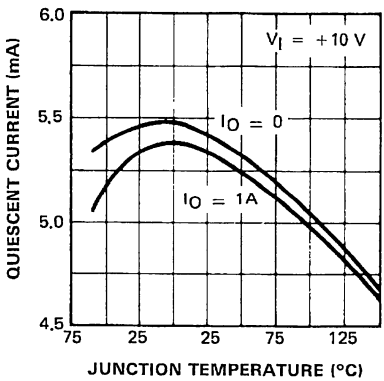
OUTPUT IMPEDANCE



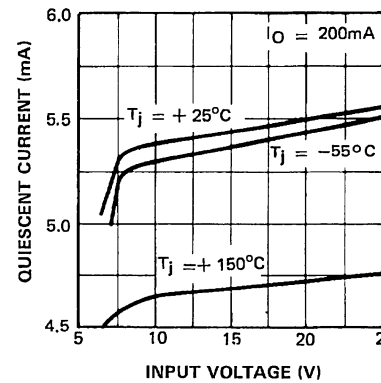
OUTPUT VOLTAGE



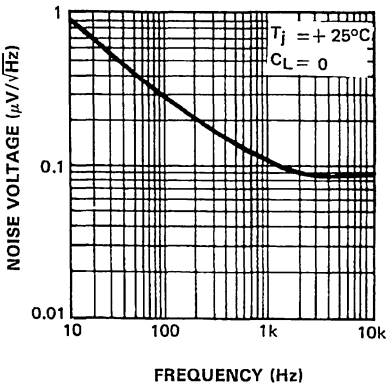
QUIESCENT CURRENT



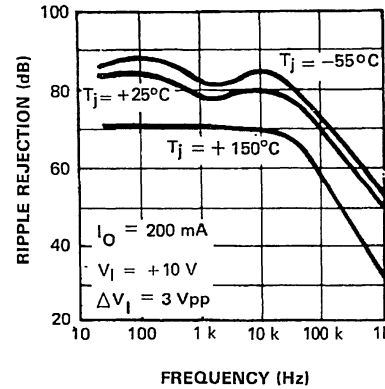
QUIESCENT CURRENT



OUTPUT NOISE VOLTAGE

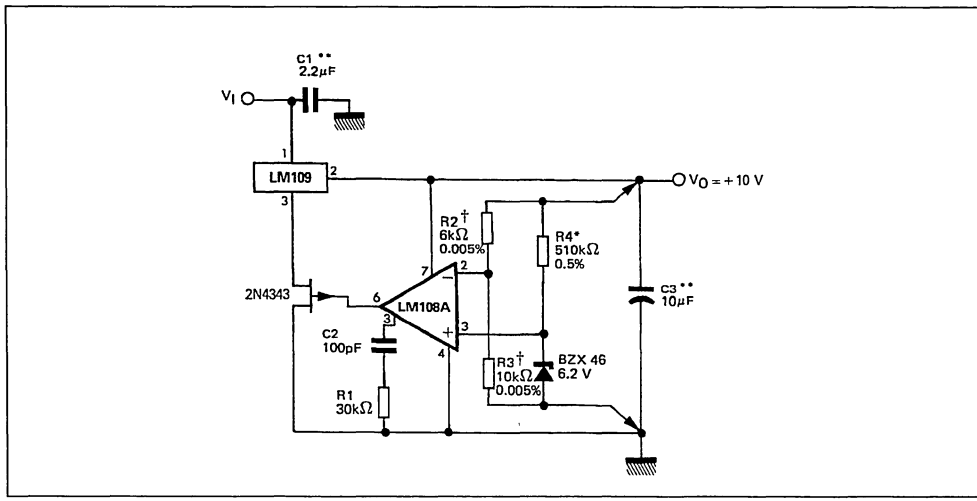


RIPPLE REJECTION



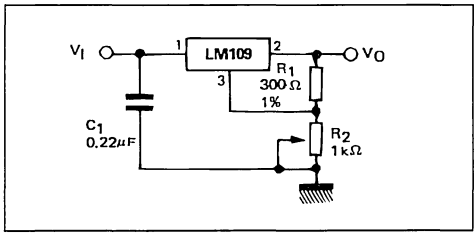
TYPICAL APPLICATION

✡ HIGH STABILITY REGULATOR

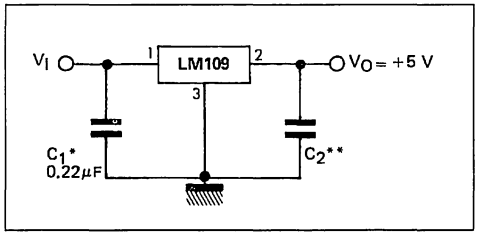


✡ Regulation better than 0.01% load, line and temperature can be obtained.
* Determines zener current. May be adjusted to minimize thermal drift.
** Solid tantalum.
↑ High stability resistors.

ADJUSTABLE OUTPUT REGULATOR



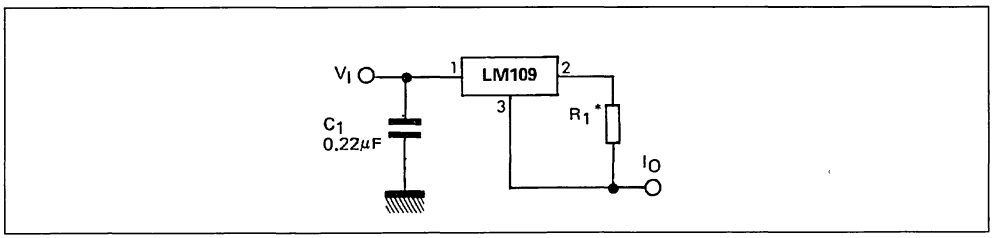
FIXED 5V REGULATOR



* Required if regulator is located an appreciable distance from power supply filter capacitor.

** Although no output capacitor is needed for stability, it does improve transient response.

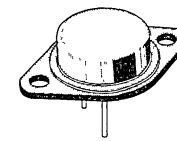
CURRENT REGULATOR



* Determines output current.

THREE-TERMINAL 3A-5V POSITIVE VOLTAGE REGULATORS

- OUTPUT CURRENT : 3A
- INTERNAL CURRENT AND THERMAL LIMITING
- TYPICAL OUPUT IMPEDANCE : 0.01Ω
- MINIMUM INPUT VOLTAGE : 7.5V
- POWER DISSIPATION : 30W



TO-3

DESCRIPTION

The LM223, LM323 are three-terminal positive voltage regulators with a preset 5V output and a load driving capability of 3A. New circuit design and processing techniques are used to provide the high output current without sacrificing the regulation characteristics of lower current devices.

The 3A regulator is virtually blowout proof.

Current limiting, power limiting and thermal shutdown provide the same high level of reliability obtained with these techniques in the LM209, 1A regulator.

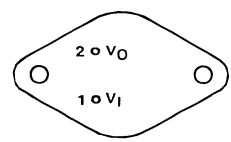
An overall worst case specification for the combined effects of input voltage, load current, ambient temperature, and power dissipation ensure that the LM223, LM323 will perform satisfactorily as a system element.

ORDER CODES

Part Number	Temperature Range	K
LM223	– 25°C to + 150°C	•
LM323	0°C to + 125°C	•

PIN CONNECTION (bottom view)

TO3



Case is ground

1 - Input
2 - Output

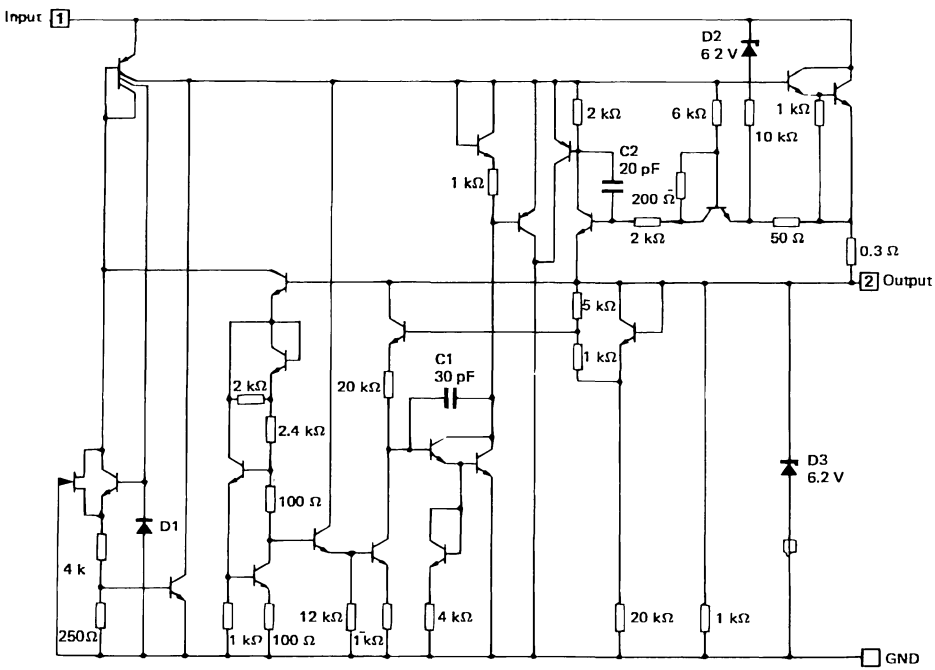
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_I	Input Voltage		20	V
I_O	Output Current		Internally Limited	
P_{tot}	Power Dissipation		Internally Limited	
T_{oper}	Operating Junction Temperature Range	LM223 LM323	– 25 to + 150 0 to + 125	°C
T_{stg}	Storage Temperature Range		– 65 to + 150	°C

THERMAL CHARACTERISTICS

Symbol	Parameter		Typ.	Max.	Unit
$R_{th(j-c)}$	Junction-case Thermal Resistance	TO-3	4		°C/W
$R_{th(j-a)}$	Junction-ambient Thermal Resistance	TO-3		35	°C/W

SCHEMATIC DIAGRAM



Case	V_I	V_O	GND
TO-3	1	2	Case

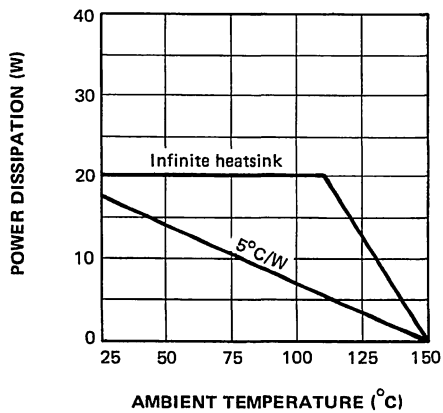
ELECTRICAL CHARACTERISTICS

LM223 : $-25°C < T_j < +150°C$
LM323 : $0°C < T_j < +125°C$
(unless otherwise specified)

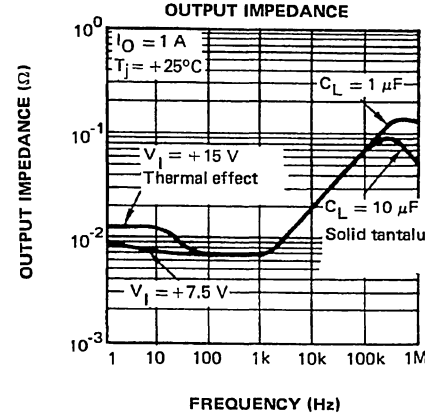
Symbol	Parameter	LM223			LM323			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_O	Output Voltage Range - (note 2) $T_j = +25°C$, $V_I = +7.5V$, $I_O = 0$ $T_{min} \le T_j \le T_{max}$, $P \le P_{max}$ $+7.5V \le V_I \le +15V$, $O \le I_O \le 3A$	4.7 4.6	5.0	5.3 5.4	4.8 4.75	5.0	5.2 5.25	V
K_{VI}	Line Regulation ($T_j = +25°C$, $+7.5V \le V_I \le +15V$) - Note 3		5	25		5	25	mV
K_{VO}	Load Regulation ($T_j = +25°C$, $V_I = +7.5V$, $0 \le I_O \le 3A$) - Note 3		25	100		25	100	mV
I_{IB}	Quiescent Current ($+7.5V \le V_I \le +15V$, $0 \le I_O \le 3A$))		12	20		12	20	mA
V_{NO}	Output Noise Voltage ($T_j = +25°C$, $10Hz \le f \le 100kHz$)		40			40		μV_{rms}
I_{OS}	Short-circuit Current Limit ($T_j = +25°C$) $V_I = +15V$ $V_I = +7.5V$		 3 4	 4.5 5		 3 4	 4.5 5	A
K_{VH}	Long Term Stability			35			35	mV

Notes : 1. Although power dissipation is internally limited, specifications apply only for $P \le 30W$.
2. Selected devices with tightened tolerance output voltage available.
3. Load and line regulation are specified at constant junction temperature. Pulse testing is required with a pulse width $\le 1ms$ and a duty cycle $\le 5\%$.

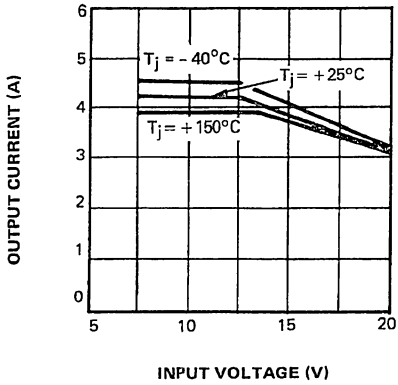
MAXIMUM POWER DISSIPATION



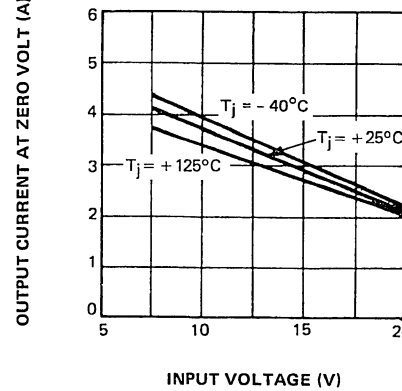
OUTPUT IMPEDANCE



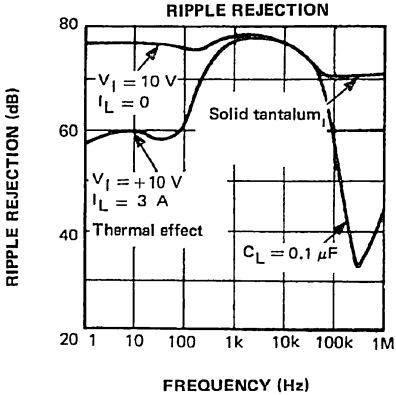
PEAK AVAILABLE OUTPUT CURRENT



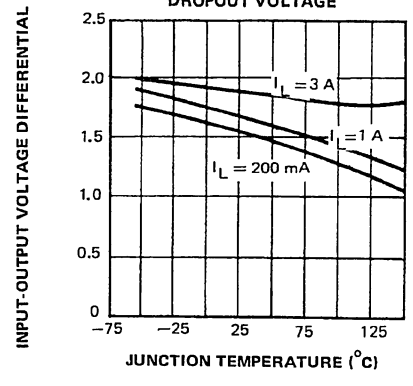
SHORT CIRCUIT.CURRENT



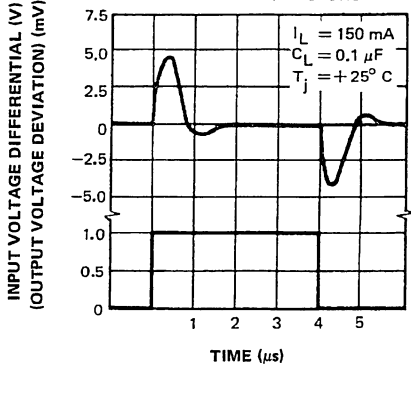
RIPPLE REJECTION



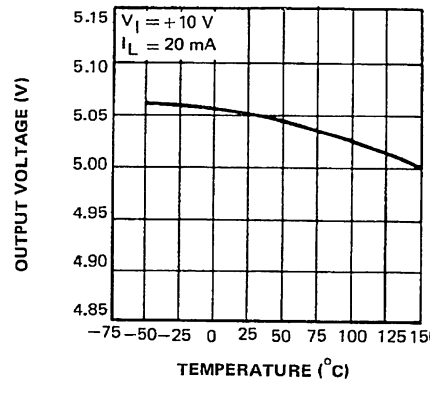
DROPOUT VOLTAGE

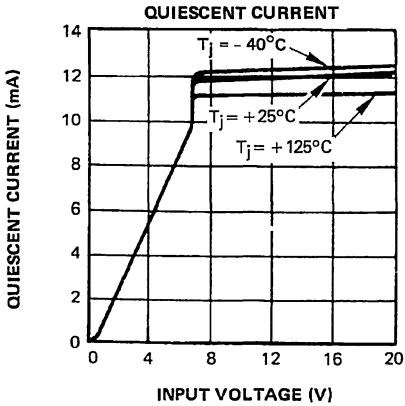


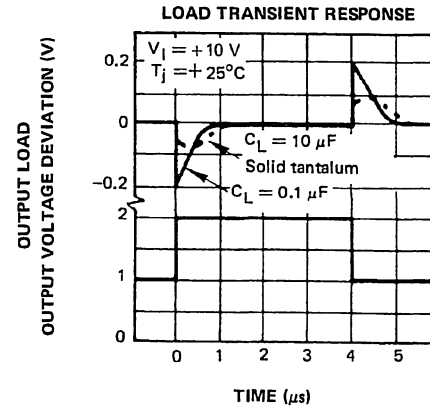
LINE TRANSIENT RESPONSE

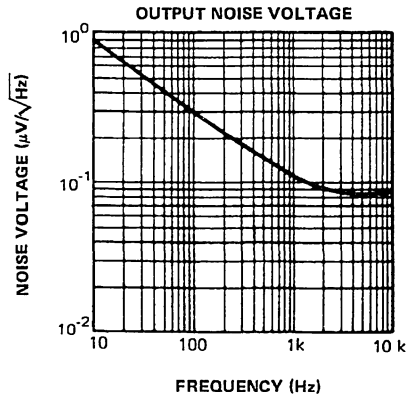


OUTPUT VOLTAGE



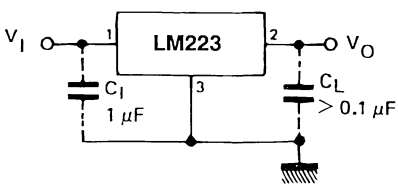






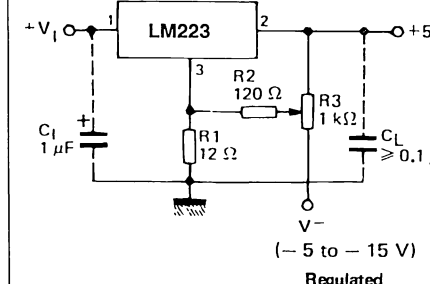
TYPICAL APPLICATIONS

BASIC 3A REGULATOR

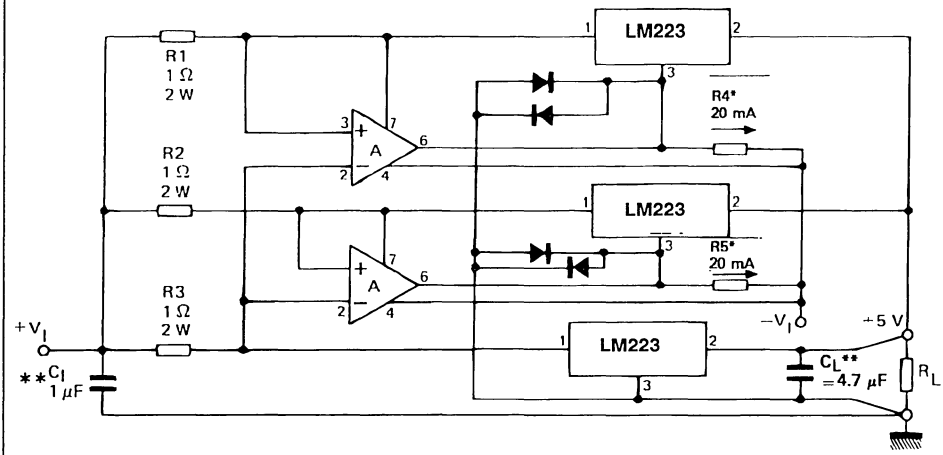


C_I = Required if regulator is distant from filter capacitors.
C_L = Regulator is stable with no load capacitor into resistive loads.

TRIMING OUTPUT TO 5V

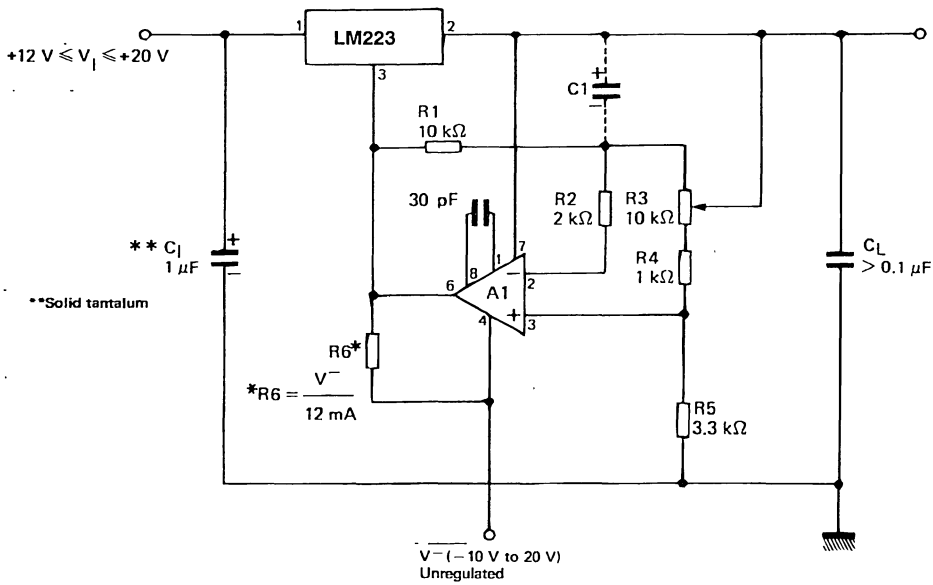


10A REGULATOR WITH COMPLETE OVERLOAD PROTECTION



* Selected for 20mA current from unregulated negative supply.
** Solid tantalum.
A = LM101A, LM201A, LM301A.

ADJUSTABLE REGULATOR 0 – 10V/3A



A1 = LM 101 A, LM 201 A, LM 301 A.
C1 = 2μF optional - improves ripple rejection, noise and transient response.

2.5 V VOLTAGE REFERENCES

- LOW TEMPERATURE COEFFICIENT
- WIDE OPERATING CURRENT OF 400 µA TO 10 mA
- 0.2 Ω DYNAMIC IMPEDANCE
- GUARANTEED TEMPERATURE STABILITY
- FAST TURN-ON

D
SO8
(Plastic Micropackage)

Z
TO92
(Plastic Package)

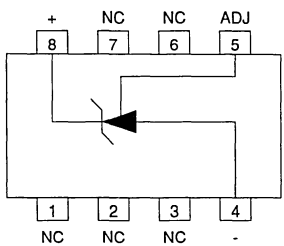
(order codes at the end of the datasheet)

DESCRIPTION

The LM236 and LM336 are precision 2.5 V regulator diodes. These voltage reference monolithic ICs operate like 2.5 V zener diodes with a low temperature coefficient and a dynamic impedance of 0.2 Ω A third pin enables adjusting the reference voltage and the temperature coefficient.

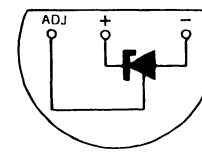
PIN CONNECTION

SO8
top view



E88LM236-01

TO92
bottom view

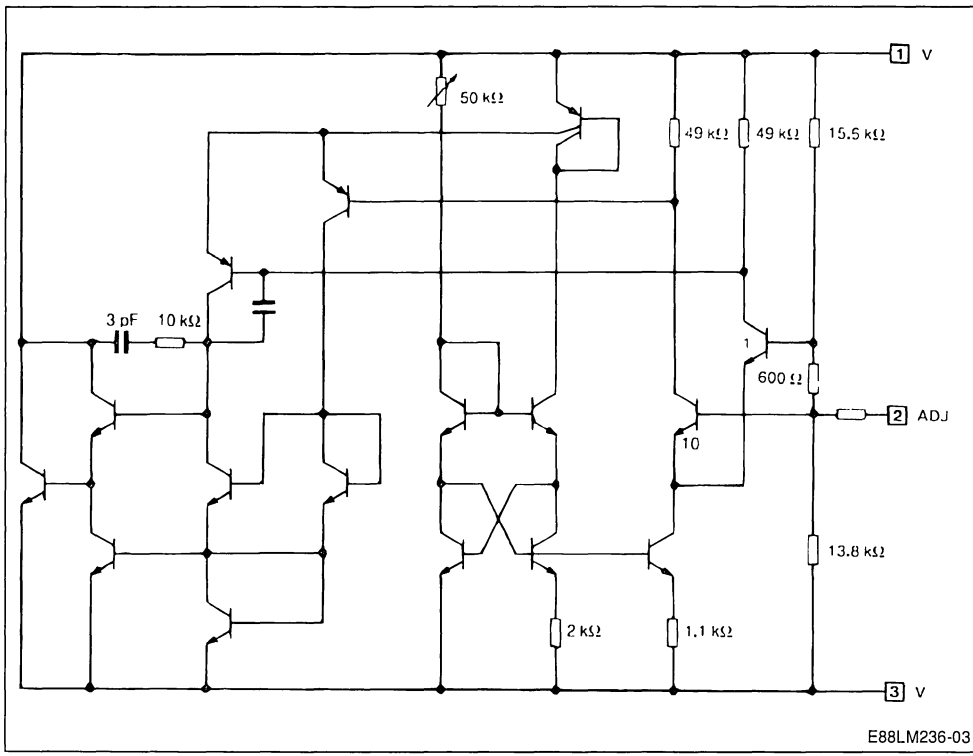


E88LM236-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		LM236, A	LM336, B	
	Current			mA
I_R	Reverse	15	15	
I_F	Foward	10	10	
T_{oper}	Operating Free-air Temperature Range	– 25 to + 85	0 to + 70	°C
T_{stg}	Storage Temperature Range	– 60 to + 150	– 60 to + 150	°C

SCHEMATIC DIAGRAM



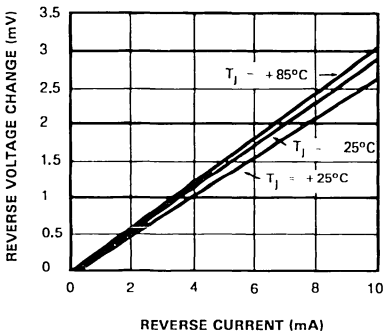
ELECTRICAL CHARACTERISTICS

LM236, A : $-25\ °C \leq T_{amb} \leq +85\ °C$
LM336, B : $0\ °C \leq T_{amb} \leq +70\ °C$
(unless otherwise specified)

Symbol	Parameter	LM236, A			LM236, B			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_R	Reserve Breakdown Voltage							V
	$T_{amb} = +25\ °C$ LM236, LM336	2.44	2.49	2.54	2.39	2.49	2.59	
	$I_R = 1$ mA LM236A, LM336B	2.465	2.49	2.515	2.44	2.49	2.54	
ΔV_R	Reserve breakdown change with current							mV
	(400 µA ≤ I_R ≤ 10 mA)							
	$T_{amb} = +25\ °C$		2.6	6		2.6	10	
	$T_{min} \leq T_{amb} \leq T_{max}$		3	10		3	12	
Z_D	Reserve Dynamic Impedance ($I_R = 1$ mA)							Ω
	$T_{amb} = +25\ °C$		0.2	0.6		0.2	1	
	$T_{min} \leq T_{amb} \leq T_{max}$		0.4	1		0.4	1.4	
K_{VT}	Temperature Stability ($V_R = 2.49$ V, $I_R = 1$ mA)		3.5	9		1.8	6	mV
K_{VH}	Long Term Stability ($T_{amb} = +25\ °C \pm 0.1\ °C$, $I_R = 1$ mA)		20			20		ppm

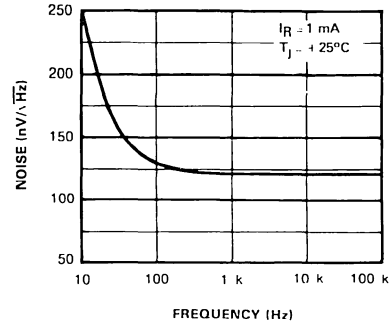
Note : 1. The maximum junction temperature of the LM236 is + 125 °C and the LM336 is + 100 °C For elevated junction temperature, devices should be derated based on a thermal resistance of 180 °C/W junction to ambient with 10 mm leads from a PC board or 160 °C/W junction to ambient with 3 mm lead length to a PC board

REVERSE VOLTAGE CHANGE



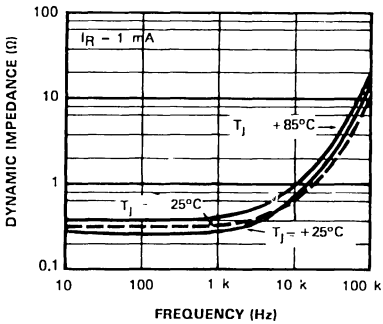
E88LM236-04

ZENER NOISE VOLTAGE



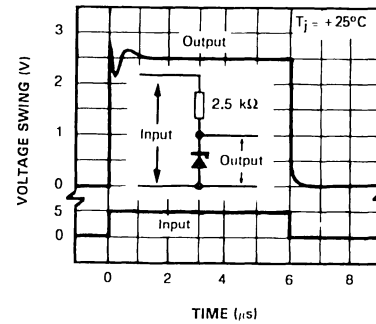
E88LM236-05

DYNAMIC IMPEDANCE



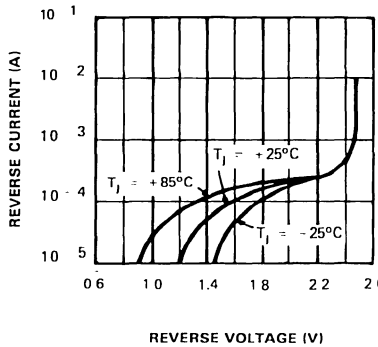
E88LM236-06

RESPONSE TIME



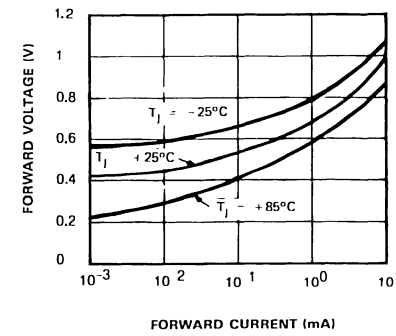
E88LM236-07

REVERSE CHARACTERISTICS



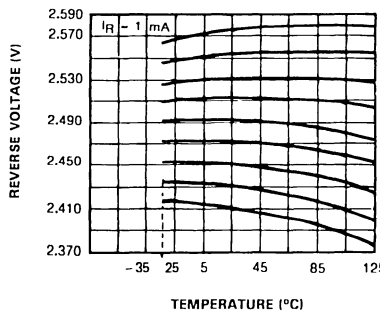
E88LM236-08

FORWARD CHARACTERISTICS



E88LM236-09

TEMPERATURE DRIFT



E88LM236-10

APPLICATIONS HINTS

The LM236, LM336 voltage references are easier to use than zener diodes. Their low impedance and wide current range facilitate biasing in any circuits. Besides, the breakdown voltage or the temperature coefficient can be ajusted so as to optimize the performance of the circuit.

Figure 1 represents a LM336 with a 10 kΩ potentiometer to adjust the reverse breakdown voltage. By adding resistor R1, the breakdown voltage can be adjusted without altering the temperature coefficient of the circuit. The adjustment range is generally sufficient to adjust the initial tolerance of the circuit and the inaccuracy of the amplifier circuit.

To obtain a lower temperature coefficient two diodes can be connected in series as indicated in fig. 2. When the circuit is adjusted to 2.49 V the temperature coefficient is minimized.

For a correct temperature coefficient, the diodes should be at the same ambient temperature as the LM336. The value of R1 is not critical (2-20 kΩ).

Figure 1 : The LM236 with Pot for Adjustment of Breakdown Voltage.

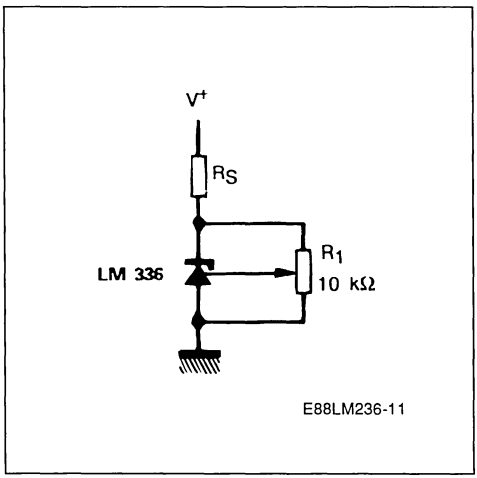
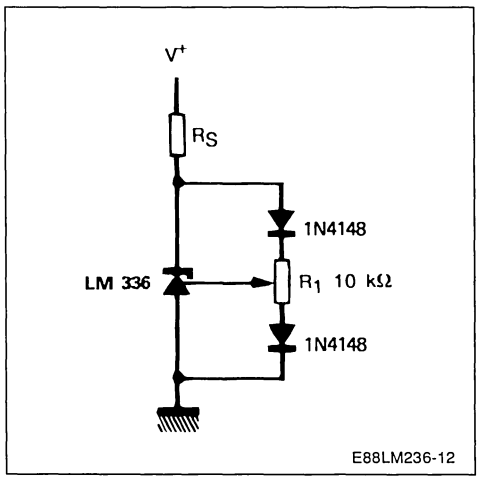


Figure 2 : Temperature Coefficient Adjustment.



TYPICAL APPLICATIONS

Figure 3 : 2.5 V Reference.

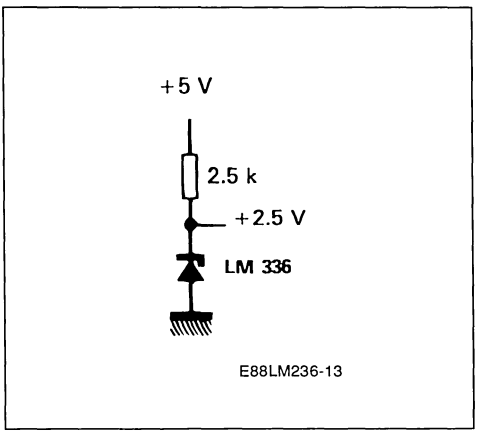


Figure 4 : Wide Input Range Reference.

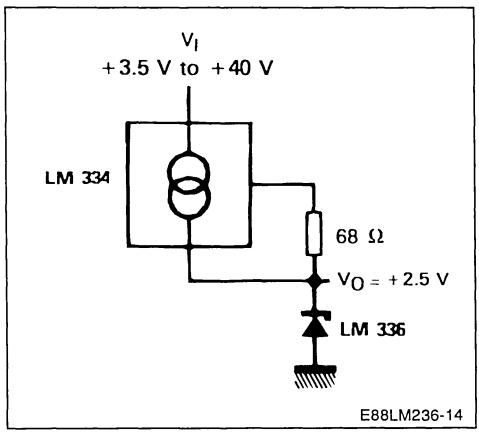


Figure 5 : Precision Power Regulator with Low Temperature Coefficient.

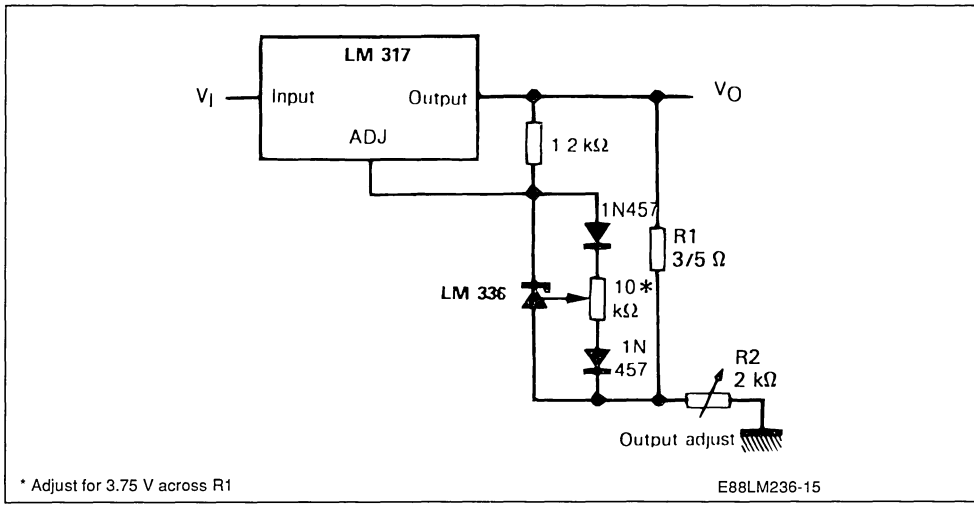


Figure 6 : Adjustable Shunt Regulator.

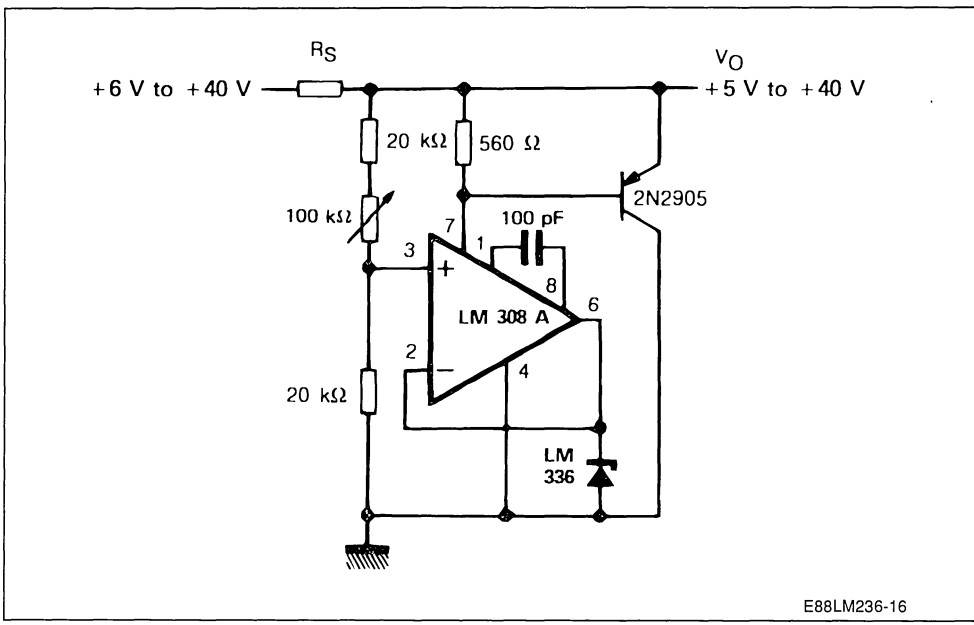


Figure 7 : Linear Ohmmeter.

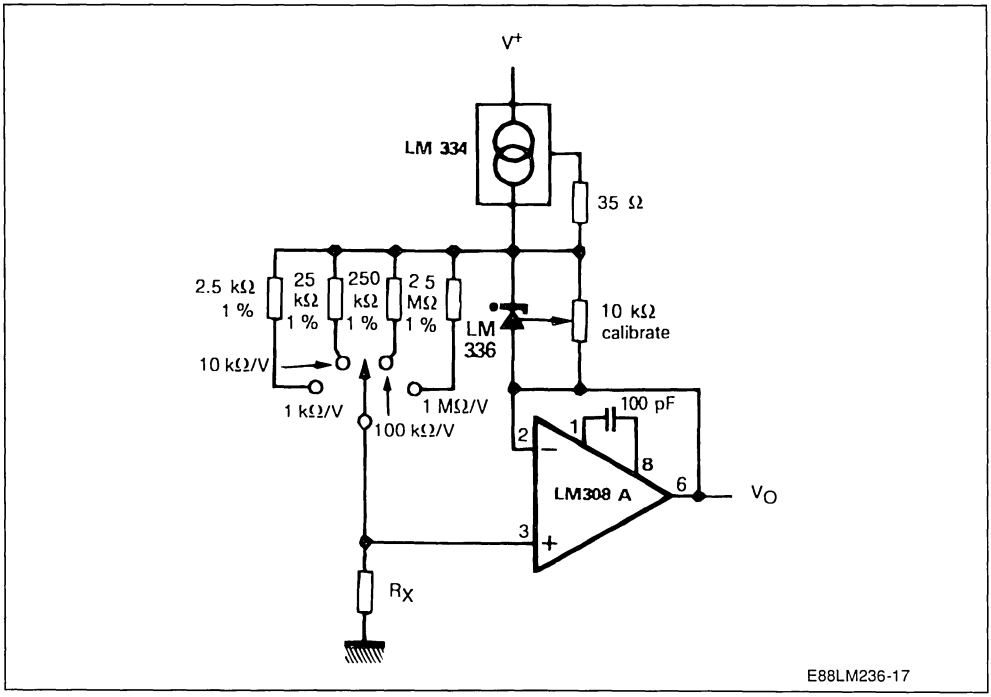


Figure 8 : Bipolar Output Reference.

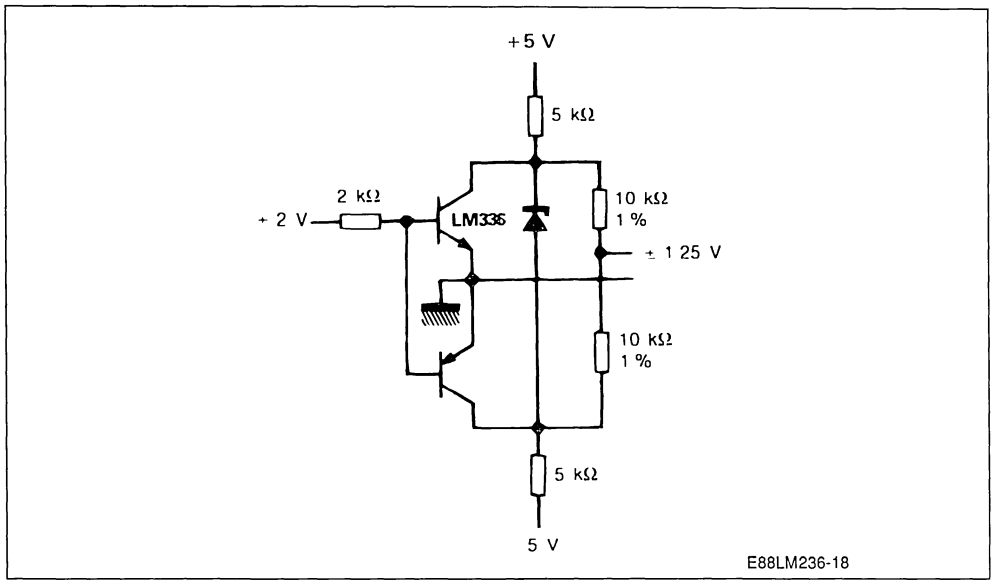


Figure 9 : 5 V Buffered Reference.

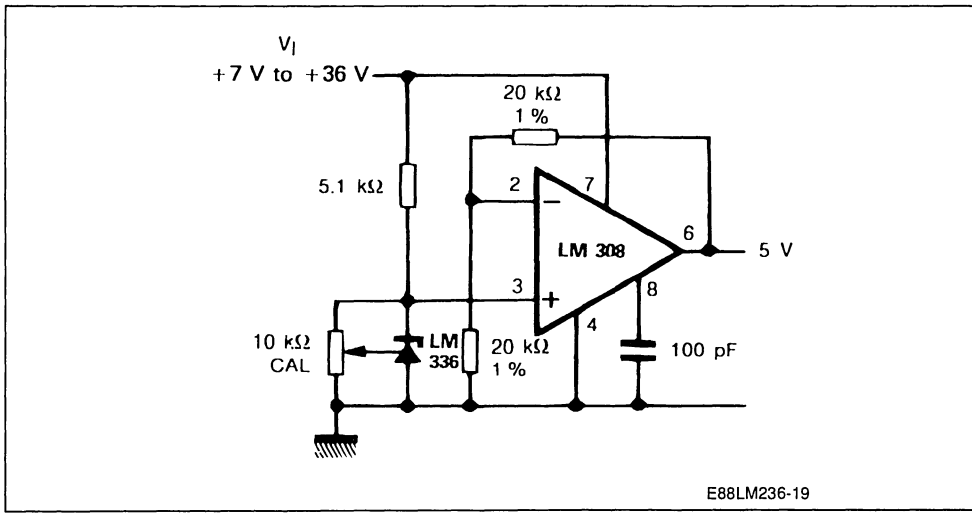
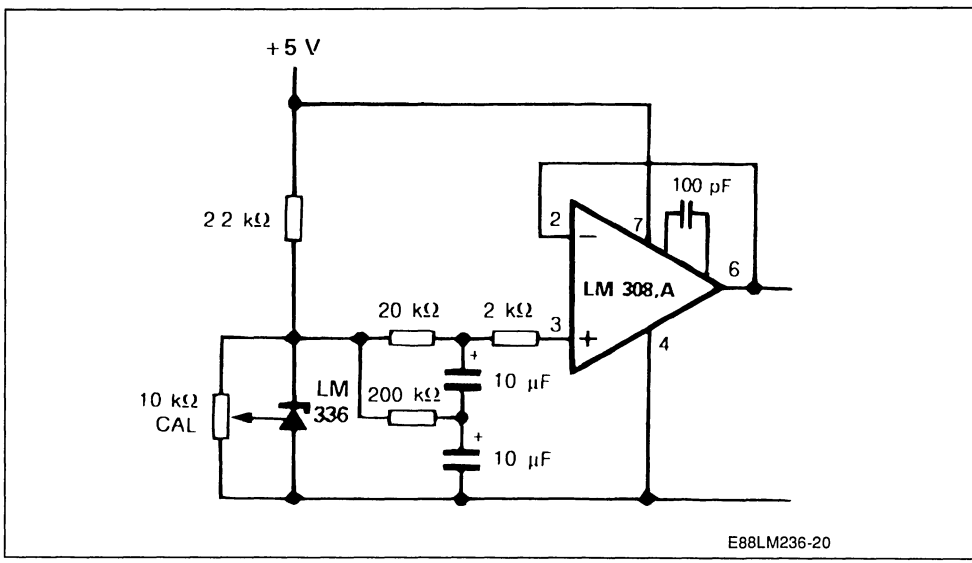


Figure 10 : Low Noise Buffered Reference.

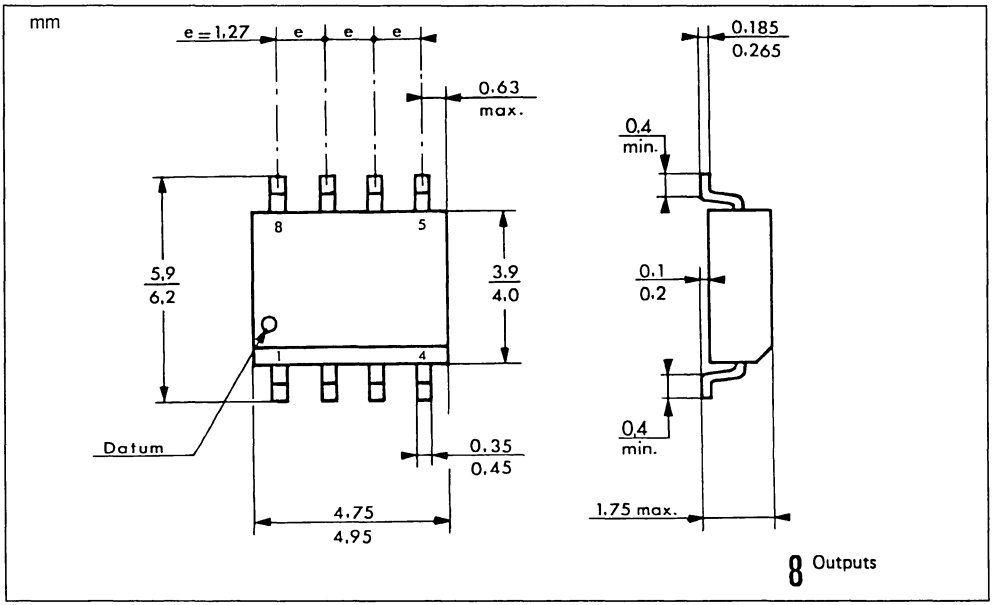


ORDER CODES

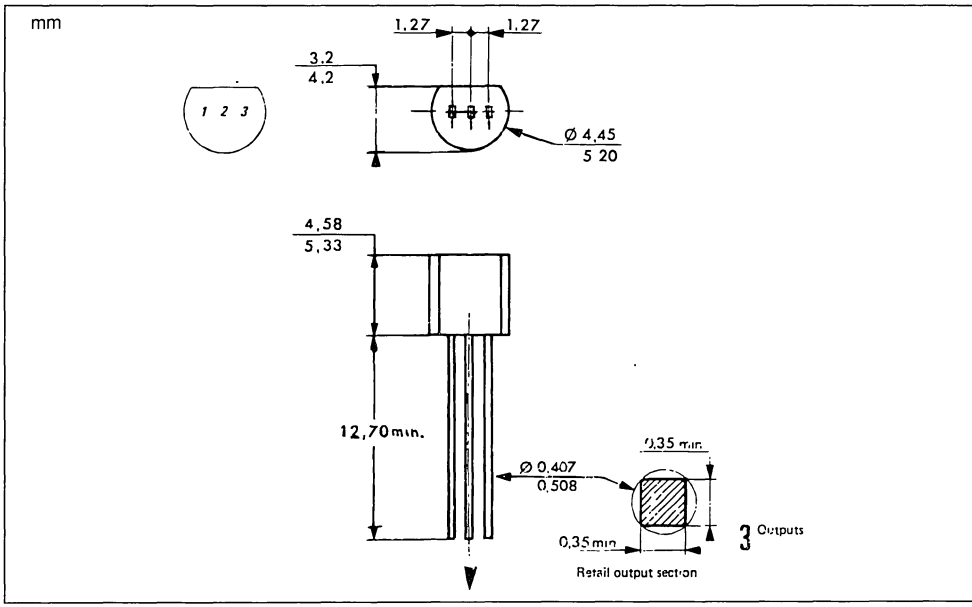
Part Number	Temperature Range	Package
LM236Z	– 25 °C to + 85 °C	To 92
LM236AZ	– 25 °C to + 85 °C	To 92
LM236D	– 25 °C to + 85 °C	So 8
LM236AD	– 25 °C to + 85 °C	So 8
LM336Z	0 °C to + 70 °C	To 92
LM336BZ	0 °C to + 70 °C	To 92
LM336D	0 °C to + 70 °C	So 8
LM336BD	0 °C to + 70 °C	So 8

PACKAGE MECHANICAL DATA

8 PINS – PLASTIC MICROPACKAGE SO



3 PINS – PLASTIC PACKAGE TO92

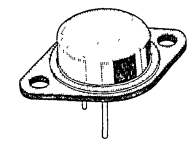


SGS-THOMSON MICROELECTRONICS

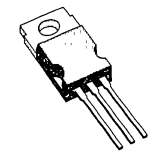
LM237
LM337

THREE-TERMINAL ADJUSTABLE NEGATIVE VOLTAGE REGULATORS

- OUTPUT VOLTAGE ADJUSTABLE DOWN TO V_{ref}
- 1.5A GUARANTEED OUTPUT CURRENT
- 0.3%/V TYPICAL LOAD REGULATION
- 0.01%/V TYPICAL LINE REGULATION
- CURRENT LIMIT CONSTANT WITH TEMPERATURE
- RIPPLE REJECTION : 77dB
- STANDARD 3-LEAD TRANSISTOR PACKAGES
- EXCELLENT THERMAL REGULATION : 0.002%/V
- 50ppm/°C TEMPERATURE COEFFICIENT



TO-3



TO-220

DESCRIPTION

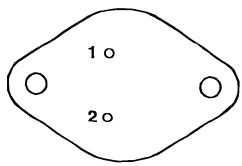
The LM237 series are adjustable 3-terminal negative voltage regulators capable of supplying in excess - 1.5A over a - 1.2 to - 37V output voltage range. They are exceptionally easy to use and require only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, LM237 regulators are supplied in standard transistor packages which are easily mounted and handled. In addition to higher performance than fixed regulators, the LM237 series offer full overload protection available only in integrated circuits. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

ORDER CODES

Part Number	Temperature Range	Package	
		K	SP
LM237	– 25°C to + 150°C	•	
LM337	0°C to + 125°C	•	•

PIN CONNECTIONS

TO-3
(bottom view)



1 - Output
2 - Adj
Case is input

TO-220
(front view)

1 - Adj
2 - Output
3 - Input

Heatsink surface connected to input

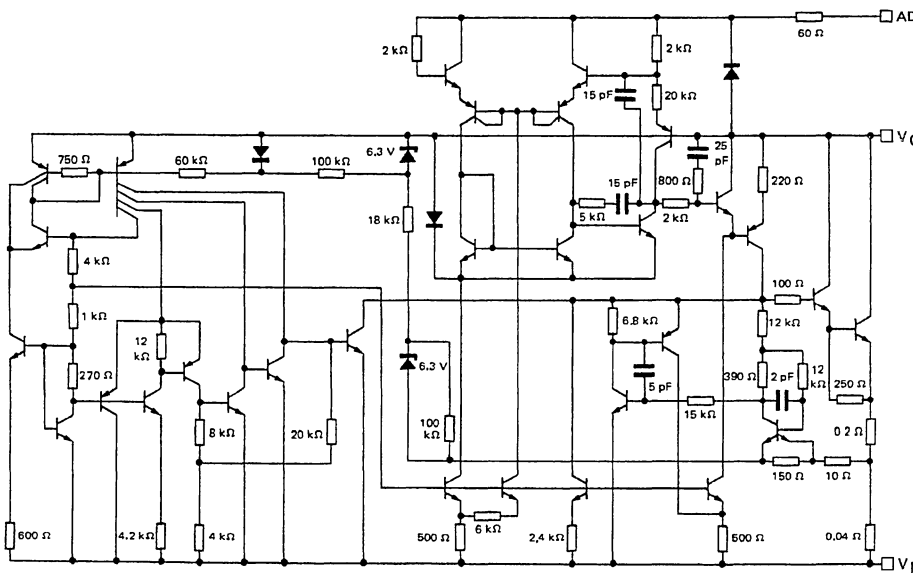
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_I-V_O	Input-output Voltage Differential		40	V
I_O	Output Current		1.5	A
T_{oper}	Operating Junction Temperature Range	LM237 LM337	– 25 to + 150 0 to + 125	°C
T_{stg}	Storage Temperature Range		– 65 to + 150	°C
P_{tot}	Power Dissipation		Internally Limited	

THERMAL CHARACTERISTICS

Symbol	Parameter		Typ.	Max.	Unit
$R_{th(j-c)}$	Junction-case Thermal Resistance	TO-3 TO-220		4 3	°C/W
$R_{th(j-a)}$	Junction-ambient Thermal Resistance	TO-3 TO-220	35	 70	°C/W

SCHEMATIC DIAGRAM



Case	V_I	V_O	ADJ
TO-3	Case	1	2
TO-220	3	2	1

ELECTRICAL CHARACTERISTICS

LM237 : $-25°C < T_j < +150°C$
LM337 : $0°C < T_j < +125°C$
$|V_I - V_O| = 5V$, $I_O = 0.5A$
(unless otherwise specified)

Symbol	Parameter	LM237			LM337-LM337I			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{ref}	Reference Voltage $T_{amb} = +25°C$ $T_{min} \le T_j \le T_{max}$ $3V \le \lvert V_I - V_O \rvert \le 40V$, $10mA \le \lvert I_O \rvert \le \lvert I_{O(max)} \rvert$, $P \le P_{max}$	- 1.225 - 1.20	- 1.25 - 1.25	- 1.275 - 1.30	- 1.213 - 1.20	- 1.25 - 1.25	- 1.287 - 1.30	V
K_{VI}	Line Regulation ($T_{amb} = +25°C$, $3V \le \lvert V_I - V_O \rvert \le 40V$) - Note 2 $I_O = 0.1A$		0.01	0.02		0.01	0.04	%/V
K_{VO}	Load Regulation ($T_{amb} = +25°C$, $10mA \le \lvert I_O \rvert \le \lvert I_{O(max)} \rvert$) - Note 2 $\lvert V_O \rvert \le 5V$ $\lvert V_O \rvert \ge 5V$		 15 0.3	 25 0.5		 15 0.3	 50 1	 mV %
	Thermal Regulation ($T_{amb} = +25°C$, pulse 10ms)		0.002	0.02		0.003	0.04	%/W
I_{adj}	Adjustment Pin Current		65	100		65	100	µA
ΔI_{adj}	Adjustment Pin Current Change ($T_{amb} = +25°C$, $10mA \le \lvert I_O \rvert \le \lvert I_{O(max)} \rvert$, $3V \le \lvert V_I - V_O \rvert \le 40V$)		2	5		2	5	µA
K_{VI}	Line Regulation ($3V \le \lvert V_I - V_O \rvert \le 40V$) - Note 2		0.02	0.05		0.02	0.07	%/V
K_{VO}	Load Regulation ($10mA \le \lvert I_O \rvert \le \lvert I_{O(max)} \rvert$) - Note 2 $V_O \le 5V$ $V_O \ge 5V$		 20 0.3	 50 1		 20 0.3	 70 1.5	 mV %
$\lvert I_{O(min)} \rvert$	Minimum Load Current $\lvert V_I - V_O \rvert \le 40V$ $\lvert V_I - V_O \rvert \le 40V$		 2.5 1.2	 5 3		 2.5 1.5	 10 6	mA
I_{OS}	Short-circuit Output Current $\lvert V_I - V_O \rvert \le 15V$ $\lvert V_I - V_O \rvert = 40V$, $T_j = +25°C$	 1.5 0.24	 2.2 0.4		 1.5 0.15	 2.2 0.4		A
V_{NO}	RMS Output Noise (% of V_O) ($T_{amb} = +25°C$, $10Hz \le f \le 10kHz$)		0.003			0.003		%
R_{vf}	Ripple Rejection Ratio $V_O = -10V$, f = 120Hz $C_{adj} = 10µF$	 66	 60 77		 66	 60 77		dB
K_{VT}	Temperature Stability ($T_{min} \le T_j \le T_{max}$)		0.6			0.6		%
K_{VH}	Long Term Stability ($T_{amb} = +125°C$, 1000H)		0.3	1		0.3	1	%

Notes : 1. Although power dissipation is internally limited, these specifications are applicable for power dissipation of :

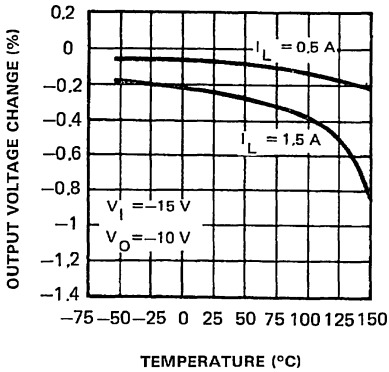
- 15W for TO-220
- 20W for TO-3 Package

$I_{O(max)}$ is :

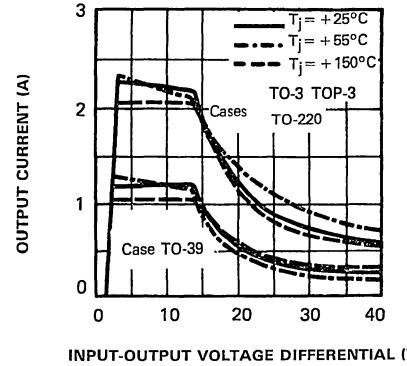
- 1.5A

2. Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

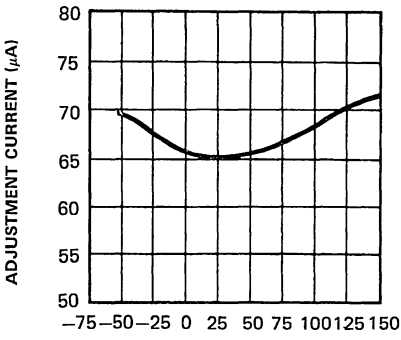
LOAD REGULATION



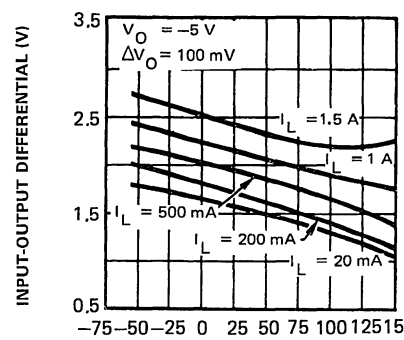
CURRENT LIMIT



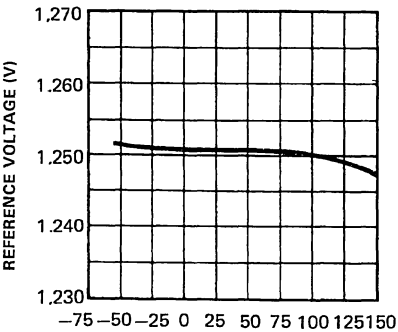
ADJUSTMENT CURRENT



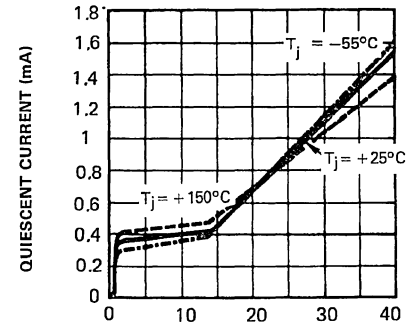
DROPOUT VOLTAGE



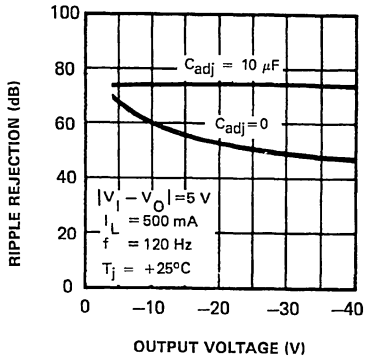
TEMPERATURE STABILITY



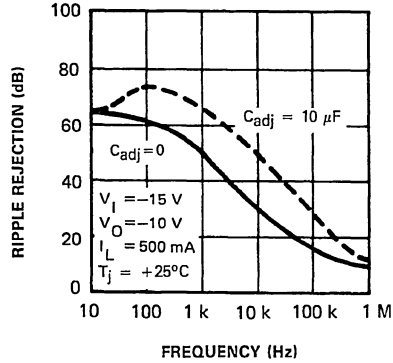
MINIMUM OPERATING CURRENT



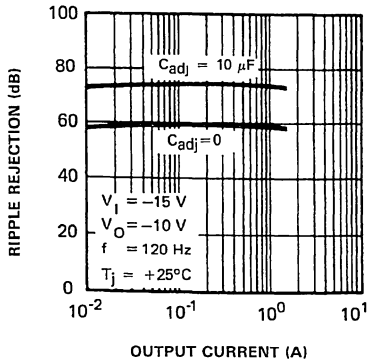
RIPPLE REJECTION VERSUS OUTPUT VOLTAGE



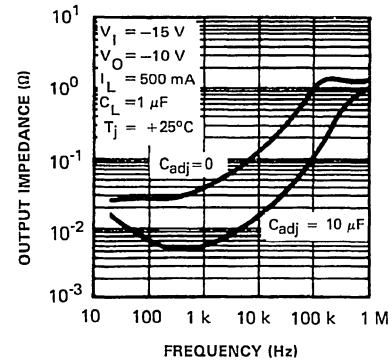
RIPPLE REJECTION VERSUS FREQUENCY



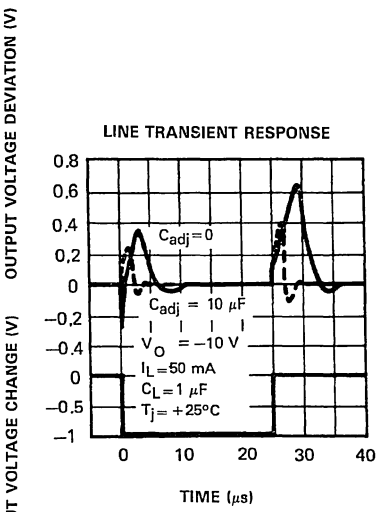
RIPPLE REJECTION VERSUS OUTPUT CURRENT



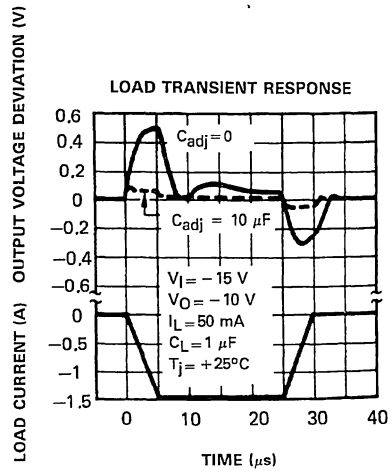
OUTPUT IMPEDANCE



LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE



THERMAL REGULATION

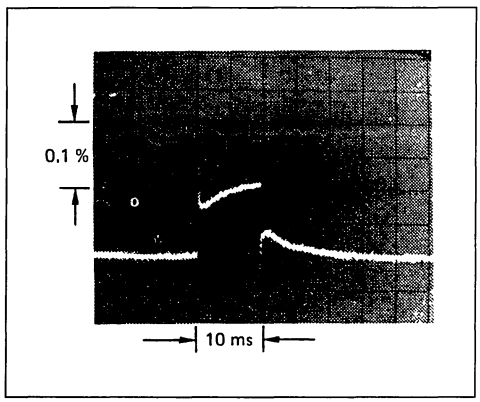
When power is dissipated in an IC, a temperature gradient occurs across the IC chip affecting the individual IC circuit components. With an IC regulator, this gradient can be especially severe since power dissipation is large.

Thermal regulation is the effect of these temperature gradients on output voltage (in percentage output change) per watt of power change in a specified time. Thermal regulation error is independent of electrical regulation or temperature coefficient, and occurs within 5ms to 50ms after a change in power dissipation. Thermal regulation depends on IC layout as well as electrical design. The thermal regulation of a voltage regulator is defined as the percentage change of V_O, per watt, within the first 10ms after a step of power, is applied.

In figure 1, a typical LM337's output drifts only 3mV for 0.03% of $V_O = -10V$) when a 10W pulse is applied for 10ms. This performance is thus well inside the specification limit of 0.02%/W x 10W = 0.2% max. When the 10W pulse is ended the thermal regulation again shows a 3mV step as the LM337 chip cools off. Note that the load regulation error of about 8mV(0.08%) is additional to the thermal regulation error.

In figure 2, when the 10W pulse is applied for 100ms, the output drifts only slightly beyond the drift in the first 10ms and the thermal error stays well within 0.1% (10mV).

Figure 1.



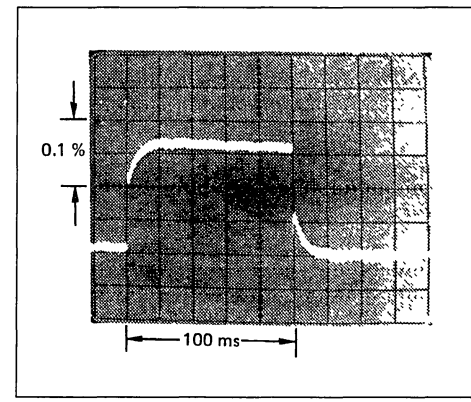
LM 337, $V_0 = -10V$

$V_I - V_0 = -40V$

$I_L = 0A \rightarrow 0.25A \rightarrow 0A$

Vertical sensitivity 5mV/div.

Figure 2.



LM 337, $V_0 = -10V$

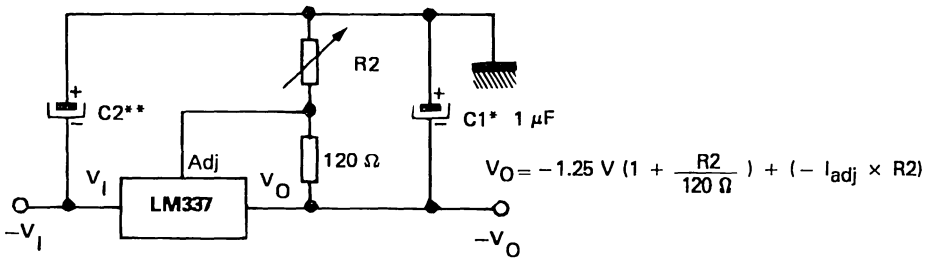
$V_I - V_0 = -40V$

$I_L = 0A \rightarrow 0.25A \rightarrow 0A$

Horizontal sensitivity 20msN/div.

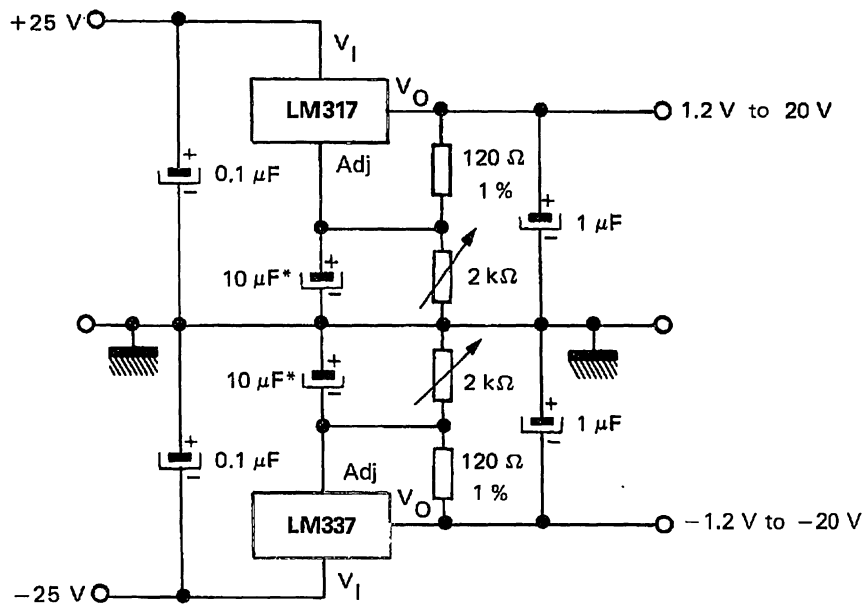
TYPICAL APPLICATIONS

ADJUSTABLE NEGATIVE VOLTAGE REGULATOR



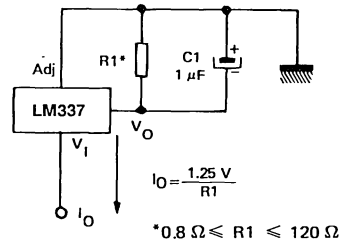
* C1 = 1µF solid tantalum or 10µF aluminium electrolytic required for stability.
** C2 = 1µF solid tantalum is required only if regulator is more than 10cm from power supply filter capacitor.

ADJUSTABLE LAB VOLTAGE REGULATOR

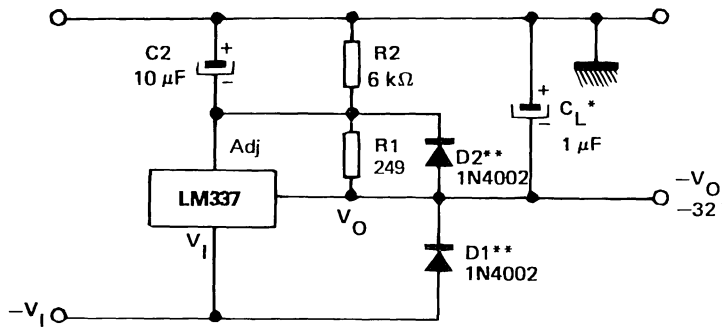


* The 10µF capacitors are optimal to improve ripple rejection.

CURRENT REGULATOR

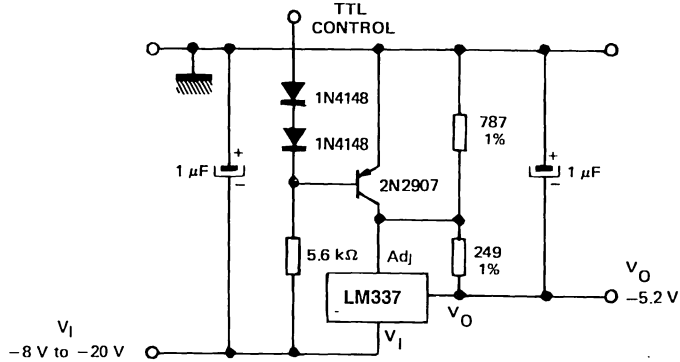


NEGATIVE REGULATOR WITH PROTECTION DIODES



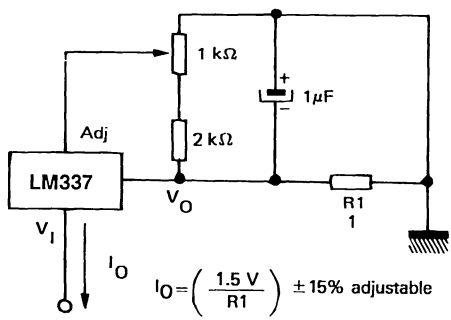
* When C_L is larger than 20µF, D1 protects the LM137 in case the input supply is shorted.
** When C2 is larger than 10µF and V_O is larger than – 25V, D2 protects the LM137 in case the output is shorted.

* – 5.2V REGULATOR WITH ELECTRONIC SHUTDOWN



* Minimum output = – 1.3V when control input is low.

ADJUSTABLE CURRENT REGULATOR

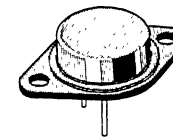


SGS-THOMSON MICROELECTRONICS

LM238
LM338

THREE-TERMINAL 5-A ADJUSTABLE VOLTAGE REGULATORS

- GUARANTEED 7A PEAK OUTPUT CURRENT
- GUARANTEED 5A OUTPUT CURRENT
- ADJUSTABLE OUTPUT DOWN TO 1.2V
- LINE REGULATION TYPICALLY 0.005% /V
- LOAD REGULATION TYPICALLY 0.1%
- GUARANTEED THERMAL REGULATION
- CURRENT LIMIT CONSTANT WITH TEMPERATURE
- STANDARD 3-LEAD TRANSISTOR PACKAGE



TO3
K SUFFIX
(Steel Can)

DESCRIPTION

The LM238/LM338 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 5A over a 1.2V to 32V output range. They are exceptionally easy to use and require only 2 resistors to set the output voltage. Careful circuit design has resulted in outstanding load and line regulation - comparable to many commercial power supplies. The LM238 family is supplied in a standard 3-lead transistor package.

A unique feature of the LM238 family is time-dependent current limiting. The current limit circuitry allows peak currents of up to 12A to be drawn from the regulator for short periods of time. This allows the LM238 to be used with heavy transient loads and speeds start-up under full-load conditions. Under sustained loading conditions, the current limit decreases to a safe value protecting the regulator. Also included on the chip are thermal overload protection and safe area protection for the power transistor. Overload protection remains functional even if the adjustment pin is accidentally disconnected.

Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators or discrete designs, the LM238 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to input differential is not exceeded.

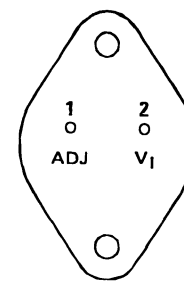
The LM228/LM338 are packaged in standard steel TO-3 transistor packages. The LM238 from – 25°C to + 150°C and the LM338 from 0°C to + 125°C.

ORDER CODES

Part Number	Temperature Range	Package K
LM238	– 25°C to + 150°C	•
LM338	0°C to + 125°C	•

Note : Hi-Rel Versions Available .
Example : LM238K

PIN CONNECTION
(bottom view)



Case is output

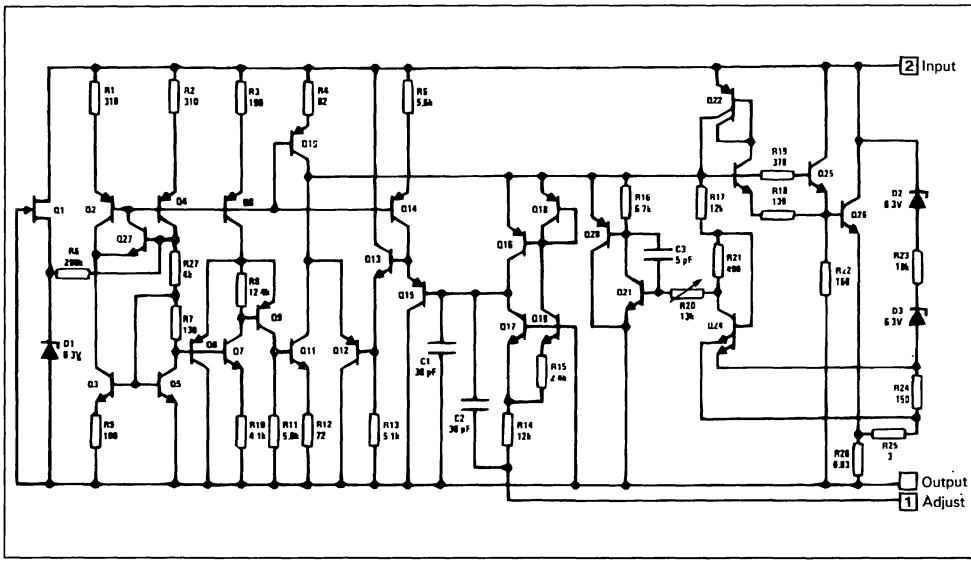
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
P_{tot}	Power Dissipation		Internally Limited	W
$V_I - V_O$	Input-output Voltage Differential		35	V
T_{oper}	Operating Junction Temperature Range	LM238 LM338	– 25 to + 150 0 to + 125	°C
T_{stg}	Storage Temperature Range		– 65 to + 150	°C
T_{lead}	Lead Temperature (soldering, 10 seconds)		300	°C

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Maximum Junction-case Thermal Resistance	4	°C/W
$R_{th(j-a)}$	Typical Junction-ambient Thermal Resistance	35	°C/W

SCHEMATIC DIAGRAM

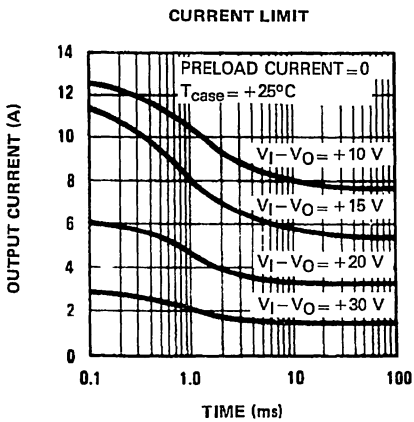


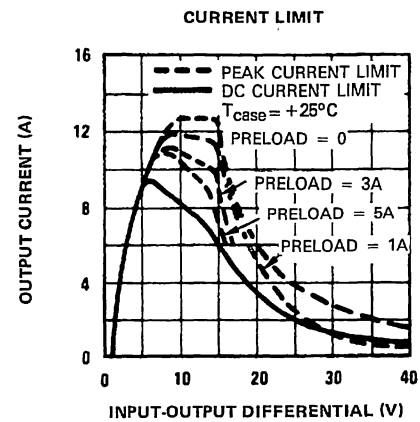
ELECTRICAL CHARACTERISTICS

LM238 : $-25°C \leq T_j \leq +150°C$, $V_I - V_O = +5V$, $I_O = 2.5A$
LM338 : $0°C \leq T_j \leq +150°C$, $V_I - V_O = +5V$, $I_O = 2.5A$
Although power dissipation is internally limited, these specifications apply to power dissipation up to 50W. (unless otherwise specified)

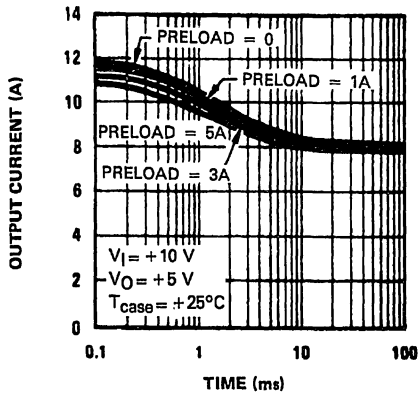
Symbol	Parameter	LM238			LM338			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
K_{VI}	Line Regulation - (note 1) $T_{amb} = +25°C$, $+3V \leq (V_I - V_O) \leq +35V$		0.005	0.01		0.005	0.03	%/V
K_{VO}	Load Regulation $T_{amb} = +25°C$, $10mA \leq I_O \leq 5A$ $V_O \leq +5V$ - (note 1) $V_O \geq +5V$ - (note 1)		5 0.1	15 0.3		5 0.1	25 0.5	mV %
	Thermal Regulation (pulse = 20ms)		0.002	0.01		0.002	0.02	%/W
I_{adj}	Adjustment Pin Current		45	100		45	100	µA
ΔI_{adj}	Adjustment Pin Current Change $10mA \leq I_L \leq 5A$, $+3V \leq (V_I - V_O) \leq +35V$		0.2	5		0.2	5	µA
$V_{(ref)}$	Reference Voltage $(+3V \leq V_I - V_O) \leq +35V$, $10mA \leq I_O \leq 5A$, $p \leq 50W$)	1.19	1.24	1.29	1.19	1.24	1.29	V
K_{VI}	Line Regulation $+3V \leq (V_I - V_O) \leq +35V$ - (note 1)		0.02	0.04		0.02	0.06	%/V
K_{VO}	Load Regulation ($10mA \leq I_O \leq 5A$) - Note 1 $V_O \leq +5V$ $V_O \geq +5V$		20 0.3	30 0.6		20 0.3	50 1.0	mV %
K_{VT}	Temperature Stability ($T_{min} \leq T_j \leq T_{max}$)		1			1		%
$I_{O(min)}$	Minimum Load Current ($V_I - V_O = +35V$)		3.5	5		3.5	10	mA
$I_{O(max)}$	Current Limit ($V_I - V_O \leq +10V$) DC 0.5ms Peak $V_I - V_O = +30V$	 5.0 7	 8 12 1		 5.0 7	 8 12 1		A
	RMS Output Noise, % of V_O ($T_{amb} = +25°C$, $10Hz \leq f \leq 10kHz$)			0.003		0.003		%
R_{vf}	Ripple Rejection Ratio $V_O = +10V$, f = 120Hz $C_{adj} = 10µF$	 60	60 75		 60	60 75		dB
K_{VH}	Long Term Stability ($T_{amb} = +125°C$)		0.3	1		0.3	1	%

Note 1 : Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects are taken into account separately by thermal rejection.

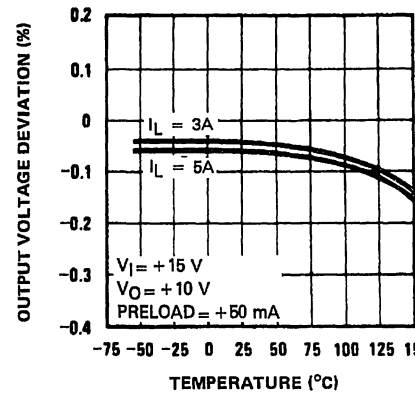




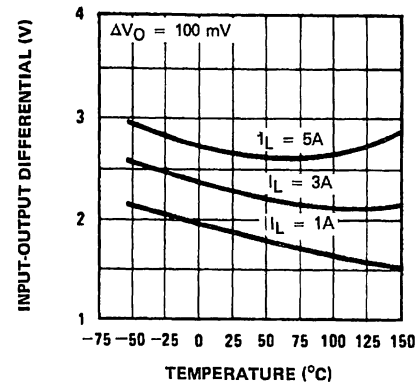
CURRENT LIMIT



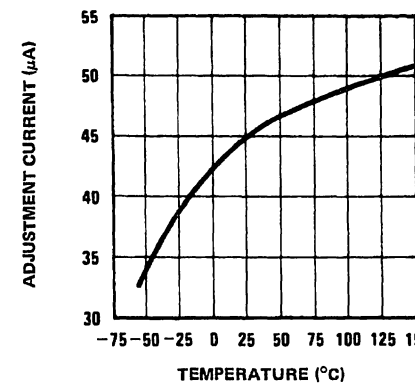
LOAD REGULATION



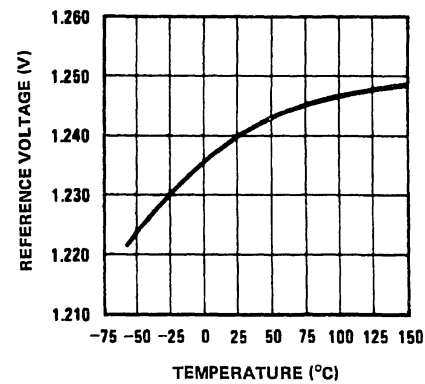
DROPOUT VOLTAGE



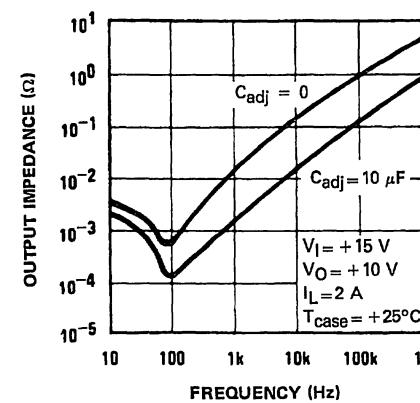
ADJUSTMENT CURRENT



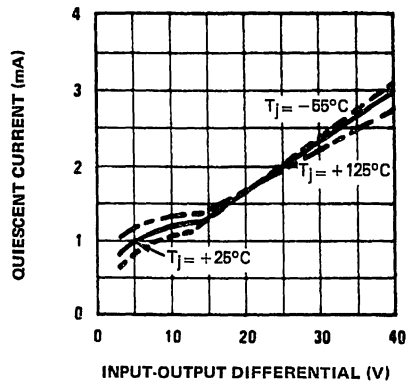
TEMPERATURE STABILITY



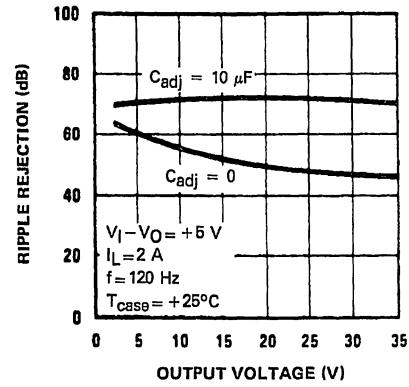
OUTPUT IMPEDANCE



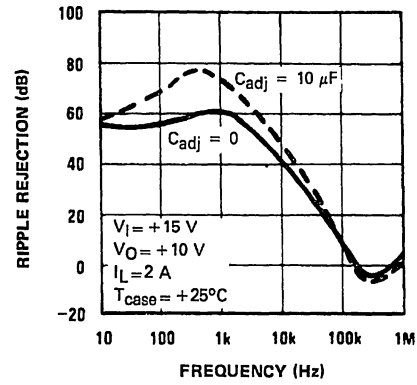
MINIMUM OPERATING CURRENT



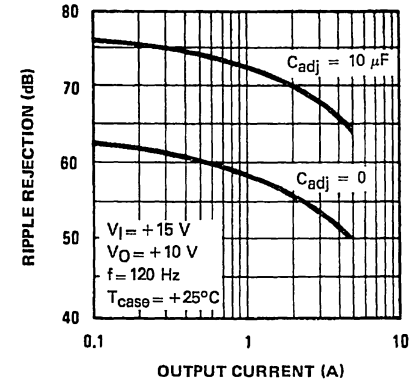
RIPPLE REJECTION



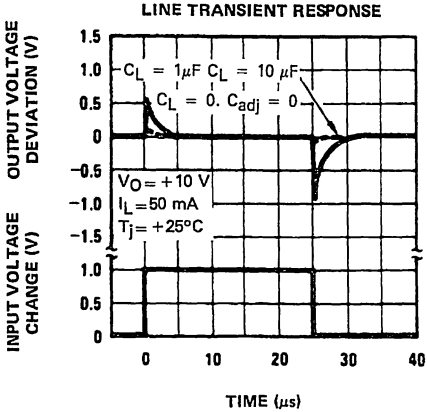
RIPPLE REJECTION



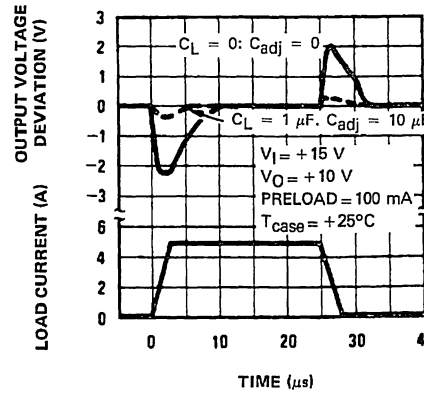
RIPPLE REJECTION



LINE TRANSIENT RESPONSE

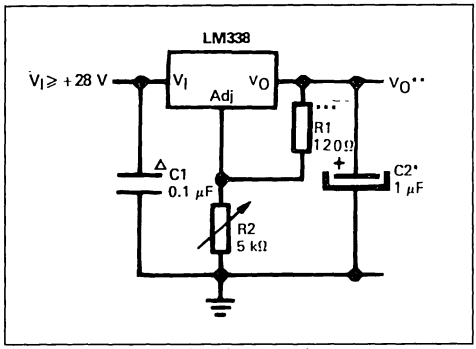


LOAD TRANSIENT RESPONSE



TYPICAL APPLICATIONS

+ 1.2V to + 25V ADJUSTABLE REGULATOR



Δ Needed if device is far from filter capacitors.

* Optional-improves transient response. Output capacitors in the range of 1μF to 100μF of aluminium or tantalum electrolytic are commonly used to provide improved output impedance and rejection of tran-sients

** $V_O = 1.25V\ (1 + \frac{R2}{R1})$

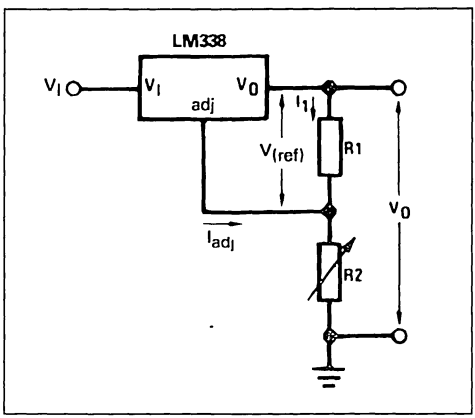
*** R1 = 240Ω for LM138 and LM238

APPLICATION HINTS

In operation, the LM338 develops a nominal 1.25V reference voltage, $V_{(ref)}$, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2, giving an output voltage of

$$V_O = V_{(ref)}\ (1 + \frac{R2}{R1}) + I_{adj}R2$$

Figure 1.



Since the 50μA current from the adjustment terminal represents an error term, the LM338 was designed to minimize I_{adj} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

EXTERNAL CAPACITORS

An input bypass capacitor is recommended. A 0.1μF disc or 1μF solid tantalum on the input is suitable input by passing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used byt the above values will eliminate the possibility of problems.

The adjustment terminal can be bypassed to ground on the LM338 to improve ripple rejection. This bypass capacitor prevents ripple form being amplified as the output voltage is increased. With a 10μF bypass capacitor 75dB ripple rejection is obtainable at any output level. Increases over 20μF do not appreciably improve the ripple rejection at frequencies above 120Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

In general, the best type of capacitors to use are solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25μF in aluminum electrolytic to equal 1μF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies, but some types have a large decrease in capacitance at frequencies around 0.5MHz. For this reason, 0.01μF disc may seem to work better than a 0.1μF disc as a bypass.

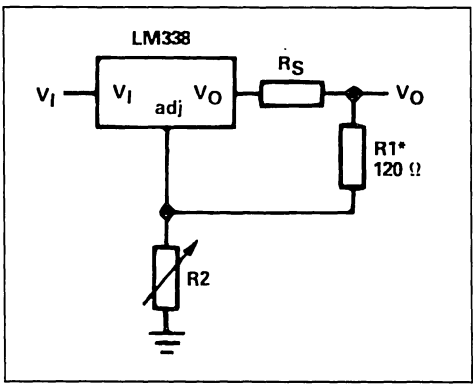
Although the LM338 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500pF and 5000pF. A 1μF solid tantalum (or 25μF aluminium electrolytic) on the output swamps this effect and insures stability.

LOAD REGULATION

The LM338 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05Ω x I_L. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

Figure 2 shows the effect of resistance between the regulator and 140Ω set resistor.

Figure 2 : Regulator with Line Resistance in Output Lead.



With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using 2 separate leads to the case. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

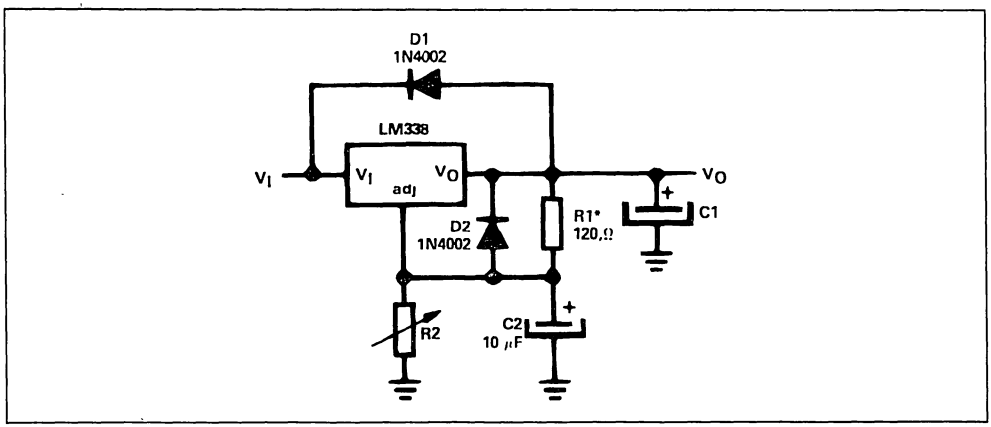
PROTECTION DIODES

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 20μF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

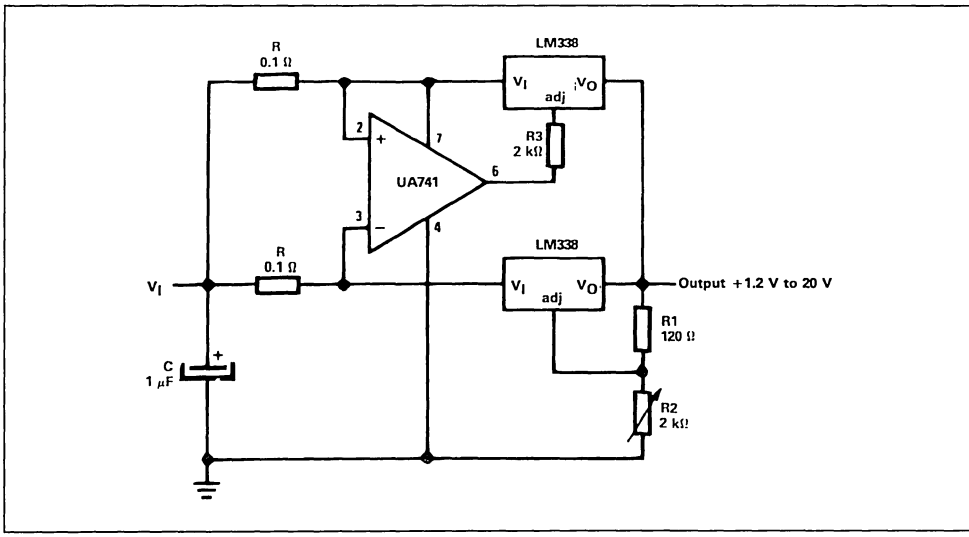
When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_I. In the LM338 this discharge path is through a large junction that is able to sustain 25A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 100μF or less at output of 15V or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when either the input or output is shorted. Internal to the LM338 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10μF capacitance. Figure 3 shows an LM338 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.

Figure 3 : Regulator with Protection Diodes.

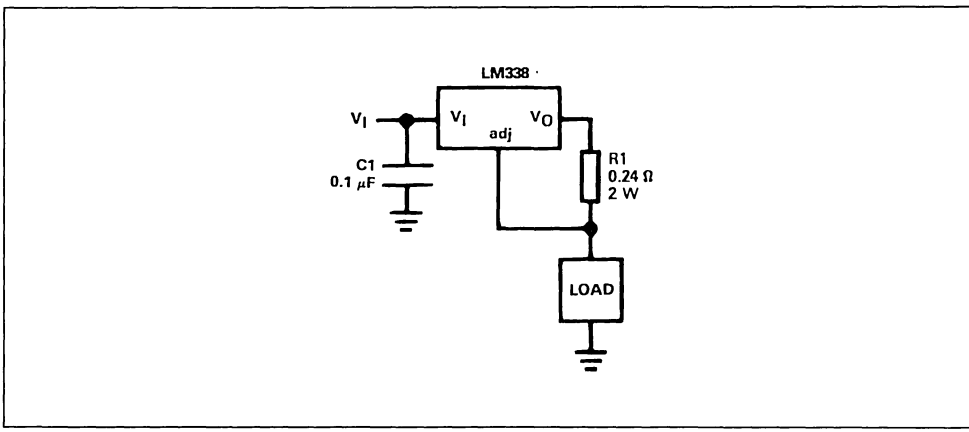


10A REGULATOR



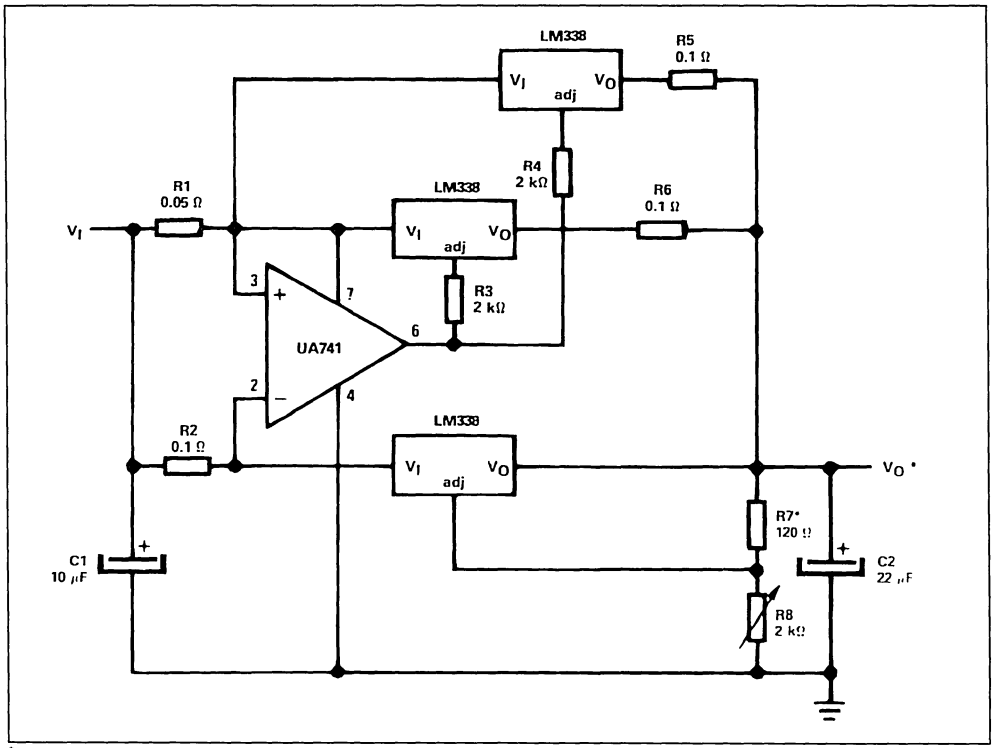
* Minimum load – 100mA
$V_I \geq 10V$
$V_O \geq 3V$
$V_I - V_O \geq 3.5V$

5A CURRENT REGULATOR



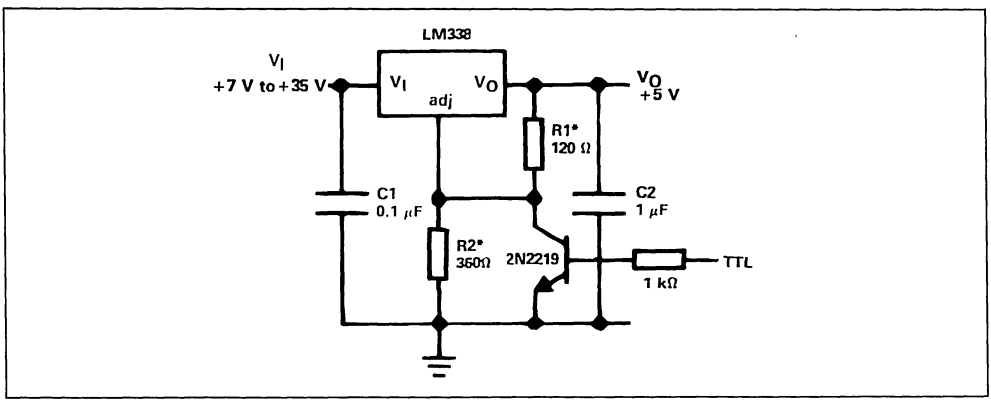
* Minimum load – 100mA
$V_I \geq 10V$
$V_O \geq 3V$
$V_I - V_O \geq 3.5V$

15A REGULATOR



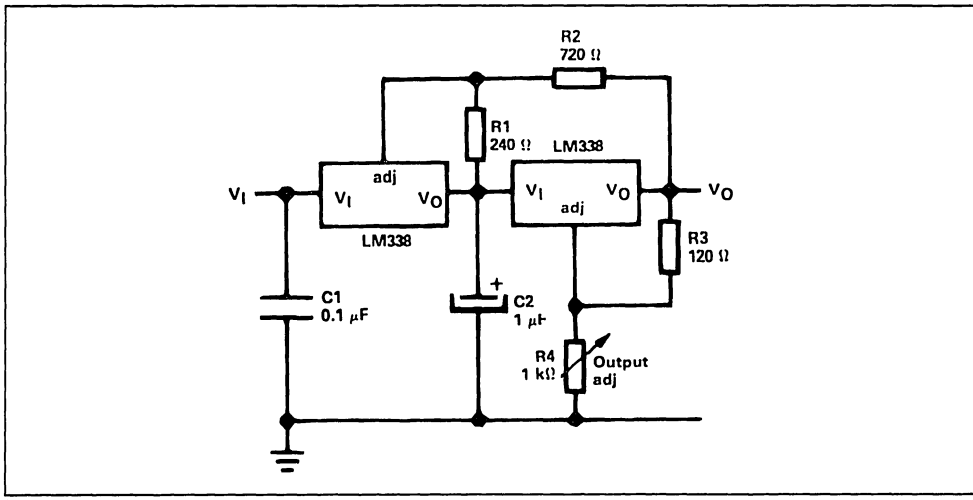
* Minimum load – 100mA
$V_I \geq +10V$
$V_O \geq +3V$
$V_I - V_O \geq +4V$

5V LOGIC REGULATOR WITH ELECTRONIC SHUTDOWN**



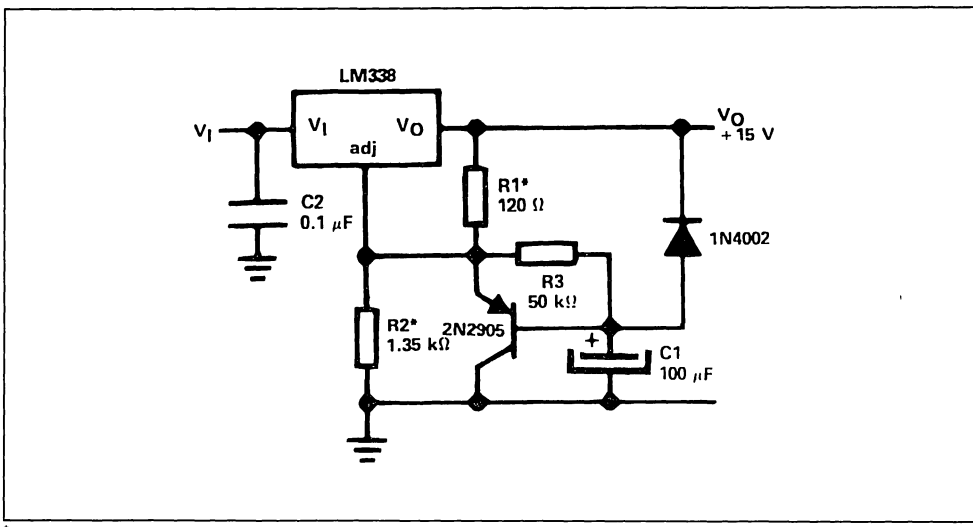
* R1 = 240Ω for LM138 or LM238
* R2 = 720Ω for LM138 or LM238
* * Minimum output ≈ +1.2V

TRACKING PREREGULATOR



* R1 = 240Ω for LM138 or LM238
* R2 = 720Ω for LM138 or LM238
* * Minimum output ≈ + 1.2V

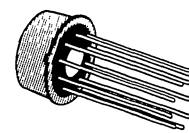
SLOW TURN-ON 15V REGULATOR



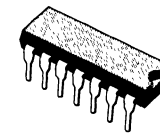
* R1 = 240Ω
* R2 = 2.7kΩ } for LM138 and LM238

HIGH PRECISION VOLTAGE REGULATOR

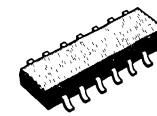
- INPUT VOLTAGE UP TO 40V
- OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 37V
- POSITIVE OR NEGATIVE SUPPLY OPERATION
- SERIES, SHUNT, SWITCHING OR FLOATING OPERATION
- OUTPUT CURRENT TO 150mA WITHOUT EXTERNAL PASS TRANSISTOR
- ADJUSTABLE CURRENT LIMITING



TO-100



DIP-14
(Ceramic and Plastic)

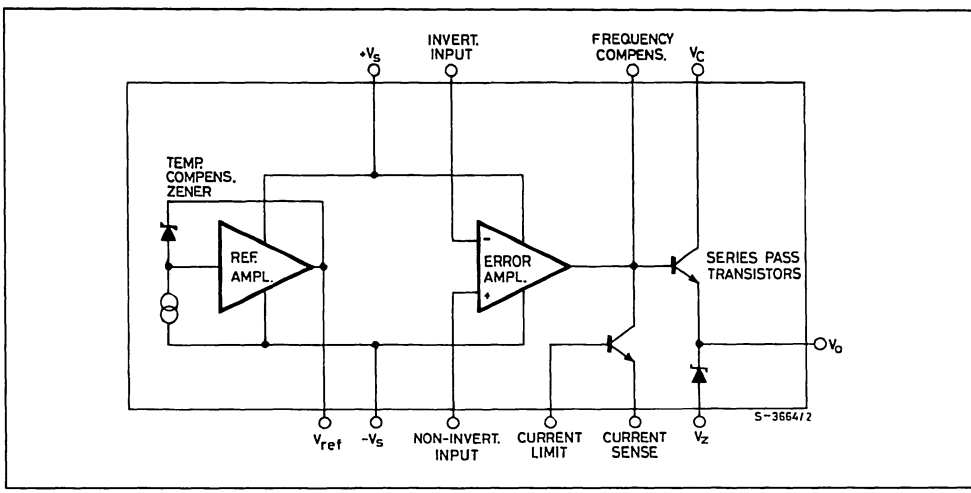


SO-14

DESCRIPTION

The LM723 is a monolithic integrated programmable voltage regulator, assembled in 14-lead dual in-line plastic and ceramic package, 10-lead Metal Can (TO-100 type) and SO-14 micropackage. The circuit provides internal current limiting. When the output current excedes 150mA an external NPN or PNP pass element may be used. Provisions are made for adjustable current limiting and remote shut-down.

BLOCK DIAGRAM



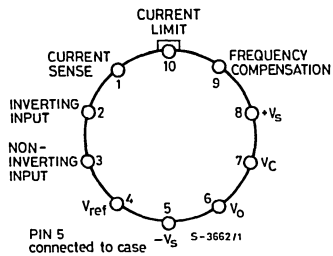
ABSOLUTE MAXIMUM RATINGS

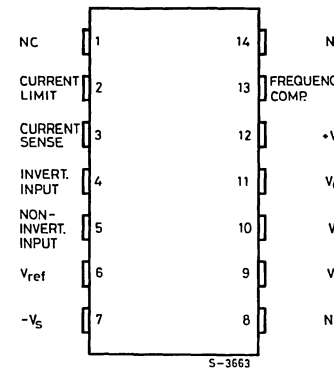
Symbol	Parameter	LM723	LM723C	Unit
V_I	Input Voltage	40	40	V
ΔV_{I-O}	Dropout Voltage	40	40	V
I_O	Output Current	150	150	mA
I_{ref}	Current from V_{ref}	15	25	mA
T_{op}	Operating Temperature	– 55 to 125	0 to 70	°C
T_{stg}	Storage Temperature	– 65 to 150	– 65 to 150	°C
T_J	Junction Temperature	150	125	°C

THERMAL DATA

Symbol	Parameter		Plastic DIP-14	Ceramic DIP-14	TO-100	SO-14	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	200	150	155	165	°C/W

PIN CONNECTION (top views)





ORDER CODES

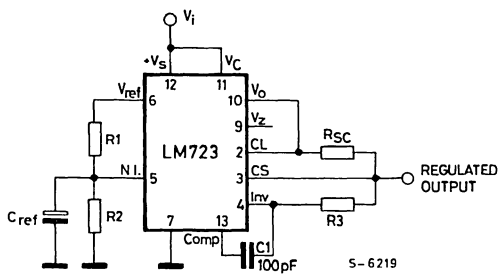
Type	TO-100	Ceramic DIP-14	Plastic DIP-14	SO-14
LM723	LM723H	LM723J		
LM723C	LM723CH	LM723CJ	LM723CN	LM723CD

ELECTRICAL CHARACTERISTICS (refer to the test circuit, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	LM723C			LM723			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$\frac{\Delta V_o}{\Delta V_i}$	Line Regulation	V_i = 12 to 15V V_i = 12 to 40V		0.01 0.1	0.1 0.5		0.01 0.02	0.1 0.2	%
		V_i = 12 to 15V ; $T_{min} \le T_{amb} \le T_{max}$			0.3			0.3	
$\frac{\Delta V_o}{V_o}$	Load Regulation	I_o = 1 to 50mA		0.03	0.2		0.03	0.15	%
		$T_{min} \le T_{amb} \le T_{max}$ I_o = 1 to 10mA			0.6			0.6	
V_{REF}	Reference Voltage	I_{ref} = 160µA	6.8	7.15	7.5	6.95	7.15	7.35	V
SVR	Ripple Rejection	f = 100Hz to 10KHz C_{ref} = 0 C_{ref} = 5µF		 74 86			 74 86		 dB dB
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift				150			150	$\frac{ppm}{°C}$
I_{sc}	Short Circuit Current Limiting	R_{sc} = 10Ω V_o = 0		65			65		mA
V_i	Input Voltage Range		9.5		40	9.5		40	V
V_o	Output Voltage Range		2		37	2		37	V
V_i-V_o			3		38	3		38	V
I_d	Quiescent Drain Current	I_o = 0 V_i = 30V		2.3	4		2.3	5	mA
	Long Term Stability			0.1			0.1		$\frac{\%}{1000\ hrs}$
e_N	Output Noise Voltage	BW = 100Hz to 10KHz C_{ref} = 0 C_{ref} = 5µF		 20 2.5			 20 2.5		 µV µV
V_z	Output Zener Voltage (for plastic package only)	I_z = 1mA	6.9		7.7				V

Note : T_{min} = 0°C (LM723C) ; 125°C (LM723)
T_{max} = 70°C (LM723C) ; – 55°C (LM723).

TEST CIRCUIT (pin configuration relative to the plastic package)



V_i = 12V
V_o = 5V
I_o = 1mA
$R_1/R_2 \le 10K\Omega$

Figure 1 : Maximum Output Current vs. Voltage Drop.

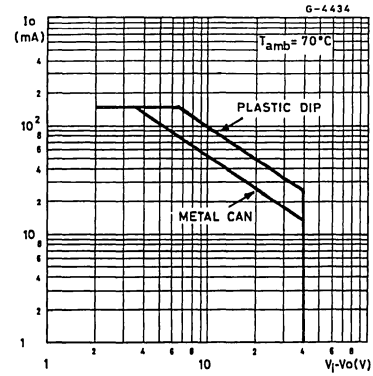


Figure 2 : Current Limiting Characteristics.

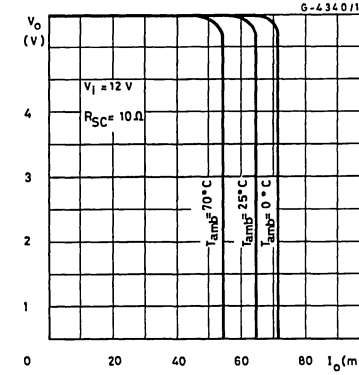


Figure 3 : Current Limiting Characteristics vs. Junction Temperature.

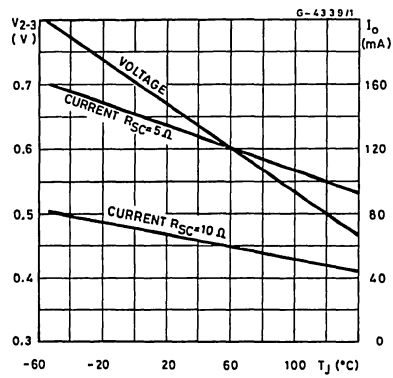


Figure 4 : Load Regulation Characteristics without Current Limiting.

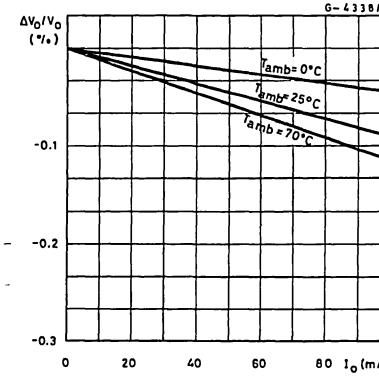


Figure 5 : Load Regulation Characteristics with Current Limiting.

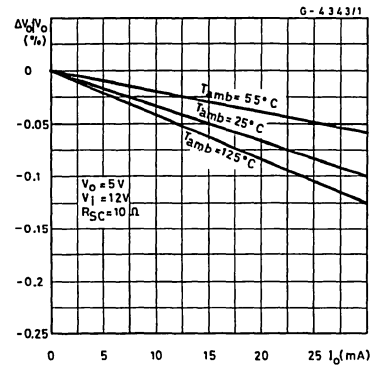


Figure 6 : Load Regulation Characteristics with Current Limiting

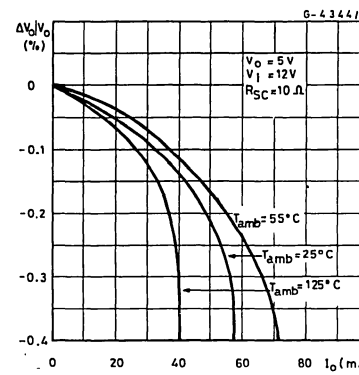


Figure 7 : Line Regulation vs. Voltage Drop.

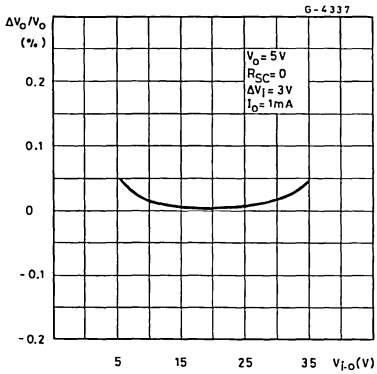


Figure 8 : Load Regulation vs. Voltage Drop.

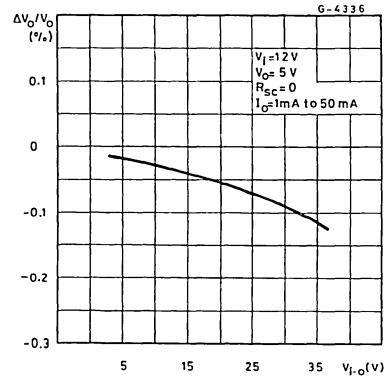


Figure 9 : Quiescent Drain Current vs. Input Voltage.

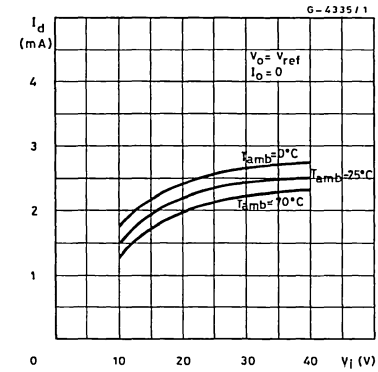


Figure 10 : Line Transient Response.

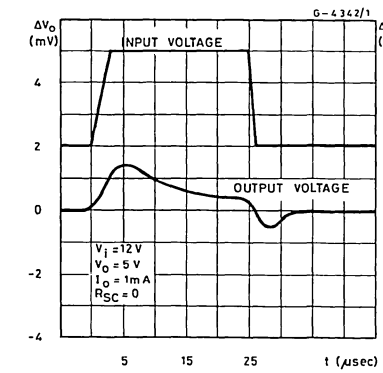


Figure 11 : Load Transient Response.

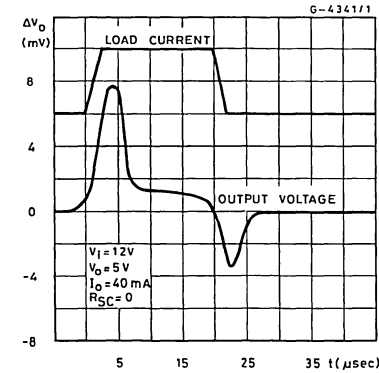


Figure 12 : Output Impedance vs. Frequency.

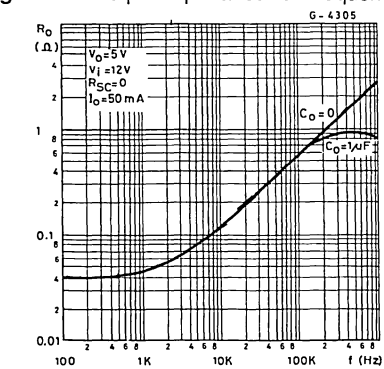


Table 1 : Resistor Values (KΩ) for Standard Output Voltages.

Output Voltage	Applicable Figures	Fixed Output ± 5%		Output Adjustable ± 10% (°)			Output Voltage	Applicable Figures	Fixed Output ± 5%		Output Adjustable ± 10% (°)		
		R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+ 3	13, 16	4.12	3.01	1.8	0.5	1.2	+ 100						
+ 5	13, 16	2.15	4.99	0.75	0.5	2.2	+ 250						
+ 6	13, 16	1.15	6.04	0.5	0.5	2.7	− 6(°°)	15	3.57	2.43	1.2	0.5	0.75
+ 9	14, 16	1.87	7.15	0.75	1	2.7	− 9	15	3.48	5.36	1.2	0.5	2
+ 12	14, 16	4.87	7.15	2	1	3	− 12	15	3.57	8.45	1.2	0.5	3.3
+ 15	14, 16	7.87	7.15	3.3	1	3	− 15	15	3.65	11.5	1.2	0.5	4.3
+ 28	14, 16	21	7.15	5.6	1	2	− 28	15	3.57	24.3	1.2	0.5	10

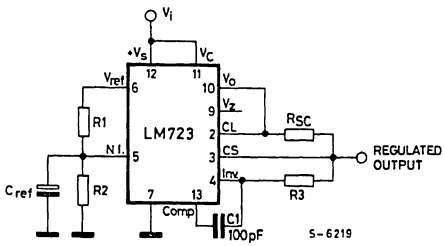
Note : (*) Replace R_1/R_2 divider with the circuit of fig. 24.
(**) V^+ must be connected to a + 3V or greater supply.

Table 2 : Formulae for Intermediate Output Voltages.

Outputs from + 2 to + 7 Volts Fig. 13, 16 $V_O = [V_{ref} \times \frac{R_2}{R_1 + R_2}]$		Current Limiting $I_{LIMIT} = \frac{V_{SENSE}}{R_{sc}}$
Outputs from + 7 to + 37 Volts Fig. 14, 16, $V_O = [V_{ref} \times \frac{R_1 + R_2}{R_2}]$	Output from − 6 to − 250 Volts Fig. 15, 20 $V_O = [\frac{V_{ref}}{2} \times \frac{R_1 + R_2}{R_1}]$; $R_3 = R_4$	Foldback Current Limiting $I_{KNEE} = [\frac{V_O R_3}{R_{sc} R_4} + \frac{V_{SENSE}(R_3 + R_4)}{R_{sc} R_4}]$ $I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}]$

APPLICATION INFORMATION (pin numbers relative to the plastic package).

Figure 13 : Basic Low Voltage Regulator (V_o = 2 to 7V).



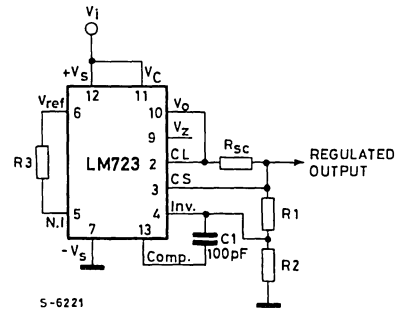
Note : $R3 = \frac{R1 \cdot R2}{R1 + R2}$ for minimum temperature drift

R3 may be eliminated for minimum component count.

Typical performance

Regulated Output Voltage	5V
Line Regulation (ΔV_i = 3V)	0.5mV
Load Regulation (ΔI_o = 50mA)	1.5mV

Figure 14 : Basic High Voltage Regulator (V_o = 7 to 37V).



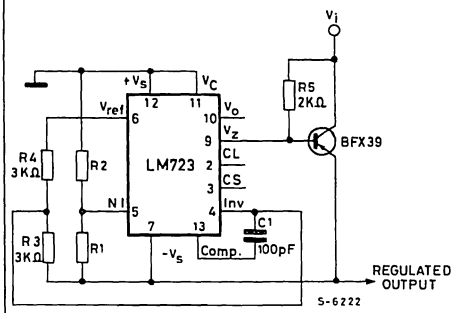
Note : $R3 = \frac{R1 \cdot R2}{R1 + R2}$ for minimum temperature drift

R3 may be eliminated for minimum component count.

Typical performance

Regulated Output Voltage	15V
Line Regulation (ΔV_i = 3V)	1.5mV
Load Regulation (ΔI_o = 50mA)	4.5mV

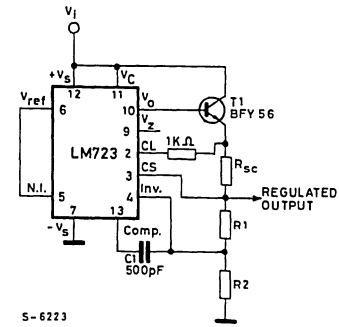
Figure 15 : Negative Voltage Regulator.



Typical performance

Regulated Output Voltage	15V
Line Regulation (ΔV_i = 3V)	1mV
Load Regulation (ΔI_o = 100mA)	2mV

Figure 16 : Positive Voltage Regulator (external NPN Pass Transistor).

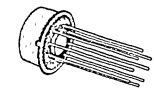


Typical performance

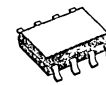
Regulated Output Voltage	+ 15V
Line Regulation (ΔV_i = 3V)	1.5mV
Load Regulation (ΔI_o = 1A)	15mV

HIGH PERFORMANCE DUAL OPERATIONAL AMPLIFIER

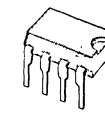
- SINGLE OR SPLIT SUPPLY OPERATION
- LOW POWER CONSUMPTION
- SHORT CIRCUIT PROTECTION
- LOW DISTORTION, LOW NOISE
- HIGH GAIN-BANDWIDTH PRODUCT
- HIGH CHANNEL SEPARATION



TO-99



SO-8J



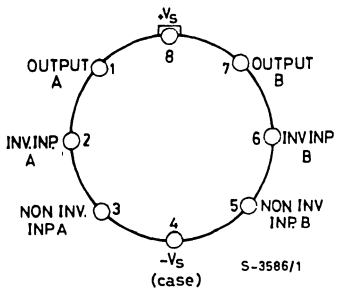
MINIDIP
(Plastic)

DESCRIPTION

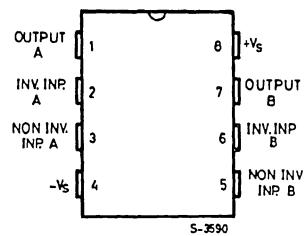
The LS204 is a high performance dual operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth products.

The circuit presents very stable electrical characteristics over the entire supply voltage range, and it particularly intended for professional and telecom applications (active filters, etc).

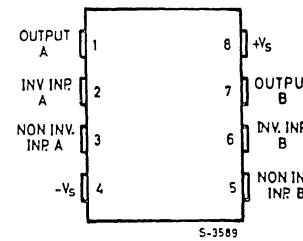
PIN CONNECTIONS (top views)



TO-99



Minidip

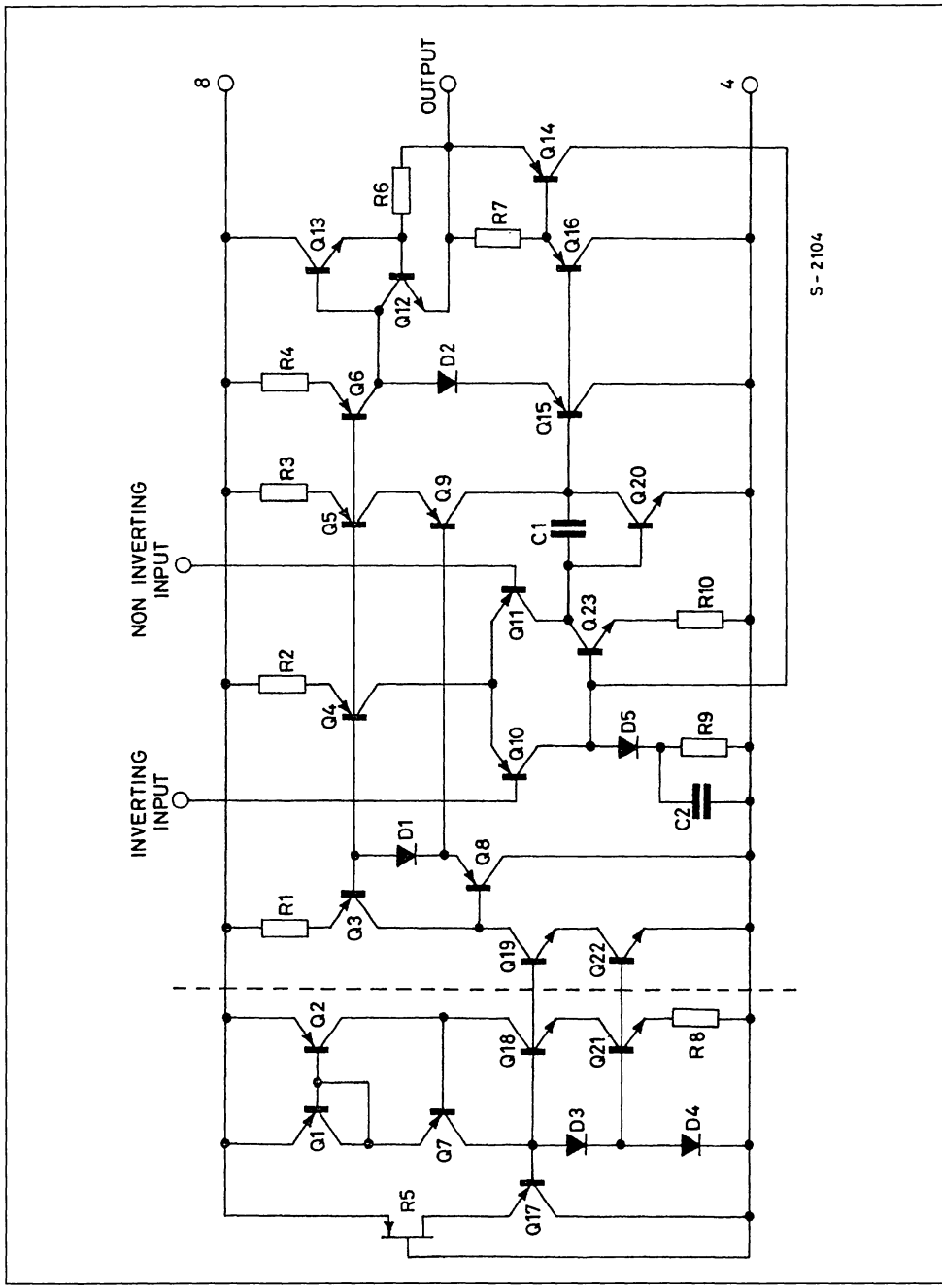


SO-8

ORDER CODES

Type	TO-99	Minidip	SO-8
LS204	LS204TB	–	LS204M
LS204A	LS204ATB	–	–
LS204C	LS204CTB	LS204CB	LS204CM

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		TO-99	Minidip	µPackage
V_s	Supply Voltage		± 18V		
V_i	Input Voltage		± V_s		
V_i	Differential Input Voltage		± (V_s – 1)		
T_{op}	Operating Temperature for	**LS204** **LS204A** **LS204C**	– 25 to 85°C – 55 to 125°C 0 to 70°C		
P_{tot}	Power Dissipation at T_{amb} = 70°C		520mW	665mW	400mW
T_j	Junction Temperature		150°C	150°C	150°C
T_{stg}	Storage Temperature		– 65 to 150°C	– 55 to 150°C	– 55 to 150°C

THERMAL DATA

			TO-99	Minidip	SO-8J
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	155°C/W	120°C/W	200°C/W

ELECTRICAL CHARACTERISTICS (V_s = ± 15V, T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	LS204/LS204A			LS204C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_s	Supply Current			0.7	1.2		0.8	1.5	mA
I_b	Input Bias Current			50	150		100	300	nA
		$T_{min} < T_{op} < T_{max}$			300			700	nA
R_i	Input Resistance	f = 1KHz		1			0.5		MΩ
V_{os}	Input Offset Voltage	$R_g \leq 10K\Omega$		0.5	2.5		0.5	3.5	mV
		$R_g \leq 10K\Omega$ $T_{min} < T_{op} < T_{max}$			3.5			5	mV
$\frac{\Delta V_{os}}{\Delta T}$	Input Offset Voltage Drift	R_g = 10KΩ $T_{min} < T_{op} < T_{max}$		5			5		µV/°C
I_{os}	Input Offset Current			5	20		12	50	nA
		$T_{min} < T_{op} < T_{max}$			40			100	nA
$\frac{\Delta I_{os}}{\Delta T}$	Input Offset Current Drift	$T_{min} < T_{op} < T_{max}$		0.08			0.1		$\frac{nA}{°C}$
I_{sc}	Output Short Circuit Current			23			23		mA
G_v	Large Signal Open Loop Voltage Gain	$T_{min} < T_{op} < T_{max}$ R_L = 2KΩ V_s = ± 15V V_s = ± 4V	90	100 95		86	100 95		dB
B	Gain-bandwidth Product	f = 20KHz	1.8	3		1.5	2.5		MHz
e_N	Total Input Noise Voltage	f = 1KHz R_g = 50Ω R_g = 1KΩ R_g = 10KΩ		8 10 18	15		10 12 20		$\frac{nV}{\sqrt{Hz}}$

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	LS204/LS204A			LS204C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
d	Distortion	G_V = 20dB R_L = 2KΩ V_o = 2 V_{PP} f = 1KHZ		0.03	0.1		0.03	0.1	%
V_o	DC Output Voltage Swing	R_L = 2KΩ V_s = ± 15V V_s = ± 4V	± 13	± 3		± 13	± 3		V
V_o	Large Signal Voltage Swing	R_L = 10KΩ f = 10KHz		28			28		V_{pp}
SR	Slew Rate	Unity Gain R_L = 2KΩ	0.8	1.5			1		V/µs
CMR	Common Mode Rejection	V_i = 10V $T_{min} < T_{op} < T_{max}$	90			86			dB
SVR	Supply Voltage Rejection	V_i = 1V f = 100Hz $T_{min} < T_{op} < T_{max}$	90			86			dB
CS	Channel Separation	f = 1KHz 100	120			120			dB

Note :

Temp.	LS204	LS204A	LS204C
$T_{min.}$	– 25°C	– 55°C	0°C
$T_{max.}$	+ 85°C	+ 125°C	+ 70°C

Figure 1: Supply Current vs. Supply Voltage.

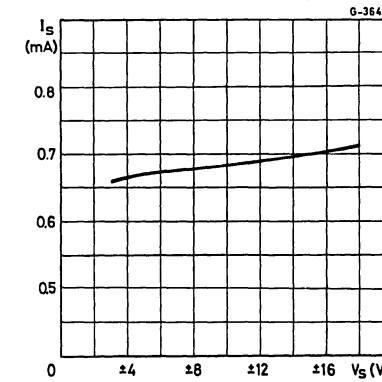


Figure 2 : Supply Current vs. Ambient Temperature.

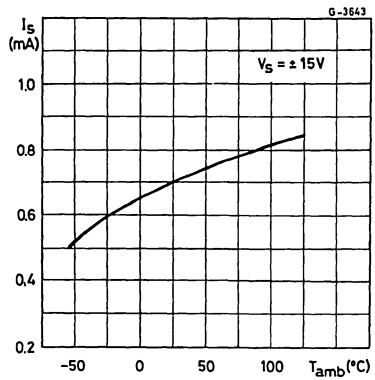


Figure 3 : Output Short Circuit Current vs. Ambient Temperature.

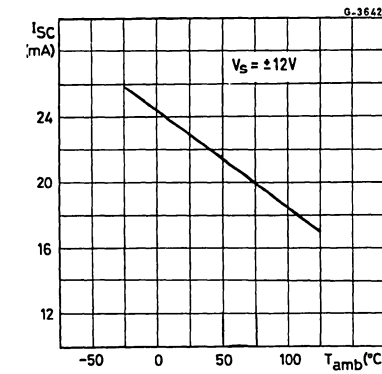


Figure 4: Open Loop Frequency and Phase Response.

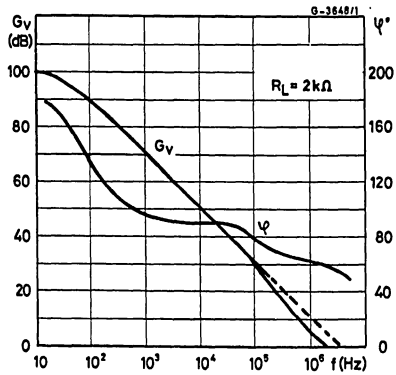


Figure 5: Open Loop Gain vs. Ambient Temperature.

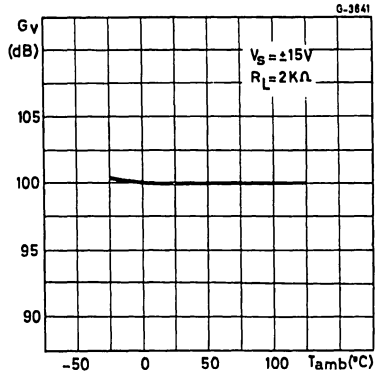


Figure 6 : Supply Voltage Rejection vs. Frequency.

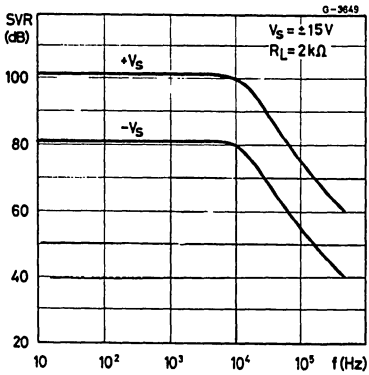


Figure 7 : Large Signal Frequency Response.

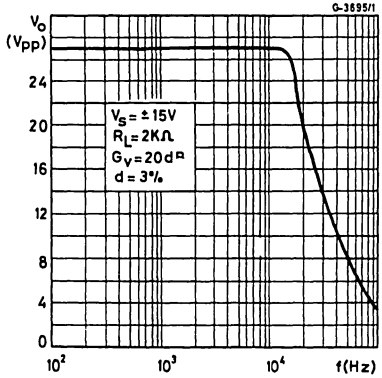


Figure 8 : Output Voltage Swing vs. Load Resistance.

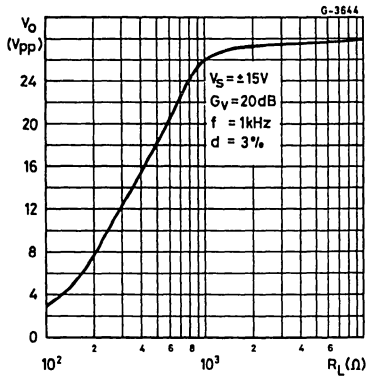
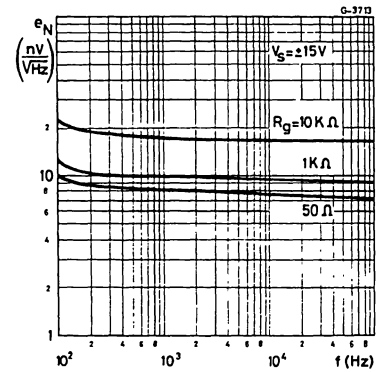


Figure 9 : Total Input Noise vs. Frequency.



APPLICATION INFORMATION

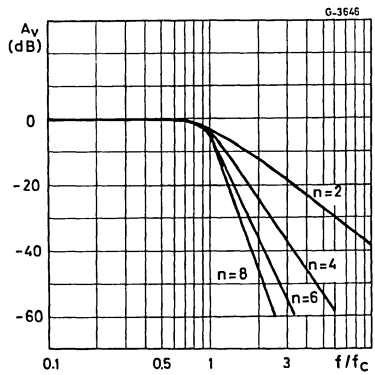
Active low-pass filter :

BUTTERWORTH

The Butterworth is a "maximally flat" amplitude response filter. Butterworth filters are used for filtering signals in data acquisition systems to prevent aliasing errors in sampled-data applications and for general purpose low-pass filtering.
The cutoff frequency, f_c, is the frequency at which the amplitude response is down 3 dB. The attenuation rate beyond the cutoff frequency is n6 dB per octave of frequency where n is the order (number of poles) of the filter.
Other characteristics :

- Flattest possible amplitude response.
- Excellent gain accuracy at low frequency end of passband.

Figure 10 : Amplitude Response.



BESSEL

The Bessel is a type of "linear phase" filter. Because of their linear phase characteristics, these filters approximate a constant time delay over a limited frequency range. Bessel filters pass transient waveforms with a minimum of distortion. They are also used to provide time delays for low pass filtering of modulated waveforms and as a "running average" type filter.

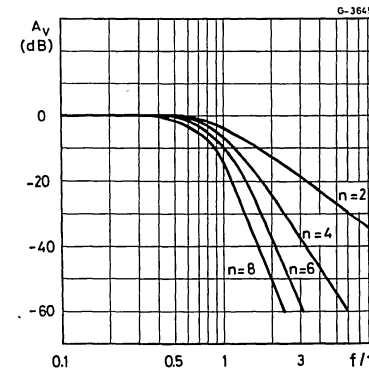
The maximum phase shift is $\frac{-n\pi}{2}$ radians where n is the order (number of poles) of the filter. The cutoff frequency, fc, is defined as the frequency at which the phase shift is one half of this value. For accurate delay, the cutoff frequency should be twice the maximum signal frequency. The following table can be used to obtain the – 3dB frequency of the filter.

	2 pole	4 Pole	6 Pole	8 Pole
– 3dB Frequency	0.77 f_c	0.67 f_c	0.57 f_c	0.50 f_c

Other characteristics :

- Selectivity not as great as Chebyschev or Butterworth.
- Very little overshoot response to step inputs.
- Fast rise time.

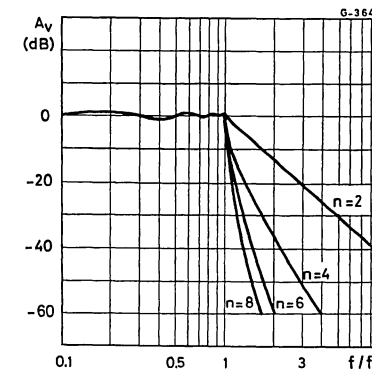
Figure 11 : Amplitude Response.



CHEBYSCHEV

Chebyschev filters have greater selectivity than either Bessel or Butterworth at the expense of ripple in the passband.

Figure 12 : Amplitude Response (± 1dB ripple).



APPLICATION INFORMATION (continued)

Chebyschev filters are normally designed with peak-to-peak ripple values from 0.2 dB to 2 dB.

Increased ripple in the passband allows increased attenuation above the cutoff frequency.
The cutoff frequency is defined as the frequency at which the amplitude response passes through the specified maximum ripple band and enters the stop band.

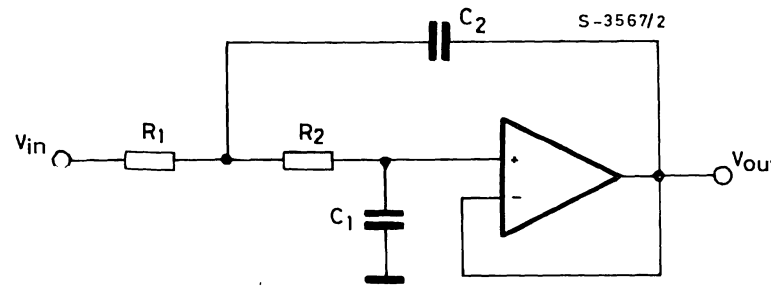
Other characteristics :
- Greater selectivity
- Very nonlinear phase response
- High overshoot response to step inputs

The table below shows the typical overshoot and settling time response of the low pass filters to a step input.

	Number of Poles	Peak Overshoot	Settling Time (% of final value)		
		% Overshoot	± 1%	± 0 .1%	± 0.01%
Butterworth	2	4	$1.1/f_c$sec.	$1.7/f_c$sec.	$1.9/f_c$sec.
	4	11	$1.7/f_c$	$2.8/f_c$	$3.8/f_c$
	6	14	$2.4/f_c$	$3.9/f_c$	$5.0/f_c$
	8	16	$3.1/f_c$	$5.1/f_c$	$7.1/f_c$
Bessel	2	0.4	$0.8/f_c$	$1.4/f_c$	$1.7/f_c$
	4	0.8	$1.0/f_c$	$1.8/f_c$	$2.4/f_c$
	6	0.6	$1.3/f_c$	$2.1/f_c$	$2.7/f_c$
	8	0.3	$1.6/f_c$	$2.3/f_c$	$3.2/f_c$
Chebyschev (ripple ± 0.25dB)	2	11	$1.1/f_c$	$1.6/f_c$	–
	4	18	$3.0/f_c$	$5.4/f_c$	–
	6	21	$5.9/f_c$	$10.4/f_c$	–
	8	23	$8.4/f_c$	$16.4/f_c$	–
Chebyschev (ripple ± 1dB)	2	21	$1.6/f_c$	$2.7/f_c$	–
	4	28	$4.8/f_c$	$8.4/f_c$	–
	6	32	$8.2/f_c$	$16.3/f_c$	–
	8	34	$11.6/f_c$	$24.8/f_c$	–

Design of 2nd order active low pass filter (Sallen and Key configuration unity gain-op-amp).

Figure 13 : Filter Configuration.



$$\frac{V_o}{V_i} = \frac{1}{1 + 2\xi \frac{S}{\omega_C} + \frac{S^2}{\omega_C^2}}$$

Where :

$\omega_C = 2\pi f_c$ with f_c = cutoff frequency

ξ = damping factor.

APPLICATION INFORMATION (continued)

Three parameters are needed to characterise the frequency and phase response of a 2nd order active filter : the gain (G_v), the damping factor (ξ) or the Q-factor ($Q = (2\xi)^{-1}$), and the cutoff frequency (f_c).

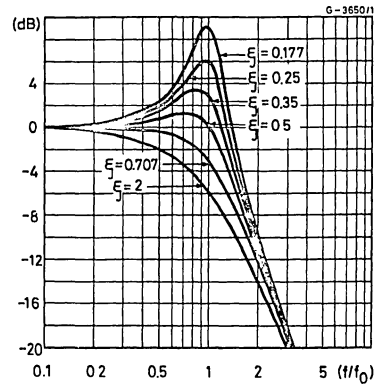
The higher order responses are obtained wit a series of 2nd order sections. A simple RC section is introduced when an odd filter is required.

The choice of 'ξ' (or Q-factor) determines the filter response (see table).

Table 1.

Filter Response	ξ	Q	Cutoff Frequency f_c
Bessel	$\frac{\sqrt{3}}{2}$	$\frac{1}{\sqrt{3}}$	Frequency at which Phase Shift is – 90°C
Butterworth	$\frac{\sqrt{2}}{2}$	$\frac{1}{\sqrt{2}}$	Frequency at Which $G_v = -3dB$
Chebyschev	$< \frac{\sqrt{2}}{2}$	$> \frac{1}{\sqrt{2}}$	Frequency at which the amplitude response passes through specified max. ripple band and enters the stop band.

Figure 14 : Filter Response vs. Damping Factor.



Fixed R = R1 = R2, we have (see fig. 13)

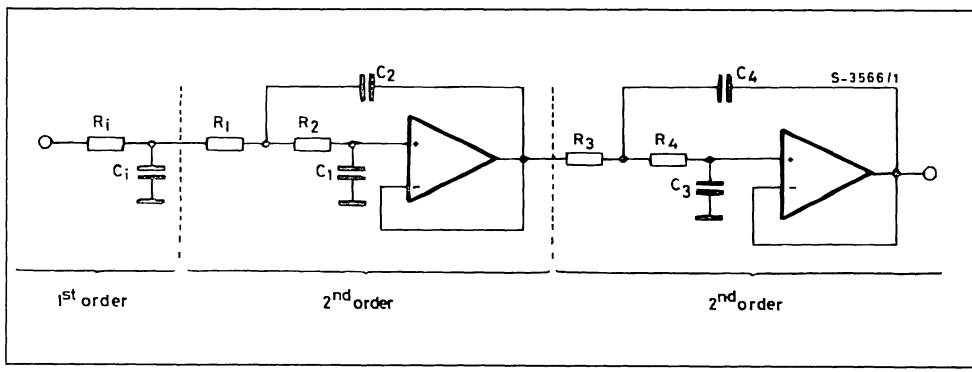
$$C_1 = \frac{1}{R}\,\frac{\xi}{\omega_c}$$

$$C_2 = \frac{1}{R}\,\frac{1}{\xi\omega_c}$$

The diagram of fig.14 shows the amplitude response for different values of damping factor ξ in

EXAMPLE

Figure 15 : 5th Order Low Pass Filter (Butterworth) with Unity Gain Configuration.



SGS-THOMSON MICROELECTRONICS

APPLICATION INFORMATION (continued)

In the circuit of fig. 15, for f_c = 3.4 KHz and $R_i = R_1 = R_2 = R_3 = R_4$ = 10 KΩ, we obtain :

$$C_i = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33\text{nF}$$

$$C_1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97\text{nF}$$

$$C_2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20\text{nF}$$

$$C_3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45\text{nF}$$

$$C_4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 15.14\text{nF}$$

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

The same method, referring to Tab. II and fig. 16, is used to design high-pass filter. In this case the damping factor is found by taking the reciprocal of the numbers in Tab. II. For f_c = 5 KHz and $C_i = C_1 = C_2 = C_3 = C_4$ = 1 nF we obtain :

$$R_i = \frac{1}{1.354} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 23.5\text{K}\Omega$$

$$R_1 = \frac{1}{0.421} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 75.6\text{K}\Omega$$

$$R_2 = \frac{1}{1.753} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 18.2\text{K}\Omega$$

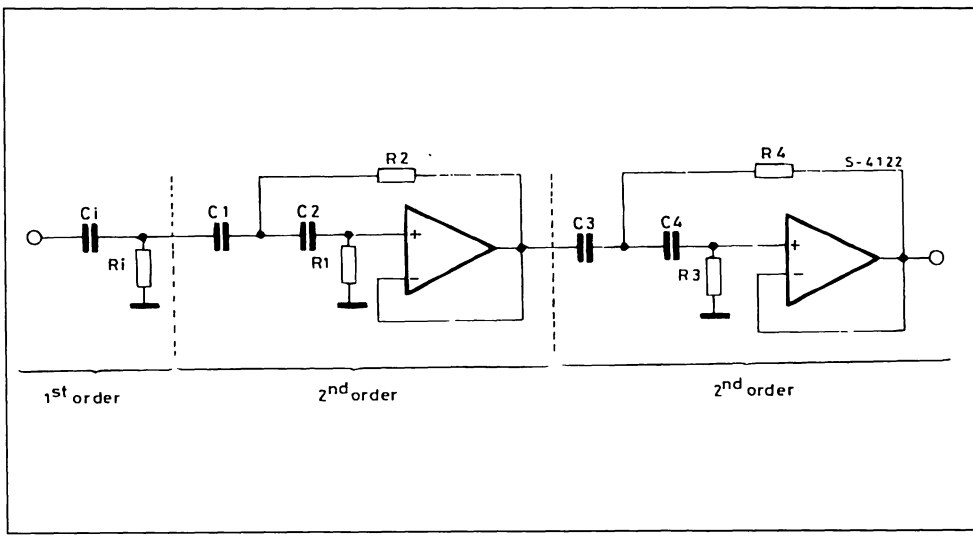
$$R_3 = \frac{1}{0.309} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 103\text{K}\Omega$$

$$R_4 = \frac{1}{3.325} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 9.6\text{K}\Omega$$

Table 2 : Damping Factor for Low-pass Butterworth Filters.

Order	C_I	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
2		0.707	1.41						
3	1.392	0.202	3.54						
4		0.92	1.08	0.38	2.61				
5	1.354	0.421	1.75	0.309	3.235				
6		0.966	1.035	0.707	1.414	0.259	3.86		
7	1.336	0.488	1.53	0.623	1.604	0.222	4.49		
8		0.98	1.02	0.83	1.20	0.556	1.80	0.195	5.125

Figure 16 : 5_{th} Order High-pass Filter (Butterworth) with Unity Gain Configuration.

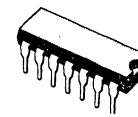


SGS-THOMSON MICROELECTRONICS

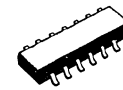
LS404

HIGH PERFORMANCE QUAD OPERATIONAL AMPLIFIERS

- SINGLE OR SPLIT SUPPLY OPERATION
- VERY LOW POWER CONSUMPTION
- SHORT CIRCUIT PROTECTION
- LOW DISTORTION, LOW NOISE
- HIGH GAIN-BANDWIDTH PRODUCT
- HIGH CHANNEL SEPARATION



DIP14
(Plastic 0.25)



SO-14J

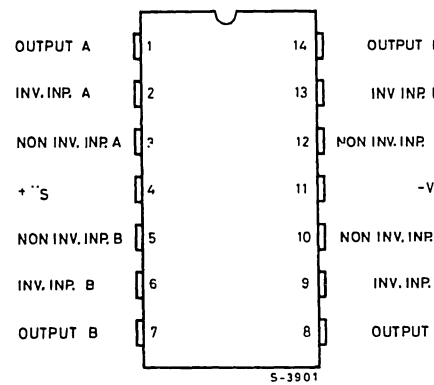
DESCRIPTION

The LS404 is a high performance quad operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth product. The circuit presents very stable electrical characteristics over the entire supply voltage range, and it is particularly intended for professional and telecom applications (active filters, etc.).

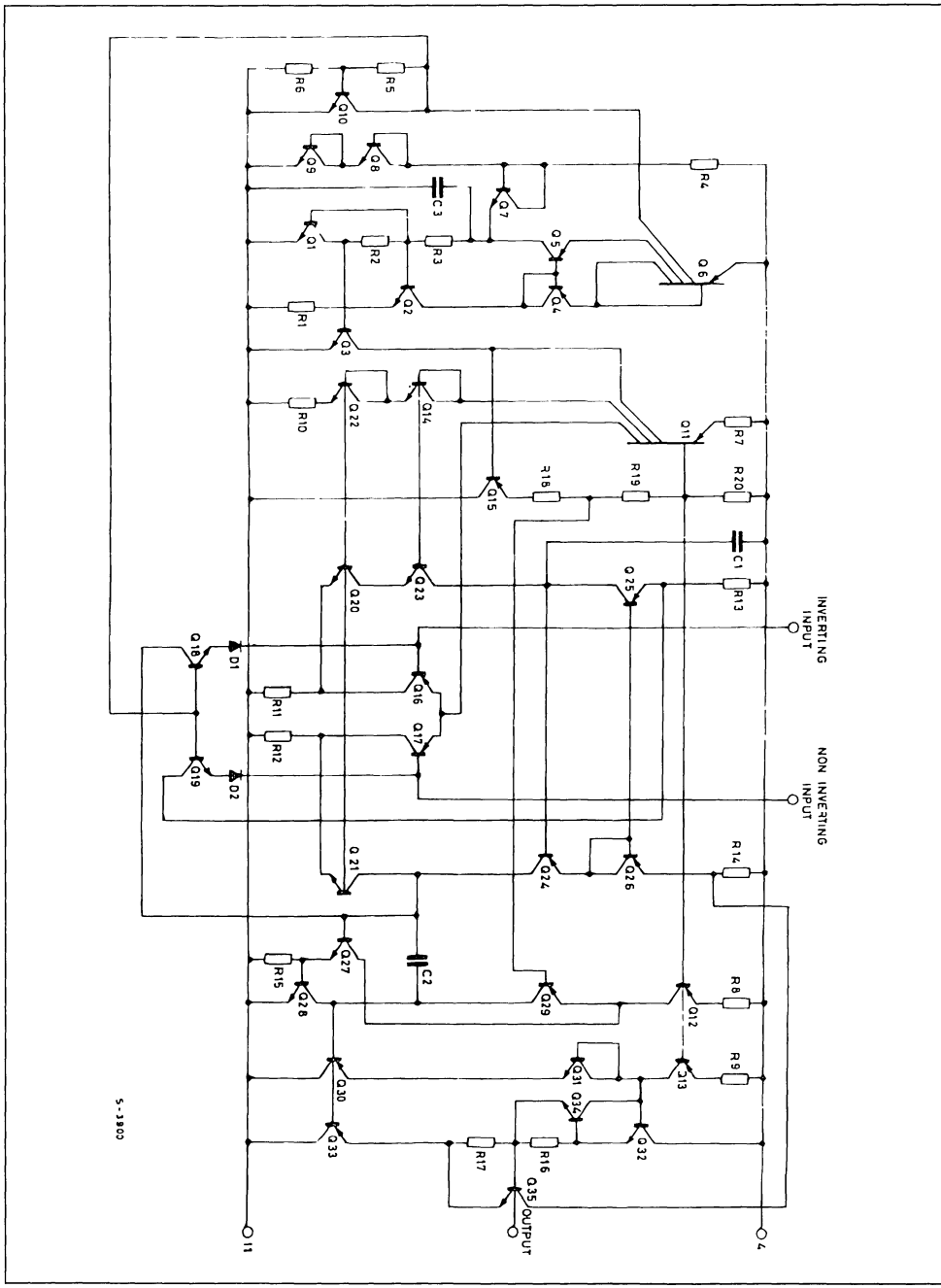
The patented input stage circuit allows small input signal swings below the negative supply voltage and prevents phase inversion when the input is over driven.

CONNECTION DIAGRAM AND ORDERING NUMBERS (top view)

Type	DIP 14	SO-14
LS404 LS404C	– LS404CB	LS404D1 LS404CD1
LS 8404 LS8404C	– –	LS 8404M LS 89404CM



SCHEMATIC DIAGRAM (one section)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_s	Supply Voltage		± 18	V
V_i	Input Voltage	(positive) (negative)	+ V_s – V_s – 0.5	V
V_i	Differential Input Voltage		± (V_s – 1)	
T_{op}	Operating Temperature	**LS404** **LS404C**	– 25 to + 85 0 to + 70	°C °C
P_{tot}	Power Dissipation	(T_{amb} = 70°C)	400	mW
T_{stg}	Storage Temperature		– 55 to + 150	°C

THERMAL DATA

			DIP 14	SO–14 J
$R_{th j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	200°C/W	200°C/W

(*) Measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm).

ELECTRICAL CHARACTERISTICS (V_s = ± 12 V, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions		LS404			LS404C			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
I_s	Supply Current				1.3	2		1.5	3	mA
I_b	Input Bias Current				50	200		100	300	nA
R_i	Input Resistance	f = 1 KHz			0.7	2.5		0.5	5	MΩ
V_{os}	Input Offset Voltage	R_g = 10 KΩ			1			1		mV
$\frac{\Delta V_{os}}{\Delta T}$	Input Offset Voltage Drift	R_g = 10 KΩ $T_{min} < T_{op} < T_{max}$			5			5		µV/°C
I_{os}	Input Offset Current				10	40		20	80	nA
$\frac{\Delta I_{os}}{\Delta T}$	Input Offset Current Drift	$T_{min} < T_{op} < T_{max}$			0.08			0.1		$\frac{nA}{°C}$
I_{sc}	Output Short Circuit Current				23			23		mA
G_v	Large Signal Open Loop Voltage Gain	R_L = 2 KΩ	V_s = ± 12 V V_s = ± 4 V	90	100 95		86	100 95		dB
B	Gain-bandwidth Product	f = 20 KHz		1.8	3		1.5	2.5		MHz
e_N	Total Input Noise Voltage	f = 1 KHz R_g = 50 Ω R_g = 1 KΩ R_g = 10 KΩ			8 10 18	15		10 12 20		$\frac{nV}{\sqrt{Hz}}$
d	Distortion	Unity Gain R_L = 2 KΩ V_o = 2 V_{PP}	f = 1 KHz f = 20 KHz		0.01 0.03	0.04		0.01 0.03		%
V_o	DC Output Voltage Swing	R_L = 2 KΩ	V_s = ± 12 V V_s = ± 4 V	± 10	± 3		± 10	± 3		V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	LS404			LS404C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Large Signal Voltage Swing	f = 10 KHz R_L = 10 KΩ R_L = 1 KΩ		22 20			22 20		V_{pp}
SR	Slew Rate	Unity Gain R_L = 2 KΩ	0.8	1.5			1		V/μs
CMR	Common Mode Rejection	V_i = 10 V	90	94		80	90		dB
SVR	Supply Voltage Rejection	V_i = 1 V f = 100 Hz	90	94		86	90		dB
CS	Channel Separation	f = 1 KHz	100	120			120		dB

Figure 1: Supply Current vs. Supply Voltage.

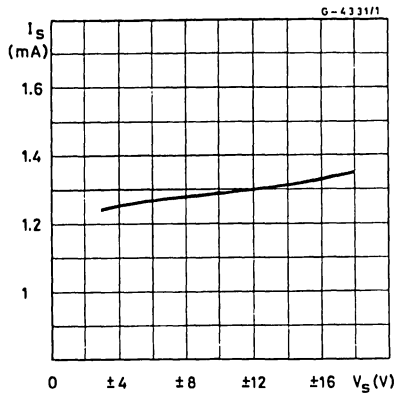


Figure 2 : Supply Current vs. Ambient Temperature.

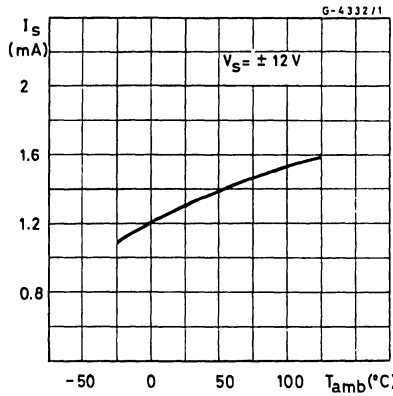


Figure 3 : Output Short Circuit Current vs. Ambient Temperature.

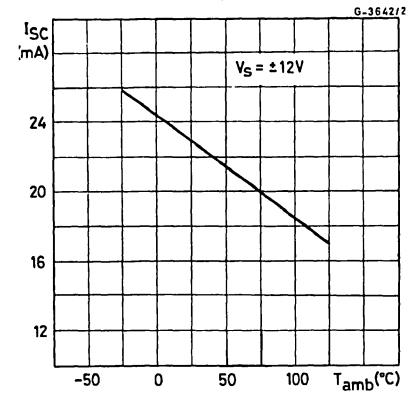


Figure 4: Open Loop Frequency and Phase Response.

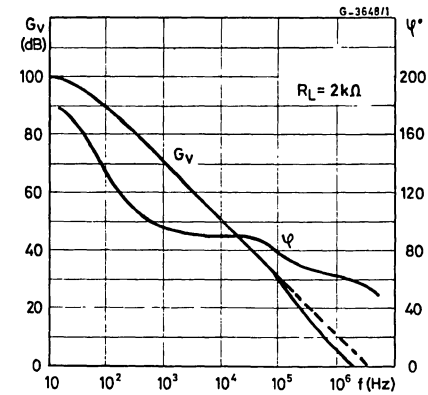


Figure 5: Open Loop Gain vs. Ambient Temperature.

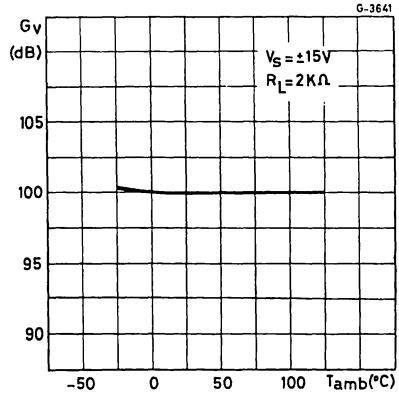


Figure 6 : Supply Voltage Rejection vs. Frequency.

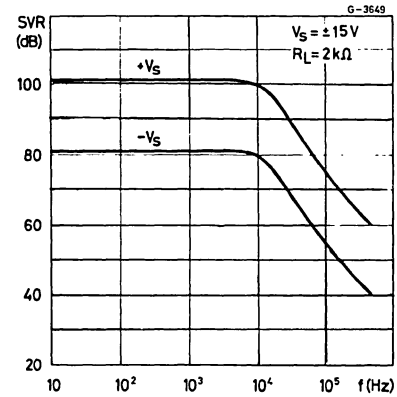


Figure 7 : Large Signal Frequency Response.

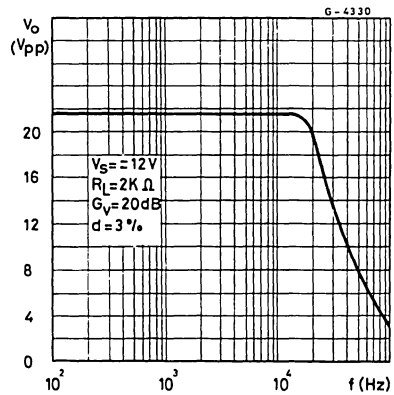


Figure 8 : Output Voltage Swing vs. Load Resistance.

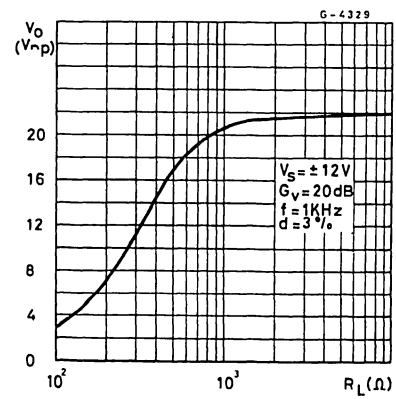
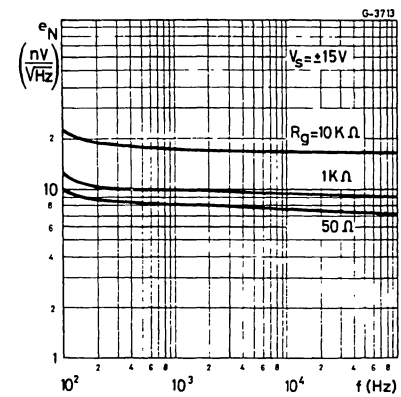


Figure 9 : Total Input Noise vs. Frequency.



APPLICATION INFORMATION

Active low-pass filter :

BUTTERWORTH

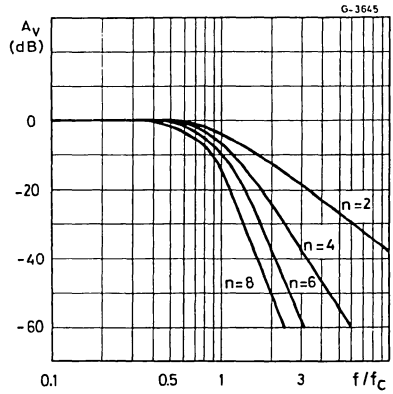
The Butterworth is a "maximally flat" amplitude response filter. Butterworth filters are used for filtering signals in data acquisition systems to prevent aliasing errors in sampled-data applications and for general purpose low-pass filtering.

The cutoff frequency, f_c, is the frequency at which the amplitude response in down 3 dB. The attenuation rate beyond the cutoff frequency is - n6 dB per octave of frequency where n is the order (number of poles) of the filter.

Other characteristics :

- Flattest possible amplitude response.
- Excellent gain accuracy at low frequency end of passband.

Figure 10 : Amplitude Response.



BESSEL

The Bessel is a type of "linear phase" filter. Because of their linear phase characteristics, these filters approximate a constant time delay over a limited frequency range. Bessel filters pass transient waveforms with a minimum of distortion. They are also used to provide time delays for low pass filtering of modulated waveforms and as a "running average" type filter.

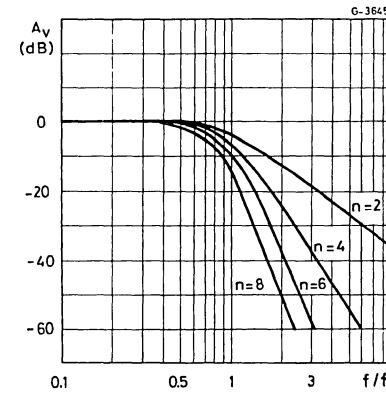
The maximum phase shift is $\frac{-n\pi}{2}$ radians where n is the order (number of poles) of the filter. The cutoff frequency, f_c, is defined as the frequency at which the phase shift is one half to this value. For accurate delay, the cutoff frequency should be twice the maximum signal frequency. The following table can be used to obtain the – 3 dB frequency of the filter.

	2 pole	4 Pole	6 Pole	8 Pole
– 3dB Frequency	0.77 f_c	0.67 f_c	0.57 f_c	0.50 f_c

Other characteristics :

- Selectivity not as great as Chebyschev or Butterworth.
- Very small overshoot response to step inputs.
- Fast rise time.

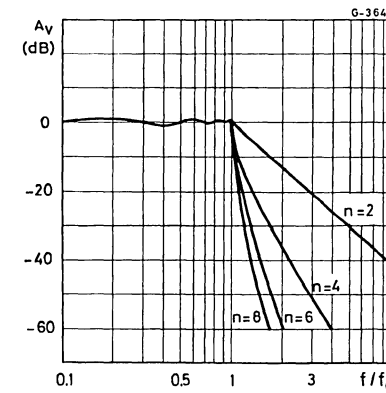
Figure 11 : Amplitude Response.



CHEBYSCHEV

Chebyschev filters have greater selectivity than either Bessel or Butterworth at the expense of ripple in the passband.

Figure 12 : Amplitude Response (± 1 dB ripple).



APPLICATION INFORMATION (continued)

Chebyschev filters are normally designed with peak-to-peak ripple values from 0.2 dB to 2 dB.

Increased ripple in the passband allows increased attenuation above the cutoff frequency.

The cutoff frequency is defined as the frequency at which the amplitude response passes through the specified maximum ripple band and enters the stop band.

Other characteristics :

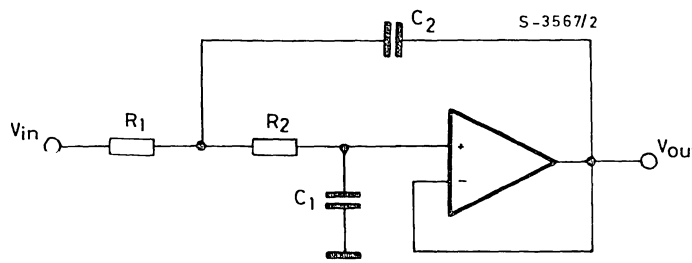
- Greater selectivity.
- Very nonlinear phase response.
- High overshoot response to step inputs.

The table below shows the typical overshoot and setting time response of the low pass filter to a step input.

	Number of Poles	Peak Overshoot	Settling Time (% of final value)		
		% Overshoot	± 1%	± 0.1%	± 0.01%
Butterworth	2	4	$1.1/f_c$ sec.	$1.7/f_c$ sec.	$1.9/f_c$ sec.
	4	11	$1.7/f_c$	$2.8/f_c$	$3.8/f_c$
	6	14	$2.4/f_c$	$3.9/f_c$	$5.0/f_c$
	8	16	$3.1/f_c$	$5.1/f_c$	$7.1/f_c$
Bessel	2	0.4	0.8/fc	1.4/fc	1.7/fc
	4	0.8	1.0/fc	1.8/fc	2.4/fc
	6	0.6	1.3/fc	2.1/fc	2.7/fc
	8	0.3	1.6/fc	2.3/fc	3.2/fc
Chebyschev (ripple ± 0.25dB)	2	11	1.1/fc	1.6/fc	–
	4	18	3.0/fc	5.4/fc	–
	6	21	5.9/fc	10.4/fc	–
	8	23	8.4/fc	16.4/fc	–
Chebyschev (ripple ± 1dB)	2	21	1.6/fc	2.7/fc	–
	4	28	4.8/fc	8.4/fc	–
	6	32	8.2/fc	16.3/fc	–
	8	34	11.6/fc	24.8/fc	–

Design of 2nd order active low pass filter (Sallen and Key configuration unity gain op-amp).

Figure 13 : Filter Configuration.



$$\frac{V_o}{V_i} = \frac{1}{1 + 2\xi \frac{S}{\omega_c} + \frac{S^2}{\omega_c^2}}$$

Where :

$\omega c = 2\pi f_c$ with f_c = cutoff frequency

ξ = damping factor.

APPLICATION INFORMATION (continued)

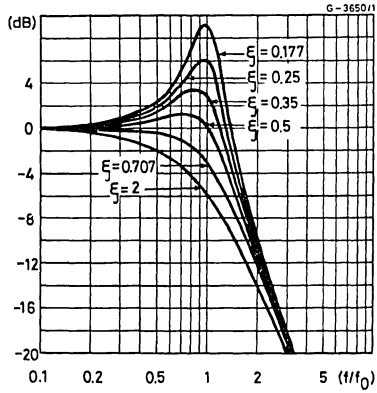
Three parameters are needed to characterize the frequency and phase response of a 2nd order active filter : the gain (G_V), the damping factor (ξ) or the Q-factor ($Q = (2\xi)^{-1}$), and the cutoff frequency (f_c).
The higher order responses are obtained with a series of 2nd order sections. A simple RC section is introduced when an odd filter is required.

The choice of 'ξ' (or Q-factor) determines the filter response (see table).

Table 1.

Filter Response	ξ	Q	Cutoff Frequency f_c
Bessel	$\frac{\sqrt{3}}{2}$	$\frac{1}{\sqrt{3}}$	Frequency at which Phase Shift is – 90°C
Butterworth	$\frac{\sqrt{2}}{2}$	$\frac{1}{\sqrt{2}}$	Frequency at which $G_v = -3$dB
Chebyschev	$< \frac{\sqrt{2}}{2}$	$> \frac{1}{\sqrt{2}}$	Frequency at which the amplitude response passes through specified max. ripple band and enters the stop band.

Figure 14 : Filter Response vs. Damping Factor.



Fixed $R = R_1 = R_2$, we have (see fig. 13)

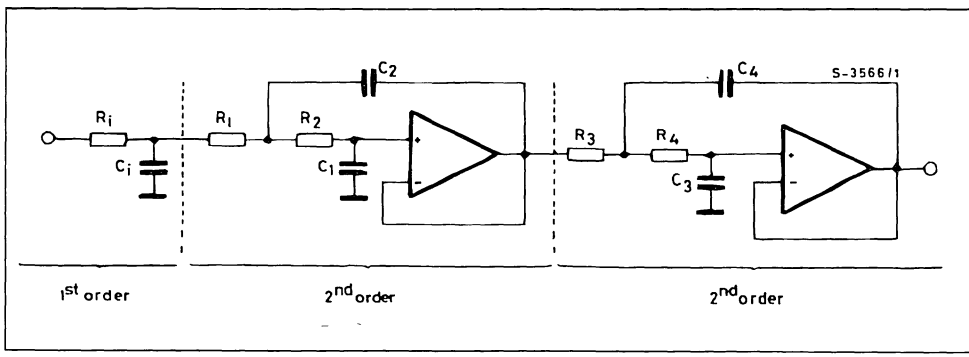
$$C_1 = \frac{1}{R}\,\frac{\xi}{\omega_c}$$

$$C_2 = \frac{1}{R}\,\frac{1}{\xi\omega_c}$$

The diagram of fig.14 shows the amplitude response for different values of damping factor ξ in 2nd order filters.

EXAMPLE

Figure 15 : 5th Order Low Pass Filter (Butterworth) with Unity Gain Configuration.



SGS-THOMSON MICROELECTRONICS

APPLICATION INFORMATION (continued)

In the circuit of fig. 15, for f_c = 3.4 KHz and $R_i = R_1 = R_2 = R_3 = R_4$ =10 KΩ, we obtain :

$$C_i = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33\text{nF}$$

$$C_1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97\ \text{nF}$$

$$C_2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20\ \text{nF}$$

$$C_3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45\ \text{nF}$$

$$C_4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 15.14\ \text{nF}$$

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

The same method, referring to Tab. II and fig. 16, is used to design high-pass filter. In this case the damping factor is found by taking the reciprocal of the numbers in Tab. II. For f_c = 5 KHz and $C_i = C_1 = C_2 = C_3 = C_4$ = 1 nF we obtain :

$$R_i = \frac{1}{1.354} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 23.5\ \text{K}\Omega$$

$$R_1 = \frac{1}{0.421} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 75.6\ \text{K}\Omega$$

$$R_2 = \frac{1}{1.753} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 18.2\ \text{K}\Omega$$

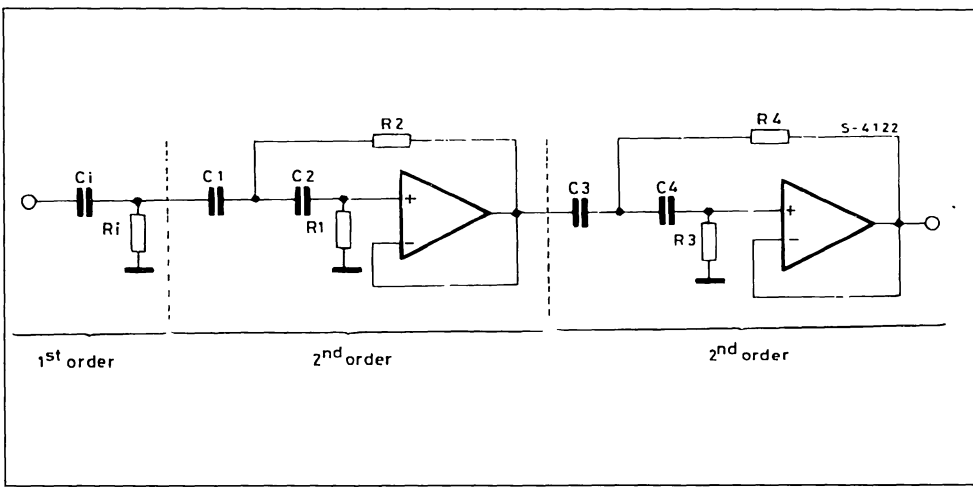
$$R_3 = \frac{1}{0.309} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 103\ \text{K}\Omega$$

$$R_4 = \frac{1}{3.325} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 9.6\ \text{K}\Omega$$

Table II : Damping Factor for Low-pass Butterworth Filters.

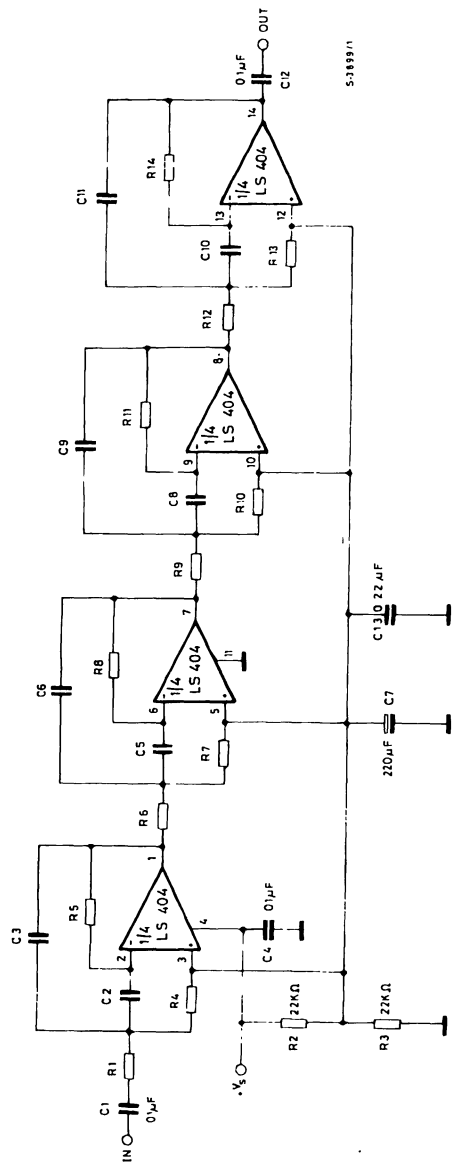
Order	C_I	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
2		0.707	1.41						
3	1.392	0.202	3.54						
4		0.92	1.08	0.38	2.61				
5	1.354	0.421	1.75	0.309	3.235				
6		0.966	1.035	0.707	1.414	0.259	3.86		
7	1.336	0.488	1.53	0.623	1.604	0.222	4.49		
8		0.98	1.02	0.83	1.20	0.556	1.80	0.195	5.125

Figure 16 : 5th Order High-pass Filter (Butterworth) with Unity Gain Configuration.



APPLICATION INFORMATION (continued)

Figure 17 : Multiple Feedback 8-pole Bandpass Filter.



f_c = 1.180 Hz ; A = 1 ; $C_2 = C_3 = C_5 = C_6 = C_8 = C_9 = C_{10} = C_{11}$ = 3.300 pF ;

$R_1 = R_6 = R_9 = R_{12}$ = 160 KΩ ; $R_5 = R_8 = R_{11} = R_{14}$ = 330 KΩ ; $R_4 = R_7 = R_{10} = R_{13}$ = 5.3 KΩ

Figure 18 : Frequency Response of Band-pass Filter.

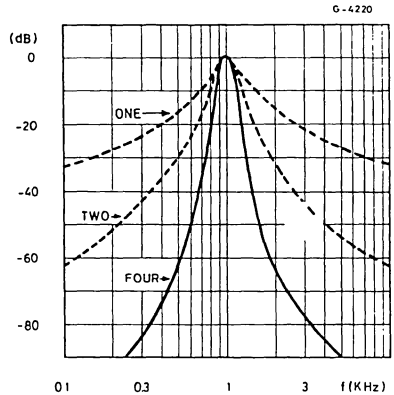


Figure 19 : Bandwidth of Band-pass Filter.

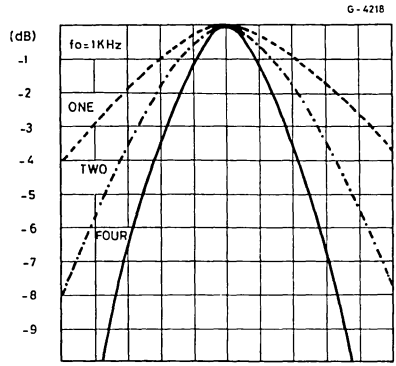
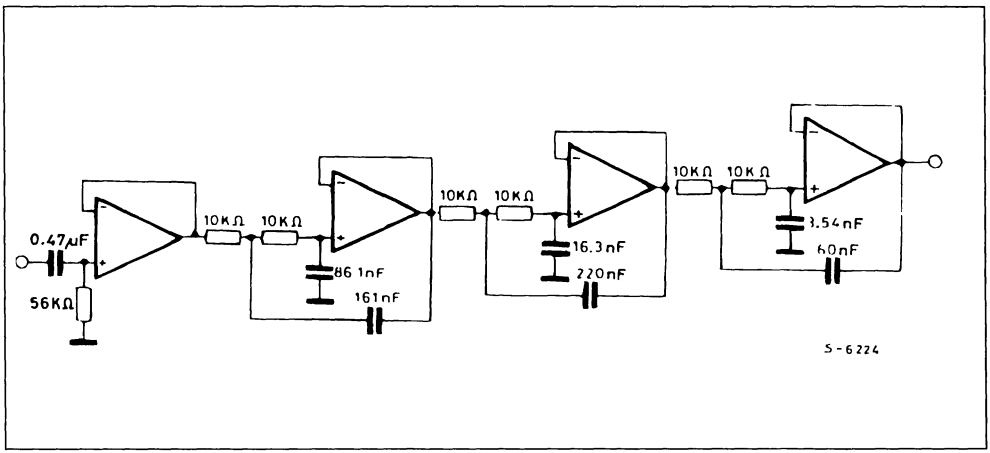
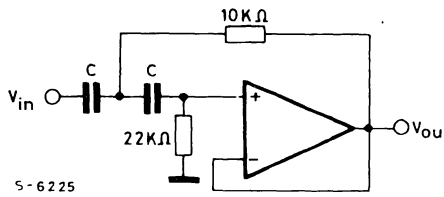


Figure 20 : Six-pole 355 Hz Low-pass Filter (chebychev type).



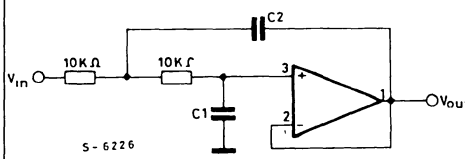
This is a 6-pole Chebychev type with ± 0.25 dB ripple in the passband. A decoupling stage is used to avoid the influence of the input impedance on the filter's characteristics. The attenuation is about 55 dB at 710 Hz and reaches 80 dB at 1065 Hz. The in band attenuation is limited in practice to the ± 0.25 dB ripple and does not exceed 0.5 dB at 0.9 fc.

Figure 21 : Subsonic Filter (G_v = 0 dB).



f_c (Hz)	C (µF)
15	0.68
22	0.47
30	0.33
55	0.22
100	0.1

Figure 22 : High Cut Filter (G_v = 0 dB).



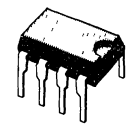
f_c (KHz)	C1 (nF)	C2 (nF)
3	3.9	6.8
5	2.2	4.7
10	1.2	2.2
15	0.68	1.5

DUAL HIGH PERFORMANCE OPERATIONAL AMPLIFIER

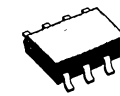
- SINGLE OR SPLIT SUPPLY OPERATION
- LOW POWER CONSUMPTION
- HIGH UNITY GAIN BANDWIDTH
- NO CROSSOVER DISTORSION
- NO POP NOISE
- SHORT-CIRCUIT PROTECTION
- HIGH CHANNEL SEPARATION

DESCRIPTION

The LS4558N is a high performance dual operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth products. The circuit presents very stable electrical characteristics over the entire supply voltage range and the specially designed input stage allow the LS4558N to be used in low noise audio signal processing application. The optimized class AB output stage completely eliminates crossover, distorsion, under any load conditions, has large source and sink capacity and is short-circuit protected.



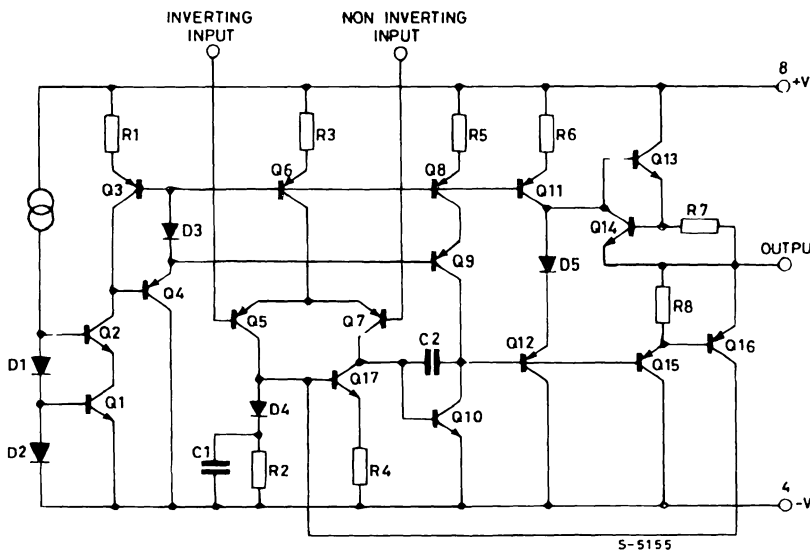
Minidip



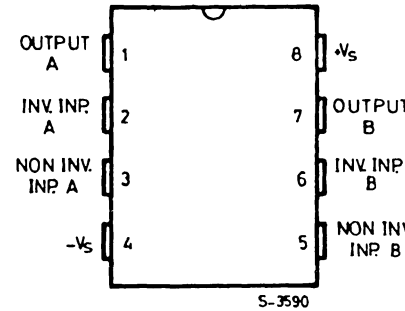
SO-8J

ORDER CODES : LS4558NB (Minidip)
LS4558NM (SO-8J)

SCHEMATIC DIAGRAM (one section)



CONNECTION DIAGRAM (top view)



ABSOLUTE MAXIMUM RATINGS

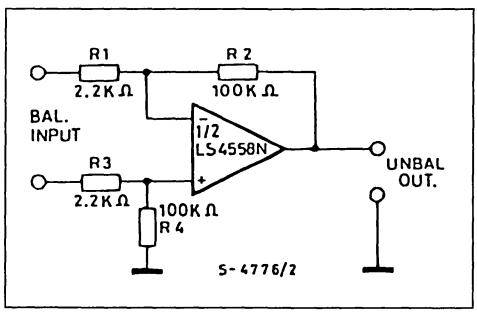
Symbol	Parameter		Value	Unit
V_s	Supply Voltage		± 18	V
V_i	Input Voltage		± V_s	
V_i	Differential Input Voltage		± (V_s – 1)	V
P_{tot}	Power Dissipation at T_{amb} = 70 °C	Minidip Micropackage	665 400	mW mW
T_{op}	Operating Temperature		0 to 70	°C
T_j	Junction Temperature		150	°C
T_{stg}	Storage Temperature		– 55 to 150	°C

THERMAL DATA

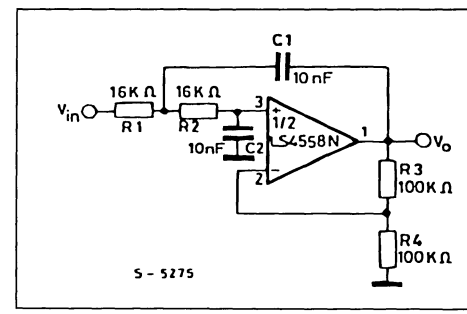
		Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	120 °C/W	200 °C/W

TYPICAL APPLICATIONS

Balanced Input Audio Preamplifier.



DC Coupled Low-pass Active Filter
(f = 1 KHz, G_V = 6 dB).



ELECTRICAL CHARACTERISTICS ($V_s = \pm 15$ V, $T_{amb} = 25$ °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_s	Supply Current (*)			1	2	mA
I_b	Input Bias Current			50	500	nA
		$T_{min} < T_{op} < T_{max}$			800	nA
R_I	Input Resistance	f = 1 KHz	0.3	1		MΩ
V_{os}	Input Offset Voltage	$R_g \leq 10$ KΩ		0.5	5	mV
		$R_g \leq 10$ KΩ $T_{min} < T_{op} < T_{max}$			7.5	mV
I_{os}	Input Offset Current			20	200	nA
		$T_{min} < T_{op} < T_{max}$			500	nA
I_{sc}	Output Short Circuit Current			23		mA
G_v	Large Signal Open Loop Voltage Gain	$R_L = 2$ KΩ	86	100		dB
B	Gain-bandwidth Product	f = 20 KHz	2	3		MHz
e_N	Total Input Noise Voltage	f = 1 KHz $R_g = 50\ \Omega$ $R_g = 1$ KΩ $R_g = 10$ KΩ		8 10 18	15	$\frac{nV}{\sqrt{Hz}}$
e_N	Popcorn Noise	B = 1 Hz to 1 KHz $R_g = 10$ KΩ t = 10 sec			10	μV Peak
d	Distortion	$G_v = 20$ dB $R_L = 2$ KΩ $V_o = 2$ Vpp f = 1 KHz		0.03		%
V_o	Output Voltage Swing	$R_L = 2$ KΩ		± 13		V
V_o	Large Signal Voltage Swing	$R_L = 10$ KΩ f = 10 KHz		28		Vpp
	Transient Response — Rise Time	$V_i = 20$ mV $R_L = 2$ KΩ $C_L = 100$ pF		0.13		μS
	Transient Response — Overshoot			5		%
SR	Slew Rate	Unity Gain $R_L = 2$ KΩ	0.8	1.5		V/μs
CMR	Common Mode Rejection	$V_i = 10$ V $T_{min} < T_{op} < T_{max}$	70	90		dB
SVR	Supply Voltage Rejection	$V_i = 1$ V f = 100 Hz $T_{min} < T_{op} < T_{max}$	80	100		dB
CS	Channel Separation	f = 10 KHz $R_g = 1$ KΩ		105		dB

(*) Both amplifiers.

Figure 1 : Open Loop Frequency and Phase Response.

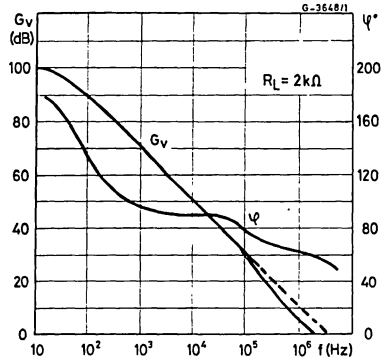


Figure 2 : Open Loop Gain vs. Ambient Temperature.

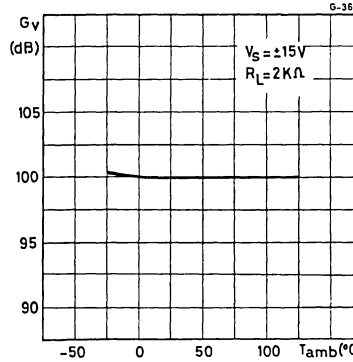


Figure 3 : Supply Voltage Rejection vs. Frequency

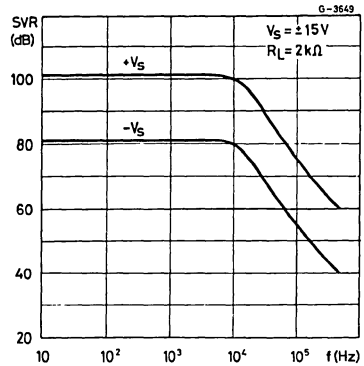


Figure 4 : Large Signal Frequency Response.

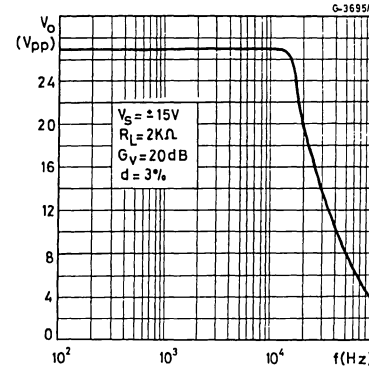


Figure 5 : Output Voltage Swing vs. Load Resistance.

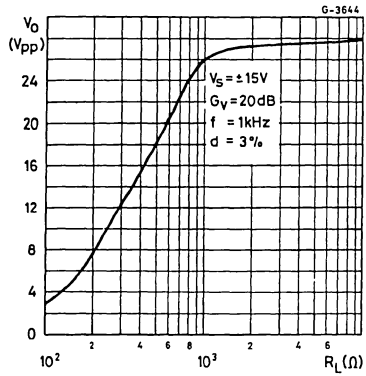


Figure 6 : Total Input Noise vs. Frequency.

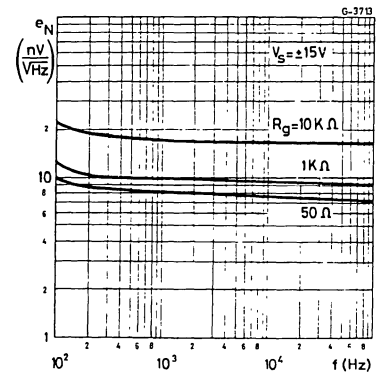


Figure 7 : Channel Separation.

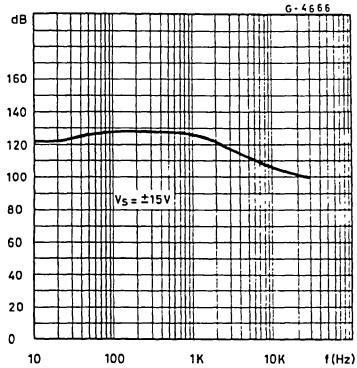


Figure 8 : Transient Response.

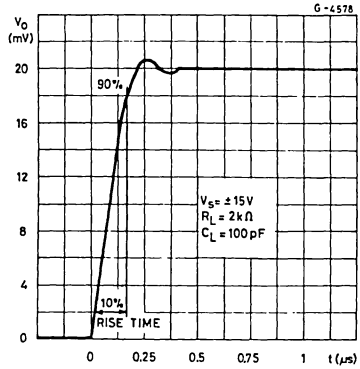
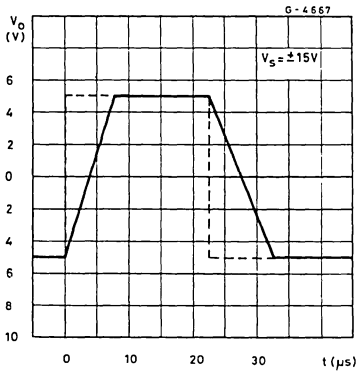
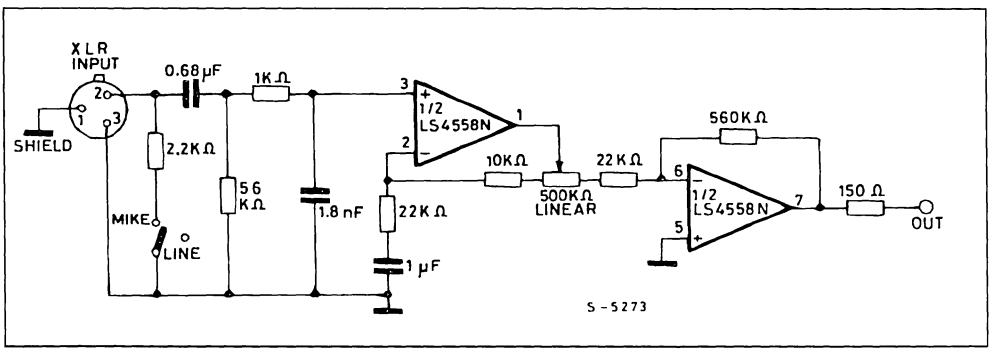


Figure 9 : Voltage Follower Large-signal Pulse Response.



APPLICATION INFORMATION

Figure 10 : Mike/Line Preamplifier for Audio Mixers (0 dB to 60 dB continuously variable gain).



Note : The particular characteristics of the circuit of Figure 10 is that using a linear potentiometer, the gain is continuously variable in a logarithmic mode from 0 dB to 60 dB in the audio band.

Figure 11 : Microphones Nomograph.

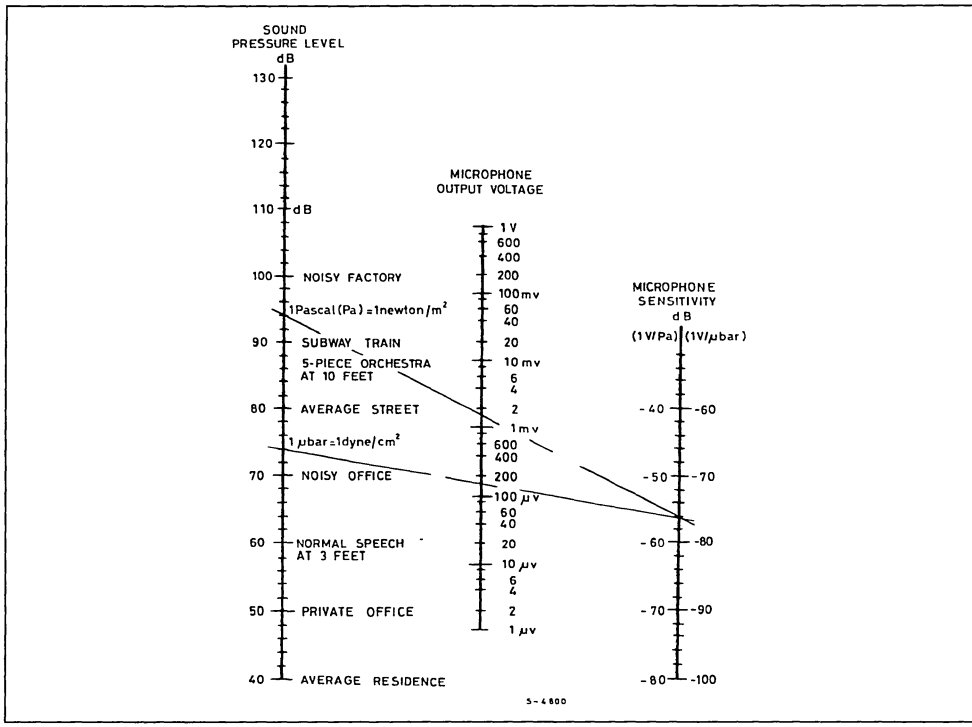


Figure 12 : Very Low-noise Mike Preamplifier (G_V = 40 dB).

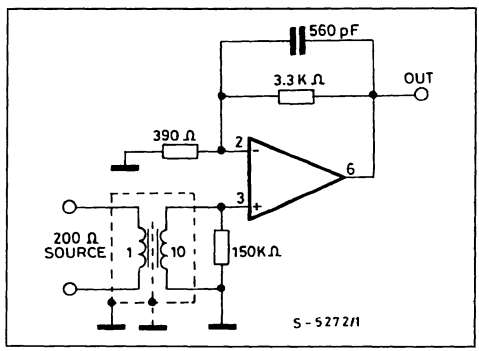


Figure 13 : Balanced Input Audio Preamplifier.

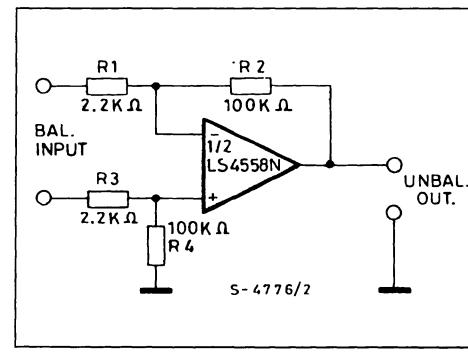


Figure 14 : 20 Hz to 200 Hz Variable High-pass Filter (G_V = 3 dB).

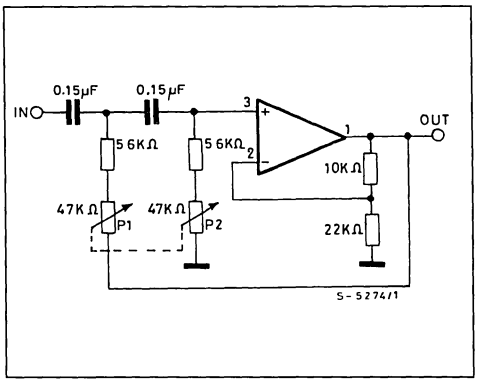


Figure 15 : Frequency Response of the High-pass Filter of Figure 14.

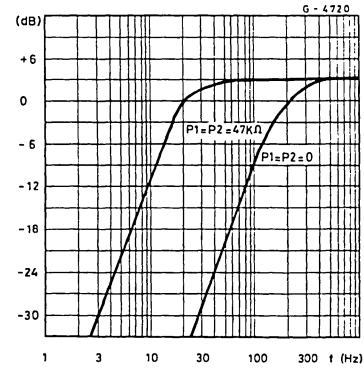


Figure 16 : DC Coupled Low-pass Active Filter (f = 1 KHz, G_V = 6 dB).

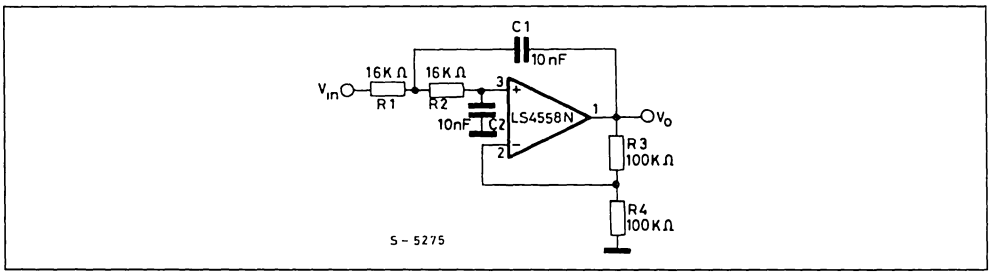


Figure 17 : Switchable HP-LP Audio Filter.

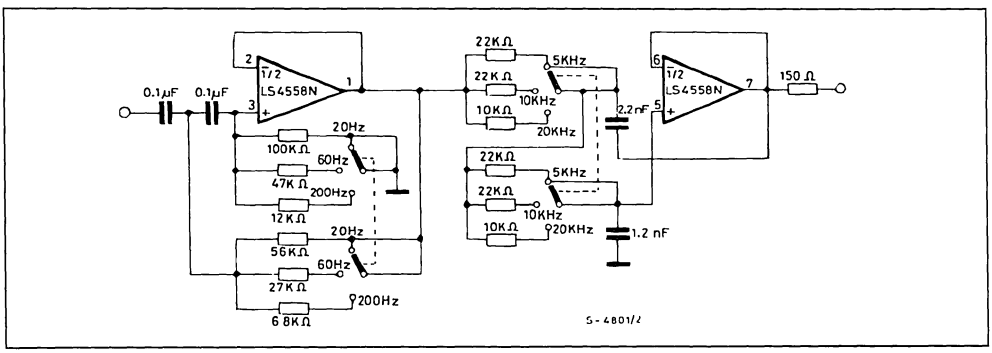
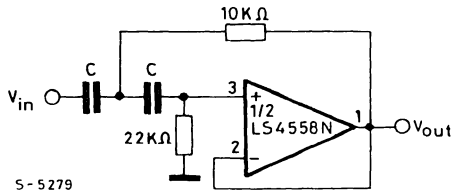
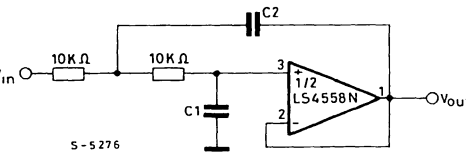


Figure 18 : Subsonic or Rumble Filter (GV = 0 dB).



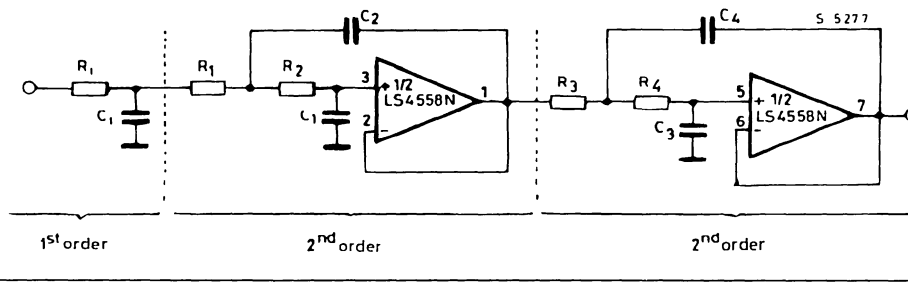
fc (Hz)	C (μF)
15	0.68
22	0.47
30	0.33
55	0.22
100	0.1

Figure 19 : High-cut Filter (G_V = 0 dB).



fc (KHz)	C1 (nF)	C2 (nF)
3	3.9	6.8
5	2.2	4.7
10	1.2	2.2
15	0.68	1.5

Figure 20 : Fifth Order 3.4 KHz Low-pass Butterworth Filter.



For f_c = 3.4 KHz and RI = R1 = R2 = R3 = R4 = 10 KΩ, we obtain :

$$C1 = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33 \text{ nF}$$

$$C1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97 \text{ nF}$$

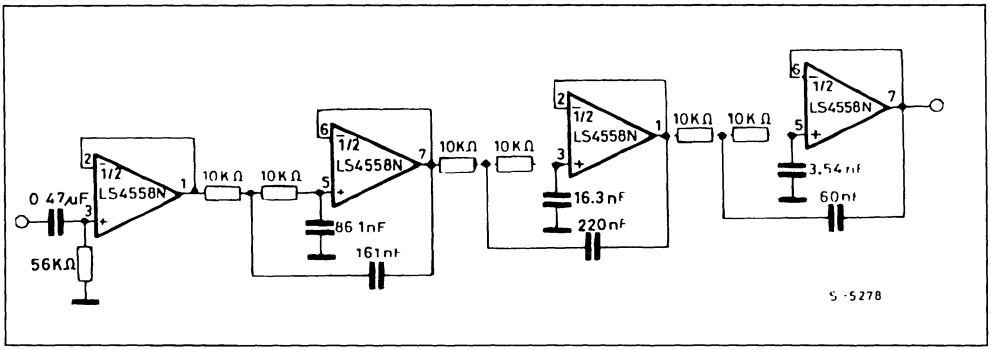
$$C1 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20 \text{ nF}$$

$$C1 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45 \text{ nF}$$

$$C1 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 15.14 \text{ nF}$$

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

Figure 21 : Six-pole 355 Hz Low-pass Filter (Chebychev type).



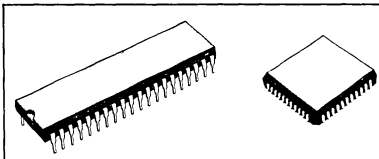
This is a 6-pole Chebychev type with ± 0.25 dB ripple in the passband A decoupling stage is used to avoid the influence of the input impedance on the filter's characteristics. The attenuation is about 55 dB at 710 Hz and reaches 80 dB at 1065 Hz. The in band attenuation is limited in practice to the ± 0.25 dB ripple and does not exceed 0.5 dB at 0.9 fc

SGS-THOMSON MICROELECTRONICS

M8438A

SERIAL INPUT LCD DRIVER

- DRIVES UP TO 32 LCD SEGMENTS
- DATA TRANSFER: FIXED ENABLE MODE FOR DIP-40, ENABLE AND LATCH-MODE FOR 44PLCC
- INPUTS ARE CMOS, NMOS AND TTL COMPATIBLE
- CASCADABLE
- REQUIRES ONLY 3 CONTROL LINES
- ON CHIP OSCILLATOR
- CMOS TECHNOLOGY FOR WIDE SUPPLY VOLTAGE RANGE
- −40 TO 85°C TEMPERATURE RANGE



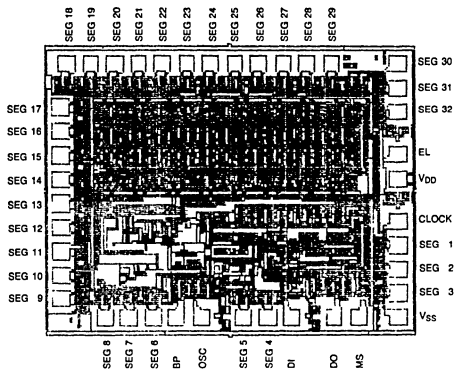
B
DIP-40 Plastic

C
44 PLCC Plastic Chip Carrier

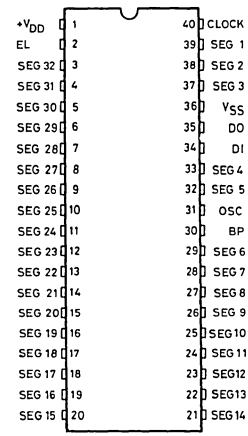
ORDERING NUMBERS: M8438A DIE 1
M8438A B6
M8438A C6

DESCRIPTION

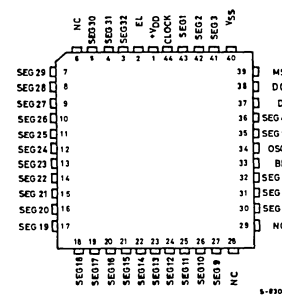
The M8438A is a CMOS integrated circuit that drives an LCD display, usually under microprocessor control. The part acts as a smart peripheral that drives up to 32 LCD segments. It needs only three control lines due to its serial input construction. It latches the data to be displayed and relieves the microprocessor from the task of generating the required waveforms.
The M8438A can drive any standard or custom parallel drive LCD whether it be field effect or dynamic scattering. Several drivers can be cascaded, if more than 32 segments are to be driven. The AC frequency of the LCD waveforms can be supplied by the user or can be generated by attaching a capacitor to the OSC input which determines the frequency of an internal oscillator.
The M8438A is available in DIE form and assembled in 40 pin dual-in line plastic or 44 PLCC packages.



PIN CONNECTIONS



5-8309



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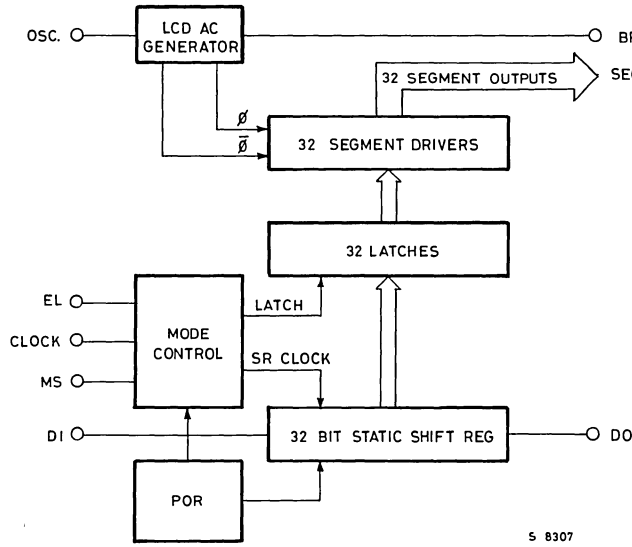
BLOCK DIAGRAM



OSC :Oscillator (capacitor or drive signal)
EL :Enable/Latch control input
MS :Mode select input (not available in 40 Pin DIL)
DI :Serial data input
DO :Serial data output
BP :Backplane output
SEG :Segment output signal

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
(VDD-VSS)	Supply voltage	−0.3 to +12	V
V_I	Input voltage	VSS−0.3 to VDD+0.3	V
V_O	Output voltage	VSS−0.3 to VDD+0.3	V
P_D	Power dissipation	250	mW
T_{stg}	Storage temperature	−55 to +125	°C
T_A	Operating temperature	−40 to +85	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C and V_{DD} = 5V unless otherwise noted)

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Test Condition	Min.	Max.	Unit
V_{DD}	Supply Voltage			3	10	V
I_{DD}	Supply Current		Oscillator f < 15kHz		60	µA
I_Q	Quiescent Current		V_{DD} = 10V		10	µA
V_{IH}	Input High Level	CLOCK DI EL		.5V_{DD}	V_{DD}	V
V_{IL}	Input Low Level			0	.2V_{DD}	V
I_{IN}	Input Current				±5	µA
C_I	Input Capacitance				5	pF
V_{IH}	Input High Level	OSC	Driven mode	.9V_{DD}		V
V_{IL}	Input Low Level		Driven mode		.1V_{DD}	V
I_{IN}	Input Current		Driven mode		±10	µA
R_{ON}	Segment Output Impedance		I_{IL} = 10µA		40	kΩ
R_{ON}	Backplane Output Impedance		I_L = 100µA		3	kΩ
V_{OFF}	Output Offset Voltage		C_L = 250pF between each SEG output and BP		±50	mV
R_{ON}	Data Output Impedance		I_L = 100µA		3	kΩ

DYNAMIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit
t_{TR}	Transition Time OSC	Driven mode		500	ns
t_{SD}	Data Set-up Time	Fig. 1 and 2	150		ns
t_{HD}	Data Hold Time	Fig. 1 and 2	50		ns
t_{SE}	EL Set-up Time	Fig. 1	100		ns
t_{HE}	EL Hold Time	Fig. 1	100		ns
t_{WE}	EL Pulse Width	Fig. 2	175		ns
t_{CE}	Clock to EL Time	Fig. 2	250		ns
t_{pd}	DO Propagation Delay	Fig. 1, 2; C_L = 55pF		500	ns
f	Clock Rate	V_{DD} = 10 50% duty cycle;	DC	1.5	MHz

FUNCTIONAL DESCRIPTION

LCD-AC-GENERATOR

This block generates a 50% duty cycle signal for the backplane output. The circuit can be used in two different modes: oscillator or driven.

OSCILLATOR MODE:

In this mode the backplane frequency is determined by the internal RC oscillator together with an 8-stage frequency divider. For generating the backplane output signal of 50% duty cycle the oscillator frequency is divided by 256. The RC oscillator requires an external capacitor to be connected between input OSC and VSS. A value of 18pF gives a backplane frequency of 80Hz ± 30% at VDD = 5V. The variation of the backplane frequency over the entire temperature and supply voltage range is ± 50%.

DRIVEN MODE:

In this mode the signal at the backplane output BP is in phase with an external driving signal applied to input OSC. This mode is used to synchronize the LCD drive of two or more cascaded driver circuits.

FUNCTIONAL DESCRIPTION (continued)

DETECTION LOGIC

The circuit is able to distinguish between the conditions for oscillator or driven mode. If the circuit is to be in the oscillator mode, the OSC pin has a capacitor connected to it. The oscillator will start as soon as the supply voltage exceeds a certain minimim value. The signal at pin OSC swings within a range from $0.3V_{DD}$ to $0.7V_{DD}$. If the circuit is to be in the driven mode, the OSC pin has to be forced to logic levels by an external source. The transition time between the logic levels must be short, so that the circuit does not react on the voltage level in between. In the driven mode the 8-stage frequency divider is by-passed.

SEGMENT OUTPUTS

A logic 0 at the data input DI causes a segment output signal to be in phase with the backplane signal and turns the segment off. A logic 1 causes a segment output to be in opposite phase to the backplane signal and turns the segment on.

MICROPROCESSOR INTERFACE

The circuit can operate in two different data transfer modes: Enable mode and latch mode. One of either mode can be chosen with the mode select input MS. An internal pull up device is provided between this input and VDD. Enable mode is selected if MS is left open or connected to VDD.
Latch mode is selected if MS is connected to VSS.
The input MS is not available, if the device is assembled in the 40 pin package, and is internally fixed to operate in ENABLE MODE.

ENABLE MODE

Fig. 3 shows a timing diagram of the enable mode. Data is serially shifted in and out of the shift register on the negative transition of the clock.
Serial entry into the shift register is permitted when the enable/latch control EL is high. When EL is low it causes the shift register clock to be inhibited and the content of the shift register to be loaded into the latches that control the segment drivers.

LATCH MODE

Fig. 4 shows a timing diagram of the latch mode. Data is serially shifted in and out of the shift register on the negative transition of the clock.
Serial entry into the shift register is permitted independently of the enable/latch control EL. When EL is high it causes a parallel load of the content in the shift register into the latches. It is acceptable to tie the EL line high. Then the latches are transparent and only two lines, clock and data input, would then be needed for data transfer.

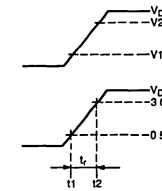
POWER-ON LOGIC

A power on reset pulse is generated internally when the supply voltage is being turned on. The generation of the reset pulse is level dependent and will occur even on a slowly rising supply voltage.
The power on reset pulse resets all shift register stages and the latches that control the segment drivers. Therefore all segment outputs are initially in phase with the backplane output. This causes the display to be blanked and no arbitrary data to show up. This condition is maintained until data is shifted into the register and loaded into the latches.

CONDITIONS FOR POWER-ON RESET FUNCTION

The POR circuit triggers on the rising slope of the positive supply voltage V_{DD}. A reset pulse will be generated, if conditions a) through d) are given:

a) Level
Rising slope from V1 to V2
V1 max = 0.5V
V2 min = 3.0V



b) Rise time
t_r min = 10 μs
t_r max = 1 s

c) Rise function
The function of V_{DD} between t1 und t2 may be nonlinear, but should not show a maximum and should not exceed 0.25 V/μs.

d) Recovery time
The minimum time between turn-off and turn-on of V_{DD} is 1s.

CASCADE CONFIGURATION

Several LCD drivers can be cascaded if a liquid crystal display with more than 32 segments is to be connected.
The phase correlation between all segment outputs is achieved by using the second (and any other) device in the driven mode.
Two different cascade configurations can be chosen depending whether the LCD frequency is to be determined by the internal RC oscillator or by an external signal.
Figure 3 shows the connection scheme for a self oscillating configuration, figure 4 shows the connection of an externally controlled one.

Fig. 1 - Timing diagram of enable mode: set-up and hold time

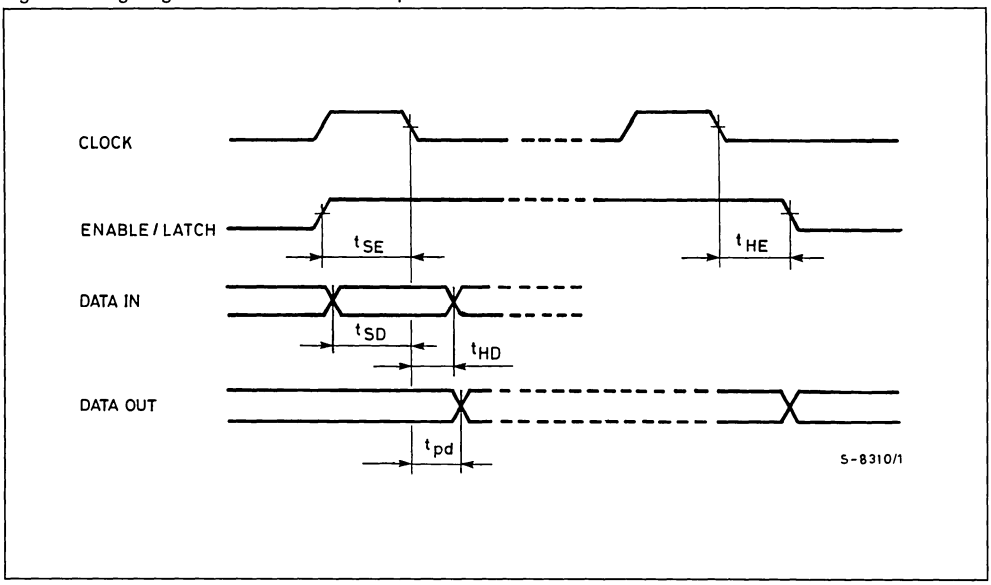


Fig. 2 - Timing diagram of latch mode: set-up and hold time

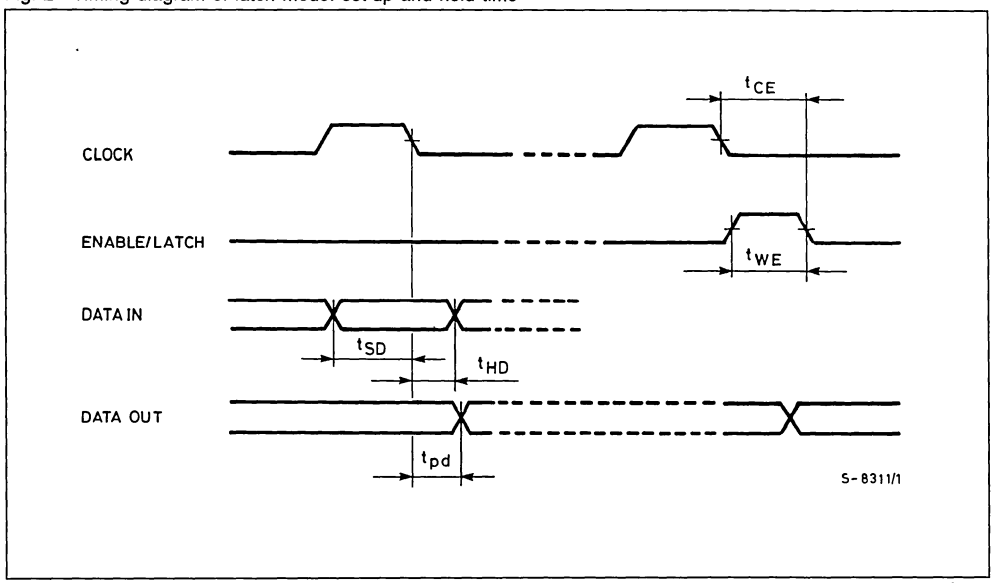


Fig. 3 - Timing diagram of enable mode: Serial load into SR and parallel transfer to LCD

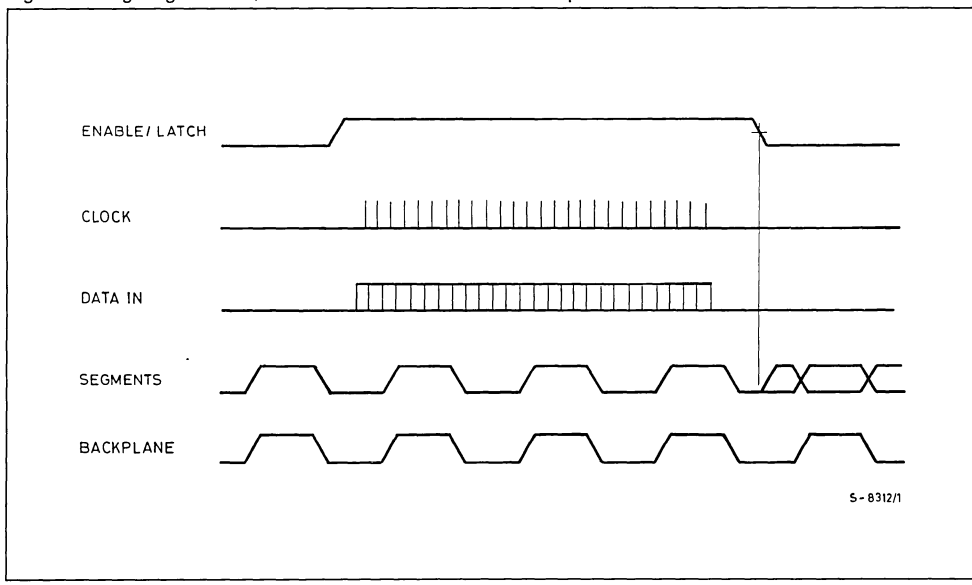


Fig. 4 - Timing diagram of latch mode: Serial load into SR and parallel transfer to LCD

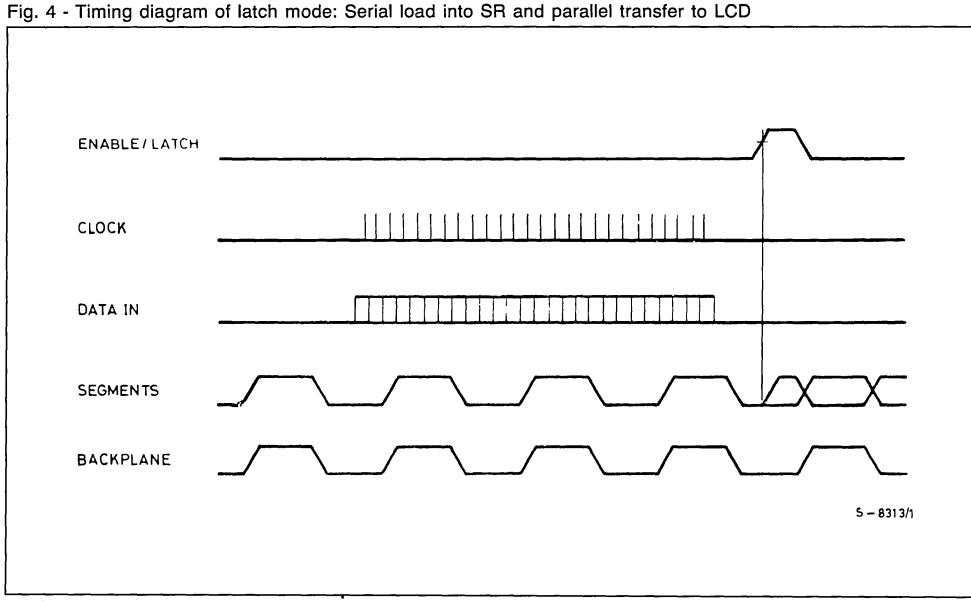


Fig. 5 - Cascade configuration, self oscillating

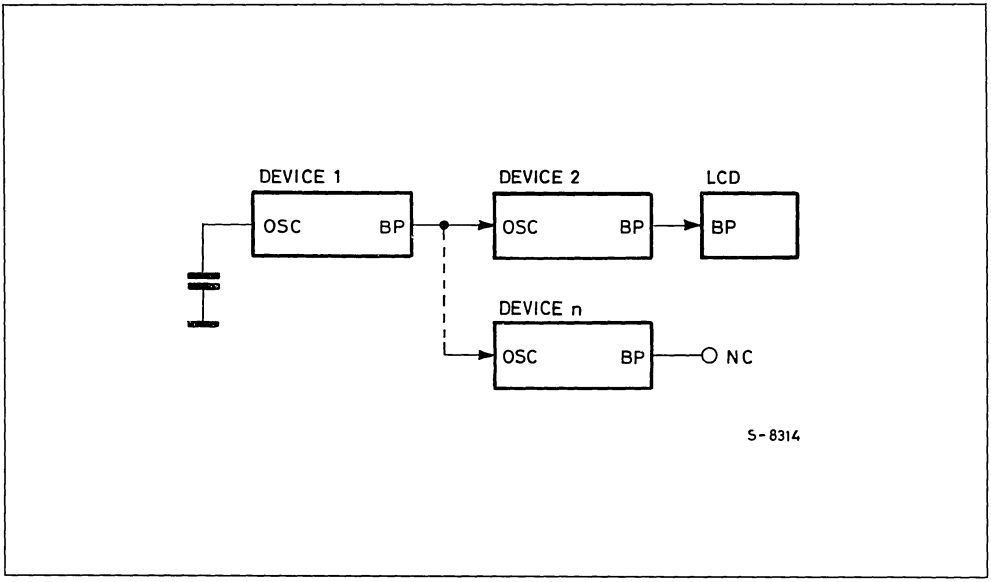
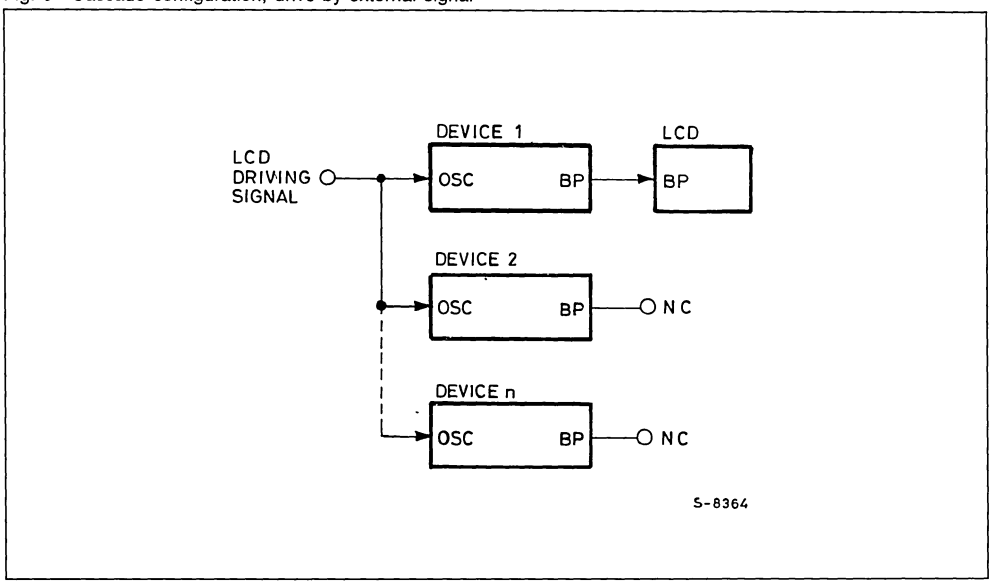
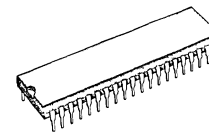


Fig. 6 - Cascade configuration, drive by external signal



SERIAL INPUT LCD DRIVER

- DRIVES UP TO 32 LCD SEGMENTS
- DATA TRANSFER: LATCH MODE
- INPUTS ARE CMOS, NMOS AND TTL COMPATIBLE
- CASCADABLE
- REQUIRES ONLY 3 CONTROL LINES
- ON CHIP OSCILLATOR
- CMOS TECHNOLOGY FOR WIDE SUPPLY VOLTAGE RANGE
- −40 TO 85°C TEMPERATURE RANGE

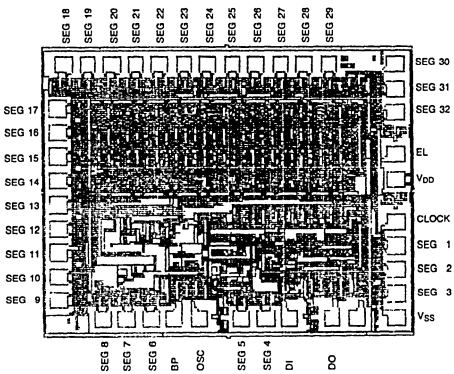


Plastic DIP-40

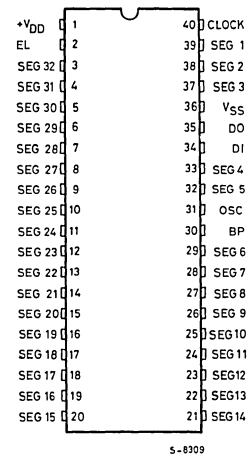
ORDERING NUMBERS: M8439 B6
M8439 DIE 1

DESCRIPTION

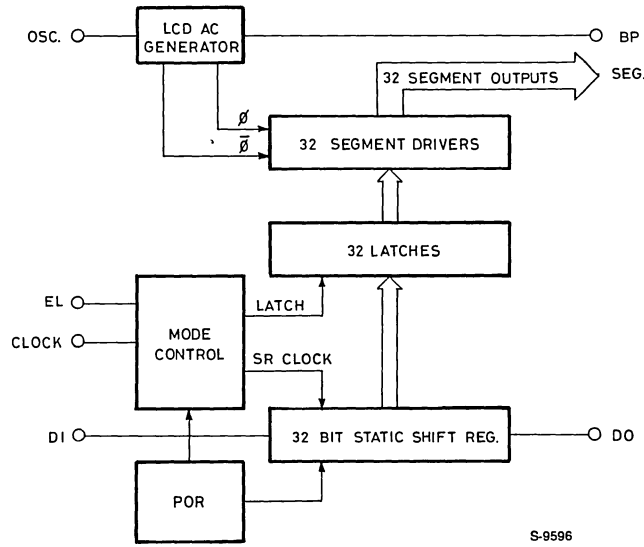
The M8439 is a CMOS integrated circuit that drives an LCD display, usually under microprocessor control. The part acts as a smart peripheral that drives up to 32 LCD segments. It needs only three control lines due to its serial input construction. It latches the data to be displayed and relieves the microprocessor from the task of generating the required waveforms.
The M8439 can drive any standard or custom parallel drive LCD whether it be field effect or dynamic scattering. Several drivers can be cascaded, if more than 32 segments are to be driven. The AC frequency of the LCD waveforms can be supplied by the user or can be generated by attaching a capacitor to the OSC input which determines the frequency of an internal oscillator.
The M8439 is available in DIE form and assembled in 40 pin dual-in line plastic.



PIN CONNECTION



BLOCK DIAGRAM



OSC :Oscillator (capacitor or drive signal)
EL :Enable/Latch control input
DI :Serial data input
DO :Serial data output
BP :Backplane output
SEG :Segment output signal

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
(VDD-VSS)	Supply voltage	−0.3 to +12	V
V_I	Input voltage	VSS−0.3 to VDD+0.3	V
V_O	Output voltage	VSS−0.3 to VDD+0.3	V
P_D	Power dissipation	250	mW
T_{stg}	Storage temperature	−55 to +125	°C
T_A	Operating temperature	−40 to +85	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C and V_{DD} = 5V unless otherwise noted)

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Test Condition	Min.	Max.	Unit
V_{DD}	Supply Voltage			3	10	V
I_{DD}	Supply Current		Oscillator f < 15kHz		60	µA
I_Q	Quiescent Current		V_{DD} = 10V		10	µA
V_{IH}	Input High Level	CLOCK DI EL		.5V_{DD}	V_{DD}	V
V_{IL}	Input Low Level			0	.2V_{DD}	V
I_{IN}	Input Current				±5	µA
C_I	Input Capacitance				5	pF
V_{IH}	Input High Level	OSC	Driven mode	.9V_{DD}		V
V_{IL}	Input Low Level		Driven mode		.1V_{DD}	V
I_{IN}	Input Current		Driven mode		±10	µA
R_{ON}	Segment Output Impedance		I_{IL} = 10µA		40	kΩ
R_{ON}	Backplane Output Impedance		I_L = 100µA		3	kΩ
V_{OFF}	Output Offset Voltage		C_L = 250pF between each SEG output and BP		±50	mV
R_{ON}	Data Output Impedance		I_L = 100µA		3	kΩ

DYNAMIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit
t_{TR}	Transition Time OSC	Driven mode		500	ns
t_{SD}	Data Set-up Time	Fig. 1 and 2	150		ns
t_{HD}	Data Hold Time	Fig. 1 and 2	50		ns
t_{SE}	EL Set-up Time	Fig. 1	100		ns
t_{HE}	EL Hold Time	Fig. 1	100		ns
t_{WE}	EL Pulse Width	Fig. 2	175		ns
t_{CE}	Clock to EL Time	Fig. 2	250		ns
t_{pd}	DO Propagation Delay	Fig. 1, 2; C_L = 55pF		500	ns
f	Clock Rate	V_{DD} = 10 50% duty cycle;	DC	1.5	MHz

FUNCTIONAL DESCRIPTION

LCD-AC-GENERATOR

This block generates a 50% duty cycle signal for the backplane output. The circuit can be used in two different modes: oscillator or driven.

OSCILLATOR MODE:

In this mode the backplane frequency is determined by the internal RC oscillator together with an 8-stage frequency divider. For generating the backplane output signal of 50% duty cycle the oscillator frequency is divided by 256. The RC oscillator requires an external capacitor to be connected between input OSC and VSS. A value of 18pF gives a backplane frequency of 80Hz ± 30% at VDD = 5V. The variation of the backplane frequency over the entire temperature and supply voltage range is ± 50%.

DRIVEN MODE:

In this mode the signal at the backplane output BP is in phase with an external driving signal applied to input OSC. This mode is used to synchronize the LCD drive of two or more cascaded driver circuits.

FUNCTIONAL DESCRIPTION (continued)

DETECTION LOGIC

The circuit is able to distinguish between the conditions for oscillator or driven mode. If the circuit is to be in the oscillator mode, the OSC pin has a capacitor connected to it. The oscillator will start as soon as the supply voltage exceeds a certain minimim value. The signal at pin OSC swings within a range from $0.3V_{DD}$ to $0.7V_{DD}$. If the circuit is to be in the driven mode, the OSC pin has to be forced to logic levels by an external source. The transition time between the logic levels must be short, so that the circuit does not react on the voltage level in between. In the driven mode the 8-stage frequency divider is by-passed.

SEGMENT OUTPUTS

A logic 0 at the data input DI causes a segment output signal to be in phase with the backplane signal and turns the segment off. A logic 1 causes a segment output to be in opposite phase to the backplane signal and turns the segment on.

MICROPROCESSOR INTERFACE

Fig. 2 shows a timing diagram.
Data is serially shifted in and out of the shift register on the negative transition of the clock.
Serial entry into the shift register is permitted independently of the enable/latch control EL. When EL is high it causes a parallel load of the content in the shift register into the latches. It is acceptable to tie the EL line high. Then the latches are transparent and only two lines, clock and data input, would then be needed for data transfer.

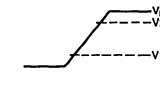
POWER-ON LOGIC

A power on reset pulse is generated internally when the supply voltage is being turned on. The generation of the reset pulse is level dependent and will occur even on a slowly rising supply voltage.
The power on reset pulse resets all shift register stages and the latches that control the segment drivers. Therefore all segment outputs are initially in phase with the backplane output. This causes the display to be blanked and no arbitrary data to show up. This condition is maintained until data is shifted into the register and loaded into the latches.

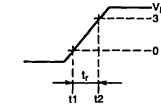
CONDITIONS FOR POWER-ON RESET FUNCTION

The POR circuit triggers on the rising slope of the positive supply voltage V_{DD}. A reset pulse will be generated, if conditions a) through d) are given:

a) Level
Rising slope from V1 to V2
V1 max = 0.5V
V2 min = 3.0V



b) Rise time
t_r min = 10 μs
t_r max = 1 s



c) Rise function
The function of V_{DD} between t1 und t2 may be nonlinear, but should not show a maximum and should not exceed 0.25 V/μs.

d) Recovery time
The minimum time between turn-off and turn-on of V_{DD} is 1s.

CASCADE CONFIGURATION

Several LCD drivers can be cascaded if a liquid crystal display with more than 32 segments is to be connected.
The phase correlation between all segment outputs is achieved by using the second (and any other) device in the driven mode.
Two different cascade configurations can be chosen depending whether the LCD frequency is to be determined by the internal RC oscillator or by an external signal.
Figure 3 shows the connection scheme for a self oscillating configuration, figure 4 shows the connection of an externally controlled one.

Fig. 1 - Timing diagram of latch mode: set-up and hold time

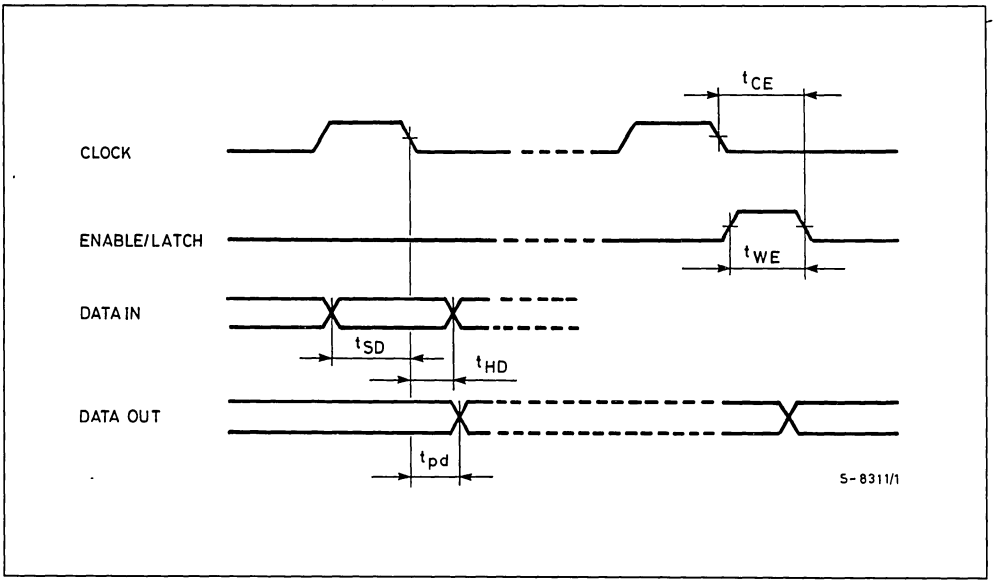


Fig. 2 - Timing diagram of latch mode: Serial load into SR and parallel transfer to LCD

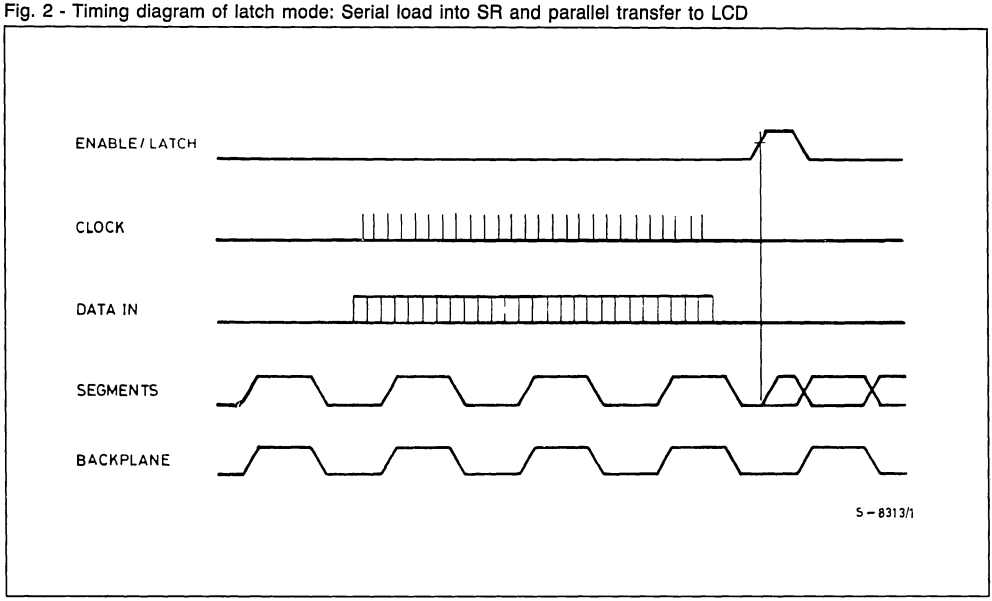


Fig. 3 - Cascade configuration, self oscillating

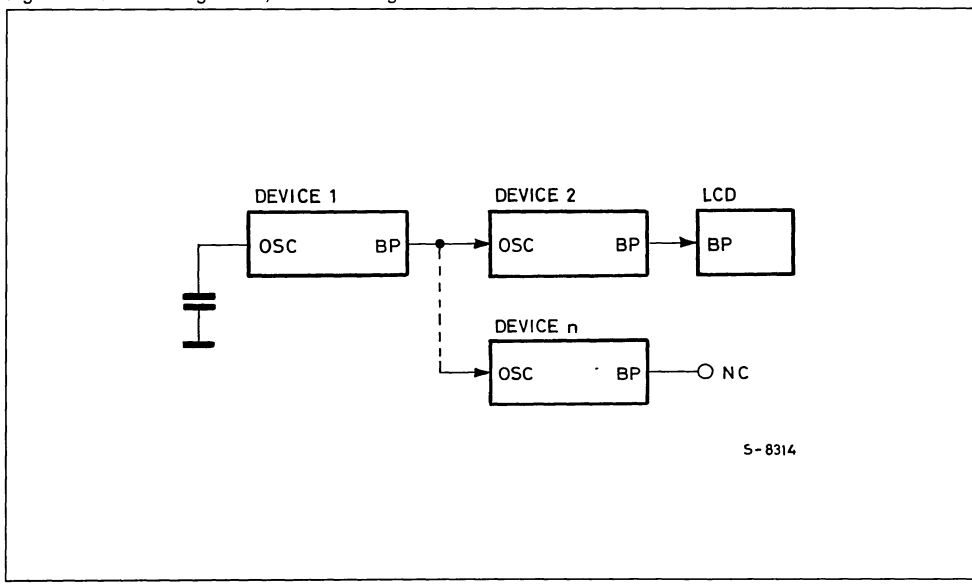
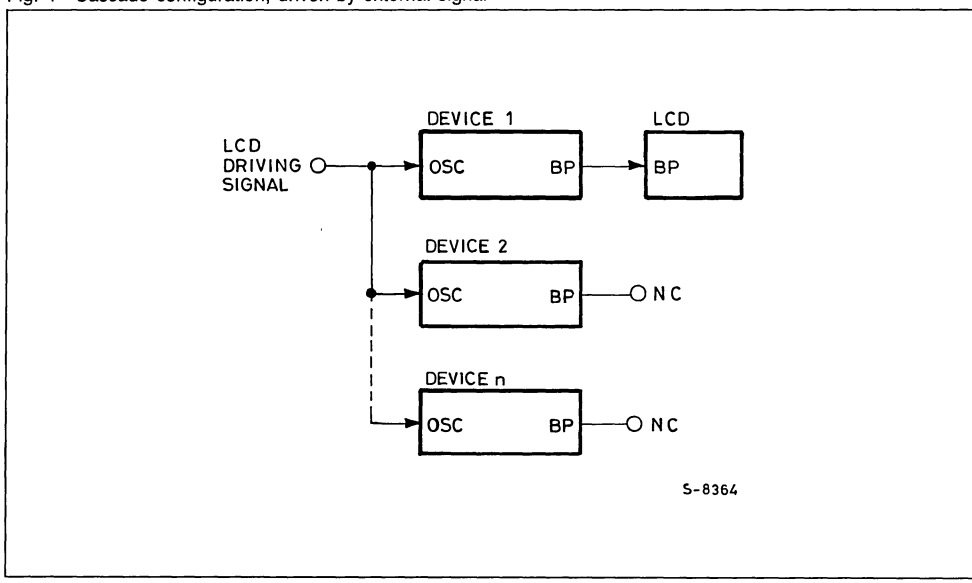


Fig. 4 - Cascade configuration, driven by external signal

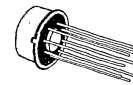


SGS-THOMSON MICROELECTRONICS

MC1458
MC1558

DUAL OPERATIONAL AMPLIFIERS

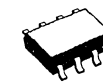
- LOW POWER CONSUMPTION
- LARGE INPUT VOLTAGE RANGE
- NO LATCH-UP
- HIGH GAIN
- SHORT-CIRCUIT PROTECTION
- NO FREQUENCY COMPENSATION REQUIRED



H
TO-99
(Metal Can)

GC
LCC20
(Tricecop (LCC))

N
DIP8
(Plastic Package)
J
CERDIP8
(Cerdip Package)



D
SO8
(Plastic Micropackage)

DESCRIPTION

The MC1458 is a high performance monolithic dual operational amplifier constructed on a single silicon chip. It is intended for a wide range of analog applications.

- Summing amplifier.
- Voltage follower.
- Integrator.
- Active filter.
- Function generator.

The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feed back applications. The internal compensation network (6 dB/octave) insures stability in closed loop applications.

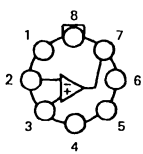
ORDER CODES

Part Number	Temperature Range	Package				
		H	N	J	D	GC
MC1458	0 to + 70 °C	•	•		•	
MC1458I	– 40 + 105 °C	•	•	•	•	
MC1558	– 55 to + 125 °C	•				•

Note : HI-Rel Versions Available
Example : MC1458H, MC1558GC.

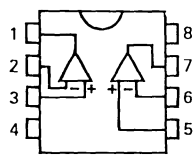
PIN CONNECTIONS (top views)

TO-99



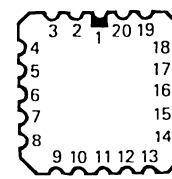
1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-

DIP8/CERDIP8/SO8



5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

LCC20



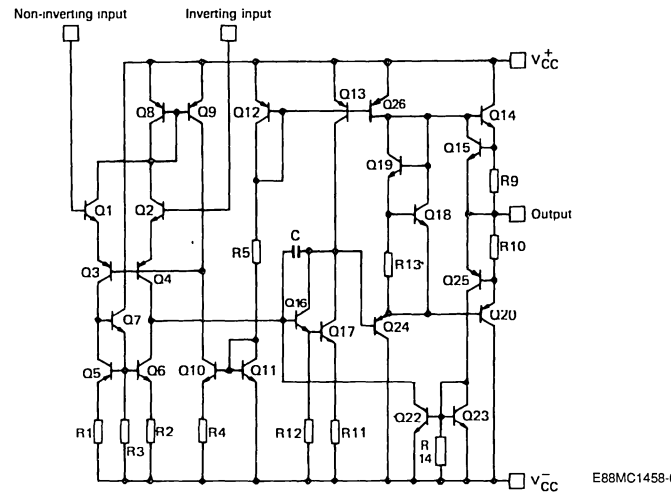
1 - NC
2 - Output 1
3 - NC
4 - NC
5 - Inverting input 1
6 - NC
7 - Non-inverting input 1
8 - NC
9 - NC
10 - V_{CC}^-

11 - NC
12 - Non-inverting input 2
13 - NC
14 - NC
15 - Inverting input 2
16 - NC
17 - Output 2
18 - NC
19 - NC
20 - V_{CC}^+

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		LM1458	LM1458I	LM1558	Unit
V_{CC}	Supply Voltage		± 22	± 22	± 22	V
V_I	Input Voltage		± 15	± 15	± 15	V
V_{ID}	Differential Input Voltage		± 30	± 30	± 30	V
P_{tot}	Power Dissipation	J Suffix		660		mW
		GC Suffix			665	
		H Suffix	660	660	660	
		D Suffix	300	300		
		N Suffix	500	500		
	Output Short-circuit Duration		Infinite			
T_{oper}	Operating Free-air Temperature Range		– 55 to + 125	– 40 to + 105	0 to + 70	°C
T_{stg}	Storage Temperature Range		– 65 to 150	– 65 to 150	– 65 to 150	°C

SCHEMATIC DIAGRAM



Case	Outputs	Non-inverting Inputs	Inverting Inputs	V_{CC}^+	V_{CC}^-
DIP8/CERDIP8	1-7	3-5	2-6	8	4
TO-99	1-7	3-5	2-6	8	4
SO8	1-7	3-5	2-6	8	4
LCC20*	2-17	7-12	5-15	20	10

* **LCC20 :** Other pins not connected

ELECTRICAL CHARACTERISTICS

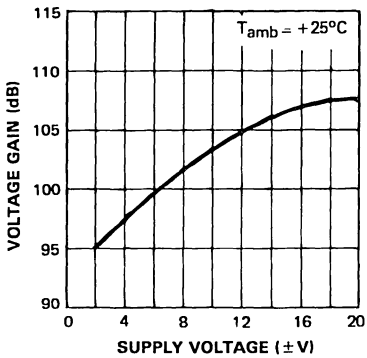
MC1458 : $0 \leq T_{amb} \leq +70$ °C $V_{CC} = \pm 15$ V
MC1458I: $-40 \leq T_{amb} \leq +105$ °C $V_{CC} = \pm 15$ V
MC1558 : $-55 \leq T_{amb} \leq +125$ °C $V_{CC} = \pm 15$ V
(unless otherwise specified)

Symbol	Parameter	MC1458 / 1458I / 1558			Unit
		Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage $R_S \leq 10$ kΩ $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$		1	5 6	mV
I_{IO}	Input Offset Current $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$		2	20 40	nA
I_{IB}	Input Bias Current $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$		30	100 200	nA
A_{VD}	Large Signal Voltage Gain ($V_O = \pm 10$ V, $R_L = 2$ kΩ) $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$	 50 25	 200		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S \leq 10$ kΩ) $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$	 77 77	 90		dB
I_{CC}	Supply Current, all Amp, no Load $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$		2.3	5 6	mA
V_I	Input Voltage Range $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$	 − 12 − 12		 + 12 + 12	V
CMR	Common-mode Rejection Ratio ($R_S \leq 10$ kΩ) $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$	 70 70	 90		dB
I_{OS}	Output Short-circuit Current $T_{amb} = 25$ °C	10	20	35	mA
$\pm V_{OPP}$	Output Voltage Swing $T_{amb} = 25$ °C $R_L = 10$ kΩ $R_L = 2$ kΩ $T_{min} \leq T_{amb} \leq T_{max}$ $R_L = 10$ kΩ $R_L = 2$ kΩ	 12 10 12 10	 14 13		V
S_{VO}	Slew-rate ($V_I = \pm 10$ V, $R_L = 2$ kΩ, $C_L \leq 100$ pF, $T_{amb} = 25$ °C, unity gain)	0.2	0.8		V/µs
t_r	Rise Time ($V_I = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF, $T_{amb} = 25$ °C, unity gain)		0.3		µs
K_{OV}	Overshoot ($V_I = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF, $T_{amb} = 25$ °C, unity gain)		5		%
R_I	Input Resistance, $T_{amb} = 25$ °C	0.3	2		MΩ
Zic	Common-mode Input Impedance		200		MΩ
C_I	Input Capacitance, $T_{amb} = 25$ °C		1.4		pF
R_O	Output Resistance, $T_{amb} = 25$ °C		75		Ω
Bom	Large Signal Bandwidth ($R_L = 2$ kΩ, $V_O \geq \pm 10$ V, $A_{VD} = 1$, THD ≤ 5 %)		14		KHz

ELECTRICAL CHARACTERISTICS (continued)

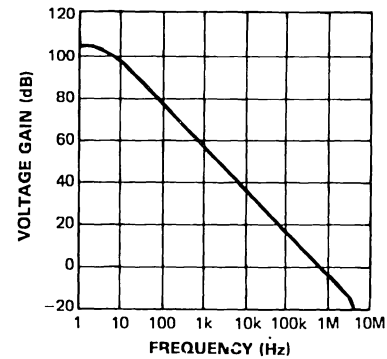
Symbol	Parameter	MC1458 / 1458I / 1558			Unit
		Min.	Typ.	Max.	
B	Unity Gain Bandwidth (V_I = 10 mV, R_L = 2 kΩ, $C_L \leq$ 100 pF, T_{amb} = 25 °C)		1		MHz
GPB	Gain Bandwidth Product (V_I = 10 mV, R_L = 2 kΩ, $C_L \leq$ 100 pF, f = 100 KHz, T_{amb} = 25 °C)	0.4	1		MHz
THD	Total Harmonic Distortion (f = 1 KHz, A_V = 20 dB, R_L = 2 kΩ, V_O = 2 V_{PP}, $C_L \leq$ 100 pF, T_{amb} = 25 °C)		0.02		%
V_n	Equivalent Input Noise Voltage (f = KHz, R_g = 100 Ω)		45		nV/√Hz
φM	Phase Margin		65		Degrees
Am	Gain Margin		11		dB

OPEN LOOP VOLTAGE GAIN



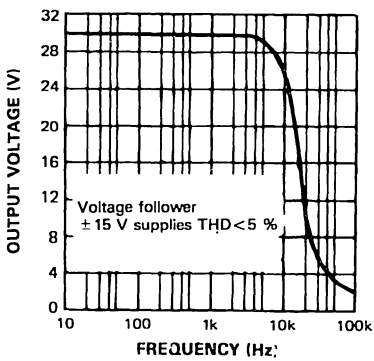
E88MC1458-02

OPEN LOOP FREQUENCY RESPONSE



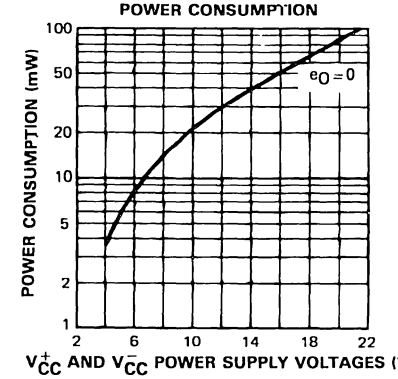
E88MC1458-03

POWER BANDWIDTH (LARGE SIGNAL SWING)



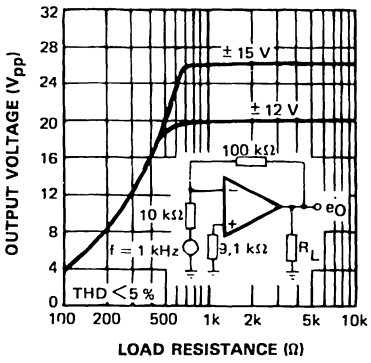
E88MC1458-04

POWER CONSUMPTION



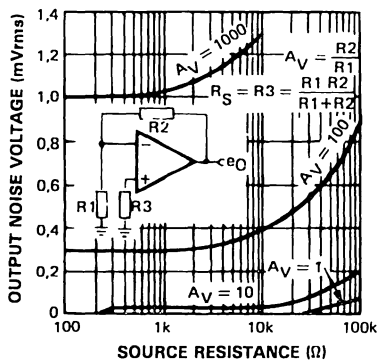
E88MC1458-05

OUTPUT VOLTAGE SWING



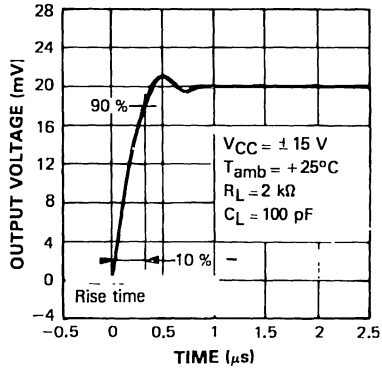
E88MC1458-06

OUTPUT NOISE VOLTAGE



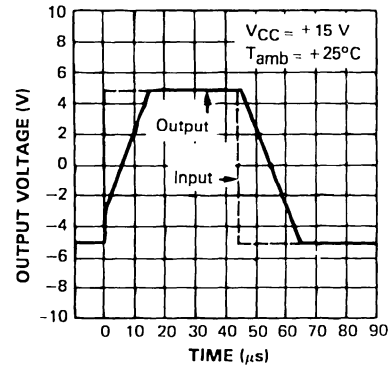
E88MC1458-07

TRANSIENT RESPONSE



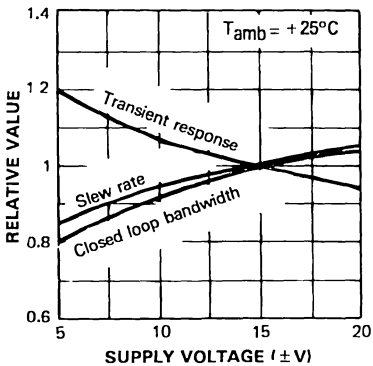
E88MC1458-08

VOLTAGE FOLLOWER
LARGE SIGNAL PULSE RESPONSE



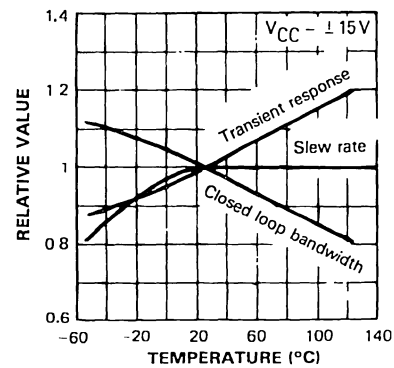
E88MC1458-09

FREQUENCY CHARACTERISTICS



E88MC1458-10

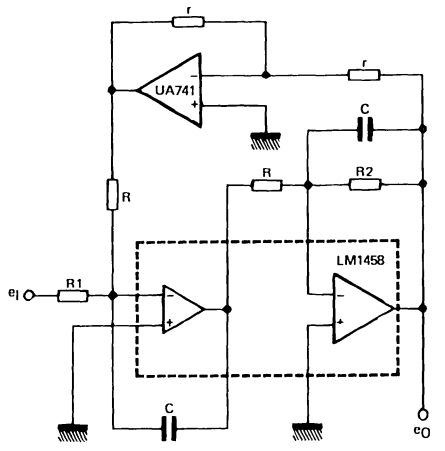
FREQUENCY CHARACTERISTICS



E88MC1458-11

TYPICAL APPLICATIONS

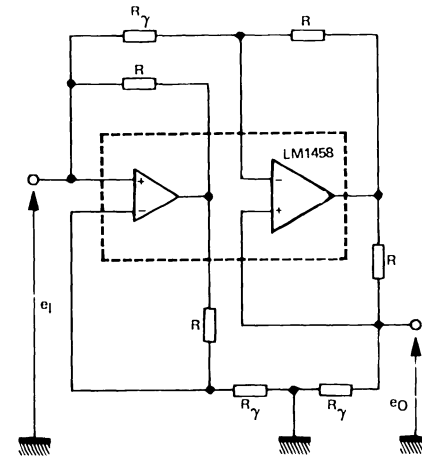
LOW PASS FILTER



$\omega_0 = \frac{1}{RC}$ $\xi = \frac{1\,R}{2\,R2}$ $A_V = \frac{R}{R1}$

E88MC1458-12

GYRATOR

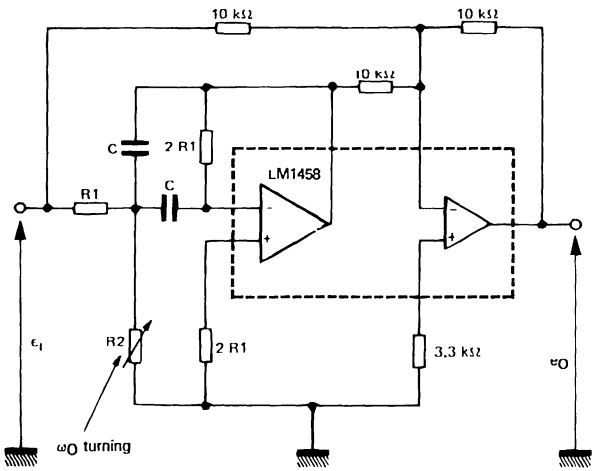


R_γ = Gyration resistance ($\geq$1.5 kΩ)

0 1 $R_\gamma \leq R \leq 0.5\ R_\gamma$

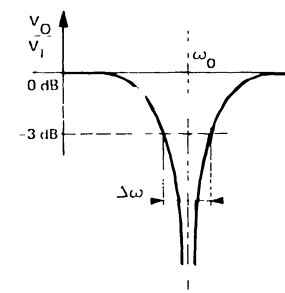
E88MC1458-13

TURNABLE NOTCH FILTER



$$\omega_0 = \frac{1}{C\sqrt{2\,R1\,\dfrac{R1\ R2}{R1 + R2}}}$$

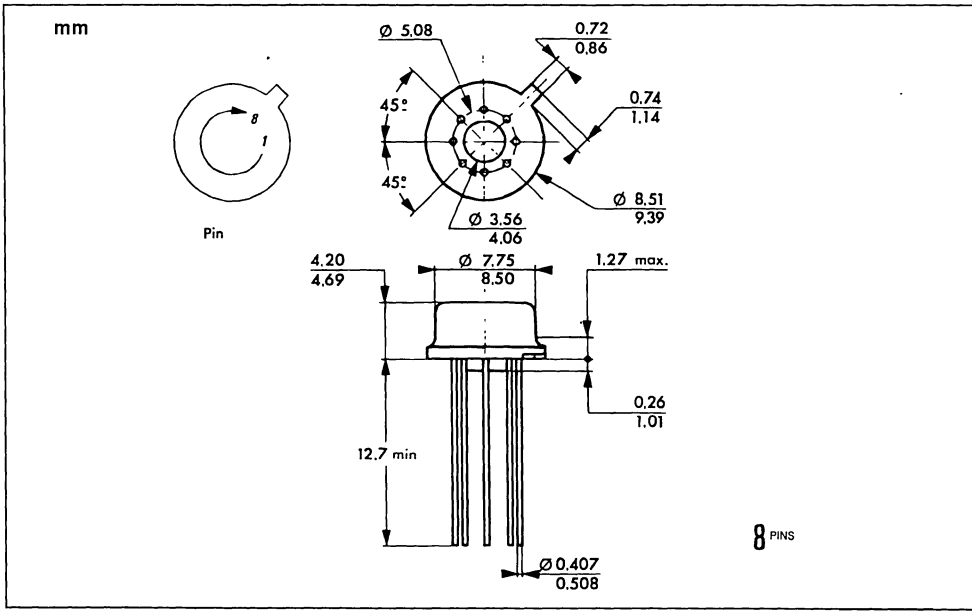
$$\Delta\omega = \frac{1}{CR1} \quad \text{(Bandwidth notched)}$$



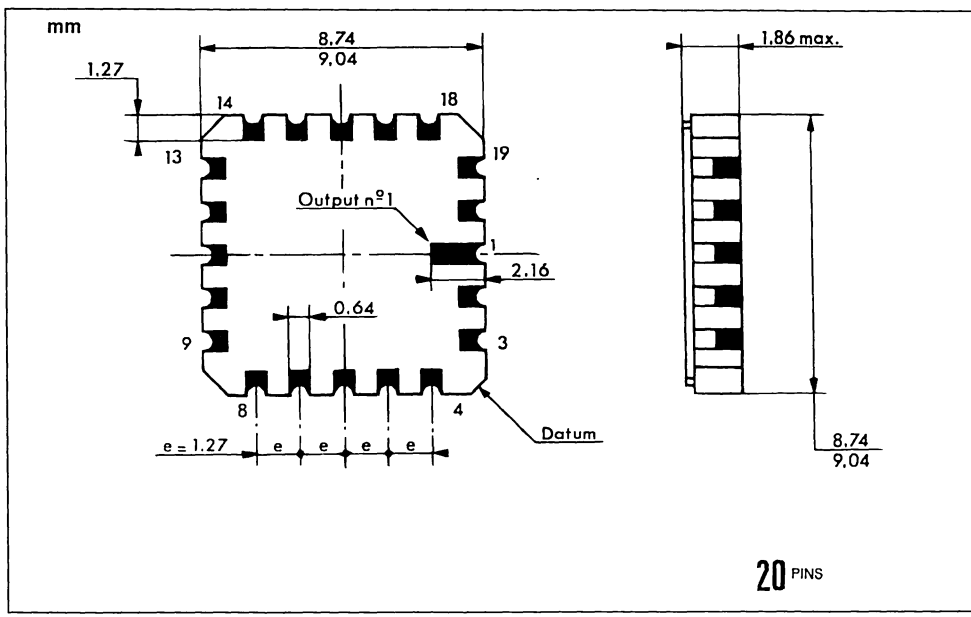
E88MC1458-14

PACKAGE MECHANICAL DATA

8 PINS – METAL CAN TO-99

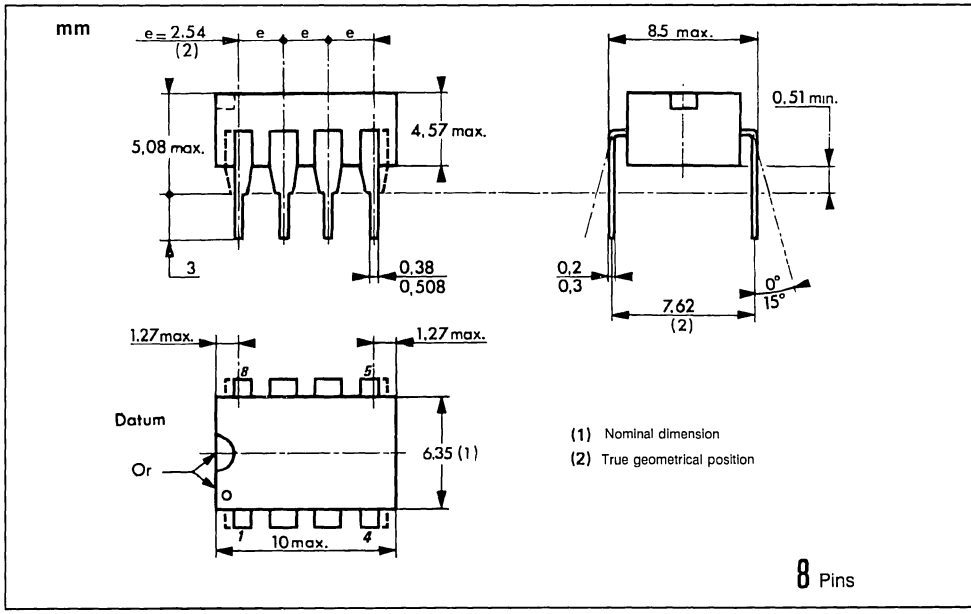


20 PINS – TRICECOP (LCC)

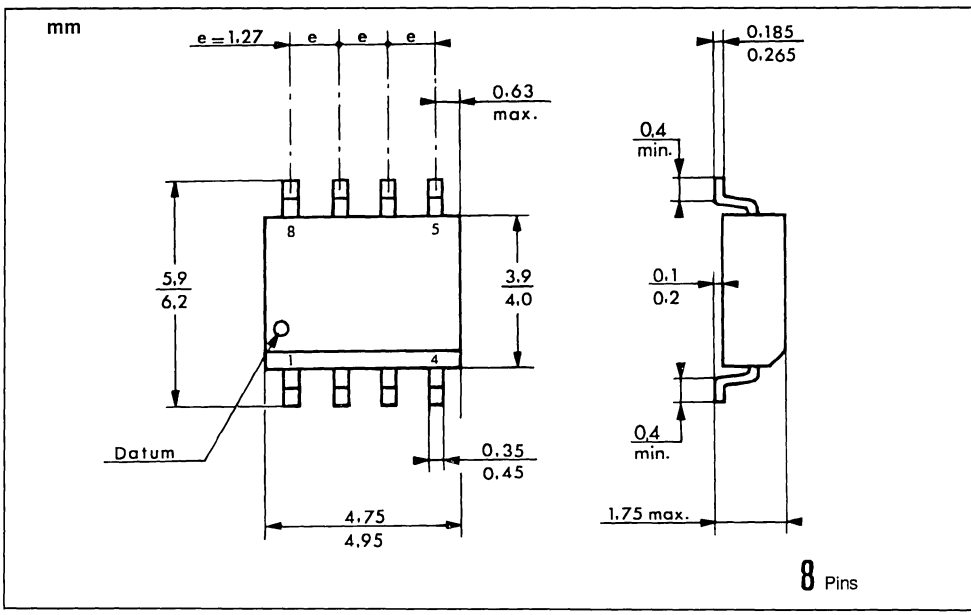


PACKAGE MECHANICAL DATA (continued)

8 PINS – PLASTIC DIP OR CERDIP

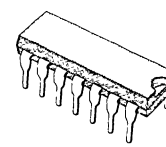


8 PINS – PLASTIC MICROPACKAGE (SO)

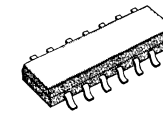


RS232C QUAD LINE DRIVER

- CURRENT LIMITED OUTPUT ± 10 mA TYP.
- POWER-OFF SOURCE IMPEDANCE 300 ΩMIN.
- SIMPLE SLEW RATE CONTROL WITH EXTERNAL CAPACITOR
- FLEXIBLE OPERATING SUPPLY RANGE
- INPUTS ARE TTL AND μP COMPATIBLE



DIP-14 (0.25)
(Plastic and Ceramic)



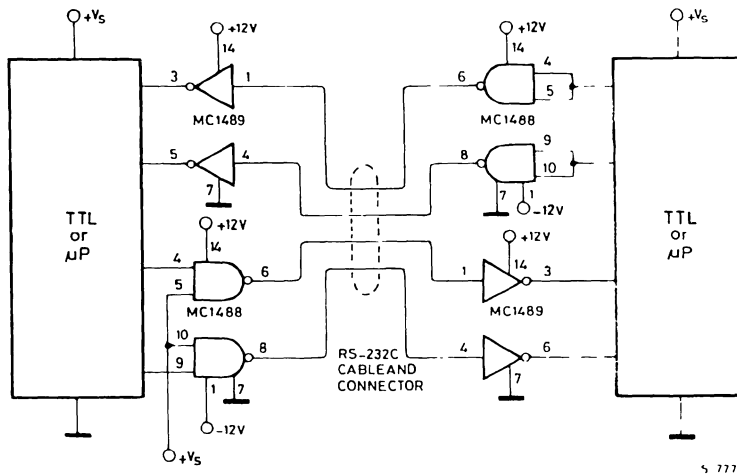
SO-14J

ORDER CODES : MC1488P (Plastic DIP)
MC1488L (Ceramic DIP)
MC1488D (SO-14)

DESCRIPTION

The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS232C.

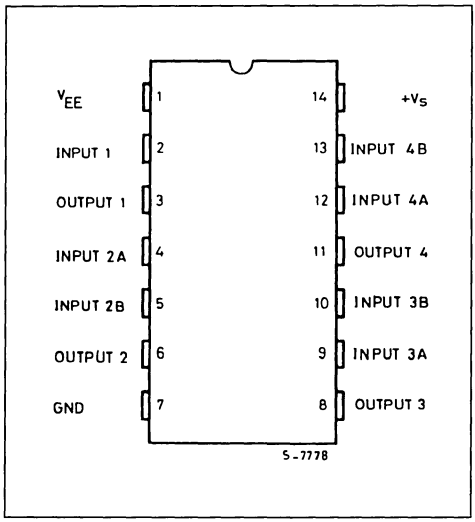
TYPICAL APPLICATION : RS232C Data Transmission.



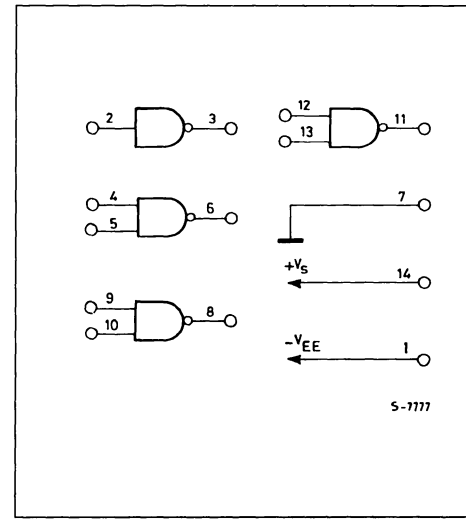
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Power Supply Voltage	15	V
V_{EE}	Power Supply Voltage	– 15	V
V_{IR}	Input Voltage Range	$-15 \leq V_{IR} \leq 7$	V
V_O	Output Signal Voltage	± 15	V
T_{amb}	Operating Ambient Temperature	0 to 75	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C

CONNECTION DIAGRAMS (top views)



LOGIC DIAGRAM



THERMAL DATA

			Plastic DIP - 14	Ceramic DIP - 14	SO - 14
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	max	200 °C/W	165 °C/W	165 °C/W

ELECTRICAL CHARACTERISTICS (V_S= 9 ±10 % V, V_{EE}= − 9 ±10 % V, T_{amb}= 0 to 75 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{IL}	Input Current	Low Logic State (V_{IL} = 0V)		1	1.6	mA	1
I_{IH}	Input Current	High Logic State (V_{IH} = 5V)			10	µA	1
V_{OH}	Output Voltage	High Logic State R_L= 3KΩ V_{IL} = 0.8V, V_S = 9V, V_{EE} = −9V V_{IL} = 0.8V, V_S = 13.2V, V_{EE} = −13.2V	 6 9	 7 10.5		 V V	 2 2
V_{OL}	Output Voltage	Low Logic State R_L = 3 KΩ V_{IH} = 1.9V, V_{EE} = −9V, V_S = 9V V_{IH} = 1.9V, V_{EE} = −13.2V, V_S = 13.2V	 − 6 − 9	 − 7 − 10.5		 V V	 2 2
I_{OS+} *	Positive Output Short - circuit Current		6	10	12	mA	3
I_{OS-} *	Negative Output Short-circuit Current		− 6	− 10	− 12	mA	3
R_O	Output Resistance	V_S = V_{EE} = 0 |Vo| = ± 2V	300			Ω	4
I_s	Positive Supply Current (R_l = ∞)	V_{IH} = 1.9 V V_S = 9 V V_{IL} = 0.8 V V_S = 9 V V_{IH} = 1.9 V V_S = 12 V V_{IL} = 0.8 V V_S = 12 V V_{IH} = 1.9 V V_S = 15 V V_{IL} = 0.8 V V_S = 15 V		15 4.5 19 5.5	20 6 25 7 34 12	mA	5
I_{EE}	Negative Supply Current (R_L = ∞)	V_{IH} = 1.9 V V_{EE} = − 9 V V_{IL} = 0.8 V V_{EE} = − 9 V V_{IH} = 1.9 V V_{EE} = − 12 V V_{IL} = 0.8 V V_{EE} = − 12 V V_{IH} = 1.9 V V_{EE} = − 15 V V_{IL} = 0.8 V V_{EE} = − 15 V		− 13 − 18	− 17 − 15 − 23 − 15 − 34 − 2.5	mA µA mA µA mA mA	5
P_c	Power Consumption	V_S = 9 V V_{EE} = − 9 V V_S = 12 V V_{EE} = − 12 V			333 567	mW	

SWITCHING CHARACTERISTICS (V_S = ± 9 ±1 % V, V_{EE} = − 9 ± 1 % V, T_{amb} = 25 °C)

t_{PLH}	Propagation Delay Time	Z_l = 3 KΩ and 15 pF		275	350	ns	6
t_{THL}	Fall Time	Z_l = 3 KΩ and 15 pF		45	75	ns	6
t_{PHL}	Propagation Delay Time	Z_l = 3 KΩ and 15 pF		110	175	ns	6
t_{TLH}	Rise Time	Z_l = 3 KΩ and 15 pF		55	100	ns	6

* Maximum package power dissipation may be exceeded if all outputs are shorted simultaneously

TEST CIRCUITS

Figure 1 : Input Current.

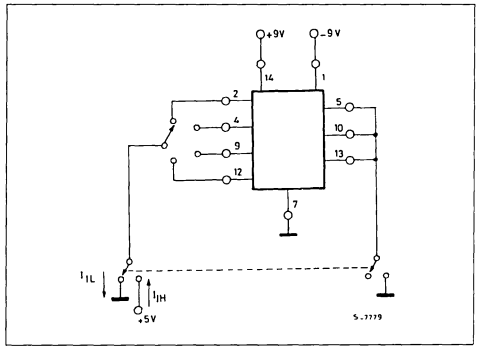


Figure 2 : Output Voltage.

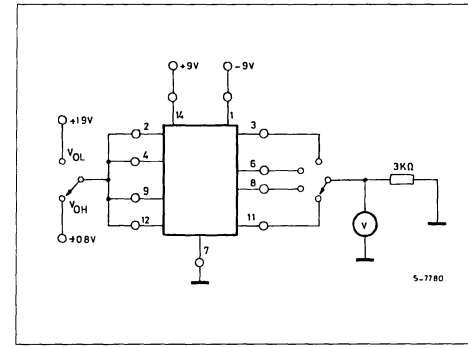


Figure 3 : Output Short-Circuit Current.

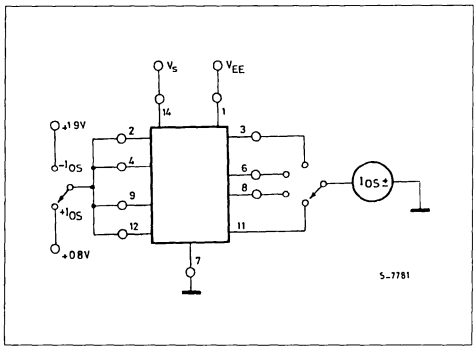


Figure 4 : Output Resistance (power off).

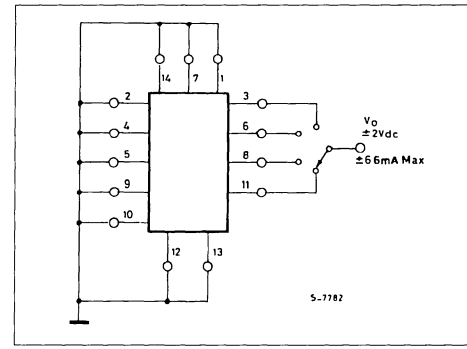


Figure 5 : Power Supply Currents.

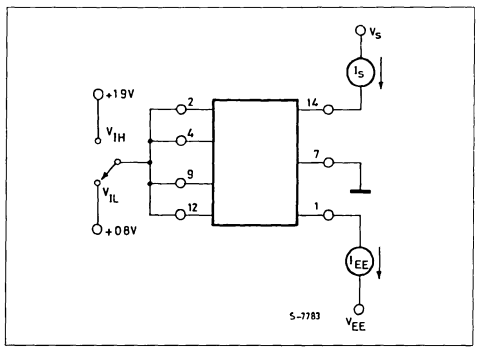


Figure 6 : Switching Response.

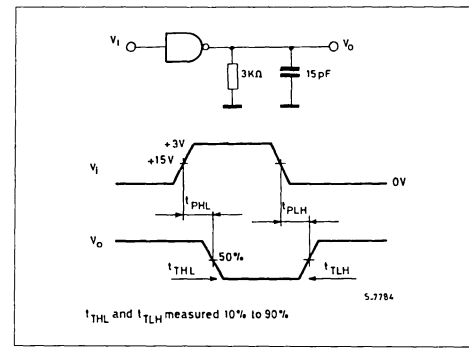


Figure 7 : Transfer Characteristics vs. Power Supply Voltage.

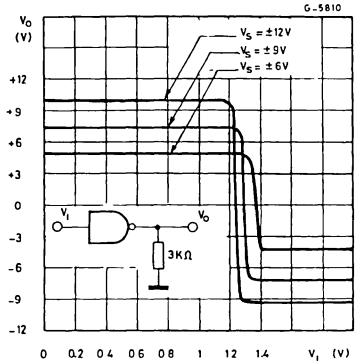


Figure 8 : Short-Circuit Output Current vs. Temperature.

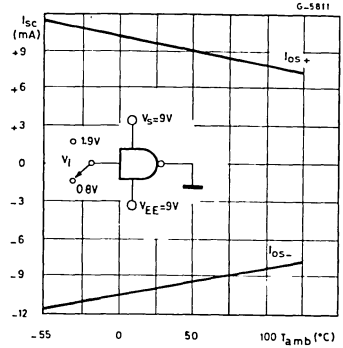


Figure 9 : Output Slew-Rate Load Capacitance.

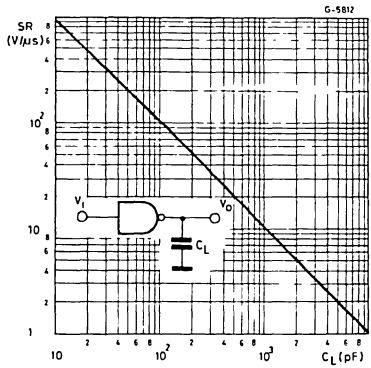


Figure 10 : Output Voltage and Current-Limiting Characteristics.

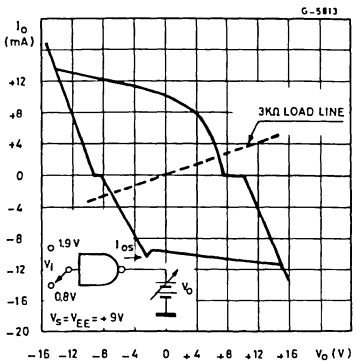
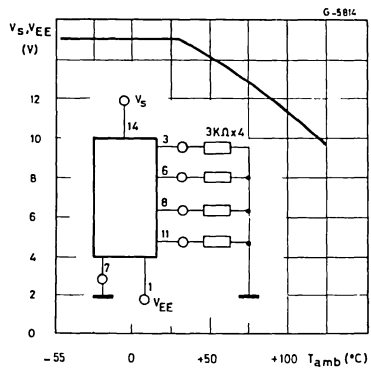


Figure 11 : Maximum Operating Temperature vs. Power-Supply Voltage.



APPLICATION INFORMATION

The Electronic Industries Association (EIA) has released the RS232C specification detailing the requirements for the interface between data processing equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined levels. The RS232C requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15 V in magnitude and are positive for a logic "0" and negative for a logic "1". These voltages are so defined when the drivers are terminated with a 3000 to 7000Ω resistor. The MC1488 meets this voltage requirement by converting a DTL/TTL logic level into RS232C levels with one stage of inversion.

The RS232C specification further requires that during transitions, the driver output slew rate must not exceed 30 V per µs. The inherent slew rate of the MC1488 is much too fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{OS} \times \Delta T / \Delta V$ from which Figure 12 is derived. Accordingly, a 330 pF capacitor on each output will guarantee a worst case slew rate of 30 V per µs.

The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15 V, 500 mA source. The MC1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0 V (i.e., VS ≥ 9.0 V ; $V_{EE} \leq$ - 9.0 V). In some power-supply designs, a loss of system power causes a low impedance on the power-supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488 effectively shorting the 300Ω output resistor to ground. If **all four outputs** were then shorted to plus or minus 15 V, the power dissipation in these resistors would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power-suppies of the drivers, a diode should be placed in each power-supply lead to prevent over-heating in this fault condition. These two diodes, as shown in Figure 13, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488 to withstand momentary shorts to the ±15 V limits specified in the earlier Standard RS232B). The addition of the diodes also permits the MC1488 to withstand faults with power-supplies of less than the 9.0 V stated above.

The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10 mA output current limiting.

Figure 12 : Slew Rate vs. Capacitance for I_{SC} = 10mA.

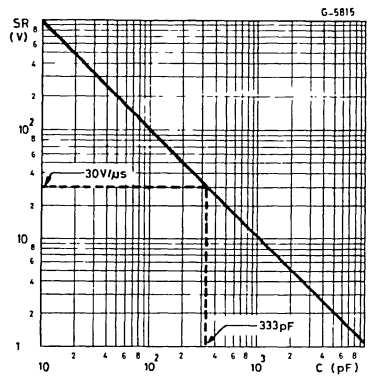
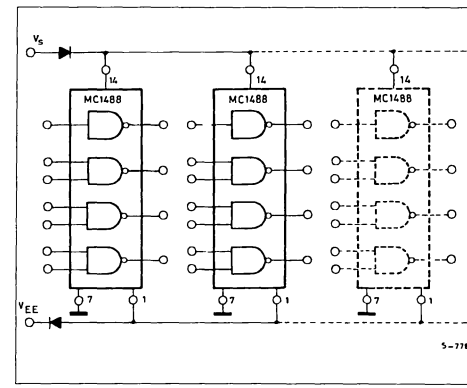


Figure 13 : Power Supply Protection to Meet Power-off Fault Conditions.



OTHER APPLICATION

The MC1488 is an extremely versatile line driver with a miriad of possible applications. Several features of the drivers enhance this versatility :

1. Output Current Limiting - this enables the circuit designer to define the ouptut voltage levels independent of power-supplies and can be accomplished by diode clamping of the output pins.

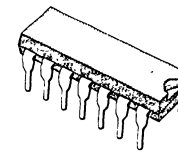
2. Power-Supply Range - as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power-supplies. In fact, the positive supply can very from a minimum seven volts (required for driving the negative pulldown section) to the maximum specified 15 V. The negative supply can vary from approximately - 2.5 V to the minimum specified - 15 V. The MC1488 will drive the ouptut to within 2 V of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current-limiting and supply-voltage features allow a wide combination of possible outputs within the same quad package.

SGS-THOMSON
MICROELECTRONICS

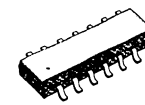
MC1489
MC1489A

QUAD LINE RECEIVERS

- INPUT RESISTANCE –3.0 K to 7.0 KΩ
- INPUT SIGNAL RANGE – ± 30 V
- INPUT THRESHOLD HYSTERESIS BUILT-IN
- RESPONSE CONTROL :
  a) LOGIC THRESHOLD SHIFTING
  b) INPUT NOISE FILTERING



DIP-14
(Plastic (0.25) and Ceramic)



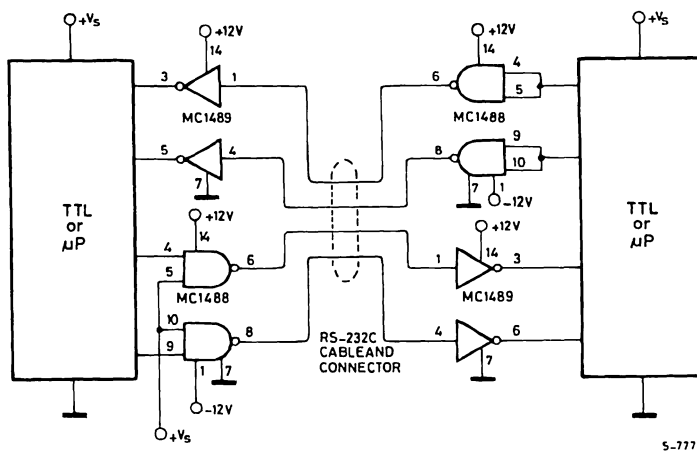
SO-14J

ORDER CODES : MC1489L, MC1489AL
(DIP–14 Ceramic)
MC1489P, MC1489AP
(DIP–14 Plastic)
MC1489D, MC1489AD (SO-14)

DESCRIPTION

The MC1489 monolithic quad line receivers are designed to interface data therminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

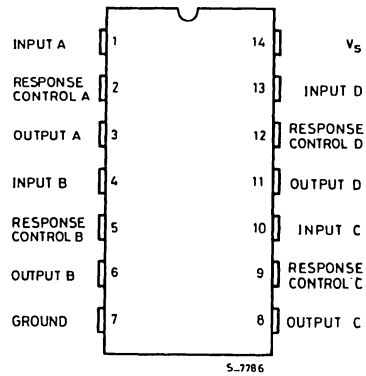
TYPICAL APPLICATION : RS232C Data Transmission



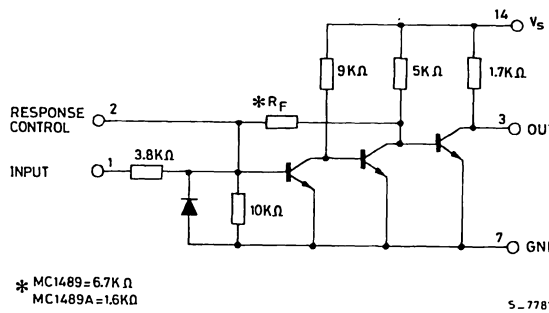
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Power Supply Voltage	10	V
V_I	Input Voltage Range	± 30	V
I_{OL}	Output Load Current	20	mA
P_{tot}	Power Dissipation	1	W
T_{amb}	Operating Ambient Temperature	0 to 75	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C

CONNECTION DIAGRAMS (top view)



SCHEMATIC DIAGRAM (1/4 of circuit shown)



ELECTRICAL CHARACTERISTICS (Response control pin is open ; V_S = 5 V, T_{amb} = 0 to 75 ° C unless otherwise specified)

Symbol	Parameter	Test Condtions	Min.	Typ.	Max.	Unit
I_{IH}	Positive Input Current	V_{IH} = 25 V V_{IH} = 3 V	3.6 0.43		8.3	mA
I_{IL}	Negative Input Current	V_{IL} = - 25 V V_{IL} = - 3 V	- 3.6 - 0.43		- 8.3	mA
V_{IH}	Input Turn-on Threshold Voltage	T_{amb} = 25 ° C $V_{OL} \leq$ 0.45 I_L = 10 mA for **MC1489** for **MC1489A**	1 1.75	1.95	1.5 2.25	V
V_{IL}	Input Turn-off Threshold Voltage	T_{amb} = 25 ° C $V_{OH} \geq$ 2.5 V I_L = - 0.5 mA	0.75		1.25	V
V_{OH}	Ouptut Voltage High	V_{IH} = 0.75 V I_L = - 0.5 mA I_L = 0.5 mA Input Open Circuit	2.5 2.5	4 4	5 5	V V
V_{OL}	Output Voltage Low	V_{IL} = 3 V I_L = 10 mA		0.2	0.45	V
I_{OS}	Output Short Circuit Current			- 3	- 4	mA
I_S	Power Supply Current	All gates "on" I_O = 0 mA V_{IH} = 5 V		16	26	mA
P_C	Power Consumption	V_{IH} = 5 V		80	130	mW

SWITCHING CHARACTERISTICS (V_S = 5 V, T_{amb} = 25 ° C, see Fig. 1)

Symbol	Parameter	Test Condtions	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation delay Time	R_L = 3.9 KΩ		25	85	ns
t_{TLH}	Rise Time	R_L = 3.9 KΩ		120	175	ns
t_{PHL}	Propagation Delay Time	R_L = 390 Ω		25	50	ns
t_{THL}	Fall Time	R_L = 390 Ω		10	20	ns

TEST CIRCUITS

Figure 1 : Switching Response.

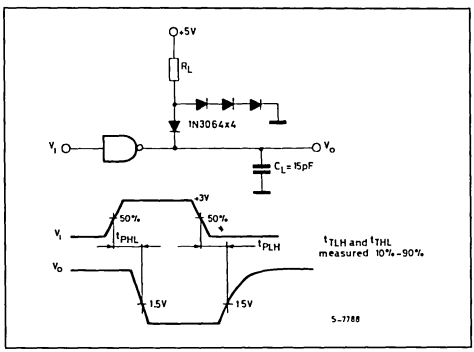
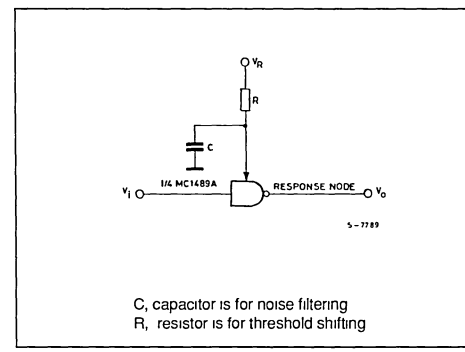


Figure 2 : Response Control Node.



C, capacitor is for noise filtering
R, resistor is for threshold shifting

Figure 3 : Input Current.

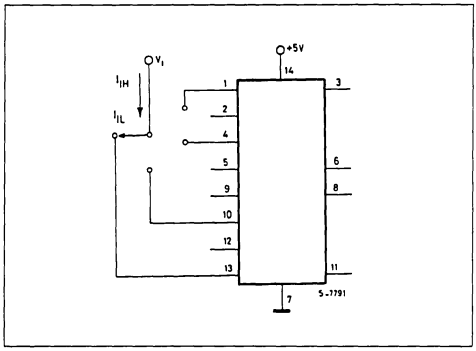


Figure 4 : Output Short-Circuit Current.

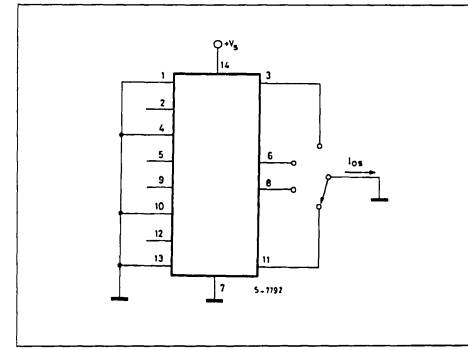


Figure 5 : Output Voltage and Input Threshold Voltage.

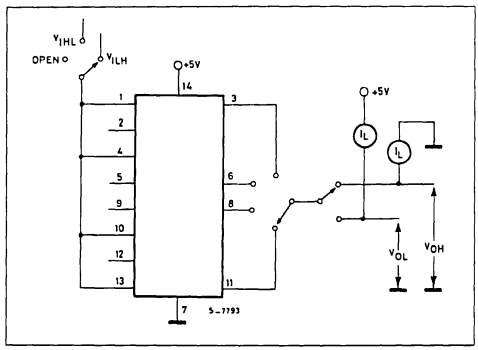
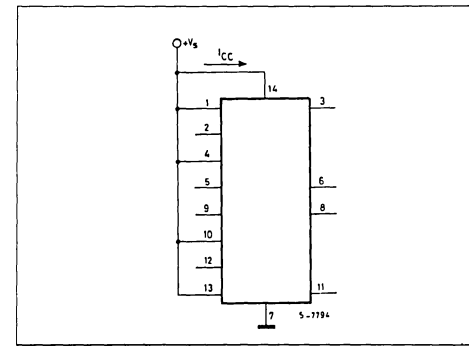


Figure 6 : Power Supply Current.



TYPICAL CHARACTERISTICS (V_S = 5 V, T_{amb} = 25 °C unless otherwise specified)

Figure 7 : Input Current.

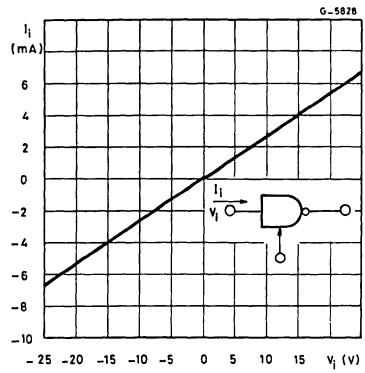


Figure 8 : MC1489 Input Threshold Voltage Adjustament.

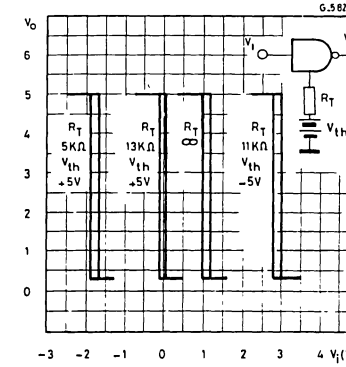


Figure 9 : MC1489A Input Threshold Voltage Adjustment.

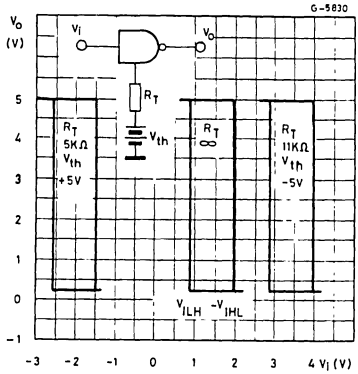


Figure 10 : Input Threshold Voltage vs. Temperature.

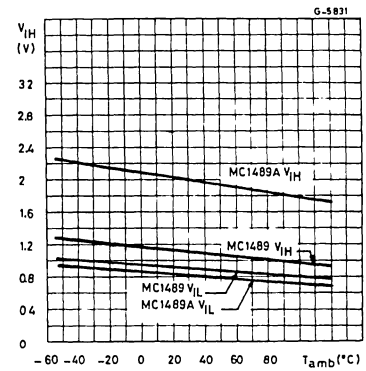
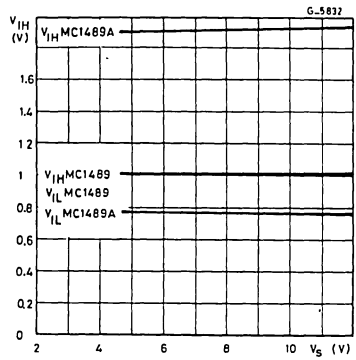


Figure 11 : Input Threshold vs. Power-Supply Voltage.



APPLICATION INFORMATION

GENERAL INFORMATION

The Electronic Industries Association (EIA) has released the RS-232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS-232C defined levels. The RS-232C requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000 Ω and 7000 Ω for input voltages between 3.0 and 25 V in magnitude ; and any voltage on the receiver input in an open circuit condition must be less than 2.0 V in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one V_{BE}.

The receiver shall detect a voltage between - 3.0 and - 25 V as a Logic "1" and inputs between + 3.0 and + 2.5 V as a Logic "0". On some interchange leads, an open circuit of power "OFF" condition (300 Ω or more to ground) shall be decoded as an "OFF" condition or Logic "1". For the reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or Logic "1" input.

DEVICE CHARACTERISTICS

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical turn-on voltage of 1.25 V and turn-off of 1.0 V for a typical hysteresis of 250 mV. The MC1489A has typical turn-on of 1.95 V and turn-off of 0.8 V for typically 1.15 V of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and and an external power supply. Figure 2, 4 and 5 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of the high-frequency, high-energy noise pulses. Figure 8 and 9 show typical noise-pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for may combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted. (with the appropiate supply and resistor values) to fall in the center of the MOS voltage logic levels. (See Figure 10).

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 11 where two receivers are slaved to the same line that must still meet the RS-232C impedance requirement.

Figure 12 : Typical Turn-on Threshold vs. Capacitance from Response Control Pin to GND.

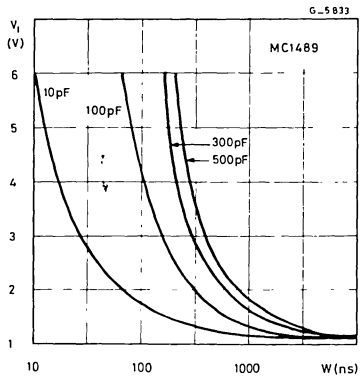


Figure 13 : Typical Turn-on Threshold vs. Capacitance from Response Control Pin to GND.

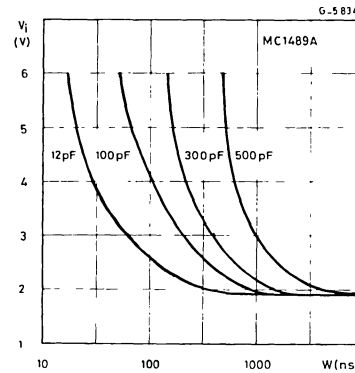
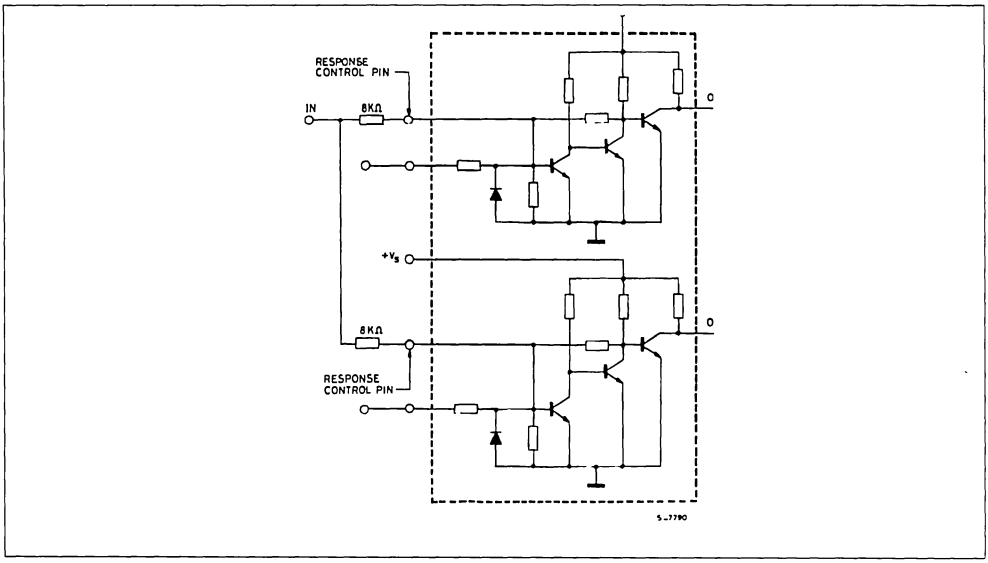
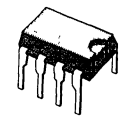


Figure 14: Typical Paralleling of Two MC1489/A Receivers to Meet RS-232C.

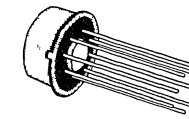


J–FET INPUT SINGLE OP–AMPs

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J–FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 13 V/µs (typ)



N
DIP8
(Plastic package)



H
TO99
(Metal can)

GC
LCC20
(Tricecop (LCC))

D
SO8
(Plastic micropackage)

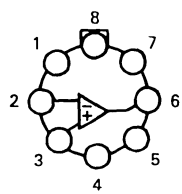
DESCRIPTION

These circuits are high speed J–FET input single operational amplifiers incorporating well matched, high voltage J–FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset current, and low offset voltage temperature coefficient.

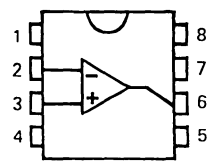
PIN CONNECTIONS (Top views)

TO99

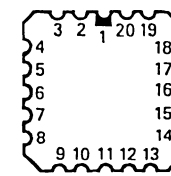


1 - Balance
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - Balance
6 - Output
7 - V_{CC}^+
8 - NC

DIP SO8



LCC20



1 - NC	11 - NC
2 - Balance	12 - Balance
3 - NC	13 - NC
4 - NC	14 - NC
5 - Inverting input	15 - Output
6 - NC	16 - NC
7 - Non-inverting input	17 - V_{CC}^+
8 - NC	18 - NC
9 - NC	19 - NC
10 - V_{CC}^-	20 - NC

ORDER CODES

Part Number	Temperature	Package
MC35001GC	– 55 °C to + 125 °C	LCC
MC35001AGC	– 55 °C to + 125 °C	LCC
MC35001BGC	– 55 °C to + 125 °C	LCC
MC35001H	– 55 °C to + 125 °C	METAL CAN
MC35001AH	– 55 °C to + 125 °C	METAL CAN
MC35001BH	– 55 °C to + 125 °C	METAL CAN
MC33001N	– 40 °C to + 105 °C	DIP8
MC33001AN	– 40 °C to + 105 °C	DIP8
MC33001BN	– 40 °C to + 105 °C	DIP8
MC33001D	– 40 °C to + 105 °C	SO8
MC33001AD	– 40 °C to + 105 °C	SO8
MC33001BD	– 40 °C to + 105 °C	SO8
MC34001N	0 °C to + 70 °C	DIP8
MC34001AN	0 °C to + 70 °C	DIP8
MC34001BN	0 °C to + 70 °C	DIP8
MC34001D	0 °C to + 70 °C	SO8
MC34001AD	0 °C to + 70 °C	SO8
MC34001BD	0 °C to + 70 °C	SO8

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	± 18	V
V_I	Input Voltage (note 3)	± 15	V
V_{CC}	Diff. Input Voltage (note 2)	± 30	V
P_{tot}	Power Dissipation	680	mW
	Output Short-circuit Duration (note 4)	Infinite	
T_{oper}	Operating Free Air Temperature Range MC34001, A, B MC33001, A, B MC35001, A, B	 0 to 70 – 40 to 105 – 55 to 125	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C

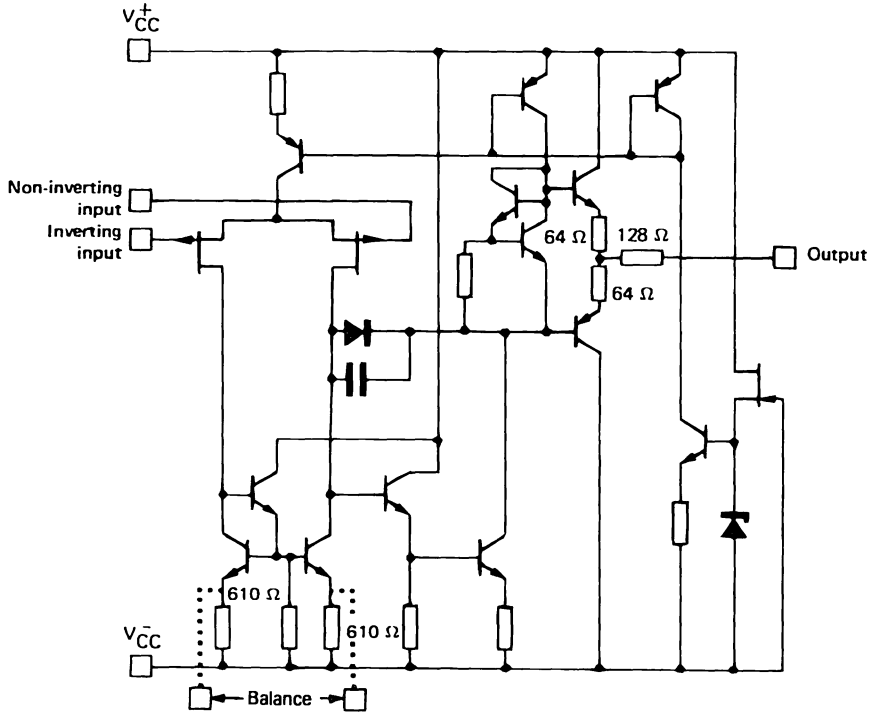
Notes : 1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.

2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.

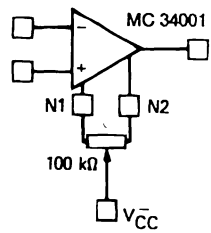
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.

4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

SCHEMATIC DIAGRAM



INPUT OFFSET VOLTAGE NULL CIRCUITS



E88MC34001-01

Case	Balance	Inverting Input	Non-inverting Input	Output	V_{CC}^{+}	V_{CC}^{-}	N.C.
DIP8 SO8 TO99	1, 5	2	3	6	7	4	8
LCC20	2, 12	5	7	15	17	10	*

* **LCC20** : Other pins are not connected.

ELECTRICAL CHARACTERISTICS

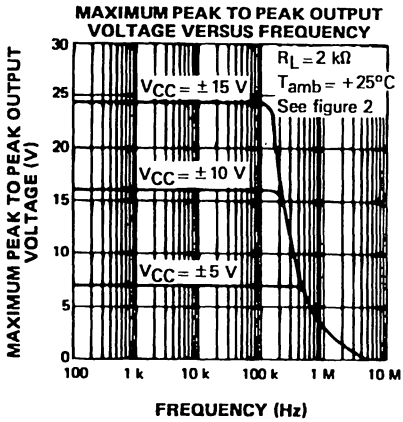
$V_{CC} = \pm 15$ V (unless otherwise specified)
MC35001, MC35001A, MC35001B $-55 \leq T_{amb} \leq +125$ °C
MC33001, MC33001A, MC33001B $-40 \leq T_{amb} \leq +105$ °C
MC34001, MC34001A, MC34001B $0 \leq T_{amb} \leq +70$ °C

Symbol	Parameter	MC35001A, B MC33001A, B MC34001A, B			MC35001 MC33001 MC34001			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage							mV
	T_{amb} = 25 °C (R_S < 10 kΩ)					3	8	
	MC35001B, MC34001B, MC33001B		3	5				
	MC35001A, MC34001A, MC33001A		0.2	1				
	$T_{min} \leq T_{amb} \leq T_{max}$						13	
	MC35001B, MC34001B, MC33001B			9				
	MC35001A, MC34001A, MC33001A			5				
DV_{IO}	Input Offset Voltage Drift		10			10		µV/°C
I_{IO}	Input Offset Current *							
	T_{amb} = 25 °C		5	50		5	50	pA
	$T_{min} \leq T_{amb} \leq T_{max}$			4			4	nA
I_{IB}	Input Bias Current *							
	T_{amb} = 25 °C		20	200		20	200	pA
	$T_{min} \leq T_{amb} \leq T_{max}$			20			20	nA
A_{VD}	Large Signal Voltage Gain							V/mV
	(R_L > 2 kΩ, $V_o = \pm 10$ V)							
	T_{amb} = 25 °C	50	200		50	200		
	$T_{min} \leq T_{amb} \leq T_{max}$	25			25			
SVR	Supply Voltage Rejection Ratio							dB
	(R_s < 10 kΩ)							
	T_{amb} = 25 °C	80	86		80	86		
	$T_{min} \leq T_{amb} \leq T_{max}$	80			80			
I_{CC}	Supply Current, No Load							mA
	T_{amb} = 25 °C		1.4	2.5		1.4	2.5	
	$T_{min} \leq T_{amb} \leq T_{max}$			2.5			2.5	
V_I	Input Voltage Range							V
	T_{amb} = 25 °C	− 11		+ 11	− 11		+ 11	
	$T_{min} \leq T_{amb} \leq T_{max}$							
CMR	Common Mode Rejection Ratio							dB
	(R_s < 10 kΩ)							
	T_{amb} = 25 °C	80	86		70	86		
	$T_{min} \leq T_{amb} \leq T_{max}$	80			70			
I_{OS}	Output Short-circuit Current							mA
	T_{amb} = 25 °C	10	40	60	10	40	60	
	$T_{min} \leq T_{amb} \leq T_{max}$	10		60	10		60	
$\pm V_{OPP}$	Output Voltage Swing							V
	T_{amb} = 25 °C $R_L \geq 2$ kΩ	11	12		11	12		
	$R_L \geq 10$ kΩ	12	13.5		12	13.5		
	$T_{min} \leq T_{amb} \leq T_{max}$ $R_L \geq 2$ kΩ	11			11			
	$R_L \geq 10$ kΩ	12			12			
S_{VO}	Slew-rate (V_I = 10 V, R_L = 2 kΩ)							V/µs
	$C_L \leq 100$ pF, T_{amb} = 25 °C, unity gain	12	16		12	16		

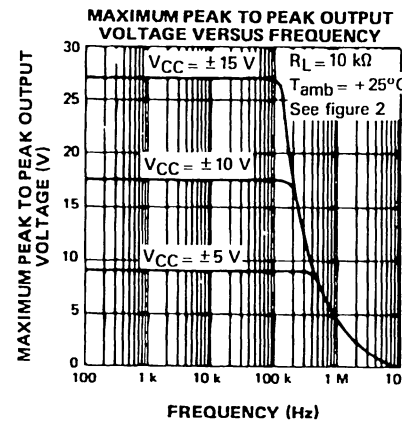
* The input bias currents are junction leakage currents wich approximatively double for every 10 °C increase in the junction temperature.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	MC34001A, B MC33001A, B MC35001A, B			MC34001 MC33001 MC35001			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_r	Rise Time (V_I = 20 mV, R_L = 2 kΩ) C_L = 100 pF, T_{amb} = 25 °C, unity gain		0.1			0.1		µs
K_{OV}	Overshoot (V_I = 20 mV, R_L = 2 kΩ $C_L \leq$ 100 pF, T_{amb} = 25 °C, unity gain)		10			10		%
GBP	Gain Bandwidth Product (f = 100 kHz, T_{amb} = 25 °C V_{IN} = 10 mV, R_L = 2 kΩ, C_L = 100 pF)	3.3	4.0	5.0	3.3	4.0	5.0	MHz
R_I	Input Resistance (T_{amb} = 25 °C)		10^{12}			10^{12}		Ω
THD	Total Harmonic Distortion (f = 1 kHz, A_V = 20 dB, R_L = 2 KΩ $C_L \leq$ 100 pF, T_{amb} = 25 °C, V_O = 2 V_{PP})		0.01			0.01		%
V_n	Equivalent Input Noise Voltage (f = 1 kHz, R_g = 100 Ω)		15			15		nV/√Hz
Øm	Phase Margin		45			45		Degrees

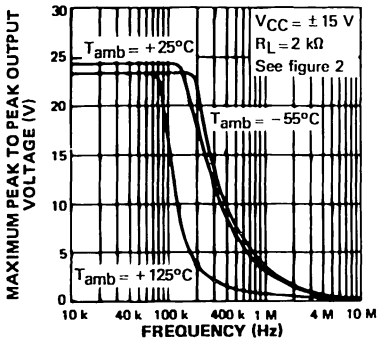


E88MC34001-02



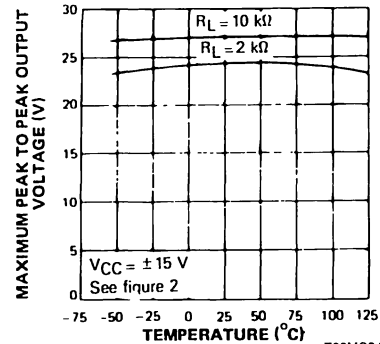
E88MC34001-03

MAXIMUM PEAK TO PEAK OUPUT VOLTAGE VERSUS FREE-AIR TEMP.



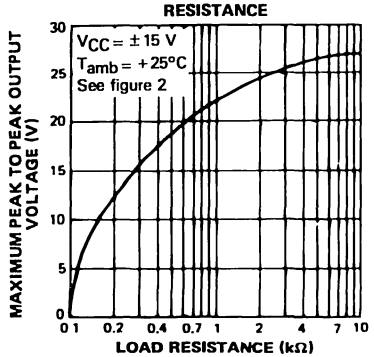
E88MC34001-04

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



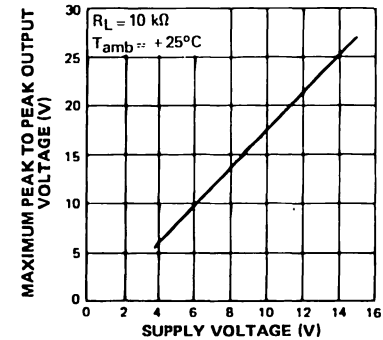
E88MC34001-05

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



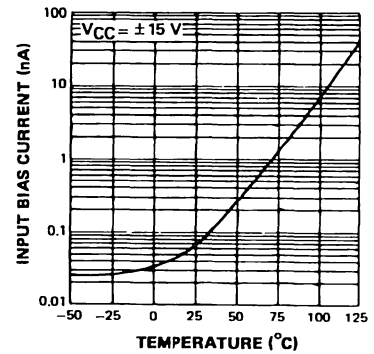
E88MC34001-06

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



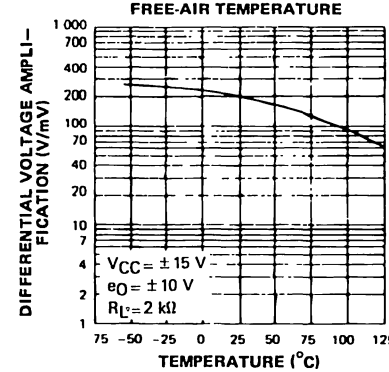
E88MC34001-07

INPUT BIAS CURRENT VERSUS FREE-AIR TEMPERATURE



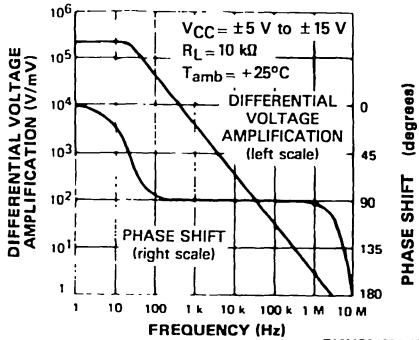
E88MC34001-08

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE-AIR TEMPERATURE



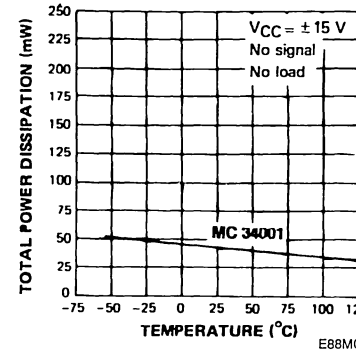
E88MC34001-09

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



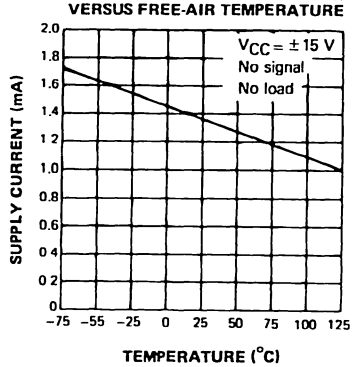
E88MC34001-10

TOTAL POWER DISSIPATION VERSUS FREE-AIR TEMPERATURE



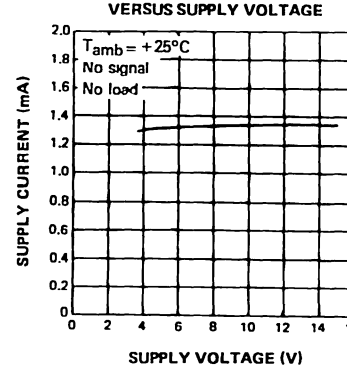
E88MC34001-11

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE-AIR TEMPERATURE



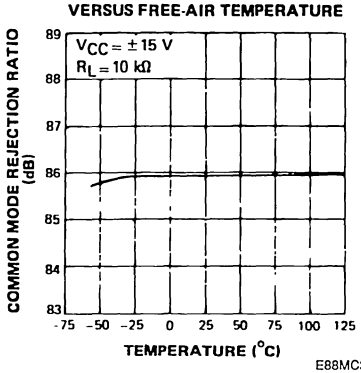
E88MC34001-12

SUPPLY CURRENT PER AMPLIFIER VERSUS SUPPLY VOLTAGE



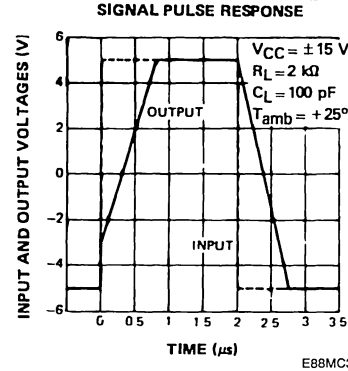
E88MC34001-13

COMMON MODE REJECTION RATIO VERSUS FREE-AIR TEMPERATURE



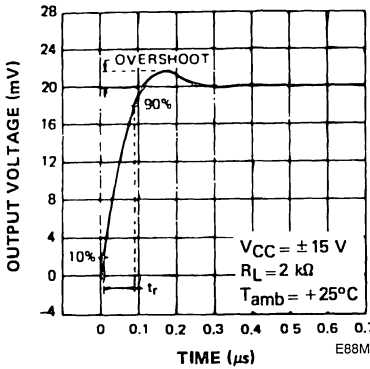
E88MC34001-14

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



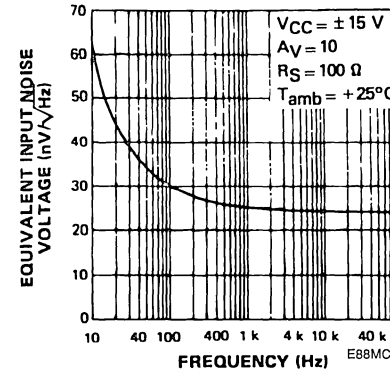
E88MC34001-15

OUTPUT VOLTAGE VERSUS TIME



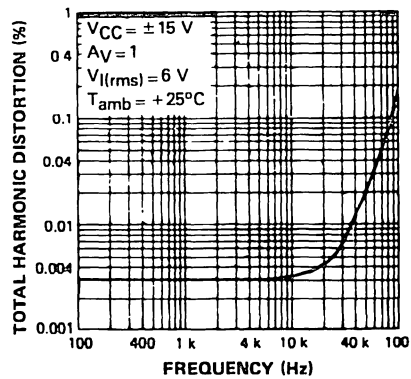
E88MC34001-16

EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



E88MC34001-17

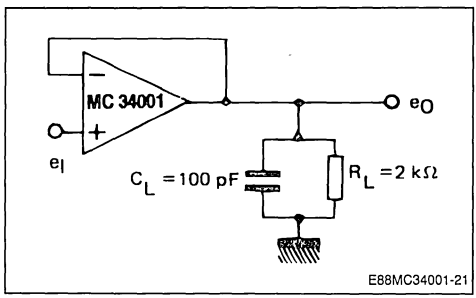
TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



E88MC34001-18

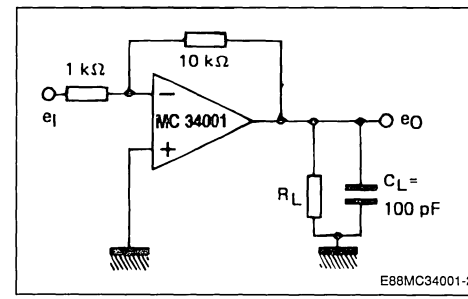
PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage Follower.



E88MC34001-21

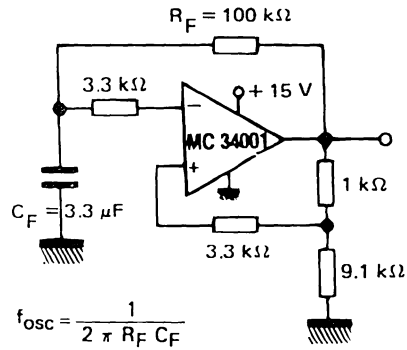
Figure 2 : Gain-of-10 Inverting Amplifier.



E88MC34001-22

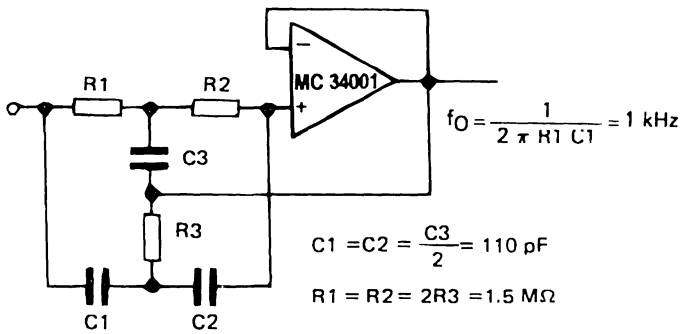
TYPICAL APPLICATIONS

(0.5 Hz) SQUARE WAVE OSCILLATOR



E88MC34001-19

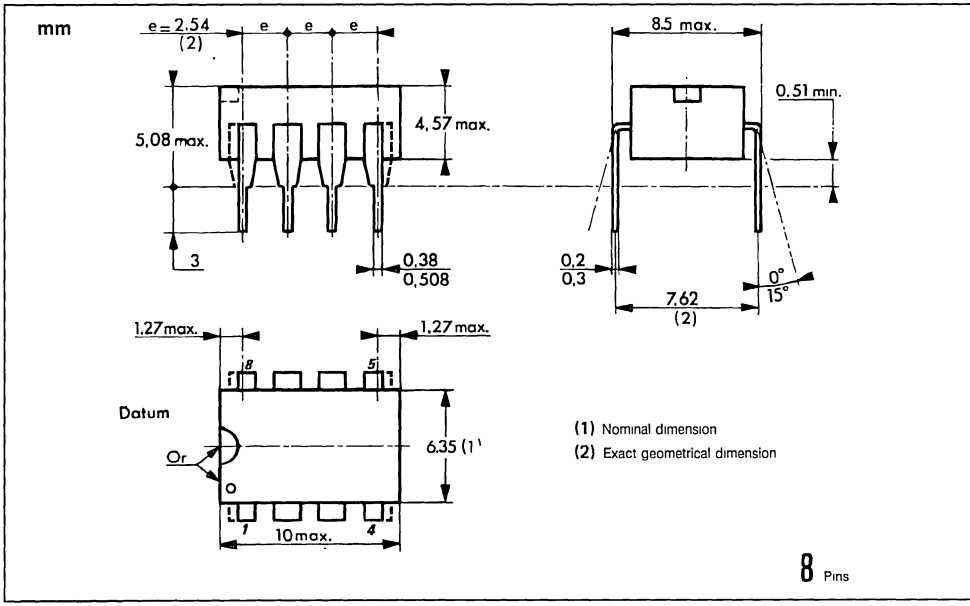
HIGH Q NOTCH FILTER



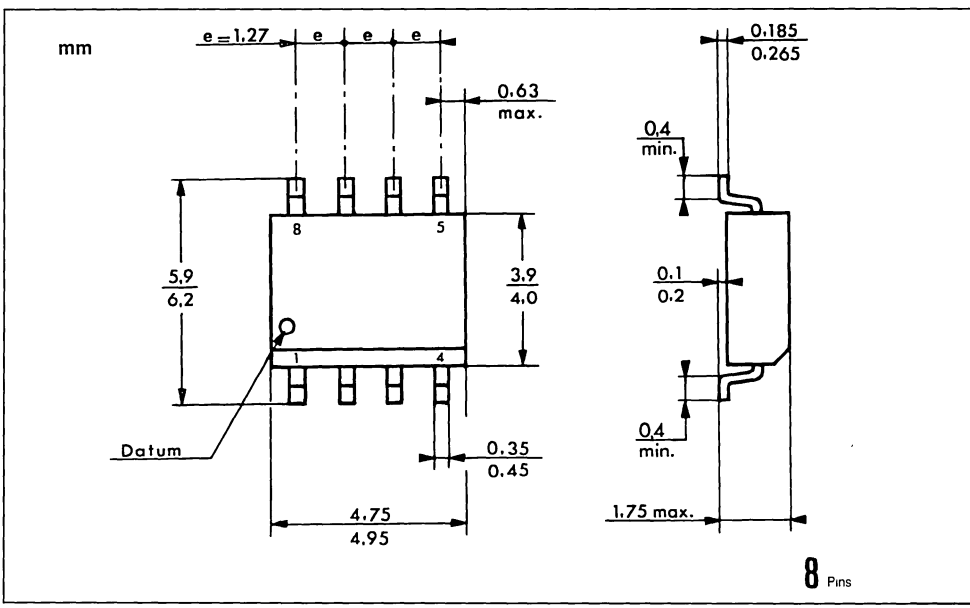
E88MC34001-20

PACKAGE MECHANICAL DATA

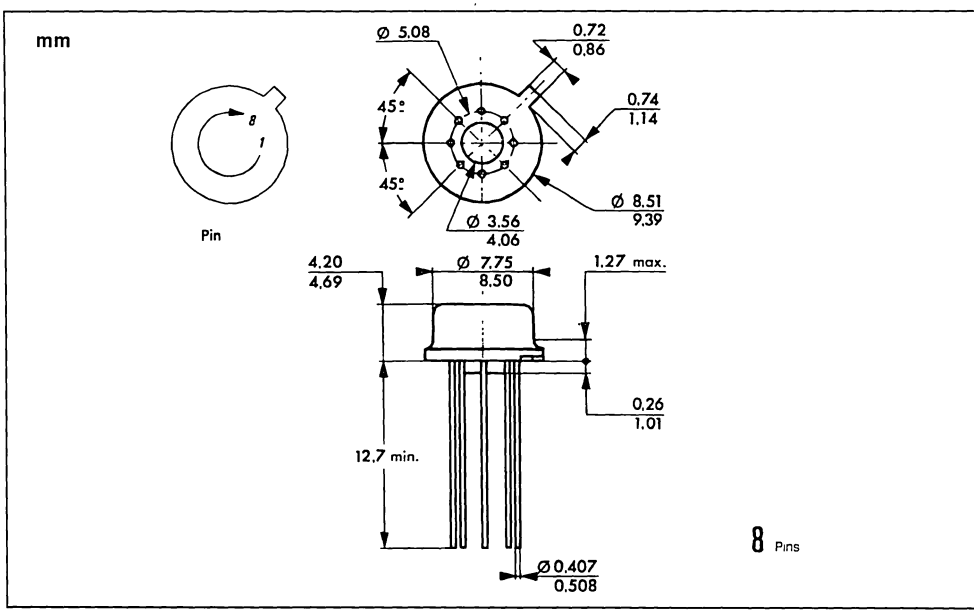
8 PINS – PLASTIC DIP



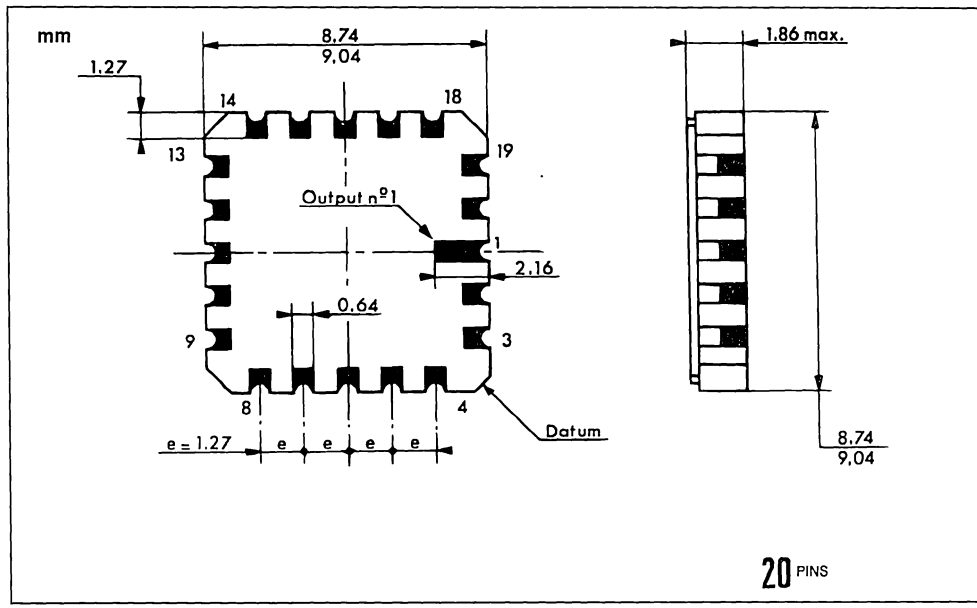
8 PINS – PLASTIC MICROPACKAGE (SO)



TO99 – METAL CAN



20 PINS – TRICECOP (LCC)

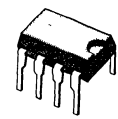


SGS-THOMSON MICROELECTRONICS

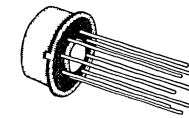
MC33002/A/B
MC34002/A/B
MC35002/A/B

J–FET INPUT DUAL OP–AMPs

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J–FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 13 V/µs (typ)

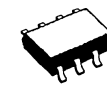


N
DIP8
(Plastic package)



H
TO99
(Metal can)

GC
LCC20
(Tricecop LCC)



D
SO8
(Plastic micropackage)

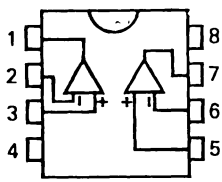
DESCRIPTION

These circuits are high speed J–FET input dual operational amplifiers incorporating well matched, high voltage J–FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset current, and low offset voltage temperature coefficient.

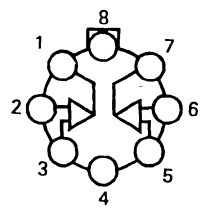
PIN CONNECTIONS (Top views)

DIP8
SO8

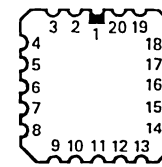


1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

TO99



LCC20



1 - NC
2 - Output 1
3 - NC
4 - NC
5 - Inverting input 1
6 - NC
7 - Non-inverting input 1
8 - NC
9 - NC
10 - V_{CC}^-
11 - NC
12 - Non-inverting input 2
13 - NC
14 - NC
15 - Inverting input 2
16 - NC
17 - Output 2
18 - NC
19 - NC
20 - V_{CC}^+

ORDER CODES

Part Number	Temperature	Package
MC35002GC	– 55 °C to + 125 °C	LCC
MC35002AGC	– 55 °C to + 125 °C	LCC
MC35002BGC	– 55 °C to + 125 °C	LCC
MC35002H	– 55 °C to + 125 °C	METAL CAN
MC35002AH	– 55 °C to + 125 °C	METAL CAN
MC35002BH	– 55 °C to + 125 °C	METAL CAN
MC33002N	– 40 °C to + 105 °C	DIP8
MC33002AN	– 40 °C to + 105 °C	DIP8
MC33002BN	– 40 °C to + 105 °C	DIP8
MC33002D	– 40 °C to + 105 °C	SO8
MC33002AD	– 40 °C to + 105 °C	SO8
MC33002BD	– 40 °C to + 105 °C	SO8
MC34002N	0 °C to + 70 °C	DIP8
MC34002AN	0 °C to + 70 °C	DIP8
MC34002BN	0 °C to + 70 °C	DIP8
MC34002D	0 °C to + 70 °C	SO8
MC34002AD	0 °C to + 70 °C	SO8
MC34002BD	0 °C to + 70 °C	SO8

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	± 18	V
V_I	Input Voltage (note 3)	± 15	V
V_{CC}	Diff. Input Voltage (note 2)	± 30	V
P_{tot}	Power Dissipation	680	mW
	Output Short-circuit Duration (note 4)	Infinite	
T_{oper}	Operating Free Air Temperature Range		°C
	MC34002, A, B	0 to 70	
	MC33002, A, B	– 40 to 105	
	MC35002, A, B	– 55 to 125	
T_{stg}	Storage Temperature Range	– 65 to 150	°C

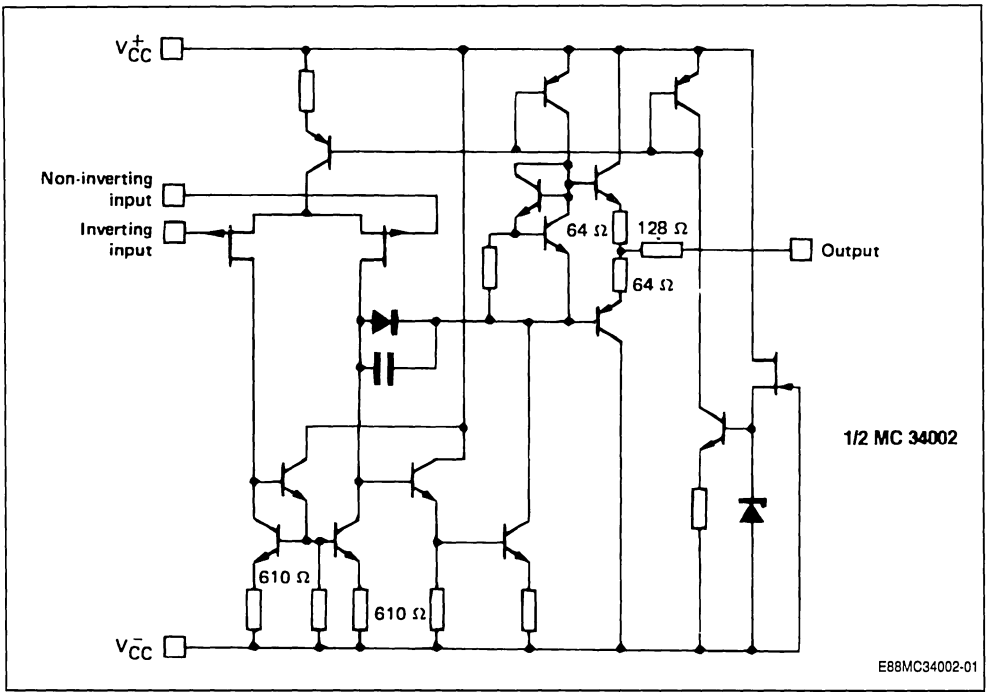
Notes : 1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.

2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.

3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.

4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

SCHEMATIC DIAGRAM



Case	Outputs	Non-Inverting Inputs	Inverting Inputs	V_{CC}^{-}	V_{CC}^{+}	N.C.
DIP8 SO8 TO99	1, 7	3, 5	2, 6	4	8	
LCC20	2, 17	7, 12	5, 15	10	20	*

* **LCC20** : Other pins are not connected.

ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 15$ V (unless otherwise specified)
MC35002, MC35002B, MC35002A $-55 \leq T_{amb} \leq +125$ °C
MC33002, MC33002B, MC33002A $-40 \leq T_{amb} \leq +105$ °C
MC34002, MC34002B, MC34002A $0 \leq T_{amb} \leq +70$ °C

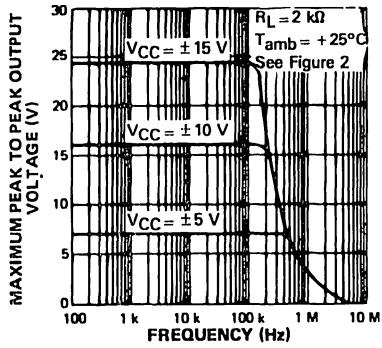
Symbol	Parameter	MC35002A, B MC33002A, B MC34002A, B			MC35002 MC33002 MC34002			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage							mV
	$T_{amb} = 25$ °C ($R_S < 10$ kΩ)					3	8	
	MC35002B, MC33002B, MC34002B		3	5				
	MC35002A, MC33002A, MC34002A		1	2				
	$T_{min} \leq T_{amb} \leq T_{max}$						13	
	MC35002B, MC33002B, MC34002B			9				
	MC35002A, MC33002A, MC34002A			5				
DV_{IO}	Input Offset Voltage Drift		10			10		µV/°C
I_{IO}	Input Offset Current *							
	$T_{amb} = 25$ °C		5	50		5	50	pA
	$T_{min} \leq T_{amb} \leq T_{max}$			4			4	nA
I_{IB}	Input Bias Current *							
	$T_{amb} = 25$ °C		20	200		20	200	pA
	$T_{min} \leq T_{amb} \leq T_{max}$			20			20	nA
A_{VD}	Large Signal Voltage Gain							V/mV
	($R_L \geq 2$ kΩ, $V_o = \pm 10$ V)							
	$T_{amb} = 25$ °C	50	200		50	200		
	$T_{min} \leq T_{amb} \leq T_{max}$	25			25			
SVR	Supply Voltage Rejection Ratio							dB
	($R_s < 10$ kΩ)							
	$T_{amb} = 25$ °C	80	86		80	86		
	$T_{min} \leq T_{amb} \leq T_{max}$	80			80			
I_{CC}	Supply Current, per Amp, no Load							mA
	$T_{amb} = 25$ °C		1.4	2.5		1.4	2.5	
	$T_{min} \leq T_{amb} \leq T_{max}$			2.5			2.5	
V_I	Input Voltage Range							V
	$T_{amb} = 25$ °C	−11		+11	−11		+11	
	$T_{min} \leq T_{amb} \leq T_{max}$							
CMR	Common Mode Rejection Ratio							dB
	($R_s \leq 10$ kΩ)							
	$T_{amb} = 25$ °C	80	86		70	86		
	$T_{min} \leq T_{amb} \leq T_{max}$	80			70			
I_{OS}	Output Short-circuit Current							mA
	$T_{amb} = 25$ °C	10	40	60	10	40	60	
	$T_{min} \leq T_{amb} \leq T_{max}$	10		60	10		60	
$\pm V_{OPP}$	Output Voltage Swing							V
	$T_{amb} = 25$ °C $R_L \geq 2$ kΩ	11	12		11	12		
	$R_L \geq 10$ kΩ	12	13.5		12	13.5		
	$T_{min} \leq T_{amb} \leq T_{max}$ $R_L \geq 2$ kΩ	11			11			
	$R_L \geq 10$ kΩ	12			12			
S_{VO}	Slew-rate ($V_I = 10$ V, $R_L = 2$ kΩ)							V/µs
	$C_L \leq 100$ pF, $T_{amb} = 25$ °C, unity gain	12	16		12	16		

* The input bias currents are junction leakage currents wich approximatively double for every 10 °C increase in the junction temperature.

ELECTRICAL CHARACTERISTICS (continued)

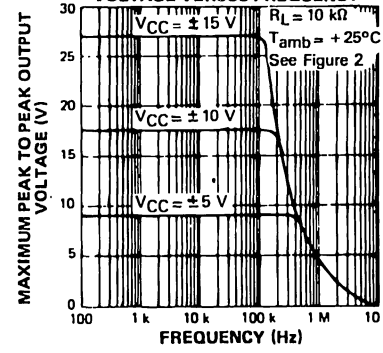
Symbol	Parameter	MC34002A, B MC33002A, B MC35002A, B			MC34002 MC33002 MC35002			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_r	Rise Time (V_I = 20 mV, R_L = 2 kΩ) C_L = 100 pF, T_{amb} = 25 °C, unity Gain		0.1			0.1		µs
K_{OV}	Overshoot (V_I = 20 mV, R_L = 2 kΩ $C_L \leq$ 100 pF, T_{amb} = 25 °C, unity gain)		10			10		%
GBP	Gain Bandwidth Product (f = 100 kHz, T_{amb} = 25 °C V_{IN} = 10 mV, R_L = 2 kΩ, C_L = 100 pF)	3.3	4.0	5.0	3.3	4.0	5.0	MHz
R_I	Input Resistance (T_{amb} = 25 °C)		10^{12}			10^{12}		Ω
THD	Total Harmonic Distortion (f = 1 kHz, A_v = 20 dB, R_L = 2 kΩ $C_L \leq$ 100 pF, T_{amb} = 25 °C, V_O = 2 V_{PP})		0.01			0.01		%
V_n	Equivalent Input Noise Voltage (f = 1 kHz, R_g = 100 Ω)		15			15		nV/√Hz
Øm	Phase Margin		45			45		Degrees
V_{O1}/V_{O2}	Channel Separation A_{VD} = 100, T_{amb} = 25 °C		120			120		dB

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



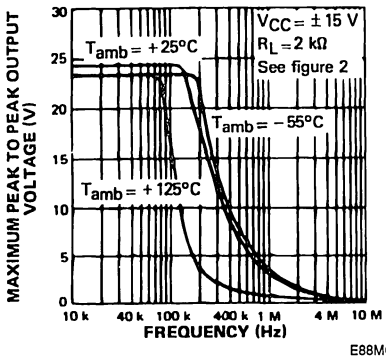
E88MC34002-02

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



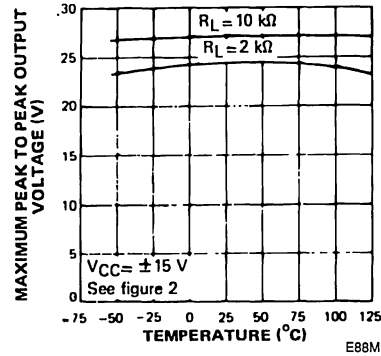
E88MC34002-03

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



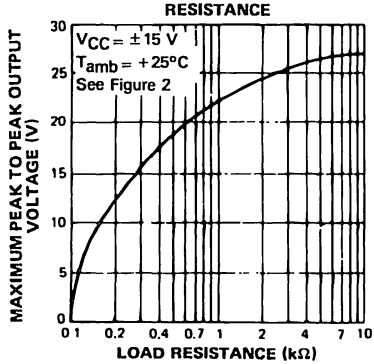
E88MC34002-04

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREE-AIR TEMP.



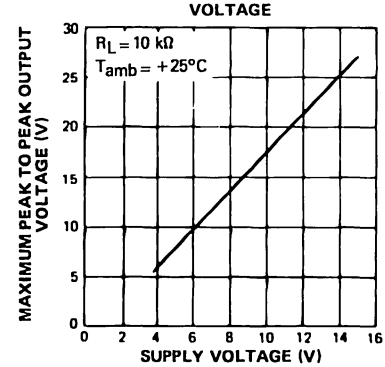
E88MC34002-05

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



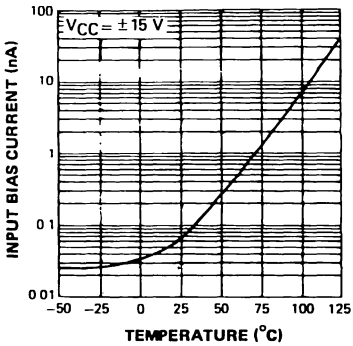
E88MC34002-06

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



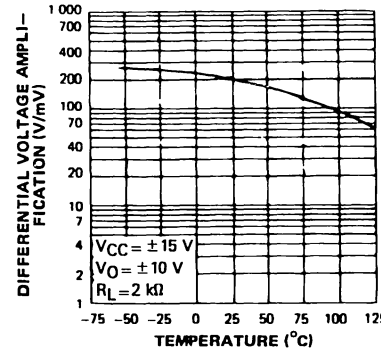
E88MC34002-07

INPUT BIAS CURRENT VERSUS FREE-AIR TEMPERATURE



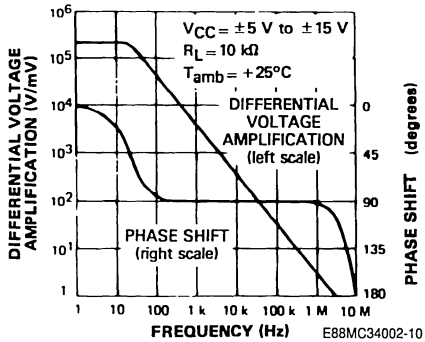
E88MC34002-08

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE-AIR TEMPERATURE



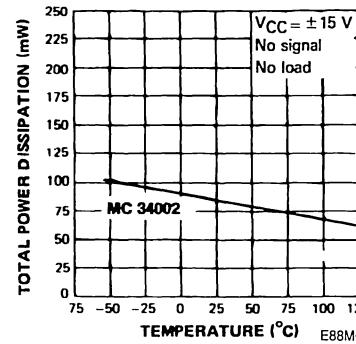
E88MC34002-09

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



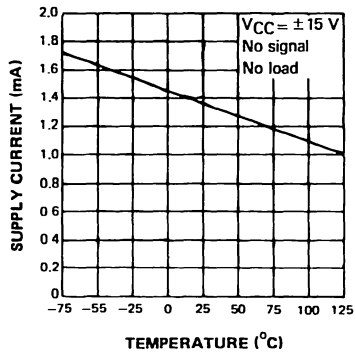
E88MC34002-10

TOTAL POWER DISSIPATION VERSUS FREE-AIR TEMPERATURE



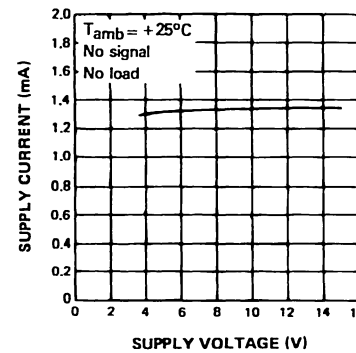
E88MC34002-11

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE-AIR TEMPERATURE



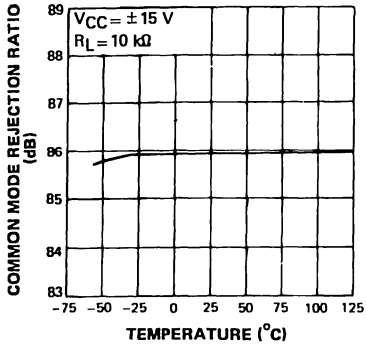
E88MC34002-12

SUPPLY CURRENT PER AMPLIFIER VERSUS SUPPLY VOLTAGE



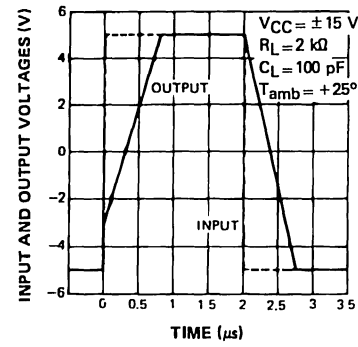
E88MC34002-13

COMMON MODE REJECTION RATIO VERSUS FREE-AIR TEMPERATURE



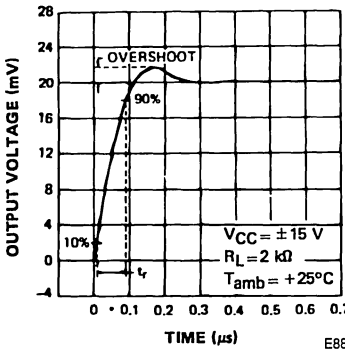
E88MC34002-14

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



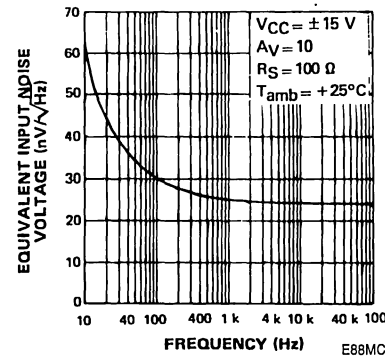
E88MC34002-15

OUTPUT VOLTAGE VERSUS TIME



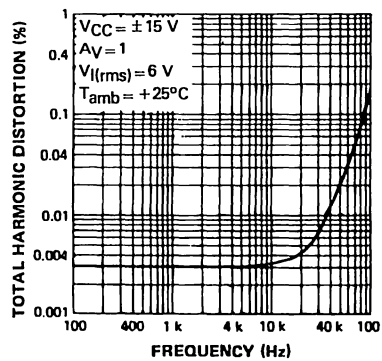
E88MC34002-16

EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



E88MC34002-17

TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



E88MC34002-18

PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage Follower.

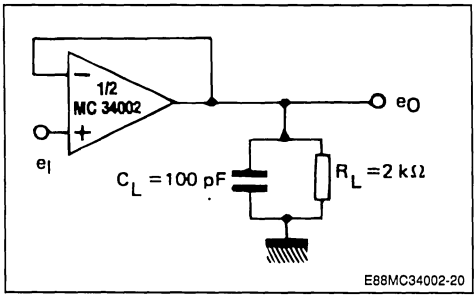
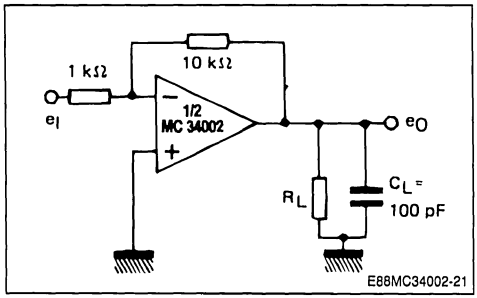
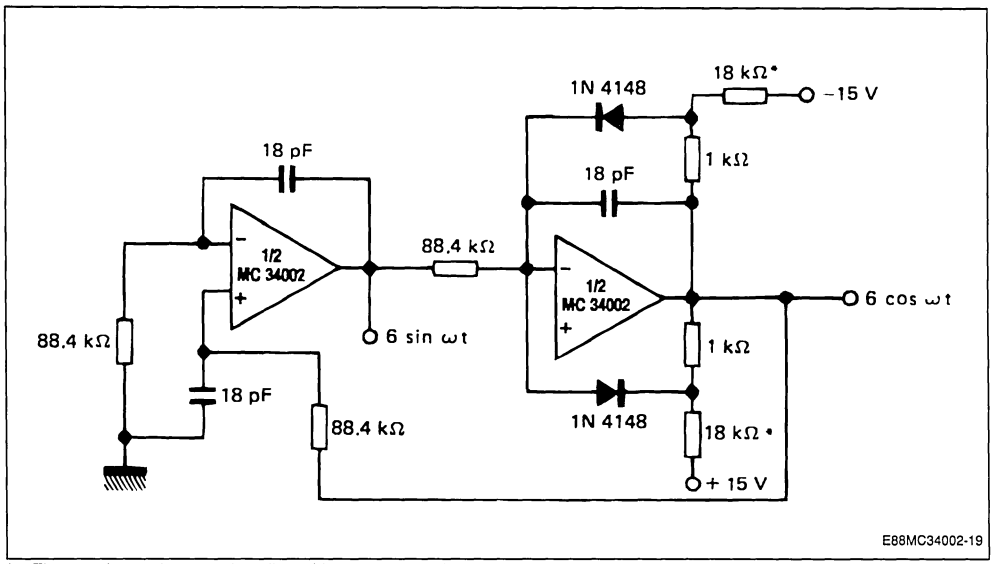


Figure 2 : Gain-of-10 Inverting Amplifier.



TYPICAL APPLICATION

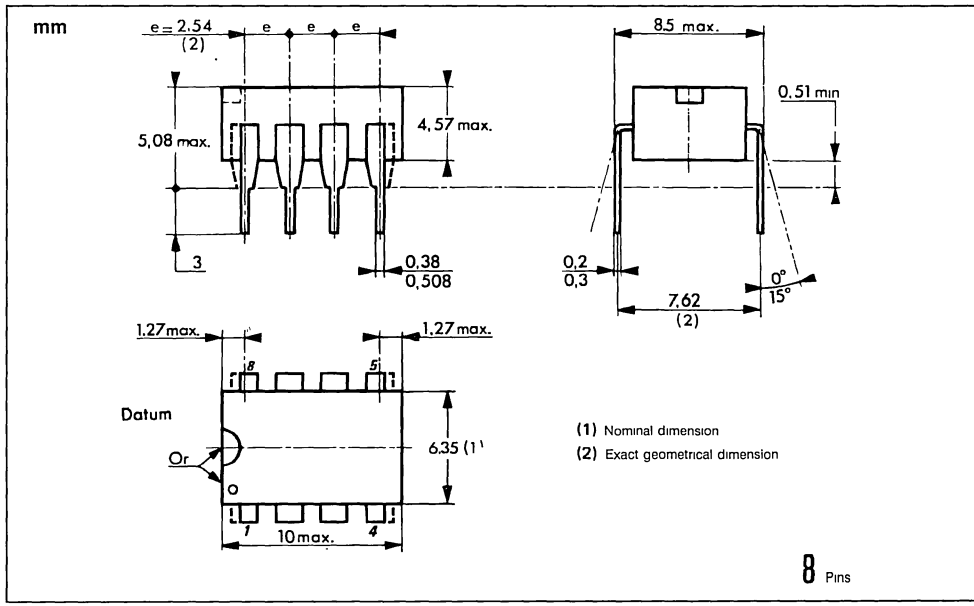
QUADRATURE OSCILLATOR



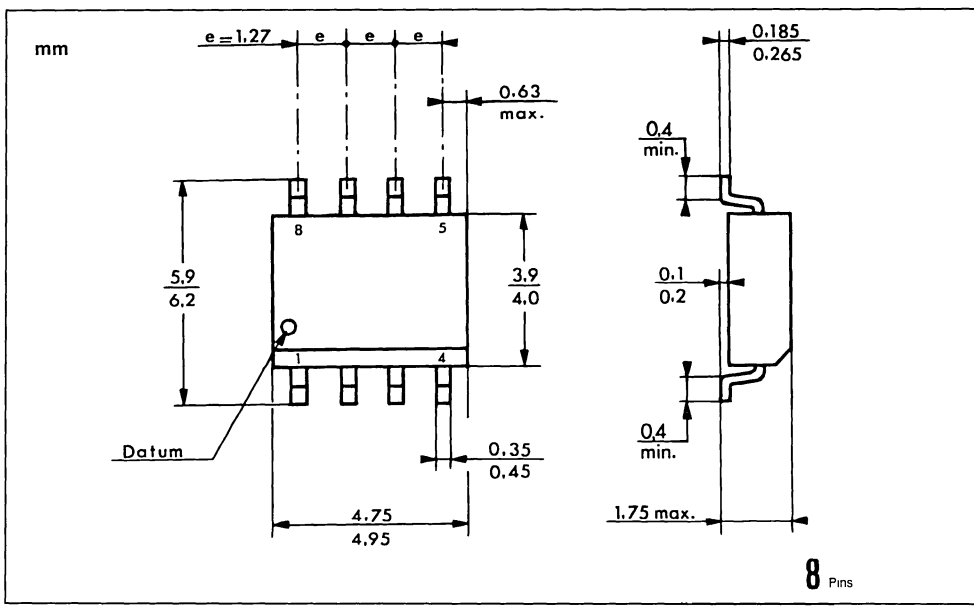
* These resistor values may be adjusted for a symmetrical output.

PACKAGE MECHANICAL DATA

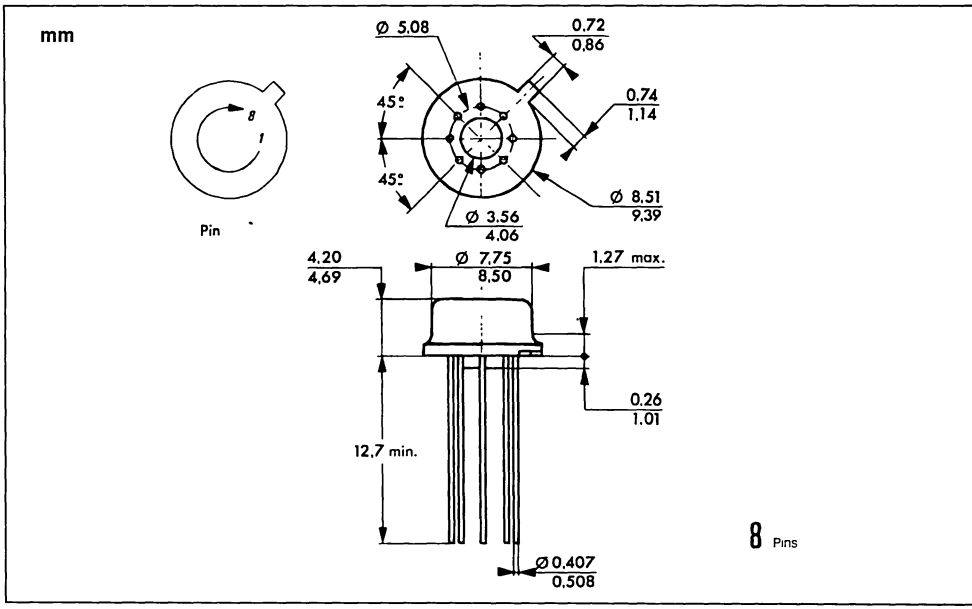
8 PINS - PLASTIC DIP



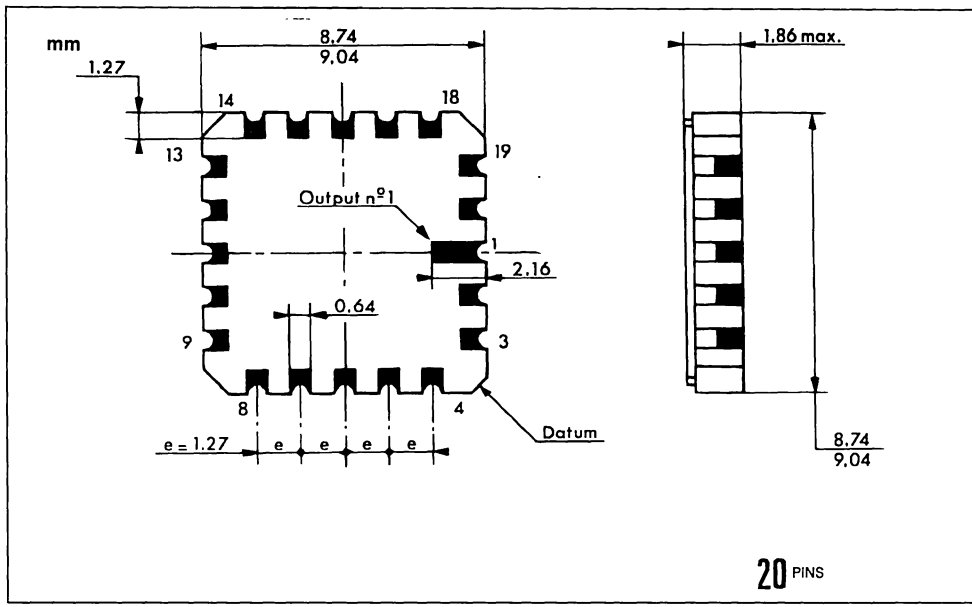
8 PINS – PLASTIC MICROPACKAGE (SO)



TO99 – METAL CAN

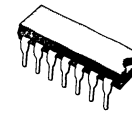


20 PINS – TRICECOP (LCC)



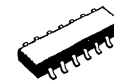
J–FET INPUT QUAD OP–AMPs

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J–FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 13 V/µs (typ)



N SUFFIX
DIP14
(Plastic package)

J SUFFIX
CERDIP14
(Cerdip package)



D SUFFIX
SO14
(Plastic micropackage)

GC SUFFIX
LCC20
(Tricecop LCC)

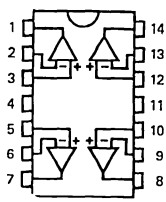
DESCRIPTION

These circuits are high speed J–FET input quad operational amplifiers incorporating well matched, high voltage J–FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset current, and low offset voltage temperature coefficient.

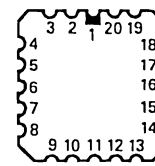
PIN CONNECTIONS (Top views)

DIP14
CERDIP14
SO14



1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - Output 3
9 - Inverting input 3
10 - Non-inverting input 3
11 - V_{CC}^+
12 - Non-inverting input 4
13 - Inverting input 4
14 - Output 4

LCC20



1 - NC
2 - Output 1
3 - Inverting input 1
4 - Non-inverting input 1
5 - NC
6 - V_{CC}^+
7 - NC
8 - Non-inverting input 2
9 - Inverting input 2
10 - Output 2
11 - NC
12 - Output 3
13 - Inverting input 3
14 - Non-inverting input 3
15 - NC
16 - V_{CC}^-
17 - NC
18 - Non-inverting input 4
19 - Inverting input 4
20 - Output 4

ORDER CODES

Part Number	Temperature	Package
MC35004GC	– 55 °C to + 125 °C	LCC
MC35004AGC	– 55 °C to + 125 °C	LCC
MC35004BGC	– 55 °C to + 125 °C	LCC
MC35004J	– 55 °C to + 125 °C	CERDIP
MC35004AJ	– 55 °C to + 125 °C	CERDIP
MC35004BJ	– 55 °C to + 125 °C	CERDIP
MC33004N	– 40 °C to + 105 °C	DIP 14
MC33004AN	– 40 °C to + 105 °C	DIP 14
MC33004BN	– 40 °C to + 105 °C	DIP 14
MC33004D	– 40 °C to + 105 °C	SO 14
MC33004AD	– 40 °C to + 105 °C	SO 14
MC33004BD	– 40 °C to + 105 °C	SO 14
MC34004N	0 °C to + 70 °C	DIP 14
MC34004AN	0 °C to + 70 °C	DIP 14
MC34004BN	0 °C to + 70 °C	DIP 14
MC34004D	0 °C to + 70 °C	SO 14
MC34004AD	0 °C to + 70 °C	SO 14
MC34004BD	0 °C to + 70 °C	SO 14

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	± 18	V
V_i	Input Voltage (note 3)	± 15	V
V_{CC}	Diff. Input Voltage (note 2)	± 30	V
P_{tot}	Power Dissipation	680	mW
	Output Short-circuit Duration (note 4)	Infinite	
T_{oper}	Operating Free Air Temperature Range		°C
	MC34004, A, B	0 to 70	
	MC33004, A, B	– 40 to 105	
	MC35004, A, B	– 55 to 125	
T_{stg}	Storage Temperature Range	– 65 to 150	°C

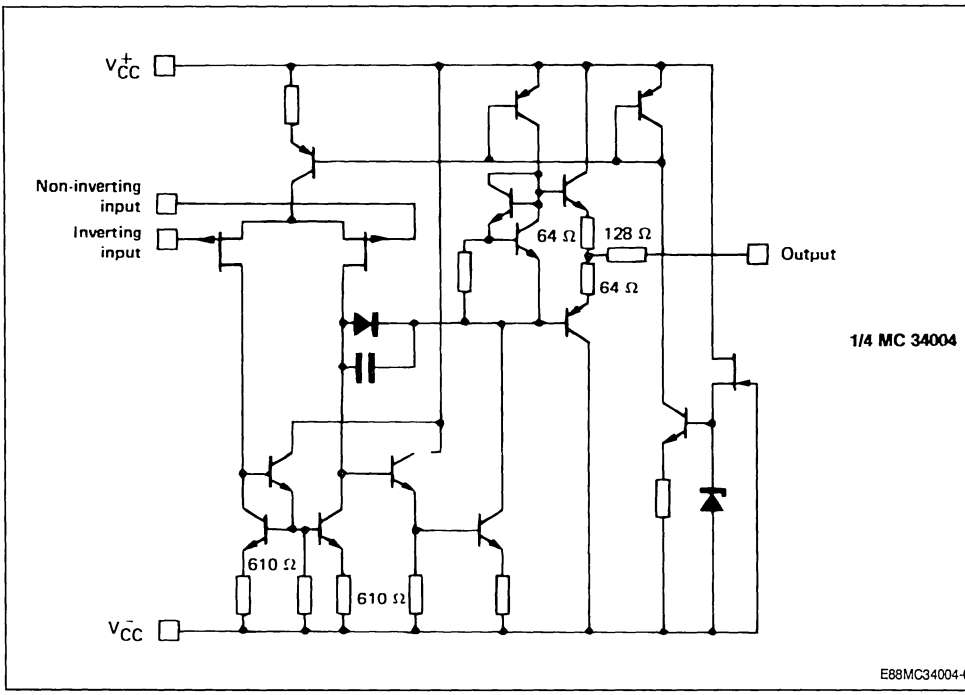
Notes : 1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.

2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.

3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.

4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

SCHEMATIC (each amplifier)



Case	Outputs	Inverting Inputs	Non-inverting Inputs	V_{CC}^{+}	V_{CC}^{-}	N.C.
DIP14 CERDIP14 SO14	1, 7, 14, 8	2, 6, 13, 9	3, 5, 12, 10	4	11	
LCC20	2, 10, 12, 20	3, 9, 13, 19		4, 8, 14, 18	6	16

* **LCC20** : Other pins are not connected.

ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 15$ V (unless otherwise specified)
MC35004, MC35004B, MC35004A $-55 \leq T_{amb} \leq +125$ °C
MC33004, MC33004B, MC33004A $-40 \leq T_{amb} \leq +105$ °C
MC34004, MC34004B, MC34004A $0 \leq T_{amb} \leq +70$ °C

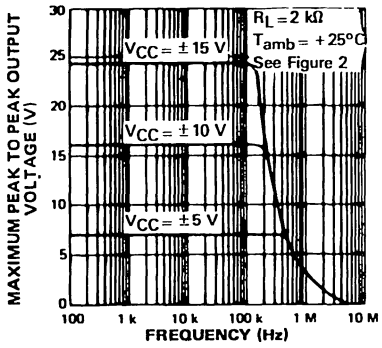
Symbol	Parameter	MC35004A, B MC33004A, B MC34004A, B			MC35004 MC33004 MC34004			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage T_{amb} = 25 °C ($R_s \leq 10$ kΩ) MC35004B, MC33004B, MC34004B MC35004A, MC33004A, MC34004A $T_{min} \leq T_{amb} \leq T_{max}$ MC35004B, MC33004B, MC34004B MC35004A, MC33004A, MC34004A		 3 1 	 5 2 9 5		 3 	 8 13 	mV
DV_{IO}	Input Offset Voltage Drift		10			10		µV/°C
I_{IO}	Input Offset Current * T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		5	50 4		5	50 4	pA nA
I_{IB}	Input Bias Current * T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		30	200 20		30	200 20	pA nA
A_{VD}	Large Signal Voltage Gain ($R_L > 2$ kΩ, $V_o = \pm 10$ V) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 50 25	 200 	 	 50 25	 200 	 	V/mV
SVR	Supply Voltage Rejection Ratio ($R_s < 10$ kΩ) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 80 80	 86 	 	 80 80	 86 	 	dB
I_{CC}	Supply Current, per Amp, no Load T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		1.4	2.5 2.5		1.4	2.5 2.5	mA
V_I	Input Voltage Range T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	− 11		+ 11	− 11		+ 11	V
CMR	Common Mode Rejection Ratio ($R_s < 10$ kΩ) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 80 80	 86 	 	 70 70	 86 	 	dB
I_{OS}	Output Short-circuit Current T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 10 10	 40 	 60 60	 10 10	 40 	 60 60	mA
$\pm V_{OPP}$	Output Voltage Swing T_{amb} = 25 °C $R_L \geq 2$ kΩ $R_L \geq 10$ kΩ $T_{min} \leq T_{amb} \leq T_{max}$ $R_L \geq 2$ kΩ $R_L \geq 10$ kΩ	 11 12 11 12	 12 13.5 	 	 11 12 11 12	 12 13.5 	 	V
S_{VO}	Slew-rate ($V_I = 10$ V, $R_L = 2$ kΩ) $C_L \leq 100$ pF, T_{amb} = 25 °C, unity gain	12	16		12	16		V/µs

* The input bias currents are junction leakage currents wich approximatively double for every 10 °C increase in the junction temperature.

ELECTRICAL CHARACTERISTICS (continued)

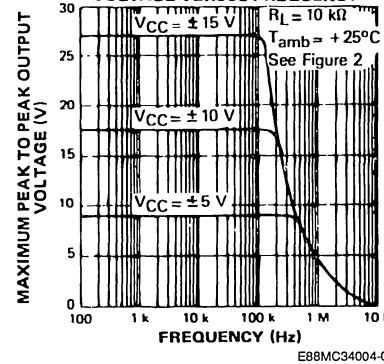
Symbol	Parameter	MC34004A, B MC33004A, B MC35004A, B			MC34004 MC33004 MC35004			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_r	Rise Time (V_I = 20 mV, R_L = 2 kΩ) C_L = 100 pF, T_{amb} = 25 °C, unity Gain		0.1			0.1		µs
K_{OV}	Overshoot (V_I = 20 mV, R_L = 2 kΩ $C_L \leq$ 100 pF, T_{amb} = 25 °C, unity gain)		10			10		%
GBP	Gain Bandwidth Product (f = 100 kHz, T_{amb} = 25 °C V_{IN} = 10 mV, R_L = 2 kΩ, C_L = 100 pF)	3.3	4.0	5.0	3.3	4.0	5.0	MHz
R_I	Input Resistance (T_{amb} = 25 °C)		10^{12}			10^{12}		Ω
THD	Total Harmonic Distortion (f = 1 kHz, A_V= 20 dB, R_L = 2 kΩ $C_L \leq$ 100 pF, T_{amb} = 25 °C, V_O = 2 V_{PP})		0.01			0.01		%
V_n	Equivalent Input Noise Voltage (f = 1 kHz, R_g = 100 Ω)		15			15		nV/√Hz
Øm	Phase Margin		45			45		Degrees
V_{O1}/V_{O2}	Channel Separation A_{VD} = 100, T_{amb} = 25 °C		120					120

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



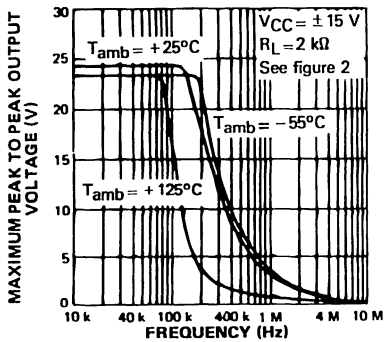
E88MC34004-02

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



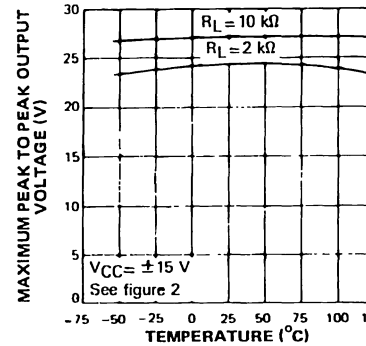
E88MC34004-03

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



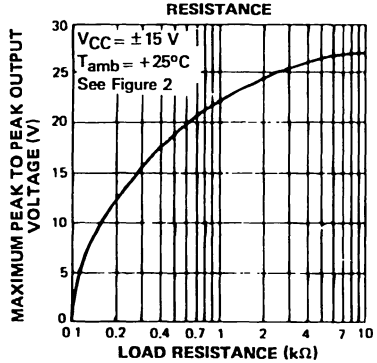
E88MC34004-04

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREE-AIR TEMP.



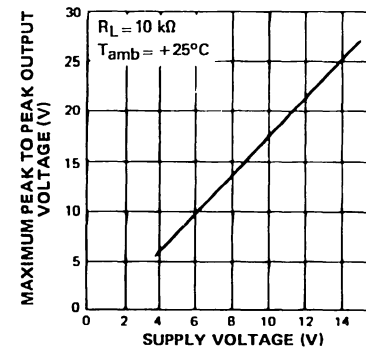
E88MC34004-05

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



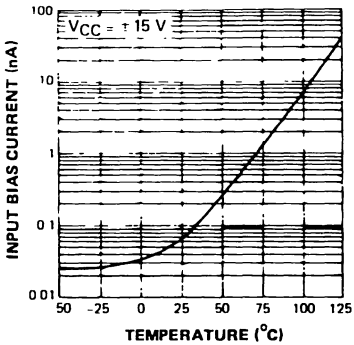
E88MC34004-06

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



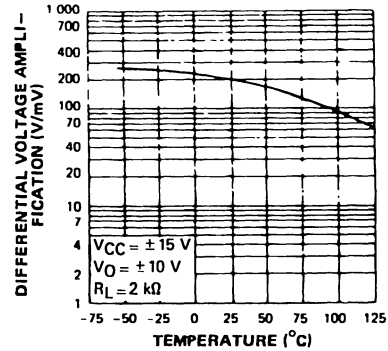
E88MC34004-07

INPUT BIAS CURRENT VERSUS FREE-AIR TEMPERATURE



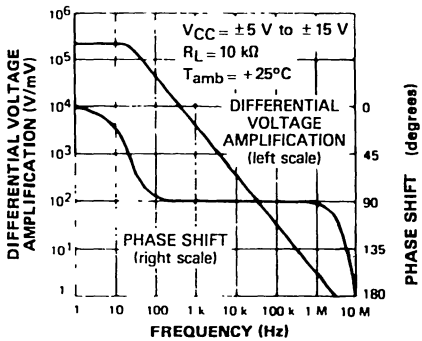
E88MC34004-08

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE-AIR TEMPERATURE



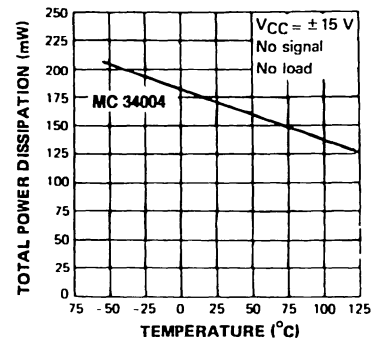
E88MC34004-09

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



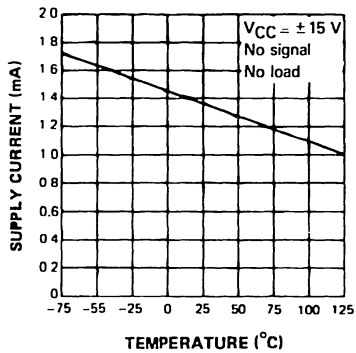
E88MC34004-10

TOTAL POWER DISSIPATION VERSUS FREE-AIR TEMPERATURE



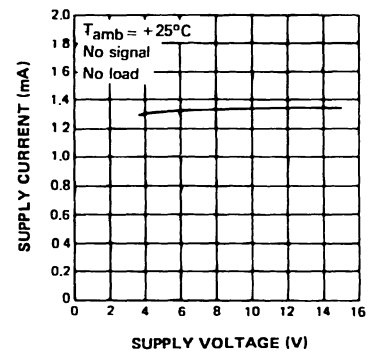
E88MC34004-11

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE-AIR TEMPERATURE



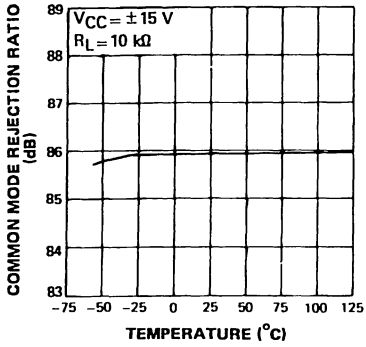
E88MC34004-12

SUPPLY CURRENT PER AMPLIFIER VERSUS SUPPLY VOLTAGE



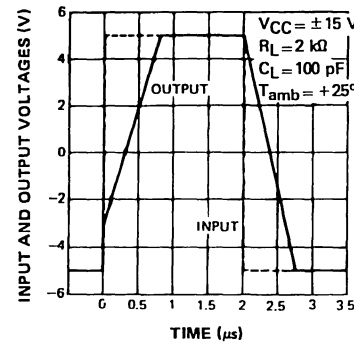
E88MC34004-13

COMMON MODE REJECTION RATIO VERSUS FREE-AIR TEMPERATURE



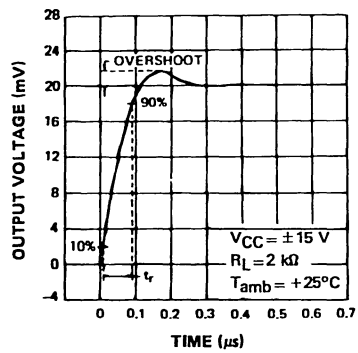
E88MC34004-14

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



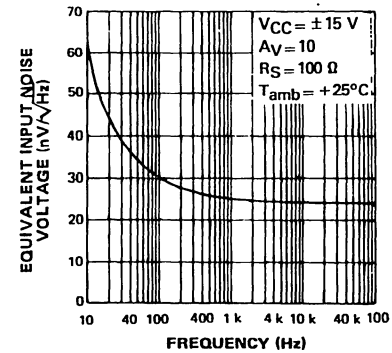
E88MC34004-15

OUTPUT VOLTAGE VERSUS TIME



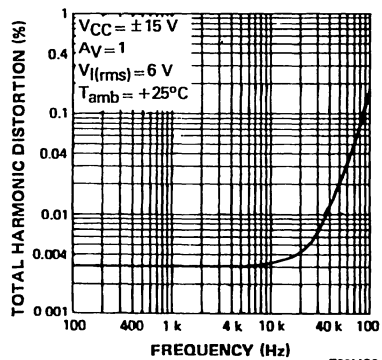
E88MC34004-16

EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



E88MC34004-17

TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



E88MC34004-18

PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage Follower.

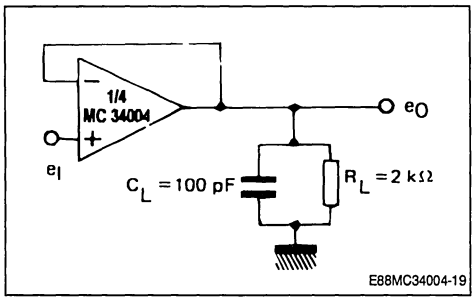
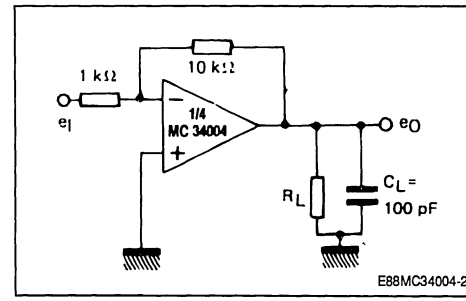
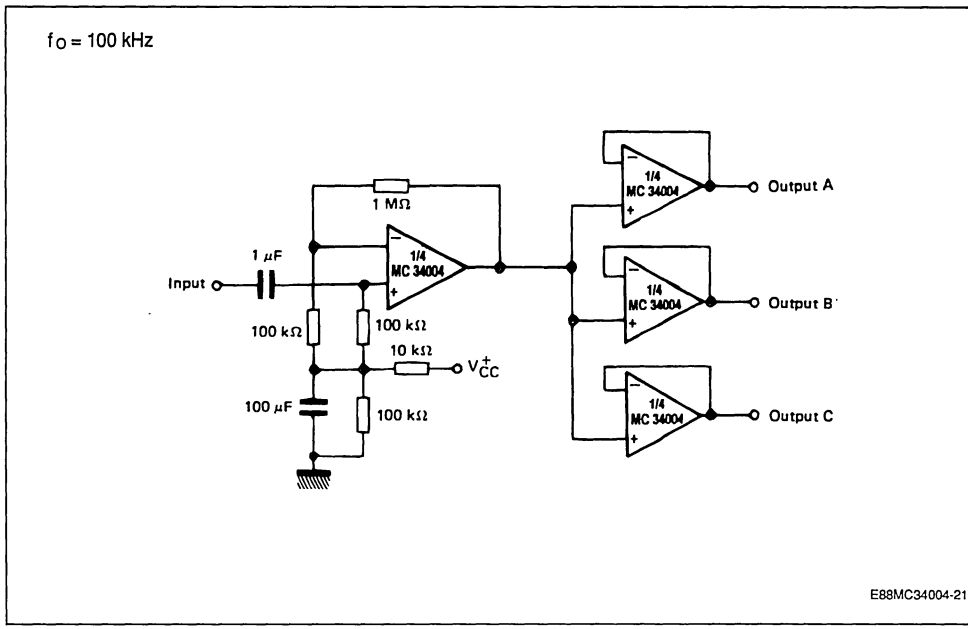


Figure 2 : Gain-of-10 Inverting Amplifier.

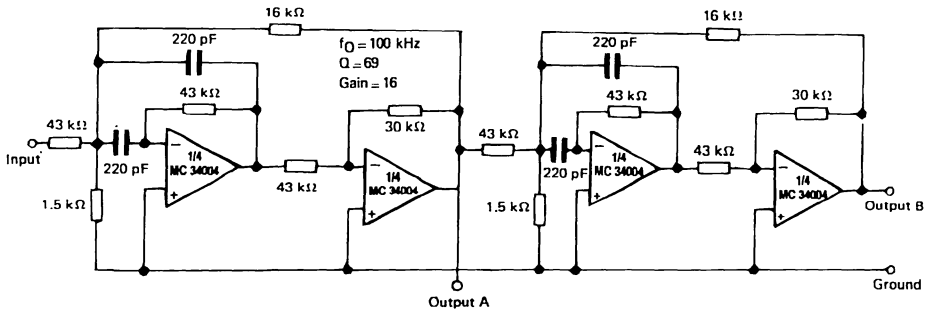


AUDIO DISTRIBUTION AMPLIFIER

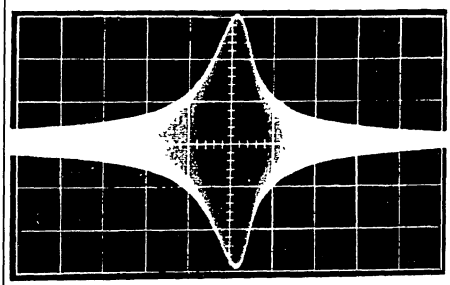


TYPICAL APPLICATION

POSITIVE FEEDBACK BANDPASS FILTER



OUTPUT A



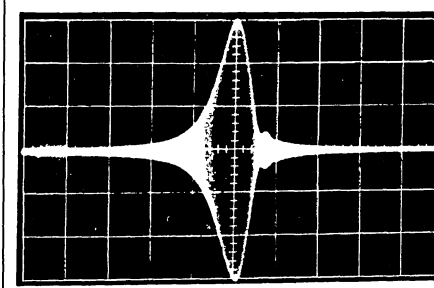
E88MC34004-23

2 kHz /div

SECOND ORDER BANDPASS FILTER

f_O = 100 kHz; Q = 30; Gain = 4

OUTPUT B



E88MC34004-24

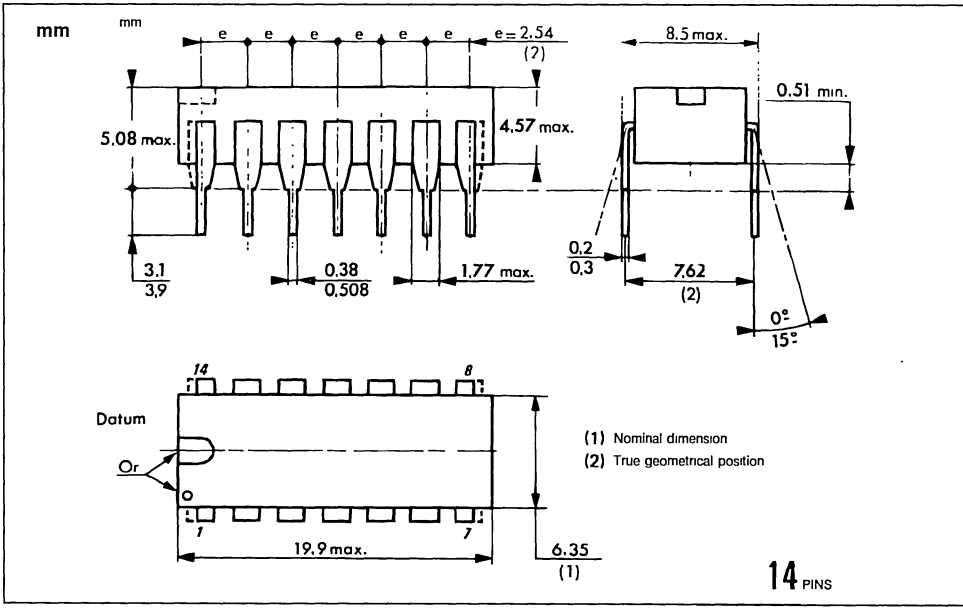
2 kHz /div

CASCADED BANDPASS FILTER

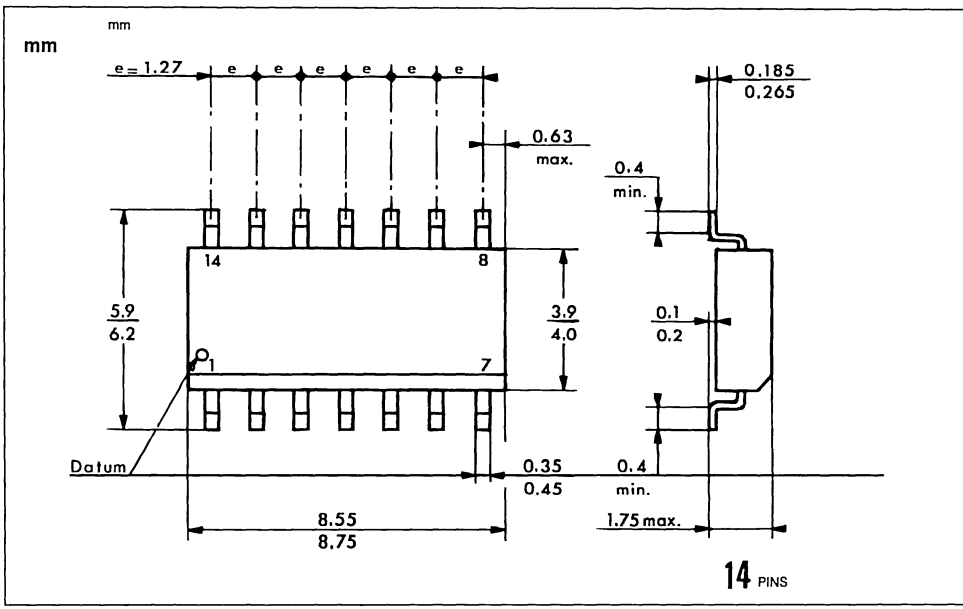
f_O = 100 kHz; Q = 69; Gain = 16

PACKAGE MECHANICAL DATA

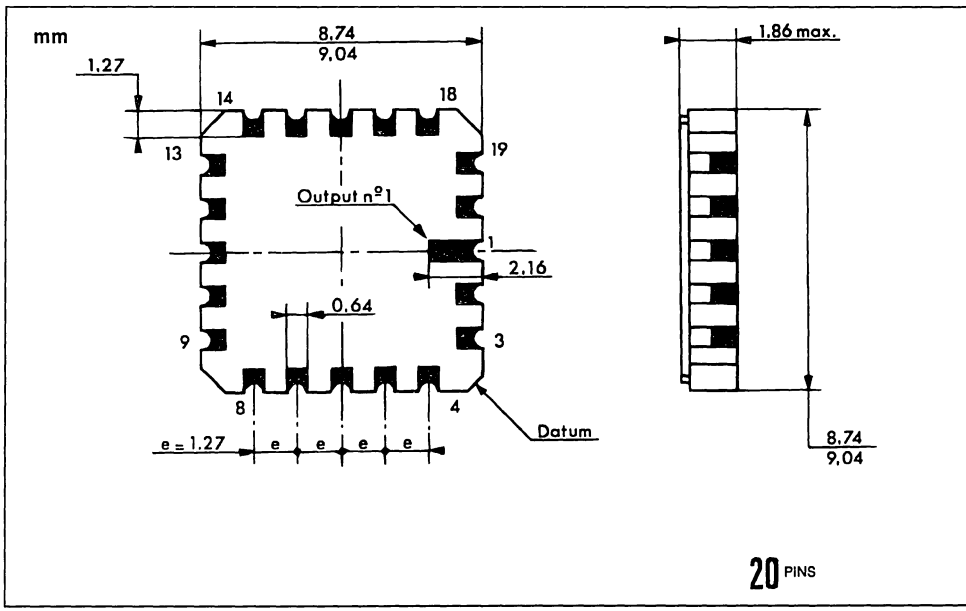
14 PINS – PLASTIC DIP OR CERDIP



14 PINS – PLASTIC MICROPACKAGE (SO)

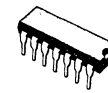


20 PINS – TRICECOP (LCC)

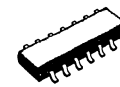


LOW POWER DIFFERENTIAL INPUT QUAD OP-AMPs

- SHORT-CIRCUIT PROTECTED OUTPUTS
- CLASS AB OUTPUT STAGE FOR MINIMAL CROSSOVER DISTORTION
- SINGLE SUPPLY OPERATION : +3 V TO +36 V
- DUAL SUPPLIES : ± 1.5 V TO ± 18 V
- LOW INPUT BIAS CURRENT : 500 nA MAX
- INTERNALLY COMPENSATED
- SIMILAR PERFORMANCE TO POPULAR UA741



N
DIP14
(Plastic Package)
J
CERDIP14
(Cerdip Package)



D
SO14
(Plastic Micropackage)

GC
LCC20
(Tricecop (LCC))

DESCRIPTION

The MC3403 is a low-cost, quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular UA741. However the MC3403, has several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 volts or as high as 36 volts with quiescent currents about one third of those associated with the UA741 (on a per amplifier basis). The common-mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

ORDER CODES

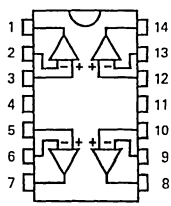
Part Number	Temperature Range	Package			
		J	N	D	GC
MC3303	– 40 °C to + 105 °C	•	•	•	
MC3403	0 °C to + 70 °C	•	•	•	
MC3503	– 55 °C to + 125 °C	•			•

Note : Hi-Rel Versions Available
Examples : MC3503J, MC3403N

PIN CONNECTIONS (top views)

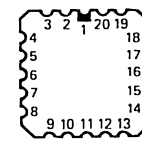
DIP14 / CERDIP14
SO14

1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^+
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - Output 3
9 - Inverting input 3
10 - Non-inverting input 3
11 - V_{CC}^-
12 - Non-inverting input 4
13 - Inverting input 4
14 - Output 4



E88MC3303-01

LCC20



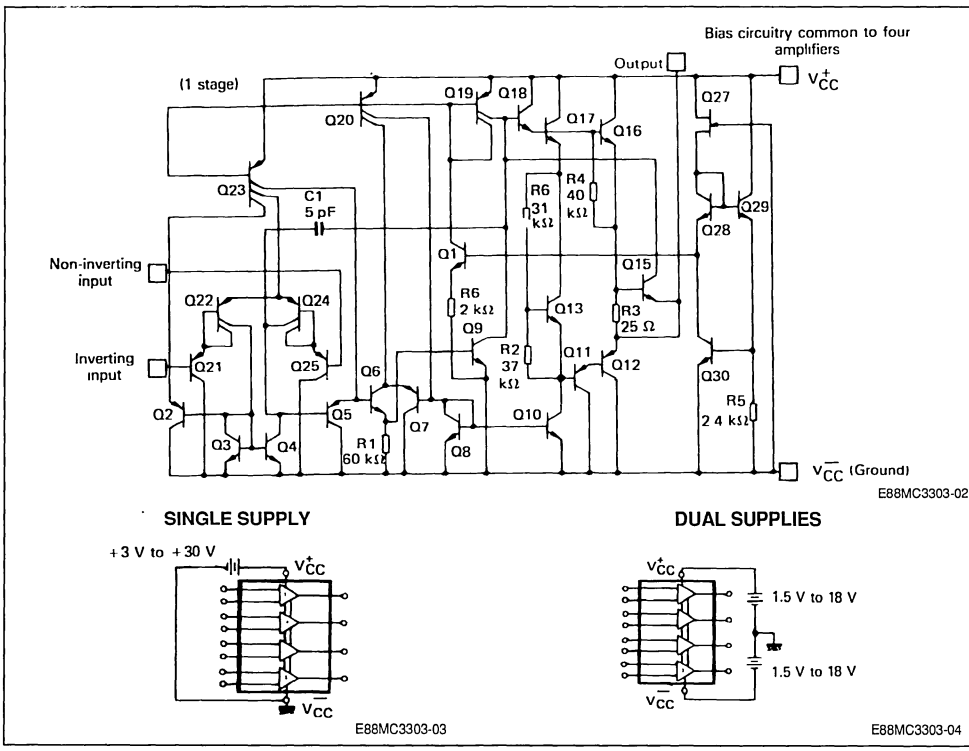
1 - NC
2 - Output 1
3 - Inverting input 1
4 - Non-inverting input 1
5 - NC
6 - V_{CC}^+
7 - NC
8 - Non-inverting input 2
9 - Inverting input 2
10 - Output 2
11 - NC
12 - Output 3
13 - Inverting input 3
14 - Non-inverting input 3
15 - NC
16 - V_{CC}^-
17 - NC
18 - Non-inverting input 4
19 - Inverting input 4
20 - Output 4

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	MC3503	MC3403	MC3303	Unit
V_{CC}	Supply Voltage	± 18	± 18	± 18	V
V_{ID}	Differential Input Voltage	± 36	± 36	± 36	V
V_I	Input Voltage (note 1)	± 18	± 18	± 18	V
–	Output Short-circuit Duration (note 2)	Indefinite	Indefinite	Indefinite	–
P_{tot}	Power Dissipation	500	500	500	mW
T_{oper}	Operating Free-air Temperature Range	– 55 to + 125	0 to + 70	– 40 to + 105	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	– 65 to + 150	– 65 to + 150	°C

Notes : 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Any of the amplifier outputs can be shorted to ground indefinitely ; however more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

SCHEMATIC DIAGRAM



Case	Outputs	Inverting Inputs	Non-inverting Inputs	V_{CC}^-	V_{CC}^+	N. C.
DIP14/CERDIP14 SO14	1, 7, 8, 14	2, 6, 9, 13	3, 5, 10, 12	11	4	
LCC20	1, 2, 12, 20	3, 9, 13, 19	4, 8, 14, 18	16	6	*

* **LCC20** : Other pins are not connected.

ELECTRICAL CHARACTERISTICS

MC3403 : $0 \leq T_{amb} \leq +70$ °C $\quad V_{CC} = \pm 15$ V
MC3303 : $-40 \leq T_{amb} \leq +105$ °C $\quad V_{CC} = \pm 15$ V
MC3503 : $-55 \leq T_{amb} \leq +125$ °C $\quad V_{CC} = \pm 15$ V

Symbol	Parameter	MC3303, MC3403, MC3503			Unit
		Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage ($R_S \leq 10$ kΩ) $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$		1	5 6	mV
I_{IO}	Input Offset Current $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$		2	20 40	nA
I_{IB}	Input Bias Current $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$		40	100 200	nA
A_{VD}	Large Signal Voltage Gain ($V_O = \pm 10$ V, $R_L = 2$ kΩ) $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$	 50 25	200		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S \leq 10$ kΩ) $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$	 77 77	90		dB
I_{CC}	Supply Current, all Amp, no Load $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$		2.8	4 5	mA
V_I	Input Voltage Range $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$	− 15 − 15		+ 13 + 13	V
CMR	Common Mode Rejection Ratio ($R_S \leq 10$ kΩ) $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$	 70 70	90		dB
I_{OS}	Output Short-circuit Current $T_{amb} = 25$ °C	10	30	45	mA
$\pm V_{opp}$	Output Voltage Swing $T_{amb} = 25$ °C $R_L = 10$ kΩ $R_L = 2$ kΩ $T_{min} \geq T_{amb} \geq T_{max}$ $R_L = 2$ kΩ $R_L = 10$ kΩ	 12 10 10 12	 13.5 13		V
S_{VO}	Slew Rate ($V_I = \pm 10$ V $R_L = 2$ kΩ $C_L \leq 100$ pF, $T_{amb} = 25$ °C, unity gain)	0.45	0.7		V/µs
t_r t_f	Rise Time and Fall Time ($V_O = \pm 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF $T_{amb} = 25$ °C, unity gain)		 0.18 0.18		µs
K_{OV}	Overshoot ($V_I = \pm 20$ mV, $R_L = 2$ kΩ $C_L \leq 100$ pF, $T_{amb} = 25$ °C, unity gain)		 10		%
Z_I	Input Impedance, $T_{amb} = 25$ °C	0.3	1		MΩ
Z_O	Output Impedance, $T_{amb} = 25$ °C		75		Ω

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	MC3303, MC3403, MC3503			Unit
		Min.	Typ.	Max.	
B_{om}	Power Bandwidth (R_L = 2 kΩ, C_L = 100 pF A_v = 1, T_{amb} = 25 °C, V_O = 2 V_{pp}, THD ≤ 5 %)		9		kHz
B	Unity Gain Bandwidth (V_O = 10 mV, R_L = 2 kΩ, C_L ≤ 100 pF, T_{amb} = 25 °C, unity gain)		1		MHz
GBP	Gain Bandwidth Product (V_O = 10 mV, R_L = 2 kΩ, C_L ≤ 100 pF, f = 100 kHz, T_{amb} = 25 °C)	0.8	1	1.6	MHz
THD	Total Harmonic Distortion (f = 1 kHz, A_v = 20 dB, R_L = 2 kΩ, V_O = 2 V_{pp} C_L ≤ 100 pF, T_{amb} = 25 °C)		0.02		%
V_n	Equivalent Input Noise Voltage (f = 1 kHz, R_g = 100 Ω)		43		nv/√Hz
Φm	Phase Margin		60		Degrees
DV_{IO}	Input Offset Voltage Drift T_{min} ≤ T_{amb} ≤ T_{max}		10		µV/°C
DI_{IO}	Input Offset Current Drift T_{min} ≤ T_{amb} ≤ 25 °C		50		pA/°C
V_{O1}/V_{02}	Channel Separation		120		dB

ELECTRICAL CHARACTERISTICS (continued)

V_{CC}^+ = 5 V, V_{CC}^- = Ground (unless otherwise specified)

Symbol	Parameter	MC3303, MC3403, MC3503			Unit
		Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage (R_S ≤ 10 kΩ) T_{amb} = 25 °C T_{min} ≤ T_{amb} ≤ T_{max}		1	5 6	mV
I_{IO}	Input Offset Current T_{amb} = 25 °C T_{min} ≤ T_{amb} ≤ T_{max}		2	20 40	nA
I_{IB}	Input Bias Current T_{amb} = 25 °C T_{min} ≤ T_{amb} ≤ T_{max}		40	100 200	nA
A_{VD}	Large Signal Voltage Gain (V_O = ± 10 V, R_L = 2 kΩ) T_{amb} = 25 °C T_{min} ≤ T_{amb} ≤ T_{max}	10 5	200		V/mV
SVR	Supply Voltage Rejection Ratio (R_S ≤ 10 kΩ) T_{amb} = 25 °C T_{min} ≤ T_{amb} ≤ T_{max}	77 77	90		dB
I_{CC}	Supply Current (all amp, V_O = 0 V)		2.5	4	mA
V_{opp}	Output Voltage Range (R_L = 10 kΩ) + 5 V≤ V_{CC} ≤ + 30 V	V_{CC}^+ – 1.7 V	V_{CC}^+ – 1.5 V		V

CIRCUIT DESCRIPTION

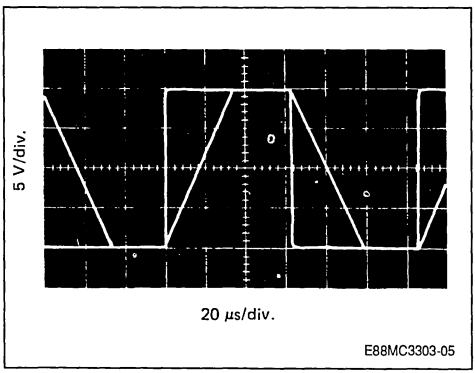
The MC3403 is made using four internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area.

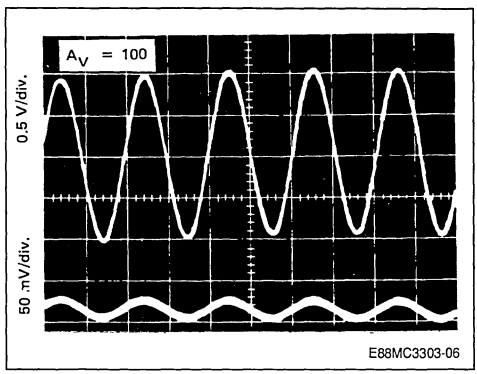
The transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input common-mode range can include the negative supply of ground, in single supply operation, without saturation either the input devices or the differential to single-ended converter.

The second stage consists of a standard current source load amplifier stage. The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operations. This is possible because class AB operation is utilized.

Each amplifier is biased from an internal voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

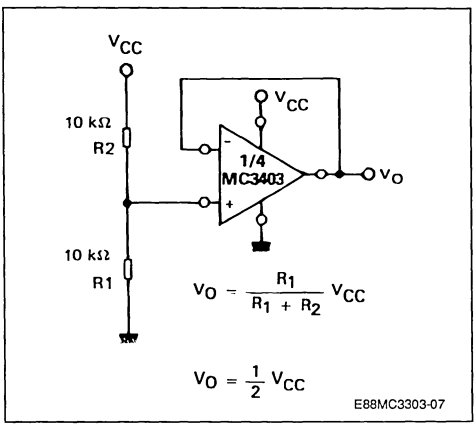
TYPICAL PERFORMANCE CURVES



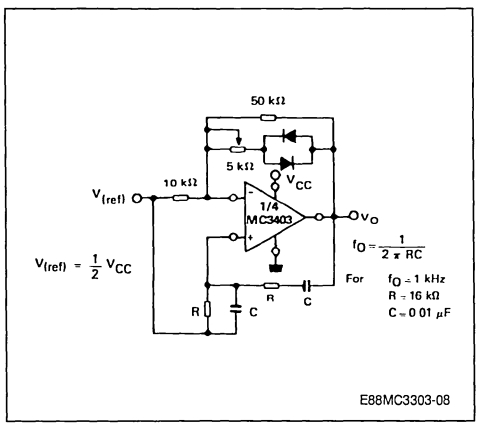


APPLICATION INFORMATION

VOLTAGE REFERENCE

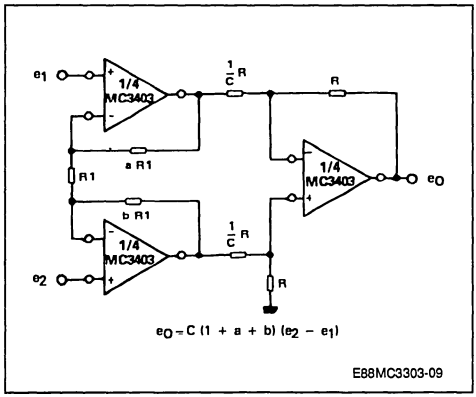


WIEN BRIDGE OSCILLATOR

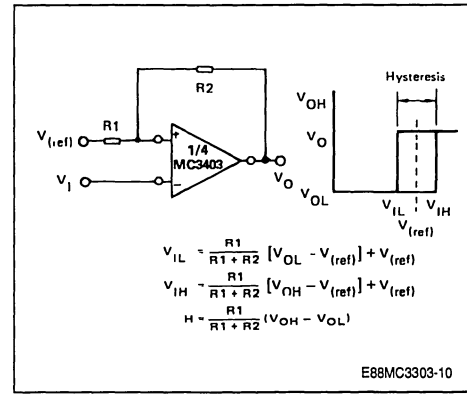


APPLICATION INFORMATION (continued)

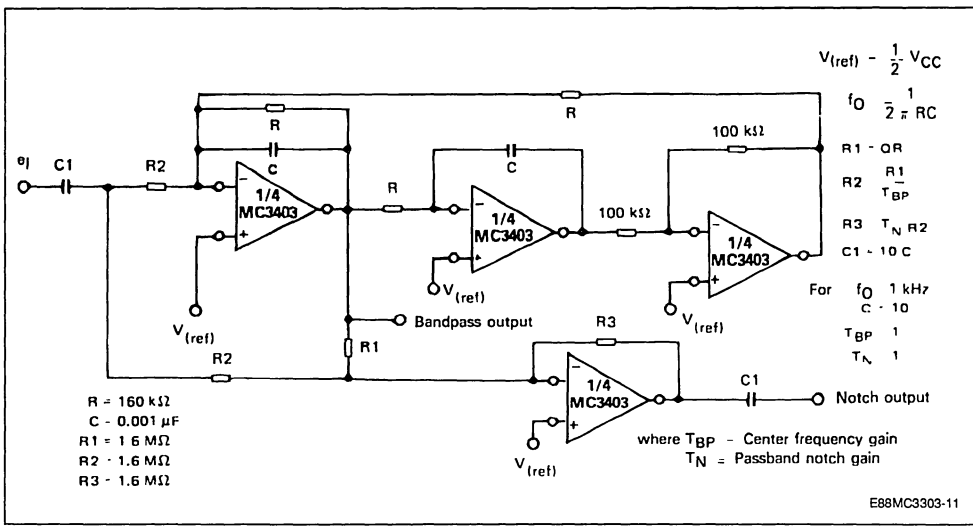
HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER



COMPARATOR WITH HYSTERESIS

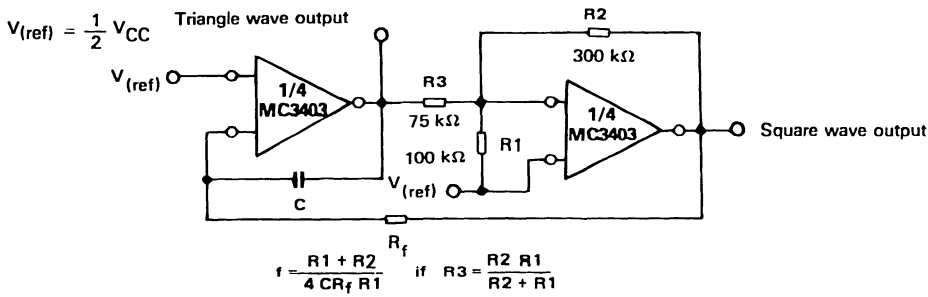


BI-QUAD FILTER



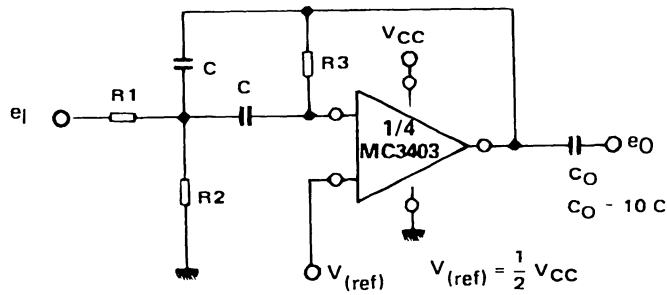
APPLICATION INFORMATION (continued)

FUNCTION GENERATOR



E88MC3303-12

MULTIPLE FEEDBACK BANDPASS FILTER



E88MC3303-13

Given f_O = Center frequency choose values f_O, C then : $R3 = \frac{Q}{\Pi f_O C}$

$A(f_O)$ = Gain at center frequency

$$R1 = \frac{R3}{2A\,(f_O)}$$

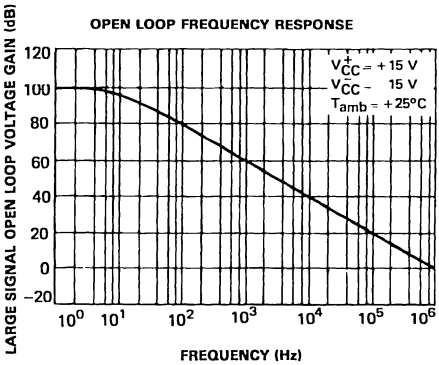
$$R2 = \frac{R1\ R5}{4Q^2\ R1 - R5}$$

For less than 10 % error operational amplifiers

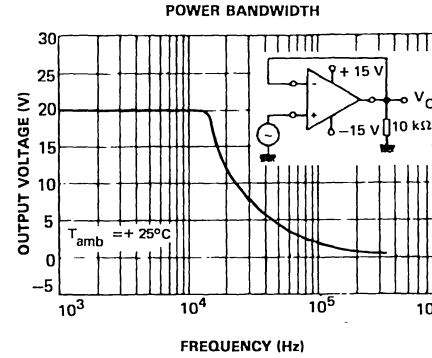
$\frac{Q_O f_O}{BW} < 0.1$ where f_O and BW are expressed in Hz

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

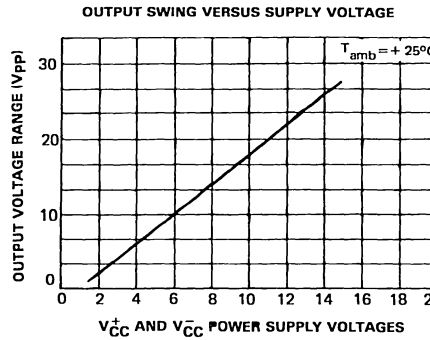
TYPICAL PERFORMANCE CURVES



E88MC3303-14



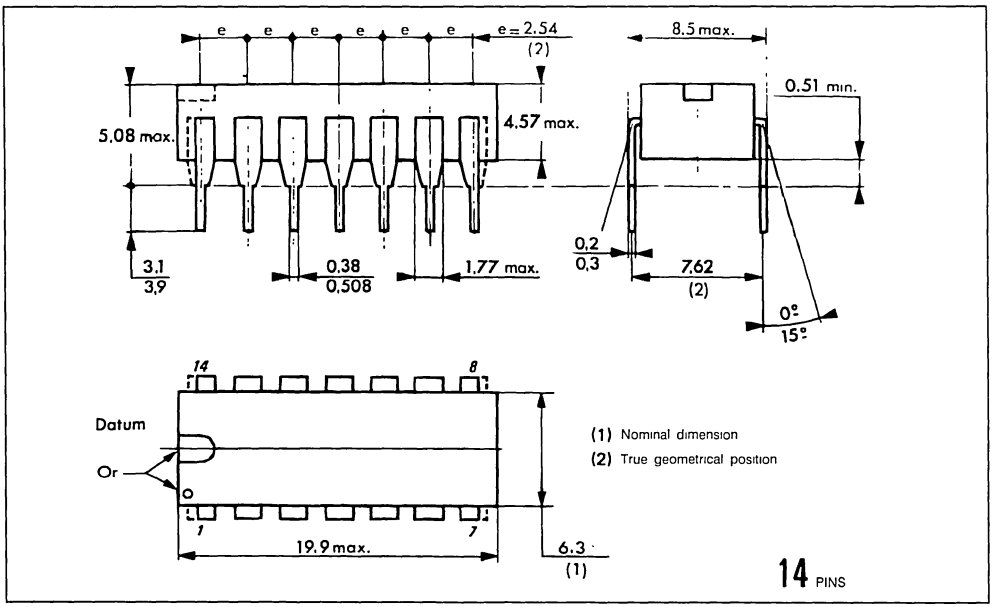
E88MC3303-15



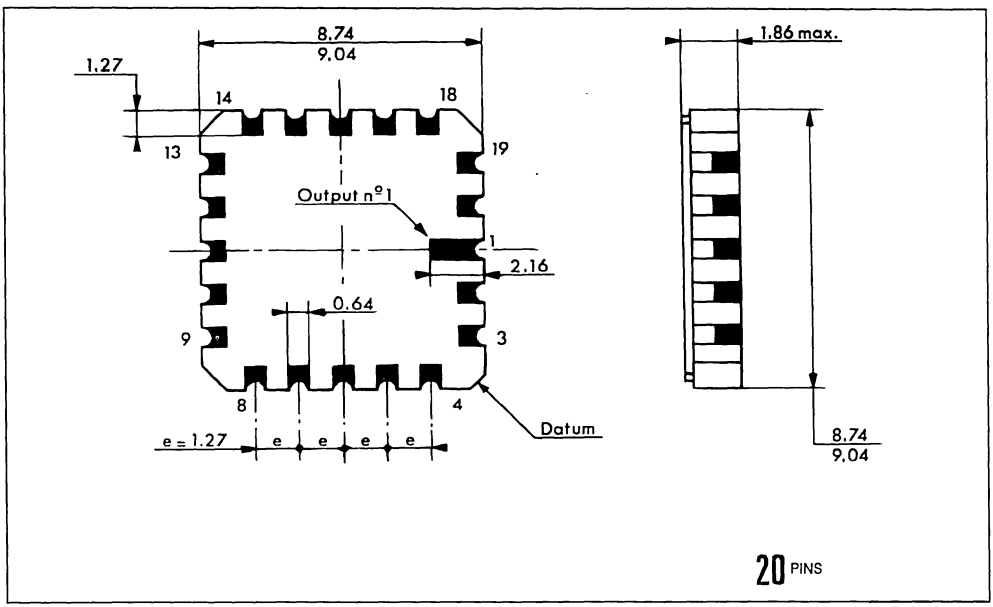
E88MC3303-16

PACKAGE MECHANICAL DATA

14 PINS – PLASTIC DIP OR CERDIP

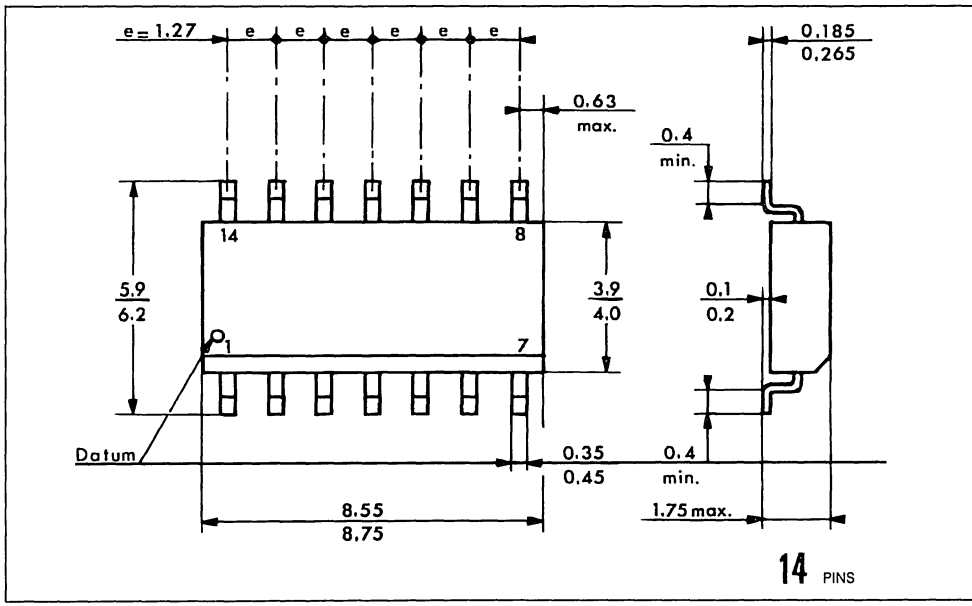


20 PINS – TRICECOP (LCC)



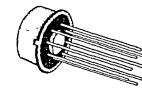
PACKAGE MECHANICAL DATA (continued)

14 PINS – PLASTIC MICROPACKAGE (SO)



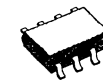
WIDEBAND DUAL OPERATIONAL AMPLIFIERS

- INTERNALLY COMPENSATED
- SHORT–CIRCUIT PROTECTION
- GAIN AND PHASE MATCH BETWEEN AMPLIFIERS
- LOW POWER CONSUMPTION
- PIN TO PIN COMPATIBLE WITH MC1458/LM358
- GAIN BANDWIDTH PRODUCT (at 20KHz) 5.5MHz



H
TO99
(Metal Can)

N
DIP8
(Plastic Package)
J
CERDIP8
(Cerdip Package)



D
SO8
(Plastic Micropackage)

DESCRIPTION

The MC4558 is a high performance monolithic dual operational amplifier constructed on a single siljcon chip.

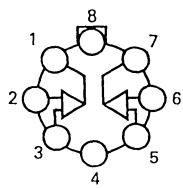
The circuit combines all the outstanding features of the MC1458 and, in addition, possesses three times the unity gain bandwidth of the industry standard.

ORDER CODES

Part Number	Temperature Range	Package			
		H	N	J	D
MC4558C	0 °C to + 70 °C	•	•	•	•
MC4558I	– 40 °C to + 105 °C	•	•	•	
Example : MC4558N					

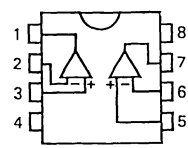
PIN CONNECTIONS (top views)

TO99



E88MC4558-00

DIP8/CERDIP8
SO8



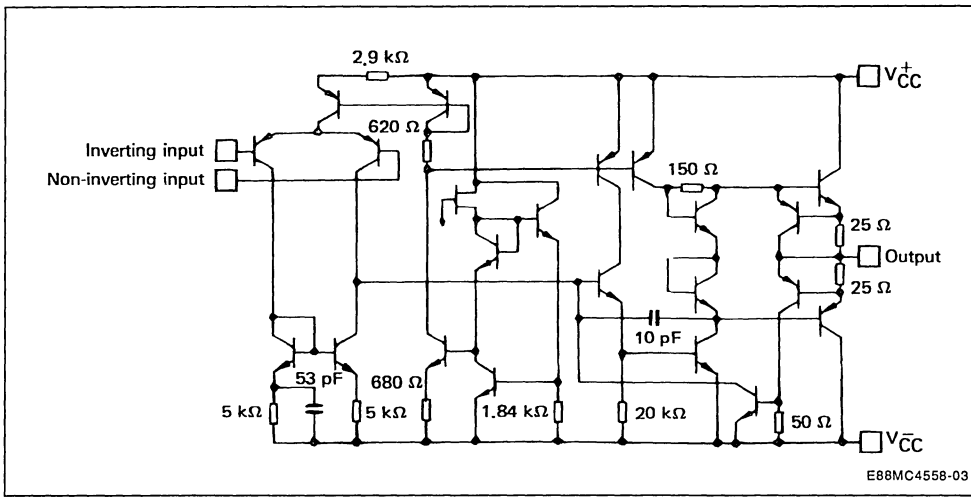
E88MC4558-01

1 – Output 1
2 – Inverting input 1
3 – Non-inverting input 1
4 – V_{CC}^-
5 – Non-inverting input 2
6 – Inverting input 2
7 – Output 2
8 – V_{CC}^+

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	MC4558I	MC4558C	Unit
V_{CC}	Supply Voltage	± 22	± 22	V
V_I	Input Voltage	± 15	± 15	V
V_{ID}	Differential Input Voltage	± 30	± 30	V
P_{tot}	Power Dissipation	680	680	mW
	Output Short-circuit Duration	Indefinite		
T_{oper}	Operating Free-air Temperature Range	− 40 to + 105	0 to + 70	°C
T_{stg}	Storage Temperature Range	− 65 to + 150	− 65 to + 150	°C

SCHEMATIC DIAGRAM (1/2 MC4558)



Case	Inverting Inputs	Non-inverting Inputs	V_{CC}^-	V_{CC}^+	Outputs
TO99 DIP8 CERDIP8 SO8	2.6	3.5	4	8	1.7

ELECTRICAL CHARACTERISTICS

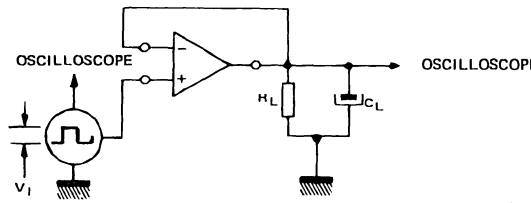
MC4558C : $0 \leq T_{amb} \leq +70$ °C, $V_{CC} = \pm 15$ V
MC4558I : $-40 \leq T_{amb} \leq +105$ °C, $V_{CC} = \pm 15$ V
(unless otherwise specified)

Symbol	Parameter	MC4558 I, C			Unit
		Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage ($R_S \leq 10$ kΩ) $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$		1	5 6	mV
I_{IO}	Input Offset Current $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$		2	20 40	nA
I_{IB}	Input Bias Current $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$		30	100 200	nA
A_{VD}	Large Signal Voltage Gain ($V_O = \pm 10$ V, $R_L = 2$ kΩ) $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$	 50 25	 200		V/mV
S_{VR}	Supply Voltage Rejection Ratio ($R_S \leq 10$ kΩ) $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$	 77 77	 90		dB
I_{CC}	Supply Current, all Amp, no Load $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$		2.3	4.5 6	mA
V_I	Input Voltage Range $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$	−12 −12		+12 +12	V
CMR	Common-mode Rejection Ratio ($R_S \leq 10$ kΩ) $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$	 70 70	 90		dB
I_{OS}	Output Short-circuit Current $T_{amb} = 25$ °C	10	20	40	mA
$\pm V_{OPP}$	Output Voltage Swing $T_{amb} = 25$ °C $R_L = 10$ kΩ $R_L = 2$ kΩ $T_{min} \leq T_{amb} \leq T_{max}$ $R_L = 10$ kΩ $R_L = 2$ kΩ	 12 10 12 10	 14 13		V
S_{VO}	Slew-rate ($V_I = \pm 10$ V, $R_L = 2$ kΩ, $C_L \leq 100$ pF, $T_{amb} = 25$ °C, unity gain)	1.5	2.2		V/µs
t_r	Rise Time ($V_I = \pm 20$ mV, $R_L = 2$ kΩ, $C_L \geq 100$ pF, $T_{amb} = 25$ °C, unity gain)		0.3		µs
K_{OV}	Overshoot ($V_I = \pm 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF, $T_{amb} = 25$ °C, unity gain)		15		%
R_I	Input Resistance, $T_{amb} = 25$ °C	0.3	2		MΩ
C_I	Input Capacitance, $T_{amb} = 25$ °C		1.4		pF
R_O	Output Resistance, $T_{amb} = 25$ °C		75		Ω
B	Unity Gain Bandwidth $T_{amb} = 25$ °C		2.8		MHz

ELECTRICAL CHARACTERISTICS (continued)

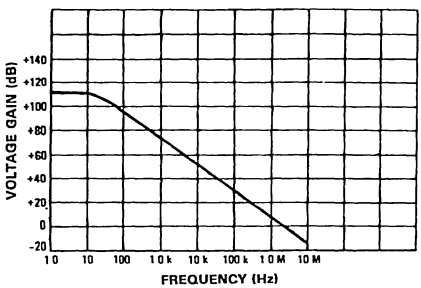
Symbol	Parameter	MC4558 I, C			Unit
		Min.	Typ.	Max.	
GPB	Gain Bandwidth Product (V_I = 10 mV, R_L = 2 kΩ, $C_L \leq$ 100 pF, f = 20 kHz, T_{amb} = 25 °C)	4	5.5	7	MHz
THD	Total Harmonic Distortion (f = 1 kHz, A_V = 20 dB, R_L = 2 kΩ, V_O = 2 V_{PP}, $C_L \leq$ 100 pF, T_{amb} = 25 °C)		0.008		%
V_n	Equivalent Input Noise Voltage (f = kHz, R_g = 100 Ω)		12		nV/√Hz

TRANSIENT RESPONSE TEST CIRCUIT



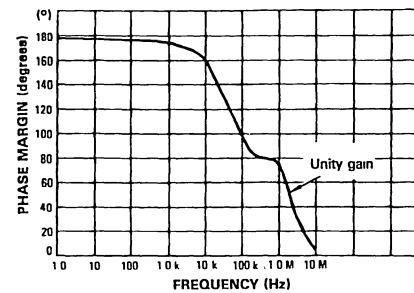
E88MC4558-02

OPEN LOOP FREQUENCY RESPONSE



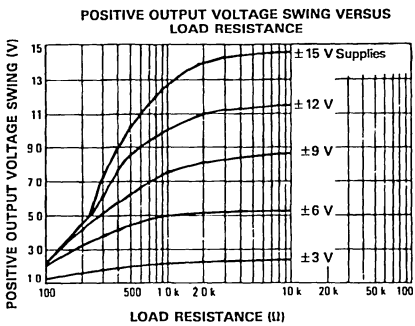
E88MC4558-04

PHASE MARGIN VERSUS FREQUENCY



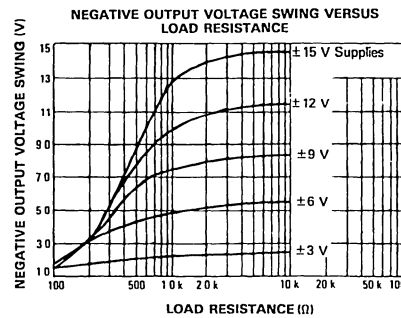
E88MC4558-05

POSITIVE OUTPUT VOLTAGE SWING VERSUS LOAD RESISTANCE

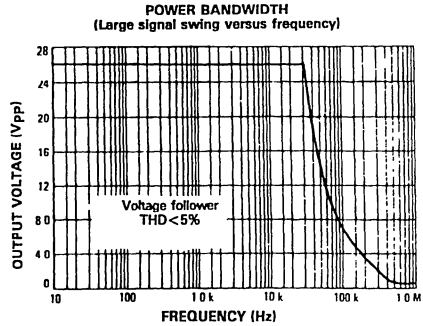


E88MC4558-06

NEGATIVE OUTPUT VOLTAGE SWING VERSUS LOAD RESISTANCE



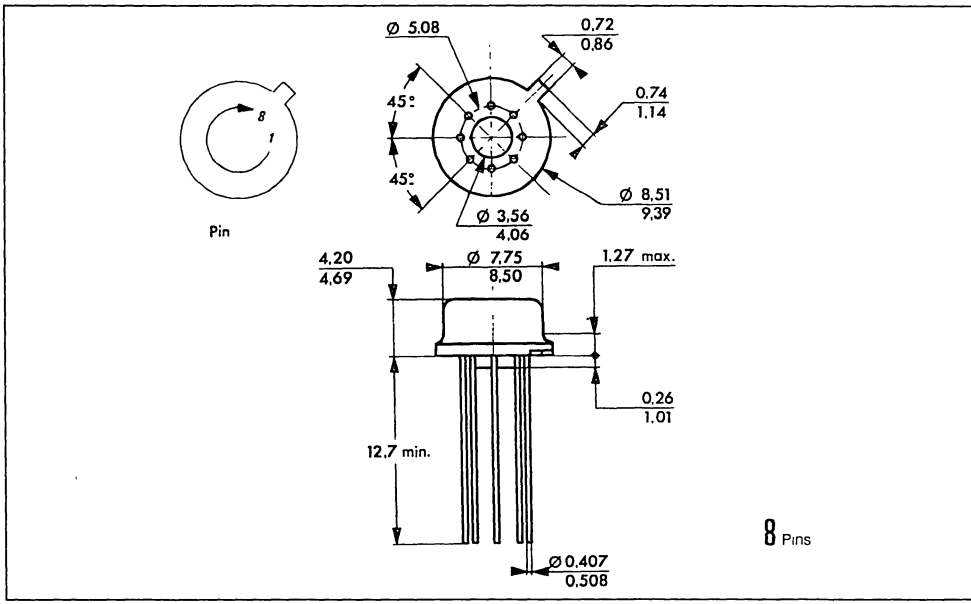
E88MC4558-07



E88MC4558-08

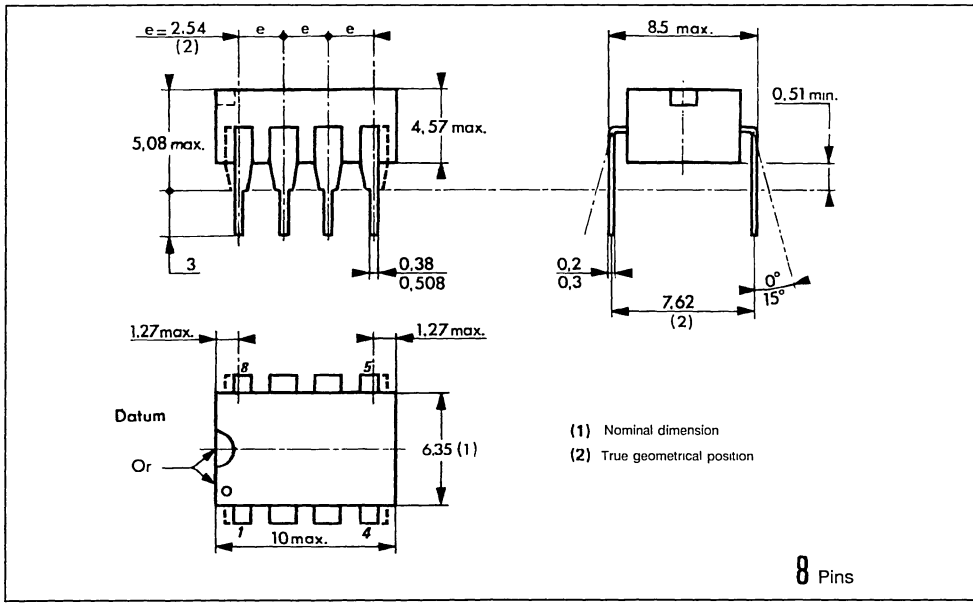
PACKAGE MECHANICAL DATA

8 PINS – METAL CAN TO99

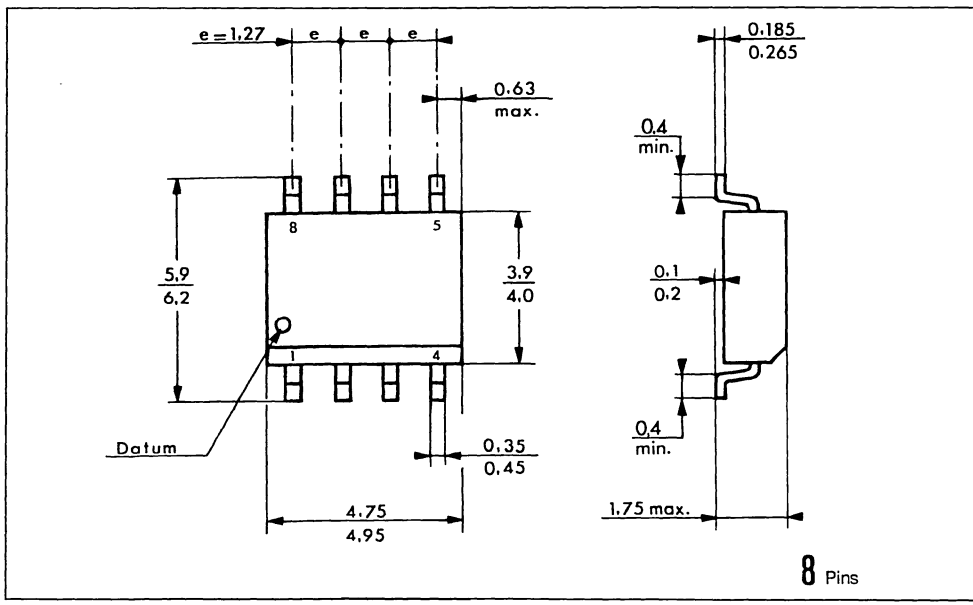


PACKAGE MECHANICAL DATA (continued)

8 PINS – PLASTIC DIP OR CERDIP



8 PINS – PLASTIC MICROPACKAGE (SO)

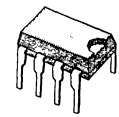


SGS-THOMSON MICROELECTRONICS

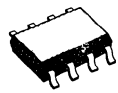
NE555 - SA555 SE555

PRECISION TIMERS

- LOW TURN OFF TIME
- MAXIMUM OPERATING FREQUENCY GREATER THAN 500Hz
- TIMING FROM MICROSECONDS TO HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- HIGH OUTPUT CURRENT CAN SOURCE OR SINK 200mA
- ADJUSTABLE DUTY CYCLE
- TTL COMPATIBLE
- TEMPERATURE STABILITY OF 0.005% PER °C

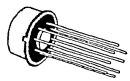


N
MINIDIP
(Plastic Package)



D
SO-8
(Plastic Micropackage)

J
MINICERDIP
(Cerdip Package)



H
TO-99
(Metal Can)

DESCRIPTION

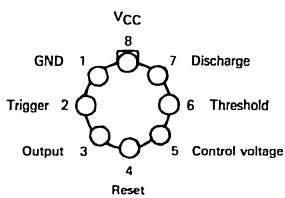
The NE555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA. The NE555 is available in plastic and ceramic minidip package and in a 8-lead micropackage and in metal can package version.

ORDER CODES

Part Number	Temperature Range	Package			
		H	N	J	D
NE555	0°C to 70°C	•	•	•	•
SA555	– 40°C to 105°C	•	•	•	•
SE555	– 55°C to 125°C	•			

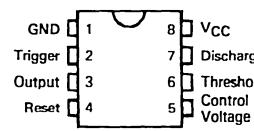
PIN CONNECTION (top views)

TO99



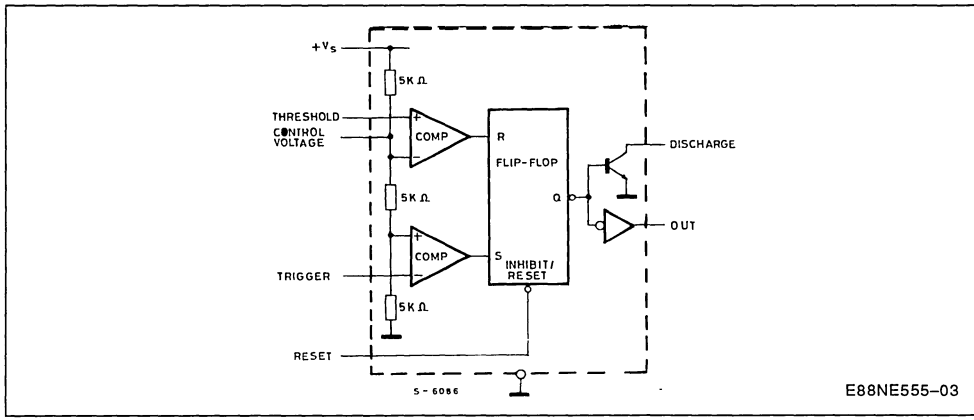
E88NE555-01

DIP8 CERDIP8
SO8



E88NE555-02

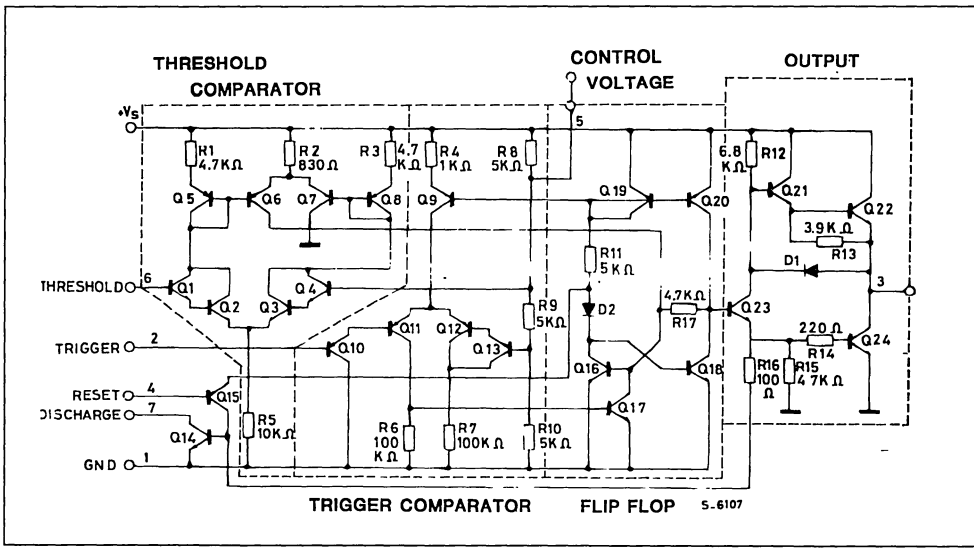
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage for **SE555** for **NE555**	18 16	V
T_{op}	Operating Temperature Range for **NE555** for **SA555** for **SE555**	0 to 70 – 40 to 105 – 55 to 125	°C
T_j	Junction Temperature	150	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C

SCHEMATIC DIAGRAM



THERMAL DATA

			Plastic Dip	Ceramic Dip	SO8	Metal Can
$Rth_{j\text{-}amb}$	Thermal Resistance Junction-ambient	max.	120°C/W	150°C/W	200°C/W	155°C/W

ELECTRICAL CHARACTERISTICS

T_{amb} = + 25°C, V_S = + 5V to + 15V (unless otherwise specified)

Symbol	Parameter	SE555			NE555/SA555			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{CC}	Supply Voltage	4.5		18	4.5		16	V
I_S	Supply Current (R_L ∞) Note 1							
	Low State V_{CC} = + 5V		3	5		3	6	mA
	V_{CC} = + 15V		10	12		10	15	
	High State V_{CC} = 5V		2			2		
	Timing Error (monostable)							
	(R_A = 2 to 100kΩ,C = 0.1µF)							
	Initial Accuracy (note 2)		0.5	2		1	3	%
	Drift with Temperature		30	100		50		ppm/°C
	Drift with Supply Voltage		0.05	0.2		0.1	0.5	%/V
	Timing Error (astable)							
	(R_A, R_B = 1kΩ to 100kΩ, C = 0.1µF,							
	V_S = + 15V) initial Accuracy (note 2)		1.5			2.25		%
	Drift with Temperature		90			150		ppm/°C
	Drift with Supply Voltage		0.15			0.3		%/V
V_{CL}	Control Voltage level							
	V_{CC} = + 15V	9.6	10	10.4	9	10	11	V
	V_{CC} = + 5V	2.9	3.33	3.8	2.6	3.33	4	
V_{th}	Threshold Voltage							
	V_{CC} = + 15V	9.4	10	10.6	8.8	10	11.2	V
	V_{CC} = + 5V	2.7	3.33	4	2.4	3.33	4.2	
I_{th}	Threshold Current (note 3)		0.1	0.25		0.1	0.25	µA
V_{trig}	Trigger Voltage							
	V_{CC} = + 15V	4.8	5	5.2	4.5	5	5.6	V
	V_{CC} = + 5V	1.45	1.67	1.9	1.1	1.67	2.2	
I_{trig}	Trigger Current (V_{trig} = 0V)		0.5	0.9		0.5	2.0	µA
V_{reset}	Reset Voltage (note 4)	0.4	0.7	1	0.4	0.7	1	V
I_{reset}	Reset Current							
	V_{reset} = + 0.4V		0.1	0.4		0.1	0.4	mA
	V_{reset} = 0V		0.4	1		0.4	1.5	
V_{OL}	Low Level Output Voltage							
	V_{CC} = + 15V, $I_{O(sink)}$ = 10mA		0.1	0.15		0.1	0.25	
	$I_{O(sink)}$ = 50mA		0.4	0.5		0.4	0.75	
	$I_{O(sink)}$ = 100mA		2	2.2		2	2.5	V
	$I_{O(sink)}$ = 200mA		2.5			2.5		
	V_{CC} = + 5V, $I_{O(sink)}$ = 8mA		0.1	0.25		0.3	0.4	
	$I_{O(sink)}$ = 5mA		0.05	0.2		0.25	0.35	
V_{OH}	High Level Output Voltage							
	V_{CC} = + 15V, $I_{O(source)}$ = 200mA		12.5			12.5		V
	$I_{O(source)}$ = 100mA	13	13.3		12.75	13.3		
	V_{CC} = + 5V, $I_{O(source)}$ = 100mA	3	3.3		2.75	3.3		

ELECTRICAL CHARACTERISTICS(continued)

Symbol	Parameter	SE555			NE555/SA555			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$I_{dis(off)}$	Discharge Pin Leakage Current (output high)		20	100		20	100	nA
$V_{dis(sat)}$	Discharge pin Saturation Voltage (output low) (note 5) V_{CC} = + 15V, I_{dis} = 15mA V_{CC} = + 5V, I_{dis} = 4.5mA		 180 80	 480 200		 180 80	 480 200	mV
t_r t_f	Output Rise Time Output Fall Time		100 100	200 200		100 100	300 300	ns
t_{off}	Turn off Time (note 6), V_{reset} = V_{CC}		0.5			0.5		µs

Notes : 1. Supply current when output is high is typically 1 mA less.
2 Tested at V_S = + 5V and V_S = +15V
3. This will determine the maximum value of $R_A + R_B$ for + 15V operation the max total is R = 20MΩ and for 5V operation, the max total R = 3.5MΩ.
4. Specified with trigger input high.
5 No protection against excessive Pin 7 current is necessary, providing the package dissipation rating will not be exceeded.
6. Time measured from a positive going input pulse from 0 to 0.8xVS into the threshold to the drop from high to Low of the output trigger is tied to treshold.

Figure 1 : Minimum Pulse Width Required for Trigering.

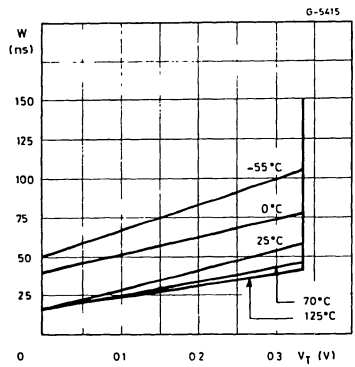


Figure 2 : Supply Current Vs. Supply Voltage.

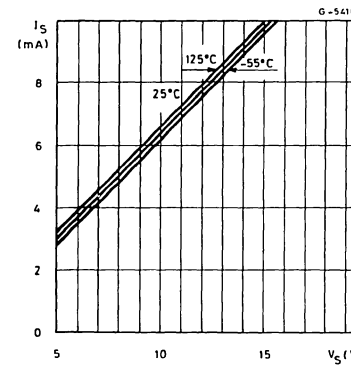


Figure 3 : Delay Time Vs. Temperature.

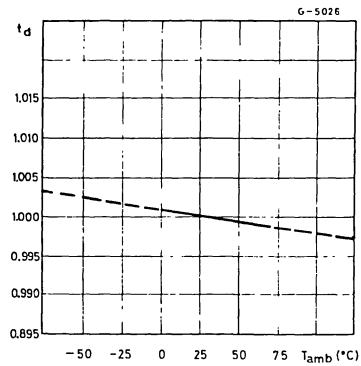


Figure 4 : Low Output Voltage Vs. Output Sink Current.

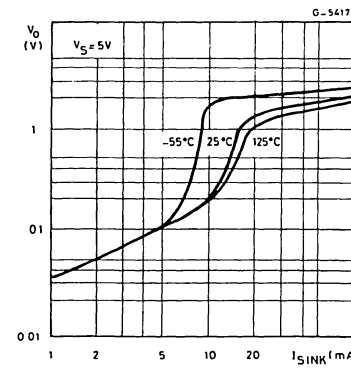


Figure 5 : Low Output Voltage Vs. Output Sink Current.

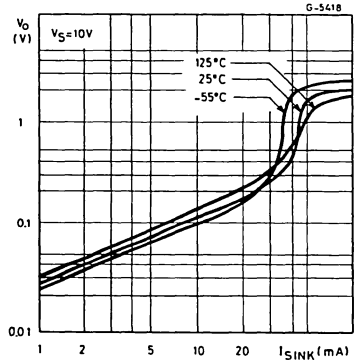


Figure 6 : Low Output Voltage Vs. Output Sink Current.

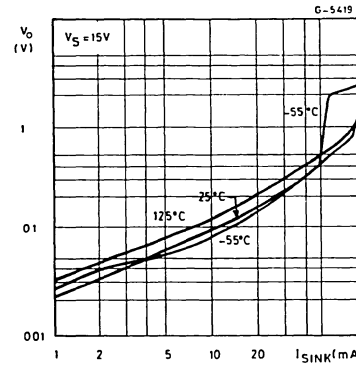


Figure 7 : High Output Voltage Drop Vs. Output Source Current.

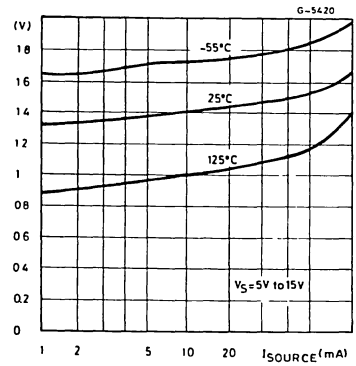


Figure 8 : Delay Time Vs. Supply Voltage.

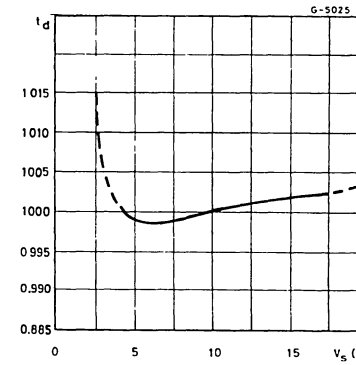
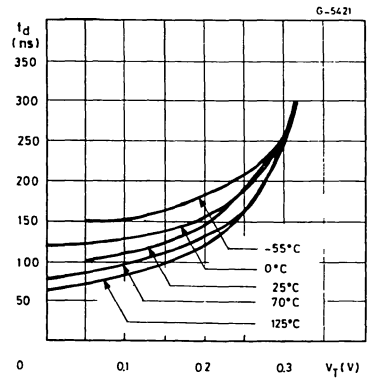


Figure 9 : Propagation Delay Vs. Voltage Level of Trigger Value.



APPLICATION INFORMATION

MONOSTABLE OPERATION

In the monostable mode, the timer functions as a one-shot. Referring to figure 10 the external capacitor is initially held discharged by a transtor inside the timer.

The circuit triggers on a negative-going input signal when the level reaches 1/3 Vs. Once triggered, the circuit remains in this state until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by t = 1.1 R1C1 and is easily determined by figure 12. Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (pin 4) and the Trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse in applied, the output is driven to its LOW state.

When a negative trigger pulse is applied to pin 2, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant $\tau = R1C1$. When the voltage across the capacitor equals 2/3 Vs, the comparator resets the flip-flop which then discharge the capacitor rapidly and drivers the output to its LOW state.

Figure 11 shows the actual waveforms generated in this mode of operation.

When Reset is not used, it should be tied high to avoid any possibly or false triggering.

Figure 10.

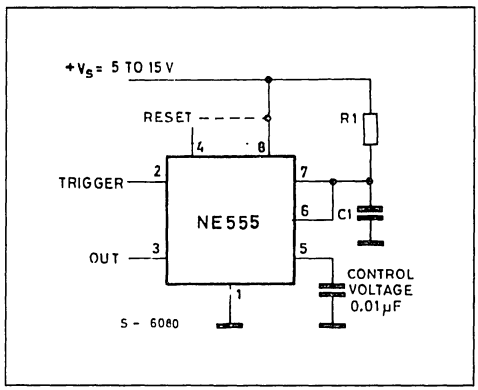


Figure 11.

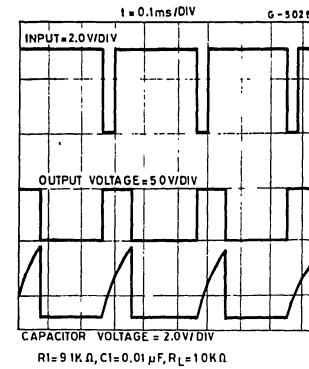
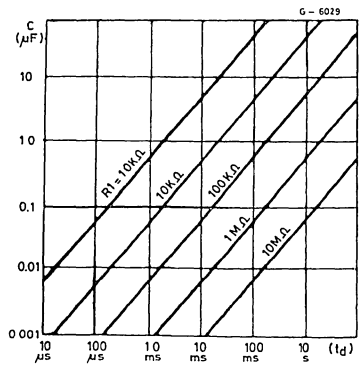


Figure 12.



ASTABLE OPERATION

When the circuit is connected as shown in figure 13 (pin 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R1 and R2 and discharges through R2 only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C1 charges and discharges between 1/3 V_S and 2/3 V_S. As in the triggered mode, the charge and discharge times and therefore frequency are independent of the supply voltage.

Figure 14 shows actual waveforms generated in this mode of operation.

Figure 13.

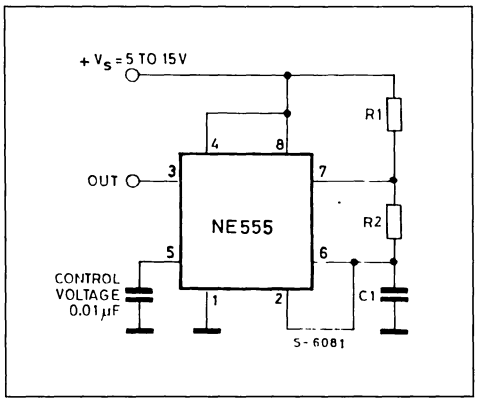
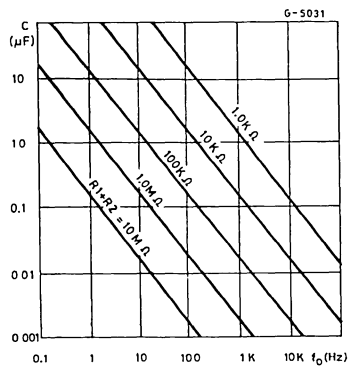


Figure 15 : FreeRunning Frequency vs. R1, R2, and C1.



The charge time (output HIGH) is given by :

$t_1 = 0.693 (R1 + R2) C1$

and the discharge time (output LOW) by :

$t_2 = 0.693 (R2) C1$

Thus the total period T is given by :

$T = t_1 + t_2 = 0.693 (R1 + 2R2) C1$

The frequency of oscillation is then :

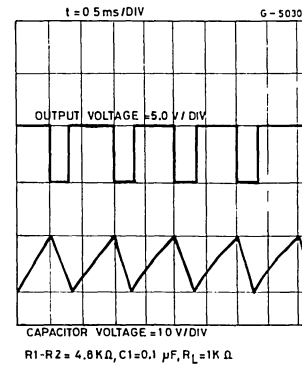
$$f = \frac{1}{T} = \frac{1.44}{(R1 + 2R2) C1}$$

and may be easily found by figure 15.

The duty cycle is given by :

$$D = \frac{R2}{R1 + 2R2}$$

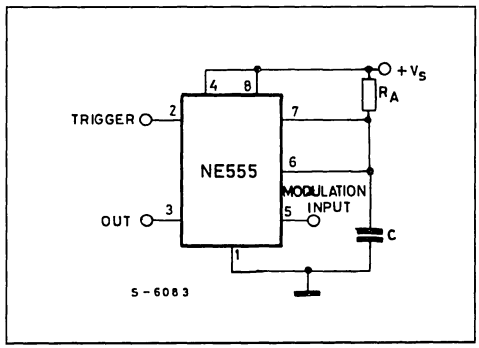
Figure 14.



PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. Figure 16 shows the circuit.

Figure 16 : Pulse Width Modulator.



LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. Figure 17 shows a circuit configuration that will perform this function.

Figure 17.

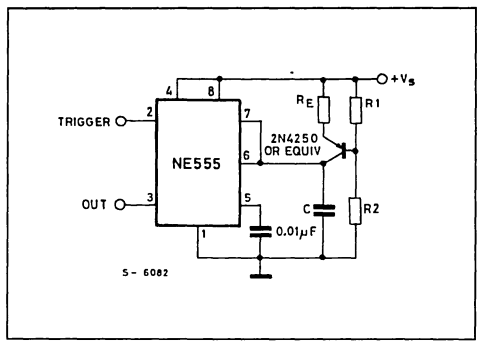


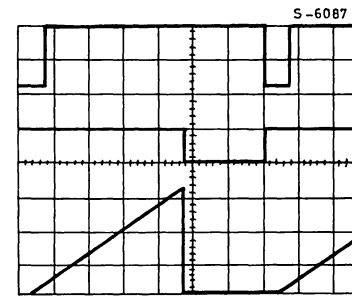
Figure 18 shows waveforms generator by the linear ramp.

The time interval is given by :

$$T = \frac{2/3\ V_S\ R_E\ (R_1 + R_2)\ C}{R_1\ V_S - V_{BE}\ (R_1 + R_2)} \quad V_{BE} \equiv 0.6V$$

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_S and trigger the lower comparator.

Figure 18 : Linear Ramp.



V_S = 5V
TIME = 20µs/DIV
R_1 = 47KΩ
R_2 = 100KΩ
R_E = 2.7KΩ
C = 0.01µF

Top trace : input 3V/DIV
Middle trace : output 5V/DIV
Bottom trace : output 5V/DIV
Bottom trace : capacitor voltage 1V/DIV

50% DUTY CYCLE OSCILLATOR

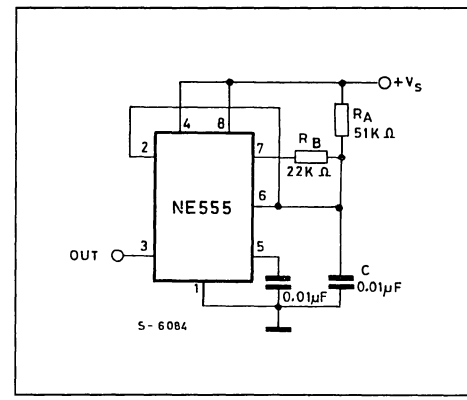
For a 50% duty cycle the resistors R_A and R_B may be connected as in figure 19. The time period for the output high is the same as previous,
$t_1 = 0.693\ R_A\ C$.

For the output low it is t_2 =

$$[(R_A\ R_B)/(R_A + R_B)]\ C \ln\left\{\frac{R_B - 2R_A}{2R_B - R_A}\right\}$$

Thus the frequency of oscillation is $f = \frac{1}{t_1 + t_2}$

Figure 19 : 50% Duty Cycle Oscillator.



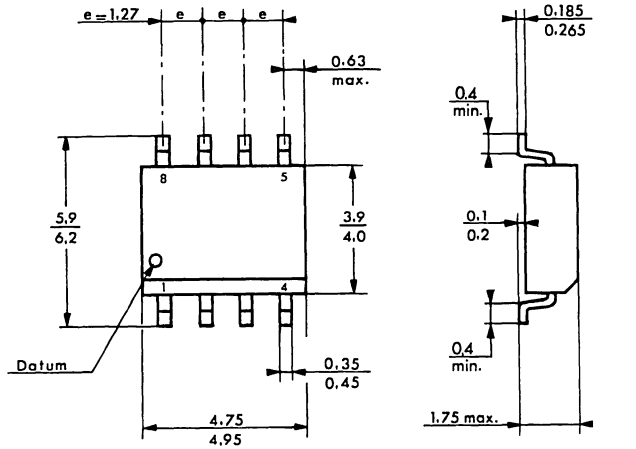
ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1µF in parallel with 1µF electrolytic.

PACKAGE MECHANICAL DATA

8 PINS – PLASTIC MICROPACKAGE (SO)

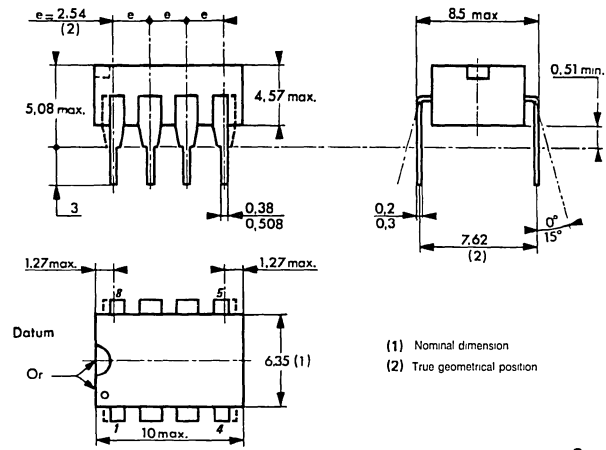
mm



8 Pins

8 PINS – PLASTIC DIP OR CERDIP

mm

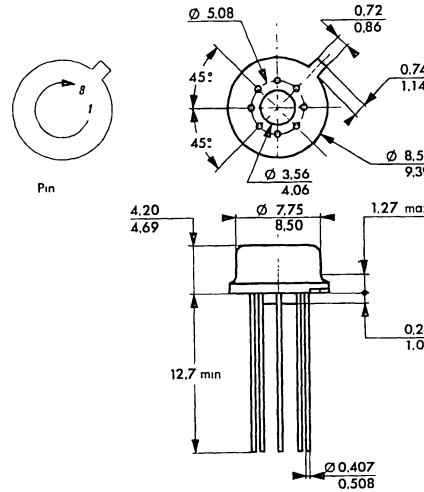


(1) Nominal dimension
(2) True geometrical position

8 Pins

8 PINS – METAL CAN TO 99

mm



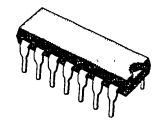
8 Pins

SGS-THOMSON MICROELECTRONICS

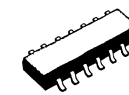
NE556 - SA556 SE556

PRECISION DUAL TIMERS

- LOW TURN-OFF TIME
- MAXIMUM OPERATING FREQUENCY GREATER THAN 500 kHz
- TIMING FROM MICROSECONDS TO HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- HIGH OUTPUT CURRENT CAN SOURCE OR SINK 200 mA
- ADJUSTABLE DUTY CYCLE
- TTL COMPATIBLE
- TEMPERATURE STABILITY OF 0.005% PER °C



N
DIP14
(Plastic Package)
J
CERDIP14
(Cerdip Package)



D
SO-14
(Plastic Micropackage)

DESCRIPTION

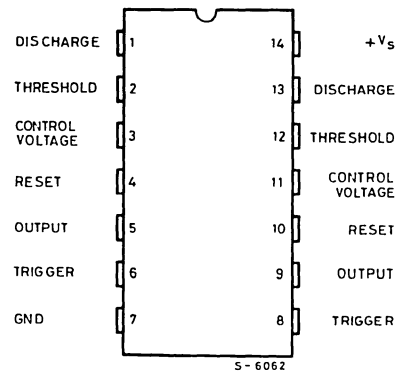
The JNE556 dual monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on failling waveforms, and the output structure can source or sink up to 200mA.

ORDER CODES

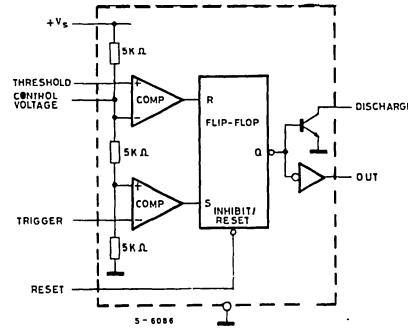
Part Number	Temperature Range	Package		
		N	J	D
NE556	0°C to + 70°C	•	•	•
SA556	– 40°C to + 105°C	•	•	•
SE556	– 55°C to + 125°C		•	

PIN CONNECTION (top views)

DIP 14 – CERDIP 14 – SO 14



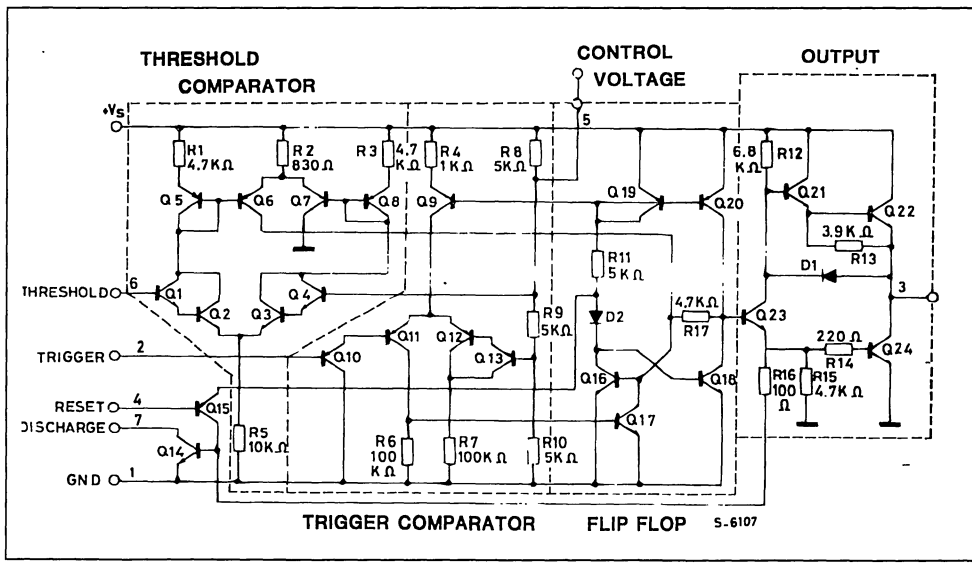
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage for **SE556** for **NE556**	18 16	V
T_{op}	Operating Temperature Range for **NE556** for **SA556** for **SE556**	0 to 70 – 40 to 105 – 55 to 125	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C
T_j	Junction Temperature	150	°C

SCHEMATIC DIAGRAM



THERMAL DATA

			Ceramic DIP14	SO14	Plastic DIP14
$Rt_{h\ j\text{-}amb}$	Thermal Resistance Junction-ambient	max.	150°C/W	165°C/W	200°C/W

ELECTRICAL CHARACTERISTICS

T_{amb} = + 25°C, V_{CC} = + 5V to + 15V (unless otherwise specified)

Symbol	Parameter	SE556			SA556			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{CC}	Supply Voltage	4.5		18	4.5		16	V
I_S	Supply Current (R_L ∞) Note 1							mA
	Low State V_{CC} = + 5V		6	10		6	12	
	V_{CC} = + 15V		20	24		20	30	
	High State V_{CC} = 5V		4			4		
	Timing Error (monostable)							
	(R_A = 2 to 100kΩ, C = 0.1µF)							
	Initial Accuracy (note 2)		0.5	2		1	3	%
	Drift with Temperature		30	100		50		ppm/°C
	Drift with Supply Voltage		0.05	0.2		0.1	0.5	%/V
	Timing Error (astable)							
	(R_A, R_B = 1kΩ to 100kΩ, C = 0.1µF,							
	V_{CC} = + 15V) initial Accuracy (note 2)		1.5			2.25		%
	Drift with Temperature		90			150		ppm/°C
	Drift with Voltage		0.15			0.3		%/V
V_{CL}	Control Voltage level							V
	V_{CC} = + 15V	9.6	10	10.4	9	10	11	
	V_{CC} = + 5V	2.9	3.33	3.8	2.6	3.33	4	
V_{th}	Threshold Voltage							V
	V_{CC} = + 15V	9.4	10	10.6	8.8	10	11.2	
	V_{CC} = + 5V	2.7	3.33	4	2.4	3.33	4.2	
I_{th}	Threshold Current (note 3)		0.1	0.25		0.1	0.25	µA
V_{trig}	Trigger Voltage							V
	V_{CC} = + 15V	4.8	5	5.2	4.5	5	5.6	
	V_{CC} = + 5V	1.45	1.67	1.9	1.1	1.67	2.2	
I_{trig}	Trigger Current (V_{trig} = 0V)		0.5	0.9		0.5	2	µA
V_{reset}	Reset Voltage (note 4)	0.4	0.7	1	0.4	0.7	1	V
I_{reset}	Reset Current							mA
	V_{reset} = + 0.4V		0.1	0.4		0.1	0.4	
	V_{reset} = 0V		0.4	1		0.4	1.5	
V_{OL}	Low Level Output Voltage							V
	V_{CC} = + 15V, $I_{O(sink)}$ = 10mA		0.1	0.15		0.1	0.25	
	$I_{O(sink)}$ = 50mA		0.4	0.5		0.4	0.75	
	$I_{O(sink)}$ = 100mA		2	2.2		2	2.5	
	$I_{O(sink)}$ = 200mA		2.5			2.5		
	V_{CC} = + 5V, $I_{O(sink)}$ = 8mA		0.1	0.25		0.3	0.4	
	$I_{O(sink)}$ = 5mA		0.05	0.2		0.25	0.35	
V_{OH}	High Level Output Voltage							V
	V_{CC} = + 15V, $I_{O(source)}$ = 200mA		12.5			12.5		
	$I_{O(source)}$ = 100mA	13	13.3		12.75	13.3		
	V_{CC} = + 5V, $I_{O(source)}$ = 100mA	3	3.3		2.75	3.3		

ELECTRICAL CHARACTERISTICS(continued)

Symbol	Parameter	SE556			SA556			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$I_{dis(off)}$	Discharge Pin Leakage Current (output high)		20	100		20	100	nA
$V_{dis(sat)}$	Discharge pin Saturation Voltage (output low) (note 5)							mV
	V_{CC} = + 15V, I_{dis} = 15mA		180	480		180	480	
	V_{CC} = + 5V, I_{dis} = 4.5mA		80	200		80	200	
t_r	Output Rise Time		100	200		100	300	ns
t_f	Output Fall Time		100	200		100	300	
t_{off}	Turn off Time (note 6), V_{reset} = V_S		0.5			0.5		µs

Notes : 1. Supply current when output is high is typically 1mA less.
2. Tested at V_S = + 5V and V_S = +15V.
3. This will determine the maximum value of $R_A + R_B$ for + 15V operation the max total is R = 20MΩ and for 5V operation, the Max total R = 3.5MΩ.
4. Specified with trigger input high.
5. No protection against excessive pin 7 current is necessary, providing the package dissipation rating will not be exceeded.
6. Time measurement from a positive going Input pulse from 0 to 0.8xV_S into the threshold to the drop from high to low of the output trigger is tied to threshold.

Figure 1 : Minimum Pulse Width Required for Triggering.

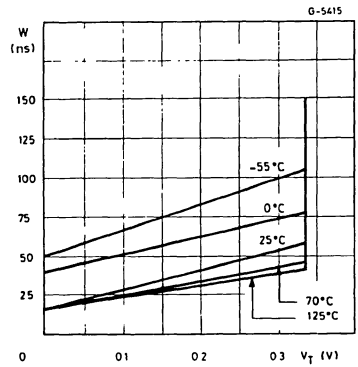


Figure 2 : Supply Current vs. Supply Voltage.

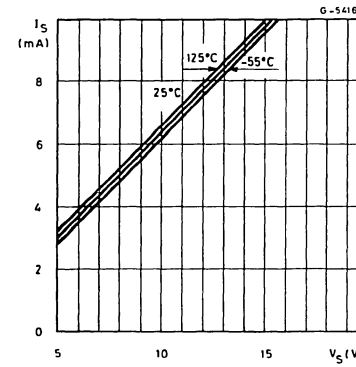


Figure 3 : Delay Time Vs. Temperature.

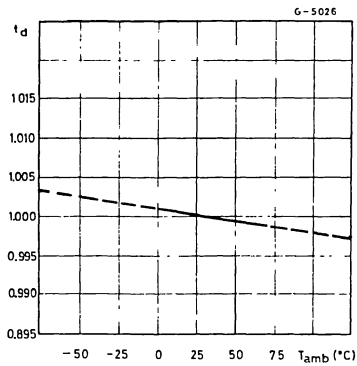


Figure 4 : Low Output Voltage Vs. Output Sink Current.

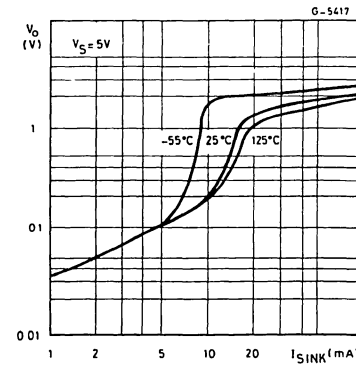


Figure 5 : Low Output Voltage Vs. Output Sink Current.

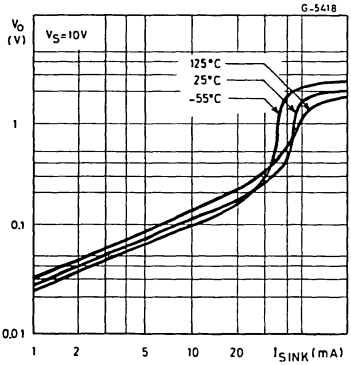


Figure 6 : Low Output Voltage Vs. Output Sink Current.

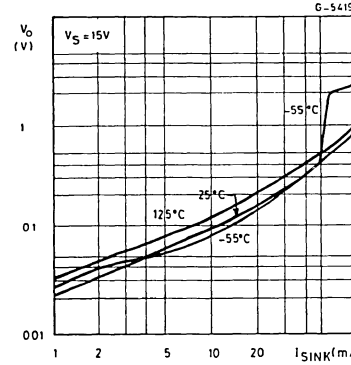


Figure 7 : High Output Voltage Drop Vs. Output Source Current.

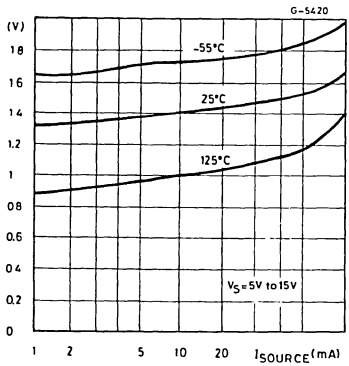


Figure 8 : Delay Time Vs. Supply Voltage.

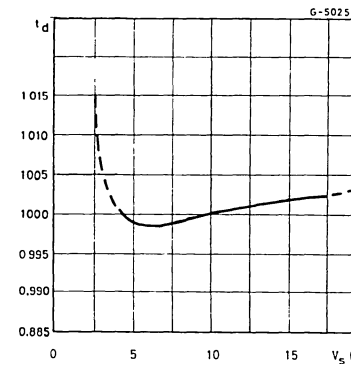
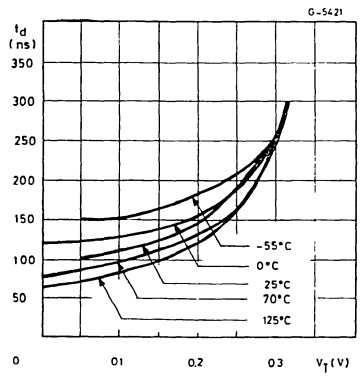
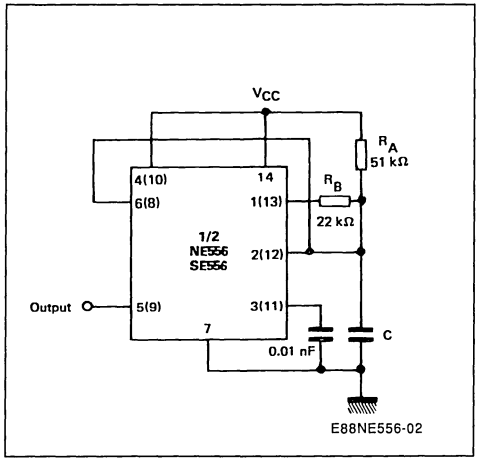


Figure 9 : Propagation Delay Vs. Voltage Level of Trigger Value.



TYPICAL APPLICATION

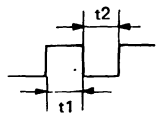
50% DUTY CYCLE OSCILLATOR



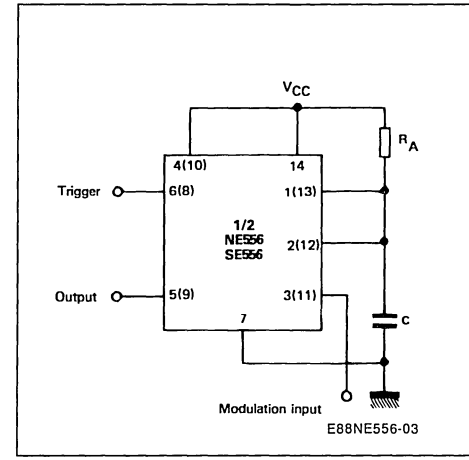
$t1 = 0.693\ R_A.C$

$t2 = [(R_A\ R_B)/(R_A + R_B)]C \quad \ln\left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$

$f = \frac{1}{t1+t2} \quad R_B < \frac{1}{2} R_A$

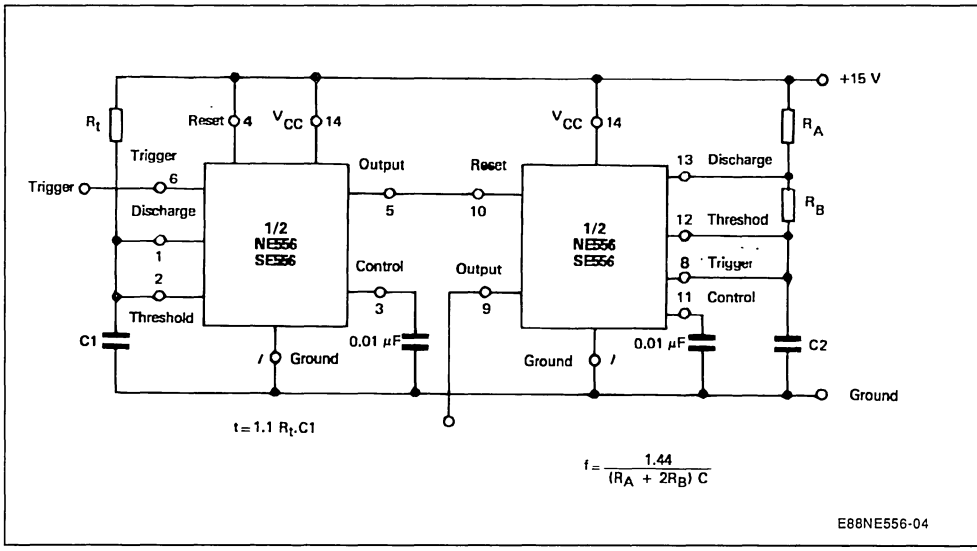


PULSE WIDTH MODULATOR

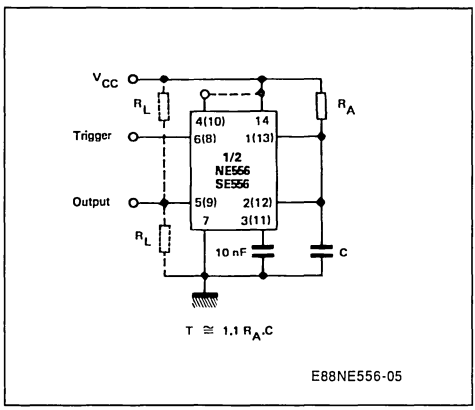


TONE BURST GENERATOR

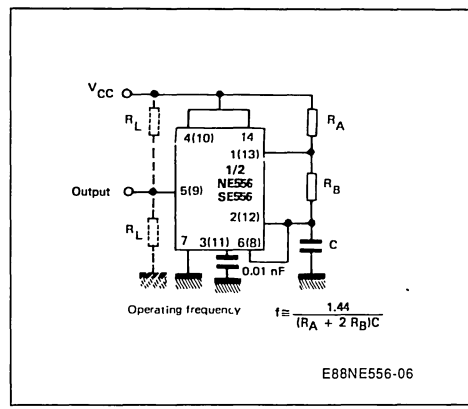
For a tone burst generator the first timer is used as a monostable and determines the tone duration when triggered by a positive pulse at pin 6. The second timer is enabled by the high output of the monostable. It is connected as an astable and determines the frequency of the tone.



MONOSTABLE OPERATION

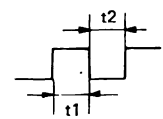


ASTABLE OPERATION



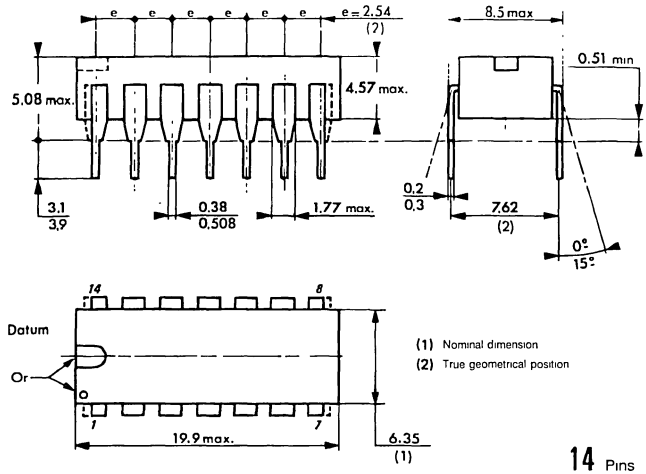
t1 = 0.693 (R_A + R_B)C Output High

t2 =0.693 R_BC Output Low

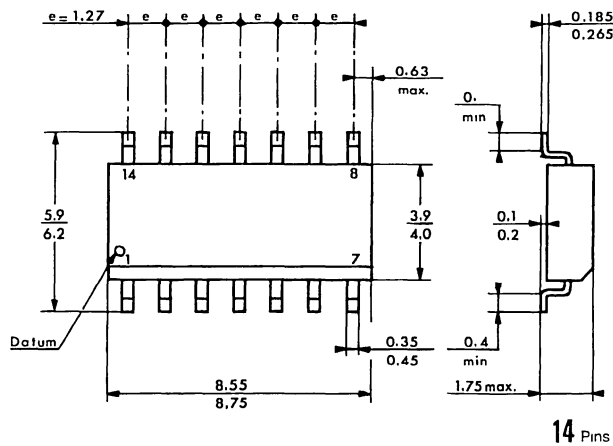


PACKAGE MECHANICAL DATA

14 PINS – PLASTIC DIP OR CERDIP



14 PINS – PLASTIC MICROPACKAGE (SO)

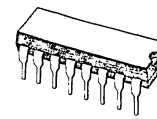


REGULATING PULSE WIDTH MODULATORS

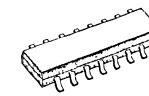
- COMPLETE PWM POWER CONTROL CIRCUITRY
- UNCOMMITTED OUTPUTS FOR SINGLE-ENDED OR PUSH PULL APPLICATIONS
- LOW STANDBY CURRENT .. 8 mA TYPICAL
- OPERATION UP TO 300 KHz
- 1 % MAXIMUM TEMPERATURE VARIATION OF REFERENCE VOLTAGE

DESCRIPTION

The SG1524 , SG2524, and SG3524 incorporate on a single monolithic chip all the function required for the construction of regulating power supplies inverters or switching regulators. They can also be used as the control element for high power-output applications. The SG1524 family was designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allows either single-ended or push-pull applications. Each device includes an on-ship reference, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shut-down circuitry.



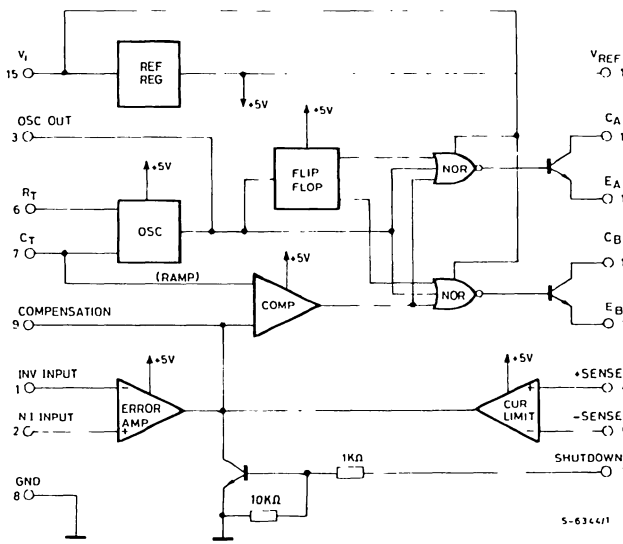
DIP-16
(Plastic –0.25– and Ceramic)



SO16 J

ORDER CODES : SG1524J – SG2524J – SG3524J (Ceramic)
SG2524N – SG3524N (Plastic)
SG2524P – SG3524P (SO–16J)

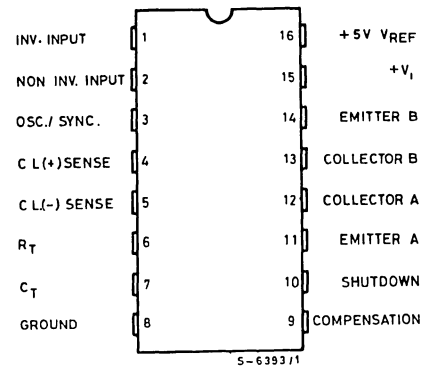
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	Supply Voltage	40	V
I_C	Collector Ouptut Current	100	mA
I_R	Reference Output Current	50	mA
I_T	Current Through C_T Terminal	– 5	mA
P_{tot}	Total Power Dissipation at Tamb = 70 °C	1000	mW
T_{stg}	Storage Temperature Range	– 65 to 150	°C
T_{op}	Operating Ambient Temperature Range **SG1524** **SG2524** **SG3524**	– 55 to 125 – 25 to 85 0 to 70	°C °C °C

CONNECTION DIAGRAMS



THERMAL DATA

			Plastic DIP-16	Ceramic DIP-16	SO16J
$R_{th\ j\text{-}amb}$	Themal Resistance Junction-ambient	Max	80 °C/W	150 °C/W	–
$R_{th\ j\text{-}alumina}$	Themal Resistance Junction-aluminia	Max	–	–	50 °C/W

* Thermal resistance junction–alumina with the device soldered on the middle of an alumina supporting substrate measuring 15 x 20 mm; 0.65 mm thickness with infinite heatsink

ELECTRICAL CHARACTERISTICS (unless otherwise stated , these specifications apply for T_j = – 55 °C to+ 125 °C for the SG1524, – 25 °C to + 85 °C for the SG2524, and 0 °C to + 70 °C for the SG3524, V_N = 20 V, and f = 20 KHz).

Symbol	Parameter	Test conditions	SG1524 SG2524			SG3524			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION									
V_{REF}	Output Voltage		4.8	5	5.2	4.6	5	5.4	V
ΔV_{REF}	Line Regulation	V_{IN} = 8 to 40 V		10	20		10	30	mV
ΔV_{REF}	Load Regulation	I_L = 0 to 20 mA		20	50		20	50	mV
	Ripple Rejection	f = 120 Hz, T_j = 25 °C		66			66		dB
	Short Circuit Current Limit	V_{REF} = 0, T_j = 25 °C		100			100		mA
$\Delta V_{REF}/\Delta T$	Temp. Stability	Over Operating Temp. Range		0.3	1		0.3	1	%
ΔV_{REF}	Long Term Stability	T_j = 125 °C, t = 1000 Hrs		20			20		mV
OSCILLATOR SECTION									
f_{MAX}	Maximum Frequency	C_T = 0.001 µF, R_T = 2 kΩ		300			300		kHz
	Initial Accuracy	R_T and C_T Constant		5			5		%
	Voltage Stability	V_{IN} = 8 to 40 V, T_j = 25 °C			1			1	%
$\Delta f/\Delta T$	Temperature Stability	Over Operating Temp. Range			2			2	%
	Output Amplitude	Pin 3, T_j = 25 °C		3.5			3.5		V
	Output Pulse Width	C_T = 0.01 µF, T_j = 25 °C		0.5			0..5		µs
ERROR AMPLIFIER SECTION									
V_{OS}	Input Offset Voltage	V_{CM} = 2.5 V		0.5	5		2	10	mV
I_b	Input Bias Current	V_{CM} = 2.5 V		2	10		2	10	µA
G_V	Open Loop Volt. Gain		72	80		60	80		dB
CMV	Common Mode Volt.	T_j = 25 °C	1.8		3.4	1.8		3.4	V
CMR	Comm. Mode Rejec.	T_j = 25 °C		70			70		dB
B	Small Signal Bandwidth	A_v = 0 dB, T_j = 25 °C		3			3		MHz
V_O	Output Voltage	T_j = 25 °C	0.5		3.8	0.5		3.8	V
COMPARATOR SECTION									
	Duty-cycle	% Each Output On	0		45	0		45	%
V_{IT}	Input Threshold	Zero Duty-cycle		1			1		V
V_{IT}	Input Threshold	Maximum Duty-cycle		3.5			3.5		V
I_b	Input Bias Current			1			1		µA

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test conditions	SG1524 SG2524			SG3524			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
CURRENT LIMITING SECTION									
	Sense Voltage	Pin 9 = 2 V With Error Amplifier Set for Max. Out, Tj = 25 °C	190	200	210	180	200	220	mV
	Sense Voltage T.C.			0.2			0.2		mV/°C
CMV	Common Mode Volt.		− 1		+ 1	− 1		+ 1	
OUTPUT SECTION (each output)									
	Collector-emitter Volt.		40			40			V
	Collector Leackage Cur.	V_{CE} = 40 V		0.1	50		0.1	50	µA
	Saturation Voltage	I_c = 50 mA		1	2		1	2	V
	Emitter Out. Voltage	V_{IN} = 20 V	17	18		17	18		V
t_r	Rise Time	R_c = 2 KΩ, T_j = 25 °C		0.2			0.2		µs
t_f	Fall Time	R_c = 2 KΩ, T_j = 25 °C		0.1			0.1		µs
I_q*	Total Standby Curr.	V_{IN} = 40 V		8	10		8	10	mA

(*) Excluding oscillator charging current, error and current limit dividers, and with outputs open.

Figure 1 : Open-loop Voltage Amplification of Error Amplifier vs. Frequency.

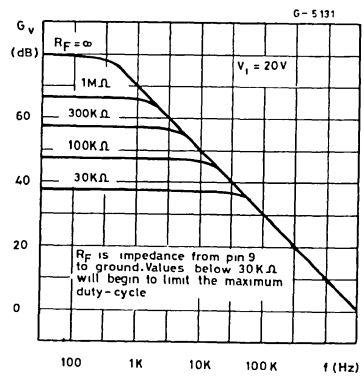


Figure 2 : Oscillator Frequency vs. Timing Components.

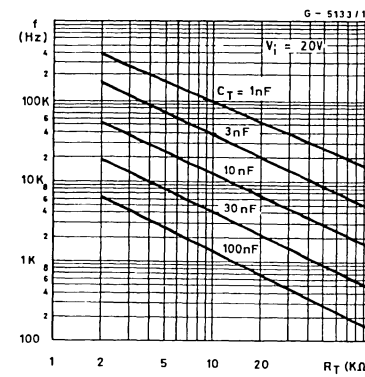


Figure 3 : Output Dead Time vs. Timing Capacitance Value.

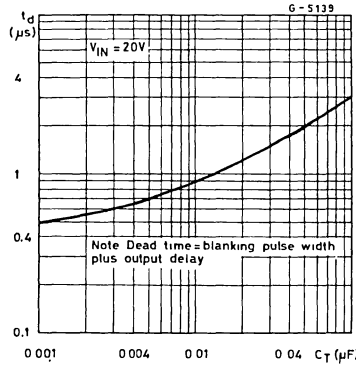


Figure 4 : Output Saturation Voltage vs. Load Current .

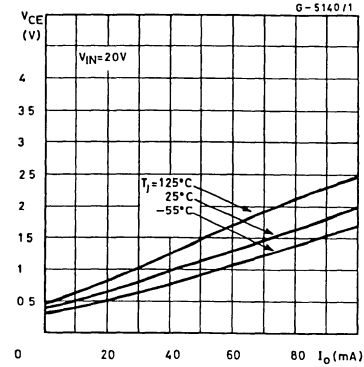
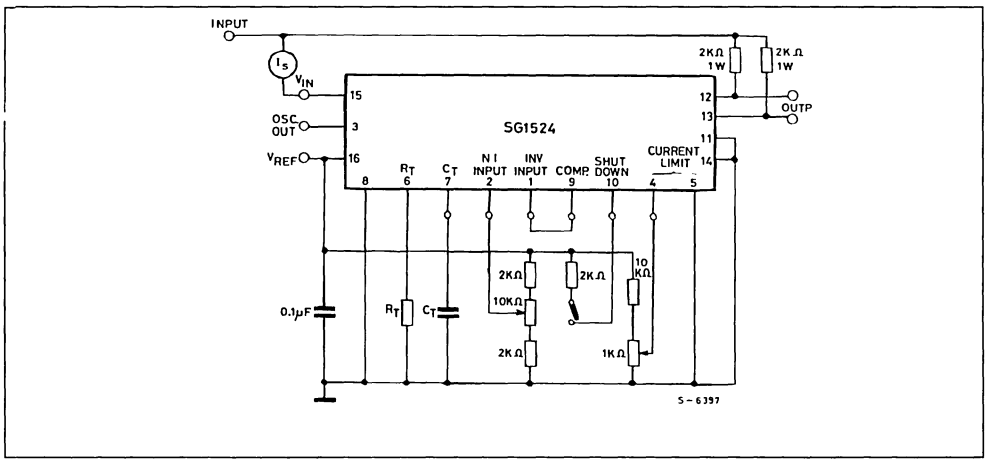


Figure 5 : Open Loop Test Circuit.



PRINCIPLES OF OPERATION

The SG1524 is a fixed-frequency pulse-with-modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor (R_T) and one timing capacitor (C_T). R_T established a constant charging current for C_T. This results in a linear voltage ramp at CT, which is fed to the comparator providing linear control of the output pulse width by the error amplifier. The SG1524 contains, an on-board 5 V regulator that serves as a reference as well as powering the SG1524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generale a feedback signal to error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at C_T. The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistors (Q_A or Q_B) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both output are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the value of C_T. The outputs

may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current limiting and shutdown circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier, or to provide additional control to the regulator.

RECOMMENDED OPERATING CONDITIONS

Supply voltage V_{IN}	8 to 40	V	Timing Resistor, R_T	1.8 to 100	KΩ
Reference Output Current	0 to 20	mA	Timing Capacitor, C_T	0.001 to 0.1	µF
Current through C_T Terminal	- 0.03 to - 2	mA			

TYPICAL APPLICATIONS DATA

OSCILLATOR

The oscillator controls the frequency of the SG1524 and is programmed by R_T and C_T according to the approximate formula :

$$f \approx \frac{1.18}{R_T C_T}$$

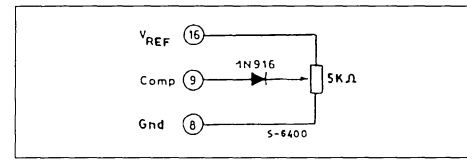
where R_T is in KΩ
C_T is in µF
f is in KHz

Pratical values of C_T fall between 0.001 and 0.1 µF. Pratical values of R_T fall between 1.8 and 100 KΩ. This results in a frequency range typically from 120 Hz to 500 KHz.

BLANKING

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse width is controlled by the value of C_T. If small values of C_T are required for frequency control, the oscillator output pulse width may still be increased by applying a shunt capacitance of up to 100 pF from pin 3 to ground. If still greater dead-time is required, it should be accomplished by limiting the maximum duty cycle by clamping the output of the error amplifier. This can easily be done with the circuit below :

Figure 6.



SYNCHRONOUS OPERATION

When an external clock is desired, a clock pulse of approximately 3 V can be applied directly to the oscillator ouptut terminal. The impedance to ground at this point is approximately 2 KΩ. In this configuration R_T C_T must be selected for a clock period slightly greater than that the external clock.

If two more SG1524 regulators are to be operated synchronously, all oscillator output terminals should be tied together, all C_T terminals connected to a single timing capacitor, and the timing resistor connected to a single R_T terminal. The other R_T terminals can be left open or shorted to V_{REF}. Minimum lead lengths should be used between the C_T terminals.

Figure 7: Flyback Converter Circuit.

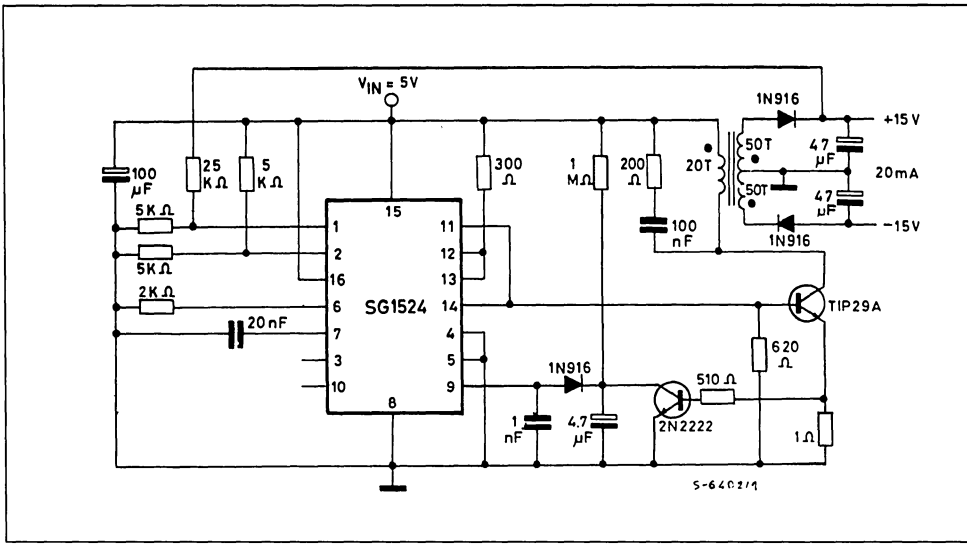
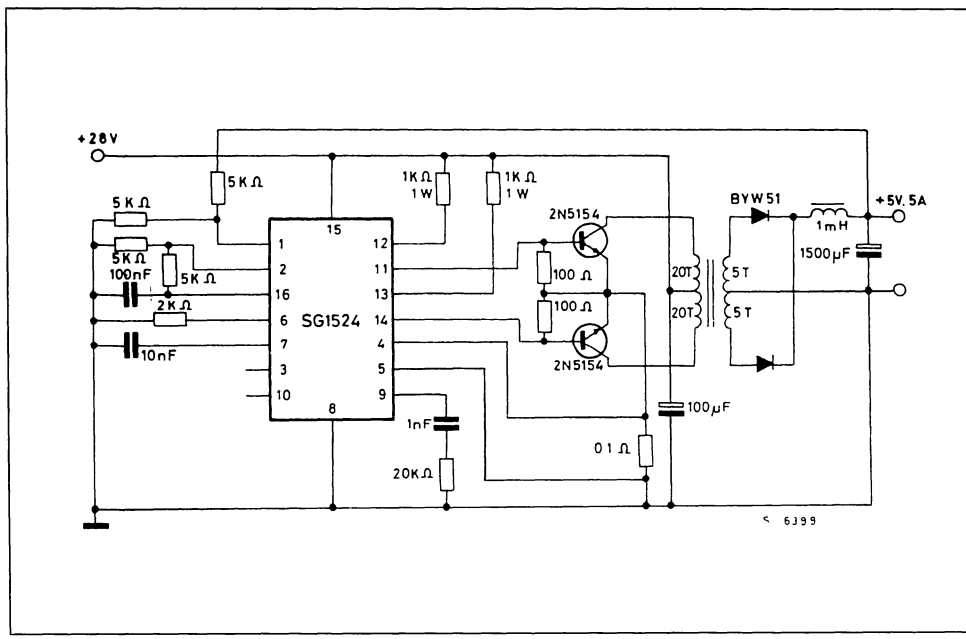


Figure 8: PUSH-PULL transformer-coupled circuit.



SGS-THOMSON MICROELECTRONICS

SG1525A/27A
SG2525A-3525A/27A

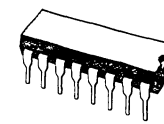
REGULATING PULSE WIDTH MODULATORS

- 8 TO 35 V OPERATION
- 5.1 V REFERENCE TRIMMED TO ± 1 %
- 100 Hz TO 500 KHz OSCILLATOR RANGE
- SEPARATE OSCILLATOR SYNC TERMINAL
- ADJUSTABLE DEADTIME CONTROL
- INTERNAL SOFT-START
- PULSE-BY-PULSE SHUTDOWN
- INPUT UNDERVOLTAGE LOCKOUT WITH HYSTERESIS
- LATCHING PWM TO PREVENT MULTIPLE PULSES
- DUAL SOURCE/SINK OUTPUT DRIVERS

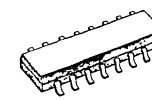
DESCRIPTION

The SG1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip + 5.1 V reference is trimmed to ± 1 % and the input common-mode range of the error amplifier includes the reference voltage eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the C_T and the discharge terminals provide a wide range of dead time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. This lockout circuitry includes approximately 500 mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulses has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200 mA. The SG1525A output stage features NOR logic, giving a LOW output for an OFF state. The SG1527A utilizes OR logic which results in a HIGH output level when OFF.

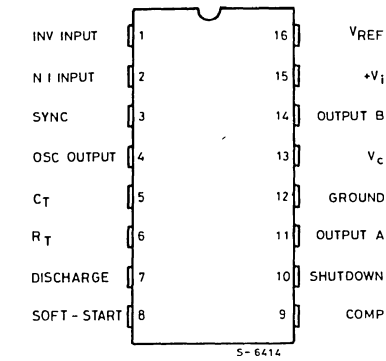
DIP-16
(Plastic -0.25 and Ceramic)



SO16J



CONNECTION DIAGRAM AND ORDERING NUMBERS (top view)



Type	Plastic DIP	Ceramic DIP	SO16J
SG1525A	–	SG1525AJ	–
SG1527A	–	SG1527AJ	–
SG2525A	SG2525AN	SG2525AJ	SG2525AP
SG2527A	SG2527AN	SG2527AJ	SG2527AP
SG3525A	SG3525AN	SG3525AJ	SG3525AP
SG3527A	SG3527AN	SG3527AJ	SG3527AP

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	Supply Voltage	40	V
V_C	Collector Supply Voltage	40	V
I_{OSC}	Oscillator Charging Current	5	mA
I_o	Output Current, Source or Sink	500	mA
I_R	Reference Output Current	50	mA
I_T	Current through C_T Terminal Logic Inputs Analog Inputs	5 – 0.3 to + 5.5 – 0.3 to V_i	mA V V
P_{tot}	Total Power Dissipation at T_{amb} = 70 °C	1000	mW
T_j	Junction Temperature Range	– 55 to 150	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C
T_{op}	Operating Ambient Temperature : **SG1525A/27A** **SG2525A/27A** **SG3525A/27A**	– 55 to 125 – 25 to 85 0 to 70	°C °C °C

THERMAL DATA (DIP-16)

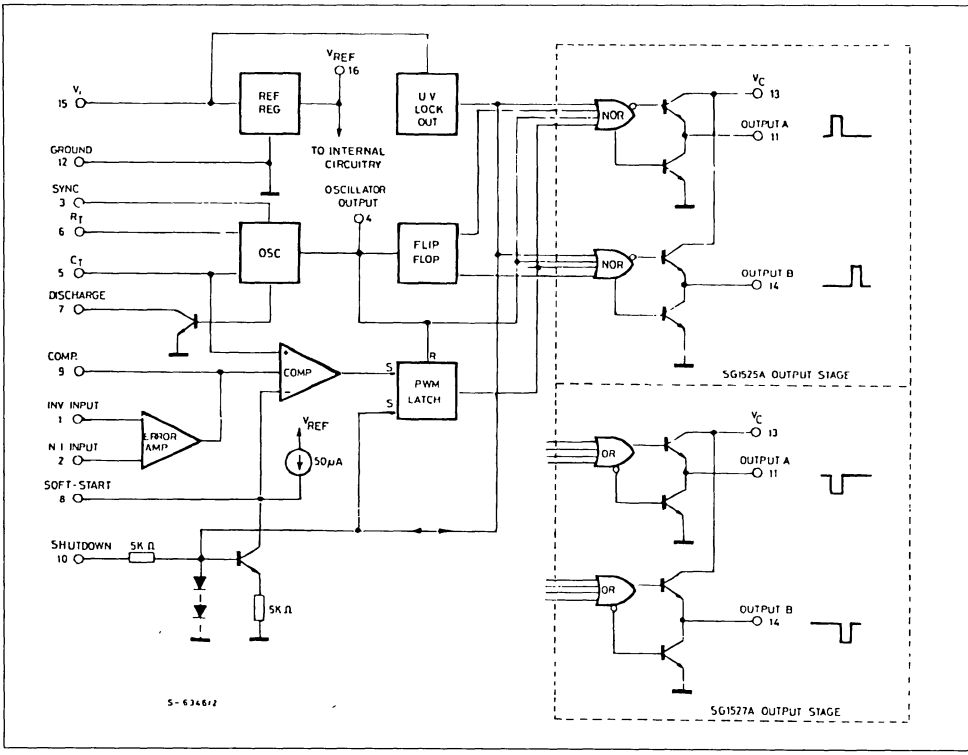
			Ceramic	Plastic
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	–	50 °C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	150 °C/W	80 °C/W

THERMAL DATA (SO16J)

$R_{th\ j\text{-}alumina}$*	Thermal Resistance Junction-alumina	Max	50	°C/W

* Thermal resistance junction-alumina with the device soldered on the middle of an alumina supporting substrate measuring 15 × 20 mm ; 0 65 mm thickness with infinite heatsink

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

(V_i = 20 V, and over operating temperature, unless otherwise specified)

Symbol	Parameter	Test Conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION									
V_{REF}	Output Voltage	T_J = 25 °C	5.05	5.1	5.15	5	5.1	5.2	V
ΔV_{REF}	Line Regulation	V_i = 8 to 35 V		10	20		10	20	mV
ΔV_{REF}	Load Regulation	I_L = 0 to 20 mA		20	50		20	50	mV
$\Delta V_{REF}/\Delta T$*	Temp. Stability	Over Operating Range		20	50		20	50	mV
*	Total Output Variation	Line, Load and Temperature	5		5.2	4.95		5.25	V
	Short Circuit Current	V_{REF} = 0 T_J = 25 °C		80	100		80	100	mA
*	Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz, T_J = 25 °C		40	200		40	200	µVrms
ΔV_{REF}*	Long Term Stability	T_J = 125 °C, 1000 hrs		20	50		20	50	mV

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
OSCILLATOR SECTION**									
*, •	Initial Accuracy	T_j = 25 °C		± 2	± 6		± 2	± 6	%
*, •	Voltage Stability	V_i = 8 to 35 V		± 0.3	± 1		± 1	± 2	%
$\Delta f/\Delta T$*	Temperature Stability	Over Operating Range		± 3	± 6		± 3	± 6	%
f_{MIN}	Minimum Frequency	R_T = 200 KΩ C_T = 0.1 µF			120			120	Hz
f_{MAX}	Maximum Frequency	R_T = 2 KΩ C_T = 470 pF	400			400			KHz
	Current Mirror	I_{RT} = 2 mA	1.7	2	2.2	1.7	2	2.2	mA
*, •	Clock Amplitude		3	3.5		3	3.5		V
*, •	Clock Width	T_j = 25 °C	0.3	0.5	1	0.3	0.5	1	µs
	Sync Threshold		1.2	2	2.8	1.2	2	2.8	V
	Sync Input Current	Sync Voltage = 3.5 V		1	2.5		1	2.5	mA
ERROR AMPLIFIER SECTION (V_{CM} = 5.1 V)									
V_{OS}	Input Offset Voltage			0.5	5		2	10	mV
I_b	Input Bias Current			1	10		1	10	µA
I_{os}	Input Offset Current				1			1	µA
	DC Open Loop Gain	$R_L \geq 10$ MΩ	60	75		60	75		dB
*	Gain Bandwidth Product	G_v = 0 dB T_j = 25 °C	1	2		1	2		MHz
*, z	DC Transconduct.	30 KΩ ≤ R_L ≤ 1 MΩ T_j = 25 °C	1.1	1.5		1.1	1.5		ms
	Output Low Level			0.2	0.5		0.2	0.5	V
	Output High Level		3.8	5.6		3.8	5.6		V
CMR	Comm. Mode Reject.	V_{CM} = 1.5 to 5.2 V	60	75		60	75		dB
PSR	Supply Voltage Rejection	V_i = 8 to 35 V	50	60		50	60		dB
PWM COMPARATOR									
	Minimum Duty-cycle				0			0	%
	Maximum Duty-cycle		45	49		45	49		%
•	Input Threshold	Zero Duty-cycle	0.7	0.9		0.7	0.9		V
		Maximum Duty-cycle		3.3	3.6		3.3	3.6	V
*	Input Bias Current			0.05	1		0.05	1	µA

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
SHUTDOWN SECTION									
	Soft Start Current	V_{SD} = 0 V, V_{SS} = 0 V	25	50	80	25	50	80	µA
	Soft Start Low Level	V_{SD} = 2.5 V		0.4	0.7		0.4	0.7	V
	Shutdown Threshold	To outputs, V_{SS} = 5.1 V T_J = 25 °C	0.6	0.8	1	0.6	0.8	1	V
	Shutdown Input Current	V_{SD} = 2.5 V		0.4	1		0.4	1	mA
*	Shutdown Delay	V_{SD} = 2.5 V T_J = 25 °C		0.2	0.5		0.2	0.5	µs
OUTPUT DRIVERS (each output) (V_C = 20 V)									
	Output Low Level	I_{sink} = 20 mA		0.2	0.4		0.2	0.4	V
		I_{sink} = 100 mA		1	2		1	2	V
	Output High Level	I_{source} = 20 mA	18	19		18	19		V
		I_{source} = 100 mA	17	18		17	18		V
	Under-Voltage Lockout	V_{comp} and V_{ss} = High	6	7	8	6	7	8	V
I_C	Collector Leakage	V_C = 35 V			200			200	µA
t_r*	Rise Time	C_L = 1 nF, T_J = 25 °C		100	600		100	600	ns
t_f*	Fall Time	C_L = 1 nF, T_J = 25 °C		50	300		50	300	ns
TOTAL STANDBY CURRENT									
I_s	Supply Current	V_I = 35 V		14	20		14	20	mA

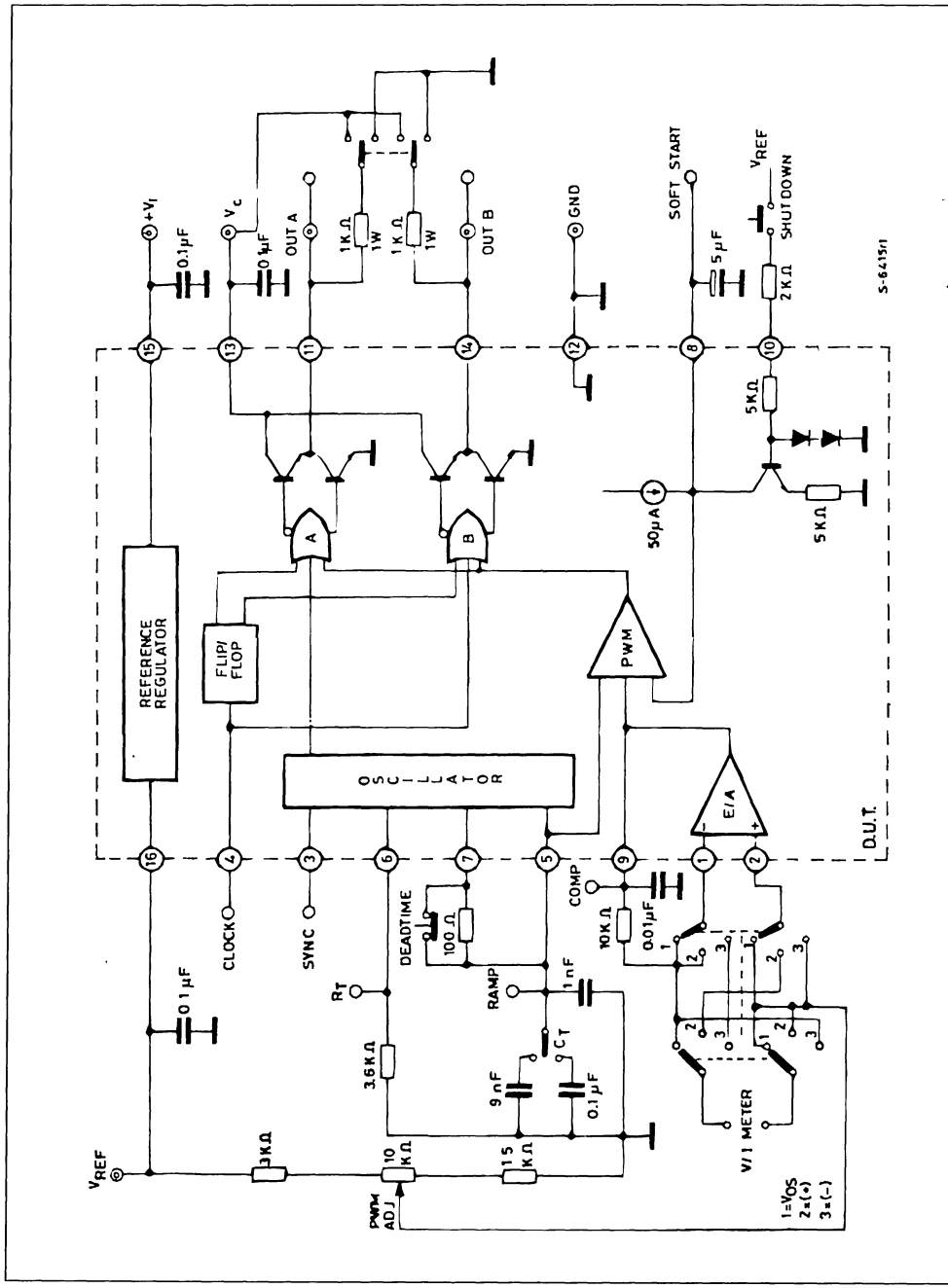
* These parameters, although guaranteed over the recommended operating conditions, are not 100 % tested in production.

Tested at f_{osc} = 40 KHz (R_T = 3.6 KΩ, C_T = 0.1 µF, R_D = 0 Ω). Approximate oscillator frequency is defined by .

$$f = \frac{1}{C_T(0.7\ R_T + 3\ R_D)}$$

■ DC transconductance (g_M) relates to DC open-loop voltage gain (G_V) according to the following equation : $G_V = g_M R_L$ where R_L is the resistance from pin 9 to ground. The minimum g_M specification is used to calculate minimum G_V when the error amplifier output is loaded

TEST CIRCUIT



RECOMMENDED OPERATING CONDITIONS (•)

Parameter	Value
Input Voltage (V_i)	8 to 35 V
Collector Supply Voltage (V_C)	4.5 to 35 V
Sink/Source Load Current (steady state)	0 to 100 mA
Sink/Source Load Current (peak)	0 to 400 mA
Reference Load Current	0 to 20 mA
Oscillator Frequency Range	100 Hz to 400 KHz
Oscillator Timing Resistor	2 KΩ to 150 KΩ
Oscillator Timing Capacitor	0.001 µF to 0.1 µF
Dead Time Resistor Range	0 to 500 Ω

(•) Range over which the device is functional and parameter limits are guaranteed.

Figure 1 : Oscillator Charge Time vs. R_T and C_T.

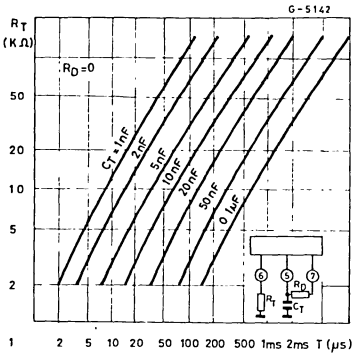


Figure 2 : Oscillator Discharge Time vs. R_D and C_T.

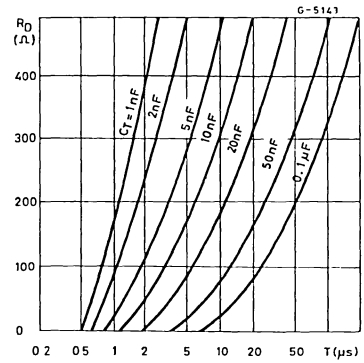


Figure 3 : SG1525A Output Saturation Characteristics.

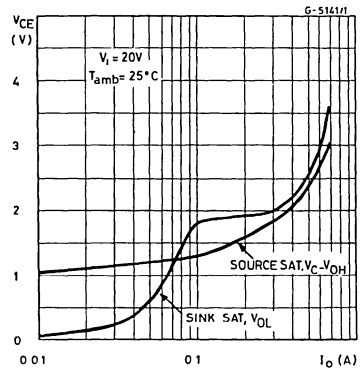


Figure 4 : Error Amplifier Voltage Gain and Phase vs. Frequency.

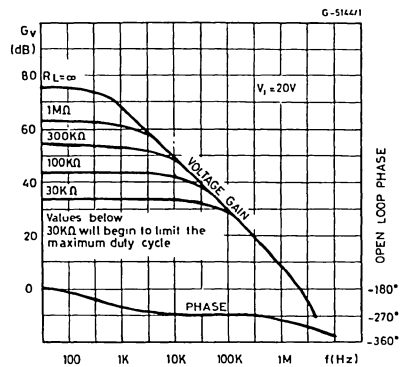
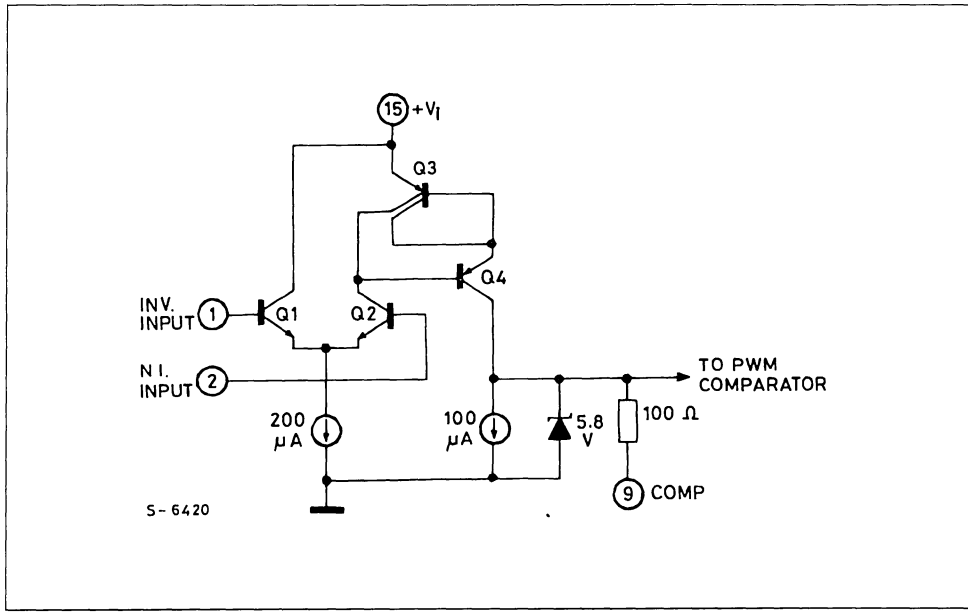


Figure 5 : SG1525A Error Amplifier.



PRINCIPLES OF OPERATION

SHUTDOWN OPTIONS (see Block Diagram)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100 µA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions : the PWM latch is immediately set providing the fastest turn-off signal to the outputs ; and a 150 µA current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

Figure 6 : SG1525A Oscillator Schematic.

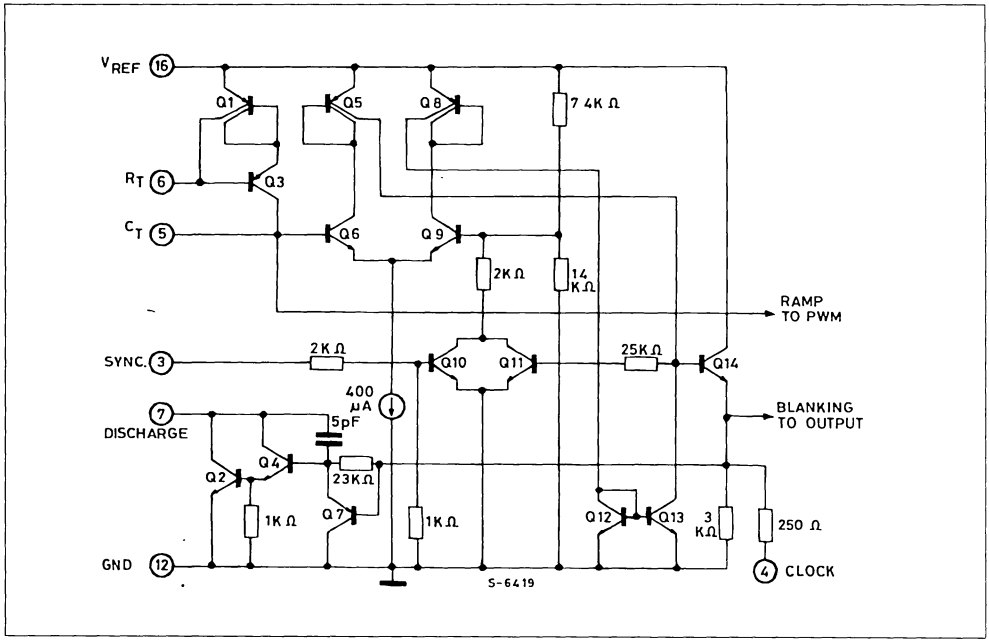


Figure 7 : SG1525A Output Circuit (1/2 circuit shown).

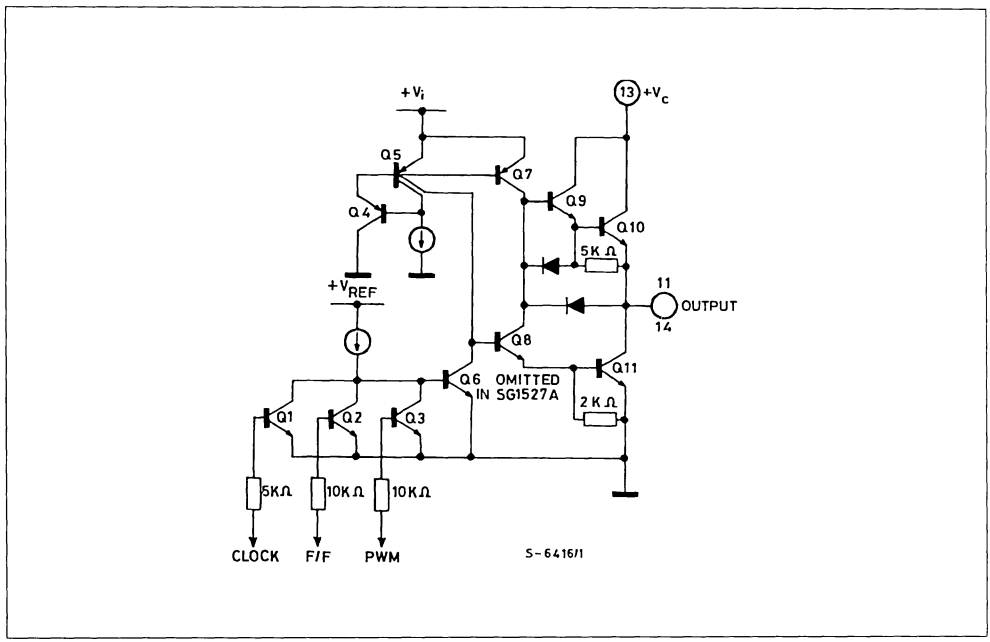
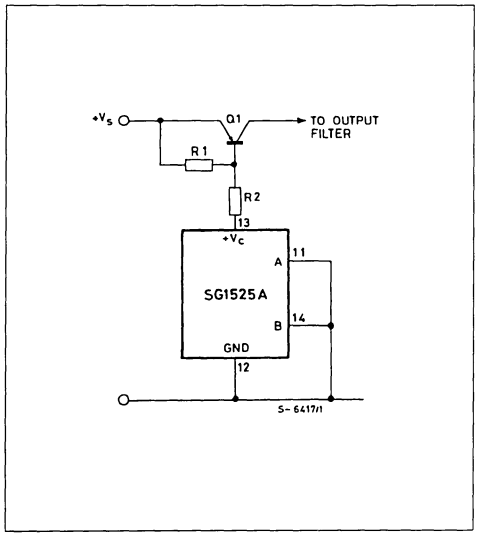
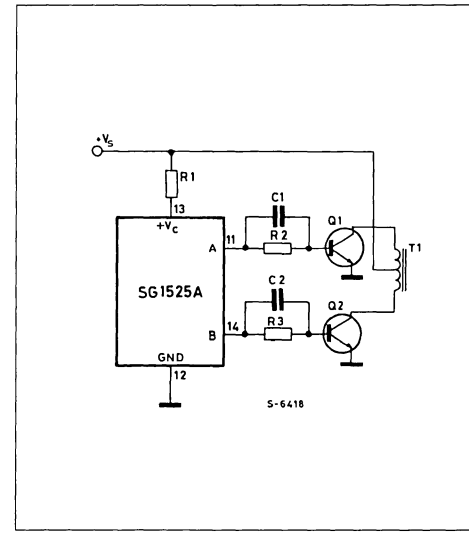


Figure 8.



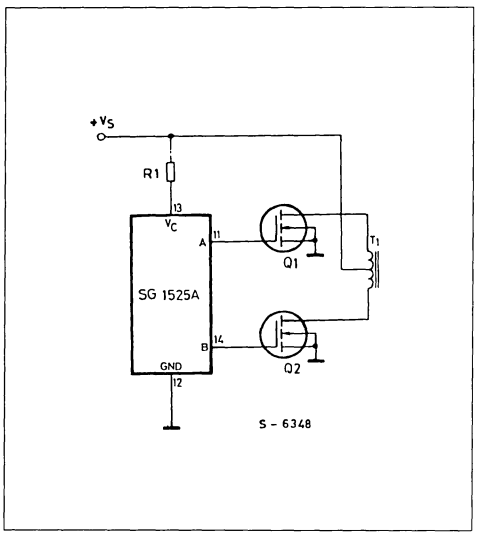
For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

Figure 9.



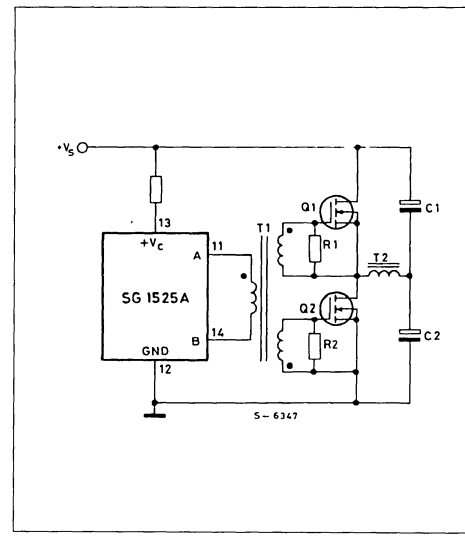
In conventional push-pull bipolar designs, forward base drive is controlled by R_1 - R_3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C_1 and C_2.

Figure 10.



The low source impedance of the output drivers provides rapid charging of Power Mos input capacitance while minimizing external components.

Figure 11.



Low power transformers can be driven directly by the SG1525A. Automatic reset occurs during dead time, when both ends of the primary winding are switched to ground.

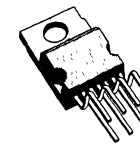
SGS-THOMSON MICROELECTRONICS

TDA8133

5.1V + 8.5V REGULATOR WITH DISABLE AND RESET

ADVANCE DATA

- OUTPUT CURRENTS UP TO 1A
- FIXED PRECISION OUTPUT 1 VOLTAGE 5.1V ± 2%
- FIXED PRECISION OUTPUT 2 VOLTAGE 8.5V ± 2%
- OUTPUT 1 WITH RESET FACILITY
- OUTPUT 2 WITH DISABLE BY TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUTPUT VOLTAGE



HEPTAWATT

ORDER CODE : TDA8133

DESCRIPTION

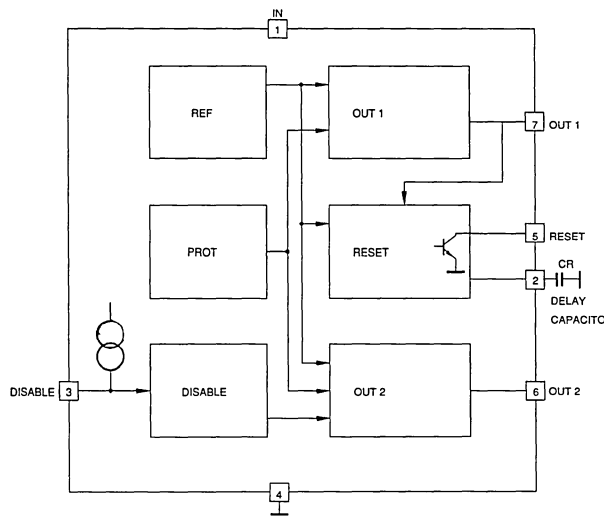
The TDA8133 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages of 5.1V and 8.5V at currents up to 1A.

An internal reset circuit generates a delayed reset pulse when the output 1 decreases below the regulated voltage value.

Output 2 can be disabled by TTL input.

Short circuit and thermal protections are included.

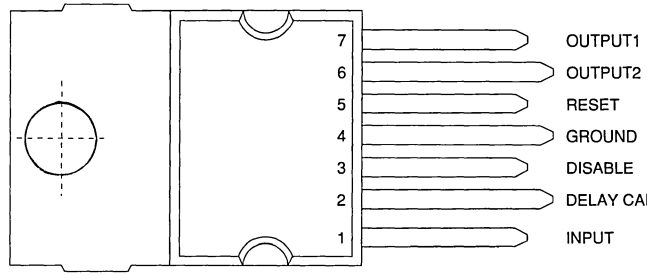
BLOCK DIAGRAM



E89TDA8133-01

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTION (top view)



Tab connected to pin 4.

E89TDA8133-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	DC Input Voltage Pin 1	20	V
V_{DIS}	Disable Input Voltage Pin 3	20	V
V_{RST}	Output Voltage at pin 5	20	V
$I_{O1,2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	– 65 to + 150	°C
T_J	Junction Temperature	0 to + 150	°C

THERMAL DATA

$R_{TH(j-c)}$	Maximum Thermal Resistance Junction-case	3	°C/W

ELECTRICAL CHARACTERISTICS (V_{IN} = 7V ; T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{01}	Output Voltage	I_{01} = 10mA	5	5.1	5.2	V
V_{02}	Output Voltage	I_{02} = 10mA	8.33	8.5	8.67	V
V_{01}	Output Voltage	7V < V_{IN1} < 14V 10.5V < V_{IN2} < 18V 5mA < $I_{01,2}$ < 750mA	4.9		5.3	V
V_{02}	Output Voltage		8.15		8.85	V
$V_{I01,2}$	Dropout Voltage	$I_{01,2}$ = 750mA			1.4	V
		$I_{01,2}$ = 1A			2	V
V_{01LI}	Line Regulation	7V < V_{IN1} < 14V 10.5V < V_{IN2} < 18V $I_{01,2}$ = 200mA			50	mV
V_{02LI}	Line Regulation				85	mV
V_{01LO}	Load Regulation	5mA < $I_{01,2}$ < 0.6A			100	mV
V_{01LO}	Load Regulation				170	mV
I_Q	Quiescent Current	I_{01} = 10mA Output 2 Disabled			2	mA
V_{01RST}	Reset Threshold Voltage	(K = V_{01})	K – 0.4	K – .25	K – 0.1	V
V_{RTH}	Reset Threshold Hysteresis	(see note 1)	20	50	75	mV
t_{RD}	Reset Pulse Delay at pin 5	C_e = 100nF (see note 1)		25		ms
V_{RL}	Saturation Volt. at pin 5 in Reset Condition	I_5 = 5mA			0.4	V
I_{RH}	Leakage Current at pin 5 in Normal Condition	V_5 = 10V			10	µA
$V_{01,2}/T$	Output Voltage Thermal Drift			100		ppm/°C
$I_{01,2SC}$	Short Circ. Output Current	V_{IN1} = 7V ; V_{IN2} = 10.5V			1.6	A
		$V_{IN1,2}$ = 18V (see note 2)			0.7	A
V_{DISH}	Disable Volt. at Pin 3 High (out 2 active)		2			V
V_{DISL}	Disable Volt. at Pin 3 Low (out 2 disabled)				0.8	V
I_{DIS}	Disable bias Current at Pin 3	0V < V_{DIS} < 7V	– 100		2	µA
T_{jsd}	Junction Temp. for Thermal Shut Down			145		°C

Notes : 1. If the output voltage OUT 1 goes below 4.85V (VOUT – 0.25V) the comparator "a" (see fig. 1) discharges rapidly the capacitor Ce and the Reset output (pin 5) goes at once LOW.
When the voltage at the OUT 1 rises above 4.9V, the voltage at pin 2 increases with this law :

$$t_d = \frac{Ce \cdot 2.5V}{10\mu A} \quad \text{(see fig. 2)}$$

as V2 reach 2.5V the Reset output (pin 5) goes HIGH again To avoid glitches in the Reset output the second comparator "b" has a large hysteresis (1.9V).

2. The output short circuit currents are tested one channel at time
During a short circuit a large consomption of power occurs, anyway the thermal protection circuit guarantees the temperature not overcomes high value.

Figure 1.

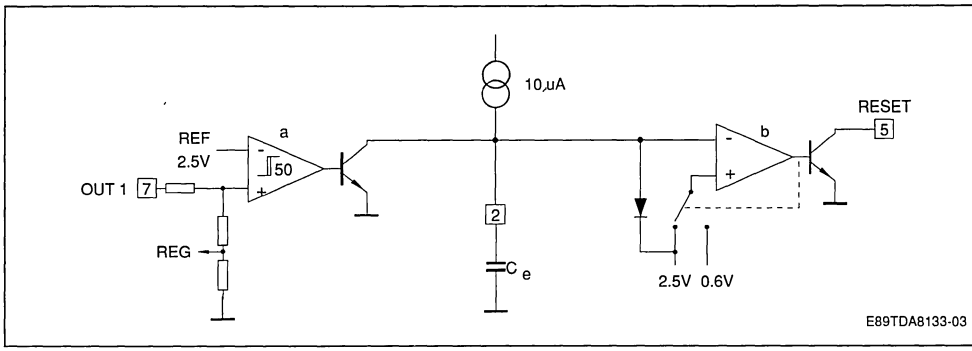
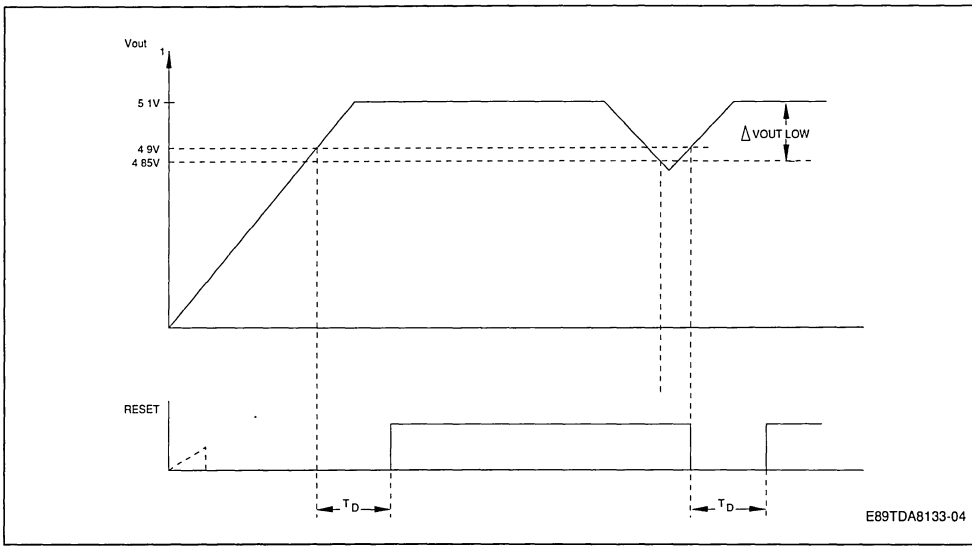


Figure 2.



CIRCUIT DESCRIPTION

The TDA8133 is a dual voltage regulator with Reset and Disable.

The two regulation parts are supplied from one voltage reference circuit trimmed by zener zap during EWS test.

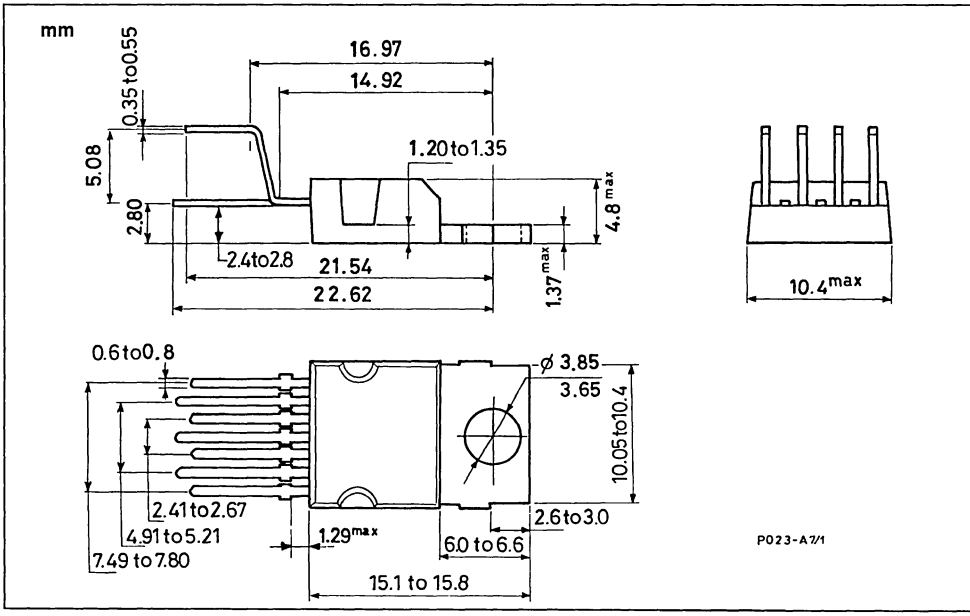
The outputs stage have been realized in darlington configuration with a drop typical 1.2V.

The disable circuit, switch-off the output 2 if a voltage lower than 0.8V is applied at pin 3.

The Reset circuit controls the voltage at the output 1, if this one decrease below 4.85V provides to generate a reset pulse at pin 5 (open collector) with a certain delay depending by an external capacitor connected at pin 2.

PACKAGE MACHANICAL DATA

HEPTAWATT – PLASTIC PACKAGE



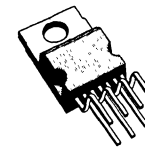
SGS-THOMSON MICROELECTRONICS

TDA8134

5V + 12V REGULATOR WITH DISABLE

ADVANCE DATA

- OUTPUT CURRENTS UP TO 600mA
- FIXED PRECISION OUTPUT 1 VOLTAGE 5V ± 2%
- FIXED PRECISION OUTPUT 2 VOLTAGE 12V ± 2%
- OUTPUT 2 VOLTAGE DISABLED BY A TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUT 1.5V AT 400mA
- HIGH SUPPLY VOLTAGE REJECTION



HEPTAWATT

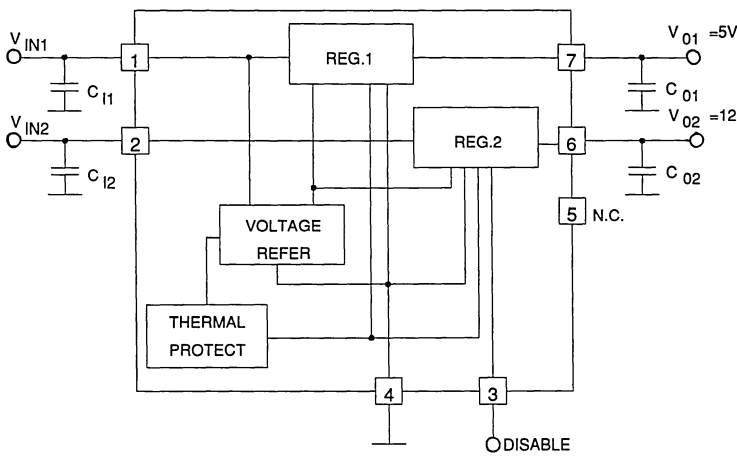
ORDER CODE : TDA8134

DESCRIPTION

The TDA8134 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages, 5V + 12V at currents up to 600mA.

Output 2 can be disabled by a TTL input. Both output currents are limited by an internal short circuit protection.

BLOCK DIAGRAM



E89TDA8134-01

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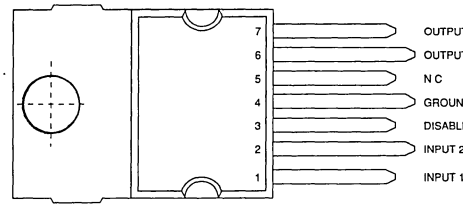
PIN CONNECTION (top view)



E89TDA8134-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{IN1,2}$	DC Input Voltages	24	V
V_{DIS}	Disable Input Voltage Pin 3	24	V
$I_{O1,2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	– 65 to + 150	°C
T_j	Junction Temperature	0 to + 150	°C

THERMAL DATA

$R_{TH(j-c)}$	Maximum Thermal Resistance Junction-case	3	°C/W

ELECTRICAL CHARACTERISTICS (V_{IN1} = 7V ; V_{IN2} = 14V ; V_{DIS} = 2.5V ; $I_{O1,2}$ = 0 ; T_j = 25°C unless otherwise specified)

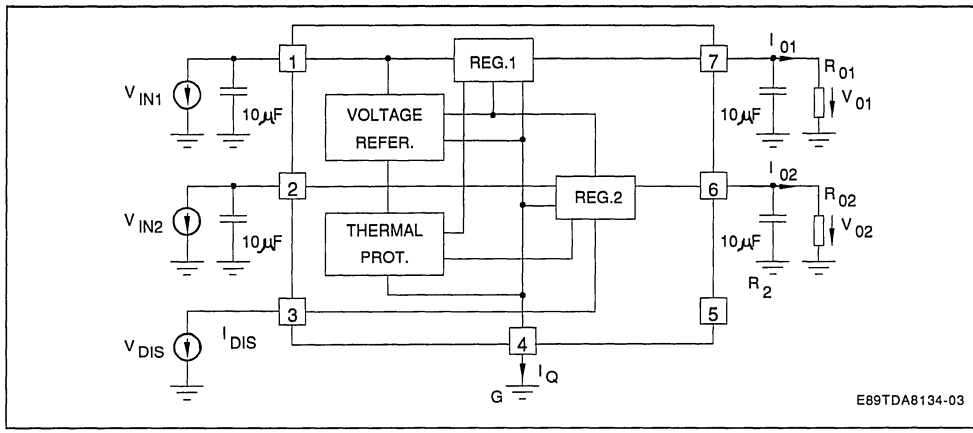
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{O1}	Output Voltage at Pin 7		4.9	5	5.1	V
V_{O2}	Output Voltage at Pin 6		11.76	12	12.24	V
I_{Q1}	Quiescent Current	V_{IN2} = 0 V_{DIS} = 0 I_{O1} = 10mA (see fig. 1)			2	mA
I_{Q2}	Quiescent Current	I_{O2} = 10mA (see fig. 1)			2	mA
V_{IN1}-V_{O1}	Drop Out Voltage 1	I_{O1} = 400mA			1.5	V
V_{IN2}-V_{O2}	Drop Out Voltage 2	I_{O2} = 400mA			1.5	V
ΔV_{O1LI}	Line Regulation 1	7V < V_{IN1} < 14V I_{O1} = 200mA			90	mV
ΔV_{O2LI}	Line Regulation 2	14V < V_{IN2} < 18V I_{O2} = 200mA			120	mV
ΔV_{O1LO}	Load Regulation 1	0 < I_{O1} < 600mA			100	mV
ΔV_{O2LO}	Load Regulation 2	0 < I_{O2} < 600mA			240	mV
I_{O1SC}	Short Circuit Current 1	14V < V_{IN1} < 18V			1.3	A
I_{O2SC}	Short Circuit Current 2	14V < V_{IN2} < 18V			1.3	A
V_{DISH}	Disable Voltage HIGH at Pin 3		2			V
V_{DISL}	Disable Voltage LOW at Pin 3				0.8	V
I_{DISH}	Bias Current at Pin 3	V_{DIS} = 5.3V			10	µA
I_{DISL}	Bias Current at Pin 3	V_{DIS} = 0.4V	– 80			µA
SVR_1	Supply Voltage Rejection 1 (see note 1)	V_{IN1} = 9V_{DC} + 1V_{PP} SIN f = 120Hz I_{O1} = 200mA	50			dB
SVR_2	Supply Voltage Rejection (see note 1)	V_{IN2} = 16V_{DC} + 1V_{PP} SIN f = 120Hz I_{O2} = 200mA	50			dB
I_Q	Quiescent Current	V_{IN1} = V_{IN2} = 14V_{DC} I_{O1} = I_{O2} = 200mA			6	mA
T_{JSD}	Thermal Shut-down Junction Temperature			145		°C

Note 1 : SVR supply voltage rejection :

$$20 \cdot \log \left| \frac{V_{IN\,ac}}{V_{O\,ac}} \right|$$

where :
- $V_{IN\,ac}$ is the value of the sinusoidal signal forced at the input. (120Hz, 1V_{PP})
- $V_{O\,ac}$ is the peak-peak ripple voltage present at the output

Figure 1 : Test Specification.



CIRCUIT DESCRIPTION

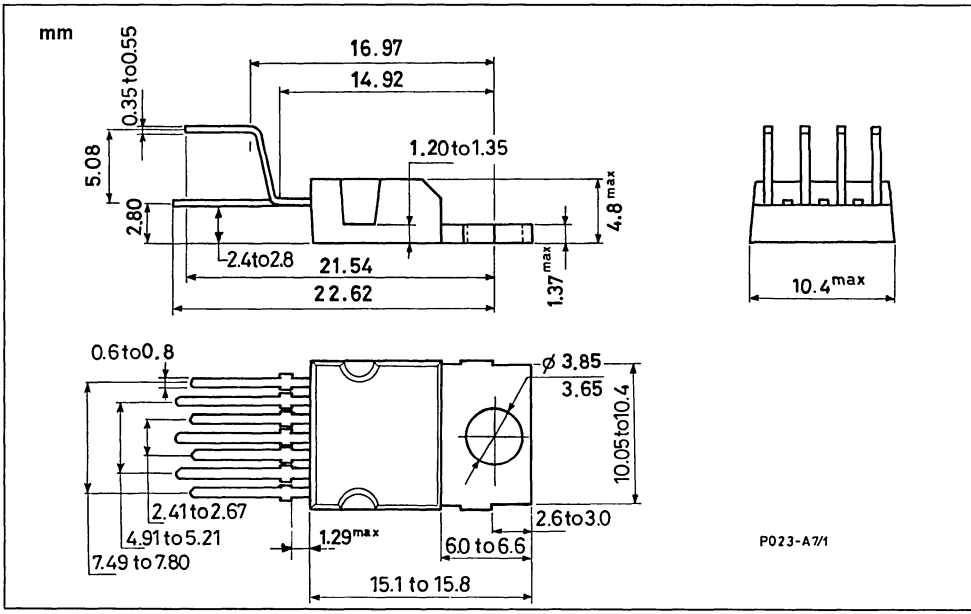
The TDA8134 is a dual voltage regulator with disable.

The two regulation parts are supplied from one voltage reference circuit, trimmed by zener zap during EWS test. Since the supply voltage of this last is connected at pin 1 (V_{IN1}), the regulator 2 will not work if the pin 1 is not supplied.

It is possible switch-off the output voltage 2 (V_{O2}) appling at pin 3 (disable input) a low TTL level.

PACKAGE MECHANICAL DATA

HEPTAWATT – PLASTIC PACKAGE



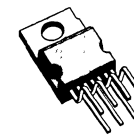
SGS-THOMSON MICROELECTRONICS

TDA8135

5V + ADJUSTABLE VOLTAGE REGULATOR WITH DISABLE

ADVANCE DATA

- OUTPUT CURRENTS UP TO 600mA
- FIXED PRECISION OUTPUT 1 VOLTAGE 5V ± 3%
- OUTPUT 2 - VOLTAGE PROGRAMMABLE FROM 5V TO 14V
- OUTPUT 2 VOLTAGE DISABLED BY A TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUT 1.5V AT 400mA
- HIGH SUPPLY VOLTAGE REJECTION



HEPTAWATT

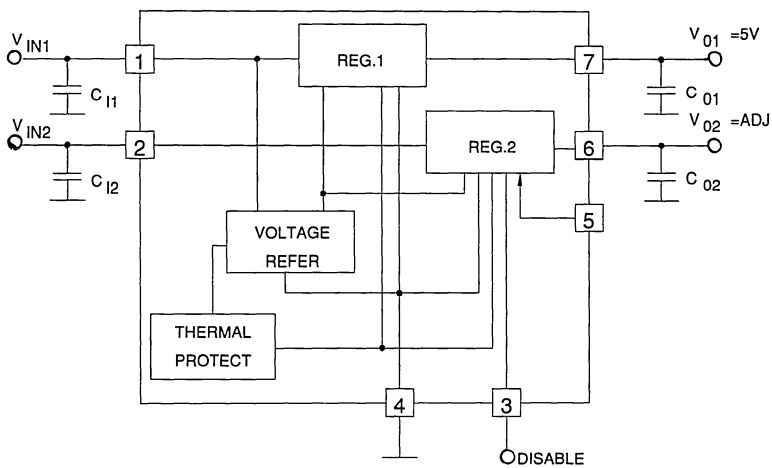
ORDER CODE : TDA8135

DESCRIPTION

The TDA8135 is a monolithic dual positive voltage regulator designed to provide precision output voltages, 5V + adjustable outputs at currents up to 600mA.

Output 2 can be disabled by a TTL input. Both output currents are limited by an internal short circuit protection.

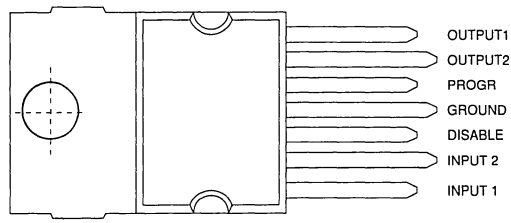
BLOCK DIAGRAM



E89TDA8135-01

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice

PIN CONNECTIONS



E89TDA8135-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{IN1,2}$	DC Input Voltages	24	V
V_{DIS}	Disable Input Voltage Pin 3	24	V
$I_{O1,2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	– 65 to + 150	°C
T_j	Junction Temperature	0 to + 150	°C

THERMAL DATA

$R_{TH(j-c)}$	Maximum Thermal Resistance Junction-case	3	°C/W

ELECTRICAL CHARACTERISTICS (V_{IN1} = 7V ; V_{IN2} = V_{O2} + 2V ; V_{DIS} = 2.5V ; $I_{O1,2}$ = 0 ; T_j = 25°C unless otherwise specified)

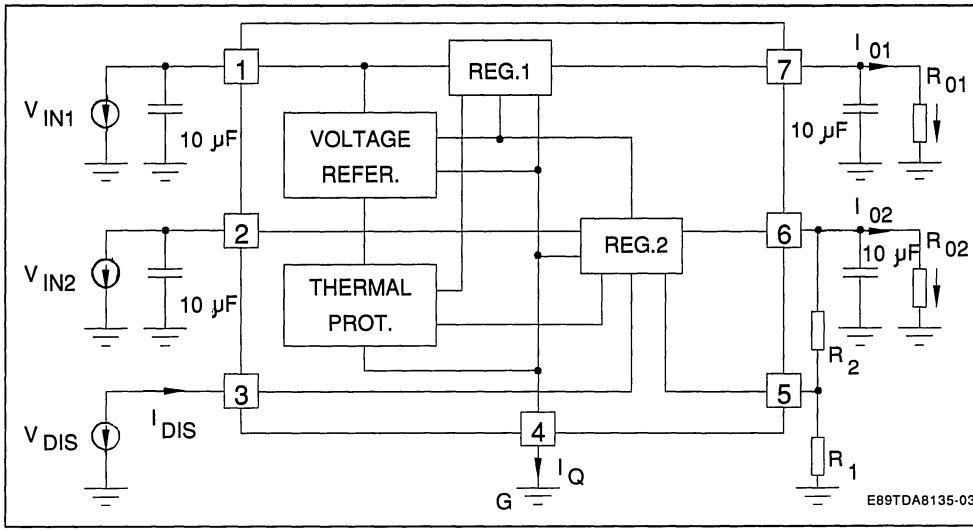
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{O1}	Output Voltage at Pin 7		4.85	5	5.15	V
V_{O2}	Output Voltage at Pin 6	Adjustable	5		14	V
I_{Q1}	Quiescent Current	V_{IN2} = 0 V_{DIS} = 0 I_{O1} = 10mA (see fig. 1)			2	mA
I_{Q2}	Quiescent Current	I_{O2} = 10mA (see fig. 1)			2	mA
V_{IN1}-V_{O1}	Drop Out Voltage 1	I_{O1} = 400mA			1.5	V
V_{IN2}-V_{O2}	Drop Out Voltage 2	I_{O2} = 400mA			1.5	V
ΔV_{O1LI}	Line Regulation	7V < V_{IN1} < 14V I_{O1} = 200mA			90	mV
ΔV_{O2LI}	Line Regulation	12V < V_{IN2} < 20V I_{O2} = 200mA V_{O2} = 10V			200	mV
ΔV_{O1LO}	Load Regulation	0 < I_{O1} < 600mA			100	mV
ΔV_{O2LO}	Load Regulation	0 < I_{O2} < 600mA V_{O2} = 10V			200	mV
I_{O1SC}	Short Circuit Current 1	7V < V_{IN1} < 14			1.3	A
I_{O2SC}	Short Circuit Current 2	V_{O2} + 2V < V_{IN2} < 20V			1.3	A
V_{DISH}	Disable Voltage HIGH at Pin 3		2			V
V_{DISL}	Disable Voltage LOW at Pin 3				0.8	V
V_{PROG}	Reference Voltage at Pin 5			2.5		V
I_{DISH}	Bias Current at Pin 3	V_{DIS} = 5.3V			10	µA
I_{DISL}	Bias Current at Pin 3	V_{DIS} = 0.4V	– 80			µA
SVR_1	Supply Voltage Rejection 1 (see note 1)	V_{IN1} = $9V_{DC}$ + $1V_{PP}$ SIN f = 120Hz I_{O1} = 200mA	50			dB
SVR_2	Supply Voltage Rejection (see note 1)	V_{IN2} = $16V_{DC}$ + $1V_{PP}$ SIN f = 120Hz I_{O2} = 200mA	50			dB
I_Q	Quiescent Current	I_{O1} = I_{O2} = 200mA			6	mA
T_{JSD}	Thermal Shut-down Junction Temperature			145		°C

Note 1:
SVR supply voltage rejection

$$20 \cdot LOG \cdot \left| \frac{V_{IN\,ac}}{V_{O\,ac}} \right|$$

where :
- $V_{IN\,ac}$ is the value of the sinusoidal signal forced at the input. (120Hz, $1V_{PP}$)
- $V_{O\,ac}$ is the peak-peak ripple voltage present at the output

TEST SPECIFICATION



CIRCUIT DESCRIPTION

The TDA8135 is a dual voltage regulator with disable.

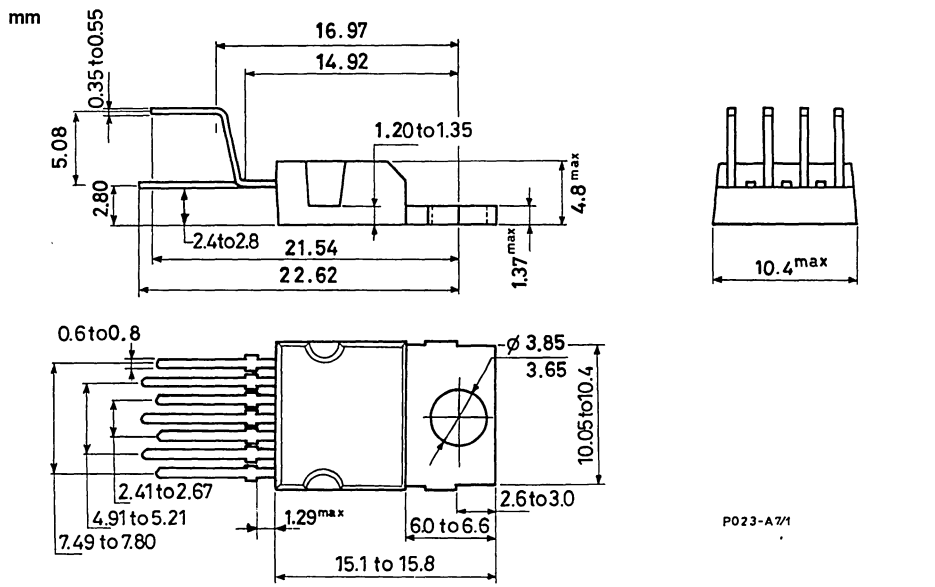
The two regulation parts are supplied from one voltage reference circuit, trimmed by zener zap during EWS test. Since the supply voltage of this last is connected at pin 1 (Vin1), the regulator 2 will not work if the pin 1 is not supplied.

It is possible switch-off the output voltage 2 (V_{O2}) appling at pin 3 (disable input) a low TTL level.

$$V_{O2} = V_{PROG} \frac{R1 + R2}{R1}$$

PACKAGE MECHANICAL DATA

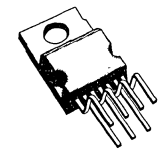
HEPTAWATT – PLASTIC PACKAGE



DUAL 12V REGULATOR WITH DISABLE

ADVANCE DATA

- OUTPUT CURRENTS UP TO 600mA
- FIXED PRECISION OUTPUT 1 VOLTAGE 12V ± 2%
- FIXED PRECISION OUTPUT 2 VOLTAGE 12V ± 2%
- OUTPUT 2 VOLTAGE DISABLED BY A TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUT 1.5V AT 400mA
- HIGH SUPPLY VOLTAGE REJECTION



HEPTAWATT

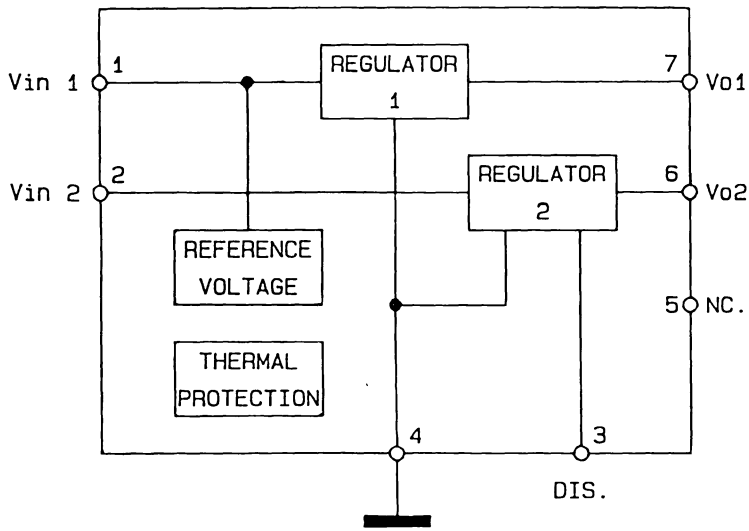
ORDER CODE : TDA8136

DESCRIPTION

The TDA8136 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages, both 12V at currents up to 600mA.

Output 2 can be disabled by a TTL input. Both output currents are limited by an internal short circuit protection.

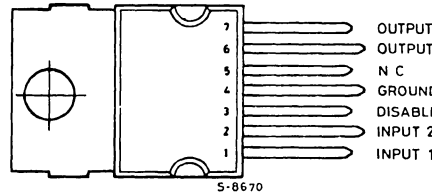
BLOCK DIAGRAM



E89TDA8136-01

This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice

PIN CONNECTION (top view)



Tab connected to pin 4.

E89TDA8136-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{IN1,2}$	DC Input Voltages	24	V
V_{DIS}	Disable Input Voltage Pin 3	24	V
$I_{O1,2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	– 65 to + 150	°C
T_j	Junction Temperature	0 to + 150	°C

THERMAL DATA

$R_{TH(j-c)}$	Maximum Thermal Resistance Junction-case	3	°C/W

ELECTRICAL CHARACTERISTICS

($V_{IN1,2}$ = 14V ; V_{DIS} = 2.5V ; $I_{O1,2}$ = 0 ; T_j = 25°C unless otherwise specified)

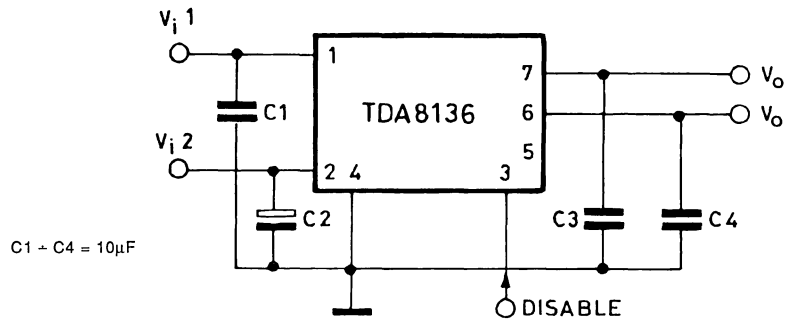
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{O1}	Output Voltage at Pin 7		11.76	12	12.24	V
V_{O2}	Output Voltage at Pin 6		11.76	12	12.24	V
I_{Q1}	Quiescent Current	V_{IN2} = 0 V_{DIS} = 0 I_{O1} = 10mA (see fig. 1)			2	mA
I_{Q2}	Quiescent Current	I_{O2} = 10mA (see fig. 1)			2	mA
V_{IN1}-V_{O1}	Drop Out Voltage 1	I_{O1} = 400mA			1.5	V
V_{IN2}-V_{O2}	Drop Out Voltage 2	I_{O2} = 400mA			1.5	V
ΔV_{O1LI}	Line Regulation 1	14V < V_{IN1} < 18V I_{O1} = 200mA			120	mV
ΔV_{O2LI}	Line Regulation 2	14V < V_{IN2} < 18V I_{O2} = 200mA			120	mV
ΔV_{O1LO}	Load Regulation 1	0 < I_{O1} < 600mA			240	mV
ΔV_{O2LO}	Load Regulation 2	0 < I_{O2} < 600mA			240	mV
I_{O1SC}	Short Circuit Current 1	14V < V_{IN1} < 18V			1.3	A
I_{O2SC}	Short Circuit Current 2	14V < V_{IN2} < 18V			1.3	A
V_{DISH}	Disable Voltage HIGH at Pin 3		2			V
V_{DISL}	Disable Voltage LOW at Pin 3				0.8	V
I_{DISH}	Bias Current at Pin 3	V_{DIS} = 5.3V			10	µA
I_{DISL}	Bias Current at Pin 3	V_{DIS} = 0.4V	– 80			µA
SVR_1	Supply Voltage Rejection 1 (see note 1)	V_{IN1} = 16 V_{DC} + 1V_{PP} SIN f = 120Hz I_{O1} = 200mA	50			dB
SVR_2	Supply Voltage Rejection (see note 1)	V_{IN2} = 16 V_{DC} + 1V_{PP} SIN f = 120Hz I_{O2} = 200mA	50			dB
I_Q	Quiescent Current	I_{O1} = I_{O2} = 200mA			6	mA
T_{JSD}	Thermal Shut-down Junction Temperature			145		°C

Note 1 : SVR supply voltage rejection

$$20 \cdot LOG \cdot \left| \frac{V_{IN\,ac}}{V_{o\,ac}} \right|$$

where :
- $V_{IN\,ac}$ is the value of the sinusoidal signal forced at the input. (120Hz, 1V_{PP})
- $V_{O\,ac}$ is the peak-peak ripple voltage present at the output.

TYPICAL APPLICATION CIRCUIT



E89TDA8136-03

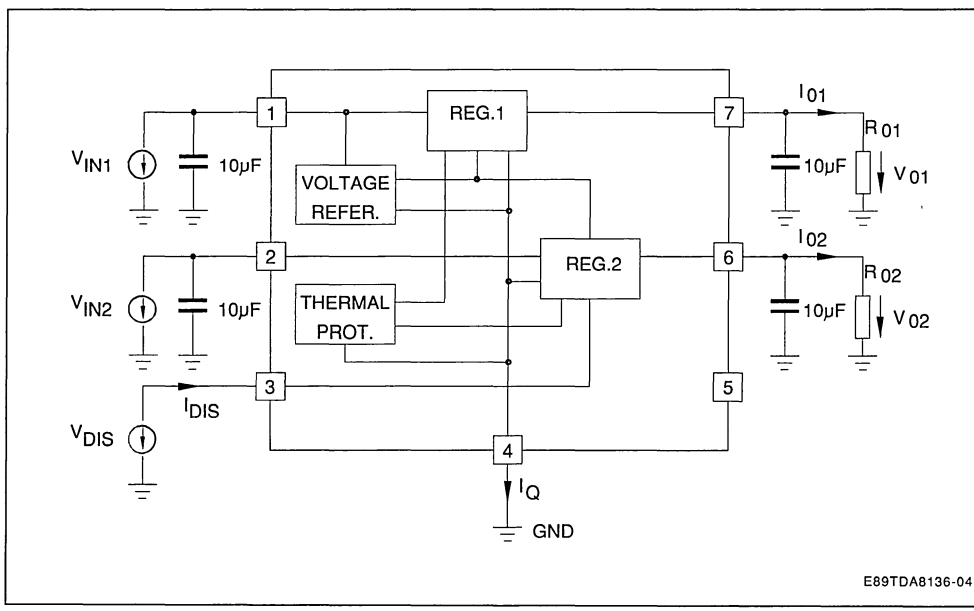
CIRCUIT DESCRIPTION

The TDA8136 is a dual voltage regulator with disable.

The two regulation parts are supplied from one voltage reference circuit, trimmed by zener zap during EWS test. Since the supply voltage of this last is connected at pin 1 (V_{IN1}), the regulator 2 will not work if the pin 1 is not supplied.

It is possible switch-off the output voltage 2 (V_{O2}) applying at pin 3 (disable input) a low TTL level.

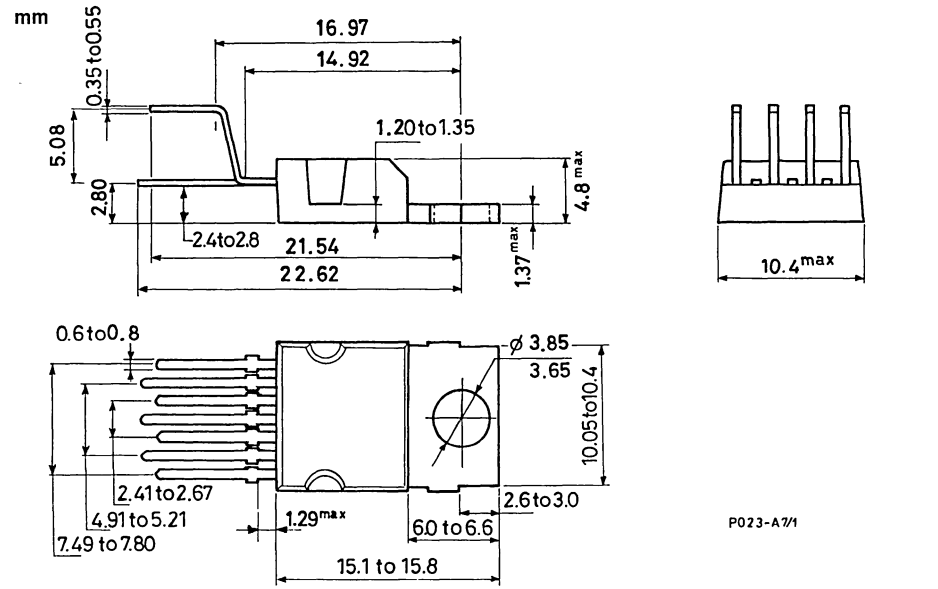
Figure 1 : Test Circuit.



E89TDA8136-04

PACKAGE MECHANICAL DATA

HEPTAWATT – PLASTIC PACKAGE



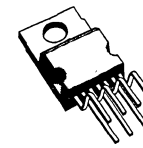
SGS-THOMSON MICROELECTRONICS

TDA8137

DUAL 5.1V REGULATOR WITH DISABLE AND RESET

ADVANCE DATA

- OUTPUT CURRENTS UP TO 1A
- FIXED PRECISION OUTPUT VOLTAGES 5.1V ± 2%
- OUTPUT 1 WITH RESET FACILITY
- OUTPUT 2 WITH DISABLE BY TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUTPUT VOLTAGE



HEPTAWATT

ORDER CODE : TDA8137

DESCRIPTION

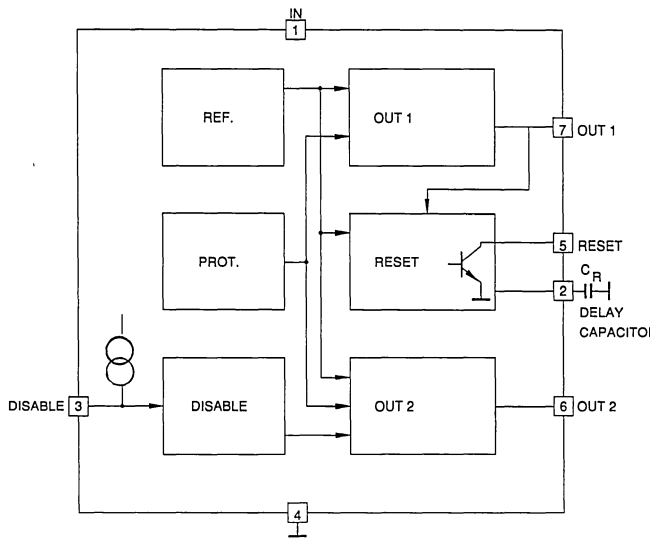
The TDA8137 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages of 5.1V at currents up to 1A.

An internal reset circuit generates a delayed reset pulse when the output 1 decrease below the regulated voltage value.

Output 2 can be disabled by TTL input.

Short circuit and thermal protections are included.

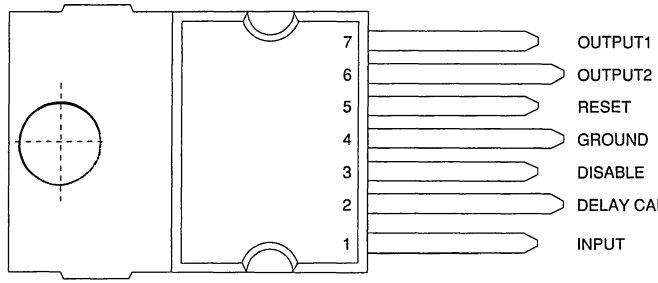
BLOCK DIAGRAM



E89TDA8137-01

This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice

PIN CONNECTION (top view)



E89TDA8137-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	DC Input Voltage Pin 1	20	V
V_{DIS}	Disable Input Voltage Pin 3	20	V
V_{RST}	Output Voltage at Pin 5	20	V
$I_{01,2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	– 65 to + 150	°C
T_j	Junction Temperature	0 to + 150	°C

THERMAL DATA

$R_{TH(j-c)}$	Maximum Thermal Resistance Junction-case	3	°C/W

ELECTRICAL CHARACTERISTICS (V_{IN} = 7V ; T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{01,2}$	Output Voltage	$I_{01,2}$ = 10mA	5	5.1	5.2	V
		7V < V_{IN} < 14V 5mA < I_0 < 750mA	4.9		5.3	V
$V_{I01,2}$	Dropout Voltage	$I_{01,2}$ = 750mA			1.4	V
		$I_{01,2}$ = 1A			2	V
$\Delta V_{01,2LI}$	Line Regulation	7V < V_{IN} < 14V $I_{01,2}$ = 200mA			50	mV
$\Delta V_{01,2LO}$	Load Regulation	5mA < $I_{01,2}$ < 0.6A			100	mV
I_Q	Quiescent Current	I_{01} = 10mA Output 2 Disabled			2	mA
V_{01RST}	Reset Threshold Voltage	(K = V_{01})	K–0.4	K–.25	K–0.1	V
V_{RTH}	Reset Threshold Hysteresis	(see note 1)	20		75	mV
t_{RD}	Reset Pulse Delay at Pin 5	C_e = 100nF (see note 1)		25		ms
V_{RL}	Saturation Volt. at Pin 5 in Reset Condition	I_5 = 5mA			0.4	V
I_{RH}	Leakage Current at Pin 5 in Normal Condition	V_5 = 10V			10	µA
$K_{01,2}$	Output Volt. Thermal Drift	$K_0 = \frac{\Delta Vo \,.\, 10^6}{\Delta T \,.\, Vo}$ T_j = 0 to + 125°C		100		ppm/°C
$I_{01,2SC}$	Short Circ. Output Current	V_{IN} = 7V			1.6	A
		V_{IN} = 18V (see note 2)			0.7	A
V_{DISH}	Disable Volt. at Pin 3 High (out 2 active)		2			V
V_{DISL}	Disable Volt. at Pin 3 Low (out 2 disabled)				0.8	V
I_{DIS}	Disable Bias Current at Pin 3	0V < V_{DIS} < 7V	– 100		2	µA
T_{jsd}	Junction Temp. for Thermal Shut Down			145		°C

Notes : 1. If the output voltage OUT 1 goes below 4.85V (V_{OUT} - 0.25V) the comparator "a" (see fig. 1) discharge rapidly the capacitor Ce and the Reset output (pin 5) goes at once LOW.
When the voltage at the OUT 1 rises above 4.9V, the voltage at pin 2 increases with this law :

$$t_d = \frac{Ce \,.\, 2.5V}{10\mu A} \quad \text{(see fig. 2)}$$

as V_2 reach 2.5V the Reset output (pin 5) goes HIGH again. To avoid glitches in the Reset output the second comparator "b" has a large hysteresis (1.9V).

2. The output short circuit currents are tested one channel at time.
During a short circuit a large consumption of power occurs, anyway the thermal protection circuit guarantees the temperature not overcomes high value.

Figure 1.

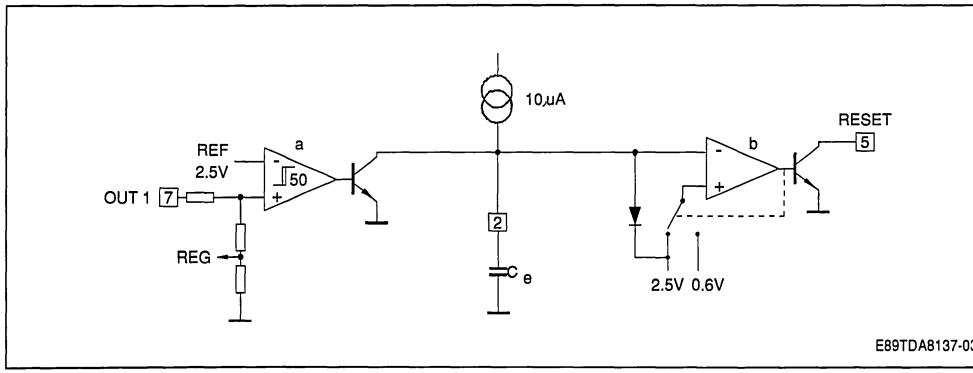
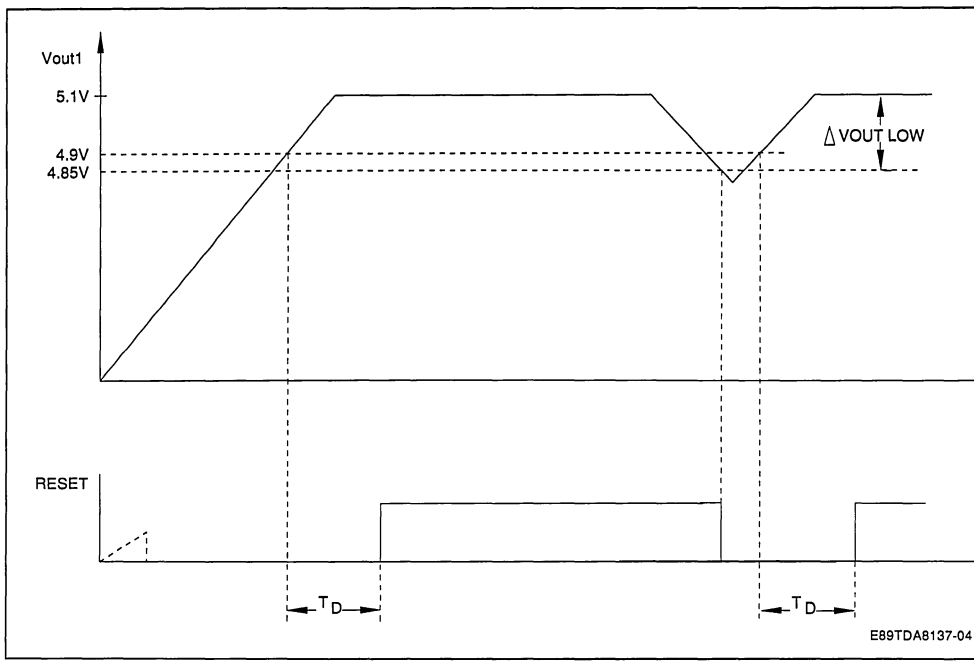
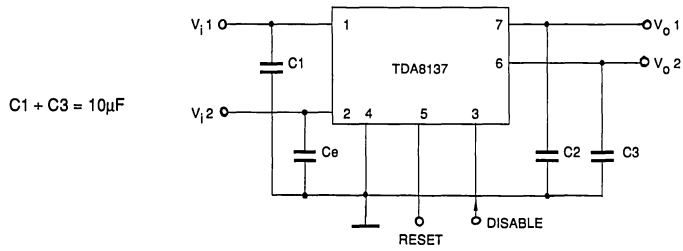


Figure 2.



TYPICAL APPLICATION CIRCUIT



E89TDA8137-05

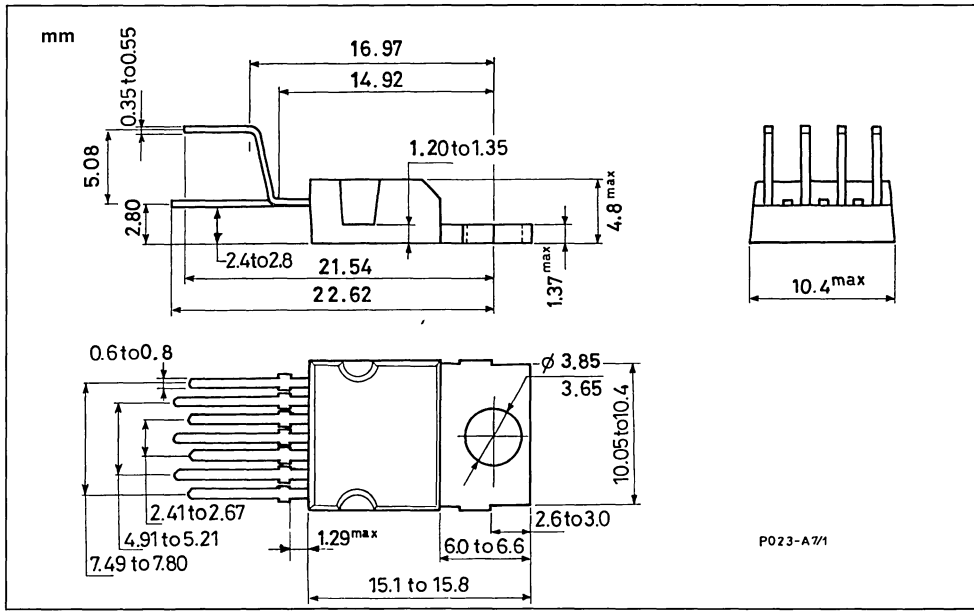
CIRCUIT DESCRIPTION

The TDA8137 is a dual voltage regulator with Reset and Disable.
The two regulation parts are supplied from one voltage reference circuit trimmed by zener zap during EWS test.
The outputs stage have been realized in darlington configuration with a drop typical 1.2V.

The disable circuit, switch-off the output 2 if a voltage lower than 0.8V is applied at pin 3.
The Reset circuit controls the voltage at the output 1, if this one decrease below 4.85V provides to generate a reset pulse at pin 5 (open collector) with a certain delay depending by an external capacitor connected at pin 2.

PACKAGE MECHANICAL DATA

HEPTAWATT – PLASTIC PACKAGE



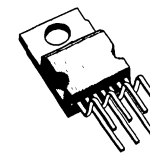
SGS-THOMSON MICROELECTRONICS

TDA8138

DEDICATED VIDEO PRODUCTS
5.1V + 12V REGULATOR WITH DISABLE AND RESET

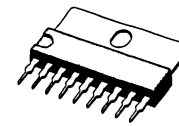
ADVANCE DATA

- OUTPUT CURRENTS UP TO 1A
- FIXED PRECISION OUTPUT 1 VOLTAGE 5.1V ± 2%
- FIXED PRECISION OUTPUT 2 VOLTAGE 12V ± 2%
- OUTPUT 1 WITH RESET FACILITY
- OUTPUT 2 WITH DISABLE BY TTL INPUT
- SHORT-CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROPOUT VOLTAGE
- AVAILABLE ALSO IN HEPTAWATT PACKAGE (but without reset facility)



HEPTAWATT

ORDER CODE : TDA8138



SIP-9

ORDER CODE : TDA8138S

DESCRIPTION

The TDA8138 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages of 5.1V and 12V at currents up to 1A.

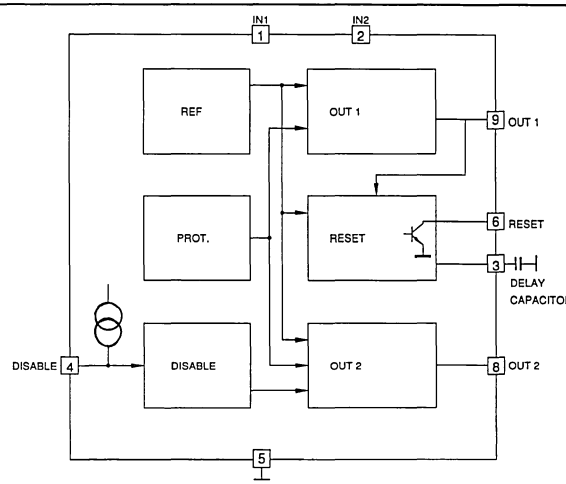
An internal reset circuit generates a delayed reset pulse when the output 1 falls below the regulated voltage value.

Output 2 can be disabled by TTL input.

Short-circuit and thermal protections are included.

BLOCK DIAGRAM

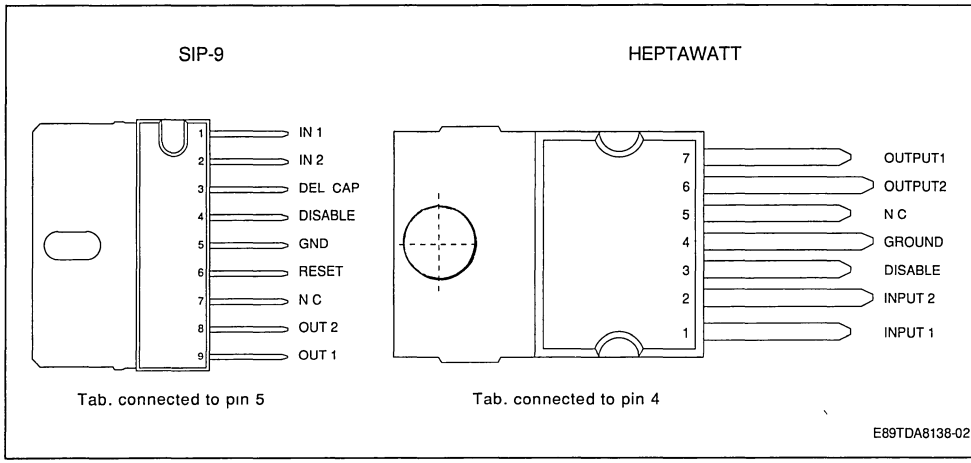
SIP-9 Package



E89TDA8138-01

This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice

PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	DC Input Voltage Pin 1	20	V
V_{DIS}	Disable Input Voltage Pin 3 (HEPTAWATT) or Pin 4 (SIP-9)	20	V
V_{RST}	Output Voltage at Pin 6	20	V
$I_{O1,2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	– 65 to + 150	°C
T_j	Junction Temperature	0 to + 150	°C

THERMAL DATA

$R_{th(j-c)}$	Maximum Thermal Resistance Junction-case for Sip-9	8	°C/W
	for Heptawatt	3	°C/W
$R_{th(j-a)}$	Maximum Thermal Resistance Junction-ambient for Sip-9	60	°C/W

ELECTRICAL CHARACTERISTICS (V_{IN1} = 7V ; V_{IN2} = 14V ; T_j = 25°C ; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{O1}	Output Voltage	I_{O1} = 10mA	5	5.1	5.2	V
V_{O2}	Output Voltage	I_{O2} = 10mA	11.76	12	12.24	
V_{O1}	Output Voltage	7V < V_{IN1} < 14V	4.9		5.3	V
V_{O2}	Output Voltage	14 < V_{IN2} < 18 5mA < $I_{O1,2}$ < 750mA	11.5		12.5	V
$V_{IO1,2}$	Dropout Voltage	$I_{O1,2}$ = 750mA			1.4	V
		$I_{O1,2}$ = 1A			2	V
$V_{O1,2LI}$	Line Regulation	7V < V_{IN1} < 14V			50	mV
		14V < V_{IN2} < 18V			120	mV
		$I_{O1,2}$ = 200mA				
$V_{O1,2LO}$	Load Regulation	5mA < I_{O1} < 0.6A 5mA < I_{O2} < 0.6A			100 250	mV mV
I_Q	Quiescent Current	I_{O1} = 10mA Output 2 Disabled			2	mA
V_{O1RST}	Reset Threshold Voltage	(K = V_{O1})	K – 0.4	K – .25	K – 0.1	V
V_{RTH}	Reset Threshold Hysteresis	(see note 1)	20	50	75	mV
t_{RD}	Reset Pulse Delay at Pin 6	C_e = 100nF (see note 1)		25		ms
V_{RL}	Saturation Volt. at Pin 6 in Reset Condition	I_5 = 5mA			0.4	V
I_{RH}	Leakage Current at Pin 6 in Normal Condition	V_5 = 10V			10	µA
$V_{O1,2}/T$	Output Volt. Thermal Drift			100		ppm/°C
$I_{O1,2SC}$	Short Circ. Output Current	V_{IN1} = 7V V_{IN2} = 14V			1.6	A
		$V_{IN1,2}$ = 18V (see note 2)			0.7	A
V_{DISH}	Disable Volt. High (out 2 active)		2			V
V_{DISL}	Disable Volt. Low (out 2 disabled)				0.8	V
I_{DIS}	Disable Bias Current	0V < V_{DIS} < 7V	– 100		2	µA
T_{jsd}	Junction Temp. for Thermal Shut Down			145		°C

Notes : 1. If the output voltage OUT 1 goes below 4.85V (V_{OUT} - 0.25V) the comparator "a" (see fig 1) discharges rapidly the capacitor Ce and the Reset output (pin 6) goes at once LOW.
When the voltage at the OUT 1 rises above 4.9V, the voltage at pin 3 increases with this law :

$$t_d = \frac{Ce \cdot 2.5V}{10/\mu A}$$ (see fig. 2)

as V_2 reach 2.5V the Reset output (pin 6) goes HIGH again.To avoid glitches in the Reset output the second comparator "b" has a large hysteresis (1.9V).

2. The output short circuit currents are tested one channel at a time.
During a short circuit a large consumption of power occurs, anyway the thermal protection circuit guarantees the temperature not overcomes high value.

Figure 1.

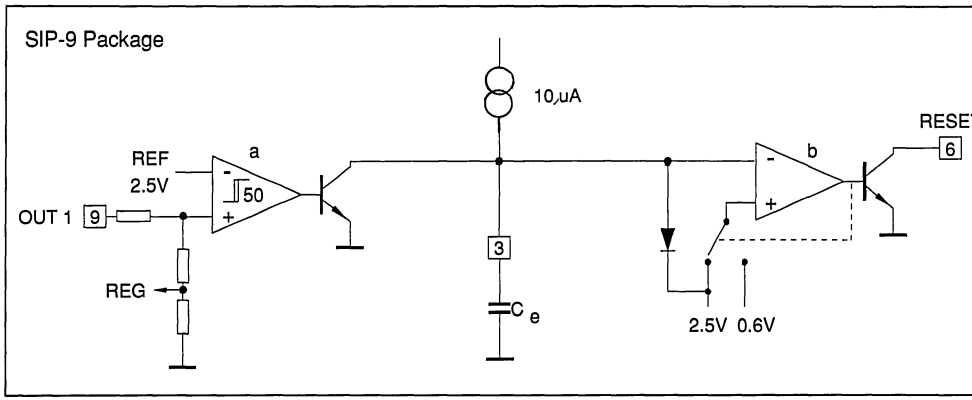
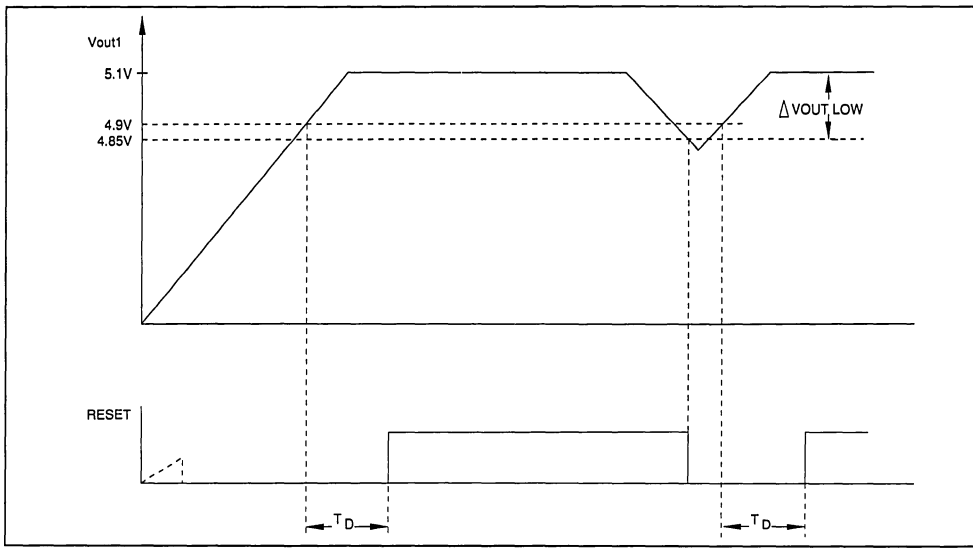


Figure 2.



CIRCUIT DESCRIPTION

The TDA8138 is a dual voltage regulator with Reset and Diasable.

The two regulation parts are supplied from one voltage reference circuit trimmed by zener zap during EWS test.

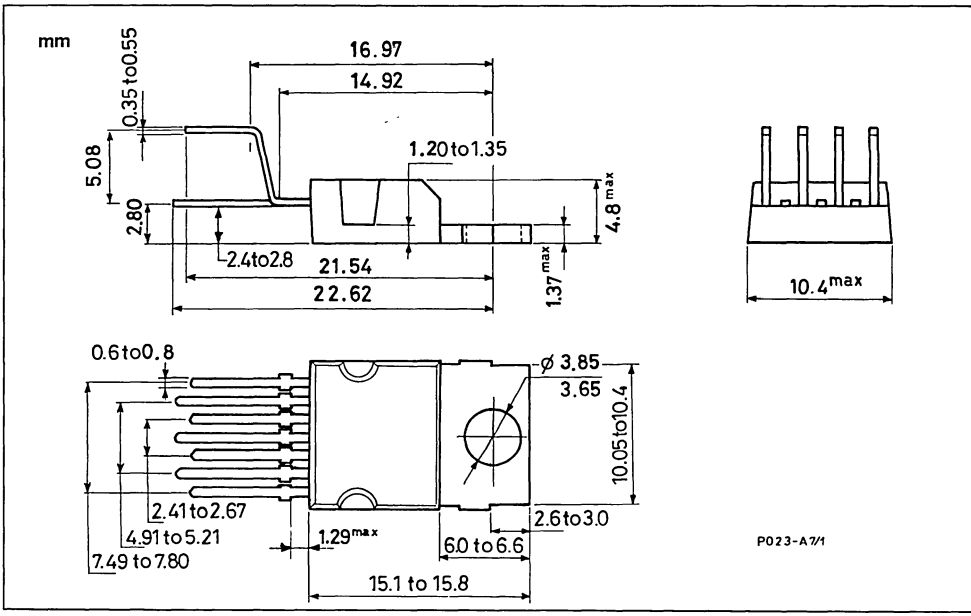
The output stages have been realized in darlington configuration with a drop typical 1.2V.

The disable circuit, switch-off the output 2 if a voltage lower than 0.8V is applied at pin 3 (HEPTAWATT) or pin 4 (SIP-9).

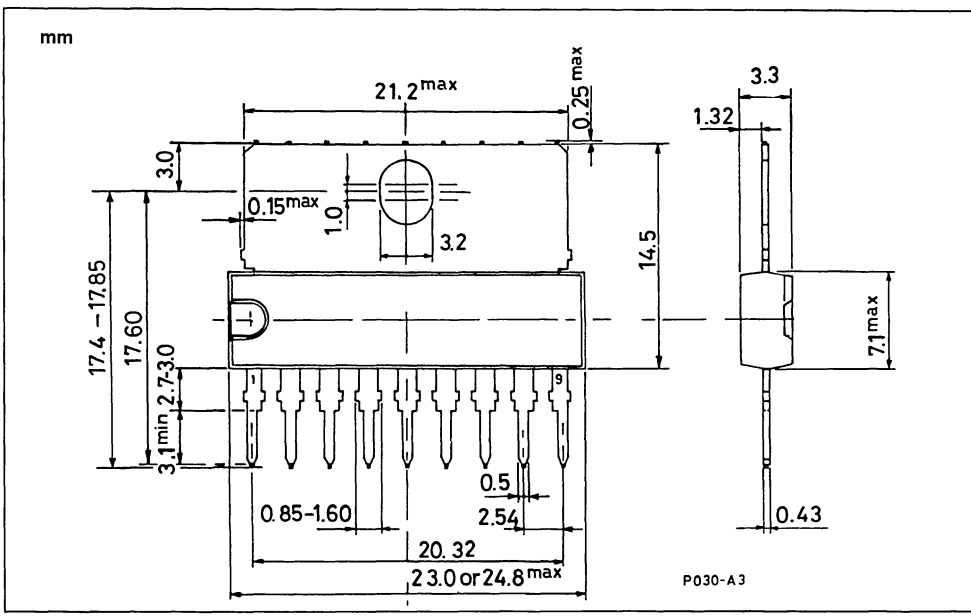
The Reset circuit controls the voltage at the output 1, if this one decrease below 4.85V provides to generate a reset pulse at pin 6 (open collector) with a certain delay depending by an external capacitor connected at pin 3.

PACKAGE MECHANICAL DATA

HEPTAWATT – PLASTIC PACKAGE



9 PINS – PLASTIC SIP



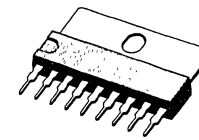
SGS-THOMSON MICROELECTRONICS

TDA8139

5.1V AND ADJUSTABLE VOLTAGE REGULATOR WITH DISABLE AND RESET

ADVANCE DATA

- OUTPUT CURRENTS UP TO 1A
- FIXED PRECISION OUTPUT 1 VOLTAGE 5.1V ± 2%
- OUTPUT 2 VOLTAGE PROGRAMMABLE FROM 2.5 TO 16V
- OUTPUT 1 WITH RESET FACILITY
- OUTPUT 2 WITH DISABLE BY TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUTPUT VOLTAGE



SIP-9

ORDER CODE : TDA8139

DESCRIPTION

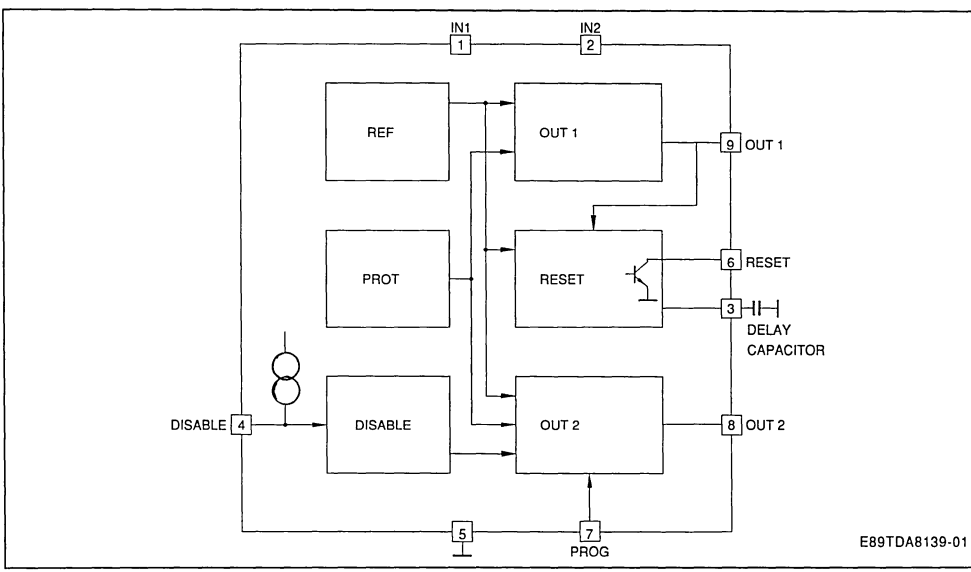
The TDA8139 is a monolithic dual positive voltage regulator designed to provide precision output voltages of 5.1V and adjustable at currents up to 1A.

An internal reset circuit generates a delayed reset pulse when the output 1 decreases below the regulated voltage value.

Output 2 can be disabled by TTL input.

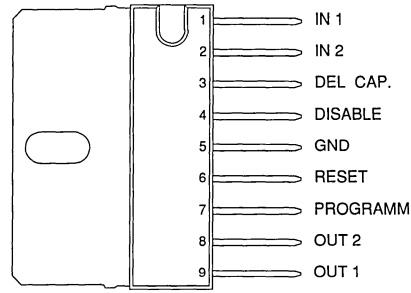
Short circuit and thermal protections are included.

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice

PIN CONNECTION (top view)



E89TDA8139-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	DC Input Voltage Pin 1, 2	20	V
V_{DIS}	Disable Input Voltage Pin 4	20	V
V_{RST}	Output Voltage at Pin 6	20	V
$I_{O1,2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	– 65 to + 150	°C
T_J	Junction Temperature	0 to + 150	°C

THERMAL DATA

$R_{TH(j-c)}$	Maximum Thermal Resistance Junction-case	8	°C/W

ELECTRICAL CHARACTERISTICS (V_{IN} = 7V ; T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{O1}	Output Voltage	I_{O1} = 10mA	5	5.1	5.2	V
V_{O2}	Output Voltage	I_{O2} = 10mA	2.5		16	V
$V_{IO1,2}$	Dropout Voltage	$I_{O1,2}$ = 750mA			1.4	V
		$I_{O1,2}$ = 1A			2	V
V_{O1}	Line Regulation	7V < V_{IN1} < 14V 12V < V_{IN2} < 18V @ V_{O2} : 10V $I_{O1,2}$ = 200mA			50	mV
V_{O2}	Line Regulation				100	mV
V_{O1}	Load Regulation	5mA < $I_{O1,2}$ < 0.6A @ V_{O2} = 10 V			100	mV
V_{O2}	Load Regulation				200	mV
I_Q	Quiescent Current	I_{O1} = 10mA Output 2 Disabled			2	mA
V_{O1RST}	Reset Threshold Voltage	(K = V_{O1})	K – 0.4	K – .25	K – 0.1	V
V_{RTH}	Reset Threshold Hysteresis	(see note 1)	20	50	75	mV
t_{RD}	Reset Pulse Delay at Pin 6	C_e = 100nF (see note 1)		25		ms
V_{RL}	Saturation Volt. at Pin 6 in Reset Condition	I_5 = 5mA			0.4	V
I_{RH}	Leakage Current at Pin 5 in Normal Condition	V_5 = 10V			10	µA
$V_{O1,2}/T$	Output Volt. Thermal Drift			100		ppm/°C
$I_{O1,2\,sc}$	Short Circ. Ouput Current	V_{IN} = 7V			1.6	A
		V_{IN} = 18V (see note 2)			0.7	A
V_{DISH}	Disable Volt. at Pin 4 High (out 2 active)		2			V
V_{DISL}	Disable Volt. at Pin 4 Low (out 2 disabled)				0.8	V
I_{DIS}	Disable Bias Current at Pin 4	0V < V_{DIS} < 7V	– 100		2	µA
V_{ref}	Pin 7			2.5		V
T_{jsd}	Junction Temp. for Thermal Shut Down			145		°C

Notes : 1. If the output voltage OUT 1 goes below 4 85V (V_{OUT} - 0.25V) the comparator "a" (see fig 1) discharges rapidly the capacitor Ce and the Reset output (pin 5) goes at once LOW.
When the voltage at the OUT 1 rises above 4.9V, the voltage at pin 2 increases with this law ;

$$t_d = \frac{Ce \,.\, 2.5V}{10\mu A} \quad \text{(see fig. 2)}$$

as V_2 reach 2.5V the Reset output (pin 5) goes HIGH again. To avoid glitches in the Reset output the second comparator "b" has a large hysteresis (1.9V).

2. The output short circuit currents are tested one channel at time.
During a short circuit a large consumption of power occurs, anyway the thermal protection circuit guarantees the temperature not overcomes high value.

Figure 1.

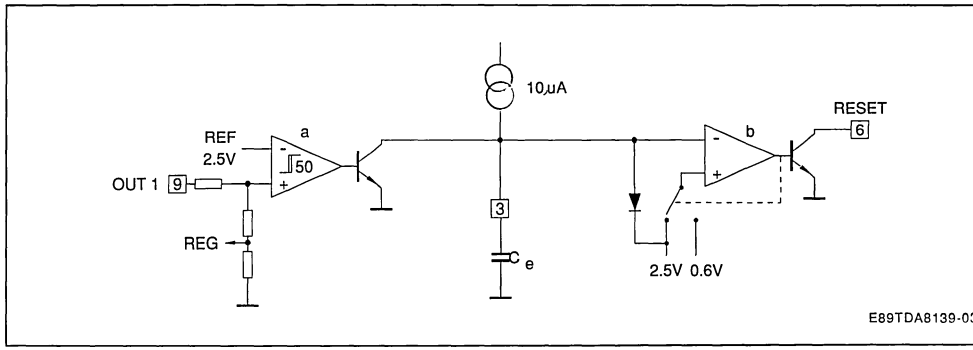
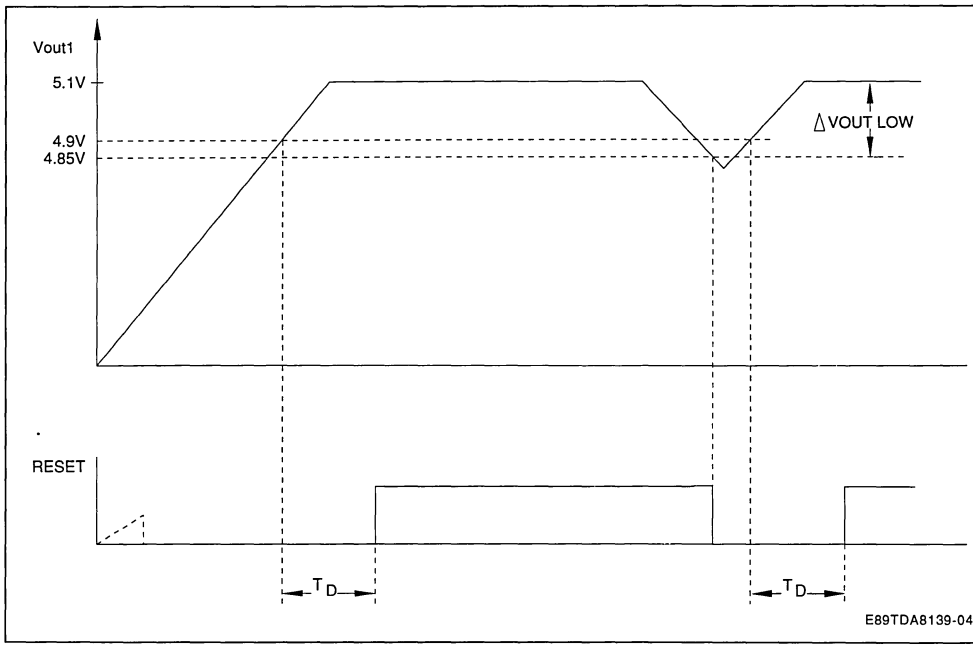
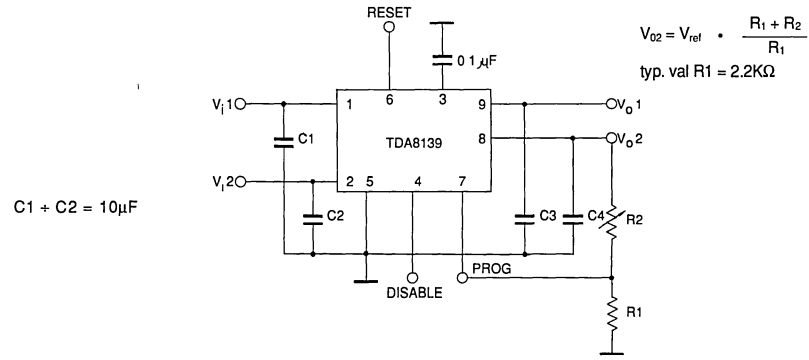


Figure 2.



TYPICAL APPLICATION CIRCUIT



CIRCUIT DESCRIPTION

The TDA8139 is a dual voltage regulator with Reset and Disable.

The two regulation parts are supplied from one voltage reference circuit trimmed by zener zap during EWS test.

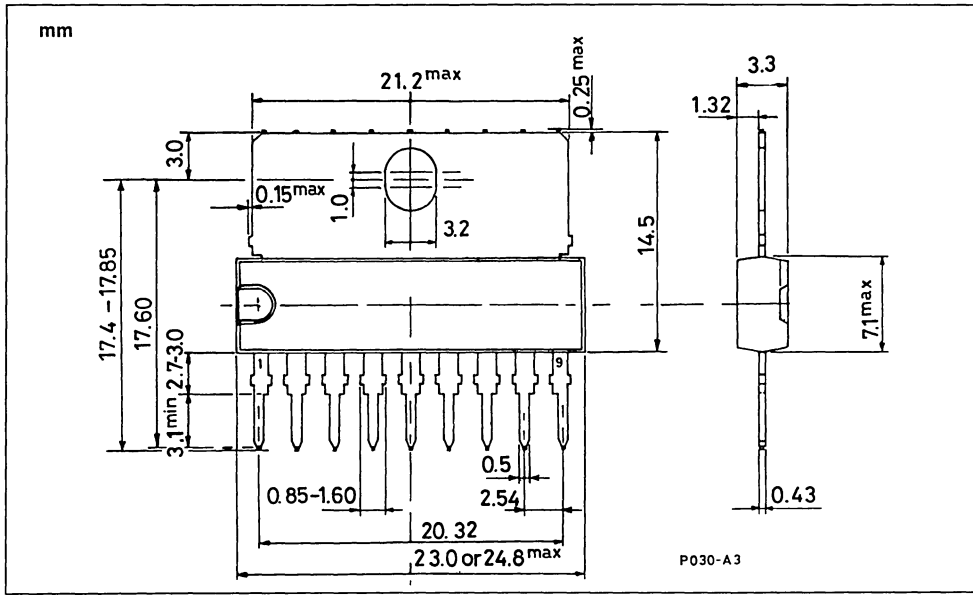
The outputs stage have been realized in darlington configuration with a drop typical 1.2V.

The disable circuit, switch-off the output 2 if a voltage lower than 0.8V is applied at pin 4.

The Reset circuit controls the voltage at the output 1, if this one decrease below 4.85V provides to generate a reset pulse at pin 6 (open collector) with a certain delay depending by an external capacitor connected at pin 3.

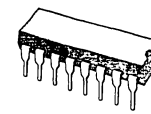
PACKAGE MECHANICAL DATA

9 PINS – PLASTIC SIP



POWER SINGLE OPERATIONAL AMPLIFIER

- OUTPUT CURRENT UP TO 500 mA
- OFFSET VOLTAGE NULL CAPABILITY
- SHORT-CIRCUIT PROTECTION
- THERMAL OVERLOAD PROTECTION
- PLASTIC PACKAGE FOR EASY ASSEMBLY



N
DIP16
(Plastic Package)

DESCRIPTION

The TDB7910 is an internally compensated medium power operational amplifier intended for use in those applications requiring load currents of several hundred milliamperes. Applications include servo amplifiers, driver interfaces, precision power comparators and motor speed control.

The amplifier is designed to operate from a single or dual power supplies and the input common-mode range includes the negative supply if balance inputs are tied to the negative supply.

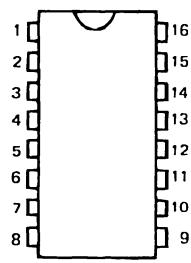
The TDB7910 is thermal overload and short-circuit protected.

ORDER CODES

Part Number	Temperature Range	Package
		N
TDB7910	0 °C to + 70 °C	•
Example : TDB7910N		

PIN CONNECTIONS (top view)

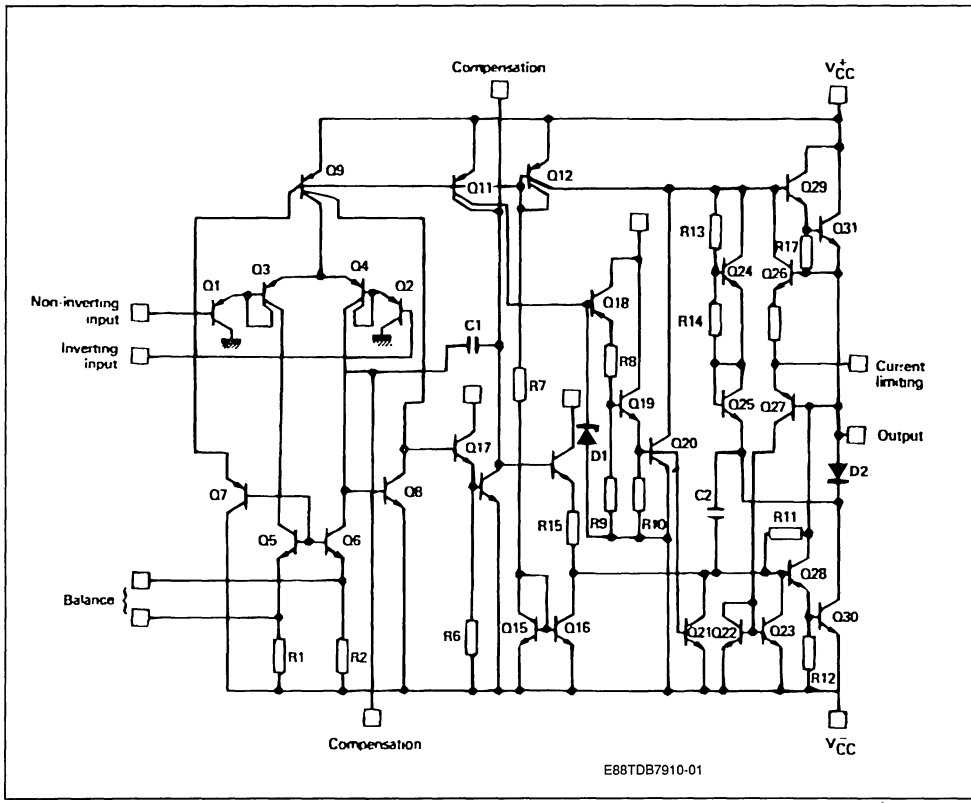
DIP16



1 - V_{CC}^-
2 - V_{CC}^-
3 -NC
4 - V_{CC}^-
5 - V_{CC}^-
6 - Output
7 - V_{CC}^+
8 - Current limiting
9 - Compensation
10 - Inverting input
11 - Non-inverting input
12 - V_{CC}^-
13 - V_{CC}^-
14 - Balance
15 - Balance
16 - Compensation

E88TDB7910-06

SCHEMATIC DIAGRAM



Case	V_{CC}^{-}	NC	V_{CC}^{+}	Output	Current Limiting	Compensation	Non-Inverting Input	Inverting input	Balance
DIP16	1, 2 4, 5 12, 13	3	7	6	8	9, 16	11	10	1

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	± 18	V
V_I	Input Voltage	± 15	V
V_{ID}	Differential Input Voltage	± 30	V
I_O	Output Current*	0.75	A
P_{tot}	Power Dissipation	7.5	W
T_{oper}	Operating Free-air Temperature Range	0 to + 70	°C
T_{stg}	Storage Temperature Range	− 65 to + 150	°C

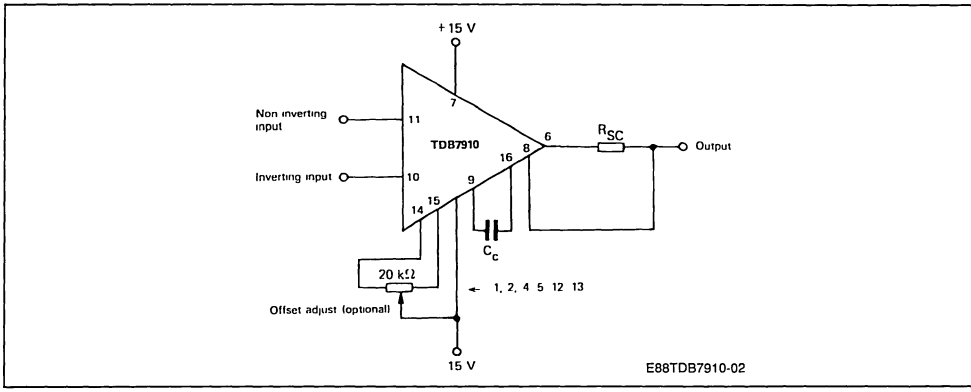
* Under short-circuit conditions, the safe operating area and dc power dissipation limitations must be observed.

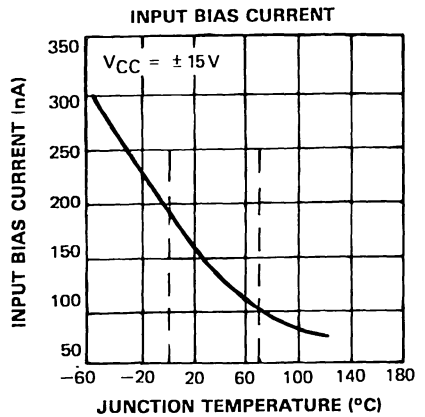
ELECTRICAL CHARACTERISTICS

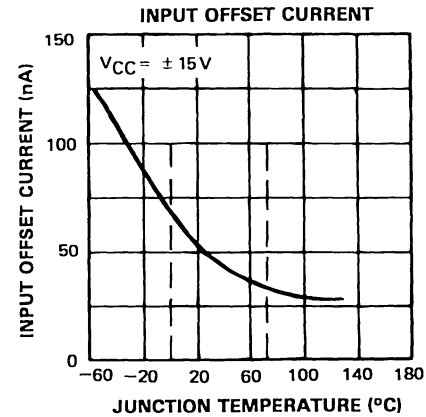
TDB7910 : 0 °C ≤ T_{amb} ≤ + 70 °C, V_{CC} = + 15 V (unless otherwise specified)

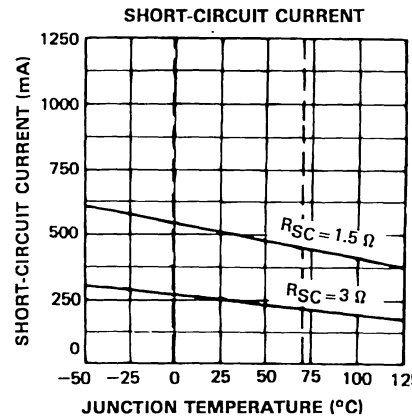
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IO}	Input Offset Voltage (R_S ≤ 10 kΩ) T_{amb} = + 25 °C T_{min} ≤ T_{amb} ≤ T_{max}		2	6 7.5	mV
I_{IO}	Input Offset Current T_{amb} = + 25 °C T_{min} ≤ T_{amb} ≤ T_{max}		20	200 300	nA
I_{IB}	Input Bias Current T_{amb} = + 25 °C T_{min} ≤ T_{amb} ≤ T_{max}		80	500 800	nA
A_{VD}	Large Signal Voltage Gain T_{amb} = + 25 °C (R_L = 47 Ω) T_{min} ≤ T_{amb} ≤ T_{max} (R_L = 2 kΩ)	20 15			V/mV
I_{CC}^+, I_{CC}^-	Supply Currents (no signal) T_{amb} = + 25 °C T_{min} ≤ T_{amb} ≤ T_{max}			20 25	mA
V_I	Input Voltage Range	± 12	± 13		V
I_{OS}	Output Circuit Current T_{amb} = + 25 °C, R_{SC} = 1.5 Ω		0.5		A
SVR	Supply Voltage Rejection Ratio			150	μV/V
CMR	Common-mode Rejection Ratio	70			dB
Z_I	Input Impedance (T_{amb} = + 25 °C)	0.3	1		MΩ
V_{OPP}	Output Voltage Swing (R_{SC} = 0, R_L = 47 Ω) T_j = + 25 °C T_{min} ≤ T_{amb} ≤ T_{max}	± 11.5 ± 10	± 12.5		V
V_{IOR}	Offset Voltage Adjustment Range		± 15		mV
SVO	Slew Rate (R_L = 47 Ω, T_{amb} = + 25 °C, A_V = 1)		0.5		V/μs
GW_R	Small Signal Bandwidth (C_C = 0, T_{amb} = + 25 °C)		1		MHz
RTH	Thermal Resistance		60		°C/W

BASIC DIAGRAM



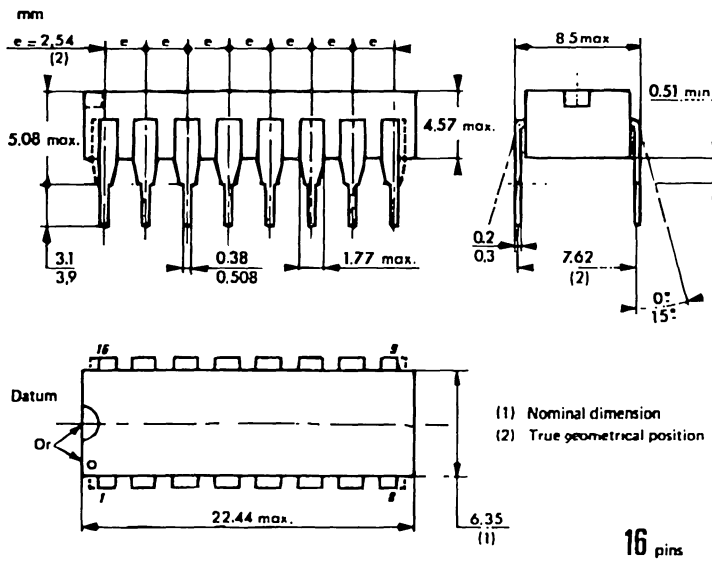






PACKAGE MECHANICAL DATA

16 PINS – PLASTIC DIP



LOW DROP-OUT 5V DUAL VOLTAGE REGULATOR

- OUTPUT CURRENT OF BOTH REGULATORS : 100 mA GUARANTEED
- INTERNAL SHORT-CIRCUIT AND THERMAL PROTECTION
- FIRST REGULATOR OUTPUT : LOW DISCHARGE CURRENT
- SECOND REGULATOR OUTPUT : SWITCHED-OFF WITH ACTIVE DISCHARGE
- RESET OUTPUT WITH ADJUSTABLE PULSE WIDTH

DESCRIPTION

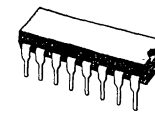
The TEA5110 is a dual positive 5V voltage regulator specially designed to supply a microprocessor and associated circuits.

The first regulator supplies the microprocessor in normal operating conditions. In standby mode, the regulator has a very high output impedance (current drain less than 1 µA) and the microprocessor may be powered by a battery.

The second regulator supplies the peripherals and provides a halt signal to the microprocessor to turn it in standby mode.

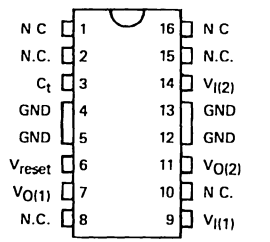
The circuit generates a reset pulse when :

- the supply voltage is applied to the circuit and the output of the second regulator is at its nominal value, and
- when the output of the second regulator is at its nominal value again after a shut-down on the output of the first regulator (see figure 2 page 4).



TEA5110
BATWING DIP16
(Plastic Package)

PIN CONNECTIONS



E88TEA5110-01

1 - N.C.
2 - N.C.
3 - C_t : Time constant capacitor
4 - GND : Ground
5 - GND : Ground
6 - V_{reset} : Reset output
7 - $V_{O(1)}$: Output voltage 1
8 - N.C.
9 - $V_{I(1)}$: Input voltage
10 - N.C.
11 - $V_{O(2)}$: Output voltage 2
12 - GND : Ground
13 - GND : Ground
14 - $V_{I(2)}$: Input voltage 2
15 - N.C.
16 - N.C.

ABSOLUTE MAXIMUM RATINGS

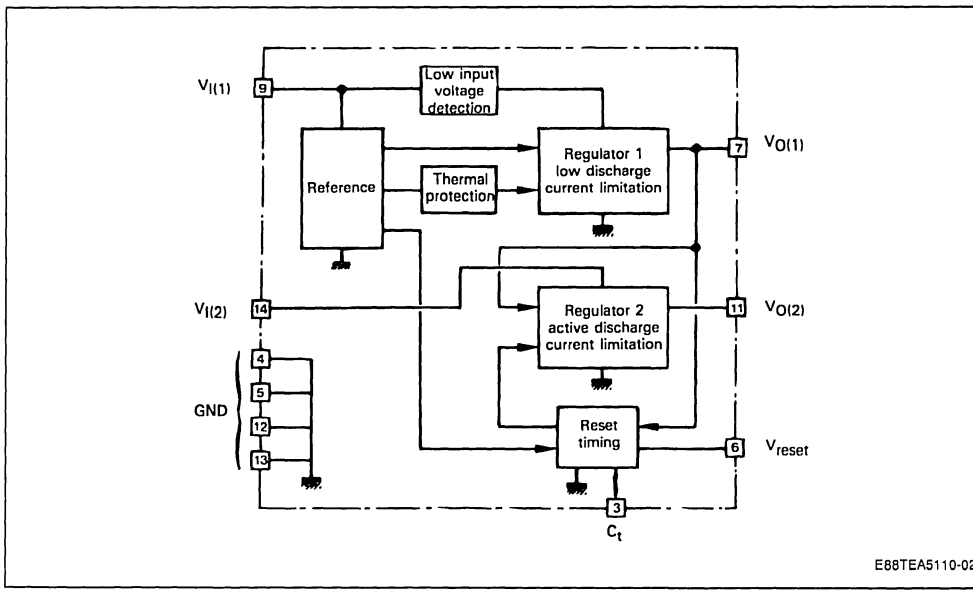
Symbol	Parameter	Value	Unit
V_I	Input Voltage	20	V
I_O	Output Current	Internally Limited	A
P_{tot}	Power Dissipation	Internally LImited	W
T_{oper}	Operating Ambient Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C

THERMAL DATA

$R_{th(j-a)}$*	Junction–ambient Thermal Resistance	45	°C/W
$R_{th(j-c)}$	Junction–case Thermal Resistance	11	°C/W

* The $R_{th(j-a)}$ is measured on devices soldered on 35 µm thick copper surface of 40 cm2.

BLOCK DIAGRAM



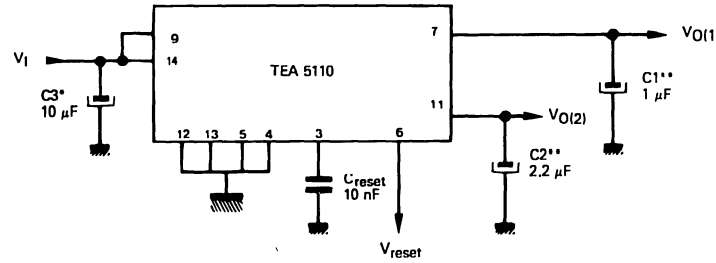
ELECTRICAL CHARACTERISTICS

T_j = + 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{O(1)}$	Output Voltage (+ 7 V ≤ V_I ≤ + 18 V, 0 ≤ $I_{O(1)}$ ≤ 100 mA)	4.9	5.05	5.2	V
$V_{O(2)}$	Output Voltage (+ 7 V ≤ V_I ≤ + 18 V, 0 ≤ $I_{O(2)}$ ≤ 100 mA)	4.8	5	5.2	V
$V_{O(1)}$–$V_{O(2)}$	Output Voltage Difference + 7 V ≤ V_I ≤ + 18 V, 0 ≤ $I_{O(1)}$ ≤ 100 mA, 0 ≤ $I_{O(2)}$ ≤ 100 mA	0	50	100	mV
	Line Regulation				
$K_{VI(1)}$	+ 6.8 V ≤ V_I ≤ + 18 V, $I_{O(1)}$ = 50 mA		10	50	mV
$K_{VI(2)}$	+ 6.8 V ≤ V_I ≤ + 18 V, $I_{O(2)}$ = 50 mA		20	50	mV
	Load Regulation				
$K_{VO(1)}$	5 mA ≤ $I_{O(2)}$ ≤ 100 mA, V_I = + 10 V		10	50	mV
$K_{VO(2)}$	5 mA ≤ $I_{O(2)}$ ≤ 100 mA, V_I = + 10 V		20	50	mV
I_Q	Quiescent Current (+ 6.8 V ≤ V_I ≤ + 18 V, $I_{Q(1)}$ = $I_{Q(2)}$ = 0)		6	8	mA
	Short–circuit Current				
$I_{SC(1)}$	V_I = + 10 V, 0 ≤ $V_{O(1)}$ ≤ + 5 V		200		mA
$I_{SC(2)}$	V_I = + 10 V, 0 ≤ $V_{O(2)}$ ≤ + 5 V		200		mA
	Minimum Dropout Voltage - (note 1)				
V_I–$V_{O(1)}$	Output 1 $I_{O(1)}$ = 0		1.4		V
	Output 1 $I_{O(1)}$ = 0.1 A		1.6		V
V_I–$V_{O(2)}$	Output 2 $I_{O(2)}$ = 0		1.5		V
	Output 2 $I_{O(2)}$ = 0.1 A		1.7		V
$I_{dis(1)}$	$V_{O(1)}$ Discharge Current (V_I = 0, $V_{O(1)}$ = + 5 V)			1	µA
	Minimum Input Voltage to Switch on $V_{O(2)}$ Output (fig. 1, note 2)	(V_{O1}+1.4)	(V_{O1}+1.6)	(V_{O1}+1.8)	V
ΔV_{IL}	Input Hysteresis to Switch off $V_{O(2)}$ Output (fig. 1)	200	300	400	mV
	Minimum $V_{O(1)}$ Output Voltage to Switch on $V_{O(2)}$	4.5	4.6	4.7	V
$\Delta V_{C(1)}$	$V_{O(1)}$ Hysteresis Voltage to switch off $V_{O(2)}$ (fig. 2)	30	50	70	mV
$V_{L(02)}$	$V_{O(2)}$ Low Output Voltage (active discharge)				
	V_I = + 10 V, $I_{O(2)}$ = – 90 mA		1.3	1.6	V
	V_I = + 10 V, $I_{O(2)}$ = – 10 mA		120	180	mV
$V_{L(reset)}$	Reset Low Output Voltage (V_I = + 10 V, I_{reset} = – 16 mA)		120	400	mV
$V_{H(reset)}$	Reset High Output Voltage (V_I = + 10 V, I_{reset} = 1 mA)	$V_{O(2)}$–1V		$V_{O(2)}$	V
t_{reset}	Reset Pulse Duration (V_I = + 10 V, C_{reset} = 10 nF) – Note 3	4	8	16	ms
KVT	Average Temperature Coefficient of Output Voltage (T_j = 0 °C to – 70 °C)		0.5		mV/°C
θ	Thermal Shut Down Temperature	110			°C
SVR	Supply Voltage Rejection Ratio				
	V_I = + 12 V, ΔV_I = 4 Vpp, I_O = 10 mA, f = 100 Hz		50		dB

Notes : 1. The dropout voltage (input-output voltage difference) is measured when the output voltage has dropped 100 mV from the nominal value obtained at 10 V input voltage.
Dropout voltage is dependent upon load current and junction temperature.
2. $V_{O(1)}$ voltage is measured at 10 V input voltage.
3. t_{reset} (ms) = 0.8 C_{reset} (nF).

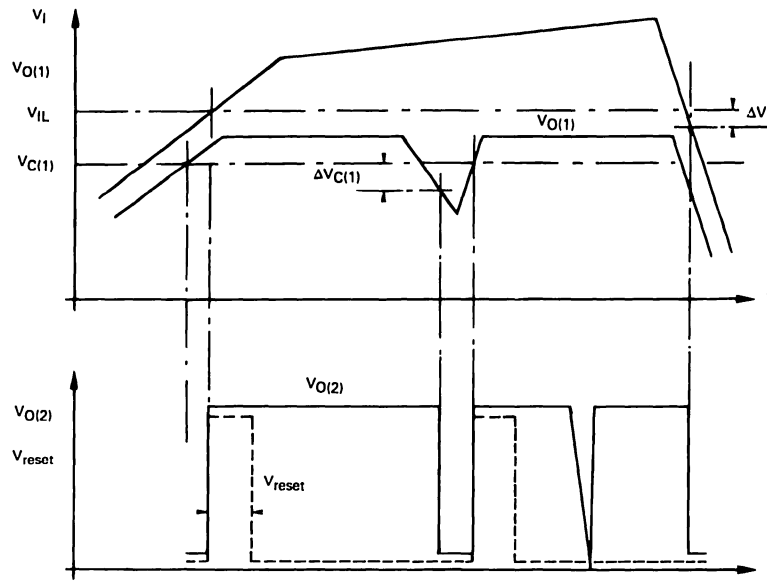
Figure 1 : Typical Application and Test Circuit.



C1, C2, C3 solid tantalum capacitors.
* Required when the circuit is far from power supply capacitors.
** Required for current limitation stability.

E88TEA5110-03

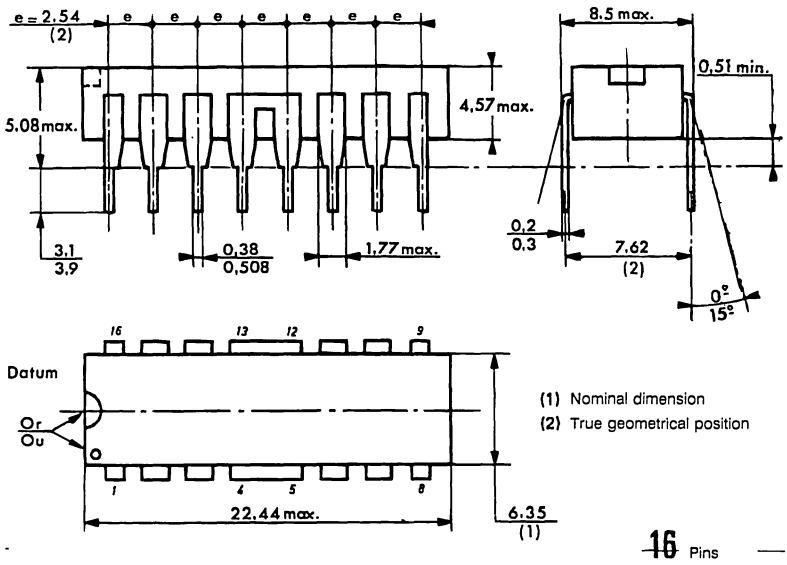
Figure 2 : Dynamic Characteristics of $V_{O(1)}$, $V_{O(2)}$, V_{reset} Outputs.



E88TEA5110-03

PACKAGE MECHANICAL DATA

16 PINS – PLASTIC DIP

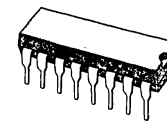


SGS-THOMSON MICROELECTRONICS

TEA7105

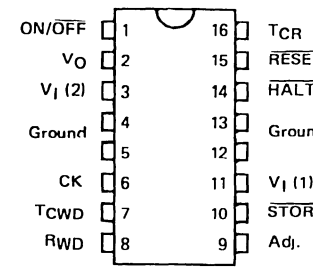
VOLTAGE REGULATOR FOR CMOS MICROPROCESSOR BASED SYSTEMS

- OUTPUT CURRENT : 100 mA
- ON-CHIP CURRENT LIMIT AND THERMAL PROTECTION
- $\overline{\text{RESET}}$ GENERATOR WITH EXTERNALLY ADJUSTABLE DELAY
- REGULATOR INPUT VOLTAGE LEVEL DETECTION SYSTEM (level adjusted externally)
- WATCH DOG TIMER
- INPUT VOLTAGE FAILURE DETECTION SYSTEM DELIVERS A $\overline{\text{STORE}}$ SIGNAL IN CASE OF INPUT VOLTAGE DISCONTINUITY
- REGULATOR ON/$\overline{\text{OFF}}$ CONTROL SIGNAL ALSO SETS THE OUTPUT TO HIGH IMPEDANCE STATE



TEA7105
BATWING DIP-16
(Plastic Package)

PIN CONNECTIONS



E88TEA7105-01

DESCRIPTION

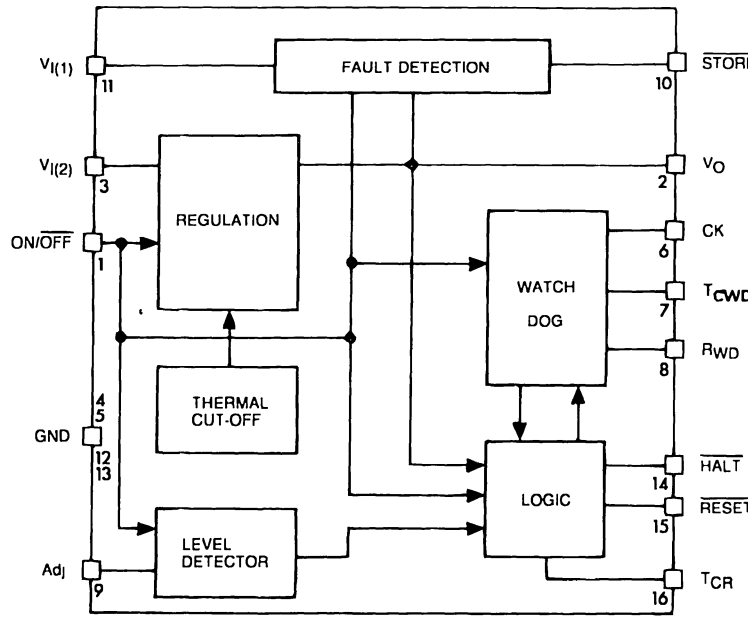
The TEA7105 is a voltage regulator especially suited to all microprocessor-based digital systems. Upon initial power on, the circuit delivers a $\overline{\text{RESET}}$ signal with programmable delay. This signal is disabled under three conditions :

- When supply voltage falls below a certain threshold level adjusted externally
- When output voltage falls below a preset level
- In the absence of trigger pulses on WATCH DOG input

The regulator features a WATCH DOG function with timing requirements met by a wide range of frequencies. The device detects the occurance of input voltage DROP and delivers a $\overline{\text{STORE}}$ signal whitebeing powered by the energy stored in the input capacitor.

An ON/$\overline{\text{OFF}}$ function is provided enabling the circuit to be put in standby mode and also to set the regulated output to high impedance state. In this mode, the power consumption is extremely low.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{I(1)}$. $V_{I(2)}$	Supply Voltage	+ 40	V
	CK Input Voltage	− 0.3 to V_O	V
	ON/$\overline{OFF}$ Input Voltage	− 0.3 to $V_{I(2)}$	V
	Adj. Pin Input Voltage	− 0.3 to $V_{I(2)}$	V
P_{tot}	Power Dissipation	Internally Limited	−
T_{oper}	Operating Ambient Temperature Range	− 40 to + 85	°C
T_{stg}	Storage Temperature Range	− 65 to + 150	°C

THERMAL DATA

$R_{th\ (j\text{-}a)}$	Maximum Junction-ambient Thermal Resistance	45	°C/W
$R_{th\ (j\text{-}c)}$	Maximum Junction-case Thermal Resistance	11	°C/W

$R_{th(j\text{-}a)}$ is measured on packages soldered on a printed circuit board with a copper area of 20 cm^2.

ELECTRICAL CHARACTERISTICS T_{amb} = + 25 °C, $V_{I(1)} = V_{I(2)}$ = + 12 V
(unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VOLTAGE REGULATOR					
V_O	Output Voltage (+ 7 V ≤ V_I ≤ + 36 V, 1 ≤ I_O ≤ 100 mA)	4.85	–	5.15	V
K_{VI}	Line Regulation (+ 7 V ≤ V_I ≤ + 36 V, I_O = 50 mA)	–	30	100	mV
K_{VO}	Load Regulation (V_I = + 10 V, 5 mA < I_O < 100 mA)	–	10	75	mV
I_{SC}	Short-circuit Current (V_I = + 10 V, 0 ≤ V_O ≤ + 5 V)	–	200	–	mA
$\overline{\text{RESET}}$ FUNCTION					
	Minimum Output Voltage to Activate $\overline{\text{RESET}}$	4.5	–	4.8	V
	Output Voltage Hysteresis to Disable $\overline{\text{RESET}}$	–	50	–	mV
$V_{(ref)}$	Internal Reference for the Adj. Detection	–	2.5	–	V
$I_{(adj)}$	Maximum Adj. Pin Current ($V_{(adj)}$ = 0 V)	–	–	1	µA
$V_{L(\overline{reset})}$	Low Level $\overline{\text{RESET}}$ Output (I_O = 2 mA)	–	–	0.4	V
$V_{H(\overline{reset})}$	High Level $\overline{\text{RESET}}$ Output (I_{OH} = – 100 µA)	V_O – 1	–	V_O	V
CK AND ON/$\overline{\text{OFF}}$ INPUTS					
V_{IL}	Maximum Low Level Input Voltage	–	–	0.8	V
I_{IL}	Maximum Low Level Input Current (V_{IL} = 0 V)	– 120	– 60	–	µA
V_{IH}	Minimum High Level Input Voltage	2.4	–	–	V
I_{IH}	Maximum High Level Input Current (V_{IH} = + 2.4 V)	–	–	100	µA
ALARM /$\overline{\text{STORE}}$ FUNCTION					
$V_{H(min)}$	Minimum Input Voltage to Activate $\overline{\text{STORE}}$ Signal	5	5.7	6.4	V
$V_{L(\overline{store})}$	Low Level $\overline{\text{STORE}}$ Output (I_O = 2 mA)	–	–	0.4	V
$V_{H(\overline{store})}$	High Level $\overline{\text{STORE}}$ Output (I_{OH} = – 100 µA)	V_O – 1	–	V_O	V
ON/$\overline{\text{OFF}}$ FUNCTION					
$I_{(sb)}$	Standby Current $V_{(ON/\overline{OFF})}$ = 2.4 V $V_{(ON/\overline{OFF})}$ = 0 V	 – –	 4 0.5	 8 –	mA
$I_{O(dis)}$	V_O Pin Discharge Current ($V_{ON/\overline{OFF}}$ = 0, V_O = + 5 V)	–	–	2	µA

ELECTRICAL CHARACTERISTICS(continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
TIMING (see timing diagrams)					
	CWD	–	–	33	nF
	C_R	–	–	220	nF
t_{init}	t_{init} (C_R = 100 nF) Note 1	–	30	–	ms
t_d	t_d (CWD = 33 nF) Note 2	–	7	–	ms
t_{reset}	t_{reset} (CWD = 33 nF, C_R = 100 nF) Note 3	–	6	–	ms
t_{cycle}	t_{cycle} (CWD = 33 nF, C_R = 100 nF) Note 4	–	13	–	ms
T_{CK}	Pulse Width at Input CK	20	–	t_d	µs

Notes : 1. This is the period at the end of which $\overline{RESET}$ signal appears after V_{OUT} rises up and when switch S1 has been closed, this is given by the following relationship.
$t_{init} = 0.3\ CR \cdot 10^6$.

2. This is the maximal clock period determined by the value of CWD.
$t_d = \frac{2.7}{11.6} \cdot CWD\ 10^6$.

3. This is the time required for microcomputer reinitialisation.
$t_{reset} = \frac{1}{11.6}\ CWD\ 10^6 + \frac{5}{125}\ CR\ 10^6$.

4. This is the time required by the microcomputer during a restart to generate at least one clock pulse.
$t_{cycle} = t_d + t_{reset}$.

Remark : For more important clock period see specific application figure 10.

PIN DESCRIPTION

$V_{I(1)}$

Input connected directly to power supply to detect any supply failure.

$V_{I(2)}$

Regulator's power input. This input is separated from power supply through a diode.

A decoupling capacitor is connected to this input.

An inadequate supply voltage level is detected at this input.

Adj

In order to detect the level of $V_{I(2)}$ a resistance inserted between Adj pin and $V_{I(2)}$ and another between Adj pin and GND are necessary.

ON/$\overline{OFF}$

Logic input. A logic 1 applied to this input will cause the TEA7105 to become fully operational ; whereas a logic O will set the circuit to standby mode.

V_O

Power cutput to microprocessor and digital systems.

Two different output voltage levels are detected according to whether the transition is from low voltage to high voltage or the inverse (Refer to timing diagram - figure 4).

High impedance output when the circuit is in standby mode.

T_{CR}

Combination of a grounded capacitor and the internal current generator will implement the $\overline{RESET}$ signal delay upon the initial power on.

T_{CWD}

A relaxation oscillator is implemented by combining a grounded capacitor and the internal current generator

R_{WD}

A resistance inserted between this pin and ground will cause the flow of additional charging current to capacitor C_{WD} thereby modifying the slope of the local oscillator and improving the choice of C_{WD} values.

C_K

This is the WATCH DOG function input. The clock signal resets the ramp of the relaxation oscillator. The circuit is triggerred on rising edge of the clock.

$\overline{\text{RESET}}$

During the initialization, TEA7105 detects at the output V_O a voltage level V_{C1} and generates a $\overline{\text{RESET}}$ signal (see timing diagrams - figure 5).

The following three conditions cause $\overline{\text{RESET}}$ signal to be forced to zero level :

- If the output voltage level falls below V_{C1} by a hysteresis of ΔV_{C1} (see timing diagrams - figure 5).
- If no signal arrives at input CK for a minimal period to 20 µs and maximal period equal to td (see timing diagrams - figure 6).
- If the input voltage falls below the adjustable threshold level (see timing diagrams - figure 4).

$\overline{\text{HALT}}$

Fonction and electrical characteristics are the same as the $\overline{\text{RESET}}$ pin.

$\overline{\text{STORE}}$

If input voltage $V_{I(1)}$ falls below V_{C2} level, TEA7105 will use the energy stored in the input capacitor to generate the $\overline{\text{STORE}}$ signal for the microprocessor data protection (see timing diagrams - figure 4).

Figure 1 : Maximum Power Dissipation Versus Junction-ambient Temperature.

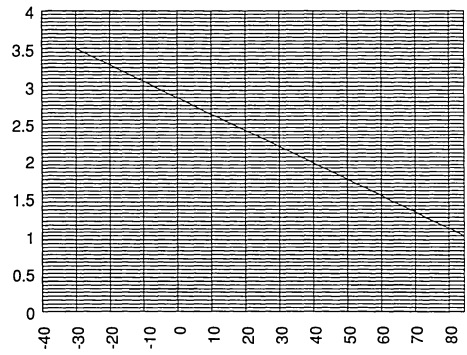
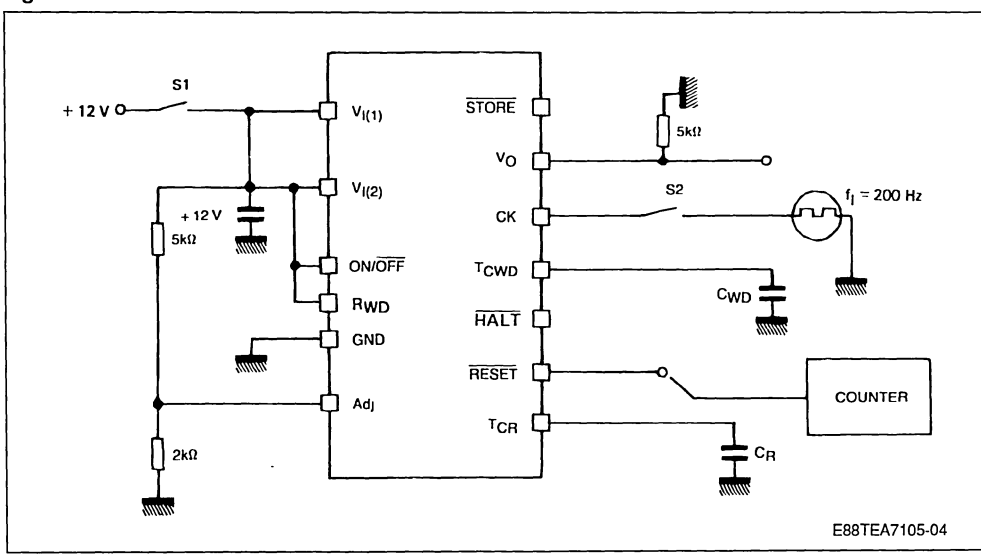


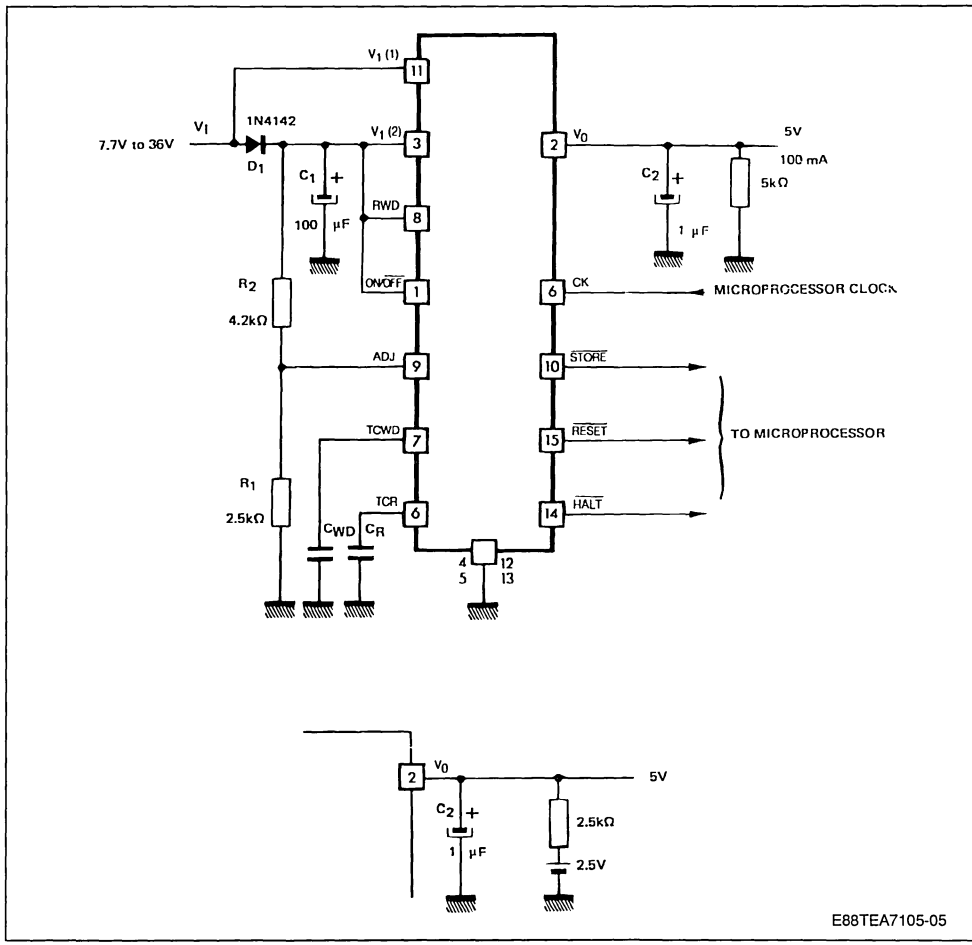
Figure 2 : Test Circuit.



TYPICAL APPLICATION

A minimum current of 1 mA should be delivered by the TEA7105 for effective voltage control. This is why a 5 KΩ resistor (or an equivalent load if a backup battery is used) shall be connected between V_O and the ground.

Figure 3 : Typical Application.



OPERATING PRINCIPLE (see block diagram)

Output V_O(+ 5 V) is supplied by voltage V_I(2) (7 to 36 V).

Input V_I(1) may be used to detect input voltage drop and to generate a STORE signal.

Warning signals $\overline{HALT}$ and $\overline{RESET}$ are generated when :

- the circuit is being powered, for a time t_{init},
- the level detector detects insufficient voltage across power supply V_I(2),
- voltage V_O drops below a given threshold,
- the watch dog detects that pulses are no more generated by the microcomputer when running a program.

The thermal protection device may produce a high impedance at the voltage regulator output.

The impedance of the complete circuit becomes high when $V_I(2)$ drops below a fixed threshold, 4.5 V < V threshold < 4.8 V or by acting on the ON/OFF input.

External capacitors allow inputs t_{CWD} and t_{CR} to define the t_{init}, t_{reset}, t_{cycle}, td times (figures 5 and 7) which are characteristic of the HALT and RESET signals.

It's possible to inhibit the watch dog function by grounding the pin 7 (CWD).

If store function is not used the diode D1 is not accessary.

WHEN POWERING (figures 4,5,6)

Outputs HALT and RESET are (at logic level O) during a time t_{init} following voltage V_O build up, which is used for microcomputer initialization.

t_{init} (ms) = 0.3 CR (nF).

WHEN NO INPUT VOLTAGE IS PRESENT (figure 4)

The TEA7105 regulates the power supply voltage $V_I(1)$. As soon as it drops below $V_I(2)$ diode D1 is blocked. The energy is delivered by capacitor C1 to supply the internal logics of the circuit and the microcomputer.

If $V_I(1)$ drops below a fixed threshold, 5 V < V threshold < 6.4 V, a STORE signal is generated to indicate to the supplied system to save the required data.

If $V_I(2)$ drops below an externally programmed threshold (7 V < V threshold < 36 V).

$V_{threshold} = (2.5\ (R1 + R2)/R1) + V_d$.

Outputs HALT and RESET switch to logic state 0.

If $V_I(2)$ drops below a fixed threshold, 4.5 V < V threshold < 4.8 V, the circuit impedance reaches a high value.

WHEN THE OUTPUT VOLTAGE DROPS (figure 4)

When voltage V_O drops below a fixed threshold, 4.5 V < $V_{threshold}$ < 4.8 V outputs HALT and RESET switch to logic state 0.

WHEN NO CLOCK SIGNAL IS PRESENT (figure 6)

The microcomputer when in operation will generate a clock signal whose period t will be between t min = 20 µs and t max = td

When this signal is not generated, or if the clock period is larger than td, this means that the microcomputer does not operate correctly.

The TEA7105 thus generates the HALT and RESET signals after a time td from the last rising edge.

In this case signals HALT and RESET are activated periodically, t reset and t cycle being fixed by capacitors Cr and CWD.

td may be adjusted by a resistor RWD connected between pin 8 and the ground (figure 9).

In normal condition the maximal clock period is to 7 ms.

It's possible to increase this value in adding some external components (figure 10).

INCREASE OF THE OUTPUT CURRENT (figure 7)

The TEA7105 can deliver a 100 mA current which can be increased by using an external transistor, which maintains the circuit characteristics. The setup illustrated in figure 10 an used in our laboratory circuit gives a 7 mV output variation for a load current varying from 0 to 1A. In this case $V_{threshold} \approx V_S + 3\ V_D + R_S.I_S$. The maximum value of power supply voltage is determined by $V_{min} \approx V_S + 3\ V_D + R_S.I_S$.

OPERATION

For small currents the V_{BE} voltage is lower than 0.6 V ; the transistor is blocked, only the regulator delivers current.

When V_{BE} reaches 0.6 V ($I = V_{BE}/R_b = 0.6/33 =$ 20 mA) the transistor starts conduction. The transistor current gain is high enough to provide a very small current drift of the controller with respect to the load, which improves voltage control.

When short-circuited the current is limited by resistor R_S.

$I_{SC} = (V_I - 2.V_d - Vsat)\ R_S$

CONCLUSION

The TEA7105 is a new generation voltage regulator giving a simple answer to microcomputer power supply problems.

It prevents untimely interruption of microcomputers and makes it possible to return to current program without any trouble.

This regulator may be used in its original version to power a microcomputer or any system with a maximum current requirement of 100 mA. A current extension is available for more powerful systems.

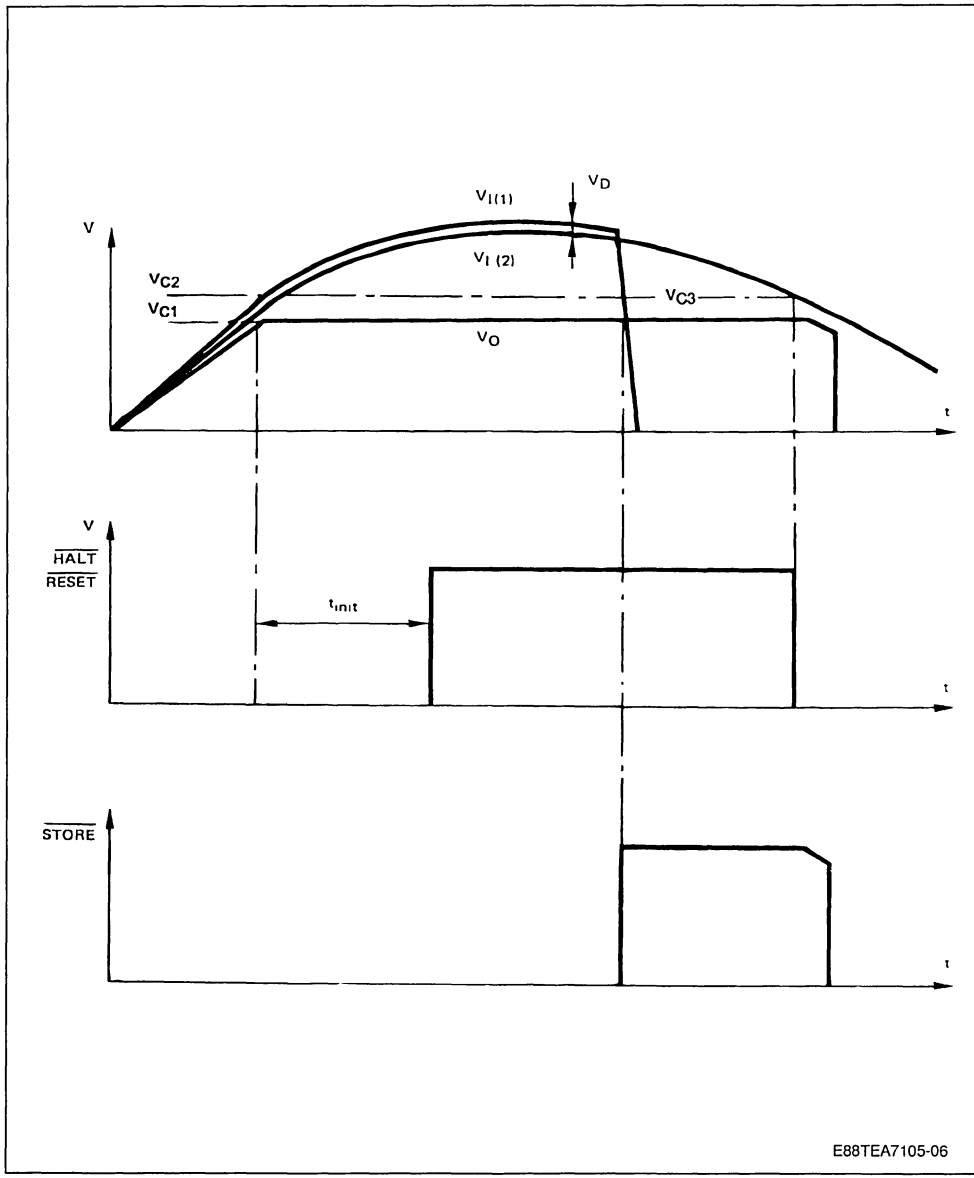
The TEA7105 provides a simple, reliable, economical and high performance power supply.

When V_I (1) becomes lower than a fixed threshold 5V < VC3 < 6.4 the $\overline{STORE}$ output switches to logic state 1. This threshold may be modified by using an external potential divider.

When V_I (2) becomes lower than an externally adjustable threshold signals $\overline{HALT}$ and $\overline{RESET}$ switch to logic state O (V_{C2} = 2.5 (R1 + R2) / R1).

When V_I (2) becomes lower than a fixed threshold 4.5 V < V threshold < 5.5 V the circuit impedance becomes high.

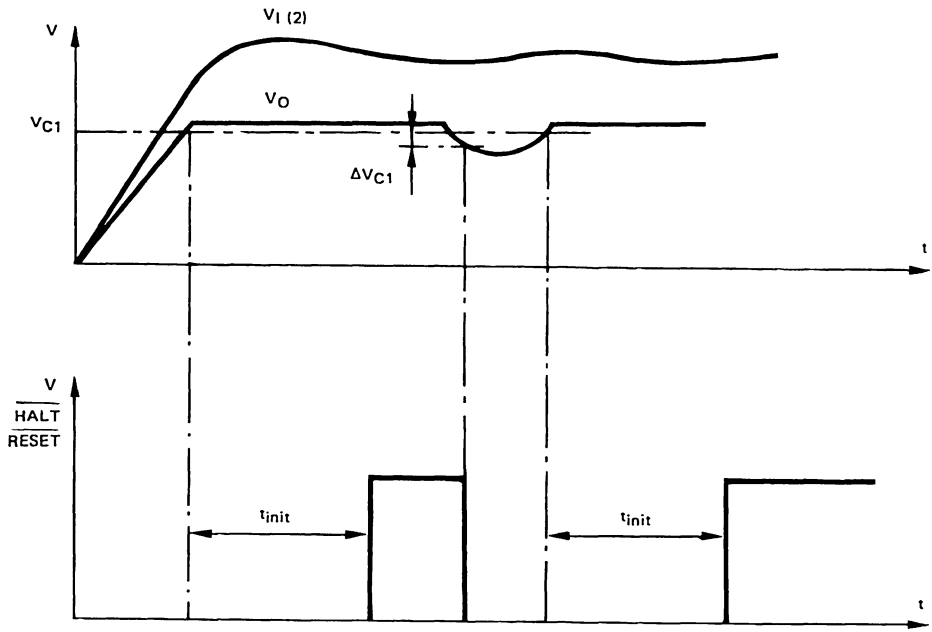
Figure 4 : Detection of Input Voltage Drop.



When the output voltage becomes lower than V threshold (4.5 < threshold < 4.8 V) the warning signals HALT and RESET switch to logic state O.

These signals become active as soon as V_O reaches the threshold to reinitialize and block the microcomputer during t_{init}.

Figure 5 : Detection of Output Voltage Drop.

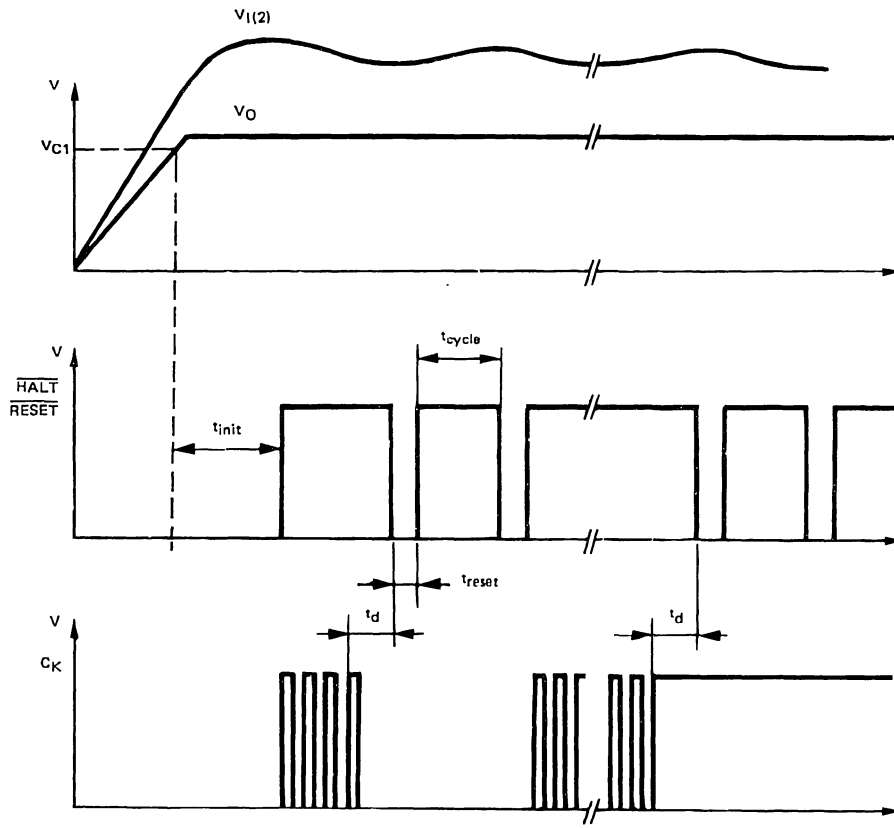


E88TEA7105-07

Signals $\overline{HALT}$ and $\overline{RESET}$ become active after a time t_d from the last clock signal rising edge.

t_d and t_{reset} depend on capacitors C_{WD} and C_R, preset curves are given in figure 8.

Figure 6 : Interruption of Clock Pulses.

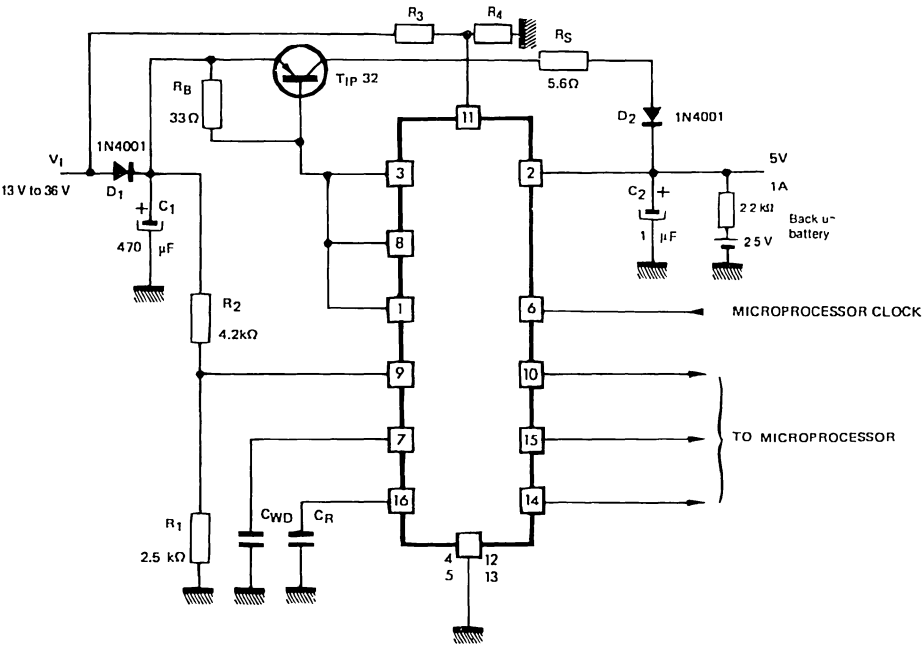


E88TEA7105-08

This application is used to deliver a 1 A current with excellent voltage control. The D2 diode avoids the discharge of the back up battery in the TEA7105 when it' s in hight impedance output in stand by mode.

The value of $V_{I(1)}$ activing $\overline{\text{STORE}}$ signal is determined by ($V_{I(1)}$ store = (5.7 (R3 + R4)/ R4).

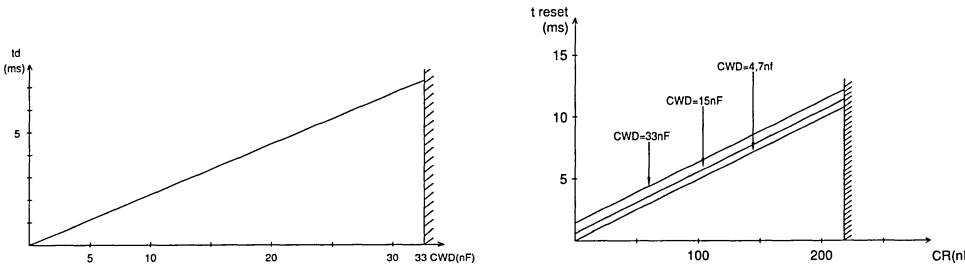
Figure 7 : Current Extension.



E88TEA7105-09

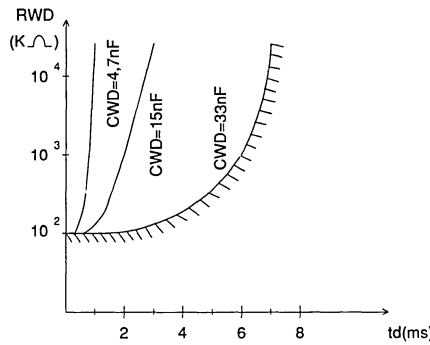
We see that C_r and C_{WD} actions are not fully independent. It is possible to adjust td more finely by using an external resistor connected between pin R_{WD} and the ground (figure 9).

Figure 8 : Determination of t_d and t_{reset} in relation to C_{WD} and C_R.



E88TEA7105-10

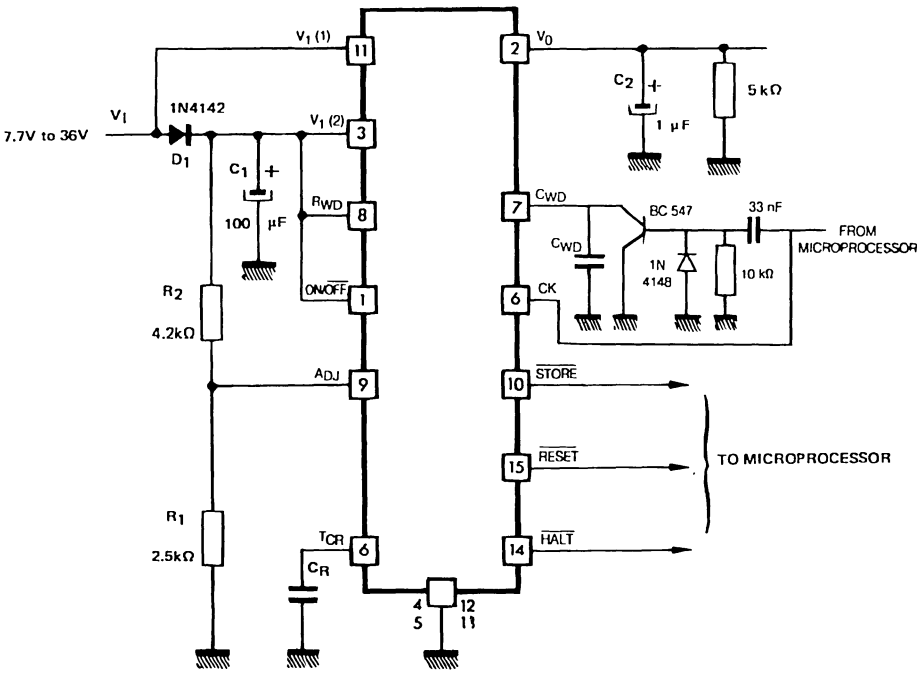
Figure 9 : Determination of t_{CK} max = t_d in relation to R_{WD} and C_{WD}.



E88TEA7105-11

For applications using very long clock period it's possible to use an external transistor. In this case the maximal clock period, in relation to C_{WD}, may be longer than 500 ms. The relationship to define t_{init}, t_d, t_{reset} are same that in typical application.

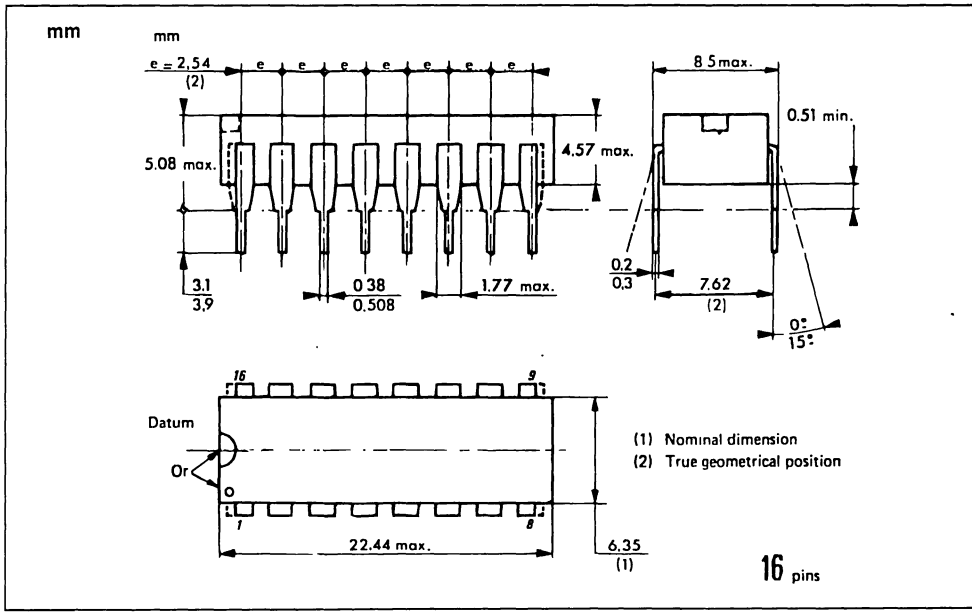
Figure 10 : Very Long Clock Period.



E88TEA7105-12

PACKAGE MECHANICAL DATA

16 PINS – PLASTIC DIP

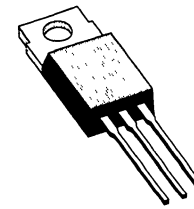


SGS-THOMSON MICROELECTRONICS

TEA7605

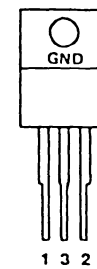
LOW-DROP VOLTAGE REGULATOR

- $V_O = 5\ V \pm 4\ \%$ ($I_O = 5$ mA)
- $I_{OS} \geq 500$ mA
- $V_I - V_O \leq 0.6$ V ($I_O = 500$ mA)
- V_I (surge) = ± 80 V
- THERMAL AND SHORT-CIRCUIT PROTECTION



TEA7605 SP
TO220
(Plastic Package)

PIN CONNECTIONS



E88TEA7605-02

1 = V_I
2 = V_O
3 = GND

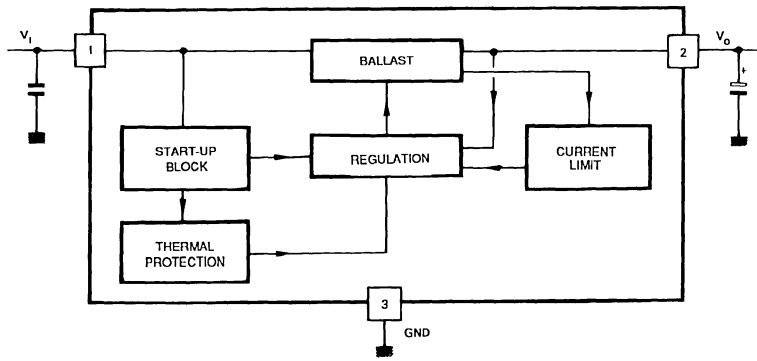
DESCRIPTION

TEA7605 is a low-drop 5 V regulator well suited to supplying stabilized voltage to µPs in harsh industrial environment.

Special care was taken to keep :

- Lowest possible quiescent current (250 µA).
- Lowest possible output capacitor (1 µF).

BLOCK DIAGRAM



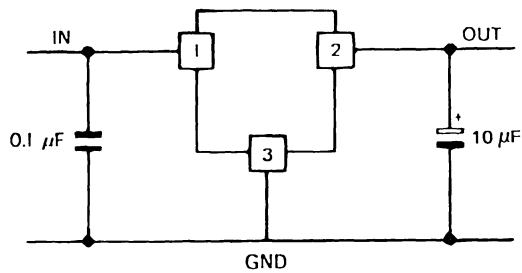
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Input Voltage - Continuous - τ = 300 ms	 30 80	 V V
V_I	Reverse Input Voltage - Continuous - τ = 120 ms	 – 18 – 80	 V V
T_J	Operating Junction Temperature Range	– 45 to 150	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

THERMAL DATA

$R_{th\ (j\text{-}c)}$	Junction-case Thermal Resistance	3	°C/W
$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance	70	°C/W

APPLICATION DIAGRAM



ELECTRICAL OPERATING CHARACTERISTICS

T_j = 25 °C, V_i = 14.4 V (unless otherwise specified) Output Capacitor = 10 µF (see note)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_o	Output Voltage (I_o = 5 to 500 mA)		4.875	5	5.125	V
V_i	Input Supply Voltage (permanent)				28	V
I_{CC}	Current Consumption	I_o = 0 mA I_o = 150 mA I_o = 500 mA		0.25 10 75	0.35 20 100	mA mA mA
kV_i	Line Regulation (V_i = 6 to 26 V ; I_o = 5 mA)			5	10	mV
kV_o	Load Regulation (I_o = 5 to 500 mA)			40	60	mV
V_i - V_o	Drop-out Voltage	I_o = 150 mA I_o = 500 mA		0.18 0.4	 0.6	V V
SVRR	Supply Voltage Rejection (I_o = 350 mA, f = 120 Hz, C_o = 1 µF, V_1 = 12 ± 5 V)			60		dB
I_{os}	Short-circuit Output Current		0.5	0.7		A

NOTE : APPLICATIONS HINTS

The output capacitor has a direct influence on output voltage stability. A 10 µF capacitor will provide satisfactory results ; there is no upper limit.

If necessary, this value can be reduced down to 1 µF ; however, in such case, it should be checked that output capacitor keeps sufficiently high capacitance and low equivalent series resistance in the whole temperature range.

Such low capacitor value is not recommended either, if output current is to switch abruptly from very high to very low values (for instance, 400 mA to < 1 mA).

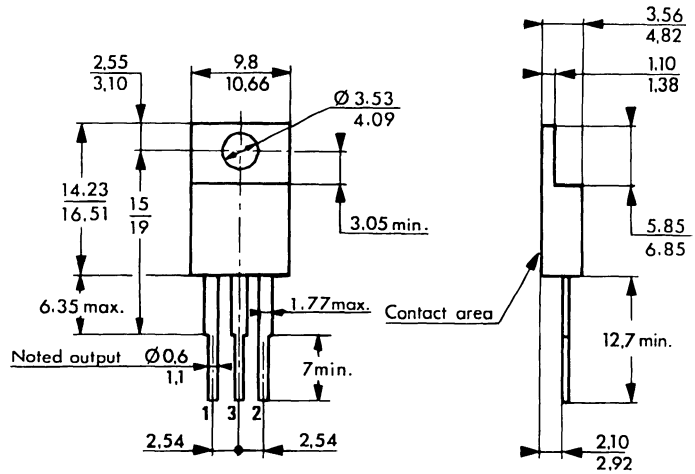
ELECTRICAL OPERATING CHARACTERISTICS

T_j = – 45 °C to + 125 °C, V_i = 14 .4 V (unless otherwise specified) Output Capacitor = 10 µF

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_o	Output Voltage (I_o = 5 to 500 mA)		4.8	5	5.2	V
$\frac{dV_o}{d_t}$	Output Voltage Drift	– 45 to 25 °C 25 to 125 °C	– 0.4 – 0.6			mV/°C
I_{CC}	Current Consumption	I_o = 0 mA I_o = 150 mA I_o = 500 mA			0.4 25 120	mA mA mA
KV_i	Line Regulation	(V_i = 6 to 26 V I_o = 5 mA)			20	mV
KV_o	Load Regulation (I_o = 5 to 500 mA)				80	mV
V_i - V_o	Drop-out Voltage	I_o = 150 mA I_o = 500 mA		0.2	 0.8	V V
I_{os}	Short Circuit Output Current		0.5			A

PACKAGE MECHANICAL DATA

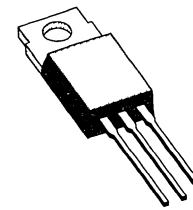
TO220 – PLASTIC PACKAGE



TEA7610

LOW-DROP VOLTAGE REGULATOR

- Vo = 10V ± 4% (Io = 5mA)
- Io = 5 TO 500mA
- Vi - Vo = 0.6V (Io = 500mA)
- Vi (surge) = ± 80V
- THERMAL AND SHORT CIRCUIT PROTECTION



TEA7610 SP
TO220
(Plastic Package)

PIN CONNECTIONS

E88TEA7610-02

1 = V_I
2 = V_O
3 = GND

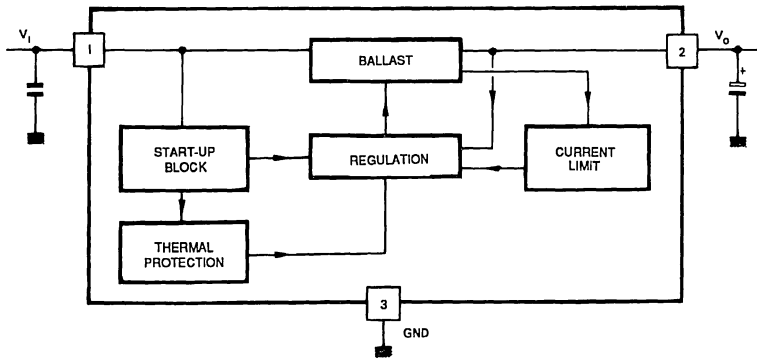
DESCRIPTION

TEA 7610 is a low-drop regulator well suited to supplying stabilized voltage to µPs in harsh industrial environment.

Special care was taken to keep :

- Lowest possible output capacitor (1µF).

BLOCK DIAGRAM



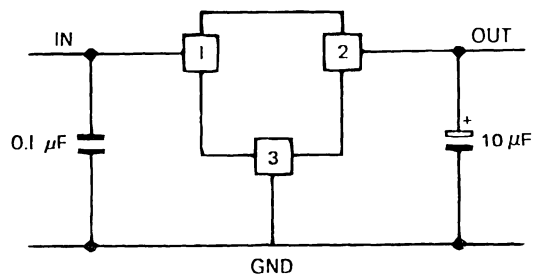
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Input Voltage - Continuous - τ = 300mS	30 80	V V
V_i	Reverse Input Voltage - Continuous - τ = 120mS	– 18 – 80	V V
T_{oper}	Operating Junction Temperature	45 to 150	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

THERMAL DATA

$R_{th\ (j\text{-}c)}$ $R_{th\ (j\text{-}a)}$	Maximum Junction-case Thermal Resistance Maximum Junction-ambient Thermal Resistance	3 70	°C/W °C/W

APPLICATION DIAGRAM



ELECTRICAL OPERATING CHARACTERISTICS

T_j = 25°C, V_i = 14.4V (unless otherwise specified), Output Capacitor = 10µF (note)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_o	Output Voltage (I_o = 5 to 500mA)	9.7	10	10.3	V
V_i	Input Supply Voltage (permanent)			28	V
I_{CC}	Current Consumption I_o = 0mA I_o = 150mA I_o = 500mA		1.5 10 75	2 20 100	mA mA mA
kV_i	Line Regulation (V_i = 6 to 26V ; I_o = 5mA)		5	20	mV
kV_o	Load Regulation (I_o = 5 to 500mA)		40	80	mV
V_i - V_o	Drop-out Voltage I_o = 150mA I_o = 500mA		0.18 0.4	 0.6	V V
SVRR	Supply Voltage Rejection (I_o = 350mA, f = 120Hz, C_o = 1µF, V_i = 12 ± 5V)		60		dB
I_{os}	Short-circuit Output Current	0.5	0.7		A

NOTE : APPLICATION HINTS

The output capacitor has a direct influence on ouptut voltage stability. A 10µF capacitor will provide satisfactory results ; there is no upper limit.

If necessary, this value can be reduced down to 1µF ; however, in such case, it should be checked that output capacitor keeps sufficiently high capacitance and low equivalent series resistance in the whole temperature range.

Such low capacitor value is not recommended either, if output current is to switch abruptly from very high to very low values (for instance 400mA to < 1mA).

ELECTRICAL OPERATING CHARACTERISTICS

T_j = – 45°C to 125°C, V_i = 14.4V (unless otherwise specified), Output Capacitor = 10µF

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_o	Output Voltage (I_o = 5 to 500mA)	9.6	10	10.4	V
d_{Vo} d_t	Output Voltage Drift – 45 to 25°C 25 to 125°C	– 1 – 1.2		0 0	mV/°C
I_{CC}	Current Consumption I_o = 0mA I_o = 150mA I_o = 500mA			2.5 25 120	mA mA mA
kV_i	Line Regulation (V_i = 6 to 26V ; I_o = 5mA)			30	mV
kV_o	Load Regulation (I_o = 5 to 500mA)			100	mV
V_i - V_o	Drop-out Voltage I_o = 150mA I_o = 500mA		0.20	 0.8	V V
I_{os}	Short-circuit Output Current	0.5			A

PACKAGE MECHANICAL DATA

TO220 – PLASTIC PACKAGE

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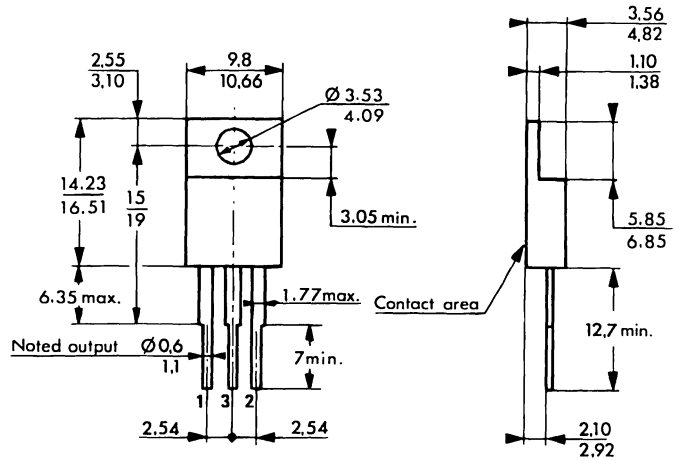
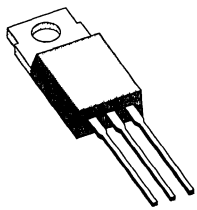


3 Pins

TEA7685

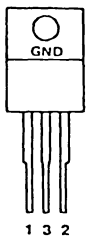
LOW-DROP VOLTAGE REGULATOR

- Vo = 8.5V ± 4% (Io = 5mA)
- Io = 5 TO 500mA
- Vi - Vo = 0.6V (Io = 500mA)
- Vi (surge) = ± 80V
- THERMAL AND SHORT CIRCUIT PROTECTION



TEA7685
TO220
(Plastic Package)

PIN CONNECTIONS



E88TEA7685-02

1 = V_I
2 = V_O
3 = GND

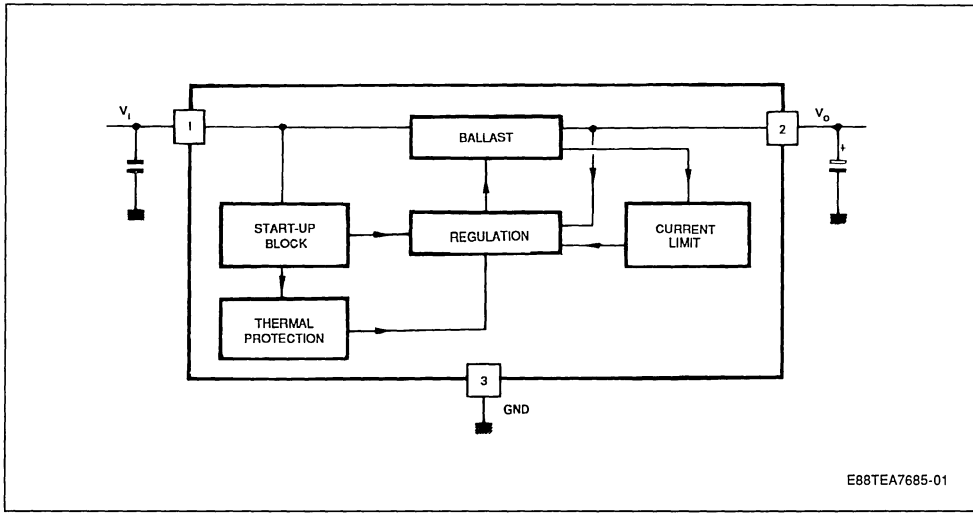
DESCRIPTION

TEA 7685 is a low-drop 8.5V regulator well suited to supplying stabilized voltage to µPs in harsh industrial environment.

Special care was taken to keep :

- Lowest possible output capacitor (1µF).

BLOCK DIAGRAM



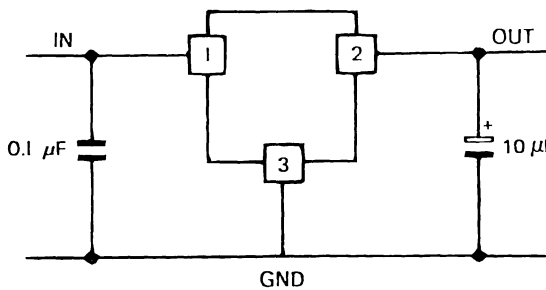
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	Input Voltage - Continuous - τ = 300mS	30 80	V V
V_i	Reverse Input Voltage - Continuous - τ = 120mS	– 18 – 80	V V
T_{oper}	Operating Junction Temperature	45 to + 150	°C
T_{stg}	Storage Temperature	– 55 to + 150	°C

THERMAL DATA

$R_{th(j-c)}$	Maximum Junction-case Thermal Resistance	3	°C/W
$R_{th(j-a)}$	Maximum Junction-ambient Thermal Resistance	70	°C/W

APPLICATION DIAGRAM



ELECTRICAL OPERATING CHARACTERISTICS

T_j = 25°C, V_I = 14.4V (unless otherwise specified) Output Capacitor = 10µF (note)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_o	Output Voltage (I_o = 5 to 500mA)	8.26	8.5	8.74	V
V_I	Input Supply Voltage (permanent)			28	V
I_{CC}	Current Consumption I_o = 0mA I_o = 150mA I_o = 500mA		1.5 10 75	2 20 100	mA mA mA
kV_I	Line Regulation (V_I = 6 to 26V ; I_o = 5mA)	– 15	5	15	mV
kV_o	Load Regulation (I_o = 5 to 500mA)	– 70	– 40	70	mV
V_I - V_o	Drop-out Voltage I_o = 150mA I_o = 500mA		0.18 0.4	 0.6	V V
SVRR	Supply Voltage Rejection (I_o = 350mA, f = 120Hz, C_o = 1µF, V_1 = 12 ± 5V)		60		dB
I_{os}	Short-circuit Output Current	0.5	0.7		A

NOTE : APPLICATION HINTS

The output capacitor has a direct influence on ouptut voltage stability. A 10µF capacittor will provide satisfactory results : there is no upper limit.

If necessary, this value can be reduced down to 1µF ; however, in such case, it should be checked that output capacitor keeps sufficiently high capacitance and low equivalent series resistance in the whole temperature range.

Such low capacitor value is not recommended either, if output current is to switch abruptly from very high to very low values (for instance 400mA to < 1mA).

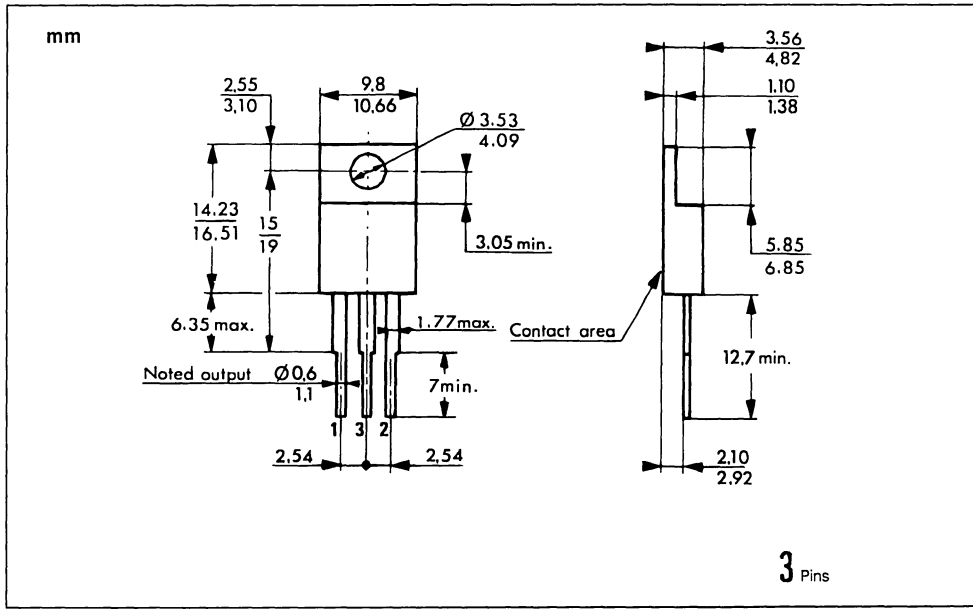
ELECTRICAL OPERATING CHARACTERISTICS

T_j = – 45°C to + 125°C, V_I = 14.4V (unless otherwise specified) Output Capacitor = 10µF

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_o	Output Voltage (I_o = 5 to 500mA)	8.16	8.5	8.84	V
$\frac{dV_o}{dt}$	Output Voltage Drift – 45 to 25°C 25 to 125°C	– 1 – 1.2		0 0	mV/°C
I_{CC}	Current Consumption I_o = 0mA I_o = 150mA I_o = 500mA			2.5 25 120	mA mA mA
kV_I	Line Regulation (V_I = 6 to 26V ; I_o = 5mA)	– 25		25	mV
kV_o	Load Regulation (I_o = 5 to 500mA)	– 90		90	mV
V_I - V_o	Drop-out Voltage I_o = 150mA I_o = 500mA		0.20	 0.8	V V
I_{os}	Short-circuit Output Current	0.5			A

PACKAGE MECHANICAL DATA

TO220 – PLASTIC PACKAGE

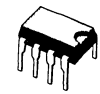


SGS-THOMSON MICROELECTRONICS

TEB1033
TEF1033 - TEC1033

BIPOLAR DUAL OPERATIONAL AMPLIFIERS

- LOW DISTORTION RATIO
- LOW NOISE
- VERY LOW SUPPLY CURRENT
- LOW INPUT OFFSET CURRENT
- VERY LOW INPUT OFFSET VOLTAGE
- LARGE COMMON-MODE RANGE
- HIGH GAIN
- HIGH OUTPUT CURRENT
- GAIN-BANDWIDTH PRODUCT : 2.5 MHz
- TEMPERATURE DRIFT : 2 µV/°C
- LONG TERM STABILITY : 8 µV/YEAR (for $T_{amb} \leq 50$ °C)
- THE TEB1033 AND TEF1033 ARE PIN TO PIN REPLACEMENT OF THE LS204C AND LS204 RESPECTIVELY



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

GC
LCC20
(Tricecop (LCC))

DESCRIPTION

The TEB1033, TEF1033 and TEC1033 are high performance dual-operational amplifiers intended for active filter applications. The internal phase compensation allows stable operation as voltage follower in spite of their high gain-bandwidth products.

The circuits present very stable electrical characteristics over the entire supply voltage range.

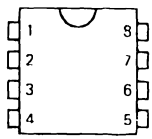
ORDER CODES

Part Number	Temperature Range	Package		
		N	D	GC
TEB1033	0 °C to + 70 °C	•	•	
TEF1033	– 40 °C to + 105 °C	•	•	
TEC1033	– 55 °C to + 125 °C			•

Examples : TEB1033N, TEC1033GC

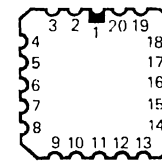
PIN CONNECTIONS (top views)

DIP8/SO8



1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

LCC20

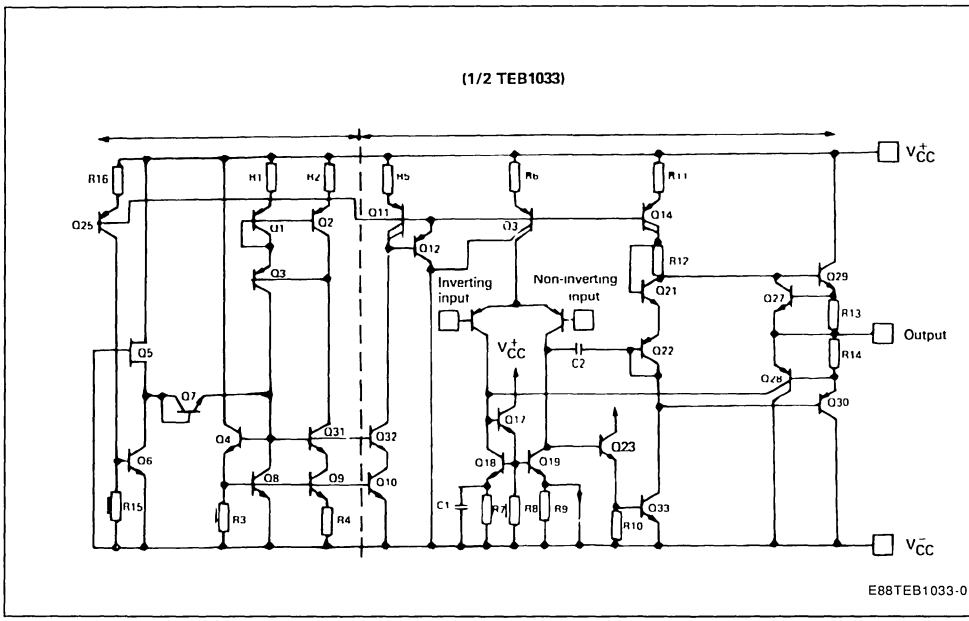


1 - NC
2 - Output 1
3 - NC
4 - NC
5 - Inverting input 1
6 - NC
7 - Non-inverting input 1
8 - NC
9 - NC
10 - V_{CC}^-
11 - NC
12 - Non-Inverting input 2
13 - NC
14 - NC
15 - Inverting Input 2
16 - NC
17 - Output 2
18 - NC
19 - NC
20 - V_{CC}^+

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		± 18	V
V_I	Input Voltage		± V_{CC}	V
V_{ID}	Differential Input Voltage		± (V_{CC} –1)	V
P_{tot}	Power Dissipation			mW
		TEB1033D, TEF1033D	400	
		TEB1033N	665	
		TEC1033GC	665	
T_{oper}	Operating Free-air Temperature Range			°C
		TEB1033	0 to + 70	
		TEF1033	– 40 to + 105	
		TEC1033	– 55 to + 125	
T_{stg}	Storage Temperature Range		– 55 to + 150	°C

BLOCK DIAGRAM



Case	Outputs	Inverting Inputs	Non-inverting Inputs	V_{CC}^+	V_{CC}^-	N. C.
DIP8 SO8	1, 7	2, 6	3, 5	8	4	
LCC20	2, 17	5, 15	7, 12	20	10	*

* **LCC20 :** Other pins are not connected.

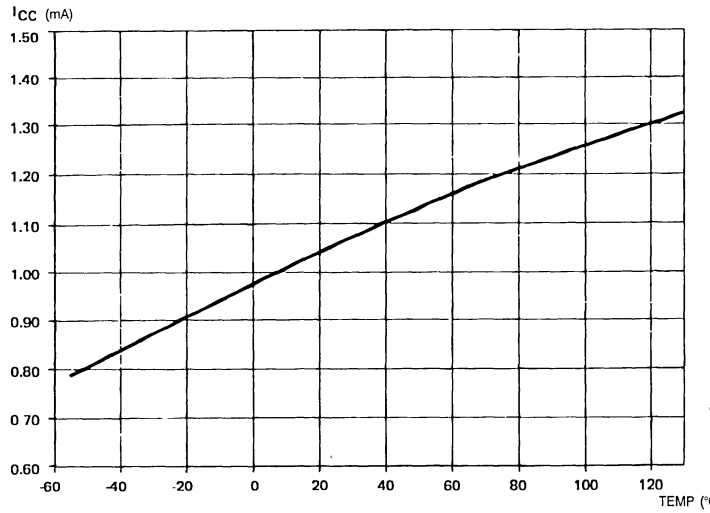
ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 15$ V (unless otherwise specified)
TEC 1033 : $-55 \leq T_{amb} \leq +125$ °C
TEF 1033 : $-40 \leq T_{amb} \leq +105$ °C
TEB 1033 : $0 \leq T_{amb} \leq +70$ °C

Symbol	Parameter	TEB 1033 TEF 1033 TEC 1033			Unit
		Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage T_{amb} = 25 °C (RS ≤ 10 kΩ) $T_{min} \leq T_{amb} \leq T_{max}$		0.3	1 3	mV
DV_{IO}	Input Offset Voltage Drift		2		µV/°C
I_{IO}	Input Offset Current T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		5	20 40	nA
I_{IB}	Input Bias Current T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		50	100 200	nA
A_{vd}	Large Signal Voltage Gain (R_L = 2 kΩ, $V_O = \pm 10$ V) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 100 100	300		V/mV
SVR	Supply Voltage Rejection Ratio DV_{CC} from ± 15 V to ± 4 V T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 100 100	110		dB
I_{CC}	Supply Current, all Amp, no Load T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		1	1.5 2	mA
V_I	Input Voltage Range T_{amb} = 25 °C	− 12		+ 12	V
CMR	Common Mode Rejection Ratio ($R_S \leq 10$ kΩ, $V_I = \pm 10$ V) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 100 100	110		dB
I_{os}	Output Short-circuit Current T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 10 10	23	40 40	mA
$\pm V_{opp}$	Output Voltage Swing T_{amb} = 25 ° C R_L = 2 kΩ $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 2 kΩ $V_{CC} = \pm 4$ V, R_L = 2 KΩ $V_{CC} = \pm 6$ V, R_L = 600 Ω	 13 12 2.8 4.6	 14 3		V
S_{vo}	Slew-rate ($V_I = \pm 10$ V, R_L = 2 kΩ, $C_L \leq 100$ pF, T_{amb} = 25 °C, unity gain)	0.6	1	3	V/µs
GBP	Gain Bandwidth Product (f = 100 KHz, T_{amb} = 25 °C, V_{IN} = 10 mV, R_L = 2 kΩ, C_L = 100 pF)	1.8	2.5	3.2	MHz
R_I	Input Resistance (T_{amb} = 25 °C)		1		MΩ

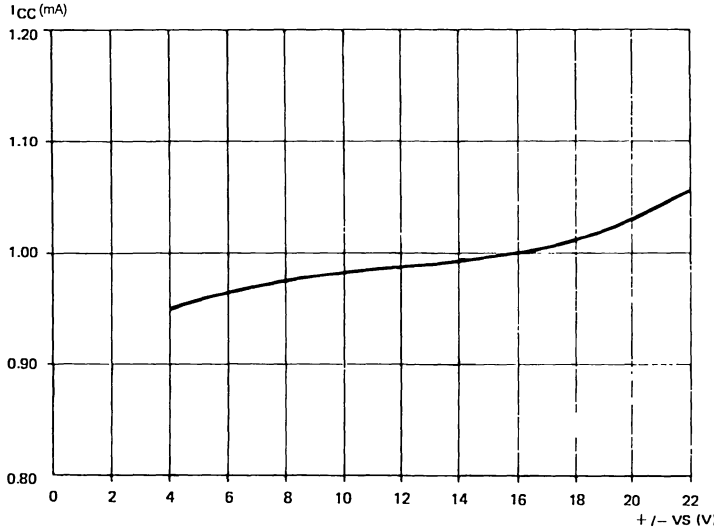
ELECTRICAL CHARACTERISTICS(continued)

Symbol	Parameter	TEB 1033 TEF 1033 TEC 1033			Unit
		Min.	Typ.	Max.	
THD	Total Harmonic Distortion (f = 1KHz, A_v = 20 dB, R_L = 2 kΩ $C_L \leq$ 100 pF, T_{amb} = 25 °C, V_o = 2 V_{pp})		0.008	0.05	%
V_n	Equivalent Input Noise Voltage (f = 1 KHz) R_S = 50 Ω R_S = 1 kΩ R_S = 10 kΩ		 8 10 18	 15	 nV/√Hz
V_{OPP}	Large Signal Voltage Swing R_L =10 kΩ, f = 10 KHz	26	28		V
φM	Phase Margin		45		Degrees
V_{o1}/V_{o2}	Channel Separation	100	120		dB



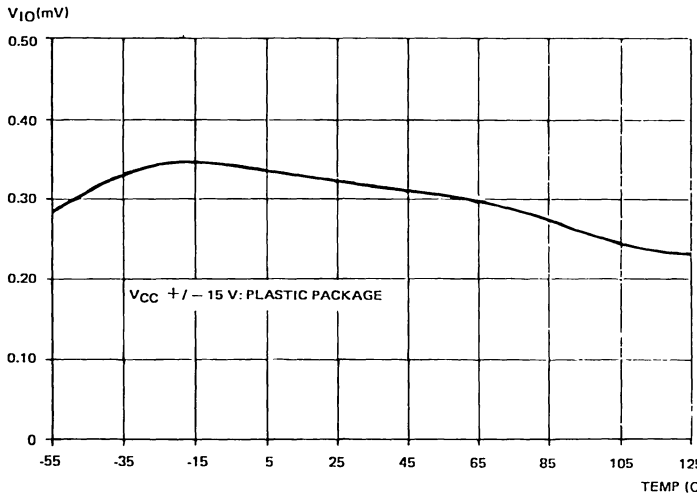
SUPPLY CURRENT VS. AMBIENT TEMPERATURE

E88TEB1033-02



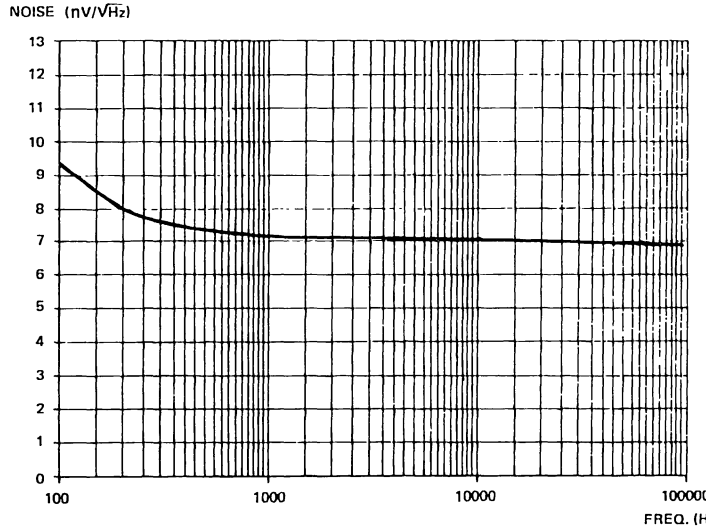
SUPPLY CURRENT VS. SUPPLY VOLTAGE

E88TEB1033-03



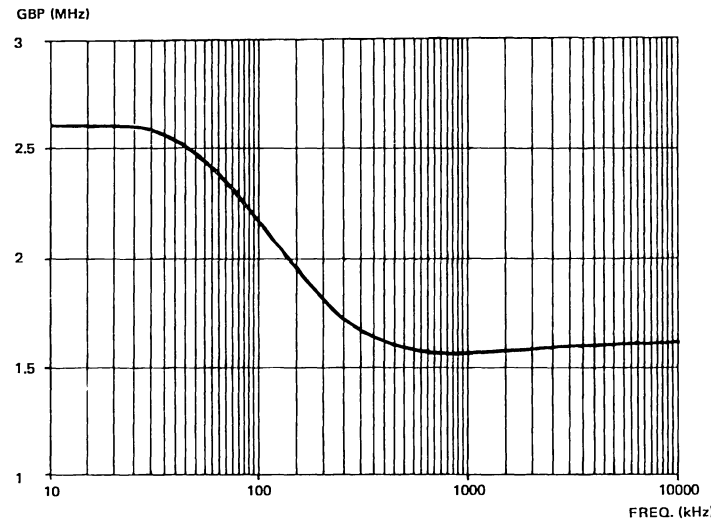
OFFSET VOLTAGE VS. AMBIENT TEMPERATURE

E88TEB1033-04



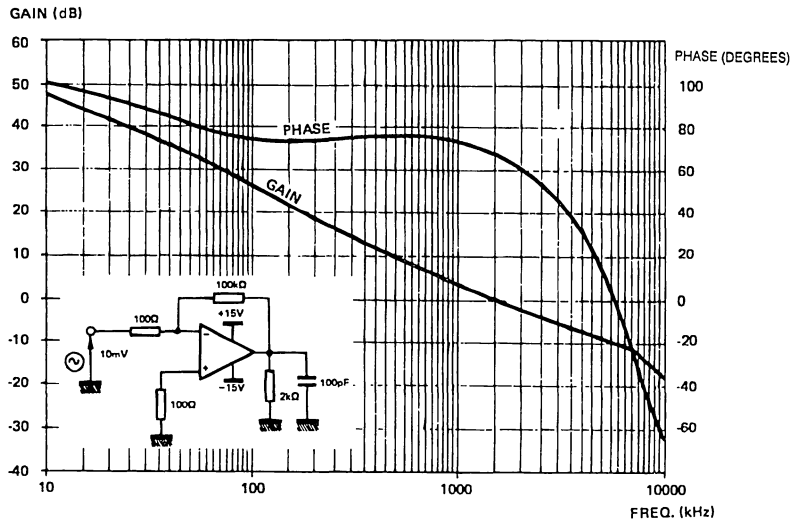
TOTAL INPUT NOISE VS. FREQUENCY

E88TEB1033-05



GAIN BANDWIDTH PRODUCT VS. FREQUENCY

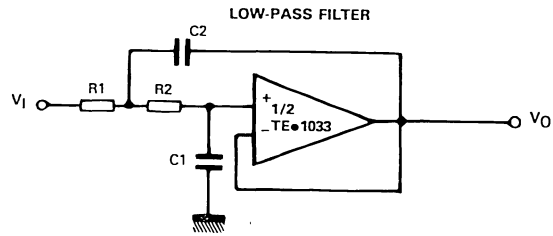
E88TEB1033-06



BODE PLOT

E88TEB1033-07

TYPICAL APPLICATION



E88TEB1033-08

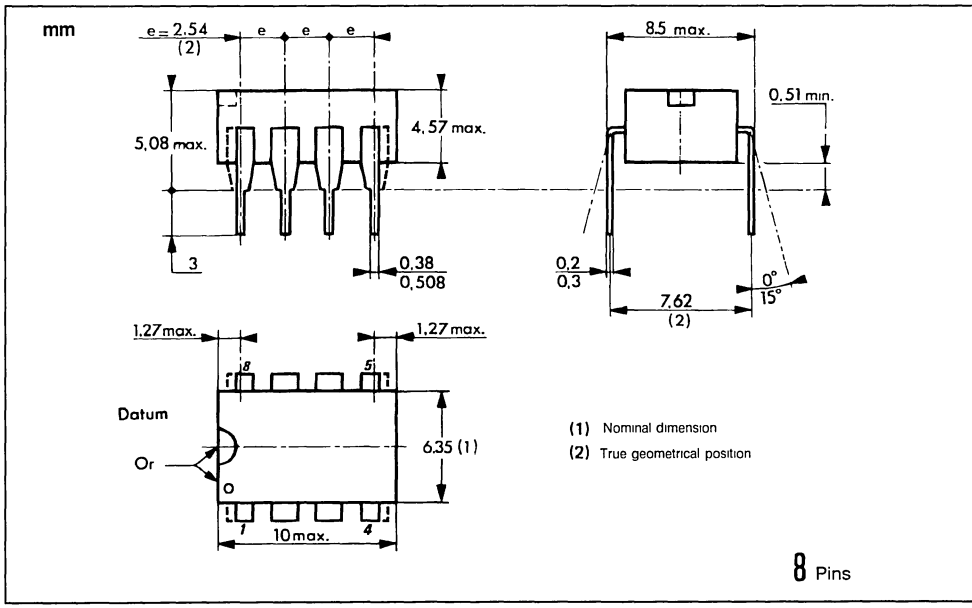
$$\frac{V_o}{V_i} = \frac{1}{1 + 2\xi \frac{S}{\omega_c} + \frac{S^2}{\omega_c^2}}$$

$\omega_c = 2\pi f_c$, with f_c = cutt-off frequency

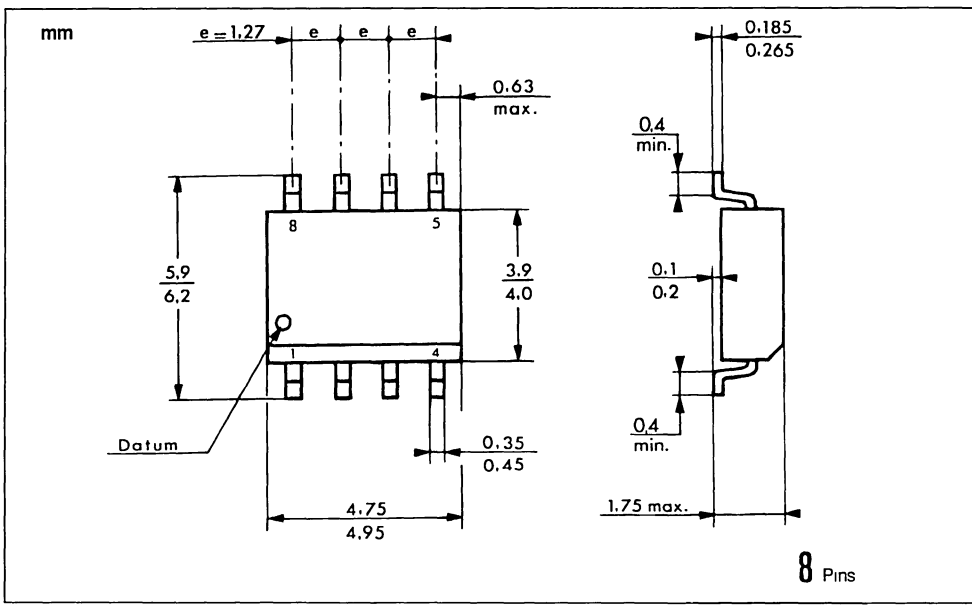
ξ = damping factor

PACKAGE MECHANICAL DATA

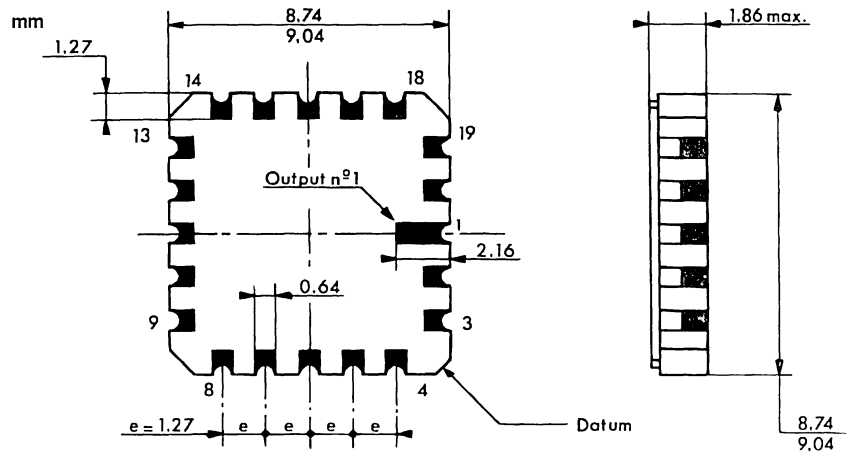
8 PINS – PLASTIC DIP



8 PINS – PLASTIC MICROPACKAGE (SO)



20 PINS – TRICECOP (LCC)

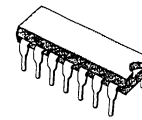


SGS-THOMSON MICROELECTRONICS

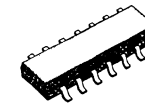
TEB4033
TEF4033 - TEC4033

BIPOLAR QUAD OPERATIONAL AMPLIFIERS

- LOW DISTORTION RATIO
- LOW NOISE
- VERY LOW SUPPLY CURRENT
- LOW INPUT OFFSET CURRENT
- VERY LOW INPUT OFFSET VOLTAGE
- LARGE COMMON-MODE RANGE
- HIGH GAIN
- HIGH OUTPUT CURRENT
- GAIN-BANDWIDTH PRODUCT : 2.5 MHz
- TEMPERATURE DRIFT : 2 µV/°C
- LONG TERM STABILITY : 8 µV/YEAR (for $T_{amb} \leq 50$ °C)
- THE TEB4033 AND TEF4033 ARE PIN TO PIN REPLACEMENT OF THE LS404C AND LS404 RESPECTIVELY



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

J
CERDIP14
(Cerdip Package)

GC
LCC20
(Tricecop (LCC))

DESCRIPTION

The TEB4033, TEF4033 and TEC4033 are high performance quad-operational amplifiers intended for active filter applications. The internal phase compensation allows stable operation as voltage follower in spite of their high gain-bandwidth products.

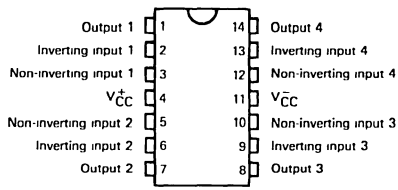
The circuits present very stable electrical characteristics over the entire supply voltage range.

ORDER CODES

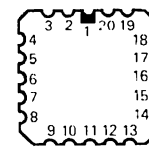
Part Number	Temperature Range	Package		
		N	D	GC
TEB4033	0 °C to + 70 °C	•	•	
TEF4033	– 40 °C to + 105 °C	•	•	
TEC4033	– 55 °C to + 125 °C			•
Examples : TEB4033N, TEC4033GC				

PIN CONNECTIONS (top views)

DIP14/CERDIP14
SO14



LCC20

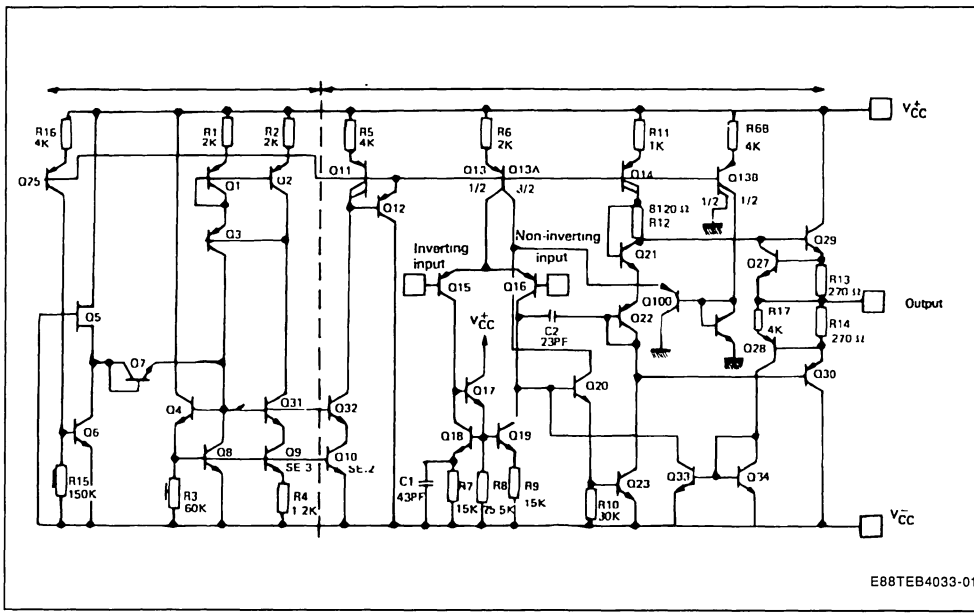


1 - NC
2 - Output 1
3 - Inverting input 1
4 - Non-inverting input 1
5 - NC
6 - V_{cc}^{+}
7 - NC
8 - Non-inverting input 2
9 - Inverting input 2
10 - Output 2
11 - NC
12 - Output 3
13 - Inverting input 3
14 - Non-inverting input 3
15 - NC
16 - V_{cc}^{-}
17 - NC
18 - Non-inverting input 4
19 - Inverting input 4
20 - Output 4

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	± 18	V
V_I	Input Voltage	± V_{CC}	V
V_{ID}	Differential Input Voltage	± (V_{CC} –1)	V
P_{tot}	Power Dissipation TEB4033D, TEF4033D TEB4033N, TEF4033N TEC4033GC	 400 665 665	mW
T_{oper}	Operating Free-air Temperature Range TEB4033 TEF4033 TEC4033	 0 to + 70 – 40 to + 105 – 55 to + 125	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

BLOCK DIAGRAM



Case	Outputs	Inverting Inputs	Non-inverting Inputs	V_{CC}^+	V_{CC}^-	N. C.
DIP14 CERDIP14 SO14	1, 7 8, 14	2, 6 9, 13	3, 5 10, 12	4	11	
LCC20	2, 10 12, 20	3, 9 13, 19	4, 8 14, 18	6	16	*

* **LCC20** : Other pins are not connected.

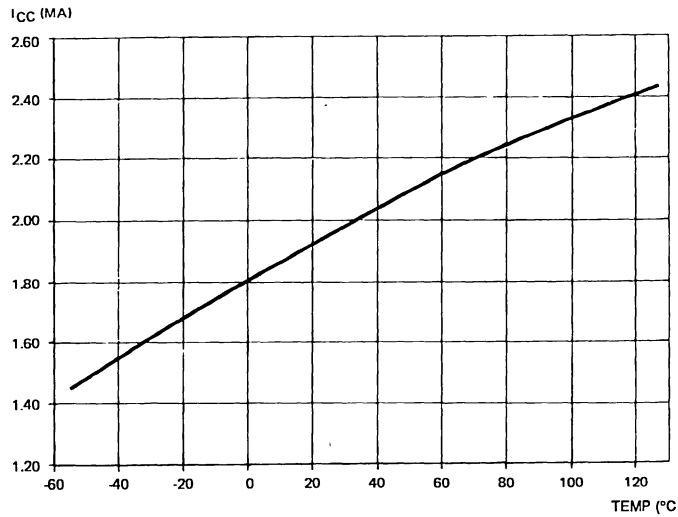
ELECTRICAL CHARACTERISTICS

V_{CC} = ± 15 V (unless otherwise specified)
TEC 4033 : $-55 \leq T_{amb} \leq +125$ °C
TEF 4033 : $-40 \leq T_{amb} \leq +105$ °C
TEB 4033 : $0 \leq T_{amb} \leq +70$ °C

Symbol	Parameter	TEB 4033 TEF 4033 TEC 4033			Unit
		Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage T_{amb} = 25 °C ($R_S \leq 10$ kΩ) $T_{min} \leq T_{amb} \leq T_{max}$		0.3	1 3	mV
DV_{IO}	Input Offset Voltage Drift		2		µV/°C
I_{IO}	Input Offset Current T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		5	20 40	nA
I_{IB}	Input Bias Current T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		50	100 200	nA
A_{vd}	Large Signal Voltage Gain (R_L = 2 kΩ, V_O = ± 10 V) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 100 100	300		V/mV
SVR	Supply Voltage Rejection Ratio DV_{CC} from ± 15 V to ± 4 V T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 100 100	110		dB
I_{CC}	Supply Current, all Amp, no Load T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		2	3 4	mA
V_I	Input Voltage Range T_{amb} = 25 °C	− 12		+ 12	V
CMR	Common Mode Rejection Ratio ($R_S \leq 10$ kΩ, V_I = ± 10 V) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 100 100	110		dB
Ios	Output Short-circuit Current T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	10 10	23	40 40	mA
± V_{opp}	Output Voltage Swing T_{amb} = 25 ° C R_L = 2 kΩ $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 2 kΩ V_{CC} = ± 4 V, R_L = 2 kΩ V_{CC} = ± 6 V, R_L = 600 Ω	13 12 2.8 4.6	14 3 		V
S_{vo}	Slew-rate (V_I = ± 10 V, R_L = 2 kΩ $C_L \leq 100$ pF, T_{amb} = 25°C, unity gain)	0.6	1	3	V/µs
GBP	Gain Bandwidth Product (f = 100 KHz, T_{amb} = 25 °C, V_{IN} = 10 mV, R_L = 2 kΩ, C_L = 100 pF)	1.8	2.5	3.2	MHz
R_I	Input Resistance (T_{amb} = 25 °C)		1		MΩ

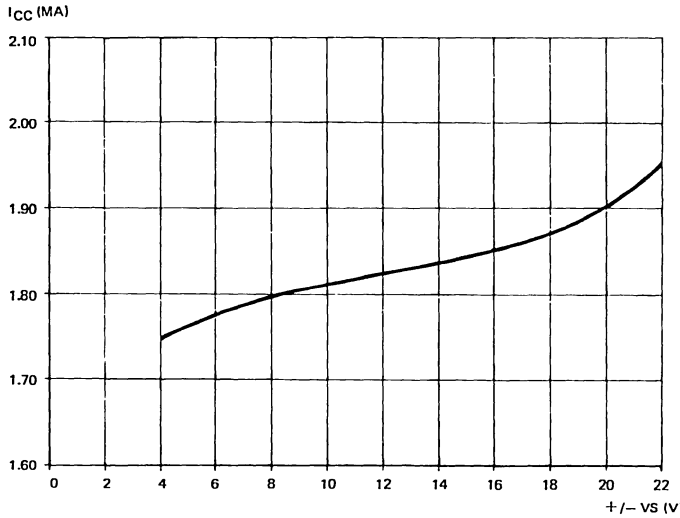
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	TEB 4033 TEF 4033 TEC 4033			Unit
		Min.	Typ.	Max.	
THD	Total Harmonic Distortion (f = 1KHz, A_v = 20 dB, R_L = 2 kΩ $C_L \leq$ 100 pF, T_{amb} = 25 °C, V_o = 2 V_{pp})		0.008	0.05	%
V_n	Equivalent Input Noise Voltage (f = 1 KHz) R_S = 50 Ω R_S = 1 kΩ R_S = 10 kΩ		 8 10 18	 15	 nV/√Hz
V_{OPP}	Large Signal Voltage Swing R_L = 10 kΩ, f = 10 KHz	26	28		V
φM	Phase Margin		45		Degrees
V_{o1}/V_{o2}	Channel Separation	100	120		dB



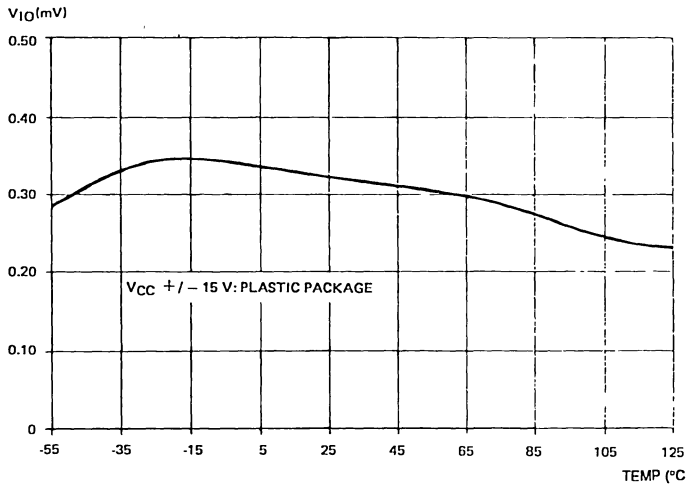
SUPPLY CURRENT VS. AMBIENT TEMPERATURE

E88TEB4033-02



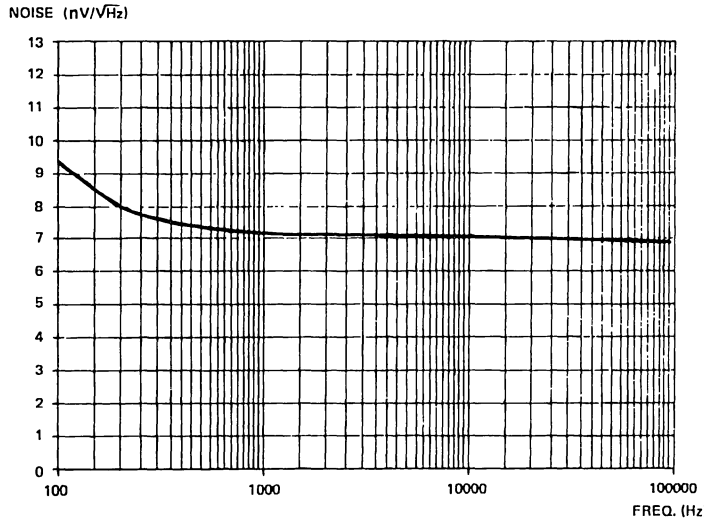
SUPPLY CURRENT VS. SUPPLY VOLTAGE

E88TEB4033-03



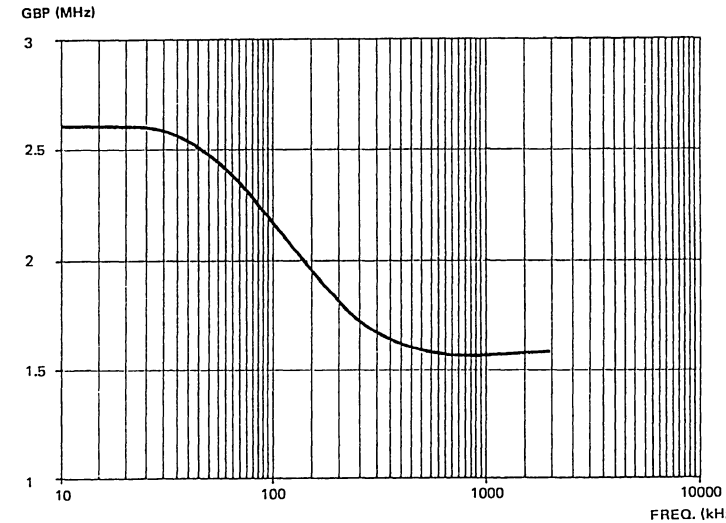
OFFSET VOLTAGE VS. AMBIENT TEMPERATURE

E88TEB4033-04



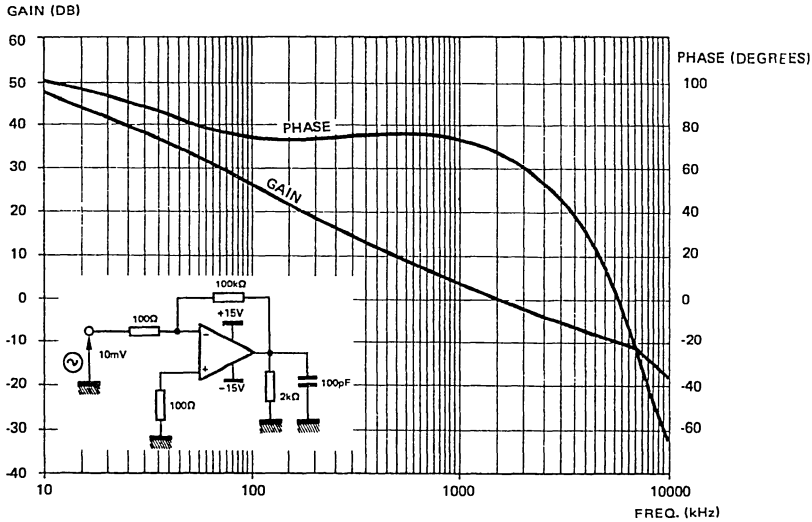
TOTAL INPUT NOISE VS. FREQUENCY

E88TEB4033-05



GAIN BANDWIDTH PRODUCT VS. FREQUENCY

E88TEB4033-06

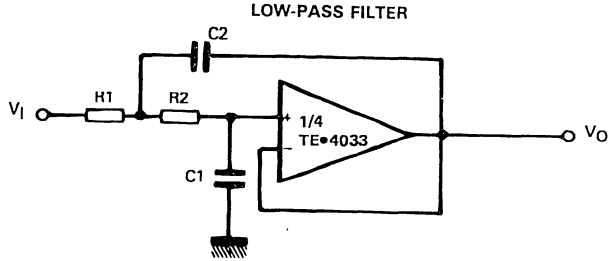


BODE PLOT

E88TEB4033-07

TYPICAL APPLICATION

LOW-PASS FILTER



E88TEB4033-08

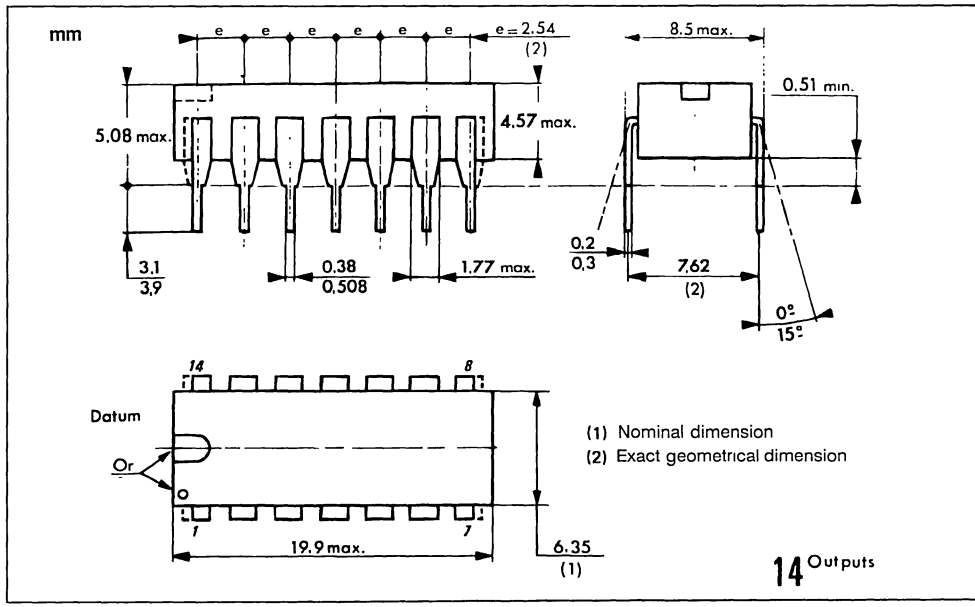
$$\frac{V_o}{V_i} = \frac{1}{1 + 2\xi\frac{S}{\omega_c} + \frac{S^2}{\omega_c^2}}$$

$\omega_c = 2\pi f_c$, with f_c = cutt-off frequency

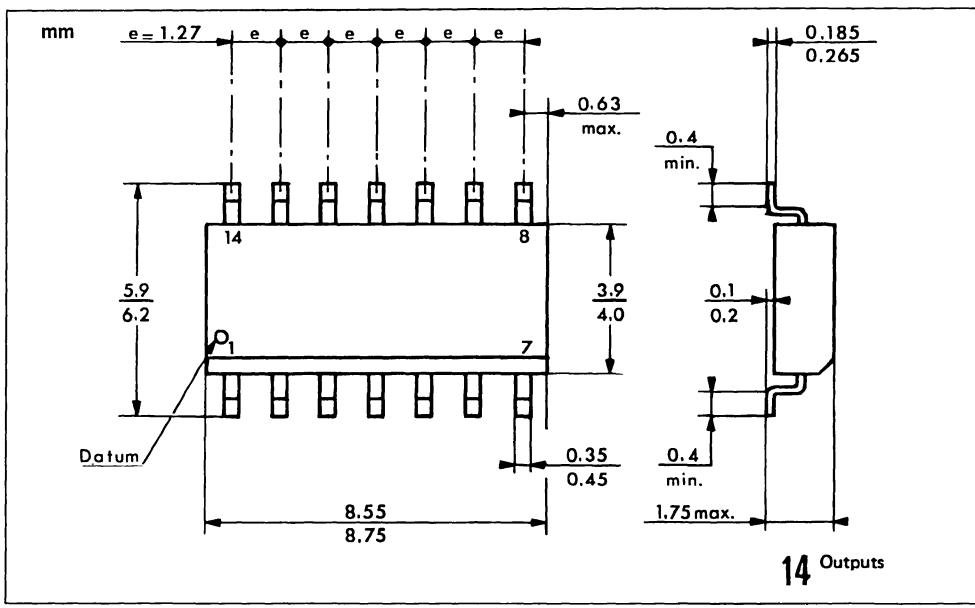
ξ = damping factor

PACKAGE MECHANICAL DATA

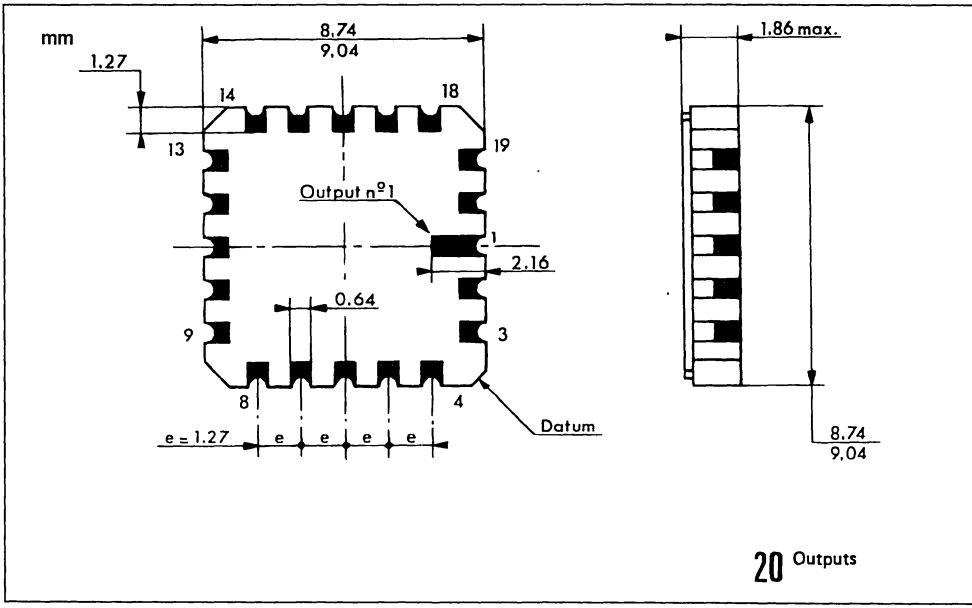
14 PINS – PLASTIC DIP OR CERDIP



14 PINS – PLASTIC MICROPACKAGE (SO)



20 PINS – TRICECOP (LCC)



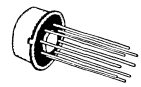
SGS-THOMSON MICROELECTRONICS

TL061
TL061A-TL061B

LOW POWER J–FET INPUT SINGLE OP–AMPs

- VERY LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW INPUT BIAS AND OFFSET CURRENTS
- TYPICAL SUPPLY CURRENT : 200 µA
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J–FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 3.5 V/µs (typ)

N
DIP8
(Plastic package)



H
TO-99
(Metal can)

D
SO8
(Plastic micropackage)

GC
LCC20
(Tricecop LCC)

DESCRIPTION

The TL061, TL061A and TL061B are high speed J–FET input single operational amplifier family. Each of these J–FET input operational amplifiers incorporates well matched, high voltage J–FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

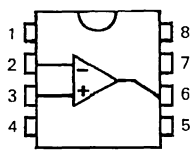
ORDER CODES

Part Number	Temperature Range	Package			
		N	D	H	GC
TL061M	– 55 °C to + 125 °C			•	•
TL061I	– 40 °C to + 105 °C	•	•		
TL061C	0 °C to + 70 °C	•	•		
TL061AC	0 °C to + 70 °C	•	•		
TL061BC	0 °C to + 70 °C	•	•		

Note : Hi-Rel Versions Available
Examples : TI061MH, TL061IN

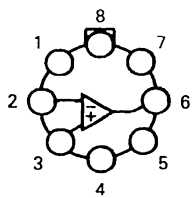
PIN CONNECTIONS (Top views)

DIP8
SO8



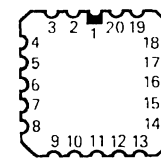
5 - Balance
6 - Output
7 - V_{CC}^{+}
8 - NC

TO-99



1 - Balance
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^{-}

LCC20



1 - NC
2 - Balance
3 - NC
4 - NC
5 - Inverting input
6 - NC
7 - Non-inverting input
8 - NC
9 - NC
10 - V_{CC}^{-}
11 - NC
12 - Balance
13 - NC
14 - NC
15 - Output
16 - NC
17 - V_{CC}^{+}
18 - NC
19 - NC
20 - NC

MAXIMUM RATINGS

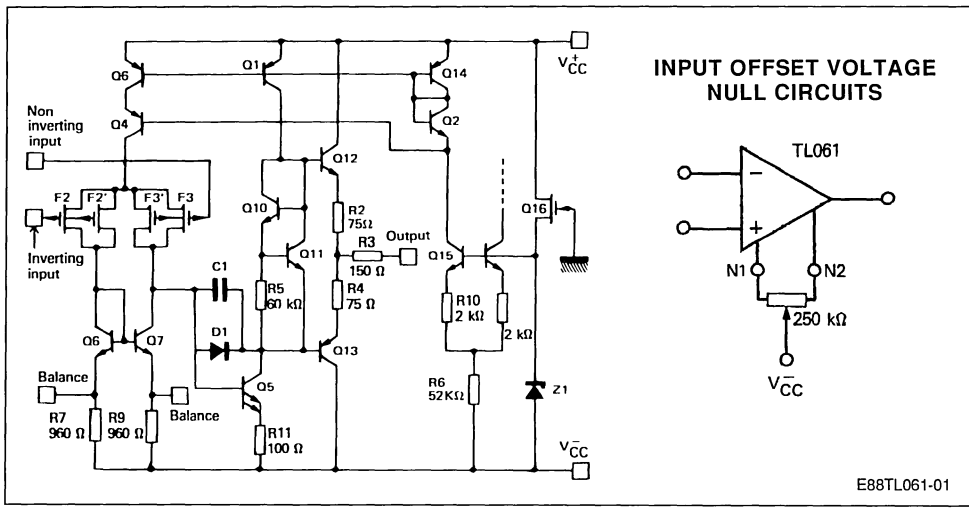
Symbol	Parameter	TL061M	TL061I	TL061C	Unit
V_{CC}	Supply Voltage (note 1)	± 18	± 18	± 18	V
V_{ID}	Differential Input Voltage (note 2)	± 30	± 30	± 30	V
V_I	Input Voltage (note 3)	± 15	± 15	± 15	V
	Output Short-circuit Duration (note 4)	Indefinite	Indefinite	Indefinite	
P_{tot}	Power Dissipation (note 5)	680	680	680	mW
T_{oper}	Operating Free-air, Temperature Range	− 55 to + 125	− 40 to + 105	0 to + 70	°C
T_{stg}	Storage Temperature Range	− 65 to + 150	− 65 to + 150	− 65 to + 150	°C

* Devices bonded on a 6 cm x 0 15 cm glass epoxy substrate with 30 mm^2 of 35 µm thick copper.

Notes : 1. All voltage values, except differential voltages, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.

2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceed.
5. For operation above + 25 °C free-air temperature, refer to dissipation derating table.

SCHEMATIC DIAGRAM



Case	Balance	Inverting Input	Non-Inverting Input	V_{CC}^-	V_{CC}^+	Output	N.C.
DIP8 SO8 TO-99	1, 5	2	3	4	7	6	8
LCC20	2, 12	5	7	10	17	15	*

* **LCC20** : Other pins are not connected.

ELECTRICAL CHARACTERISTICS

TL061M : – 55 °C ≤ T_{amb} ≤ + 125 °C
TL061I : – 40 °C ≤ T_{amb} ≤ + 105 °C
TL061C : 0 °C ≤ T_{amb} ≤ + 70 °C
V_{CC} = ± 15V.
All characteristics are specified under open-loop conditions unless otherwise specified.

Symbol	Parameter	TL061M			TL061I			TL061C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage T_{amb} = + 25 °C, R_S = 50 Ω T_{min} ≤ T_{amb} ≤ T_{max}, R_S = 50 Ω		3	6 9		3	6 9		3	15 20	mV
α V_{IO}	Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω)		10			10			10		µV/°C
I_{IO}	Input Offset Current * T_{amb} = + 25 °C T_{min} ≤ T_{amb} ≤ T_{max}		5	100 20		5	100 10		5	200 5	pA nA
I_{IB}	Input Bias Current * T_{amb} = + 25 °C T_{min} ≤ T_{amb} ≤ T_{max}		30	200 50		30	200 20		30	400 10	pA nA
V_I	Input Common-mode Voltage Range (T_{amb} = + 25 °C)	± 11	± 12		± 11.5	± 12		± 10	± 11		V
V_{OPP}	Output Voltage Swing : R_L = 10 KΩ, T_{amb} = + 25 °C R_L ≥ 10 KΩ, T_{min} ≤ T_{amb} ≤ T_{max}	20 20	27		20 20	27		20 20	27		V
A_{VD}	Large Signal Voltage Gain T_{amb} = + 25 °C, R_l ≥ 10 KΩ, V_O = ± 10 V T_{min} ≤ T_{amb} ≤ T_{max}, R_L ≥ 10 KΩ, V_O = ± 10 V	4 4	6		4 4	6		3 3	6		V/mV
GW_R	Small Signal Bandwidth (T_{amb} = + 25 °C, R_L = 10 KΩ)		1			1			1		MHz
R_I	Input Resistance (T_{amb} = + 25 °C)		10^{12}			10^{12}			10^{12}		Ω
CMR	Common-mode Rejection Ratio (R_S ≥ 10 KΩ, T_{amb} = + 25 °C)	80	86		80	86		70	76		dB
SVR	Supply Voltage Rejection Ratio ($\Delta V_{CC}/\Delta V_{IO}$) R_S ≥ 10 KΩ, T_{amb} = + 25 °C	80	95		80	95		70	95		dB
I_{CC}	Supply Current (T_{amb} = + 25 °C, no load, no signal)		200	250		200	250		200	250	µA
P_D	Total Power Consumption (each amplifier) T_{amb} = + 25 °C, No load, no signal		6	7.5		6	7.5		6	7.5	mW

* Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	TL061M			TL061I, C			Unit.
		Min.	Typ.	Max.	Min.	Typ.	Max.	
S_{VO}	Slew Rate (e_I = 10 V, R_L = 10 KΩ, C_L = 100 pF, A_V = 1)	2	3 5			3.5		V/µs
t_r	Rise Time (e_I = 20 mV, R_L = 10 KΩ, C_L = 100 pF, A_V = 1) (see fig. 1)		0.2			0.2		µs
K_{OV}	Overshoot Factor (e_I = 20 mV, R_L = 10 KΩ, C_L = 100 pF, A_V = 1) (see fig. 1)		10			10		%
Vn	Equivalent Input Noise Voltage (R_S = 100 KΩ, f = 1 KHz)		42			42		nV/√Hz

ELECTRICAL CHARACTERISTICS

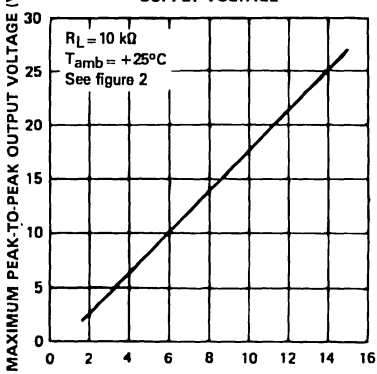
TL061C : 0 °C ≤ T_{amb} ≤ + 70 °C
V_{CC} = ± 15V
All characteristics are specified under open-loop conditions unless otherwise specified.

Symbol	Parameter	TL061C			TL061AC			TL061BC			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage T_{amb} = + 25 °C, R_S = 50 Ω $T_{min} \le T_{amb} \le T_{max}$, R_S = 50 Ω		3	15 20		3	6 7.5		2	3 5	mV
α V_{IO}	Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω)		10			10			10		µV/°C
I_{IO}	Input Offset Current * T_{amb} = + 25 °C $T_{min} \le T_{amb} \le T_{max}$		5	200 5		5	100 3		5	100 3	pA nA
I_{IB}	Input Bias Current * T_{amb} = + 25 °C $T_{min} \le T_{amb} \le T_{max}$		30	400 10		30	200 7		30	200 7	pA nA
V_I	Input Common-mode Voltage Range	± 10	± 11		± 11.5	± 12		±11.5	± 12		V
V_{OPP}	Output Voltage Swing : R_L = 10 KΩ, T_{amb} = + 25 °C $R_L \ge$ 10 KΩ, $T_{min} \le T_{amb} \le T_{max}$	20 20	27		20 20	27		20 20	27		V
A_{VD}	Large Signal Voltage Gain T_{amb} = + 25 °C, $R_l \ge$ 10 KΩ, V_O = ± 10 V $T_{min} \le T_{amb} \le T_{max}$	3 3	6		4 4	6		4 4	6		V/mV
GW_R	Small Signal Bandwidth (T_{amb} = + 25 °C, R_L = 10 KΩ)		1			1			1		MHz
R_i	Input Resistance (T_{amb} = + 25 °C)		10^{12}			10^{12}			10^{12}		Ω
CMR	Common-mode Rejection Ratio ($R_S \ge$ 10 KΩ ; T_{amb} = + 25 °C)	70	76		80	86		80	86		dB
SVR	Supply Voltage Rejection Ratio ($\Delta V_{CC}/\Delta V_{IO}$) $R_S \ge$ 10 KΩ, T_{amb} = + 25 °C	70	95		80	95		80	95		dB
I_{CC}	Supply Current (T_{amb} = + 25 °C, no load, no signal)		200	250		200	250		200	250	µA
P_D	Total Power Consumption (each amplifier) T_{amb} = + 25 °C, no load, no signal		6	7.5		6	7 5		6	7.5	mW

* Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

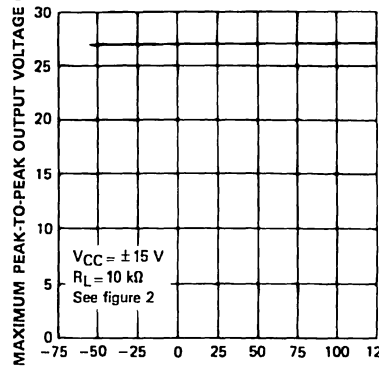
TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE



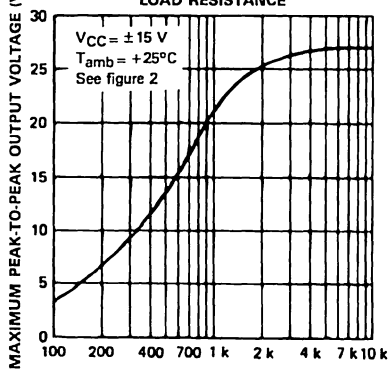
E88TL061-02

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE



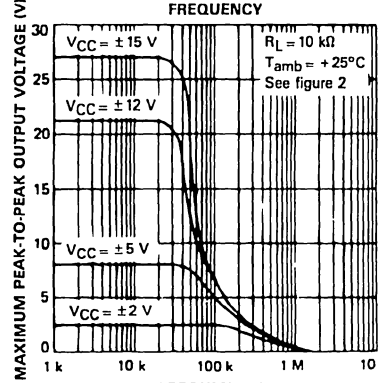
E88TL061-03

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE



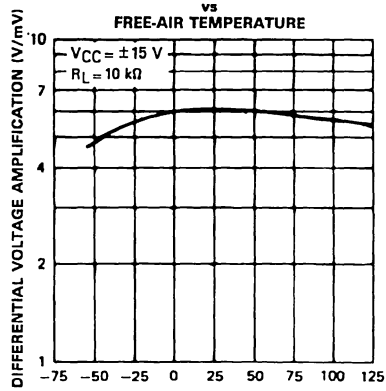
E88TL061-04

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY



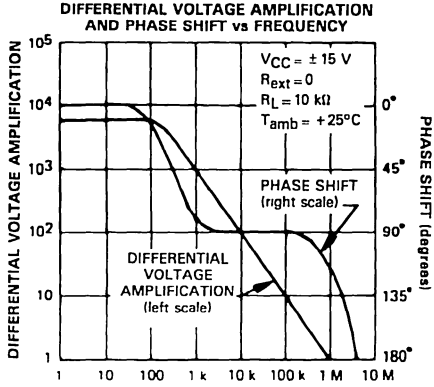
E88TL061-05

DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE



E88TL061-06

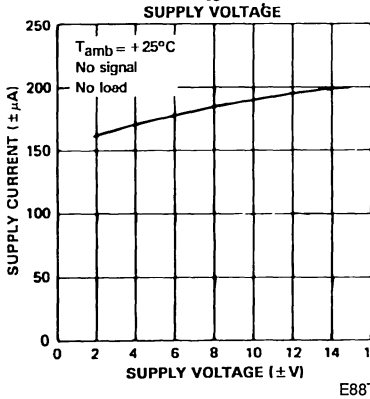
LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY



E88TL061-07

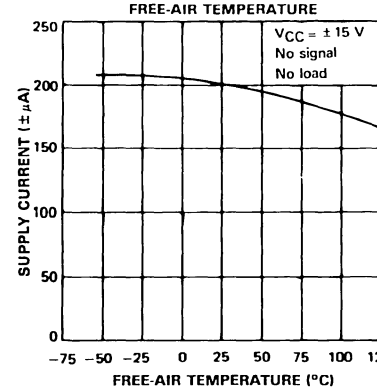
TYPICAL CHARACTERISTICS (continued)

SUPPLY CURRENT PER AMPLIFIER
vs
SUPPLY VOLTAGE



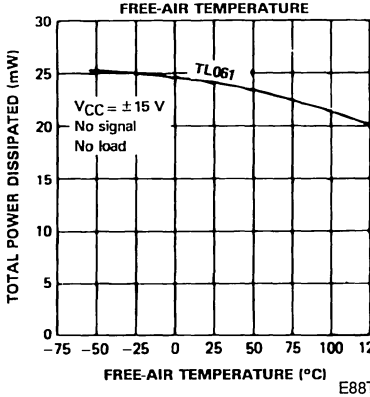
E88TL061-08

SUPPLY CURRENT PER AMPLIFIER
vs
FREE-AIR TEMPERATURE



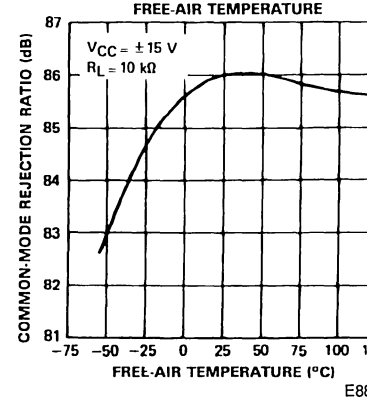
E88TL061-09

TOTAL POWER DISSIPATED
vs
FREE-AIR TEMPERATURE



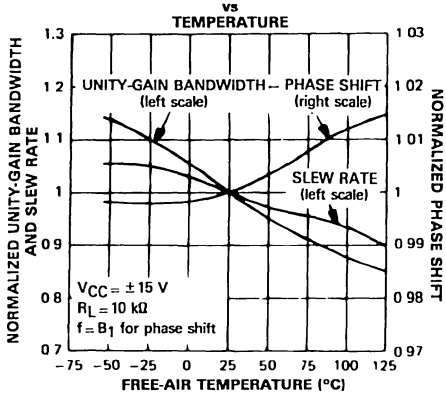
E88TL061-10

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE



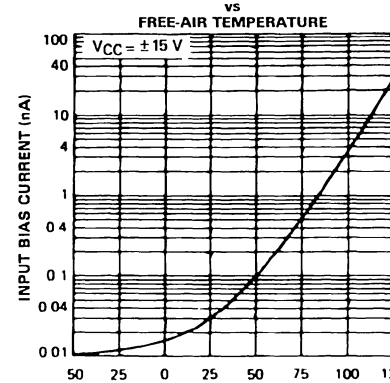
E88TL061-11

NORMALIZED UNITY-GAIN BANDWIDTH
SLEW RATE, AND PHASE SHIFT
vs
TEMPERATURE



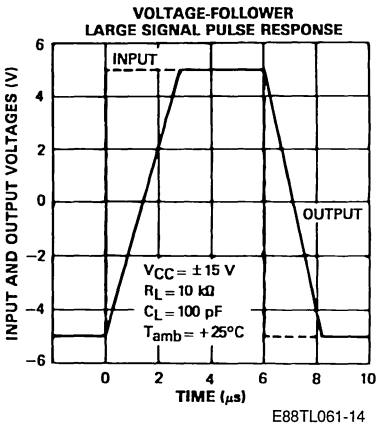
E88TL061-12

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

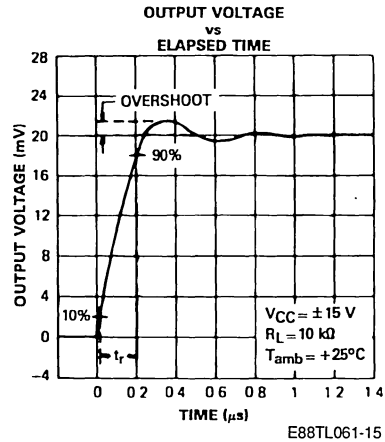


E88TL061-13

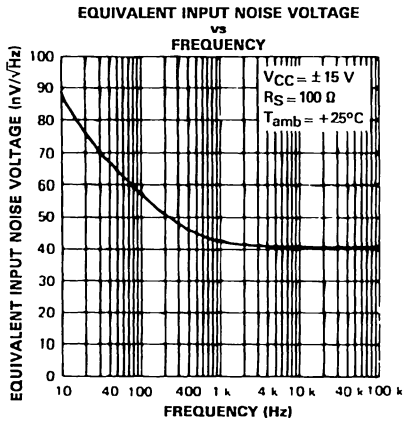
TYPICAL CHARACTERISTICS (continued)



E88TL061-14



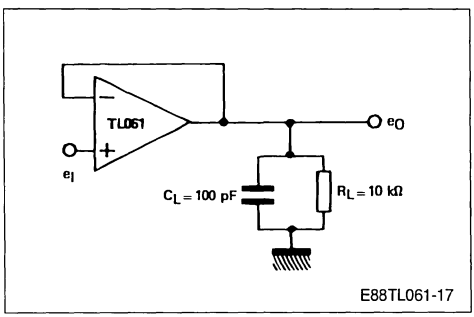
E88TL061-15



E88TL061-16

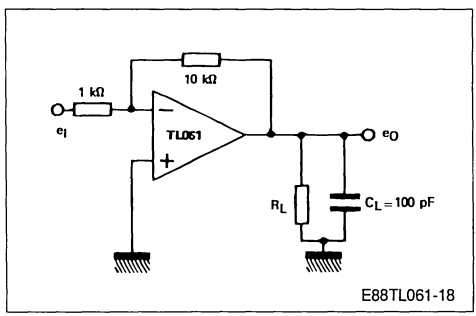
PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage follower.



E88TL061-17

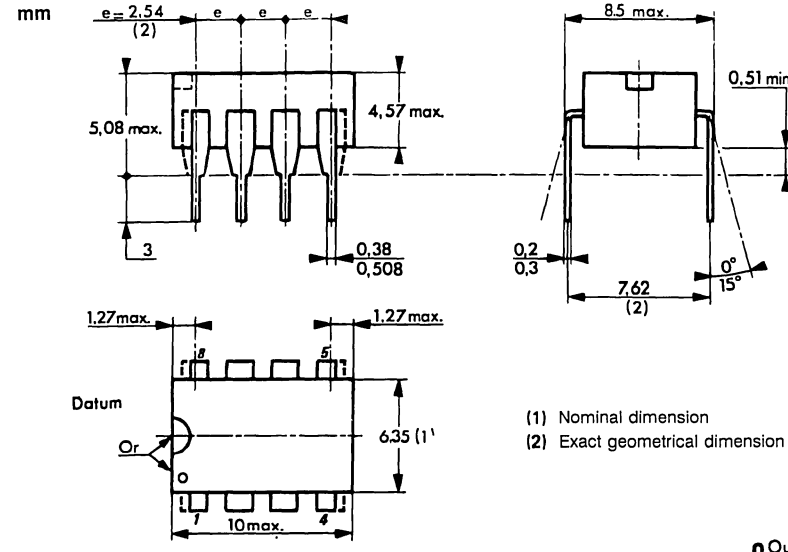
Figure 2 : Gain-of-10 inverting amplifier.



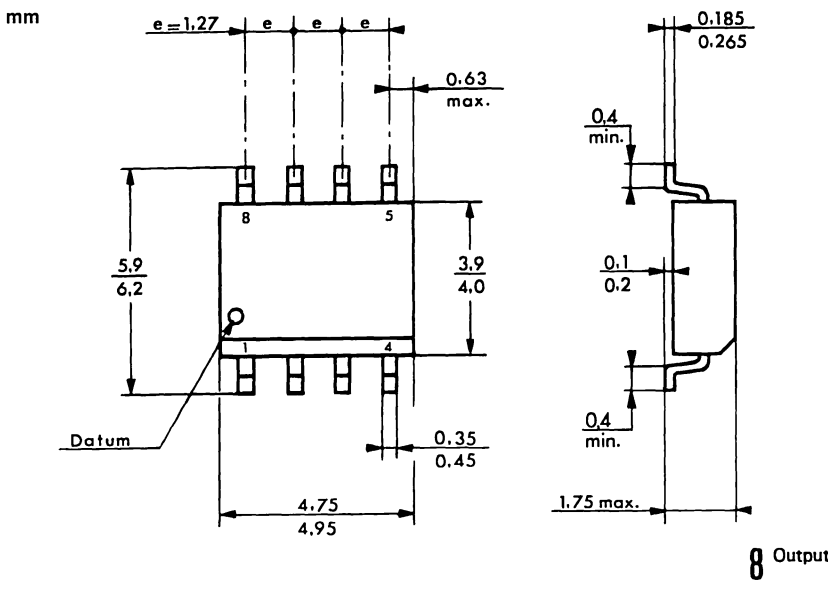
E88TL061-18

PACKAGE MECHANICAL DATA

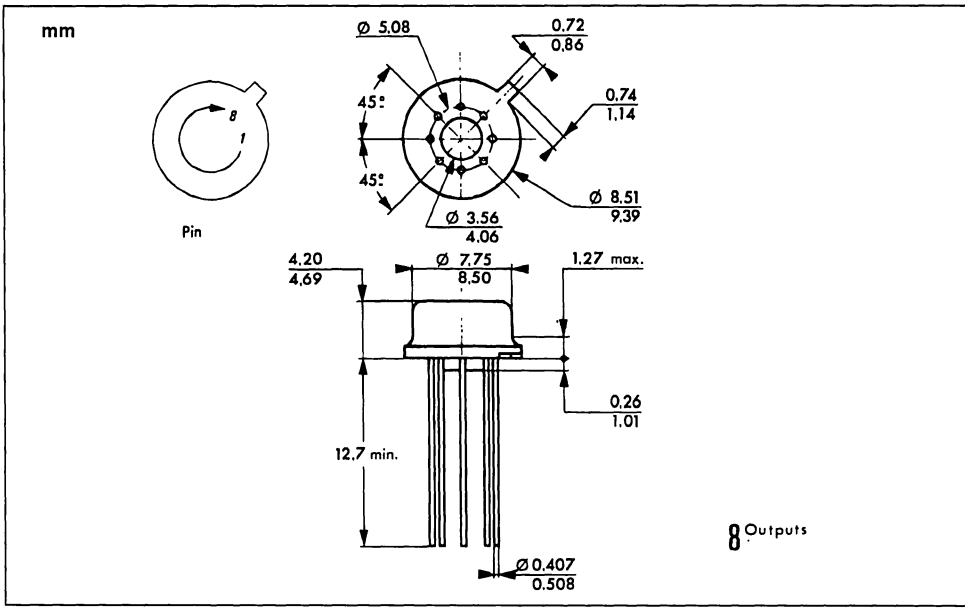
8 PINS – PLASTIC DIP



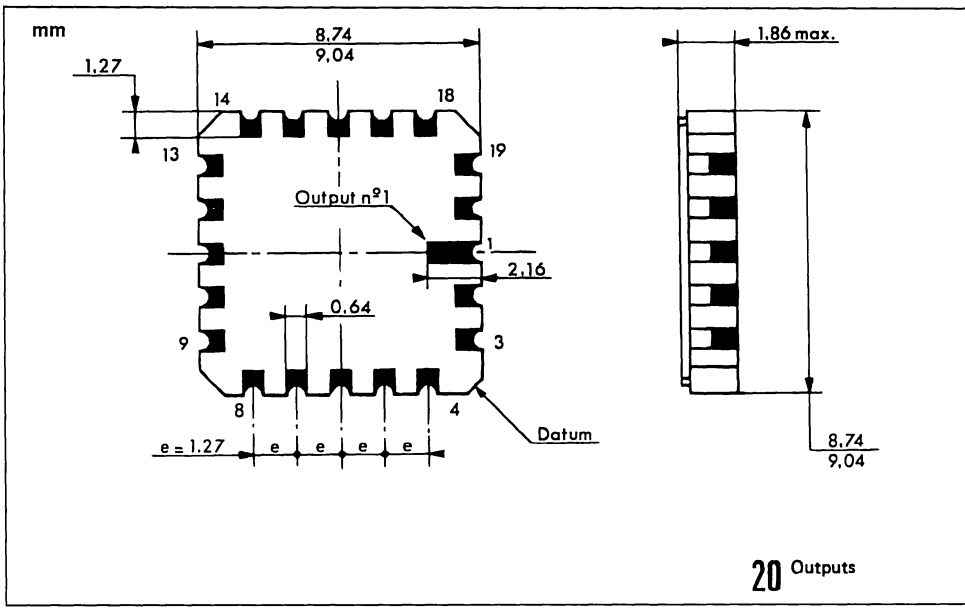
8 PINS – PLASTIC MICROPACKAGE (SO)



TO-99 – METAL CAN



20 PINS – TRICECOP (LCC)



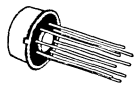
SGS-THOMSON MICROELECTRONICS

TL062
TL062A-TL062B

LOW POWER J–FET INPUT DUAL OP–AMPs

- VERY LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW INPUT BIAS AND OFFSET CURRENTS
- TYPICAL SUPPLY CURRENT : 200 µA
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J–FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 3.5 V/µs (typ.)

N
DIP8
(Plastic package)



H
TO-99
(Metal Can)

D
SO8
(Plastic micropackage)

GC
LCC20
(Tricecop - LCC)

ORDER CODES

Part Number	Temperature Range	Package			
		N	H	D	GC
TL062M	– 55 °C to + 125 °C		•		•
TL062I	– 40 °C to + 105 °C	•		•	
TL062C	0 °C to + 70 °C	•		•	
TL062AC	0 °C to + 70 °C	•		•	
TL062BC	0 °C to + 70 °C	•		•	

Note : Hi-Rel versions available
Examples : TL062 MH, TL062 CN

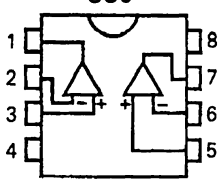
DESCRIPTION

The TL062, TL062A and TL062B are high speed J–FET input dual operational amplifier family. Each of these J–FET input operational amplifiers incorporates well matched, high voltage J–FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rate, low input bias and offset currents, and low offset voltage temperature coefficient.

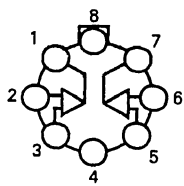
PIN CONNECTIONS (Top views)

DIP8
SO8



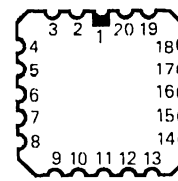
1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-

TO-99



5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

LCC20



1 - NC
2 - Output 1
3 - NC
4 - NC
5 - Inverting input 1
6 - NC
7 - Non-inverting input 1
8 - NC
9 - NC
10 - V_{CC}^-
11 - NC
12 - Non-inverting input 2
13 - NC
14 - NC
15 - Inverting input 2
16 - NC
17 - Output 2
18 - NC
19 - NC
20 - V_{CC}^+

MAXIMUM RATINGS

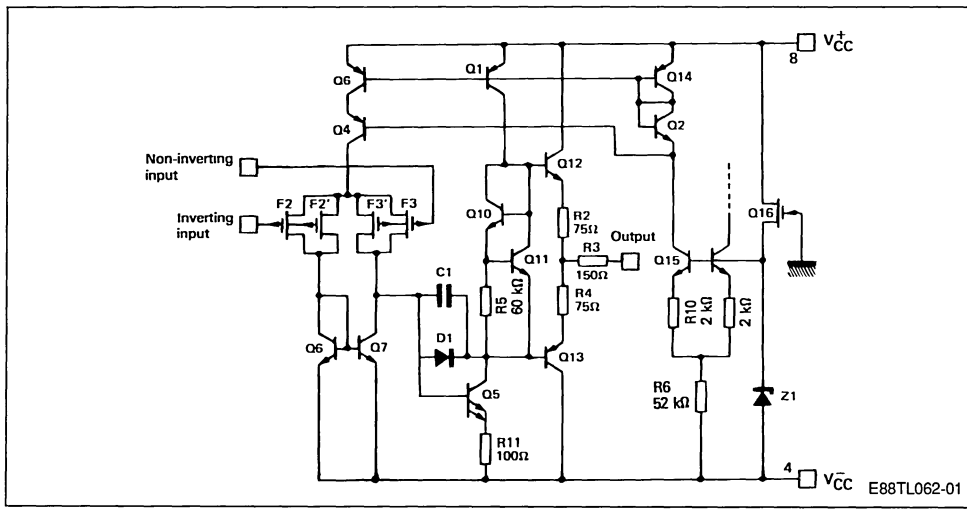
Symbol	Parameter	TL064M	TL064I	TL064C	Unit
V_{CC}	Supply Voltage (note 1)	± 18	± 18	± 18	V
P_{tot}	Power Dissipation (note 5)	680	680	680	mW
V_{ID}	Differential Input Voltage (note 2)	± 30	± 30	± 30	V
V_I	Input Voltage (note 3)	± 15	± 15	± 15	V
	Ouput Short-circuit Duration (note 4)	Indefinite	Indefinite	Indefinite	
T_{oper}	Operating Free-air, Temperature Range	− 55 to + 125	− 40 to + 105	0 to + 70	°C
T_{stg}	Storage Temperature Range	− 65 to + 150	− 65 to + 150	− 65 to + 150	°C

* Devices bonded on a 6 cm x 0.15 cm glass epoxy substrate with 30 mm^2 of 35 µm thick copper.

Notes : 1. All voltage values, except differential voltages, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.

2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceed.
5. For operation above + 25 °C free-air temperature, refer to dissipation derating table.

SCHEMATIC DIAGRAM 1/2 TL062



Case	Outputs	Inverting Inputs	Non-inverting Inputs	V_{cc}^-	V_{cc}^+	N.C.
DIP8 SO8 TO-99	1, 7	2, 6	3, 5	4	8	
LCC20	2, 17	5, 15	7, 12	10	20	*

* **LCC20** : Other pins are not connected.

ELECTRICAL CHARACTERISTICS

TL062M : – 55 °C ≤ T_{amb} ≤ + 125 °C
TL062I : – 40 °C ≤ T_{amb} ≤ + 105 °C
TL062C : 0 °C ≤ T_{amb} ≤ + 70 °C
V_{CC} = ± 15V.
All characteristics are specified under open-loop conditions unless otherwise specified.

Symbol	Parameter	TL062M			TL062I			TL062C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage (R_S = 50 Ω) T_{amb} = + 25 °C T_{min} ≤ T_{amb} ≤ T_{max}		3	6 15		3	6 9		3	15 20	mV
α V_{IO}	Temperature Coefficient of Input Offset Voltage R_S = 50 Ω		10			10			10		µV/°C
I_{IO}	Input Offset Current * T_{amb} = + 25 °C T_{min} ≤ T_{amb} ≤ T_{max}		5	100 20		5	100 10		5	200 5	pA nA
I_{IB}	Input Bias Current * T_{amb} = + 25 °C T_{min} ≤ T_{amb} ≤ T_{max}		30	200 50		30	200 20		30	400 10	pA nA
V_I	Input Common-mode Voltage Range T_{amb} = + 25 °C	±11	±12		±11.5	±12		±10	±11		V
V_{OPP}	Output Voltage Swing T_{amb} = + 25 °C, R_L = 10 KΩ T_{min} ≤ T_{amb} ≤ T_{max} , R_L ≥ 10 KΩ	20 20	27		20 20	27		20 20	27		V
A_{VD}	Large Signal Voltage Gain (R_L ≥ 10 KΩ, V_O = ± 10 V) T_{amb} = + 25 °C T_{min} ≤ T_{amb} ≤ T_{max}	4 4	6		4 4	6		3 3	6		V/mV
GW_R	Small Signal Bandwidth (T_{amb} = + 25 °C, R_L = 10 KΩ)		1			1			1		MHz
R_I	Input Resistance (T_{amb} = + 25 °C)		10^{12}			10^{12}			10^{12}		Ω
CMR	Common-mode Rejection Ratio R_S ≤ 10 KΩ, T_{amb} = + 25 °C	80	86		80	86		70	76		dB
SVR	Supply Voltage Rejection Ratio ($\Delta V_{CC}/\Delta V_{IO}$) R_S ≤ 10 KΩ, T_{amb} = + 25 °C	80	95		80	95		70	95		dB
I_{CC}	Supply Current (Per Amplifier) T_{amb} = + 25 °C, No Load, No Signal		200	250		200	250		200	250	µA
V_{O1}/V_{O2}	Channel Separation (A_{VD} = 100, T_{amb} = + 25 °C)		120			120			120		mW
P_D	Total Power Consumption (Each Amplifier) No Load , No Signal T_{amb} = + 25 °C		6	7.5		6	7.5		6	7.5	mW

* Input bias currents of a FET–input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as closes to the ambient temeprature as is possible.

ELECTRICAL CHARACTERISTICS

V_{CC} = ± 15V, T_{amb} = + 25 °C.

Symbol	Parameter	TL062M			TL062I, C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
S_{VO}	Slew Rate (e_I = 10 V, R_L = 10 KΩ, C_L = 100 pF, A_V = 1)	2	3.5			3.5		V/µs
t_r	Rise Time (e_I = 20 mV, R_L = 10 KΩ, C_L = 100 pF, A_V = 1) (See Fig. 1)		0.2			0.2		µs
K_{OV}	Overshoot Factor (e_I = 20 mV, R_L = 10 KΩ, C_L = 100 pF, A_V = 1 V) (See Fig. 1)		10			10		%
Vn	Equivalent Input Noise Voltage (R_S = 100 KΩ, f = 1 KHz)		42			42		nV/√Hz

ELECTRICAL CHARACTERISTICS

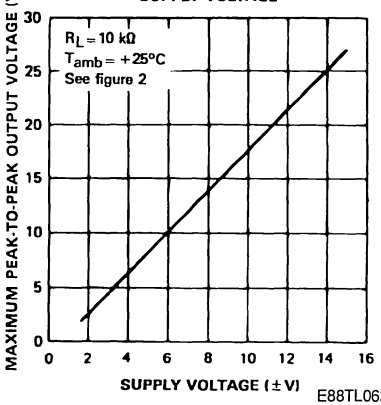
TL062C : 0 °C ≤ Tamb≤ + 70 °C
V_{CC} = ± 15V
All characteristics are specified under open-loop conditions unless otherwise specified.

Symbol	Parameter	TL062C			TL062AC			TL062BC			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage (R_S = 50 Ω) T_{amb} = + 25 °C $T_{min} \le T_{amb} \le T_{max}$		3	15 20		3	6 7.5		2	3 5	mV
αV_{IO}	Temperature Coefficient of Input Offset Voltage R_S = 50 Ω		10			10			10		µV/°C
I_{IO}	Input Offset Current * T_{amb} = + 25 °C $T_{min} \le T_{amb} \le T_{max}$		5	200 5		5	100 3		5	100 3	pA nA
I_{IB}	Input Bias Current * T_{amb} = + 25 °C $T_{min} \le T_{amb} \le T_{max}$		30	400 10		30	200 7		30	200 7	pA nA
V_I	Input Common-mode Voltage Range T_{amb} = + 25 °C	±10	±11		±11.5	±12		±11.5	±12		V
V_{OPP}	Output Voltage Swing T_{amb} = + 25 °C, R_L = 10 KΩ $T_{min} \le T_{amb} \le T_{max}$	20 20	27		20 20	27		20 20	27		V
A_{VD}	Large Signal Voltage Gain ($R_L \ge$ 10 KΩ, V_O = ± 10 V) T_{amb} = + 25 °C $T_{min} \le T_{amb} \le T_{max}$	3 3	6		4 4	6		4 4	6		V/mV
GW_R	Small Signal Bandwidth (T_{amb} = + 25 °C, R_L = 10 KΩ)		1			1			1		MHz
R_I	Input Resistance (T_{amb} = + 25 °C)		10^{12}			10^{12}			10^{12}		Ω
CMR	Common-mode Rejection Ratio $R_S \le$ 10 KΩ, T_{amb} = + 25 °C	70	76		80	86		80	86		dB
SVR	Supply Voltage Rejection Ratio ($\Delta V_{CC}/\Delta V_{IO}$) $R_S \le$ 10 KΩ, T_{amb} = + 25 °C	70	95		80	95		80	95		dB
I_{CC}	Supply Current (Per Amplifier) T_{amb} = + 25 °C, No Load, No Signal		200	250		200	250		200	250	µA
V_{O1}/V_{O2}	Channel Separation (A_{VD} = 100, T_{amb} = + 25 °C)		120			120			120		dB
P_D	Total Power Consumption (Each Amplifier) No Load , No Signal T_{amb} = + 25 °C		6	7.5		6	7.5		6	7.5	mW

* Input bias currents of a FET–input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

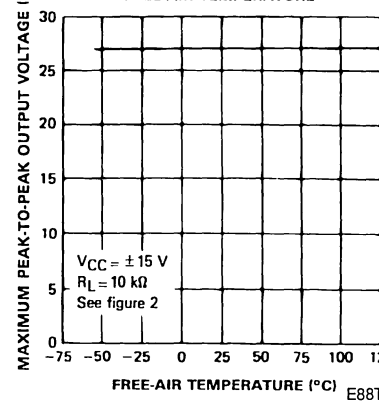
TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE



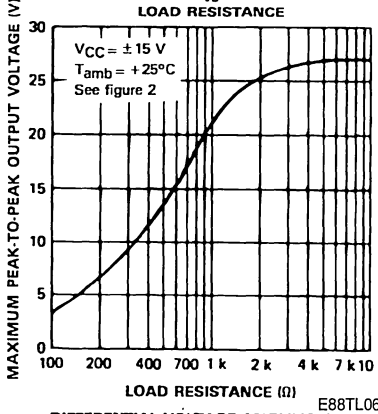
E88TL062-02

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE



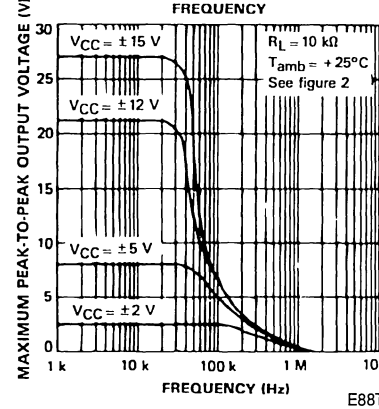
E88TL062-03

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE



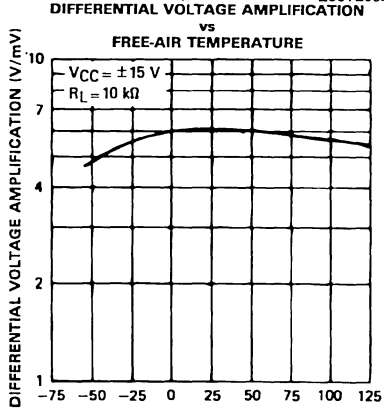
E88TL062-04

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY



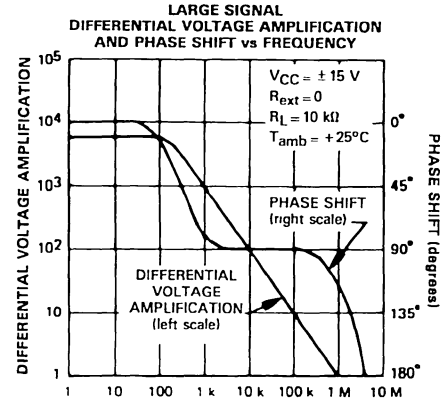
E88TL062-05

DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE



E88TL062-06

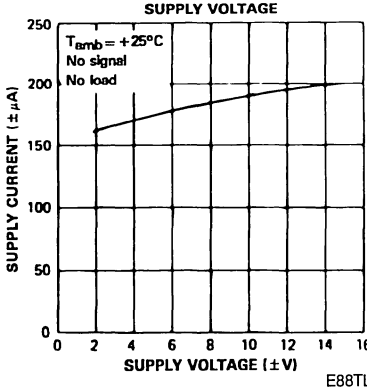
LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY



E88TL062-07

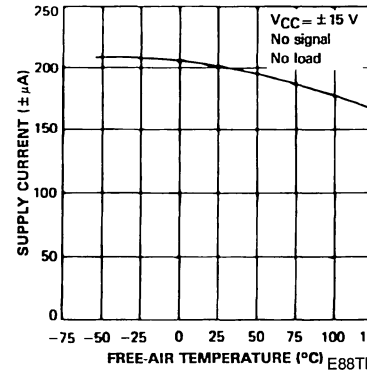
TYPICAL CHARACTERISTICS (continued)

SUPPLY CURRENT PER AMPLIFIER vs SUPPLY VOLTAGE



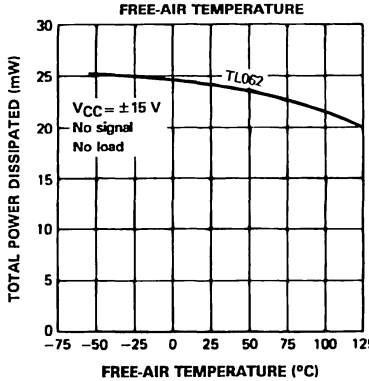
E88TL062-08

SUPPLY CURRENT PER AMPLIFIER vs FREE-AIR TEMPERATURE



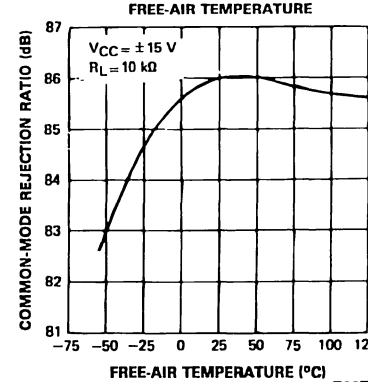
E88TL062-09

TOTAL POWER DISSIPATED vs FREE-AIR TEMPERATURE



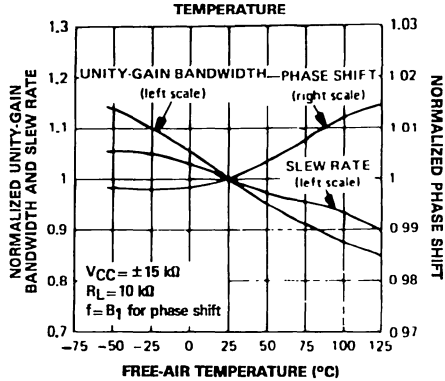
E88TL062-10

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE



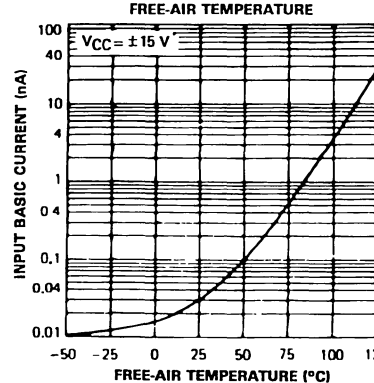
E88TL062-11

NORMALIZED UNITY-GAIN BANDWIDTH SLEW RATE, AND PHASE SHIFT vs TEMPERATURE



E88TL062-12

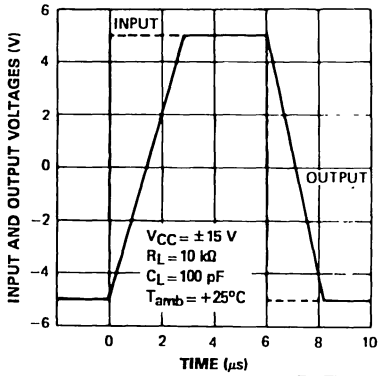
INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE



E88TL062-13

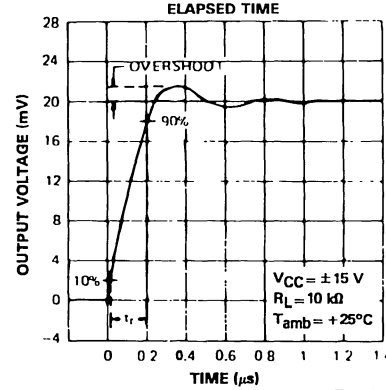
TYPICAL CHARACTERISTICS (continued)

VOLTAGE-FOLLOWER
LARGE SIGNAL PULSE RESPONSE



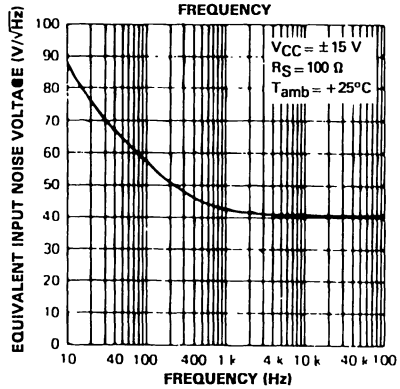
E88TL062-14

OUTPUT VOLTAGE
vs
ELAPSED TIME



E88TL062-15

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY



E88TL062-16

PARAMETER MEASUREMENT INFORMATION
TEST CIRCUITS

Figure 1 : Voltage follower.

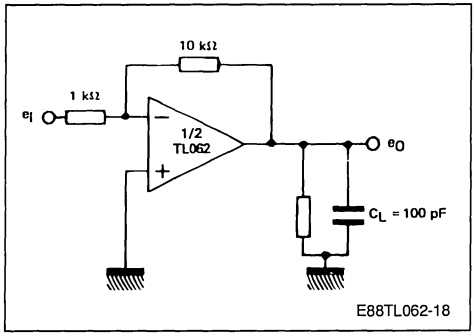
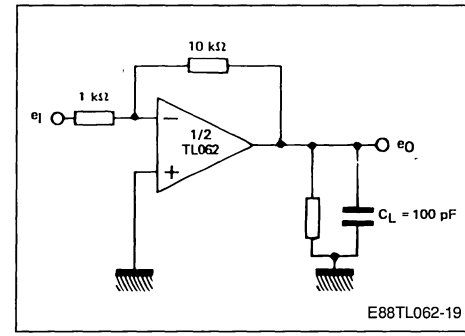
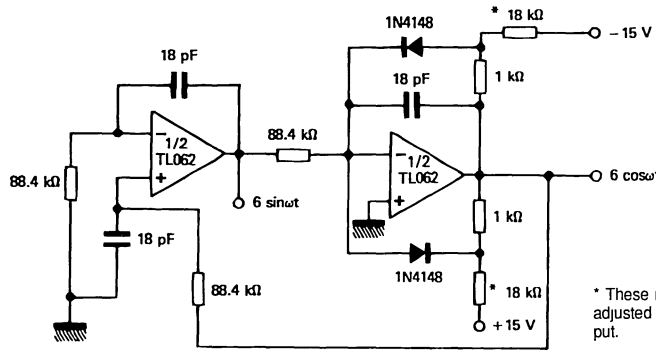


Figure 2 : Gain-of-10 inverting amplifier.



TYPICAL APPLICATION

QUADRATURE OSCILLATOR

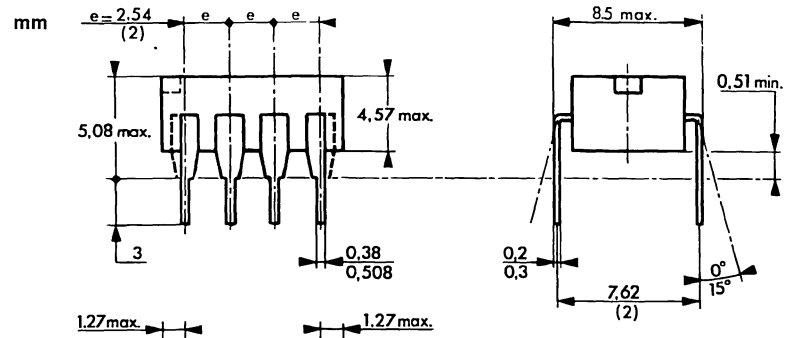


* These resistor values may be adjusted for a symmetrical output.

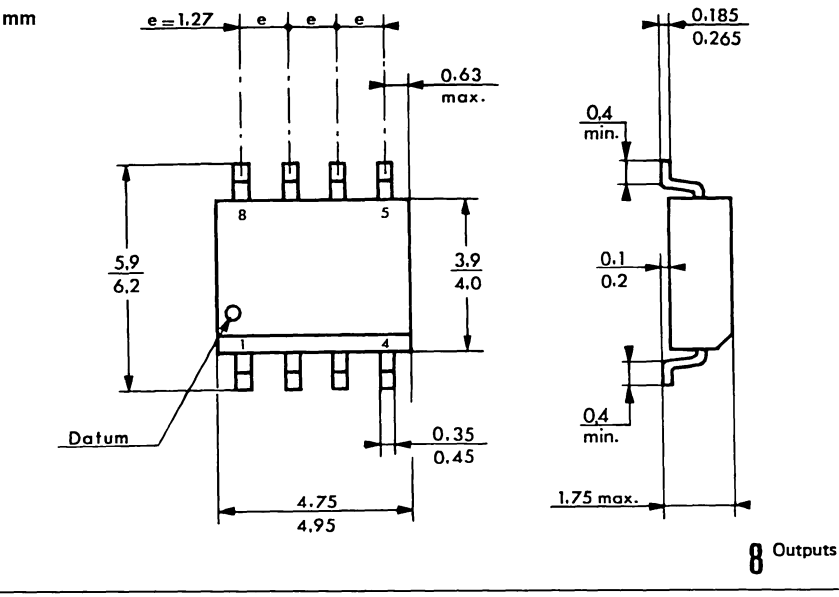
E88TL062-17

PACKAGE MECHANICAL DATA

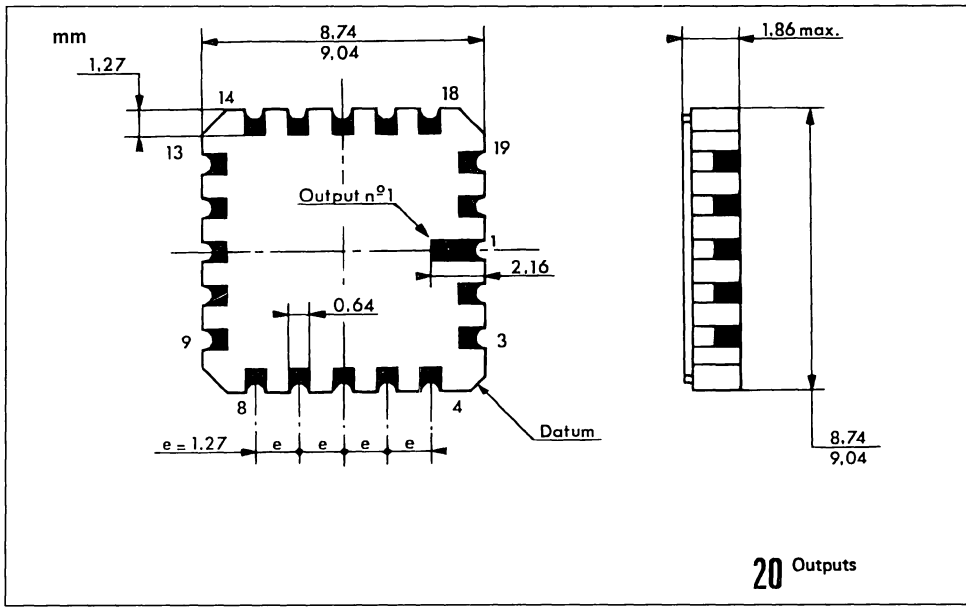
8 PINS– PLASTIC DIP



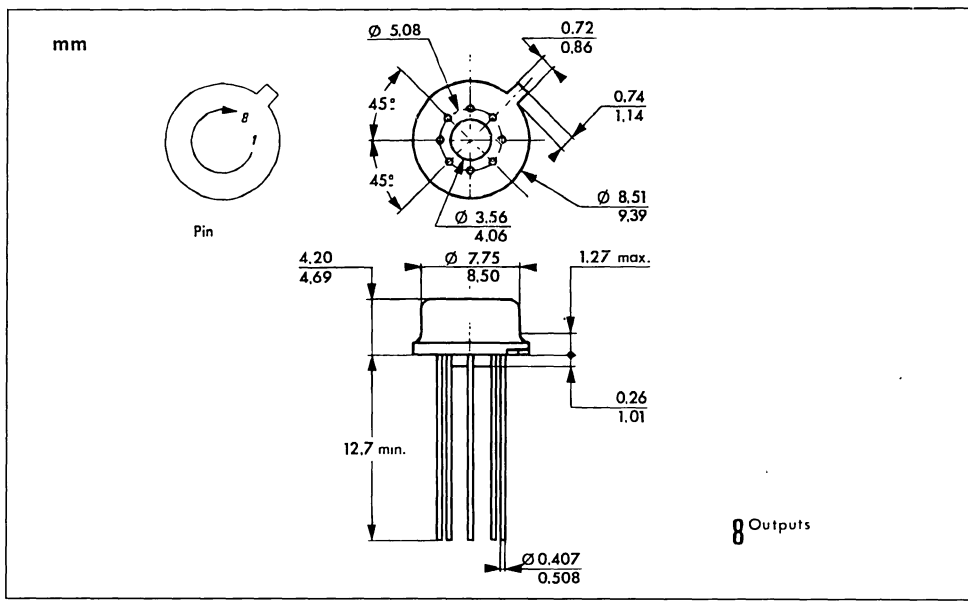
8 PINS – PLASTIC MICROPACKAGE (SO)



20 PINS – TRICECOP (LCC)



TO-99 – METAL CAN

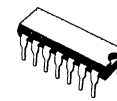


SGS-THOMSON MICROELECTRONICS

TL064
TL064A-TL064B

LOW POWER J–FET INPUT QUAD OP-AMPs

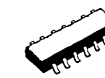
- VERY LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW INPUT BIAS AND OFFSET CURRENTS
- TYPICAL SUPPLY CURRENT : 200 µA
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J–FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 3.5 V/µs (typ)



N
DIP14
(Plastic package)

J
CERDIP14
(Cerdip package)

GC
LCC20
(Tricecop - LCC)



D
SO14
(Plastic micropackage)

DESCRIPTION

The TL064, TL064A and TL064B are high speed J–FET input quad operational amplifiers. Each of these J–FET input operational amplifiers incorporates well matched, high voltage J–FET and bipolar transistors in a monolithic integrated circuit.

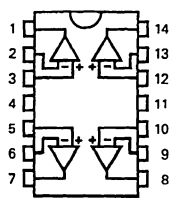
The devices feature high slew rates, low input bias current and offset currents, and low offset voltage temperature coefficient.

Part Number	Temperature Range	Package			
		N	J	D	GC
TL064M	– 55 °C to + 125 °C		•		•
TL064I	– 40 °C to + 105 °C	•		•	
TL064C	0 °C to + 70 °C	•		•	
TL064AC	0 °C to + 70 °C	•		•	
TL064BC	0 °C to + 70 °C	•		•	

Note : Hi-Rel versions available
Examples : TL064 MJ, TL064 CN

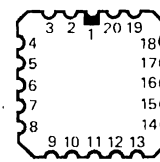
PIN CONNECTIONS (Top views)

DIP14
CERDIP14
SO14



1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^{+}
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - Output 3
9 - Inverting input 3
10 - Non-inverting input 3
11 - V_{CC}^{-}
12 - Non-inverting input 4
13 - Inverting input 4
14 - Output 4

LCC20



1 - NC
2 - Output 1
3 - Inverting input 1
4 - Non-inverting input 1
5 - NC
6 - V_{CC}^{+}
7 - NC
8 - Non-inverting input 2
9 - Inverting input 2
10 - Output 2
11 - NC
12 - Output 3
13 - Inverting input 3
14 - Non-inverting input 3
15 - NC
16 - V_{CC}^{-}
17 - NC
18 - Non-inverting input 4
19 - Inverting input 4
20 - Output 4

MAXIMUM RATINGS

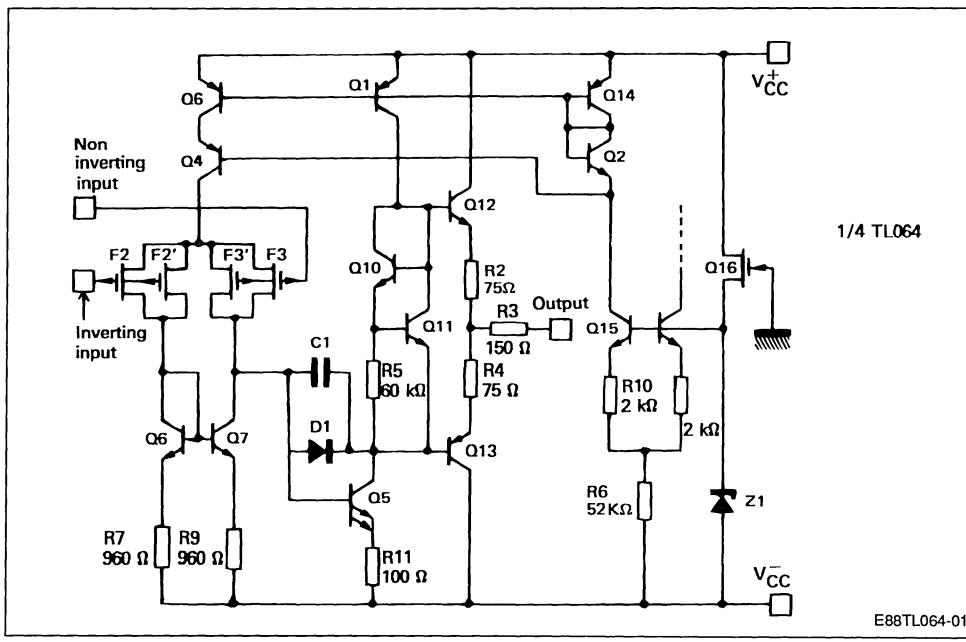
Symbol	Parameter	TL064M	TL064I	TL064C	Unit
V_{CC}	Supply Voltage (note 1)	± 18	± 18	± 18	V
V_{ID}	Differential Input Voltage (note 2)	± 30	± 30	± 30	V
V_I	Input Voltage (note 3)	± 15	± 15	± 15	V
	Ouput Short-circuit Duration (note 4)	Indefinite	Indefinite	Indefinite	
P_{tot}	Power Dissipation (note 5)	680	680	680	mW
T_{oper}	Operating Free-air, Temperature Range	− 55 to + 125	− 40 to + 105	0 to + 70	°C
T_{stg}	Storage Temperature Range	− 65 to +150	− 65 to + 150	− 65 to + 150	°C

* Devices bonded on a 6 cm x 0.15 cm glass epoxy substrate with 30 mm^2 of 35 µm thick copper.

Notes : 1. All voltage values, except differential voltages, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.

2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. For operation above + 25 °C free-air temperature, refer to dissipation derating table.

SCHEMATIC DIAGRAM



Case	V_{cc}^-	V_{cc}^+	Output	Non-inverting Input	Inverting Input	N.C.
DIP14 CERDIP14 SO14	11	4	1, 7, 8, 14	3, 5, 10, 12	2, 6, 9, 13	
LCC20	16	6	2, 10, 12, 20	4, 8, 14, 18	3, 9, 13, 19	*

* **LCC20** : Other pins are not connected.

ELECTRICAL CHARACTERISTICS

TL064M : – 55 °C ≤ T_{amb} ≤ + 125 °C
TL064I : – 40 °C ≤ T_{amb} ≤ + 105 °C
TL064C : 0 °C ≤ T_{amb} ≤ + 70 °C
V_{CC} = ± 15V.
All characteristics are specified under open-loop conditions unless otherwise specified.

Symbol	Parameter	TL064M			TL064I			TL064C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage (R_S = 50 Ω) T_{amb} = + 25 °C $T_{min} \le T_{amb} \le T_{max}$		3	6 15		3	6 9		3	15 20	mV
αV_{IO}	Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω)		10			10			10		µV/°C
I_{IO}	Input Offset Current * T_{amb} = + 25 °C $T_{min} \le T_{amb} \le T_{max}$		5	100 20		5	100 10		5	200 5	pA nA
I_{IB}	Input bias Current * T_{amb} = + 25 °C $T_{min} \le T_{amb} \le T_{max}$		30	200 50		30	200 20		30	400 10	pA nA
V_I	Input Common-mode Voltage Range (T_{amb} = + 25 °C)	±11	±12		±11.5	±12		±10	±11		V
V_{OPP}	Output Voltage Swing : R_L = 10 kΩ, T_{amb} = + 25 °C $R_L \ge$ 10 kΩ, $T_{min} \le T_{amb} \le T_{max}$	20 20	27		20 20	27		20 20	27		V
A_{VD}	Large Signal Voltage Gain ($R_L \ge$ 10 kΩ, V_O = ± 10 V) T_{amb} = + 25 °C $T_{min} \le T_{amb} \le T_{max}$	4 4	6		4 4	6		3 3	6		V/mV
GW_R	Small Signal Bandwidth (T_{amb} = + 25 °C, R_L = 10 kΩ)		1			1			1		MHz
R_I	Input Resistance (T_{amb} = + 25 °C)		10^{12}			10^{12}			10^{12}		Ω
CMR	Common-mode Rejection Ratio ($R_S \le$ 10 kΩ, T_{amb} = + 25 °C)	80	86		80	86		70	76		dB
SVR	Supply Voltage Rejection Ratio ($\Delta V_{CC}/\Delta V_{IO}$) $R_S \le$ 10 kΩ, T_{amb} = + 25 °C	80	95		80	95		70	95		dB
I_{CC}	Supply Current (per amplifier) T_{amb} = + 25 °C, no Load, no Signal		200	250		200	250		200	250	µA
V_{O1}/V_{O2}	Channel Separation (A_{VD} = 100, T_{amb} = + 25 °C)		120			120			120		dB
P_D	Total Power Consumption (each amplifier) T_{amb} = + 25 °C, no Load, no Signal		6	7.5		6	7.5		6	7.5	mW

* Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

ELECTRICAL CHARACTERISTICS

V_{CC} = ± 15V, T_{amb} = + 25 °C.

Symbol	Parameter	TL064M			TL064I, C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
S_{VO}	Slew Rate (e_I = 10 V, R_L = 10 kΩ, C_L = 100 pF, A_V = 1)	2	3.5			3.5		V/µs
t_r	Rise Time (e_I = 20 mV, R_L = 10 kΩ, C_L = 100 pF, A_V = 1) (see fig. 1)		0.2			0.2		µs
K_{OV}	Overshoot Factor (e_I = 20 mV, R_L = 10 kΩ, C_L = 100 pF, A_V = 1) (see fig. 1)		10			10		%
V_n	Equivalent Input Noise Voltage (R_S = 100 kΩ, f = 1 kHz)		42			42		nV/√Hz

ELECTRICAL CHARACTERISTICS

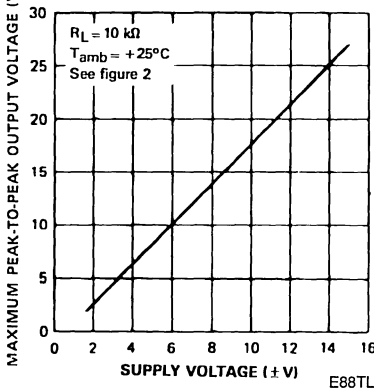
TL064C : 0 °C ≤ T_{amb} ≤ + 70 °C
V_{CC} = ± 15V
All characteristics are specified under open-loop conditions unless otherwise specified.

Symbol	Parameter	TL064C			TL064AC			TL064BC			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage (R_S = 50 Ω) T_{amb} = + 25 °C $T_{min} \le T_{amb} \le T_{max}$		3	15 20		3	6 7.5		2	3 5	mV
αV_{IO}	Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω)		10			10			10		µV/°C
I_{IO}	Input Offset Current * T_{amb} = + 25 °C $T_{min} \le T_{amb} \le T_{max}$		5	200 5		5	100 3		5	100 3	pA nA
I_{IB}	Input bias Current * T_{amb} = + 25 °C $T_{min} \le T_{amb} \le T_{max}$		30	400 10		30	200 7		30	200 7	pA nA
V_I	Input Common-mode Voltage Range (T_{amb} = + 25 °C)	±10	±11		±11.5	±12		±11.5	±12		V
V_{OPP}	Output Voltage Swing : R_L = 10 kΩ, T_{amb} = + 25 °C $R_L \ge$ 10 kΩ, $T_{min} \le T_{amb} \le T_{max}$	20 20	27		20 20	27		20 20	27		V
A_{VD}	Large Signal Voltage Gain ($R_L \ge$ 10 kΩ, V_O = ± 10 V) T_{amb} = + 25 °C $T_{min} \le T_{amb} \le T_{max}$	3 3	6		4 4	6		4 4	6		V/mV
GW_R	Small Signal Bandwidth (T_{amb} = + 25 °C, R_L = 10 kΩ)		1			1			1		MHz
R_I	Input Resistance (T_{amb} = + 25 °C)		10^{12}			10^{12}			10^{12}		Ω
CMR	Common-mode Rejection Ratio ($R_S \le$ 10 kΩ, T_{amb} = + 25 °C)	70	76		80	86		80	86		dB
SVR	Supply Voltage Rejection Ratio ($\Delta V_{CC}/\Delta V_{IO}$) $R_S \le$ 10 kΩ, T_{amb} = + 25 °C	70	95		80	95		80	95		dB
I_{CC}	Supply Current (per amplifier) T_{amb} = + 25 °C, no Load, no Signal		200	250		200	250		200	250	µA
V_{O1}/V_{O2}	Channel Separation (A_{VD} = 100, T_{amb} = + 25 °C)		120			120			120		dB
P_D	Total Power Consumption (each amplifier) T_{amb} = + 25 °C, no Load, no Signal		6	7.5		6	7.5		6	7.5	mW

* Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

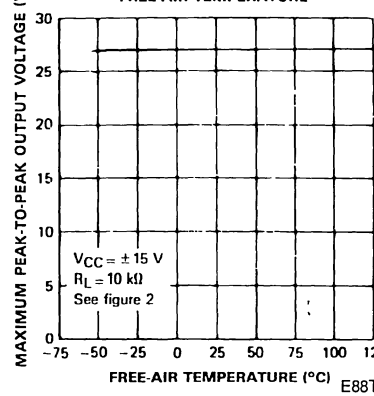
TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE



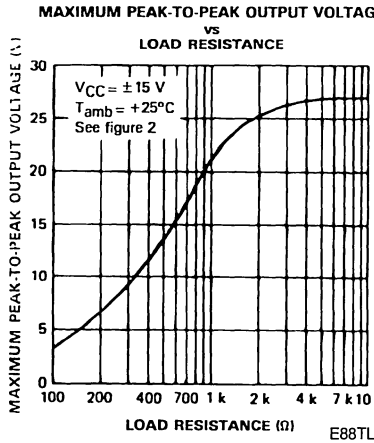
E88TL064-02

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE



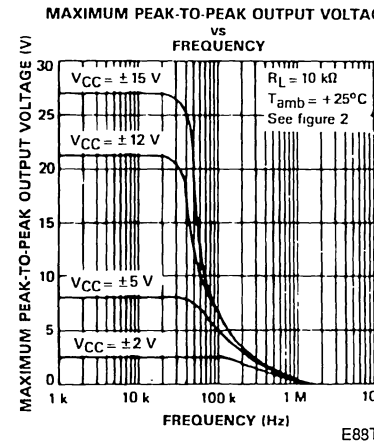
E88TL064-03

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE



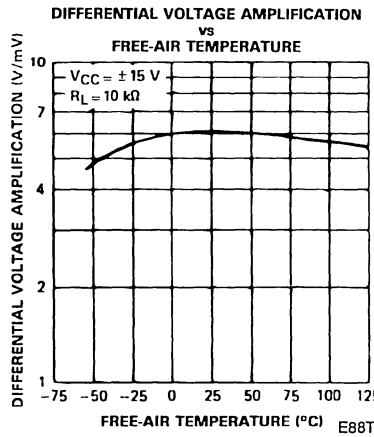
E88TL064-04

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY



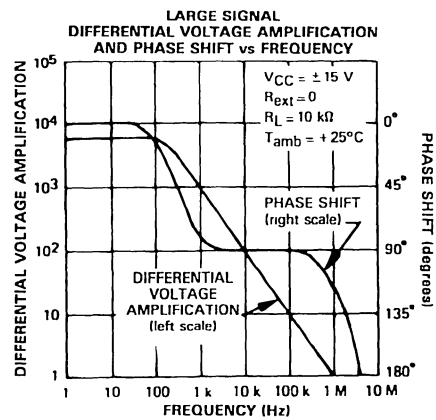
E88TL064-05

DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE



E88TL064-06

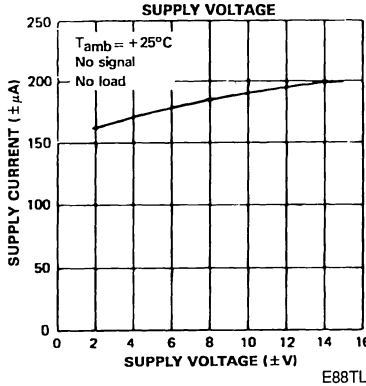
LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY



E88TL064-07

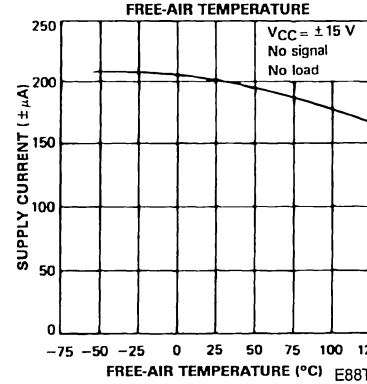
TYPICAL CHARACTERISTICS (continued)

SUPPLY CURRENT PER AMPLIFIER vs SUPPLY VOLTAGE



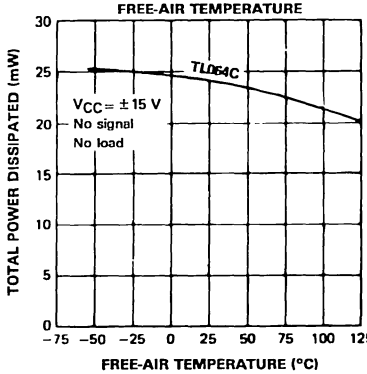
E88TL064-08

SUPPLY CURRENT PER AMPLIFIER vs FREE-AIR TEMPERATURE



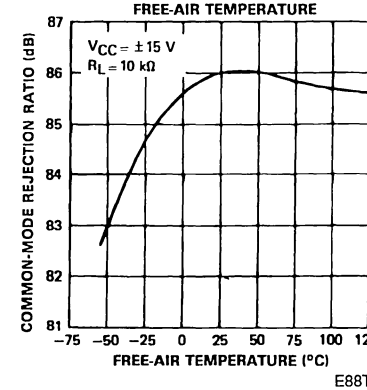
E88TL064-09

TOTAL POWER DISSIPATED vs FREE-AIR TEMPERATURE



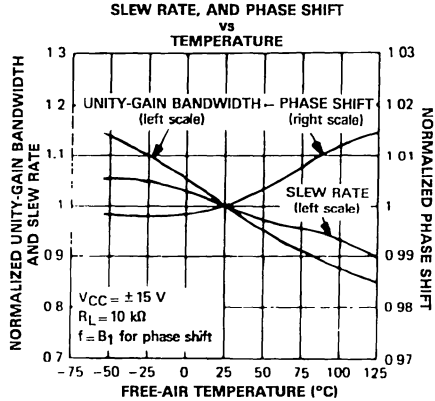
E88TL064-10

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE



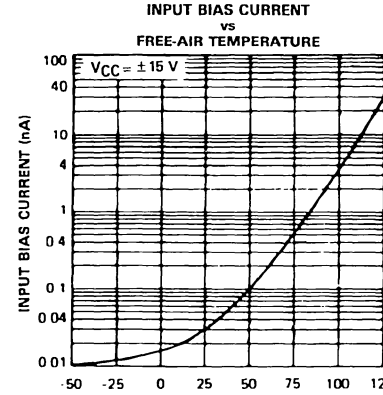
E88TL064-11

NORMALIZED UNITY-GAIN BANDWIDTH SLEW RATE, AND PHASE SHIFT vs TEMPERATURE



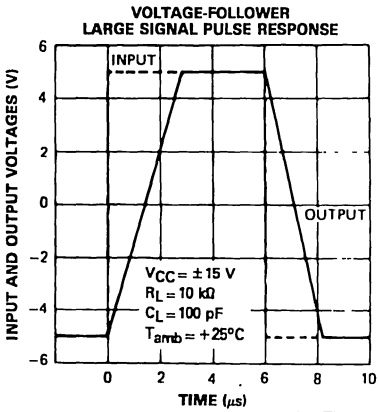
E88TL064-12

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

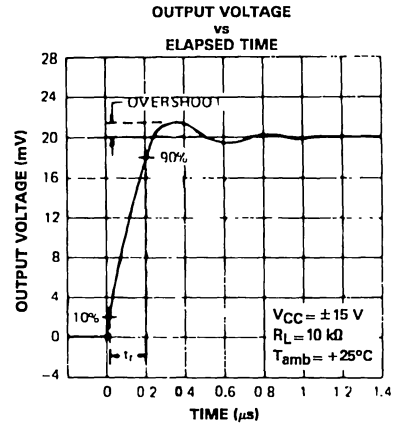


E88TL064-13

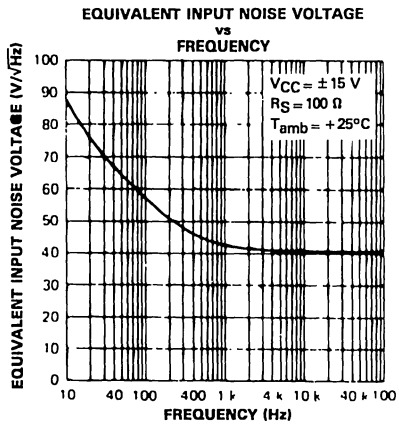
TYPICAL CHARACTERISTICS (continued)



E88TL064-14



E88TL064-15



E88TL064-16

PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage follower.

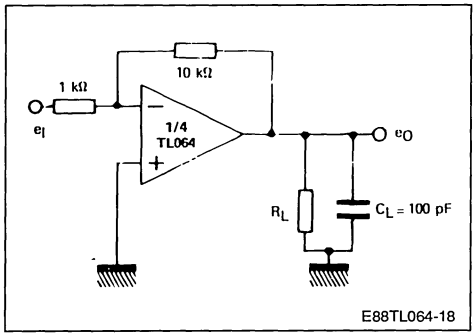
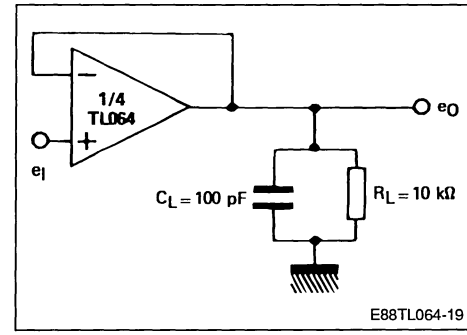
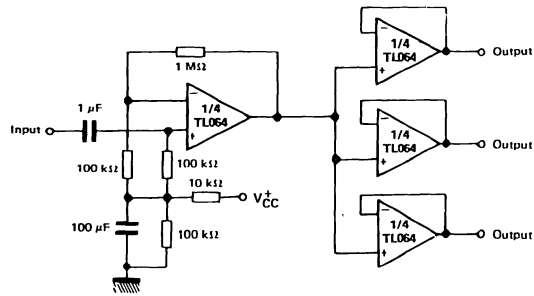


Figure 2 : Gain-of-10 inverting amplifier.



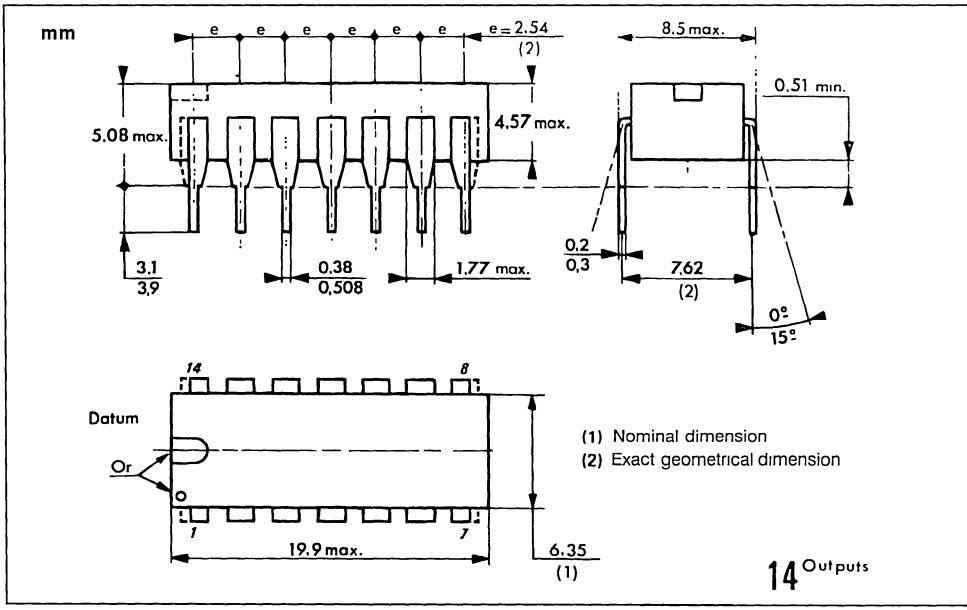
TYPICAL APPLICATION

AUDIO DISTRIBUTION AMPLIFIER

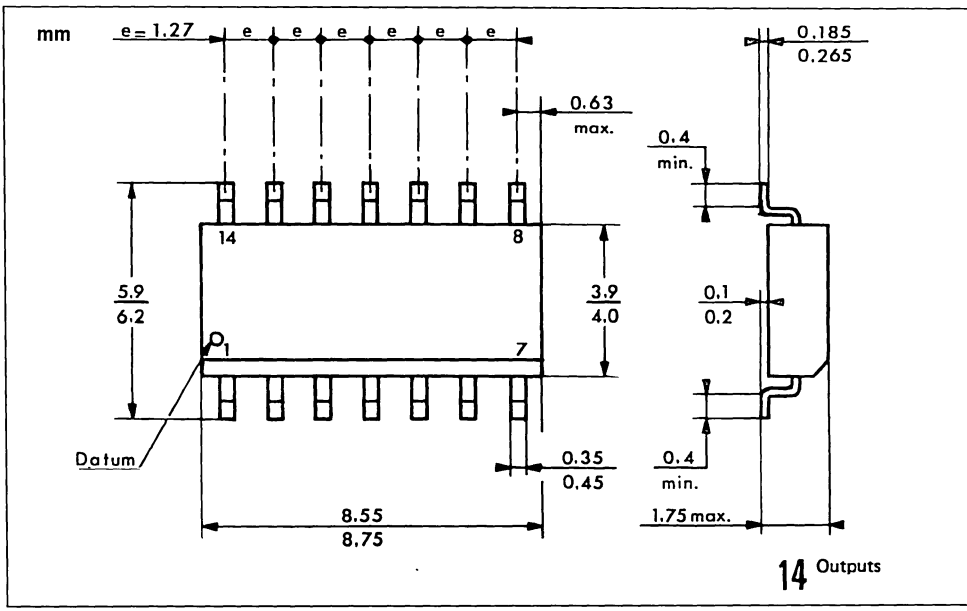


PACKAGE MECHANICAL DATA

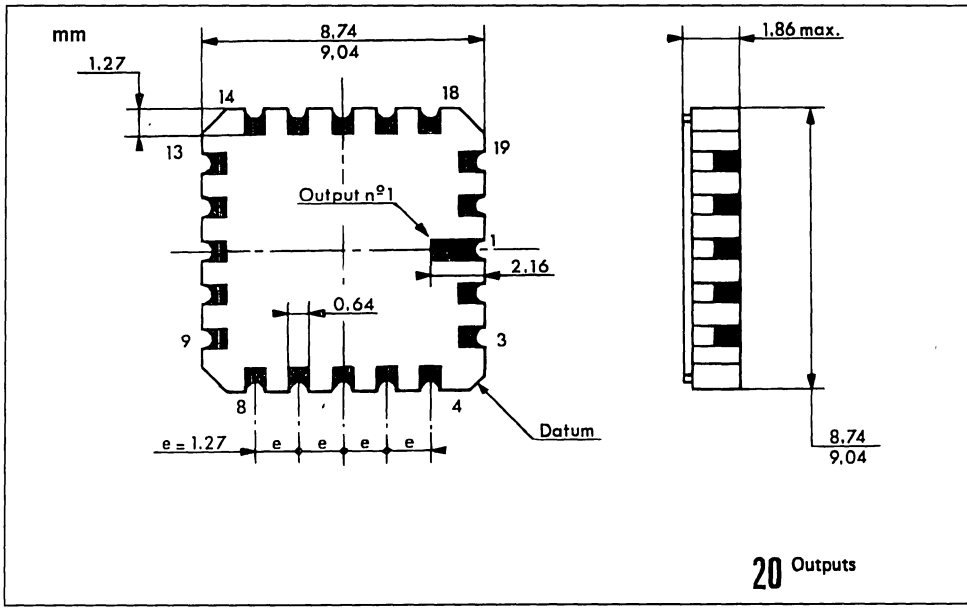
14 PINS – PLASTIC DIP OR CERDIP



14 PINS – PLASTIC MICROPACKAGE (SO)



20 PINS – TRICECOP (LCC)



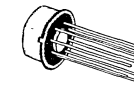
SGS-THOMSON MICROELECTRONICS

TL071
TL071A-TL071B

LOW NOISE J-FET INPUT SINGLE OP-AMPs

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- LOW NOISE V_n = 18 nV/√ Hz (typ)
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J–FET INPUT STAGE
- LOW HARMONIC DISTORTION : 0.01 % (typ)
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 13 V/µs (typ)

N
DIP8
(Plastic package)



H
TO-99
(Metal can)

D
SO8
(Plastic micropackage)

GC
LCC20
(Tricecop - LCC)

ORDER CODES

Part Number	Temperature Range	Package			
		N	H	D	GC
TL071M	– 55 °C to + 125 °C		•		•
TL071I	– 40 °C to + 105 °C	•		•	
TL071C	0 °C to + 70 °C	•		•	
TL071AC	0 °C to + 70 °C	•		•	
TL071BC	0 °C to + 70 °C	•		•	

Note : Hi-Rel Versions Available
Examples : TL071 MH, TL071 CN

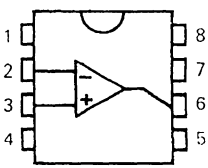
DESCRIPTION

The TL071, TL071A and TL071B are high speed J–FET input single operational amplifiers incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rate, low input bias and, offset current, and low voltage temperature coefficient.

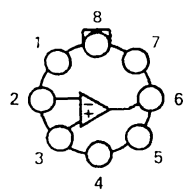
PIN CONNECTIONS (Top views)

DIP8
SO8



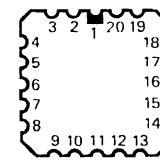
1 - Offset null
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-

TO-99



5 - Offset null
6 - Output
7 - V_{CC}^+
8 - NC

LCC20



1 - NC
2 - Offset null
3 - NC
4 - NC
5 - Inverting input
6 - NC
7 - Non-inverting input
8 - NC
9 - NC
10 - V_{CC}^-
11 - NC
12 - Offset null
13 - NC
14 - NC
15 - Output
16 - NC
17 - V_{CC}^+
18 - NC
19 - NC
20 - NC

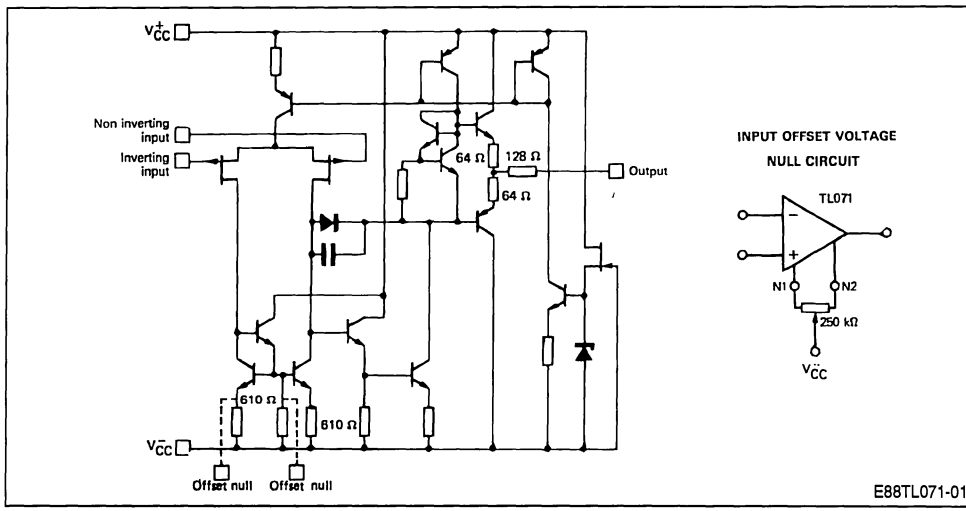
MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	± 18	V
V_i	Input Voltage (note 3)	± 15	V
V_{ID}	Diff. Input Voltage (note 2)	± 30	V
P_{tot}	Power Dissipation	680	mW
	Ouput Short-circuit Duration (note 4)	Indefinite	
T_{oper}	Operating Free-air Temperature Range TL071C, AC, BC TL071I, BI TL071M	 0 to 70 – 40 to 105 – 55 to 125	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C

Notes : 1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.

2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

SCHEMATIC DIAGRAM



Case	Balance	Inverting Input	Non-Inverting Input	V_{CC}^-	V_{CC}^+	Output	N.C.
DIP8 SO8 TO-99	1, 5	2	3	4	7	6	8
LCC20	2, 12	5	7	10	17	15	*

* **LCC20** : Other pins are not connected.

ELECTRICAL CHARACTERISTICS

V_{CC} = ± 15 V (unless otherwise specified)
TL071M : − 55 °C ≤ T_{amb} ≤ + 125 °C
TL071I, BI : − 40 °C ≤ T_{amb} ≤ + 105 °C
TL071C, AC, BC: 0 °C ≤ T_{amb} ≤ + 70 °C

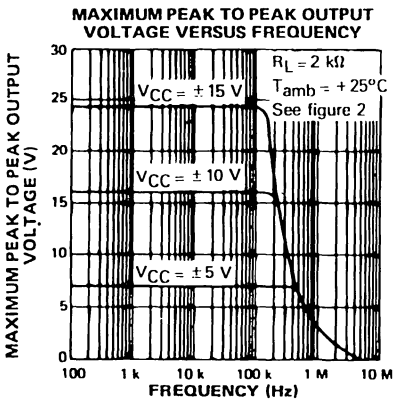
Symbol	Parameter	TL071M, I, BI TL071BC, AC			TL071C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage							mV
	T_{amb} = 25 °C (Rs ≤ 10 kΩ)		3	5		3	8	
	TL071BI, BC		1	3				
	$T_{min} \le T_{amb} \le T_{max}$			9			13	
	TL071BI, BC			5				
αV_{IO}	Input Offset Voltage Drift		10			10		µV/°C
I_{IO}	Input Offset Current *							
	T_{amb} = 25 °C		5	50		5	50	pA
	$T_{min} \le T_{amb} \le T_{max}$			4			4	nA
I_{IB}	Input Bias Current *							
	T_{amb} = 25 °C		20	200		20	200	pA
	$T_{min} \le T_{amb} \le T_{max}$			20			20	nA
A_{VD}	Large Signal Voltage Gain							V/mV
	(R_L ≥ 2 kΩ, V_O = ± 10 V)							
	T_{amb} = 25 °C	50	200		50	200		
	$T_{min} \le T_{amb} \le T_{max}$	25			25			
SVR	Supply Voltage Rejection Ratio							dB
	(R_S ≤ 10 kΩ)							
	T_{amb} = 25 °C	80	86		80	86		
	$T_{min} \le T_{amb} \le T_{max}$	80			80			
I_{CC}	Supply Current, no Load							mA
	T_{amb} = 25 °C		1.4	2.5		1.4	2.5	
	$T_{min} \le T_{amb} \le T_{max}$			2.5			2.5	
V_I	Input Voltage Range	− 11		+ 11	− 11		+ 11	V
CMR	Common Mode Rejection Ratio							dB
	(R_S ≤ 10 kΩ)							
	T_{amb} = 25 °C	80	86		70	86		
	$T_{min} \le T_{amb} \le T_{max}$	80			70			
I_{OS}	Output Short-circuit Current							mA
	T_{amb} = 25 °C	10	40	60	10	40	60	
	$T_{min} \le T_{amb} \le T_{max}$	10		60	10		60	
± V_{OPP}	Output Voltage Swing							V
	T_{amb} = 25 °C R_L ≥ 2 kΩ	11	12		11	12		
	R_L ≥ 10 kΩ	12	13.5		12	13.5		
	$T_{min} \le T_{amb} \le T_{max}$ R_L ≥ 2 kΩ	11			11			
	R_L ≥ 10 kΩ	12			12			
S_{VO}	Slew-rate (V_I = 10 V, R_L = 2 kΩ							V/µs
	C_L ≤ 100 pF, T_{amb} = 25 °C, unity gain)	12	16		8	16		
t_r	Rise Time							µs
	(V_I = 20 mV, R_L = 2 kΩ							
	C_L = 100 pF, T_{amb} = 25 °C, unity gain)		0.1			0.1		

* The input bias currents are junction leakage currents wich approximatevely double for every 10 °C increase in the junction temperature.

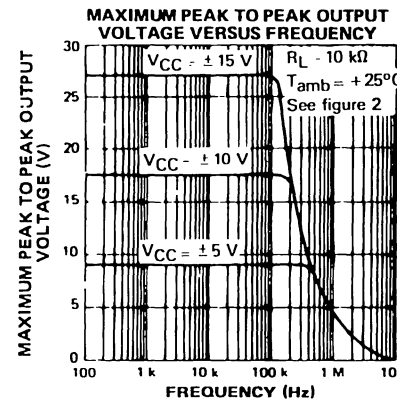
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	TL071M, I, BI TL071BC, AC			TL071C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
K_{OV}	Overshoot (V_I = 20 mV, R_L = 2 kΩ $C_L \leq 100$ pF, T_{amb} = 25 °C, unity gain)		10			10		%
GBP	Gain Bandwidth Product (f = 100 kHz, T_{amb} = 25 °C V_{IN} = 10 mV, R_L = 2 kΩ, C_L = 100 pF) TL071BI, BC	2.5 3.3	4.0 4.0	5.0 5.0	2.5	4 0	5.0	MHz
R_I	Input Resistance (T_{amb} = 25 °C)		10^{12}			10^{12}		Ω
THD	Total Harmonic Distortion (f = 1 kHz, A_V = 20 dB, R_L = 2 kΩ $C_L \leq 100$ pF, T_{amb} = 25 °C, V_O = 2 V_{PP})		0.01			0.01		%
V_n	Equivalent Input Noise Voltage (f = 1 kHz, R_g = 100 Ω)		15			15		nV/√Hz
Øm	Phase Margin		45			45		Degrees

TYPICAL CHARACTERISTICS



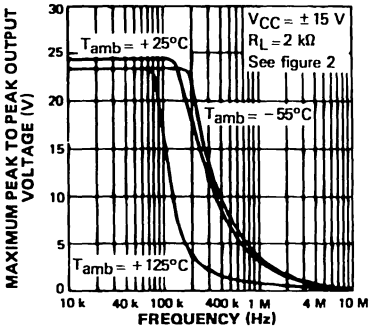
E88TL071-02



E88TL071-03

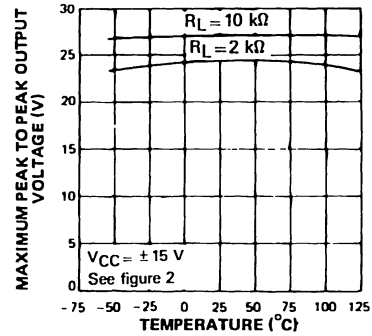
TYPICAL CHARACTERISTICS (continued)

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



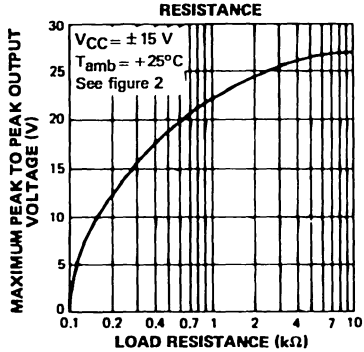
E88TL071-04

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREE-AIR TEMP.



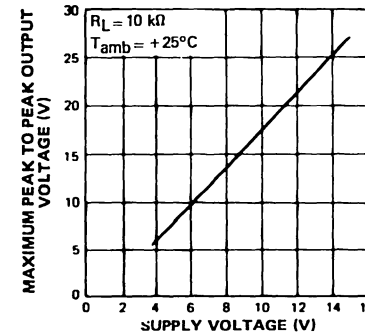
E88TL071-05

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



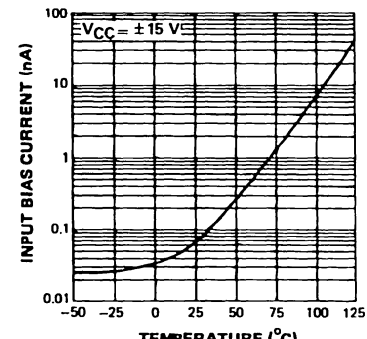
E88TL071-06

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



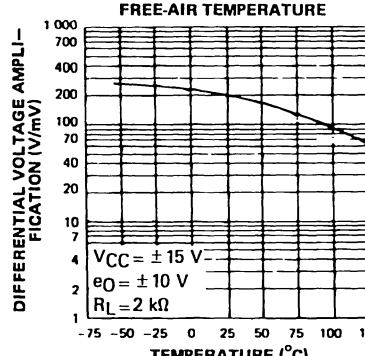
E88TL071-07

INPUT BIAS CURRENT VERSUS FREE-AIR TEMPERATURE



E88TL071-08

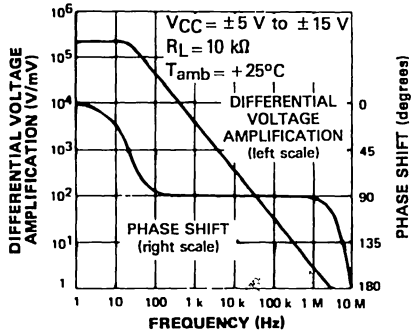
LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE-AIR TEMPERATURE



E88TL071-09

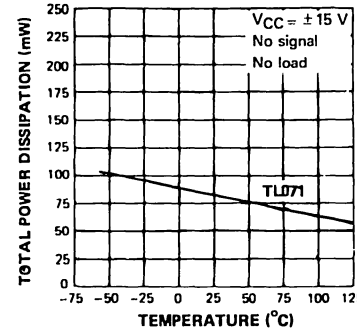
TYPICAL CHARACTERISTICS (continued)

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



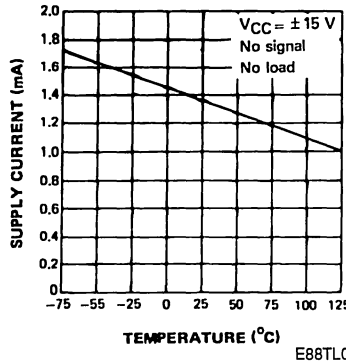
E88TL071-10

TOTAL POWER DISSIPATION VERSUS FREE-AIR TEMPERATURE



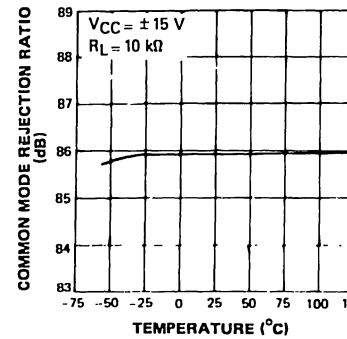
E88TL071-11

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE-AIR TEMPERATURE



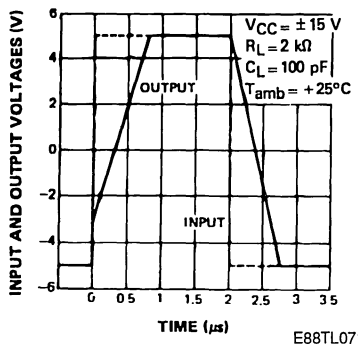
E88TL071-12

COMMON MODE REJECTION RATIO VERSUS FREE-AIR TEMPERATURE



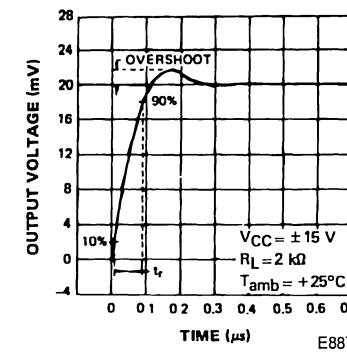
E88TL071-13

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



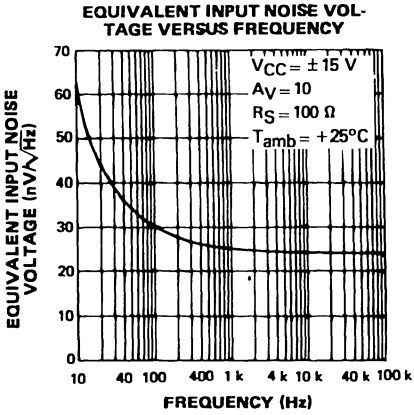
E88TL071-14

OUTPUT VOLTAGE VERSUS TIME

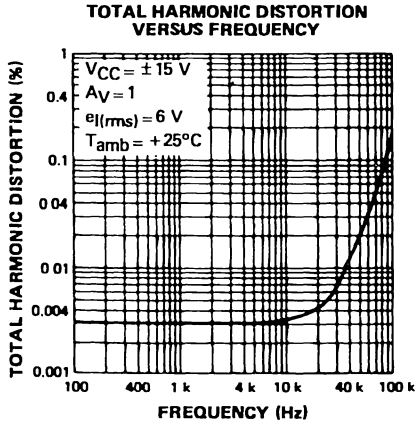


E88TL071-15

TYPICAL CHARACTERISTICS (continued)



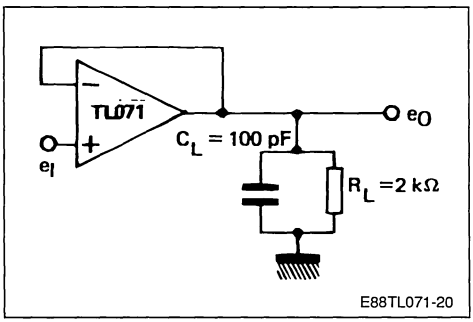
E88TL071-16



E88TL071-17

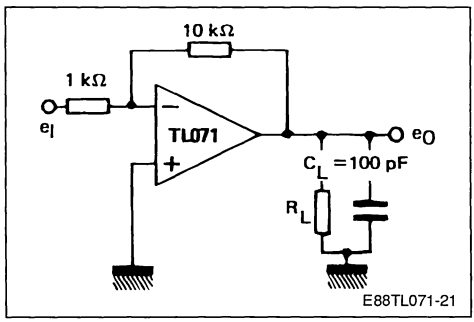
PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage follower.



E88TL071-20

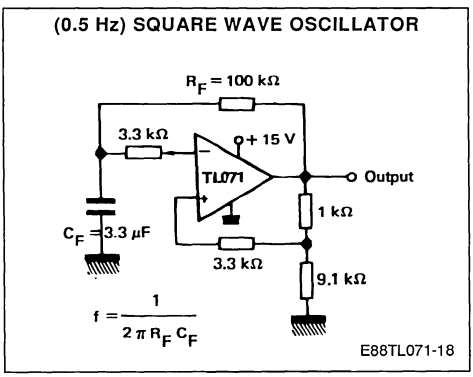
Figure 2 : Gain-of-10 inverting amplifier.



E88TL071-21

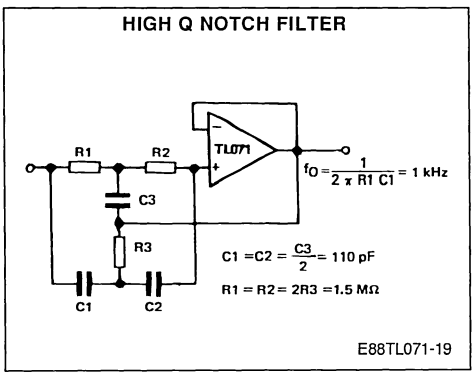
TYPICAL APPLICATIONS

(0.5 Hz) SQUARE WAVE OSCILLATOR



E88TL071-18

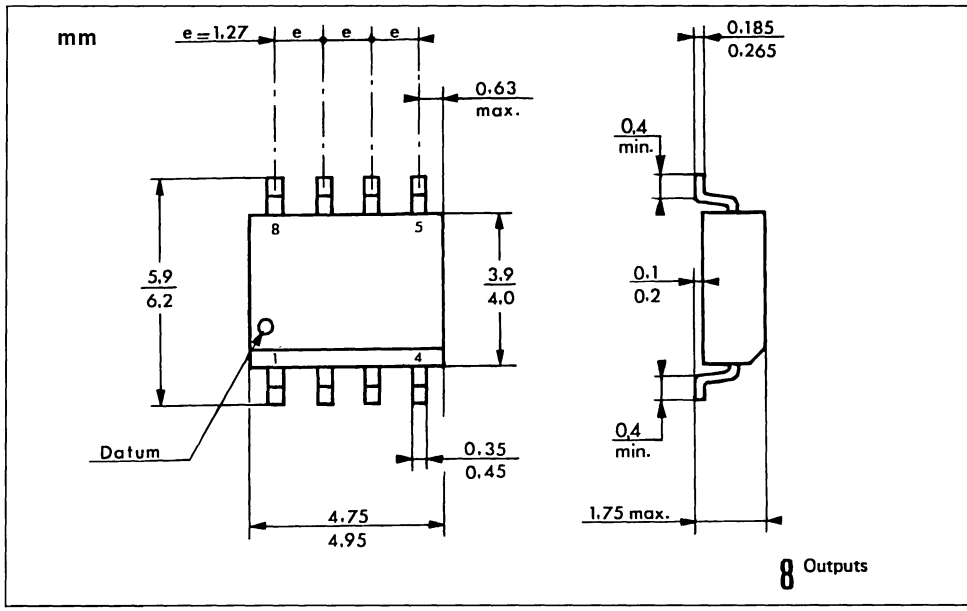
HIGH Q NOTCH FILTER



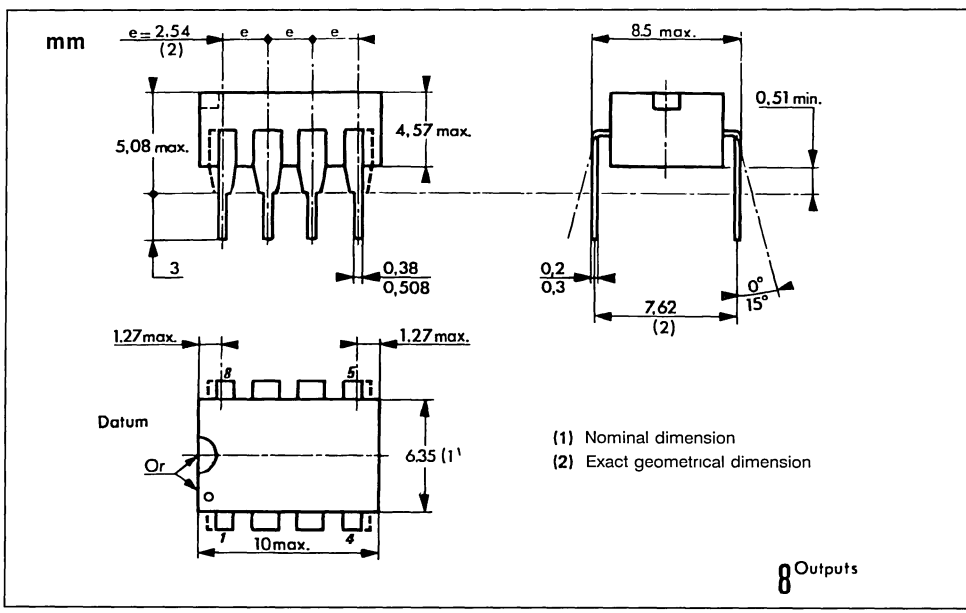
E88TL071-19

PACKAGE MECHANICAL DATA

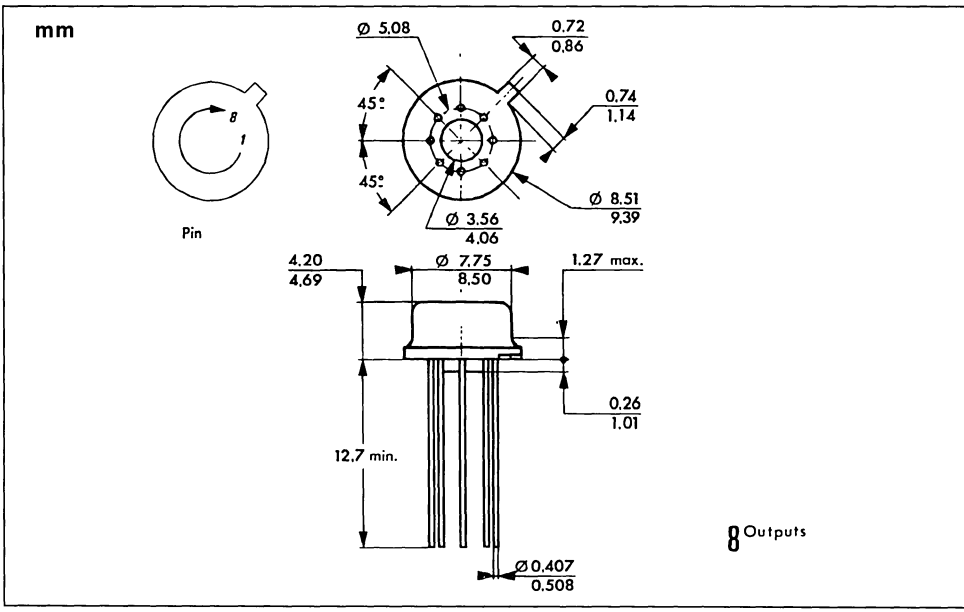
8 PINS – PLASTIC MICROPACKAGE (SO)



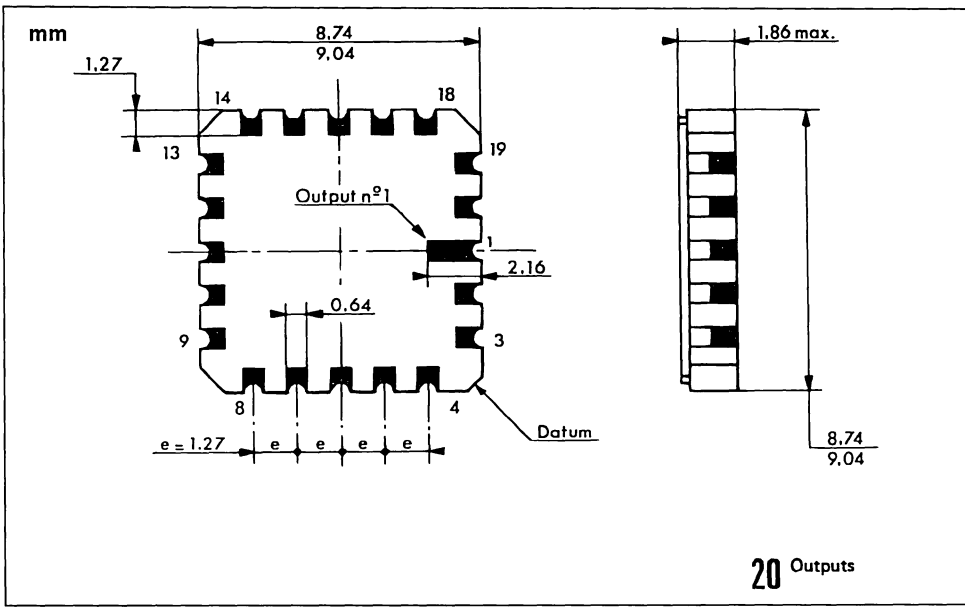
8 PINS – PLASTIC DIP



TO-99 – METAL CAN



20 PINS – TRICECOP (LCC)

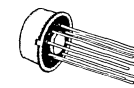


TL072
TL072A-TL072B

LOW NOISE J-FET INPUT DUAL OP–AMPs

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- LOW NOISE V_n = 18 nV /$\sqrt{Hz}$ (typ)
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J–FET INPUT STAGE
- LOW HARMONIC DISTORTION : 0.01 % (typ)
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 13 V/µs (typ)

N
DIP8
(Plastic package)



H
TO-99
(Metal can)

D
SO8
(Plastic micropackage)

GC
LCC20
(Tricecop LCC)

ORDER CODES

Part Number	Temperature Range	Package			
		N	H	D	GC
TL072M	– 55 °C to + 125 °C		•		•
TL072I	– 40 °C to + 105 °C	•		•	
TL072C	0 °C to + 70 °C	•		•	
TL072AC	0 °C to + 70 °C	•		•	
TL072BC	0 °C to + 70 °C	•		•	

Note : Hi-Rel Versions Available
Examples : TL072 MH, TL072 CN

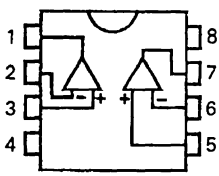
DESCRIPTION

The TL072, TL072A and TL072B are high speed J–FET input dual operational amplifiers incorporating well matched, high voltage J–FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

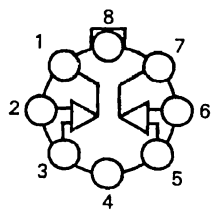
PIN CONNECTIONS (Top views)

DIP8
SO8



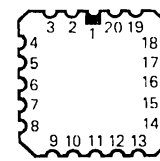
1 - Output
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-

TO-99



5 - Non-inverting input
6 - Inverting input
7 - Output
8 - V_{CC}^+

LCC20



1 - NC
2 - Output
3 - NC
4 - NC
5 - Inverting input
6 - NC
7 - Non-inverting input
8 - NC
9 - NC
10 - V_{CC}^-
11 - NC
12 - Non-inverting input
13 - NC
14 - NC
15 - Inverting input
16 - NC
17 - Output
18 - NC
19 - NC
20 - V_{CC}^+

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	± 18	V
V_I	Input Voltage (note 3)	± 15	V
V_{CC}	Diff Input Voltage (note 2)	± 30	V
P_{tot}	Power Dissipation	680	mW
	Output Short-circuit Duration (note 4)	Indefinite	
T_{oper}	Operating Free-air Temperature Range TL072C, AC, BC TL072I, BI TL072M	 0 to 70 – 40 to 105 – 55 to 125	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C

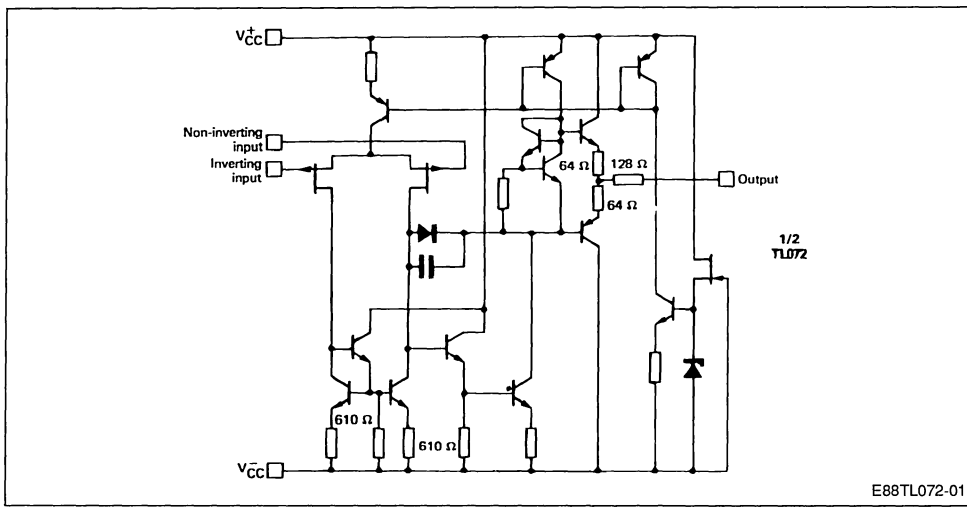
Notes : 1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.

2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.

3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less

4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

SCHEMATIC DIAGRAM



Case	Balance	Inverting Input	Non-inverting Input	V_{CC}^-	V_{CC}^+	Output	N.C.
DIP8 SO8 TO-99	1, 5	2	3	4	7	6	8
LCC20	2, 12	5	7	10	17	15	*

* **LCC20** : Other pins are not connected.

ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 15$ V (unless otherwise specified)
TL072M : $-55\ ^\circ C \leq T_{amb} \leq +125\ ^\circ C$
TL072I, BI : $-40\ ^\circ C \leq T_{amb} \leq +105\ ^\circ C$
TL072C, AC, BC : $0\ ^\circ C \leq T_{amb} \leq +70\ ^\circ C$

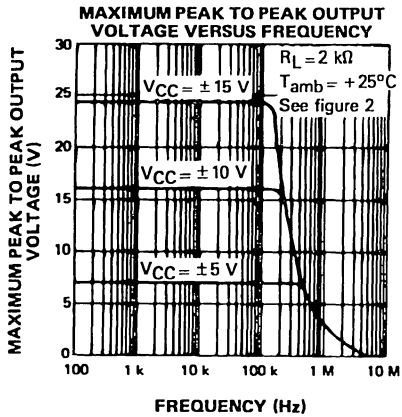
Symbol	Parameter	TL072M, I, BI TL072BC, AC			TL072C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage							mV
	T_{amb} = 25 °C (Rs ≤ 10 kΩ)		3	5		3	8	
	TL072BI, BC		1	3				
	$T_{min} \leq T_{amb} \leq T_{max}$			9			13	
	TL072BI, BC			5				
DV_{io}	Input Offset Voltage Drift		10			10		µV/°C
I_{io}	Input Offset Current *							
	T_{amb} = 25 °C		5	50		5	50	pA
	$T_{min} \leq T_{amb} \leq T_{max}$			4			4	nA
I_{ib}	Input Bias Current *							
	T_{amb} = 25 °C		20	200		20	200	pA
	$T_{min} \leq T_{amb} \leq T_{max}$			20			20	nA
A_{vd}	Large Signal Voltage Gain							V/mV
	($R_L \geq 2$ kΩ, $V_o = \pm 10$ V)							
	T_{amb} = 25 °C	50	200		50	200		
	$T_{min} \leq T_{amb} \leq T_{max}$	25			25			
SVR	Supply Voltage Rejection Ratio							dB
	($R_S \leq 10$ kΩ)							
	T_{amb} = 25 °C	80	86		80	86		
	$T_{min} \leq T_{amb} \leq T_{max}$	80			80			
I_{cc}	Supply Current, per Amp, no Load							mA
	T_{amb} = 25 °C		1.4	2.5		1.4	2.5	
	$T_{min} \leq T_{amb} \leq T_{max}$			2.5			2.5	
V_i	Input Voltage Range	−11		+11	−11		+11	V
CMR	Common Mode Rejection Ratio							dB
	($R_S \leq 10$ kΩ)							
	T_{amb} = 25 °C	80	86		70	86		
	$T_{min} \leq T_{amb} \leq T_{max}$	80			70			
I_{os}	Output Short-circuit Current							mA
	T_{amb} = 25 °C	10	40	60	10	40	60	
	$T_{min} \leq T_{amb} \leq T_{max}$	10		60	10		60	
$\pm V_{opp}$	Output Voltage Swing							V
	T_{amb} = 25 °C $R_L \geq 2$ kΩ	11	12		11	12		
	$R_L \geq 10$ kΩ	12	13.5		12	13.5		
	$T_{min} \leq T_{amb} \leq T_{max}$ $R_L \geq 2$ kΩ	11			11			
	$R_L \geq 10$ kΩ	12			12			
S_{vo}	Slew-rate (V_i = 10 V, R_L = 2 kΩ							V/µs
	$C_L \leq 100$ pF, T_{amb} = 25 °C, unity gain)	12	16		8	16		
t_r	Rise Time							µs
	(V_i = 20 mV, R_L = 2 kΩ							
	C_L = 100 pF, T_{amb} = 25 °C, unity gain)		0.1			0.1		

* The input bias currents are junction leakage currents wich approximatevely double for every 10 °C increase in the junction temperature.

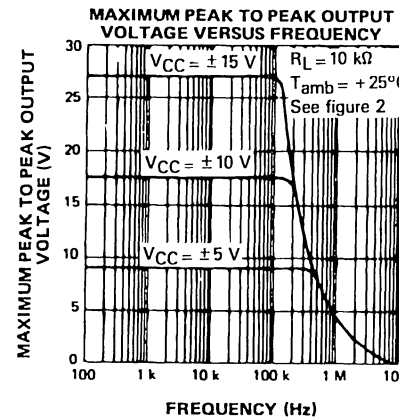
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	TL072M, I, BI TL072BC, AC			TL072C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
K_{ov}	Overshoot (V_i = 20 mV, R_L = 2 kΩ $C_L \leq$ 100 pF, T_{amb} = 25 °C, unity gain)		10			10		%
GBP	Gain Bandwidth Product (f = 100 kHz, T_{amb} = 25 °C V_{in} = 10 mV, R_L = 2 kΩ, C_L = 100 pF) TL082BI, BC	2.5 3.3	4.0 4.0	5.0 5.0	2.5	4 0	5.0	MHz
R_i	Input Resistance (T_{amb} = 25 °C)		10^{12}			10^{12}		Ω
THD	Total Harmonic Distortion (f = 1 kHz, A_v = 20 dB, R_L = 2 kΩ $C_L \leq$ 100 pF, T_{amb} = 25 °C, V_o = 2 V_{pp})		0.01			0.01		%
V_n	Equivalent Input Noise Voltage (f = 1 kHz, R_g = 100 Ω)		15			15		$nV/\sqrt{Hz}$
Øm	Phase Margin		45			45		Degrees
V_{o1}/V_{o2}	Channel Separation A_{vd} = 100, T_{amb} = 25 °C		120			120		dB

TYPICAL CHARACTERISTICS



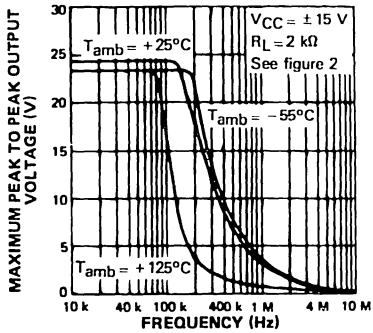
E88TL072-02



E88TL072-03

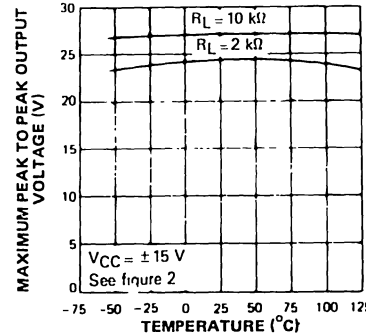
TYPICAL CHARACTERISTICS (continued)

MAXIMUM PEAK TO PEAK OUPUT VOLTAGE VERSUS FREE-AIR TEMP.



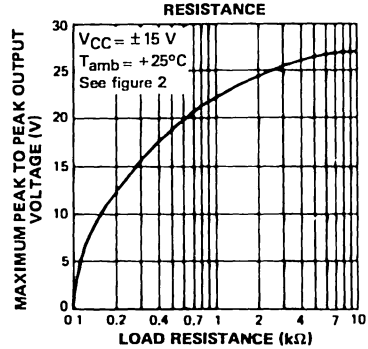
E88TL072-04

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



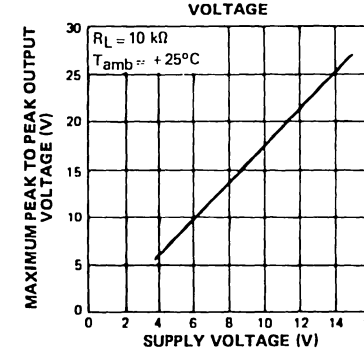
E88TL072-05

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



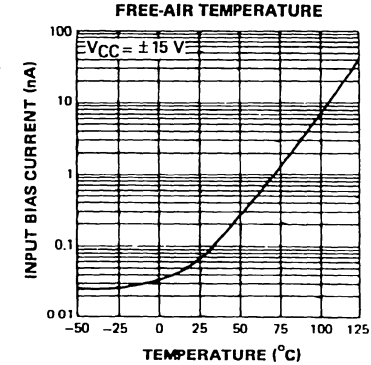
E88TL072-06

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



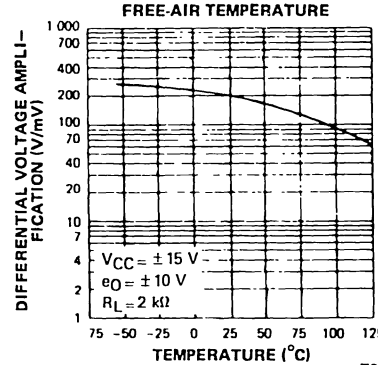
E88TL072-07

INPUT BIAS CURRENT VERSUS FREE-AIR TEMPERATURE



E88TL072-08

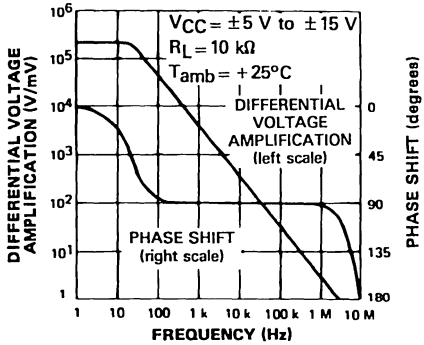
LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE-AIR TEMPERATURE



E88TL072-09

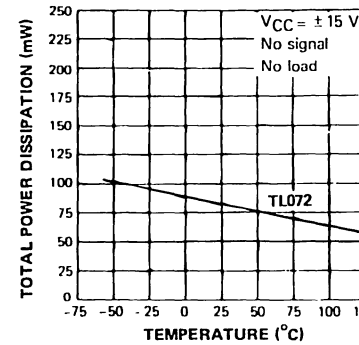
TYPICAL CHARACTERISTICS (continued)

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



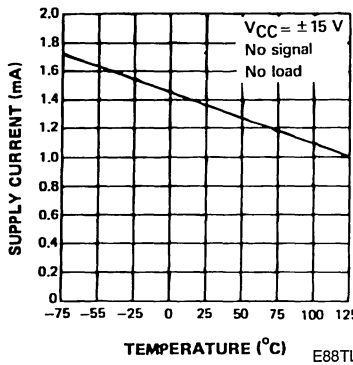
E88TL072-10

TOTAL POWER DISSIPATION VERSUS FREE-AIR TEMPERATURE



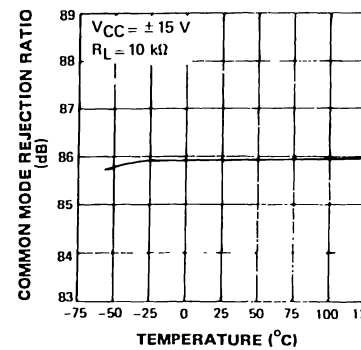
E88TL072-11

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE-AIR TEMPERATURE



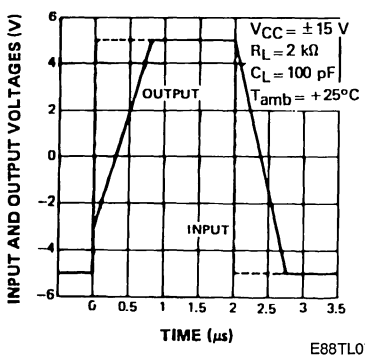
E88TL072-12

COMMON MODE REJECTION RATIO VERSUS FREE-AIR TEMPERATURE



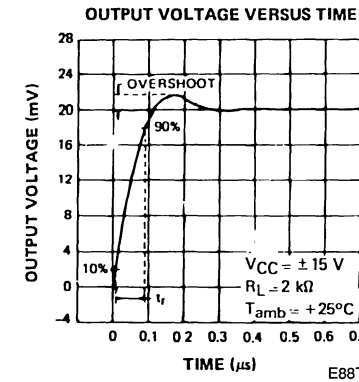
E88TL072-13

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



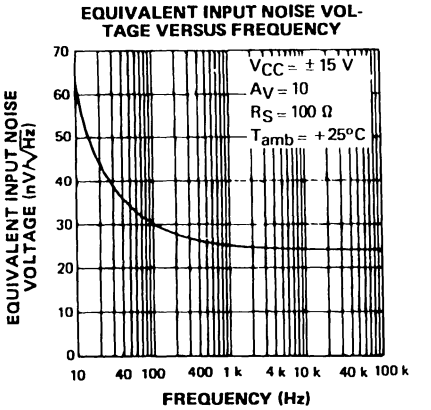
E88TL072-14

OUTPUT VOLTAGE VERSUS TIME

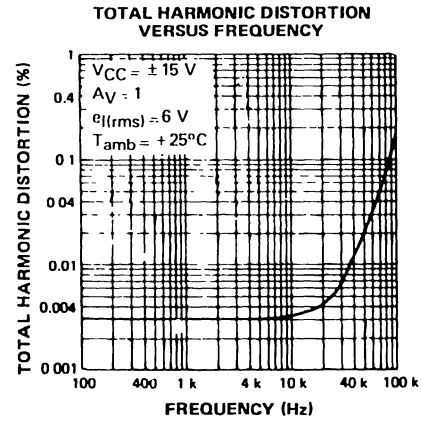


E88TL072-15

TYPICAL CHARACTERISTICS (continued)



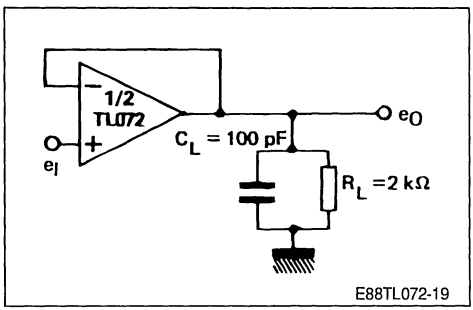
E88TL072-16



E88TL072-17

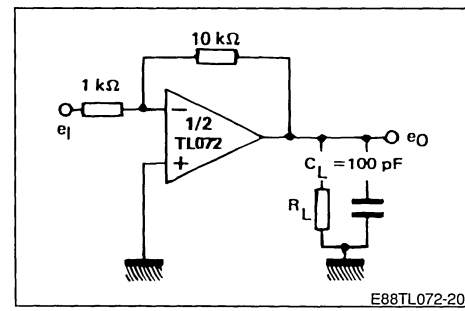
PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage follower.



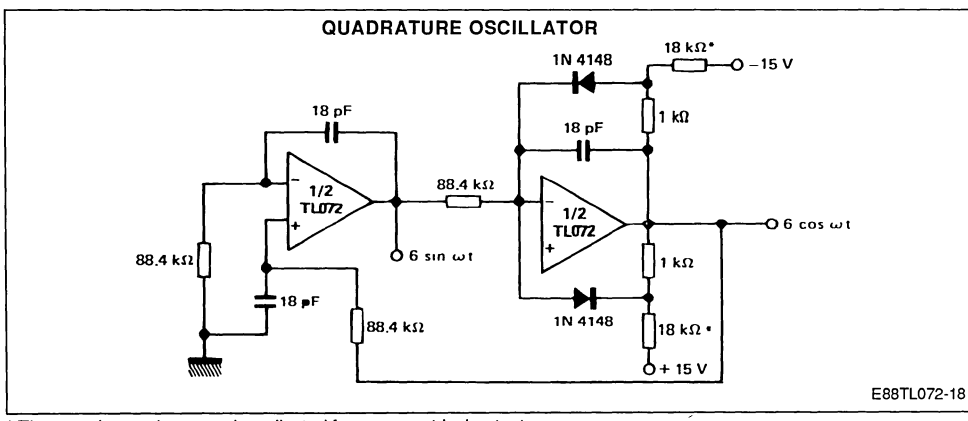
E88TL072-19

Figure 2 : Gain-of-10 inverting amplifier.



E88TL072-20

TYPICAL APPLICATION

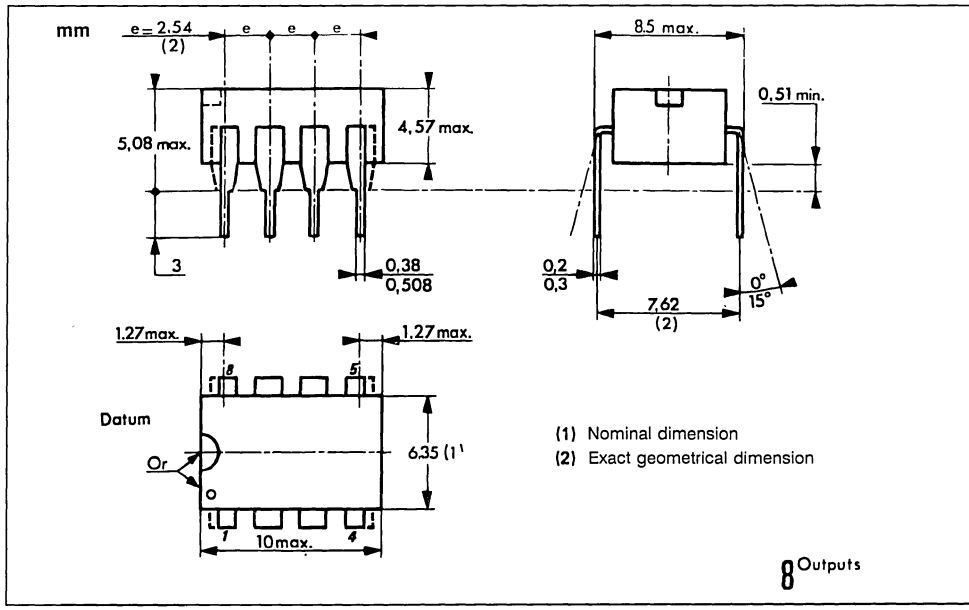


E88TL072-18

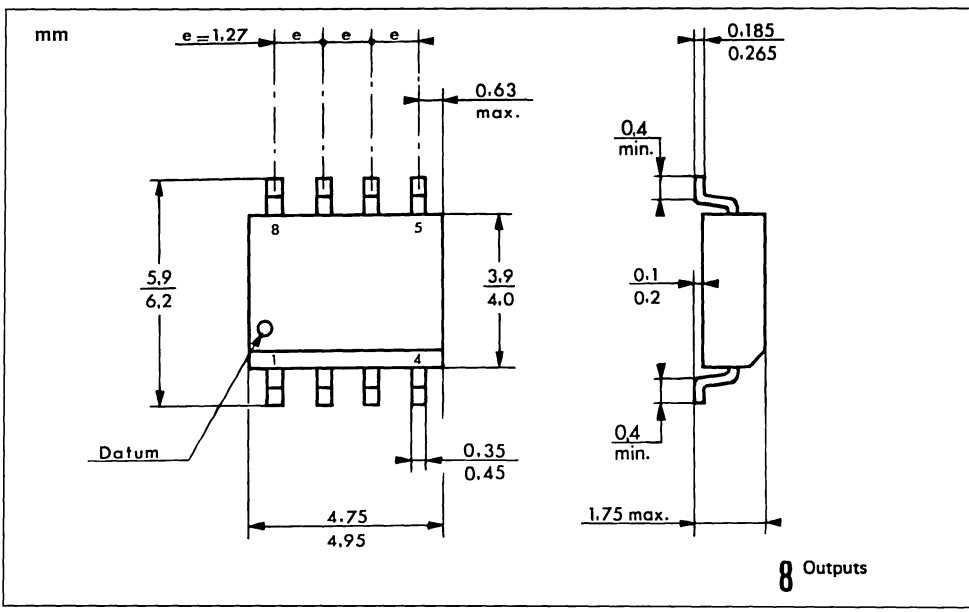
* These resistor values may be adjusted for a symmetrical output.

PACKAGE MECHANICAL DATA

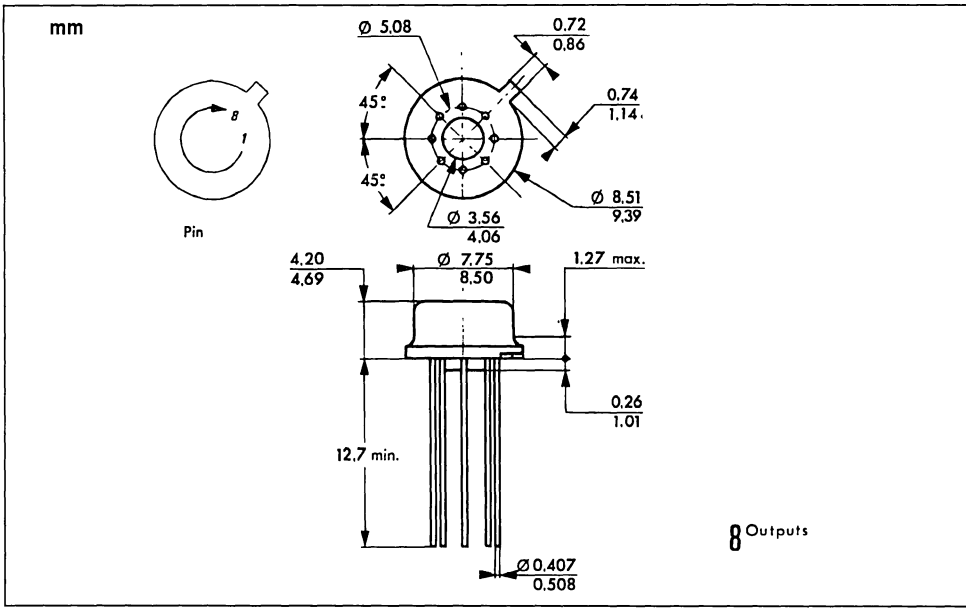
8 PINS – PLASTIC DIP



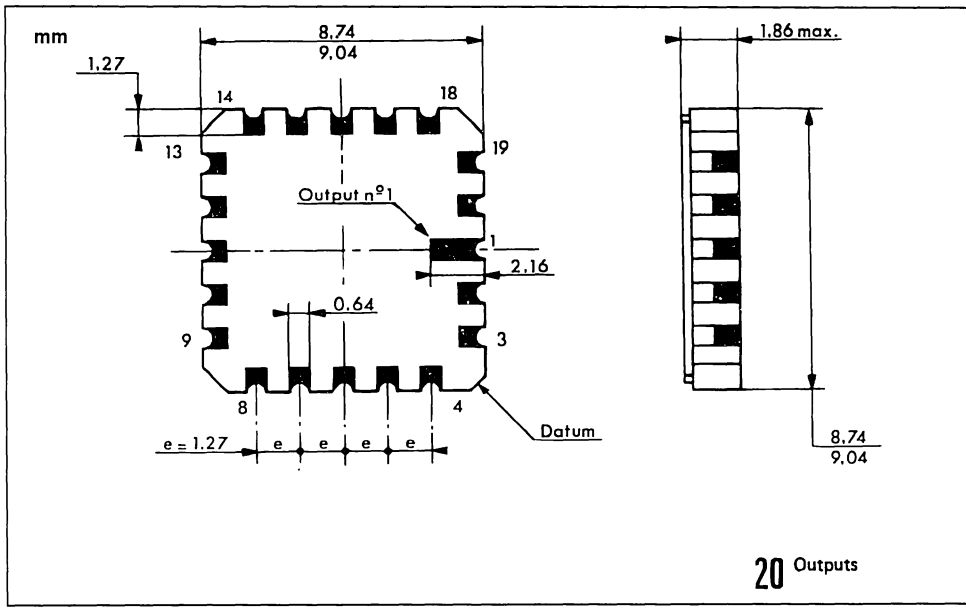
8 PINS – PLASTIC MICROPACKAGE (SO)



T0-99 – METAL CAN



20 PINS – TRICECOP (LCC)

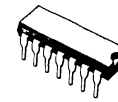


SGS-THOMSON MICROELECTRONICS

TL074
TL074A-TL074B

LOW NOISE J–FET INPUT QUAD OP–AMPs

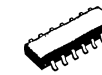
- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- LOW NOISE V_n = 18 nV/√Hz (typ)
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J–FET INPUT STAGE
- LOW HARMONIC DISTORTION : 0.01 % (typ)
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 13 V/µs (typ.)



N
DIP14
(Plastic package)

GC
LCC20
(Tricecop - LCC)

J
CERDIP14
(Cerdip package)



D
SO14
(Plastic micropackage)

ORDER CODES

Part Number	Temperature Range	Package			
		N	J	D	GC
TL074M	– 55 °C to + 125 °C		•		•
TL074I	– 40 °C to + 105 °C	•		•	
TL074C	0 °C to + 70 °C	•		•	
TL074AC	0 °C to + 70 °C	•		•	
TL074BC	0 °C to + 70 °C	•		•	

Note : Hi-Rel Versions Available
Examples : TL074 MJ, TL074 IN

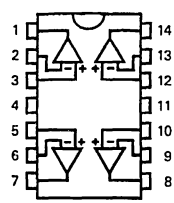
DESCRIPTION

The TL074, TL074A and TL074B are high speed J–FET input quad operational amplifiers incorporating well matched, high voltage J–FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

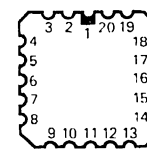
PIN CONNECTIONS (Top views)

DIP14
CERDIP14
SO14



1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{cc}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - Output 3
9 - Inverting input 3
10 - Non-inverting input 3
11 - V_{cc}^+
12 - Non-inverting input 4
13 - Inverting input 4
14 - Output 4

LCC20



1 - NC
2 - Output 1
3 - Inverting input 1
4 - Non-inverting input 1
5 - NC
6 - V_{cc}^+
7 - NC
8 - Non-inverting input 2
9 - Inverting input 2
10 - Output 2
11 - NC
12 - Output 3
13 - Inverting input 3
14 - Non-inverting input 3
15 - NC
16 - V_{cc}^-
17 - NC
18 - Non-inverting input 4
19 - Inverting input 4
20 - Output 4

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{cc}	Supply Voltage (note 1)	± 18	V
V_i	Input Voltage (note 3)	± 15	V
V_{ID}	Diff. Input Voltage (note 2)	± 30	V
P_{tot}	Power Dissipation	680	mW
	Output Short-circuit Duration (note 4)	Indefinite	
T_{oper}	Operating Free-air Temperature Range		°C
	TL074C, AC, BC	0 to 70	
	TL074I, BI	– 40 to 105	
	TL074M	– 55 to 125	
T_{stg}	Storage Temperature Range	– 65 to 150	°C

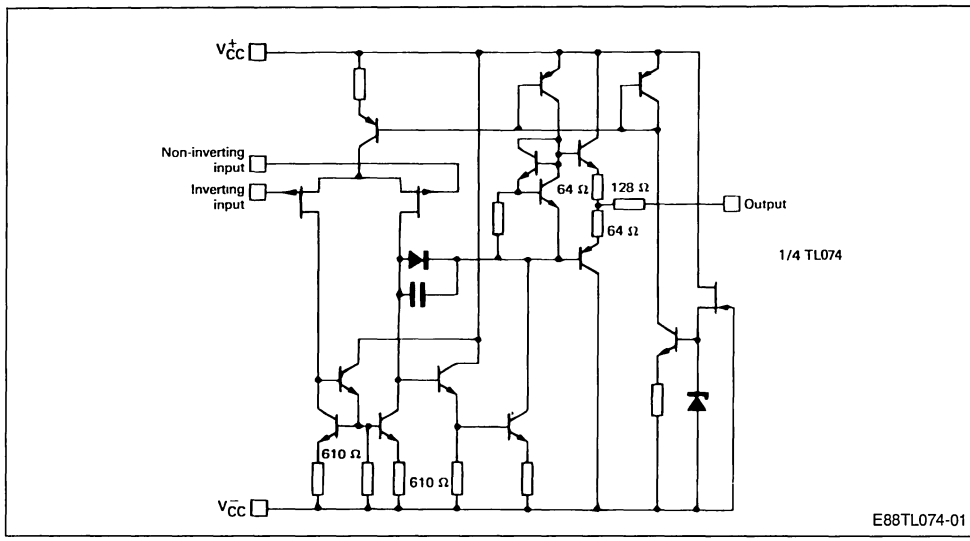
Notes : 1. All voltage values, except differential voltages, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.

2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.

3 The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.

4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

SCHEMATIC DIAGRAM



Case	Outputs	Inverting Inputs	Non-inverting Inputs	V_{cc}^-	V_{cc}^+	N.C.
DIP14 CERDIP14 SO14	1, 7, 8, 14	2, 6, 9, 13	3, 5, 10, 12	11	4	
LCC20	2, 10, 12, 20	3, 9, 13, 19	4, 8, 14, 18	16	6	*

* **LCC20** . Other pins are not connected.

ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 15$ V (unless otherwise specified)
TL074M : $-55\ °C \le T_{amb} \le +125\ °C$
TL074I, BI : $-40\ °C \le T_{amb} \le +105\ °C$
TL074C, AC, BC: $0\ °C \le T_{amb} \le +70\ °C$

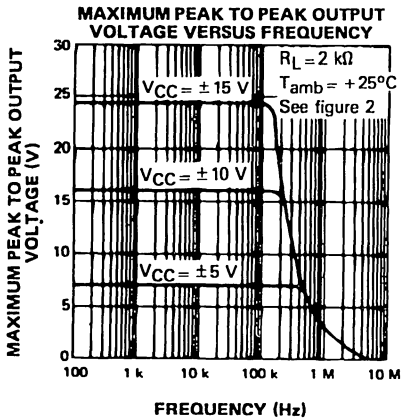
Symbol	Parameter	TL074M, I, BI TL074BC, AC			TL074C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage							mV
	T_{amb} = 25 °C (Rs ≤ 10 kΩ)		3	5		3	8	
	TL074BI, BC		1	3				
	$T_{min} \le T_{amb} \le T_{max}$			9			13	
	TL074BI, BC			5				
DV_{io}	Input Offset Voltage Drift		10			10		µV/°C
I_{io}	Input Offset Current *							
	T_{amb} = 25 °C		5	50		5	50	pA
	$T_{min} \le T_{amb} \le T_{max}$			4			4	nA
I_{ib}	Input Bias Current *							
	T_{amb} = 25 °C		30	200		30	200	pA
	$T_{min} \le T_{amb} \le T_{max}$			20			20	nA
A_{vd}	Large Signal Voltage Gain							V/mV
	($R_L \ge 2$ kΩ, $V_o = \pm 10$ V)							
	T_{amb} = 25 °C	50	200		50	200		
	$T_{min} \le T_{amb} \le T_{max}$	25			25			
SVR	Supply Voltage Rejection Ratio							dB
	($R_S \le 10$ kΩ)							
	T_{amb} = 25 °C	80	86		80	86		
	$T_{min} \le T_{amb} \le T_{max}$	80			80			
I_{cc}	Supply Current, per Amp, no Load							mA
	T_{amb} = 25 °C		1.4	2.5		1.4	2.5	
	$T_{min} \le T_{amb} \le T_{max}$			2.5			2.5	
V_i	Input Voltage Range	−11		+11	−11		+11	V
CMR	Common Mode Rejection Ratio							dB
	($R_S \le 10$ kΩ)							
	T_{amb} = 25 °C	80	86		70	86		
	$T_{min} \le T_{amb} \le T_{max}$	80			70			
I_{os}	Output Short-circuit Current							mA
	T_{amb} = 25 °C	10	40	60	10	40	60	
	$T_{min} \le T_{amb} \le T_{max}$	10		60	10		60	
$\pm V_{opp}$	Output Voltage Swing							V
	T_{amb} = 25 °C $R_L \ge 2$ kΩ	11	12		11	12		
	$R_L \ge 10$ kΩ	12	13.5		12	13.5		
	$T_{min} \le T_{amb} \le T_{max}$ $R_L \ge 2$ kΩ	11			11			
	$R_L \ge 10$ kΩ	12			12			
S_{vo}	Slew-rate (V_i = 10 V, R_L = 2 kΩ							V/µs
	$C_L \le 100$ pF, T_{amb} = 25 °C, unity gain)	12	16		8	16		
t_r	Rise Time							µs
	(V_i = 20 mV, R_L = 2 kΩ,							
	C_L = 100 pF, T_{amb} = 25 °C, unity gain)		0.1			0.1		

* The input bias currents are junction leakage currents wich approximatevely double for every 10 °C increase in the junction temperature

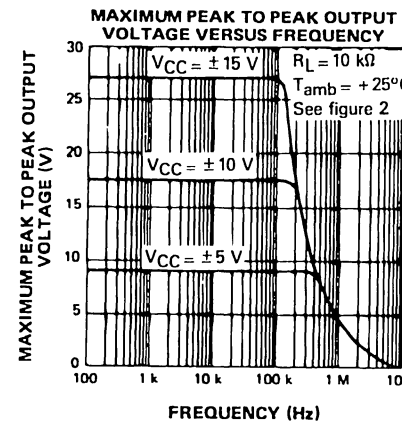
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	TL074M, I, BI TL074BC, AC			TL074C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
K_{ov}	Overshoot (V_i = 20 mV, R_L = 2 kΩ $C_L \leq 100$ pF, T_{amb} = 25 °C, unity gain)		10			10		%
GBP	Gain Bandwidth Product (f = 100 kHz, T_{amb} = 25 °C V_{in} = 10 mV, R_L = 2 kΩ, C_L = 100 pF) TL074BI, BC	2.5 3.3	4.0 4.0	5.0 5.0	2.5	4.0	5.0	MHz
R_i	Input Resistance (T_{amb} = 25 °C)		10^{12}			10^{12}		Ω
THD	Total Harmonic Distortion (f = 1 kHz, A_V = 20 dB, R_L = 2 kΩ $C_L \leq 100$ pF, T_{amb} = 25 °C, V_o = 2 V_{pp})		0.01			0.01		%
V_n	Equivalent Input Noise Voltage (f = 1 kHz, R_g = 100 Ω)		15			15		$nV/\sqrt{Hz}$
Øm	Phase Margin		45			45		Degrees
V_{O1}/V_{O2}	Channel Separation A_{vd} = 100, T_{amb} = 25 °C		120			120		dB

TYPICAL CHARACTERISTICS



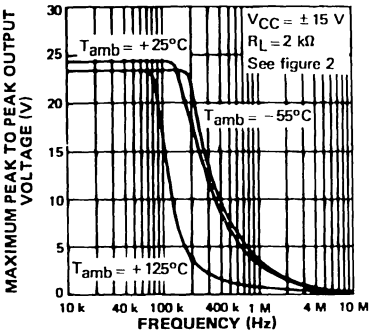
E88TL074-02



E88TL074-03

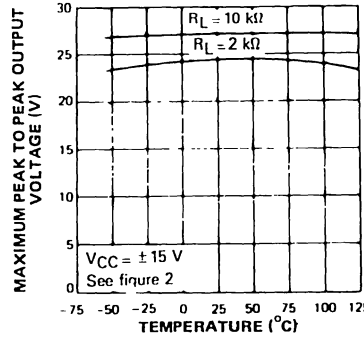
TYPICAL CHARACTERISTICS (continued)

MAXIMUM PEAK TO PEAK OUPUT VOLTAGE VERSUS FREE-AIR TEMP.



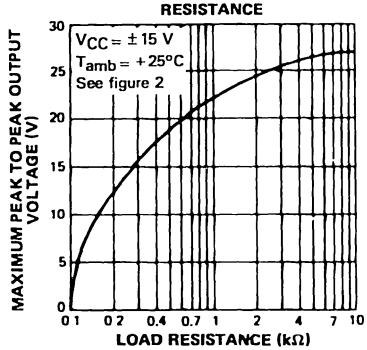
E88TL074-04

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



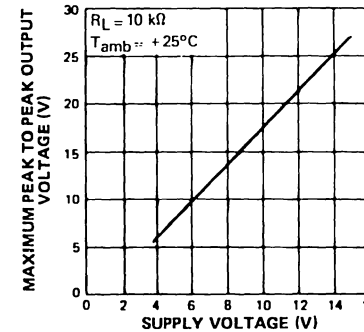
E88TL074-05

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



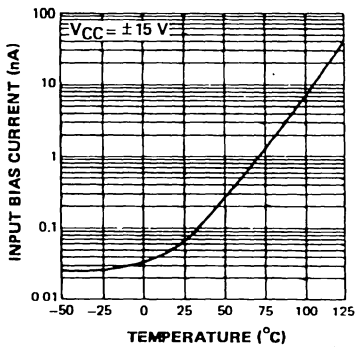
E88TL074-06

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



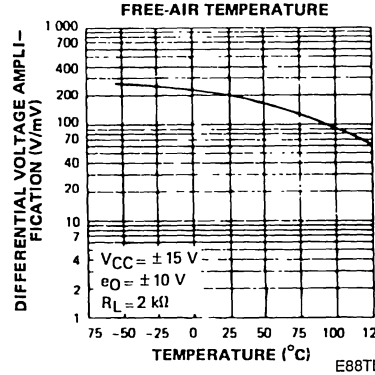
E88TL074-07

INPUT BIAS CURRENT VERSUS FREE-AIR TEMPERATURE



E88TL074-08

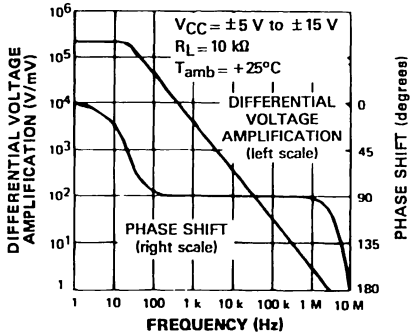
LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE-AIR TEMPERATURE



E88TL074-09

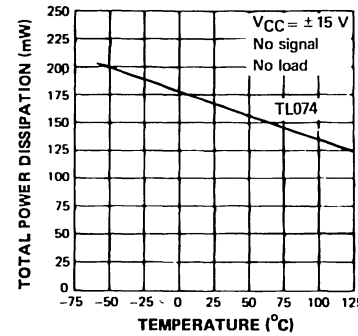
TYPICAL CHARACTERISTICS (continued)

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



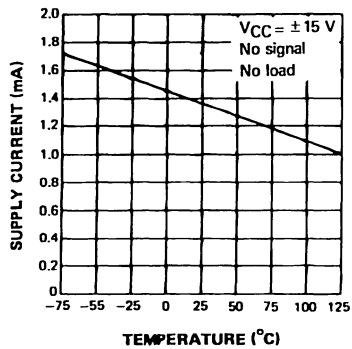
E88TL074-10

TOTAL POWER DISSIPATION VERSUS FREE-AIR TEMPERATURE



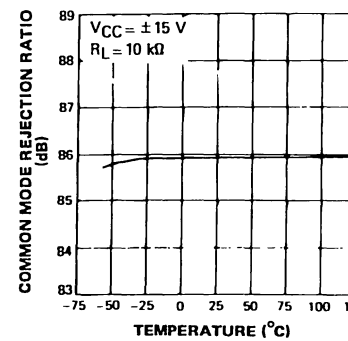
E88TL074-11

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE-AIR TEMPERATURE



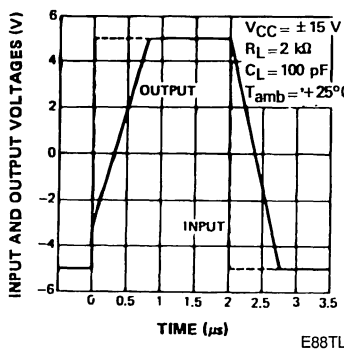
E88TL074-12

COMMON MODE REJECTION RATIO VERSUS FREE-AIR TEMPERATURE



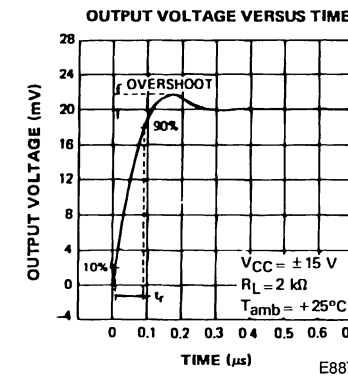
E88TL074-13

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



E88TL074-14

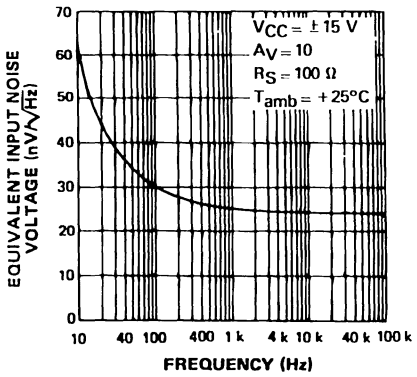
OUTPUT VOLTAGE VERSUS TIME



E88TL074-15

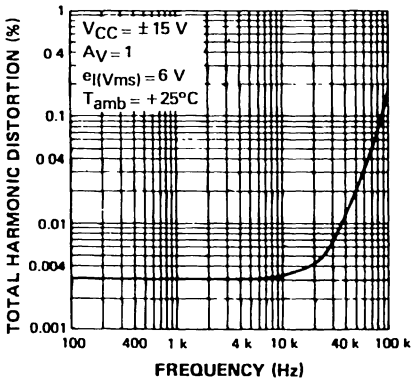
TYPICAL CHARACTERISTICS (continued)

EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



E88TL074-16

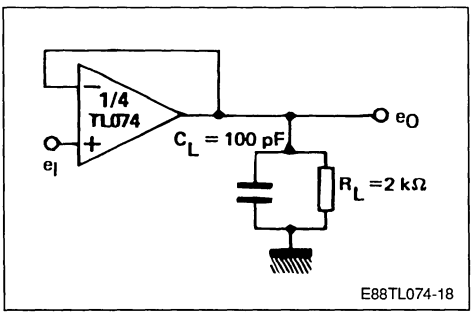
TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



E88TL074-17

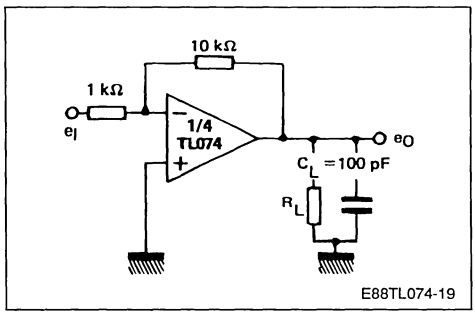
PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage follower.



E88TL074-18

Figure 2 : Gain-of-10 inverting amplifier.

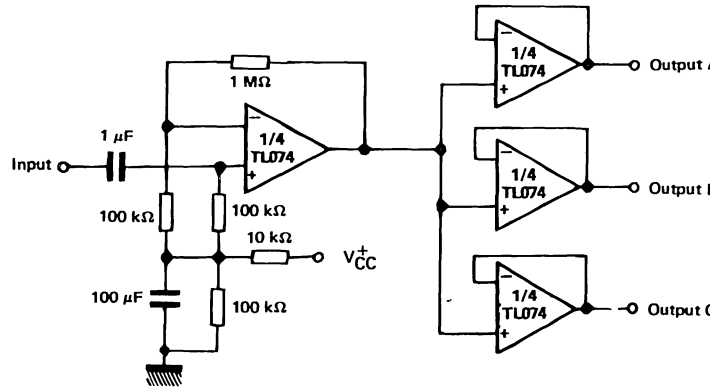


E88TL074-19

TYPICAL APPLICATIONS

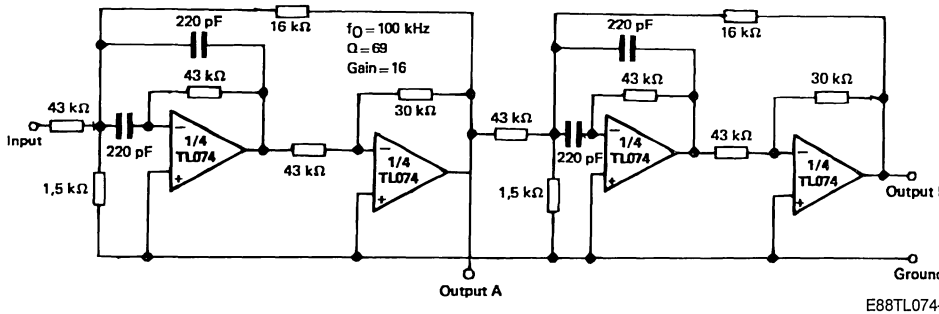
AUDIO DISTRIBUTION AMPLIFIER

f_O = 100 kHz



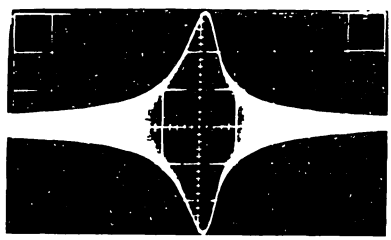
E88TL074-20

POSITIVE FEEDBACK BANDPASS-FILTER



E88TL074-21

OUTPUT A



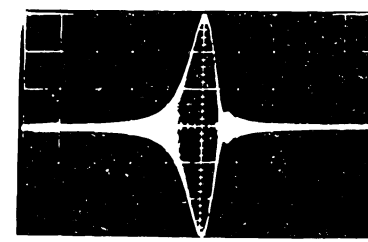
E88TL074-23

2 kHz /div

SECOND ORDER BANDPASS FILTER

f_O = 100 kHz; Q = 69; Gain = 16

OUTPUT B



E88TL074-22

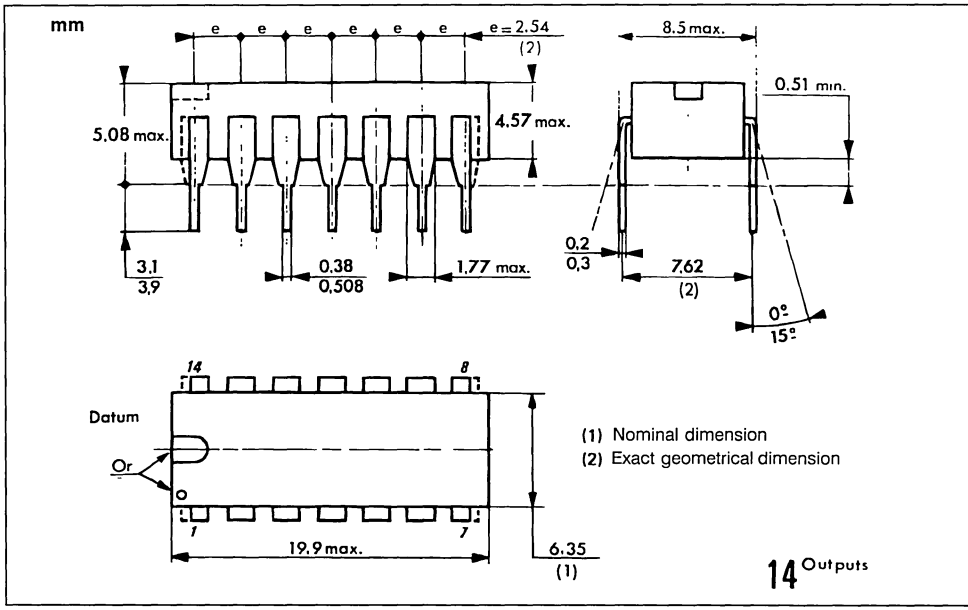
2 kHz /div

CASCADED BANDPASS FILTER

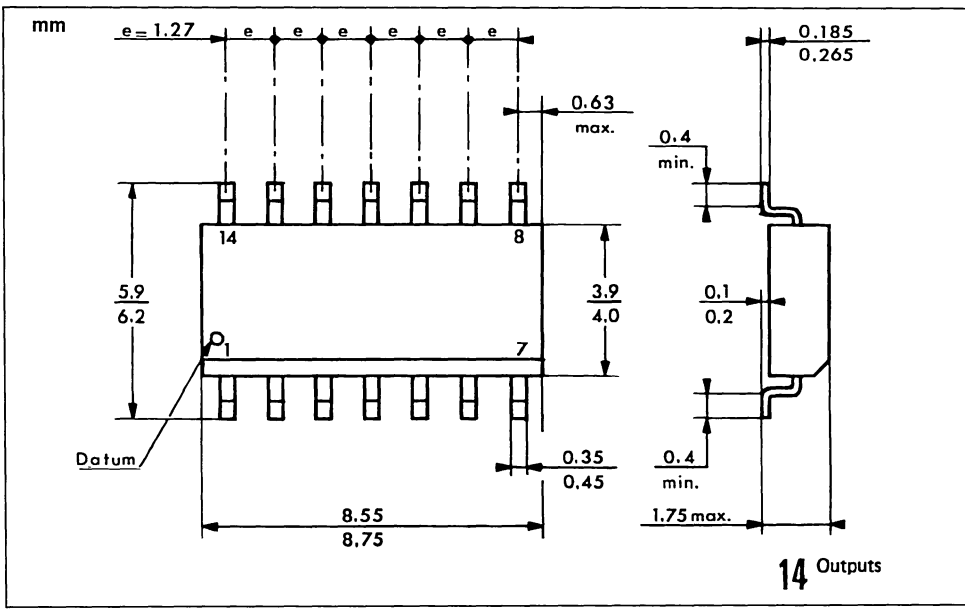
f_O = 100 kHz; Q = 30; Gain = 4

PACKAGE MECHANICAL DATA

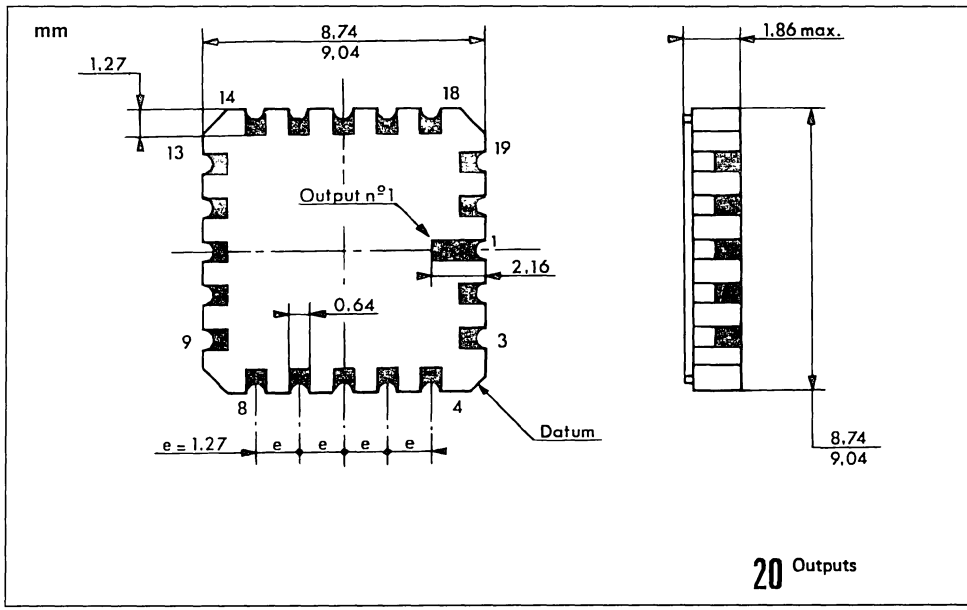
14 PINS – PLASTIC DIP OR CERDIP



14 PINS – PLASTIC MICROPACKAGE (SO)



20 PINS – TRICECOP (LCC)



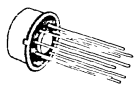
SGS-THOMSON MICROELECTRONICS

TL081
TL081A-TL081B

J–FET INPUT SINGLE OP–AMPs

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J–FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 13 V/µs (typ)

N
DIP8
(Plastic package)



H
TO-99
(Metal can)

D
SO8
(Plastic micropackage)

GC
LCC20
(Tricecop - LCC)

ORDER CODES

Part Number	Temperature Range	Package			
		N	H	D	GC
TL082M	– 55 °C to + 125 °C		•		•
TL082I	– 40 °C to + 105 °C	•		•	
TL082C	0 °C to + 70 °C	•		•	
TL082AC	0 °C to + 70 °C	•		•	
TL082BC	0 °C to + 70 °C	•		•	

Note : Hi-Rel Versions Available
Examples : TL082CD, TL082MGC, TL082IN

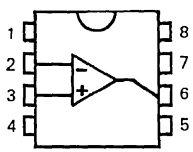
DESCRIPTION

The TL081, TL081A and TL081C are high speed J–FET input single operational amplifiers incorporating well matched, high voltage J–FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset current, and low offset voltage temperature coefficient.

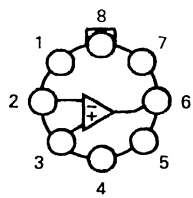
PIN CONNECTIONS (Top views)

DIP8
SO8



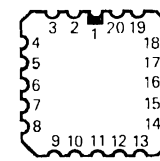
5 - Balance
6 - Output
7 - V_{CC}^{+}
8 - NC

TO-99



1 - Balance
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^{-}

LCC20



1 - NC
2 - Balance
3 - NC
4 - NC
5 - Inverting input
6 - NC
7 - Non-inverting input
8 - NC
9 - NC
10 - V_{CC}^{-}
11 - NC
12 - Balance
13 - NC
14 - NC
15 - Output
16 - NC
17 - V_{CC}^{+}
18 - NC
19 - NC
20 - NC

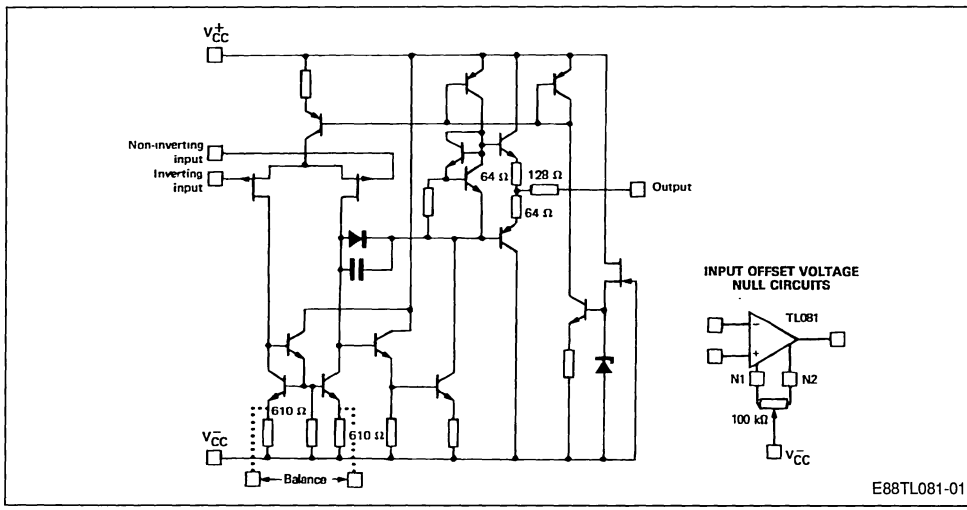
MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	± 18	V
V_I	Input Voltage (note 3)	± 15	V
V_{ID}	Differential Input Voltage (note 2)	± 30	V
P_{tot}	Power Dissipation	680	mW
	Output Short-circuit Duration (note 4)	Indefinite	
T_{oper}	Operating Free Air Temperature Range TL082C, AC, BC TL082I, BI TL082M	 0 to + 70 − 40 to + 105 − 55 to + 125	°C
T_{stg}	Storage Temperature Range	− 65 to + 150	°C

Notes : 1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.

2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

SCHEMATIC DIAGRAM



Case	Balance	Inverting Input	Non-inverting Input	Output	V_{cc}^+	V_{cc}^-	N.C.
DIP8 SO8 TO-99	1, 5	2	3	6	7	4	8
LCC20	2, 12	5	7	15	17	10	*

* **LCC20** : Other pins are not connected.

ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 15$ V (unless otherwise specified)
TL081M : $-55\ ^\circ C \le T_{amb} \le +125\ ^\circ C$
TL081I, BI : $-40\ ^\circ C \le T_{amb} \le +105\ ^\circ C$
TL081C, AC, BC: $0\ ^\circ C \le T_{amb} \le +70\ ^\circ C$

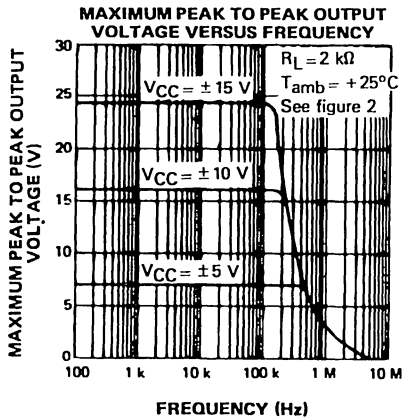
Symbol	Parameter	TL082M, I, BI TL082BC, AC			TL082C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage							mV
	T_{amb} = 25 °C (Rs ≤ 10 kΩ)		3	5		3	8	
	TL082BI, BC		1	3				
	$T_{min} \le T_{amb} \le T_{max}$			9			13	
	TL082BI, BC			5				
DV_{IO}	Input Offset Voltage Drift		10			10		µV/°C
I_{IO}	Input Offset Current *							
	T_{amb} = 25 °C		5	50		5	50	pA
	$T_{min} \le T_{amb} \le T_{max}$			4			4	nA
I_{IB}	Input Bias Current *							
	T_{amb} = 25 °C		20	200		20	200	pA
	$T_{min} \le T_{amb} \le +70$ °C			20			20	nA
A_{VD}	Large Signal Voltage Gain							V/mV
	($R_L \ge 2$ kΩ, $V_O = \pm 10$ V)							
	T_{amb} = 25 °C	50	200		50	200		
	$T_{min} \le T_{amb} \le T_{max}$	25			25			
SVR	Supply Voltage Rejection Ratio							dB
	($R_S \le 10$ kΩ)							
	T_{amb} = 25 °C	80	86		80	86		
	$T_{min} \le T_{amb} \le T_{max}$	80			80			
I_{CC}	Supply Current, per Amp, no Load							mA
	T_{amb} = 25 °C		1.4	2.5		1.4	2.5	
	$T_{min} \le T_{amb} \le T_{max}$			2.5			2.5	
V_I	Input Voltage Range	−11		+11	−11		+11	V
CMR	Common Mode Rejection Ratio							dB
	($R_S \le 10$ kΩ)							
	T_{amb} = 25 °C	80	86		70	86		
	$T_{min} \le T_{amb} \le T_{max}$	80			70			
I_{OS}	Output Short-circuit Current							mA
	T_{amb} = 25 °C	10	40	60	10	40	60	
	$T_{min} \le T_{amb} \le T_{max}$	10		60	10		60	
$\pm V_{OPP}$	Output Voltage Swing							V
	T_{amb} = 25 °C $R_L \ge 2$ kΩ	11	12		11	12		
	$R_L \ge 10$ kΩ	12	13.5		12	13.5		
	$T_{min} \le T_{amb} \le T_{max}$ $R_L \ge 2$ kΩ	11			11			
	$R_L \ge 10$ kΩ	12			12			
S_{VO}	Slew-rate (V_I = 10 V, R_L = 2 kΩ							V/µs
	$C_L \le 100$ pF, T_{amb} = 25 °C, unity gain)	12	16		8	16		
t_r	Rise Time							µs
	(V_I = 20 mV, R_L = 2 kΩ							
	C_L = 100 pF, T_{amb} = 25 °C, unity gain)		0.1			0.1*		

* The input bias currents are junction leakage currents wich approximatevely double for every 10 °C increase in the junction temperature.

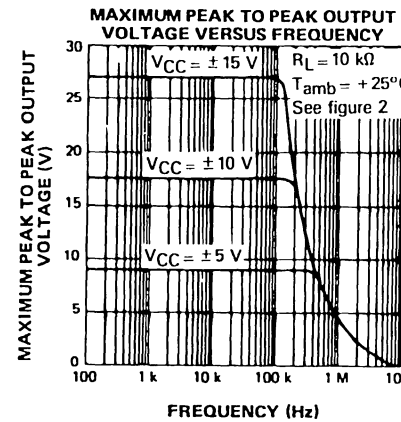
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	TL082M, I, BI TL082BC, AC			TL082C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
K_{OV}	Overshoot (V_I = 20 mV, R_L = 2 kΩ $C_L \leq 100$ pF, T_{amb} = 25 °C, unity gain)		10			10		%
GBP	Gain Bandwidth Product (f = 100 kHz, T_{amb} = 25 °C V_{IN} = 10 mV, R_L = 2 kΩ, C_L = 100 pF) TL082BI, BC	2.5 3 3	4.0 4.0	5.0 5 0	2.5	4 0	5 0	MHz
R_I	Input Resistance (T_{amb} = 25 °C)		10^{12}			10^{12}		Ω
THD	Total Harmonic Distortion (f = 1 kHz, A_V = 20 dB, R_L = 2 kΩ $C_L \leq 100$ pF, T_{amb} = 25 °C, V_O = 2 V_{PP})		0.01			0.01		%
V_n	Equivalent Input Noise Voltage (f = 1 kHz, R_g = 100 Ω)		15			15		nV/√Hz
Øm	Phase Margin		45			45		Degrees
V_{O1} / V_{O2}	Channel Separation Avd = 100, T_{amb} = 25 °C		120			120		dB

TYPICAL CHARACTERISTICS



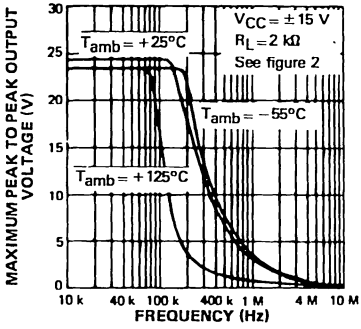
E88TL071-02



E88TL071-03

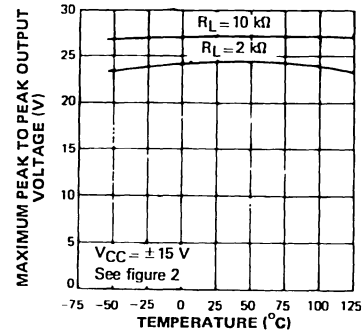
TYPICAL CHARACTERISTICS (continued)

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



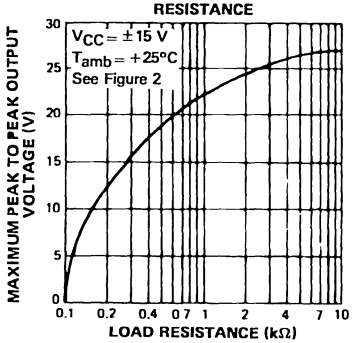
E88TL071-04

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREE-AIR TEMP.



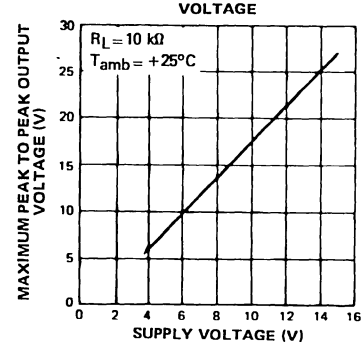
E88TL071-05

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



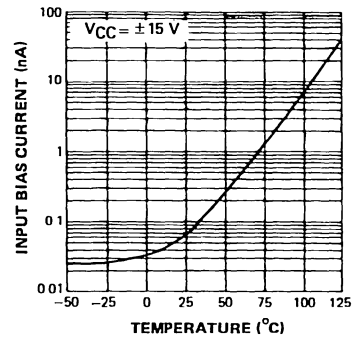
E88TL071-06

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



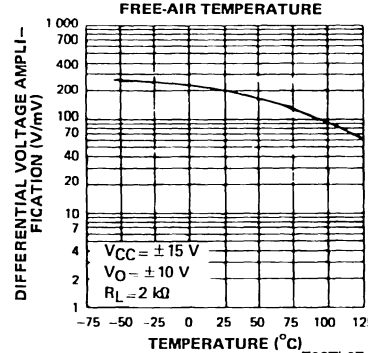
E88TL071-07

INPUT BIAS CURRENT VERSUS FREE-AIR TEMPERATURE



E88TL071-08

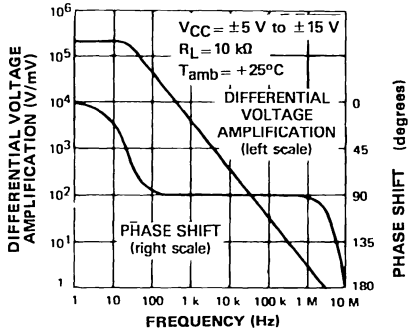
LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE-AIR TEMPERATURE



E88TL071-09

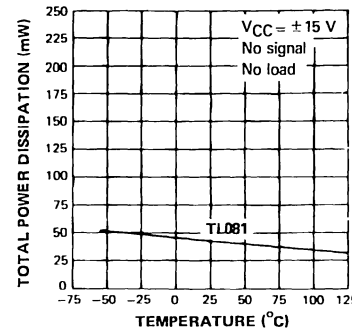
TYPICAL CHARACTERISTICS (continued)

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



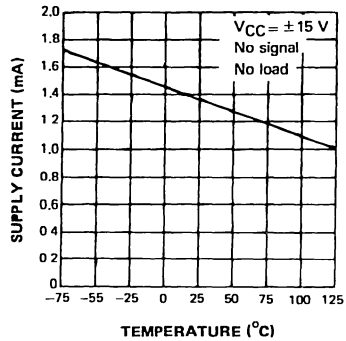
E88TL071-10

TOTAL POWER DISSIPATION VERSUS FREE-AIR TEMPERATURE



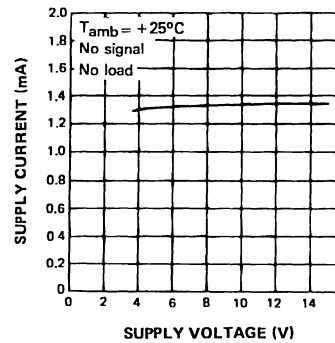
E88TL071-11

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE-AIR TEMPERATURE



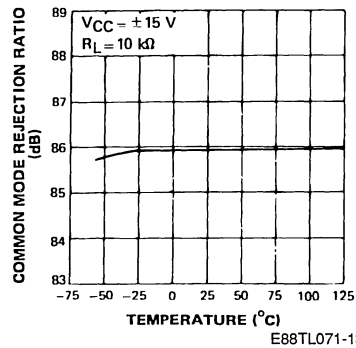
E88TL071-12

SUPPLY CURRENT PER AMPLIFIER VERSUS SUPPLY VOLTAGE



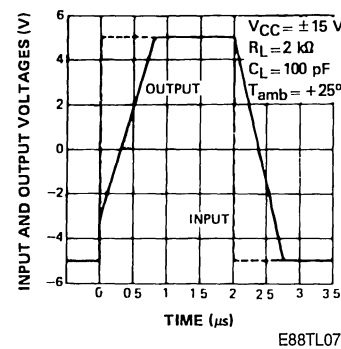
E88TL081-02

COMMON MODE REJECTION RATIO VERSUS FREE-AIR TEMPERATURE



E88TL071-13

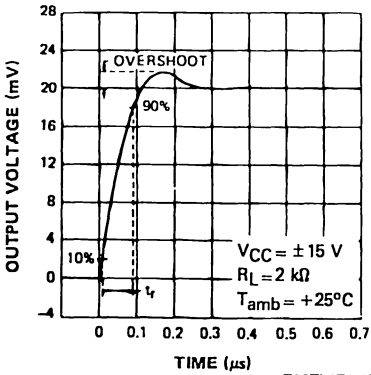
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



E88TL071-14

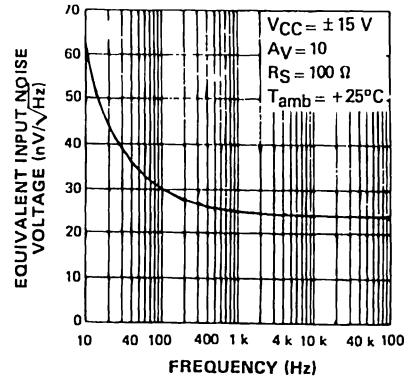
TYPICAL CHARACTERISTICS (continued)

OUTPUT VOLTAGE VERSUS TIME



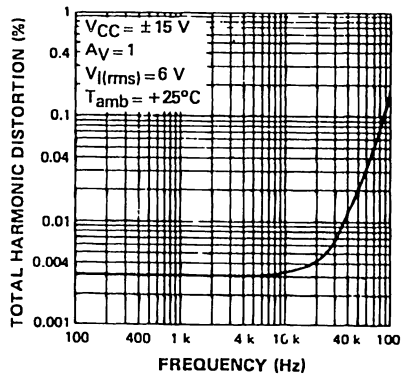
E88TL071-15

EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



E88TL071-16

TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



E88TL071-17

PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage follower.

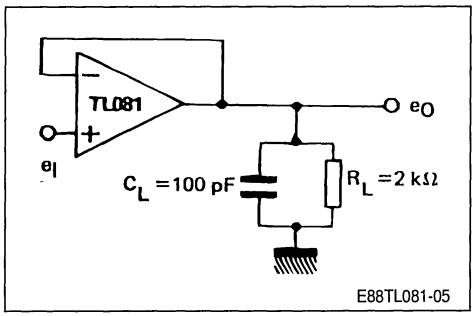
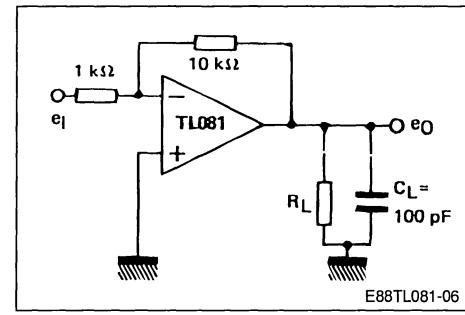
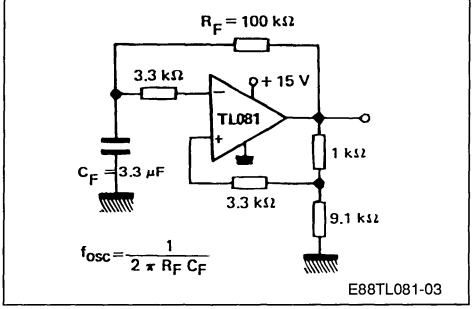


Figure 2 : Gain-of-10 inverting amplifier.

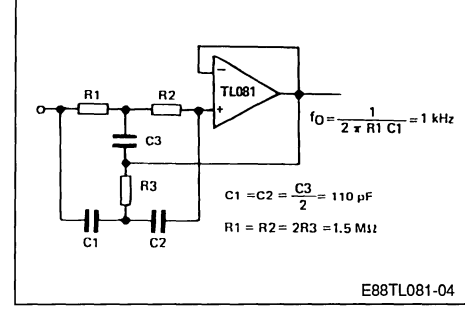


TYPICAL APPLICATIONS

(0.5 Hz) SQUARE WAVE OSCILLATOR

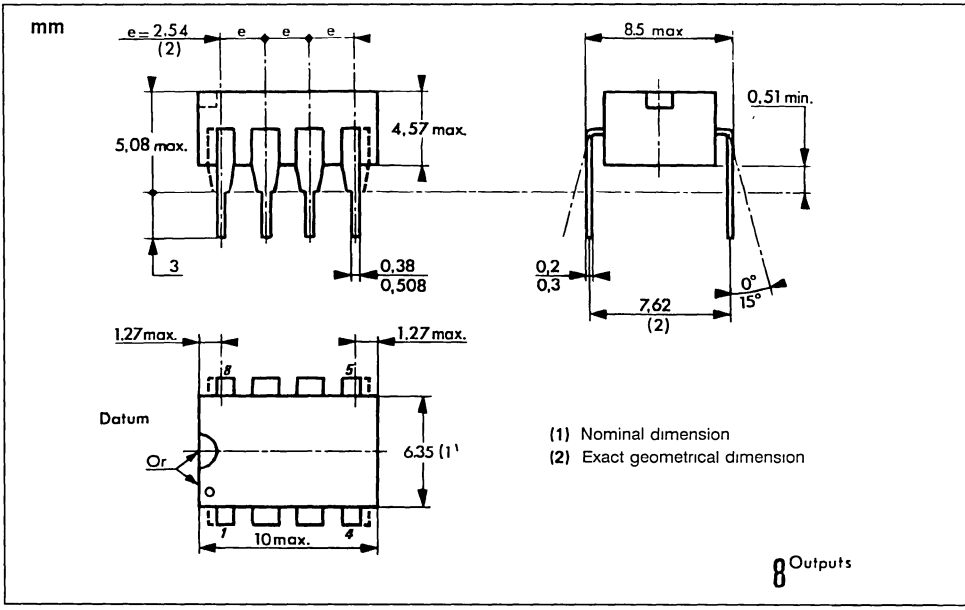


HIGH Q NOTCH FILTER

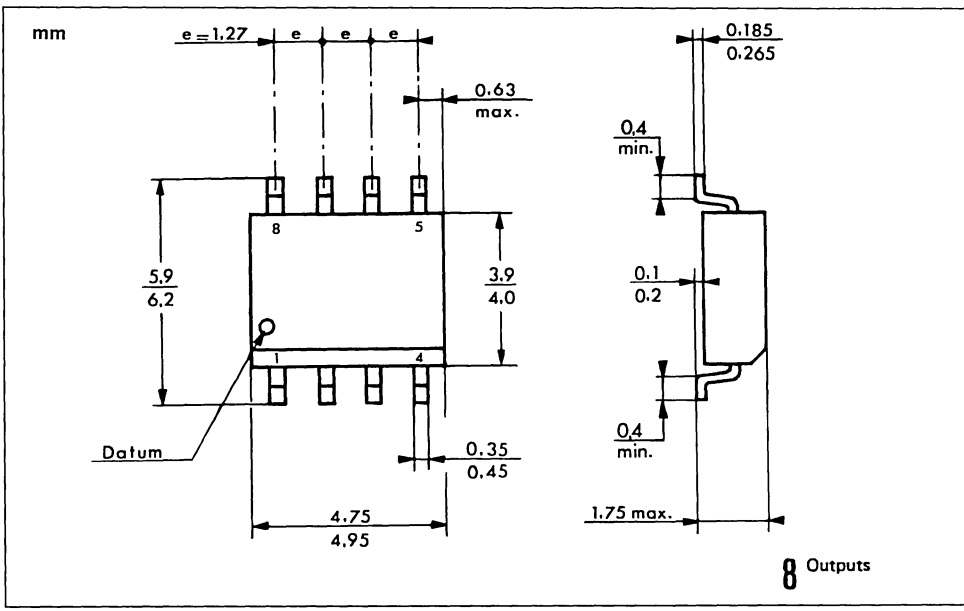


PACKAGE MECHANICAL DATA

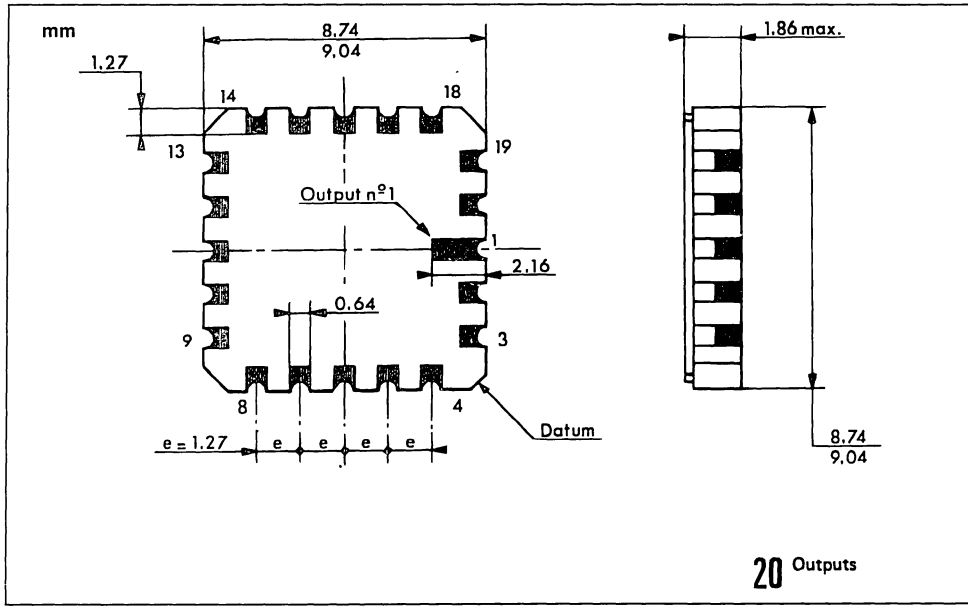
8 PINS – PLASTIC DIP



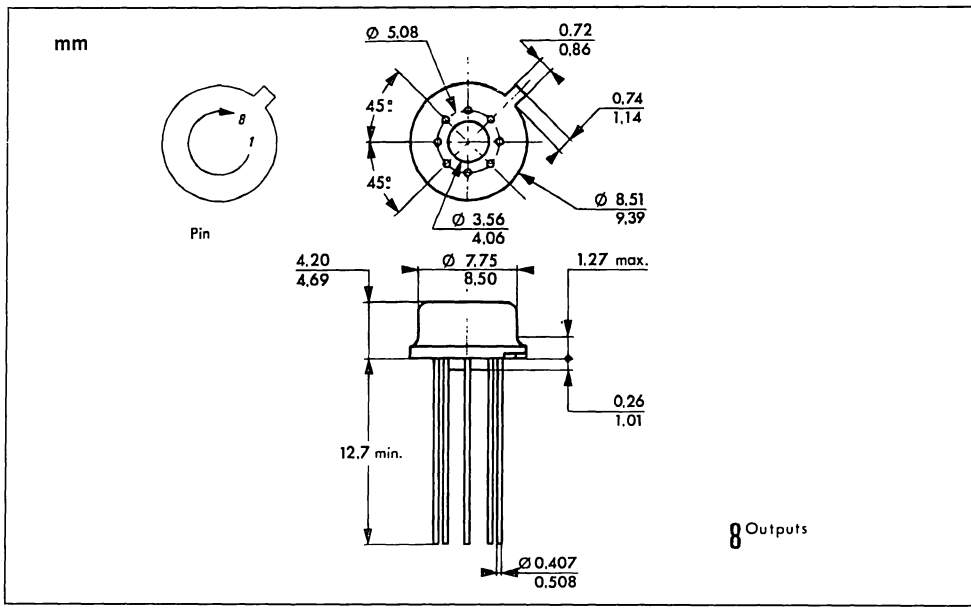
8 PINS – PLASTIC MICROPACKAGE (SO)



20 PINS – TRICECOP (LCC)



TO-99 – METAL CAN



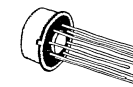
SGS-THOMSON MICROELECTRONICS

TL082
TL082A-TL082B

J–FET INPUT DUAL OP–AMPs

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J–FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 13 V/µs (typ)

N
DIP8
(Plastic package)



H
TO-99
(Metal can)

D
SO8
(Plastic micropackage)

GC
LCC20
(Tricecop - LCC)

ORDER CODES

Part Number	Temperature Range	Package			
		N	H	D	GC
TL082M	– 55 °C to + 125 °C		•		•
TL082I	– 40 °C to + 105 °C	•		•	
TL082C	0 °C to + 70 °C	•		•	
TL082AC	0 °C to + 70 °C	•		•	
TL082BC	0 °C to + 70 °C	•		•	

Note : Hi-Rel Versions Available
Examples : TL082CD, TL082MGC, TL082IN

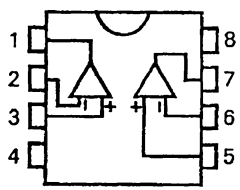
DESCRIPTION

The TL082, TL082A and TL082B are high speed J–FET input dual operational amplifiers incorporating well matched, high voltage J–FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset current, and low offset voltage temperature coefficient.

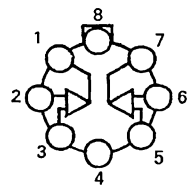
PIN CONNECTIONS (Top views)

DIP8
SO8



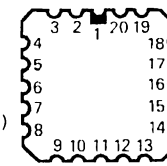
1 - Output (1)
2 - Inverting input (1)
3 - Non-inverting input (1)
4 - V_{CC}^-

TO-99



5 - Non-inverting input (2)
6 - Inverting input (2)
7 - Output (2)
8 - V_{CC}^+

LCC20



1 - NC
2 - Output (1)
3 - NC
4 - NC
5 - Inverting input (1)
6 - NC
7 - Non-inverting input (1)
8 - NC
9 - NC
10 - V_{CC}^-
11 - NC
12 - Non-inverting input (2)
13 - NC
14 - NC
15 - Inverting input (2)
16 - NC
17 - Output (2)
18 - NC
19 - NC
20 - V_{CC}^+

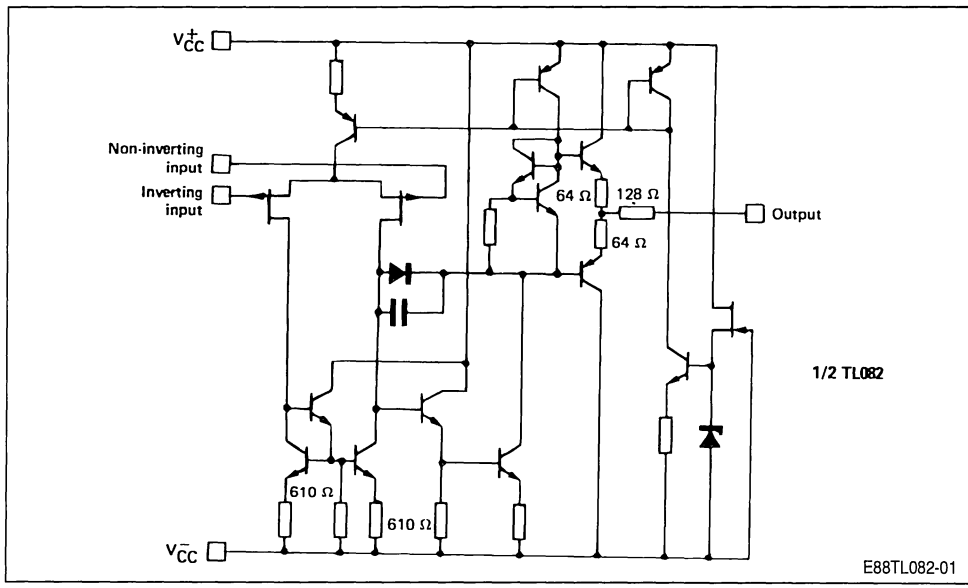
MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	± 18	V
V_I	Input Voltage (note 3)	± 15	V
V_{ID}	Differential Input Voltage (note 2)	± 30	V
P_{tot}	Power Dissipation	680	mW
	Output Short-circuit Duration (note 4)	Indefinite	
T_{oper}	Operating Free Air Temperature Range TL082C, AC, BC TL082I, BI TL082M	 0 to + 70 − 40 to + 105 − 55 to + 125	°C
T_{stg}	Storage Temperature Range	− 65 to + 150	°C

Notes : 1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.

2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

SCHEMATIC DIAGRAM



Case	Outputs	Inverting Inputs	Non-inverting Inputs	V_{cc}^-	V_{cc}^+	N.C.
DIP8 SO8 TO-99	1, 7	3, 5	2, 6	4	8	
LCC20	2, 17	7, 12	5, 15	10	20	*

* **LCC20 :** Other pins are not connected.

ELECTRICAL CHARACTERISTICS

V_{CC} = ± 15 V (unless otherwise specified)
TL082M : − 55 °C ≤ T_{amb} ≤ + 125 °C
TL082I, BI : − 40 °C ≤ T_{amb} ≤ + 105 °C
TL082C, AC, BC : 0 °C ≤ T_{amb} ≤ + 70 °C

Symbol	Parameter	TL082M, I, BI TL082BC, AC			TL082C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage							mV
	T_{amb} = 25 °C (Rs ≤ 10 kΩ)		3	5		3	8	
	TL082BI, BC		1	3				
	$T_{min} \le T_{amb} \le T_{max}$			9			13	
	TL082BI, BC			5				
DV_{IO}	Input Offset Voltage Drift		10			10		µV/°C
I_{IO}	Input Offset Current *							
	T_{amb} = 25 °C		5	50		5	50	pA
	$T_{min} \le T_{amb} \le T_{max}$			4			4	nA
I_{IB}	Input Bias Current *							
	T_{amb} = 25 °C		20	200		20	200	pA
	$T_{min} \le T_{amb} \le$ + 70 °C			20			20	nA
A_{VD}	Large Signal Voltage Gain							V/mV
	($R_L \ge 2$ kΩ, V_O = ± 10 V)							
	T_{amb} = 25 °C	50	200		50	200		
	$T_{min} \le T_{amb} \le T_{max}$	25			25			
SVR	Supply Voltage Rejection Ratio							dB
	($R_S \le 10$ kΩ)							
	T_{amb} = 25 °C	80	86		80	86		
	$T_{min} \le T_{amb} \le T_{max}$	80			80			
I_{CC}	Supply Current, per Amp, no Load							mA
	T_{amb} = 25 °C		1.4	2.5		1.4	2.5	
	$T_{min} \le T_{amb} \le T_{max}$			2.5			2.5	
V_I	Input Voltage Range	− 11		+ 11	− 11		+ 11	V
CMR	Common Mode Rejection Ratio							dB
	($R_S \le 10$ kΩ)							
	T_{amb} = 25 °C	80	86		70	86		
	$T_{min} \le T_{amb} \le T_{max}$	80			70			
I_{OS}	Output Short-circuit Current							mA
	T_{amb} = 25 °C	10	40	60	10	40	60	
	$T_{min} \le T_{amb} \le T_{max}$	10		60	10		60	
± V_{OPP}	Output Voltage Swing							V
	T_{amb} = 25 °C $R_L \ge 2$ kΩ	11	12		11	12		
	$R_L \ge 10$ kΩ	12	13.5		12	13.5		
	$T_{min} \le T_{amb} \le T_{max}$ $R_L \ge 2$ kΩ	11			11			
	$R_L \ge 10$ kΩ	12			12			
S_{VO}	Slew-rate (V_I = 10 V, R_L = 2 kΩ							V/µs
	$C_L \le 100$ pF, T_{amb} = 25 °C, unity gain)	12	16		8	16		
t_r	Rise Time							µs
	(V_I = 20 mV, R_L = 2 kΩ							
	C_L = 100 pF, T_{amb} = 25 °C, unity gain)		0.1			0.1		

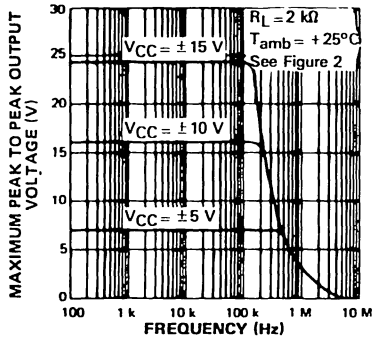
* The input bias currents are junction leakage currents wich approximatevely double for every 10 °C increase in the junction temperature

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	TL082M, I, BI TL082BC, AC			TL082C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
K_{OV}	Overshoot (V_I = 20 mV, R_L = 2 kΩ $C_L \leq 100$ pF, T_{amb} = 25 °C, unity gain)		10			10		%
GBP	Gain Bandwidth Product (f = 100 kHz, T_{amb} = 25 °C V_{IN} = 10 mV, R_L = 2 kΩ, C_L = 100 pF) TL082BI, BC	2.5 3.3	4.0 4.0	5.0 5.0	2.5	4.0	5 0	MHz
R_I	Input Resistance (T_{amb} = 25 °C)		10^{12}			10^{12}		Ω
THD	Total Harmonic Distortion (f = 1 kHz, A_V = 20 dB, R_L = 2 kΩ $C_L \leq 100$ pF, T_{amb} = 25 °C, V_O = 2 V_{PP})		0.01			0.01		%
V_n	Equivalent Input Noise Voltage (f = 1 kHz, R_g = 100 Ω)		15			15		nV/√Hz
Øm	Phase Margin		45			45		Degrees
V_{O1} / V_{O2}	Channel Separation Avd = 100, T_{amb} = 25 °C		120			120		dB

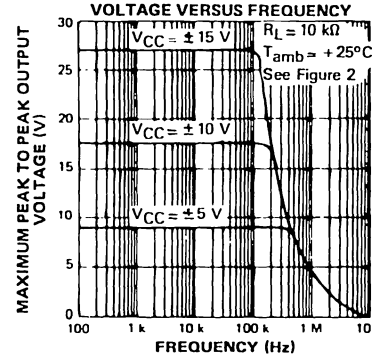
TYPICAL CHARACTERISTICS

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



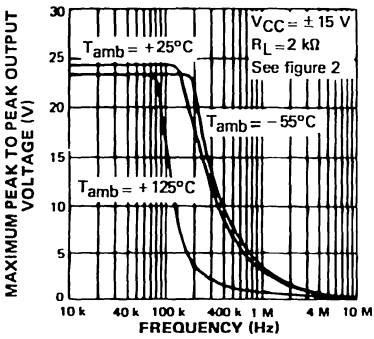
E88TL072-02

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



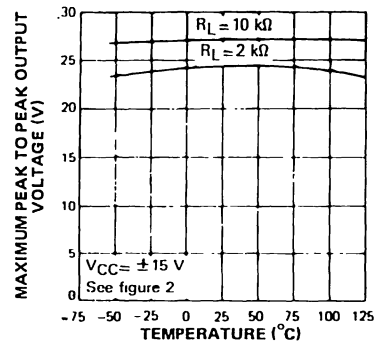
E88TL072-03

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



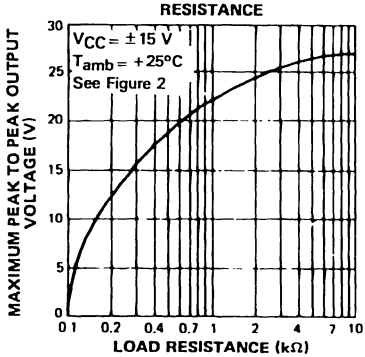
E88TL072-04

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREE-AIR TEMP.



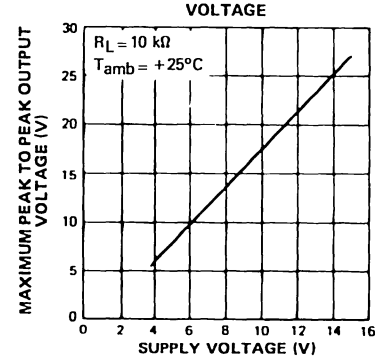
E88TL072-05

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



E88TL072-06

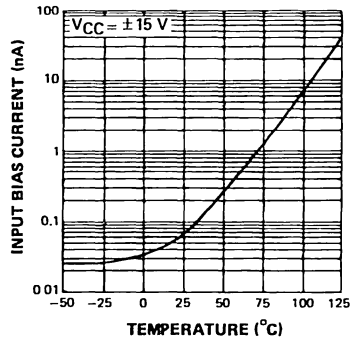
MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



E88TL072-07

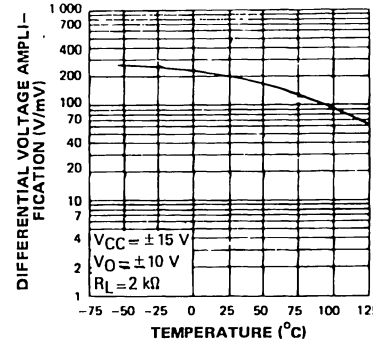
TYPICAL CHARACTERISTICS (continued)

INPUT BIAS CURRENT VERSUS FREE-AIR TEMPERATURE



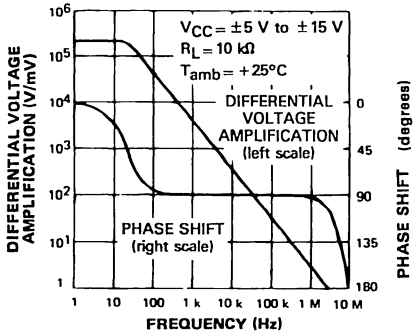
E88TL072-08

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE-AIR TEMPERATURE



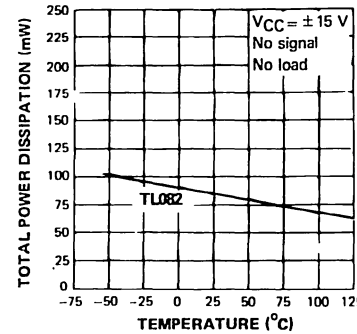
E88TL072-09

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



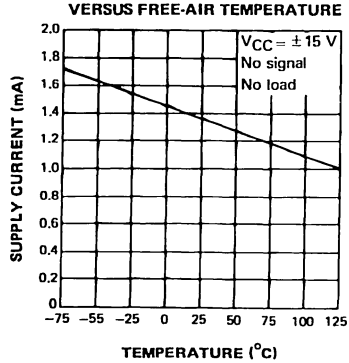
E88TL072-10

TOTAL POWER DISSIPATION VERSUS FREE-AIR TEMPERATURE



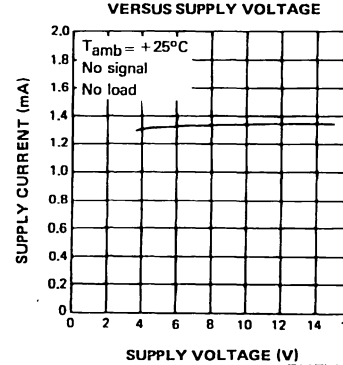
E88TL072-11

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE-AIR TEMPERATURE



E88TL072-12

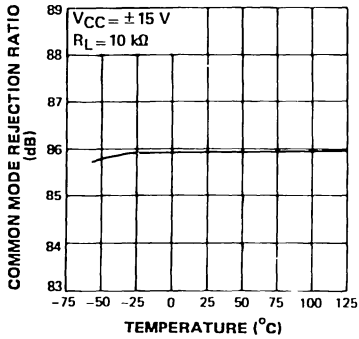
SUPPLY CURRENT PER AMPLIFIER VERSUS SUPPLY VOLTAGE



E88TL082-02

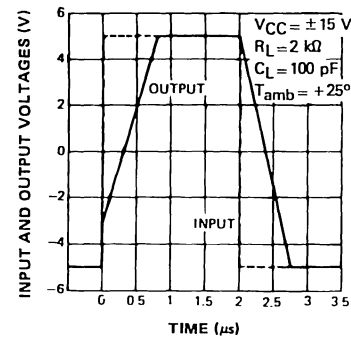
TYPICAL CHARACTERISTICS (continued)

COMMON MODE REJECTION RATIO VERSUS FREE-AIR TEMPERATURE



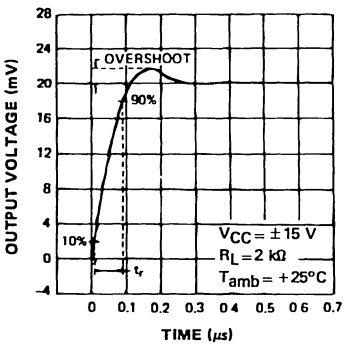
E88TL072-13

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



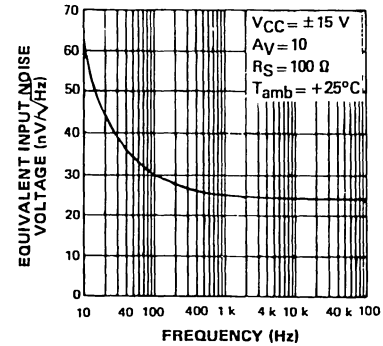
E88TL072-14

OUTPUT VOLTAGE VERSUS TIME



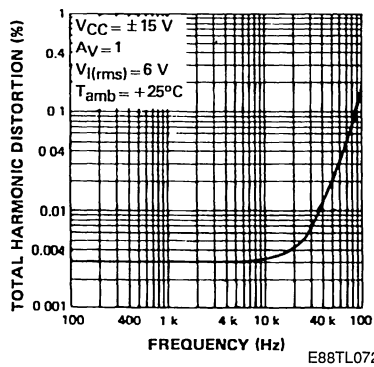
E88TL072-15

EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



E88TL072-16

TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



E88TL072-17

PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage follower.

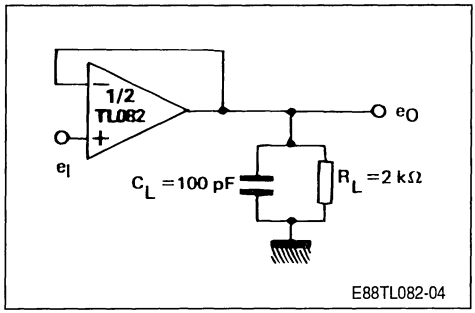
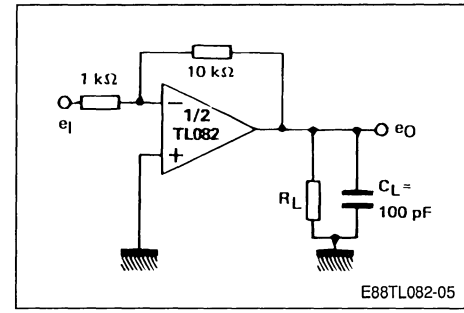
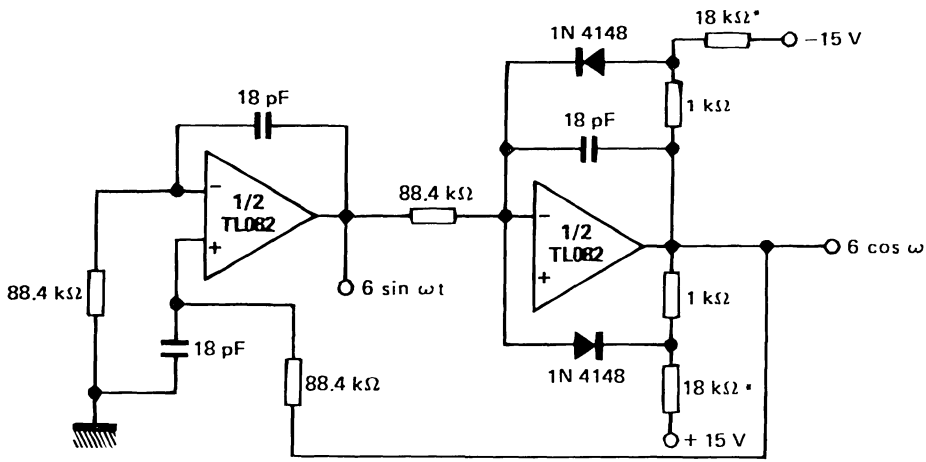


Figure 2 : Gain-of-10 inverting amplifier.



TYPICAL APPLICATION

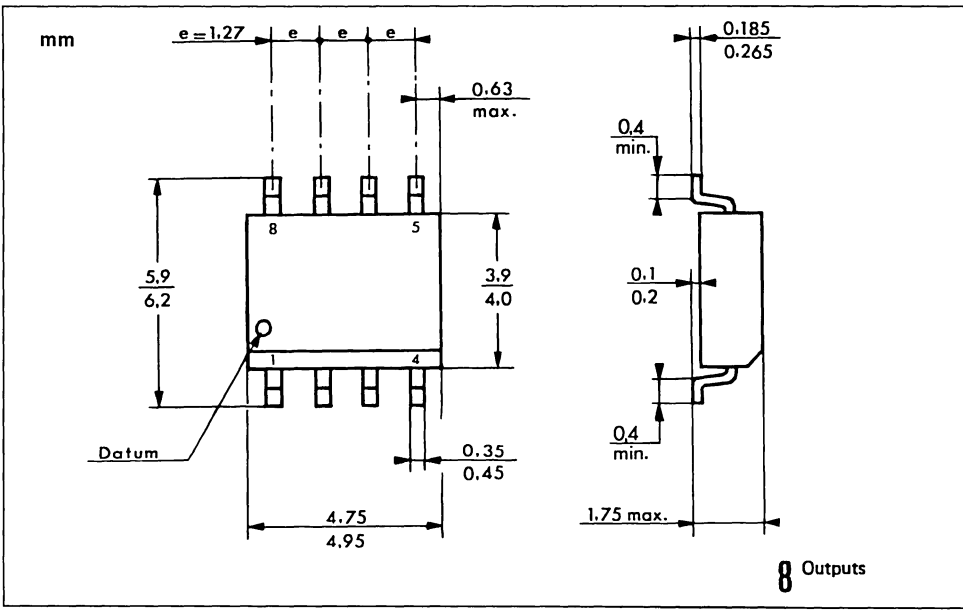
QUADRATURE OSCILLATOR



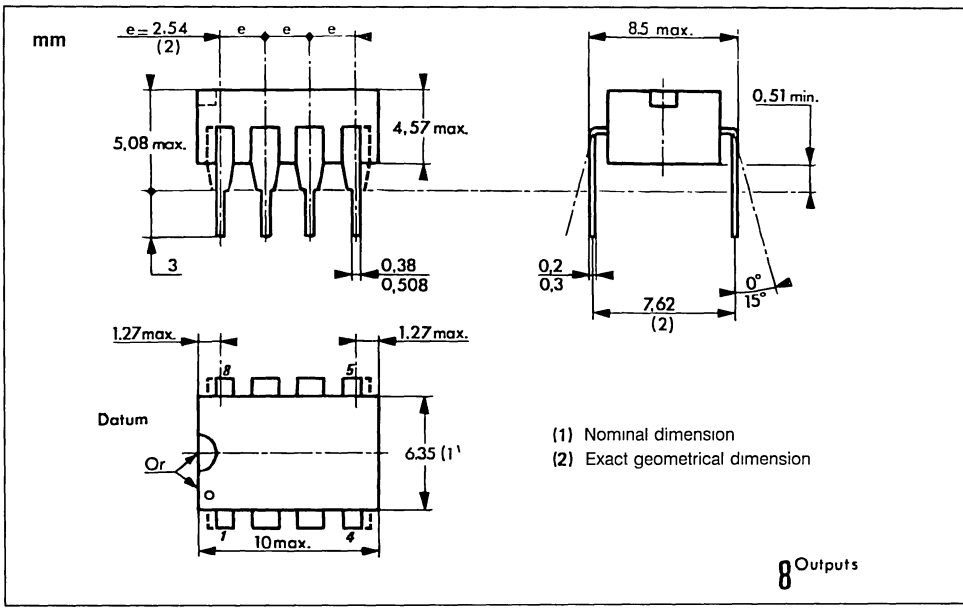
E88TL082-03

PACKAGE MECHANICAL DATA

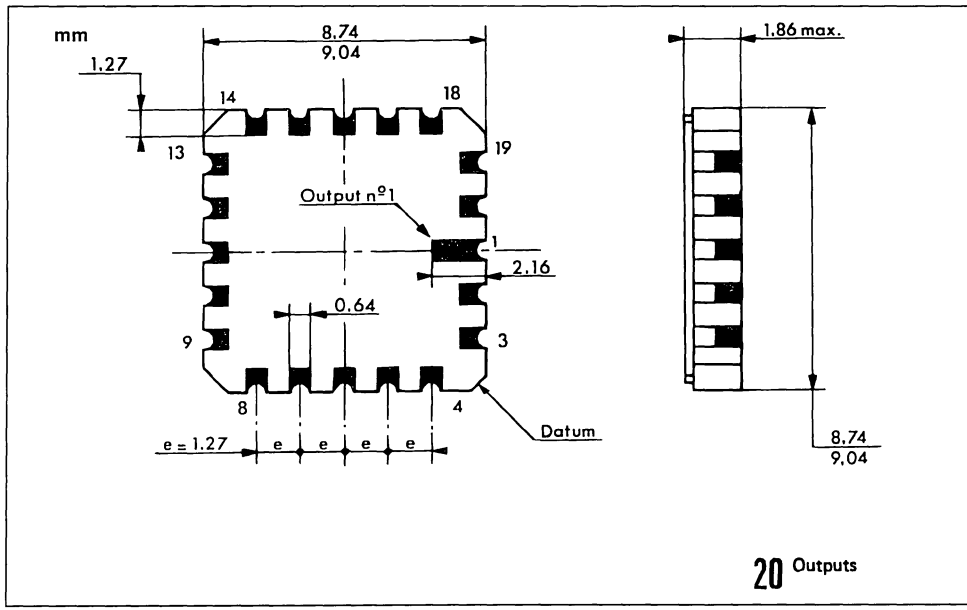
8 PINS - PLASTIC MICROPACKAGE (SO)



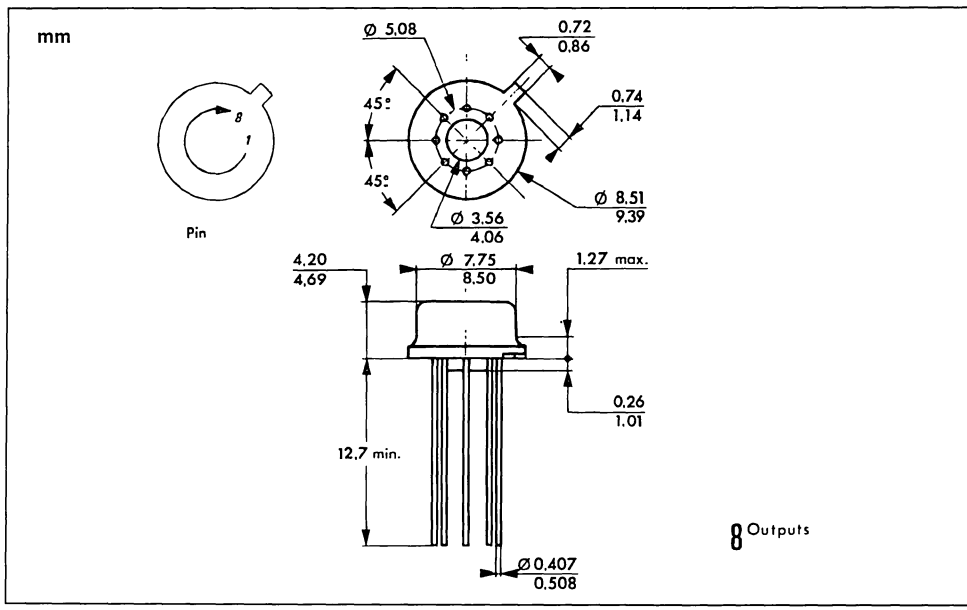
8 PINS – PLASTIC DIP



20 PINS - TRICECOP (LCC)



TO-99 – METAL CAN

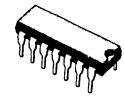


SGS-THOMSON MICROELECTRONICS

TL084
TL084A-TL084B

J–FET INPUT QUAD OP-AMPs

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J–FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 13 V/µs (typ)



N
DIP14
(Plastic package)

GC
LCC20
(Tricecop (LCC))

J
CERDIP14
(Cerdip package)

D
SO14
(Plastic micropackage)

ORDER CODES

Part Number	Temperature Range	Package			
		N	J	D	GC
TL084M	– 55 °C to + 125 °C		•		•
TL084I	– 40 °C to + 105 °C	•		•	
TL084C	0 °C to + 70 °C	•		•	
TL084AC	0 °C to + 70 °C	•		•	
TL084BC	0 °C to + 70 °C	•		•	

Note : Hi-Rel Versions Available
Examples : TL084MGC, TL084CN, TL084CD

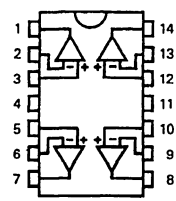
DESCRIPTION

The TL084, TL084A and TL084B are high speed J–FET input quad operational amplifiers incorporating well matched, high voltage J–FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

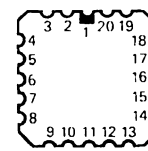
PIN CONNECTIONS (Top views)

DIP14
CERDIP14
SO14



1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^{+}
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - Output 3
9 - Inverting input 3
10 - Non-inverting input 3
11 - V_{CC}^{-}
12 - Non-inverting input 4
13 - Inverting input 4
14 - Output 4

LCC20



1 - NC
2 - Output 1
3 - Inverting input 1
4 - Non-inverting input 1
5 - NC
6 - V_{CC}^{+}
7 - NC
8 - Non-inverting input 2
9 - Inverting input 2
10 - Output 2
11 - NC
12 - Output 3
13 - Inverting input 3
14 - Non-inverting input 3
15 - NC
16 - V_{CC}^{-}
17 - NC
18 - Non-inverting input 4
19 - Inverting input 4
20 - Output 4

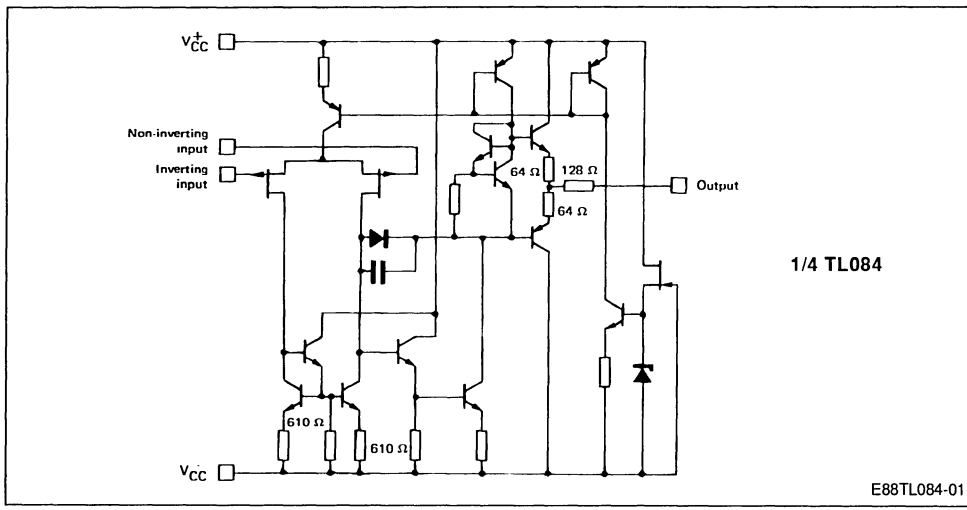
MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	± 18	V
V_i	Input Voltage (note 3)	± 15	V
V_{ID}	Differential Input Voltage (note 2)	± 30	V
P_{tot}	Power Dissipation	680	mW
	Output Short-circuit Duration (note 4)	Indefinite	
T_{oper}	Operating Free-air Temperature Range TL084C, AC, BC TL084I, BI TL084M	 0 to 70 – 40 to 105 – 55 to 125	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C

Notes : 1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.

2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded

SCHEMATIC (each amplifier)



Case	Outputs	Inverting Inputs	Non-inverting Inputs	V_{cc}^-	V_{cc}^+	N.C.
DIP14 CERDIP14 SO14	1, 7, 14, 8	2, 6, 13, 9	3, 5, 12, 10	4	11	
LCC20	2, 10, 12, 20	3, 9, 13, 19	4, 8, 14, 18	6	16	*

* **LCC20 :** Other pins are not connected

ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 15$ V (unless otherwise specified)
TL084M : $-55\ °C \le T_{amb} \le +125\ °C$
TL084I, BI : $-40\ °C \le T_{amb} \le +105\ °C$
TL084C, AC, BC: $0\ °C \le T_{amb} \le +70\ °C$

Symbol	Parameter	TL084M, I, BI TL084BC, AC			TL084C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage							mV
	T_{amb} = 25 °C (Rs ≤ 10 kΩ)		3	5		3	8	
	TL084BI, BC		1	3				
	$T_{min} \le T_{amb} \le T_{max}$			9			13	
	TL084BI, BC			5				
DV_{io}	Input Offset Voltage Drift		10			10		µV/°C
I_{io}	Input Offset Current *							
	T_{amb} = 25 °C		5	50		5	50	pA
	$T_{min} \le T_{amb} \le T_{max}$			4			4	nA
I_{ib}	Input Bias Current *							
	T_{amb} = 25 °C		30	200		30	200	pA
	$T_{min} \le T_{amb} \le T_{max}$			20			20	nA
A_{vd}	Large Signal Voltage Gain							V/mV
	(R_L > 2 kΩ, V_o = ± 10 V)							
	T_{amb} = 25 °C	50	200		50	200		
	$T_{min} \le T_{amb} \le T_{max}$	25			25			
SVR	Supply Voltage Rejection Ratio							dB
	(R_S < 10 kΩ)							
	T_{amb} = 25 °C	80	86		80	86		
	$T_{min} \le T_{amb} \le T_{max}$	80			80			
I_{cc}	Supply Current, per Amp, no Load							mA
	T_{amb} = 25 °C		1.4	2.5		1.4	2.5	
	$T_{min} \le T_{amb} \le T_{max}$			2.5			2.5	
V_i	Input Voltage Range	− 11		+ 11	− 11		+ 11	V
CMR	Common Mode Rejection Ratio							dB
	($R_S \le 10$ kΩ)							
	T_{amb} = 25 °C	80	86		70	86		
	$T_{min} \le T_{amb} \le T_{max}$	80			70			
I_{os}	Output Short-circuit Current							mA
	T_{amb} = 25 °C	10	40	60	10	40	60	
	$T_{min} \le T_{amb} \le T_{max}$	10		60	10		60	
$\pm V_{opp}$	Output Voltage Swing							V
	T_{amb} = 25 °C $R_L \ge 2$ kΩ	11	12		11	12		
	$R_L \ge 10$ kΩ	12	13.5		12	13.5		
	$T_{min} \le T_{amb} \le T_{max}$ $R_L \ge 2$ kΩ	11			11			
	$R_L \ge 10$ kΩ	12			12			
S_{vo}	Slew-rate (V_i = 10 V, R_L = 2 kΩ							V/µs
	$C_L \le 100$ pF, T_{amb} = 25 °C, unity gain)	12	16		8	16		
t_r	Rise Time							µs
	(V_i = 20 mV, R_L = 2 kΩ							
	C_L = 100 pF, T_{amb} = 25 °C, unity gain)		0.1			0.1		

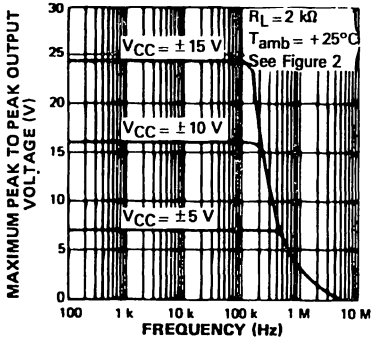
* The input bias currents are junction leakage currents wich approximatevely double for every 10 °C increase in the junction temperature

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	TL084M, I, BI TL084BC, AC			TL084C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
K_{ov}	Overshoot (V_i = 20 mV, R_L = 2 kΩ C_L < 100 pF, T_{amb} = 25 °C, unity gain)		10			10		%
GBP	Gain Bandwidth Product (f = 100 kHz, T_{amb} = 25 °C V_{in} = 10 mV, R_L = 2 kΩ, C_L = 100 pF) TL084BI, BC	2.5 3.3	4.0 4.0	5.0 5.0	2.5	4.0	5.0	MHz
R_i	Input Resistance (T_{amb} = 25 °C)		10^{12}			10^{12}		Ω
THD	Total Harmonic Distortion (f = 1 kHz, A_v = 20 dB, R_L = 2 kΩ C_L < 100 pF, T_{amb} = 25 °C, V_o = 2 V_{pp})		0.01			0.01		%
V_n	Equivalent Input Noise Voltage (f = 1 kHz, R_g = 100 Ω)		15			15		$nV/\sqrt{Hz}$
Øm	Phase Margin		45			45		Degrees
V_{O1}/V_{O2}	Channel Separation A_{vd} = 100, T_{amb} = 25 °C		120			120		dB

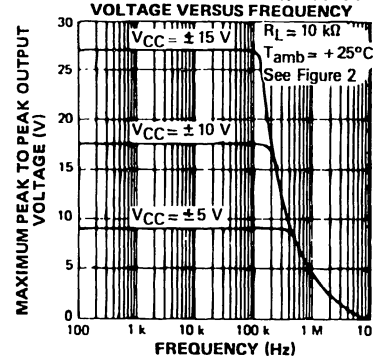
TYPICAL CHARACTERISTICS

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



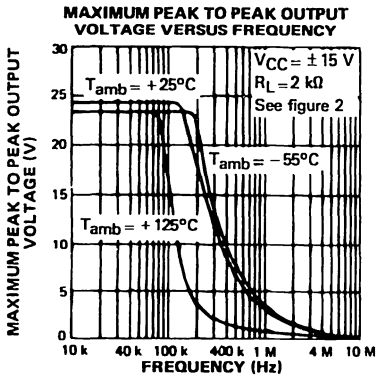
E88TL074-02

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



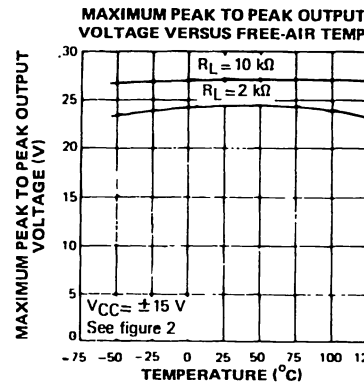
E88TL074-03

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



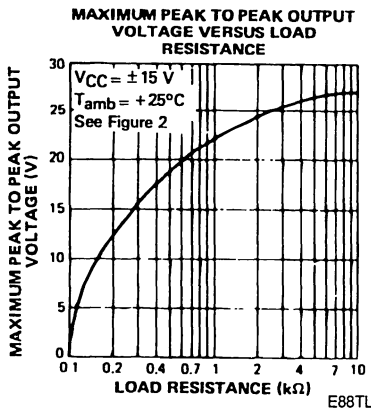
E88TL074-04

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS FREE-AIR TEMP.



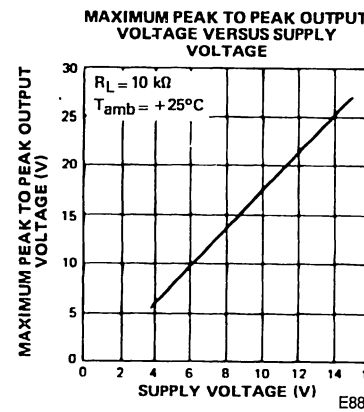
E88TL074-05

MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



E88TL074-06

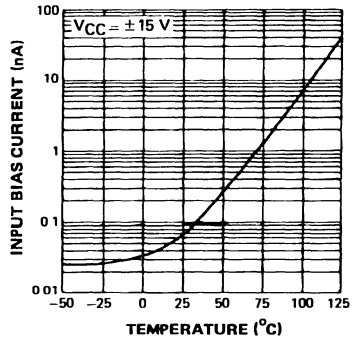
MAXIMUM PEAK TO PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



E88TL074-07

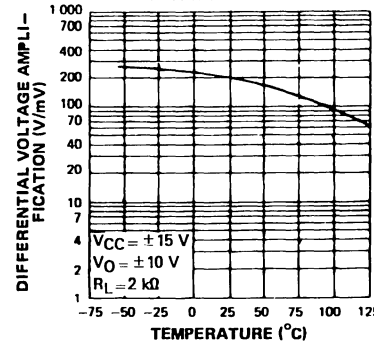
TYPICAL CHARACTERISTICS (continued)

INPUT BIAS CURRENT VERSUS FREE-AIR TEMPERATURE



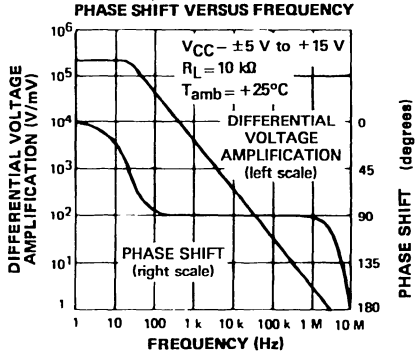
E88TL074-08

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE-AIR TEMPERATURE



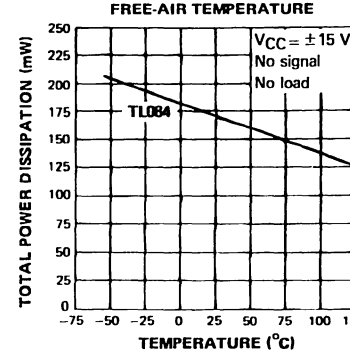
E88TL074-09

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



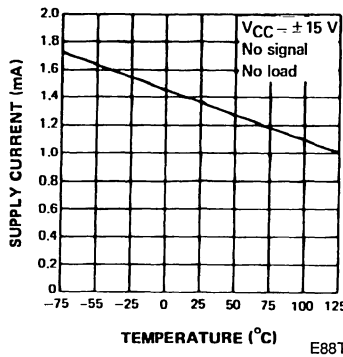
E88TL074-10

TOTAL POWER DISSIPATION VERSUS FREE-AIR TEMPERATURE



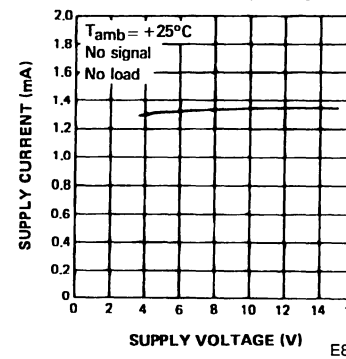
E88TL074-11

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE-AIR TEMPERATURE



E88TL074-12

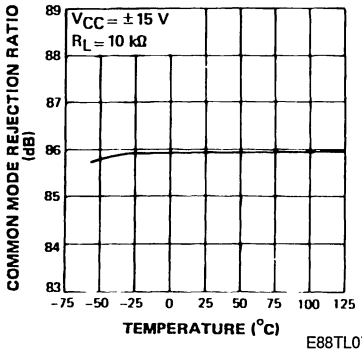
SUPPLY CURRENT PER AMPLIFIER VERSUS SUPPLY VOLTAGE



E88TL084-02

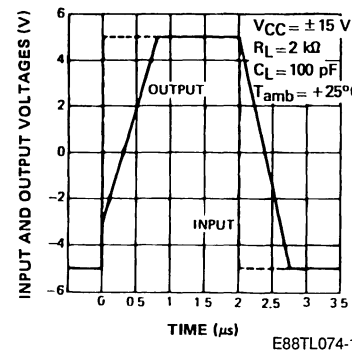
TYPICAL CHARACTERISTICS (continued)

COMMON MODE REJECTION RATIO VERSUS FREE-AIR TEMPERATURE



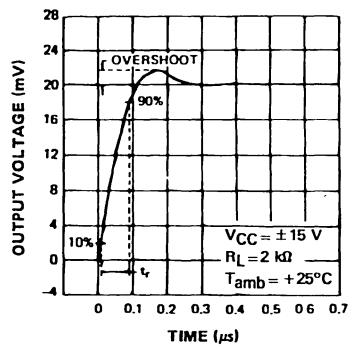
E88TL074-13

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



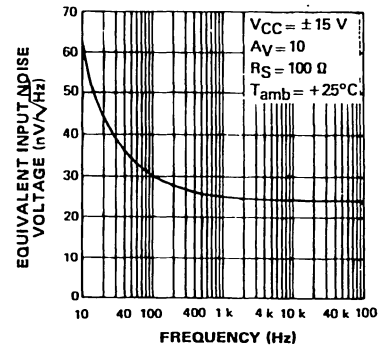
E88TL074-14

OUTPUT VOLTAGE VERSUS TIME



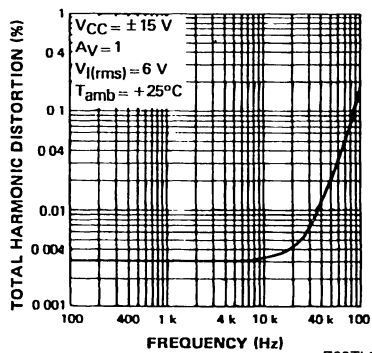
E88TL074-15

EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



E88TL074-16

TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



E88TL074-17

PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage follower.

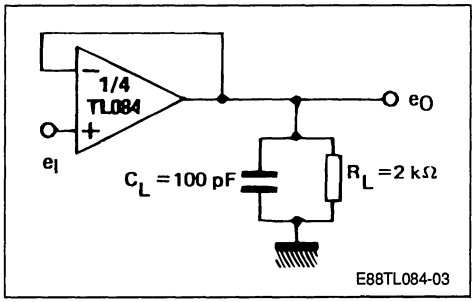
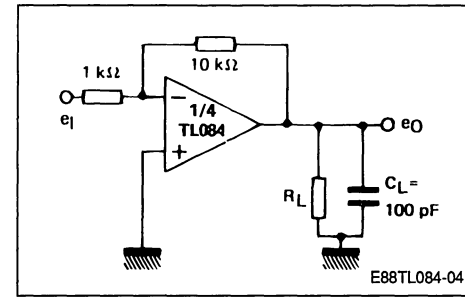
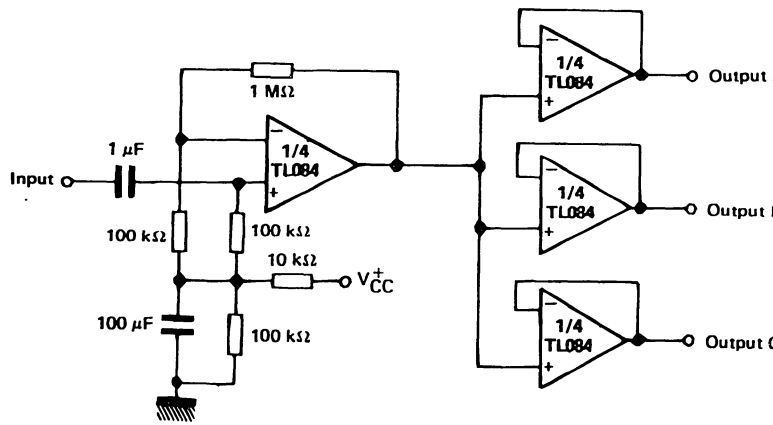


Figure 2 : Gain-of-10 inverting amplifier.



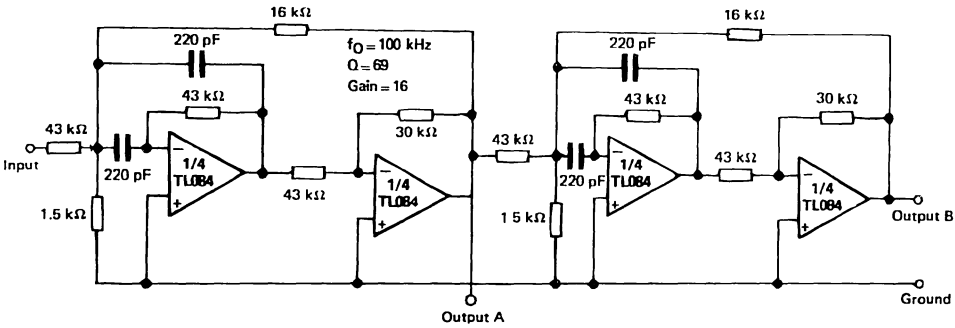
TYPICAL APPLICATION

AUDIO DISTRIBUTION AMPLIFIER
f_O = 100 kHz



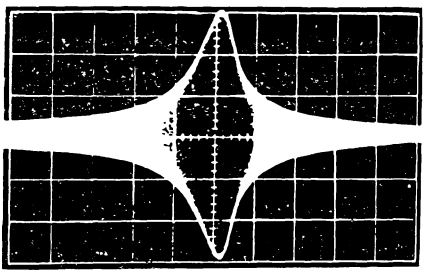
TYPICAL APPLICATION (continued)

POSITIVE FEEDBACK BANDPASS FILTER



E88TL074-21

OUTPUT A



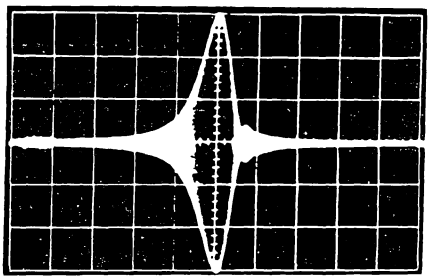
E88TL074-23

2 kHz /div

SECOND ORDER BANDPASS FILTER

f_O = 100 kHz; Q = 30; Gain = 4

OUTPUT B



E88TL074-22

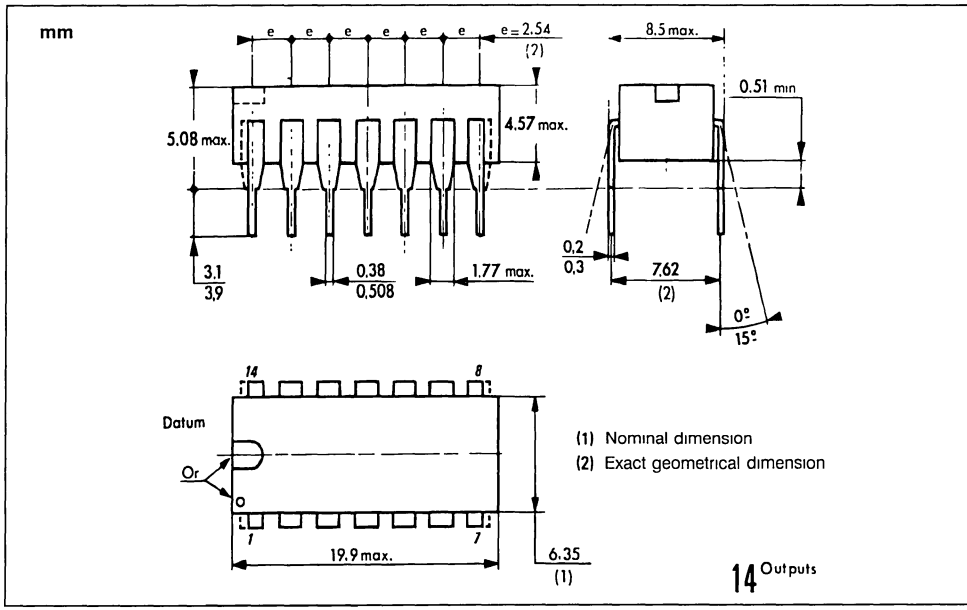
2 kHz /div

CASCADED BANDPASS FILTER

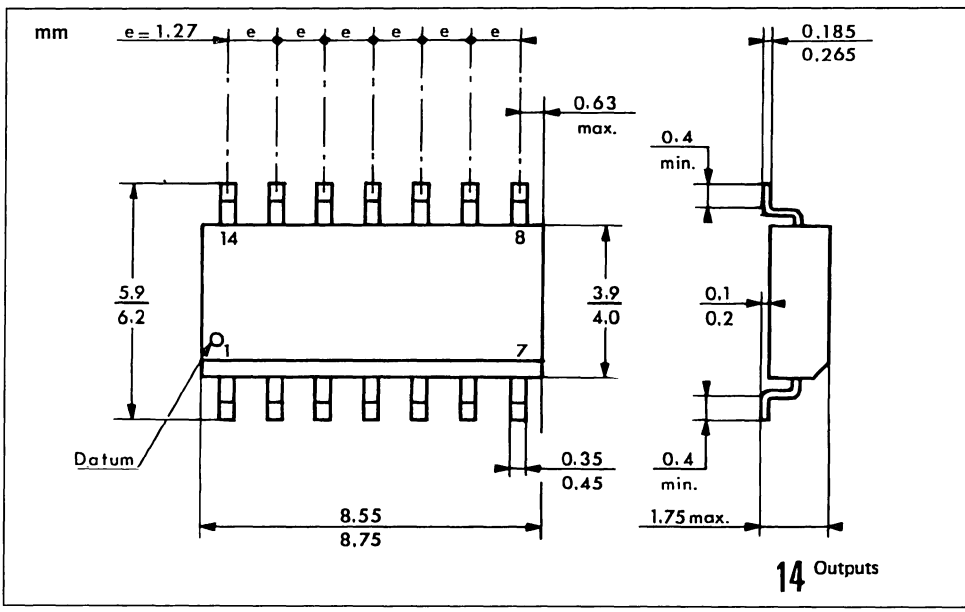
f_O = 100 kHz; Q = 69; Gain = 16

PACKAGE MECHANICAL DATA

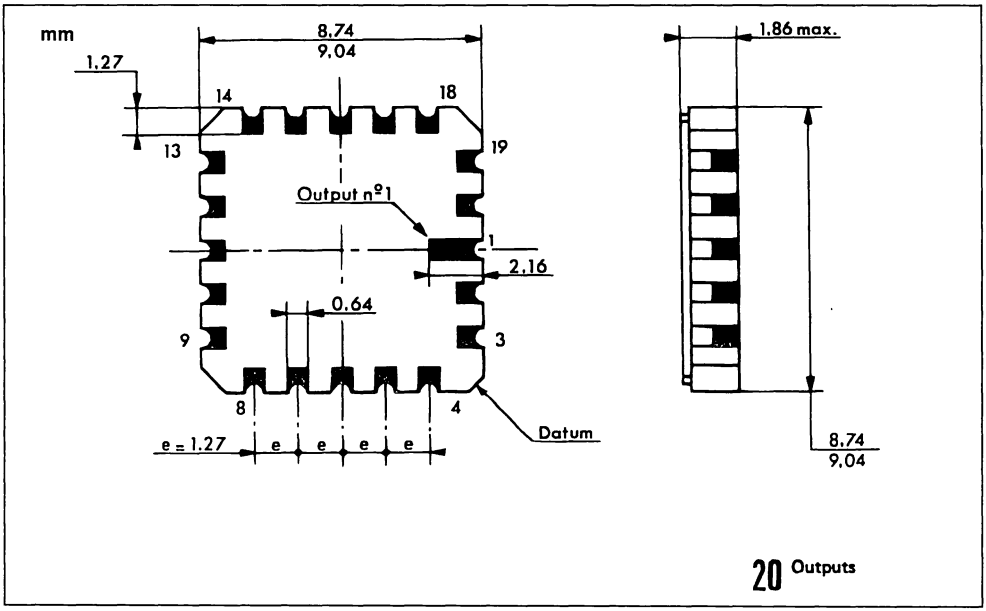
14 PINS – PLASTIC DIP OR CERDIP



14 PINS – PLASTIC MICROPACKAGE (SO)



20 PINS – TRICECOP (LCC)



SUPPLY VOLTAGE SUPERVISORS

- POWER-ON RESET GENERATOR
- AUTOMATIC RESET GENERATION AFTER VOLTAGE DROP
- WIDE SUPPLY VOLTAGE RANGE ... 3 V TO 18 V
- PRECISION VOLTAGE SENSOR
- TEMPERATURE-COMPENSATED VOLTAGE REFERENCE
- TRUE AND COMPLEMENT RESET OUTPUTS
- EXTERNALLY ADJUSTABLE PULSE WIDTH

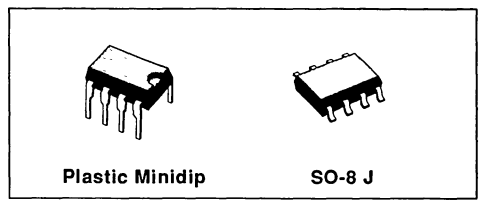
DESCRIPTION

The TL7700A series are monolithic integrated circuit supply voltage supervisors specifically designed for use as reset controllers in microcomputer and microprocessor systems. During power-up the device tests the supply voltage and keeps the RESET and $\overline{\text{RESET}}$ outputs active (high and low, respectively) as long as the supply voltage has not reached its nominal voltage value. Taking $\overline{\text{RESIN}}$ low has the same effect. To ensure that the microcomputer system has reset, the TL7700A then initiates an internal time delay that delays the return of the reset outputs to their inactive states. Since the time delay for most microcomputers and microprocessors is in the order of several machine cycles, the device internal time delay is determined by an external time delay is determined by an external capacitor connected to the C_T input (pin 3).

$t_d = 1.3 \times 10^4 \times C_T$

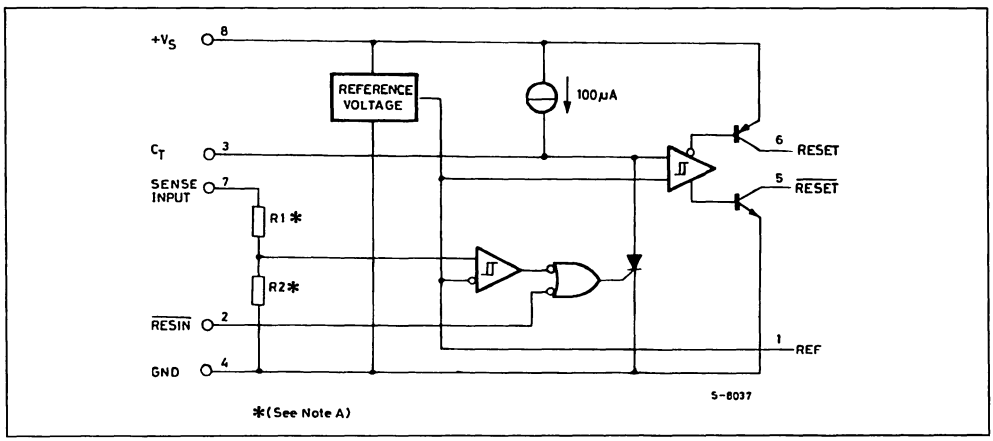
Where : C_T is in farads (F) and t_d in seconds (s). In addition, when the supply voltage drops below the nominal value, the outputs will be active until the supply voltage returns to the nominal value. An external capacitor (typically 0.1 µF) must be connected to the REF output (pin 1) to reduce the influence of fast transients in the supply voltage.

The TL7700AI series is characterized for operation from – 25°C to 85°C ; the TL7700AC series is characterized from 0°C to 70°C.



Plastic Minidip **SO-8 J**

BLOCK DIAGRAM



* TL7702A R1 = 0Ω, R2 = open ; TL7705A R1 = 7.8 KΩ, R2 = 10 KΩ ; TL7709A R1 = 19.7 KΩ, R2 = 10 KΩ ; TL7712A R1 = 32.7 KΩ, R2 = 10 KΩ ; TL7715A R1 = 43.4 KΩ, R2 = 10 KΩ

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage, V_{CC} (see note 1)	20	V
V_I	Input Voltage Range at $\overline{RESIN}$	– 0.3 to 20	V
V_I	Input Voltage at SENSE : TL7702A (see note 2)	– 0.3 to 6	V
	TL7705A	– 0.3 to 10	V
	TL7709A	– 0.3 to 15	V
	TL7712A	– 0.3 to 20	V
	TL7715A	– 0.3 to 20	V
I_{OH}	High-level Output Current at RESET	– 30	mA
I_{OL}	Low-level Output Current at $\overline{RESET}$	30	mA
T_{amb}	Operating Free-air Temperature Range : TL77XXAI	– 25 to 85	°C
	TL77XXAC	0 to 70	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C

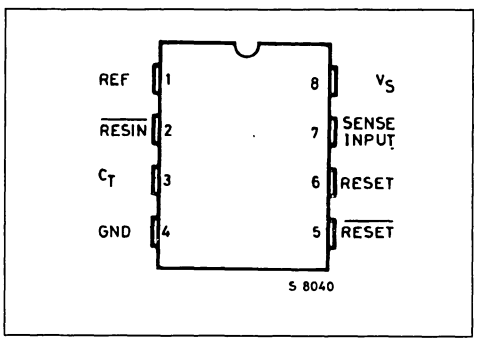
Notes : 1. All voltage values are with respect to the network ground terminal.
2. For the TL7700A, the voltage applied to the SENSE terminal must never exceed V_S.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min.	Max.	Unit
V_S	Supply Voltage		3.6	18	V
V_{IH}	High-level Input Voltage at RESIN		2		V
V_{IL}	Low-level Input Voltage at RESIN			0.6	V
V_i	Voltage at Sense Input	TL7702A	0	See Note 3	V
		TL7705A	0	10	
		TL7709A	0	15	
		TL7712A	0	20	
		TL7715A	0	20	
I_{OH}	High-level Output Current at RESET			– 16	mA
I_{OL}	Low-level Output Current at $\overline{RESET}$			16	mA
T_{amb}	Operating Free-air Temperature Range	TL77 - AI	– 25	85	°C
		TL77 - AC	0	70	

Note : 3. For proper operation of the TL7702A, the voltage applied to the SENSE terminal should not exceed V_S – 1 V or 6 V, whichever is less.

CONNECTION DIAGRAM AND ORDER CODE



Temperature Range	Plastic Minidip	SO-8
Commercial 0 to 70 °C	TL77XXACP	TL77XXACD
Industrial – 40 to 85 °C	TL77XXAIP	TL77XXAID

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	120	°C/W

ELECTRICAL CHARACTERISTICS these specifications unless otherwise specified, apply for : T_{amb} = – 25 to 85 °C (TLXXAI) ; T_{amb} = 0 to 70 °C (TL77XXAC)

Symbol	Parameter		Test Conditions (1)	Min.	Typ.	Max.	Unit
V_{OH}	High-level Output Voltage at RESET		I_{OH} = – 16 mA	V_S–1.5			V
V_{OL}	Low-Level Output Voltage at $\overline{RESET}$		I_{OL} = 16 mA			0.4	V
V_{ref}	Reference Voltage		T_{amb} = 25 °C	2.48	2.53	2.58	V
V_T	Threshold Voltage at SENSE Input	TL7702A	V_S = 3.6 V to 18 V T_{amb} = 25 °C	2.48	2.53	2.58	V
		TL7705A		4.5	4.55	4.6	
		TL7709A		7.5	7.6	7.7	
		TL7712A		10.6	10.8	11.0	
		TL7715A		13.2	13.5	13.8	
V_T	Threshold Voltage at SENSE Input	TL7702A	V_S = 3.6 V to 18 V	2.45	2.53	2.58	V
		TL7705A		4.45	4.55	4.6	
		TL7709A		7.4	7.6	7.7	
		TL7712A		10.4	10.8	11.0	
		TL7715A		13.0	13.5	13.8	
V_{T+}, V_{T-}	Hysteresis (2) at SENSE Input	TL7702A	V_S = 3.6 V to 18 V T_{amb} = 25 °C		10		mV
		TL7705A			15		
		TL7709A			20		
		TL7712A			35		
		TL7715A			45		
I_I	Input Current at $\overline{RESIN}$ Input		V_I = 2.4 V to V_S			20	µA
			V_I = 0.4 V			– 100	
I_I	Input Current at SENSE Input	TL7702A	$V_{ref} < V_I < V_S$ –1.5 V		0.5	2	
I_{OH}	High-level Output Current at $\overline{RESET}$		V_O = 18 V			50	
I_{OL}	Low-level Output Current at RESET		V_O = 0 V			– 50	
I_S	Supply Current		All Inputs and out. open		1.8	3.3	mA

Notes : 1. All characteristics are measured with C = 0.1 µF from Pin 1 to GND, and with C = 0.1 µF from Pin 3 to GND.
2. Hysteresis is the difference between the positive going input threshold voltage. V_{T+}, and the negative going input threshold voltage, V_{T-}.

SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{pi}	Pulse Width at SENSE Input	$V_{ih} = V_{ityp} + 0.04 \times V_i$ $V_{iL} = V_{ityp} - 0.04 \times V_i$	0.9			µs
t_{pi}	Pulse Width at $\overline{RESIN}$ Input		0.4			µs
t_{po}	Pulse Width at Output	$C_f = 0.1$ µF	0.65	1.3	2.6	ms
t_{pdHL}	Propagation Delay Time from $\overline{RESIN}$ to $\overline{RESET}$	$C_L = 100$ pF $V_S = 5$ V $R_L = 4.7$ KΩ			1	µs
$t_{r/f}$	Rise/Falltime at RESET and $\overline{RESET}$	$C_L = 10$ pF $V_S = 5$ V $R_L = 4.7$ KΩ			1	µs

Figure 1 : Multiple Power Supply System Reset Generation.

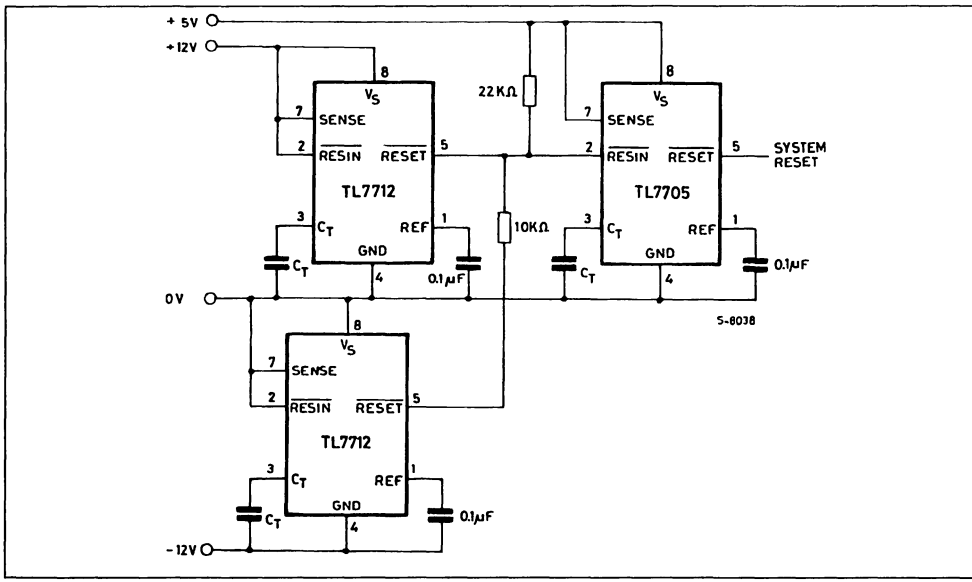
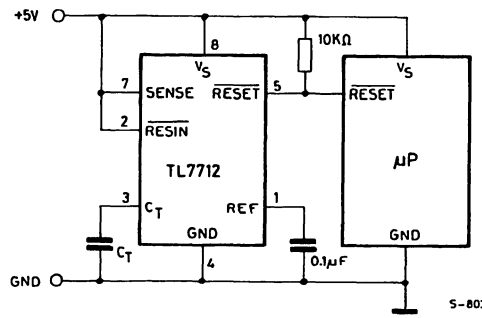
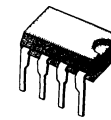


Figure 2 : Reset Controller for µP.



CMOS SINGLE OPERATIONAL AMPLIFIERS

- OFFSET NULL CAPABILITY (by external compensation)
- SYMMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT
- THE TRANSFER FUNCTION IS LINEAR
- CONSUMPTION CURRENT AND DYNAMIC PARAMETERS ARE STABLE REGARDING THE VOLTAGE POWER SUPPLY VARIATIONS
- DYNAMIC CHARACTERISTICS ADJUSTABLE BY I_{set}
- VERY LARGE I_{set} RANGE
- PIN COMPATIBLE TO SINGLE OPERATIONAL AMPLIFIER (UA776)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10 mV), A (5 mV), B (2 mV)



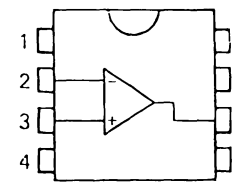
N
DIP8
(Plastic Package)

J
CERDIP8
(Cerdip Package)

D
SO8
(Plastic Micropackage)

(Order Codes at the end of the datasheet)

PIN CONNECTIONS (top view)



E88TS271-01

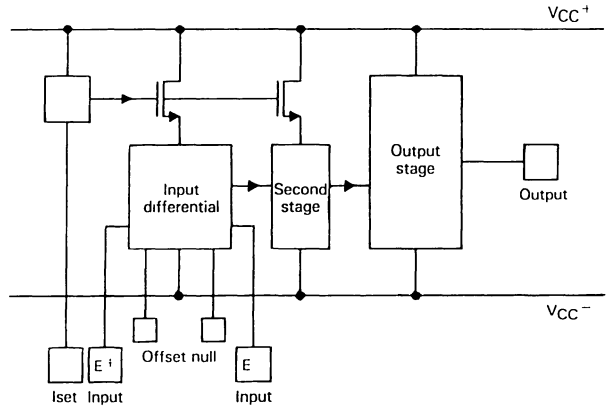
1 – Offset null 1
2 – Inverting input
3 – Non-inverting input
4 – V_{CC}^-
5 – Offset null 2
6 – Output
7 – V_{CC}^+
8 – I_{set}

DESCRIPTION

The TS271 is a low cost, low power single operational amplifier designed to operate with single or dual supplies. This operational amplifier uses the SGS-THOMSON Microelectronics silicon gate LIN MOS process giving it an excellent consumption-speed ratio. This amplifier is ideally suited for low consumption applications.
The power supply is externally programmable with a resistor connected between pins 8 and 4. It allows to choose the best consumption-speed ratio and the consumption can be minimized according to the needed speed. These devices are specified for the following I_{set} current values : 1.5 µA, 25 µA, 130 µA.

The input impedance is similar to the J-FET input impedance : very high input impedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

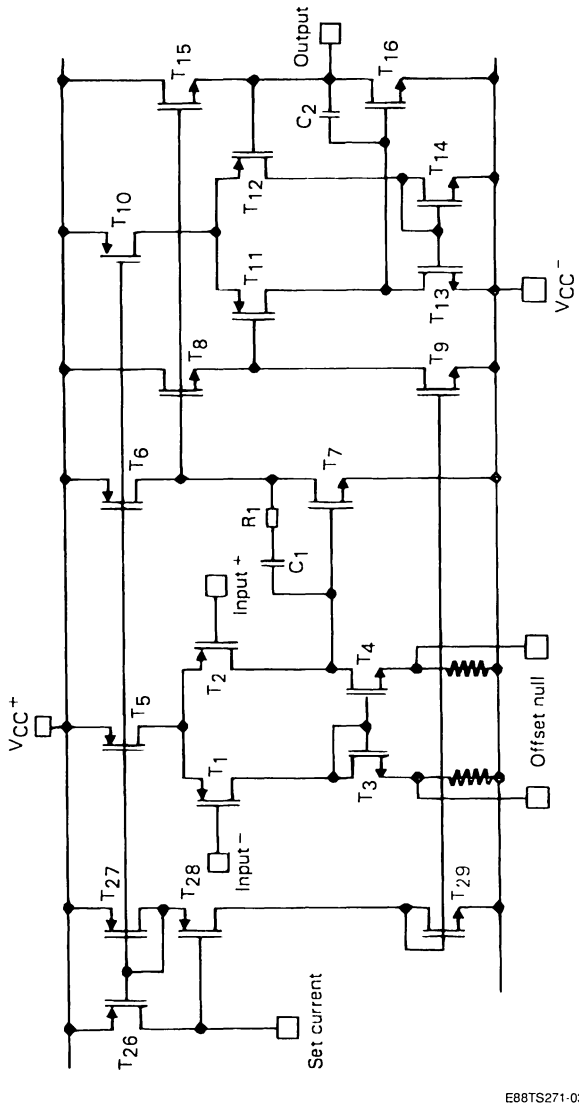
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	12	V
V_{id}	Differential Input Voltage (note 2)	± 12	V
V_i	Input Voltage (note 3)	- 0.3 to 12	V
T_{oper}	Operating Free-air Temperature TS271C TS271I TS271M	0 to 70 - 40 to 105 - 55 to 125	°C
T_{stg}	Storage Temperature	- 65 to 150	°C
I_{set}	I_{set} Range	1 to 200	µA

Notes : 1. All voltage values, except differential voltages, are with respect to network ground terminal
2. Differential voltages are at the noninverting input terminal with respect to the input terminal
3 The magnitude of the input voltage must never exceed the magnitude of the positive supply voltage.

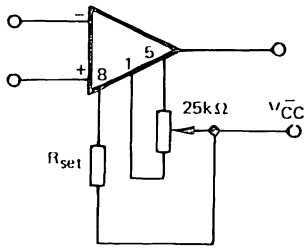
OPTIMAL OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	4 to 10	V
V_i	Common-mode Input Voltage V_{CC} = 10 V	0 to 9	V

SCHEMATIC DIAGRAM



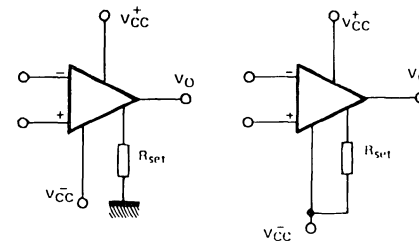
OFFSET VOLTAGE NULL CIRCUIT



E88TS271-04

OFFSET COMPENSATION GUARANTEED FOR TS271BCX (I_{set} > 25 µA), TS271ACX (I_{set} > 90 µA)

RESISTOR BIASING

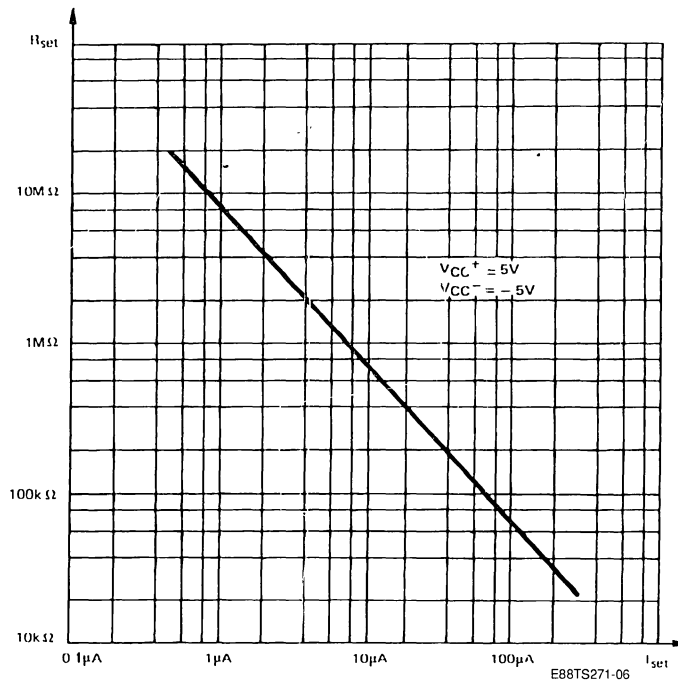


E88TS271-05

R_{set} CONNECTED TO GROUND

R_{set} CONNECTED TO V_{CC}^- (R_{set} VALUE : SEE FIG. 1)

Figure 1 : R_{set} Connected to V_{CC}^-.



E88TS271-06

ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C, V_{CC} = 10 V, I_{set} = 1.5 µA (unless otherwise specified)
R_L Connected to V_{CC} -

Symbol	Parameter	TS271C			TS271I, TS271M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS271 $T_{min} < T < T_{max}$ TS271A $T_{min} < T < T_{max}$ TS271B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		0.7			0.7		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 100		1	 200	pA
I_b	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 150		1	 300	pA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 1 mΩ $T_{min} < T < T_{max}$	8.8 8.7	9		8.8 8.6	9		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V V_i = 5 V R_L = 1 mΩ $T_{min} < T < T_{max}$	30 20	100		30 20	100		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 1 MΩ C_L = 100 pF fin = 10 KHz		0.1			0.1		MHz
CMR	Common-mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	60	80		60	80		dB
SVR•	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V, V_i = 5 V $T_{min} < T < T_{max}$		10	15 17		10	15 18	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		0.04			0.04		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 1 MΩ C_L = 10 pF C_L = 100 pF		 35 10			 35 10		Degrees
K_{OV}	Overshoot Factor C_L = 10 pF C_L = 100 pF		 40 70			 40 70		%
V_n	Input Equivalent Noise Voltage F = 1 KHz R_S = 10 Ω		70			70		nV/√Hz

Note : 1. Low output voltage is less than 50mV

ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C, V_{CC} = 10 V, I_{set} = 25 µA (unless otherwise specified)
R_L Connected to V_{CC} -

Symbol	Parameter	TS271C			TS271I, TS271M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS271 $T_{min} < T < T_{max}$ TS271A $T_{min} < T < T_{max}$ TS271B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		2			2		µV/°C
I_{io}	Input Offset Current V_i = 5 V , V_o = 5 V $T_{min} < T < T_{max}$		1	 100		1	 200	pA
I_b	Input Bias Current V_i = 5 V , V_o = 5 V $T_{min} < T < T_{max}$		1	 150		1	 300	pA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 100KΩ $T_{min} < T < T_{max}$	8.7 8.6	8.9		8.7 8.5	8.9		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V V_i = 5 V R_L = 100 KΩ $T_{min} < T < T_{max}$	30 20	50		30 10	50		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 100 KΩ C_L = 100 pF fin = 100 KHz		0.7			0.7		MHz
CMR	Common-mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	60	80		60	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V , V_i = 5 V $T_{min} < T < T_{max}$		150	200 250		150	200 300	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		0.6			0.6		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 100 KΩ C_L = 10 pF C_L = 100 pF		 50 30			 50 30		Degrees
K_{OV}	Overshoot Factor C_L = 10 pF C_L = 100 pF		 30 50			 30 50		%
V_n	Input Equivalent Noise Voltage F = 1 KHz R_S =10 Ω		38			38		nV/√Hz

Note : 1. Low output voltage is less than 50mV.

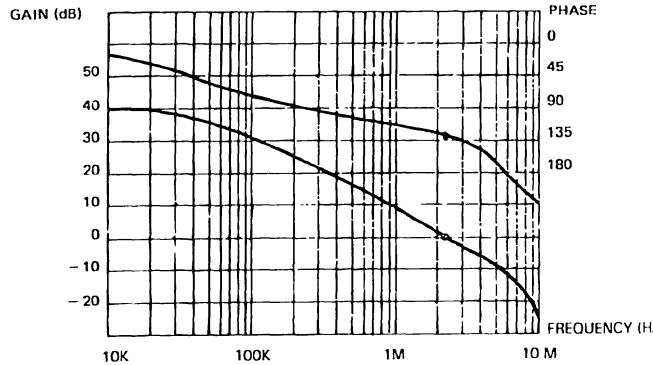
ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C, V_{CC} = 10 V, I_{set} = 130 µA (unless otherwise specified)
R_L Connected to V_{CC} -

Symbol	Parameter	TS271C			TS271I, TS271M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS271 $T_{min} < T < T_{max}$ TS271A $T_{min} < T < T_{max}$ TS271B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		5			5		µV/°C
I_{io}	Input Offset Current V_i = 5 V , V_o = 5 V $T_{min} < T < T_{max}$		1	 100		1	 200	pA
I_b	Input Bias Current V_i = 5 V , V_o = 5 V $T_{min} < T < T_{max}$		1	 150		1	 300	pA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 10 KΩ $T_{min} < T < T_{max}$	8.2 8.1	8.4		8.2 8	8.4		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V V_i = 5 V R_L = 10 KΩ $T_{min} < T < T_{max}$	10 7	15		10 6	15		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 10 KΩ C_L = 100 pF fin = 200 KHz		2.3			2.3		MHz
CMR	Common-mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	60	80		60	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	70		60	70		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V , V_i = 5 V $T_{min} < T < T_{max}$		800	1300 1400		800	1300 1500	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		4.5			4.5		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 10 KΩ C_L = 10 pF C_L = 100 pF		 56 56			 56 56		Degrees
K_{OV}	Overshoot Factor C_L = 10 pF C_L = 100 pF		 30 30			 30 30		%
V_n	Input Equivalent Noise Voltage F =1 KHz R_S = 10 Ω		30			30		nV/√Hz

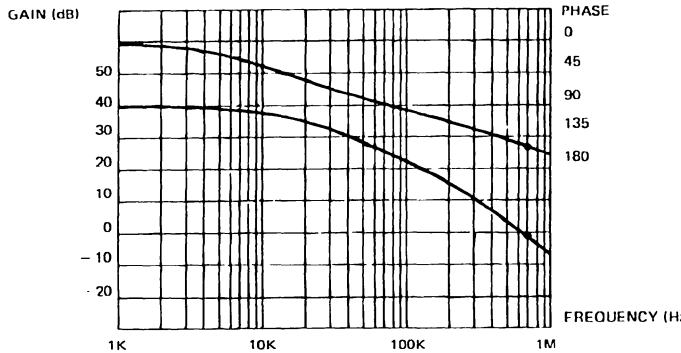
Note : 1. Low output voltage is less than 50mV.

I_{set} = 130 µA



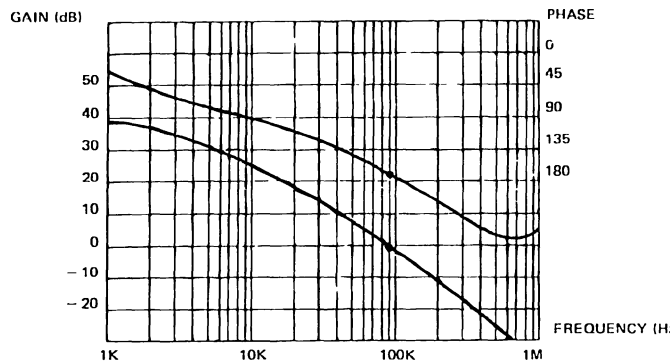
OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
$V_{CC} \pm 5$ V, $R_L = 10$ KΩ, $C_L = 100$ pF, $T_{amb} = 25$ °C E88TS271-07

I_{set} = 25 µA



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
$V_{CC} \pm 5$ V, $R_L = 100$ KΩ, $C_L = 100$ pF, $T_{amb} = 25$ °C E88TS271-08

I_{set} = 1.5 µA



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
$V_{CC} \pm 5$ V, $R_L = 1$ MΩ, $C_L = 100$ pF, $T_{amb} = 25$°C E88TS271-09

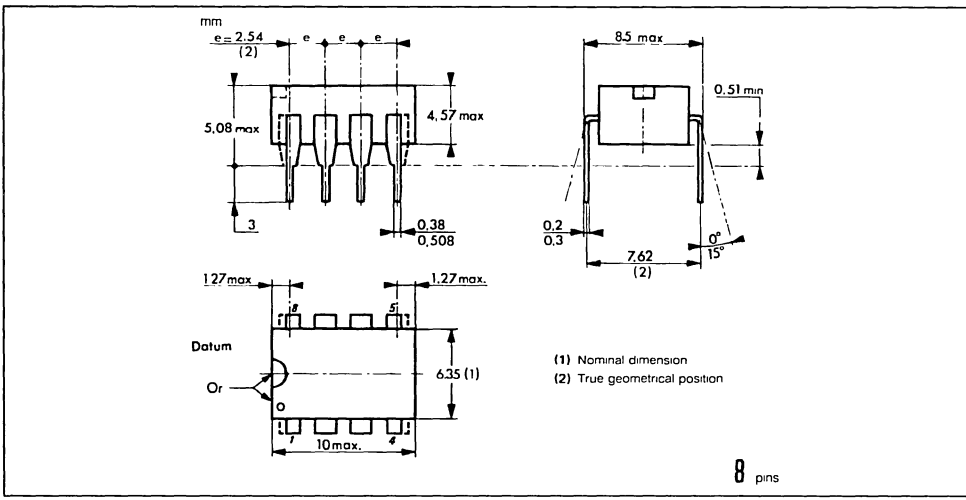
ORDER CODES

Part Number	Temperature Range °C	Package		
		N	D	J
TS271C	0 to + 70	•	•	
TS271AC	0 to + 70	•	•	
TS271BC	0 to + 70	•	•	
TS271I	- 40 to + 105	•	•	
TS271M	- 55 to + 125			•
TS271AI	- 40 to + 105	•	•	
TS271AM	- 55 to + 125			•
TS271BI	- 40 to + 105	•	•	
TS271BM	- 55 to + 125			•

Examples : TS271 ACN, TS271 CD

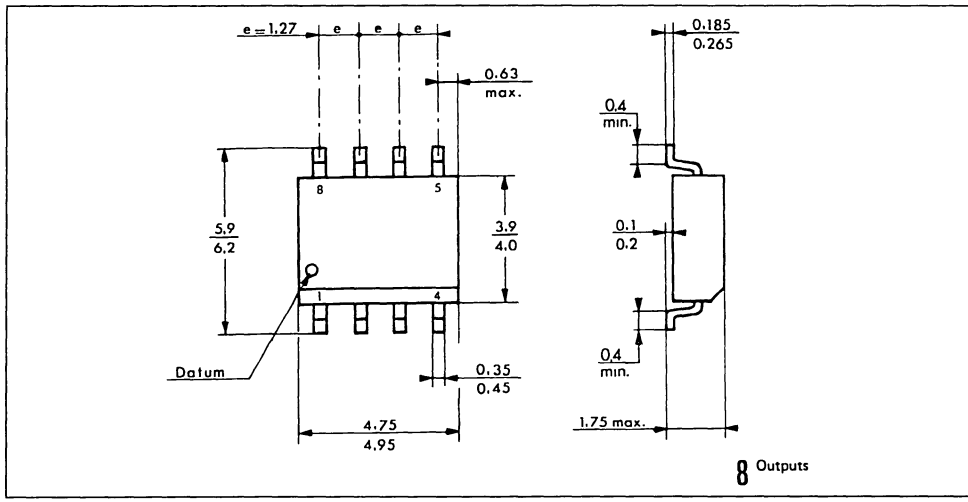
PACKAGE MECHANICAL DATA

8 PINS – PLASTIC DIP OR CERDIP



PACKAGE MECHANICAL DATA (continued)

8 PINS – PLASTIC MICROPACKAGE SO

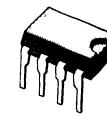


SGS-THOMSON MICROELECTRONICS

TS272
TS27M2/TS27L2

CMOS DUAL OPERATIONAL AMPLIFIERS

- EXCELLENT PHASE MARGIN ON CAPACITANCE LOADS
- SYMMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT FOR TS272
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN COMPATIBLE TO STANDARD DUAL OPERATIONAL AMPLIFIERS (TL082 - LM358)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10 mV), A (5 mV), B (2 mV)



N
DIP8
(Plastic package)

J
CERDIP8
(Cerdip package)

D
SO8
(Plastic micropackage)

(Order Codes at the end of the Data sheet)

DESCRIPTION

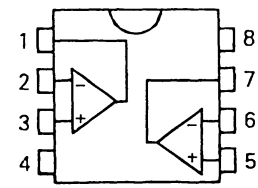
The TS272 series are low cost, low power dual operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS THOMSON Microelectronics silicon gate LIN MOS process giving them an excellent consumption speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio.

- I_{CC} = **10** µA per amplifier : TS27L2 (Low bias versions)
- I_{CC} = **150** µA per amplifier : TS27M2 (Medium bias versions)
- I_{CC} = **1 mA** per amplifier : TS272 (High bias versions)

The input impedance is similar to the J-FET input impedance. Very high input impedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

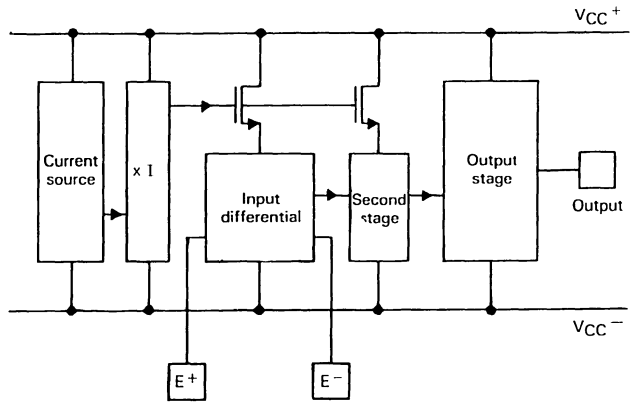
PIN CONNECTIONS (top view)



E88TS272-01

1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

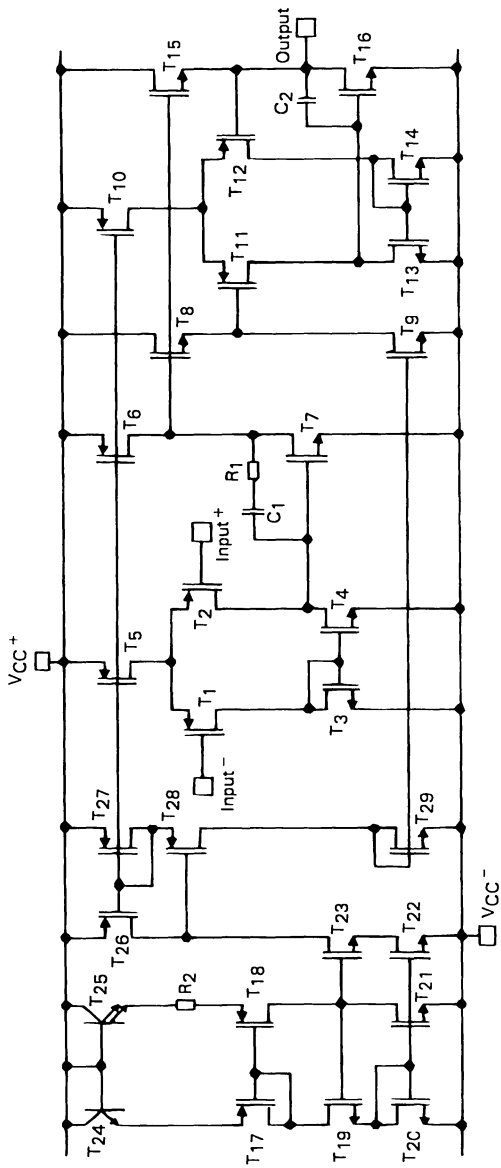
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	12	V
V_{id}	Differential Input Voltage (note 2)	± 12	V
V_i	Input Voltage (note 3)	– 0.3 to 12	V
T_{oper}	Operating Free-air Temperature		
	TS272C	0 to 70	°C
	TS272I	– 40 to 105	
	TS272M	– 55 to 125	
	TS27M2C	0 to 70	
	TS27M2I	– 40 to 105	
	TS27M2M	– 55 to 125	
	TS27L2C	0 to 70	
	TS27L2I	– 40 to 105	
	TS27L2M	– 55 to 125	
T_{stg}	Storage Temperature	– 65 to 150	°C

Notes : 1. All voltage values, except differential voltages, are with respect to network ground terminal
2 Differential voltages are at the non-inverting input terminal respect to the terminal
3 The magnitude of the input voltage must never exceed the magnitude of the positive supply voltage

OPTIMAL OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	4 to 10	V
V_i	Common Mode Input Voltage V_{CC} = 10 V	0 to 9	V

SCHEMATIC DIAGRAM (For 1/2 TS27x2)



E88TS272-03

ELECTRICAL CHARACTERISTICS FOR TS272

T_{amb} = 25 °C, V_{CC} = 10 V (unless otherwise specified)
R_L Connected to V_{CC} −

Symbol	Parameter	TS272C			TS272I/TS272M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS272 $T_{min} < T < T_{max}$ TS272A $T_{min} < T < T_{max}$ TS272B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		5			5		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.1		1	 0.2	pA nA
I_{IB}	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.15		1	 0.3	pA nA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 10 kΩ $T_{min} < T < T_{max}$	8.2 8.1	8.4		8.2 8	8.4		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V V_i = 5 V R_L = 10 KΩ $T_{min} < T < T_{max}$	10 7	15		10 6	15		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 10 kΩ C_L = 100 pF Fin = 200 KHz		3.5			3.5		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	70		60	70		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_O = 5 V $T_{min} < T < T_{max}$		1000	1500 1600		1000	1500 1700	µA
I_s	Output Current V_i = 10 mV, V_O = 0 V	45	60	85	45	60	85	mA
I_s (sink)	Output Current V_i = − 10 mV, V_O = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		5.5			5.5		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 10 kΩ C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot Factor		30			30		%
V_n	Input Equivalent Noise Voltage f = 1 KHz R_S = 10 Ω		30			30		nV/√Hz
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

Note : 1. Low output voltage is less than 50mV.

ELECTRICAL CHARACTERISTICS FOR TS27M2

T_{amb} = 25 °C, V_{CC} = 10 V (unless otherwise specified)
R_L Connected to V_{CC} –

Symbol	Parameter	TS27M2C			TS27M2I/TS27M2M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS27M2 $T_{min} < T < T_{max}$ TS27M2A $T_{min} < T < T_{max}$ TS27M2B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		2			2		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.1		1	 0.2	pA nA
I_{IB}	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.15		1	 0.3	pA nA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 100 kΩ $T_{min} < T < T_{max}$	 8.7 8.6	 8.9		 8.7 8.5	 8.9		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V R_L = 100 kΩ V_i = 5 V $T_{min} < T < T_{max}$	 30 20	 50		 30 10	 50		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 100 kΩ C_L = 100 pF Fin = 100 KHz		1			1		MHz
CMR	Common-mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V $T_{min} < T < T_{max}$		150	200 250		150	200 300	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{vo}	Slew Rate at Unity Gain		0.6			0.6		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 100 kΩ C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot Factor		30			30		%
V_n	Input Equivalent Noise Voltage f = 1 KHz R_S = 10 Ω		38			38		nV/√Hz
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

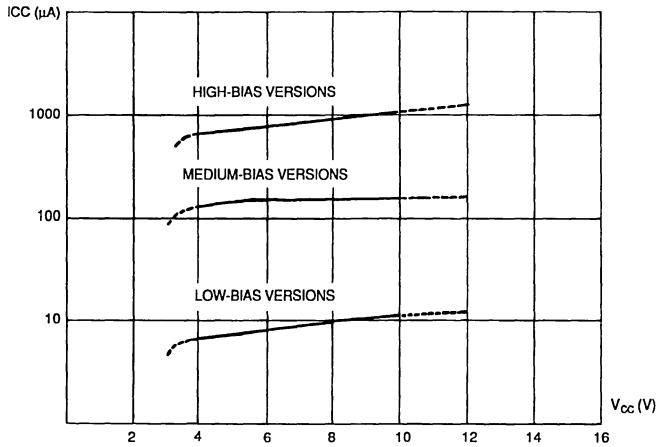
Note : 1. Low output voltage is less than 50mV

ELECTRICAL CHARACTERISTICS FOR TS27L2

T_{amb} = 25 °C, V_{CC} = 10 V (unless otherwise specified)
R_L Connected to V_{CC} −

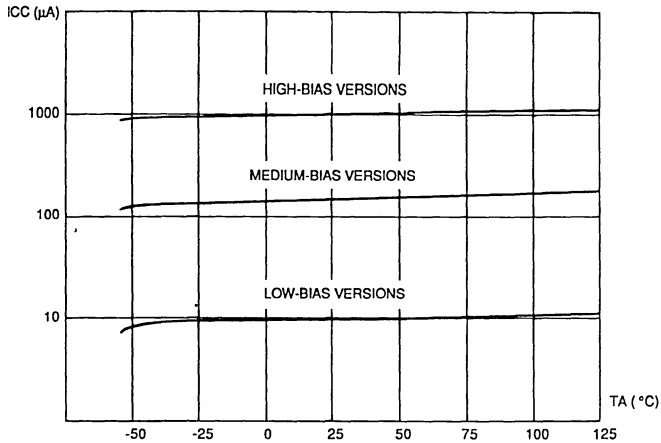
Symbol	Parameter	TS27L2C			TS27L2I/TS27L2M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS27L2 $T_{min} < T < T_{max}$ TS27L2A $T_{min} < T < T_{max}$ TS27L2B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		0.7			0.7		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.1		1	 0.2	pA nA
I_{IB}	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.15		1	 0.3	pA nA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 1 MΩ $T_{min} < T < T_{max}$	 8.8 8.7	 9		 8.8 8.6	 9		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V R_L = 1 MΩ V_i = 5 V $T_{min} < T < T_{max}$	 60 45	 100		 60 40	 100		V/mV
G_{wr}	Gain Bandwidth Product A_V = 40 dB R_L = 1 MΩ C_L = 100 pF Fin = 100 KHz		0.1			0.1		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V $T_{min} < T < T_{max}$		10	15 17		10	15 18	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		0.04			0.04		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 1 MΩ C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot Factor		30			30		%
V_n	Input Equivalent Noise Voltage f = 1 KHz R_S = 10 Ω		70			70		nV/√Hz
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

Note : 1. Low output voltage is less than 50mV



SUPPLY CURRENT vs FREE-AIR TEMPERATURE
$V_O = V_{IC} = 0.2\ V_{CC}$, $T_{amb} = 25$ °C, NO LOAD

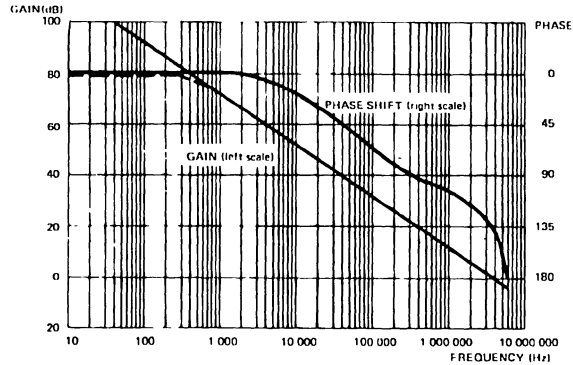
E88TS272-04



SUPPLY CURRENT vs FREE-AIR TEMPERATURE
$V_{CC} = 10$ V, $V_{IC} = 5$ V, $V_O = 5$ V, NO LOAD

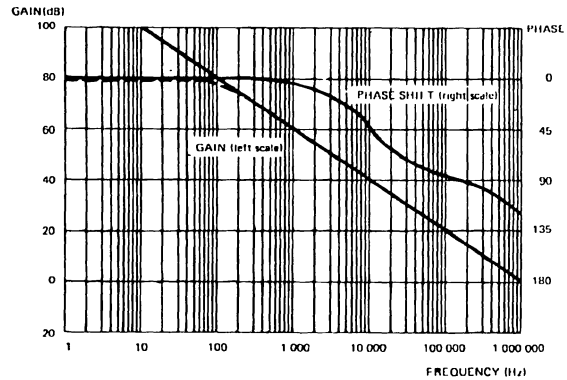
E88TS272-05

TS272



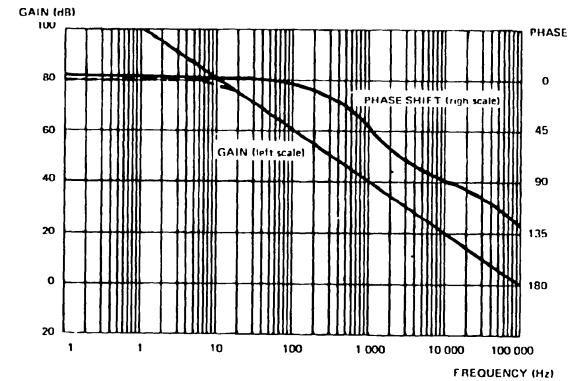
OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} = 10V, R_L = 10kΩ, C_L = 100pF, T_{amb} = 25°C E88TS272-06

TS27M2



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} = 10V, R_L = 100kΩ, C_L = 100pF, T_{amb} = 25°C E88TS272-07

TS27L2



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} = 10V, R_L = 1MΩ, C_L = 100pF, T_{amb} = 25°C E88TS272-08

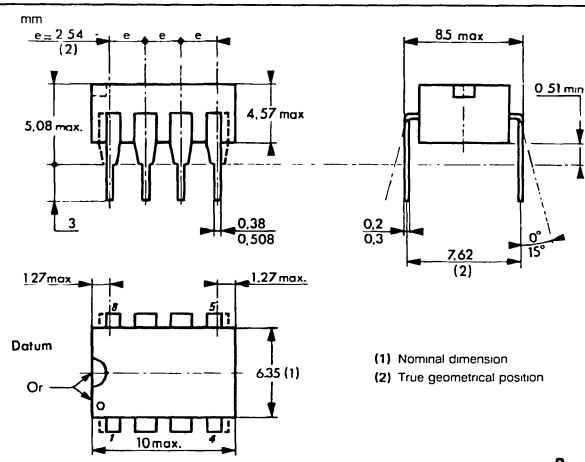
ORDER CODES

Part Number	Temperature Range °C	Package		
		N	D	J
TS272C	0 to 70	•	•	
TS272AC	0 to 70	•	•	
TS272BC	0 to 70	•	•	
TS272I	– 40 to 105	•	•	
TS272M	– 55 to 125			•
TS27M2C	0 to 70	•	•	
TS27M2AC	0 to 70	•	•	
TS27M2BC	0 to 70	•	•	
TS27M2I	– 40 to 105	•	•	
TS27M2M	– 55 to 125			•
TS27L2C	0 to 70	•	•	
TS27L2AC	0 to 70	•	•	
TS27L2BC	0 to 70	•	•	
TS27M2I	– 40 to 105	•	•	
TS27L2M	– 55 to 125			•
TS272AI	– 40 to 105	•	•	
TS272BI	– 40 to 105	•	•	
TS272AM	– 55 to 125			•
TS272BM	– 55 to 125			•
TS27M2AI	– 40 to 105	•	•	
TS27M2BI	– 40 to 105	•	•	
TS27L2AI	– 40 to 105	•	•	
TS27L2BI	– 40 to 105	•	•	
TS27M2AM	– 55 to 125			•
TS27M2BM	– 55 to 125			•
TS27L2AM	– 55 to 125			•
TS27L2BM	– 55 to 125			•

Examples : TS27L2ACN, TS272CD

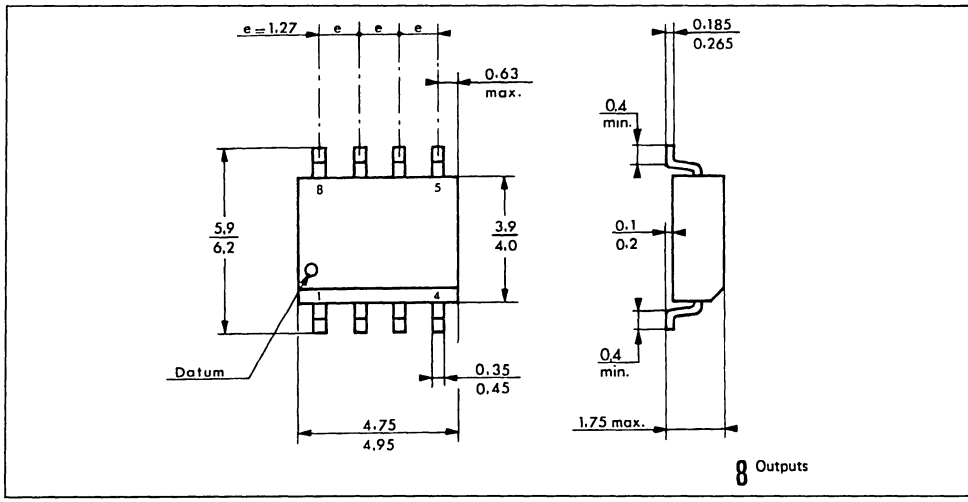
PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP OR CERDIP



PACKAGE MECHANICAL DATA (continued)

8 PINS - PLASTIC MICROPACKAGE SO

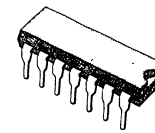


SGS-THOMSON MICROELECTRONICS

TS274
TS27M4/TS27L4

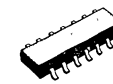
CMOS QUAD OPERATIONAL AMPLIFIERS

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT FOR TS274
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN COMPATIBLE TO STANDARD QUAD OPERATIONAL AMPLIFIERS (TL084-LM324)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10 mV), A (5 mV), B (2 mV)



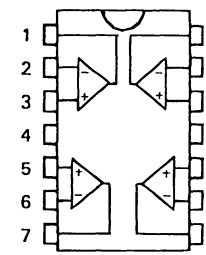
N
DIP14
(Plastic Package)

J
CERDIP14
(Cerdip Package)



D
SO14
(Plastic Micropackage)
(Order Codes at the end of the datasheet)

PIN CONNECTIONS (top view)



E88TS274-01

1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^+
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - Output 3
9 - Inverting input 3
10 - Non-inverting input 3
11 - V_{CC}^-
12 - Non-inverting input 4
13 - Inverting input 4
14 - Output 4

DESCRIPTION

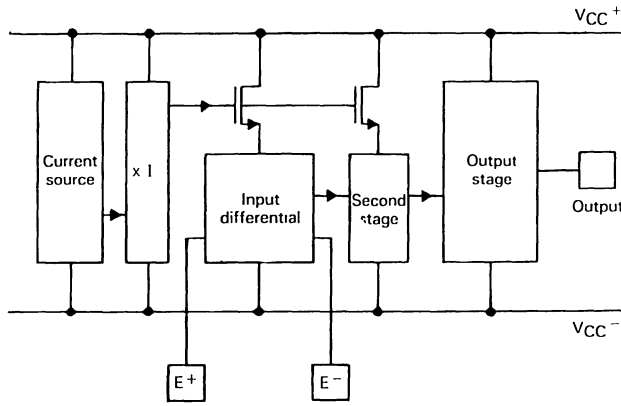
The TS274 series are low cost, low power quad operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON Microelectronics silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio.

- I_{CC} = **10 µA** per amplifier : TS27L4 (Low bias versions)
- I_{CC} = **150 µA** per amplifier : TS27M4 (Medium bias versions)
- I_{CC} = **1 mA** per amplifier : TS274 (High bias versions)

The input impedance is similar to the J-FET input impedance : very high input inpedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

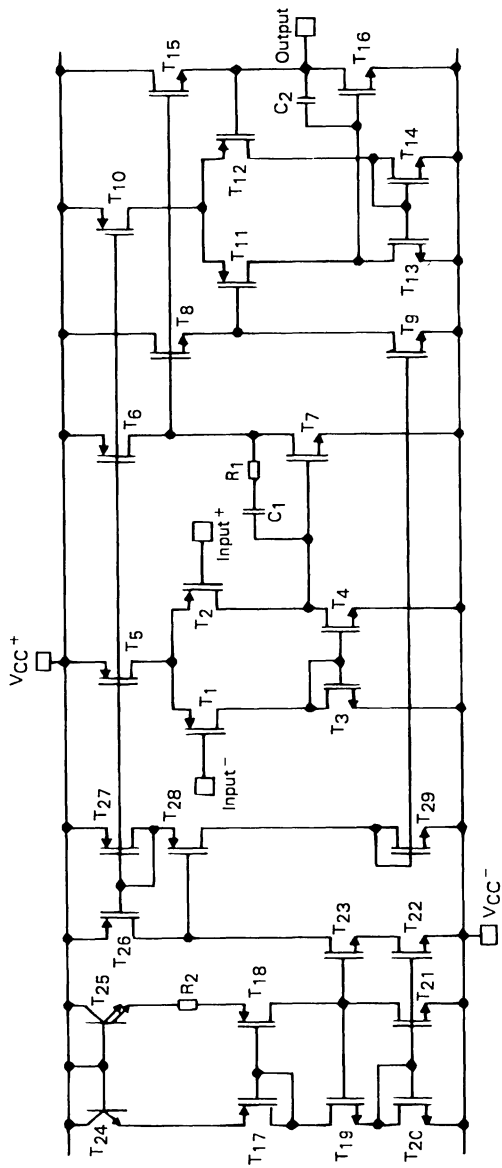
Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage (note 1)		12	V
V_{id}	Differential Input Voltage (note 2)		± 12	V
V_i	Input Voltage (note 3)		- 0.3 to 12	V
T_{oper}	Operating Free-air Temperature			
		TS274C	0 to 70	°C
		TS274I	- 40 to 105	
		TS274M	- 55 to 125	
		TS27M4C	0 to 70	
		TS27M4I	- 40 to 105	
		TS27M4M	- 55 to 125	
		TS27L4C	0 to 70	
		TS27L4I	- 40 to 105	
		TS27L4M	- 55 to 125	
T_{stg}	Storage Temperature		- 65 to 150	°C

Notes : 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2 Differential voltages are at the noninverting input terminal with respect to the input terminal
3 The magnitude of the input voltage must never exceed the magnitude of the positive supply voltage

OPTIMAL OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	4 to 10	V
V_i	Common Mode Input Voltage V_{CC} = 10 V	0 to 9	V

SCHEMATIC DIAGRAM (for 1/4 TS27 x 4)



E88TS272-03

ELECTRICAL CHARACTERISTICS FOR TS274

T_{amb} = 25 °C, V_{CC} = 10 V (unless otherwise specified)
R_L Connected to V_{CC} -

Symbol	Parameter	TS274C			TS274I/TS274M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS274 $T_{min} < T < T_{max}$ TS274A $T_{min} < T < T_{max}$ TS274B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		5			5		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.1		1	 0.2	pA nA
I_b	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.15		1	 0.3	pA nA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 10 kΩ $T_{min} < T < T_{max}$	8.2 8.1	8.4		8.2 8	8.4		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V R_L = 10 kΩ V_i = 5 V $T_{min} < T < T_{max}$	10 7	15		10 6	15		V/mV
G_{wr}	Gain Bandwidth Product A_V = 40 dB R_L = 10 kΩ C_L = 100 pF fin = 200 KHz		3.5			3.5		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	70		60	70		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V $T_{min} < T < T_{max}$		1000	1500 1600		1000	1500 1700	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		5.5			5.5		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 10 kΩ C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot Factor		30			30		%
V_n	Input Equivalent Noise Voltage f = 1 KHz R_S = 10 Ω		30			30		$nV/\sqrt{Hz}$
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

Note : 1. Low output voltage is less than 50mV.

ELECTRICAL CHARACTERISTICS FOR TS27M4

T_{amb} = 25 °C, V_{CC} = 10 V (unless otherwise specified)
R_L Connected to V_{CC} -

Symbol	Parameter	TS27M4C			TS27M4I/TS27M4M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS27M4 $T_{min} < T < T_{max}$ TS27M4A $T_{min} < T < T_{max}$ TS27M4B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		2			2		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.1		1	 0.2	pA nA
I_b	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.15		1	 0.3	pA nA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 100 kΩ $T_{min} < T < T_{max}$	8.7 8.6	8.9		8.7 8.5	8.9		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V R_L = 100 kΩ V_i = 5 V $T_{min} < T < T_{max}$	30 20	50		30 10	50		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 100 kΩ C_L = 100 pF f_{in} = 100 KHz		1			1		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V $T_{min} < T < T_{max}$		150	200 250		150	200 300	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
$S_{V\,O}$	Slew Rate at Unity Gain		0.6			0.6		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 100 kΩ C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot Factor		30			30		%
V_n	Input Equivalent Noise Voltage f = 1 KHz R_S = 10 Ω		38			38		nV/√Hz
V_{01}/V_{02}	Cross Talk Attenuation		120			120		dB

Note : 1. Low output voltage is less than 50mV.

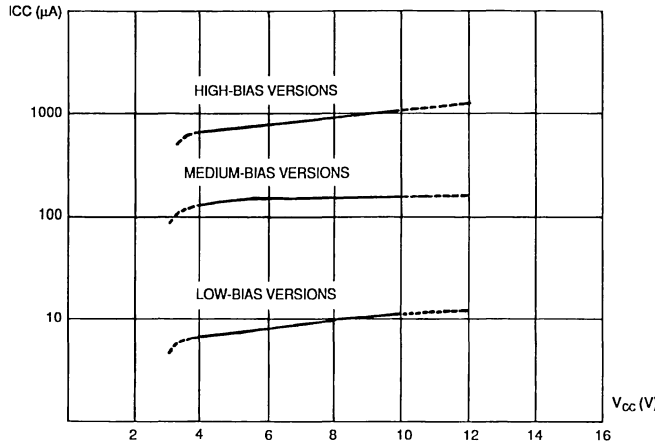
ELECTRICAL CHARACTERISTICS FOR TS27L4

T_{amb} = 25 °C, V_{CC} = 10 V (unless otherwise specified)
R_L Connected to V_{CC} -

Symbol	Parameter	TS27L4C			TS27L4I/TS27L4M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS27L4 $T_{min} < T < T_{max}$ TS27L4A $T_{min} < T < T_{max}$ TS27L4B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		0.7			0.7		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.1		1	 0.2	pA nA
I_b	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.15		1	 0.3	pA nA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 1 MΩ $T_{min} < T < T_{max}$	8.8 8.7	9		8.8 8.6	9		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V R_L = 100 kΩ V_i = 5 V $T_{min} < T < T_{max}$	60 45	100		60 40	100		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 1 MΩ C_L = 100 pF fin = 10 KHz		0.1			0.1		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V $T_{min} < T < T_{max}$		10	15 17		10	15 18	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		0.04			0.04		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 1 MΩ C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot Factor		30			30		%
V_n	Input Equivalent Noise Voltage f = 1 KHz R_S = 10 Ω		70			70		nV/√Hz
V_{O1} / V_{O2}	Cross Talk Attenuation		120			120		dB

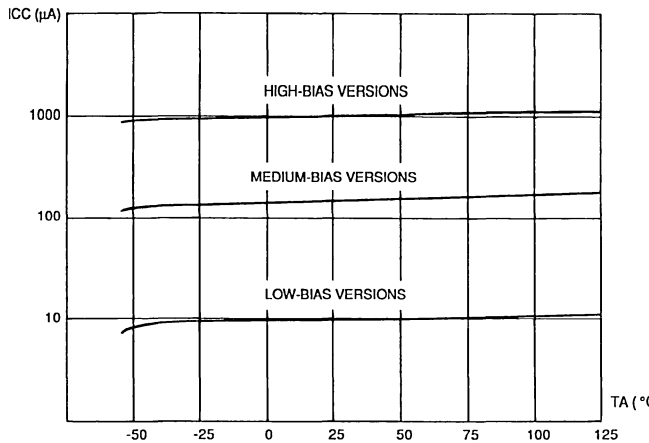
Note : 1. Low output voltage is less than 50mV.

SGS-THOMSON MICROELECTRONICS



SUPPLY CURRENT vs FREE-AIR TEMPERATURE
$V_O = V_{IC} = 0.2\ V_{CC}$, $T_{amb} = 25\ °C$, NO LOAD

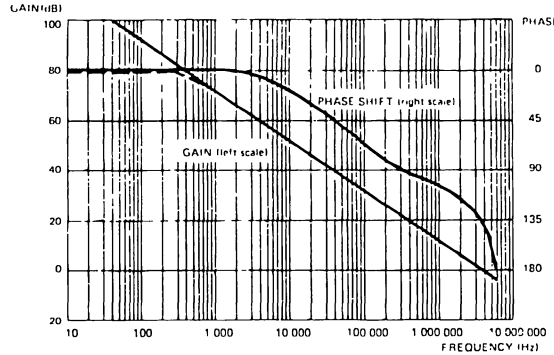
E88TS274-02



SUPPLY CURRENT vs FREE-AIR TEMPERATURE
$V_{CC} = 10\ V$, $V_{IC} = 5\ V$, $V_O = 5\ V$, NO LOAD

E88TS274-03

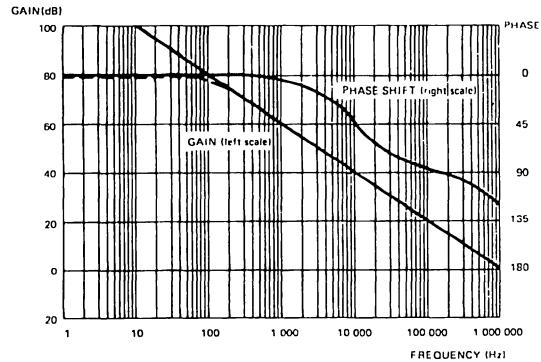
TS274



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} = 10V, R_L = 10kΩ, C_L = 100pF, T_{amb} = 25°C

E88TS274-04

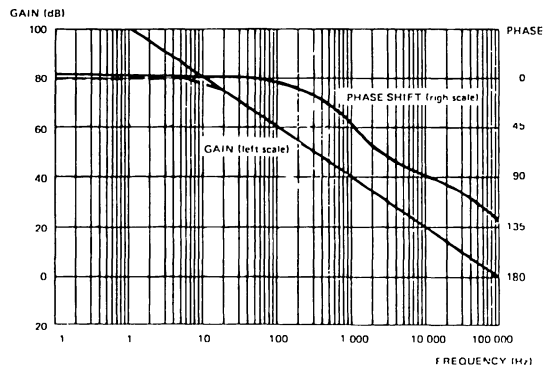
TS27M4



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} = 10V, R_L = 100kΩ, C_L = 100pF, T_{amb} = 25 °C

E88TS274-05

TS27L4



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} = 10V, R_L = 1MΩ, C_L = 100pF, T_{amb} = 25°C

E88TS274-06

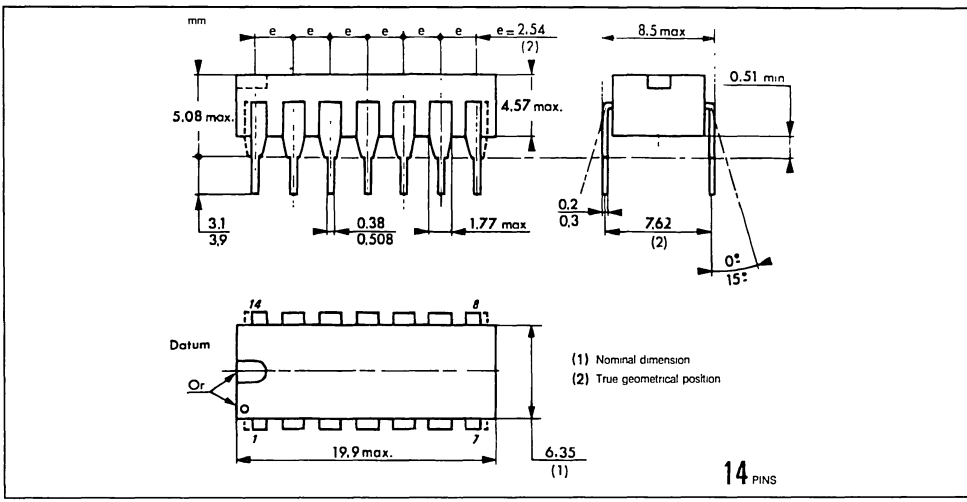
ORDER CODES

Part Number	Temperature Range °C	Package		
		N	D	J
TS274C	0 to + 70	•	•	
TS274AC	0 to + 70	•	•	
TS274BC	0 to + 70	•	•	
TS274I	- 40 to + 105	•	•	
TS274M	- 55 to + 125			•
TS27M4C	0 to + 70	•	•	
TS27M4AC	0 to + 70	•	•	
TS27M4BC	0 to + 70	•	•	
TS27M4I	- 40 to + 105	•	•	
TS27M4M	- 55 to + 125			•
TS27L4C	0 to + 70	•	•	
TS27L4AC	0 to + 70	•	•	
TS27L4BC	0 to + 70	•	•	
TS27M4I	- 40 to + 105	•	•	
TS27L4M	- 55 to + 125			•
TS27M4AI	- 40 to + 105	•	•	
TS27M4AM	- 55 to + 125			•
TS27M4BI	- 40 to + 105	•	•	
TS27M4BM	- 55 to + 125			•
TS27L4AI	- 40 to + 105	•	•	
TS27L4AM	- 55 to + 125			•
TS27L4BI	- 40 to + 105	•	•	
TS27L4BM	- 55 to ± 125			•

Examples : TS27L4ACN, TS274CD

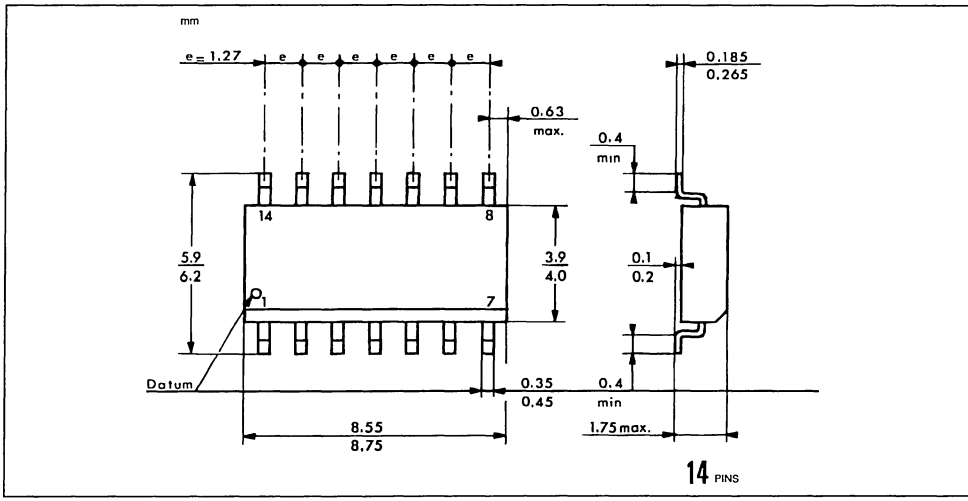
PACKAGE MECHANICAL DATA

14 PINS - PLASTIC DIP OR CERDIP



PACKAGE MECHANICAL DATA (continued)

14 PINS - PLASTIC MICROPACKAGE SO



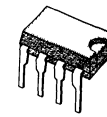
SGS-THOMSON MICROELECTRONICS

TS372

CMOS DUAL DIFFERENTIAL COMPARATOR

ADVANCE DATA

- WIDE SINGLE SUPPLY RANGE OR DUAL SUPPLIES 4V TO 10V OR ± 2V TO ± 5V
- VERY LOW SUPPLY CURRENT : 0.4 mA INDEPENDENT OF SUPPLY VOLTAGE
- EXTREMELY LOW INPUT BIAS CURRENT : 1 pA TYP
- EXTREMELY LOW INPUT OFFSET CURRENT : 1 pA TYP
- LOW INPUT OFFSET VOLTAGE
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- LOW OUTPUT SATURATION VOLTAGE 150 mV TYP
- OUTPUT COMPATIBLE WITH TTL.MOS AND CMOS
- BUILT-IN ESD PROTECTION
- HIGH INPUT IMPEDANCE 10^{12} ΩTYP
- FAST REPONSE TIME : 200 NS TYP FOR TTL LEVEL INPUT STEP



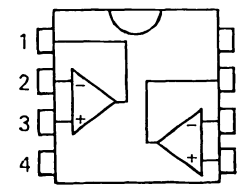
N
DIP14
(Plastic Package)

J
CERDIP14
(Cerdip Package)

D
SO14
(Plastic Micropackage)

(Order Codes at the end of the datasheet)

PIN CONNECTIONS (top view)



E88TS272-01

1 - Output 1
2 - Inverting input 1
3 - Non-inverting Input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

DESCRIPTION

These devices consist of two independent precision voltage comparators, designed to operate with single or dual supplies.

These differential comparators use the SGS THOMSON Microelectronics silicon lin MOS process giving them an excellent consumption-speed ratio.

These devices are ideally suited for low consumption applications.

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage (note 1)		12	V
V_{id}	Differential Input Voltage (note 2)		± 12	V
V_i	Input Voltage (note 3)		12	V
V_O	Output Voltage		12	V
I_O	Output Current		20	mA
	Duration of Output Short-circuit to GND (note 4)		Unlimited	
T_{oper}	Operating Free-air Temperature	TS372C TS372I TS372M	0 to 70 – 40 to 105 – 55 to 125	°C
T_{stg}	Storage Temperature		– 65 to 150	°C

Notes : 1. All voltage values, except differential voltages are with respect to network ground terminal.
2. Differential voltages are at the non-inverting input terminal with respect to the input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the positive supply voltage.
4. Short circuit from outputs to V_{CC}^+ can cause excessive heating and eventual destruction.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage Range	4 to 10	V
V_{CC}	Min Supply Voltage (for selected devices)	3	V
V_{CC}	Max Supply Voltage	12	V

ELECTRICAL CHARACTERISTICS (V_{CC} = + 5 V, T = 25 °C)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{io}	Input Offset Voltage for $V_{IC} = V_{ICR\ Min}$ (note 1)		2	10	mV
I_{io}	Input Offset Current (note 1)		1		pA
I_{ib}	Input Bias Current		1		pA
V_{ICR}	Input Common Mode Voltage Range	0 to V_{CC} – 1.5 V			V
A_{vd}	Large Signal Voltage Gain V_{CC} = 10 V ; R_L > 15 KΩ at V_{CC}		200		V/mV
I_{oh}	High Level Output Current V_{id} = 1 V ; V_{oh} = + 5 V		0.1		nA
V_{ol}	Low Level Output Voltage V_{id} = 1 V ; I_{ol} = 4 mA		150	400	mV
I_{CC}	Supply Current (4 comparators) V_{id} = – 1 V ; R_L = ∞		0.4	1	mA
I_{ol}	Low Level Output Current V_{id} = – 1 V ; V_{OL} = 1.5 V	6	16		mA
T_{re}	Response Time R_L = 5.1 KΩ ; C_L = 15 pF Overdrive 5 mV (note 2)		600		ns
T_{re}	Response Time R_L = 5.1 KΩ ; C_L = 15 pF TTL Input (note 2)		200		ns

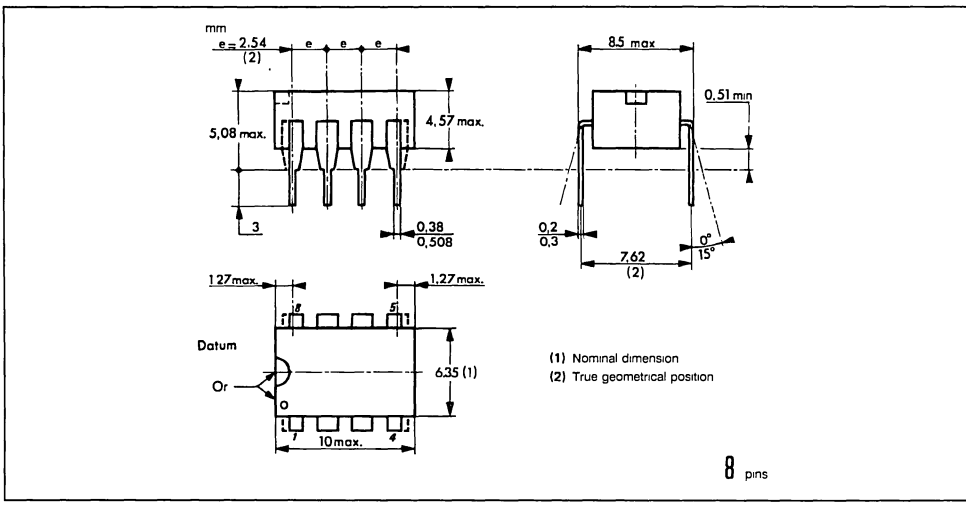
Notes : 1. The offset voltage and offset current which are given are the maximum values required to drive the output down to 400 mV or up to 4 V with R_L = 2.5 KΩ to V_{CC}.
2. The response time which is specified is the interval between the input signal and the instant when the output signal crosses 1.4 V.

ORDER CODES

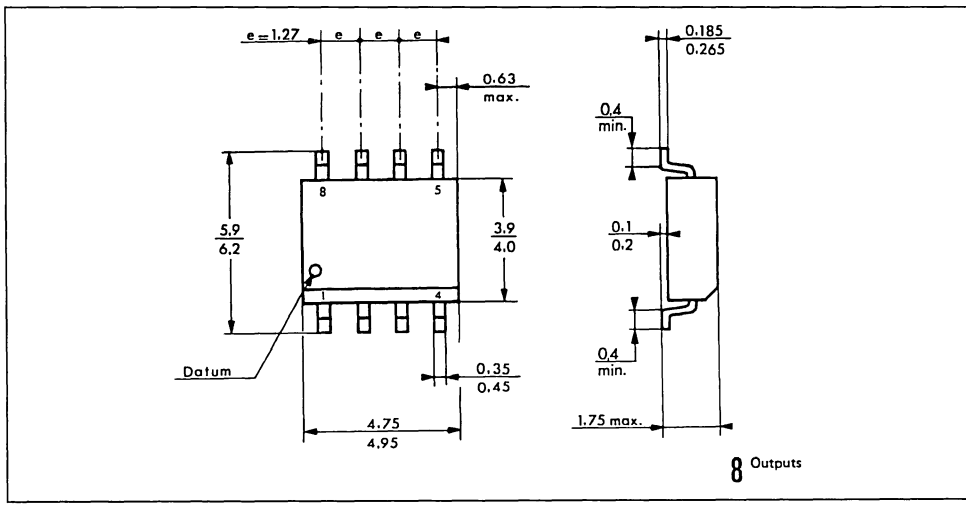
Part Number	Temperature Range	Package		
		N	D	J
TS372	0 to 70	•	•	
TS372I	– 40 to 105	•	•	
TS372M	– 55 to 125			•
Examples : TS372ID				

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP OR CERDIP



8 PINS - PLASTIC MICROPACKAGE SO



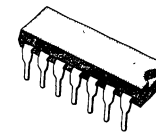
SGS-THOMSON MICROELECTRONICS

TS374

CMOS QUAD DIFFERENTIAL COMPARATOR

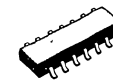
ADVANCE DATA

- WIDE SINGLE SUPPLY RANGE OR DUAL SUPPLIES 4V TO 10V OR ± 2V TO ± 5V
- VERY LOW SUPPLY CURRENT : 0.4 mA INDEPENDENT OF SUPPLY VOLTAGE
- EXTREMELY LOW INPUT BIAS CURRENT : 1 pA TYP
- EXTREMELY LOW INPUT OFFSET CURRENT : 1 pA TYP
- LOW INPUT OFFSET VOLTAGE
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- LOW OUTPUT SATURATION VOLTAGE 150 mV TYP
- OUTPUT COMPATIBLE WITH TTL.MOS AND CMOS
- BUILT-IN ESD PROTECTION
- HIGH INPUT IMPEDANCE 10^{12} ΩTYP
- FAST REPONSE TIME : 200 NS TYP FOR TTL LEVEL INPUT STEP



N
DIP14
(Plastic Package)

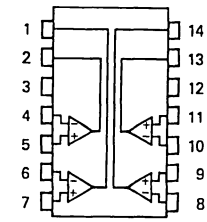
J
CERDIP14
(Cerdip Package)



D
SO14
(Plastic Micropackage)

(Order Codes at the end of the datasheet)

PIN CONNECTIONS (top view)



1 - Output 2
2 - Output 1
3 - V_{CC}^+
4 - Inverting input 1
5 - Non-inverting input 1
6 - Inverting input 2
7 - Non-inverting input 2
8 - Inverting input 3
9 - Non-inverting input 3
10 - Inverting input 4
11 - Non-inverting input 4
12 - V_{CC}^-
13 - Output 4
14 - Output 3

DESCRIPTION

These devices consist of four independent precision voltage comparators, designed to operate with single or dual supplies.

These differential comparators use the SGS THOMSON Microelectronics silicon lin MOS process giving them an excellent consumption-speed ratio.

These devices are ideally suited for low consumption applications.

This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage (note 1)		12	V
V_{id}	Differential Input Voltage (note 2)		± 12	V
V_i	Input Voltage (note 3)		12	V
V_O	Output Voltage		12	V
I_O	Output Current		20	mA
	Duration of Output Short-circuit to GND (note 4)		Unlimited	
T_{oper}	Operating Free-air Temperature	TS374C TS374I TS374M	0 to 70 – 40 to 105 – 55 to 125	°C
T_{stg}	Storage Temperature		– 65 to 150	°C

Notes : 1. All voltage values, except differential voltages are with respect to network ground terminal.
2. Differential voltages are at the non-inverting input terminal with respect to the input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the positive supply voltage.
4. Short circuit from outputs to V_{CC}^+ can cause excessive heating and eventual destruction.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage Range	4 to 10	V
V_{CC}	Min Supply Voltage (for selected devices)	3	V
V_{CC}	Max Supply Voltage	12	V

ELECTRICAL CHARACTERISTICS (V_{CC} = + 5 V, T = 25 °C)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{io}	Input Offset Voltage for $V_{IC} = V_{ICR\ Min}$ (note 1)		2	10	mV
I_{io}	Input Offset Current (note 1)		1		pA
I_{ib}	Input Bias Current		1		pA
V_{ICR}	Input Common Mode Voltage Range	0 to V_{CC} – 1.5 V			V
A_{vd}	Large Signal Voltage Gain V_{CC} = 10 V ; R_L > 15 KΩ at V_{CC}		200		V/mV
I_{oh}	High Level Output Current V_{id} = 1 V ; V_{oh} = + 5 V		0.1		nA
V_{ol}	Low Level Output Voltage V_{id} = 1 V ; I_{ol} = 4 mA		150	400	mV
I_{CC}	Supply Current (4 comparators) V_{id} = – 1 V ; R_L = ∞		0.4	1	mA
I_{ol}	Low Level Output Current V_{id} = – 1 V ; V_{OL} = 1.5 V	6	16		mA
T_{re}	Response Time R_L = 5.1 KΩ ; C_L = 15 pF Overdrive 5 mV (note 2)		600		ns
T_{re}	Response Time R_L = 5.1 KΩ ; C_L = 15 pF TTL Input (note 2)		200		ns

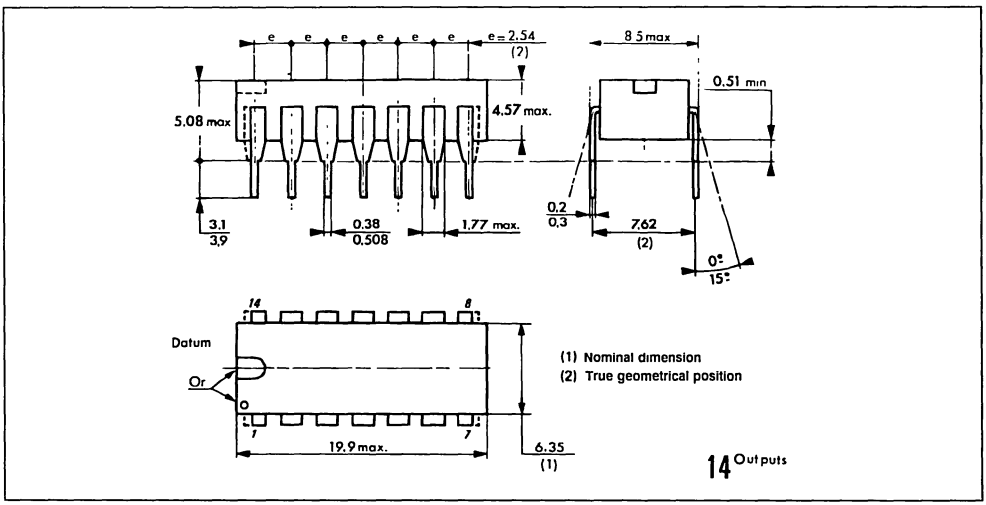
Notes : 1. The offset voltage and offset current which are given are the maximum values required to drive the output down to 400 mV or up to 4 V with R_L = 2.5 KΩ to V_{CC}.
2. The response time which is specified is the interval between the input signal and the instant when the output signal crosses 1.4 V.

ORDER CODES

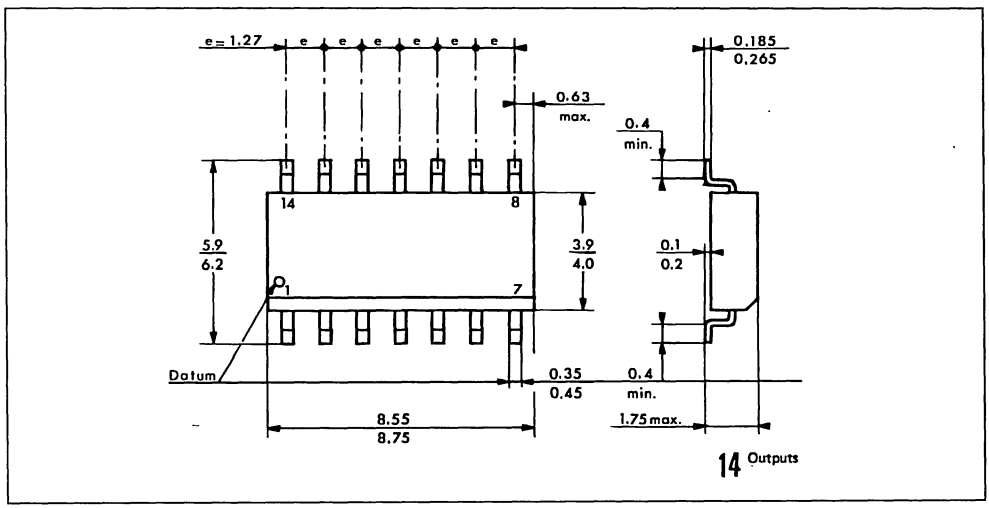
Part Number	Temperature Range	Package		
		N	D	J
TS374	0 to 70	•	•	
TS374I	– 40 to 105	•	•	
TS374M	– 55 to 125			•
Examples : TS374ID				

PACKAGE MECHANICAL DATA

14 PINS - PLASTIC DIP OR CERDIP



14 PINS - PLASTIC MICROPACKAGE SO



SGS-THOMSON MICROELECTRONICS

TSGF SERIES

MASK PROGRAMMABLE FILTERS ANALOG SWITCHED CAPACITOR FILTER ARRAYS

- HCMOS MASK PROGRAMMABLE SWITCHED CAPACITOR FILTERS : FAST DESIGN TURN-AROUND TIME (5 to 6 weeks average), THANKS TO GATE ARRAY APPROACH
- INTEGRATION OF ANY KIND OF CLASSIC, NON-CLASSIC FILTERS : BANDPASS, LOW-PASS, HIGHPASS, BAND REJECT...
- CAUER, CHEBYCHEV, BUTTERWORTH, LEGENDRE...
- FILTER ORDER : FROM 2ND TO 12TH
- CASCADABLE STRUCTURE : HIGHER ORDER ACHIEVABLE
- NO EXTERNAL COMPONENTS REQUIRED TO REALIZE THE FILTERING FUNCTION
- ADDITIONAL OPTIONS AVAILABLE ON CHIP :
  - UNCOMMITED OP-AMPS (for anti-aliasing and/or smoothing filters, half or full wave rectifiers...) ;
  - INTERNAL DIVIDER (sampling frequency generated from external clock) ;
  - OUTPUT SAMPLE-AND-HOLD
- TSGF SERIES PROVIDES :
  - LEAPFROG STRUCTURE FOR VERY LOW SENSITIVITY FILTERS ;
  - CASCADABLE BIQUADRATIC CELLS FOR NON-CLASSIC FILTER DESIGN
- TSGF SERIES FULLY SUPPORTED BY "FILCAD"® CAD SOFTWARE FROM FILTER SYNTHESIS AND SIMULATION UP TO LAYOUT
  - APPLICATION NOTES
  - EVALUATION BOARDS
  - INPUT SIGNAL FREQUENCY : 0 TO 30KHz
  - SIGNAL TO NOISE RATIO : 60 TO 85dB
- POWER SUPPLY : DUAL ± 5V
  SINGLE 0 - 10V
  SINGLE 0 - 5V
- ADJUSTABLE POWER CONSUMPTION : 0.5mW TO 20mW PER FILTER ORDER
- QUALITY FACTOR : UP TO 50
- PASS-BAND GAIN : UP TO 40dB
- INPUT SENSITIVITY : 1mVRMS (min)

DESCRIPTION

TSGF series is a family of Mask Programmable Filters (MPFs) developed by SGS-THOMSON Microelectronics.

The TSGF product range is composed of 3 switched capacitor filter base arrays, TSGF04, TSGF08 and TSGF12 providing filter integration capability from 2nd to 12th order.

TSGF04/08/12 are using "gate array" technique : the filter customization is achieved only by the final metallization mask.

Therefore TSGF series provide users with filter integration solutions with very fast design turn-around time : 5 to 6 weeks up to delivery of full tested prototypes.

TSGF04/08/12 base arrays provide on chip all necessary functions to realize all kind of filters :

- transconductance amplifiers
- switches
- capacitor fields
- sample-and-hold
- non overlapping phase generator

Additional on-chip integration capabilities are offered by TSGF products such as :

- prefiltering and post filtering functions antialiasing and smoothing filters)
- cosine filter
- output sample-and-hold driving
- power consumption adjustment
- output DC level adjustment.

TSGF series provide users a fast and complete design solution for their specific filter circuits resulting in highly accurate and reliable products thanks to switched capacitor technique.

But SGS-THOMSON filtering approach is not only limited to the Mask Programmable Filter (MPF) products.

TSGF SERIES PRODUCT RANGE

Part Number	Number of on-chips Filters	Filter Order	Uncommitted Op-amps	Clock	Output Sample-and Hold	Packages
TSGF04	1	2 to 4	1	Internal Oscillator* TTL/CMOS Levels	External* Driving	PDIP 8-14 Pins CDIP 14 Pins SO Wide 16 Pins
TSGF08	1	4 to 8	2	1 Clock Input TTL/CMOS Levels	Internal Driving	PDIP 8-16 Pins CDIP 16 Pins SO Wide 16 Pins
TSGF12	1 or 2	8 to 12	2	2 Clock Inputs TTL/CMOS Levels	External* Driving	PDIP 16-18-20 Pins CDIP 16-18-20 Pins SO Wide 18-24 Pins

* Optional.

Users are given :

- Standard Device Filters which are general purpose filters designed by SGS-THOMSON from the 3 TSGF base arrays.
  - TSG 87xx developed on TSGF04 filter array (2nd to 4th order)
  - TSG 85xx developed on TSGF08 filter array (4th to 8th order)
  - TSG 86xx developed on TSGF12 filter array (8th to 12th order).

Refer to data sheets of these standard filter products.

- "Gate Array" Filters which are the TSGF04, TSGF08, TSGF12 filter arrays described in this data sheet.
- "Standard Cell" Filters described in the TSGSM Series Data Sheet.

By offering TSGF-like macrocells in its library, the mixed analog/digital TSGSM Standard Cell family also provides filtering capabilities and then can extend integration possibilities offered by TSGF series.

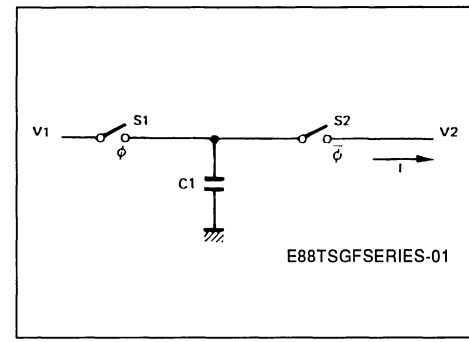
For example higher than 12th order filters or circuit combining filters with digital and analog functions on the same chip are achievable with TSGSM Standard Cells.

SWITCHED CAPACITOR TECHNIQUE

SGS-THOMSON TSGF products are active filters where resistors are replaced by capacitors which are switched at a frequency, named sampling frequency (F_i).

Figure 1 is showing the basic principle of switched capacitor technique.

Figure 1.



The 2 switches (S1 and S2) are controlled by 2 complementary and non overlapping clock phases.

During the phase $\varnothing = 1$ (S1 on, S2 off) the charge stored in C1 is :

$Q1 = C1.V1$ (1)

During the phase $\overline{\varnothing} = 1$ (S1 off, S2 on) the charge stored in C1 becomes :

$Q2 = C1.V2$ (2)

During a complete clock period $Ti = \frac{1}{Fi} = \varnothing + \overline{\varnothing}$

the transferred charge is :

$\Delta Q = Q1 - Q2 = C1\ (V1 - V2)$ (3)

During this Ti period, this charge flow is equivalent to a current, I :

$\Delta Q = C1\ (V1 - V2) = I.Ti$ (4)

$$I = C1.Fi\,(V1 - V2) = \frac{C1\,(V1 - V2)}{T_i} \quad (5)$$

Comparing (5) with Ohm's law applied to a resistance :

$$I = \frac{V1 - V2}{R} \quad (6)$$

The equivalent resistor is then :

$$Req = \frac{T_i}{C1} \quad (7)$$

Then, with (7), a RC product becomes :

$$Req.\,C = \frac{C}{C1}\,T_i \quad (8)$$

product but the component values R and C used with the Op-amp are absolutely uncorrelated : so trimmings, tunings are very often needed to obtain an accurate template. On the other hand, with switched capacitor networks, only capacitor ratios are used. These ratios are obtained with capacitors integrated on the same chip. The available accuracy is 0.1% to 0.5% whatever the temperature condition may be.

As the time constant is fixed by capacitor ratio, fully integrated filters are achievable without trimming. In addition, as shown in (8) the time constant RC is proportional to the sampling period Ti : the filter cut-off frequency can be shifted by tuning the sampling clock frequency without any change on the shape of response curves.

SWITCHED CAPACITOR FILTER BENEFITS

In active filters, the time constant is fixed by the RC

SWITCHED CAPACITOR FILTER FEATURES

Key Points	Results
• Monolithic Filter. • The coefficients of the filter transfer function are completely determined by : – a single crystal controlled clock frequency – and ratioed capacitors • Fully HCMOS Integrated Filters • Switched capacitor filters are sampled-and-hold circuits.	• Board Size Reduction. • High Accuracy Template. • Stability in Temperature and Time. • High Order Filter Achievable. • No Adjustment. • Clock Tunable Cutoff Frequency. • Low Power. • No External Components. • Ease and Safety of Use. • Antialiasing prefiltering is required if the input signal is wide band. • Smoothing post filtering may be used to avoid spectral rays around the sampling frequency.

SWITCHED CAPACITOR FILTER ARRAY ARCHITECTURE

Analog switched capacitor filter arrays, TSGF series, are processed with a 3.5/2 polysilicon layer/1 metal layer HCMOS process.

SGS-THOMSON offers 3 filter base arrays, TSGF04, TSGF08 and TSGF12, providing filtering capabilities from 2nd to 12th order.

The 3 arrays are designed around a "Universal biquadratic filter cell", SGS-THOMSON patented. This cell consists of 2 adder integrators using a transconductance amplifier, switches, and capacitor fields. Fields of capacitors are composed of hundred unit capacitors (0.1pF) and then provide high and accurate capacitor values.

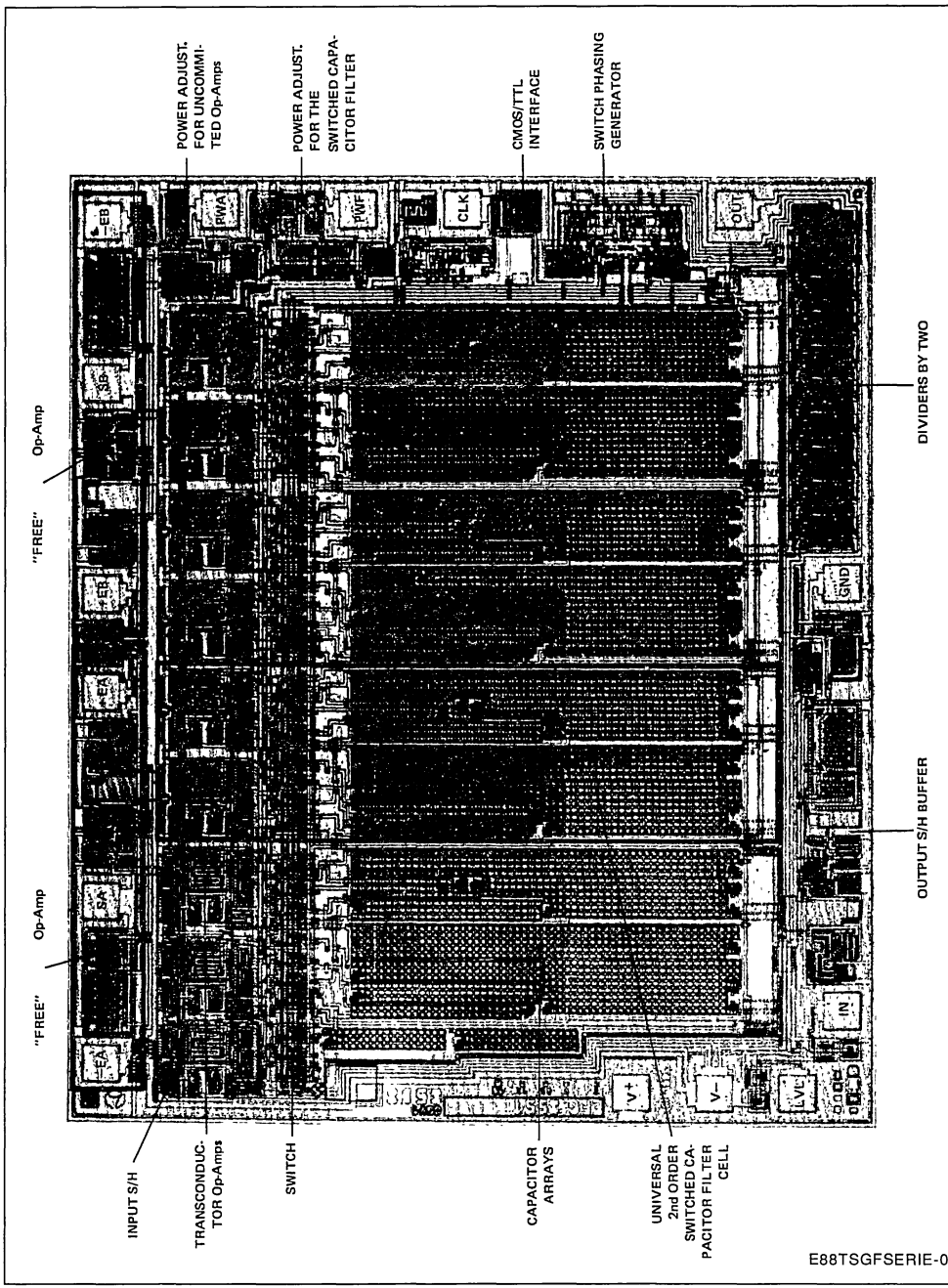
Figure 2 shows the TSGF08 chips, outlining all functions available on TSGF filter arrays :

- Universal 2nd order Filter Cell. Clock divider generating internal sampling frequency from external clock.
- Non overlapping phase generator.
- Input Sample-and-Hold.
- Uncommitted free Op-amps. Power consumption Adjustment cells for filter and Op-amps.
- Output Sample-and-Hold.

The internal sampling frequency Fi can be set from 500Hz to 700KHz by an external oscillator (or an internal one with TSGF04 base wafer).

When the external available clock frequency is

Figure 2 : TSGF08 CHIP.



higher than 700KHz, the set of Mask Programmable dividers by 2 is used to adapt the external clock frequency to the sampling frequency. In any case the external clock frequency must be lower than 5MHz.

As the ratio Fi/Fc between sampling frequency Fi and selected filter frequency Fc is a constant, designers can move the filter characteristics (central or cut-off frequency) only by tuning the clock.

A 10V power supply, either 0V and 10V, or - 5V and + 5V, gives the best performances : maximum output swing of 8V. The TSGF filters can also operate with a standard 0/5V power supply. In that case the maximum output swing is 2.2V.

Typical power consumption is 0.5mA per filter order. This power consumption is user adjustable between 0.1mA and 2mA with an external resistor, depending on the frequency range.

The power consumption adjustment is also provided to the uncommitted operational amplifiers : the bias current must be increased when a high gain - bandwidth product is required.

These uncommitted Op-amps give the designer the capability to create auxiliary circuits like voltage gain, prefiltering and post filtering functions half or full wave rectifier functions, or local oscillator (refer to application notes AN-061, AN-069, AN-070, AN-075).

The offset voltage of TSGF products is typically a few millivolts, with a 300mV max depending of the filter type.

Moreover, there is a possibility to adjust the filter output DC levels, thanks to an external bias voltage applied on "LVL" pin. Automatic offset compensation can be done by mean of one uncommitted on-chip operational amplifier, as indicated in Application note AN-069.

The TSGF products feature a high input impedance (typ. : 3MΩ) and a low output impedance (typ. : 10Ω) allowing then cascadable filter network in order to achieve higher than 12th order.

The output buffers are configurated as sample-and-hold amplifiers which can drive a 1KΩ load resistance and a 100pF load capacitance.

On the TSGF04 and TSGF12 an external sample-and-hold clocking allows to connect the filter output directly to an analog to digital converter (Optional ; see fig. 7).

In addition some particular switched capacitor cells have been implemented on the first 2 integrators of each chip allowing realization of special functions like :

- cosine filter
- complementary high pass filter
- exact bilinear leapfrog filter.

Figure 3a : TSG8512 : 7th Order Cauer Low pass Filter.

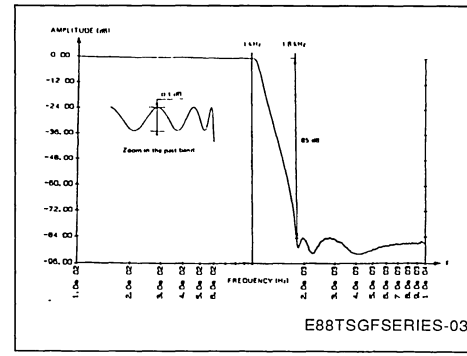
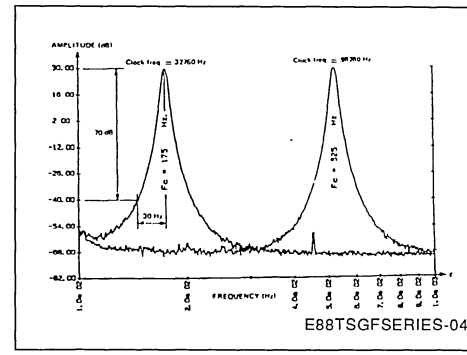


Figure 3b : TSG8551 : 8th Order High-Q Band pass Filter (Q = 35).



BENEFITS

With the TSGF series of SGS-THOMSON, designers are given unique "Gate Array" filter products for the replacement of their passive/active filters or the design of new filters.

The TSGF04/08/12 provide then with gate Array technique 3 complete arrays where all functions necessary to realize the filter function and its external circuit environment are available on chips.

The switched capacitor process permits the realization of very accurate and fully integrated filters and breaks down the equipment production costs by providing fully tested filters parts : tuning or adjustment of external components are no more ne-

cessary with TSGF series.

Figures 3A, 3B is showing 2 examples of Standard Filters designed with the TSGF08 matrix.

APPLICATIONS

TSGF products from SGS-THOMSON can integrate all filtering functions (replacement of active or passive filters...) and then can be implemented very quickly into an application/equipment requiring a filter with a maximum input signal frequency of 30KHz.

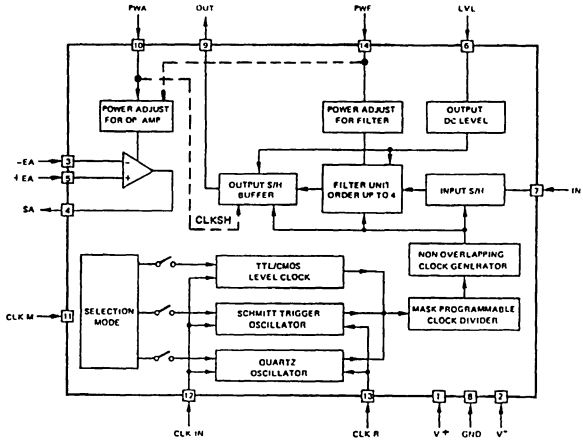
Mask Programmable Filters (MPFs) typical applications are :
- audio filtering/processing
- signal/frequency detection
- scrambling/coding
- spectrum analysis
- process control
- remote control
- harmonic analysis
- equalization
- frequency tracking
- alarm systems
- robotics
- anti-knock system
- data acquisition (before A/D and after D/A converters)
- automatic answering
- inwarding
- speech processing
- security system (coding, recognition)
- sonar detection
- mobile radio
- modems

BLOCK DIAGRAMS

Figure 4 outlines the mean features and options offered by each of the 3 MPF arrays by showing TSGF04, TSGF08 and TSGF12 block diagrams.

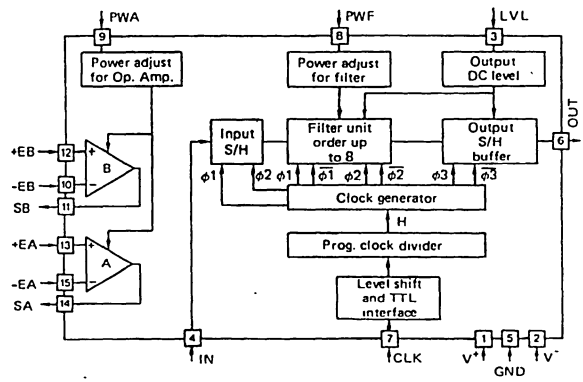
Figure 4 : Block Diagrams.

TSGF04



E88TSGF SERIES-05

TSGF08



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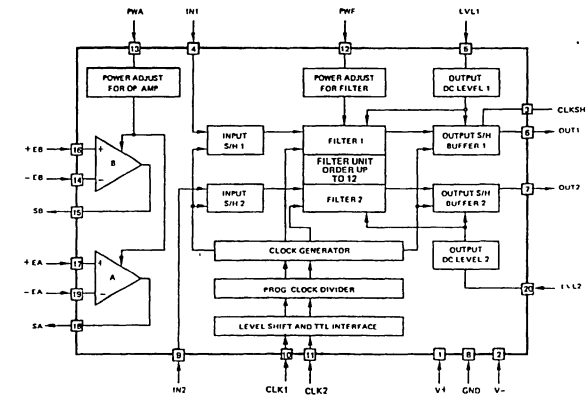
TSGF12



E88TSGF SERIES-07

PIN DESCRIPTION

The table below gives the pin description of the 3 MPF arrays, TSGF04 TSGF08 and TSGF12. The pin assignment is given for the extended and complete version of each array, it means with all the available on-chip options connected to the package.

Name	Pin Type	TSGF04 N°	TSGF08 N°	TSGF12 N°	Function	Description
V^+	I	1	1	1	Positive Supply	
V^-	I	2	2	2	Negative Supply	
LVL	I	6	3	LVL1 5 LVL2 20	Output DC Level Adjustment	Filter output DC level adjustment when connecting a potentiometer between V^+ and V^- with its middle point to LVL. When no adjustment is needed, LVL pin is connected to GND.
IN	I	7	4	IN1 4 IN2 9	Filter Input	
GND	I	8	5	8	General Ground	GND Voltage = $\frac{V^+ + V^-}{2}$
OUT	O	9	6	OUT1 6 OUT2 7	Filter Output	
CLK	I	See CLKIN	7	CLK1 10 CLK2 11	Clock Input	TTL/CMOS Level Compatibility
PWF	I	14	8	12	Filter Power Adjustment	Filter power consumption can be chosen by connecting a resistor between PWF and GND (or V^+). Stand by mode is obtained by connecting PWF to V^- (or non connected)
PWA	I	10*	9	13	Op Amp Power Adjustment	Idem PWF but for Op Amp (PWA)
–EB	I		10	14	Inverting Input Op Amp B	
SB	O		11	15	Output Op Amp B	
+EB	I		12	16	Non Inverting Input Op Amp B	
+EA	I	5	13	17	Non Iverting Input Op Amp A	
SA	O	4	14	18	Output Op Amp A	
–EA	I	3	15	19	Inverting Input Op Amp A	
NC			16		Non Connected	
CLKSH	I	10*		3	S/H Clock Input	External Driving Clock of Output Sample-and-hold
CLKIN	I	12			Clock Input	See TSGF04 Clock Oscillator Section
CLKR	O	13			Clock Pin for External Oscillator	For TSGF04, external RC or crystal oscillator are connected to CLKIN and CLKR pins. See TSGF04 clock oscillator section
CLKM	I	11			Clock Selection Mode	Connected to GND or V^- see TSGF04 clock oscillator section

* For TSGF04 when external driving clock of output sample-and-hold (CLKSH) is used, PWF realizes the power adjustment of both uncommitted Op-amp and filter.

Note : For other packing pin-out, refer to package drawings and pin-out at the end of data sheet.

FUNCTIONAL DESCRIPTION

INTERNAL CLOCK DIVIDER (CLK)

The internal sampling frequency F_i can be fixed from 500Hz to 700KHz (F_i can be used between 700KHz and 1MHz with some limitations) by an external oscillator (or internal one with TSGF04 filter array). When the external clock frequency F_e, is higher than 700KHz, a mask programmable on-chip divider is used to adapt available clock frequency to the sampling rate.

	TSGF04	TSGF08	TSGF12
Number of Divide by 2 Available Per Chip	8	10	8
Max. F_e/Fi Ratio	256	1024	256

In any case, the external clock frequency F_e must be less than 5MHz.

Example : The TSG8510 features (TSG8510 is a standard filter based on TSGF08 array) :

F_e max = 1.5MHz and F_i max = 750KHz then

$$\frac{F_e}{F_i} = 2$$

only one divider by 2 is used for this filter (which is the case of most of SGS-THOMSON' general purpose filters).

Note : As the internal clock divider is mask programmable, the ratio F_e/F_i is fixed for each filter. The change of this ratio is possible but results into a new part number.

ADJUSTMENT OF OUTPUT DC LEVEL (LVL)

The output DC offset voltage can be removed thanks to an external bias voltage applied on "LVL" pin, as shown on figure 8.

However automatic offset compensation can be implemented by using one of the uncommitted on-chip Op-amps, as indicated in application note AN-069 (see fig. 9 in AN-069).

The offset voltage of TSGF filters is typically a few millivolts, with a 300mV max, depending on the type of the filter.

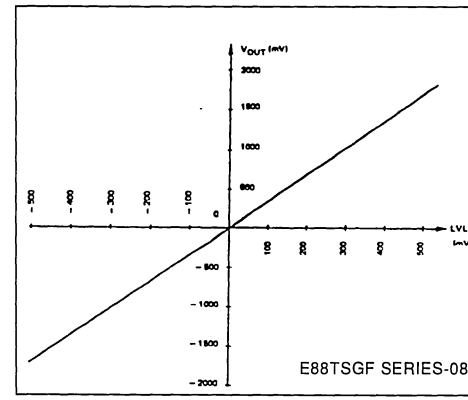
A drift of this offset voltage can be observed when user increases the power consumption of the filter with an external resistor connected to PWF pin. So when the filter operates at high frequencies, a compromise exists between the filter frequency response performance and its output DC offset voltage.

When no DC output level adjustment is required, LVL pin has to be connected to the GND voltage.

The level gain, LG, of each filter can be deduced from the curve representing V_{OUT} = f (LVL). This curve is filter dependent.

For example the TSG8510 presents following curve shown in figure 5 (measured with F_e = 256KHz, I_{PWF} = 100µA) :

Figure 5 : Output DC Voltage Adjustment from LVL Pin.



The TSG8510's level gain is :

$$LG = \frac{V_{OUT}}{LVL} \cong \frac{1000}{300} 3.3$$

For example if one TSG8510 presents a 100mV offset voltage at its output, user must apply an external bias voltage LVL = 30mV to compensate it.

FILTER POWER ADJUSTMENT (PWF)

The filter power consumption can be chosen by connecting an external resistor, R_{PWF} between PWF and GND (or V+) pins.

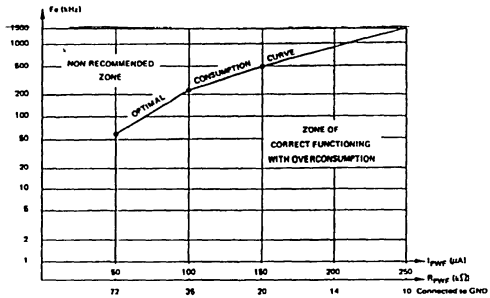
This power adjustment operates the variation of the bias current of the integrators used in the switched capacitor filter. This current, I_{PWF}, can be low when filter operates at low cut-off frequencies ($F_c \cong 1$KHz), but must be increased at high cut-off frequencies ($F_c \cong 20$KHz), in order to charge and discharge the capacitors at a higher rate.

As a result, an optimal choice of I_{PWF} bias current can be deduced from the curve representing I_{PWF} = f (F_e), F_e being the external clock frequency applied on CLK pin.

This curve is dependent on the filter. For example, as shown in figure 6, the TSG8510 presents following characteristics :

Example : if the cutoff frequency of the low pass TSG8510 filter has to be set at 3.4KHz, user must apply the external clock frequency F_e = 75.3 x 3.4 = 256KHz.

Figure 6 : TSGF10 user's Guide for IPWFand RPWF Choise.



E88TSGFSERIES-09

The User's guide for I_{PWF} choice indicates :

- optimal I_{PWF} = 100µA
  R_{PWF} = 35kΩ
- non recommanded zone for I_{PWF} 100µA
  Operation within this area can lead to increase the ripple in the pass band and to decrease the stop band attenuation.
- zone of correct functioning with over consumption for I_{PWF} > 100µA.

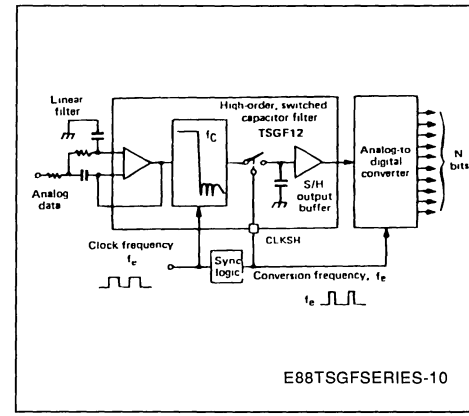
Note : Power consumption choice has to be prioritized when major concern in TSGF design is the frequency response (gain versus frequency). The output DC offset voltage comes in 2nd position in that case.

EXTERNAL DRIVING OF OUTPUT SAMPLE-AND-HOLD

This facility allows the filter output to be connected directly to an analog-to-digital converter, as illustrated in figure 7.

The clock signal which enters on the CLKSH pin must be synchronous with the sampling frequency. As a result, the external clock frequency F_e must be the sampling frequency F_i (the on-chip divider does not have to be used).

Figure 7 : External Driving of Output Sample and Hold (example).



E88TSGFSERIES-10

The clock signal applied on CLKSH pin has to be optimized in order to read a settled signal issued from the switched capacitor filter.

On the example shown in figure 7, a 12th order low pass filter makes an ideal antialiasing filter to precede data conversion. The filter precludes the need for oversampling when driving the A/D converter.

CLKSH option is only available on TSGF04 and TSGF12 arrays.

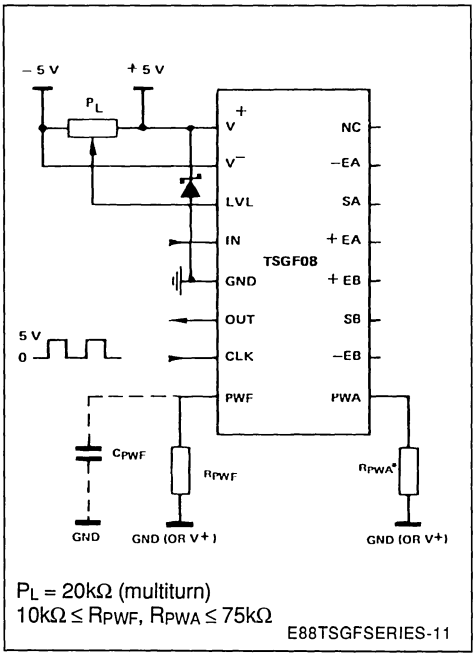
USE OF THE MPF WITH - 5V/+5V DUAL POWER SUPPLY

The adjustment of the DC output level of the M.P.F. is achieved by an external voltage source (for example, a bridge divider connected between the positive and the negative power supplies and whose the middle point is connected to the LVL pin of the M.P.F.). If no output DC adjustment is required, the LVL pin can be directly connected to GND.

The consumption of the filter can be also adjusted by means of an external resistance connected between GND (or V^+) and the PWF pin of the circuit.

The consumption can thus be chosen to match the particular application.

Figure 8 : Example of a TSGF08 Fed in Dual Supply : +5V, 0, -5V.



If the Op-Amps are not used, RPWA has not to be connected between PWA and GND.

The stand-by mode is obtained by strapping the PWF pin to V⁻ (or non connected).

The adjustment of the power consumption of the two operational amplifiers can be achieved exactly like for the previous case, but via the PWA pin of the circuit. The stand-by mode is also obtained by strapping the PWA pin to V⁻ (or non connected).

The clock levels are TTL, but CMOS levels are accepted. With these previous conditions, the output linear dynamic range of the M.P.F. is about 8V, between - 4.5V and + 3.5V.

A capacitor C_{PWF} can be added in parallel with R_{PWF} in order to improve the clock feedthrough rejection : (Typical value C_{PWF} = 33pF).

As for all CMOS circuits operating with dual power supply (- 5V, 0, + 5V), it is advised to use clamping diodes (Threshold voltage less than 0.6V) (Schottky is preferrable) in order to avoid transients during power up which could drive TSGF circuits over their maximum ratings. Only 1 Schottky diode between GND and V+ is sufficient for TSGF products.

USE OF THE MPF WITH 0/10V SINGLE POWER SUPPLY

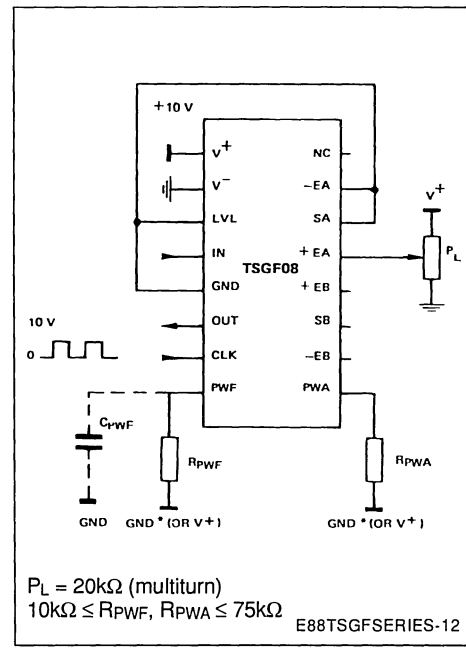
In this case, V⁻ is the reference ground of the circuit and GND must be adjusted to + 5V by means of the potentiometer P_L (V+ - V⁻)/2), or by using a simple bridge divider. But in that case small resistors values (2kΩ) have to be used in order to set GND at a low impedance value.

The adjustments of the DC output level of the M.P.F. of the power consumptions of the filter and of the operational amplifiers can be achieved exactly like previously.

The high level of the clock must be at least 1.4V upper the GND level.

With these previous conditions, the output linear dynamic range of the M.P.F. is about 8V between 0.5 and 8.5V.

Figure 9 : Example of a TSGF08 FED, in Single Power Supply 0 - 10V.



* GND is used, when the user provides the 5V voltage.

USE OF THE MPF WITH 0/5V SINGLE POWER SUPPLY

In this case, V⁻ is the reference ground of the circuit

and GND must be adjusted to + 2.5V by means of the potentiometer P_L ((V+ - V⁻)/2), and one Op-amp used as buffer in order to provide a low impedance on GND reference.

Otherwise, without Op-amp, a simple bridge divider is sufficient, but small resistor values (2kΩ) have to be used in order to set GND at a low impedance value.

The other adjustments are achieved exactly like previously except for bias resistance of the filter and of the operational amplifiers (R_{PWF} and R_{PWA}), whose must be exclusively to V+.

The clock levels must be CMOS levels. With these previous conditions, the output linear dynamic range of the M.P.F. is about 2.2V, between 1.2 and 3.4V.

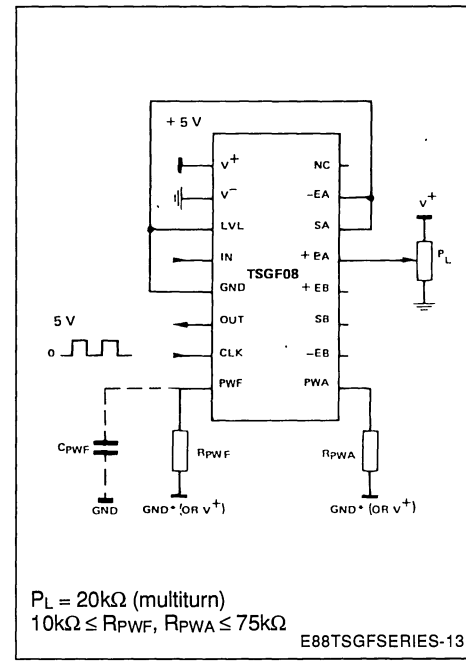
ANTI-ALIASING AND SMOOTHING

Anti-aliasing : The switched capacitor filters are sampled systems and must verify the SHANNON condition imposing a sampling frequency (F_i) equal, at least, to the double of the upper frequency (F_c) contained in the spectrum to transmit. With this condition, no information is added or lost on the transmitted signal. This theorem describes the well-known phenomenon called spectrum aliasing shown figure 11 where the entire spectrum to transmit appears around F_i, 2 F_i, 3 F_i... and so on.

Thus, all spectrum components of the signal contained around these frequencies are transmitted by the M.P.F., oppositively to the desired result.

To cancel the effects of this phenomenon, it is required, before all sampled systems, to filter all the spectrum components of the intput signal upper than F_i - F_c. An analog filter, called "anti-aliasing filter", must be therefore applied before the M.P.F.

Figure 10 : Example of a TSGF08 FED in Single Power Supply 0-5V.

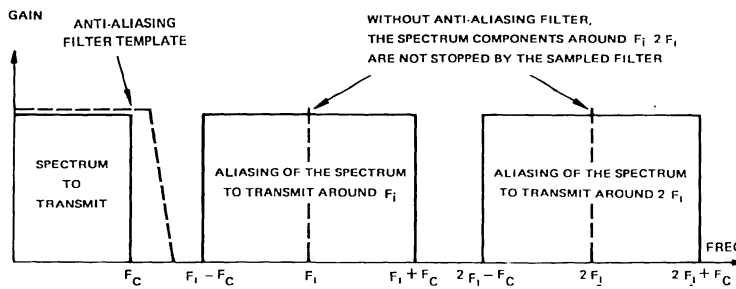


P_L = 20kΩ (multiturn)
10kΩ ≤ R_{PWF}, R_{PWA} ≤ 75kΩ

E88TSGFSERIES-13

*GND is used, when the user provides the 2.5V Voltage.

Figure 11.



Phenomenon of the spectrunm aliasing

E88TSGFSERIES-14

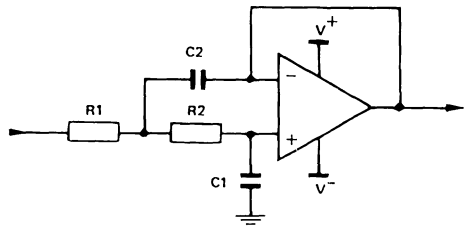
- Without anti-aliasing filter : Spectrum to transmit ≠ transmitted spectrum
- With anti-aliasing filter : Spectrum to transmit = transmitted spectrum

The selectivity of this filter depends upon the F_i/F_c ratio.

If F_i/F_c 200, a RC filter (first order low-pass) is sufficient.

If F_i/F_c 200, a SALLEN-KEY structure (second order low-pass) must be used. This structure and its relationships are described (figure 12). In these relationships, F_c is the cut-off frequency desired of the anti-aliasing filter and ξ its damping coefficient. For a cut-off as tight as possible and in order to correct the sin x/x effect, ξ must have a value around 0.7.

Figure 12.



E88TSGFSERIES-15

R1 = R2 = arbitrary value
F_c = cut-off frequency for the antialiasing filter.
An optimal choice is Fc = 2 x cut-off frequency of the main filter
ξ = damping coefficient ; the optimal value is 0.7

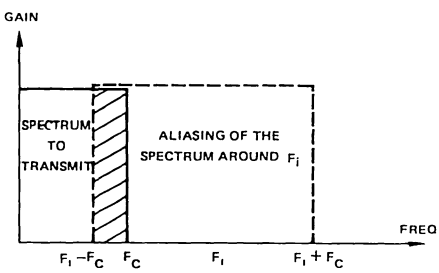
$$C1 = \frac{\xi}{2\pi R1 Fc}$$

$$(C1 = \xi 2 - C2)$$

$$C2 = \frac{1}{2\pi \xi R1 Fc}$$

SALLEN-KEY structure (second order low-pass Filter) for anti-aliasing and smoothing.
Note : If F_i/F_c 2 (figure 13), the spectrum to transmit and the spectrum aliased have a part in common and it becomes impossible to share the useful signals from the undesirable signals.

Figure 13.



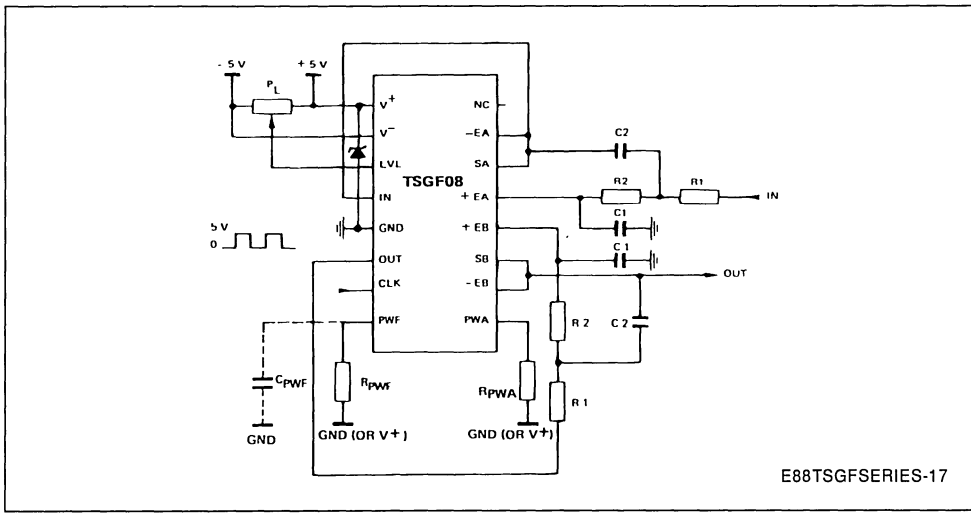
E88TSGFSERIES-16

When Fi/Fc<2, the spectrum component included between Fi-Fc and Fc and which are due to spectrum aliasing are not stopped by the sampled filter.

- Smoothing : As the signal obtained at the output of the M.P.F. is a sampled and hold signal, it is often required to smooth it. This smoothing filter can be achieved from the SALLEN-KEY structure previously described (figure 12).
- Hardware implementation : In order to make easier anti-aliasing and smoothing. SGS-THOMSON has designed, on the TSGF chip one or, two general purpose operational amplifiers. A few external components are therefore sufficient to achieve these functions (figure 14).

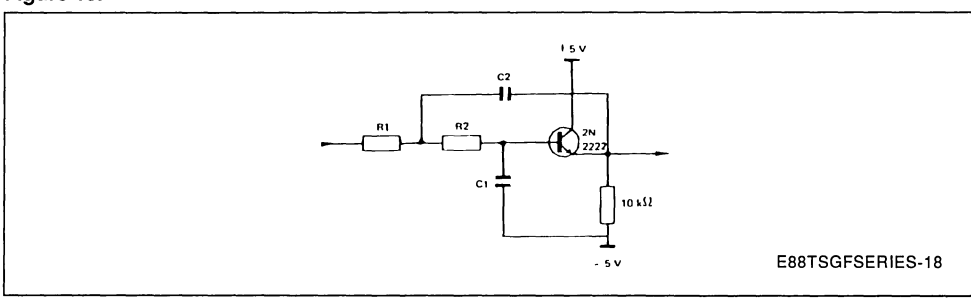
On the other hand, in the most of M.P.F.'s, a special integrated cell is included in the chip (cosine filter) to reduce the aliasing effects around F_i.

Figure 14.



M.P.F. With anti-aliasing and smoothing filters
P_L = 20kΩ (multiturn)
10kΩ ≤ R_{PWF}, R_{PWA} ≤ 75kΩ
R1,R2,C1,C2 } See anti-aliasing
R'1, R'2,C'1,C'2 } and smoothing considerations

Figure 15.



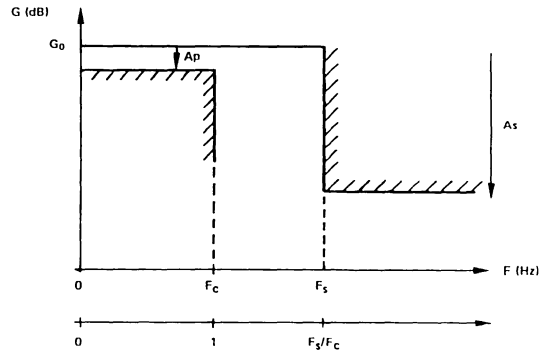
Second order low-pass Filter (SALLEN-KEY STRUCTURE) with a transistor replacing the operational amplifier.

Nonetheless, if the application allows it, these two operational amplifiers can be used to implement other functions (gain, comparator, oscillator...).

In this case, the circuit shown figure 15 can be used as anti-aliasing or smoothing filter. This structure is the same as the SALLEN-KEY structure described figure 12 (second order low-pass), in the same way as the corresponding relationships.

CUT-OFF FREQUENCY DEFINITION

Figure 16 : Design Specifications.

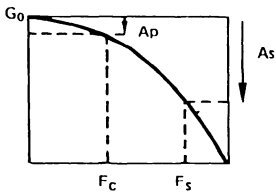


E88TSGFSERIES-19

The cut-off frequency F_c is the passband limit frequency as defined on the design specifications above mentioned. The maximum value of the attenuation variation in the passband : Ap is 3dB for Butterworth, Bessel and Legendre filters (figure 17a), and is called passband ripple for Chebychev (figure 17b) and Cauer filters (figure 17c).

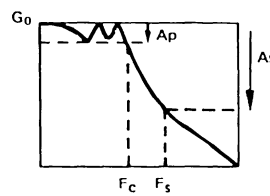
The passband ripple is design dependent and between 0.05dB and 0.2dB with TSGF standard filters. The parameters G_o called passband gain is the maximum value of the gain in the passband, and may have low variation from part to part.

Figure 17a.



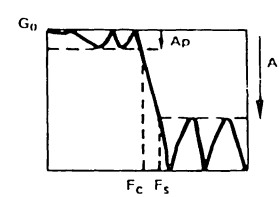
E88TSGFSERIES-20

Figure 17b.



E88TSGFSERIES-21

Figure 17c.



E88TSGFSERIES-22

ELECTRICAL SPECIFICATION

The following electrical characteristics are common to the 3 base filter arrays TSGF04, TSGF08 and TSGF12, because their structures are designed with the same basic components.

ABSOLUTE MAXIMUM RATINGS

T_{amb} = 25°C, V+ = 5V, GND = 0V, V– = – 5V, I_{PWF} = 100µA (unless otherwise specified)

Symbol	Parameter	Value	Unit
V+	Positive Supply Voltage	– 0.15 to + 7	V
V–	Negative Supply Voltage	– 7 to + 0.15	V
V	Voltage to any Pin (except for GND)	(V–) – 0.3 to (V+) + 0.3	V
T_{oper}	Operating Temperature Range	T_{min} – 5°C to T_{max} + 5°C	°C
T_{stg}	Storage Temperature Range	– 60 to + 150	°C

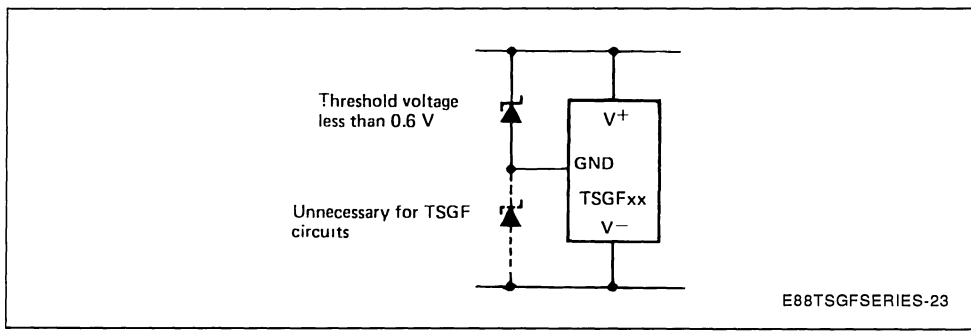
WARNING : DUAL POWER SUPPLY (- 5V, 0, + 5V)

Although TSGF circuits are internally gate protected to minimize the possibility of static damage, MOS handling and operating procedure precautions should be observed. Maximum rated supply voltages must not be exceeded. Use decoupling networks to remove power supply turn on/off transients, ripple and switching transients.

Do not apply independently powered signals or clocks to the chip with power off as this will forward bias the substrate. Damage may result if external protection precautions are not taken :

As for all CMOS circuits operating with three supply voltages (V+, GND, V-), it is advised to use clamping diodes (Schottky is preferable), in order to avoid transient during power up that would drive the circuit over its maximum ratings (see figure 18).

Figure 18 : Application Hint for CMOS ICs with Three Supply Voltages.



ELECTRICAL OPERATING CHARACTERISTICS

$V^+ = 5V$, GND = 0V, $V^- = -5V$, $T_{amb} = 25°C$, $I_{PWF} = 100\mu A$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V^+	Positive Supply Voltage	4	5	6	V
V^-	Negative Supply Voltage	−6	−5	−4	V
V_{OUT}	Output Voltage Swing (*)	$(V^-) + 0.5$		$(V^+) - 1.5$	V_{PP}
V_{IN}	Input Voltage (*) (with filter gain = 0dB)	$(V^-) + 0.5$		$(V^+) - 1.5$	V_{PP}
I_{PWF}	Bias Current on PWF (stand-by mode by connecting PWF to V^-)	50		250	µA
V_{IL}	TTL Clock Input "0" (**)			+ 0.8	V
V_{IH}	TTL Clock Input "1" (**)	2			V
T_{CP}	Ext. Clock Pulse Width	80			ns
R_{IN}	Input Resistance	1	3		MΩ
C_{IN}	Input Capacitance			20	pF
R_{OUT}	Output Resistance		10		Ω
C_L	Load Capacitance			100	pF
R_L	Load Resistance	0.1	1		kΩ

Note : with supply (0, + 10V) : same specifications
with single supply (0, + 5V) : contact SGS-THOMSON sales office or representative.
(*) Depending on I_{PWF} current
(**) TTL levels are referenced to GND voltage

Other filter's characteristics, such as noise, power supply rejection ratio, total harmonic distortion... are filter dependent. As a result, for such characteristics, SGS-THOMSON can only guarantee the lower level of performance for each parameter, as indicated below. (this lower level has been determined from measurements on a set of hundred different TSGF filters, as shown in figure 19).

PSRR + > 2dB : V+ Power supply rejection ratio.

PSRR − > 10dB : V^- Power supply rejection ratio.

$V_n < 1mVrms$: V_n is the total output noise voltage measured in the passband of the filter.

SNR > 57dBm/600 Ohm : Signal to noise ratio with $V_{IN} = 775mVrms$.

SNR > 65dBV : signal to noise ratio with $V_{IN} = 2Vrms$.

THD < 0.1% : Total harmonic distortion.

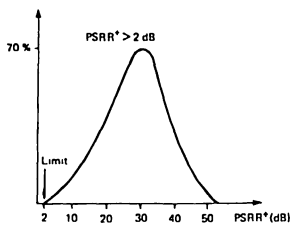
As such characteristics are not predictable from simulation results, their typical values are provided from measurements of the customized filter prototypes. (These measurements could be performed by SGS-THOMSON on special request).

These typical values, obtained with TSGF products, are better than the lowest level guaranteed, and designers can get a more accurate idea about them by two means.

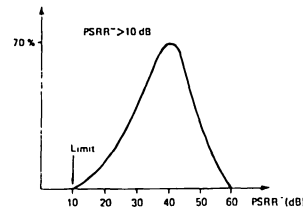
1) Such characteristics are given for general-purpose filters. Refer to TSG85xx, 86xx, 87xx data sheets.

2) Figure 19 gives histograms of the 5 parameters discussed above. These histograms indicate the distribution of the typical value of the considered parameter over a set of hundred different TSGF filters. (Note that the aim of these histograms indicate the dispersion of the considered characteristic for a given TSGF filter).

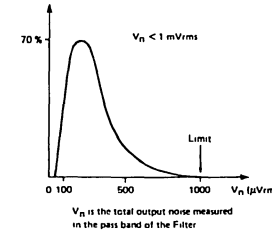
Figure 19 : Distribution of Typical Value Over a set of Hundred Different TSGF Filters.



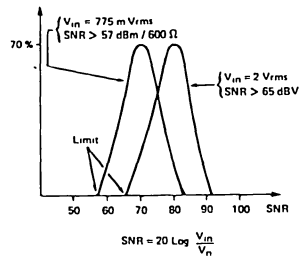
E88TSGFSERIES-24



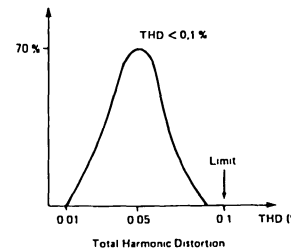
E88TSGFSERIES-25



E88TSGFSERIES-26

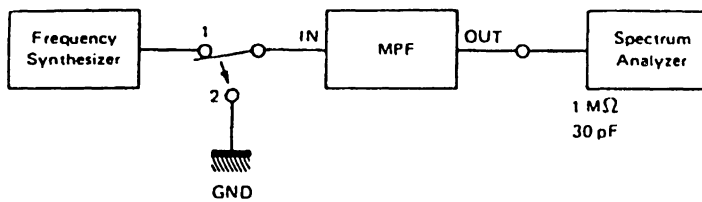


E88TSGFSERIES-27



E88TSGFSERIES-28

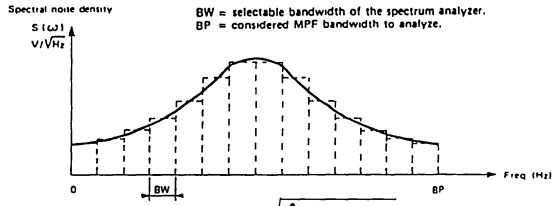
Figure 20 : Method of Noise Measurement.



Position 1 : Calibration of the spectrum analyzer to 0dBV (1Vrms).
Position 2 : Measurement with filter input connected to GND.

E88TSGFSERIES-29

Figure 20 : (continued).



We obtain theoretical noise voltage : $Vn(Vrms) = \sqrt{\int_0^{BP} S^2(\omega).d\omega}$

and measured noise voltage : $Vn(Vrms) = \sqrt{\sum_{k=1}^{BP/BW} S^2(k) \cdot BW}$

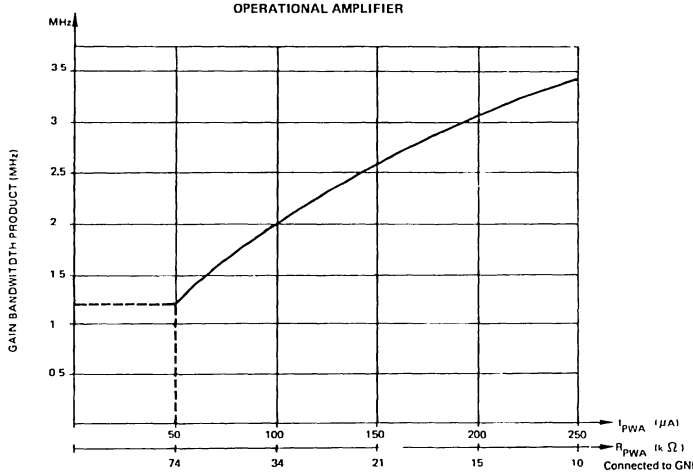
E88TSGFSERIES-30

UNCOMMITTED ON-CHIP OPERATIONAL AMPLIFIERS

$V^+ = 5V$, $GND = 0V$, $V^- = -5V$, $T_{amb} = 25°C$, $RL = 2k\Omega$, $I_{PWA} = 100\mu A$ (unless otherwise specified)

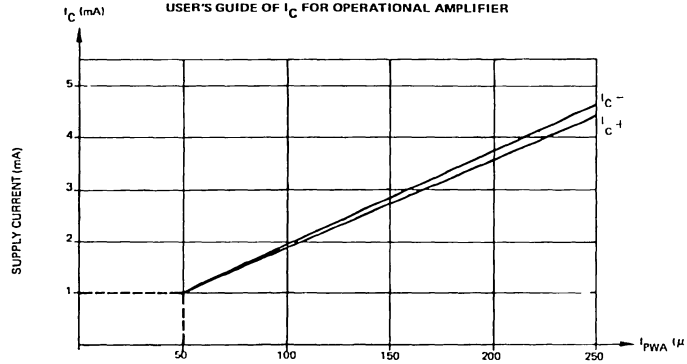
Symbol	Parameter	Min.	Typ.	Max.	Unit
G_0^+ G_0^-	DC Open Loop Gain (without load)	60 60	75 75		dB dB
G_{BP}	Gain Bandwidth Product (without load)	1	2		MHz
V_{IO}	Input Offset Voltage (without load)		± 5	± 10	mV
$V_{OP}P$	Output Swing		− 4.5 3.5	− 4.7 3.7	V V
I_{IB}	Input Bias Current (without load)		± 5	± 10	nA
SVR	Supply Rejection (without load)	60	65		dB
CMR	Common Mode Rejection V_{CM} = 1V (without load)	60	65		dB
R_O	Output Resistance		10		Ω
Ia^+ Ia^-	Supply Current		2.6 2.6	3.2 3.2	mA mA
SR^+ SR^-	Slew Rate	2 2	5 6		V/µs V/µs

USER'S GUIDE OF I_{PWA} AND R_{PWA} FOR UNCOMMITTED ON-CHIP OPERATIONAL AMPLIFIER



E88TSGFSERIES-31

USER'S GUIDE OF I_C FOR OPERATIONAL AMPLIFIER



E88TSGFSERIES-32

CAD SOFTWARE : FILCAD

In order to take full advantage of its Mask Programmable filter TSGF approach for Semicustom applications, SGS-THOMSON has developed a comprehensive software package called FILCAD® to cover all the development steps, starting from the feasibility evaluation of the customer's specifications, up to the single-metal interconnection routing required for the MPF customization.

More specifically, the FILCAD system gives the de signer strong assistance during the following steps :

- Evaluation of MPF solutions well suited to specific filter circuit requirements,
- Filter synthesis, leading to a switched capacitor electrical schematic,
- MPF filter simulation (performed with MPF capacitor capabilities),
- Schematic capture and routing of the optional connections,
- Layout file generation, and final verification performed by accurate post-routing simulation.

All FILCAD modules run on VAX® under VMS operating System, and are linked toghether as shown in figure 21. All modules are fully described in the TSGF's User's manual (Vol. 5 of SGS-THOMSON ASIC User's Manuals).

The entry to FILCAD is the customer filter specification which can be provided to SGS-THOMSON in different forms :

- amplitude - phase - group delay templates
- poles and zeros
- biquadratic cell coefficients
- polynomial transfer functions

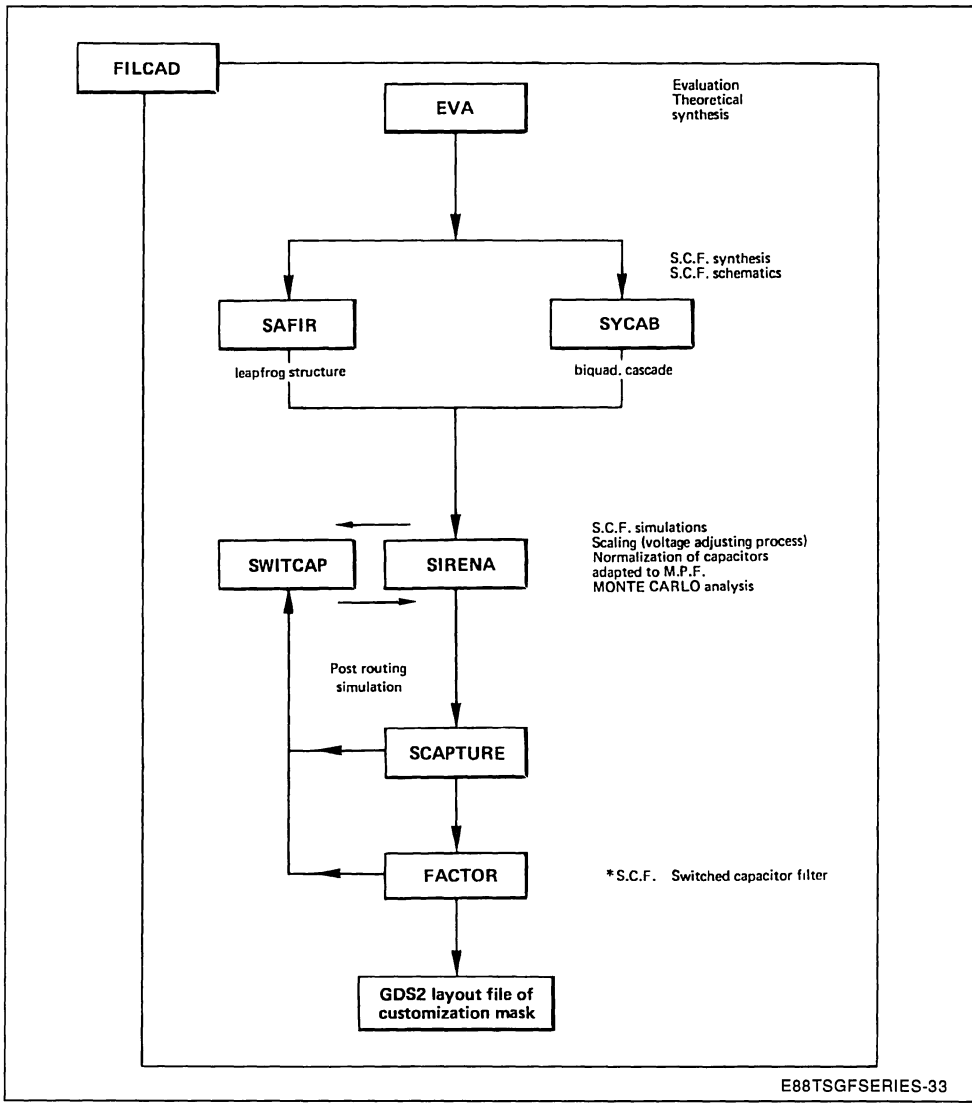
In addition SGS-THOMSON can perform feasibility study of customer specific filter circuits : in order for customers to get fast and accurate answer, SGS-THOMSON generated a feasibility analysis TSGF questionnaire that customers are kindly required to fill. This questionnaire is available on request at SGS-THOMSON Design centers or nearest sales office or representative.

MPF® and FILCAD ® are registered trademarks of SGS-THOMSON.

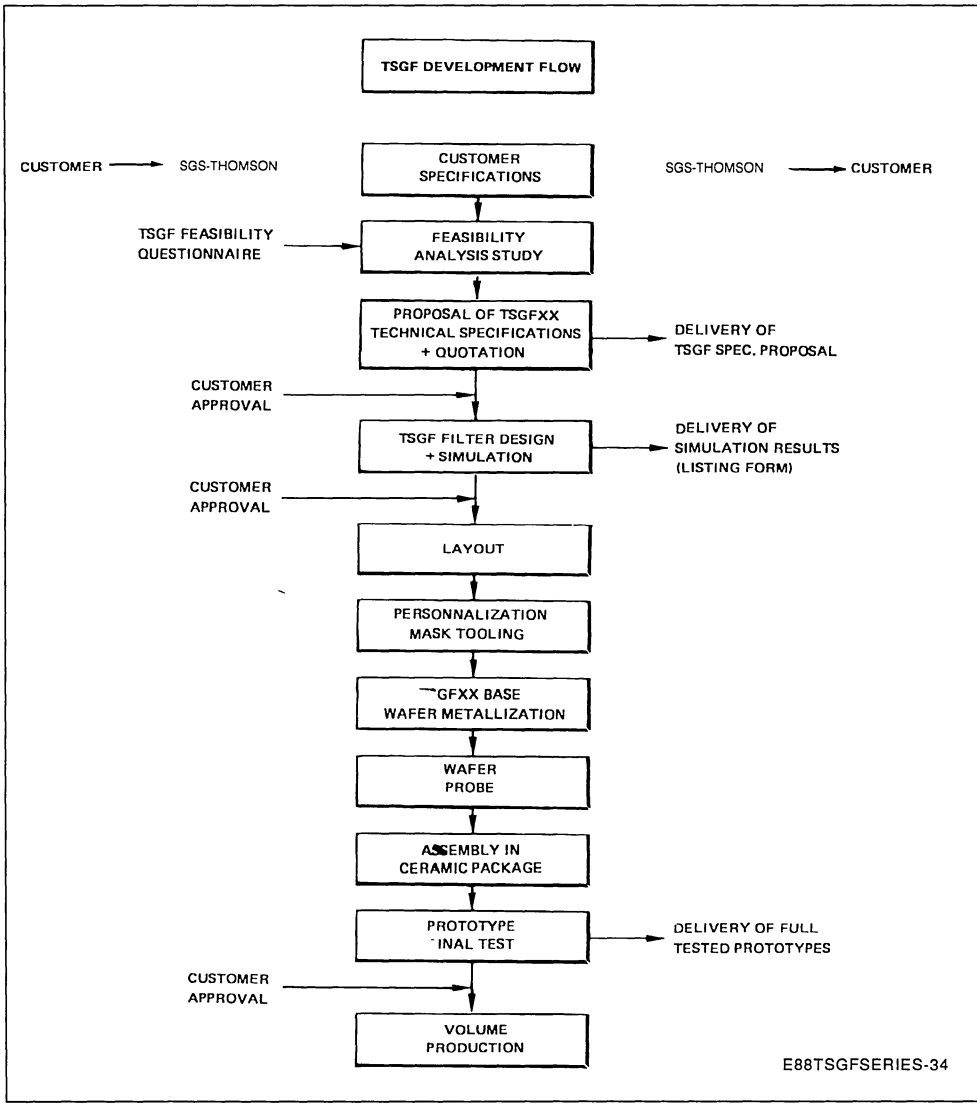
VAX® is a registered trademark of Digital Equipment Corp.

FILCAD, CAD software package developed by SGS-THOMSON for Switched Capacitor Filter designs, TSGF series, is also available for mixed analog-digital TSGSM Standard Cells or Full custom circuits integrating TSGF-like filtering functions.

Figure 21.



FILCAD is a trademark of SGS-Thomson
SWITCAP is a trademark of Columbia University



SGS-THOMSON proposes presently 2 design interfaces to customers for the design of their filter circuits with TSGF series :

- design entirely done by SGS-THOMSON within its Design Centers ;
- design done by customer up to simulation and then completed by SGS-THOMSON.

The table below outlines customer and SGS-THOMSON respective responsibilities for these 2 design interfaces.

DESIGN INTERFACES

Design Step	FILCAD Software	Int 2	Int 3
Theoretical Synthesis	EVA	SGS-THOMSON	Customer
Switched Capacitor Filters Schematics before Scaling	SYCAB or SAFIR	SGS-THOMSON	Customer
Final Schematics	SIRENA (SWITCAP)	SGS-THOMSON	Customer
Additional Simulation	SIRENA (SWITCAP)	SGS-THOMSON	Customer
Approval		Customer	SGS-THOMSON
Schematics Capture	SCAPTURE	SGS-THOMSON	SGS-THOMSON
Layout - Personnalization Mask Generation	FACTOR	SGS-THOMSON	SGS-THOMSON
Post Routing Simulation	SIRENA (SWITCAP)	SGS-THOMSON	SGS-THOMSON

DOCUMENTATION AND SUPPORT

In order to bring users the maximum support on switched capacitor TSGF filter arrays, SGS-THOMSON generated a complete set of documentation and tools which are available on request :

* TSGF User's Manual

* Application Notes
  - AN052 : How to choose a filter in a specific application
  - AN061 : implementation and applications around Standard MPFS
  - AN069 : A supplement to the utilization of switched capacitor filters.
    AN070 : Band Pass and Band Stop Filters.
  - AN075 : Signal detection and sinewave generation.

* MPF's evaluation boards.

* TSGF feasibility/analysis questionnaire.

In addition specialists can be contacted within SGS-THOMSON Microelectronics Filter Design Centers.

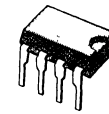
2nd TO 4th ORDER ANALOG FILTER ARRAY

With the TSGF04 array, whose block diagram is given below, user is given 2 different pin-out configurations :

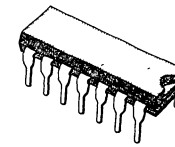
- 8 pin DIL only the filter up to 4th order is accessible.
- 14 pin DIL version where in addition, one uncommitted Op-amp and one internal oscillator capability are offered.

When the external driving of output sample-and-hold is used (CLKSH pin), PWF pin realizes the power adjustement of both uncommited Op-amp and filter unit.

TSGF04 are also available in SO wide package version (0.3 inch) : 16 pin version only.



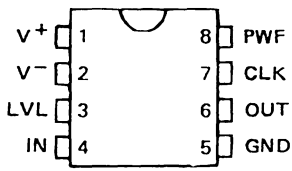
P
DIP-8
(Plastic Package)



P
DIP-14
(Plastic Package)

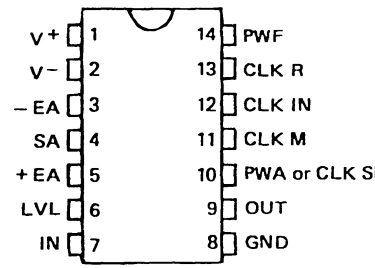
TSGF04
BLOCK DIAGRAM
See figure 4 (E88TSGFSERIES-05)

PIN CONNECTIONS



E88TSGF04-01

8 pins : FILTER ONLY
Compatible with TSGF08



E88TSGF04-02

14 pins : Filter
: + 1 Op - Amp

CLOCK OSCILLATOR

The TSGF04 base accepts external compatible TTL/CMOS clocks on CLKIN pin and provides an internal oscillator performed either by RC or crystal connected between CLKIN and CLKR pins.

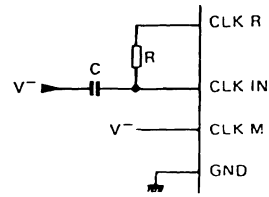
The clock selection mode is provided by CLKM pad which can be connected to V- or GND voltage levels. This connection is realized by two means, depending on the package type chosen :

- with 14-pin package, via CLKM pin.
- with 8-pin package, by internal connection readily performed, only on custom filters.

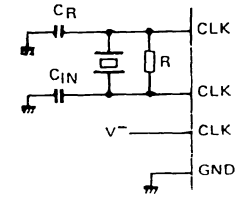
(Note that CLKM pin connected to V+, allows the selection of the internal crystal-controlled oscillator, but the selection by CLKM connected to V- is recommended).

The different possibilities are :

- two internal oscillator modes :
  - RC
  - Crystal

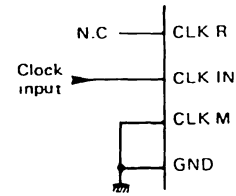


E88TSGF04-03



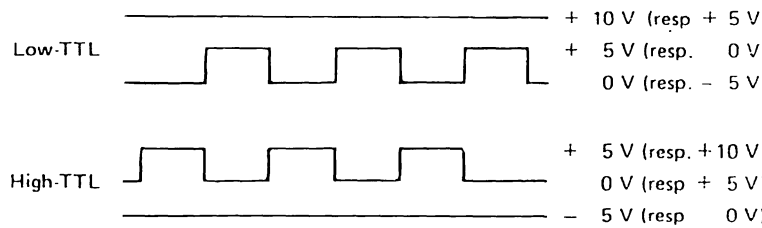
E88TSGF04-04

- three external clocks :
  - low-TTL
  - high-TTL
  - CMOS



E88TSGF04-05

The "low-TTL" and "high-TTL" clock levels are :



E88TSGF04-06

For each package version, the following tables resume, the availability of the different clocks, in terms of the power supply.

Note that in 8-pin version, the clock mode (CLKM) is internally set to GND voltage, except in the case of CMOS clock and 0-5V power supply, where CLKM is internally connected to V- voltage.

8-pin Package			
	0/5V	0/10V	– 5/+ 5V
Low-TTL	NO	C	C
High-TTL	NO	YES	YES
CMOS	C	YES	YES
RC Mode	NO	NO	NO
Crystal Mode	NO	NO	NO

C = Customization option.

14-pin Package			
	0/5V	0/10V	– 5/+ 5V
Low-TTL	NO	C	C
High-TTL	NO	CLKM=GND	CLKM=GND
CMOS	CLKM=V–	CLKM=GND	CLKM=GND
RC Mode	CLKM=V–	CLKM=V–	CLKM=V–
Crystal Mode	CLKM=V–	CLKM=V–	CLKM=V–

ELECTRICAL OPERATING CHARACTERISTICS :

WITH SINGLE SUPPLY VOLTAGE :
T_{amb} = 25°C, V + = 10V, V – = 0V, GND = 5V (unless otherwise specified)

CLKM	Parameter	Min.	Typ.	Max.	Unit
GND	Threshold Voltage		1.5		V
	External Clock Frequency			5	MHz
V –	RC MODE :				
	High Threshold Voltage on CLKIN	1	1.25	1.5	V
	Corresponding Voltage on CLKR		– 5		V
	Low Threshold Voltage on CLKIN	1.5	– 1.25	– 1	V
	Corresponding Voltage on CLKR		+ 5		V
	Oscillator Frequency			5	MHz
	Resistor	2		10 000	kΩ
	Capacitor	0		47	nF
V –	CRYSTAL MODE :				
	Oscillator Frequency			5	MHz
	Resistor		1		MΩ
	Capacitor C_R	10		100	pF
	Capacitor C_{IN}	10		30	pF

ELECTRICAL OPERATING CHARACTERISTICS (continued)

WITH DUAL SUPPLY VOLTAGE :
T_{amb} = 25°C, V + = 5V, V – = – 5V, GND = 0V (unless otherwise specified)

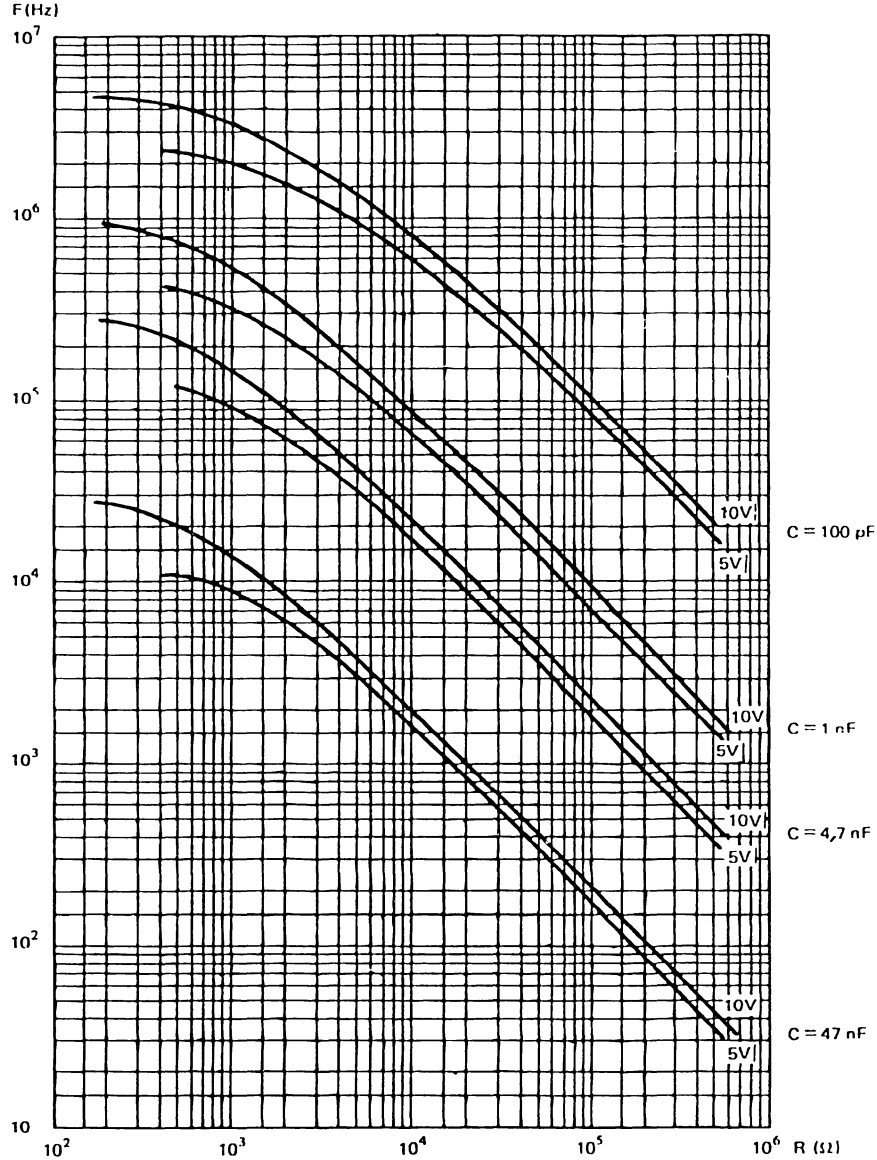
CLKM	Parameter	Min.	Typ.	Max.	Unit
GND	Threshold Voltage		6.5		V
	External Clock Frequency			5	MHz
V –	RC MODE :				
	High Threshold Voltage on CLKIN	6	6.25	6.5	V
	Corresponding Voltage on CLKR		0		V
	Low Threshold Voltage on CLKIN	3.5	3.75	4	V
	Corresponding Voltage on CLKR		+ 10		V
	Oscillator Frequency			5	MHz
	Resistor	2		10 000	kΩ
	Capacitor	0		47	nF
V –	CRYSTAL MODE :				
	Oscillator Frequency			5	MHz
	Resistor		1		MΩ
	Capacitor C_R	10		100	pF
	Capacitor C_{IN}	10		30	pF

WITH SINGLE SUPPLY VOLTAGE :
T_{amb} = 25°C, V + = 5V, V – = 0V, GND = 2.5V (unless otherwise specified)

CLKM	Parameter	Min.	Typ.	Max.	Unit
GND	Threshold Voltage		3.8		V
	External Clock Frequency			5	MHz
V –	RC MODE :				
	High Threshold Voltage on CLKIN	3	3.2	3.4	V
	Corresponding Voltage on CLKR		0		V
	Low Threshold Voltage on CLKIN	1.5	1.8	2	V
	Corresponding Voltage on CLKR		+ 5		V
	Oscillator Frequency			5	MHz
	Resistor	2		10 000	kΩ
	Capacitor	0		47	nF
V –	CRYSTAL MODE :				
	Oscillator Frequency			5	MHz
	Resistor		1		MΩ
	Capacitor C_R	10		100	pF
	Capacitor C_{IN}	10		30	pF

INVERTING TRIGGER FUNCTIONING FREQUENCY VARIATION AS FUNCTION OF R

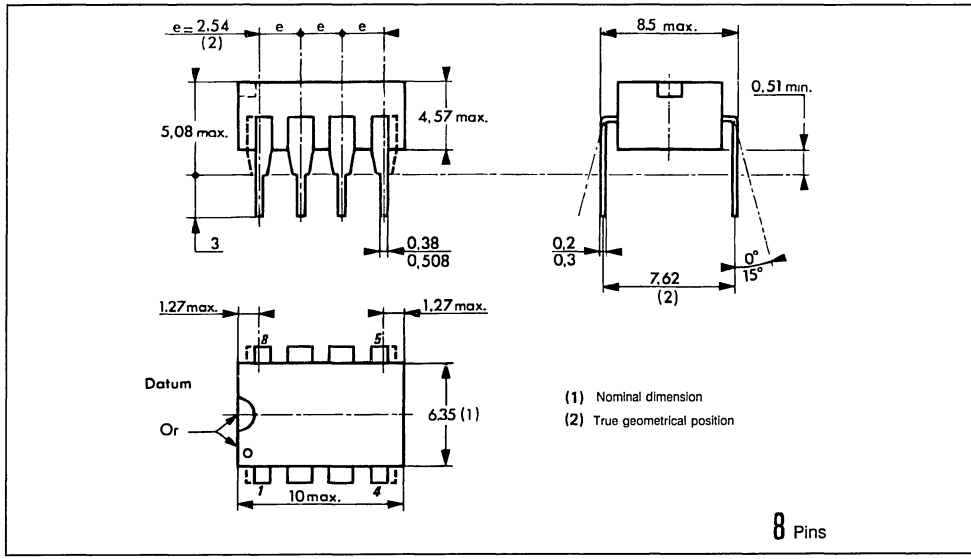
With internal RC oscillator mode, the user's guide for R and C choice is given by following curves and for both supply voltages : 0.5V, 0.10V.



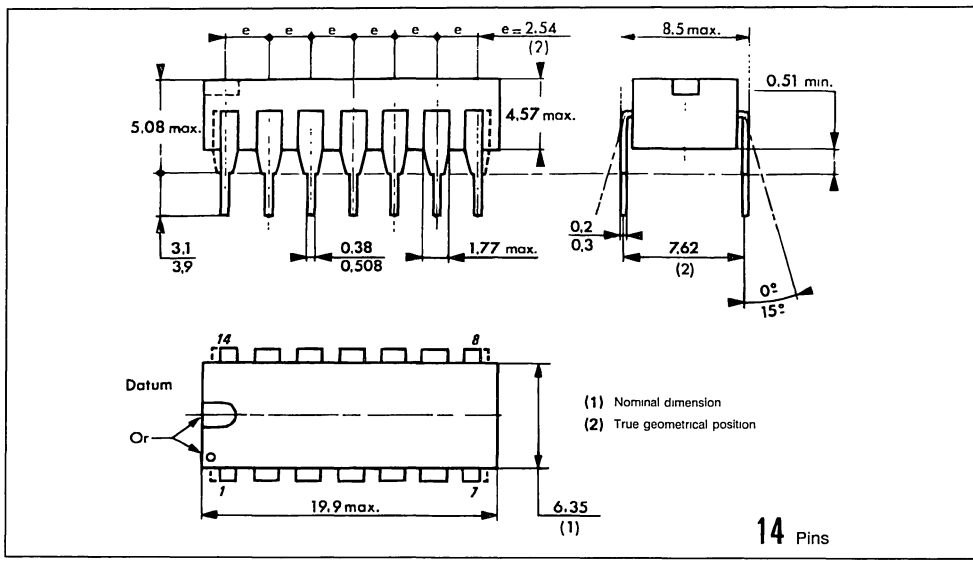
E88TSGF04-07

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP



14 PINS - PLASTIC DIP

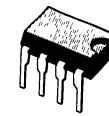


TSGF08 - 4th TO 8th ORDER ANALOG FILTER

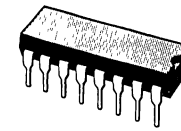
The TSGF08 array provides users with filter integration from 4th to 8th order. 2 package versions are offered to users :

- 8 pin DIL, where only the filter unit is accessible,
- 16 pin DIL, where 2 uncommitted Op-amps are added to previous version.

TSGF08 are also available in SO wide package version (0.3 inch) : 16 pin version only.



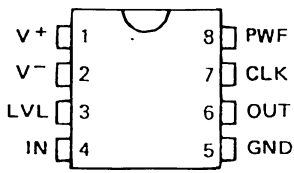
P
DIP-8
(Plastic Package)



P
DIP-16
(Plastic Package)

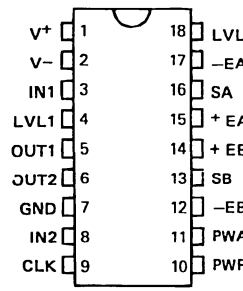
TSGF08
BLOCK DIAGRAM
See figure 4 (E88TSGFSERIES-05)

PIN CONNECTIONS



E88TSGF08-01

8 pins : FILTER ONLY
Compatible with TSGF04

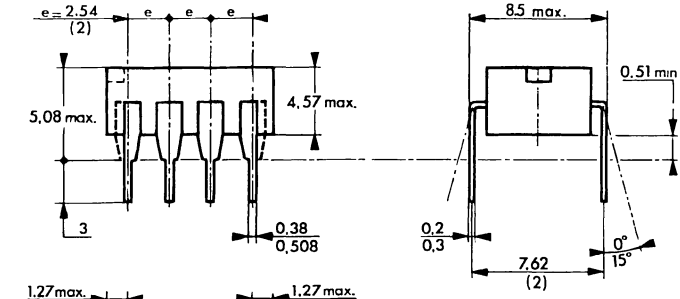


E88TSGF08-02

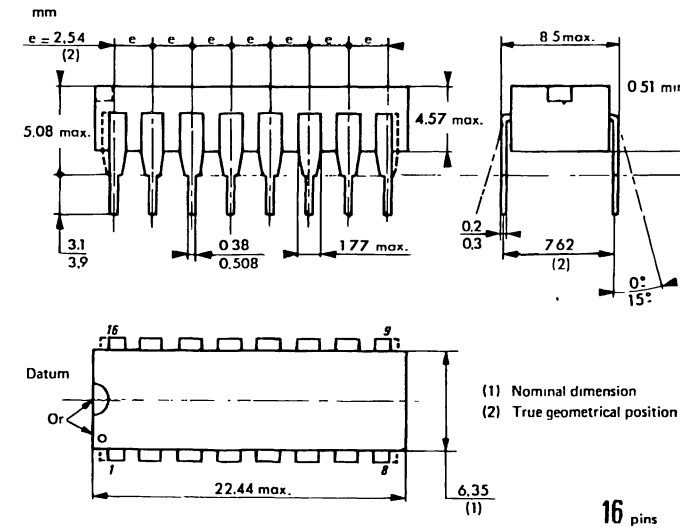
16 pins : Filter
: + 2 Op - Amp
Compatible with TSGF12 (with a single filter)

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP



16 PINS - PLASTIC DIP



TSGF12 - 8th TO 12th ORDER ANALOG FILTER

TSGF12 array offers the capability to integrate either one single from 8th to 12th order or 2 different filters whose sum of orders cannot exceed 12.

These 2 different filters can have either same clock or 2 different clock inputs.

The TSGF12 package versions are :

- 16 pin DIL : 1 filter + 2 Op-amps
- 16 pin DIL : 1 filter + 2 Op-amps + driving of output S/H
- 16 pin DIL : 2 filters + 1 Op-amp + 2 clock inputs.
- 18 pin DIL : 2 filters + 2 Op-amps + 1 clock input.
- 20 pin DIL : 2 filters + 2 Op-amps + 2 clock inputs.
- 20 pin DIL : 2 filters + 2 Op-amps + 2 clock inputs + driving of output S/H.

TSGF12 array are also avaialble in SO wide package version (0.3 inch) : 18 and 24 pin versions.

In case of dual filter integration, the CLKSH pin operates only on the output of filter n° 1 (OUTPUT 1). In the same case, for the 16 pin version, only LVL2 pin is available : therefore user can only adjust the Output DC level of filter 2.

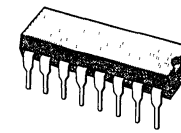
Clock divider :

The number of dividers by 2 available on TSGF12 array is 8.

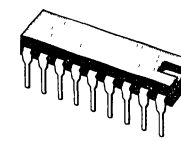
Therefore in case of dual filter on chip integration, there are 2 possibilities to use the clock divider :

- if one filter does not require internal dividers, the 8 dividers by 2 are available for the second filter ;
- if the first filter requires n internal dividers, it remains only 7-n ones available for the second filter.

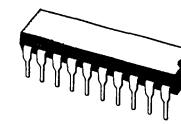
TSGF12
BLOCK DIAGRAM
See figure 4 (E88TSGFSERIES-05)



P
DIP-16
(Plastic Package)

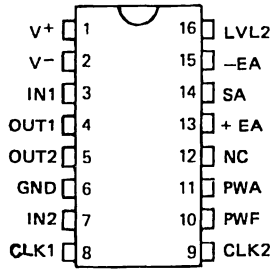


P SUFFIX
DIP-18
(Plastic Package)



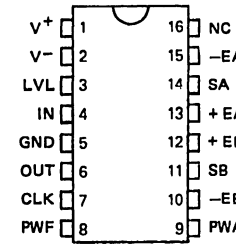
P
DIP-20
(Plastic Package)

PIN CONNECTIONS



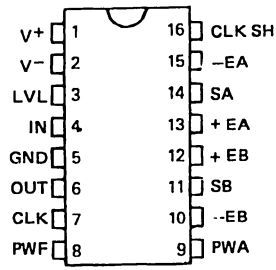
E88TSGF12-01

16 PINS : 2 filters
+ 1 OP - Amp
+ 2 Clock inputs.



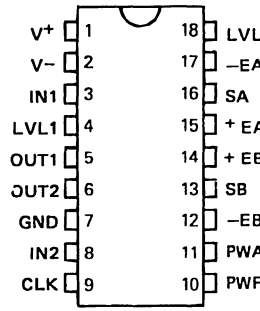
E88TSGF12-02

16 PINS : 1 filter
+ 2 OP - Amp
Compatible with TSGF08



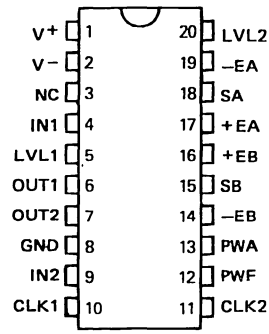
E88TSGF12-03

16 PINS : 1 filters
+ 2 OP - Amps
+ Driving of output S/H.



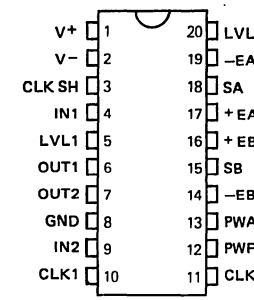
E88TSGF12-04

18 PINS : 2 filters
+ 1 OP - Amp
+ 1 Clock input.



E88TSGF12-05

20 PINS : 2 filters
+ 2 OP - Amps
+ 2 Clock inputs.

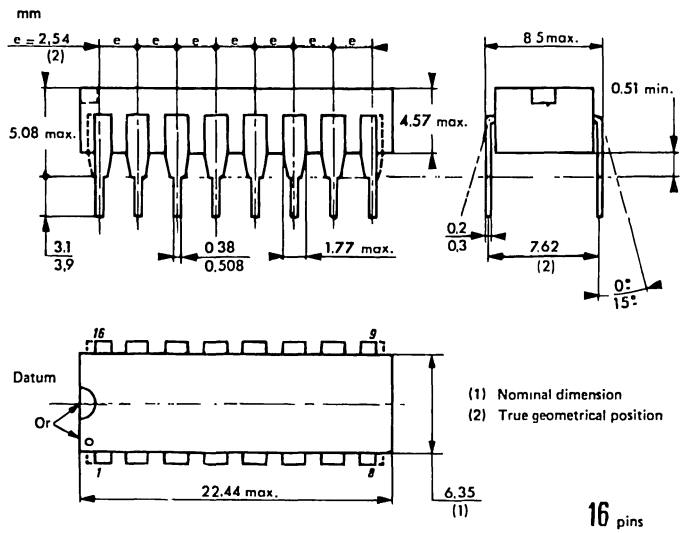


E88TSGF12-06

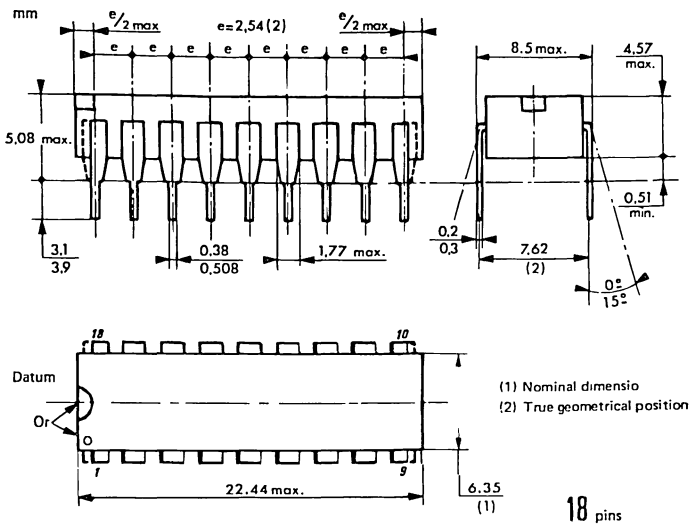
20 PINS : 2 filters
+ 2 OP - Amps
+ 2 Clock inputs
+ Driving of output S/H.

PACKAGE MECHANICAL DATA

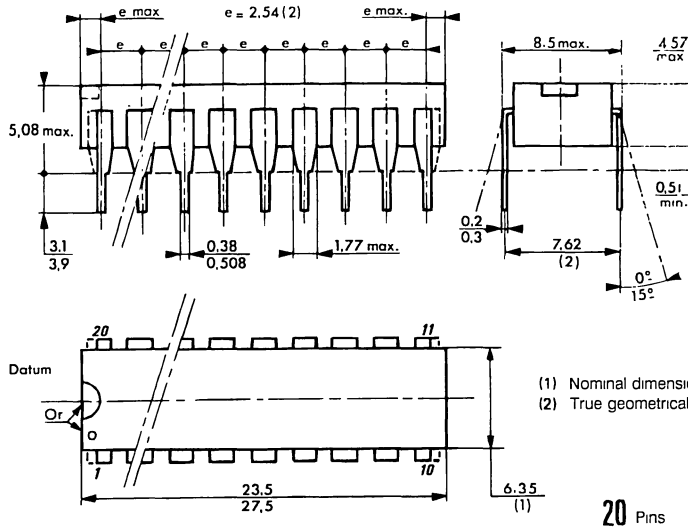
16 PINS - PLASTIC DIP



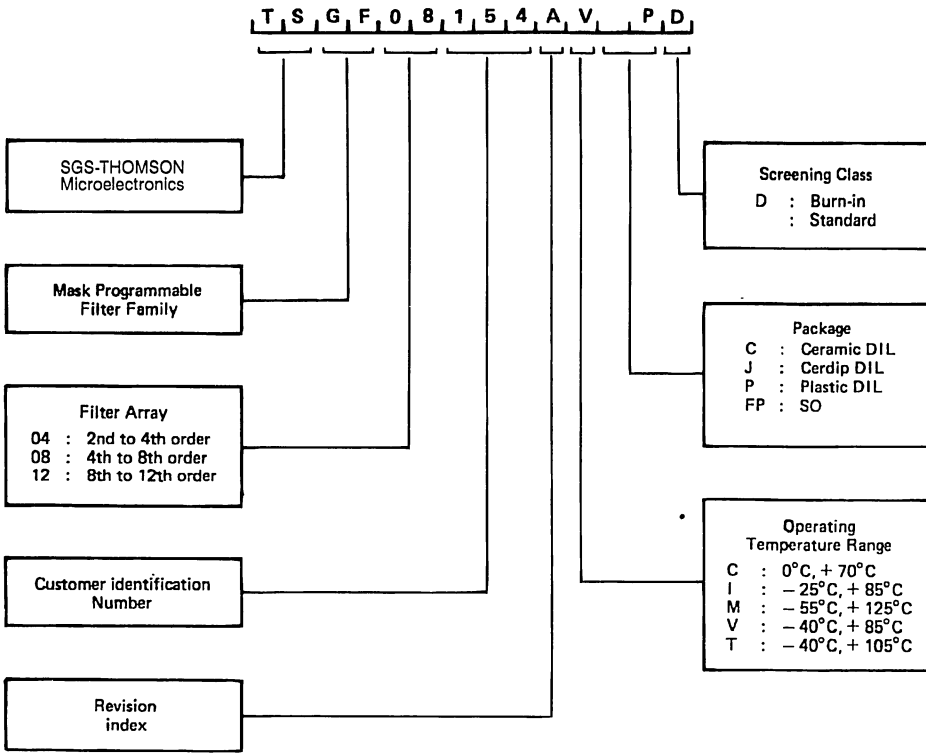
18 PINS - PLASTIC DIP



20 PINS - PLASTIC DIP



ORDER CODES


T S G F 0 8 1 5 4 A V P D
SGS-THOMSON Microelectronics
Mask Programmable Filter Family
Filter Array
04 : 2nd to 4th order
08 : 4th to 8th order
12 : 8th to 12th order
Customer identification Number
Revision index
Screening Class
D : Burn-in
: Standard
Package
C : Ceramic DIL
J : Cerdip DIL
P : Plastic DIL
FP : SO
Operating Temperature Range
C : 0°C, + 70°C
I : − 25°C, + 85°C
M : − 55°C, + 125°C
V : − 40°C, + 85°C
T : − 40°C, + 105°C

SGS-THOMSON MICROELECTRONICS

TSGSM SERIES

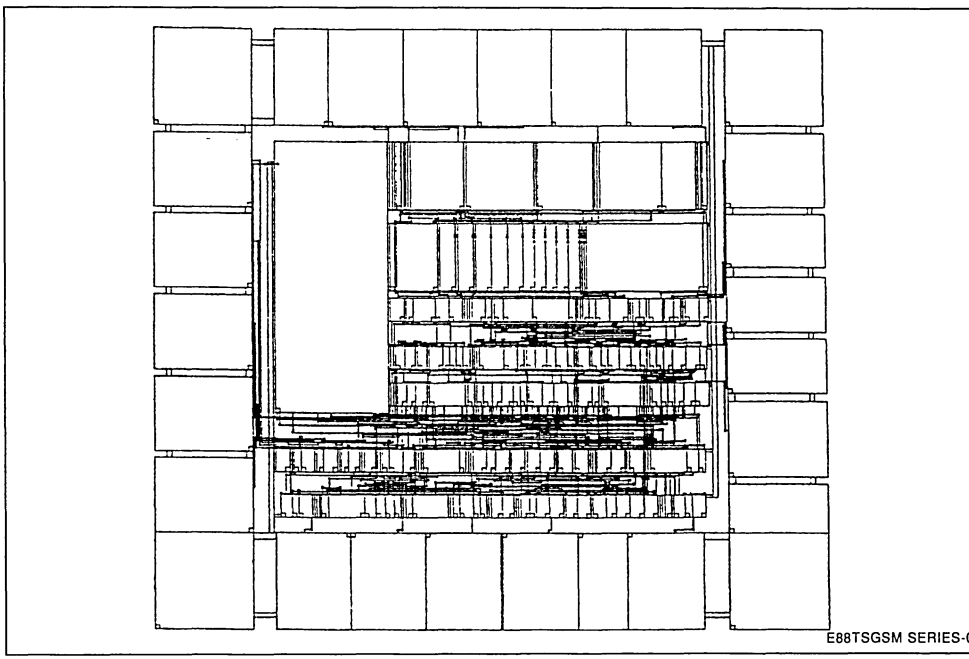
3.5µ/2 POLY / 1 METAL HCMOS MIXED ANALOG-DIGITAL STANDARD CELLS

- ADVANCED HCMOS TECHNOLOGY :
  - 3.5µ drawn channel length
  - 2 polysilicon layers
  - 1 metal layer
  - P well silicon gate CMOS process
- HIGH LATCH-UP IMMUNITY
- FULL ESD PROTECTION
- POWER SUPPLY
  Maximum ratings : - 0.5V to + 12V
  Operating conditions : 3 to 10V
- EXTENSIVE MACROCELL LIBRARY
  - 94 logic cells
  - 66 analog cells
    with programmable cells : soft macro cells, abuttable cells
- INPUT/OUTPUT CELLS
  Compatibility : TTL or CMOS levels
  Configurability : input/output/bidirectional i/o/analog I/O ...
- CAD SOFTWARE SUPPORT
  - ADS (Analog Design System)
  - Fully integrated (+ FILCAD™ for filter design)
  - Flexible design interfaces
- OPERATING TEMPERATURE RANGE
  COMMERCIAL : 0 TO + 70°C
  INDUSTRIAL : − 40 TO + 85°C
  MILITARY : − 55 TO + 125°C
- PACKAGE OPTIONS
  DIL : PLASTIC OR CERAMIC
  SMD : SO, PLCC, LCCC, QF

DESCRIPTION

The TSGSM Series, mixed analog-digital Standard Cell products from SGS-THOMSON Microelectronics, represents a major step allowing the system designer dealing with both digital and high level ana-

Figure 1 : Example of TSGSM Chip Layout.



log functions to benefit of the state of the art semi-custom circuit integration capabilities.

The large variety of predefined and precharacterized functions ranging :

- in digital from simple gates to counters, registers...
- in analog from single operational amplifier to A/D or D/A converters, switched capacitors filters ...

has been proven extremely efficient in the design of many mixed HCMOS Analog-Digital ASIC's circuits in such various applications as consumer, computer, industrial, military, telecommunications and automotive fields.

TSGSM ARCHITECTURE

TECHNOLOGY

TSGSM Series developed by SGS-THOMSON is using an advanced silicon gate P well, dual poly-silicon layer, single metal layer HCMOS technology.

The process is very well suited for the design and integration of high performance analog functions combined with digital. It achieves operating speeds up to 15MHz for the digital part of the TSGSM circuit.

Thanks to the 2 polysilicon layers, TSGSM Series can integrate high accuracy switched capacitors filters based on the same concept of TSGF Series, switched capacitor Filter Arrays (Refer to TSGF04/08/12 Data Sheet). True capacitors are realized with Poly 1 and Poly 2 layers.

CELLS

Predesigned and precharacterized Macrocells are selected, placed and interconnected on the chip to implement the mixed analog-digital function.

Digital and Analog Macrocells have different height, as shown on the chip layout of fig. 1. In addition some cells like A/D or D/A converters are designed as fixed blocks.

CHIP TOPOLOGY

The inputs and outputs of cells are interconnected by using 2 conductive layers : polysilicon and metal.

The chip layout is composed of cell rows, whose number is determined to optimize the die size, and of horizontal routing channels.

Peripheral cells surround the internal active chip area in order to interface it with its external environment.

Despite the row base architecture complex block functions can be placed and routed on the chip.

Generally for design optimization purpose, power busses of the analog and the digital parts of the chip are routed separately.

CELL LIBRARY

The TSGSM Macrocell library features around 160 different macros :

- 94 digital cells.
- 66 analog cells.

The main characteristics of TSGSM library is to offer users a high flexibility for cell definition and generation :

- The **DIGITAL LIBRARY** provides in addition of existing hard macros the capability to generate soft macros like counters, shift registers, dividers...
  These modulo N parameterized cells are generated at the layout level by lateral abutment of hard macros.
- The **ANALOG LIBRARY** presents particular features such as :
  - Biasing strategy with a current bias generator, programmable current mirrors, and current biased cells and voltage biased cells.
  - Use of programmable cells for capacitor fields (0.1 to 30pF typically), resistor fields (150 to 1.8MΩ), bipolar transistors, MOS transistors, current mirrors.
  - Grounded shield for power supply rejection improvement.

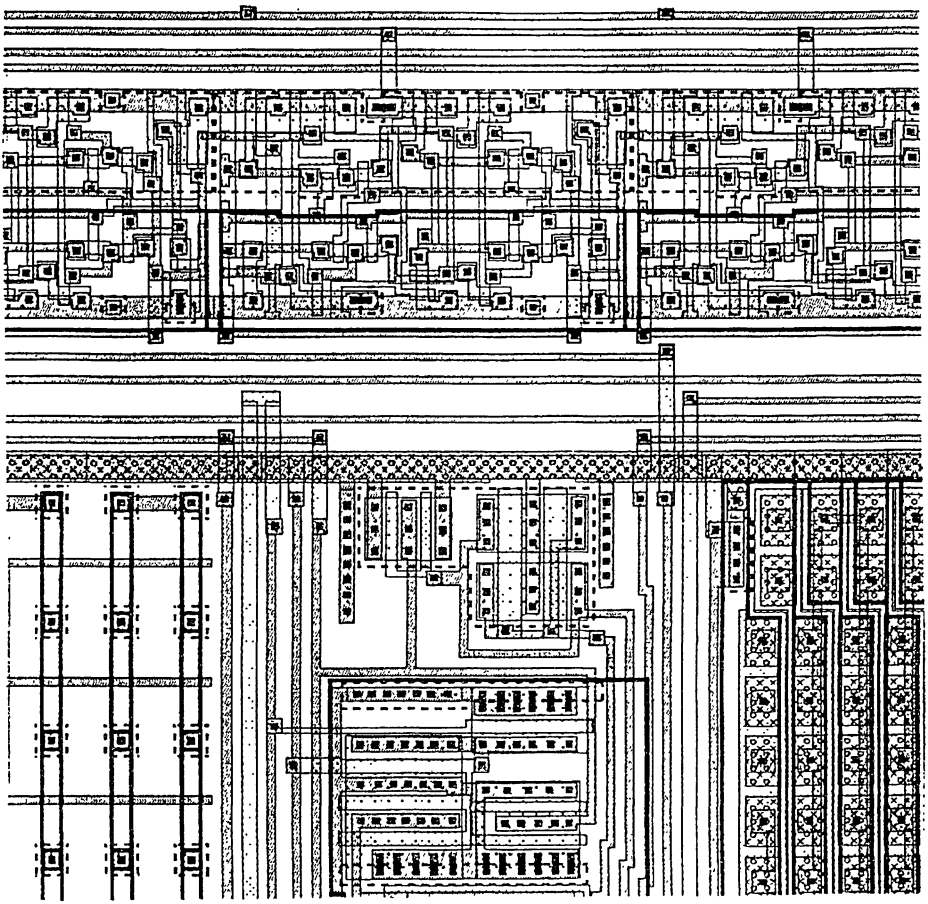
The complete TSGSM library is fully described within the TSGSM User's Manual of the SGS-THOMSON library.

Fig. 4 and Fig. 5 give an abstract of all available digital and analog cells within TSGSM' library.

For more details, users have to refer to the TSGSM User's Manual they can require to their nearest SGS-THOMSON sales office or representative.

Note : SGS-THOMSON can develop on request a special cell for a specific customer circuit : new cell or existing cell with different electrical characteristics.

Figure 2 : Example of Interconnection between Analog and Digital Cells.



E88TSGSM-SERIES-02

Figure 3 : Example of a Mixed Analog-Digital Function.

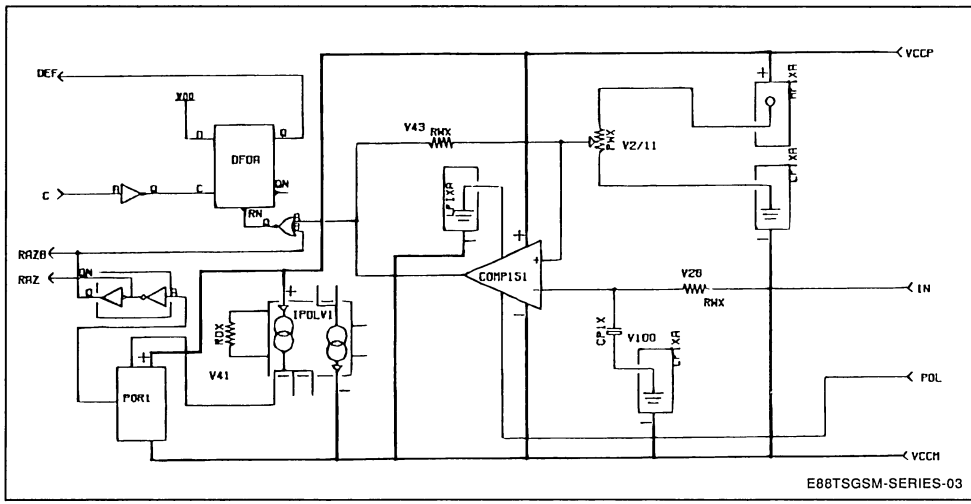


Figure 4 : TSGSM Series Digital Library Abstract.

INTERNAL CELLS

Cell Type	Description	Number of Different Options (1)
AA..	AND Gates	3
AN..	AND into NOR Gates	4
DF..	D Flip-flops	4
DL..	D Latches	5
EN..	Exclusive NOR	1
EO..	Exclusive OR	2
FF..	D Flip-flops (2 clocks)	4
II..	Dual Buffers	2
IN..	Inverters	5
IT..	Tri-state Internal Buffers	3
MU..	Multiplexers	3
NA..	NAND Gates	4
NO..	NOR Gates	4
ON..	OR into NAND Gates	2
OR..	OR Gates	3
TF..	Toggle Flip-flops	3
TG..	Schmitt Triggers	3
TT..	Level Shifters	3
ZZ..	Supply Cells	2
CCG	Clock Generators	3
FPCG	Non-overlapping 4-phase Clock Generator	1
TPCG	Non-overlapping 2-phase Clock Generator	1
INVL	Delay Inverter	1

(1) For each type of cell, the TSGSM library provides extensive number of options as for example :
- NAND type cells : 2, 3, 4 or 6 input NAND's
- D flip-flop cells : with low set, with low reset ..
- input buffers : TTL, CMOS, with pull-up...

Figure 4 (continued).

I/O CELLS

Cell Type	Description	Number of Different Options (1)
OB..	Output Buffers	4
PP..	Power Pads	3
OB..	Tri-state Output Buffers	4
IB..	Input Buffers	8
IO..	Bidirectional Buffers	5
OB..	Open-drain Output Buffers	4

(1) For each type of cell, the TSGSM library provides extensive number of options as for example :
- NAND type cells : 2, 3, 4 or 6 input NAND's
- D flip-flop cells : with low set, with low reset...
- input buffers : TTL, CMOS, with pull-up...

Figure 5 : TSGSM Series Analog Library Abstract.

INTERNAL CELLS

Cell Type	Description	Number of Different Options	Metal Mask Programmable
COMP...	Comparators	6	
MN...	N MOS Transistors	4	x
MP...	P MOS Transistors	4	x
OSC..	Oscillators (crystal RC)	4	
POR.	Power on Reset	2	
SW..	Switches	3	
TRIG	Schmitt Trigger	1	
CP..	Capacitor Fields	1	x
BOPA/BOTA	Bias for Op amps and Transconductance Amplifiers	3	
BIP	Bipolar Transistors	1	x
OP	Operational Amplifiers	5	
OO	Output Stage for Op Amp	1	
OT	Transconductance Amplifiers	2	
R..	Resistance Fields	3	x
P..	Potentiometer Fields	3	x
VREF	Voltage Reference Bandgap	1	
ZEN..	Zener Diodes	3	
IPNV	Current Mirror Source-sink	1	x
IPOL..	Bias Current Generator	2	x
ISN/ISP	Current Mirror Source/sink	4	x
HF/LF	Internal V^+/V^- Analog Cell	2	

BLOCKS AND SOFT MACROS

Cell Type	Description	Number of Different Options	Metal Mask Programmable
ADC8	8 Bit Analog to Digital Converters	2	
ADC12	12 Bit Analog to Digital Converter	1	
DAC8	8 Bit Digital to Analog Converter	1	
DBP/DS1	LCD Drivers	3	
SCF	Biquadratic 2nd Order Filter	1	x
VRLCD	LCD Voltage Reference	1	

ADS ANALOG DESIGN SYSTEM

The SGS-THOMSON TSGSM Series is fully supported by a complete Computer Aided Design (CAD) system. The SGS-THOMSON CAD system, ADS, is complete in that once a design is entered all the tools necessary to complete that design are available to the user in this one system.

These tools include schematic capture, logic and analog simulations, fault simulation, automatic place and route, parasitic delay extraction and test pattern generation.

ADS ANALOG DESIGN SYSTEM is available on DEC™ VAX™ computer systems.

In addition, the TSGSM library is implemented on CAE workstations :
- Mentor™
- Daisy™.

SGS-THOMSON developped direct interfaces between these CAE workstations and its ADS system.

The ADS package allows the development of analog and digital standard cell circuits so easily that each system designer can handle it.

The development of mixed analog and digital circuit is done with advanced concepts such as :
- parameterized cells (resistors, capacitors, current generators ...)
- metal mask programmable cells (switched capacitor filters ...)
- compiled cells (bit slice concept for digital functions like counters, dividers ...).

The main CAD tools available within ADS are :

■ SCHEMATIC GRAPHIC CAPTURE

SDS™ provides graphic capture of schematic circuit diagram. Designer can create blocks by using the 100% hierarchy of SDS™ and also can specify values of parameterized cells.

After the net list generation, the modules generated under SDS™ are oriented automatically thru logic or analog simulation.

■ LOGIC SIMULATION

HILO3™, hierarchical logic simulator, allows design verification and timing analysis of the circuit. A pre-layout timing analysis is run with calculated delays based on fanout, VDD, temperature and best, typical or worst case process conditions.

The 2 input files to HILO3™ are the net list generated from graphic capture and the input test pattern description.

HILO3™ simulator allows mixed analog and digital simulation for analog cells having an equivalent model described under HILO3™.

■ ANALOG SIMULATION

H3SPICE electrical simulator allows pre-layout or post-layout timing analysis of the analog blocks of the circuit.

H3SPICE input files are the net list and the input test pattern descriptions.

With the improvements brought by SGS-THOMSON to H3SPICE, the analog simulator becomes a powerful CAD tool :
- special level modelling for speed improvement on digital sub-circuits,
- fast execution on full analog part of TSGSM circuit, thanks to macro modelling, allows simulation of large analog blocks.

■ PLACEMENT AND ROUTING

CALMP™ software is an efficient standard cell automatic place and route whose main features are :
- use of different heights of cells on the chip
- interactive pre-placement of blocks, cells and I/O's for die size optimization
- capability to force priorities on nets for critical path routing
- capability to generate soft macros, blocks by cell abutment.

A check program performs at the end of the layout, design rule checking and verifies conformity of the graphic data base versus the schematics data base.

■ PARASITIC DELAY EXTRACTION

ADS is computing the exact parasitic delays brought by the placement and routing. Delays are based both on resistance and capacitance of each interconnect.

As soon as the parasitic RC delays are extracted, user can run a post layout simulation for accurate timing new analysis.

■ TEST GENERATION

According to the input test patterns already described, user can determinate the testability coverage ratio of its digital test sequence thanks to the fault simulator which is incorporated within HILO3™.

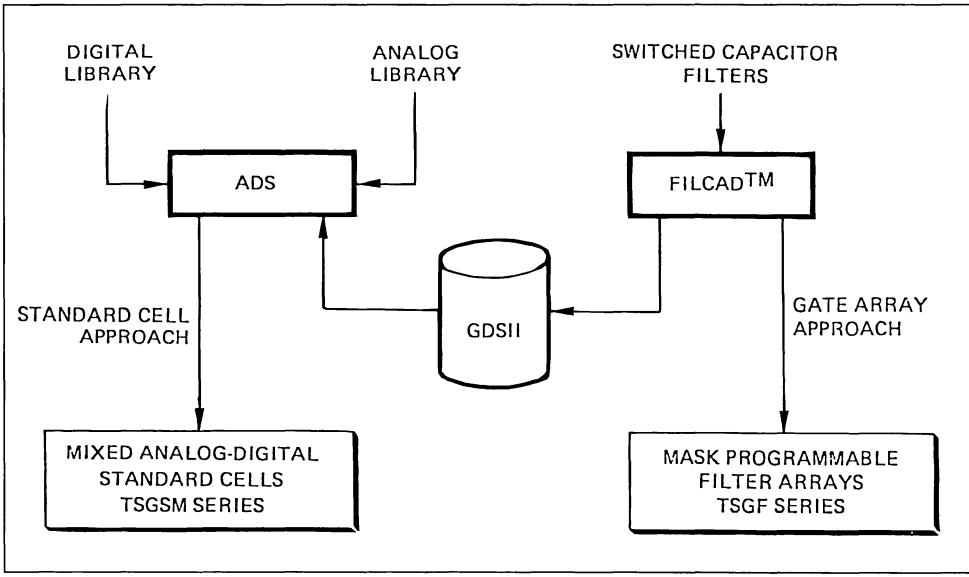
Depending of the fault simulator results user can generate new input test patterns in order to improve testability coverage.

ADS software converts automatically the post layout simulation (with parasitic delays) file into test patterns directly compatible with SGS-THOMSON test equipments.

At same time static and dynamic parameters are added to the functional test pattern file : all input/output levels are tested during the functional test sequence.

Fig. 6 outlines the SGS-THOMSON approach for the design of analog or mixed analog/digital circuits.

Figure 6 : SGS-THOMSON CAD Tools and Product for Analog and Mixed Analog-Digital Circuits.



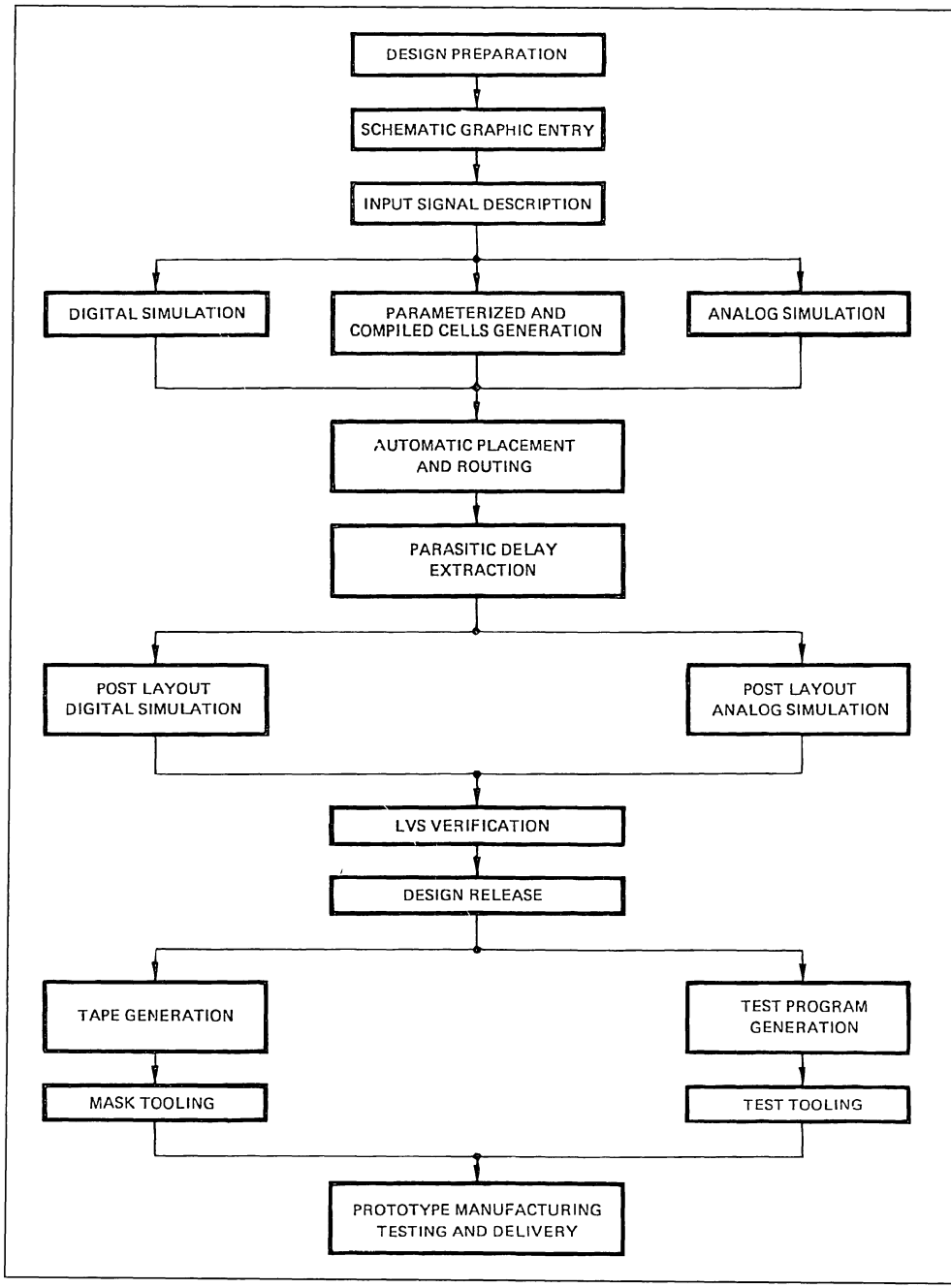
One of the particularities of TSGSM series is to provide switched capacitor filter integration capabilities. The filter cells available within TSGSM library are identical to those used on the SGS-THOMSON Analog Filter Arrays, TSGF Series, which are mask programmable switched capacitor filters.

For filter synthesis, simulation and layout, designers are given an efficient Filter CAD design tool : FILCAD™.

For more informations about SGS-THOMSON switched capacitor filter design solutions and CAD tools, please refer to TSGF04/08/12, 4th to 12th order switched capacitor filter arrays data sheet.

Fig. 7 shows the development phases of a TSGSM Series standard cell. The design translation phase up to the prelayout simulation can be done either on CAE workstations like Daisy Systems™ and Mentor Graphics™, or on VAX™ computer with ADS Analog Design System.

Figure 7 : TSGSM Series Development Flow.



CUSTOMER DESIGN INTERFACE

SGS-THOMSON has developed several interfaces for customers giving them easy and flexible design approaches for TSGSM 3.5µ/2 poly/1 metal HCMOS mixed Analog Digital Standard Cells series.

User can access ADS Analog Design System.
- via the SGS-THOMSON Design Centers,
- via connection to SGS-THOMSON CAD Center,
- via the SGS-THOMSON associated Design Centers.

CAE workstations capabilities are :
- Daisy Systems™
- Mentor Graphics™.

In that case direct interfaces will be offered to user in order to make design implementation and test generation with ADS.

According to all of these design possibilities, SGS-THOMSON defined 3 main customer design interfaces.

Figure 8 outlines these interfaces. Each interface delineates the responsibilities of customer and SGS-THOMSON during circuit development flow shown in fig. 7.

Figure 8 : Design Interface.

	Interface 2	Interface 3	Interface 4
Definition of Circuit Specification	Customer	Customer	Customer
Logic and Electrical Description	Customer	Customer	Customer
Test Pattern Definition	Customer	Customer	Customer
Graphic Capture + Input Signal Entry	ST	Customer	Customer
Design Verification	ST	Customer	Customer
Pre-layout Simulation	ST	Customer	Customer
Approval	Customer	Customer/ST	
Auto Place and Route	ST	ST	Customer
Post-layout Simulation	ST	ST	Customer
Design Release	Customer	Customer/ST	Customer/ST
Test Program Generation - Test Tooling	ST	ST	ST
Mask Tooling	ST	ST	ST
Prototype Manufacturing and Testing	ST	ST	ST
Prototype Delivery	ST	ST	ST

With interface 3, design can be done either at SGS-THOMSON Microelectronics Design Center facilities or at customer location.

ABSOLUTE MAXIMUM RATINGS (note 1) $T_{amb.}$ = 25°C, voltage referenced to V_{SS}.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage	– 0.5	12.0	V
V_I, V_O	I/O Voltage	– 0.5	V_{DD} + 0.5	V
I_I, I_O	I/O Current	– 40	+ 40	mA
T_{stg}	Storage Temperature (ceramic)	– 65	+ 150	°C
	Storage Temperature (plastic)	– 40	+ 125	°C

Note : 1. Stresses above those listed order "maximum rating" may cause permanent damage to the device. This is a stress rating only and functional operation to the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS Voltage referred to V_{SS}

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Operating Supply Voltage	4.5 9.0	5.0 10.0	5.5 11.0	V
V_{DD}	Extended Supply Voltage (note 2)	3		12.0	V
$T_{amb.}$	Operating Ambient Temperature Military Industrial Commercial	 – 55 – 40 0		 + 125 + 85 + 70	°C

Note : 2. For extended supply voltage please consult SGS-THOMSON Microelectronics.

DC GENERAL ELECTRICAL CHARACTERISTICS V_{DD} = 5V ± 10% or V_{DD} = 10V ± 10% (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	High Level TTL Input Voltage	V_{DD} = 5V ± 10% T° = 0°C/= 70°C T° = – 40°C/+ 85°C T° = – 55°C/+125°C	 2.0 2.25 2.25			V
V_{IL}	Low Level TTL Input Voltage	V_{DD} = 5V ± 10% All Temp. Ranges			0.8	V
V_{IH} V_{IL}	High Level CMOS Input Voltage Low Level CMOS Input Voltage		70% V_{DD}		 30% V_{DD}	V
I_{OZH}	Tristate Output Leakage Current	V_O = V_{DD} T° = 0°C/+ 70°C T° = – 40°C/+ 85°C T° = – 55°C/+ 125°C			2.5 5 10	µA
I_{OZL}		V_O = V_{SS} T° = 0°C/+ 70°C T° = – 40°C/+ 85°C T° = 55°C/+ 125°C	 – 2.5 – 5.0 – 10.0			µA
I_{IH}	High Level Input Leakage Current	V_I = V_{DD} T° = 0°C/+ 70°C T° = – 40°C/+ 85°C T° = – 55°C/+ 125°C			 1.0 3.0 5.0	µA
I_{IL}	Low Level Input Leakage Current	V_I = V_{SS} T° = 0°C/+ 70°C T° = – 40°C/+ 85°C T° = – 55°C/+ 125°C	 – 1.0 – 3.0 – 5.0			µA
I_{CC}	Max Admissible Current per Pin : – Analog – Digital				 ± 20 ± 40	mA

DIGITAL LIBRARY AC ELECTRICAL CHARACTERISTICS ABSTRACT V_{DD} = 10V ± 10%, T_{amb} = 25°C, Typical Process Standard Condition = 2 Loads + 1mm of Metal Interconnect

Cell Code	Description	V_{DD} = 10V ± 10%			Unit
		T_{PHL}	T_{PLH}	Other	
IN01	Standard Inverter	5.7	4.7		ns
NA02	2-input NAND	6.2	5.8		ns
NO02	2-input NOR	6.4	5.1		ns
DF08	Positive Edge D Flip-Flop from CKL to Q : T_{SH} T_H T_{WH} T_{WL}	10.6	6.1	 14.0 5.0 20.0 16.0	ns
OB2	TTL Inverting Output Buffer Capacitance Load = 50pF = 25pF = 15pF	 4.1 3.6 3.4	 5.0 4.3 4.0		ns
T02	Tri-state TTL Output Buffer Capacitance Load = 50pF = 25pF = 15pF	 4.1 3.6 3.4	 5.0 4.3 4.0		ns
IB021	CMOS Inverting Input Buffer	7.4	8.7		ns

Note : Refer to TSGSM User's Manual for more detailed informations

ANALOG LIBRARY AC ELECTRICAL CHARACTERISTICS ABSTRACT V_{DD} = 10V ± 10%, unless otherwise specified T = 25°C, typical process.

Cell Code	Description	Parameter/conditions	Min.	Typ.	Max.	Unit
COMP	Static Comparator	Propagation Delay (overdrive = 10mV) Offset		1 ± 5	2 ± 15	µs mV
CP1X	Capacitor Fields	Unit Capacitance Capacitor Value Range Absolute Accuracy Matching (capacitor ratio)	0.08 0.1	0.1 0.5	0.12 50 ± 15 1.0	pF pF % %
	Resistors					
RPX/PPX	. Polysilicon	Resistor Value Range Absolute Accuracy Matching Temperature Coefficient	.15		20 ± 20 ± 1 0.15	kΩ % % %/°C
RDX/PDX	. P^+ Diffusion	Resistor Value Range Absolute Accuracy Matching Temperature Coefficient	.75		100 ± 20 ± 1 0.15	kΩ % % %/°C
RWX/PWX	. P^- Well	Resistor Value Range Absolute Accuracy Matching Temperature Coefficient Voltage Coefficient	5		2000 ± 20 ± 2 ± 1 5	kΩ % % %/°C %/V
	Switches					Ω
SWIX	. Analog Switch	R_{ON} Value Range		10k	30k	
MN1X/MP1X	. MOS Switch	R_{ON} Value Range	50		500	
IPOLxx + ISyy	Programmable Reference Current Generator	Current Current Step Supply Voltage Rejection (4V < V_{DD} < 10V)	1	 1 + 2	250	µA µA %/V
OPA2	General Purpose Operational Amplifier	Phase Margin Unit Gain Bandwidth (C_L = 100pF, R_L = 10kΩ) Offset		80 3.3 ± 5	 ± 10	deg MHz mV
OTA1	Transconductance Amplifier	Unit Gain Bandwidth (C_L = 3.5pF)	7	10.5		MHz
POR1	Static Power on Reset	Active Voltage (V_{DD} = 10V) (V_{DD} = 5V)		4.5 3.5		V V
VREF	Voltage Bandgap Reference	Output Voltage	1.15	1.18	1.20	V
ZENx	Zener Diode	Zener Voltage (bias current = 50µA)	5.3	5.6	5.9	V
OSC11	Crystal Oscillator	Frequency	0.1		12	MHz
OSC31	RC Timer	Frequency Stability Versus Temperature Stability Versus Supply Voltage		100 0.02 0.5	500	kHz %/°C %/V
ADC8Bx	8 Bits Analog to Digital Converter	Conversion Time Integral non Linearity			25 ± 0.5	µs LSB
ADC12B	12 Bits Analog to Digital Converter	Conversion Time Differential non Linearity			25 ± 0.7	µs LSB
SCFx	Biquadratic Filter Cell	Signal Frequency Order	 2		30 12	kHz

Note : Refer to TSGSM User's Manual for more detailed informations.

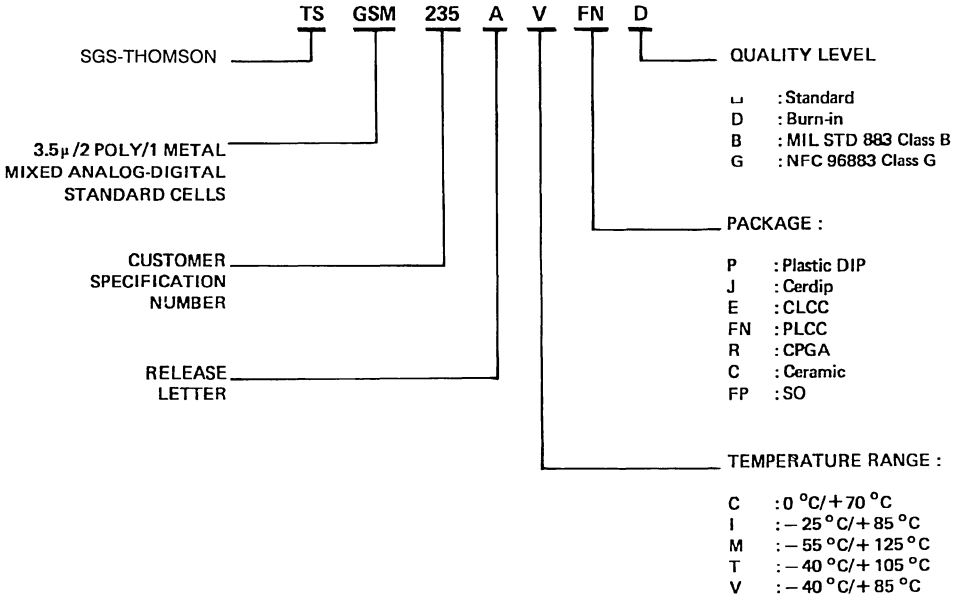
PACKAGING

SGS-THOMSON has a wide variety of package options available to the user :

- Dual in line packages (DIP)
  - Plastic
  - Cerdip
  - Side Braze
- Chip carriers
  - Plastic Leaded Chip Carriers (PLCC)
  - Ceramic Leadless Chip Carriers (CLCC)
  - Ceramic Leaded Chip Carriers (LDCC)
- Small outlines (SO)

Where different packaging requirements are needed, contact SGS-THOMSON Marketing. SGS-THOMSON Microelectronics can also supply standard cells products in dice form (chip tray or wafer form).

ORDER CODES

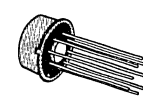


SGS-THOMSON MICROELECTRONICS

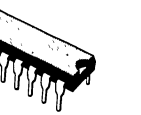
UA741

GENERAL-PURPOSE SINGLE OP-AMPs

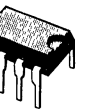
- LARGE INPUT VOLTAGE RANGE
- NO LATCH-UP
- HIGH GAIN
- SHORT-CIRCUIT PROTECTION
- NO FREQUENCY COMPENSATION REQUIRED
- SAME PIN CONFIGURATION AS THE UA709



H
TO99
(Metal Can)



N
DIP14
(Plastic Package)



N
DIP8
(Plastic package)
J
CERDIP8
(Cerdip Package)

D
SO8
(Plastic Micropackage)

GC
LCC20
(Tricecop (LCC))

DESCRIPTION

The UA741 is a high performance monolithic operational constructed on a single silicon chip. It is intended for a wide range of analog applications.

- Summing amplifier
- Voltage follower
- Integrator
- Active filter
- Function generator.

The high gain and wide range of operating voltages provides superior performance integrator, summing amplifier, and general feedback applications. the internal compensation network (6 dB/octave) insures stability in closed loop applications.

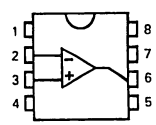
ORDER CODES

Part Number	Temperature Range	Package					
		H	J	GC	N	N 14	D
UA741C/E	0 °C to + 70 °C	•	•		•	•	•
UA741I	–40 °C to + 105 °C	•			•	•	
UA741M/A	–55 °C to + 125 °C	•	•	•			

Note : Hi-Rel Versions Available
Examples : UA741CN, UA741IH

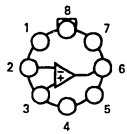
PIN CONNECTIONS (top views)

DIP8/CERDIP8
SO8



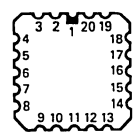
1 - Offset null
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-

TO99



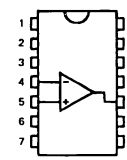
5 - Offset null
6 - Output
7 - V_{CC}^+
8 - NC

LCC20



1 - NC
2 - Offset null
3 - NC
4 - NC
5 - Inverting input
6 - NC
7 - Non-inverting input
8 - NC
9 - NC
11 - NC
12 - Offset null
13 - NC
14 - NC
15 - Output
16 - NC
17 - V_{CC}^+
18 - NC
19 - NC
20 - NC

DIP14

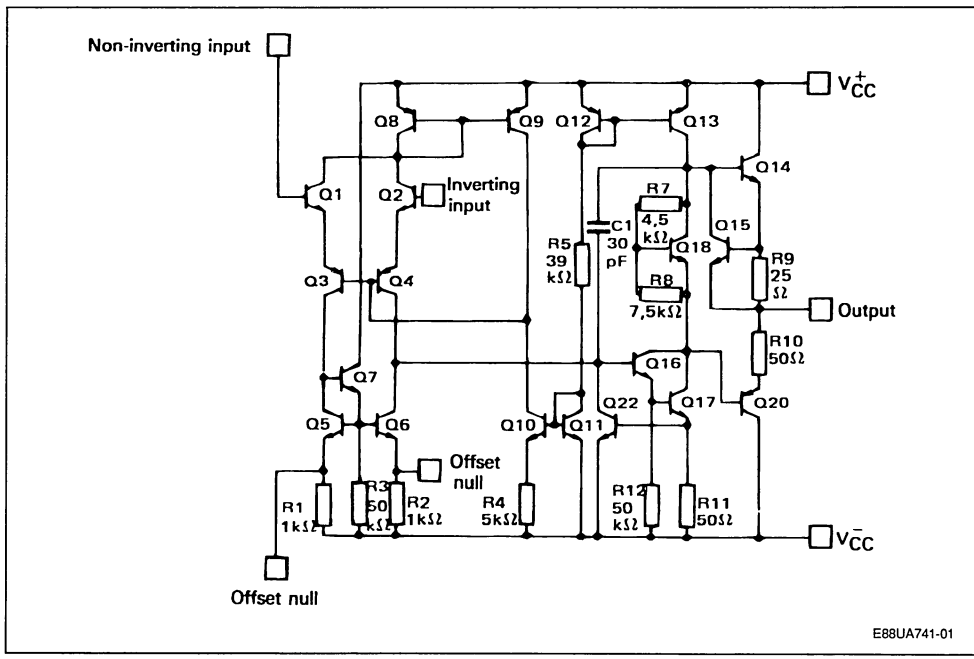


1 - NC
2 - NC
3 - Offset null
4 - Inverting input
5 - Non-inverting input
6 - V_{CC}^-
7 - NC
8 - NC
9 - Offset null
10 - Output
11 - V_{CC}^+
12 - NC
13 - NC
14 - NC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit
		UA741M, A	UA741I	UA741C, E	
V_{CC}	Supply Voltage	± 22	± 22	± 22	V
V_i	Input Voltage	± 15	± 15	± 15	V
V_{id}	Differential Input Voltage	± 30	± 30	± 30	V
P_{tot}	Power Dissipation	500	500	500	mW
	Output Short-circuit Duration	Infinite			
T_{oper}	Operating Free-air Temperature Range	– 55 to + 125	– 40 to + 105	0 to + 70	°C
T_{stg}	Storage Temperature Range	– 65 to 150	– 65 to 150	– 65 to 150	°C

SCHEMATIC DIAGRAM



Case	Offset Null	Inverting Input	Non-inverting Input	V_{CC}^-	V_{CC}^+	Output	N.C.
TO99/DIP8/CERDIP8/SO8	1, 5	2	3	4	7	6	8
DIP14	3, 9	4	5	6	11	10	*
LCC20	2, 12	5	7	10	17	15	*

* **TO116, LCC20 :** Other pins are not connected.

ELECTRICAL CHARACTERISTICS

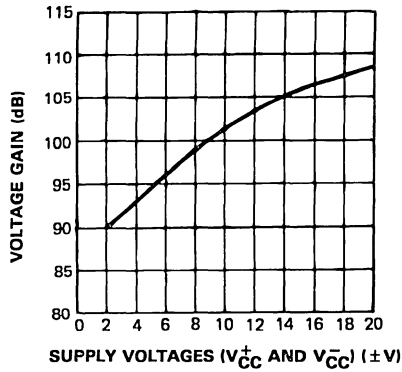
UA741M/A : $-55\ °C \le T_{amb} \le +125\ °C$, $V_{CC} = \pm 15\ V$
UA741I : $-40\ °C \le T_{amb} \le +105\ °C$, $V_{CC} = \pm 15\ V$
UA741C/E : $0\ °C \le T_{amb} \le +70\ °C$, $V_{CC} = \pm 15\ V$
(unless otherwise specified)

Symbol	Parameter	UA741C, E, I, M, A			Unit
		Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage $R_S \le 10\ k\Omega$				mV
	$T_{amb} = 25\ °C$		1	5	
	$T_{min} \le T_{amb} \le T_{max}$			6	
	UA741E, A $T_{amb} = 25\ °C$		1	2	
	UA741E, A $T_{min} \le T_{amb} \le T_{max}$			4	
I_{IO}	Input Offset Current				nA
	$T_{amb} = 25\ °C$		2	20	
	$T_{min} \le T_{amb} \le T_{max}$			40	
I_{IB}	Input Bias Current				nA
	$T_{amb} = 25\ °C$		10	100	
	$T_{min} \le T_{amb} \le T_{max}$			200	
A_{VD}	Large Signal Voltage Gain ($V_O = \pm 10\ V$, $R_L = 2\ k\Omega$)				V/mV
	$T_{amb} = 25\ °C$	50	200		
	$T_{min} \le T_{amb} \le T_{max}$	25			
SVR	Supply Voltage Rejection Ratio ($R_S \le 10\ k\Omega$)				dB
	$T_{amb} = 25\ °C$	77	90		
	$T_{min} \le T_{amb} \le T_{max}$	77			
I_{CC}	Supply Current, no Load				mA
	$T_{amb} = 25\ °C$		1.7	2.8	
	$T_{min} \le T_{amb} \le T_{max}$			3.3	
V_I	Input Voltage Range				V
	$T_{amb} = 25\ °C$	−12		+12	
	$T_{min} \le T_{amb} \le T_{max}$	−12		+12	
CMR	Common Mode Rejection Ratio ($R_S \le 10\ k\Omega$)				dB
	$T_{amb} = 25\ °C$	70	90		
	$T_{min} \le T_{amb} \le T_{max}$	70			
I_{OS}	Output Short-circuit Current $T_{amb} = 25\ °C$	10	25	40	mA
$\pm V_{OPP}$	Output Voltage Swing				V
	$T_{amb} = 25\ °C$ $R_L = 10\ k\Omega$	12	14		
	$T_{amb} = 25\ °C$ $R_L = 2\ k\Omega$	10	13		
	$T_{min} \le T_{amb} \le T_{max}$ $R_L = 10\ k\Omega$	12			
	$T_{min} \le T_{amb} \le T_{max}$ $R_L = 2\ k\Omega$	10			
S_{VO}	Slew-rate ($V_I = \pm 10\ V$, $R_L = 2\ k\Omega$ $C_L \le 100\ pF$, $T_{amb} = 25\ °C$, unity gain)	0.25	0.5		V/µs
t_r	Rise Time ($V_I = \pm 20\ mV$, $R_L = 2\ k\Omega$, $C_L \le 100\ pF$ $T_{amb} = 25\ °C$, unity gain)		0.3		µs
K_{OV}	Overshoot ($V_I = \pm 20\ mV$, $R_L = 2\ k\Omega$, $C_L \le 100\ pF$, $T_{amb} = 25\ °C$, unity gain)		5		%
R_I	Input Resistance, $T_{amb} = 25\ °C$	0.3	2		MΩ

ELECTRICAL CHARACTERISTICS (continued)

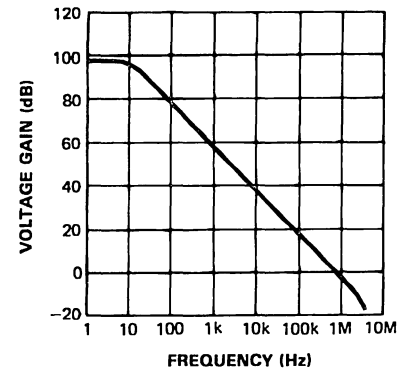
Symbol	Parameter	UA741C, E, I, M, A			Unit
		Min.	Typ.	Max.	
GPB	Gain Bandwidth Product (V_I = 10 mV, R_L = 2 kΩ, $C_L \leq$ 100 pF f = 100 kHz, T_{amb} = 25 °C)	0.7	1	1.6	MHz
THD	Total Harmonic Distortion (f = 1 kHz, A_v = 20 dB, R_L 2 kΩ, V_O = 2 V_{pp} $C_L \leq$ 100 pF, T_{amb} = 25 °C)		0.06		%
V_N	Equivalent Input Noise Voltage (f = 1 kHz, R_G = 100 Ω)		23		$nV/\sqrt{Hz}$
	Phase Margin		50		Degrees

OPEN LOOP VOLTAGE GAIN (Typ.)



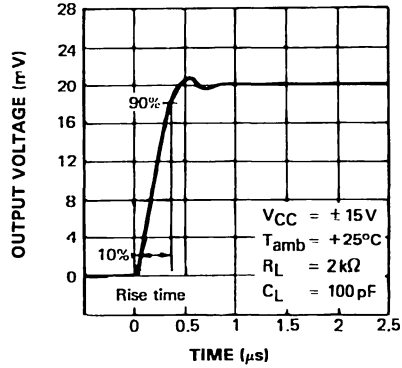
E88UA741-02

OPEN LOOP FREQUENCY RESPONSE (Typ.)



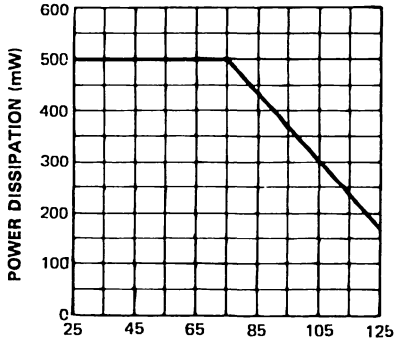
E88UA741-03

TRANSIENT RESPONSE (Typ.)



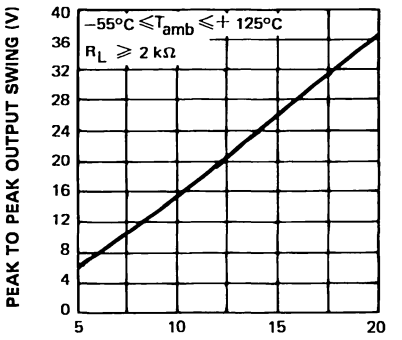
E88UA741-04

ABSOLUTE MAXIMUM POWER DISSIPATION



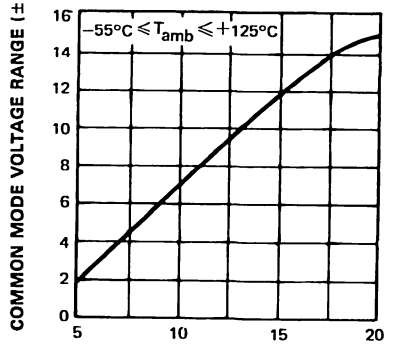
E88UA741-05

OUTPUT VOLTAGE SWING



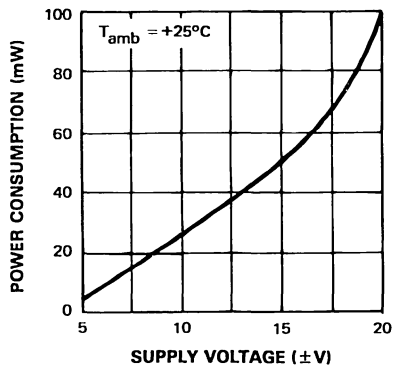
E88UA741-06

INPUT COMMON MODE VOLTAGE RANGE



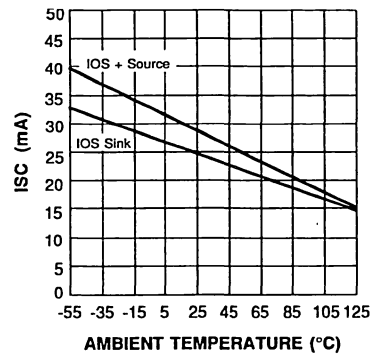
E88UA741-07

POWER CONSUMPTION



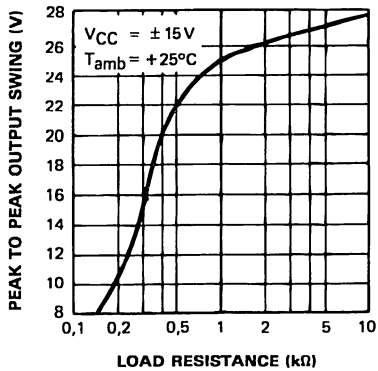
E88UA741-08

OUTPUT CURRENT vs AMBIENT TEMPERATURE



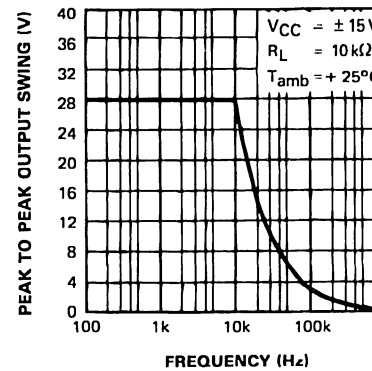
E88UA741-09

OUTPUT VOLTAGE SWING



E88UA741-10

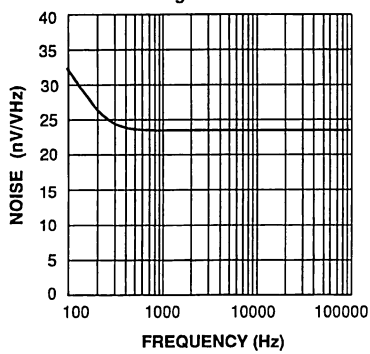
OUTPUT VOLTAGE SWING



E88UA741-11

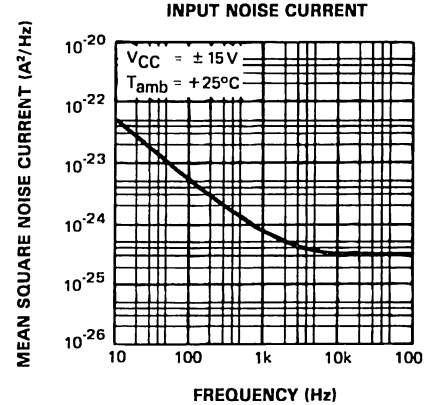
EQUIVALENT INPUT NOISE vs FREQUENCY

Rg = 100 Ω



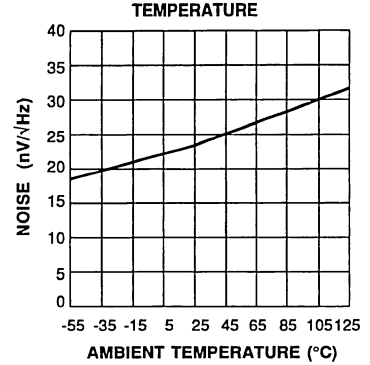
E88UA741-12

INPUT NOISE CURRENT



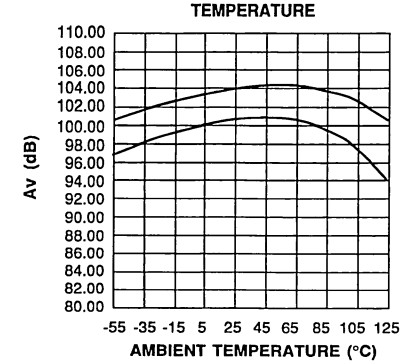
E88UA741-13

EQUIVALENT INPUT NOISE vs AMBIENT TEMPERATURE



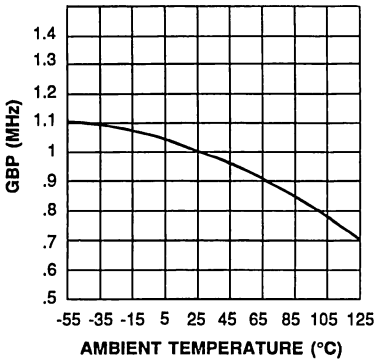
E88UA741-14

LARGE SIGNAL VOLTAGE GAIN vs AMBIENT TEMPERATURE



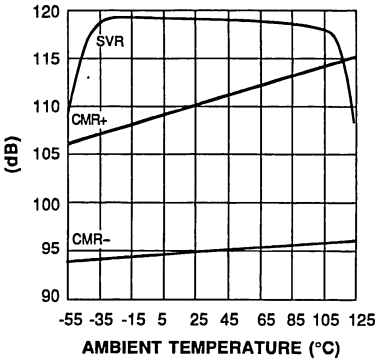
E88UA741-15

GAIN BANDWIDTH PRODUCT vs AMBIENT TEMPERATURE



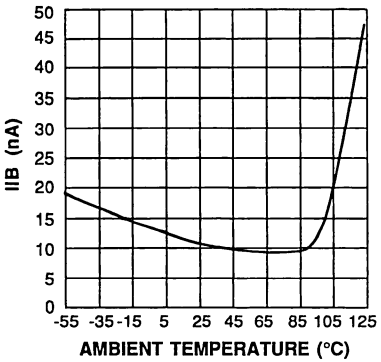
E88UA741-16

POWER SUPPLY & COMMON MODE REJECTION RATIO vs AMBIENT TEMPERATURE



E88UA741-17

INPUT BIAS CURRENT vs AMBIENT TEMPERATURE

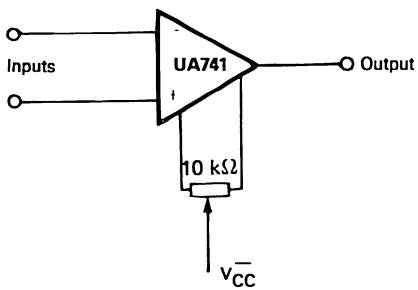


E88UA741-18

MEASUREMENT DIAGRAMS

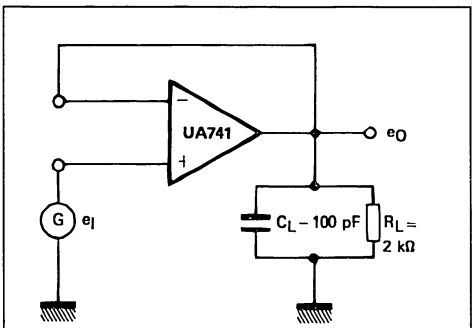
VOLTAGE OFFSET NULL CIRCUIT

TO99 – DIP8 – CERDIP8



E88UA741-19

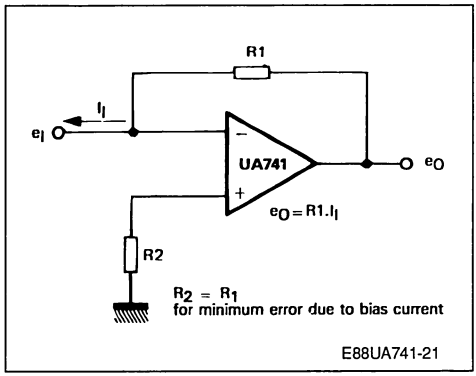
TRANSIENT RESPONSE TEST CIRCUIT



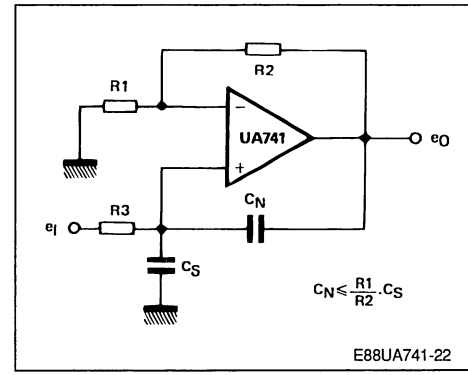
E88UA741-20

MEASUREMENT DIAGRAMS (continued)

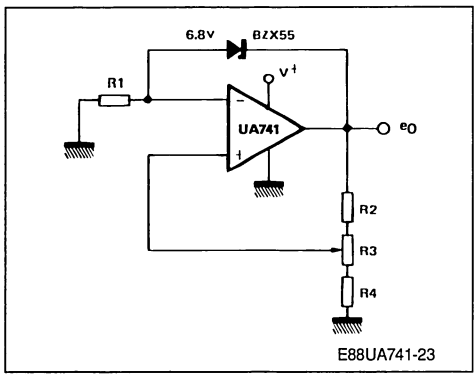
CURRENT TO VOLTAGE CONVERTER



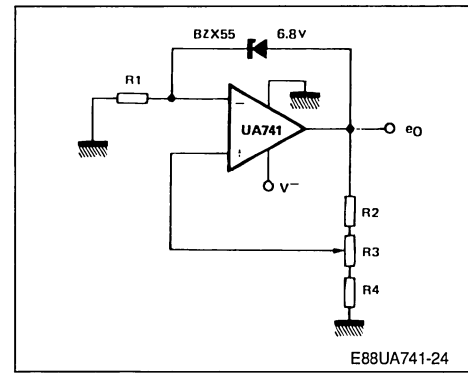
NEUTRALIZING INPUT CAPACITANCE TO OPTIMIZE RESPONSE TIME



POSITIVE VOLTAGE REFERENCE

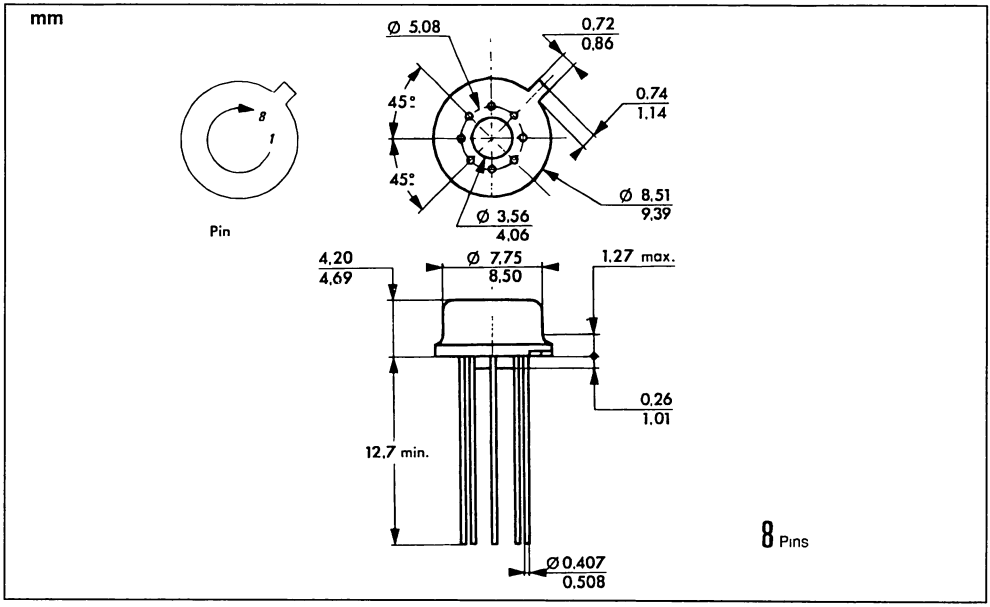


NEGATIVE VOLTAGE REFERENCE

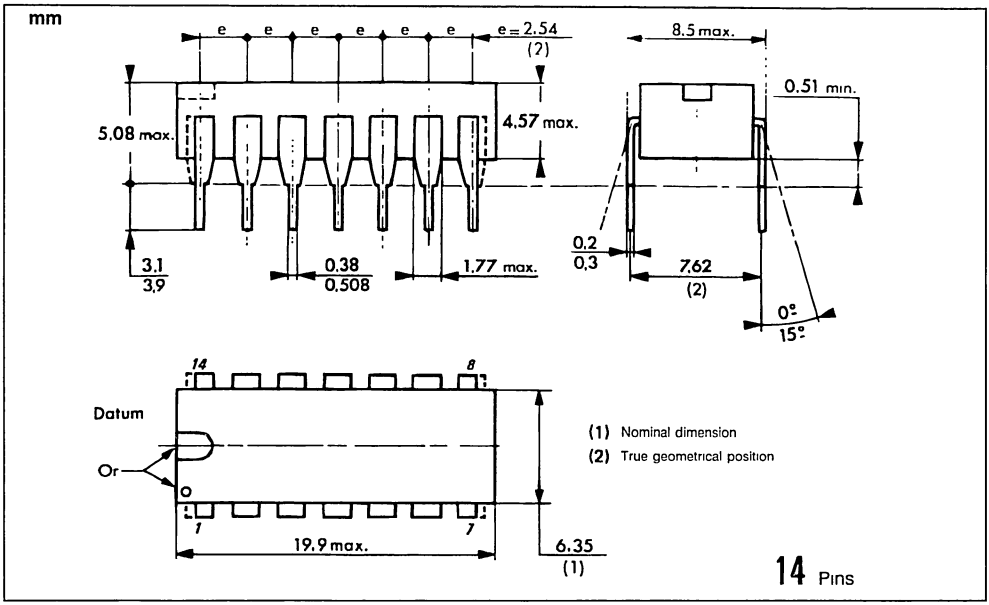


PACKAGE MECHANICAL DATA

8 PINS – TO99 – METAL CAN

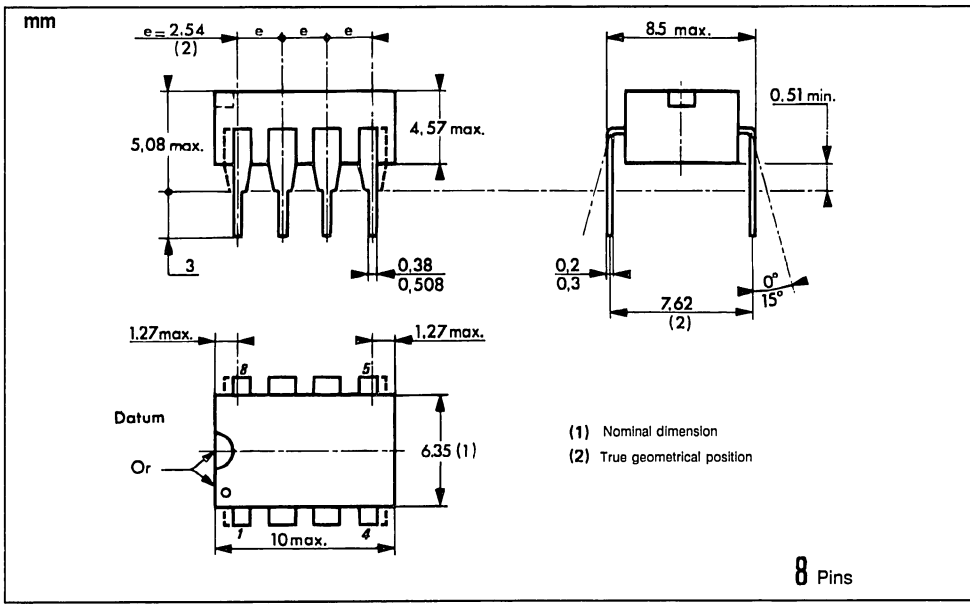


14 PINS – PLASTIC DIP

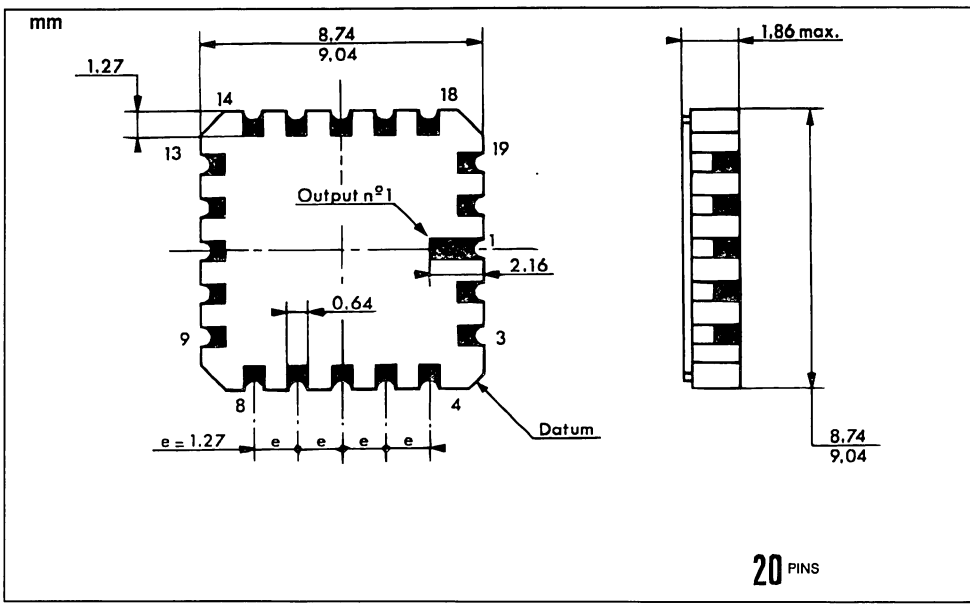


PACKAGE MECHANICAL DATA (continued)

8 PINS – PLASTIC DIP OR CERDIP

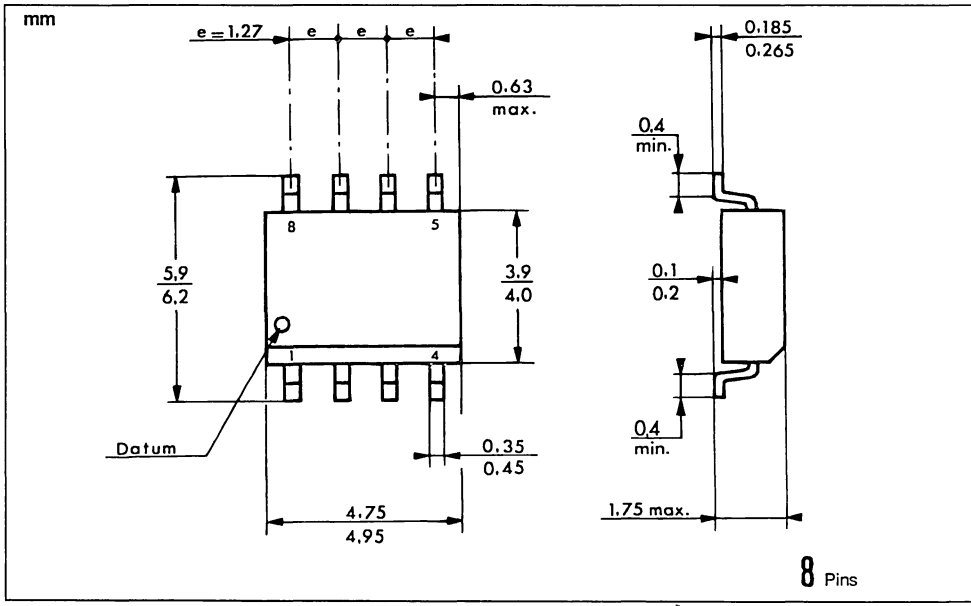


20 PINS – TRICECOP (LCC)



PACKAGE MECHANICAL DATA (continued)

8 PINS – PLASTIC MICROPACKAGE (SO)



SGS-THOMSON MICROELECTRONICS

UA748

GENERAL PURPOSE SINGLE OP-AMPs

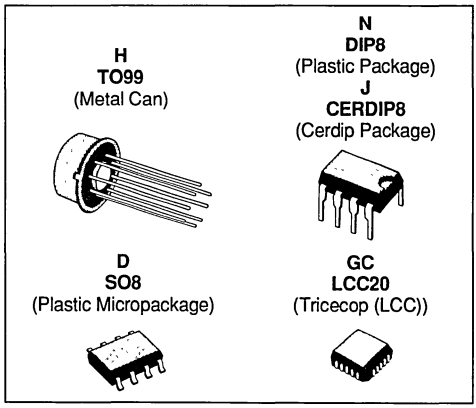
- FREQUENCY COMPENSATION WITH A SINGLE 30 pF CAPACITOR
- OPERATION FROM ± 5 V TO ± 15 V
- LOW POWER CONSUMPTION : 50 mW AT ± 15 V
- CONTINUOUS SHORT-CIRCUIT PROTECTION
- OPERATION AS A COMPARATOR WITH DIFFERENTIAL INPUTS AS HIGH AS ± 30 V
- NO LATCH-UP WHEN COMMON-MODE RANGE IS EXCEEDED
- SAME PIN CONFIGURATION AS THE LM101A

DESCRIPTION

The UA748 is a general-purpose operational amplifier built on a single silicon chip. The resulting close match and tight thermal coupling gives low offsets and temperature drift as well as fast recovery from thermal transients.

- Short-circuit protection.
- Offset voltage null capability.
- Large common-mode and differential voltage ranges.
- Low power consumption.
- No latch-up

The unity-gain compensation specified makes the circuit stable for all feedback configurations, even with capacitive loads. However, it is possible to optimize compensation for best high frequency performance at any gain. As a comparator the output can be clamped at any desired level to make it compatible with logic circuits. Further, the low power dissipation permits high voltage operation and simplifies packaging in full-temperature range systems.

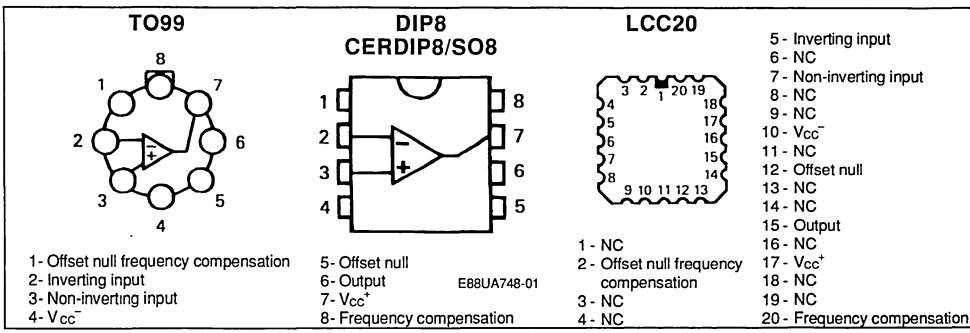


ORDER CODES

Part Number	Temperature Range	Package			
		H	N	GC	D
UA748C	0 °C to + 70 °C	•	•		•
UA748I	40 °C to + 105 °C	•	•		•
UA748M	– 55 °C to + 125 °C	•		•	

Note : Hi-rel Versions Available
Examples : UA748CH, UA748MGC

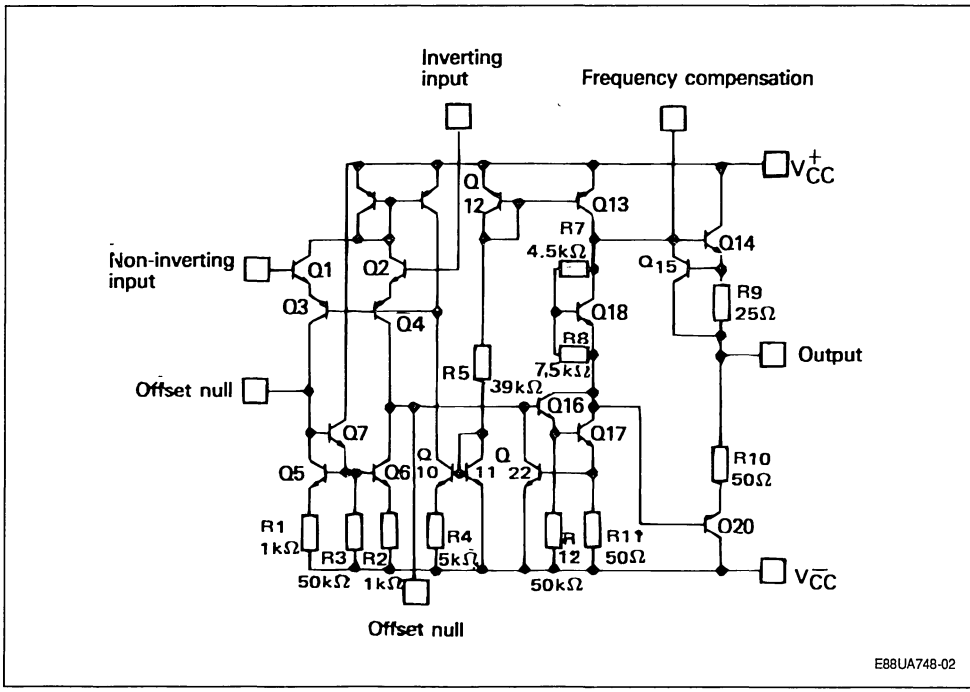
PIN CONNECTIONS (top views)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	UA748M	UA748I	UA748C	Unit
V_{CC}	Supply Voltage	± 22	± 22	± 22	V
V_I	Input Voltage	± 15	± 15	± 15	V
V_{ID}	Differential Input Voltage	± 30	± 30	± 30	V
P_{tot}	Power Dissipation GC Suffix	500 665	500	500 300	mW
	Output Short-circuit Duration	Infinite for T_{amb} = 70 °C		Infinite for T = 55 °C	
T_{oper}	Operating Free Air Temperature Range	– 55 to + 125	– 40 to + 105	0 to + 70	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	– 65 to + 150	– 65 to + 150	°C

SCHEMATIC DIAGRAM



Case	Offset Null	Non-inverting Input	Inverting Input	V_{CC}^-	V_{CC}^+	Output	Frequency Comp.	Off. Null. Freq. Comp.	N.C.
TO99 DIP8 CERDIP8 SO8	5	3	2	4	7	6	8	1	
LCC20 *	12	7	5	10	17	1	5	20	2

* **LCC20 :** Other pins are not connected.

ELECTRICAL CHARACTERISTICS

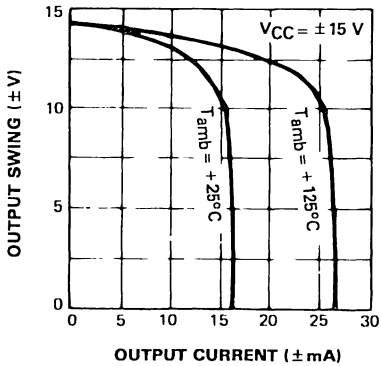
UA748C : 0 °C < T_{amb} < + 70 °C ± 5 V < V_{CC} < ± 20 V C1 = 30 pF
UA748I : – 40 °C < T_{amb} < + 105 °C ± 5 V < V_{CC} < ± 20 V C1 = 30 pF
UA748M : – 55 °C < T_{amb} < + 125 °C . ± 5 V < V_{CC} < ± 20 V C1 = 30 pF
* => V_{CC} = ± 15 V
(unless otherwise specified)

Symbol	Parameter	UA748M, I			UA748C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage $R_S \leq 10$ kΩ T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		0.2	1 3		2	5 6	mV
I_{IB}	Input Bias Current T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		25	75 100		70	100 200	nA
I_{IO}	Input Offset Current T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		1.5	10 20		2	20 40	nA
A_{VD}	Large Signal Voltage Gain * (V_O = ± 10 V, R_L = 2 kΩ) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 50 25	 100		 50 25	 100		V/mV
SVR	Supply Voltage Rejection Ratio (R_S < 10 kΩ) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 80 80	 96		 80 80	 96		dB
I_{CC}	Supply Current, no Load T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		1.8	3 3		1.8	3 3	mA
V_I	Input Voltage Range (V_{CC} = ± 20 V) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	– 15 – 15		+ 15 + 15	– 15 – 15		+ 15 + 15	V
CMR	Common-mode Rejection Ratio ($R_S \leq 10$ kΩ) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	80 80	96		80 80	96		dB
I_{OS}	Output Short-circuit Current * T_{amb} = 25 °C	10	30	50	10	30	50	mA
± V_{OPP}	Output Voltage Swing * T_{amb} = 25 °C R_L = 10 kΩ R_L = 2 kΩ $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 10 kΩ R_L = 2 kΩ	 12 10 12 10	 14 13		 12 10 12 10	 14 13		V
S_{VO}	Slew-rate (V_I = ± 10 V, R_L = 2 kΩ, $C_L \leq 100$ pF, T_{amb} = 25 °C, unity gain) *	0.25	0.5		0.25	0.5		V/µs
t_r	Rise Time * (V_I = ± 20 mV, R_L = 2 kΩ, $C_L \leq 100$ pF, T_{amb} = + 25 °C, unity gain)		0.3			0.3		µs
K_{OV}	Overshoot (V_I = 20 mV, R_L = 2 kΩ, $C_L \leq 100$ pF, T_{amb} = + 25 °C, unity gain)		5			5		%
Z_I	Input Impedance, T_{amb} = 25 °C *	1.5	4		1.5	4		MΩ
R_O	Output Resistance, T_{amb} = 25 °C *		75			75		Ω

ELECTRICAL CHARACTERISTICS (continued)

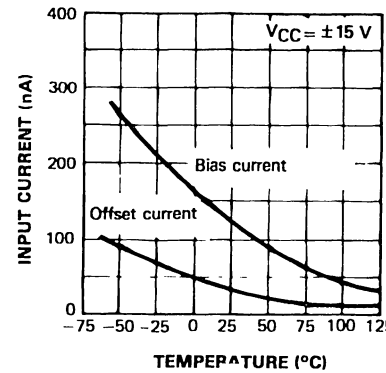
Symbol	Parameter	UA748M, I			UA748C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
GBP	Gain Bandwidth Product * (V_I = 10 mV, R_L = 2 kΩ, $C_L \leq$ 100 pF, f = 100 KHz, T_{amb} = 25 °C)	0.5	1	1.6	0.5	1	1.6	MHz
THD	Total Harmonic Distortion * (f = 1 KHz, A_V = 20 dB, R_L = 2 kΩ, V_O = 2 V_{PP}, $C_L \leq$ 100 pF, T_{amb} = 25 °C)		0.015			0.015		%
V_n	Equivalent Input Noise Voltage (f = 1 KHz, R_g = 100 Ω) *		25			25		nV/√Hz
DV_{IO}	Input Offset Voltage Drift $T_{min} \leq T_{amb} \leq T_{max}$		3	15		6	30	µV/°C
DI_{IO}	Input Offset Current Drift 25°C ≤ T_{amb} ≤ T_{max} $T_{min} \leq T_{amb}$ < 25°C		10 20	100 200		10 20	100 200	pA/°C

CURRENT LIMITING



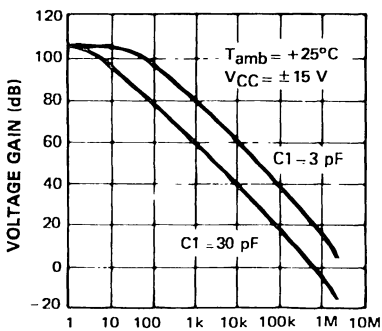
E88UA748-03

INPUT CURRENT



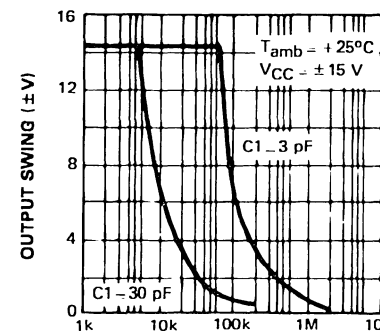
E88UA748-04

OPEN LOOP FREQUENCY RESPONSE



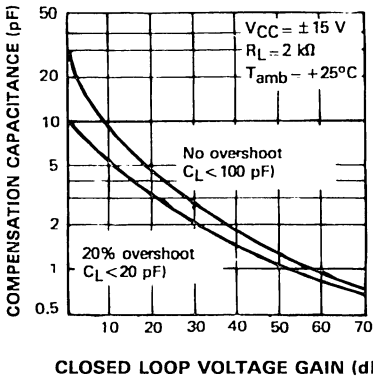
E88UA748-05

LARGE SIGNAL FREQUENCY RESPONSE



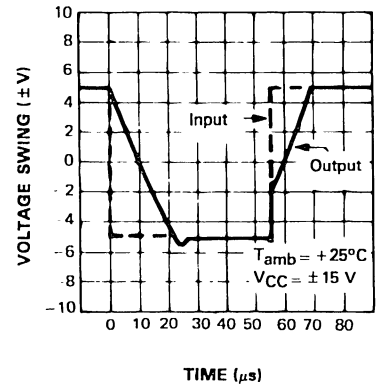
E88UA748-06

FREQUENCY COMPENSATION



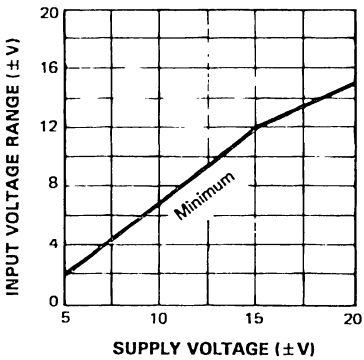
E88UA748-07

VOLTAGE FOLLOWER PULSE RESPONSE



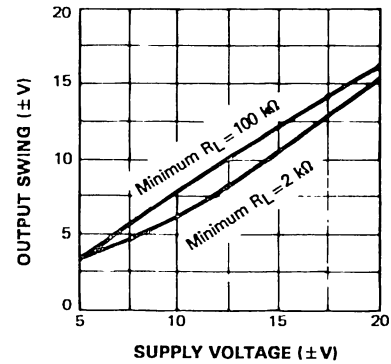
E88UA748-08

INPUT VOLTAGE RANGE



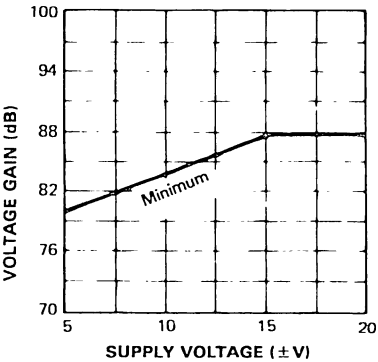
E88UA748-09

OUTPUT SWING



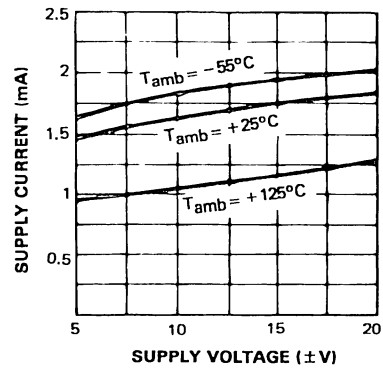
E88UA748-10

VOLTAGE GAIN



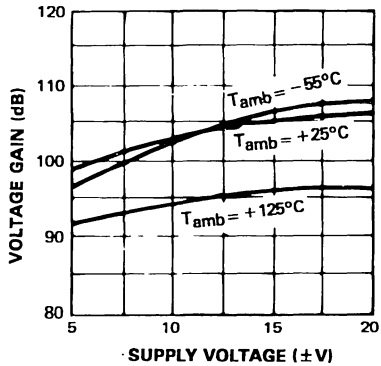
E88UA748-11

SUPPLY CURRENT



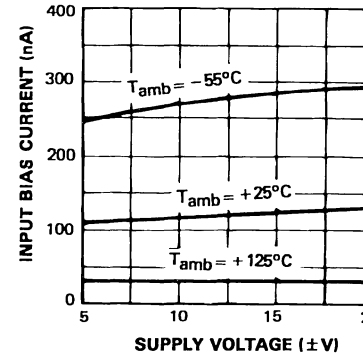
E88UA748-12

VOLTAGE GAIN



E88UA748-13

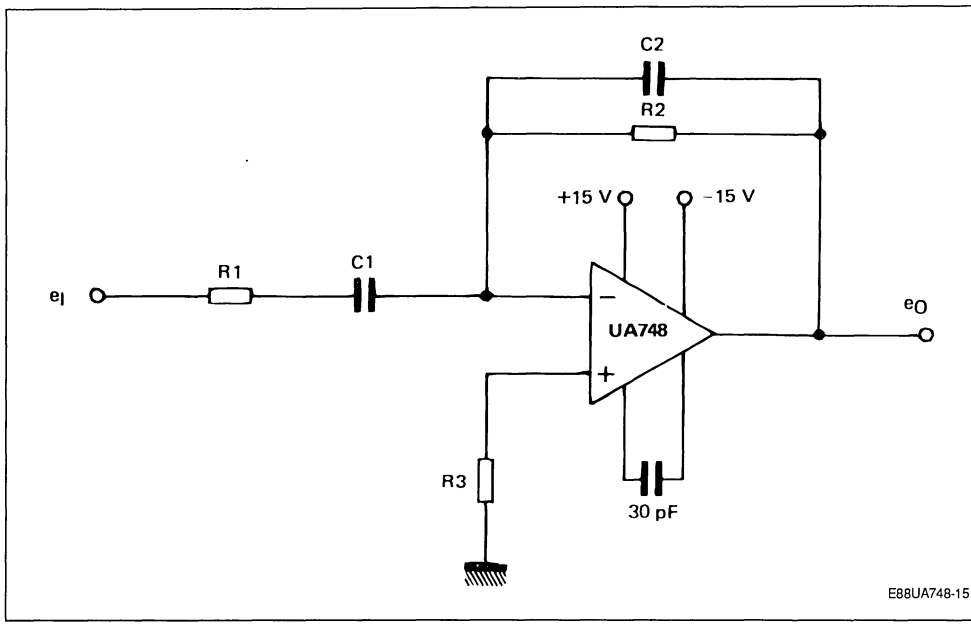
INPUT BIAS CURRENT



E88UA748-14

TYPICAL APPLICATIONS

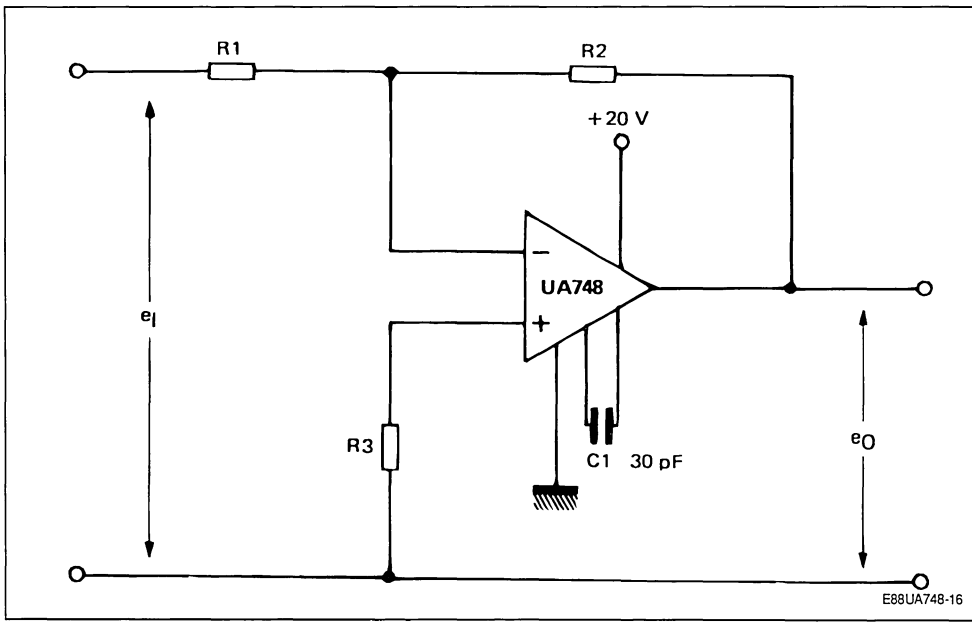
PRACTICAL DIFFERENTIATOR



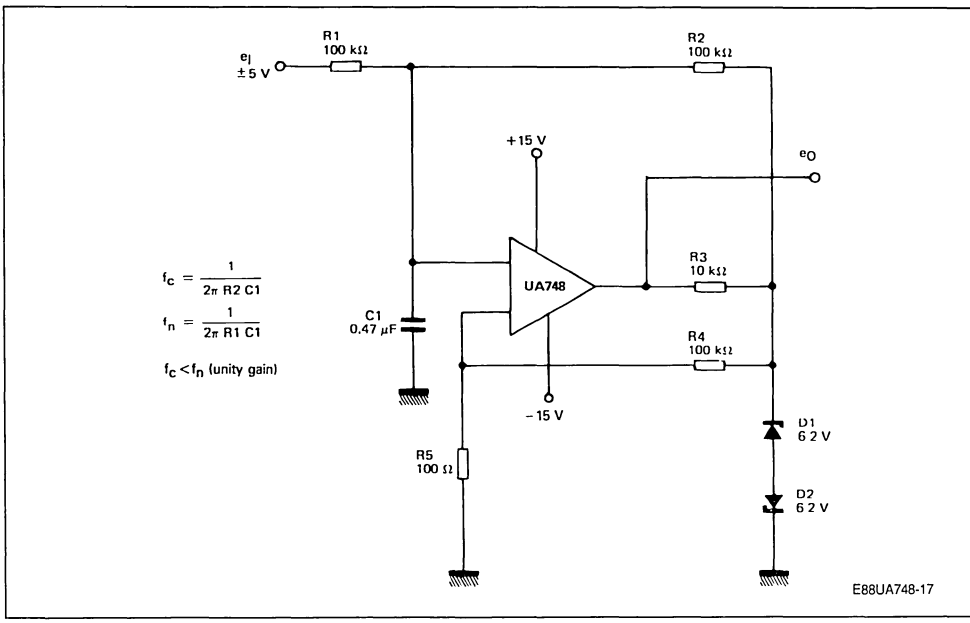
E88UA748-15

TYPICAL APPLICATIONS (continued)

SINGLE SUPPLY OPERATION

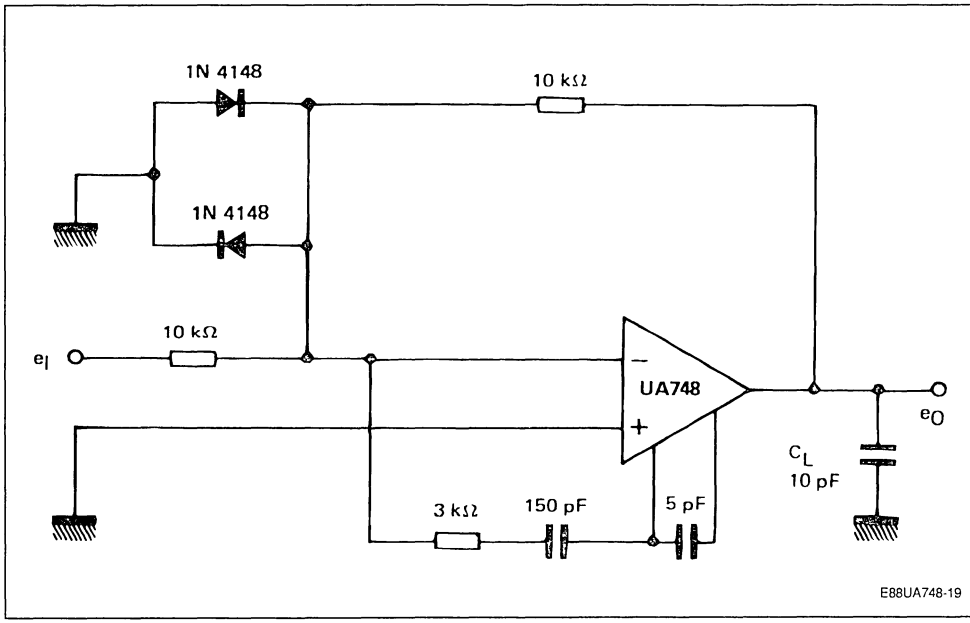


PULSE WIDTH MODULATOR

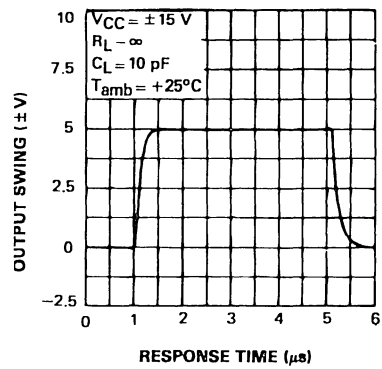


TYPICAL APPLICATIONS (continued)

FEED-FORWARD COMPENSATION



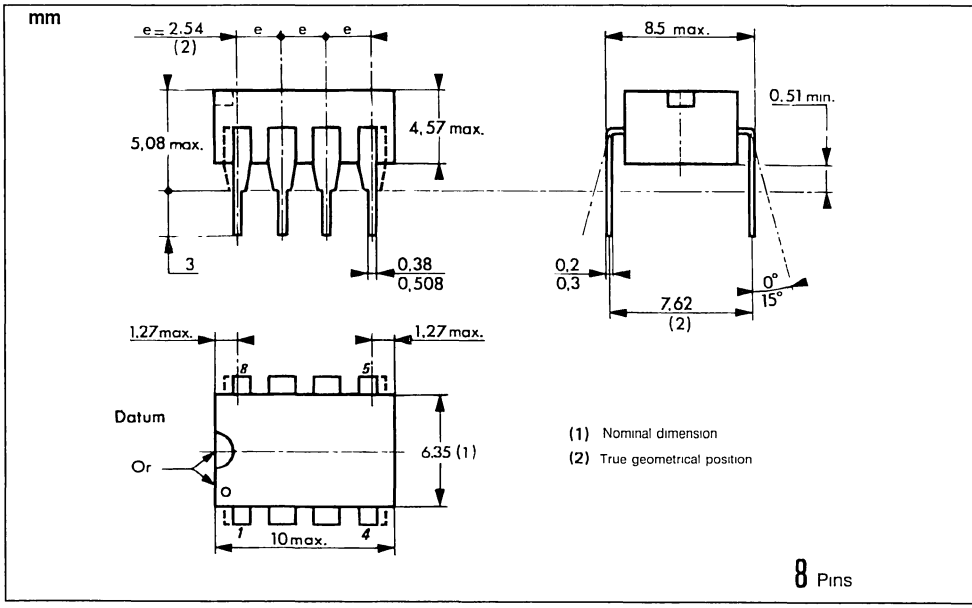
LARGE SIGNAL FEED-FORWARD TRANSIENT RESPONSE



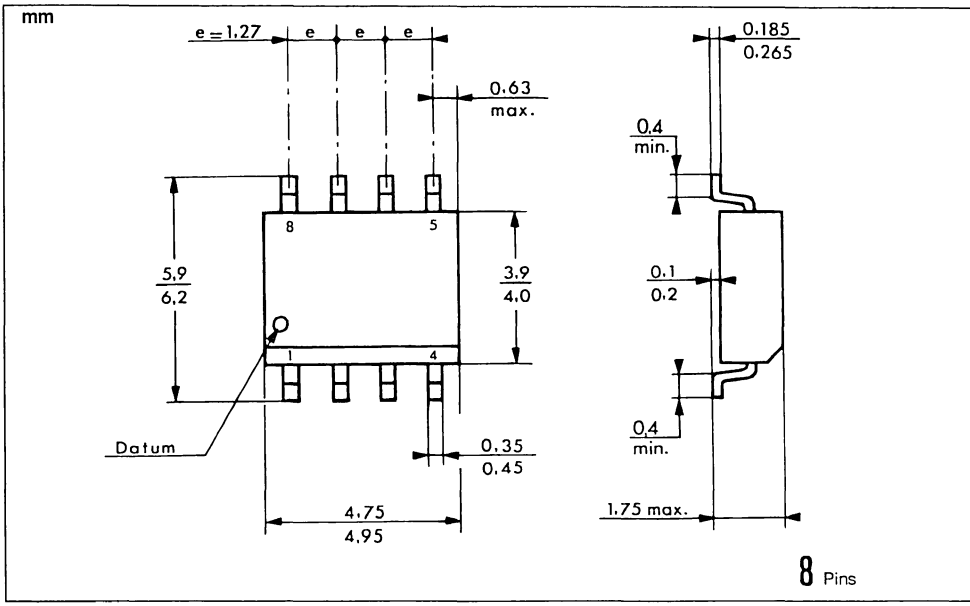
E88UA748-18

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP OR CERDIP

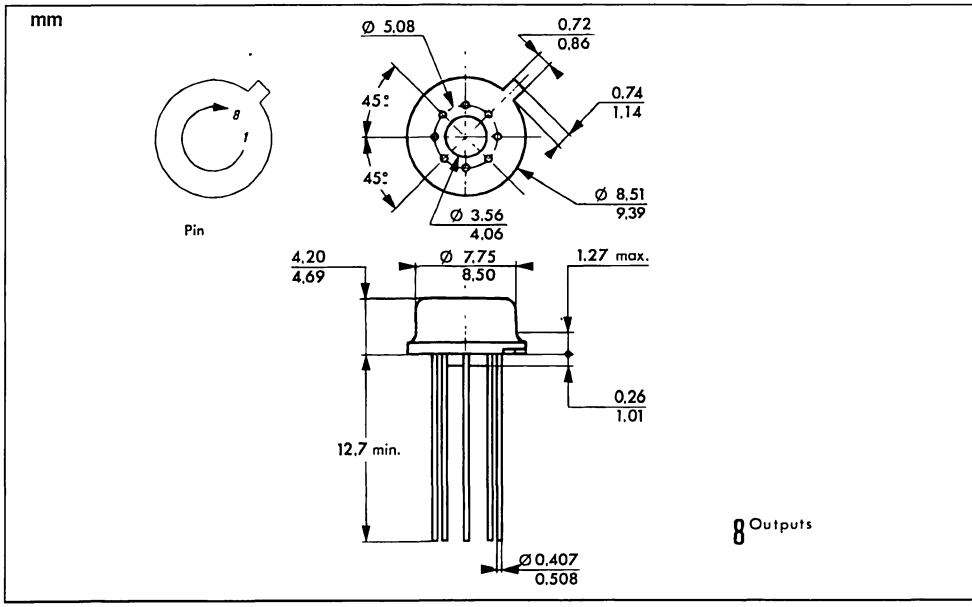


8 PINS - PLASTIC MICROPACKAGE (SO)

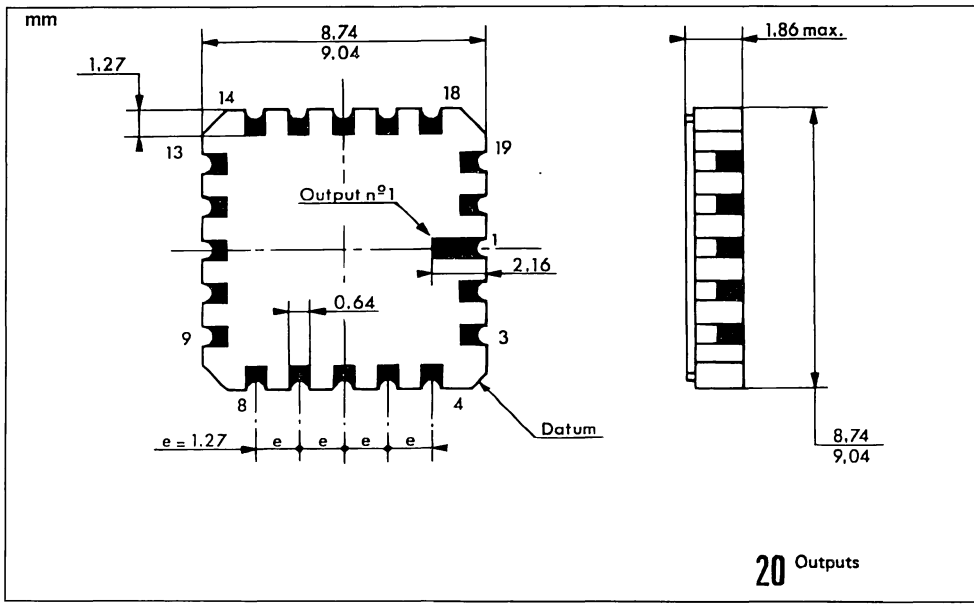


PACKAGE MECHANICAL DATA (continued)

8 PINS - METAL CAN TO99

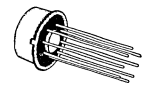


20 PINS - TRICECOP (LCC)



PROGRAMMABLE SINGLE OP-AMPs

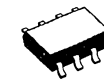
- MICROPOWER OPERATION
- NO FREQUENCY COMPENSATION REQUIRED
- WIDE PROGRAMMING RANGE
- HIGH SLEW RATE
- SHORT-CIRCUIT PROTECTION
- PROGRAMMABLE SINGLE OP-AMPs



H
TO99
(Metal Can)

N
DIP8
(Plastic Package)

GC
LCC20
(Tricecop (LCC))



D
SO8
(Plastic Micropackage)

DESCRIPTION

The UA776 programmable operational amplifier is characterized by high input impedance, low supply currents and low input noise over a wide range of operating supply voltages.

Coupled with programmable electrical characteristics it is an extremely versatile amplifier for use in high accuracy, low power consumption analog applications.

Input noise voltage and current, power consumption, and input current can be optimized by a single resistor or current source that sets the chip quiescent current for nano-watt power consumption or for characteristics similar to the UA741.

Internal frequency compensation, absence of latch up, high slew rate and short-circuit protection assure ease of use in long time integrators, active filters, and sample and hold circuits.

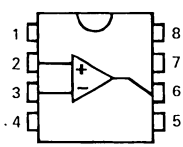
ORDER CODES

Part Number	Temperature Range	Package			
		H	N	GC	D
UA776C	0 to + 70 °C	•	•		•
UA776I	– 40 to + 105°C	•	•		•
UA776M	– 55 to + 125 °C	•		•	

Note . Hi-Rel Versions Available.
Examples : UA776CH, UA776CN, UA776CD

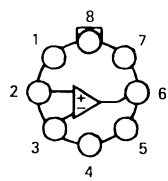
PIN CONNECTIONS (top views)

TO99



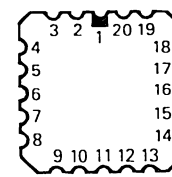
1 - Offset null
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-

DIP8
SO8



5 - Offset null
6 - Output
7 - V_{CC}^+
8 - I_{set}

LCC20



1 - NC
2 - Offset null
3 - NC
4 - NC
5 - Inverting input
6 - NC
7 - Non-inverting input
8 - NC
9 - NC
10 - V_{CC}^-
11 - NC
12 - Offset null
13 - NC
14 - NC
15 - Output
16 - NC
17 - V_{CC}^+
18 - NC
19 - NC
20 - I_{set}

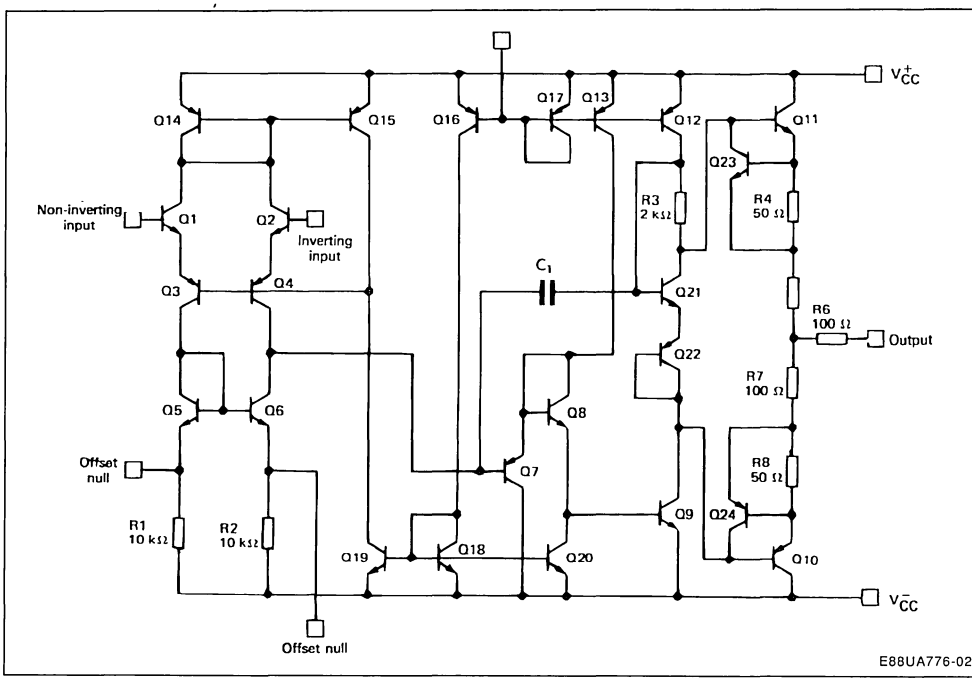
E88UA776-01

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	UA776M	UA776I	UA776C	Unit
V_{CC}	Supply Voltage	± 18	± 18	± 18	V
V_I	Input voltage	± 15	± 15	± 15	V
V_{ID}	Differential Input Voltage	± 30	± 30	± 30	V
P_{tot}	Power Dissipation UA776GC UA776CH	500 665	310 500	310 500	mW
	Output Short-circuit Duration	Indefinite			
T_{oper}	Operating Free Air Temperature Range	– 55 to + 125	– 40 to + 105	0 to + 70	°C
T_{stg}	Storage Temperature Range	– 65 to 150	– 65 to 150	– 65 to 150	°C

Notes : 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
2 Short-circuit may be to ground or either supply Rating applies to + 125 °C package temperature serial M or + 75 °C serial C ambient temperature for $I_{set} \leq 30\ \mu A$.

SCHEMATIC DIAGRAM



Case	Offset Null	Inverting Input	Non-inverting Input	Output	V_{CC}^-	V_{CC}^+	I_{set}
TO99/SO8 DIP8	1, 5	2	3	6	4	7	8
LCC20	2, 12	5	7	15	10	17	20

* **LCC20** : Other pins are not connected.

ELECTRICAL CHARACTERISTICS

$V_{CC}^{+} = \pm 15$ V (unless otherwise specified)

UA776C: $0 \leq T_{amb} \leq +70$ °C
UA776I : $-40 \leq T_{amb} \leq +105$ °C
UA776M: $-55 \leq T_{amb} \leq +125$ °C

Symbol	Parameter		I_{set} = 1.5 µA			I_{set} = 15 µA			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage								mV
	T_{amb} = 25 °C			2	5		2	5	
	$T_{min} \leq T_{amb} \leq T_{max}$				6			6	
I_{IO}	Input Offset Current								nA
	T_{amb} = 25 °C			0.7	3		2	15	
	$T_{min} \leq T_{amb} \leq T_{max}$				10			40	
I_{IB}	Input Bias Current								nA
	T_{amb} = 25 °C	UA776M		2	7.5		15	50	
		UA776I, C		2	10		15	50	
	$T_{min} \leq T_{amb} \leq T_{max}$				20			100	
A_{VD}	Large Signal Voltage Gain ($V_O = \pm 10$ V)								V/mV
	T_{amb} = 25 °C	R_L = 5 kΩ				100	400		
		R_L = 75 kΩ	200	400					
	$T_{min} \leq T_{amb} \leq T_{max}$	R_L = 75 kΩ	100						
		R_L = 5 kΩ				75			
SVR	Supply Voltage Rejection Ratio ($R_S \leq 10$ kΩ)								dB
	T_{amb} = 25 °C		77	92		77	92		
	$T_{min} \leq T_{amb} \leq T_{max}$		77			77			
I_{CC}	Supply Current, no Load								µA
	T_{amb} = 25 °C			20	25		160	180	
	$T_{min} \leq T_{amb} \leq T_{max}$				30			200	
V_I	Input Voltage Range								V
	T_{amb} = 25 °C		− 10		+ 10	− 10		+ 10	
CMR	Common Mode Rejection Ratio ($R_S \leq 10$ kΩ)								dB
	T_{amb} = 25 °C		70	90		70	90		
	$T_{min} \leq T_{amb} \leq T_{max}$		70			70			
I_{OS}	Output Short-circuit Current		0.5	3	15	6	12	30	mA
$\pm V_{OPP}$	Output Voltage Swing								V
	T_{amb} = 25 °C	RL ≥ 5 kΩ				10	13		
		$R_L \geq 75$ kΩ	12	14					
	$T_{min} \leq T_{amb} \leq T_{max}$	$R_L \geq 75$ kΩ	10			10			
V_{IOR}	Offset Voltage Adjustement Range			9			18		mV
S_{VO}	Slew-rate	($V_I = \pm 10$ V							V/µs
	$C_L \leq 100$pF, T_{amb} = 25 °C, unity gain)								
		R_L = 5 kΩ				0.2	0.8	2	
		R_L = 75 kΩ	0.01	0.1	1				

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	I_{set} = 1.5 µA			I_{set} = 15 µA			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_r	Rise Time (V_I = + 20 mV, $C_L \leq$ 100pF, T_{amb} = 25 °C, unity gain) R_L = 5 kΩ R_L = 75 kΩ		 1.6			 0.35		µs
K_{OV}	Overshoot Factor (V_I = ± 20 mV, C_L < 100 pF, T_{amb} = 25 °C, unity gain) R_L = 5 kΩ R_L = 75 kΩ		 0			 10		%
R_I	Input Resistance ,T_{amb} = 25 °C		50			5		MΩ
C_{ID}	Differential Input Capacitance		2			2		pF
R_O	Output Resistance, T_{amb} = 25 °C		5			1		kΩ
GBP	Gain Bandwidth Product (T_{amb} = 25 °C, C_L = 100 pF) f = 100 kHz R_L = 5 kΩ f = 10 kHz R_L = 75 kΩ	 0.03	 0.1	 0.5	 0.4	 0.7	 1.2	MHz
THD	Total Harmonic distorsion (f = 1 kHz, A_V = 20 dB, V_{opp} = 2 V_{pp} $C_L \leq$ 100 pF, T_{amb} = 25 °C R_L = 5 kΩ R_L = 75 kΩ		 0.8			 0.025		%
V_n	Equivalent Input Noise Voltage (f = 1 kHz)		20			20		nV/√Hz

ELECTRICAL CHARACTERISTICS

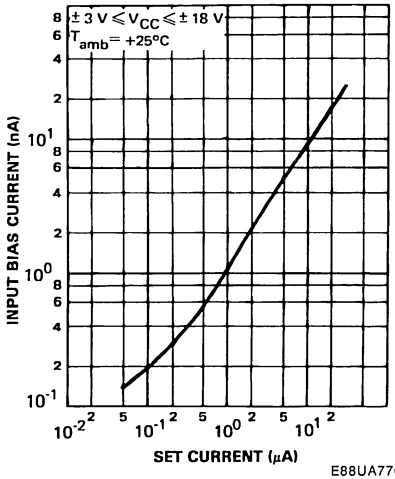
V_{CC}^+ = ± 3 V (unless otherwise specified)

Symbol	Parameter	I_{set} = 1.5 µA			I_{set} = 15 µA			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		2	5 6		2	5 6	mV
I_{IO}	Input Offset Current T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		0.7	3 10		2	15 40	nA
I_{IB}	Input Bias Current T_{amb} = 25 °C UA776M UA776I, C $T_{min} \leq T_{amb} \leq T_{max}$		2 2	7 10 20		15 15	50 50 100	nA
A_{VD}	Large Signal Voltage Gain (V_O = ± 10 V) T_{amb} = 25 °C R_L = 5 kΩ R_L = 75 kΩ $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 5 kΩ R_L = 75 kΩ	 50 25	 200		 50 25	 200		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S \leq$ 10 kΩ) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 77 77	 92		 77 77	 92		dB
I_{CC}	Supply Current, no Load T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		13	20 25		130	160 180	µA

ELECTRICAL CHARACTERISTICS (continued)

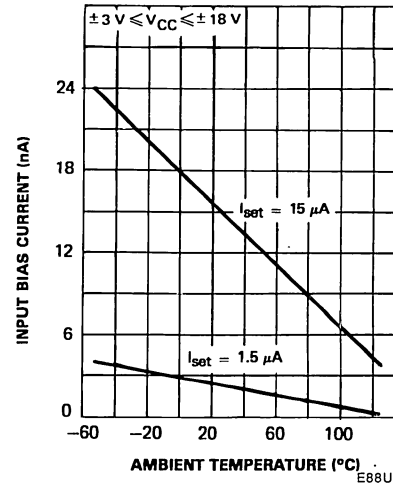
Symbol	Parameter	I_{set} = 1.5 µA			I_{set} = 15 µA			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_I	Input Voltage Range T_{amb} = 25 °C	− 1		+ 1	− 1		+ 1	V
CMR	Common Mode Rejection Ratio ($R_S \leq 10$ kΩ) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		70 70	90		70 70	90	dB
I_{OS}	Output Short-circuit Current	0.5	3	15	2	5	20	mA
V_{OPP}	Output Voltage Swing T_{amb} = 25 °C $R_L \geq 75$ kΩ RL ≥ 5 kΩ $T_{min} \leq T_{amb} \leq T_{max}$ $R_L \geq 75$ kΩ RL ≥ 5 kΩ	2 2	2.4		2 1.9 2 1.9	2.4 2.1		V
V_{IOR}	Offset Voltage Adjustement Range		9			18		mV
S_{VO}	Slew Rate (V_I = ± 10 V $C_L \leq$ 100pF, T_{amb} = 25 °C, unity gain) R_L = 5 kΩ R_L = 75 kΩ		 0.03			0.35		V/µs
t_r	Rise Time (V_I = + 20 mV, $C_L \leq$ 100pF, T_{amb} = 25 °C, unity gain) R_L = 5 kΩ R_L = 75 kΩ		 3			0.6		µs
K_{OV}	Overshoot (V_I = ± 20 mV, R_L = 2 kΩ $C_L \leq$ 100 pF, T_{amb} = 25 °C, unity gain) $R_L \geq$ 5 kΩ $R_L \geq$ 75 kΩ		 0			5		%
R_I	Input Resistance ,T_{amb} = 25 °C		50			5		MΩ
C_{ID}	Differential Input Capacitance		2			2		pF
R_O	Output Resistance, T_{amb} = 25 °C		5			1		kΩ
GBP	Gain Bandwidth Product (T_{amb} = 25 °C, C_L = 100 pF) f = 100 kHz R_L = 5 kΩ f = 10 kHz R_L = 75 kΩ		 0.075			0.5		MHz
THD	Total Harmonic distortion (f = 1 kHz, A_v = 20 dB , R_L = 2 kΩ C_L < 100 pF, T_{amb} = 25 °C, V_{opp} = 1 V_{pp} R_L = 5 kΩ R_L = 75 kΩ		 1			0.03		%
V_n	Equivalent Input Noise Voltage (f = 1 kHz)		20			20		nV/√Hz

INPUT BIAS CURRENT



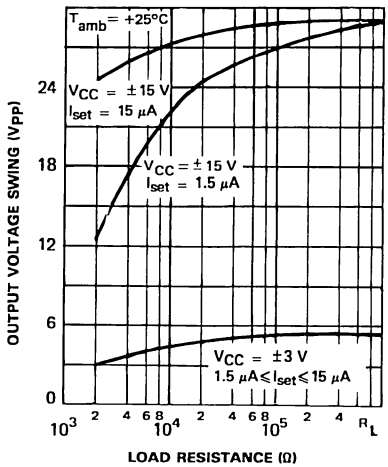
E88UA776-03

INPUT BIAS CURRENT



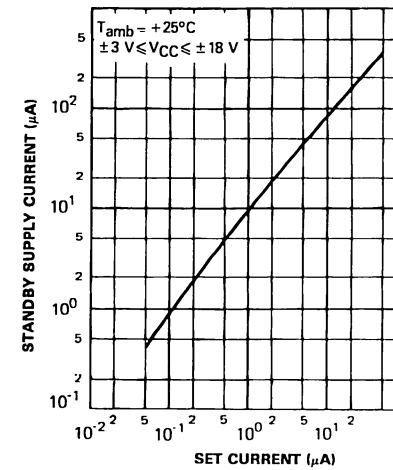
E88UA776-04

OUTPUT VOLTAGE SWING



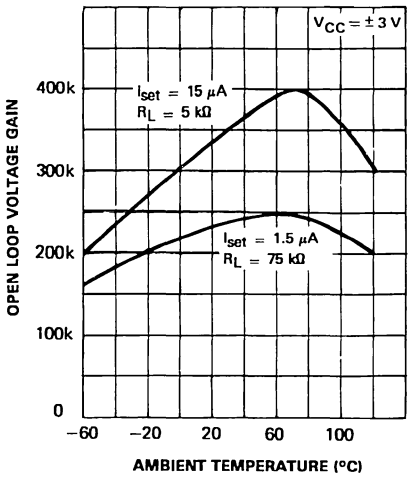
E88UA776-05

STANDBY SUPPLY CURRENT VERSUS SET CURRENT



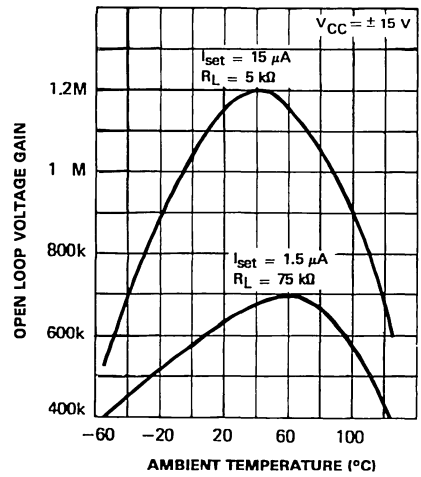
E88UA776-06

OPEN LOOP VOLTAGE GAIN



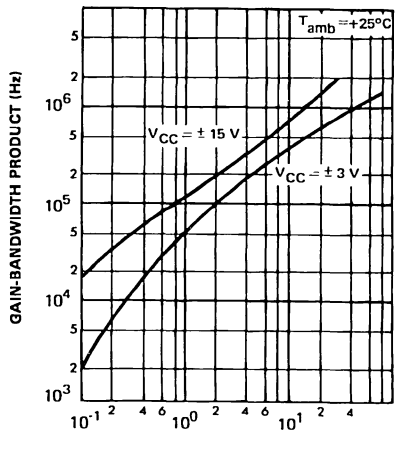
E88UA776-07

OPEN LOOP VOLTAGE GAIN



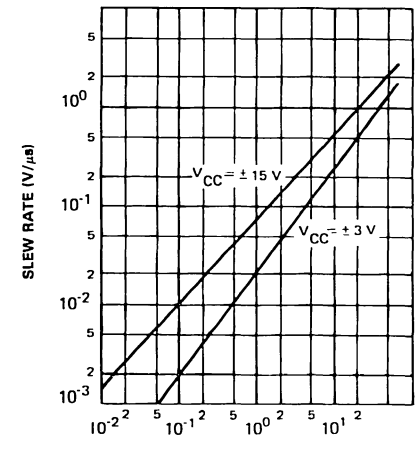
E88UA776-08

GAIN-BANDWIDTH



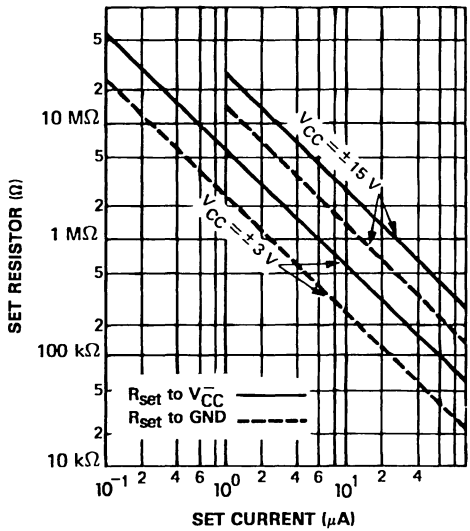
E88UA776-09

SLEW RATE



E88UA776-10

SET RESISTOR vs SET CURRENT



I_{set} EQUATIONS

$$I_{set} = \frac{V_{CC}^+ - 0.7 - V_{CC}^-}{R_{set}}$$

when R_{set} is connected to V_{CC}^-.

$$I_{set} = \frac{V_{CC}^+ - 0.7}{R_{set}}$$

when R_{set} is connected to ground.

E88UA776-11

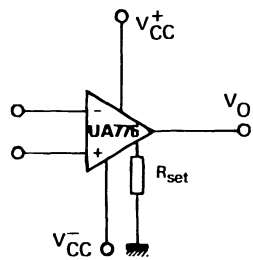
QUIESCENT CURRENT SETTLING RESISTOR (I_{set} to V_{CC}^-)

V_{CC}	I_{set}	
	1.5 μA	15 μA
± 1.5 V	1.7 MΩ	170 kΩ
± 3 V	3.6 MΩ	360 kΩ
± 6 V	7.5 MΩ	750 kΩ
± 15 V	20 MΩ	2 MΩ

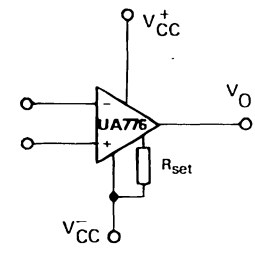
Note : The UA776 may be operated with Rset connected to ground or V_{CC}^-.

BIASING CIRCUITS

RESISTOR BIASING



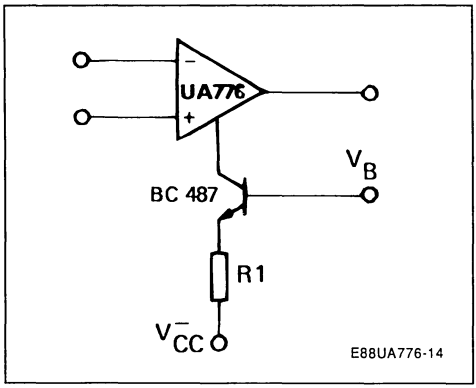
R_{set} connected to ground. E88UA776-12



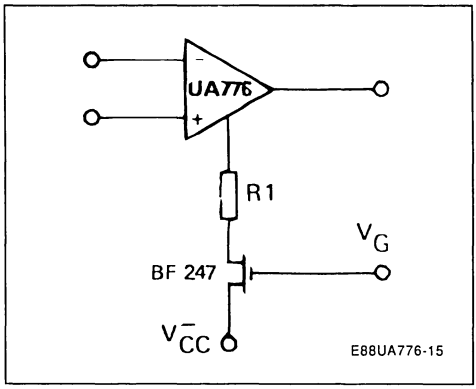
R_{set} connected to V_{CC}^-
Recommended for : $V_{CC} \leq \pm 6$ V E88UA776-13

BIASING CIRCUITS (continued)

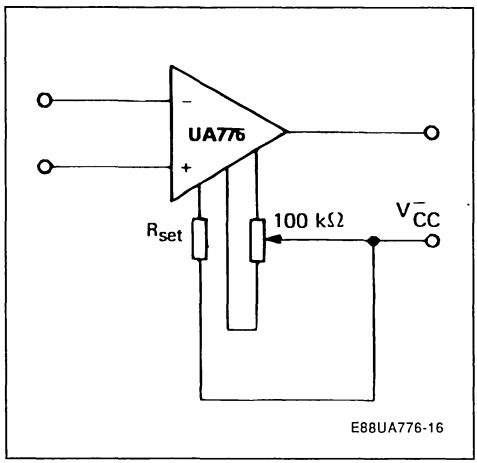
TRANSISTOR CURRENT SOURCE BIASING



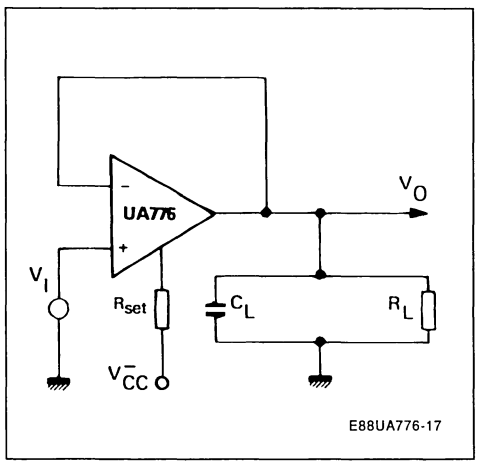
FET CURRENT SOURCE BIASING



VOLTAGE OFFSET NULL CIRCUIT

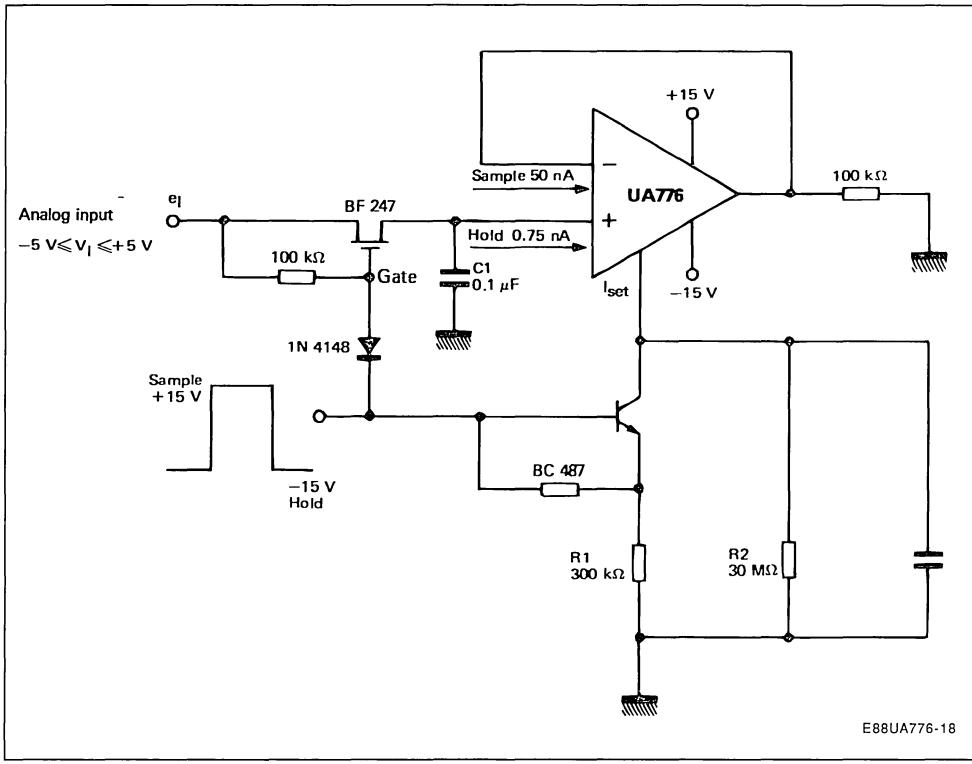


TRANSIENT RESPONSE TIME TEST CIRCUIT

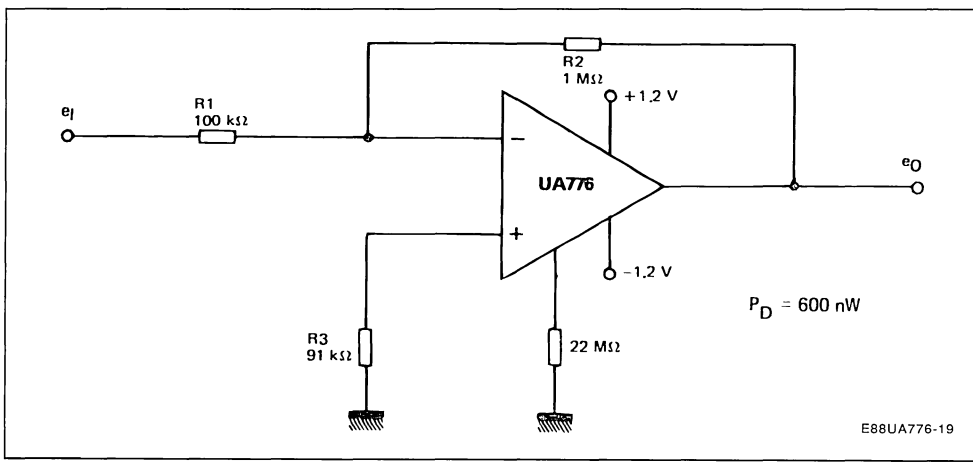


TYPICAL APPLICATIONS

HIGH ACCURACY SAMPLE AND HOLD

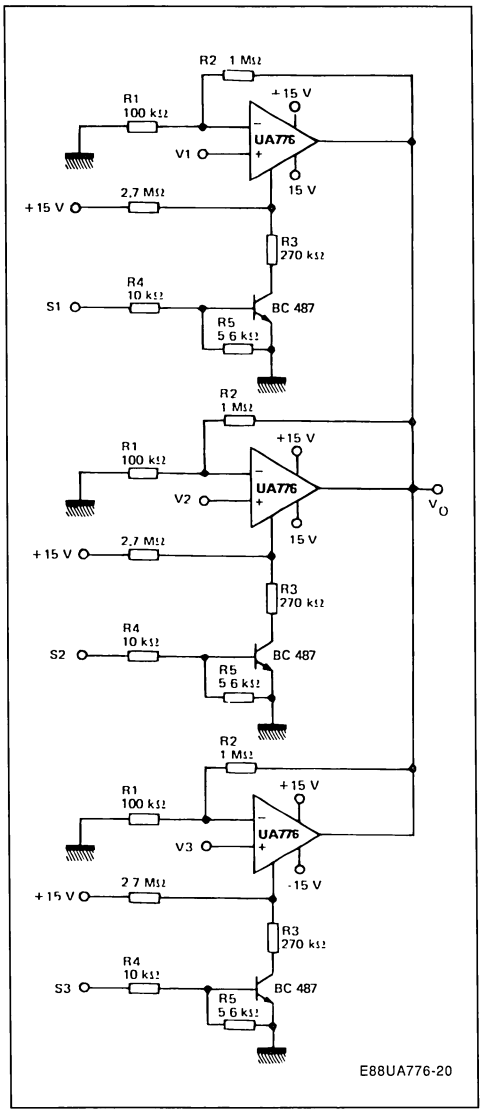


NANO-WATT AMPLIFIER

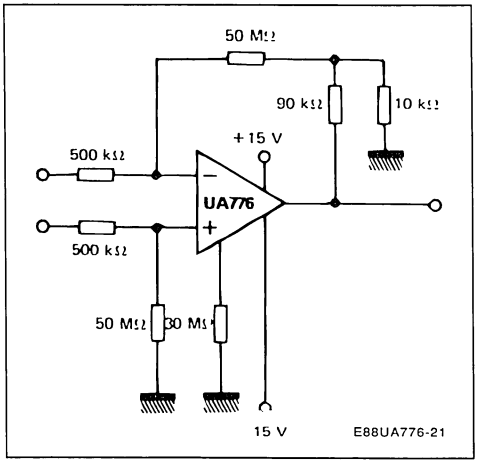


TYPICAL APPLICATIONS (continued)

MULTIPLEXING AND SIGNAL CONDITIONING WITHOUT FETs

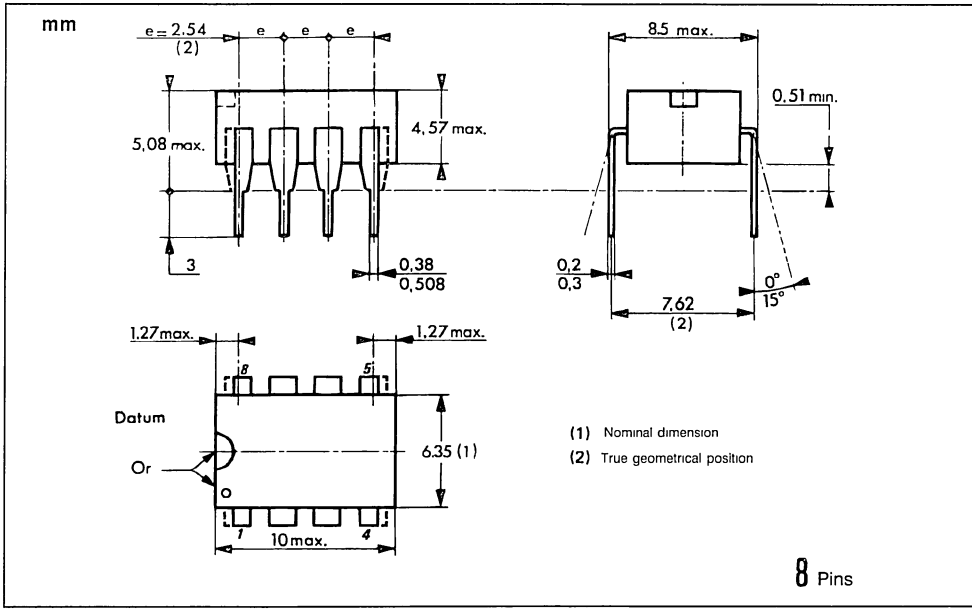


HIGH INPUT IMPEDANCE AMPLIFIER

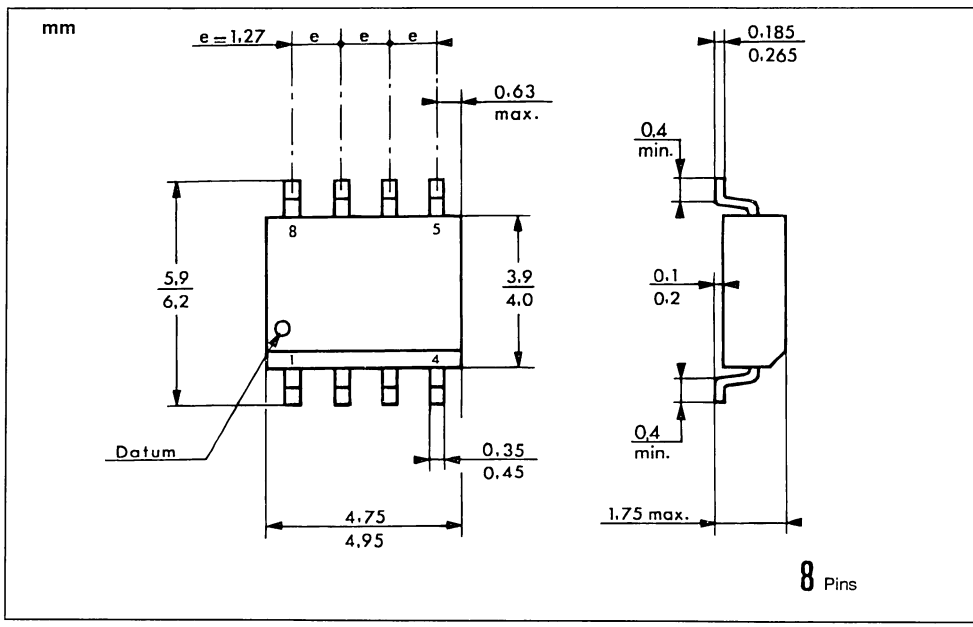


PACKAGE MECHANICAL DATA

8 PINS – PLASTIC DIP OR CERDIP

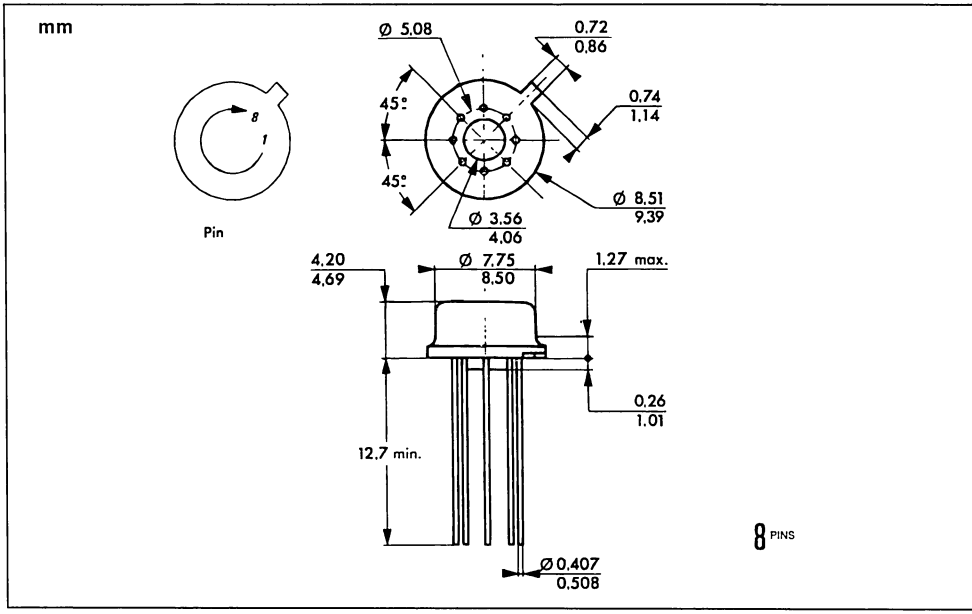


8 PINS – PLASTIC MICROPACKAGE (SO)

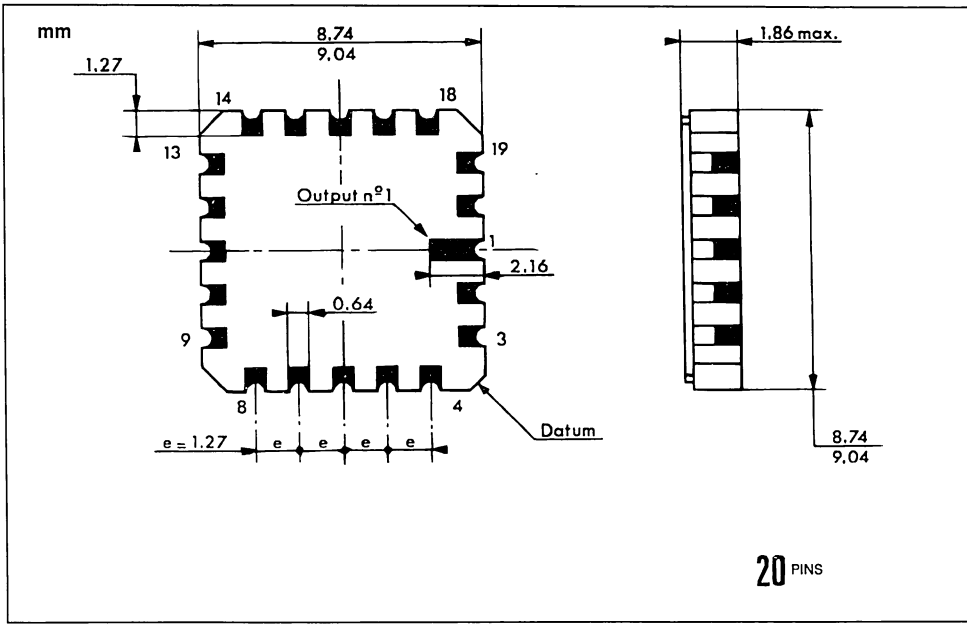


PACKAGE MECHANICAL DATA (continued)

8 PINS – METAL CAN TO99

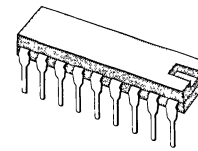


20 PINS – TRICECOP (LCC)



PROGRAMMABLE, OFF-LINE, PWM CONTROLLER

- ALL CONTROL, DRIVING, MONITORING, AND PROTECTION FUNCTIONS INCLUDED
- LOW-CURRENT, OFF-LINE START CIRCUIT
- FEED-FORWARD LINE REGULATION OVER 4 TO 1 INPUT RANGE
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- PULSE-BY-PULSE CURRENT LIMITING PLUS SHUTDOWN FOR OVER-CURRENT FAULT
- NO START-UP OR SHUTDOWN TRANSIENTS
- SLOW TURN-ON AND MAXIMUM DUTY-CYCLE CLAMP
- SHUTDOWN UPON OVER-OR UNDERVOLTAGE SENSING
- LATCH OFF OR CONTINUOUS RETRY AFTER FAULT
- REMOTE, PULSE-COMMANDABLE START/STOP
- PWM OUTPUT SWITCH USABLE TO 1A PEAK CURRENT
- 1% REFERENCE ACCURACY
- 500 kHz OPERATION



DIP-18
(Plastic and Ceramic)

DESCRIPTION

Although containing most of the features required by all types of switching power supply controllers, the UC1840 family has been optimized for highly-efficient boot-strapped primaryside operation in forward or flyback power converters. Two important features for this mode are a starting circuit which requires little current from the primary input voltage and feed-forward control for constant volt-second operation over a wide input voltage range.

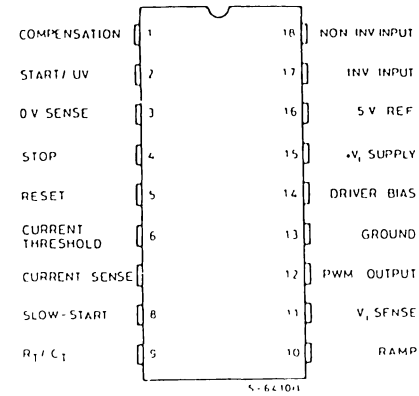
In addition to startup and normal regulating PWM functions, these devices ofter built-in protection from over-voltage, under-voltage, and over-current fault conditions. This monitoring circuitry contains the added features that any fault will initiate a complete shutdown with provisions for either latch off or automatic restart. In the latch-off mode, the controller may be started and stopped with external pulsed or steady-state commands.

Other performance features of these devices include a 1% accurate reference, provision for slow-turn-on and duty-cycle limiting, and highspeed pulse-by-pulse current limiting in addition to current fault shutdown.

The UC1840's PWM output stage includes a latch to insure only a single pulse per period and is designed to optimize the turn off of an external switching device by conducting during the "OFF" time with a capability for both high peak current and low saturation voltage. These devices are available in an 18-pin dual-in-line plastic or ceramic package.

The UC1840 is characterized for operation over the full military temperature range of –55°C to +125°C. The UC2840 and UC3840 are designed for operation from –25°C to +85°C and 0°C to +70°C, respectively.

PIN CONNECTION AND ORDER CODES



Type	Plastic	Ceramic
UC1840	–	UC1840J
UC2840	UC2840N	UC2840J
UC3840	UC3840N	UC3840J

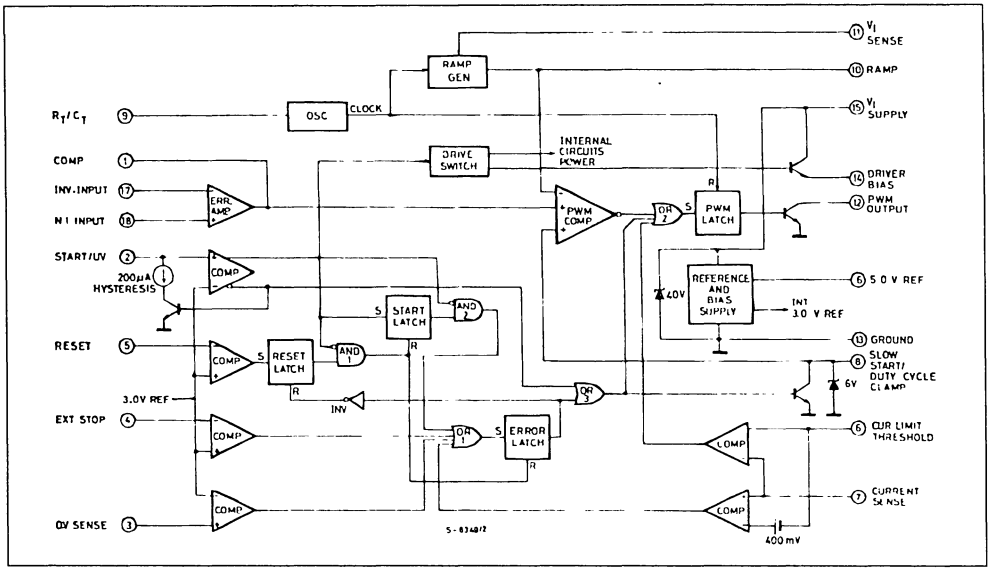
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_i	Supply Voltage + V_i (pin 15) Voltage Driven Current Driven 100 mA Maximum	 32 Self Limiting	 V
V_o	PWM Output Volage (pin 12)	40	V
I_o	PWM Output Current, Steady-state (pin 12)	400	mA
E_{op}	PWM Output Peak Energy Discharge Driver Bias Current (pin 14)	20 –200	µJ mA
$I_{o(REF)}$	Reference Output Current (pin 16) Slow Start Sink Current (pin 8) V_i Sense Current (pin 11) Current Limit Inputs (pins 6, 7) Comparator Inputs (pins 2, 3, 4, 5, 17, 18)	– 50 20 10 – 0.5 to + 55 – 0.3 to + 32	mA mA mA V V
P_{tot}	Power Dissipation at T_{amb} = 70 °C	1000	mW
T_j	Junction Temperature Range	– 55 to + 150	°C
T_{op}	Operating Ambient Temperature Range : UC1840 UC2840 UC3840	– 55 to + 125 – 25 to + 85 0 to + 70	°C °C °C
T_{stg}	Storage Temperature	– 65 to + 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Name	Function

PWM CONTROL

OSCILLATOR	Generates a fixed-frequency internal clock from an external R_T and C_T. Frequency = $\frac{K_c}{R_T C_T}$ where K_c is a first-order correction factor ~ 0.3 log (C_T x 10^{12}).
RAMP GENERATOR	Develops a linear ramp with a slope defined externally by $\frac{dv}{dt} = \frac{\text{sense voltage}}{R_R C_R}$. C_R is normally selected ≤ C_T and its value will have some effect upon valley voltage C_R terminal can be used as an input port for current mode control
ERROR AMPLIFIER	Conventional operational amplifier for closed-loop gain and phase compensation Low output impedance . unity-gain stable
REFERENCE GENERATOR	Precision 5 0 V for internal and external usage to 50 mA. Tracking 3.0 V reference for internal usage only with nominal accuracy of ± 2 % 40 V clamp zener for chip 0. V. protection, 100 mA maximum current.
PWM COMPARATOR	Generates output pulse wich starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs
PWM LATCH	Terminates the PWM output pulse when set by inputs for either the PWM comparator, the pulse-by-pulse current limit comparator, or the error latch. Resets wich each internal clock pulse
PWM OUTPUT SWITCH	Transistor capable of sinking current to ground wich is off during the PWM on-time and turns on to terminate the power pulse Current capacity is 400 mA saturated with peak capacitance discharge in excess of one amp

FUNCTIONAL DESCRIPTION (continued)

Name	Function

SEQUENCING FUNCTIONS

START/U. V. SENSE	This comparator performs three functions. With an increasing voltage, it generates a turn-on signal at a start threshold With a decreasing voltage, it generates a U. V. fault signal at a lower level separated by a 200 µA hysteresis current. At the U. V. threshold, it also resets the Error Latch if the Reset Latch has been set.
DRIVE SWITCH	Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold.
DRIVE BIAS	Supplies drive current to external power switch to provide turn-on bias.
SLOW START	Clamps low to hold PWM OFF Upon release, rises with rate controlled by R_SC_S for slow increase of output pulse width. Also used to clamp maximum duty cycle with divider R_S R_{DC}.
START LATCH	Keeps low input voltage at initial turn-on from being defined as a U. V. fault. Sets at start level to monitor for U V. fault.
RESET LATCH	When reset, this latch insures no reset signal to either Start or Error latches so that first fault will lock the PWM off. When set, this latch resets the Start and Error latches at the U. V. low threshold, allowing a restart.

PROTECTION FUNCTIONS

ERROR LATCH	When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are : a. U. V. low (after turn-on) b. O. V. high c. Step low d. Current Sense 400 mV over threshold Error Latch resets at U. V. threshold if Reset Latch is set.
CURRENT LIMITING	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400 mV above threshold, a shutdown signal it sent to Error Latch.

ELECTRICAL CHARACTERISTICS (refer to the test circuit. Unless otherwise stated, these specifications apply for T_j = – 55 to + 125 °C for the UC1840, – 25 °C to + 85 °C for the UC2840 and 0 to + 70 °C for the UC3840; V_i = 20 V, R_T = 20 KΩ, C_T = 0.001μF, C_R = 0.001 μF, current limit threshold = 200 mV)

Symbol	Parameter	Test Conditions	UC1840 UC2840			UC3840			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
POWER INPUTS									
I_{ST}	Start-up Current	V_i = 30 V, Pin 2 = 2.5 V, T_j = 25 °C		4	5.5		4	5.5	mA
	*Start-up Current T.C.	V_i = 30 V, Pin 2 = 2.5 V		– 0.1	– 0.2		– 0.1	– 0.2	%/°C
I_i	Operating Current	V_i = 30 V, Pin 2 = 3.5 V	5	10	15	5	10	15	mA
V_{SOV}	Supply O.V. Clamp	I_i = 20 m A	33	40	45	33	40	48	V
REFERENCE SECTION									
V_{REF}	Reference Voltage	T_j = 25 °C	4.95	5	5.05	4.9	5	5.1	V
ΔV_{REF}	Line Regulation	V_i = 8 to 30 V		10	15		10	20	mV
ΔV_{REF}	Load Regulation	I_L = 0 to 20mA		10	20		10	30	mV
$\Delta V_{REF}/\Delta T$*	Temperature Coeff.	Over Op. Temp. Range			± 0.4			± 0.4	mV/°C
I_{SC}	Short Circuit Curr.	V_{REF} = 0, T_j = 25 °C		– 80	– 100		– 80	– 100	mA
OSCILLATOR									
f_s	Nominal Frequency	T_j = 25 °C	47	50	53	45	50	55	KHz
	Voltage Stability	V_i = 8 to 30 V		0.5	1		0.5	1	%
	*Temperature Coeff.	Over Op. Temp. Range			± 0.8			± 0.8	%/°C
$f_{s(max)}$	Maxim. Frequency	R_T = 2 KΩ, C_T = 330 pF	500			500			KHz
RAMP GENERATOR									
	Ramp Current Min.	I_{SENSE} = – 10 μA		– 11	– 14		– 11	–14	μA
	Ramp Current Max.	I_{SENSE} = 1 mA	– 0.9	– 0.95		–0.9	–0.95		mA
	Ramp Valley		0.3	0.5	0.7	0.3	0.5	0.7	V
	Ramp Peak	Clamping Level	3.9	4.2	4.5	3.9	4.2	4.5	V

ELECTRICAL CHARACTERISTICS (continued)

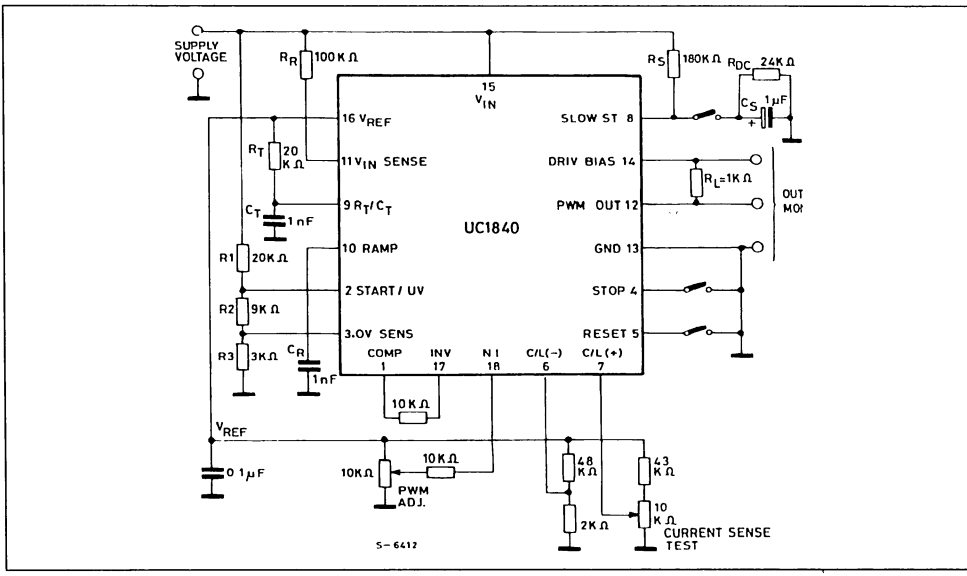
Symbol	Parameter	Test Conditions	UC1840 UC2840			UC3840			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
ERROR AMPLIFIER									
V_{os}	Input Offset Voltage	V_{CM} = 5 V		0.5	5		2	10	mV
I_b	Input Bias Current			0.5	2		1	5	µA
I_{os}	Input Offset Current				0.5			0.5	µA
G_v	Open Loop Gain	ΔV_o = 1 to 3 V	60	66		60	66		dB
	Output Swing (max Out ≤ Ramp Peak – 100 mV)	Minimum Total Range	0.3		3.5	0.3		3.5	V
CMR	Common Mode Rejection	V_{CM} = 1.5 to 5.5 V	70	80		70	80		dB
SVR	Supply Voltage Rejection	V_i = 8 to 30 V	40	50		40	50		dB
I_{SC}	Short Circuit Current	V_{comp} = 0V		– 4	– 10		– 4	– 10	mA
B*	Gain Bandwidth	T_j = 25 °C, G_V = 0 dB	1	2		1	2		MHz
SR*	Slew Rate	T_j = 25 °C, G_V = 0 dB		0.8			0.8		V/µs
PWM SECTION									
	*Continuous Duty Cycle Range (other than zero)	Min. Total Cont. Range Ramp Peak < 4.2 V	5		95	5		95	%
$V_{o(sat)}$	Output Saturation	I_o = 20 mA		0.2	0.4		0 2	0.4	V
$V_{o(sat)}$	Output Saturation	I_o = 200 mA		1.7	2.2		1.7	2.2	V
I_{OL}	Output Leakage	V_o = 40 V		0.1	10		0.1	10	µA
τ_d	*Comparator Delay	Pin 8 to pin 12 T_j = 25 °C, R_l = 1 KΩ		300	500		300	500	ns
SEQUENCING FUNCTIONS									
V_T	Comparator Threshold	Pins 2, 3, 4, 5	2 8	3	3 2	2.8	3	3 2	V
I_h	Input Bias Current	Pins 3, 4, 5 = 0V		– 1	– 3		–1	–3	µA
	Start/UV Hysteresis Current	Pin 2 = 2.5 V, T_j = 25 °C	120	180	240	120	180	240	µA
	Input Leakage	V_i = 20 V		0.1	10		0.1	10	µA
	Driver Bias Saturation Voltage V_{IN}–V_{OH}	I_B = – 50 mA		2	3		2	3	V
	Driver Bias Leakage	V_B = 0V		– 0.1	– 10		– 0.1	– 10	µA
	Slow-start Saturation	I_s = 2 mA		0 2	0.5		0 2	0.5	V
	Slow-start Leakage	V_s = 4.5 V		0.1	2		0.1	2	µA

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	UC1840 UC2840			UC3840			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
CURRENT CONTROL									
	Current Limit Offset			0	5		0	10	mV
	Current Shutdown Offset		340	400	440	340	400	440	mV
I_b	Input Bias Current	Pin 7 = 0V		– 2	– 5		– 2	– 5	µA
	*Common mode Range		– 0.3		3	– 0.3		3	V
τ_d*	Current Limit Delay	T_j = 25 °C, Pin 7 to 12 R_L = 1 KΩ		200	400		200	400	ns

* Guaranteed by design Not 100 % tested in production

Figure 1 : Open Loop Test Circuit.



Nominal frequency = $\frac{1}{R_T C_T}$ = 50 kHz

Start voltage = $3 \frac{(R1 + R2 + R3)}{R2 + R3}$ + 0.2 R1 = 12 V

U.V. fault voltage = $3 \frac{(R1 + R2 + R3)}{R2 + R3}$ = 8 V

O.V. fault voltage = $3 \frac{(R1 + R2 + R3)}{R3}$ = 32 V

Current limit = 200mV
Current fault voltage = 600mV
Duty cycle clamp = 50%

Figure 2 : Start U.V. Hysteresis Current.

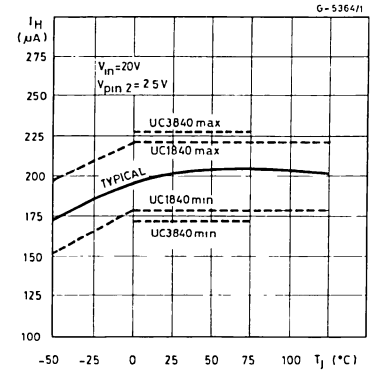


Figure 3 : PWM Output Saturation Voltage.

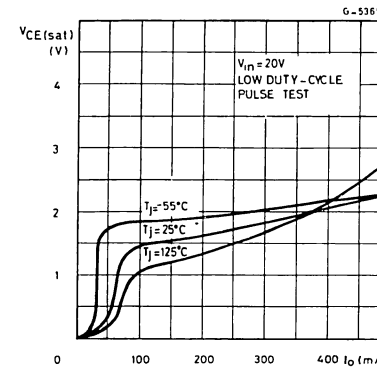


Figure 4 : Oscillator Frequency.

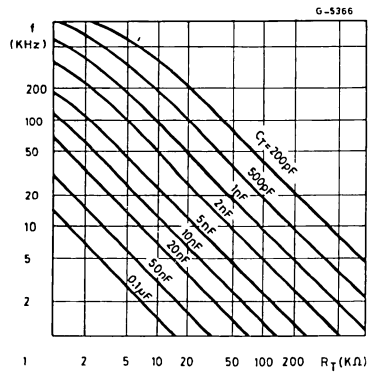


Figure 5 : PWM Output Minimum Pulse Width.

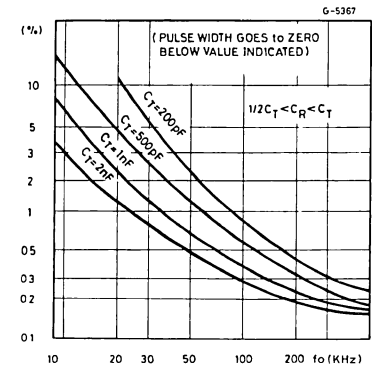


Figure 6 : Error Amplifier Open-loop Gain and Phase.

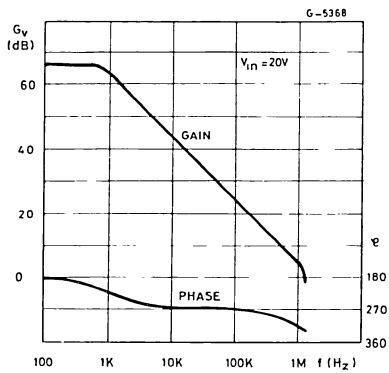
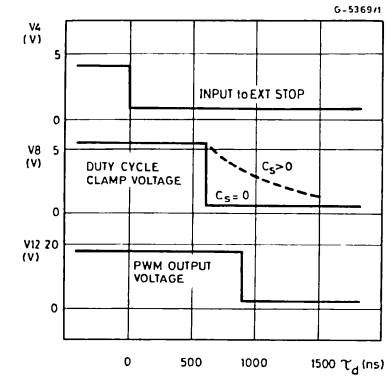
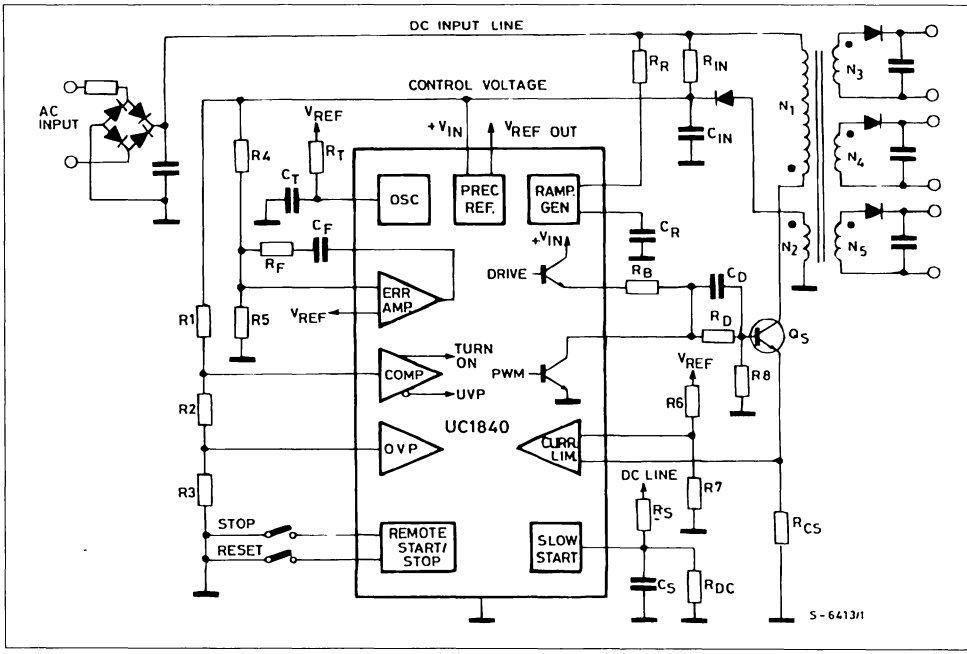


Figure 7 : Shutdown Timing.



APPLICATION INFORMATION

Figure 8 : Programmable PWM Controller in a Simplified Flyback Regulator.

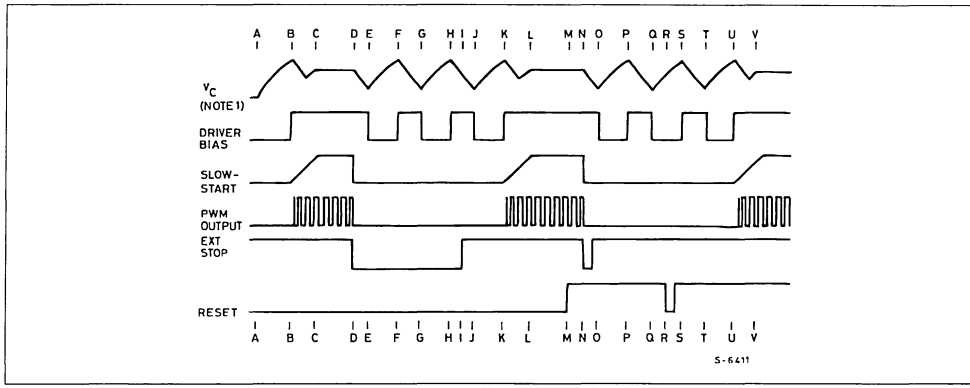


In this application [see Fig.8] complete control is maintained on the primary side. Control power is provided by R_{IN} and C_{IN} during start-up, and by a primary-referenced low voltage winding. N2, for efficient operation after start. The error amplifier loop is closed to regulate the DC voltage from N2 with other outputs following through their magnetic coupling - a task made even easier with the UC1840's feed-forward line regulation.

The UC1840 will readily accept digital start/stop commands transmitted from the secondary side by means of optical couplers.

Not shown are protective snubbers or additional interface circuitry which may be required by the choice of the high-voltage switch, Qs, or the application

Figure 9 : Power Sequencing Functions.



Notes : 1. VC represents an analog of the output voltage generated by a primary-referenced secondary winding of the power transformer. It is the voltage monitored by the start/U.V. comparator and, in most cases, is the supply voltage, Vi, for the UC1840
2. Although input to External Stop, Pin 4, is shown, results are the same for any fault input which sets the Error Latch.

POWER FREQUENCY FUNCTIONS

Time	Event
A	Initial Turn-on, V_c Rises with Light Load
B	Start Threshold. Driver Bias Loads V_c
C	Operating PWM Regulates V_c
D	Stop Input Sets Error Latch Turning off PWM
E	U. V. Low Threshold. Error Latch Remain Set
F	Start Turns on Driver Bias Bus Error Latch Still Set
G H	V_c and Driver Bias Continue to Cycle
I	Stop Command Removed
J	Error Latch Reset at U. V. Low Threshold
K	Start Threshold Now Removes Slow-start Clam

Time	Event
L	Return to Normal Run State
M	Reset Latch Set Signal Removed
N	Error Latch Set with Momentary Fault
O	Error Latch does not reset as Reset Latch is reset
P Q	V_c and Driver Bias Recycle with no Turn-on
R	Reset Latch Set is Set with Momentary Reset Signal
S	V_c must Complete Cycle to Turn-on
T	Start and Error Latches Reset
U	Normal Start Initiated
V	Return to Normal Run State

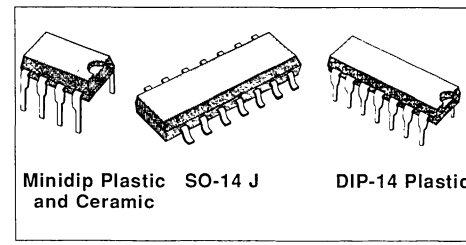
CURRENT MODE PWM CONTROLLER

- OPTIMIZED FOR OFF-LINE AND DC TO DC CONVERTERS
- LOW START-UP CURRENT (< 1 mA)
- AUTOMATIC FEED FORWARD COMPENSATION
- PULSE-BY-PULSE CURRENT LIMITING
- ENHANCED LOAD RESPONSE CHARACTERISTICS
- UNDER-VOLTAGE LOCKOUT WITH HYSTERESIS
- DOUBLE PULSE SUPPRESSION
- HIGH CURRENT TOTEM POLE OUTPUT
- INTERNALLY TRIMMED BANDGAP REFERENCE
- 500 KHz OPERATION
- LOW R_O ERROR AMP

DESCRIPTION

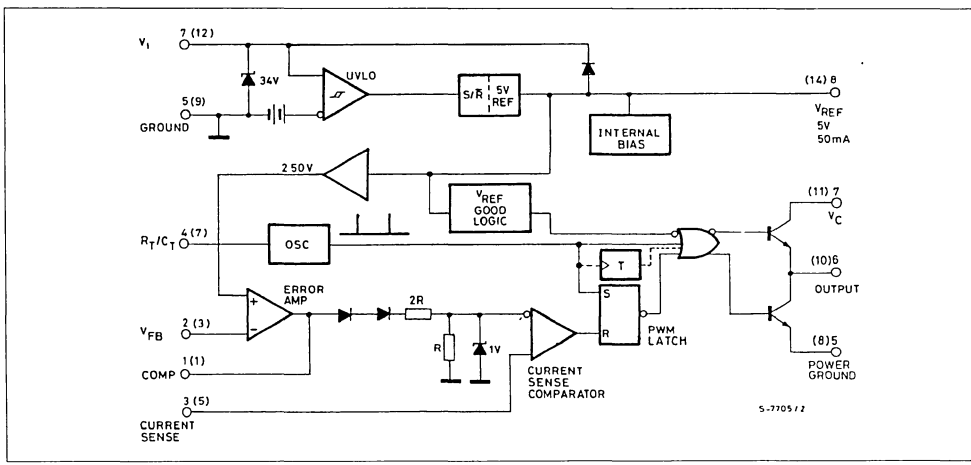
The UC1842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under voltage lockout featuring start-up current less than 1 mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off-state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16 V (on) and 10 V (off), ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.5 V and 7.9 V. The UC1842 and UC1843 can operate to duty cycles approaching 100 %. A range of the zero to < 50 % is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.



Minidip Plastic and Ceramic **SO-14 J** **DIP-14 Plastic**

BLOCK DIAGRAM (toggle flip flop used only in UC1844 and UC1845)



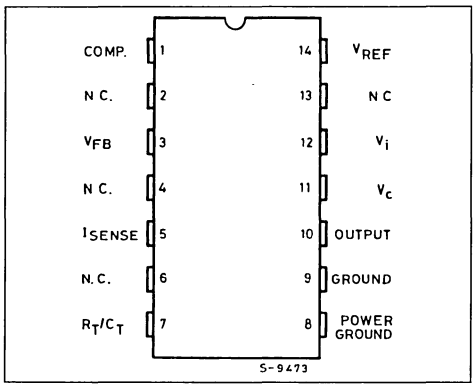
ABSOLUTE MAXIMUM RATINGS *

Symbol	Parameter	Value	Unit
V_i	Supply Voltage (low impedance source)	30	V
V_i	Supply Voltage (I_i < 30 mA)	Self Limiting	
I_O	Output Current	± 1	A
E_O	Output Energy (capacitive load)	5	μJ
	Analog Inputs (pins 2, 3)	– 0.3 to 6.3	V
	Error Amplifier Output Sink Current	10	mA
P_{tot}	Power Dissipation at $T_{amb} \leq 50$ ° C (minidip, DIP-14)	1	W
P_{tot}	Power Dissipation at $T_{amb} \leq 25$ ° C (SO-14)	725	mW
T_{stg}	Storage Temperature Range	– 65 to 150	°C
T_L	Lead Temperature (soldering 10 s)	300	°C

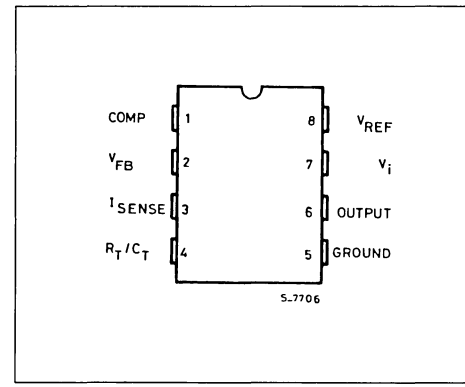
* All voltages are with respect to pin 5, all currents are positive into the specified terminal

BLOCK DIAGRAM (top view)

DIP-14 / SO-14.



Minidip Plastic and Ceramic.



ORDERING NUMBERS

TYPE	PLASTIC MINIDIP	CERAMIC MINIDIP	DIP-14	SO-14
UC1842 UC1843 UC1844 UC1845		UC1842J UC1843J UC1844J UC1845J		
UC2842 UC2843 UC2844 UC2845	UC2842N UC2843N UC2844N UC2845N	UC2842J UC2843J UC2844J UC2845J	UC2842B UC2843B UC2844B UC2845B	UC2842D UC2843D UC2844D UC2845D
UC3842 UC3843 UC3844 UC3845	UC3842N UC3843N UC3844N UC3845N	UC3842J UC3843J UC3844J UC3845J	UC3842B UC3843B UC3844B UC3845B	UC3842D UC3843D UC3844D UC3845D

THERMAL DATA

		Ceramic Minidip	Plastic Minidip	DIP-14 Plastic	SO-14
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	200 °C/W	100 °C/W	100 °C/W	165 °C/W

ELECTRICAL CHARACTERISTICS (unless otherwise stated, these specifications apply for $-55 \le T_{amb} \le 125$ °C for UC184X ; $-25 \le T_{amb} \le 85$ °C for UC284X ; $0 \le T_{amb} \le 70$ °C for UC384X ; $V_i = 15$ V (Note 5) ; $R_T = 10$ K ; $C_T = 3.3$ nF)

Symbol	Parameter	Test Conditions	UC184X 284X			UC384X			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION									
V_{REF}	Output Voltage	$T_j = 25$ °C $I_o = 1$ mA	4 95	5 00	5 05	4 90	5 00	5 10	V
ΔV_{REF}	Line Regulation	$12\ V \le V_i \le 25$ V		6	20		6	20	mV
ΔV_{REF}	Load Regulation	$1 \le I_o \le 20$ mA		6	25		6	25	mV
$\Delta V_{REF}/\Delta T$	Temperature Stability	(Note 2)		0 2	0 4		0.2	0 4	mV/°C
	Total Output Variation	Line, Load Temperature (Note 2)	4 9		5 1	4 82		5 18	V
e_N	Output Noise Voltage	10 Hz ≤ f ≤ 10 KHz $T_j = 25$ °C (Note 2)		50			50		µV
	Long Term Stability	$T_{amb} = 125$ °C, 1000 Hrs (Note 2)		5	25		5	25	mV
I_{sc}	Output Short Circuit		−30	−100	−180	− 30	−100	−180	mA
OSCILLATOR SECTION									
f_s	Initial Accuracy	$T_j = 25$ °C (Note 6)	47	52	57	47	52	57	KHz
	Voltage Stability	$12 \le V_i \le 25$ V		0.2	1		0.2	1	%
	Temperature Stability	$T_{MIN} \le T_{amb} \le T_{MAX}$ (Note 2)		5			5		%
V_4	Amplitude	V_{PIN4} Peak to Peak		1.7			1.7		V
ERROR AMP SECTION									
V_2	Input Voltage	$V_{PIN1} = 2.5$ V	2.45	2 50	2.55	2 42	2.50	2.58	V
I_b	Input Bias Current			− 0.3	− 1		− 0.3	− 2	µA
	A_{VOL}	$2 \le V_o \le 4$ V	65	90		65	90		dB
B	Unity Gain Bandwidth	(Note 2)	0 7	1		0 7	1		MHz
SVR	Supply Voltage Rejection	$12 \le V_i \le 25$ V	60	70		60	70		dB
I_o	Output Sink Current	$V_{PIN2} = 2.7$ V $V_{PIN1} = 1.1$ V	2	6		2	6		mA
I_o	Output Source Current	$V_{PIN2} = 2.3$ V $V_{PIN1} = 5$ V	− 0.5	− 0.8		− 0.5	− 0.8		mA
	V_{OUT} High	$V_{PIN2} = 2.3$ V ; $R_l = 15$ KΩ to Ground	5	6		5	6		V
	V_{OUT} Low	$V_{PIN2} = 2.7$ V ; $R_L = 15$ KΩ to Pin 8		0 7	1 1		0.7	1.1	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	UC184X UC284X			UC384X			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
CURRENT SENSE SECTION									
G_v	Gain	(Notes 3 & 4)	2.85	3	3.15	2.8	3	3.2	V/V
V_3	Maximum Input Signal	V_{PIN1} = 5 V (Note 3)	0.9	1	1 1	0.9	1	1 1	V
SVR	Supply Voltage Rejection	12 ≤ V_i ≤ 25 V (Note 3)		70			70		dB
I_b	Input Bias Current			– 2	– 10		– 2	– 10	µA
	Delay to Output			150	300		150	300	ns
OUTPUT SECTION									
I_{OL}	Output Low Level	I_{SINK} = 20 mA		0.1	0.4		0.1	0.4	V
		I_{SINK} = 200 mA		1.5	2.2		1.5	2.2	
I_{OH}	Output High Level	I_{SOURCE} = 20 mA	13	13.5		13	13.5		V
		I_{SOURCE} = 200 mA	12	13.5		12	13.5		
t_r	Rise Time	T_J = 25 °C C_L = 1 nF (Note 2)		50	150		50	150	ns
t_f	Fall Time	T_J = 25 °C C_L = 1 nF (Note 2)		50	150		50	150	ns
UNDER-VOLTAGE LOCKOUT SECTION									
	Start Threshold	X842/4	15	16	17	14.5	16	17.5	V
		X843/5	7.8	8.4	9.0	7.8	8.4	9.0	
	Min. Operating Voltage After Turn-on	X842/4	9	10	11	8.5	10	11.5	V
		X843/5	7.0	7.6	8.2	7.0	7.6	8.2	
PWM SECTION									
	Maximum Duty Cycle	X842/3	93	97	100	93	97	100	%
		X844/5	44	48	50	45	48	50	
	Minimum Duty Cycle				0			0	%
TOTAL STANDBY CURRENT									
I_{st}	Start-up Current			0.5	1		0.5	1	mA
I_i	Operating Supply Current	V_{PIN2} = V_{PIN3} = 0 V		11	20		11	20	mA
V_{iz}	Zener Voltage	I_i = 25 mA		34			34		V

Notes : 2. These parameters, although guaranteed, are not 100% tested in production
3 Parameter measured at trip point of latch with V_{PIN2} = 0
4. Gain defined as

$$A = \frac{\Delta V_{PIN1}}{\Delta V_{PIN3}} ; 0 \le V_{PIN3} \le 0.8 \text{ V}$$

5 Adjust V_i above the start threshold before setting at 15 V.
6. Output frequency equals oscillator frequency for the UC1842 and UC1843.
Output frequency is one half oscillator frequency for the UC1844 and UC1845

Figure 1 : Error Amp Configuration.

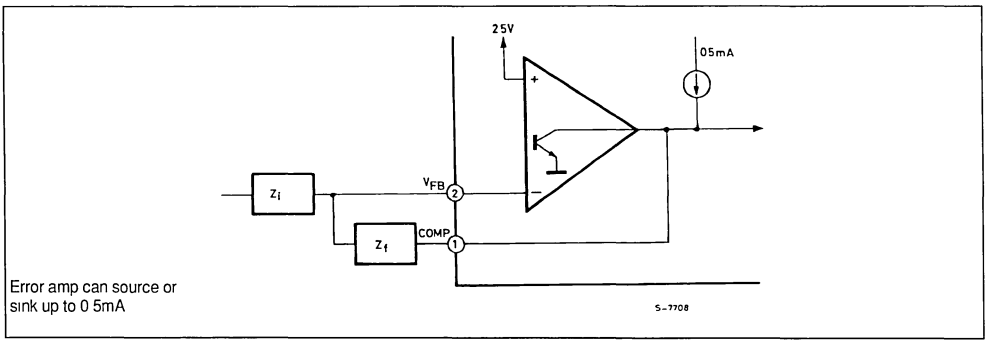
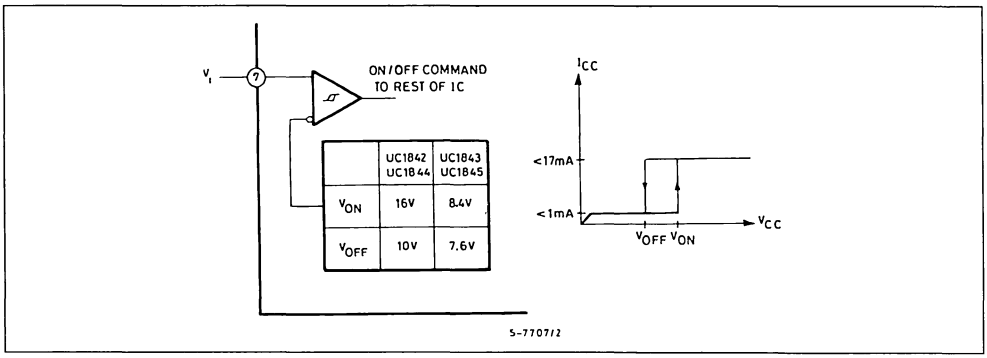
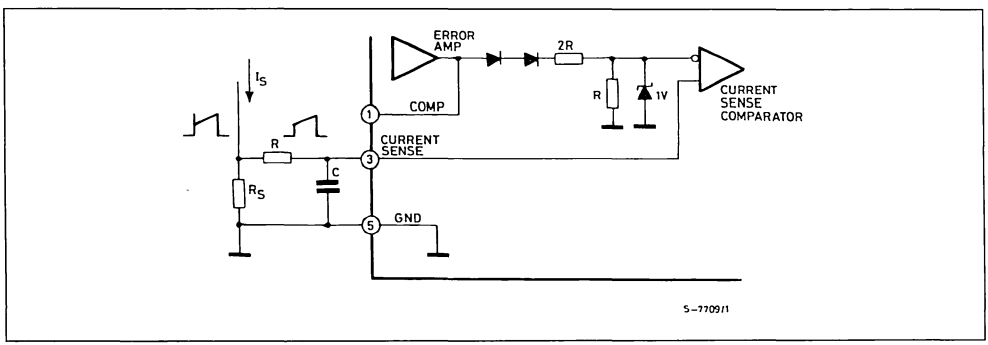


Figure 2 : Under Voltage Lockout.



During Under-Voltage Lockout, the output driver is biased to sink minor amounts of current. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with extraneous leakage currents.

Figure 3 : Current Sense Circuit .



PEAK CURRENT (I_S) IS DETERMINED BY THE FORMULA

$$I_{S\,max} \approx \frac{1.0\ V}{R_S}$$

A SMALL RC FILTER MAY BE REQUIRED TO SUPPRESS SWITCH TRANSIENTS.

Figure 4.

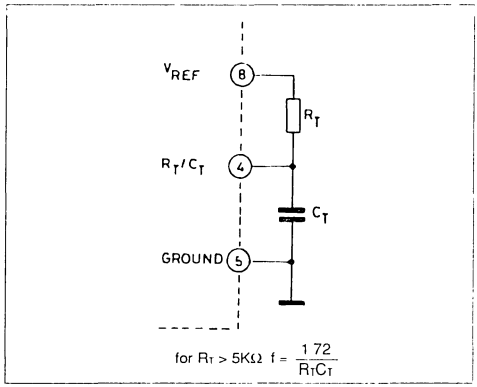


Figure 5 : Deadtime vs. C_T ($R_T > 5K\Omega$).

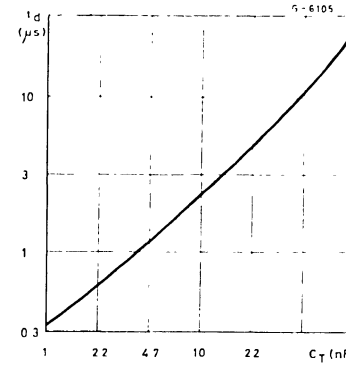


Figure 6 : Timing Resistance vs. Frequency.

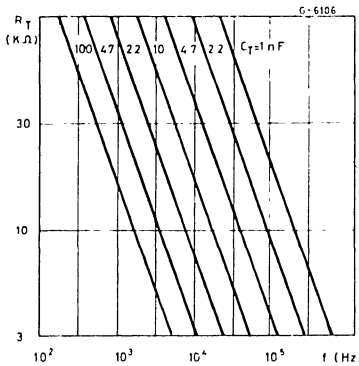


Figure 7 : Output Saturation Characteristics.

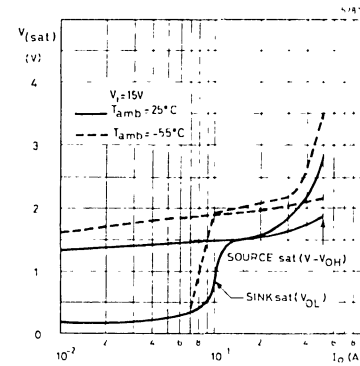


Figure 8 : Error Amplifier Open-loop Frequency Response.

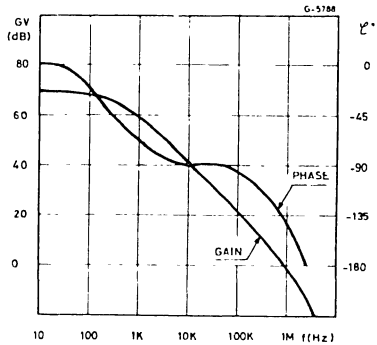
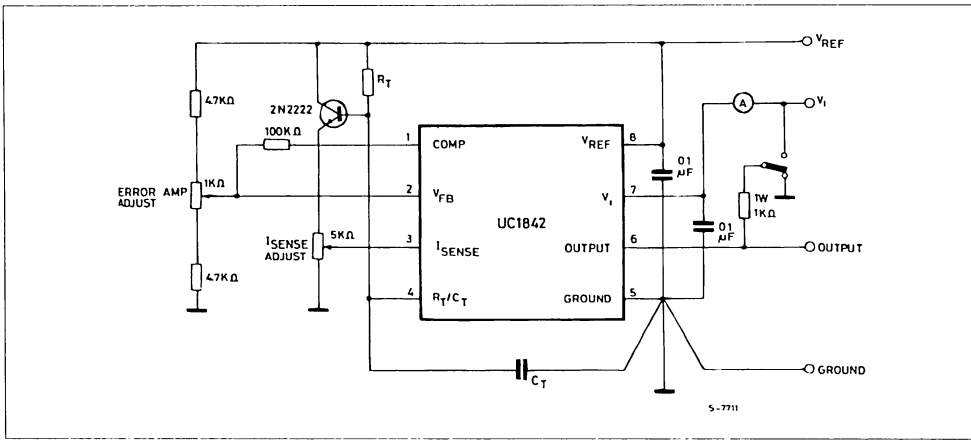
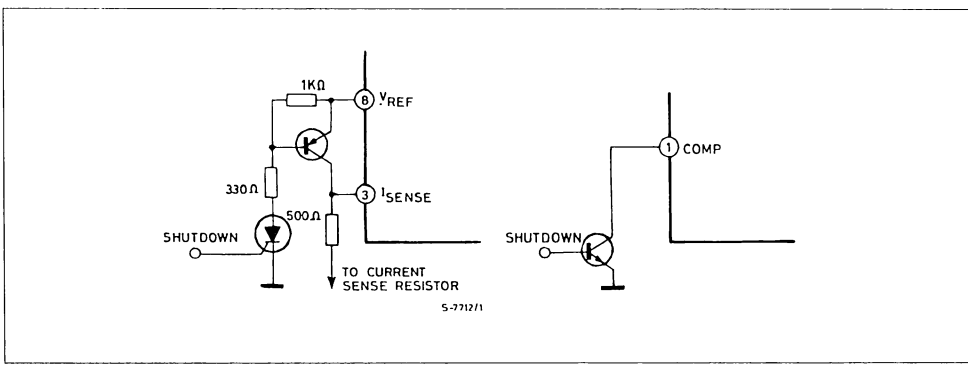


Figure 9 : Open Loop Test Circuit.



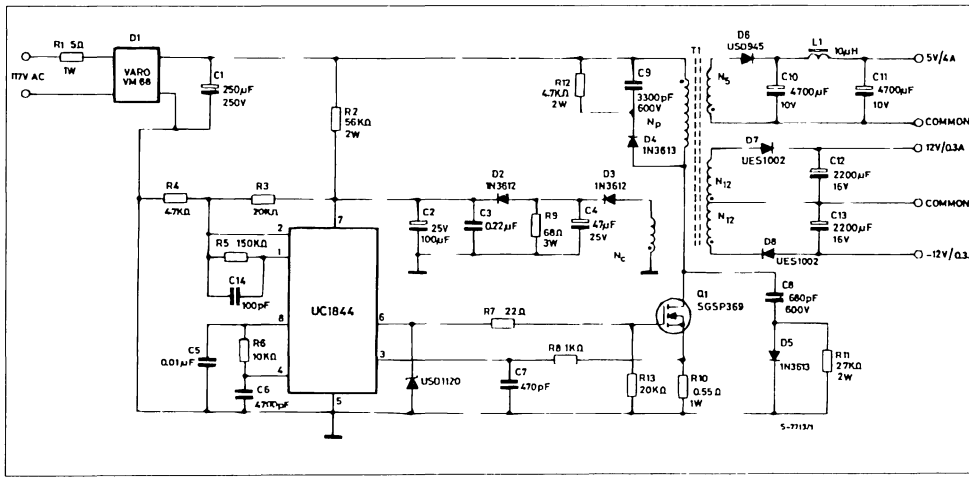
High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5 KΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 10 : Shutdown Techniques.



Shutdown of the UC1842 can be accomplished by two methods ; either raise pin 3 above 1 V or pull pin 1 below a voltage two diode drops above ground. Either method cause the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pins 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling V_i below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.

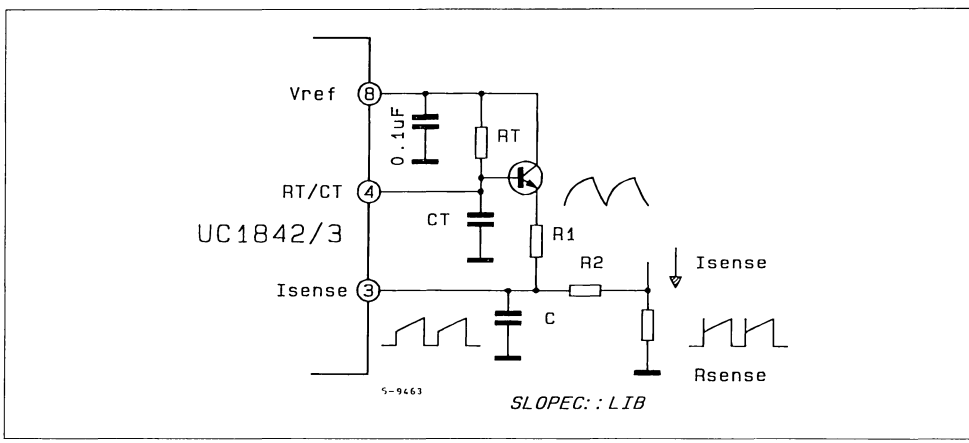
Figure 11 : Off-line Flyback Regulator.



Power Supply Specifications

1. Input Voltage : 95 VAC to 130 VAC (50 Hz/60 Hz)
2. Line Isolation : 3750 V
3. Switching Frequency : 40 KHz
4. Efficiency @ Full Load : 70 %
5. Output Voltage :
   A. + 5 V, ± 5 % : 1 A to 4 A load
   Ripple voltage : 50 mV P-P Max.
   B. + 12 V, ± 3 % : 0.1 A to 0.3 A load
   Ripple voltage : 100 mV P-P Max.
   C. – 12 V, ± 3 % : 0.1 A to 0.3 A load
   Ripple voltage : 100 mV P-P Max.

Figure 12 : Slope Compensation.



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50 %.

Note that capacitor, C, forms a filter with R_2 to supress the leading edge switch spikes.

SGS-THOMSON MICROELECTRONICS

UCN4801A

BIMOS LATCH/DRIVERS

ADVANCE DATA

- HIGH-VOLTAGE, HIGH-CURRENT OUTPUTS
- OUTPUT TRANSIENT PROTECTION
- CMOS, PMOS, NMOS, TTL COMPATIBLE INPUTS
- INTERNAL PULL-DOWN RESISTORS
- LOW-POWER CMOS LATCHES

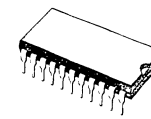
DESCRIPTION

The UCN4801A is a high-voltage, high-current latch/driver comprised of eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions. The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility.

The CMOS inputs are compatible with standard CMOS, PMOS and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors. The bipolar outputs are suitable for use with relays, solenoids, stepping motors, LED or incandescent displays, and other high-power load.

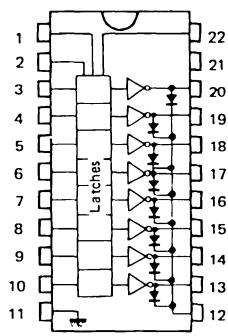
The unit feature open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 500 mA and will sustain at least 50 V in the OFF state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.

DIP-22
(Plastic)



ORDER CODE : UCN4801ADP

PIN CONNECTIONS (Top view)



1 - Clear
2 - Strobe
3 - Input 1
4 - Input 2
5 - Input 3
6 - Input 4
7 - Input 5
8 - Input 6
9 - Input 7
10 - Input 8
11 - GND

22 - Output enable
21 - V_{CC}
20 - Output 1
19 - Output 2
18 - Output 3
17 - Output 4
16 - Output 5
15 - Output 6
14 - Output 7
13 - Output 8
12 - Common

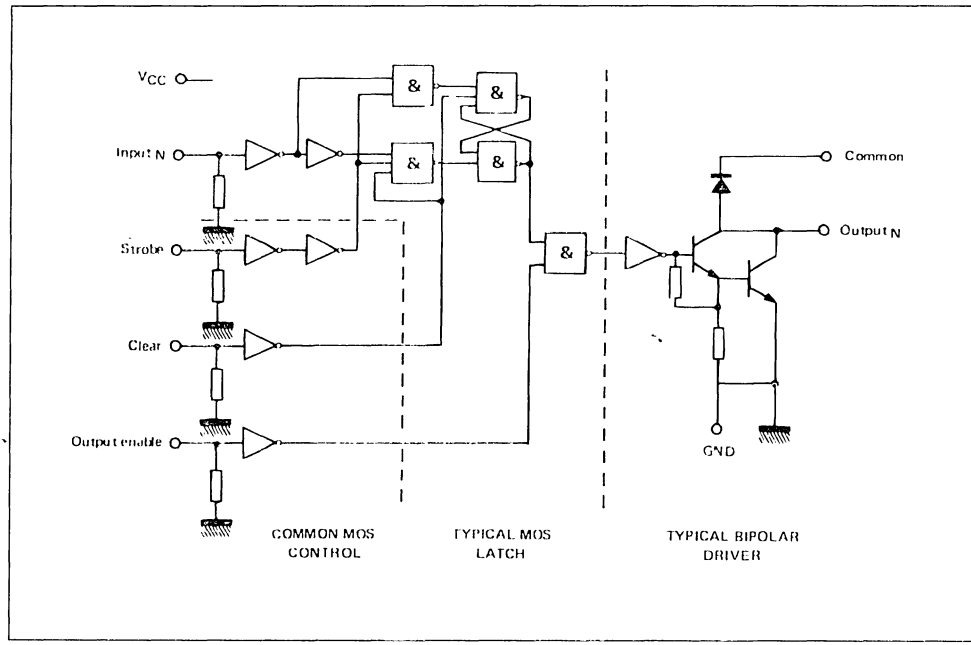
This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_{CC}	Supply Voltage	18	V
V_I	Input Voltage Range	− 0.3 to V_{CC} + 0.3	V
I_C	Continuous Collector Current	500	mA
P_{tot}	Power Dissipation*	2.0	W
T_{op}	Operating Ambient Temperature Range	− 20 to + 85	°C
T_{stg}	Storage Temperature	− 55 to + 125	°C

* Derate at the rate of 16 mW/°C above T_{amb} = + 25 °C

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS T_{amb} = + 25 °C. V_{CC} = 5 V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_O	Output Leakage Current (V_O = 50 V)				µA
	T_{amb} = + 25 °C	–	–	50	
	T_{amb} = + 70 °C	–	–	100	
$V_{O(Sat)}$	Collector-emitter Saturation Voltage				V
	I_O = 100 mA	–	0.9	1.1	
	I_O = 200 mA	–	1.1	1.3	
	I_O = 350 mA, V_{CC} = 7 V	–	1.3	1.6	
$V_{I(O)}$	Input Voltage	–	–	1	V
$V_{I(1)}$	V_{CC} = 15 V	13.5	–	–	
	V_{CC} = 10 V	8.5	–		
	V_{CC} = 5 V - (note 1)	3.5	–	–	
R_{IN}	Input Resistance				KΩ
	V_{CC} = 15 V	50	200	–	
	V_{CC} = 10 V	50	300	–	
	V_{CC} = 5 V	50	600	–	
$I_{CC(on)}$	Supply Current - Outputs Open				mA
(each stage)	V_{CC} = 15 V	–	1	2	
	V_{CC} = 10 V	–	0.9	1.7	
	V_{CC} = 5 V	–	0.7	1	
$I_{CC(off)}$	All Drivers off, All Inputs = 0 V	–	50	100	µA
I_R	Clamp Diode Leakage Current (V_R = 50 V)				µA
	T_{amb} = + 25 °C	–	–	50	
	T_{amb} = + 70 °C	–	–	100	
V_F	Clamp Diode Forward Voltage I_F = 350 mA	–	1.7	2	V

Note : 1 Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure the minimum logic '1'

TRUTH TABLE

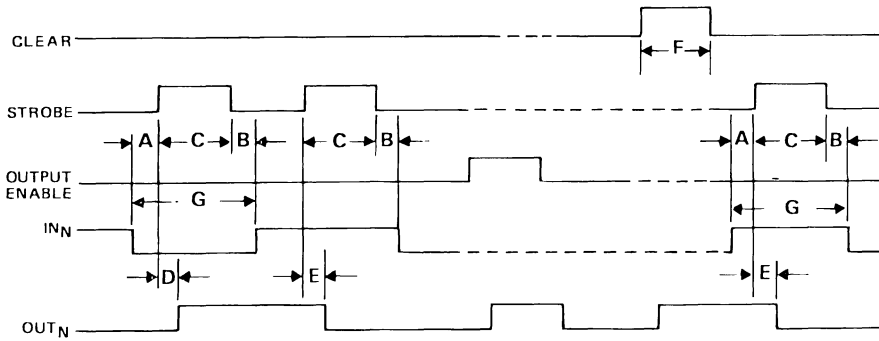
IN_N	Strobe	Clear	Output Enable	OUT_N t–1	OUT_N t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON

X = irrelevant
t-1 = previous output state
t = present output state

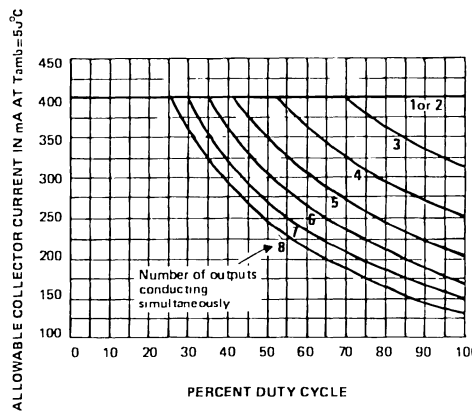
Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

TIMING CONDITIONS

(Logic levels are V_{CC} and GND) V_{CC} = 5 V, Tamb + 25°C



A Minimum data active time before strobe enabled (data set-up time)	100 ns
B Minimum data active time after strobe disabled (data hold time)	100 ns
C Minimum strobe pulse width	300 ns
D Typical time between strobe activation and output on to off transition	500 ns
E Typical time between strobe activation and output off to on transition	500 ns
F Minimum clear pulse width	300 ns
G Minimum data pulse width	500 ns



SGS-THOMSON MICROELECTRONICS

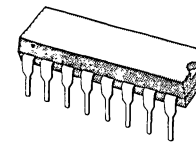
ULN2001A-ULN2003A
ULN2002A-ULN2004A

SEVEN DARLINGTON ARRAYS

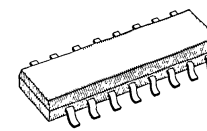
- SEVEN DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 500 mA PER DRIVER (600 mA PEAK)
- OUTPUT VOLTAGE 50 V
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays filament lamps, thermal printheads and high power buffers.

The ULN2001A/2002A/2003A and 2004A are supplied in 16 pin plastic DIP packages with a copper leadframe to reduce thermal resistance. They are available also in small outline package (SO-16) as ULN2001D/2002D/2003D/2004D.



DIP-16 Plastic
(0.25)



SO-16J

ORDER CODES :
ULN2001A/2A/3A/4A (DIP-16)
ULN2001D/2D/3D/4D (SO-16)

DESCRIPTION

The ULN2001A, ULN2002A, ULN2003 and ULN2004A are high voltage, high current darlington arrays each containing seven open collector darlington pairs with common emitters. Each channel is rated at 500 mA and can withstand peak currents of 600 mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

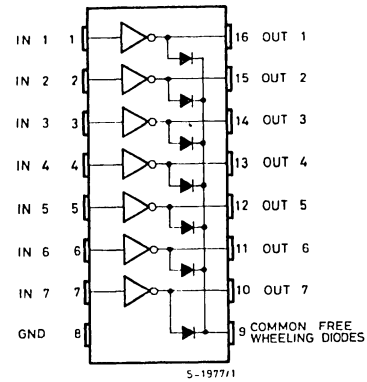
The four versions interface to all common logic families :

ULN2001A	General Purpose, DTL, TTL, PMOS, CMOS
ULN2002A	14-25 V PMOS
ULN2003A	5 V TTL, CMOS
ULN2004A	6–15 V CMOS, PMOS

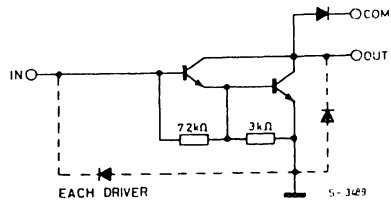
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_{in}	Input Voltage (for ULN2002A/D - 2003A/D - 2004A/D)	30	V
I_c	Continuous Collector Current	500	mA
I_b	Continuous Base Current	25	mA
T_{amb}	Operating Ambient Temperature Range	– 20 to 85	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C
T_j	Junction Temperature	150	°C

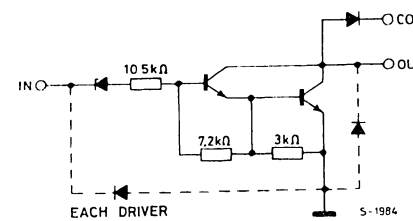
PIN CONNECTION



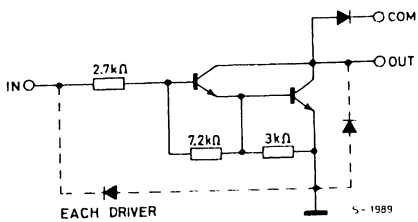
SCHEMATIC DIAGRAM



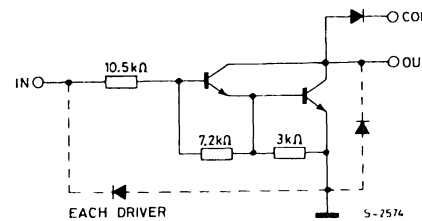
Series ULN-2001A
(each driver)



Series ULN-2002A
(each driver)



Series ULN-2003A
(each driver)



Series ULN-2004A
(each driver)

THERMAL DATA

			DIP-16	SO-16
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	70 C/W	165 C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 50 V			50	µA	1a
		T_{amb} = 70 °C V_{CE} = 50 V			100	µA	1a
		T_{amb} = 70 °C for **ULN2002A** V_{CE} = 50 V V_i = 6 V			500	µA	1b
		for **ULN2004A** V_{CE} = 50 V V_i = 1 V			500	µA	1b
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 100 mA I_B = 250 µA		0.9	1.1	V	2
		I_C = 200 mA I_B = 350 µA		1.1	1.3	V	2
		I_C = 350 mA I_B = 500 µA		1.3	1.6	V	2
$I_{i(on)}$	Input Current	for **ULN2002A** V_i = 17 V		0.82	1.25	mA	3
		for **ULN2003A** V_i = 3.85 V		0.93	1.35	mA	3
		for **ULN2004A** V_i = 5 V		0.35	0.5	mA	3
		V = 12 V		1	1.45	mA	3
$I_{i(off)}$	Input Current	T_{amb} = 70 °C I_C = 500 µA	50	65		µA	4
$V_{i(on)}$	Input Voltage	for **ULN2002A** V_{CE} = 2 V I_C = 300 mA			13	V	5
		for **ULN2003A** V_{CE} = 2 V I_C = 200 mA			2.4	V	5
		V_{CE} = 2 V I_C = 250 mA			2.7	V	5
		V_{CE} = 2 V I_C = 300 mA			3	V	5
		for **ULN2004A** V_{CE} = 2 V I_C = 125 mA			5	V	5
		V_{CE} = 2 V I_C = 200 mA			6	V	5
		V_{CE} = 2 V I_C = 275 mA			7	V	5
		V_{CE} = 2 V I_C = 350 mA			8	V	5
h_{FE}	DC Forward Current Gain	for **ULN2001A** V_{CE} = 2 V I_C = 350 mA	1000			–	2
C	Input Capacitance			15	25	pF	–
t_{PLH}	Turn-on Delay Time	0.5 V to 0.5 V_o		0.25	1	µs	–
t_{PHL}	Turn-off Delay Time	0.5 V to 0.5 V_o		0.25	1	µs	–
I_R	Clamp Diode Leakage Current	V_R = 50 V			50	µA	6
		T_{amb} = 70 °C V_R = 50 V			100	µA	6
V_F	Clamp Diode Forward Voltage	I_F = 350 mA		1.7	2	V	7

TEST CIRCUITS

Figure 1a.

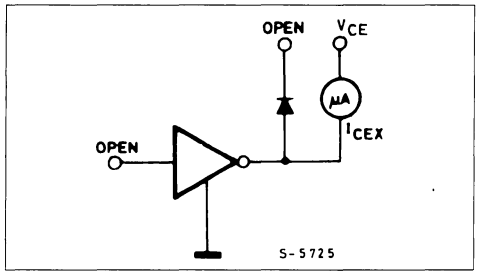


Figure 1b.

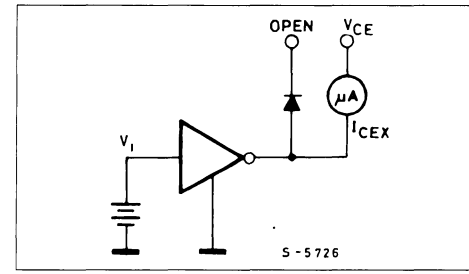


Figure 2.

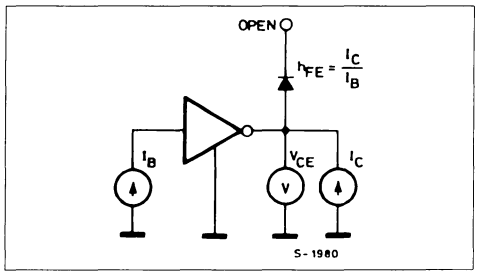


Figure 3.

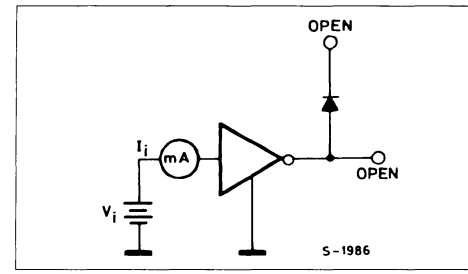


Figure 4.

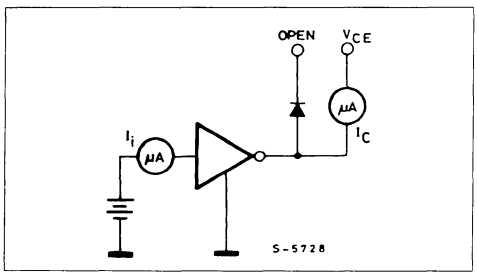


Figure 5.

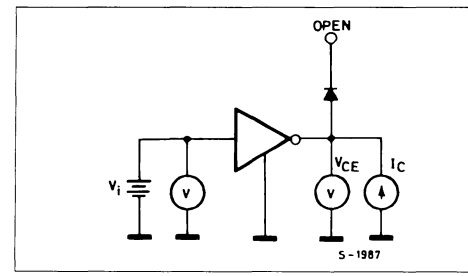


Figure 6.

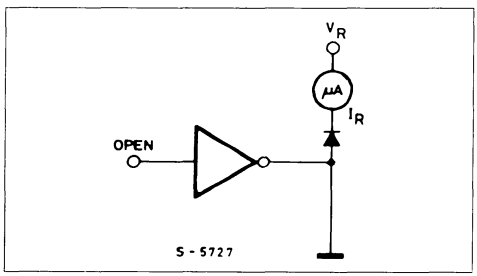
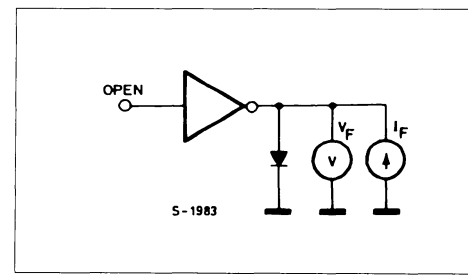


Figure 7.

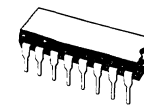


50 V - 1.5 A QUAD DARLINGTON SWITCHES

- OUTPUT CURRENT TO 1.5 A EACH DARLINGTON
- MINIMUM BREAKDOWN 50 V
- SUSTAINING VOLTAGE AT LEAST 35 V
- INTEGRAL SUPPRESSION DIODES (ULN2064B, ULN2066B, ULN2068B and ULN2070B)
- ISOLATED DARLINGTON PINOUT (ULN2074B, ULN2076B)
- VERSIONS COMPATIBLE WITH ALL POPULAR LOGIC FAMILIES

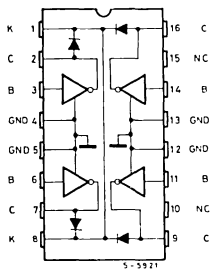
DESCRIPTION

Designed to interface logic to a wide variety of high current, high voltage loads, these devices each contain four NPN darlington switches delivering up to 1.5 A with a specified minimum breakdown of 50 V and a sustaining voltage of 35 V measured at 100 mA. The ULN2064B, ULN2066B, ULN2068B and ULN2070B contain integral suppression diodes for inductive loads have common emitters. The ULN2074B and ULN2076B feature isolated darlington pinouts and are intended for applications such as emitter follower configurations. Inputs of the ULN2064B, ULN2068B and ULN2074B are compatible with popular 5 V logic families and the ULN2066B and ULN2076B are compatible with 6-15 V CMOS and PMOS. Types ULN2068B and ULN2070B include a predriver stage to reduce loading on the control logic.

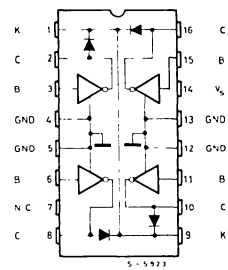


POWERDIP
12 + 2 + 2

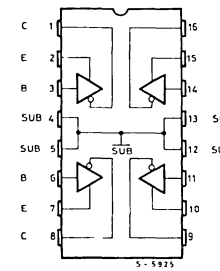
PIN CONNECTIONS (top view) and ORDER CODES



ULN2064B
ULN2068B



ULN2068B
ULN2070B

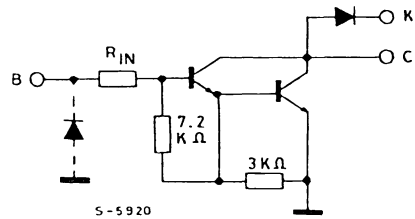


ULN2074B
ULN2076B

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CEX}	Output Voltage	50	V
$V_{CE(sus)}$	Output Sustaining Voltage	35	V
I_o	Output Current	1.75	A
V_i	Input Voltage for **ULN2066B/70B/74B/76B** for **ULN2064B/68B**	30 15	V V
I_i	Input Current	25	mA
V_s	Supply Voltage for **ULN2068B** for **ULN2070B**	10 20	V V
P_{tot}	Power Dissipation : at T_{amb} = 90 °C at T_{amb} = 70 °C	4.3 1	W W
T_{amb}	Operating Ambient Temperature Range	– 20 to 85	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

SCHEMATIC DIAGRAM



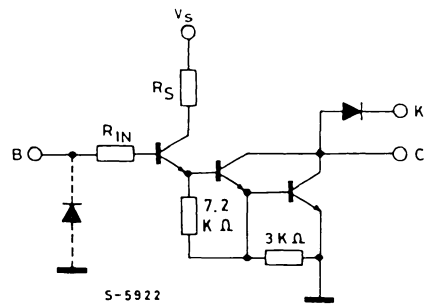
ULN2064B : R_{IN} = 35 Ω
ULN2066B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig
I_{CEX}	Output Leakage Current	for **ULN2064B – ULN2066B**					
		V_{CE} = 50 V			100	µA	1
		V_{CE} = 50 V T_{amb} = 70 °C			500	µA	
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2064B – ULN2066B** I_C = 100 mA V_I = 0.4 V	35			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 500 mA I_B = 625 µA			1.1	V	3
		I_C = 750 mA I_B = 935 µA			1.2	V	
		I_C = 1 A I_B = 1.25 mA			1.3	V	
		I_C = 1.25 A I_B = 2 mA			1.4	V	
$I_{I(on)}$	Input Current	for **ULN2064B** V_I = 2.4 V	1.4		4.3	mA	4
		for **ULN2064B** V_I = 3.75 V	3.3		9.6	mA	
		for **ULN2066B** V_I = 5 V	0.6		1.8	mA	
		for **ULN2066B** V_I = 12 V	1.7		5.2	mA	
$V_{I(on)}$	Input Voltage	for **ULN2064B**					5
		V_{CE} = 2 V I_C = 1 A			2	V	
		V_{CE} = 2 V I_C = 1.5 A			2 5	V	
		for **ULN2066B**					
		V_{CE} = 2 V I_C = 1 A			6 5	V	
		V_{CE} = 2 V I_C = 1.5 A			10	V	
t_{PLH}	Turn – on Delay Time	0.5 V_I to 0.5 V_o			1	µs	
t_{PHL}	Turn – off Delay Time	0.5 V_I to 0.5 V_o			1.5	µs	
I_R	Clamp Diode Leakage Current	for **ULN2064B – ULN2066B**					
		V_R = 80 V			50	µA	6
		V_R = 80 V T_{amb} = 70 °C			100	µA	
V_F	Clamp Diode Forward Voltage	I_F = 1 A			1.75	V	7
		I_F = 1.5 A			2	V	

Notes : 1 Input voltage is with reference to the substrate (no connection to any other pins) for the ULN2074B and ULN2076B reference is ground for all other types
2 Input current may be limited by maximum allowable input voltage

SCHEMATIC DIAGRAM

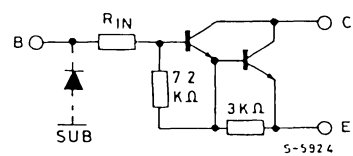


ULN2068B : R_{IN} = 2.5 kΩ R_s = 900 Ω
ULN2070B : R_{IN} = 11.6 kΩ R_s = 3.4 KHΩ

ELECTRICAL CHARACTERISTICS (V_s = 5 V for ULN2068B, V_s = 12 V for ULN2070B, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig
I_{CEX}	Output Leakage Current	for **ULN2068B – ULN2070B**					
		V_{CE} = 50 V			100	µA	1
		V_{CE} = 50 V T_{amb} = 70 °C			500	µA	
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2068B – ULN2070B** I_C = 100 mA V_i = 0.4 V	35			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	for **ULN2068B**					
		I_C = 500 mA V_i = 2.75 V			1.1	V	
		I_C = 750 mA V_i = 2.75 V			1.2	V	
		I_C = 1 A V_i = 2.75 V			1.3	V	
		I_C = 1.25 A V_i = 2.75 V			1.4	V	
		for **ULN2070B**					2
		I_B = 500 mA V_i = 5 V			1.1	V	
		I_B = 750 mA V_i = 5 V			1.2	V	
		I_B = 1 A V_i = 5 V			1.3	V	
		I_B = 1.25 A V_i = 5 V			1.4	V	
$I_{i(on)}$	Input Current	for **ULN2068B** V_i = 2.75 V			550	µA	
		for **ULN2068B** V_i = 3.75 V			1000	µA	
		for **ULN2070B** V_i = 5 V			400	µA	4
		for **ULN2070B** V_i = 12 V			1250	µA	
$V_{i(on)}$	Input Voltage	V_{CE} = 2 V I_C = 1.5 A					
		for **ULN2068B**			2.75	V	5
		for **ULN2070B**			5	V	
I_s	Supply Current	for **ULN2068B**					
		I_C = 500 mA V_i = 2.75 V			6	mA	
		for **ULN2070B**					8
		I_C = 500 mA V_i = 5 V			4.5	mA	
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o I_C = 1.25 A			1.5	µs	
I_R	Clamp Diode Leakage Current	for **ULN2068B – ULN2070B**					
		V_R = 50 V			50	µA	6
		V_R = 50 V T_{amb} = 70 °C			100	µA	
V_F	Clamp Diode Forward Voltage	I_F = 1 A			1.75	V	7
		I_F = 1.5 A			2	V	

SCHEMATIC DIAGRAM



ULN2074B R_{IN} = 350 Ω
ULN2076B . R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig
I_{CEX}	Output Leakage Current	for **ULN2074B – ULN2076B** V_{CE} = 50 V V_{CE} = 50 V T_{amb} = 70 °C			 100 500	 µA µA	1
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2074B – ULN2076B** I_C = 100 mA V_I = 0.4 V	 35			 V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 500 mA I_B = 625 µA I_C = 750 mA I_B = 935 µA I_C = 1 A I_B = 1.25 mA I_C = 1.25 A I_B = 2 mA			1.1 1.2 1.3 1.4	V V V V	3
$I_{I(on)}$	Input Current	for **ULN2074B** V_I = 2.4 V for **ULN2074B** V_I = 3.75 V for **ULN2076B** V_I = 5 V for **ULN2076B** V_I = 12 V	1.4 3.3 0.6 1.7		4.3 9.6 1.8 5.2	mA mA mA mA	4
$V_{I(on)}$	Input Voltage	for **ULN2074B** V_{CE} = 2 V I_C = 1 A V_{CE} = 2 V I_C = 1.5 A for **ULN2076B** V_{CE} = 2 V I_C = 1 A V_{CE} = 2 V I_C = 1.5 A			 2 2.5 6.5 10	 V V V V	5
t_{PLH}	Turn-on Delay Time	0.5 V_I to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_I to 0.5 V_o			1.5	µs	

TEST CIRCUITS

Figure 1.

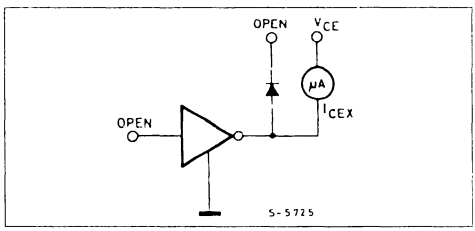


Figure 2.

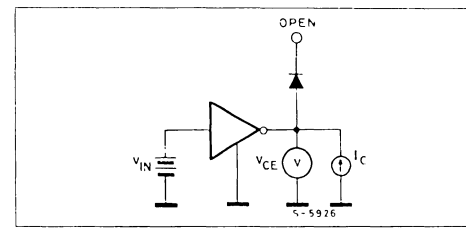


Figure 3.

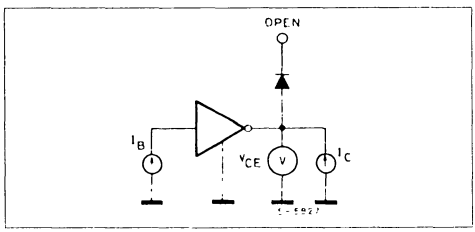


Figure 4.

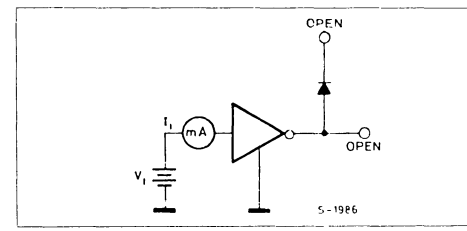


Figure 5.

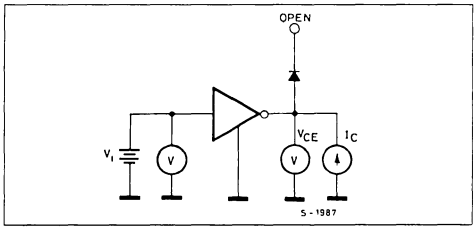


Figure 6.

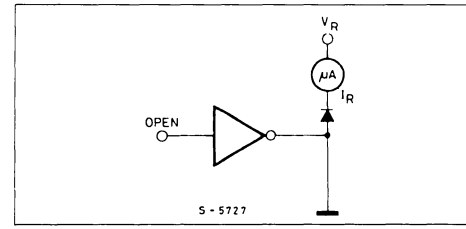


Figure 7.

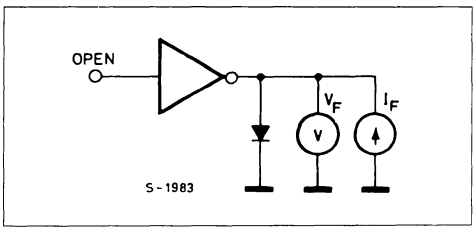


Figure 8.

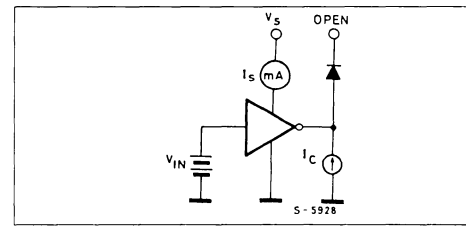


Figure 9 : Input Current as a Function of Input Voltage.

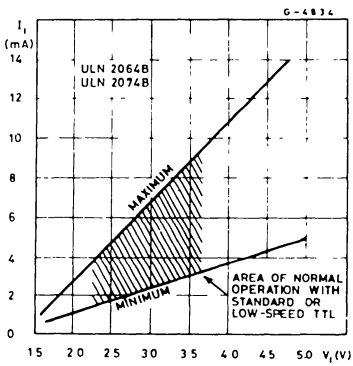


Figure 10 : Input Current as a Function of Input Voltage.

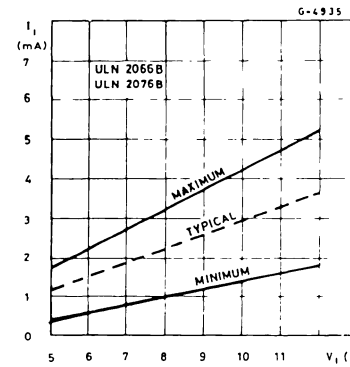
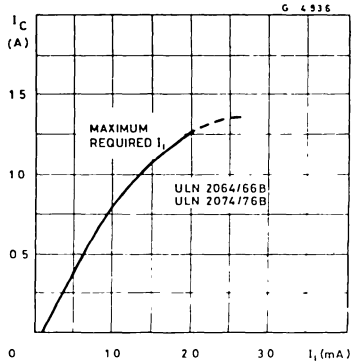


Figure 11 : Collector Current as a Function of Input Current.



TYPICAL APPLICATIONS

Figure 12 : Common-anode LED Drivers.

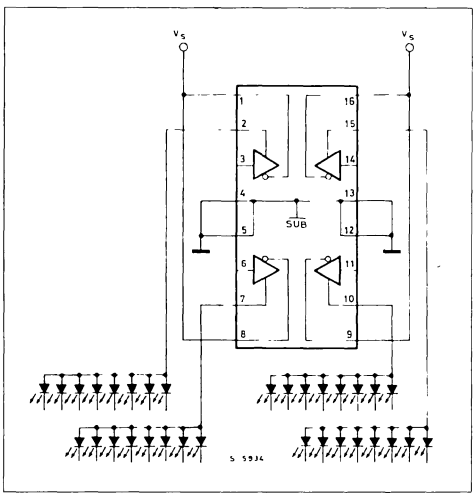
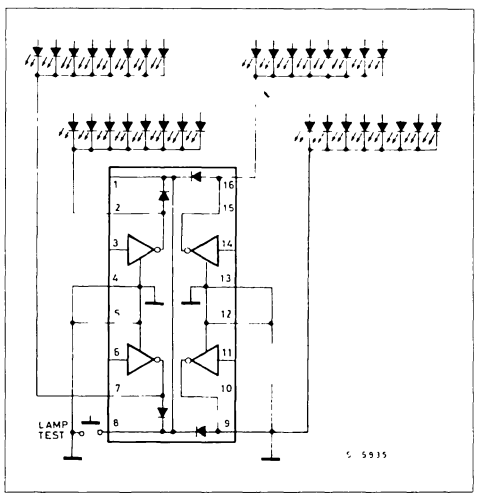


Figure 13 : Common-cathode LED Drivers.



MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 14) or to an external heatsink (Fig. 15).

The diagram of figure 16 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "α" of two equal square copper areas having a thickness of 35 μ (1.4 mils).

During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 14 : Example of P.C. Board Copper Area which is Used as Heatsink.

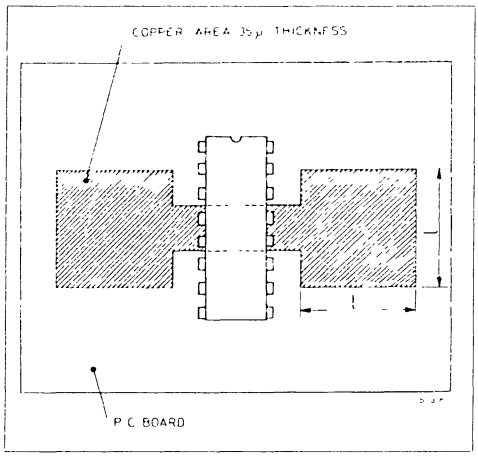


Figure 15 : External Heatsink Mounting Example.

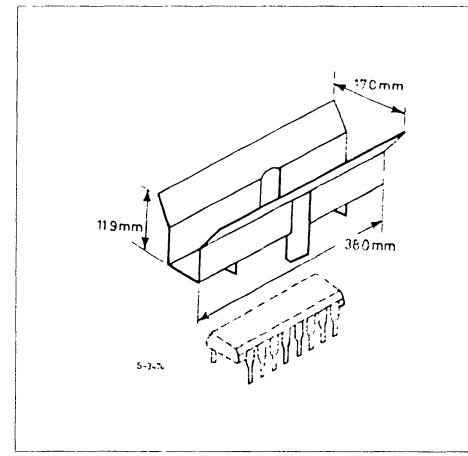


Figure 16 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side "α".

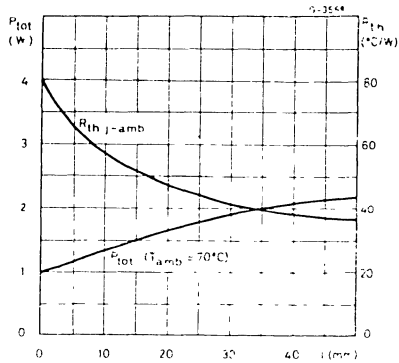
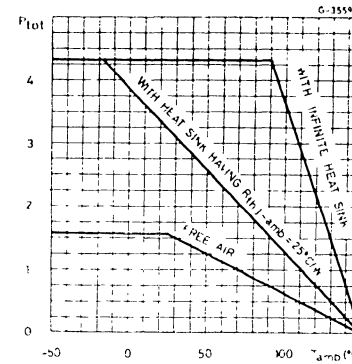


Figure 17 : Maximum Allowable Power Dissipation vs. Ambient Temperature.

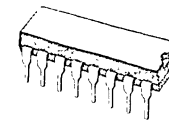


80 V - 1.5 A QUAD DARLINGTON SWITCHES

- OUTPUT CURRENT TO 1.5 A EACH DARLINGTON
- MINIMUM BREAKDOWN 80 V
- SUSTAINING VOLTAGE AT LEAST 50 V
- INTEGRAL SUPPRESSION DIODES (ULN2065B. ULN2067B, ULN2069B and ULN2071B)
- ISOLATED DARLINGTON PINOUT (ULN2075B and ULN2077B)
- VERSIONS COMPATIBLE WITH ALL POPULAR LOGIC FAMILIES

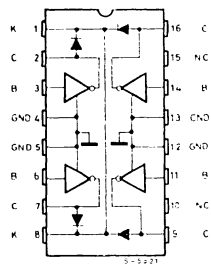
DESCRIPTION

Designed to interface logic to a wide variety of high current, high voltage loads, these devices each contain four NPN darlington switches delivering up to 1.5 A with a specified minimum breakdown of 80 V and a sustaining voltage of 50 V. The ULN2065B, ULN2067B, ULN2069B and ULN2071B contain integral suppression diodes for inductive loads and have common emitters ; the ULN2075B and ULN2077B feature isolated darlington pinouts and are intended for applications such as emitter follower configurations. Inputs of the ULN2065B. ULN2069B and ULN2075B are compatible with popular 5 V logic families and the ULN2067B, ULN2071B and ULN2077B are compatible with 6-15 VCMOS and PMOS. The ULN2069B and ULN2071B include a predriver stage to provide extragain, reducing the load on control logic.

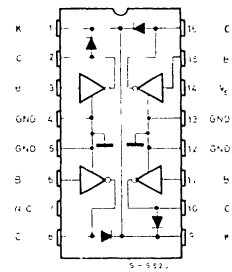


POWERDIP
12 + 2 + 2

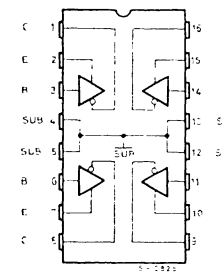
PIN CONNECTIONS AND ORDER CODES



ULN2065B
ULN2067B



ULN2069B
ULN2071B

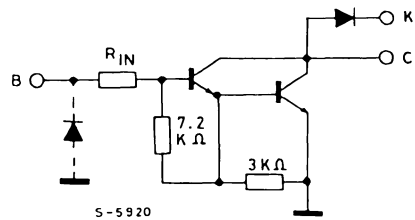


ULN2075B
ULN2077B

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CEX}	Output Voltage	80	V
$V_{CE(sus)}$	Output Sustaining Voltage	50	V
I_O	Output Current	1.75	A
V_i	Input Voltage for **ULN2075B – 2077B** for **ULN2067B – 2071B** for **ULN2065B – 2069B**	60 30 15	V V V
I_I	Input Current	25	mA
V_s	Supply Voltage for **ULN2069B** for **ULN2071B**	10 20	V V
P_{tot}	Power Dissipation : at T_{pins} = 90 °C at T_{amb} = 70 °C	4.3 1	W W
T_{amb}	Operating Ambient Temperature Range	– 20 to 85	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

SCHEMATIC DIAGRAM



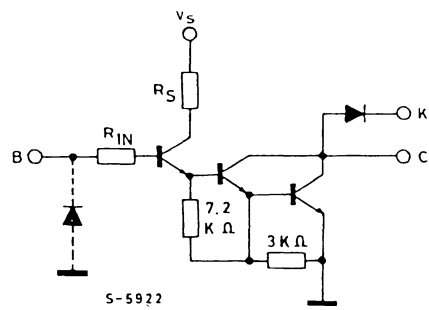
ULN2065B : R_{IN} = 350 Ω
ULN2067B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	for **ULN2065B – ULN2067B**					
		V_{CE} = 80 V			100	µA	1
		V_{CE} = 80 V T_{amb} = 70 °C			500	µA	
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2065B – ULN2067B** I_C = 100 mA V_I = 0.4 V	50			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 500 mA I_B = 625 µA			1.1	V	3
		I_C = 750 mA I_B = 935 µA			1.2	V	
		I_C = 1 A I_B = 1.25 mA			1.3	V	
		I_C = 1.25 A I_B = 2 mA			1 4	V	
		for **ULN2065B – ULN2067B**					
		I_C = 1.5 A I_B = 2.25 mA			1.5	V	
$I_{I(on)}$	Input Current	for **ULN2065B** V_I = 2.4 V	1 4		4.3	mA	4
		for **ULN2065B** V_I = 3.75 V	3.3		9 6	mA	
		for **ULN2067B** V_I = 5 V	0.6		1.8	mA	
		for **ULN2067B** V_I = 12 V	1.7		5.2	mA	
$V_{I(on)}$	Input Voltage	for **ULN2065B**					5
		V_{CE} = 2 V I_C = 1 A			2	V	
		V_{CE} = 2 V I_C = 1.5 A			2.5	V	
		for **ULN2067B**					
		V_{CE} = 2 V I_C = 1 A			6.5	V	
		V_{CE} = 2 V I_C = 1 5 A			10	V	
t_{PLH}	Turn-on Delay Time	0.5 V_I to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_I to 0.5 V_o			1.5	µs	
I_R	Clamp Diode Leakage Current	for **ULN2065B – ULN2067B**					6
		V_R = 80 V			50	µA	
		V_R = 80 V T_{amb} = 70 °C			100	µA	
V_F	Clamp Diode Forward Voltage	I_F = 1 A			1.75	V	7
		I_F = 1.5 A			2	V	

Notes : 1 Input voltage is with reference to the substrate (no connection to any other pins) for the ULN2075B and ULN2077B reference is ground for all other types
2 Input current may be limited by maximum allowable input voltage.

SCHEMATIC DIAGRAM

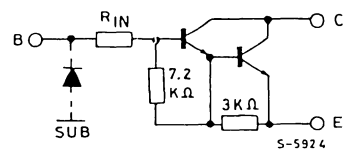


ULN2069B : R_{IN} = 2.5 KΩ, R_S = 900 Ω
ULN2071B : R_{IN} = 11.6 KΩ, R_S = 3.4 KΩ

ELECTRICAL CHARACTERISTICS (V_s = 5 V for ULN2069B, V_s = 12 V for ULN2071B, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	for **ULN2069B – ULN2071B**					
		V_{CE} = 80 V			100	µA	1
		V_{CE} = 80 V T_{amb} = 70 °C			500	µA	
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2069B – ULN2071B** I_C = 100 mA V_I = 0.4 V	50			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	for **ULN2069B**					2
		I_C = 500 mA V_I = 2.75 V			1.1	V	
		I_C = 750 mA V_I = 2.75 V			1.2	V	
		I_C = 1 A V_I = 2.75 V			1.3	V	
		I_C = 1.25 A V_I = 2.75 V			1.4	V	
		I_C = 1.5 A V_I = 2.75 V			1.5	V	
		for **ULN2071B**					
		I_C = 500 mA V_I = 5 V			1.1	V	
		I_C = 750 mA V_I = 5 V			1.2	V	
		I_C = 1 A V_I = 5 V			1.3	V	
		I_C = 1.25 A V_I = 5 V			1.4	V	
		I_C = 1.5 A V_I = 5 V			1.5	V	
$I_{I(on)}$	Input Current	for **ULN2069B** V_I = 2.75 V			550	µA	4
		for **ULN2069B** V_I = 3.75 V			1000	µA	
		for **ULN2071B** V_I = 5 V			400	µA	
		for **ULN2071B** V_I = 12 V			1250	µA	
$V_{I(on)}$	Input Voltage	V_{CE} = 2 V I_C = 1.5 A					5
		for **ULN2069B**			2.75	V	
		for **ULN2071B**			5		
I_S	Supply Current	for **ULN2069B**					8
		I_C = 500 mA V_I = 2.75 V			6	mA	
		for **ULN2071B**					
		I_C = 500 mA V_I = 5 V			4.5	mA	
t_{PLH}	Turn-on Delay Time	0.5 V_I to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_I to 0.5 V_o I_C = 1.25 A			1.5	µs	
I_R	Clamp Diode Leakage Current	for **ULN2069B – ULN2071B**					6
		V_R = 80 V			50	µA	
		V_R = 80 V T_{amb} = 70 °C			100	µA	
V_F	Clamp Diode Forward Voltage	I_F = 1 A			1.75	V	7
		I_F = 1.5 A			2	V	

SCHEMATIC DIAGRAM



ULN2075B : R_{IN} = 350 Ω
ULN2077B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	for **ULN2075B – ULN2077B**					
		V_{CE} = 80 V			100	µA	1
		V_{CE} = 80 V T_{amb} = 70 °C			500	µA	
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2075B – ULN2077B** I_C = 100 mA V_I = 0.4 V	50			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 500 mA I_B = 625 µA			1.1	V	3
		I_C = 750 mA I_B = 935 µA			1.2	V	
		I_C = 1 A I_B = 1.25 mA			1.3	V	
		I_C = 1.25 A I_B = 2 mA			1.4	V	
		for **ULN2075B – ULN2077B**					
		I_C = 1.5 A I_B = 2.25 mA			1.5	V	
$I_{I(on)}$	Input Current	for **ULN2075B** V_I = 2.4 V	1.4		4.3	mA	4
		for **ULN2075B** V_I = 3.75 V	3.3		9.6	mA	
		for **ULN2077B** V_I = 5 V	0.6		1.8	mA	
		for **ULN2077B** V_I = 12 V	1.7		5.2	mA	
$V_{I(on)}$	Input Voltage	for **ULN2075B**					5
		V_{CE} = 2 V I_C = 1 A			2	V	
		V_{CE} = 2 V I_C = 1.5 A			2.5	V	
		for **ULN2077B**					
		V_{CE} = 2 V I_C = 1 A		-	6.5	V	
		V_{CE} = 2 V I_C = 1.5 A			10	V	
t_{PLH}	Turn-on Delay Time	0.5 V_I to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_I to 0.5 V_o			1.5	µs	

TEST CIRCUITS

Figure 1.

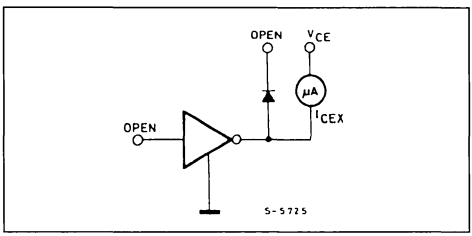


Figure 2.

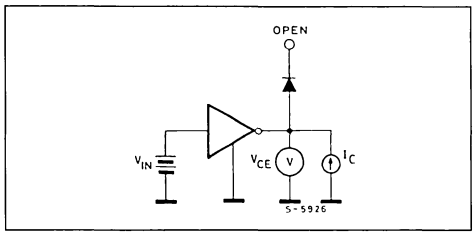


Figure 3.

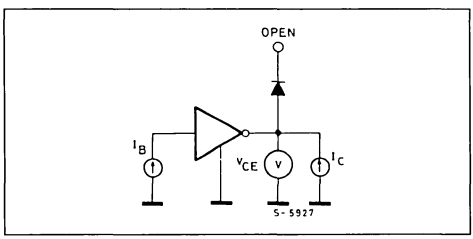


Figure 4.

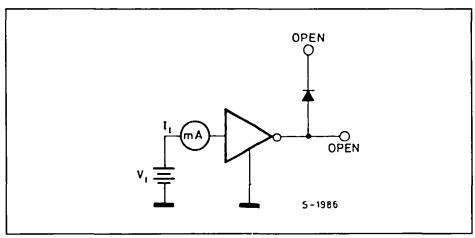


Figure 5.

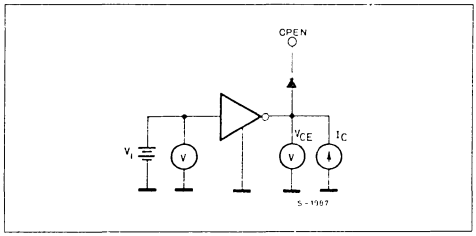


Figure 6.

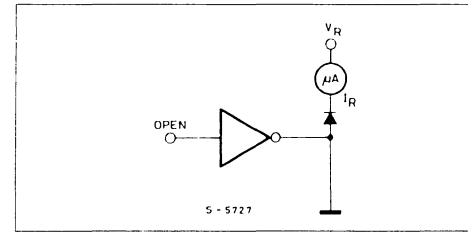


Figure 7.

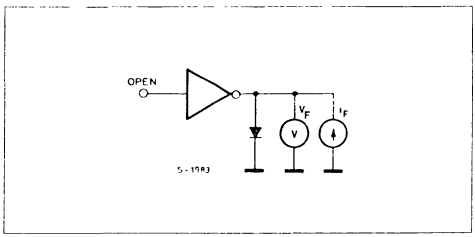


Figure 8.

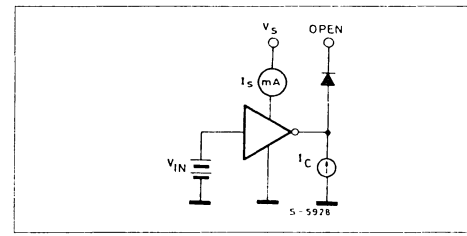


Figure 9 : Input Current as a Function of Input Voltage.

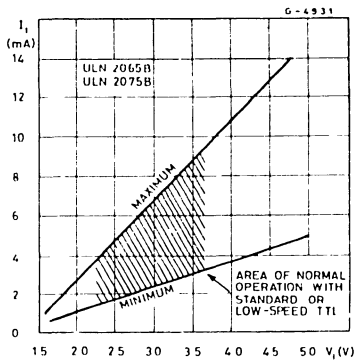


Figure 10 : Input Current as a Function of Input Voltage.

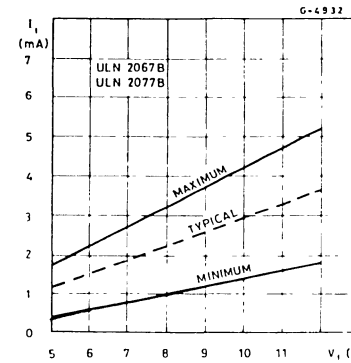
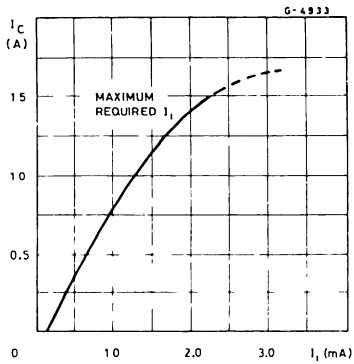


Figure 11 : Collector Current as a Function of Input Current.



MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 12) or to an external heatsink (Fig. 13).

The diagram of figure 14 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35 μ (1.4 mils).

During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 12 : Example of P.C. Board Area which is Used as Heatsink.

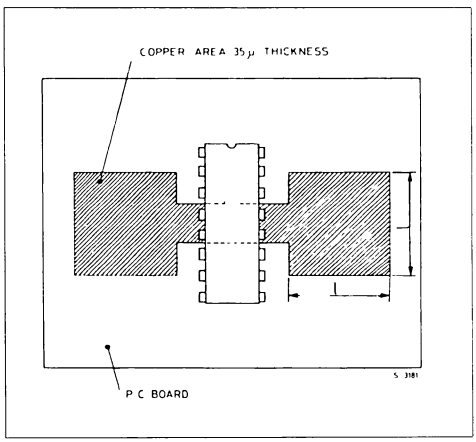


Figure 13 : External Heatsink Mounting Example.

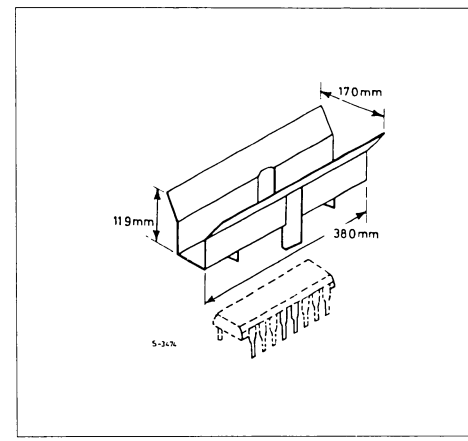


Figure 14 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side "l".

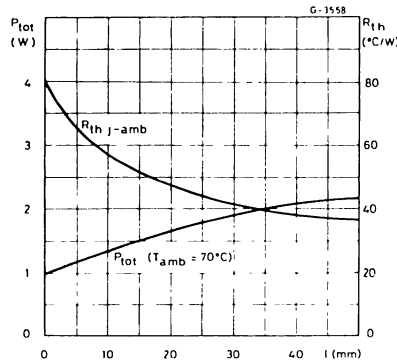
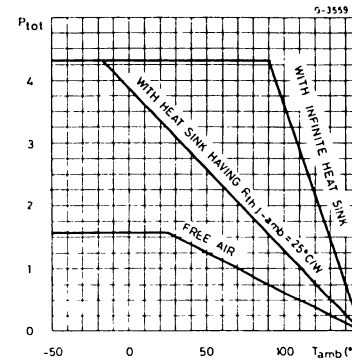


Figure 15 : Maximum Allowable Power Dissipation vs. Ambient Temperature.



SGS-THOMSON MICROELECTRONICS

ULN2801A ULN2802A ULN2803A ULN2804A ULN2805A

EIGHT DARLINGTON ARRAYS

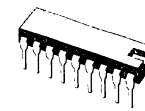
- EIGHT DARLINGTONS WITH COMMON EMITTERS
- OUTPUT CURRENT TO 500 mA
- OUTPUT VOLTAGE TO 50 V
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR ALL POPULAR LOGIC FAMILIES
- OUTPUT CAN BE PARALLELED
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY BOARD LAYOUT

DESCRIPTION

The ULN2801A-ULN2805A each contain eight darlington transistors with common emitters and integral suppression diodes for inductive loads. Each darlington features a peak load current rating of 600 mA (500 mA continuous) and can withstand at least 50 V in the off state. Outputs may be paralleled for higher current capability.

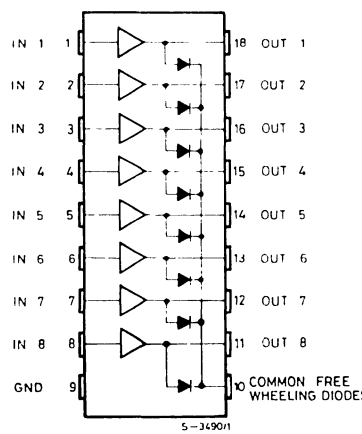
Five versions are available to simplify interfacing to standard logic families : the ULN2801A is designed for general purpose applications with a current limit resistor : the ULN2802A has a 10.5 KΩ input resistor and zener for 14-25 V PMOS ; the ULN2803A has a 2.7 KΩ input resistor for 5 V TTL and CMOS ; the ULN2804A has a 10.5 KΩ input resistor for 6-15 V CMOS and the ULN2805A is designed to sink a minimum of 350 mA for standard and Schottky TTL where higher output current is required.

All types are supplied in a 18-lead plastic DIP with a copper lead from and feature the convenient input-opposite-output pinout to simplify board layout.



DIP-18
(Plastic)

CONNECTION DIAGRAM (top view)

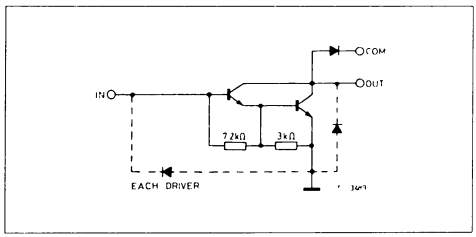


ABSOLUTE MAXIMUM RATINGS

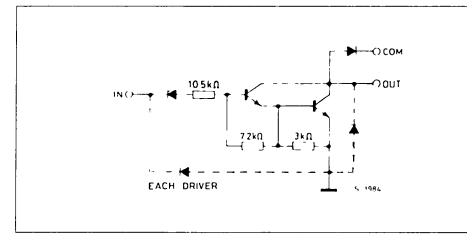
Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_i	Input Voltage for ULN2802A, 2803A, 2804A for ULN2805A	30 15	V V
I_C	Continuous Collector Current	500	mA
I_B	Continuous Base Current	25	mA
P_{tot}	Power Dissipation (one Darlington pair) (total package)	1 0 2.25	W W
T_{amb}	Operating Ambient Temperature Range	– 20 to 85	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

SCHEMATIC DIAGRAM AND ORDER CODES

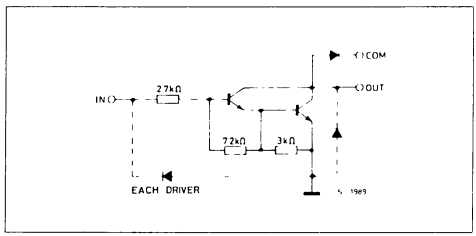
For ULN2801A (each driver for PMOS-CMOS)



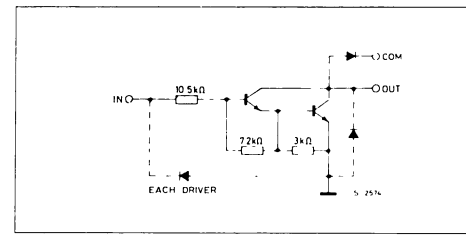
For ULN2802A (each driver for 14-15 V PMOS)



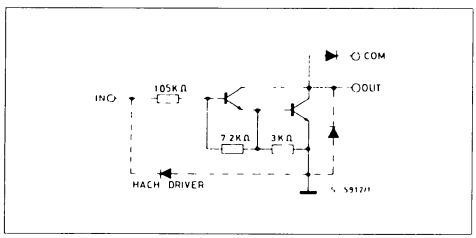
For ULN2803A (each driver for 5 V, TTL/CMOS)



For ULN2804A (each driver for 6-15 V CMOS/PMOS



For ULN2805A (each driver for high out TTL)



THERMAL DATA

$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	Max.	55	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 50 V			50	µA	1a
		T_{amb} = 70 °C V_{CE} = 50 V			100	µA	1a
		T_{amb} = 70 °C for **ULN2802A**					
		V_{CE} = 50 V V_i = 6 V			500	µA	1b
		for **ULN2804A**					
		V_{CE} = 50 V V_i = 1 V			500	µA	1b
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 100 mA I_B = 250 µA		0.9	1.1	V	
		I_C = 200 mA I_B = 350 µA		1.1	1.3	V	2
		I_C = 350 mA I_B = 500 µA		1.3	1.6	V	
$I_{i(on)}$	Input Current	for **ULN2802A** V_i = 17 V		0.82	1.25	mA	
		for **ULN2803A** V_i = 3.85 V		0.93	1.35	mA	
		for **ULN2804A** V_i = 5 V		0.35	0.5	mA	3
		V_i = 12 V		1	1.45	mA	
		for **ULN2805A** V_i = 3 V		1.5	2.4	mA	
$I_{i(off)}$	Input Current	T_{amb} = 70 °C I_C = 500 µA	50	65		µA	4
$V_{i(on)}$	Input Voltage	for **ULN2802A**					
		V_{CE} = 2 V I_C = 300 mA			13	V	
		for **ULN2803A**					
		V_{CE} = 2 V I_C = 200 mA			2.4	V	
		V_{CE} = 2 V I_C = 250 mA			2.7	V	
		V_{CE} = 2 V I_C = 300 mA			3	V	
		for **ULN2804A**					5
		V_{CE} = 2 V I_C = 125 mA			5	V	
		V_{CE} = 2 V I_C = 200 mA			6	V	
		V_{CE} = 2 V I_C = 275 mA			7	V	
		V_{CE} = 2 V I_C = 350 mA			8	V	
		for **ULN2805A**					
		V_{CE} = 2 V I_C = 350 mA			2.4	V	
h_{FE}	DC Forward Current Gain	for **ULN2801A**					
		V_{CE} = 2 V I_C = 350 mA	1000			–	2
C_i	Input Capacitance			15	25	pF	–
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	–
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	–
I_R	Clamp Diode Leakage Current	V_R = 50 V			50	µA	6
		T_{amb} = 70 °C V_R = 50 V			100	µA	
V_F	Clamp Diode Forward Voltage	I_F = 350 mA		1.7	2	V	7

TEST CIRCUITS

Figure 1a.

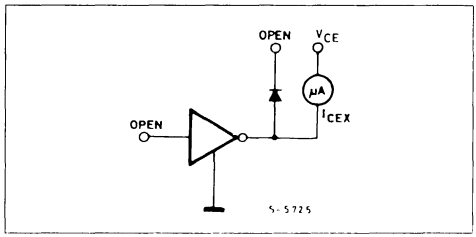


Figure 1b.

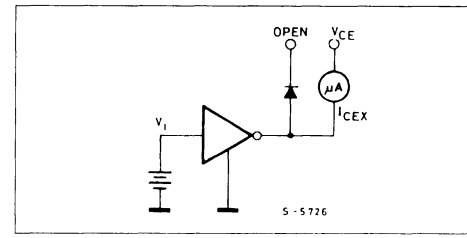


Figure 2.

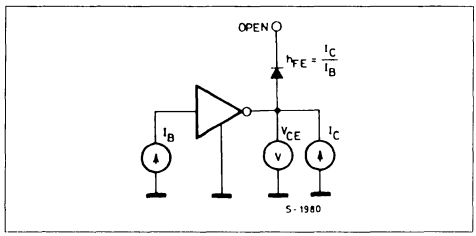


Figure 3.

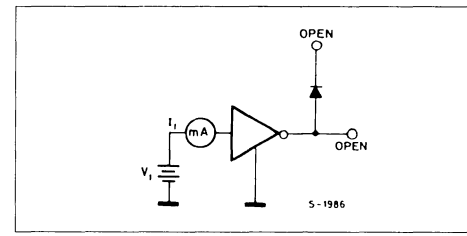


Figure 4.

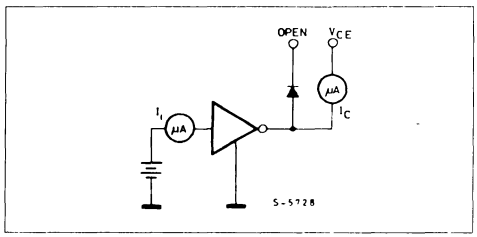


Figure 5.

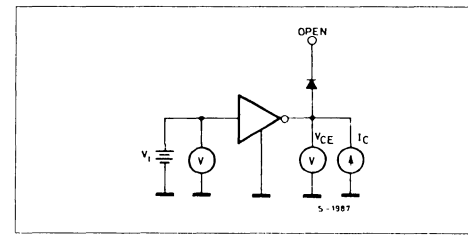


Figure 6.

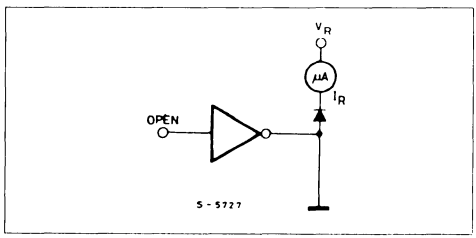


Figure 7.

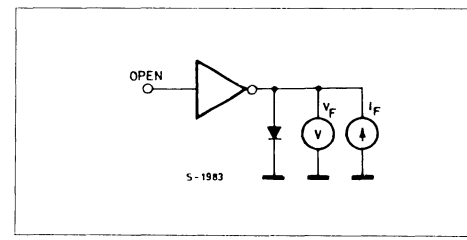


Figure 8 : Collector Current as a Function of Saturation Voltage.

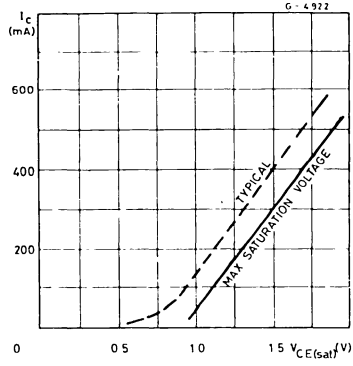


Figure 9 : Collector Current as a Function of Input Current.

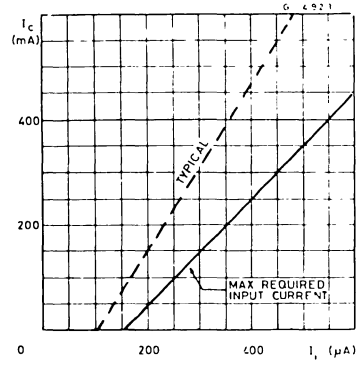


Figure 10 : Allowable Average Power Dissipation as a Function of Ambient Temperature.

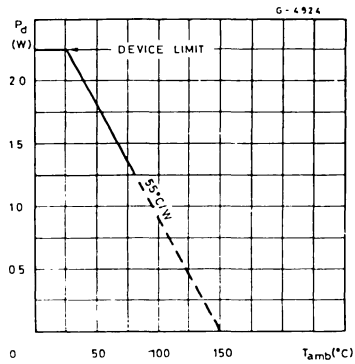


Figure 11 : Peak Collector Current as a Function of Duty Cycle.

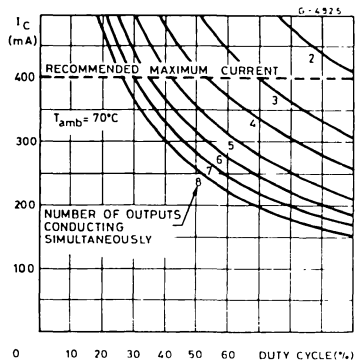


Figure 12 : Peak Collector Current as a Function of Duty.

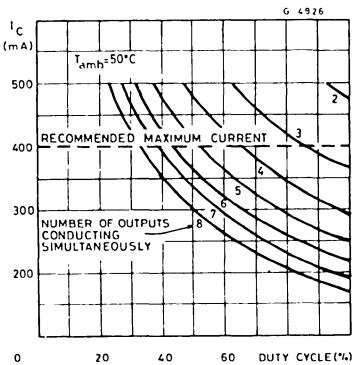


Figure 13 : Input Current as a Function of Input Voltage (for ULN2802A).

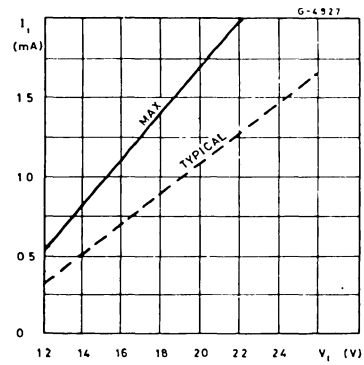


Figure 14 : Input Current as a Function of Input Voltage (for ULN2804A)

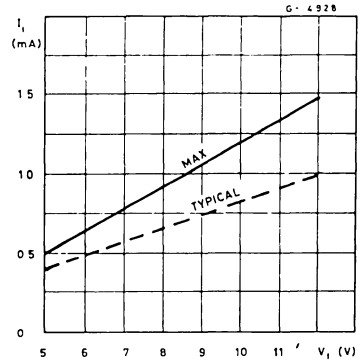


Figure 15 : Input Current as a Function of Input Voltage (for ULN2803A)

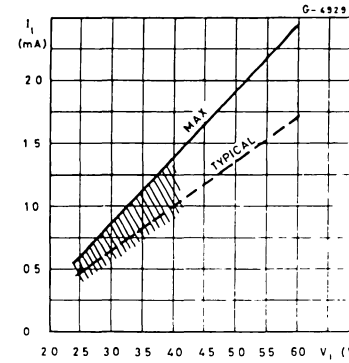
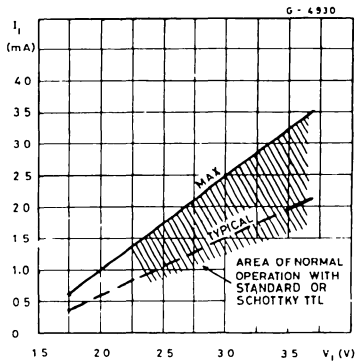


Figure 16 : Input Current as a Function of Input Voltage (for ULN2805A)

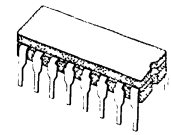


SGS-THOMSON
MICROELECTRONICS

ULQ2001R/2R
ULQ2003R/4R

SEVEN DARLINGTON ARRAYS

- SEVEN DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 500 mA PER DRIVER (600 mA PEAK)
- OUTPUT VOLTAGE 50 V
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUT CAN BE PARRALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT



DIP-16 Ceramic

DESCRIPTION

The ULQ2001R, ULQ2002R, ULQ2003R and ULQ2004R are high voltage, high current darlington arrays each containing seven open collector darlington pairs with common emitters. Each channel is rated at 500 mA and can withstand peak currents of 600 mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

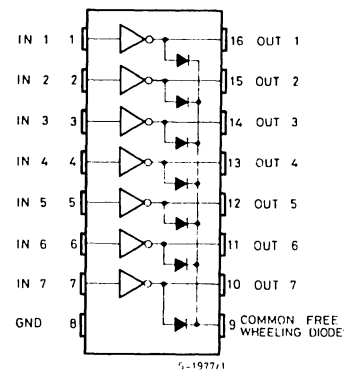
The four versions interface to all common families.

ULQ2001R	General Purpose, DTL, TTL, CMOS
ULQ2002R	15-25 V PMOS
ULQ2003R	5 V TTL, CMOS
ULQ2004R	6-15 V CMOS, PMOS

These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays, filament lamps, thermal printheads and high power buffers.

The ULQ2001R, ULQ2002R, ULQ2003R and ULQ 2004R are supplied in 16 pin ceramic DIP packages.

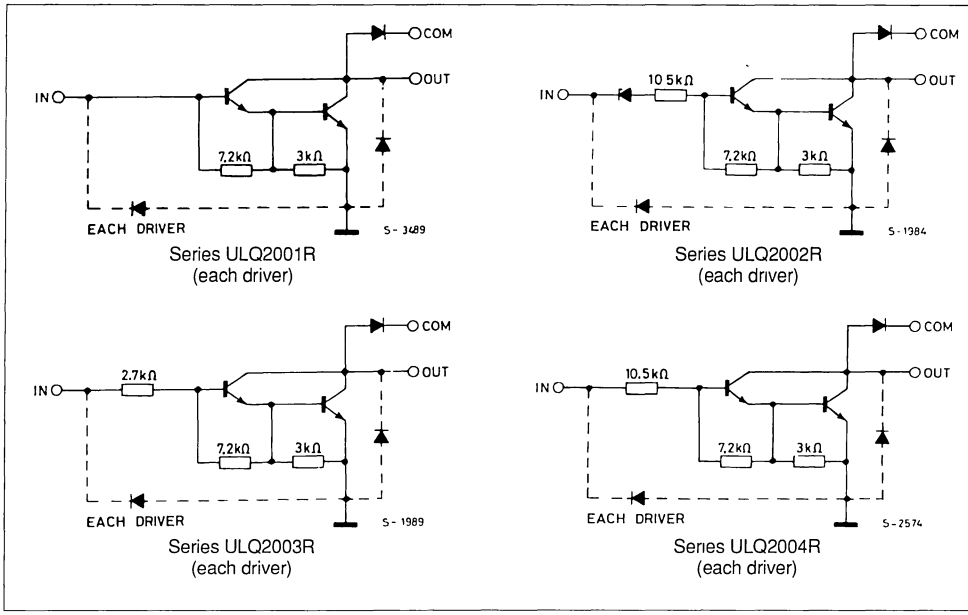
PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_{in}	Input Voltage (for ULQ2002R/2003R/2004R)	30	V
I_c	Continuous Collector Current	500	mA
I_b	Continuous Base Current	25	mA
T_{amb}	Operating Ambient Temperature Range	− 20 to + 85	C
T_{stg}	Storage Temperature Range	− 55 to 150	C

SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	150	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb}= 25° C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 50 V				50	µA	1a
		T_{amb} = 70 °C	V_{CE} = 50 V			100	µA	1a
		T_{amb} = 70 °C for **ULQ2002R**						
		V_{CE} = 50 V	V_i = 6 V			500	µA	1b
		for **ULQ2004R**						
		V_{CE} = 50 V	V_i = 1 V			500	µA	1b
$V_{CE\ (sat)}$	Collector-emitter Saturation Voltage	I_C = 100 mA	I_B = 250 µA		0.9	1.1	V	2
		I_C = 200 mA	I_B = 350 µA		1.1	1.3	V	2
		I_C = 350 mA	I_B = 500 µA		1.3	1.6	V	2
$I_{i(on)}$	Input Current	for **ULQ2002R**	V_i = 17 V		0.82	1.25	mA	3
		for **ULQ2003R**	V_i = 3.85 V		0.93	1.35	mA	3
		for **ULQ2004R**	V_i = 5 V		0.35	0.5	mA	3
		V_i = 12 V			1	1.45	mA	3
$I_{i(off)}$	Input Current	T_{amb} = 70 °C	I_C = 500 µA	50	65		µA	4
$V_{I(on)}$	Input Voltage	for **ULQ2002R**						
		V_{CE} = 2 V	I_C = 300 mA			13	V	5
		for **ULQ2003R**						
		V_{CE} = 2 V	I_C = 200 mA			2.4	V	5
		V_{CE} = 2 V	I_C = 250 mA			2.7	V	5
		V_{CE} = 2 V	I_C = 300 mA			3	V	
		for **ULQ2004R**						5
		V_{CE} = 2 V	I_C = 125 mA			5	V	
		V_{CE} = 2 V	I_C = 200 mA			6	V	5
		V_{CE} = 2 V	I_C = 275 mA			7	V	5
		V_{CE} = 2 V	I_C = 350 mA			8	V	5
h_{FE}	DC Forward Current Gain	for **ULQ2001R**						
		V_{CE} = 2 V	I_C = 350 mA	1000			-	2
C_i	Input Capacitance				15	25	pF	-
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			0.25	1	µs	-
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o			0.25	1	µs	-
I_R	Clamp Diode Leakage Current	V_R = 50 V				50	µA	6
		T_{amb} = 70 °C	V_R = 50 V			100	µA	6
V_F	Clamp Diode Forward Voltage	I_F = 350 mA			1.7	2	V	7

TEST CIRCUITS

Figure 1a.

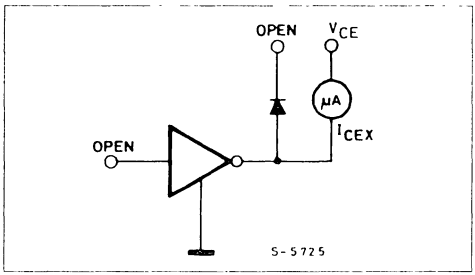


Figure 1b.

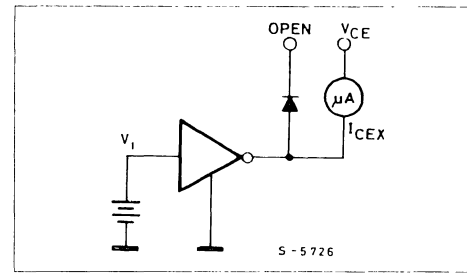


Figure 2.

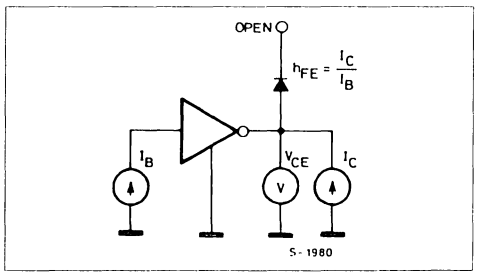


Figure 3.

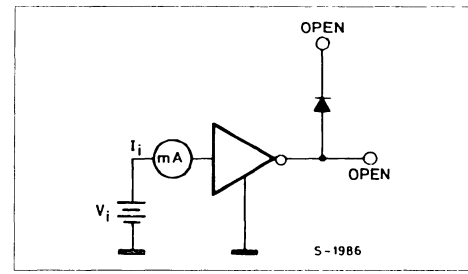


Figure 4.

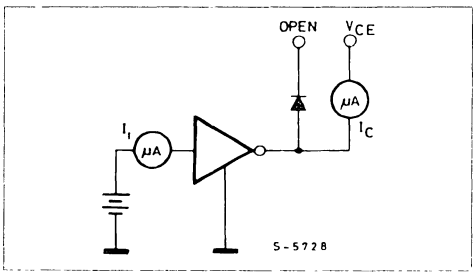


Figure 5.

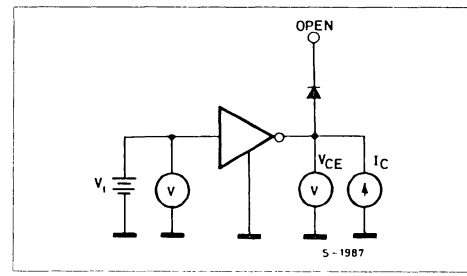


Figure 6.

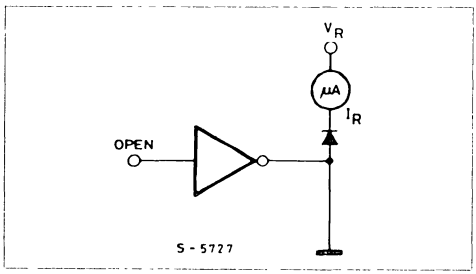
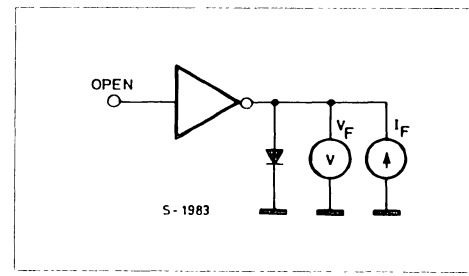


Figure 7.



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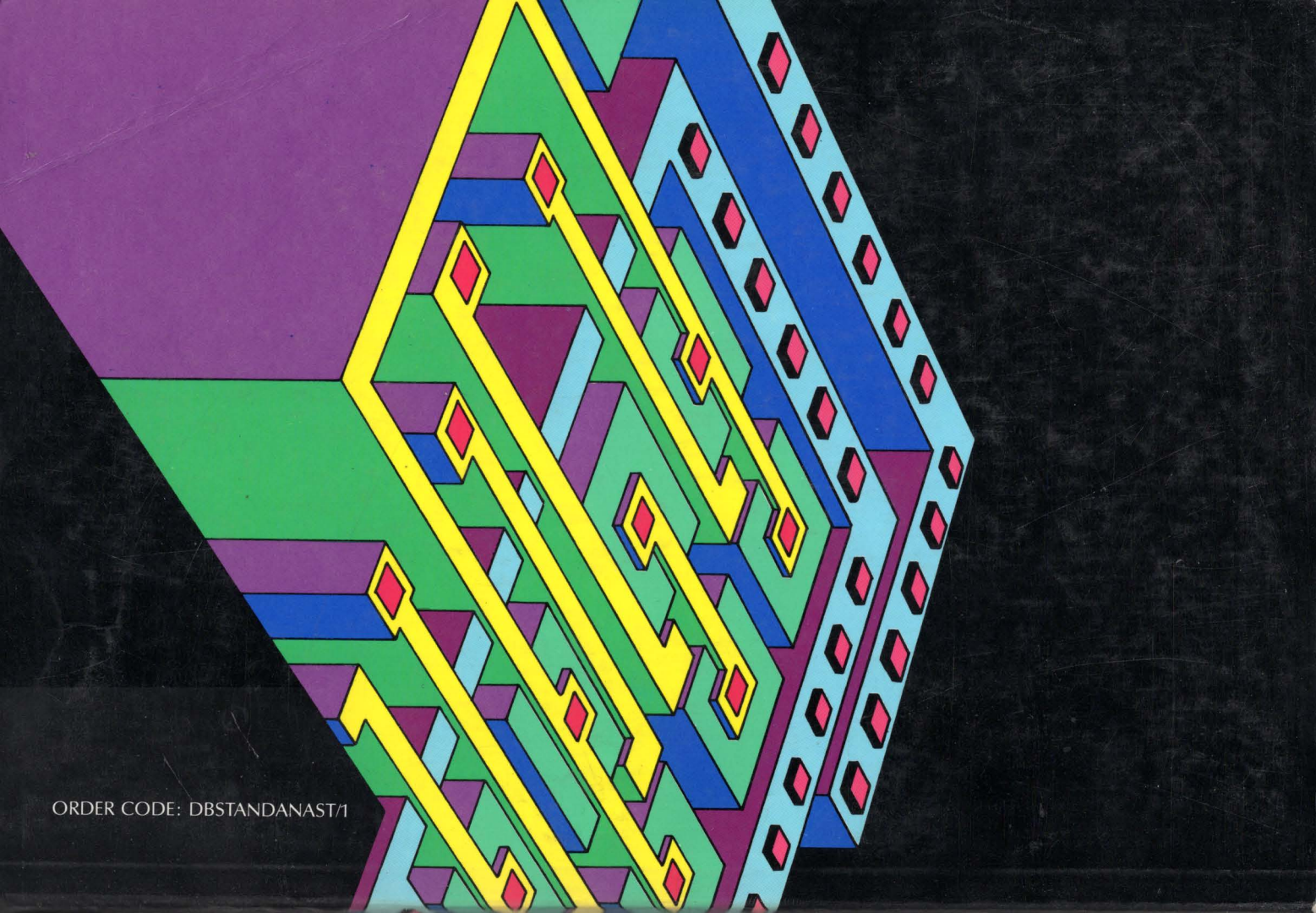

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