STATIC RAMs

DATABOOK

1st EDITION

inmos®

STATIC RAMs
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OMSON ONICS

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DATABOOK

1st EDITION

NOVEMBER 1989

INMOS is a member of the SGS-THOMSON Microelectronics group

USE IN LIFE SUPPORT DEVICES FOR SYSTEMS MUST BE EXPRESSLY AUTHORIZED

SGS-THOMSON PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

TABLE OF CONTENTS

INTRODUCTION

The SGS-THOMSON Microelectronics Group SRAM Databook is a comprehensive collection of information on advanced, high density, high speed SRAM products for specific applications. SGS-THOMSON Microelectronics is a major supplier of a wide range of semiconductor devices, and commands leading market positions in Intelligent Power, Power Transistors, and EPROM Memories. The recent acquisition of INMOS has strengthened SGS-THOMSON's portfolio. INMOS, based in the UK, manufactures very fast SRAMs, microprocessors called transputers, color graphics products, and digital signal processing devices.

STATIC RAMs

The SGS-THOMSON Group offer static RAM products which cover Standard SRAMs, Biport™ devices, Zeropower™ Timekeeper™ RAMs, and Cache Tag RAMs.

* Standard SRAM memories with a device density range of 4K bits to 1024k bits and performance from 15ns to 200ns. Organizational flexibility (4K x 1, 1K x 4, 16K x 1, 4K x 4, 64K x 1, 16K x 4, 8K x 8, 8K x 9, 256K x 1, 64K x 4, 32k x 8, 128k x 8) covers a vast range of applications, including large mainframes, high speed controllers, communications, graphics display and workstations.

* BIPORT™ devices consist of a family of FIFO (First-In First-Out) buffers. These FIFOs provide an interface between digital information paths with widely varying speeds. Each information source can thus operate at its own intrinsic speed, while results are processed or distributed at speed from 25ns to 200ns. The Biport™ FIFO family also includes single chip bidirectional FIFOs, and clocked FIFOs running at up 40 MHz

* The Cache-Tag family consists of devices, like very fast SRAMs with on board comparators, called TAGRAMs. A TAGRAM™ is that part of a cache subsystem that determines if data or instructions is retained in the cache memory (data cache). SGS-THOMSON offers various organizations x4, x8 and x20 and speed as fast as 12ns.

* The Zeropower™ and Timekeeper™ RAM family combines the operating simplicity of conventional byte-wide SRAMs with the excellent data integrity of Zeropower™ technology. This integrity is achieved, thanks to the use of advanced CMOS technology and long-life lithium cells. With density from 2k x 8 to 32k x 8 and access/cycle from 55ns to 200ns, SGS-THOMSON covers the full range of non-volatile needs for all microprocessor based systems. Thanks to the combined features of Zeropower™ technology with an on chip real-time clock, Timekeeper™ RAM offer unparalleled non-volatile performances while maintaining standard pin-out. Applications include RAM - clock/timer for communication, industrial systems, PCs, workstations.

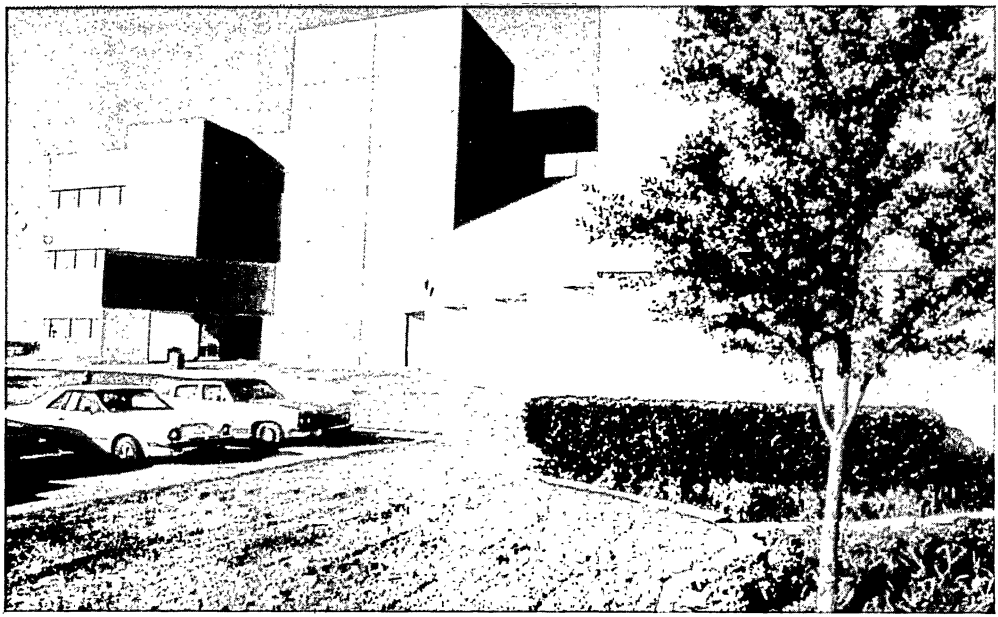
PRODUCTION

There are two facilities which presently manufacture the SRAM product line, Newport (UK) and Carrollton (USA). The Newport facility is an 8000 square meter building with a 3000 square meter clean room operating to Class 10 environment in the work areas. The facility operates a 4" wafer line and has the capacity to upgrade to a 6" sub micron capability. The Carrollton facility has a 5000 square meter class 100 4" wafer line and a 700 square meter class 10 6" wafer line with sub-micron capability. Additional manufacturing capacity is available in Rousset, France where both a 4 and 5" line are in operation.

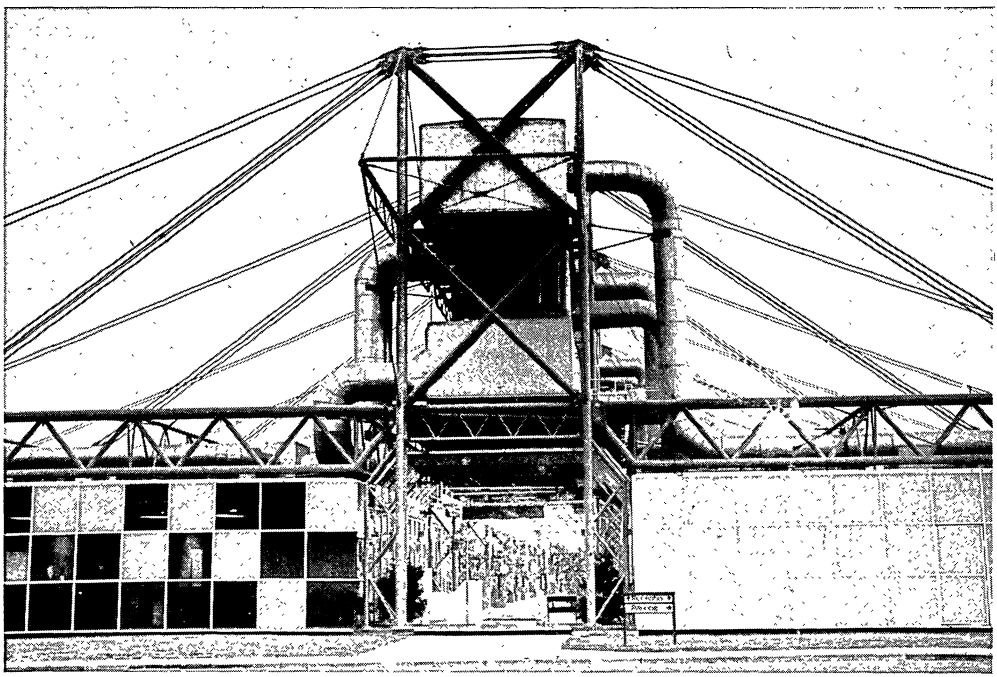
Advanced manufacturing equipment is used in these facilities to produce high performance devices, some consisting of up to one million transistors. Wafer steppers, plasma etchers and ion implanters form the basis of fabrication.

SGS-THOMSON Muar (Malaysia) is the main in-house assembly facility for SRAM.

The in-house facilities used for final SRAM testing are located in Newport (UK), Colorado Springs (USA), Toa Payoh (Singapore) and Muar (Malaysia).



Carrolton, TX (USA)



Newport (UK)

MILITARY

Many of our static RAMs are available in military versions processed in full compliance with MIL-STD-883C. Additionally, several JAN qualified devices are available for some of the product lines.

We also supports the US Government Defense Electronics Supply Center (DESC) Standard Military Drawing (SMD) program and is an approved supplier of a range of the SMDs already established by DESC.

FUTURE DEVELOPMENTS

Research and Development
The SGS-THOMSON Group has achieved technical success based on a position of leadership in products and process technology in conjunction with substantial R&D investment which, in 1988, represented 20 percent of sales, well above the estimated worldwide average of 13 percent for the top 10 semiconductor manufacturers.
Process Developments
New process technologies are continuing to be developed for next generation products. Work is taking place now to scale present technologies while new sub micron CMOS technologies are being brought into production.
Package Developments
A wide selection of packages are available including plastic and ceramic DIP. Where surface mount technology is desirable, the package offerings include PLCC, LCC, SOIC, SOJ, and Flat-pack. Refer to the individual datasheets for a listing of the packages available for a particular device.

INTRODUCTION

The Quality and Reliability of a product depend on all the activities from the conception and design of a new product, through production and shipment, to the service given to the customers.

It is well known that Reliability must be designed into the product and the process. To manufacture consistently reliable high quality products, SGS-THOMSON Microelectronics believes that it is essential for everyone in the Group to appreciate the importance of maintaining and improving the levels of Quality and Reliability.

SGS-THOMSON has adopted a Total Quality Control approach which means that everyone in the Group must work to improve Quality.

With this approach problems can be solved at the stage where they arise, so that latent failures are not carried over to the next stage or to the finished product. Total Quality Control assures the conditions to avoid quality problems rather than simply eliminating defective finished products.

The following information describes in a precis form the SGS-THOMSON approach to Quality and Reliability. The subject is comprehensively detailed in the SGS-THOMSON Quality and Reliability publication SURE 5. This program is also applied totally to INMOS products.

QUALITY CULTURE

It is the precise choice of SGS-THOMSON to win its customers' trust via the establishment of a position of leadership for Service and Quality. The Group must therefore have a quality based culture.

This culture can be seen in the behavior of every person within the Group and in the way each person interacts with his or her fellow worker to establish new and ever more demanding goals. It is sustained and nurtured through well defined policies, procedures, training and, of paramount importance, through examples from the very highest Group management levels.

That quality is perceived as a company wide responsibility is no more obvious than in the field of training. An ongoing program called Total Quality Control, was begun in 1982 to improve all people and departments in the Group wherever the Group operates throughout the world.

Total Quality Control takes the position that it is not enough to believe that things must be done, you must be able to do them. To this end it has as its primary objectives:

* Promotion of the Total Quality Control concept
* Training on statistical tools for people from all departments
* The creation of technical work groups for specific quality improvement programs
* The introduction of Quality Circles

Fundamental to this program is the conviction that quality is not an option, it is an obligation and that everyone in the Group can, given suitable motivation and training, make a real contribution to overall improvements in quality levels.

From the very highest management levels and involving designers, engineers, production, supervisors and line operators in addition to Quality and Reliability people, the Total Quality Control program is focused on:

* Personal motivation
* Quality in design
* Reliability in design
* Improved Statistical Process Control
* Customer satisfaction

In addition quality circles have been set up within the Group. The first, in 1982, was in the Group's Far East factories, with the first Quality Circle Convention being held in Singapore on January 30th 1983.

Recently SGS-THOMSON has begun a new company wide campaign - Quality and Service Culture for Excellence - based on the premise that basic quality ideas and methodology, if applied properly, will give:

* Complete Customer satisfaction
* Zero defect products
* Minimum product costs

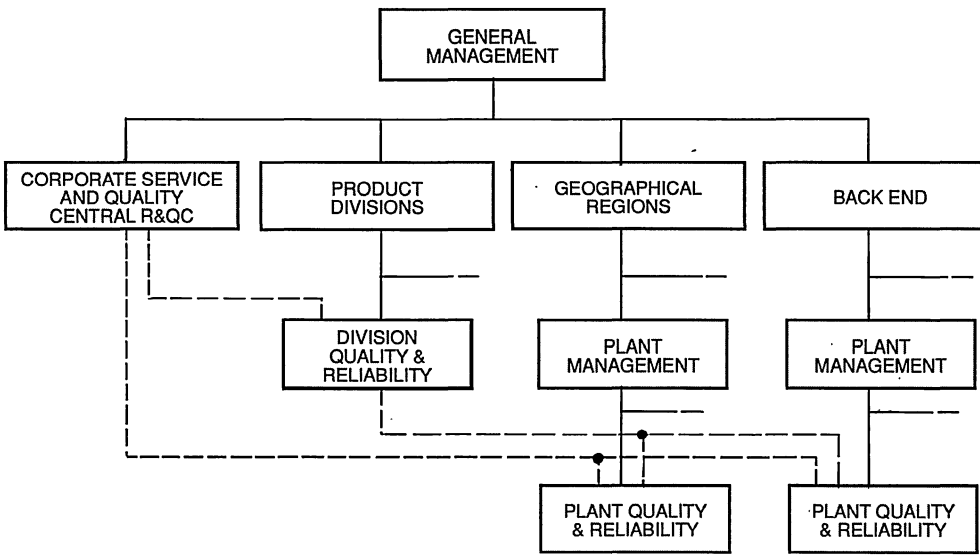
These three basic ingredients for excellence will be complemented by a long term program to improve data processing networks and to reduce response times at all levels as well as the localization of everyone's efforts on service, on quality and on process stability.

Our ultimate goal is to supply the products requested by our customers with zero delinquency, zero defects and of course "just in time".

ORGANIZATION AND MANAGEMENT

SGS-THOMSON is organized in product divisions, geographical sales areas (Regions) and Corporate departments.

Quality and Reliability control activities are managed, performed and promoted by the Corporate Service and Quality group (which reports to the top management) and Quality and Reliability departments at division and plant levels.



Part of Corporate Service and Quality group is the Central Reliability and Quality Control department. This organization makes it possible for SGS-THOMSON to handle Quality and Reliability for an extensive product range both effectively and efficiently.

Education and training programs in the field of Excellence and Quality are managed by the Corporate Service and Quality organization in cooperation with Human Resources department.

At every production location there is an incoming inspection department with the job of assuring the quality of purchased materials.
Division Q&R departments evaluate the reliability of new processes and new products, before they go into volume production.

They require and coordinate corrective actions necessary to improve Q&R of products and processes; these improvements are planned in quality budgets.
They perform and collect reliability results and issue reliability reports for their products.
Division Q&R departments interface directly with customers from design phase to approval of customers' product specifications.
In the past, successful in-house customer qualification, testing and joint qualification programs with customers has been achieved. SGS-THOMSON remains committed to these joint customer/vendor programs.

Plant Q&R departments perform all Quality and Reliability inspections and controls relevant to production done in their plants such as: incoming inspection, in process control, outgoing inspection, reliability testing and failure analysis.

QUALITY BY DESIGN

Since the Quality and Reliability of semiconductor devices depend to a large extent on the basic structure, SGS-THOMSON pays careful attention to Q&R studies at the design stage, paying deep attention to user's reliability requirements and operating conditions. Quality and Reliability checkpoints for materials, process and device structure are considered from the design phase on.

One of the key steps in the Design Review which consists of a study of design documents, the definition of reliability test methods to check on the compatibility of processes with design goals and conditions of use, and review of failure mechanism history in similar products.

In addition, qualification procedures are used mainly to ascertain the main characteristics of new processes/products (or to evaluate process/product changes) and to guarantee the availability of a characterization and the complete set of specifications for introduction to SGS-THOMSON manufacturing. Qualification should demonstrate capability to meet customer requirements.

QUALITY AUDITING

SGS-THOMSON performs quality audits to verify that products, processes, programs and the Quality and Reliability organizations are still in accordance with the written procedures and specifications.
A quality audit does not replace the normal quality monitors or acceptance but helps to ensure that everything is being done as it should be and to anticipate quality problems.
SGS-THOMSON factories are familiar with internal and external audits.

THE SPECIFICATION SYSTEM

Quality and Reliability are measurable features. But, for measurements to have any meaning, they must be carried out in accordance with strict procedures and methods. Similarly production processes must be managed in a repeatable way. This means that detailed instructions and descriptions of every process step must be prepared and kept updated.

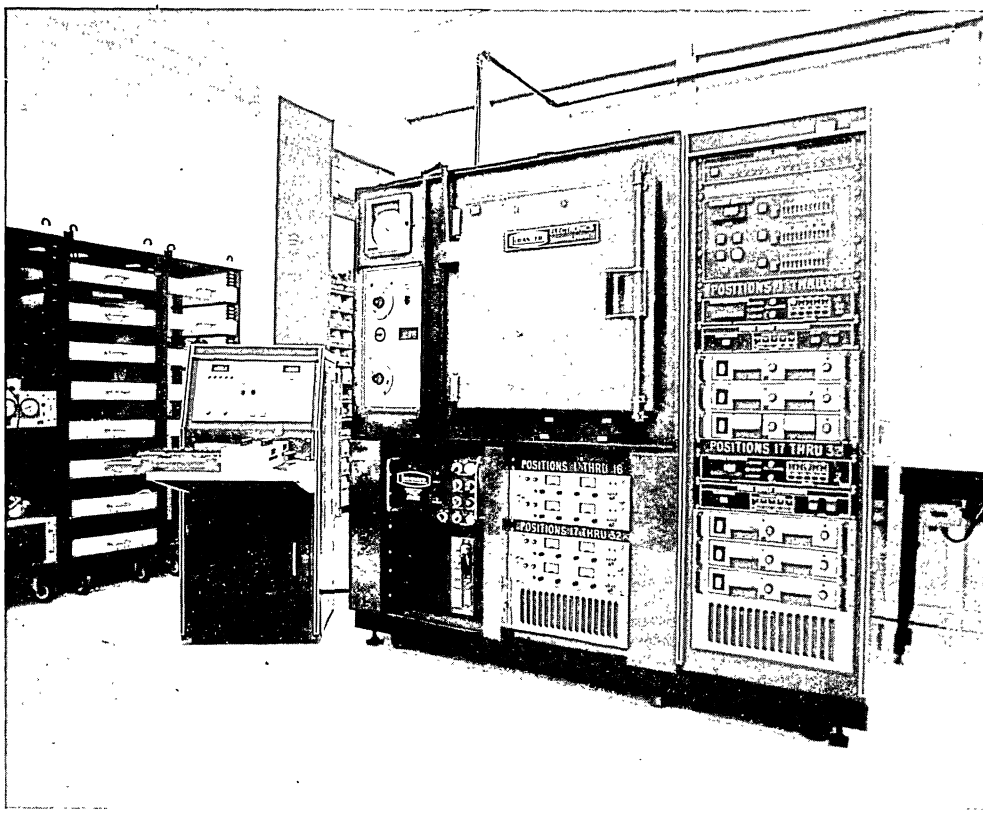
This information is formalized in the Group's specifications that cover all the procedures and process instructions. This the Specification System documents all the various manufacturing processes and encompasses the SGS-THOMSON technical know-how.

The Specification System consists of a series of documents properly organized by subject and content. The system is managed and administered by Document Control at Divisional Specification Centres for efficiently issuing, updating, approving and distributing specifications to all the relevant departments. Special text processing software is used to ensure rapid updating and distribution of specification documents. The Specification Centres guarantee homogeneity in specifications, record changes histories and issues general specification procedures.

A very strict Group procedure governs the engineering changes (issue, approval and modifications).

RELIABILITY ASSURANCE

Reliability testing is an ongoing process adopted to identify and then improve reliability performance.
Accelerated tests, such as extended temperature operating life, THB and temperature cycling, are important tools for evaluating long-term reliability and stability of process and product parameters.



MOS device life test equipment

SGS-THOMSON also performs rigorous tests throughout production to ensure that production devices have the properly designed reliability.
Reliability tests are conducted in two stages:

first we test our engineering samples during design and development stages to see if their Q&R corresponds to that called for in the design. Reliability testing is usually performed on a small sample but for long periods or under very accelerated conditions to investigate wear out failures and to determine tolerances and limits of design. For these tests it is also possible to use the step-stress procedure (eg ESD resistance evaluation);
the second type of test is performed periodically during production to check, maintain and improve the assured Quality and Reliability levels.

The reliability tests involve both environmental and endurance examination and are performed under conditions more severe than those met in the field. These conditions are chosen to accelerate the occurrence of failures that would appear in actual operation, and care is taken to ensure that the failure modes and mechanisms are unchanged. The data from reliability tests provide an objective tool for product performance evaluation under a wide range of conditions.

When a failure occurs, the SGS-THOMSON engineers conduct an in-depth analysis of the failure mechanism/mode to apply immediate suitable corrective actions.
Reliability testing activity during recent years has been extended to all SGS-THOMSON factories with new and advanced equipment enabling all the plants to perform all the main tests.

MILITARY PRODUCT PROGRAM

A Military Product Program has been developed to meet the increasingly demanding requirements for Class B memory product in accordance with paragraph 1.2.1 of MIL-STD-883 "Provisions for the use of MIL-STD-883 in conjunction with non-JAN devices".

Our MIL-STD-883 Class B product is screened to the specifications of Method 5004 with electrical testing executed over the military temperature range -55 C to + 125 C.

Each inspection lot is subjected to the requirements of method 5004 Group A Electrical sampling and Group B Mechanical and Environmental sample testing. Additionally, all new product and changes to product as defined in MIL-M-38510 paragraph 3.4.2 (major changes) is qualified per method 5005 Group C
(Die related) and Group D (Package related tests). Periodic Conformance Testing is carried out per the requirements of MIL-STD-883 paragraph 1.2.1 for all relevant die families and package types.

Full details of our military processing are included in a "General Military Processing Specification", which may be obtained upon request.

Suitability for use in specific applications should be determined by using the guidelines of MIL-STD-454.

By specifying one of our military products, the user is assured of a product which has been subjected to the full Screening and Quality Conformance requirements of paragraph 1.2.1 of MIL-STD-883 in addition to the full range of in-house process, test and quality control functions designed to enhance the quality and reliability of all products.

STANDARD MILITARY DRAWING PROGRAM

The in-house Standard Military Drawing (SMD) program was introduced in 1986 to supply military and governmental products. The SMD Program was implemented by the US Government and its associated subcontractors to provide the industry with a single SMD for each military IC requirement. These SMDs are intended to replace the multiplicity of Source Control Drawings (SCDs) generated by each contractor. Components specified according to the SMD Program are standard military MIL-STD-883 compliant devices.

SGS-THOMSON and other IC manufacturers, initiate the development of SMDs in conjunction with military contractors who have significant demand for the particular device. Together they initiate an SMD proposal which the Defense Electronics Supply Center (DESC) screens and approves. Accepted SMDs are then circulated by DESC to industry vendors and consumers to obtain multiple sources and registered users.

The SGS-THOMSON Group fully supports the Standard Military Drawing Program and the DESC efforts to expand its usage.

Refer to the cross reference information which lists each approved product by its SMD number and the corresponding part number

(unless otherwise specified all Static RAMs listed are produced in CMOS technology)

PRODUCT GUIDE

ZEROPOWERS

ORGANISATION DESCRIPTION	PART NUMBER	SPEEDns	ICCma			VCC	TEMP RANGE	PACKAGE
			ACTIVE mA@ns	TTL STBY	CMOS STBY			
– 2KX8	MK48Z02	120, 150, 200, 250	90	3	1	5V + 10 - 5%	0 to + 70°C	P DIP 24
– 2KX8 UL-CERTIFIED	MK48Z02BU	120, 150, 200, 250	90	3	1	5V + 10 - 5%	0 to + 70°C	P DIP 24
– 2K 8	MK48Z12	120, 150, 200, 250	90	3	1	5V + 10 - 10%	0 to + 70°C	P DIP 24
– 2KX8 UL-CERTIFIED	MK48Z12BU	120, 150, 200, 250	90	3	1	5V + 10 - 10%	0 to + 70°C	P DIP 24
– 2KX8	MKI48Z02	120, 150, 200, 250	90	3	1	5V + 10 - 5%	- 40 to + 85°C	P DIP 24
– 2KX8 UL-CERTIFIED	MKI48Z02BU	120, 150, 200, 250	90	3	1	5V + 10 - 5%	- 40 to + 85°C	P DIP 24
– 2KX8	MKI48Z12	120, 150, 200, 250	90	3	1	5V + 10 - 10%	- 40 to + 85°C	P DIP 24
– 2KX8 UL-CERTIFIED	MKI48Z12BU	120, 150, 200, 250	90	3	1	5V + 10 - 10%	- 40 to + 85°C	P DIP 24
– 2KX8 W/O BATTERY	MK48C02AN	150, 200, 250	90	3	1	5V + 10 - 5%	0 to + 70°C	P DIP 24
– 2KX8 W/O BATTERY	MK48C02AK	150, 200, 250	90	3	1	5V + 10 - 5%	0 to + 70°C	PLCC 32
– 8KX8 UL-CERTIFIED	MK48Z08	55,70	125@70	3	3	5V + 10 - 10%	0 to + 70°C	P DIP 28
		100, 150, 200	80@100					
– 8KX8 UL-CERTIFIED	MK48Z08BU	55,70	125@70	3	3	5V + 10 - 10%	0 to + 70°C	P DIP 28
		100, 150, 200	80@100					
– 8KX8	MK48Z18	55,70	125@70	3	3	5V + 10 - 10%	0 to + 70°C	P DIP 28
		100, 150, 200	80@100					
– 8KX8 UL-CERTIFIED	MK48Z18BU	55,70	125@70	3	3	5V + 10 - 10%	0 to + 70°C	P DIP 28
		100, 150, 200	80@100					
– 8KX8 PWR FAIL INT	MK48Z09	55,70	125@70	3	3	5V + 10 - 10%	0 to + 70°C	P DIP 28
		100, 150, 200	80@100					
– 8KX8 UL-CERTIFIED PWR FAIL INT	MK48Z09BU	55,70	125@70	3	3	5V + 10 - 10%	0 to + 70°C	P DIP 28
		100, 150, 200	80@100					
– 8KX8 PWR FAIL INT	MK48Z19	55,70	125@70	3	3	5V + 10 - 10%	0 to + 70°C	P DIP 28
		100, 150, 200	80@100					
– 8KX8 UL-CERTIFIED PWR FAIL INT	MK48Z19BU	55,70	125@70	3	3	5V + 10 - 10%	0 to + 70°C	P DIP 28
		100, 150, 200	80@100					
– 32KX8 10 YEARS -25°C	MK48Z30	100, 120, 150	90	5	2	5V + 10 - 5%	0 to + 70°C	P DIP 28
– 32KX8 10 YEARS -25°C	MK48Z30A	100, 120, 150	90	5	2	5V + 10 - 5%	0 to + 70°C	P DIP 28
– 32KX8 10 YEARS -70°C	MK48Z32	100, 120, 150	90	5	2	5V + 10 - 5%	0 to + 70°C	P DIP 28

TIMEKEEPERS

ORGANISATION DESCRIPTION	PART NUMBER	SPEEDns	ICCma			VCC	TEMP RANGE	PACKAGE
			ACTIVE mA@ns	TTL STBY	CMOS STBY			
– 2KX8	MK48T02	120, 150, 200, 250	80	5	3	5V + 10 - 5%	0 to + 70°C	P DIP 24
– 2KX8 UL-CERTIFIED	MK48T02BU	120, 150, 200, 250	80	5	3	5V + 10 - 5%	0 to + 70°C	P DIP 24
– 2KX8	MK48T12	120, 150, 200, 250	80	5	3	5V + 10 - 10%	0 to + 70°C	P DIP 24
– 2KX8 UL-CERTIFIED	MK48T12BU	150, 200, 250	80	5	3	5V + 10 - 10%	0 to + 70°C	P DIP 24
– 2KX8	MKI48T02	120, 150, 200, 250	80	5	3	5V + 10 - 5%	– 40 to + 85°C	P DIP 24
– 2KX8 UL-CERTIFIED	MKI48T02BU	120, 150, 200, 250	80	5	3	5V + 10 - 10%	– 40 to + 85°C	P DIP 24
– 8KX8	MK48T08	100, 150, 200	80	3	3	5V + 10 -5%	0 to + 70°C	P DIP 24
– 8KX8	MK48T18	100, 150, 200	80	3	3	5V + 10-10%	0 to + 70°C	P DIP 24
– PC REAL TIME CLOCK	MK48T87/87A	100	15	NA	NA	5V + 10 - 10%	0 to + 70°C	P DIP 24
–PC REAL TIME CLOCK W/O BATTERY	MK48T85Q	100	15	0,5	NA	5V + 10 - 10%	0 to + 70°C	PLCC 28

CACHETAG MEMORIES

ORGANISATION DESCRIPTION	PART NUMBER	SPEEDns	ICCma			VCC	TEMP RANGE	PACKAGE
			ACTIVE mA@ns	TTL STBY	CMOS STBY			
– 4KX4	MK41H80	20,22, 25, 35	120	NA	NA	5V + 10 - 10%	0 to + 70°C	P DIP 22
– 4KX4	MK41S80	12, 15	120	NA	NA	5V + 10 - 10%	0 to + 70°C	P DIP 22 /SOJ 24
– 2KX20	MK4202	20, 22, 25	250	50	NA	5V + 10 - 10%	0 to + 70°C	PLCC 68
– 8KX8	MK48S74	20, 22, 25	150	NA	NA	5V + 10 - 10%	0 to + 70°C	P DIP 28 /SOJ 28
8KX8 Totem Pole Output	MK48S80	20, 22, 25	150	NA	NA	5V + 10 - 10%	0 to + 70°C	P DIP 28 /SOJ 28
16KX4	MK44S80	15, 17, 20	150	NA	NA	5V + 10 - 10%	0 to + 70°C	P DIP 24 300 MIL

FIFO's

ORGANISATION DESCRIPTION	PART NUMBER	SPEEDns	ICCma			VCC	TEMP RANGE	PACKAGE
			ACTIVE mA@ns	TTL STBY	CMOS STBY			
– 512X9	MK4501	65, 80, 100, 120 150 & 200	80	8	NA	5V + 10 - 10%	0 to + 70°C	P DIP 28 /PLCC 32
– 512X9 FAST	MK45H01	25, 35, 50, 65, 120	120	12	NA	5V + 10 - 10%	0 to + 70°C	P DIP 28(1) /PLCC 32
– 1KX9 FAST	MK45H02	25, 35, 50, 65, 120	120	12	NA	5V + 10 - 10%	0 to + 70°C	P DIP 28(1) /PLCC 32
– 2KX9	MK4503	65, 80, 100, 120 150 & 200	120	12	NA	5V + 10 - 10%	0 to + 70°C	P DIP 28 /PLCC 32
– 2KX9 FAST	MK45H03	25, 35, 50, 65, 120	120	12	NA	5V + 10 - 10%	0 to + 70°C	P DIP 28(1) /PLCC 32
– 4KX9 FAST	MK45H04	25, 35, 50, 65, 120	120	12	NA	5V + 10 - 10%	0 to + 70°C	P DIP 28 (1)
– 8KX9 FAST	MK45H08	25, 35, 50, 65, 120	120	12	NA	5V + 10 - 10%	0 to + 70°C	P DIP 28
– 1KX9 clk 40MHz	MK4505 M	25, 33, 50	100	NA	NA	5V + 10 - 10%	0 to + 70°C	P DIP 24
MASTER & SLAVE	MK4505 S	25, 33, 50	100	NA	NA	5V + 10 - 10%	0 to + 70°C	P DIP 20
– 64X5X2	MK45264	55, 70	60	NA	NA	5V + 10 - 10%	0 to + 70°C	P DIP 24
BIDIRECTIONAL	MK45265	55, 70	60	NA	NA	5V + 10 - 10%	0 to + 70°C	P DIP 24

(1) 600 mil and 300 mil PDIP.

STATIC RAM

ORGANISATION DESRIPTION	PART NUMBER	SPEEDns	ICC ma			ICC_{DR} µA	VCC	TEMP RANGE	PACKAGE
			ACTIVE @ ns	TTL STBY	CMOS STBY				
– 4KX1	IMS1203	25, 35, 45	80	15	13		5V + 10-10%	0 °C to 70 °C	P DIP 18
– 1KX4	IMS1223	25, 35, 45	100	15	8		5V + 10-10%	0 °C to 70 °C	P DIP 18
– 2KX8	MK6116	150, 200, 250	70	3	1	1	5V + 10-10%	0 °C to + 70 ° C	P DIP 24 /SOIC 28
– 2KX8 LOW POWER	MK6116L	150, 200, 250	70	3	0.001	1	5V + 10-10%	0 °C to + 70 °C	P DIP 24 /SOIC 28
– 2KX8	MKI6116	150, 200, 250	55	3	1	1	5V + 10-10%	–40 ° C to + 105 ° C	P DIP 24 /SOIC 28
– 2KX8 LOW POWER	MKI6116L	150, 200, 250	55	3	0.01	1	5V + 10-10%	–40 ° C to + 105 ° C	P DIP 24 /SOIC 28
– 16KX1 FAST CS	MK41H66	20, 25, 35	120	10			5V + 10-10%	0 °C to + 70 °C	P DIP 20
– 16KX1	IMS1403	25, 35, 45, 55	75	15	10		5V + 10-10%	0 °C to 70 °C	P DIP/LCC 20
– 16KX1	MK41H67	20, 25, 35	120	10	0.05	50	5V + 10-10%	0 °C to + 70 °C	P DIP 20
– 4KX4	MK41H68	20, 25, 35	120	8	0.05	50	5V + 10-10%	0 °C to + 70 °C	P DIP 20
– 4KX4	IMS1423	25, 35, 45, 55	105@25 100@35	15	0.01		5V + 10-10%	0 °C to 70 °C	P DIP/LCC 20 SOJ 20
– 4KX4 FAST CS	MK41H69	20, 25, 35	120	8			5V + 10-10%	0 °C to + 70 °C	P DIP 20
– 4KX4 OE	MK41H78	20, 25, 35	120	10	0.05	50	5V + 10-10%	0 °C to + 70 °C	P DIP 22
– 4KX4 OE+FLASH CLR	MK41H79	20, 25, 35	120	16	0.05	50	5V + 10-10%	0 °C to + 70 °C	P DIP 22
– 64KX1	IMS1600	25, 35, 45, 55	77@25 70@35	25	15		5V + 10-10%	0 °C to + 70 °C	P DIP/LCC 22 SOJ 24
– 64KX1	IMS1601	35, 45, 55	70	15	5	100	5V + 10-10%	0 °C to + 70 °C	P DIP/LCC 22 SOJ 24
– 64KX1	IMS1605	15, 20, 25	100	25	10	350	5V + 10-10%	0 °C to + 70 °C	P DIP/LCC 22 SOJ 24
– 16KX4	IMS1620	25, 35, 45, 55	110@25 100@35	25	17		5V + 10-10%	0 °C to + 70 °C	P DIP/LCC 22 SOJ 24
– 16KX4	IMS1625	15, 20, 25	100	25	10	350	5V + 10-10%	0 °C to + 70 °C	P DIP/LCC 22 SOJ 24
– 16KX4 OE	IMS1624	25, 35, 45, 55	110@25 100@35	25	17		5V + 10-10%	0 °C to + 70 °C	P DIP/SOJ 24 LCC 28
– 16KX4 OE	IMS1629	15, 20, 25	100	25	10	350	5V + 10-10%	0 °C to + 70 °C	P DIP/SOJ 24 LCC 28
– 16KX4 OE Sep I/O	IMS1626/7	15, 20, 25	100	25	10	350	5V + 10-10%	0 °C to + 70 °C	P DIP/SOJ 28 LCC 28
– 8KX8 OE	IMS1630L	45, 55, 70, 100, 120	90	20	10	350	5V + 10-10%	0 °C to + 70 °C	P DIP /SOIC 28

STATIC RAM (Continued)

ORGANISATION DESCRIPTION	PART NUMBER	SPEEDns	ICC ma			ICC_{DR} µA	VCC	TEMP RANGE	PACKAGE
			ACTIVE @ ns	TTL STBY	CMOS STBY				
– 8KX8 OE	MK48H64	70, 120	100@70 90@120	5	500	500	5V + 10-10%	0 °C to + 70 °C	P DIP 28 /SOIC 28
– 8KX8 OE	MK48H64L	70, 120	100@70 90@120	5	0.05	25	5V + 10-10%	0 °C to + 70 ° C	P DIP 28 /SOIC 28
– 8KX8 OE	IMS1635	15, 20, 25	100	25	10	350	5V + 10-10%	0 °C to + 70 ° C	P DIP 28
– 8KX9 OE	MK48H89	20, 25, 35	120	25	1	500	5V + 10-10%	0 °C to + 70 ° C	P DIP 28
– 8KX9 OE	IMS1695	15, 20, 25	100	25	10	350	5V + 10-10%	0 °C to + 70 ° C	P DIP/SOJ 28 LCC 32
– 8KX8\9 PARITY	MK48H98\99	20, 30, 40	120	25	1	500	5V + 10-10%	0 °C to + 70 ° C	P DIP 28
– 256KX1	IMS1800	25, 30, 35, 45	120	30	15		5V + 10-10%	0 °C to + 70 ° C	P DIP/SOJ 24 LCC 28
– 64KX4	IMS1820	25, 30, 35, 45	120	30	15		5V + 10-10%	0 °C to + 70 ° C	P DIP/SOJ 24 LCC 28
– 32KX8 OE	MK4832	70, 120	70	3	1	500	5V + 10-10%	0 °C to + 70 ° C	P DIP 28
– 32KX8 OE	MK4832L	70, 120	70	3	0.05	20	5V + 10-10%	0 °C to + 70 ° C	P DIP 28
– 128KX8 (1)	MK48127	55, 70, 85	80	3	0.2	150	5V + 10-10%	0 °C to + 70 ° C	P DIP 32 /SOJ 32
– 128KX8 (1) CHIP ENABLE 2	MK48128	55, 70, 85	80	3	0.2	150	5V + 10-10%	0 °C to + 70 ° C	P DIP 32 /SOJ 32

(1) Product preview.

MILITARY PRODUCTS

ORGANISATION DESCRIPTION	PART NUMBER	Speed ns	Active current (mA @ ns)	ICC max Stdby 1	Icc max Stdby 2	ICC_{DR} @ 3V	V_{CC}	Temp Range	Packages
– 4KX1	IMS1203M	25, 35, 45	80 mA	15 mA	10 mA		5 ± 10 %	– 55 to 125	DIP, F-PACK
– 1KX4	IMS1223M	25, 35, 45	110 mA	15 mA	10 mA		5 ± 10 %	– 55 to 125	DIP, F-PACK
– 16KX1	IMS1400M	45, 55, 70	120 mA	30 mA	(3)		5 ± 10 %	– 55 to 125	DIP, LCC
– 16KX1	IMS1403M	35, 45, 55	75 mA	15 mA	10 mA		5 ± 10 %	– 55 to 125	DIP, LCC
– 16KX1	IMS1403LM	35, 45, 55	75 mA	15 mA	10 mA	400 µA	5 ± 10 %	– 55 to 125	DIP, LCC
– 16KX1	MKB41H67	25, 35, 45	115 mA	10 mA	0,05 mA		5 ± 10 %	– 55 to 125	DIP 20
– 2KX8	MKB6116	150, 200, 250	70 mA	10 mA	0,1 mA		5 ± 10 %	– 55 to 125	DIP 24
– 512X9 (FIFO)	MKB4501	100, 120, 140, 175, 235	90 mA	8 mA	0,9 mA		5 ± 10 %	– 55 to 125	DIP 24
– 4KX4	IMS1420M	55, 70	120 mA	30 mA	(3)		5 ± 10 %	– 55 to 125	DIP, LCC
– 4KX4	IMS1423M	35, 45, 55	130@35, 110@55	20 mA	15 mA		5 ± 10 %	– 55 to 125	DIP, LCC, F-PACK
– 64KX1	IMS1600M	45, 55, 70	70 mA	25 mA	19 mA		5 ± 10 %	– 55 to 125	DIP, LCC
– 64KX1	IMS1601M	45, 55, 70	70 mA	20 mA	15 mA	1200 µA	5 ± 10 %	– 55 to 125	DIP, LCC
– 16KX4	IMS1620M	45, 55, 70	100 mA	30 mA	20 mA		5 ± 10 %	– 55 to 125	DIP, LCC
– 16KX4	IMS1620LM	45, 55, 70	100 mA	20 mA	8 mA	1200 µA	5 ± 10 %	– 55 to 125	DIP, LCC
– 16KX4	IMS1624M (1)	45, 55, 70	100 mA	30 mA	20 mA		5 ± 10 %	– 55 to 125	DIP, LCC
– 16KX4	IMS1624LM (1)	45, 55, 70	100 mA	20 mA	8 mA	1200 µA	5 ± 10 %	– 55 to 125	DIP, LCC
– 8KX8	IMS1630M	45, 55, 70	85 mA	30 mA	20 mA		5 ± 10 %	– 55 to 125	DIP, LCC
– 8KX8	IMS1630LM	45, 55, 70	85 mA	30 mA	20 mA	1200 µA	5 ± 10 %	– 55 to 125	DIP, LCC
– 64KX1	IMS1605M	20, 25, 35					5 ± 10 %	– 55 to 125	DIP, LCC
– 16KX4	IMS1625M	20, 25, 35					5 ± 10 %	– 55 to 125	DIP, LCC
– 16KX4	IMS1629M (1)	20, 25, 35					5 ± 10 %	– 55 to 125	DIP, LCC
– 16KX4	IMS1626M (1, 2)	20, 25, 35					5 ± 10 %	– 55 to 125	DIP, LCC
– 16KX4	IMS1627M (1, 2)	20, 25, 35					5 ± 10 %	– 55 to 125	DIP, LCC
– 8KX8	IMS1635M (1)	20, 25, 35					5 ± 10 %	– 55 to 125	DIP, LCC
– 8KX9	IMS1695M (1)	20, 25, 35					5 ± 10 %	– 55 to 125	DIP, LCC
– 256KX1	IMS1800M	30, 35, 45					5 ± 10 %	– 55 to 125	DIP, LCC
– 64KX4	IMS1820M	30, 35, 45					5 ± 10 %	– 55 to 125	DIP, LCC

(1) Output Enable

(2) Separate I/O

Stdby 1 : Stable Input, TTL Levels

Stdby 2 : Cycling Input, CMOS Levels

AMD	SGS-THOMSON Group
AM2147	IMS1203
AM2148/9	IMS1223
AM2167	IMS1403
AM2168	IMS1423 or MK41H68
AM9126	MK6116
AM99C68	IMS1423 or MK41H68
AM99C88	MK48H64
AM99C89	MK48H89
AM67C4501	MK4501/H01
AM67C4502	MK45H02
AM67C4503	MK4503/H03

DALLAS Semiconductor	SGS-THOMSON Group
DS2009	MK4501/H01
DS2010	MK45H02
DS2011	MK4503/H03
DS2012	MK45H04
DS1210	MK48Z02
DS1225	MK48Z08
DS1243	MK48T08
DS1287	MK48T87
DS1235	MK48Z30
DS1230	MK48Z30A

CYPRESS	SGS-THOMSON Group
CY2147	IMS1203
CY2148/9	IMS1223
CY7C147	IMS1203
CY7C148	IMS1223
CY7C164	IMS1620
CY7C166	IMS1624
CY7C167	IMS1403 or MK41H67
CY7C168	MK41H68
CY7C185	IMS1630L
CY7C187	IMS1600
CY7194	IMS1820
CY7C197	IMS1800
CYC412	MK4501/H01
CY7C424	MK45H02
CYC429	MK4503/H03

FUJITSU	SGS-THOMSON Group
MB81C67	IMS1403 orMK41H67
MB81C68	IMS1423 or MK41H68
MB81C71	IMS1600
MB81C74	IMS1620
MB81C75	IMS1624
MB81C78	MK48H64

HARRIS	SGS-THOMSON Group
HM65747	IMS1203
HM65748	IMS1223
HM65767	IMS1403
HM65261	IMS1403
HM65768	IMS1423 or MK41H68
HM65787	IMS1600
HM65764	IMS1630L
HM6116/L	MK6116/L
HM20256	MK4832

HITACHI	SGS-THOMSON Group
HM6116	MK6116
HM6147	IMS1203
HM6148	IMS1223
HM6167	IMS1403
HM6168	IMS1423 or MK41H79
HM6264	MK48H64
HM6267	IMS1403

MICRON Technology	SGS-THOMSON Group
MT5C1601	IMS1403 or MK41H67
MT5C1604	IMS1423 or MK41H68
MT5C6401	IMS1600
MT5C6404	IMS1620
MT5C6405	IMS1624

HYUNDAI	SGS-THOMSON Group
HY6116	MK6116
HY61C68	MK41H68
HY61C67	MK41H67
HY62256	MK4832
HY62C87	IMS1600
HY62C88	IMS1620
HY6264	MK48H64

MITSUBISHI	SGS-THOMSON Group
M5M21C67P	IMS1403
M5M21C68P	IMS1423 or MK41H68
M5M5165P	IMS1630 or MK48H64
M5M5187P	IMS1600
M5M5188P	IMS1620
M5M5178P	IMS1630
M5M5256	MK4832

IDT	SGS-THOMSON Group
IDT6167A	IMS1403 or MK41H67
IDT6168	IMS1423 or MK41H68
IDT7164	IMS1630
IDT7187	IMS1600
IDT7188	IMS1620
IDT7198	IMS1624
IDT7201	MK4501/H01
IDT7202	MK4502/H02
IDT7103	MK4503/H03
IDT7204	MK45H04
IDT7105	MK45H08
IDT6178S	MK41H80 or MK41S80
IDT7174	MK48H74

MOTOROLA	SGS-THOMSON Group
MCM1423	IMSZ1420 or MH41H66
MCM6064	MK48H64
MCM6164L	IMS1630 L
MCM6168	IMS1420L or MH41H68
MCM6264	MK48H98
MCM6268	MK41H68
MCM6268	IMS1423 or MK41H68
MCM6269	IMS1421
MCM6287	IMS1601L
MCM6287	IMS1600
MCM6288	IMS1620
MCM6290	IMS1624
MCM4180	MK41H80 or MK41S80

NEC	SGS-THOMSON Group
µPD2147	IMS1203
µPD4311	IMS1403 orMK41H67
µPD21467	IMS1403 or MK41H67
µPD4314	IMS1423 or MK41H68
µPD4361	IMS1600
µPD4362	MK48H64IMS1630
µPD4364	MK48H64
µPD43256	MK4832

SONY	SGS-THOMSON Group
CXK5816	MK6116
CXK5416	MK41H68
CXK5864	MK48H64
CXK5854	MK48H64

OKI	SGS-THOMSON Group
MSM5165	MK48H64
MSM5188	MK4832

TOSHIBA	SGS-THOMSON Group
TC55416	IMS1620
TC55417	IMS1624
TC5561	IMS1600
TMM2068	IMS1423
TMM315	IMS1203
TMM5562	IMS1620

SARRATOGA	SGS-THOMSON Group
SSM2148	IMS1223
SSM2149	IMS1223
SSM6167	IMS1403 orMK41H67
SSM6168	IMS1423 orMK41H68
SSM7164	IMS1630L
SSM7166	IMS1624
SSM7188	IMS1620
SSL4180	MK41H80
SSM6170	MK41H78
SSL7201	MK4501/H01
SSL7203	MK4503/H03

UMC	SGS-THOMSON Group
UM4501	MK4501
UM4502	MK4502
UM6116	MK6116

VITELIC	SGS-THOMSON Group
V61C67	IMS1403 or MK41H67
V61C68	IMS1423 or MK41H68
V62C16	MK6116
V62C64	MK48H64
V62C256	MK4832

VLSI	SGS-THOMSON Group
VT20C50	IMS1423 or MK41H68
VT20C68	IMS1423 or MK41H68
VT20C69	IMS1423 or MK41H68
VT62K54	IMS1620

STANDARD MILITARY DRAWING REFERENCE

SMD Number	INMOS Part Number
4K X 1 (IMS 1203)	
5962-8751301VC	SMD1203S-25M
5962-8751301XC	SMD1203A-25M
5962-8751302VC	SMD1203S-35M
5962-8751302XC	SMD1203A-35M
5962-8751303VC	SMD1203S-45M
5962-8751303XC	SMD1203A-45M
1K X 4 (IMS1223)	
5962-8751304VC	SMD1223S-25M
5962-8751304XC	SMD1223A-25M
5962-8751305VC	SMD1223S-35M
5962-8751305XC	SMD1223A-35M
5962-8751306VC	SMD1223S-45M
5962-8751306XC	SMD1223A-45M
16K X 1 (IMS1403)	
8413202RC	SMD1403S-45M
8413202YA	SMD1403N-45M
8413205RC	SMD1403S-35M
8413205YA	SMD1403N-35M
8413208RC	SMD1403S-55M
8413208YA	SMD1403N-55M
4K X 4 (IMS1423)	
5962-8670512RC	SMD1423S-35M
5962-8670512XA	SMD1423N-35M
5962-8670512ZC	SMD1423Y-35M
5962-8670513RC	SMD1423S-45M
5962-8670513XA	SMD1423N-45M
5962-8670513ZC	SMD1423Y-45M
5962-8670514RC	SMD1423S-55M
5962-8670514XA	SMD1423N-55M
5962-8670514ZC	SMD1423Y-55M
5962-8670515RC	SMD1423S-70M
5962-8670515XA	SMD1423N-70M
5962-8670515ZC	SMD1423Y-70M

SMD Number	INMOS Part Number
64K X 1 (IMS1600:IMS1601L)	
5962-8601503XC	SMD1600S-45M
5962-8601503ZA	SMD1600N-45M
5962-8601504XC	SMD1601S-45LM
5962-8601504ZA	SMD1601N-45LM
5962-8601505XC	SMD1600S-55M
5962-8601505ZA	SMD1600N-55M
5962-8601506XC	SMD1601S-55LM
5962-8601506ZA	SMD1601N-55LM
5962-8601507XC	SMD1600S-70M
5962-8601507ZA	SMD1600N-70M
5962-8601508XC	SMD1601S-70LM
5962-8601508ZA	SMD1601N-70LM
16K X 4 (IMS1624)	
5962-8685911LC	SMD1624S-70LM
5962-8685911XA	SMD1624N-70LM
5962-8685912LC	SMD1624S-70M
5962-8685912XA	SMD1624N-70M
5962-8685913LC	SMD1624S-55LM
5962-8685913XA	SMD1624N-55LM
5962-8685914LC	SMD1624S-55M
5962-8685914XA	SMD1624N-55M
5962-8685915LC	SMD1624S-45LM
5962-8685915XA	SMD1624N-45LM
5962-8685916LC	SMD1624S-45M
5962-8685916XA	SMD1624N-45M
8K X 8 (IMS1630)	
5962-8552504XC	SMD1630S-70M
5962-8552504YA	SMD1630N-70M
5962-8552505XC	SMD1630S-55M
5962-8552505YA	SMD1630N-55M
5962-8552510XC	SMD1630S-55LM
5962-8552510YA	SMD1630N-55LM
5962-8552511XC	SMD1630S-70LM
5962-8552511YA	SMD1630N-70LM

COMMERCIAL SRAMs

IMS1203
CMOS
High Performance
4K x 1 Static RAM

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 4K x 1 Bit Organization
- 25, 35, and 45 nsec Access Times
- 25, 35, and 45 nsec Chip Enable Access Times
- Fully TTL Compatible
- Separate Data Input and Output
- Three-state Output
- 18 Pin, 300-mil DIP
- Single +5V ± 10% Operation
- Power Down Function

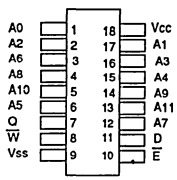
DESCRIPTION

The INMOS IMS1203 is a high performance 4Kx1 CMOS static RAM. The IMS1203 allows speed enhancements to existing 4Kx1 applications with the additional benefit of reduced power consumption.

The IMS1203 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1203 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

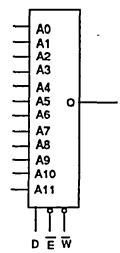
The IMS1203M is a MIL-STD-883 version intended for military applications.

PIN CONFIGURATION

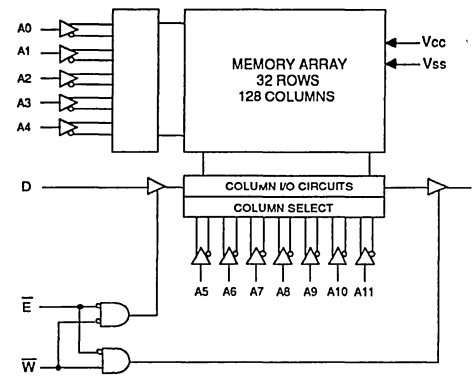


DIP

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{11}	ADDRESS INPUTS	Vcc	POWER
$\overline{W}$	WRITE ENABLE	Vss	GROUND
D	DATA INPUT		
$\overline{E}$	CHIP ENABLE		
Q	DATA OUTPUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −2.0 to 7.0V
Voltage on Q . . . . . −1.0 to (V_{CC} + 0.5V)
Temperature Under Bias. . . . . −55°C to 125°C
Storage Temperature . . . . . −65°C to 150°C
Power Dissipation 1W
DC Output Current 25mA
(One Second Duration)

*Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect reliability

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc +.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0		70	°C	400 linear ft/min air flow

* V_{IL} Min = -3.0V for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC_1}	Average V_{CC} Power Supply Current		80	mA	$t_{AVAV} = t_{AVAV}$ (min)
I_{CC_2}	V_{CC} Power Supply Current (Standby, Stable TTL Input Levels)		15	mA	$\overline{E} \geq V_{IH}$ All other inputs $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$
I_{CC_3}	V_{CC} Power Supply Current (Standby, Stable CMOS Input Levels)		6	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ All other inputs at $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{CC_4}	V_{CC} Power Supply Current (Standby, Cycling CMOS Input Levels)		13	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ Inputs cycling at $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current (Any Input)		±1	μA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		±5	μA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage	2.4		V	$I_{OUT} = -4mA$
V_{OL}	Output Logic "0" Voltage		0.4	V	$I_{OUT} = 12mA$

Note a I_{CC} is dependent on output loading and cycle rate. the specified values are obtained with the output unloaded

AC TEST CONDITIONS

Input Pulse Levels	V_{SS} to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1 5V
Output Load	See Figure 1

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)[b]

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	4	pF	ΔV = 0 to 3V

Note b This parameter is sampled and not 100% tested

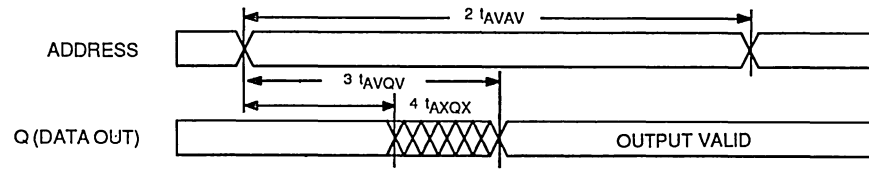
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[g]

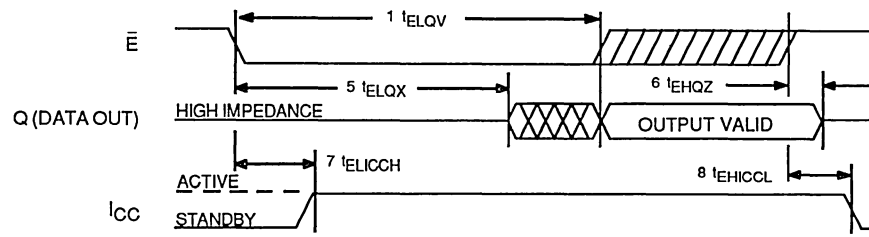
NO.	SYMBOL		PARAMETER	1203-25		1203-35		1203-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	25		35		45		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		25		35		45	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	3		3		3		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	j
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive	0	20	0	30	0	30	ns	f, j
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
8	t_{EHICCL}	t_{PD}	Chip Enable to Power Down		20		20		20	ns	j
		t_T	Input Rise and Fall Times		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c, d]



READ CYCLE 2[c]



DEVICE OPERATION

The IMS1203 has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), twelve address inputs (A_0-A_{11}), a data in (D_{IN}) and a data out (D_{OUT}). The $\overline{E}$ input controls device selection as well as active and standby modes With $\overline{E}$ low, the device is selected and the twelve address inputs are decoded to select one memory cell out of 4096. Read and Write operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than one-third of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low The output remains active throughout READ CYCLE 1 and is valid at the specified address access time The address inputs may change at access time and as long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

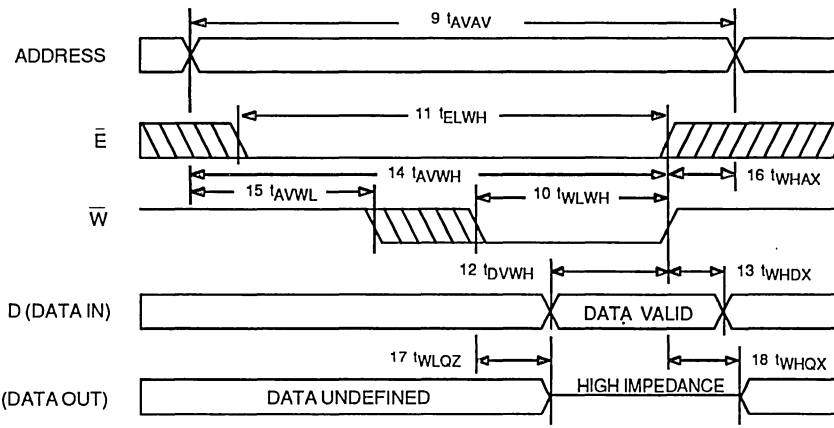
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	1203-25		1203-35		1203-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
9	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns	
10	t_{WLWH}	t_{WP}	Write Pulse Width	15		20		25		ns	
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write	20		30		40		ns	
12	t_{DVWH}	t_{DW}	Data Set-up to End of Write	15		20		25		ns	
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
14	t_{AVWH}	t_{AW}	Address Set-up to End of Write	20		30		40		ns	
15	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	15	0	20	0	20	ns	f, j
18	t_{WHQX}	t_{OW}	Output Active After End of Write	0		0		0		ns	i

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



The READ CYCLE 2 waveform shows a read access that is initiated by $\overline{E}$ going low As long as address is stable when $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when $\overline{E}$ goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1203 is initiated by the latter of $\overline{E}$ or $\overline{W}$ to fall. In the case of $\overline{W}$ falling last, the output buffer will be turned on t_{ELQX} after the falling edge of $\overline{E}$ (just as in a read cycle) The output buffer is then turned off within t_{WLQZ} of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with D and Q connected together in a common I/O configuration Contention can be avoided in a carefully designed system During a write cycle, data on the input is written into the selected cells and the output is floating.

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high Data set-up and hold times are referenced to the rising edge of $\overline{W}$ When $\overline{W}$ goes high at the end of the cycle with $\overline{E}$ active, the output of

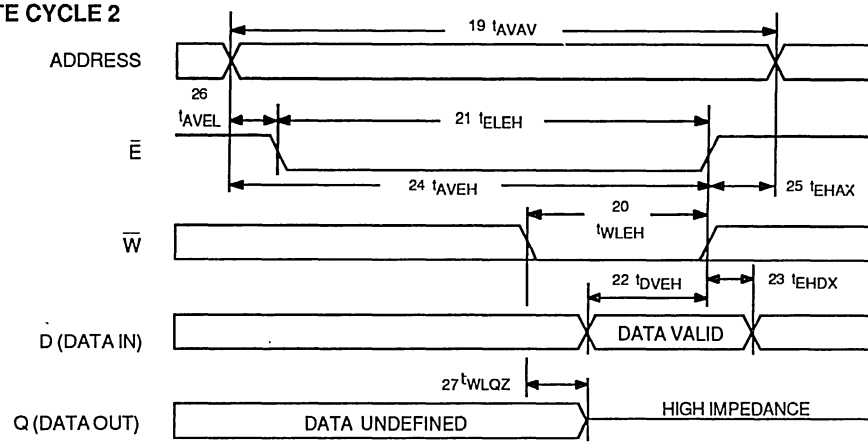
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	1203-25		1203-35		1203-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	15		20		25		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		30		40		ns	
22	t_{DVEH}	t_{DW}	Data Set-up to End of Write	15		20		25		ns	
23	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
24	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		30		40		ns	
25	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
26	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	15	0	20	0	20	ns	f, j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, the outputs remain in the high impedance state.

APPLICATION

It is imperative when designing with any very high speed memory, such as the IMS1203, that the fundamental rules in regard to memory board layout be followed to ensure proper system operation.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1203 The impedance in the decoupling path from the power pin (18) through the decoupling capacitor to the ground pin (9) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1203 have very high frequency

components, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad, and be placed between each row of devices in the array (see drawing). A larger tantalum capacitor, with a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

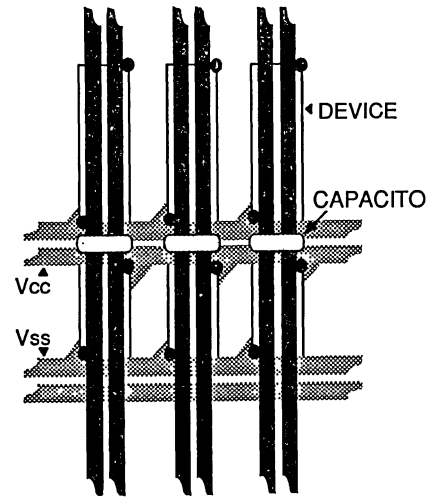
The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

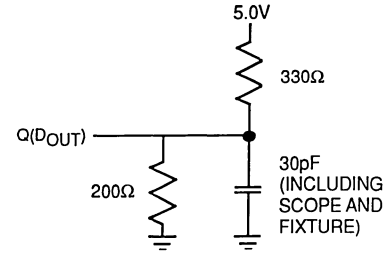
Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

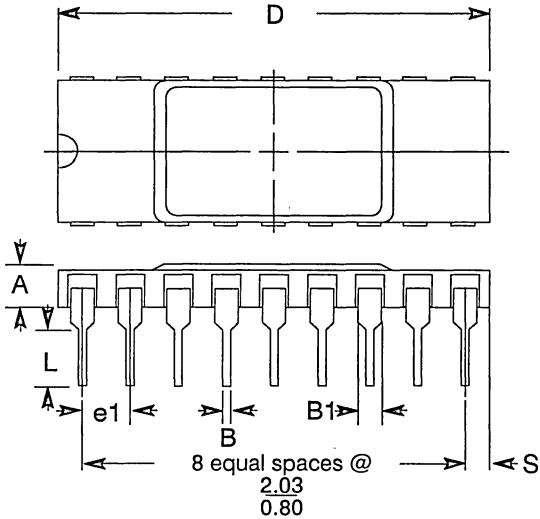
FIGURE 1. OUTPUT LOAD



DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1203	25ns	PLASTIC DIP	IMS1203P-25
	25ns	CERAMIC DIP	IMS1203S-25
	35ns	PLASTIC DIP	IMS1203P-35
	35ns	CERAMIC DIP	IMS1203S-35
	45ns	PLASTIC DIP	IMS1203P-45
	45ns	CERAMIC DIP	IMS1203S-45

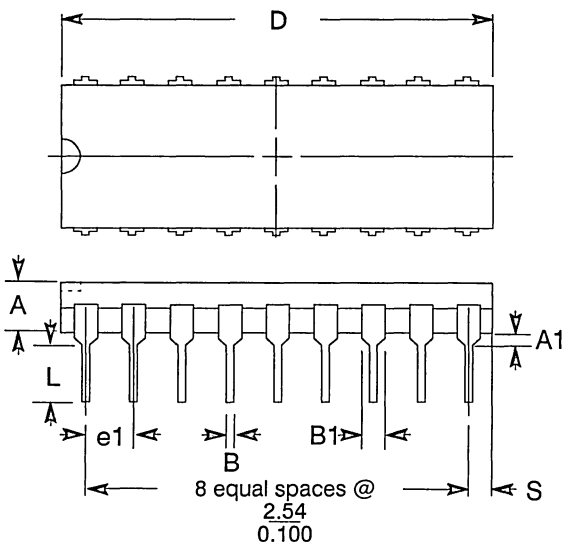
PACKAGING INFORMATION

18 Pin Ceramic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.085	.010	2.18	.230
B	.018	.003	.457	.152
B1	.054	Typ	.137	Typ
D	.900	.011	22.86	.279
E	.310	.010	7.874	.254
E1	.295	.015	7.493	.381
e1	.100	.010	2.54	.254
L	.145	.020	3.683	.508
S	.005		.127	

18 Pin Plastic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.130	.007	3.302	.178
A1	.020	min	.508	min
B	.018	.003	.457	.152
B1	.060	Typ	1.524	Typ
D	.900	.011	22.86	.279
E	.300	.003	7.874	.254
E1	.295	.015	7.620	.076
e1	.100	.010	2.54	.254
eA	.330	.020	8.382	.508
L	.135	max	3.429	max
S	.050		.127	

IMS1223
CMOS
High Performance
1K x 4 Static RAM

inmos®

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 1K x 4 Bit Organization
- 25, 35, and 45 nsec Access Times
- 25, 35, and 45nsec Chip Enable Access Times
- Fully TTL Compatible
- Common Data Input and Output
- Three-state Output
- 18 Pin, 300-mil DIP
- Single +5V ± 10% Operation
- Power Down Function

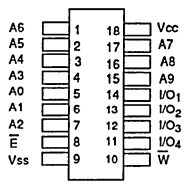
DESCRIPTION

The INMOS IMS1223 is a high performance 1Kx4 CMOS static RAM. The IMS1223 allows speed enhancements to existing 1Kx4 applications with the additional benefit of reduced power consumption.

The IMS1223 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1223 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

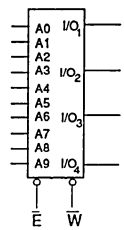
The IMS1223M is a MIL-STD-883 version intended for military applications.

PIN CONFIGURATION

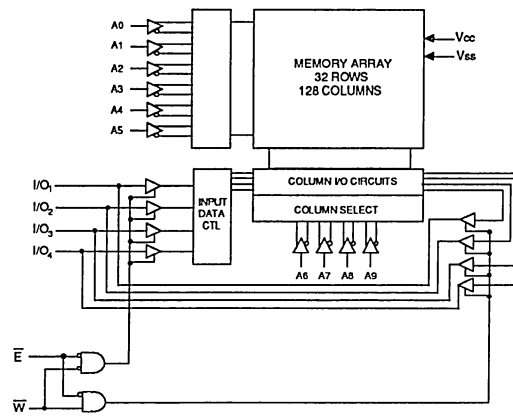


DIP

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_9	ADDRESS INPUTS	Vcc	POWER
$\overline{W}$	WRITE ENABLE	Vss	GROUND
$\overline{E}$	CHIP ENABLE		
I/O	DATA IN/OUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −2.0 to 7.0V
Voltage on Q . . . . . −1.0 to (V_{CC} + 0.5V)
Temperature Under Bias. . . . . −55°C to 125°C
Storage Temperature . . . . . −65°C to 150°C
Power Dissipation 1W
DC Output Current 25mA
(One Second Duration)

*Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect reliability

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		V_{CC}+.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0		70	°C	400 linear ft/min air flow

* V_{IL} Min = -3.0V for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ± 10%)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC_1}	Average V_{CC} Power Supply Current		100	mA	$t_{AVAV} = t_{AVAV}$ (min)
I_{CC_2}	V_{CC} Power Supply Current (Standby, Stable TTL Input Levels)		15	mA	$\overline{E} \geq V_{IH}$ All other inputs V_{IN} ≤ V_{IL} or ≥ V_{IH}
I_{CC_3}	V_{CC} Power Supply Current (Standby, Stable CMOS Input Levels)		6	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ All other inputs at V_{IN} ≤ 0.2V or ≥ (V_{CC} −0.2V)
I_{CC_4}	V_{CC} Power Supply Current (Standby, Cycling CMOS Input Levels)		8	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ Inputs cycling at V_{IN} ≤ 0.2V or ≥ (V_{CC} −0.2V)
I_{ILK}	Input Leakage Current (Any Input)		±1	μA	V_{CC} = max V_{IN} = V_{SS} to V_{CC}
I_{OLK}	Off State Output Leakage Current		±5	μA	V_{CC} = max V_{IN} = V_{SS} to V_{CC}
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OUT} = −4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OUT} = 8mA

Note a I_{CC} is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded

AC TEST CONDITIONS

Input Pulse Levels	V_{SS} to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figure 1

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)[b]

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	4	pF	ΔV = 0 to 3V

Note b This parameter is sampled and not 100% tested

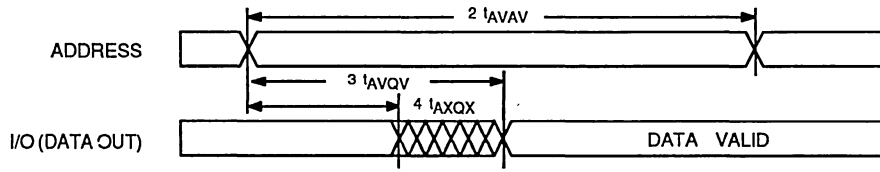
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[g]

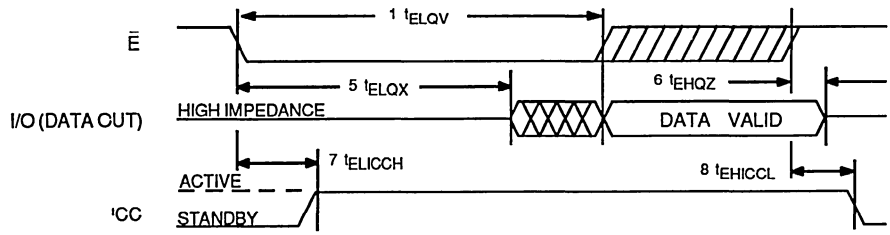
NO.	SYMBOL		PARAMETER	1223-25		1223-35		1223-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELOV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	25		35		45		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		25		35		45	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	0		0		0		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	j
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive		15		20		20	ns	f, j
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
8	t_{EHICCL}	t_{PD}	Chip Enable to Power Down		20		20		20	ns	j
		t_T	Input Rise and Fall Times		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c, d]



READ CYCLE 2[c]



DEVICE OPERATION

The IMS1223 has two control inputs: Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), ten address inputs (A_0-A_9), and four data I/O lines. The $\overline{E}$ input controls device selection as well as active and standby modes. With $\overline{E}$ low, the device is selected and the ten address inputs are decoded to select one 4 bit word out of 1024. Read and Write operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the outputs are disabled, and the power consumption is reduced to less than one-third of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and as long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

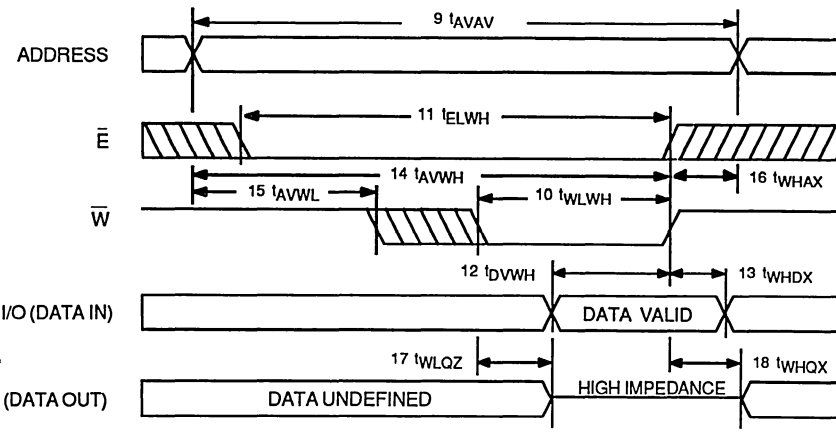
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	1223-25		1223-35		1223-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
9	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns	
10	t_{WLWH}	t_{WP}	Write Pulse Width	20		25		35		ns	
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write	20		25		30		ns	
12	t_{DVWH}	t_{DW}	Data Set-up to End of Write	10		15		15		ns	
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
14	t_{AVWH}	t_{AW}	Address Set-up to End of Write	20		25		35		ns	
15	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable		15		20		20	ns	f, j
18	t_{WHQX}	t_{OW}	Output Active After End of Write	5		5		5		ns	i

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



The READ CYCLE 2 waveform shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable when $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when $\overline{E}$ goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1223 is initiated by the latter of $\overline{E}$ or $\overline{W}$ to transition from a high to a low. In the case of $\overline{W}$ falling last, the output buffer will be turned on t_{ELQX} after the falling edge of $\overline{E}$ (just as in a read cycle). The output buffer is then turned off within t_{WLQZ} of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with common I/O configurations. Contention can be avoided in a carefully designed system. During a write cycle, data on the input is written into the selected cells and the output is floating.

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. When $\overline{W}$ goes high at the end of the cycle with $\overline{E}$ active, the output of the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes

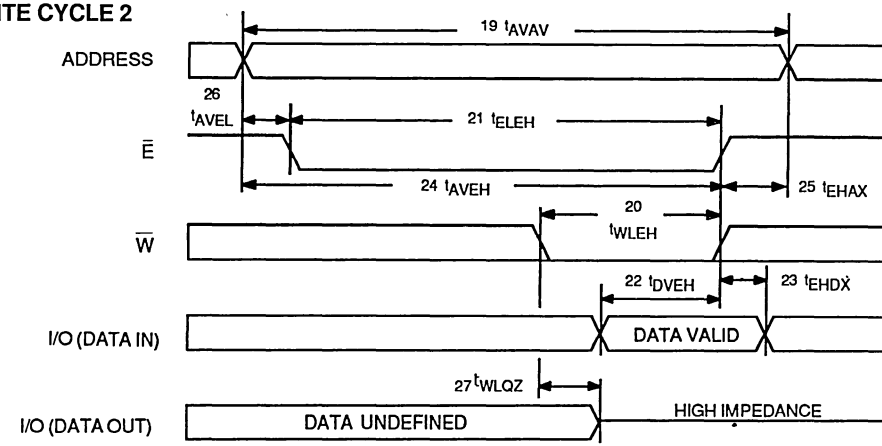
RECOMMENDED AC OPERATING CONDITIONS ($-0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	1223-25		1223-35		1223-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	15		25		35		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		30		ns	
22	t_{DVEH}	t_{DW}	Data Set-up to End of Write	10		15		15		ns	
23	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
24	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		25		35		ns	
25	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
26	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable		15		20		20	ns	f, j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



WRITE CYCLE 2 waveform shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, the outputs remain in the high impedance state.

APPLICATION

It is imperative when designing with any very high speed memory, such as the IMS1223, that the fundamental rules in regard to memory board layout be followed to ensure proper system operation.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1223. The impedance in the decoupling path from the power pin (18) through the decoupling capacitor to the ground pin (9) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1223 have very high frequency components, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy

for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad, and be placed between each row of devices in the array (see drawing). A larger tantalum capacitor, with a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

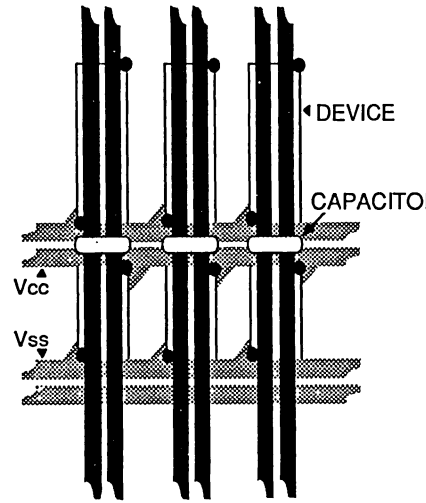
The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

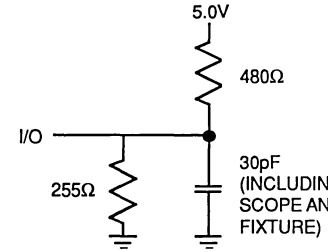
Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

FIGURE 1. OUTPUT LOAD

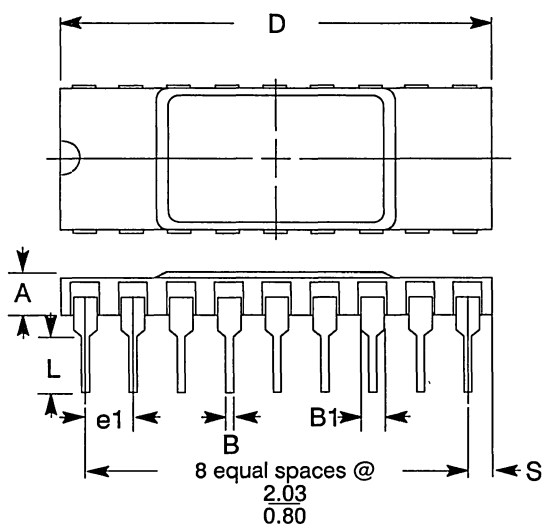


ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1223	25ns	PLASTIC DIP	IMS1223P-25
	25ns	CERAMIC DIP	IMS1223S-25
	35ns	PLASTIC DIP	IMS1223P-35
	35ns	CERAMIC DIP	IMS1223S-35
	45ns	PLASTIC DIP	IMS1223P-45
	45ns	CERAMIC DIP	IMS1223S-45

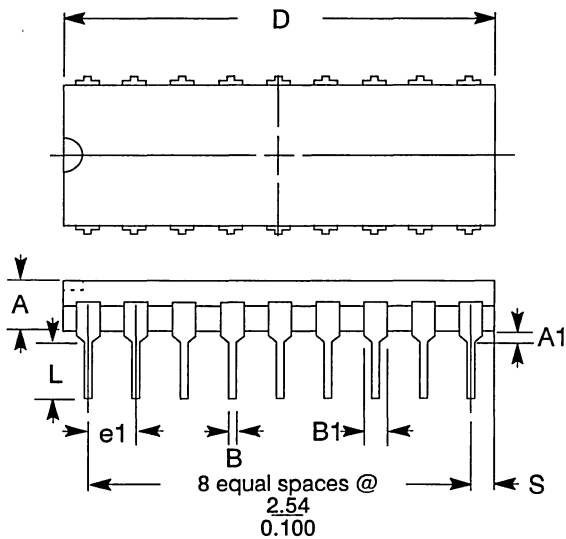
PACKAGING INFORMATION

18 Pin Ceramic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.085	.010	2.18	.230
B	.018	.003	.457	.152
B1	.054	Typ	.137	Typ
D	.900	.011	22.86	.279
E	.310	.010	7.874	.254
E1	.295	.015	7.493	.381
e1	.100	.010	2.54	.254
L	.145	.020	3.683	.508
S	.005		.127	

18 Pin Plastic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.130	.007	3.302	.178
A1	.020	min	.508	min
B	.018	.003	.457	.152
B1	.060	Typ	1.524	Typ
D	.900	.011	22.86	.279
E	.300	.003	7.874	.254
E1	.295	.015	7.620	.076
e1	.100	.010	2.54	.254
eA	.330	.020	8.382	.508
L	.135	max	3.429	max
S	.050		.127	

IMS1403

CMOS High Performance 16K x 1 Static RAM

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 16K x 1 Bit Organization
- 25, 35, 45 and 55 nsec Access Times
- Fully TTL Compatible
- Separate Data Input & Output
- Three-state Output
- Power Down Function
- Single +5V ± 10% Operation
- 20-Pin, 300-mil DIP (JEDEC Std.)
- 20-Pin Ceramic LCC (JEDEC Std.)

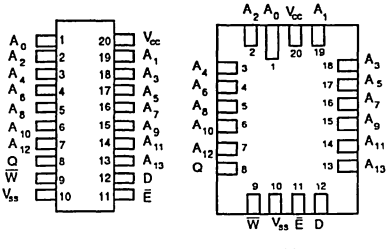
DESCRIPTION

The INMOS IMS1403 is a high performance 16K x 1 CMOS Static RAM. The IMS1403 provides maximum density and speed enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1403 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1403 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

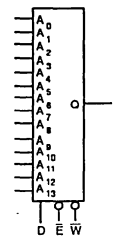
The IMS1403M and IMS1403LM are MIL-STD-883 versions intended for military applications.

PIN CONFIGURATION

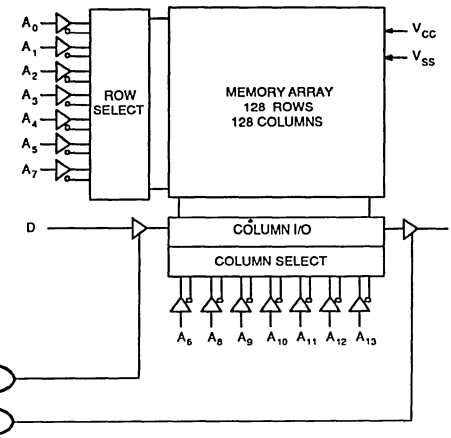


DIP CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{13}	ADDRESS INPUTS	Q	DATA OUTPUT
$\overline{W}$	WRITE ENABLE	V_{CC}	POWER
$\overline{E}$	CHIP ENABLE	V_{SS}	GROUND
D	DATA INPUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on Q .....-1.0 to (Vcc+0.5)
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One Second Duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0	25	70	°C	400 linear ft/min air flow

*V_{IL} min = -3 volts for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		75	mA	$t_{AVAV} = t_{AVAV}$ (min)
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		15	mA	$\bar{E} \geq V_{IH}$. All other inputs at $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		5	mA	$\bar{E} \geq$ (Vcc - 0.2). All other inputs at $V_{IN} \leq 0.2$ or $\geq$ (Vcc - 0.2V)
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		10	mA	$\bar{E} \geq$ (Vcc - 0.2). Inputs cycling at $V_{IN} \leq 0.2$ or $\geq$ (Vcc - 0.2V)
I_{ILK}	Input Leakage Current (Any Input)		±1	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		±5	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OL} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OH} = 16mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels .....Vss to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0MHZ)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	4	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

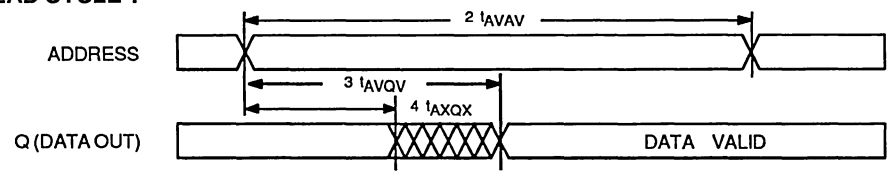
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE [g]

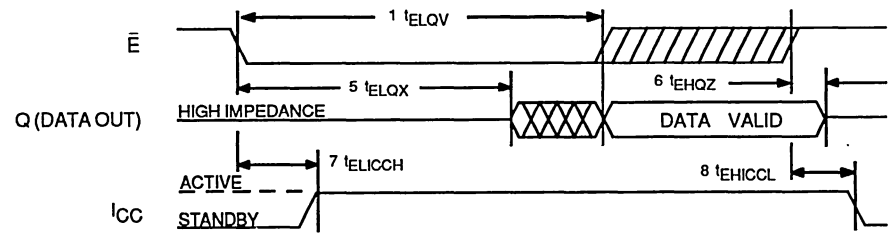
NO.	SYMBOL		PARAMETER	1403-25		1403-35		1403-45		1403-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45		55	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	25		35		40		50		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		25		35		40		50	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		5		5		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		5		ns	j
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive	0	20	0	20	0	20	0	25	ns	f, j
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		0		ns	j
8	t_{EHICCL}	t_{PD}	Chip Enable To Power Down		30		30		30		30	ns	j
		t_T	Input Rise and Fall Times		50		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected, $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ± 200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1 [c, d]



READ CYCLE 2 [c]



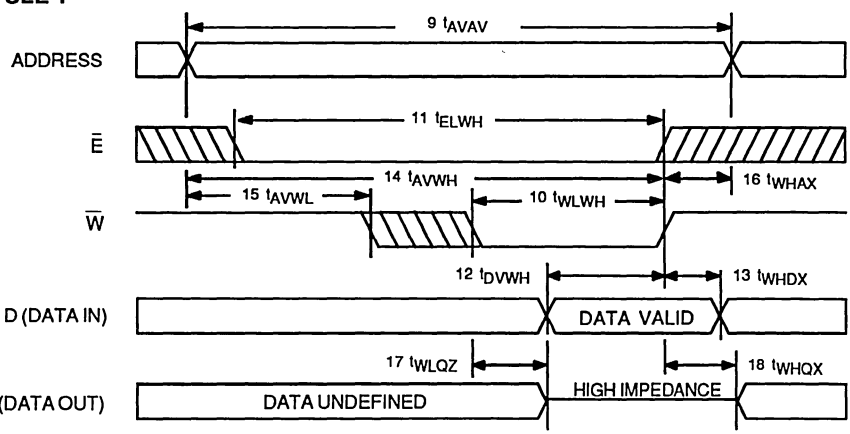
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	1403-25		1403-35		1403-45		1403-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
9	t_{AVAV}	t_{WC}	Write Cycle Time	20		30		40		50		ns	
10	t_{WLWH}	t_{WP}	Write Pulse Width	15		20		20		25		ns	
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write	20		30		35		45		ns	
12	t_{DVWH}	t_{DW}	Data Set-up to End of Write	15		15		15		20		ns	
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	0		0		0		0		ns	
14	t_{AVWH}	t_{AW}	Address Set-up to End of Write	20		30		35		45		ns	
15	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		0		ns	
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	0		0		0		0		ns	
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	20	0	20	0	20	ns	f, j
18	t_{WHQX}	t_{OW}	Output Active After End of Write	0		0		0		0		ns	i

Note f: Measured ± 200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



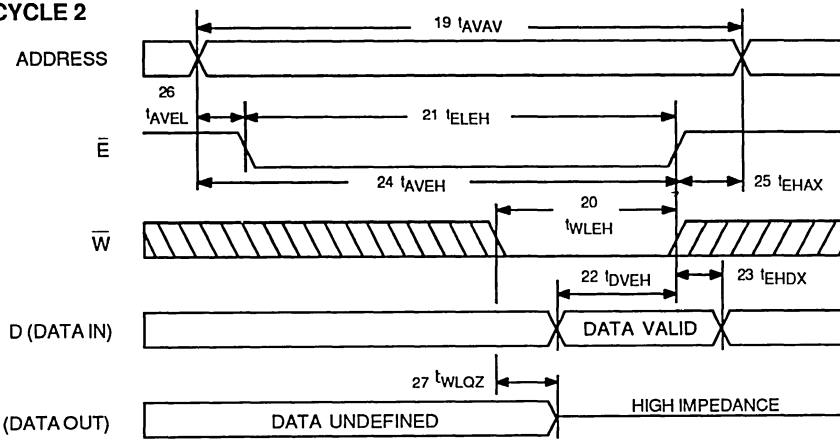
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	1403-25		1403-35		1403-45		1403-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	20		30		40		50		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	15		20		20		25		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		30		35		45		ns	
22	t_{DVEH}	t_{DW}	Data Set-up to End of Write	15		15		15		20		ns	
23	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		0		ns	
24	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		30		35		45		ns	
25	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		0		ns	
26	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		0		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	20	0	20	0	25	ns	f, j

Note f: Measured ± 200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1403 has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), fourteen address inputs (A_0 - A_{13}), a Data in (D) and a Data out (Q). The $\overline{E}$ input controls device selection as well as active and standby modes. With $\overline{E}$ low, the device is selected and the fourteen address inputs are decoded to select one bit out of 16K bits. Read and Write operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is de-selected, the output is disabled, and power consumption is reduced to less than one-fourth of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time as long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable when $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when $\overline{E}$ goes low, the timing is as specified in READ CYCLE 1 Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

A write cycle of the IMS1403 is initiated by the latter of $\overline{E}$ or $\overline{W}$ to transition from a high to a low. In the case of $\overline{W}$ falling last, the output buffer will be turned on t_{ELOX} after the falling edge of $\overline{E}$ (just as in a read cycle). The output buffer is then turned off within t_{WLOZ} of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with D and Q connected together in a common I/O configuration Contention can be avoided in a carefully designed system. During a write cycle, data on the input is written into the selected cells and the output is floating.

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. When $\overline{W}$ goes high at the end of the cycle with $\overline{E}$ active, the output of the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$ With $\overline{E}$ high, the outputs remain in the high impedance state.

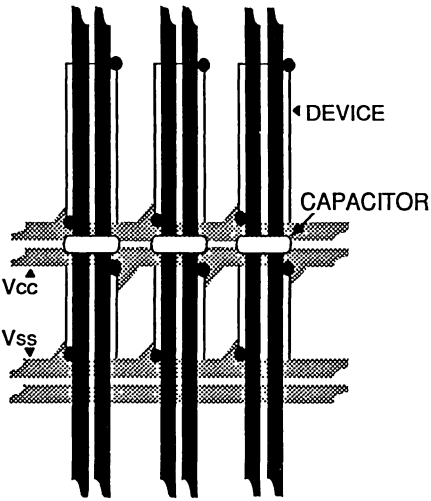
APPLICATION

It is imperative when designing with any very high speed memory, such as the IMS1403, that the fundamental rules in regard to memory board layout be followed to ensure proper system operation.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1403. The impedance in the decoupling path from the power pin through the decoupling capacitor, to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1403 have very high frequency components, the line inductance is the dominating factor.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1μF, and be placed between each row of devices in the array (see drawing). A larger tantalum capacitor, with a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

The ground grid of the memory array should extend to the TTL periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

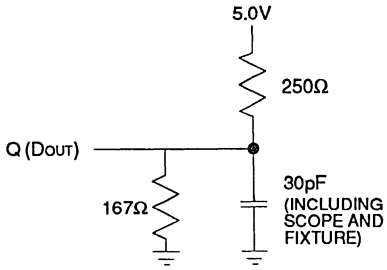
Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically

Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

FIGURE 1. OUTPUT LOAD

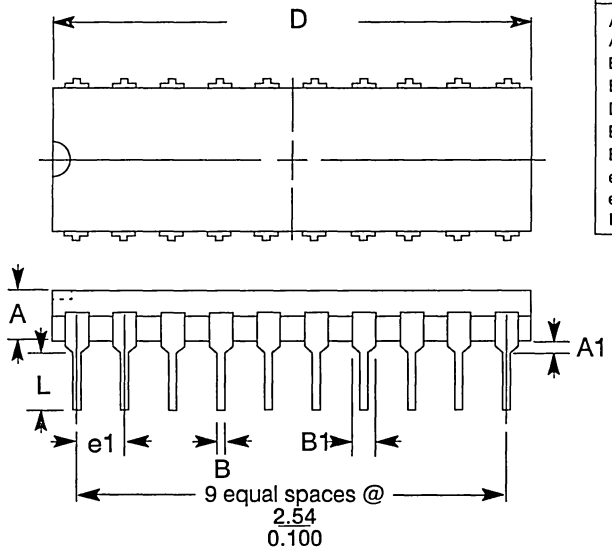


ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1403	25ns	PLASTIC DIP	IMS1403P-25
	25ns	CERAMIC DIP	IMS1403S-25
	25ns	CERAMIC LCC	IMS1403W-25
	35ns	PLASTIC DIP	IMS1403P-35
	35ns	CERAMIC DIP	IMS1403S-35
	35ns	CERAMIC LCC	IMS1403W-35
	45ns	PLASTIC DIP	IMS1403P-45
	45ns	CERAMIC DIP	IMS1403S-45
	45ns	CERAMIC LCC	IMS1403W-45
	55ns	PLASTIC DIP	IMS1403P-55
	55ns	CERAMIC DIP	IMS1403S-55
	55ns	CERAMIC LCC	IMS1403W-55

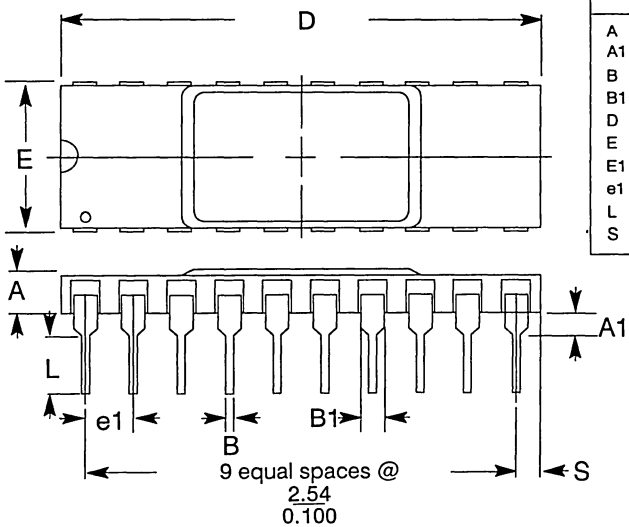
PACKAGING INFORMATION

20 Pin Plastic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.140	.015	3.566	.381
A1	.020	min	.508	min
B	.018	.003	.457	.152
B1	.060	Typ	1.524	Typ
D	1.035	.015	26.289	.381
E	.300	.003	7.620	.076
E1	.250		6.350	
e1	.100	.010	2.54	.254
eA	.330	.020	8.382	.508
L	.120	min	3.048	min

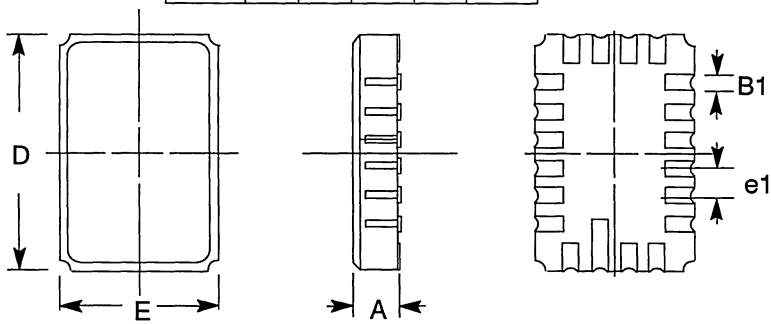
20 Pin Ceramic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.096	.012	2.438	.305
A1	.015		.381	
B	.018	.003	.457	.152
B1	.054	Typ	.137	Typ
D	1.00	.015	25.40	.381
E	.315	.010	8.001	.254
E1	.295	.015	7.493	.381
e1	.100	.010	2.54	.254
L	.125	min	3.175	min
S	.005		.127	

20 Pin Leadless Chip Carrier

Dim	Inches		mm		Notes
	Nom	Tol	Nom	Tol	
A	.071	.007	1.803	.178	
B1	.025	.003	.635	.076	
D	.425	.010	10.795	.254	
E	.290	.010	7.360	.254	
e1	.050	.005	1.270		



IMS1423
High Performance 4K x 4 CMOS Static RAM

inmos®

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 4K x 4 Bit Organization
- 25, 35, 45 and 55 nsec Access Times
- Fully TTL Compatible
- Common Data Input & Output
- Three-state Output
- 20-Pin, 300-mil DIP & SOJ (JEDEC Std.)
- 20-Pin Ceramic LCC (JEDEC Std.)
- Single +5V ± 10% Operation
- Power Down Function for Low Standby Power
- Pin Compatible with IMS1420

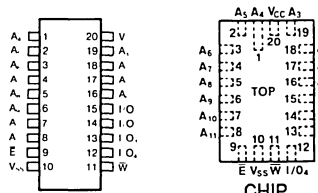
DESCRIPTION

The INMOS IMS1423 is a high performance 4K x 4 CMOS static RAM. The IMS1423 provides maximum density and speed enhancements with the additional CMOS benefits of lower power and superior reliability.

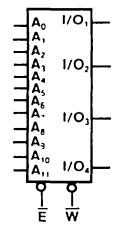
The IMS1423 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1423 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

The IMS1423M is a MIL-STD-883 version intended for military applications that demand superior performance and reliability.

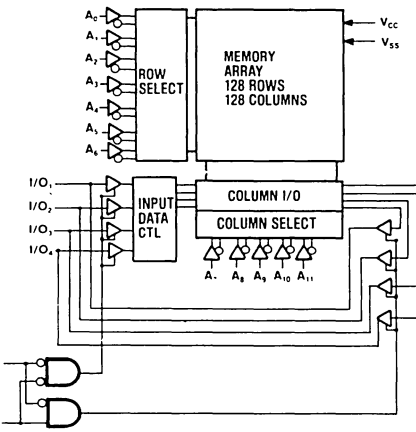
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
$\overline{E}$	CHIP ENABLE		
I/O	DATA IN/OUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −2.0 to 7.0V
Voltage on I/O (Pins 13-16) . . . . −1.0 to (V_{CC} + 0.5V)
Temperature Under Bias . . . . . −55°C to 125°C
Storage Temperature (Ambient) . . . . −65°C to 150°C
Power Dissipation 1W
DC Output Current 25mA
(One Second Duration)

*Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc + .5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0	25	70 .	°C	400 linear ft/min air flow

* V_{IL} Min = -3.0V for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		105 100 100	mA mA mA	t_{AVAV} = 25ns t_{AVAV} = 35ns t_{AVAV} = 45ns & 55ns
I_{CC2}	V_{CC} Power Supply Current (Standby, Stable TTL Input Levels)		15	mA	$\bar{E} \geq V_{IH}$ All other inputs at $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$
I_{CC3}	V_{CC} Power Supply Current (Standby, Stable CMOS Input Levels)		5	mA	$\bar{E} \geq (V_{CC} - 0.2)$ All other inputs at $V_{IN} \leq 0.2$ or $\geq (V_{CC} - 0.2V)$
I_{CC4}	V_{CC} Power Supply Current (Standby, Cycling CMOS Input Levels)		10	mA	$\bar{E} \geq (V_{CC} - 0.2)$ Inputs cycling at $V_{IN} \leq 0.2$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current (Any Input)		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		±5	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 8mA

Note a: I_{CC} is dependent on output loading and cycle rate, the specified values are obtained with the outputs unloaded.

AC TEST CONDITIONS

Input Pulse Levels.....V_{SS} to 3V
Input Rise and Fall Times.....5ns
Input and Output Timing Reference Levels.....1.5V
Output Load.....See Figure 1

CAPACITANCE[b] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	4	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

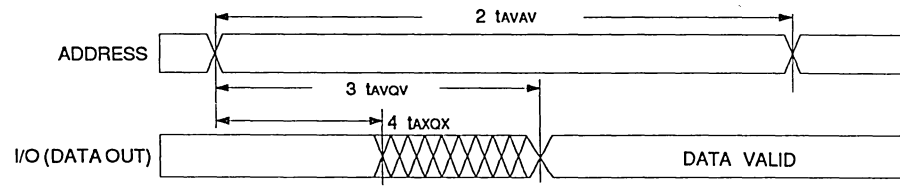
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE [g]

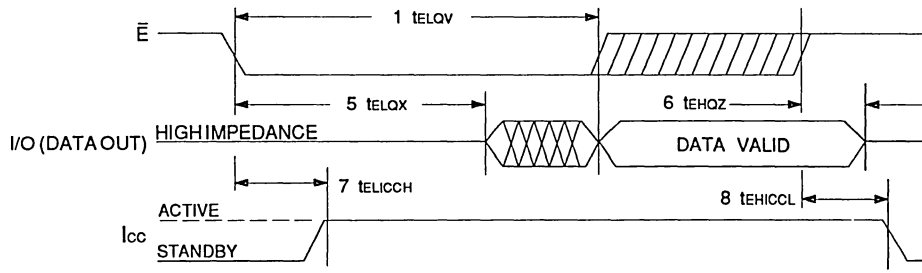
NO.	SYMBOL		PARAMETER	1423-25		1423-35		1423-45		1423-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45		55	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	25		35		40		50		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		25		35		40		50	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	3		3		3		3		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		5		ns	j
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive	0	15	0	15	0	15	0	15	ns	f, j
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		0		ns	j
8	t_{EHICCL}	t_{PD}	Chip Disable To Power Down		30		30		30		30	ns	j
		t_T	Input Rise and Fall Times		50		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected, $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f. Measured ± 200mV from steady state output voltage. Load capacitance is 5pF
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1 [c,d]



READ CYCLE 2 [c]



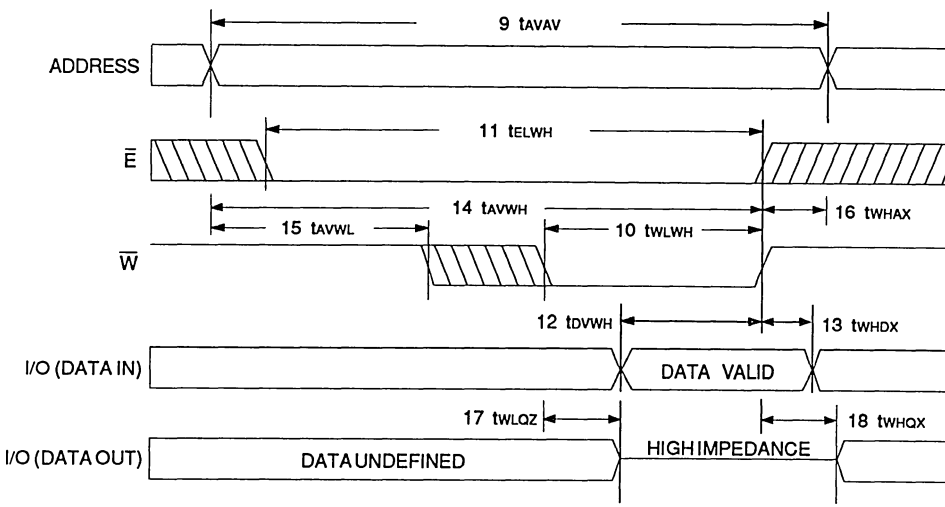
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	1423-25		1423-35		1423-45		1423-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
9	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		40		50		ns	
10	t_{WLWH}	t_{WP}	Write Pulse Width	20		25		35		45		ns	
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write	20		25		35		45		ns	
12	t_{DVWH}	t_{DW}	Data Set-up to End of Write	10		13		15		20		ns	
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	2		2		3		3		ns	
14	t_{AVWH}	t_{AW}	Address Set-up to End of Write	20		25		30		40		ns	
15	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		0		ns	
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	2		3		5		5		ns	
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	15	0	15	0	20	0	25	ns	f,j
18	t_{WHQX}	t_{OW}	Output Active After End of Write	6		6		6		6		ns	i

Note f: Measured ± 200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



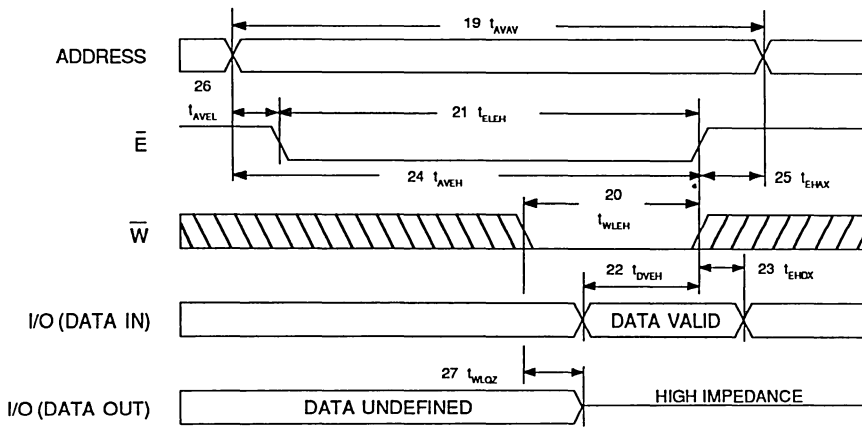
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	1423-25		1423-35		1423-45		1423-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		40		50		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		35		45		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		35		45		ns	
22	t_{DVEH}	t_{DW}	Data Set-up to End of Write	10		13		15		20		ns	
23	t_{EHDX}	t_{DH}	Data Hold After End of Write	3		3		3		5		ns	
24	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		25		30		40		ns	
25	t_{EHAX}	t_{WR}	Address Hold After End of Write	2		3		5		5		ns	
26	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		0		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	15	0	15	0	20	0	25	ns	f,j

Note f: Measured ± 200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1423 has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), twelve address inputs (A_0-A_{11}), and four Data I/O lines. The $\overline{E}$ input controls device selection as well as active and standby modes. With $\overline{E}$ low, the device is selected and the twelve address inputs are decoded to select one 4-bit word out of 4K words. Read and Write operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the outputs are disabled and the power consumption is reduced to less than one-fourth of the active mode power with TTL levels and even lower with CMOS levels

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low The outputs remain active throughout READ CYCLE 1 and is valid at the specified address access time The address inputs may change at access time and as long as $\overline{E}$ remains low, the cycle time is equal to the address access time

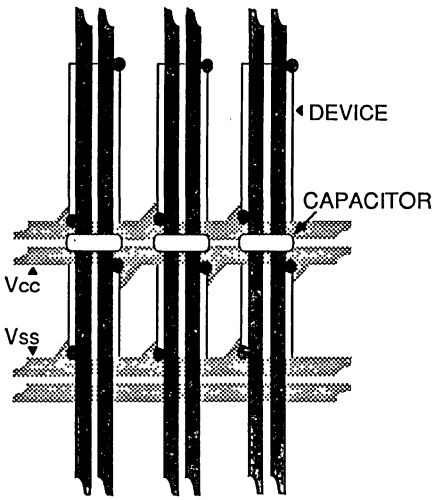
The READ CYCLE 2 waveform shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable when $\overline{E}$ goes low, valid data is at the outputs at the specified Chip Enable Access time. If address is not valid when $\overline{E}$ goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1423 is initiated by the latter of $\overline{E}$ or $\overline{W}$ to transition from a high level to a low level. In the case of $\overline{W}$ falling last, the output buffers will be turned on t_{ELQX} after the falling edge of $\overline{E}$ (just as in a read cycle). The output buffers are then turned off within t_{WLQZ} of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with common I/O configurations. Therefore input data should not be active until t_{WLQZ} to avoid bus contention

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. When $\overline{W}$ goes high at the end of the cycle with $\overline{E}$ active, the outputs of the memory become active. The data from the memory will be the same as the input data unless the input data or address changes

WRITE CYCLE 2 waveform shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, the outputs remain in the high impedance state.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

APPLICATION

It is imperative, when designing with any very high speed memory such as the IMS1423, that the fundamental rules in regard to memory board layout be followed to ensure proper system operation.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the wide operating margins of the IMS1423. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1423 have very high frequency components, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1μF, and be placed between each row of devices in the array (see drawing). A larger tantalum capacitor, with a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

The ground grid of the memory array should extend to the TTL periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

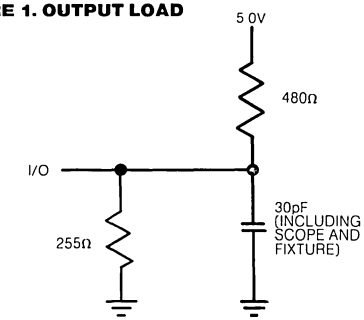
Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.

Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

FIGURE 1. OUTPUT LOAD

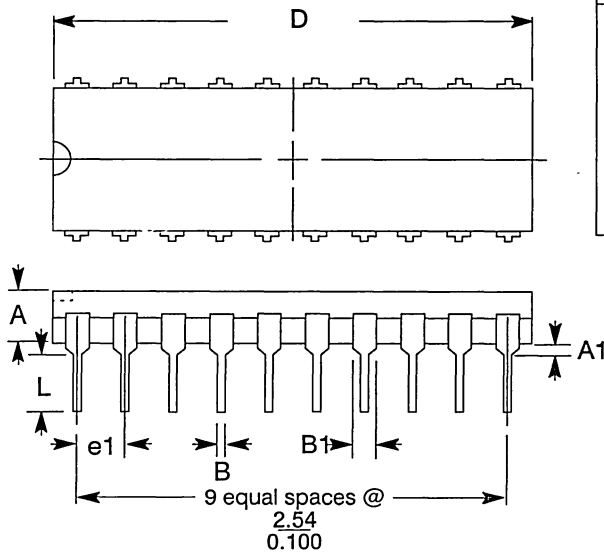


ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1423	25ns	PLASTIC DIP	IMS1423P-25
	25ns	PLASTIC SOJ	IMS1423E-25
	25ns	CERAMIC DIP	IMS1423S-25
	25ns	CERAMIC LCC	IMS1423W-25
	35ns	PLASTIC DIP	IMS1423P-35
	35ns	PLASTIC SOJ	IMS1423E-35
	35ns	CERAMIC DIP	IMS1423S-35
	35ns	CERAMIC LCC	IMS1423W-35
	45ns	PLASTIC DIP	IMS1423P-45
	45ns	PLASTIC SOJ	IMS1423E-45
	45ns	CERAMIC DIP	IMS1423S-45
	45ns	CERAMIC LCC	IMS1423W-45
	55ns	PLASTIC DIP	IMS1423P-55
	55ns	PLASTIC SOJ	IMS1423E-55
	55ns	CERAMIC DIP	IMS1423S-55
	55ns	CERAMIC LCC	IMS1423W-55

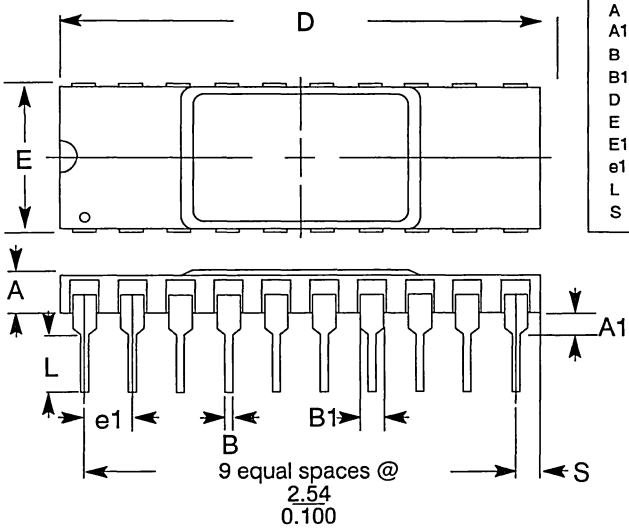
PACKAGING INFORMATION

20 Pin Plastic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.140	.015	3.566	.381
A1	.020	min	.508	min
B	.018	.003	.457	.152
B1	.060	Typ	1.524	Typ
D	1.035	.015	26.289	.381
E	.300	.003	7.620	.076
E1	.250		6.350	
e1	.100	.010	2.54	.254
eA	.330	.020	8.382	.508
L	.120	min	3.048	min

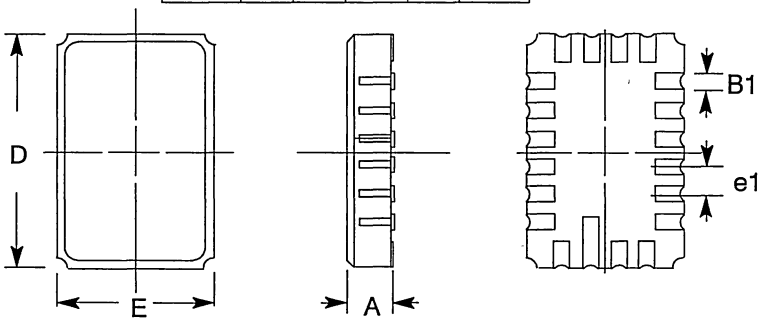
20 Pin Ceramic Dual-In-Line



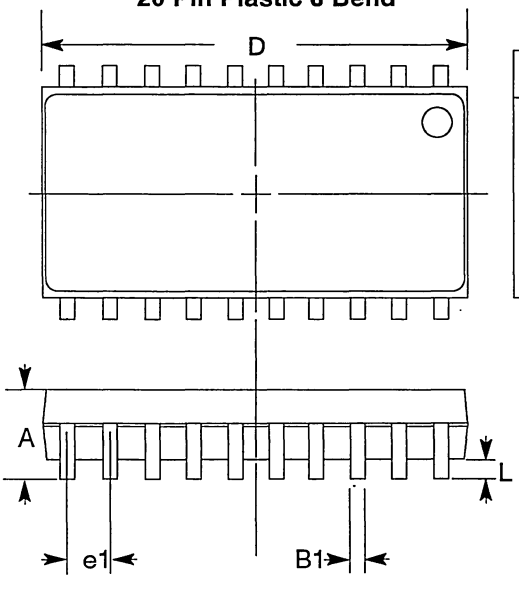
Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.096	.012	2.438	.305
A1	.015		.381	
B	.018	.003	.457	.152
B1	.054	Typ	.137	Typ
D	1.00	.015	25.40	.381
E	.315	.010	8.001	.254
E1	.295	.015	7.493	.381
e1	.100	.010	2.54	.254
L	.125	min	3.175	min
S	.005		.127	

20 Pin Leadless Chip Carrier

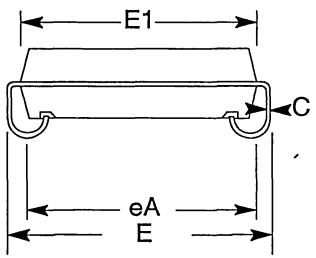
Dim	Inches		mm		Notes
	Nom	Tol	Nom	Tol	
A	.071	.007	1.803	.178	
B1	.025	.003	.635	.076	
D	.425	.010	10.795	.254	
E	.290	.010	7.360	.254	
e1	.050	.005	1.270		



20 Pin Plastic J Bend



Dim	Inches		mm		Notes
	Min	Max	Min	Max	
A	.120	.140	3.05	3.556	
B1	.014	.019	.350	.480	
C	.009	.0125	.230	.320	
D	.500	.510	12.70	12.95	
E	.335	.347	8.510	8.810	
E1	.292	.299	7.420	7.590	
e1	.050	.050	1.270	1.270	
eA	.262	.272	6.650	6.910	
L	.028	.036	.071	.091	



IMS1600
IMS1601L
CMOS
High Performance
64K x 1 Static RAM

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 64K x 1 Bit Organization
- 25, 30, 35, 45 and 55 nsec Access Times
- Fully TTL Compatible
- Separate Data Input & Output
- Three-state Output
- Power Down Function
- Single +5V ± 10% Operation
- 22-Pin, 300-mil DIP (JEDEC Std.)
- 22-Pin Ceramic LCC (JEDEC Std.)
- 24-Pin, 300-mil SOJ
- Battery Backup Operation - 2V Data Retention (L version only)

DESCRIPTION

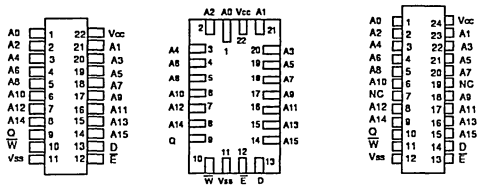
The INMOS IMS1600 is a high performance 64K x 1 CMOS Static RAM. The IMS1600 provides maximum density and speed enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1600 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1600 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

The IMS1601L is a low power version offering battery backup data retention operating from a 2 volt supply.

The IMS1600M and IMS1601LM are MIL-STD-883 versions intended for military applications.

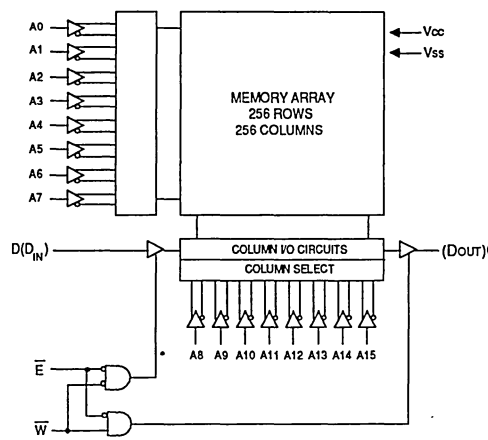
PIN CONFIGURATION



PIN NAMES

A_0 - A_{15}	ADDRESS INPUTS	Q	DATA OUTPUT
$\overline{W}$	WRITE ENABLE	Vcc	POWER
$\overline{E}$	CHIP ENABLE	Vss	GROUND
D	DATA INPUT		

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on Q.....-1.0 to (Vcc+0.5)
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One Second Duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+0.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0	25	70	°C	400 linear ft/min air flow

*V_{IL} min = -3 volts for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ 70°C) (Vcc = 5.0 V ± 10%)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		77 70	mA mA	tAVAV = 25ns and 30ns (PRELIM) tAVAV = 35, 45 and 55ns
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		25	mA	$\overline{E}$ ≥ V_{IH}. All other inputs at V_{IN} ≤ V_{IL} or ≥ V_{IH}
	IMS1601L version		15		
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		14	mA	$\overline{E}$ ≥ (Vcc - 0.2). All other inputs at V_{IN} ≤ 0.2 or ≥ (Vcc - 0.2V)
	IMS1601L version		2		
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		15	mA	$\overline{E}$ ≥ (Vcc - 0.2). Inputs cycling at V_{IN} ≤ 0.2 or ≥ (Vcc - 0.2V)
	IMS1601L version		5		
I_{ILK}	Input Leakage Current (Any Input)		±1	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		±5	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OL} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OH} = 8mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels .....Vss to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

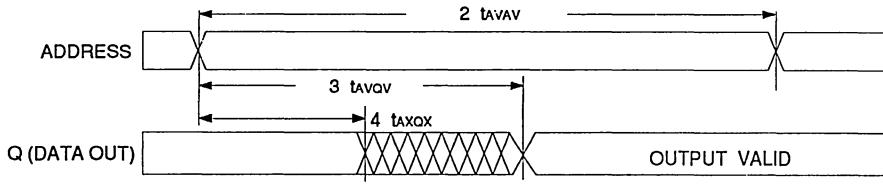
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[g]

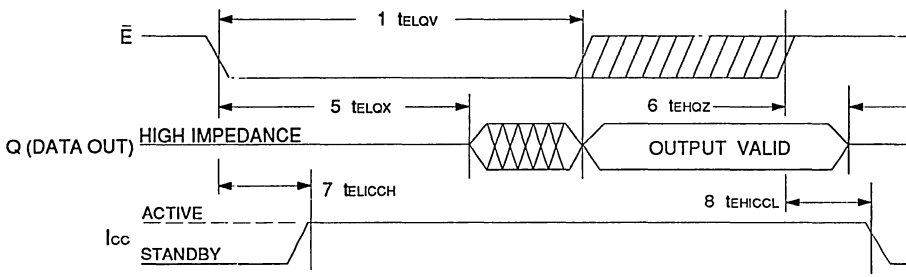
No.	SYMBOL		PARAMETER	IMS 1600-25 PRELIM		IMS 1600-30 PRELIM		IMS 1600-35 & 1601-35		IMS 1600-45 & 1601-45		IMS 1600-55 & 1601-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		30		35		45		55	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	25		30		35		45		55		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		25		30		35		45		55	ns	d
4	t_{AXQX}	t_{OH}	O/P Hold After Address Change	3		3		5		5		5		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to O/P Active	3		3		5		5		5		ns	j
6	t_{EHQZ}	t_{HZ}	Chip Disable to O/P Inactive	0	15	0	15	0	20	0	25	0	30	ns	f, j
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		0		0		ns	j
8	t_{EHICCL}	t_{PD}	Chip Enable to Power Down		25		30		35		45		55	ns	j
		t_T	I/P Rise and Fall Times		50		50		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



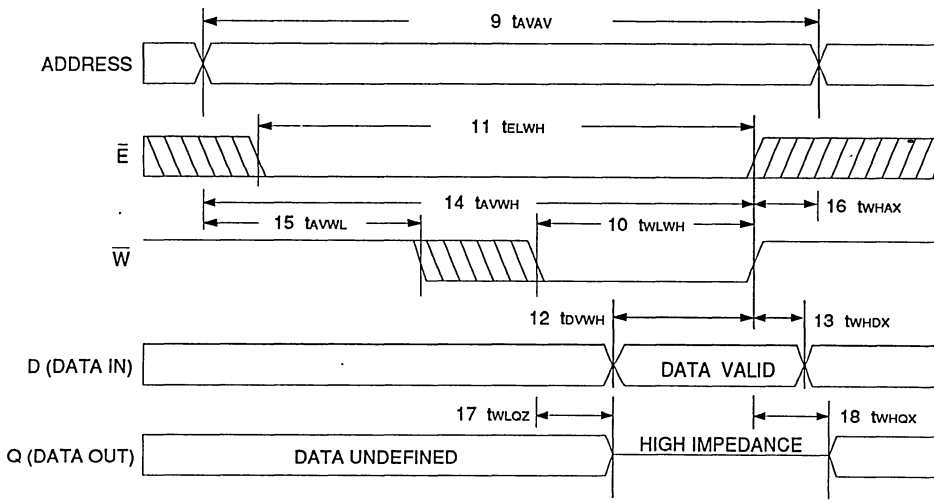
RECOMMENDED AC OPERATING CONDITIONS (0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ±10%)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g,h]

No	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1600-25 PRELIM MIN	IMS 1600-25 PRELIM MAX	IMS 1600-30 PRELIM MIN	IMS 1600-30 PRELIM MAX	IMS 1600-35 & 1601-35 MIN	IMS 1600-35 & 1601-35 MAX	IMS 1600-45 & 1601-45 MIN	IMS 1600-45 & 1601-45 MAX	IMS 1600-55 & 1601-55 MIN	IMS 1600-55 & 1601-55 MAX	UNITS	NOTES
9	tAVAV	tWC	Write Cycle Time	25		30		35		45		55		ns	
10	tWLWH	tWP	Write Plus Width	20		20		20		20		25		ns	
11	tELWH	tCW	Chip Enable to End of Write	20		20		30		30		30		ns	
12	tDVWH	tDW	Data Setup to End of Write	15		15		15		20		20		ns	
13	tWHDX	tDH	Data Hold after End of Write	0		0		0		0		0		ns	
14	tAVWH	tAW	Address Setup End of Write	20		20		25		25		30		ns	
15	tAVWL	tAS	Address Setup to Start of Write	5		5		5		5		5		ns	
16	tWHAX	tWR	Address Hold after End of Write	5		5		5		5		5		ns	
17	tWLQZ	tWZ	Write Enable to Output Disable	0	15	0	15	0	20	0	20	0	25	ns	f,j
18	tWHQX	tOW	Write Enable to Output Disable	0		0		0		0		0		ns	i

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



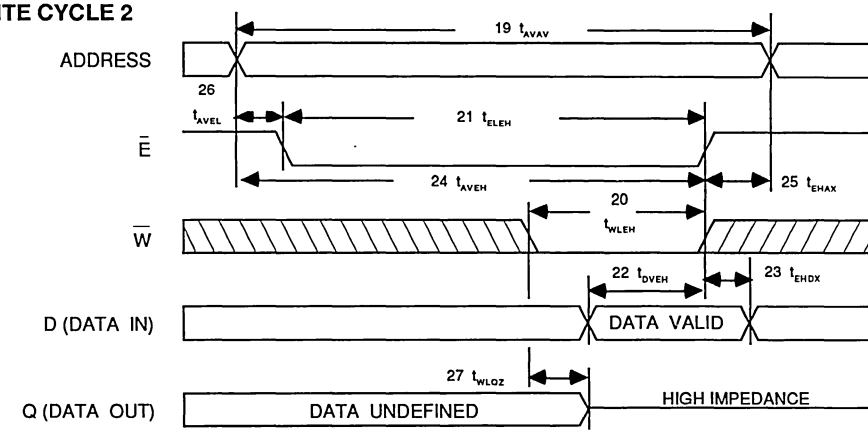
RECOMMENDED AC OPERATING CONDITIONS (0°C ≤ Ta ≤ 70°C) (Vcc = 5.0V ±10%)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

No	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1600-25 PRELIM MIN	IMS 1600-25 PRELIM MAX	IMS 1600-30 PRELIM MIN	IMS 1600-30 PRELIM MAX	IMS 1600-35 1601-35 MIN	IMS 1600-35 1601-35 MAX	IMS 1600-45 1601-45 MIN	IMS 1600-45 1601-45 MAX	IMS 1600-55 1601-55 MIN	IMS 1600-55 1601-55 MAX	UNITS	NOTES
19	tAVAV	tWC	Write Cycle Time	25		30		35		45		55		ns	
20	tWLEH	tWP	Write Plus Width	20		20		20		20		25		ns	
21	tELEH	tCW	Chip Enable to End of Write	20		20		30		30		30		ns	
22	tDVEH	tDW	Data Setup to End of Write	15		15		15		20		20		ns	
23	tEHDX	tDH	Data Hold after End of Write	0		0		0		0		0		ns	
24	tAVEH	tAW	Address Setup to End of Write	20		20		30		30		30		ns	
25	tEHAX	tWR	Address Hold after End of Write	5		5		5		5		5		ns	
26	tAVEL	tAS	Address Setup to Start of Write	0		0		0		0		0		ns	
27	tWLQZ	tWZ	Write Enable to Output Disable	0	15	0	15	0	20	0	20	0	25	ns	f,j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1600 has two control inputs, Chip Enable (/E) and Write Enable (/W), 16 address inputs (A0 -A15), a data in (D) and a data out (Q).

The /E input controls device selection as well as active and standby modes. With /E low, the device is selected and the 16 address inputs are decoded to select one memory cell out of 65,536. Read and Write operations on the memory cell are controlled by the /W input. With /E high, the device is deselected, the output is disabled and the power consumption is reduced to less than one-fourth of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as /W $\geq$ V_{IH} min with /E $\leq$ V_{IL} max. Read access time is measured from either /E going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while /E is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and long as /E remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by /E going low. As long as address is stable when /E goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when /E goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1600 is initiated by the latter of /E or /W to transition from a high to a low. In the case of /W falling last, the output buffer will be turned on t_{ELOX} after the falling edge of /E (just as in a read cycle). The output buffer is then turned off within t_{WLOZ} of the falling edge of /W. During this interval it is possible to have bus contention between devices with D and Q connected together in a common I/O configuration. Therefore input data should not be active until t_{WLOZ} to aviod bus contention.

WRITE CYCLE 1 waveform shows a write cycle terminated by /W going high. Data set-up and hold times are referenced to the rising edge of /W. When /W goes high at the end of the cycle with /E active, the output of the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by /E going high. Data set-up and hold times are referenced to the rising edge of /E. With /E high the output remains in the high impedance state.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1600. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Current transients associated with the operation of any high speed device have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad and be placed between each row of devices in the array. A larger tantalum capacitor of a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit area. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

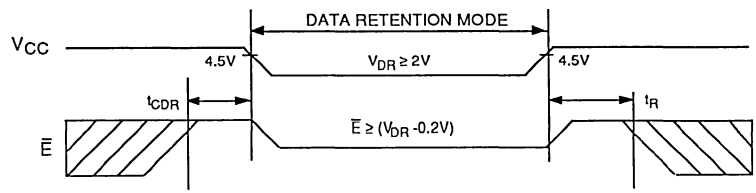
Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.

DATA RETENTION (L version only) ($0°C \le T_A \le 70°C$)

SYMBOL	PARAMETER	MIN	TYP*	MAX	UNITS	NOTES
V_{DR}	Data Retention Voltage	2.0			volts	$V_{IN} \le 0.2V$ or $\ge (V_{CC}-0.2V)$ $\overline{E} \ge (V_{CC}-0.2V)$
I_{CCDR1}	Data Retention Current		8	100	µA	V_{CC}= 3.0 volts
I_{CCDR2}	Data Retention Current		5	70	µA	V_{CC}= 2.0 volts
t_{EHVCCL}	Deselect Time (t_{CDR})	0			ns	j, k
t_{VCCHEL}	Recovery Time (t_R)	t_{RC}			ns	j, k (t_{RC}= Read Cycle Time)

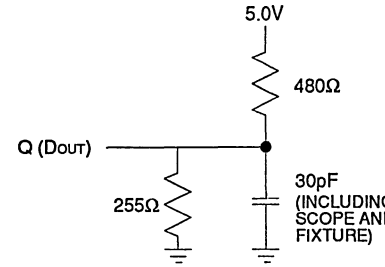
*Typical data retention parameters at 25°C.
Note j: Parameter guaranteed but not tested.
Note k: Supply recovery rate should not exceed 100mV per µs from V_{DR} to V_{CC} min.

LOW V_{CC} DATA RETENTION



Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

FIGURE 1. OUTPUT LOAD

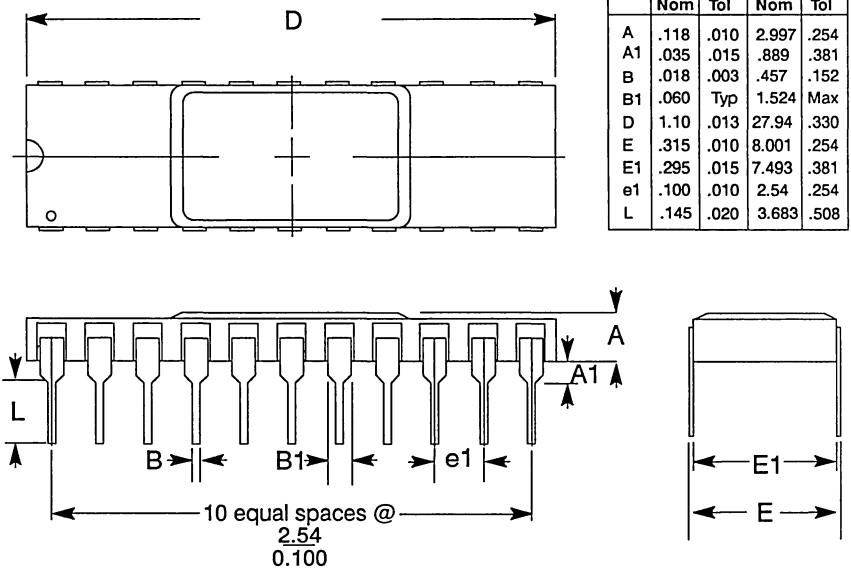


ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER	
			STANDARD	LOW POWER
IMS1600 IMS1601L	25ns	PLASTIC DIP	IMS1600P-25	
	25ns	CERAMIC DIP	IMS1600S-25	
	25ns	CERAMIC LCC	IMS1600W-25	
	25ns	PLASTIC SOJ	IMS1600E-25	
	30ns	PLASTIC DIP	IMS1600P-30	
	30ns	CERAMIC DIP	IMS1600S-30	
	30ns	CERAMIC LCC	IMS1600W-30	
	30ns	PLASTIC SOJ	IMS1600E-30	
	35ns	PLASTIC DIP	IMS1600P-35	IMS1601LP35
	35ns	CERAMIC DIP	IMS1600S-35	IMS1601LS35
	35ns	CERAMIC LCC	IMS1600W-35	IMS1601LW35
	35ns	PLASTIC SOJ	IMS1600E-35	IMS1601LE35
	45ns	PLASTIC DIP	IMS1600P-45	IMS1601LP45
	45ns	CERAMIC DIP	IMS1600S-45	IMS1601LS45
	45ns	CERAMIC LCC	IMS1600W-45	IMS1601LW45
	45ns	PLASTIC SOJ	IMS1600E-45	IMS1601LE45
	55ns	PLASTIC DIP	IMS1600P-55	IMS1601LP55
	55ns	CERAMIC DIP	IMS1600S-55	IMS1601LS55
	55ns	CERAMIC LCC	IMS1600W-55	IMS1601LW55
	55ns	PLASTIC SOJ	IMS1600E-55	IMS1601LE55

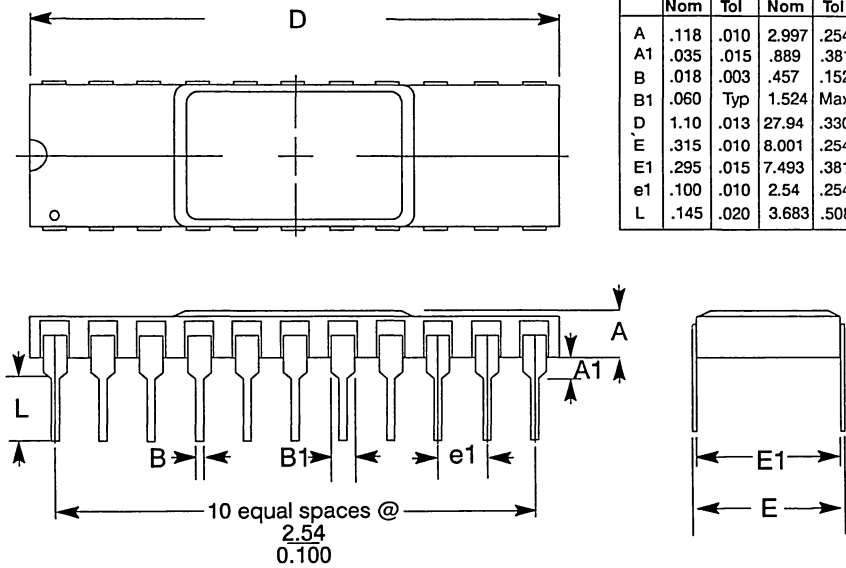
PACKAGING INFORMATION

22 Pin Dual-In-Line-Package



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.118	.010	2.997	.254
A1	.035	.015	.889	.381
B	.018	.003	.457	.152
B1	.060	Typ	1.524	Max
D	1.10	.013	27.94	.330
E	.315	.010	8.001	.254
E1	.295	.015	7.493	.381
e1	.100	.010	2.54	.254
L	.145	.020	3.683	.508

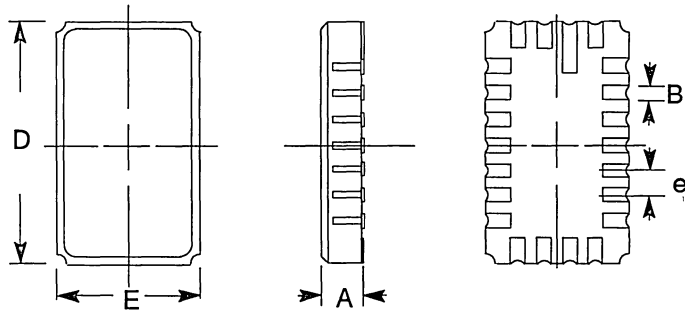
22 Pin Ceramic Dual-In-Line



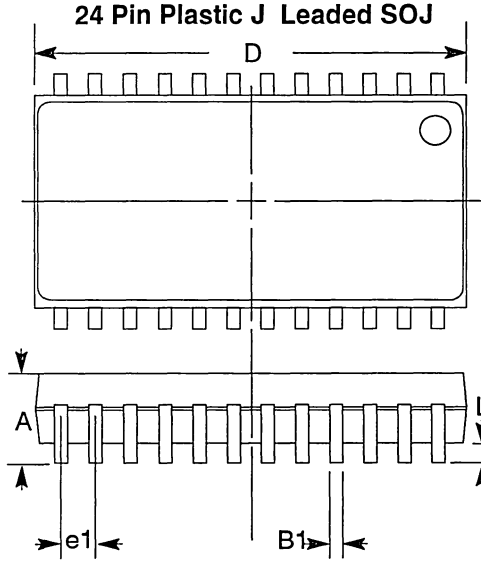
Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.118	.010	2.997	.254
A1	.035	.015	.889	.381
B	.018	.003	.457	.152
B1	.060	Typ	1.524	Max
D	1.10	.013	27.94	.330
E	.315	.010	8.001	.254
E1	.295	.015	7.493	.381
e1	.100	.010	2.54	.254
L	.145	.020	3.683	.508

22 Pin Leadless Chip Carrier

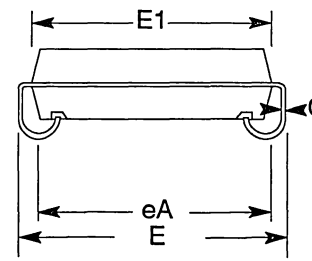
Dim	Inches		mm		Notes
	Nom	Tol	Nom	Tol	
A	.071	.007	1.803	.178	
B1	.025	.003	.635	.076	
D	.490	.006	13.446	.152	
E	.290	.006	7.366	.152	
e1	.050		1.270		



24 Pin Plastic J Leaded SOJ



Dim	Inches		mm		Notes
	Min	Max	Min	Max	
A	.120	.140	3.048	3.556	
B1	.014	.019	.356	.483	
C	.010		.254		
D	.602	.612	15.291	15.545	
E	.335	.347	8.509	8.814	
E1	.292	.299	7.417	7.595	
e1	.050	.050	1.270	1.270	
eA	.262	.272	6.655	6.909	
L	.028	.036	.711	.914	



IMS1620
CMOS
High Performance
16K x 4 Static RAM

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 16K x 4 Bit Organization
- 25, 30, 35, 45 and 55 nsec Access Times
- Fully TTL Compatible
- Common Data Input & Output
- Three-state Output
- Power Down Function
- Single +5V ± 10% Operation
- 22-Pin, 300-mil DIP (JEDEC Std.)
- 22-Pin Ceramic LCC (JEDEC Std.)
- 24-Pin, 300-mil SOJ

DESCRIPTION

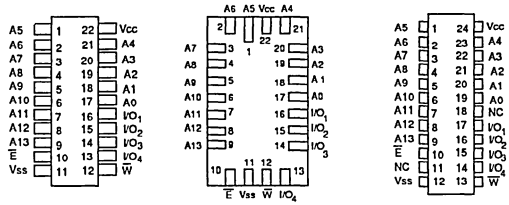
The INMOS IMS1620 is a high performance 16K x 4 CMOS Static RAM. The IMS1620 provides maximum density and speed enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1620 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1620 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

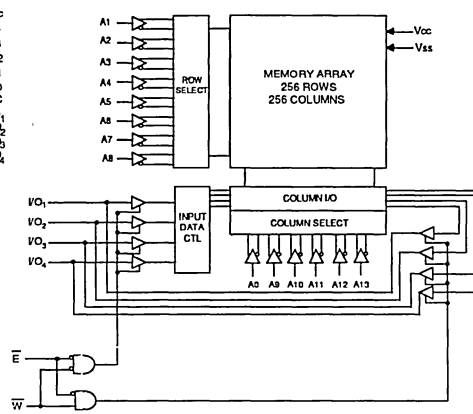
The IMS1624 is the functional equivalent of the IMS1620 with the addition of an Output Enable input.

The IMS1620M and IMS1620LM are MIL-STD-883 versions intended for military applications.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{13} ADDRESS INPUTS	I/O DATA IN/OUT
$\overline{W}$ WRITE ENABLE	Vcc POWER (+5V)
$\overline{E}$ CHIP ENABLE	Vss GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on I/O.....-1.0 to Vcc+0.5
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One output at a time, one second duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0	25	70	°C	400 linear ft/min air flow

*V_{IL} min = -3 volts for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		110 100	mA mA	t_{AVAV} = 25ns and 30ns t_{AVAV} = 35, 45 and 55ns
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		25	mA	$\bar{E} \geq V_{IH}$. All other inputs at $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		14	mA	$\bar{E} \geq$ (Vcc - 0.2) . All other inputs at $V_{IN} \leq$ 0.2 or $\geq$ (Vcc - 0.2V)
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		17	mA	$\bar{E} \geq$ (Vcc - 0.2). Inputs cycling at $V_{IN} \leq$ 0.2 or $\geq$ (Vcc - 0.2V)
I_{ILK}	Input Leakage Current (Any Input)		±1	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		±5	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 8mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels .....Vss to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0MHZ)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested

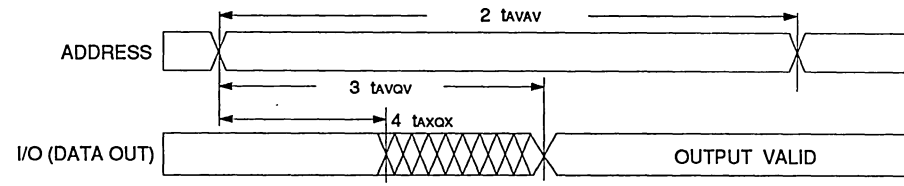
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[g]

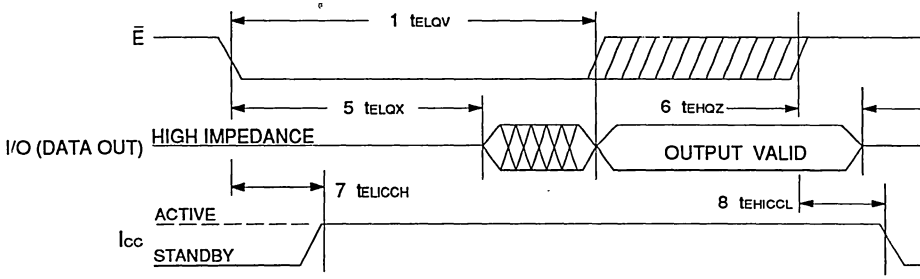
No	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1620-25 MIN	IMS 1620-25 MAX	IMS 1620-30 MIN	IMS 1620-30 MAX	IMS 1620-35 MIN	IMS 1620-35 MAX	IMS 1620-45 MIN	IMS 1620-45 MAX	IMS 1620-55 MIN	IMS 1620-55 MAX	UNITS	NOTES
1	tELQV	tACS	Chip Enable Access Time		25		30		35		45		55	ns	
2	tAVAV	tRC	Read Cycle Time	25		30		35		45		55		ns	c
3	tAVQV	tAA	Address Access Time		25		30		35		45		55	ns	d
4	tAXQX	tOH	O/P Hold After Address Change	5		5		5		5		5		ns	
5	tELQX	tLZ	Chip Enable to O/P Active	5		5		5		5		5		ns	j
6	tEHQZ	tHZ	Chip Disable to Output Inactive	0	15	0	15	0	15	0	20	0	25	ns	f, j
7	tELICCH	tPU	Chip Enable to Power Up	0		0		0		0		0		ns	j
8	tEHICCL	tPD	Chip Enable to Power Down		25		30		35		45		55	ns	j
		tT	Input Rise and Fall Times		50		50		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



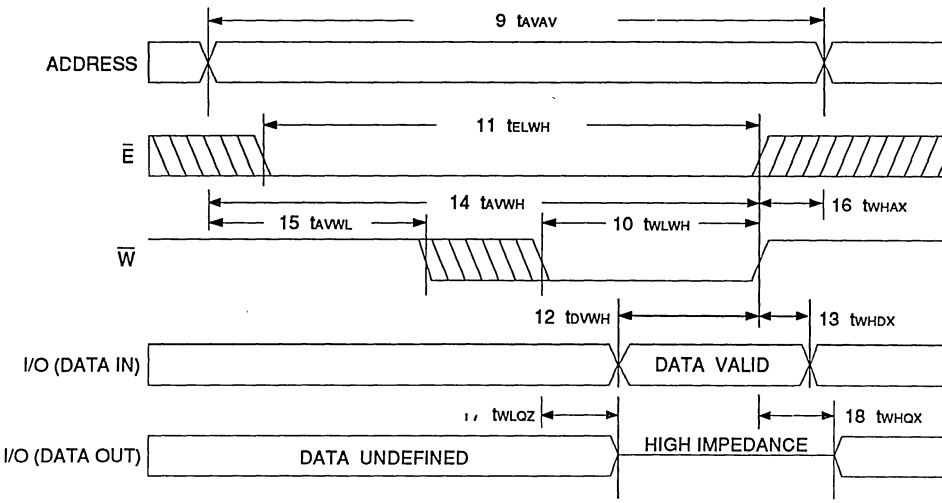
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g,h]

No	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1620-25 MIN	IMS 1620-25 MAX	IMS 1620-30 MIN	IMS 1620-30 MAX	IMS 1620-35 MIN	IMS 1620-35 MAX	IMS 1620-45 MIN	IMS 1620-45 MAX	IMS 1620-55 MIN	IMS 1620-55 MAX	UNITS	NOTES
9	tAVAV	tWC	Write Cycle Time	25		30		35		45		55		ns	
10	tWLWH	tWP	Write Pulse Width	20		20		30		30		40		ns	
11	tELWH	tCW	Chip Enable to End of Write	20		20		30		30		40		ns	
12	tDVWH	tDW	Data Setup to End of Write	13		15		15		20		25		ns	
13	tWHDX	tDH	Data Hold after End of Write	0		0		0		0		0		ns	
14	tAVWH	tAW	Address Setup End of Write	20		25		30		30		40		ns	
15	tAVWL	tAS	Address Setup to Start of Write	0		0		0		0		0		ns	
16	tWHAX	tWR	Address Hold after End of Write	5		5		5		0		0		ns	
17	tWLQZ	tWZ	Write Enable to Output Disable	0	15	0	15	0	20	0	20	0	25	ns	f,j
18	tWHQX	tOW	Write Enable to Output Disable	0		0		0		0		0		ns	i

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



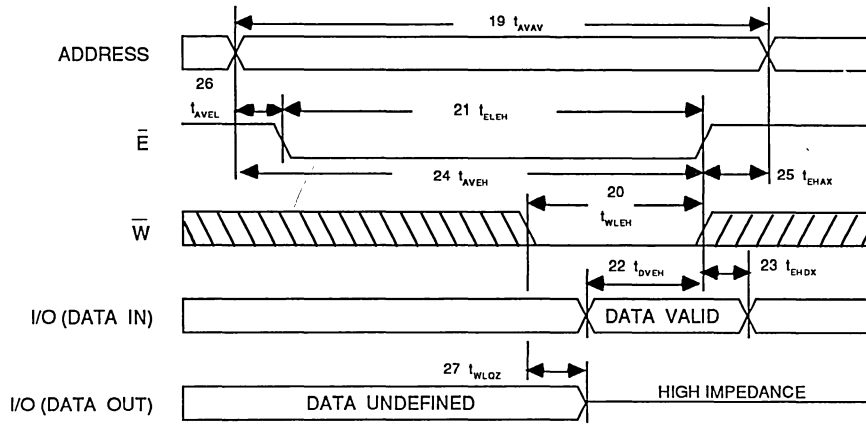
RECOMMENDED AC OPERATING CONDITIONS (0°C ≤ Ta ≤ 70°C) (Vcc = 5.0V ±10%)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

No	SYMBOL		PARAMETER	IMS 1620-25		IMS 1620-30		IMS 1620-35		IMS 1620-45		IMS 1620-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
19	tAVAV	tWC	Write Cycle Time	25		30		35		45		55		ns	
20	tWLEH	tWP	Write Pulse Width	20		20		30		30		40		ns	
21	tELEH	tCW	Chip Enable to End of Write	20		20		30		30		40		ns	
22	tDVEH	tDW	Data Setup to End of Write	13		15		15		20		25		ns	
23	tEHDX	tDH	Data Hold after End of Write	0		0		0		0		0		ns	
24	tAVEH	tAW	Address Setup to End of Write	20		25		30		30		40		ns	
25	tEHAX	tWR	Address Setup to Start of Write	5		5		5		0		0		ns	
26	tAVEL	tAS	Address Hold after End of Write	0		0		0		0		0		ns	
27	tWLQZ	tWZ	Write Enable to Output Disable	0	15	0	15	0	15	0	20	0	25	ns	f,j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1620 has two control inputs, Chip Enable (/E) and Write Enable (/W), 14 address inputs (A0 -A13), and four Data I/O pins.

The /E input controls device selection as well as active and standby modes. With /E low, the device is selected and the 14 address inputs are decoded to select one 4-bit word out of 16,384. Read and Write operations on the memory cells are controlled by the /W input. With /E high, the device is deselected, the outputs are disabled and the power consumption is reduced to less than one-fourth of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as /W $\geq$ V_{IH} min with /E $\leq$ V_{IL} max. Read access time is measured from either /E going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while /E is low. The outputs remain active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and long as /E remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by /E going low. As long as address is stable when /E goes low, valid data is at the outputs at the specified Chip Enable Access time. If address is not valid when /E goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1620 is initiated by the latter of /E or /W to transition from a high to a low. In the case of /W falling last, the output buffers are turned on t_{ELOX} after the falling edge of /E (just as in a read cycle). The output buffers are then turned off within t_{WLOZ} of the falling edge of /W. During this interval it is possible to have bus contention between devices with common I/O configurations. Therefore input data should not be active until t_{WLOZ} to aviod bus contention.

WRITE CYCLE 1 waveform shows a write cycle terminated by /W going high. Data set-up and hold times are referenced to the rising edge of /W. When /W goes high at the end of the cycle with /E active, the output of the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by /E going high. Data set-up and hold times are referenced to the rising edge of /E. With /E high the outputs remain in the high impedance state.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1620. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Current transients associated with the operation of any high speed device have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad and be placed between each row of devices in the array. A larger tantalum capacitor of a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit area This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

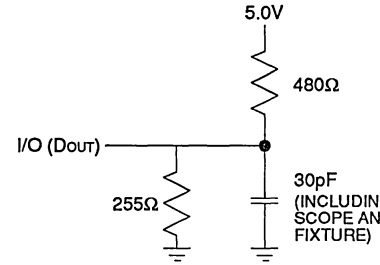
Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.

Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

FIGURE 1. OUTPUT LOAD

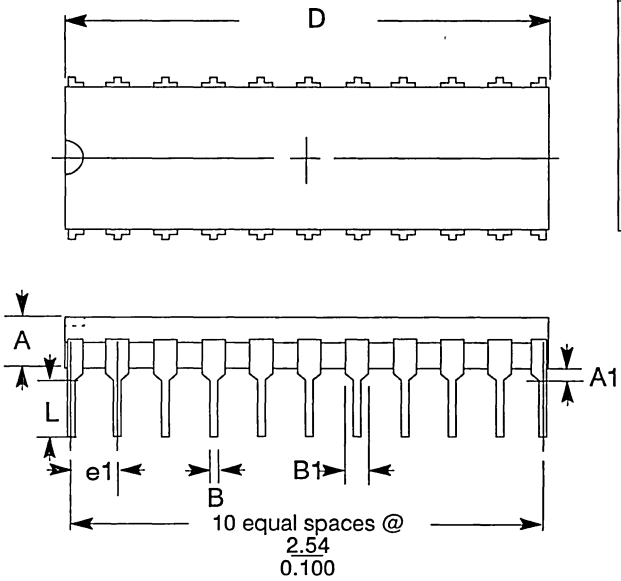


ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1620	25ns	PLASTIC DIP	IMS1620P-25
	25ns	CERAMIC DIP	IMS1620S-25
	25ns	CERAMIC LCC	IMS1620W-25
	25ns	PLASTIC SOJ	IMS1620E-25
	30ns	PLASTIC DIP	IMS1620P-30
	30ns	CERAMIC DIP	IMS1620S-30
	30ns	CERAMIC LCC	IMS1620W-30
	30ns	PLASTIC SOJ	IMS1620E-30
	35ns	PLASTIC DIP	IMS1620P-35
	35ns	CERAMIC DIP	IMS1620S-35
	35ns	CERAMIC LCC	IMS1620W-35
	35ns	PLASTIC SOJ	IMS1620E-35
	45ns	PLASTIC DIP	IMS1620P-45
	45ns	CERAMIC DIP	IMS1620S-45
	45ns	CERAMIC LCC	IMS1620W-45
	45ns	PLASTIC SOJ	IMS1620E-45
	55ns	PLASTIC DIP	IMS1620P-55
	55ns	CERAMIC DIP	IMS1620S-55
	55ns	CERAMIC LCC	IMS1620W-55
	55ns	PLASTIC SOJ	IMS1620E-55

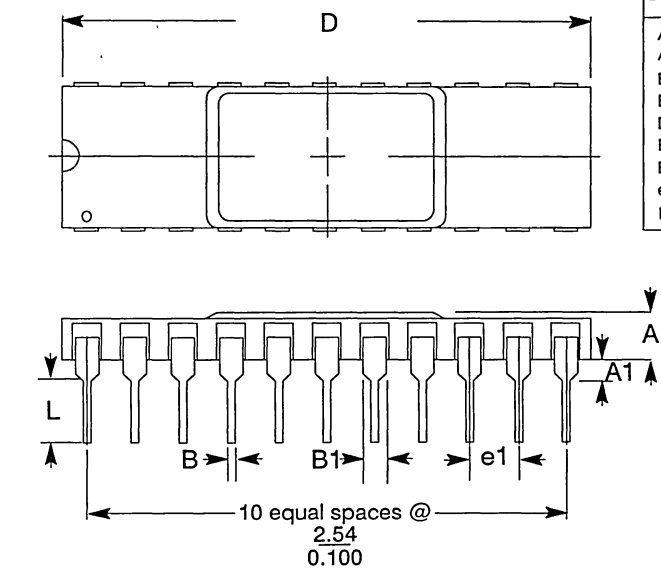
PACKAGING INFORMATION

22 Pin Plastic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.140	.015	3.566	.381
A1	.020	min	.508	min
B	.018	.003	.457	.152
B1	.060	Typ	1.524.	Typ
D	1.035	.015	26.289	.381
E	.300	.003	7.620	.076
E1	.250		6.350	
e1	.100	.010	2.54	.254
eA	.330	.020	8.382	.508
L	.120	min	3.048	min

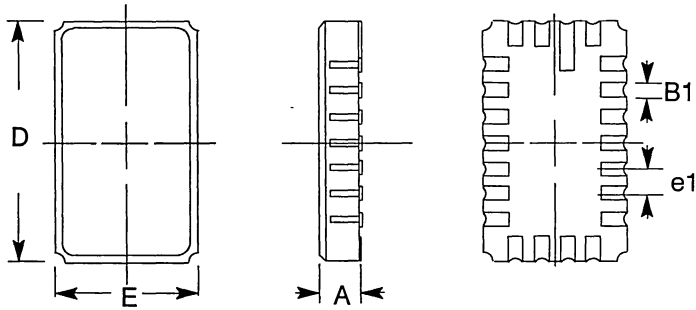
22 Pin Ceramic Dual-In-Line



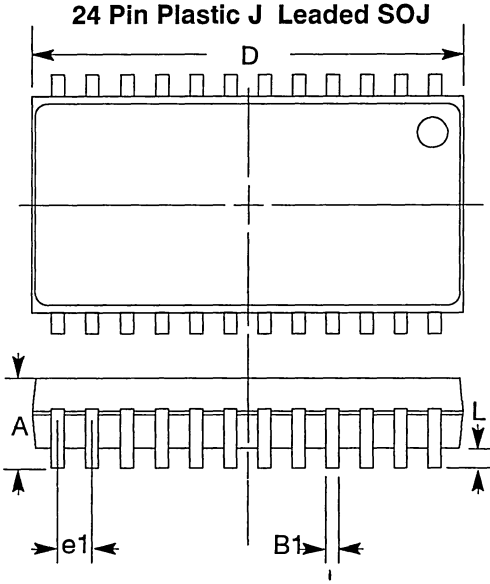
Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.118	.010	2.997	.254
A1	.035	.015	.889	.381
B	.018	.003	.457	.152
B1	.060	Typ	1.524	Max
D	1.10	.013	27.94	.330
E	.315	.010	8.001	.254
E1	.295	.015	7.493	.381
e1	.100	.010	2.54	.254
L	.145	.020	3.683	.508

22 Pin Leadless Chip Carrier

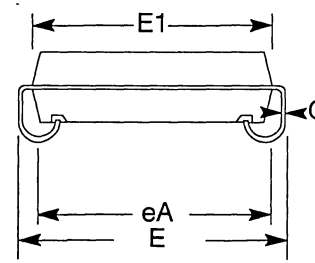
Dim	Inches		mm		Notes
	Nom	Tol	Nom	Tol	
A	.071	.007	1.803	.178	
B1	.025	.003	.635	.076	
D	.490	.006	13.446	.152	
E	.290	.006	7.366	.152	
e1	.050		1.270		



24 Pin Plastic J Leaded SOJ



Dim	Inches		mm		Notes
	Min	Max	Min	Max	
A	.120	.140	3.048	3.556	
B1	.014	.019	.356	.483	
C	.010		.254		
D	.602	.612	15.291	15.545	
E	.335	.347	8.509	8.814	
E1	.292	.299	7.417	7.595	
e1	.050	.050	1.270	1.270	
eA	.262	.272	6.655	6.909	
L	.028	.036	.711	.914	



IMS1624
CMOS
High Performance
16K x 4 Static RAM
with Output Enable

inmos®

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 16K x 4 Bit Organization with Output Enable
- 25, 30, 35, 45 and 55 nsec Address Access Times
- 25, 30, 35, 45 and 55 nsec Chip Enable Access Times
- Fully TTL Compatible
- Common Data Input & Output
- Three-state Output
- Power Down Function
- Single +5V ± 10% Operation
- 24-Pin, 300-mil DIP (JEDEC Std.)
- 28-Pin Ceramic LCC (JEDEC Std.)
- 24-Pin, 300-mil SOJ

DESCRIPTION

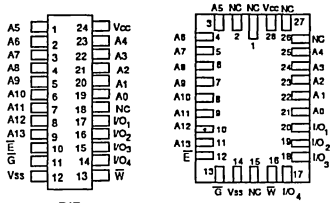
The INMOS IMS1624 is a high performance 16K x 4 CMOS Static RAM. The IMS1624 provides maximum density and speed enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1624 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The IMS1624 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode. The IMS1624 also includes an Output Enable (/G) for fast access to data and enhanced bus contention control.

The IMS1624 is the functional equivalent of the IMS1620 with the addition of an Output Enable input.

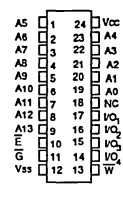
The IMS1624M and IMS1624LM are MIL-STD-883 versions intended for military applications.

PIN CONFIGURATION



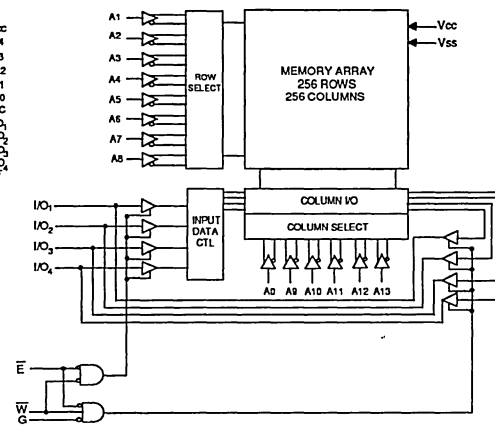
DIP CHIP CARRIER

LOGIC SYMBOL



SOJ

BLOCK DIAGRAM



PIN NAMES

A_0-A_{13}	ADDRESS INPUTS	I/O	DATA IN/OUT
$\overline{W}$	WRITE ENABLE	Vcc	POWER (+5V)
$\overline{E}$	CHIP ENABLE	Vss	GROUND
$\overline{G}$	OUTPUT ENABLE		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on I/O.....-1.0 to Vcc+0.5
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One output at a time, one second duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0	25	70	°C	400 linear ft/min air flow

*V_{IL} min = -3 volts for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ± 10%)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		110 100	mA mA	t_{AVAV} = 25ns and 30ns t_{AVAV} = 35, 45, and 55ns
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		25	mA	$\overline{E}$ ≥ V_{IH}. All other inputs at V_{IN} ≤ V_{IL} or ≥ V_{IH}
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		14	mA	$\overline{E}$ ≥ (Vcc - 0.2). All other inputs at V_{IN} ≤ 0.2 or ≥ (Vcc - 0.2V)
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		17	mA	$\overline{E}$ ≥ (Vcc - 0.2). Inputs cycling at V_{IN} ≤ 0.2 or ≥ (Vcc - 0.2V)
I_{ILK}	Input Leakage Current (Any Input)		±1	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		±5	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 8mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels .....V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0MHZ)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested

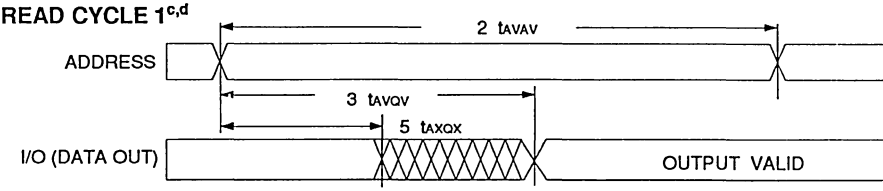
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[g]

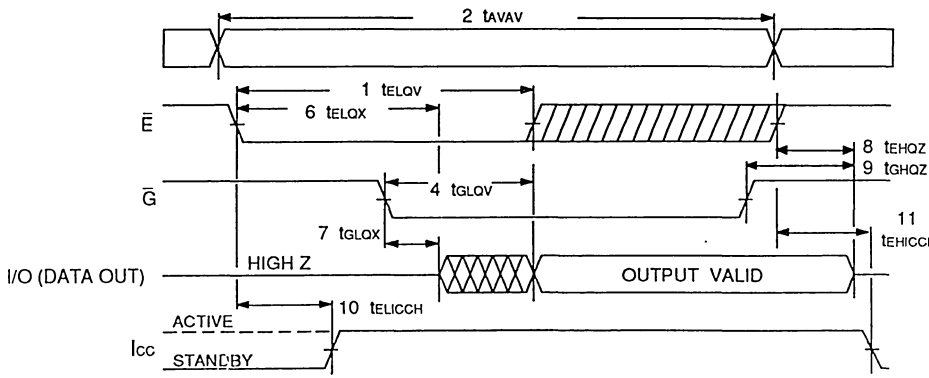
No	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1624-25 MIN	IMS 1624-25 MAX	IMS 1624-30 MIN	IMS 1624-30 MAX	IMS 1624-35 MIN	IMS 1624-35 MAX	IMS 1624-45 MIN	IMS 1624-45 MAX	IMS 1624-55 MIN	IMS 1624-55 MAX	UNITS	NOTES
1	tELQV	tACS	Chip Enable Access Time		25		30		35		45		55	ns	
2	tAVAV	tRC	Read Cycle Time	25		30		35		45		55		ns	c
3	tAVQV	tAA	Address Access Time		25		30		35		45		55	ns	d
4	tGLQV	tTOE	O/P Enable Access Time		15		15		20		20		25	ns	
5	tAXQX	tOH	O/P Hold After Address Change	5		5		5		5		5		ns	j
6	tELQX	tLZ	O/P Enable to O/P Active	5		5		5		5		5		ns	j
7	tGLQX	tOLZ	O/P Enable to O/P Active	0		0		0		0		0		ns	j
8	tEHQZ	tHZ	Chip Disable to Output Inactive	0	15	0	15	0	15	0	20	0	25	ns	f, j
9	tGHQZ	tOHZ	O/P Disable to Output Inactive	0	15	0	15	0	15	0	20	0	25	ns	f, j
10	tELICCH	tPU	Chip Enable to Power Up	0		0		0		0		0		ns	j
11	tEHICCL	tPD	Chip Disable to Power Down		25		30		35		45		55	ns	j
		tT	Input Rise and Fall Times		50		50		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ and $\overline{G}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$, $\overline{G}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



RECOMMENDED AC OPERATING CONDITIONS (0°C ≤ TA ≤ 70°C) (Vcc = 5.0V ±10%)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g,h]

No	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1624-25 MIN	IMS 1624-25 MAX	IMS 1624-30 MIN	IMS 1624-30 MAX	IMS 1624-35 MIN	IMS 1624-35 MAX	IMS 1624-45 MIN	IMS 1624-45 MAX	IMS 1624-55 MIN	IMS 1624-55 MAX	UNITS	NOTES
12	tAVAV	t WC	Write Cycle Time	25		30		35		45		55		ns	
13	tWLWH	t WP	Write Pulse Width	20		20		30		30		40		ns	
14	tELWH	t CW	Chip Enable to End of Write	20		20		30		30		40		ns	
15	tDVWH	t DW	Data Setup to End of Write	13		15		15		20		25		ns	
16	tWHDX	t DH	Data Hold after End of Write	0		0		0		0		0		ns	
17	tAVWH	t AW	Address Setup to End of Write	20		25		30		30		40		ns	
18	tAVWL	t AS	Address Setup to Start of Write	0		0		0		0		0		ns	
19	tWHAX	t WR	Address Hold after End of Write	5		5		5		0		0		ns	
20	tWLQZ	t WZ	Write Enable to Output Disable	0	15	0	15	0	15	0	20	0	25	ns	f,j
21	tWHQX	t OW	O/P Active after end of Write	0		0		0		0		0		ns	j

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g,h]

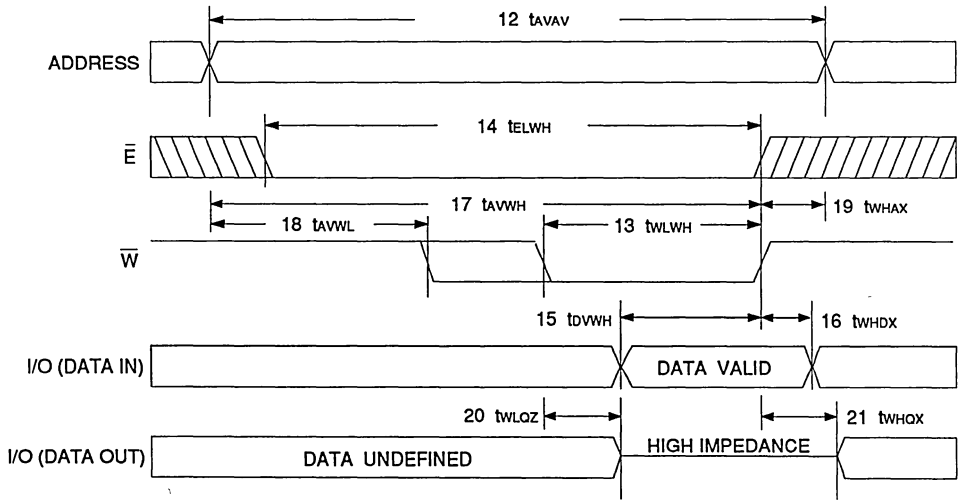
No	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1624-25 MIN	IMS 1624-25 MAX	IMS 1624-30 MIN	IMS 1624-30 MAX	IMS 1624-35 MIN	IMS 1624-35 MAX	IMS 1624-45 MIN	IMS 1624-45 MAX	IMS 1624-55 MIN	IMS 1624-55 MAX	UNITS	NOTES
22	tAVAV	t WC	Write Cycle Time	25		30		35		45		55		ns	
23	tWLEH	t WP	Write Pulse Width	20		20		30		30		40		ns	
24	tELEH	t CW	Chip Enable to End of Write	20		20		30		30		40		ns	
25	tDVEH	t DW	Data Setup to End of Write	13		15		15		20		25		ns	
26	tEHDX	t DH	Data Hold after End of Write	0		0		0		0		0		ns	
27	tAVEH	t AW	Address Setup to End of Write	20		25		30		30		40		ns	
28	tEHAX	t WR	Address Hold after End of Write	5		5		5		0		0		ns	
29	tAVEL	t AS	Address Setup to Start of Write	0		0		0		0		0		ns	
30	tWLQZ	t WZ	Write Enable to Output Disable	0	15	0	15	0	15	0	20	0	25	ns	f,j

WRITE CYCLE 3: Fast Write, Outputs Disabled[g,h]

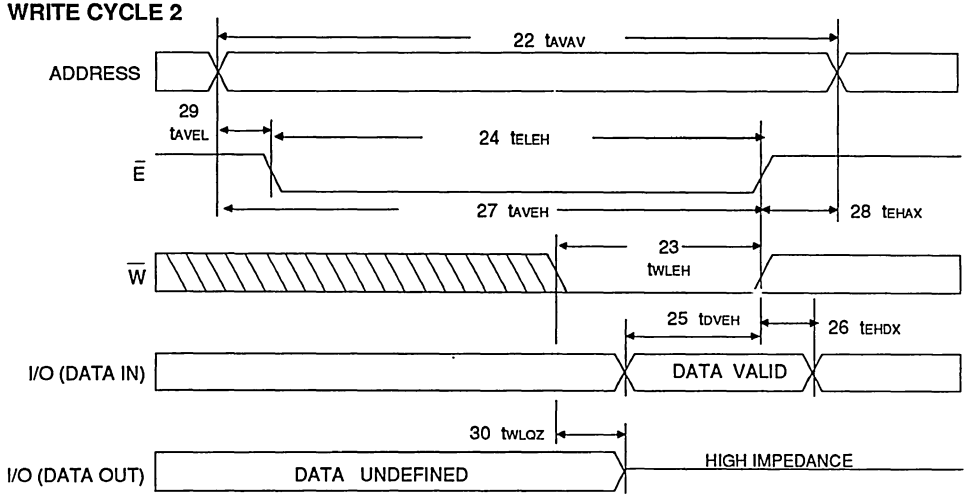
No	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1624-25 MIN	IMS 1624-25 MAX	IMS 1624-30 MIN	IMS 1624-30 MAX	IMS 1624-35 MIN	IMS 1624-35 MAX	IMS 1624-45 MIN	IMS 1624-45 MAX	IMS 1624-55 MIN	IMS 1624-55 MAX	UNITS	NOTES
31	tAVAV	t WC	Write Cycle Time	18		20		20		25		30		ns	
32	tWLWH	t WP	Write Pulse Width	13		15		15		20		25		ns	
33	tDVWH	t DW	Data Setup to End of Write	18		20		20		25		30		ns	
34	tWHDX	t DH	Data Hold after End of Write	0		0		0		0		0		ns	
35	tAVWH	t AW	Address Setup to End of Write	12		15		15		20		25		ns	
36	tWHAX	t WR	Address Hold after End of Write	5		5		5		0		0		ns	
37	tAVWL	t AS	Address Setup to Start of Write	0		0		0		0		0		ns	

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$, $\overline{G}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

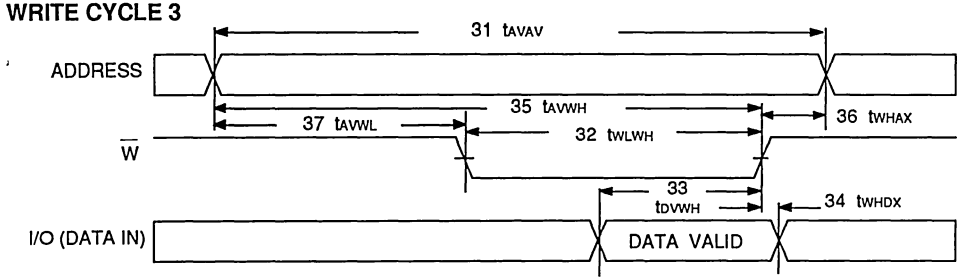
WRITE CYCLE 1



WRITE CYCLE 2



WRITE CYCLE 3



DEVICE OPERATION

The IMS1624 has three control inputs, Chip Enable (/E), Output Enable (/G) and Write Enable (/W), 14 address inputs (A0 -A13), and four Data I/O pins.

The /E input controls device selection as well as active and standby modes. With /E low, the device is selected and the 14 address inputs are decoded to select one 4-bit word out of 16,384. Read and Write operations on the memory cells are controlled by the /W and /G inputs. With /E high, the device is deselected, the outputs are disabled and the power consumption is reduced to less than one-fourth of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as /W $\geq$ V_{IH} min with /E and /G $\leq$ V_{IL} max. Read access time is measured from the latter of either /E or /G going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while /E and /G are low. The outputs remain active throughout READ CYCLE 1 and are valid at the specified address access time. The address inputs may change at access time and long as /E and /G remain low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated bythe latter of /E or /G going low. As long as address is stable when /E goes low, valid data is at the outputs at thelatter of specified Chip Enable Access or Output Enable Access times. If address is not valid when /E goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

Since /G controls the output buffers, /G is required to be low in order for the outputs to be active.

WRITE CYCLE

The write cycle of the IMS1624 is initiated by the latter of /E or /W to transition from a high to a low. In the case of /W falling last, the output buffers are turned on t_{ELOX} after the falling edge of /E if /G is already low (just as in a read cycle). The output buffers are then turned off within t_{WLOZ} of the falling edge of /W. During this interval it is possible to have bus contention between devices with common I/O configurations. Therefore input data should not be active until t_{WLOZ}. To aviod bus contention, the /G input can be held high throughout the write operation.

WRITE CYCLE 1 waveform shows a write cycle terminated by /W going high. Data set-up and hold times are referenced to the rising edge of /W. When /W goes high at the end of the cycle with /E active, the output of the memory becomes active (if /G is low). The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by /E going high. Data set-up and hold times are referenced to the rising edge of /E. With /E high the outputs remain in the high impedance state.

WRITE CYCLE 3 waveform shows a write cycle controlled by /W, with /G high and /E low throughout the cycle. As the outputs will not become active during this operation, maximum data bandwidth is provided by allowing very short write cycles and eliminating any bus contention considerations.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1624. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Current transients associated with the operation of any high speed device have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad and be placed between each row of devices in the array. A larger tantalum capacitor of a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit area This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

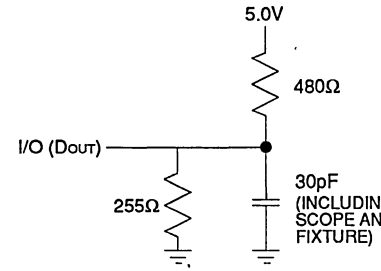
Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.

Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

FIGURE 1. OUTPUT LOAD

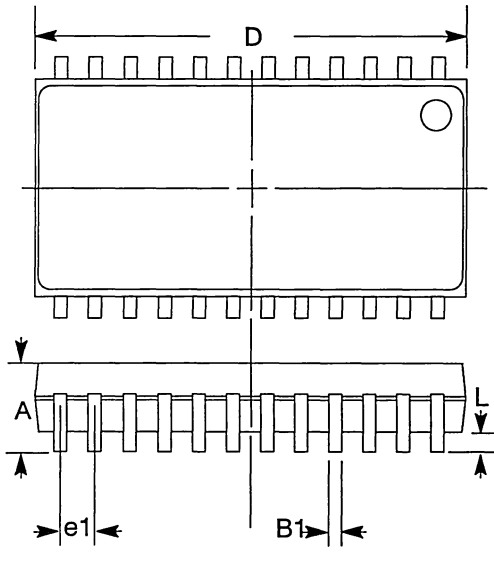


ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1624	25ns	PLASTIC DIP	IMS1624P-25
	25ns	CERAMIC DIP	IMS1624S-25
	25ns	CERAMIC LCC	IMS1624W-25
	25ns	PLASTIC SOJ	IMS1624E-25
	30ns	PLASTIC DIP	IMS1624P-30
	30ns	CERAMIC DIP	IMS1624S-30
	30ns	CERAMIC LCC	IMS1624W-30
	30ns	PLASTIC SOJ	IMS1624E-30
	35ns	PLASTIC DIP	IMS1624P-35
	35ns	CERAMIC DIP	IMS1624S-35
	35ns	CERAMIC LCC	IMS1624W-35
	35ns	PLASTIC SOJ	IMS1624E-35
	45ns	PLASTIC DIP	IMS1624P-45
	45ns	CERAMIC DIP	IMS1624S-45
	45ns	CERAMIC LCC	IMS1624W-45
	45ns	PLASTIC SOJ	IMS1624E-45
	55ns	PLASTIC DIP	IMS1624P-55
	55ns	CERAMIC DIP	IMS1624S-55
	55ns	CERAMIC LCC	IMS1624W-55
	55ns	PLASTIC SOJ	IMS1624E-55

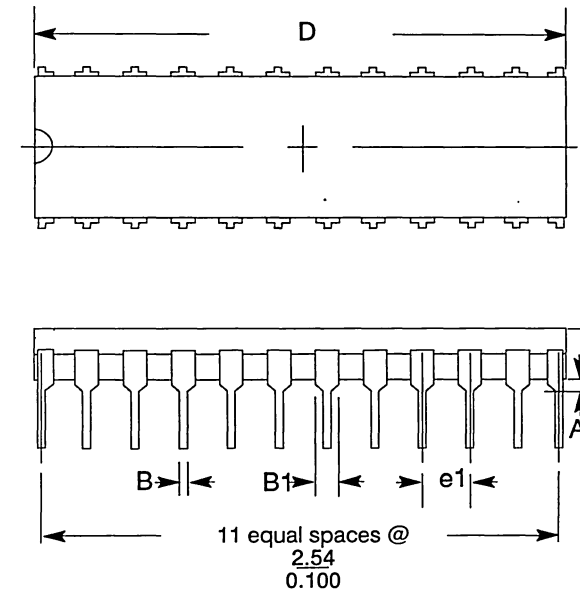
PACKAGING INFORMATION

24 Pin Plastic J Leaded SOJ



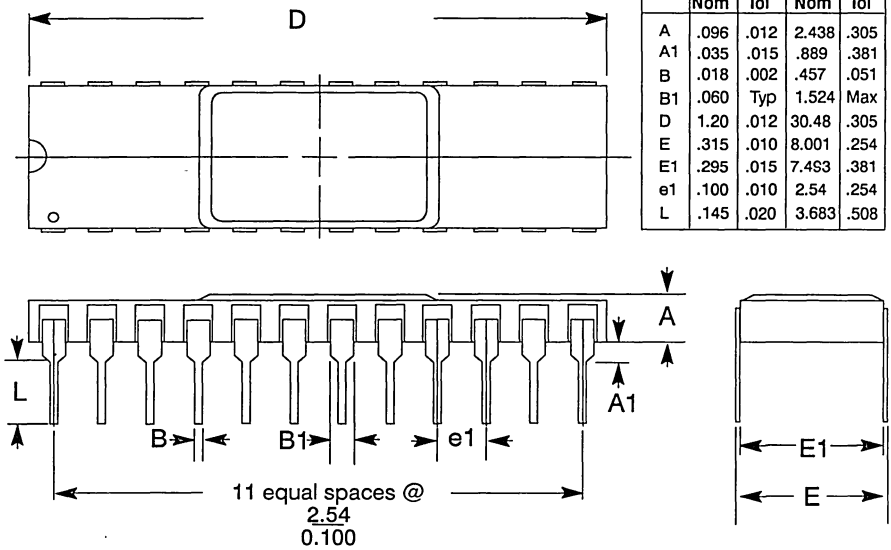
Dim	Inches		mm		Notes
	Min	Max	Min	Max	
A	.120	.140	3.048	3.556	
B1	.014	.019	.356	.483	
C	.010		.254		
D	.602	.612	15.291	15.545	
E	.335	.347	8.509	8.814	
E1	.292	.299	7.417	7.595	
e1	.050	.050	1.270	1.270	
eA	.262	.272	6.655	6.909	
L	.028	.036	.711	.914	

24 Pin Plastic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.165		4.551	
A1	.045	.025	1.143	.635
B	.018	.006	0.457	.152
B1	.060	.003	1.524	.127
D	1.160	.002	29.46	.05
E	.300	.003	7.620	.076
e1	.100	.010	2.54	.254
eA	.325	.010	8.255	.254

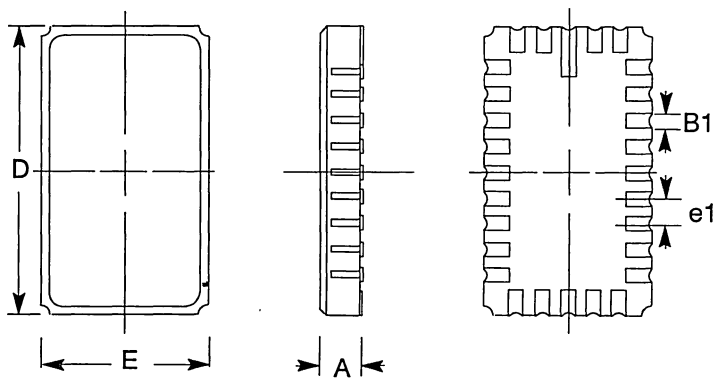
24 Pin Ceramic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.096	.012	2.438	.305
A1	.035	.015	.889	.381
B	.018	.002	.457	.051
B1	.060	Typ	1.524	Max
D	1.20	.012	30.48	.305
E	.315	.010	8.001	.254
E1	.295	.015	7.493	.381
e1	.100	.010	2.54	.254
L	.145	.020	3.683	.508

28 Pin Leadless Chip Carrier

Dim	Inches		mm		Notes
	Nom	Tol	Nom	Tol	
A	.071	.007	1.803	.178	
B1	.025	.003	.635	.076	
D	.550	.010	13.970	.254	
E	.350	.010	8.890	.254	
e1	.050	.002	1.270	.051	



IMS1630L CMOS High Performance 8K x 8 Static RAM

inmos®

FEATURES

- INMOS' high performance CMOS
- Advanced Process - 1.6 Micron Design Rules
- 8K x 8 Bit Organization
- 45, 55, 70, 100 and 120 ns Address Access Times
- 45, 55, 70, 100 and 120 ns Chip Enable Access Times
- Fully TTL Compatible
- Common Data Inputs and Outputs
- Single +5V ± 10% Operation
- Standard 28 Pin 600-mil DIP, 28-Lead SOIC and Skinny DIP Package
- Battery Backup Operation - 2V Data Retention

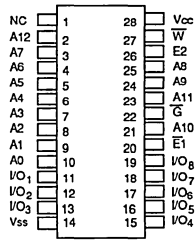
DESCRIPTION

The INMOS IMS1630L is a high performance 8Kx8 CMOS Static RAM.

The IMS1630L features fully static operation requiring no external clocks or timing strobes, with equal access and cycle times. The IMS1630L provides two Chip Enable functions ($\overline{E1}$, E2) to place the device into a reduced power standby mode.

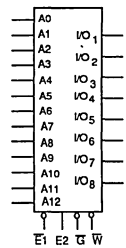
In the low power battery backup data retention mode, the IMS1630L consumes typically 10µA at 2 volts supply.

PIN CONFIGURATION

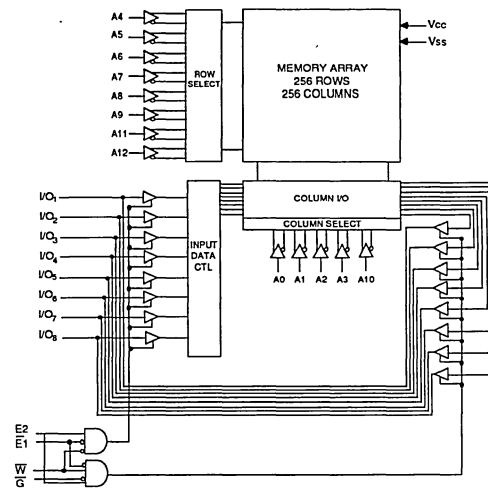


DIP and SOIC

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{12}	ADDRESS INPUTS	Vcc	POWER (+5V)
$\overline{W}$	WRITE ENABLE	Vcc	GROUND
I/O1-I/O8	DATA IN/OUT		
$\overline{E1}$, E2	CHIP ENABLE		
$\overline{G}$	OUTPUT ENABLE		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on I/O.....-1.0 to (Vcc+0.5)
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One output at a time, one second duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+0.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0		70	°C	400 linear ft/min air flow

*V_{IL} min = -3.0 volts for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		90	mA	$t_{AVAV} = t_{AVAV}$ (min)
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		20	mA	$\bar{E}1 \geq V_{IH}$ or $E2 \leq V_{IL}$. All other inputs at $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		8	mA	$\bar{E}1 \geq$ (Vcc - 0.2V) or $E2 \leq 0.2V$. All other inputs at $V_{IN} \leq 0.2$ or $\geq$ (Vcc - 0.2V)
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		10	mA	$\bar{E}1 \geq$ (Vcc - 0.2V) or $E2 \leq 0.2V$. Inputs cycling at $V_{IN} \leq 0.2$ or $\geq$ (Vcc - 0.2V)
I_{ILK}	Input Leakage Current (Any Input)		±1	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		±5	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 8mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the outputs unloaded.

AC TEST CONDITIONS

Input Pulse Levels ..... V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0 MHZ)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

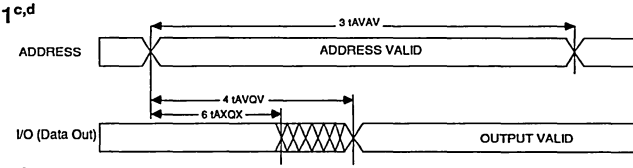
RECOMMENDED AC OPERATING CONDITIONS (0°C ≤ TA ≤ 70°C) (Vcc = 5.0V ±10%)

READ CYCLE[g]

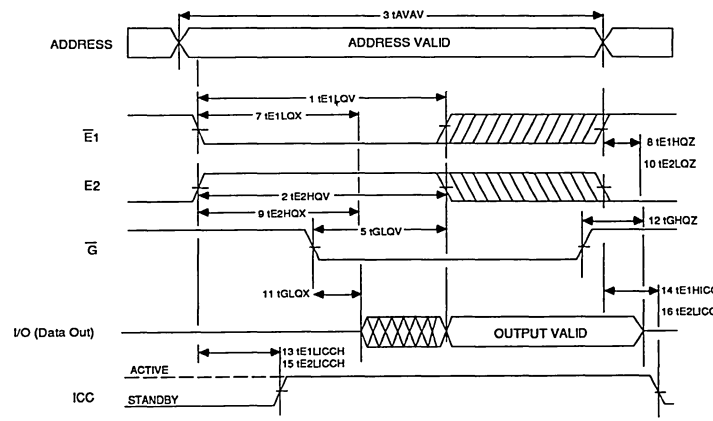
No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1630L-45 MIN	IMS 1630L-45 MAX	IMS 1630L-55 MIN	IMS 1630L-55 MAX	IMS 1630L-70 MIN	IMS 1630L-70 MAX	IMS 1630L-100 MIN	IMS 1630L-100 MAX	IMS 1630L-120 MIN	IMS 1630L-120 MAX	UNITS	NOTES
1	tE1LQV	tACS	Chip Enable Access Time		45		55		70		100		120	ns	
2	tE2HQV	tACS	Chip Enable Access Time		45		55		70		100		120	ns	
3	tAVAV	tRC	Read Cycle Time	45		55		70		100		120		ns	c
4	tAVQV	tAA	Address Access Time		45		55		70		100		120	ns	d
5	tGLQV	tOE	O/P Enable to Data Valid		20		20		35		40		50	ns	
6	tAXQX	tOH	O/P Hold After Addr's Ch'ge	5		5		10		10		10		ns	
7	tE1LQZ	tLZ	Chip Enable to O/P Active	5		5		10		10		10		ns	
8	tE1HQZ	tHZ	Chip Disable to O/P Inactive	0	20	0	25	0	25	0	35	0	40	ns	f, j
9	tE2HQZ	tLZ	Chip Enable to O/P Active	5		5		10		10		10		ns	
10	tE2LQZ	tHZ	Chip Disable to O/P Inactive	0	20	0	25	0	25	0	35	0	40	ns	f, j
11	tGLQX	tLZ	O/P Enable to O/P Active	5		5		5		5		5		ns	
12	tGHQZ	tHZ	O/P Disable to O/P Inactive	0	20	0	25	0	25	0	35	0	40	ns	f, j
13	tE1HICCH	tPU	Chip Enable to Power Up	0		0		0		0		0		ns	j
14	tE1LICCL	tPD	Chip Enable to Power Down		20		20		20		25		30	ns	j
15	tE2HICCH	tPU	Chip Enable to Power Up	0		0		0		0		0		ns	j
16	tE2LICCL	tPD	Chip Disable to Power Down		20		20		20		25		30	ns	j
17		tT	I/P Rise and Fall Times		50		50		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E1}$ low, $\overline{G}$ low and E2 high.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E1}$, E2, $\overline{G}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



RECOMMENDED AC OPERATING CONDITIONS ($0°C \le T_A \le 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g,h]

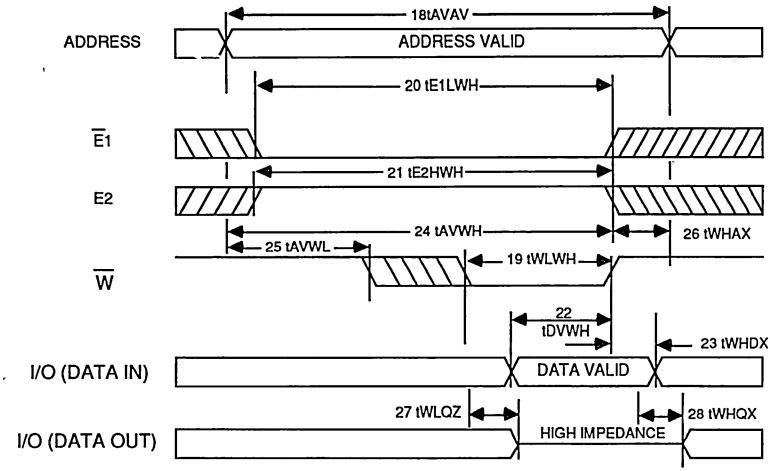
No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1630L-45 MIN	IMS 1630L-45 MAX	IMS 1630L-55 MIN	IMS 1630L-55 MAX	IMS 1630L-70 MIN	IMS 1630L-70 MAX	IMS 1630L-100 MIN	IMS 1630L-100 MAX	IMS 1630L-120 MIN	IMS 1630L-120 MAX	UNITS	NOTES
18	tAVAV	tWC	Write Cycle Time	45		55		70		100		120		ns	
19	tWLWH	tWP	Write Pulse Width	35		40		40		60		70		ns	
20	tE1LWH	tCW	Chip Enable 1 to End of Write	35		40		40		60		70		ns	
21	tE2HWH	tCW	Chip Enable 2 to End of Write	35		40		40		60		70		ns	
22	tDVWH	tDW	Data Setup to End of Write	20		20		20		40		40		ns	
23	tWHDX	tDH	Data Hold after End of Write	0		0		0		0		0		ns	
24	tAVWH	tAW	Address Setup to End of Write	35		40		40		80		85		ns	
25	tAVWL	tAS	Address Setup to Start of Write	0		0		0		0		0		ns	
26	tWHAX	tWR	Address Hold after End of Write	0		0		0		0		0		ns	
27	tWLQZ	tWZ	Write Enable to Output Disable	0	20	0	20	0	20	0	35	0	40	ns	f,j
28	tWHQX	tOW	Output Active After End of Write	5		5		5		5		5		ns	i,j

WRITE CYCLE 2: $\overline{E}1$ OR E2 CONTROLLED[g,h]

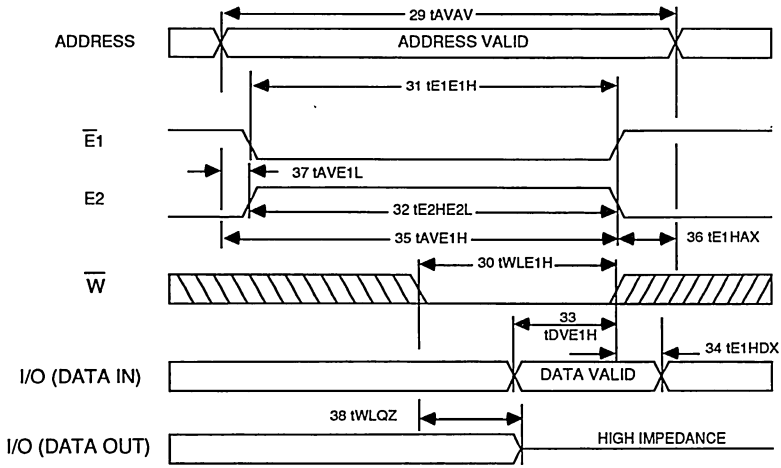
No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1630L-45 MIN	IMS 1630L-45 MAX	IMS 1630L-55 MIN	IMS 1630L-55 MAX	IMS 1630L-70 MIN	IMS 1630L-70 MAX	IMS 1630L-100 MIN	IMS 1630L-100 MAX	IMS 1630L-120 MIN	IMS 1630L-120 MAX	UNITS	NOTES
29	tAVAV	tWC	Write Cycle Time	45		55		70		100		120		ns	
30	tWLE1H	tWP	Write Pulse Width	35		40		40		60		70		ns	
31	tE1LE1H	tCW	Chip Enable 1 to End of Write	35		40		40		60		70		ns	
32	tE2HE2L	tCW	Chip Enable 2 to End of Write	35		40		40		60		70		ns	
33	tDVE1H	tDW	Data Setup to End of Write	20		20		20		40		40		ns	
34	tE1HDX	tDH	Data Hold after End of Write	0		0		0		0		0		ns	
35	tAVE1H	tAW	Address Setup to End of Write	35		40		40		80		85		ns	
36	tE1HAX	tWR	Address Hold after End of Write	0		0		0		0		0		ns	
37	tAVE1L	tAS	Address Setup to Start of Write	0		0		0		0		0		ns	
38	tWLQZ	tWZ	Write Enable to Output Disable	0	20	0	20	0	20	0	30	0	35	ns	f,j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}1$, E2, $\overline{G}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}1$, or $\overline{W}$ must be $\ge V_{IH}$ or E2 must be $\le V_{IL}$ during address transitions.
Note i: If $\overline{W}$ is low when the later of $\overline{E}1$ goes low or E2 goes high, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



WRITE CYCLE 2



DEVICE OPERATION

The IMS1630L has four control inputs, Chip Enable1 ($\overline{E1}$), Chip Enable 2 (E2), Write Enable ($\overline{W}$) and Output Enable ($\overline{G}$). There are also13 address inputs (A0 -A12) and eight Data I/O lines (I/O 1 to I/O 8). The Enable inputs control device selection as well as active and standby modes. The $\overline{W}$ input controls the mode of operation (Read or Write). The $\overline{G}$ input controls only the state of the eight output drivers.

With both $\overline{E1}$ low and E2 high, the device is selected and the 13 address inputs are decoded to select one 8-bit word out of 8K words. Read and Write operations on the memory cells are controlled by the $\overline{W}$ input. With either $\overline{E1}$ high or E2 low, the device is deselected, the outputs disabled and the power consumption is reduced to less than one-fourth of the active mode power. $\overline{G}$ serves only to control the operation of the output drivers. When $\overline{G}$ is high, the output drivers are in a high impedance state, independant of the $\overline{E1}$, E2 and $\overline{W}$ inputs.

READ CYCLE

A read cycle is defined as $W \geq V_{IH}$ min with $\overline{E1} \leq V_{IL}$ max, $E2 \geq V_{IH}$ min and $\overline{G} \leq V_{IL}$ max. Read access time is measured from the later of either $\overline{E1}$ going low, E2 going high, valid address, or $\overline{G}$ going low.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E1}$ is low and E2 is high (with $\overline{G}$ low). The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and the output remains valid for a minimum of tAXQX. As long as $\overline{E1}$ remains low and E2 is high, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by the later of $\overline{E1}$ going low, E2 going high or $\overline{G}$ going low. As long as address is stable when the later of $\overline{E1}$ goes low or E2 goes high, valid data is at the output at the later of tE1LQV, tE2HQV or tGLQV. If address is not valid when the later of $\overline{E1}$ goes low or E2 goes high, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

The $\overline{G}$ signal controls the output buffer. $\overline{G}$ is required to be low (along with $\overline{E1}$ low and E2 high) in order for I/O1 - I/O 8 to be active.

WRITE CYCLE

The write cycle of the IMS1630L is initiated by the later of $\overline{E1}$ or $\overline{W}$ to transition from a high to a low or E2 transitioning from low to high. The $\overline{G}$ control will remove bus contention if held high throughout the duration of the write cycle. If $\overline{G}$ is low during a $\overline{W}$ controlled write cycle (Write Cycle 1), the output buffer will be turned on by the later of tE1LQX after the falling edge of $\overline{E1}$ or tE2HQX after the rising edge of E2. The output buffer is then turned off within tWLQZ of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with common input/output connections. Therefore the recommended mode of operation is to keep $\overline{G}$ high during the write cycle. During a write cycle, data on the inputs is written into the selected cells and the outputs are floating.

For any write cycle, tAVWL, tAVE1L, or tAVE2H must be met, depending on whether $\overline{E1}$, E2 or $\overline{W}$ is the last to transition. After either $\overline{W}$ or $\overline{E1}$ goes high or E2 goes low to terminate the write cycle, addresses may change. If address set-up and hold times are not met, contents of other cells may be altered in unpredictable ways. The fidelity of the $\overline{W}$ control signal is very important. Excessive ringing on high to low transitions may cause signals to rise above V_{IL} max, violating the minimum $\overline{W}$ pulse width specification - tWLWH.

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. When $\overline{W}$ goes high while $\overline{E1}$ is low and E2 is high, the outputs remain in a high impedance state (unless $\overline{G}$ is low). If $\overline{G}$ is low when $\overline{W}$ goes high at the end of a write cycle the data read from the memory will be the same as the data just written into the memory. Thus, no data bus contention will occur.

WRITE CYCLE 2 waveform shows a write cycle terminated by the later $\overline{E1}$ going high or E2 going low. Data set-up and hold times are referenced to the later of the rising edge of $\overline{E1}$ or the falling edge of E2. With either $\overline{E1}$ high or E2 low the outputs remain in the high impedance state.

When using WRITE CYCLE 1 proper management of the $\overline{G}$ control signal will avoid bus contention. If $\overline{G}$ is low when $\overline{W}$ goes high (with $\overline{E1}$ low and E2 high) the output buffers will be active tWHQX after the rising edge of $\overline{W}$. Data out will be the same as the data just written, unless the address changes. If input data from the previous cycle is still valid after the address changes, contention may result. Contention may also result if the device is selected ($\overline{E1}$ low, E2 high, $\overline{G}$ low) before $\overline{W}$ goes low and input data is valid early in the cycle. The recommended mode of operation is to keep $\overline{G}$ high except when reading data from the device, thus avoiding bus contention.

TTL VS. CMOS INPUTLEVELS

The INMOS 1630L is fully compatible with TTL input levels. The input circuitry of the IMS1630L is designed for maximum speed and also for conversion of TTL level signals to the CMOS levels required for internal operation. The IMS1630L consumes less power when CMOS levels are used instead of TTL levels. The lower CMOS Icc specifications (Icc3 and Icc4) may be achieved by using CMOS levels. The power consumption will be lower at typical TTL levels than at the worst case levels.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1630L. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Current transients associated with the operation of any high speed device have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 µF and be placed between each row of devices in the array. A larger tantalum capacitor of a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit area. This will provide a solid ground reference for the drivers and prevent loss of operating margin due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically. A resistor of predetermined value may not properly terminate the transmission line.

Proper power distribution techniques, including adequate use of decoupling capacitors, and proper termination of TTL drive outputs are some of the most important yet basic guidelines that need to be followed when designing and building a memory board. The guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment free of noise spikes, undershoot, and excessive ringing. It is wise to verify signal fidelity by observation utilising a wideband oscilloscope and probe.

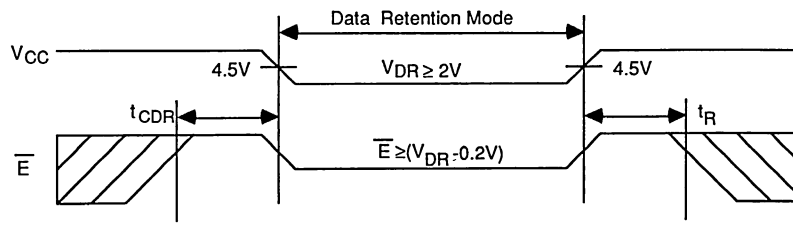
DATA RETENTION (L version only) ($0°C \le T_A \le 70°C$)

SYMBOL	PARAMETER	MIN	TYP*	MAX	UNITS	NOTES
V_{DR}	Data Retention Voltage	2.0			volts	$V_{IN} \le 0.2V$ or $\ge (Vcc - 0.2V)$ $\overline{E} \ge (Vcc - 0.2V)$
I_{CCDR1}	Data Retention Current		10	100	µA	$V_{CC} = 3.0$ volts
I_{CCDR2}	Data Retention Current		5	70	µA	$V_{CC} = 2.0$ volts
t_{EHVCCL}	Deselect Time (t_{CDR})	0			ns	j,k
t_{VCCHEL}	Recovery Time (t_R)	t_{RC}			ns	j,k (t_{RC} = Read Cycle Time)

* Typical data retention parameters at 25 °C

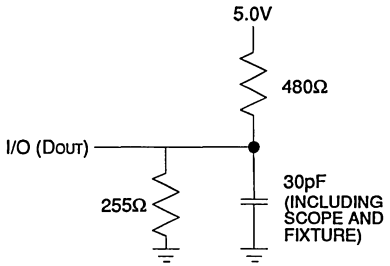
Note j: Parameter guaranteed but not tested

Note k: Supply recovery rate should not exceed 100mV per10µs from V_{DR} to V_{CC} min



Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

FIGURE 1. OUTPUT LOAD



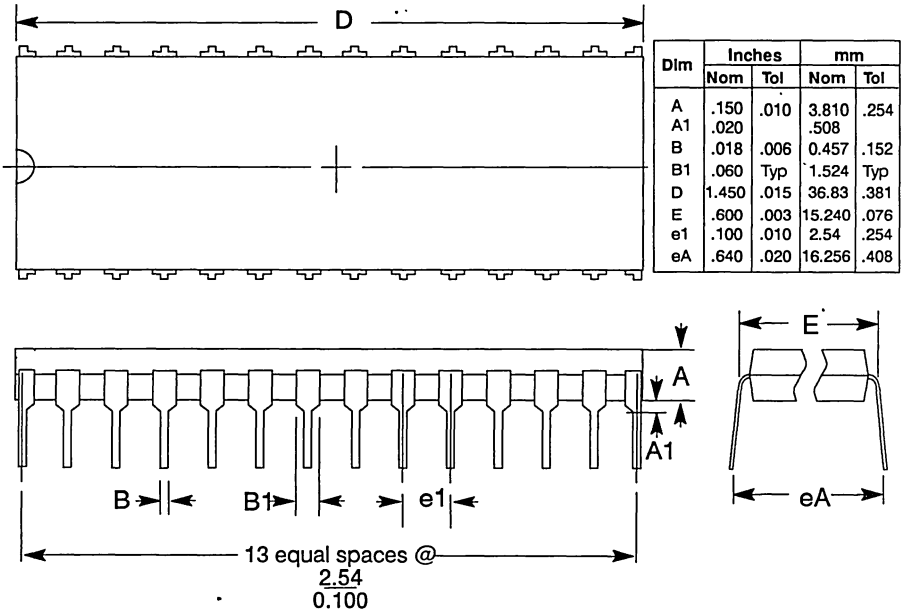
$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$	I/O	MODE
H	X	X	X	HI-Z	Standby (Isb)
X	L	X	X	HI-Z	Standby (Isb)
L	H	H	H	HI-Z	Output disable
L	H	H	L	DOUT	Read
L	H	L	X	DIN	Write

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1630	45ns	PDIP	IMS1630LP45
	45ns	SOIC	IMS1630LH45
	45ns	Skinny DIP	IMS1630LP45Z
	55ns	PDIP	IMS1630LP55
	55ns	SOIC	IMS1630LH55
	55ns	Skinny DIP	IMS1630LP55Z
	70ns	PDIP	IMS1630LP70
	70ns	SOIC	IMS1630LH70
	70ns	Skinny DIP	IMS1630LP70Z
	100ns	PDIP	IMS1630LP10
	100ns	SOIC	IMS1630LH10
	100ns	Skinny DIP	IMS1630LP10Z
	120ns	PDIP	IMS1630LP12
	120ns	SOIC	IMS1630LH12
	120ns	Skinny DIP	IMS1630LP12Z

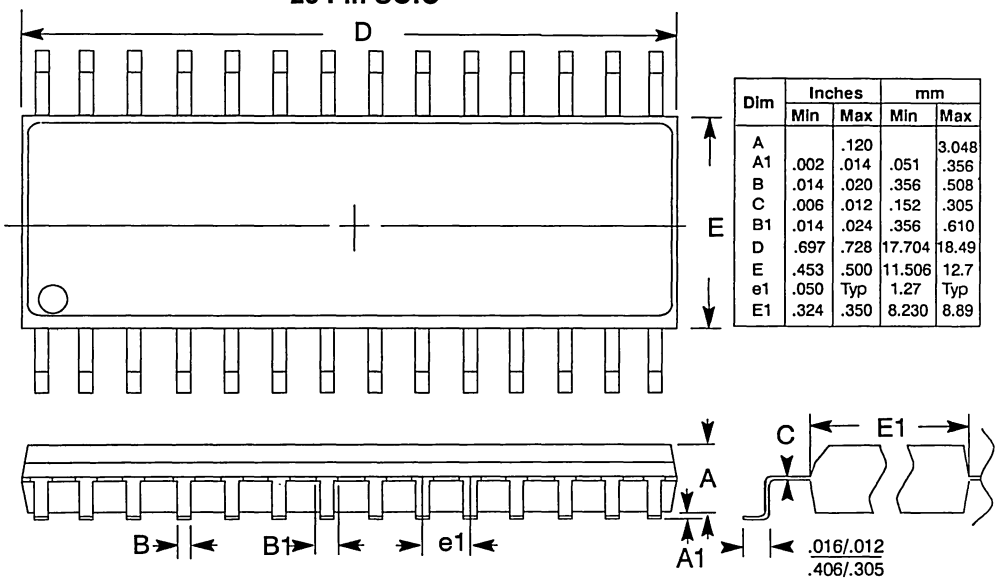
PACKAGING INFORMATION

28 Pin Plastic Dual-In-Line



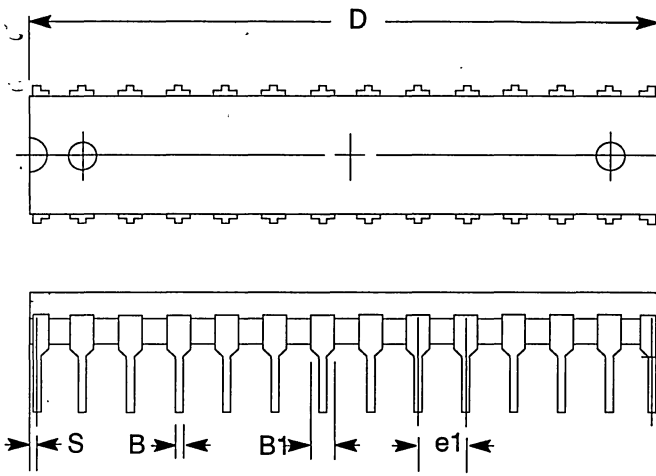
Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.150	.010	3.810	.254
A1	.020		.508	
B	.018	.006	0.457	.152
B1	.060	Typ	1.524	Typ
D	1.450	.015	36.83	.381
E	.600	.003	15.240	.076
e1	.100	.010	2.54	.254
eA	.640	.020	16.256	.408

28 Pin SOIC



Dim	Inches		mm	
	Min	Max	Min	Max
A		.120		3.048
A1	.002	.014	.051	.356
B	.014	.020	.356	.508
C	.006	.012	.152	.305
B1	.014	.024	.356	.610
D	.697	.728	17.704	18.49
E	.453	.500	11.506	12.7
e1	.050	Typ	1.27	Typ
E1	.324	.350	8.230	8.89

28 Pin Skinny DIP



Dim	Inches		mm	
	Min	Max	Min	Max
A	.130		3.302	
A1	.040		1.016	
B	.016	.020	0.406	.457
B1	.045	.055	1.143	1.397
D	1.345	1.355	34.163	3.442
E	.300	.325	7.62	8.255
e1	.100	Typ	2.54	Typ
S	.020	.030	.508	.762

IMS16X5 series High Performance Memory Products

Advance Information

IMS 1605: 64K x 1
IMS 1625: 16K x 4
IMS 1629: 16K x 4 with Output Enable
IMS 1626/7: 16K x 4 with Separate I/Os
IMS 1635: 8K x 8
IMS 1695: 8K x 9

FEATURES

- INMOS' Very High Speed Double Metal CMOS
- Advanced Process-1.2 Micron Design Rules
- 64K Bit Devices
- 15, 20 and 25 ns Address Access Times
- 15, 20 and 25 ns Chip Enable Access Times
- Fully TTL Compatible
- Single +5V ± 10% Operation
- Battery Backup Operation - 2V Data Retention, 10µA typical at 25°C
- Packages include: DIP, LCC and SOJ
- Military Versions Available

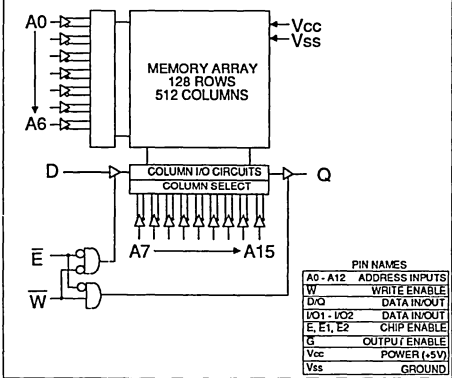
DESCRIPTION

The INMOS IMS16X5 series are high speed advanced 64K double layer metal CMOS Static RAMs.

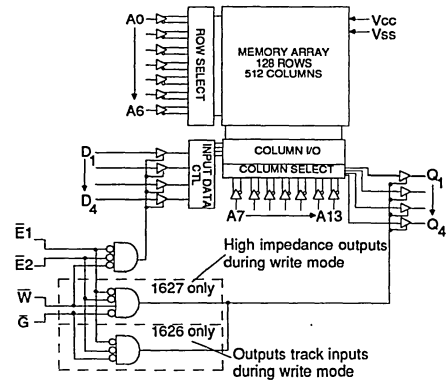
The range features fully static operation requiring no external clocks or timing strobes, with equal access and cycle times. A chip enable function (E) that can be used to place the device into a low-power standby mode is available on all organisations. The 8K x 8 organisations provide an additional Chip Enable for reduced low-power standby mode. Output Enable ($\overline{G}$) is an enhancement on organisations requiring fast access to data and enhanced bus contention control.

Military versions of the 16X5 are also available.

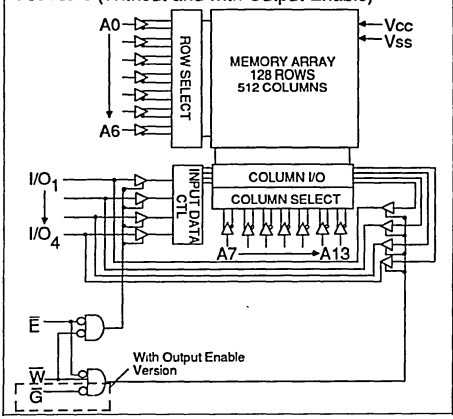
64K x 1



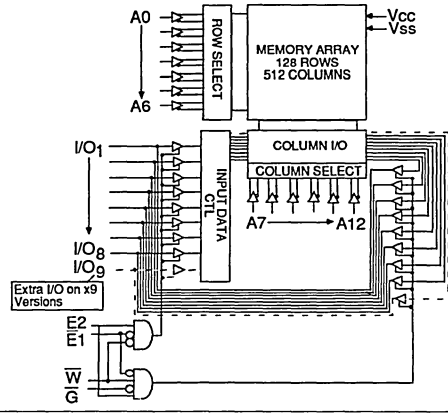
16K x 4 (Separate Inputs and Outputs)



16K x 4 (Without and with Output Enable)



8K x 8 / 8K x 9



2.1 Electrical specifications

2.1.1 Absolute maximum ratings[1]

Symbol	Parameter	Min	Max	Unit
V_{SS}	Value on relative pin	−2.0	7.0	V
	Voltage on I/O	−1.0	V_{CC} +0.5	V
T_A	Temperature under bias	−55	125	°C
	Storage temperature	−65	150	°C
	Power dissipation		1	W
	DC output current		25	mA

(One output at a time, one second duration).

2.1.2 DC operating conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic '1' Voltage	2.0		V_{CC} + 0.5	V	All inputs
V_{IL}	Input Logic '0' Voltage	−0.5*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0		70	°C	400 linear ft/min air flow

*V_{IL}min. = −3.0V for pulse width <10ns, note b

2.1.3 DC electrical characteristics ($0°C \leq T_A \leq 70°C$)($V_{CC} = 5.0V \pm 10\%$)[a]

For suffixes refer to section 2.1.7.

Symbol	Parameter	Min	Max	Units	Notes
I_{CC1}	Average V_{CC} Power Supply Current		100	mA	$t_{AVAV} = t_{AVAV}$(min).
I_{CC2}	V_{CC} Power Supply Current (Standby, Stable TTL Input Levels)		40	mA	$\overline{E}_1 \geq V_{IH}$ or $E_2 \leq V_{IL}$. All other inputs at $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$.
I_{CC3}	V_{CC} Power Supply Current (Standby, Stable CMOS Input Levels)		2	mA	$\overline{E}_1 \geq (V_{CC} - 0.2V)$ or $E_2 \leq 0.2V$. All other inputs at $V_{IN} \leq 0.2$ or $\geq (V_{CC} - 0.2V$.
I_{CC4}	V_{CC} Power Supply Current (Standby, Cycling CMOS Input Levels)		25	mA	$\overline{E}_1 \geq (V_{CC} - 0.2V)$ or $E_2 \leq 0.2V$. Inputs cycling at $V_{IN} \leq 0.2$ or $\geq (V_{CC} - 0.2V$.
I_{ILK}	Input Leakage Current (any input)		±1	µA	V_{CC} = max. $V_{IN} = V_{SS}$ to V_{CC}.
I_{OLK}	Off State Output Leakage Current		±5	µA	V_{CC} = max. $V_{IN} = V_{SS}$ to V_{CC}.
V_{OH}	Output Logic '1' Voltage	2.4		V	$I_{OH} = -4mA$.
V_{OL}	Output Logic '0' Voltage		0.4	V	$I_{OL} = 8mA$.

[1]Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2.1.4 AC test condition

Input pulse levels	V_{SS} to 3.0V
Input rise and fall times	5ns
Input and output timing reference levels	1.5V
Output load	see figure 2.1

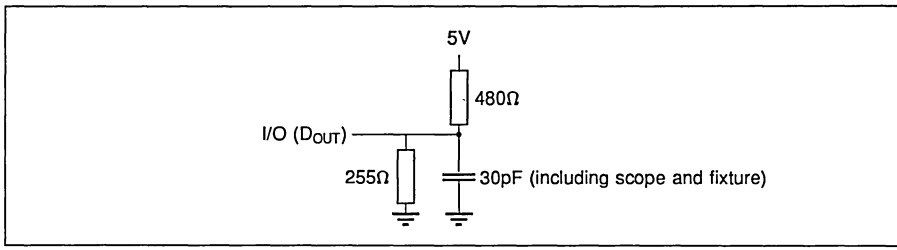


Figure 2.1 Output load

2.1.5 Capacitance[b]

Symbol	Parameter	Min	Max	Units	Conditions
C_{IN}	Input capacitance		5	pF	ΔV = 0 to 3.0V
C_{OUT}	Output capacitance		7	pF	ΔV = 0 to 3.0V

2.1.6 Recommended AC operating conditions ($0°C \leq T_A \leq 70°C$)($V_{CC} = 5.0V \pm 10\%$)

Read cycle[g]

	Symbol			16X5-15		16X5-20		16X5-25			
No.	Stand.	Alt.	Parameter	min	max	min	max	min	max	Units	Notes*
1	t_{E1LQV}	t_{ACS}	Chip Enable Access Time		15		20		25	ns	
2	t_{E2HQV}	t_{ACS}	Chip Enable Access Time		15		20		25	ns	
3	t_{AVAV}	t_{RC}	Read Cycle Time	15		20		25		ns	c
4	t_{AVQV}	t_{AA}	Address Access Time		15		20		25	ns	d
5	t_{GLQV}	t_{OE}	O/P Enable to Data Valid		8		10		10	ns	
6	t_{AXQX}	t_{OH}	O/P Hold After Add's Ch'ge	3		3		3		ns	
7	t_{E1LQX}[1]	t_{LZ}	Chip Enable to O/P Active	8		8		10		ns	
8	t_{E1HQZ}	t_{HZ}	Chip Disable to O/P inactive		8		10		10	ns	f,j
9	t_{E2HQZ}	t_{LZ}	Chip Enable to O/P Active	8		10		10		ns	
10	t_{E2LQZ}	t_{HZ}	Chip Disable to O/P Inactive		8		10		10	ns	f,j
11	t_{GLQX}	t_{LZ}	O/P Enable to O/P Active	3		3		3		ns	
12	t_{GHQZ}	t_{HZ}	O/P Disable to O/P Inactive		8		10		10	ns	f,j
13	$t_{E1LICCH}$	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
14	$t_{E1LICCL}$	t_{PD}	Chip Disable to Power Down		15		20		25	ns	j
15	$t_{E2HICCH}$	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
16	$t_{E2LICCL}$	t_{PD}	Chip Disable to Power down		15		20		25	ns	j
17		t_T	I/P Rise and Fall Times		50		50		50	ns	e,j

* Refer to section 2.1.7.
[1] T_{ELQX} is always greater than T_{EHQZ}

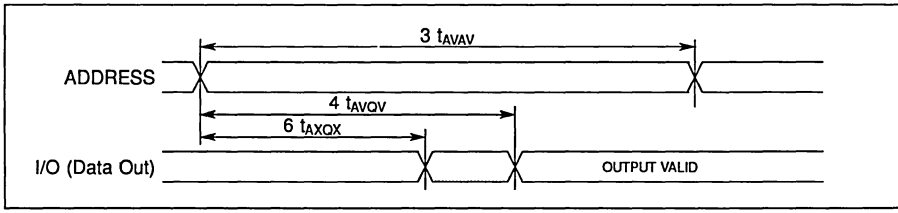


Figure 2.2 Read cycle 1[c,d]

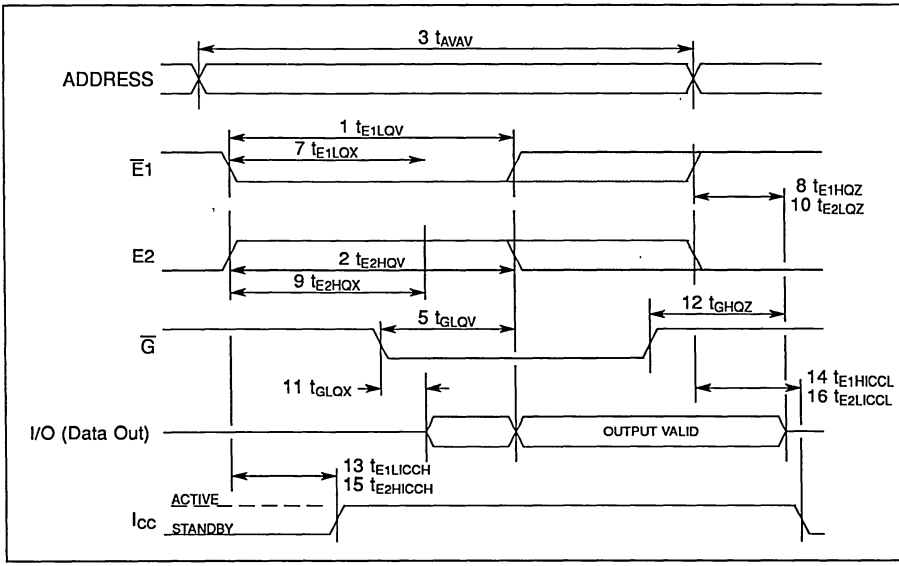


Figure 2.3 Read cycle 2[c]

Write cycle 1: $\overline{W}$ controlled[g,h]

No.	Symbol Stand.	Symbol Alt.	Parameter	16X5-15 min	16X5-15 max	16X5-20 min	16X5-20 max	16X5-25 min	16X5-25 max	Units	Notes*
18	t_{AVAV}	t_{WC}	Write Cycle Time	15		20		25		ns	
19	t_{WLWH}	t_{WP}	Write Pulse Width	12		15		20		ns	
20	t_{E1LWH}	t_{CW}	Chip Enable 1 to End of Write	12		15		20		ns	
21	t_{E2HWH}	t_{CW}	Chip Enable 2 to End of Write	12		15		20		ns	
22	t_{DVWH}	t_{DW}	Data Setup to End of Write	10		12		15		ns	
23	t_{WHDX}	t_{DH}	Data Hold after End of Write	0		0		0		ns	
24	t_{AVWH}	t_{AW}	Address Setup to End of Write	15		15		20		ns	
25	t_{AVWL}	t_{AS}	Address Setup to Start of Write	0		0		0		ns	
26	t_{WHAX}	t_{WR}	Add's Hold After End of Write	0		0		0		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	8	0	10	0	10	ns	f,j
28	t_{WHQX}	t_{OW}	Output Active after End of Write	0		0		0		ns	i,j

Write cycle 2: $\overline{E}1$ or E2 controlled[g,h]

No.	Symbol Stand.	Symbol Alt.	Parameter	16X5-15 min	16X5-15 max	16X5-20 min	16X5-20 max	16X5-25 min	16X5-25 max	Units	Notes*
29	t_{AVAV}	t_{WC}	Write Cycle Time	15		20		25		ns	
30	t_{WLWE1H}	t_{WP}	Write Pulse Width	12		15		20		ns	
31	t_{E1LE1H}	t_{CW}	Chip Enable 1 to End of Write	12		15		20		ns	
32	t_{E2HE2L}	t_{CW}	Chip Enable 2 to End of Write	12		15		20		ns	
33	t_{DVE1H}	t_{DW}	Data Setup to End of Write	10		12		15		ns	
34	t_{E1HDX}	t_{DH}	Data Hold after End of Write	0		0		0		ns	
35	t_{AVE1H}	t_{AW}	Address Setup to End of Write	15		15		20		ns	
36	t_{E1HAX}	t_{WR}	Address Hold after End of Write	0		0		0		ns	
37	t_{AVE1L}	t_{AS}	Address Setup to Start of Write	0		0		0		ns	
38	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	8	0	10	0	10	ns	f,j

* Refer to section 2.1.7.

2.1.7 Notes

Note a: I_{CC} is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.
Note b: This parameter is sampled and not 100% tested.
Note c: For Read Cycle 1 and 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continually selected, $\overline{E}1$ low $\overline{G}$ low and E2 high.
Note e: Measured between V_{IL} max. and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}1$, E2, $\overline{G}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}1$ or $\overline{W}$ must be $\geq V_{IH}$ or E2 must be $\leq V_{IL}$ during address transitions.
Note I: If $\overline{W}$ is low when the later of $\overline{E}1$ goes low or E2 goes high, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.
Note k: Supply recovery rate should not exceed 100mV per 10μs from V_{DR} to V_{CC} min.

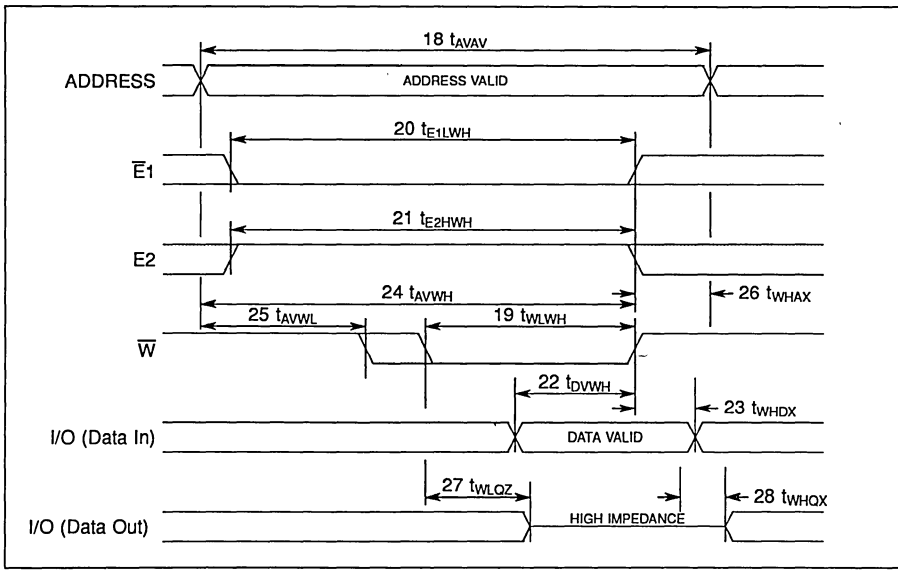


Figure 2.4 WRITE CYCLE 1

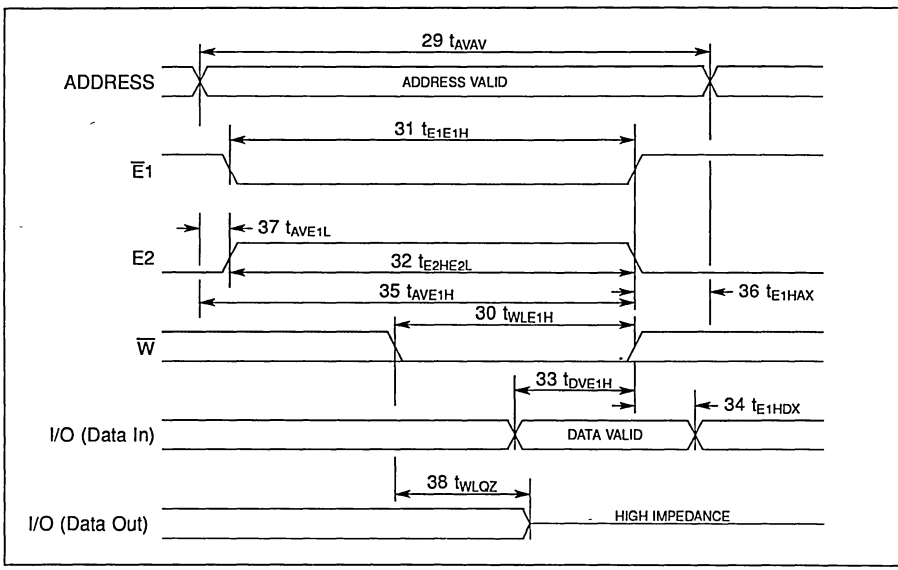


Figure 2.5 WRITE CYCLE 2

2.1.8 Power distribution

Recommended power distribution schemes combine proper power trace layout and placement of decoupling capacitors to maintain the wide operating margins of the IMS 16X5 series. The impedance in the decoupling path from the V_{CC} power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance/reactance of the decoupling capacitor.

Current transients associated with the operation of high speed memories have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as near the memory as possible, with the shortest lead lengths practical. The high frequency decoupling capacitor should have a minimum value of 0.1μF and be placed between the rows of memory devices in the array. A larger tantalum capacitor for low frquency current transients should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the drivers and prevent loss of operating margin due to differential ground noise.

2.1.9 Termination

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the line, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended series termination technique uses no DC current and a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The termination resistor should be placed as close to the driver package as possible. The line should be kept short by placing the driver–termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimise reflections, but generally a series resistor in the 10 to 33Ω range will be required. Because the characteristic impedance of each layout will be different, it is necessary to select the proper value of this resistor by trial and error. A resistor of predetermined value may not properly terminate the transmission line.

Proper power distribution techniques, including adequate use of decoupling capacitors, and proper termination of TTL drive outputs are some of the most important yet basic guidelines that need to be followed when designing and building a memory board. The guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment free of noise spikes, undershoot, and excessive ringing. It is wise to verify signal fidelity by observation utilizing a wideband oscilloscope and probe.

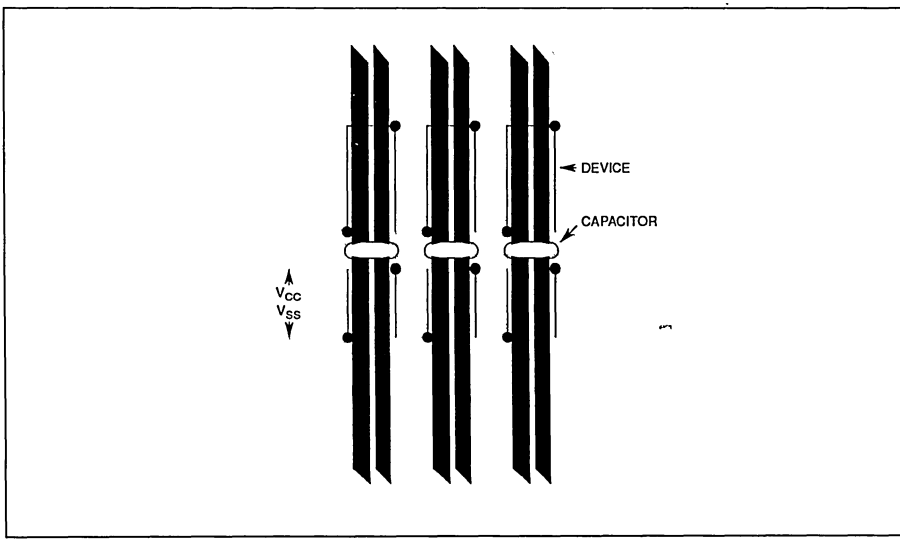


Figure 2.6 Grid showing decoupling capacitors

2.1.10 Data retention (low power versions only)($0°C \leq T_A \leq 70°C$)

Symbol	Parameter	Min	Typ(25°C)	Max	Units	Notes*
V_{DR}	Data Retention Voltage	2.0			V	$V_{IN} \leq 0.2V$ or $\geq (V_{CC}-0.2V)$ $\overline{E} \geq (V_{CC} - 0.2V)$
I_{CCDR1}	Data Retention Current		15	100	μA	$V_{CC} = 3.0V$
I_{CCDR2}	Data Retention Current		10	70	μA	$V_{CC} = 2.0V$
t_{EHVCCL}	Deselect Time (t_{CDR})	0			ns	j,k
t_{VCCHEL}	Recovery Time (t_R)	t_{RC}			ns	j,k (t_{RC} = Read Cycle Time)

* Refer to section 2.1.7.

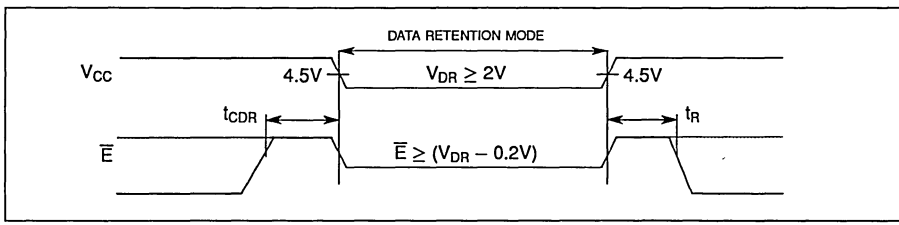


Figure 2.7 Data retention

2.2 Packaging information

2.2.1 Pin-outs and packages

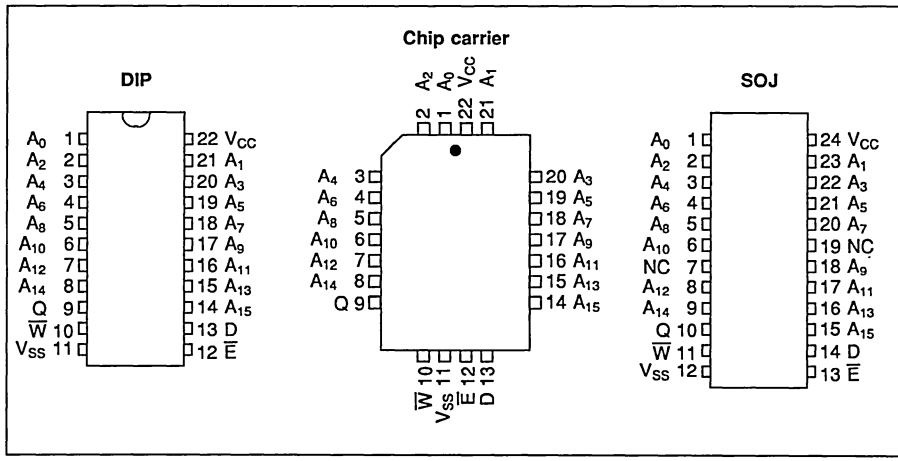


Figure 2.8 64K x 1 pin configuration

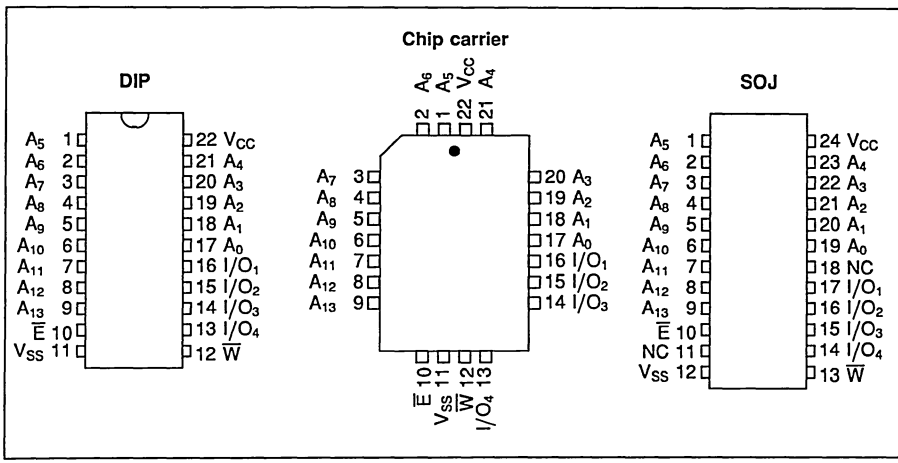


Figure 2.9 16K x 4 pin configuration

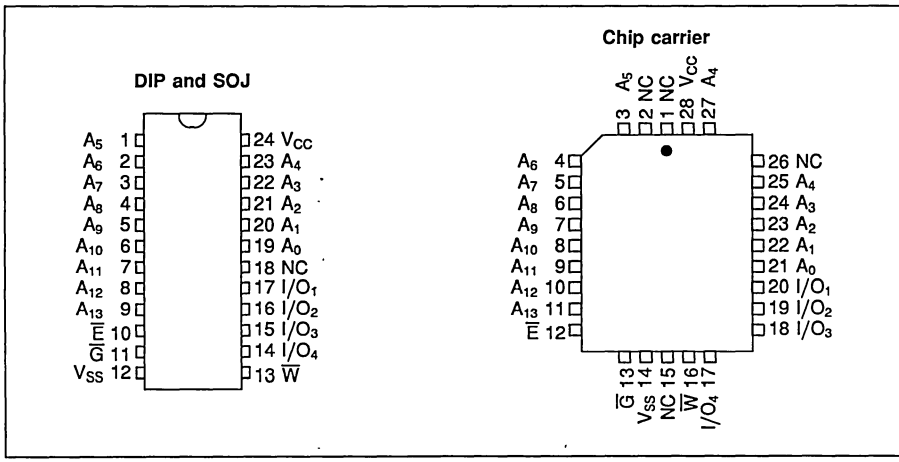


Figure 2.10 16K x 4 (with output enable) pin configuration

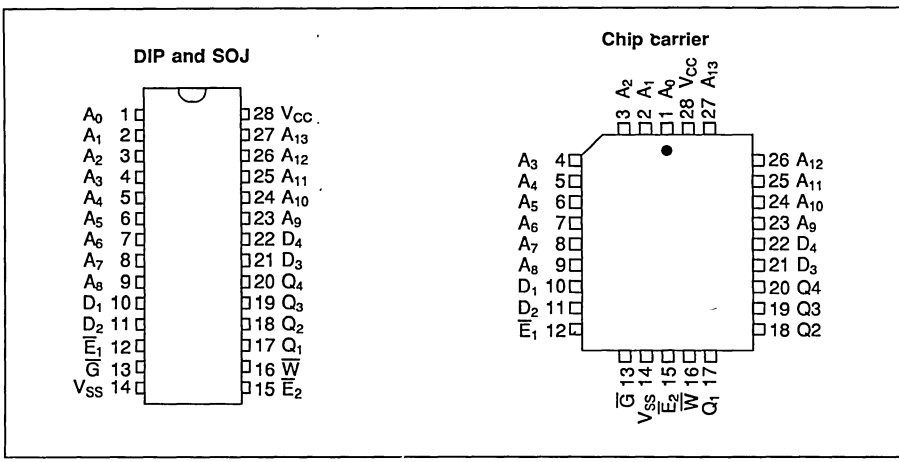


Figure 2.11 16K x 4 (with separate Inputs and Outputs) pin configuration

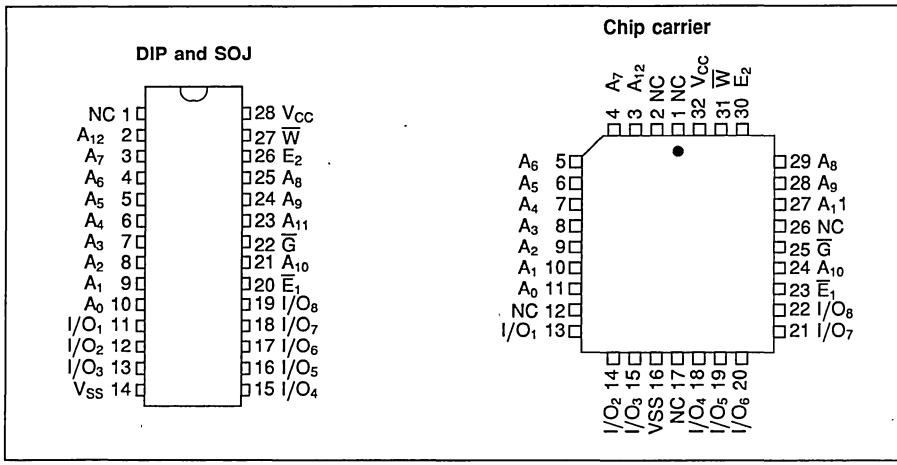


Figure 2.12 8K x 8 pin configuration

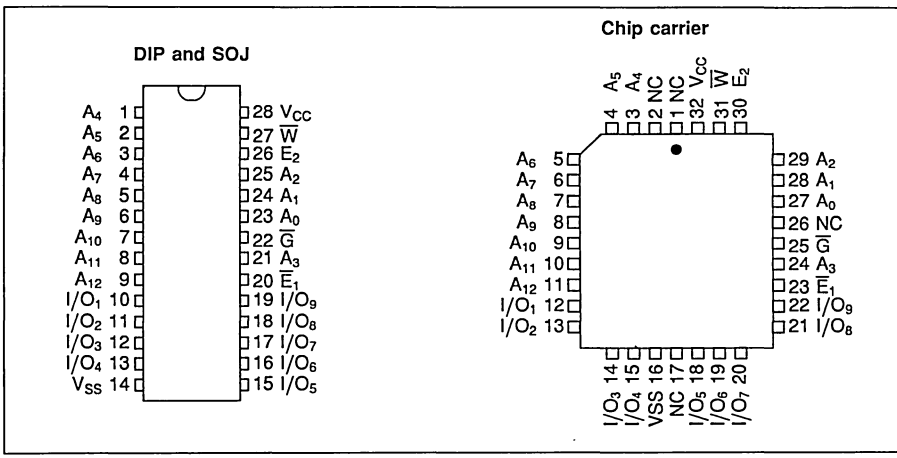


Figure 2.13 8K x 9 pin configuration

2.3 Ordering information

Device	Speed	Part Number
IMS1605	15ns	IMS1605*x*–15
	20ns	IMS1605*x*–20
	25ns	IMS1605*x*–25
IMS1625	15ns	IMS1625*x*–15
	20ns	IMS1625*x*–20
	25ns	IMS1625*x*–25
IMS1629	15ns	IMS1629*x*–15
	20ns	IMS1629*x*–20
	25ns	IMS1629*x*–25
IMS1626	15ns	IMS1626*x*–15
	20ns	IMS1626*x*–20
	25ns	IMS1626*x*–25
IMS1627	15ns	IMS1627*x*–15
	20ns	IMS1627*x*–20
	25ns	IMS1627*x*–25
IMS1635	15ns	IMS1635*x*–15
	20ns	IMS1635*x*–20
	25ns	IMS1635*x*–25
IMS1695	15ns	IMS1695*x*–15
	20ns	IMS1695*x*–20
	25ns	IMS1695*x*–25

Where *x* refers to packages P, S, E, or W. See also Appendix D.

IMS1800
CMOS
High Performance
256K x 1 Static RAM

inmos®

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.2 Micron Design Rules
- 256K x 1 Bit Organization
- 25, 30, 35 and 45 ns Address Access Times
- 25, 30, 35 and 45 ns Chip Enable Access Times
- Fully TTL Compatible
- Separate Data Input and Outputs
- Three-state Output
- 24 Pin 300-mil DIP, SOJ and 28 Pin LCC
- Single +5V ± 10% Operation
- Power Down Function

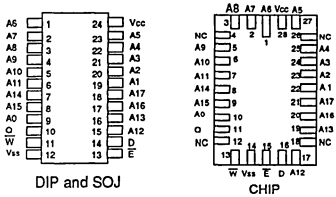
DESCRIPTION

The INMOS IMS1800 is a high performance 256Kx1 CMOS Static RAM. The IMS1800 provides maximum density and speed enhancements with the additional benefits of lower power and superior reliability.

The IMS1800 features fully static operation requiring no external clocks or timing strobes, with equal access and cycle times. Additionally, the IMS1800 provides a Chip Enable function ($\overline{E}$) that can be used to place the device into a low power standby mode.

The IMS1800E is an extended temperature version pending military qualification of the IMS1800M.

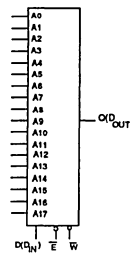
PIN CONFIGURATION



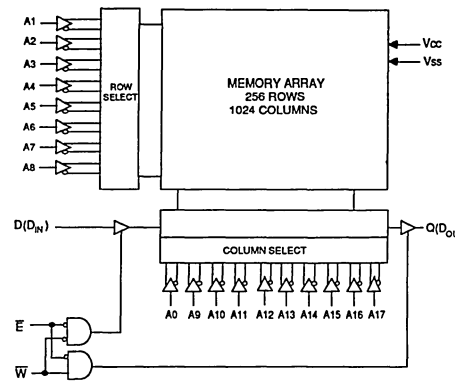
DIP and SOJ

CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{17}	ADDRESS INPUTS	Q	DATA OUT
$\overline{W}$	WRITE ENABLE	Vcc	POWER (+5V)
$\overline{E}$	CHIP ENABLE	Vss	GROUND
D	DATA INPUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on I/O.....-1.0 to 6.0V
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One output at a time, one second duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		+0.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-0.5 *		0.8	V	All inputs
T_A	Ambient Operating Temperature	0		70	°C	

*V_{IL} min = -3.0V for pulse width <10ns, note b

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		120	mA	tAVAV = tAVAV (min)
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		30	mA	E ≥ V_{IH}. All other inputs at $V_{IN} \leq V_{IL}$ or ≥ V_{IH}
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		10	mA	E ≥ (Vcc - 0.2V). All other inputs at $V_{IN} \leq$ 0.2 or ≥ (Vcc - 0.2V)
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		15	mA	E ≥ (Vcc - 0.2V). Inputs cycling at $V_{IN} \leq$ 0.2 or ≥ (Vcc - 0.2V)
I_{ILK}	Input Leakage Current (Any Input)		±1	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		±10	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 8mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels .....Vss to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0 MHZ)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	4	pF	ΔV = 0 to 3V

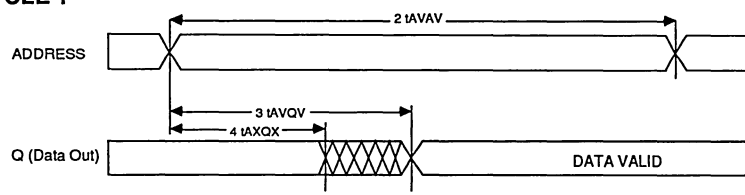
Note b: This parameter is sampled and not 100% tested.

RECOMMENDED AC OPERATING CONDITIONS (0°C ≤ TA ≤ 70°C) (Vcc = 5.0V ±10%)
READ CYCLE[g]

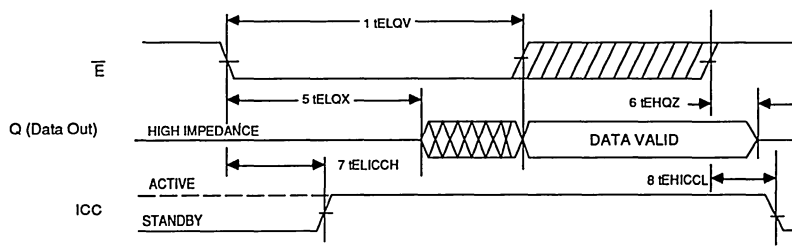
No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1800-25 MIN	IMS 1800-25 MAX	IMS 1800-30 MIN	IMS 1800-30 MAX	IMS 1800-35 MIN	IMS 1800-35 MAX	IMS 1800-45 MIN	IMS 1800-45 MAX	UNITS	NOTES
1	t ELQV	t ACS	Chip Enable Access Time		25		30		35		45	ns	
2	t AVAV	t RC	Read Cycle Time	25		30		35		45		ns	c
3	t AVQV	t AA	Address Access Time		25		30		35		45	ns	d
4	t AXQX	t OH	O/P Hold After Addr's Ch'ge	3		3		3		3		ns	
5	t ELQX	t LZ	Chip Enable to O/P Active	3		3		3		3		ns	
6	t EHQZ	t HZ	Chip Disable to O/P Inactive	0	20	0	20	0	20	0	20	ns	f,j
7	t ELICCH	t PU	Chip Enable to Power Up	0		0		0		0		ns	j
8	t ELICCL	t PD	Chip Enable to Power Down		30		30		30		30	ns	j
		t T	Input Rise and Fall Times		50		50		50		50	ns	e,j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



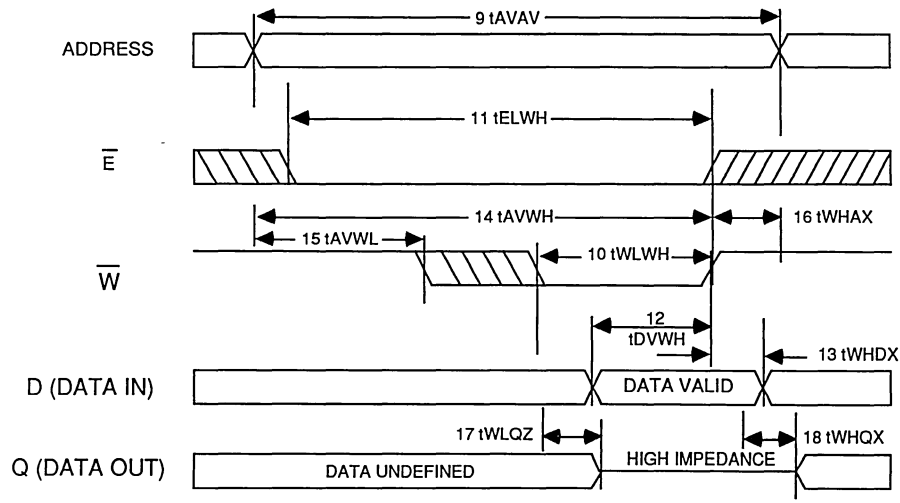
RECOMMENDED AC OPERATING CONDITIONS (0°C ≤ TA ≤ 70°C) (Vcc = 5.0V ±10%)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g,h]

No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1800-25 MIN	IMS 1800-25 MAX	IMS 1800-30 MIN	IMS 1800-30 MAX	IMS 1800-35 MIN	IMS 1800-35 MAX	IMS 1800-45 MIN	IMS 1800-45 MAX	UNITS	NOTES
9	tAVAV	tWC	Write Cycle Time	25		30		35		45		ns	
10	tWLWH	tWP	Write Pulse Width	20		25		30		40		ns	
11	tELWH	tCW	Chip Enable to End of Write	20		25		30		40		ns	
12	tDVWH	tDW	Data Setup to End of Write	10		12		15		20		ns	
13	tWHDX	tDH	Data Hold after End of Write	0		0		0		0		ns	
14	tAVWH	tAW	Address Setup to End of Write	20		25		30		40		ns	
15	tAVWL	tAS	Address Setup to Start of Write	0		0		0		0		ns	
16	tWHAX	tWR	Address Hold after End of Write	2		2		0		0		ns	
17	tWLQZ	tWZ	Write Enable to Output Disable	0	10	0	10	0	20	0	20	ns	f,j
18	tWHQX	tOW	Output Active After End of Write	5		5		5		5		ns	i

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and W must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$, or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2: $\overline{E}$1 OR E2 CONTROLLED[g,h]



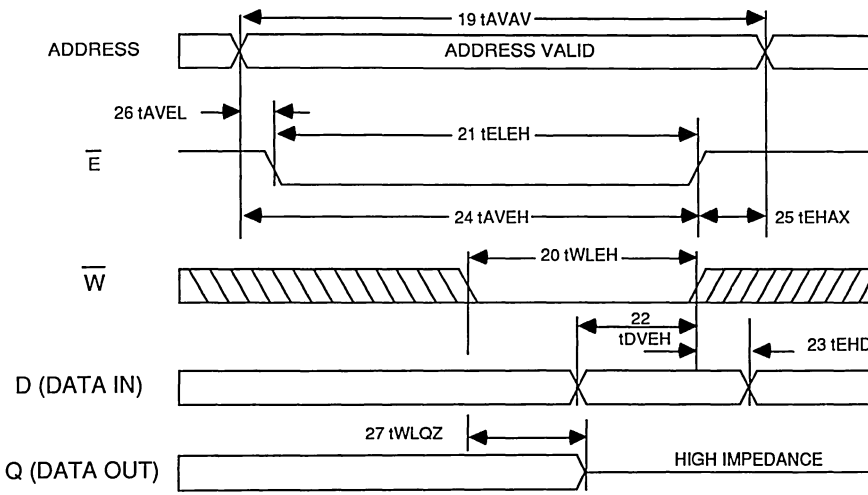
RECOMMENDED AC OPERATING CONDITIONS (0°C ≤ Ta ≤ 70°C) (Vcc = 5.0V ±10%)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1800-25 MIN	IMS 1800-25 MAX	IMS 1800-30 MIN	IMS 1800-30 MAX	IMS 1800-35 MIN	IMS 1800-35 MAX	IMS 1800-45 MIN	IMS 1800-45 MAX	UNITS	NOTES
19	tAVAV	t WC	Write Cycle Time	25		30		35		45		ns	
20	t WLEH	t WP	Write Pulse Width	20		25		30		40		ns	
21	tELEH	t CW	Chip Enable to End of Write	20		25		30		40		ns	
22	tDVEH	t DW	Data Setup to End of Write	10		12		15		20		ns	
23	tEHDX	t DH	Data Hold after End of Write	0		0		0		0		ns	
24	tAVEH	t AW	Address Setup to End of Write	20		25		30		40		ns	
25	tEHAX	t WR	Address Hold after End of Write	2		2		0		0		ns	
26	tAVEL	t AS	Address Setup to Start of Write	0		0		0		0		ns	
27	tWLQZ	t WZ	Write Enable to Output Disable	0	10	0	10	0	15	0	20	ns	f,j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1800 has two control inputs, Chip Enable (/E) and Write Enable (/W), 18 address inputs (A0 -A17), a Data In (D) and a Data Out (Q). The /E input controls device selection as well as active and standby modes. With /E low, the device is selected and the 18 address inputs are decoded to select one bit out of 256 Kbits. Read and Write operations on the memory cell are controlled by the /W input. With /E high, the device is deselected, the outputs are disabled and the power consumption is reduced to less than one-third of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as /W $\geq$ V_{IH} min with /E $\leq$ V_{IL} max. Read access time is measured from either /E going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while /E is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and long as /E remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by /E going low. As long as address is stable when /E goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when /E goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1800 is initiated by the latter of /E or /W to transition from a high to a low. In the case of /W falling last, the output buffer will be turned on t_{ELQX} after the falling edge of /E (just as in a read cycle). The output buffer is then turned off within t_{WLQZ} of the falling edge of /W. During this interval it is possible to have bus contention between devices with D and Q connected together in a common I/O configuration. Therefore input data should not be active until t_{WLQZ} to aviod bus contention.

WRITE CYCLE 1 waveform shows a write cycle terminated by /W going high. Data set-up and hold times are referenced to the rising edge of /W. When /W goes high at the end of the cycle with /E active, the output of the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by /E going high. Data set-up and hold times are referenced to the rising edge of /E. With /E high the output remains in the high impedance state.

APPLICATION

It is imperative when designing with any very high speed memory, such as the IMS1800, that the fundemental rules in regard to memory board layout be followed to ensure proper system operation.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1800. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Current transients associated with the operation of any high speed device have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad and be placed between each row of devices in the array. A larger tantalum capacitor of a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit area. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

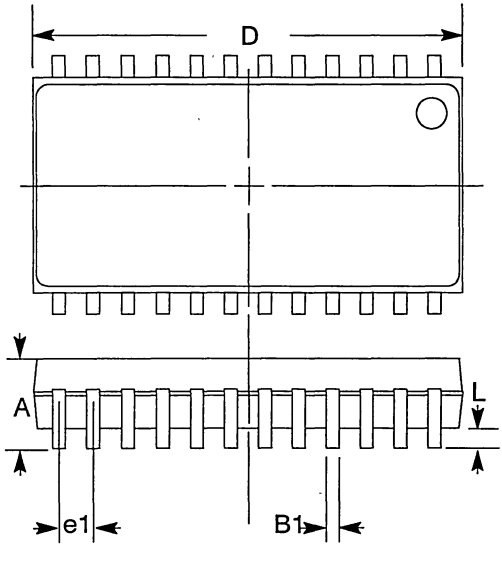
ORDERING INFORMATION

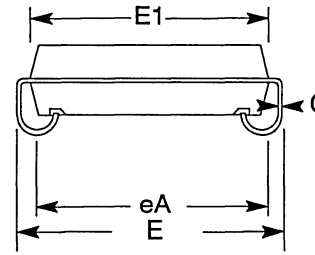
DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1800	25ns	Plastic DIP	IMS1800P-25
	25ns	Ceramic DIP	IMS1800S-25
	25ns	SOJ	IMS1800E-25
	25ns	Ceramic LCC	IMS1800W-25
	25ns	Ceramic LCC	IMS1800N-25
	30ns	Plastic DIP	IMS1800P-30
	30ns	Ceramic DIP	IMS1800S-30
	30ns	SOJ	IMS1800E-30
	30ns	Ceramic LCC	IMS1800W-30
	30ns	Ceramic LCC	IMS1800N-30
	35ns	Plastic DIP	IMS1800P-35
	35ns	Ceramic DIP	IMS1800S-35
	35ns	SOJ	IMS1800E-35
	35ns	Ceramic LCC	IMS1800W-35
	35ns	Ceramic LCC	IMS1800N-35
	45ns	Plastic DIP	IMS1800P-45
	45ns	Ceramic DIP	IMS1800S-45
	45ns	SOJ	IMS1800E-45
	45ns	Ceramic LCC	IMS1800W-45
	45ns	Ceramic LCC	IMS1800N-45

Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

PACKAGING INFORMATION

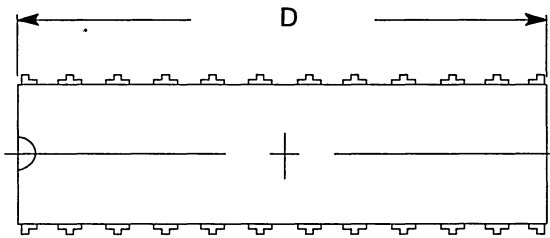
24 Pin Plastic J Leaded Small Outline



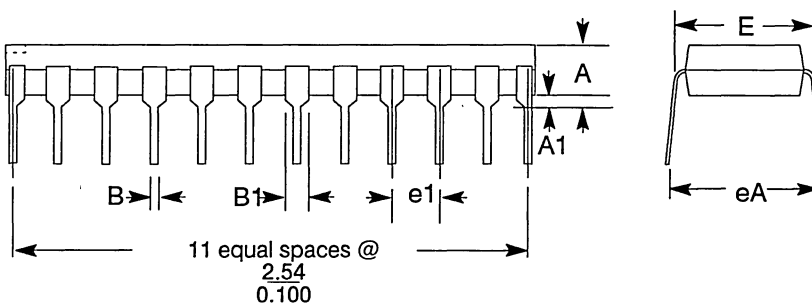


Dim	Inches		mm		Notes
	Min	Max	Min	Max	
A	.120	.140	3.048	3.556	
B1	.014	.019	.356	.483	
C	.010		.254		
D	.602	.612	15.291	15.545	
E	.335	.347	8.509	8.814	
E1	.292	.299	7.417	7.595	
e1	.050	.050	1.270	1.270	
eA	.262	.272	6.655	6.909	
L	.028	.036	.711	.914	

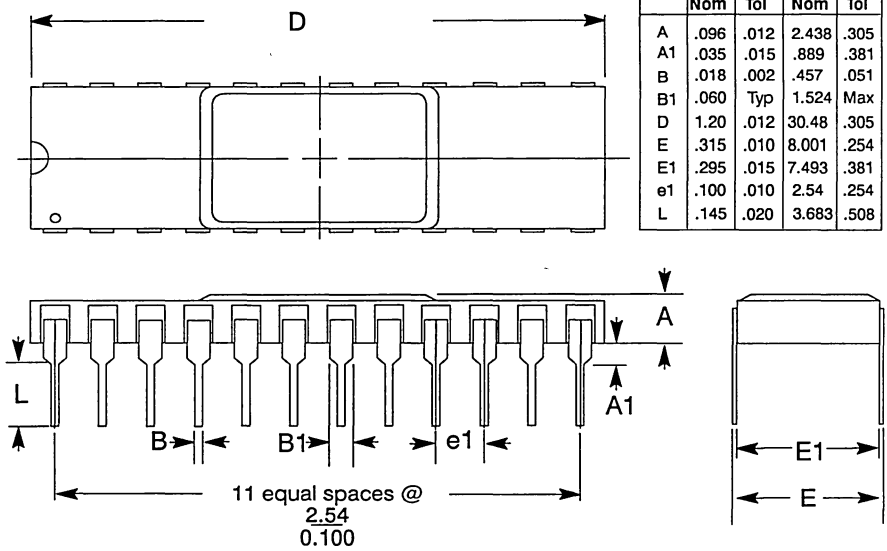
24 Pin Plastic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.165		4.551	
A1	.045	.025	1.143	.635
B	.018	.006	0.457	.152
B1	.060	.003	1.524	.127
D	1.160	.002	29.46	.05
E	.300	.003	7.620	.076
e1	.100	.010	2.54	.254
eA	.325	.010	8.255	.254



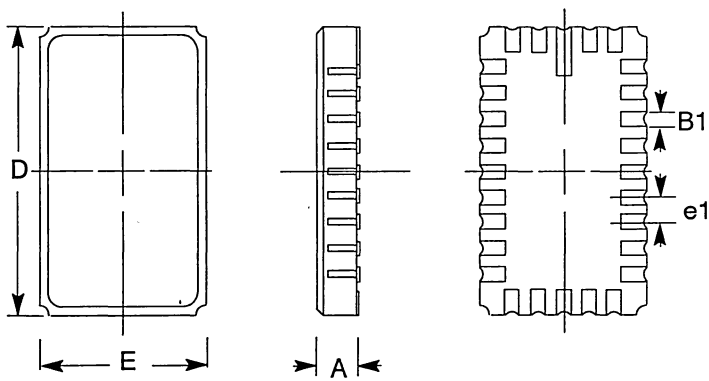
24 Pin Ceramic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.096	.012	2.438	.305
A1	.035	.015	.889	.381
B	.018	.002	.457	.051
B1	.060	Typ	1.524	Max
D	1.20	.012	30.48	.305
E	.315	.010	8.001	.254
E1	.295	.015	7.493	.381
e1	.100	.010	2.54	.254
L	.145	.020	3.683	.508

28 Pin Leadless Chip Carrier

Dim	Inches		mm		Notes
	Nom	Tol	Nom	Tol	
A	.071	.007	1.803	.178	
B1	.025	.003	.635	.076	
D	.550	.010	13.970	.254	
E	.350	.010	8.890	.254	
e1	.050	.002	1.270	.051	



IMS1820
CMOS
High Performance
64K x 4 Static RAM

inmos®

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.2 Micron Design Rules
- 64K x 4 Bit Organization
- 25, 30, 35 and 45 ns Address Access Times
- 25, 30, 35 and 45 ns Chip Enable Access Times
- Fully TTL Compatible
- Common Data Input and Outputs
- Three-state Outputs
- 24 Pin 300-mil DIP, SOJ and 28 Pin LCC
- Single +5V ± 10% Operation
- Power Down Function

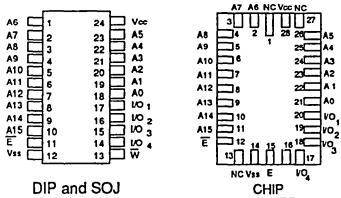
DESCRIPTION

The INMOS IMS1820 is a high performance 64Kx4 CMOS Static RAM. The IMS1820 allows speed enhancements to existing 64K x 4 applications with the additional benefit of reduced power consumption .

The IMS1820 features fully static operation requiring no external clocks or timing strobes, with equal access and cycle times. Additionally, the IMS1820 provides a Chip Enable function (/E) that can be used to place the device into a low power standby mode.

The IMS1820E is an extended temperature version pending military qualification of the IMS1820M.

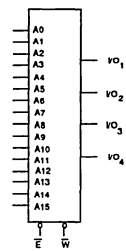
PIN CONFIGURATION



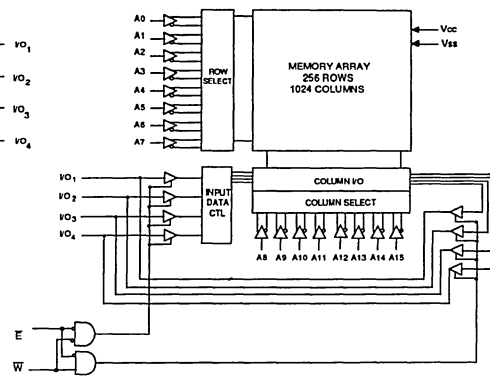
DIP and SOJ

CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{15}	ADDRESS INPUTS	Vcc	POWER (+5V)
$\overline{W}$	WRITE ENABLE	Vss	GROUND
I/O-I/O	DATA IN/OUT		
$\overline{E}$	CHIP ENABLE		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on I/O.....-1.0 to (Vcc+0.5V)
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One output at a time, one second duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		V_{CC} + 0.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-0.5 *		0.8	V	All inputs
T_A	Ambient Operating Temperature	0		70	°C	400 linear ft/min air flow

* V_{IL} min = -3.0V for pulse width < 10ns, note b

DC ELECTRICAL CHARACTERISTICS ($0°C \le T_A \le 70°C$) ($V_{CC} = 5.0V \pm 10\%$)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		120	mA	$t_{AVAV} = t_{AVAV}$ (min)
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		30	mA	$\overline{E1} \ge V_{IH}$ or $E2 \le V_{IL}$. All other inputs at $V_{IN} \le V_{IL}$ or $\ge V_{IH}$
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		10	mA	$\overline{E1} \ge (V_{CC} - 0.2V)$ or $E2 \le 0.2V$. All other inputs at $V_{IN} \le 0.2$ or $\ge (V_{CC} - 0.2V)$
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		15	mA	$\overline{E1} \ge (V_{CC} - 0.2V)$ or $E2 \le 0.2V$. Inputs cycling at $V_{IN} \le 0.2$ or $\ge (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current (Any Input)		±1	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		±10	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 8mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the outputs unloaded.

AC TEST CONDITIONS

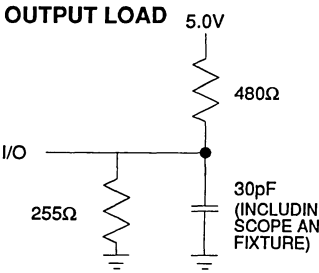
Input Pulse Levels .....V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0 MHZ)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	4	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested

FIGURE 1. OUTPUT LOAD



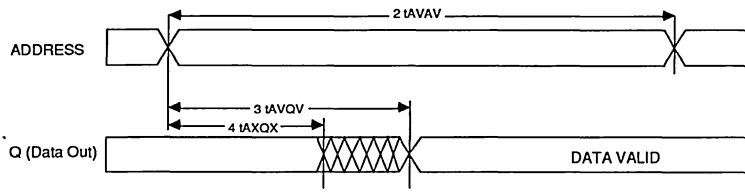
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[g]

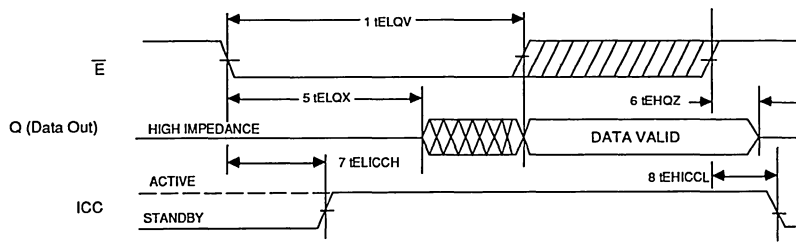
No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1820-25 MIN	IMS 1820-25 MAX	IMS 1820-30 MIN	IMS 1820-30 MAX	IMS 1820-35 MIN	IMS 1820-35 MAX	IMS 1820-45 MIN	IMS 1820-45 MAX	UNITS	NOTES
1	tELQV	tACS	Chip Enable Access Time		25		30		35		45	ns	
2	tAVAV	tRC	Read Cycle Time	25		30		35		45		ns	c
3	tAVQV	tAA	Address Access Time		25		30		35		45	ns	d
4	tAXQX	tOH	O/P Hold After Addr's Ch'ge	3		3		3		3		ns	
5	tELQX	tLZ	Chip Enable to O/P Active	3		3		3		3		ns	
6	tEHQZ	tHZ	Chip Disable to O/P Inactive	0	12	0	15	0	15	0	20	ns	f,j
7	tELICCH	tPU	Chip Enable to Power Up	0		0		0		0		ns	j
8	tEHICCL	tPD	Chip Enable to Power Down		30		30		30		30	ns	j
		tT	Input Rise and Fall Times		50		50		50		50	ns	e,j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



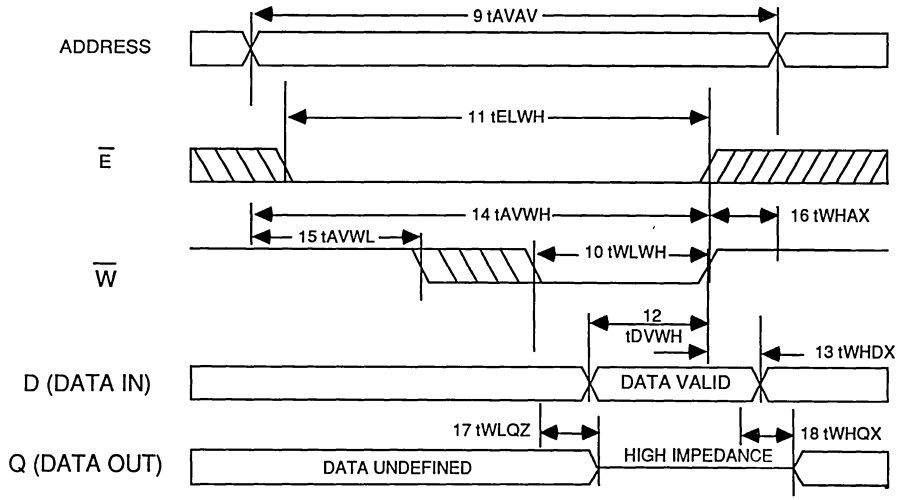
RECOMMENDED AC OPERATING CONDITIONS (0°C ≤ TA ≤ 70°C) (VCC = 5.0V ±10%)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g,h]

No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1820-25 MIN	IMS 1820-25 MAX	IMS 1820-30 MIN	IMS 1820-30 MAX	IMS 1820-35 MIN	IMS 1820-35 MAX	IMS 1820-45 MIN	IMS 1820-45 MAX	UNITS	NOTES
9	tAVAV	t WC	Write Cycle Time	25		30		35		45		ns	
10	tWLWH	t WP	Write Pulse Width	20		25		30		40		ns	
11	tELWH	t CW	Chip Enable to End of Write	20		25		30		40		ns	
12	tDVWH	t DW	Data Setup to End of Write	10		12		15		20		ns	
13	tWHDX	t DH	Data Hold after End of Write	0		0		0		0		ns	
14	tAVWH	t AW	Address Setup to End of Write	20		25		30		40		ns	
15	tAVWL	t AS	Address Setup to Start of Write	0		0		0		0		ns	
16	tWHAX	t WR	Address Hold after End of Write	2		2		0		0		ns	
17	tWLQZ	t WZ	Write Enable to Output Disable	0	10	0	10	0	15	0	20	ns	f,i
18	tWHQX	t OW	Output Active After End of Write	5		5		5		5		ns	i

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and W must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$, or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



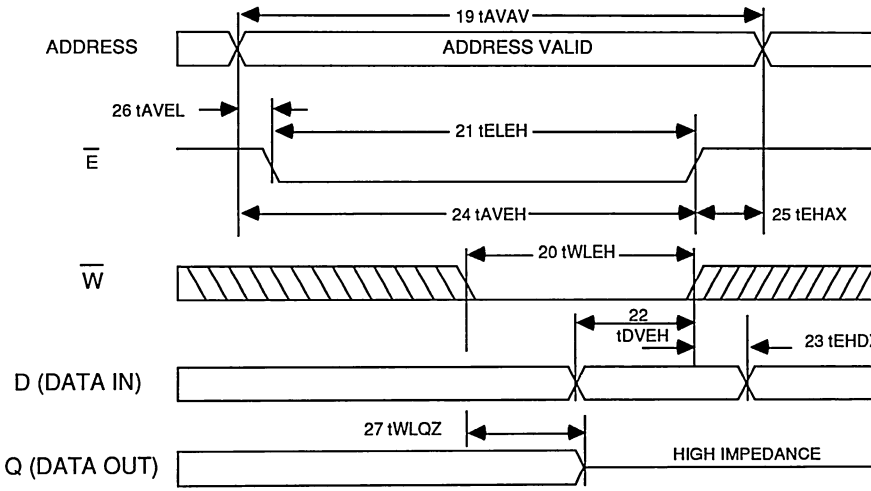
RECOMMENDED AC OPERATING CONDITIONS (0°C ≤ Ta ≤ 70°C) (Vcc = 5.0V ±10%)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1820-25 MIN	IMS 1820-25 MAX	IMS 1820-30 MIN	IMS 1820-30 MAX	IMS 1820-35 MIN	IMS 1820-35 MAX	IMS 1820-45 MIN	IMS 1820-45 MAX	UNITS	NOTES
19	tAVAV	t WC	Write Cycle Time	25		30		35		45		ns	
20	tWLEH	t WP	Write Pulse Width	20		25		30		40		ns	
21	tELEH	t CW	Chip Enable to End of Write	20		25		30		40		ns	
22	tDVEH	t DW	Data Setup to End of Write	10		12		15		20		ns	
23	tEHDX	t DH	Data Hold after End of Write	0		0		0		0		ns	
24	tAVEH	t AW	Address Setup to End of Write	20		25		30		40		ns	
25	tEHAX	t WR	Address Hold after End of Write	2		2		0		0		ns	
26	tAVEL	t AS	Address Setup to Start of Write	0		0		0		0		ns	
27	tWLQZ	t WZ	Write Enable to Output Disable	0	10	0	10	0	15	0	20	ns	f,j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1820 has two control inputs, Chip Enable (/E) and Write Enable (/W), 16 address inputs (A0 -A15), and four data I/O lines.

The /E input controls device selection as well as active and standby modes. With /E low, the device is selected and the 16 address inputs are decoded to select one 4 bit word out of 64K words. Read and Write operations on the memory cell are controlled by the /W input. With /E high, the device is deselected, the output is disabled and the power consumption is reduced to less than one-third of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as /W $\geq$ V_{IH} min with /E $\leq$ V_{IL} max. Read access time is measured from either /E going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while /E is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and long as /E remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by /E going low. As long as address is stable when /E goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when /E goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1820 is initiated by the latter of /E or /W to transition from a high to a low. In the case of /W falling last, the output buffer will be turned on t_{ELOX} after the falling edge of /E (just as in a read cycle). The output buffer is then turned off within t_{WLOZ} of the falling edge of /W. During this interval it is possible to have bus contention between devices with D and Q connected together in a common I/O configuration. Therefore input data should not be active until t_{WLOZ} to aviod bus contention.

WRITE CYCLE 1 waveform shows a write cycle terminated by /W going high. Data set-up and hold times are referenced to the rising edge of /W. When /W goes high at the end of the cycle with /E active, the output of the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by /E going high. Data set-up and hold times are referenced to the rising edge of /E. With /E high the output remains in the high impedance state.

APPLICATION

It is imperative when designing with any very high speed memory, such as the IMS1820, that the fundemental rules in regard to memory board layout be followed to ensure proper system operation.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1820. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Current transients associated with the operation of any high speed device have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad and be placed between each row of devices in the array. A larger tantalum capacitor of a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit area. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

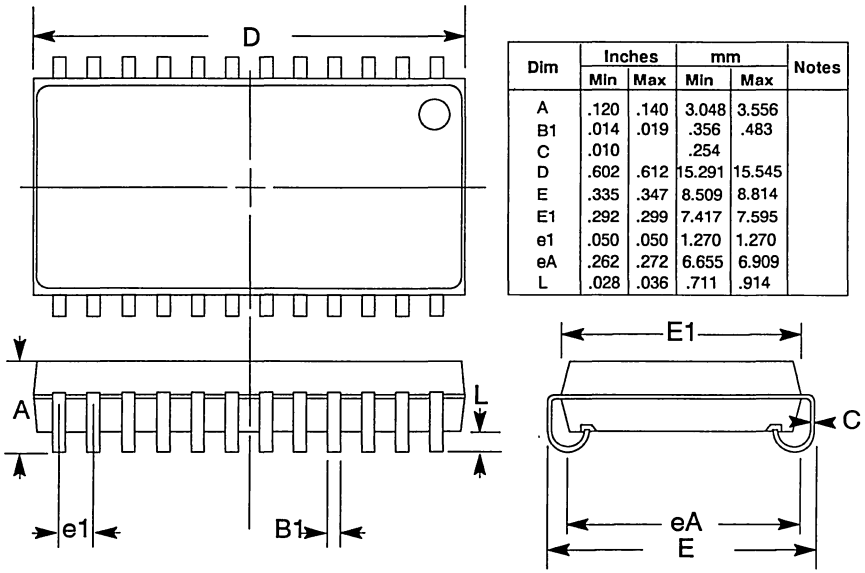
ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1820	25ns	Plastic DIP	IMS1820P-25
	25ns	Ceramic DIP	IMS1820S-25
	25ns	SOJ	IMS1820E-25
	25ns	Ceramic LCC	IMS1820W-25
	25ns	Ceramic LCC	IMS1820N-25
	30ns	Plastic DIP	IMS1820P-30
	30ns	Ceramic DIP	IMS1820S-30
	30ns	SOJ	IMS1820E-30
	30ns	Ceramic LCC	IMS1820W-30
	30ns	Ceramic LCC	IMS1820N-30
	35ns	Plastic DIP	IMS1820P-35
	35ns	Ceramic DIP	IMS1820S-35
	35ns	SOJ	IMS1820E-35
	35ns	Ceramic LCC	IMS1820W-35
	35ns	Ceramic LCC	IMS1820N-35
	45ns	Plastic DIP	IMS1820P-45
	45ns	Ceramic DIP	IMS1820S-45
	45ns	SOJ	IMS1820E-45
	45ns	Ceramic LCC	IMS1820W-45
	45ns	Ceramic LCC	IMS1820N-45

Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

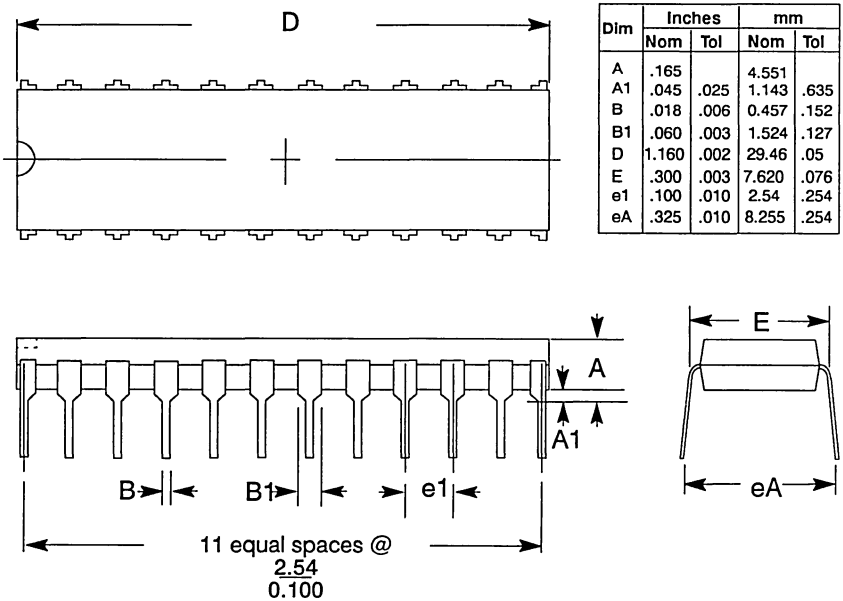
PACKAGING INFORMATION

24 Pin Plastic J Leaded Small Outline



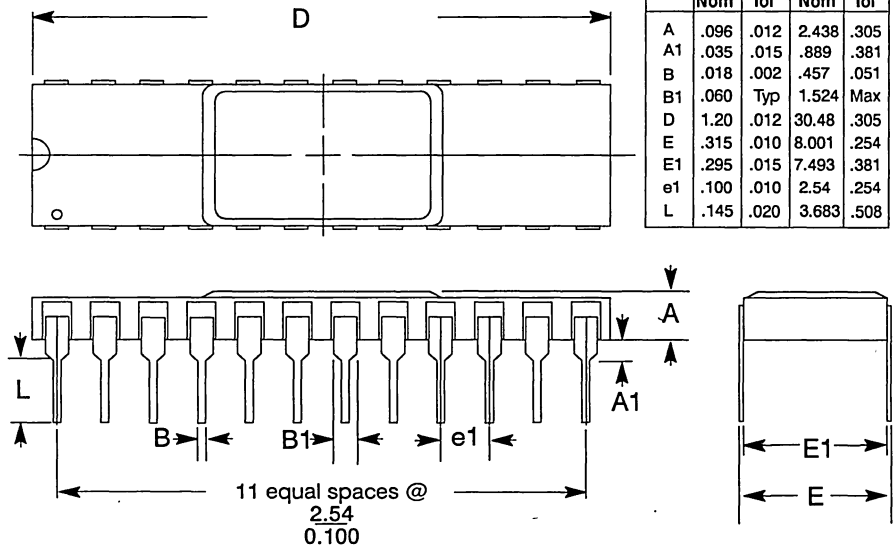
Dim	Inches		mm		Notes
	Min	Max	Min	Max	
A	.120	.140	3.048	3.556	
B1	.014	.019	.356	.483	
C	.010		.254		
D	.602	.612	15.291	15.545	
E	.335	.347	8.509	8.814	
E1	.292	.299	7.417	7.595	
e1	.050	.050	1.270	1.270	
eA	.262	.272	6.655	6.909	
L	.028	.036	.711	.914	

24 Pin Plastic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.165		4.551	
A1	.045	.025	1.143	.635
B	.018	.006	0.457	.152
B1	.060	.003	1.524	.127
D	1.160	.002	29.46	.05
E	.300	.003	7.620	.076
e1	.100	.010	2.54	.254
eA	.325	.010	8.255	.254

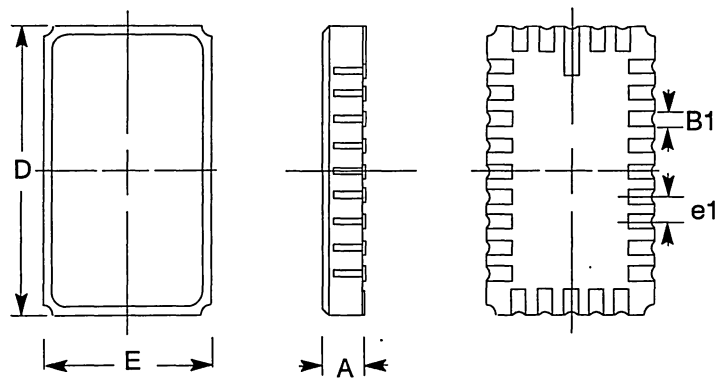
24 Pin Ceramic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.096	.012	2.438	.305
A1	.035	.015	.889	.381
B	.018	.002	.457	.051
B1	.060	Typ	1.524	Max
D	1.20	.012	30.48	.305
E	.315	.010	8.001	.254
E1	.295	.015	7.493	.381
e1	.100	.010	2.54	.254
L	.145	.020	3.683	.508

28 Pin Leadless Chip Carrier

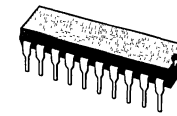
Dim	Inches		mm		Notes
	Nom	Tol	Nom	Tol	
A	.071	.007	1.803	.178	
B1	.025	.003	.635	.076	
D	.550	.010	13.970	.254	
E	.350	.010	8.890	.254	
e1	.050	.002	1.270	.051	



MK41H66/MK41H67(N,P) -20/25/35

16K x 1 CMOS STATIC RAM

- 20, 25, AND 35NS ADDRESS ACCESS TIME
- EQUAL ACCESS AND CYCLE TIMES
- 20-PIN, 300 MIL PLASTIC
- ALL INPUT AND OUTPUT PINS TTL COMPATIBLE, LOW CAPACITANCE, AND PROTECTED AGAINST STATIC DISCHARGE
- 50µa CMOS STANDBY CURRENT (MK41H67)
- HIGH SPEED CHIP SELECT (MK41H66)
- JEDEC STANDARD PINOUT



N
DIP–20
(Plastic Package)

TRUTH TABLE (MK41H66)

$\overline{CS}$	$\overline{WE}$	Mode	DQ	Power
H	X	Deselect	High Z	Active
L	L	Write	High Z	Active
L	H	Read	Data Out	Active

X = Don't Care

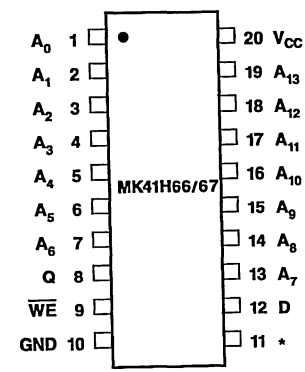
TRUTH TABLE (MK41H67)

$\overline{CE}$	$\overline{WE}$	Mode	DQ	Power
H	X	Deselect	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	Data Out	Active

PIN NAMES

A_0 - A_{13} - Address	$\overline{WE}$ - Write Enable
$\overline{CE}$ - Chip Enable (MK41H67)	GND - Ground V_{CC} - + 5 V
$\overline{CS}$ - Chip Select (MK41H66)	D - Data In Q - Data Out

Figure 1 : Pin Connections.



* $\overline{CS}$ = MK41H66 ; $\overline{CE}$ = MK41H67.

DESCRIPTION

The MK41H66 and MK41H67 feature fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Both require only a single + 5V ± 10 percent power supply. Both devices are fully TTL compatible.

The MK41H67 has a Chip Enable power down feature which automatically reduces power dissipation when the $\overline{CE}$ pin is brought inactive (high). Standby power can be further reduced to microwatt levels by holding the Address and $\overline{CE}$ pins at full supply rail voltages.

The MK41H66 Chip Select pin provides a high speed chip select access, allowing fast read cycles despite decoder delays.

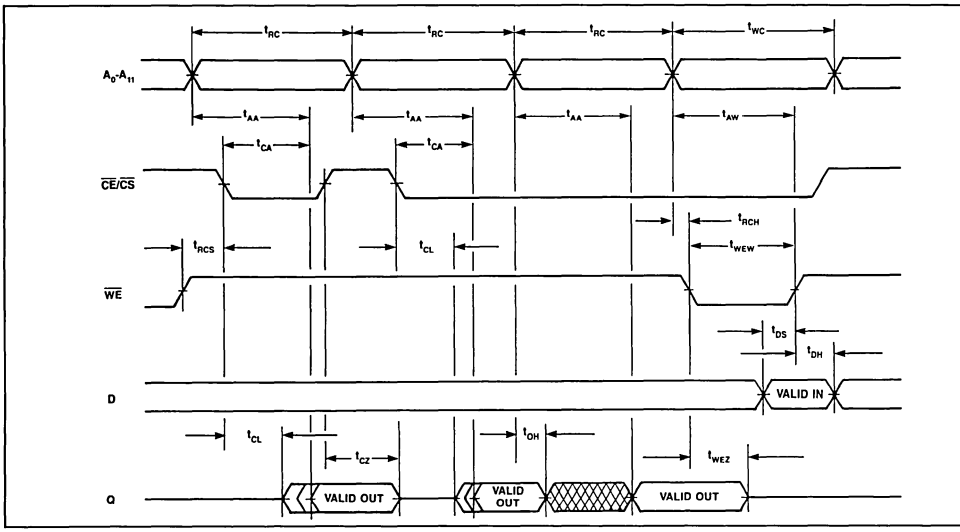
The MK41H66 Chip Select pin provides a high speed chip select access, allowing fast read cycles despite decoder delays.

OPERATIONS

READ MODE

The MK41H66/7 is in the Read Mode whenever $\overline{WE}$ (Write Enable) is high and $\overline{CE}/\overline{CS}$ (Chip Enable/Select) is low, providing a ripple-through access to any one of 16,384 locations in the static storage array. Valid data will be available at the Data Output pin (Q) within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}/\overline{CS}$ access time is satisfied. If $\overline{CE}/\overline{CS}$ access time is not met, data access will be measured from the limiting parameter (t_{CA}) rather than the address. The state of the Data Output pin is controlled by the $\overline{CE}/\overline{CS}$, and $\overline{WE}$ control signals. The Q may be in an indeterminate state at t_{CL}, but the Q will always have valid data at t_{AA}.

FIGURE 2. READ-READ-READ-WRITE TIMING



READ CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS
(0°C≤T_A≤70°C) (V_{CC} = 5.0 V ± 10 percent)

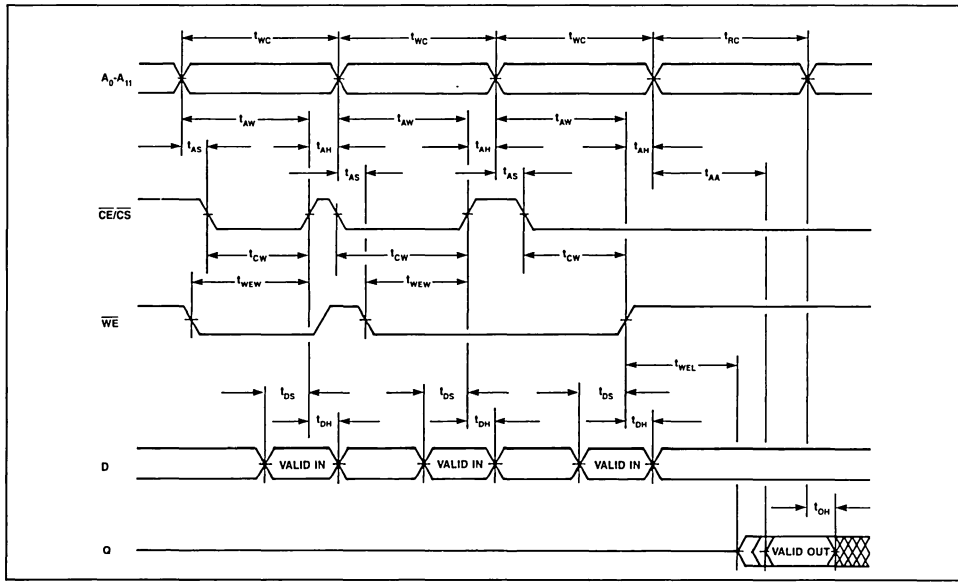
		MK41H6X-20		MK41H6X-25		MK41H6X-35			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	20		25		35		ns	
t_{AA}	Address Access Time		20		25		35	ns	1
t_{CL}	Chip Enable to Low-Z (MK41H67)	5		5		5		ns	2
t_{CL}	Chip Select to Low-Z (MK41H66)	5		5		5		ns	2
t_{CA}	Chip Enable Access Time (MK41H67)		20		25		35	ns	1
t_{CA}	Chip Select Access Time (MK41H66)		10		12		15	ns	1
t_{RCS}	Read Command Setup Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{OH}	Valid Data Out Hold Time	5		5		5		ns	1
t_{CZ}	Chip Enable to High-Z (MK41H67)		8		10		13	ns	2
t_{CZ}	Chip Select to High-Z (MK41H66)		7		8		10	ns	2
t_{WEZ}	Write Enable to High-Z		8		10		13	ns	2

WRITE MODE

The MK41H66/7 is in the Write Mode whenever the $\overline{WE}$ and $\overline{CE}/\overline{CS}$ inputs are in the low state. $\overline{CE}/\overline{CS}$ or $\overline{WE}$ must be high during address transitions. Addresses must be held valid throughout a write cycle. The Write begins with the concurrence of a low on $\overline{WE}$ and $\overline{CE}$ /$\overline{CS}$. Therefore, t_{AS} is referenced to the latter occurring edge of $\overline{CE}/\overline{CS}$, or $\overline{WE}$.

If the output is enabled ($\overline{CE}/\overline{CS}$ is low), then $\overline{WE}$ will return the output to high impedance within t_{WEZ} of its falling edge. Data-In must remain valid t_{DH} after the rising edge of $\overline{CE}/\overline{CS}$ or $\overline{WE}$.

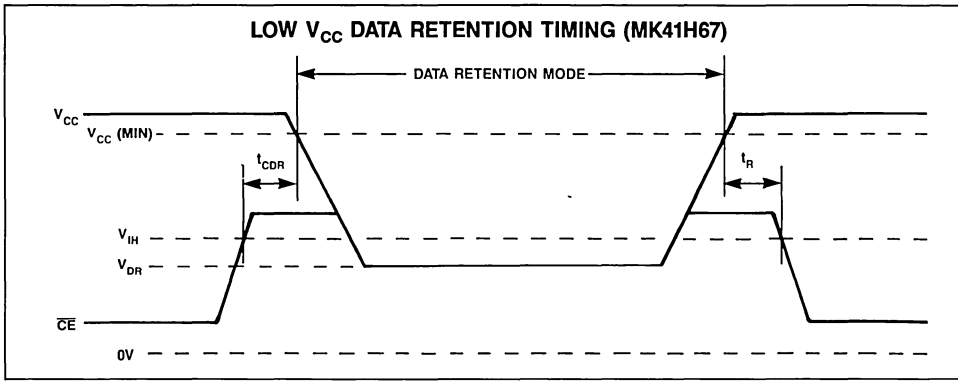
FIGURE 3. WRITE-WRITE-WRITE-READ TIMING



WRITE CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS
(0°C≤T_A≤70°C) (V_{CC} = 5.0 V ± 10 percent)

		MK41H6X-20		MK41H6X-25		MK41H6X-35			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	Write Cycle Time	20		25		35		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AW}	Address Valid to End of Write	16		20		30		ns	
t_{AH}	Address Hold after End of Write	0		0		0		ns	
t_{CW}	Chip Enable/Select to End of Write	18		22		32		ns	
t_{WEW}	Write Enable to End of Write	16		20		30		ns	
t_{DS}	Data Setup Time	12		14		15		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WEL}	Write Enable to Low-Z	5		5		5		ns	2

FIGURE 4. DATA RETENTION TIMING



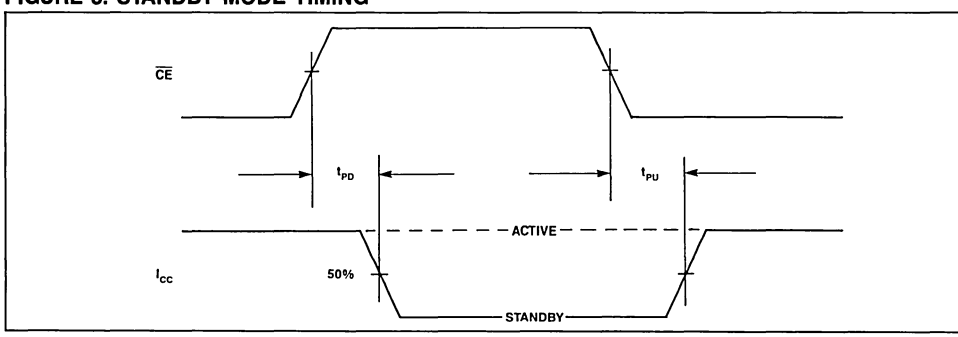
LOW V_{CC} DATA RETENTION CHARACTERISTICS
($0°C \leq T_A \leq 70°C$)

SYM	PARAMETERS	MIN	MAX	UNIT	NOTES
V_{DR}	V_{CC} for Data Retention	2.0	V_{CC} (min)	V	7
I_{CCDR}	Data Retention Power Supply Current	—	50	μA	7
t_{CDR}	Chip Deselection to Data Retention Time	0	—	ns	
t_R	Operation Recovery Time	t_{RC}	—	ns	

STANDBY MODE (MK41H67 Only)

The MK41H67 is in Standby Mode whenever $\overline{CE}$ is held at or above V_{IH}.

FIGURE 5. STANDBY MODE TIMING



STANDBY MODE
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

		MK41H67-20		MK41H67-25		MK41H67-35			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{PD}	Chip Enable High to Power Down		20		25		35	ns	
t_{PU}	Chip Enable Low to Power Up	0		0		0		ns	

APPLICATION

The MK41H66/7 operates from a 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the 41H66/7 can also interface to 5 volt CMOS on all inputs and outputs. Refer to the normalized performance curves that follow.

Since very high frequency current transients will be associated with the operation of the MK41H66/7, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. Additionally, a high frequency decoupling capacitor should be placed next to each RAM. The capacitor should be 0.1µF or larger.

Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Value	Unit
Voltage on any Pin Relative to GND	–1.0 to +7.0	V
Ambient Operating Temperature (T_A)	0 to + 70	°C
Ambient Storage Temperature (plastic)	–55 to +125	°C
Ambient Storage Temperature (ceramic)	-65 to +150	°C
Total Device Power Dissipation	1	W
Output Current per Pin	50	mA

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	3
GND	Supply Voltage	0	0	0	V	
V_{IH}	Logic 1 Voltage, All Inputs	2.2		V_{CC} + 1.0	V	3
V_{IL}	Logic 0 Voltage, All Inputs	– 0.3		0.8	V	3, 4

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0V ± 10 percent)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
I_{CC1}	Average Power Supply Current			120	mA	5
I_{CC2}	TTL Standby Current (MK41H67 only)			10	mA	6
I_{CC3}	CMOS Standby Current (MK41H67 only)			50	µA	7
I_{IL}	Input Leakage Current (any input pin)	– 1		+ 1	µA	8
I_{OL}	Output Leakage Current (any output pin)	– 10		+ 10	µA	9
V_{OH}	Output Logic 1 Voltage (I_{OUT} = – 4mA)	2.4			V	3
V_{OL}	Output Logic 0 Voltage (I_{OUT} = + 8mA)			0.4	V	3

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_1	Capacitance on input pins	4	5	pF	10
C_2	Capacitance on Q pins	8	10	pF	5, 10

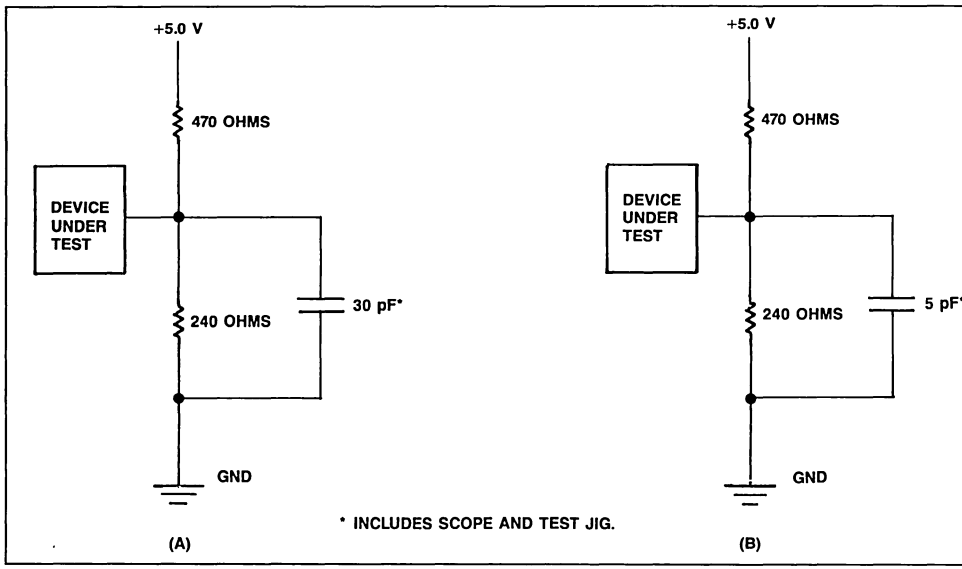
NOTES

1. Measured with load shown in Figure 6(A).
2. Measured with load shown in Figure 6(B).
3. All voltages referenced to GND.
4. V_{IL} may undershoot to −2.0 volts for 200ns or less during input transitions.
5. I_{CC1} is measured as the average AC current with V_{CC} = V_{CC} (max) and with the outputs open circuit. tcycle = min. duty cycle 100%.
6. $\overline{CE}$ = V_{IH}, All Other Inputs = Don't Care.
7. V_{CC} (max) $\geq \overline{CE} \geq V_{CC}$ − 0.3 V GND + 0.3 V $\geq A_0$-$A_{13} \geq V_{IL}$ (min) or V_{IH} (max) $\geq A_0$-$A_{13} \geq V_{CC}$ −0.3 V. All Other Inputs = Don't Care.
8. Input leakage current specifications are valid for all V_{IN} such that 0 V < V_{IN} < V_{CC}. Measured at V_{CC} = V_{CC} (max).
9. Output leakage current specifications are valid for all V_{OUT} such that 0 V < V_{OUT} < V_{CC}, $\overline{CE}/\overline{CS}$ = V_{IH} and V_{CC} in valid operating range.
10. Capacitances are sampled and not 100% tested.

AC TEST CONDITIONS

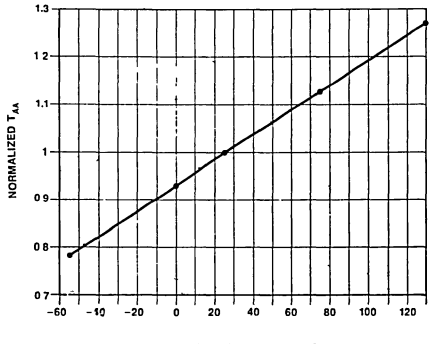
Input Levels ..... GND to 3.0 V
Transition Times ..... 5 ns
Input and Output Signal Timing Reference Level ..... 1.5 V
Ambient Temperature ..... 0°C to 70°C
V_{CC} ..... 5.0 V ± 10 percent

FIGURE 6. OUTPUT LOAD CIRCUITS

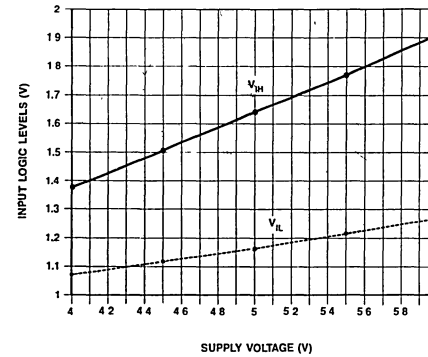


NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

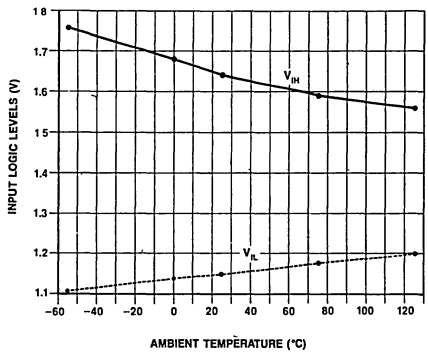
NORMALIZED CHIP ENABLE ACCESS TIME VS. AMBIENT TEMPERATURE V_{CC}=5.0V



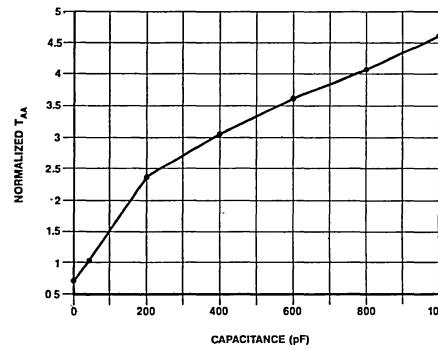
LOGIC THRESHOLD VOLTAGE VS. SUPPLY VOLTAGE T_A=25°C



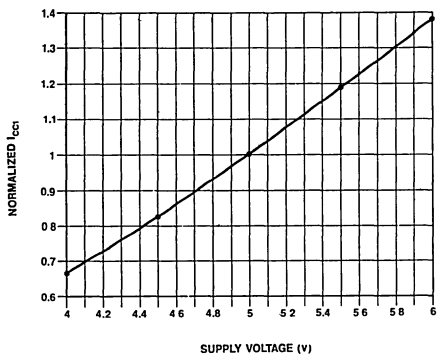
LOGIC THRESHOLD VOLTAGE VS. AMBIENT TEMPERATURE V_{CC}=5.0V



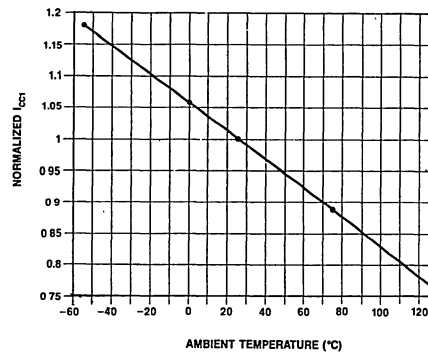
NORMALIZED ACCESS TIME VS. OUTPUT LOADING V_{CC}=5.0 V T_A=25°C



NORMALIZED SUPPLY CURRENT VS. SUPPLY VOLTAGE T_A=0°C

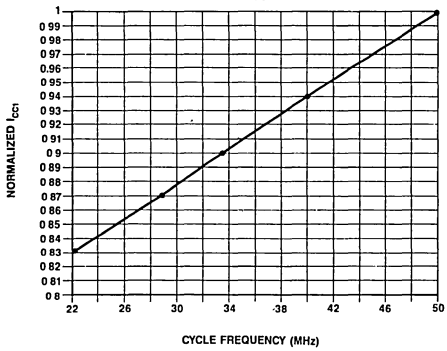


NORMALIZED SUPPLY CURRENT VS. AMBIENT TEMPERATURE V_{CC}=5.0V

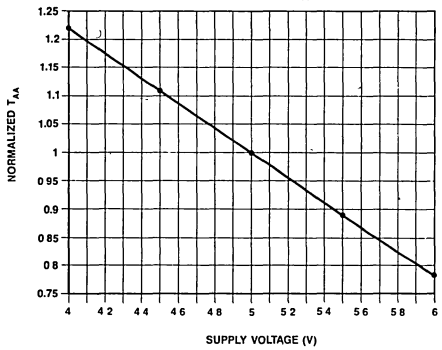


NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

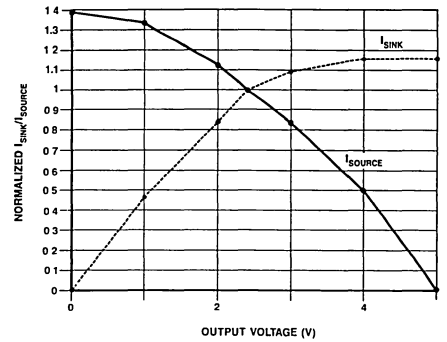
NORMALIZED SUPPLY CURRENT VS.
CYCLE TIME V_{CC}=5.0V T_A=25°C



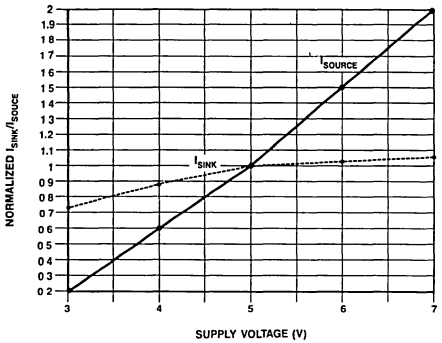
NORMALIZED ACCESS TIME VS.
SUPPLY VOLTAGE T_A=25°C



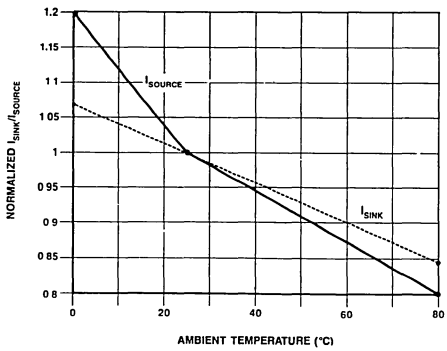
NORMALIZED SOURCE AND SINK CURRENTS VS.
OUTPUT VOLTAGE VOLTAGE V_{CC}=5.0V T_A=25°C

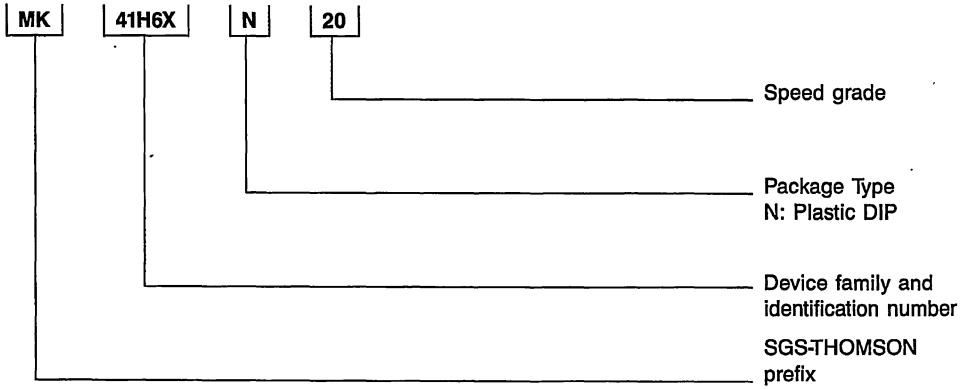


NORMALIZED SOURCE AND SINK CURRENTS VS.
SUPPLY VOLTAGE T_A=25°C



NORMALIZED SOURCE AND SINK CURRENTS VS.
AMBIENT TEMPERATURE V_{CC}=5.0V



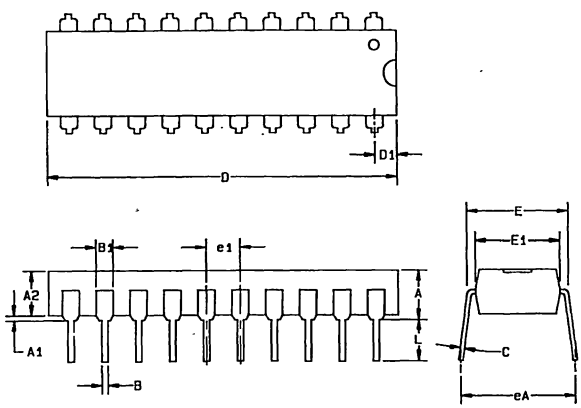


ORDER CODES

Part Number	Access Time	Package Type	Temperature Range
MK41H67N-20	20ns	20 Pin Plastic DIP	0°C to 70°C
MK41H67N-25	25ns	20 Pin Plastic DIP	0°C to 70°C
MK41H67N-35	35ns	20 Pin Plastic DIP	0°C to 70°C
MK41H66N-20	20ns	20 Pin Plastic DIP	0°C to 70°C
MK41H66N-25	25ns	20 Pin Plastic DIP	0°C to 70°C
MK41H66N-35	35ns	20 Pin Plastic DIP	0°C to 70°C

PACKAGE DESCRIPTION

20 PIN "N" PACKAGE PLASTIC DIP



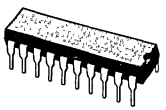
Dim.	mm		Inches		Notes
	Min.	Max.	Min.	Max.	
A		5.334		.210	2
A1	0.381		.015		2
A2	3.048	3.556	.120	.140	
B	0.381	0.533	.015	.021	3
B1	1.27	1.778	.050	.070	
C	0.203	0.304	.008	.012	3
D	25.908	26.67	1.020	1.050	1
D1	1.524	1.905	.060	.075	
E	7.62	8.255	.300	.325	
E1	6.096	6.858	.240	.270	
e1	2.286	2.794	.090	.110	
eA	7.62	10.16	.300	.400	
L	3.048		.120		

Notes : 1. Overall length includes 010 in flash on either end of the package.
2. Package standoff to be measured per jedec requirements.
3. The maximum limit shall be increased by 003 in when solder lead finish is specified.

MK41H68/MK41H69(N,P) -20/25/35

4K x 4 CMOS STATIC RAM

- 20, 25, AND 35ns ADDRESS ACCESS TIME
- EQUAL ACCESS AND CYCLE TIMES
- 20-PIN, 300 MIL PLASTIC
- ALL INPUTS AND OUTPUTS TTL COMPATIBLE, LOW CAPACITANCE, AND PROTECTED AGAINST STATIC DISCHARGE
- 50µA CMOS STANDBY CURRENT (MK41H68)
- TTL STANDBY CURRENT UNAFFECTED BY ADDRESS ACTIVITY (MK41H68)
- HIGH SPEED CHIP SELECT (MK41H69)
- JEDEC STANDARD PINOUT



N
DIP-20
(Plastic Package)

TRUTH TABLE (MK41H68)

$\overline{CE}$	$\overline{WE}$	Mode	DQ	Power
H	X	Deselect	High Z	Standby
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

TRUTH TABLE (MK41H69)

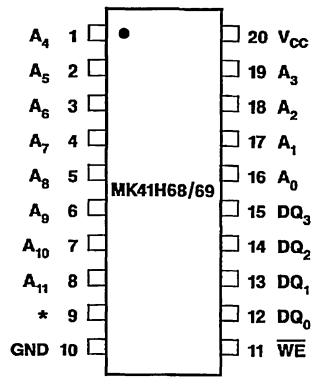
$\overline{CS}$	$\overline{WE}$	Mode	DQ	Power
H	X	Deselect	High Z	Active
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

X : Don't care.

PIN NAMES

A_0 - A_{11} - Address	$\overline{WE}$ - Write Enable
DQ_0 - DQ_3 - Data I/O	GND - Ground
	V_{CC} - + 5 Volts
$\overline{CE}$ - Chip Enable (MK41H68)	
$\overline{CS}$ - Chip Select (MK41H69)	

Figure 1 : Pin Connections.



* $\overline{CS}$ = 41H69 ; $\overline{CE}$ = 41H68

DESCRIPTION

The MK41H68 and MK41H69 feature fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Both require only a single + 5V ± 10 percent power supply. Both devices are fully TTL compatible.

The MK41H68 has a Chip Enable power down feature which automatically reduces power dissipation when the $\overline{CE}$ pin is brought inactive (high). Standby power can be further reduced to microwatt levels by raising the $\overline{CE}$ pin to the full V_{CC} voltage.

The MK41H69 Chip Select pin provides a high speed chip select access, allowing fast read cycles despite decoder delays.

power can be further reduced to microwatt levels by raising the $\overline{CE}$ pin to the full V_{CC} voltage.

The MK41H69 Chip Select pin provides a high speed chip select access, allowing fast read cycles despite decoder delays.

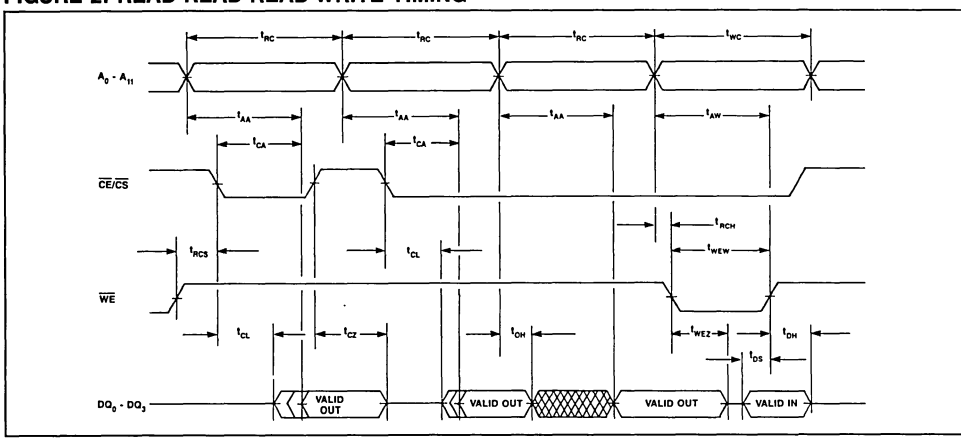
OPERATIONS

READ MODE

The MK41H68/9 is in the Read Mode whenever $\overline{WE}$ (Write Enable) is high and $\overline{CE}/\overline{CS}$ (Chip Enable/Select) is low, providing a ripple-through access to data from four of 16,384 locations in the static storage array. The unique address specified by the 12 Address Inputs defines which one of 4096 nibbles of data is to be accessed.

Valid data will be available at the four Data Output pins within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}/\overline{CS}$ access time is satisfied. If $\overline{CE}/\overline{CS}$ access time is not met, data access will be measured from the limiting parameter (t_{CA}) rather than the address. The state of the four Data I/O pins is controlled by the $\overline{CE}/\overline{CS}$, and $\overline{WE}$ control signals. The data lines may be in an indeterminate state at t_{CL}, but the data lines will always have valid data at t_{AA}.

FIGURE 2. READ-READ-READ-WRITE TIMING



READ CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

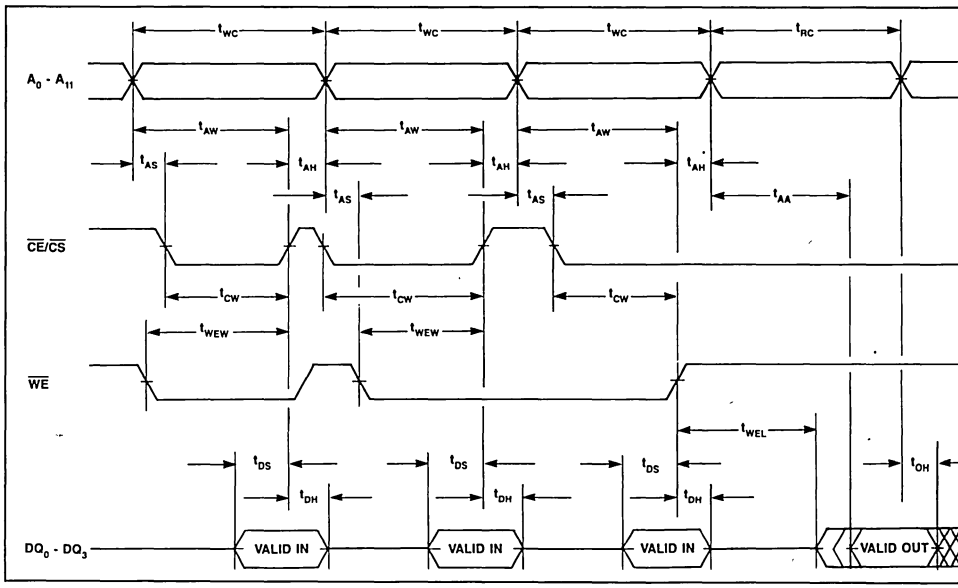
		MK41H6X-20		MK41H6X-25		MK41H6X-35			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	20		25		35		ns	
t_{AA}	Address Access Time		20		25		35	ns	1
t_{CL}	Chip Enable to Low-Z (MK41H68)	7		7		7		ns	2
t_{CL}	Chip Select to Low-Z (MK41H69)	5		5		5		ns	2
t_{CA}	Chip Enable Access Time (MK41H68)		20		25		35	ns	1
t_{CA}	Chip Select Access Time (MK41H69)		10		12		15	ns	1
t_{RCS}	Read Command Setup Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{OH}	Valid Data Out Hold Time	5		5		5		ns	1
t_{CZ}	Chip Enable to High-Z (MK41H68)		8		10		13	ns	2
t_{CZ}	Chip Select to High-Z (MK41H69)		7		8		10	ns	2
t_{WEZ}	Write Enable to High-Z		8		10		13	ns	2

WRITE MODE

The MK41H68/9 is in the Write Mode whenever the $\overline{WE}$ and $\overline{CE}/\overline{CS}$ inputs are in the low state. $\overline{CE}/\overline{CS}$ or $\overline{WE}$ must be high during address transitions. Addresses must be held valid throughout a write cycle. The Write begins with the concurrence of a low on $\overline{WE}$ and $\overline{CE}$ /$\overline{CS}$. Therefore, t_{AS} is referenced to the latter occurring edge of $\overline{CE}/\overline{CS}$, or $\overline{WE}$.

If the output is enabled ($\overline{CE}/\overline{CS}$ is low), then $\overline{WE}$ will return the outputs to high impedance within t_{WEZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-In must remain valid t_{DH} after the rising edge of $\overline{CE}/\overline{CS}$ or $\overline{WE}$.

FIGURE 3. WRITE-WRITE-WRITE-READ TIMING

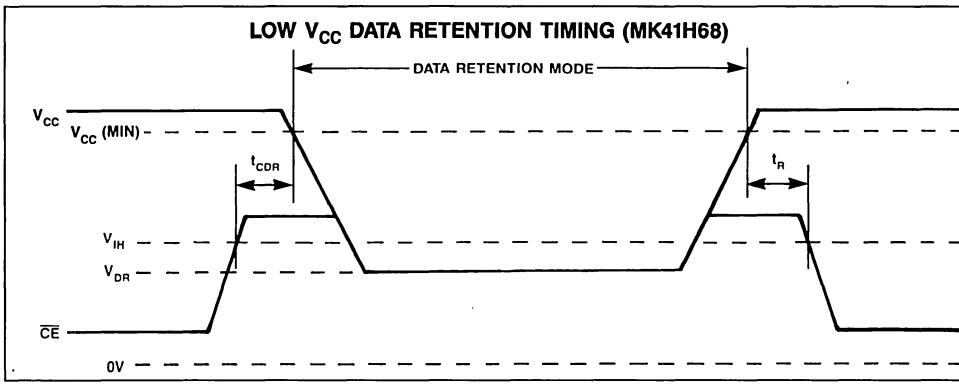


WRITE CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS

(0°C≤T_A≤70°C) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MK41H6X-20		MK41H6X-25		MK41H6X-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WC}	Write Cycle Time	20		25		35		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AW}	Address Valid to End of Write	16		20		30		ns	
t_{AH}	Address Hold after End of Write	0		0		0		ns	
t_{CW}	Chip Enable/Select to End of Write	18		22		32		ns	
t_{WEW}	Write Enable to End of Write	16		20		30		ns	
t_{DS}	Data Setup Time	12		14		15		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WEL}	Write Enable to Low-Z	5		5		5		ns	2

FIGURE 4. DATA RETENTION TIMING



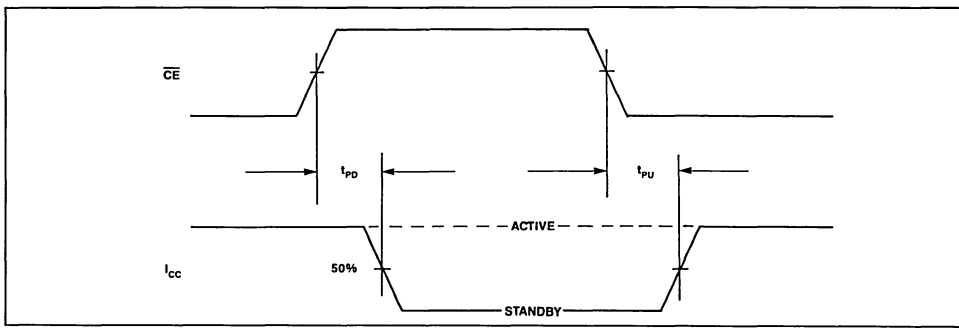
LOW V_{CC} DATA RETENTION CHARACTERISTICS
($0°C \leq T_A \leq 70°C$)

SYM	PARAMETERS	MIN	MAX	UNIT	NOTES
V_{DR}	V_{CC} for Data Retention	2.0	V_{CC} (min)	V	6
I_{CCDR}	Data Retention Power Supply Current	—	50	μA	6
t_{CDR}	Chip Deselection to Data Retention Time	0	—	ns	
t_R	Operation Recovery Time	t_{RC}	—	ns	

STANDBY MODE (MK41H68 Only)

The MK41H68 is in Standby Mode whenever $\overline{CE}$ is held at or above V_{IH}.

FIGURE 5. STANDBY MODE TIMING



STANDBY MODE
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

		MK41H68-20		MK41H68-25		MK41H68-35			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{PD}	Chip Enable High to Power Down		20		25		35	ns	
t_{PU}	Chip Enable Low to Power Up	0		0		0		ns	

APPLICATION

The MK41H68/9 operates from a 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the 41H68/9 can also interface to 5 volt CMOS on all inputs and outputs. Refer to the normalized performance curves that follow.

Since very high frequency current transients will be associated with the operation of the MK41H68/9, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. Additionally, a high frequency decoupling capacitor should be placed next to each RAM. The capacitor should be 0.1 μF or larger.

Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND ..... −1.0 V to +7.0 V
Ambient Operating Temperature (T_A) ..... 0°C to +70°C
Ambient Storage Temperature (Plastic) ..... −55°C to +125°C
Ambient Storage Temperature (Ceramic) ..... −65°C to +150°C
Total Device Power Dissipation ..... 1 Watt
Output Current per Pin ..... 50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	3
GND	Supply Voltage	0	0	0	V	
V_{IH}	Logic 1 Voltage, All Inputs	2.2		V_{CC}+1.0	V	3
V_{IL}	Logic 0 Voltage, All Inputs	−0.3		0.8	V	3

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Power Supply Current		120	mA	4
I_{CC2}	TTL Standby Current (MK41H68 only)		8	mA	5
I_{CC3}	CMOS Standby Current (MK41H68 only)		50	μA	6
I_{IL}	Input Leakage Current (Any Input Pin)	−1	+1	μA	7
I_{OL}	Output Leakage Current (Any Output Pin)	−10	+10	μA	8
V_{OH}	Output Logic 1 Voltage (I_{OUT} = −4 mA)	2.4		V	3
V_{OL}	Output Logic 0 Voltage (I_{OUT} = +8 mA)		0.4	V	3

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_1	Capacitance on input pins	4	5	pF	9
C_2	Capacitance on DQ pins	8	10	pF	5,9

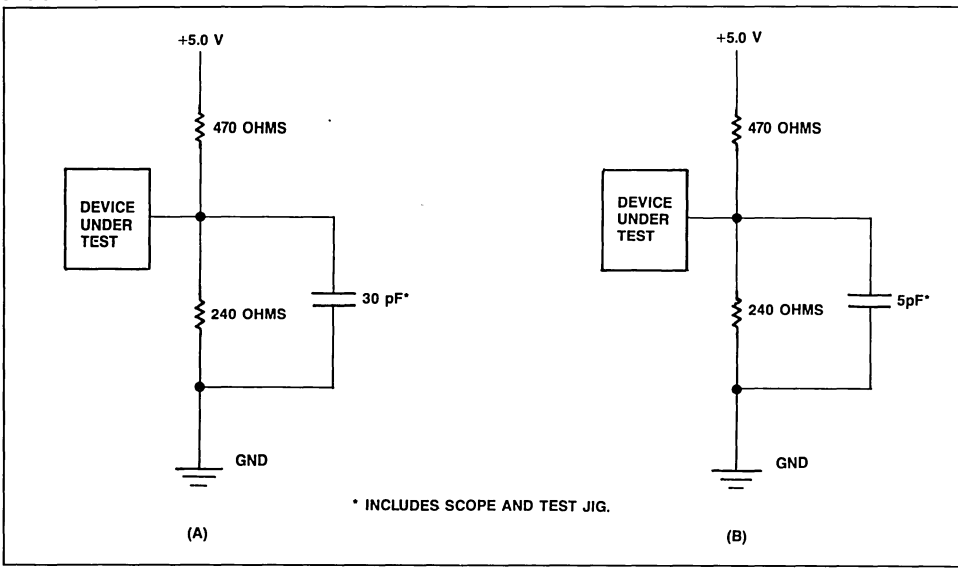
NOTES

1. Measured with load shown in Figure 6(A).
2. Measured with load shown in Figure 6(B).
3. All voltages referenced to GND.
4. I_{CC1} is measured as the average AC current with V_{CC} = V_{CC} (max) and with the outputs open circuit. tcycle = min. duty cycle 100%.
5. $\overline{CE}$ = V_{IH}, All Other Inputs = Don't Care.
6. V_{CC} (max) ≥ $\overline{CE}$ ≥ V_{CC} − 0.3 V, All Other Inputs = Don't Care.
7. Input leakage current specifications are valid for all V_{IN} such that 0 V < V_{IN} < V_{CC}. Measured at V_{CC} = V_{CC} (max).
8. Output leakage current specifications are valid for all V_{OUT} such that 0 V < V_{OUT} < V_{CC}, $\overline{CE}$/$\overline{CS}$ = V_{IH} and V_{CC} in valid operating range.
9. Capacitances are sampled and not 100% tested.

AC TEST CONDITIONS

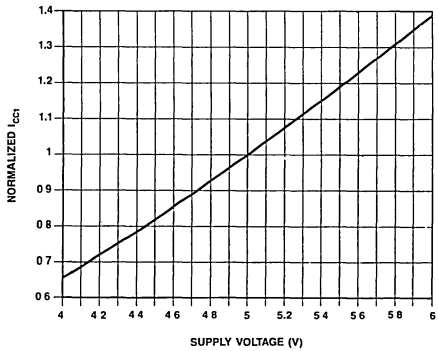
Input Levels ..... GND to 3.0 V
Transition Times ..... 5 ns
Input and Output Signal Timing Reference Level ..... 1.5 V
Ambient Temperature ..... 0°C to 70°C
V_{CC} ..... 5.0 V ± 10 percent

FIGURE 6. OUTPUT LOAD CIRCUITS

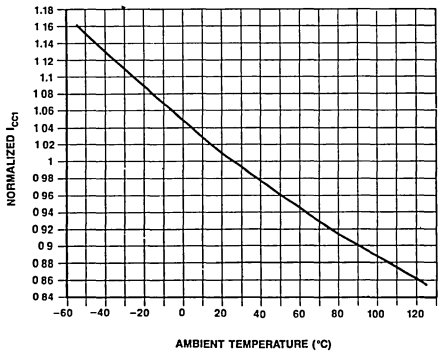


NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

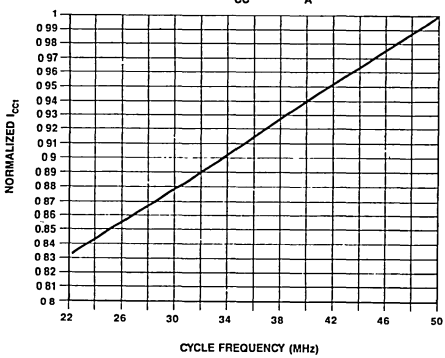
NORMALIZED SUPPLY CURRENT VS.
SUPPLY VOLTAGE T_A=0°C



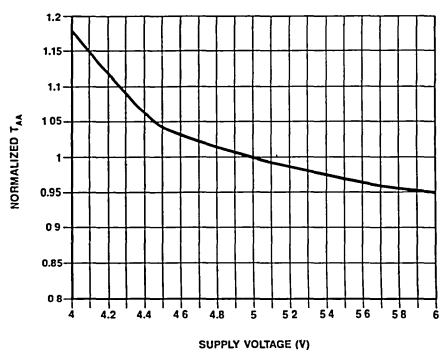
NORMALIZED SUPPLY CURRENT VS.
AMBIENT TEMPERATURE V_{CC}=5.0V



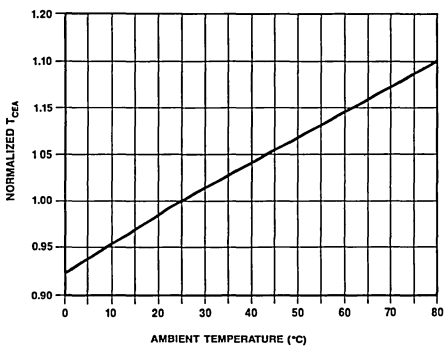
NORMALIZED SUPPLY CURRENT VS.
CYCLE TIME V_{CC}=5.0V T_A=25°C



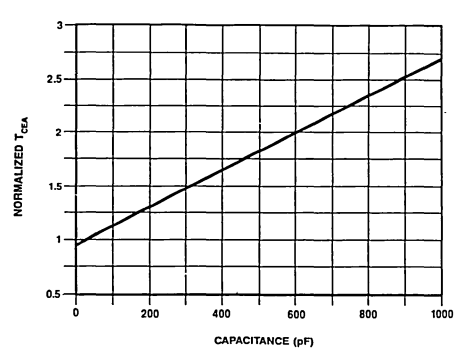
NORMALIZED ACCESS TIME VS.
SUPPLY VOLTAGE T_A=25°C



NORMALIZED ACCESS TIME VS.
AMBIENT TEMPERATURE V_{CC}=5.0V

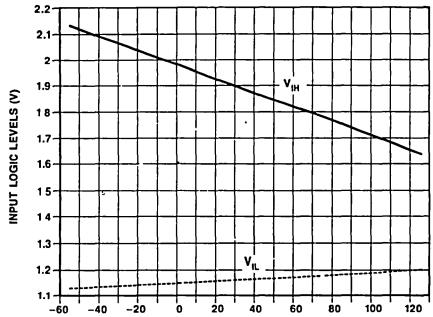


NORMALIZED ACCESS TIME VS.
OUTPUT LOADING V_{CC}=5.0V T_A=25°C

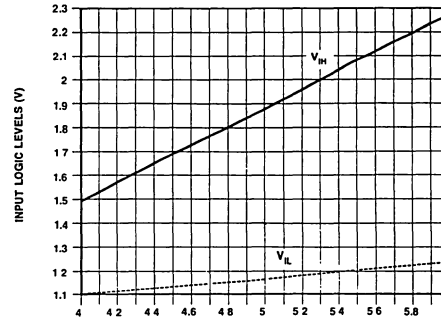


NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

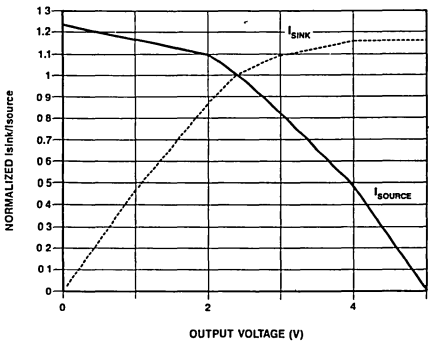
LOGIC THRESHOLD VOLTAGE VS. AMBIENT TEMPERATURE V_{CC}=5.0V



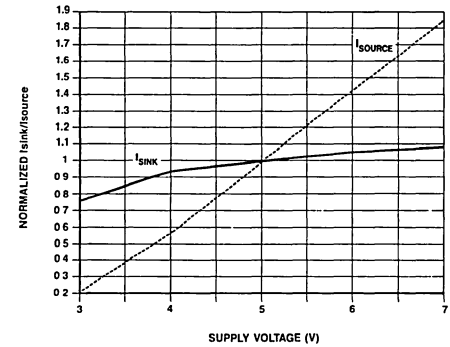
LOGIC THRESHOLD VOLTAGE VS. SUPPLY VOLTAGE T_A=25°C



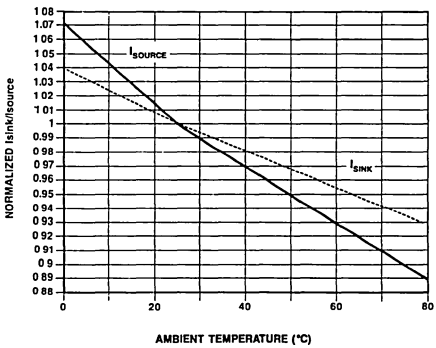
NORMALIZED SOURCE AND SINK CURRENTS VS. OUTPUT VOLTAGE V_{CC}=5.0V T_A=25°C

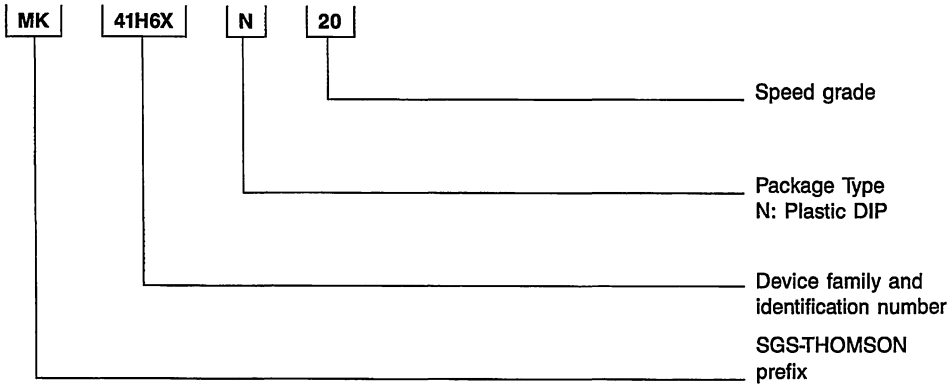


NORMALIZED SOURCE AND SINK CURRENTS VS. SUPPLY VOLTAGE T_A=25°C



NORMALIZED SOURCE AND SINK CURRENTS VS. AMBIENT TEMPERATURE V_{CC}=5.0V



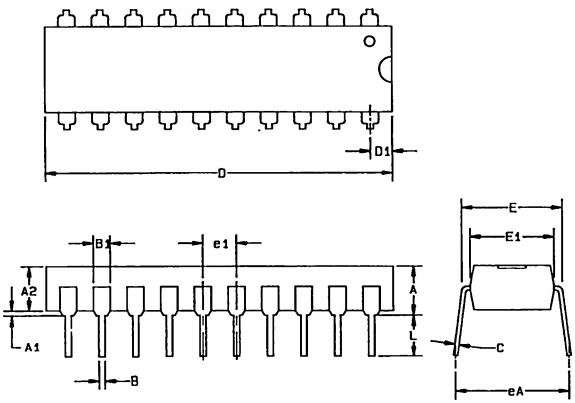


ORDER CODES

Part Number	Access Time	Package Type	Temperature Range
MK41H68N-20	20ns	20 Pin Plastic DIP	0°C to 70°C
MK41H68N-25	25ns	20 Pin Plastic DIP	0°C to 70°C
MK41H68N-35	35ns	20 Pin Plastic DIP	0°C to 70°C
MK41H69N-20	20ns	20 Pin Plastic DIP	0°C to 70°C
MK41H69N-25	25ns	20 Pin Plastic DIP	0°C to 70°C
MK41H69N-35	35ns	20 Pin Plastic DIP	0°C to 70°C

PACKAGE DESCRIPTION

20 PIN "N" PACKAGE, PLASTIC DIP

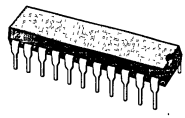


Dim.	mm		Inches		Notes
	Min.	Max.	Min.	Max.	
A		5.334		.210	2
A1	0.381		.015		2
A2	3.048	3.556	.120	.140	
B	0.381	0.533	.015	.021	3
B1	1.27	1.778	.050	.070	
C	0.203	0.304	.008	.012	3
D	25.908	26.67	1.020	1.050	1
D1	1.524	1.905	.060	.075	
E	7.62	8.255	.300	.325	
E1	6.096	6.858	.240	.270	
e1	2.286	2.794	.090	.110	
eA	7.62	10.16	.300	.400	
L	3.048		.120		

Notes : 1. Overall length includes .010 in. Flash on either end of the package.
2. Package standoff to be measured per jedec requirements.
3. The maximum limit shall be increased by .003 in. When solder lead finish is specified.

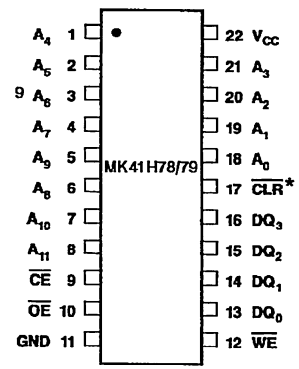
4K x 4 CMOS STATIC RAM

- 20, 25, AND 35ns ADDRESS ACCESS TIME
- EQUAL ACCESS AND CYCLE TIMES
- 22-PIN, 300 MIL PLASTIC
- ALL INPUTS AND OUTPUTS TTL COMPATIBLE, LOW CAPACITANCE, AND PROTECTED AGAINST STATIC DISCHARGE
- TTL STANDBY CURRENT UNAFFECTED BY ADDRESS ACTIVITY
- SEPARATE OUTPUT ENABLE CONTROL
- FLASH CLEAR FUNCTION



N
DIP–22
(Plastic Package)

Figure 1 : Pin Connection.



* Applies to MK41H79 only.

DESCRIPTION

The MK41H78/79 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. It requires a single + 5V ± 10 percent power supply and is fully TTL compatible.

The device has a Chip Enable power down feature which automatically reduces power dissipation when the $\overline{CE}$ pin is brought inactive (high). Standby power can be further reduced by raising the $\overline{CE}$ pin to the full V_{CC} voltage. An Output Enable ($\overline{OE}$) pin provides a high speed tristate control, allowing fast read/write cycles to be achieved with the common-I/O data bus.

Flash $\overline{Clear}$ operation is provided on the MK41H79 via the $\overline{CLR}$ pin, and $\overline{CE}$ active (low). A low applied to the $\overline{CLR}$ pin clears all RAM bits to zero, making it especially useful for high speed cache and buffer storage applications.

PIN NAMES

A_0 - A_{11} - Address	$\overline{OE}$ - Ouput Enable
DQ_0 - DQ_3 - Data I/O	$\overline{WE}$ - Write Enable
$\overline{CLR}$ - Flash Clear	GND - Ground
$\overline{CE}$ - Chip Enable	V_{CC} - + 5V

ABSOLUTE MAXIMUM RATINGS*

Parameter	Value	Unit
Voltage on any Pin Relative to GND	- 1.0 to + 7.0	V
Ambient Operating Temperture (T_A)	0 to 70	°C
Ambient Storage Temperature (plastic)	- 55 to + 125	°C
Ambient Storage Temperature (ceramic)	- 65 to +150	°C
Total Device Power Dissipation	1	W
Output Currrent per Pin	50	mA

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{CLR}$ *	Mode	DQ	Power
H	X	X	X	Deselect	High Z	Standby
L	X	L	H	Write	D_{IN}	Active
L	L	H	H	Read	D_{OUT}	Active
L	H	H	H	Read	High Z	Active
L	X	L	L	Flash Clear	High Z	Active
L	L	H	L	Flash Clear	Low Z	Active
L	H	H	L	Flash Clear	High Z	Active

X = Don't Care
* Applies to MK41H79 only.

RECOMMENDED DC OPERATING CONDITIONS ($0°C \le T_A \le 70°C$)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	3
GND	Supply Voltage	0	0	0	V	
V_{IH}	Logic 1 Voltage, All Inputs	2.2		V_{CC} + 1.0	V	3
V_{IL}	Logic 0 Voltage, All Inputs	- 0.3		0.8	V	3

DC ELECTRICAL CHARACTERISTICS ($0°C \le T_A \le 70°C$) (V_{CC} = 5.0V ± 10 percent)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
I_{CC1}	Average Power Supply Current			120	mA	4
I_{CC2}	TTL Standby Current			16	mA	5
I_{CC3}	CMOS Standby Current			8	mA	6
I_{IL}	Input Leakage Current (any input pin)	- 1		+ 1	µA	7
I_{OL}	Output Leakage Current (any output pin)	- 10		+ 10	µA	8
V_{OH}	Output Logic 1 Voltage (I_{OUT} = – 4 mA)	2.4			V	3
V_{OL}	Output Logic 0 Voltage (I_{OUT} = + 8 mA)			0.4	V	3

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

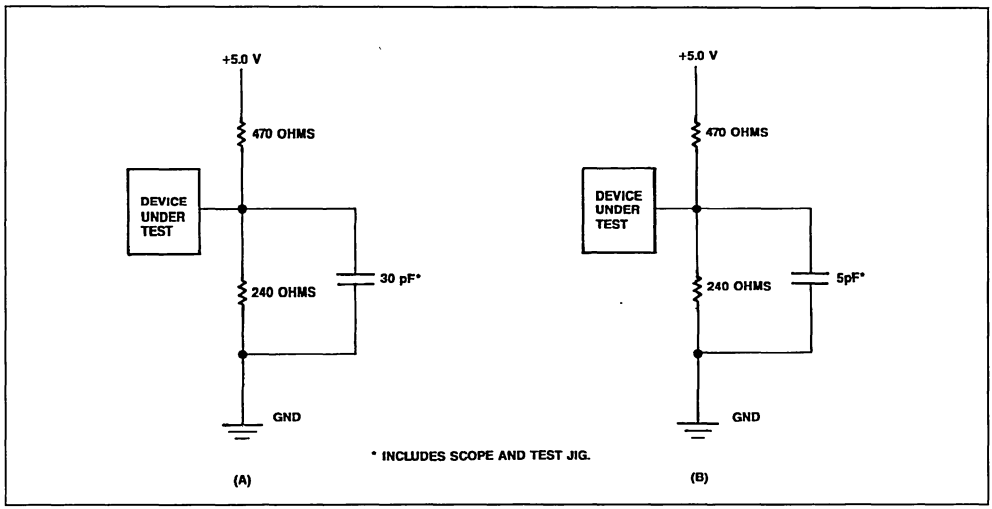
Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
C_1	Capacitance on Input Pins	4		5	pF	9
C_2	Capacitance on DQ Pins	8		10	pF	9

Notes : 1. Measured with load shown in figure 2(A).
2. Measured with load shown in figure 2(B).
3. All voltages referenced to GND.
4. I_{CC1} is measured as the average AC current with V_{CC} = V_{CC} (max) and with the outputs open circuit. t_{RC} = t_{RC} (min) is used.
5. $\overline{CE}$ = V_{IH}, all other inputs = Don't Care.
6. V_{CC} (max) ≥ $\overline{CE}$ ≥ V_{CC} - 0.3V, all other inputs = Don't Care.
7. Input leakage current specifications are valid for all V_{IN} such that 0V < V_{IN} < V_{CC}. Measured at V_{CC} = V_{CC} (max).
8. Output leakage current specifications are valid for all V_{OUT} such that 0V < V_{OUT} < V_{CC}, $\overline{CE}$ = V_{IH} and V_{CC} in valid

AC TEST CONDITIONS

Input Levels ..... GND to 3.0V
Transition Times 5ns
Input and Output Signal Timing Reference Level 1.5V
Ambient Temperature ..... 0°C to 70°C
Vcc ..... 5.0V ± 10 percent

Figure 2 : Output Load Circuits.



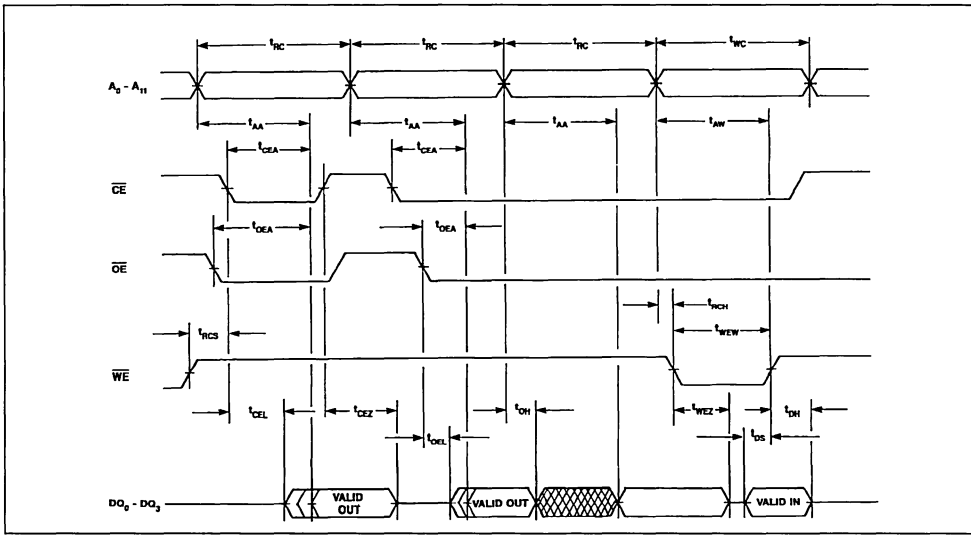
OPERATIONS

READ MODE

The MK41H78/79 is in the Read Mode whenever WE (Write Enable) is high and CE (Chip Enable) is low, providing a ripple-through access to data from four of 16,384 locations in the static storage array. The unique address specified by the 12 Address Inputs defines which one of 4096 nibbles of data is to be accessed.

Valid data will be available at the four Data Output pins within t_{AA} after the last address input signal is stable, providing that the CE and OE (output Enable) access times are satisfied. If CE or OE access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}) rather than the address. The state of the four Data I/O pins is controlled by the CE, WE and OE control signals. The data lines may be in an indeterminate state at t_{CEL} and t_{OEL}, but the data lines will always have valid data at t_{AA}.

Figure 3 : Read–read–read–write Timing.



AC ELECTRICAL CHARACTERISTICS (read cycle timing)
($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10$ percent)

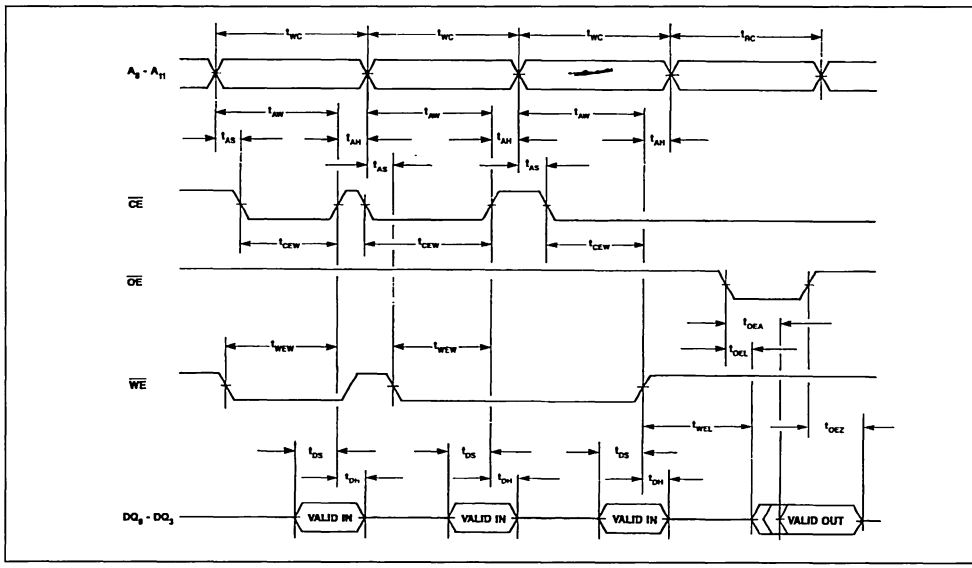
Symbol	Parameter	MK41H7X-20		MK41H7X-25		MK41H7X-35		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	20		25		35		ns	
t_{AA}	Address Access Time		20		25		35	ns	1
t_{CEL}	Chip Enable to Low-Z	7		7		7		ns	2
t_{CEA}	Chip Enable Access Time		20		25		35	ns	1
t_{OEL}	Output Enable to Low-Z	2		2		2		ns	2
t_{OEA}	Output Enable Access Time		10		12		15	ns	1
t_{RCS}	Read Command Setup Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{OH}	Valid Data Out Hold Time	5		5		5		ns	1
t_{CEZ}	Chip Enable to High-Z		8		10		13	ns	2
t_{OEZ}	Output Enable to High-Z		7		8		10	ns	2
t_{WEZ}	Write Enable to High-Z		8		10		13	ns	2

WRITE MODE

The MK41H78/79 is in the Write Mode whenever the $\overline{WE}$ and $\overline{CE}$ inputs are in the low state. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions. Addresses must be held valid throughout a write cycle. The Write begins with the concurrence of a low on $\overline{WE}$ and $\overline{CE}$. Therefore, t_{AS} is referenced to the latter occurring edge of $\overline{CE}$ or $\overline{WE}$. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$.

If the output is enabled ($\overline{CE}$ and $\overline{OE}$ low), then $\overline{WE}$ will return the outputs to high impedance within t_{WEZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-In must remain valid t_{DH} after the rising edge of $\overline{CE}$ or $\overline{WE}$.

Figure 4 : Write–write–write–read Timing.



AC ELECTRICAL CHARACTERISTICS (write cycle timing)

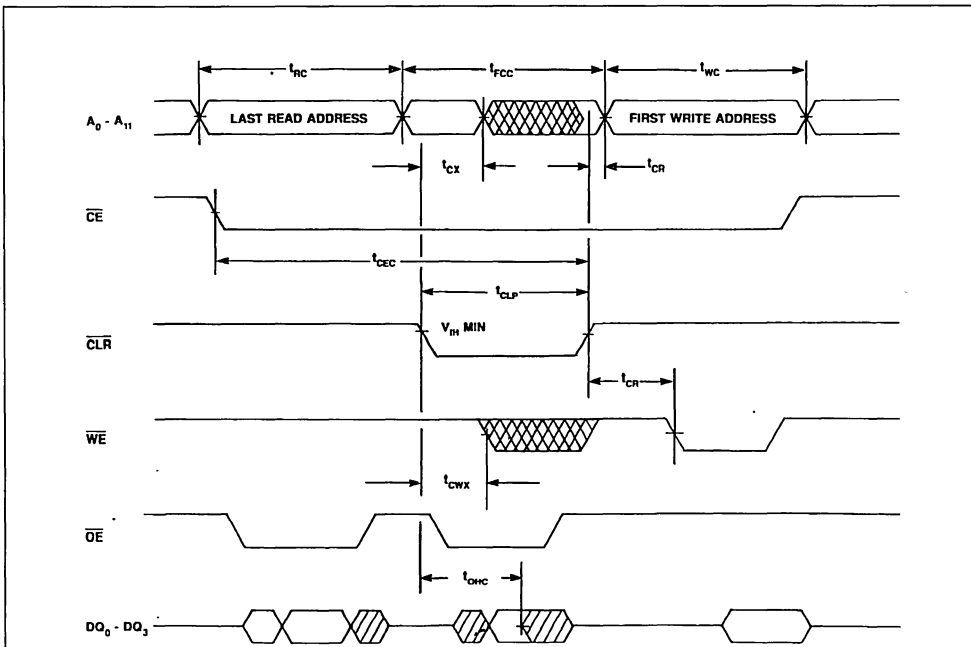
($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10$ percent)

Symbol	Parameter	MK41H7X-20		MK41H7X-25		MK41H7X-35		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	20		25		35		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AW}	Address Stable to End of Write	16		20		30		ns	
t_{AH}	Address Hold after End of Write	0		0		0		ns	
t_{CEW}	Chip Enable to End of Write	18		22		32		ns	
t_{WEW}	Write Enable to End of Write	16		20		30		ns	
t_{DS}	Data Setup Time	12		14		15		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WEL}	Write Enable to Low-Z	5		5		5		ns	2

FLASH CLEAR

A Flash Clear cycle sets all 16,384 bits in the RAM to logic zero. A Clear begins at the concurrence of a low on Chip Enable ($\overline{CE}$) and Flash Clear ($\overline{CLR}$). A Clear may be ended by a high on either $\overline{CE}$ or $\overline{CLR}$. A low on $\overline{CLR}$ has no effect if the device is disabled ($\overline{CE}$ high). A Clear may be executed within either a Read or a Write cycle. Figure 4 illustrates a Clear within a Read cycle. Clears within Write cycles are constrained only in that Write timing parameters must be observed as soon as the Flash Clear pin returns high.

Figure 5 : Last Read–flash Clear–first Write (MK41H79 only).



CAUTION : Application of transient levels below VIH minimum on the $\overline{CLR}$ input during normal operation may result in partial flash clear.

AC ELECTRICAL CHARACTERISTICS (clear cycle timing)

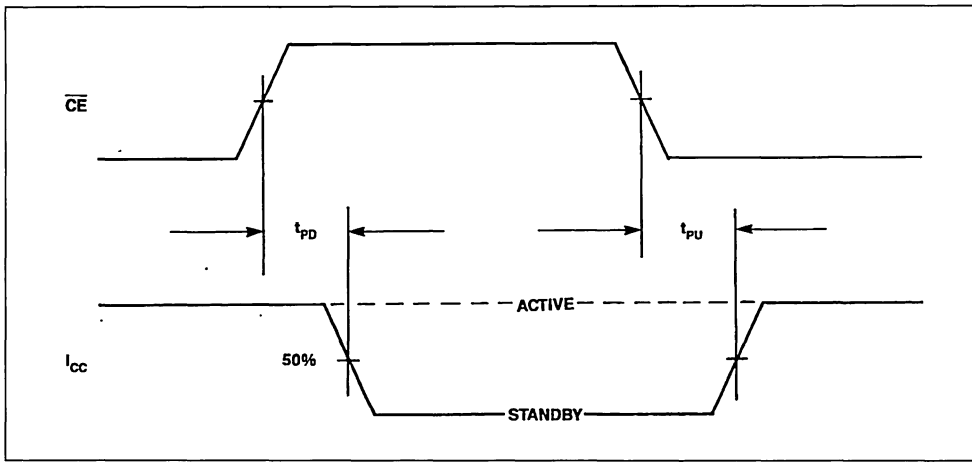
($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0 \pm 10\%$)

Symbol	Parameter	MK41H7X-20		MK41H7X-25		MK41H7X-35		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{FCC}	Flash Clear Cycle Time	40		50		70		ns	
t_{CEC}	Chip Enable Low to End of Clear	40		50		70		ns	
T_{CLP}	Flash Clear Low to End of Clear	38		48		68		ns	
t_{CX}	Clear to Inputs Don't Care	0		0		0		ns	
t_{CR}	End of Clear to Inputs Recognized	0		0		0		ns	
t_{CWX}	Clear to Write Enable Don't Care	0		0		0		ns	
t_{OHC}	Valid Data Out Hold from Clear	5		5		5		ns	1

STANDBY MODE

The MK41H78/79 is in Standby Mode whenever $\overline{CE}$ is held at or above V_{IH}.

Figure 6 : Standby Mode.



AC ELECTRICAL CHARACTERISTICS (standby mode)

($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10$ percent)

Symbol	Parameter	MK41H7X-20		MK41H7X-25		MK41H7X-35		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PD}	Chip Enable High to Power Down		20		25		35	ns	
t_{PU}	Chip Enable Low to Power up	0		0		0		ns	

APPLICATION

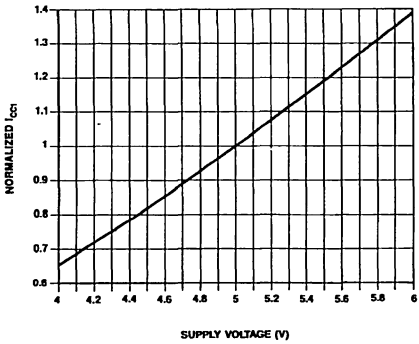
The MK41H78/79 operates from a 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the 41H79 can also interface to 5 volt CMOS on all inputs and outputs. Refer to the normalized performance curves that follow.

Since very high frequency current transients will be associated with the operation of the MK41H79, power line inductance must be minimized on the circuit board power distribution network. Power and ground tracegridding or separate power planes can be employed to reduce line inductance. Additionally, a high frequency decoupling capacitor should be placed next to each RAM. The capacitor should be 0.1µF or larger. A pull-up resistor is also recommended for CLR on the MK41H79. This will ensure that any low going system noise, coupled onto the input, does not drive CLR below V_{IH} minimum specifications.

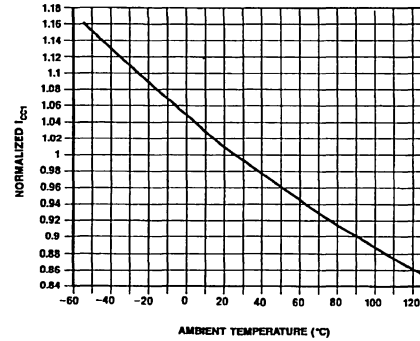
Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33Ω often prove most suitable.

NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

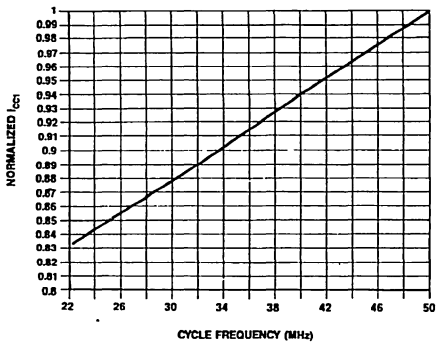
NORMALIZED SUPPLY CURRENT VS.
SUPPLY VOLTAGE T_A=0°C



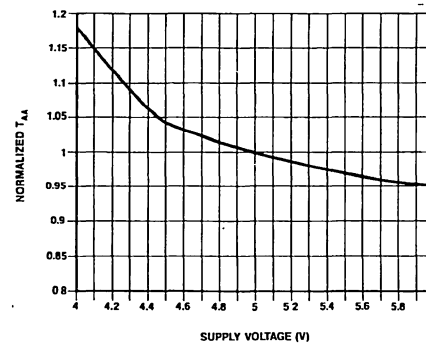
NORMALIZED SUPPLY CURRENT VS.
AMBIENT TEMPERATURE V_{CC}=5.0V



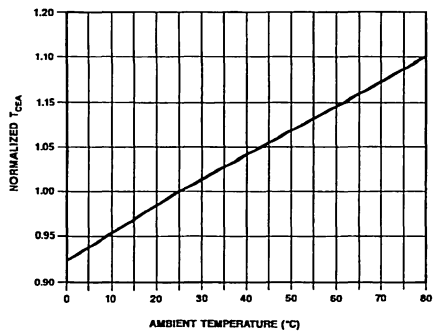
NORMALIZED SUPPLY CURRENT VS.
CYCLE TIME V_{CC}=5.0V T_A=25°C



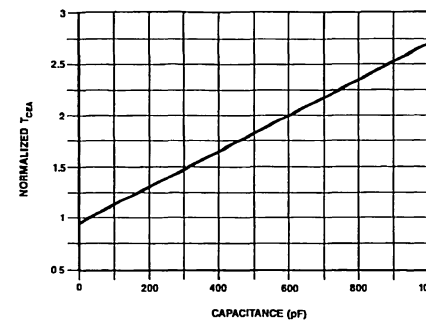
NORMALIZED ACCESS TIME VS.
SUPPLY VOLTAGE T_A=25°C



NORMALIZED ACCESS TIME VS.
AMBIENT TEMPERATURE V_{CC}=5.0V

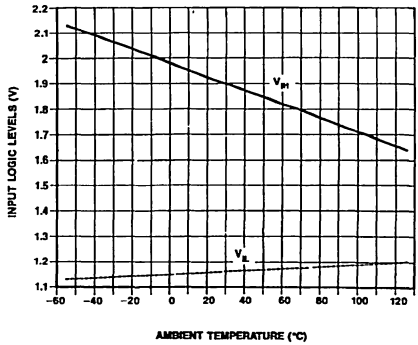


NORMALIZED ACCESS TIME VS.
OUTPUT LOADING V_{CC}=5.0V T_A=25°C

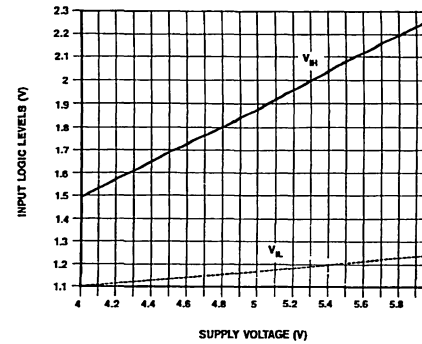


NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

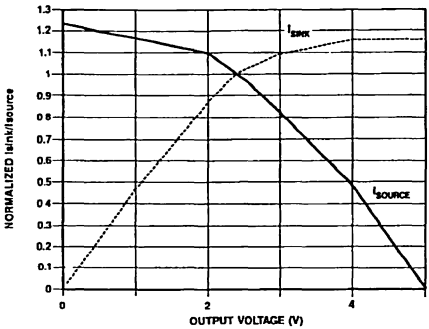
LOGIC THRESHOLD VOLTAGE VS.
AMBIENT TEMPERATURE V_{CC}=5.0V



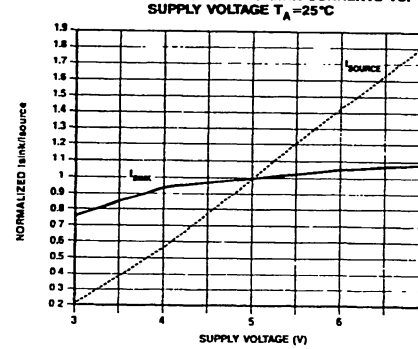
LOGIC THRESHOLD VOLTAGE VS.
SUPPLY VOLTAGE T_A=25°C



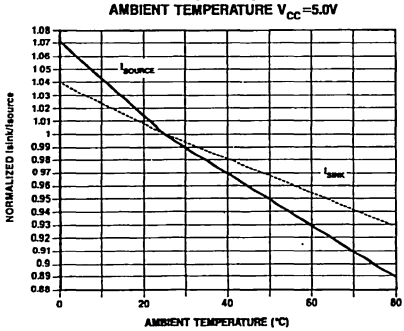
NORMALIZED SOURCE AND SINK CURRENTS VS.
OUTPUT VOLTAGE V_{CC}=5.0V T_A=25°C

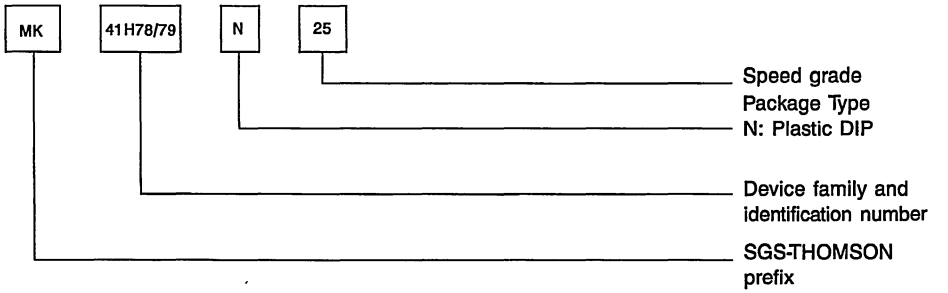


NORMALIZED SOURCE AND SINK CURRENTS VS.
SUPPLY VOLTAGE T_A=25°C



NORMALIZED SOURCE AND SINK CURRENTS VS.
AMBIENT TEMPERATURE V_{CC}=5.0V



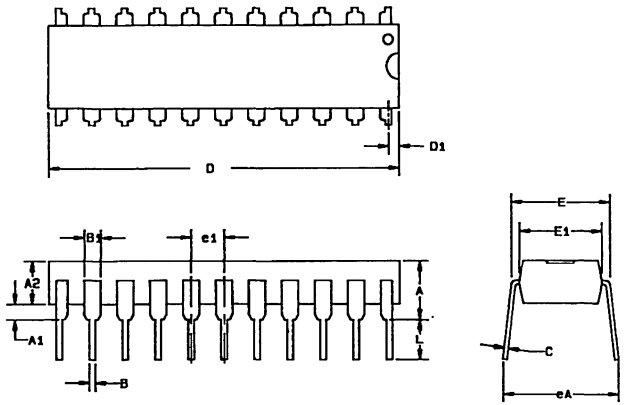


ORDER CODES

Part Number	Access Time	Package Type	Temperature Range
MK41H78N-20	20ns	22 Pin Plastic DIP	0°C to 70°C
MK41H78N-25	25ns	22 Pin Plastic DIP	0°C to 70°C
MK41H78N-35	35ns	22 Pin Plastic DIP	0°C to 70°C
MK41H79N-20	20ns	22 Pin Plastic DIP	0°C to 70°C
MK41H79N-25	25ns	22 Pin Plastic DIP	0°C to 70°C
MK41H79N-35	35ns	22 Pin Plastic DIP	0°C to 70°C

PACKAGE DESCRIPTION

22 PIN "N" PACKAGE PLASTIC DIP



Dim.	mm		Inches		Notes
	Min.	Max.	Min.	Max.	
A		5.334		.210	2
A1	0.381		.015		2
A2	3.048	3.556	.120	.140	
B	0.381	0.533	.015	.021	3
B1	1.143	1.778	.045	.070	
C	0.203	0.304	.0008	.012	3
D	25.908	26.67	1.020	1.050	1
D1	0.254	0.635	.010	.025	
E	7.62	8.255	.300	.325	
E1	6.096	6.858	.240	.270	
e1	2.286	2.794	.090	.110	
eA	7.62	9.271	.300	.365	
L	3.175		.125		

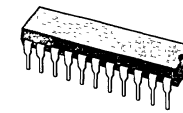
Notes : 1. Overall length includes 010 in flash on either end of the package.
2. Package standoff to be measured per jedec requirements.
3. The maximum limit shall be increased by 003 in when solder lead finish is specified.

SGS-THOMSON MICROELECTRONICS

MK41H80(N) -20/22/25/35

4K x 4 CMOS TAGRAM™

- 4K x 4 SRAM WITH ONBOARD 4 BIT COMPARATOR
- 20, 22, 25, AND 35ns ADDRESS TO COMPARE ACCESS TIME
- EQUAL ACCESS, READ AND WRITE CYCLE TIMES
- FLASH CLEAR FUNCTION
- 22-PIN, 300 MIL PLASTIC



N
DIP–22
(Plastic Package)

Figure 1 : Pin Connections.

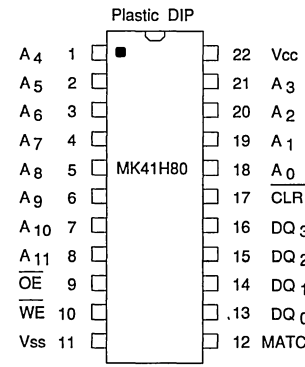
DESCRIPTION

The MK41H80 is a member of SGS-THOMSON Microelectronics 4K x 4 CMOS Static RAM family featuring fully static operation requiring no external clocks or timing strobes. Cycle Time and Compare Access Time are equal. The MK41H80 is powered by a single + 5V ± 10% power supply and the inputs and outputs are fully TTL compatible.

The MK41H80 features an onboard 4 bit comparator that compares RAM contents and current input data. The result is an active high match on the MATCH pin or an active low miss on the MATCH pin. The MATCH pins of several MK41H80's can be nanded together to provide enabling or acknowledging signals to the data cache or processor.

Tag data can be read from the data pins by bringing Output Enable ($\overline{OE}$) low. This will allow data stored in the memory array to be displayed at the Outputs (DQ_0-DQ_3).

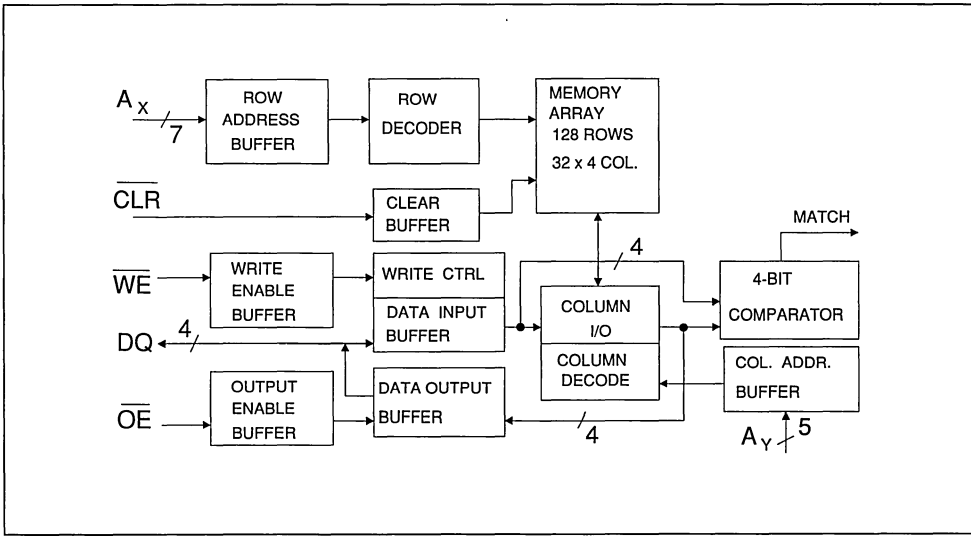
Flash Clear operation is provided on the MK41H80 via the ($\overline{CLR}$) pin. A low applied to the $\overline{CLR}$ pin clears all RAM bits to a logic zero.



PIN NAMES

A_0 - A_{11}	Address Inputs
DQ_0 - DQ_3	Data Input/output
MATCH	Comparator Output
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CLR}$	Flash Clear
V_{CC}	Power (+ 5V)
V_{SS}	Ground

Figure 2 : MK41H80 Block Diagram.



ABSOLUTE MAXIMUM RATINGS*

Parameter	Value	Unit
Voltage on any Terminal Relative to V_{SS}	- 1.0 to + 7.0	V
Operating Temperture T_A (ambient)	0 to + 70	°C
Storage Temperature (ceramic)	- 65 to + 150	°C
Storage Temperature (plastic)	- 55 to +125	°C
Power Dissipation	1	W
Output Currrent per Pin	50	mA

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sectionsof this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time

TRUTH TABLE (MK41H80)

$\overline{WE}$	$\overline{OE}$	$\overline{CLR}$	Match	Mode
H	H	H	Valid	Compare Cycle
L	X	H	Invalid	Write Cycle
H	L	H	Invalid	Read Cycle
X	X	L	Invalid	Flash Clear Cycle

X = Don't Care

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{CC}	Supply Voltage (referenced to V_{SS})	4.5	5.0	5.5	V	
V_{SS}	Ground	0.0	0.0	0.0	V	
V_{IH}	Input High (logic 1) Voltage, All Inputs (referenced to V_{SS})	2.2		V_{CC} + 0.3	V	
V_{IL}	Input Low (logic 0) Voltage, All Inputs (referenced to V_{SS})	- 0.3		0.8	V	

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0V ±10%)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
I_{CC1}	Operating Current - Average Power Supply Operating Current			120	mA	1
I'_{IL}	Input Leakage Current, Any Input	- 1		1	µA	5
I_{OL}	Output Leakage Current	- 10		10	µA	6
V_{OH}	Output High (logic 1) Voltage Referenced to V_{SS} ; I_{OH} = - 4mA	2.4			V	
V_{OL}	Output Low (logic 0) Voltage Referenced to V_{SS} ; I_{OL} = + 8mA			0.4	V	

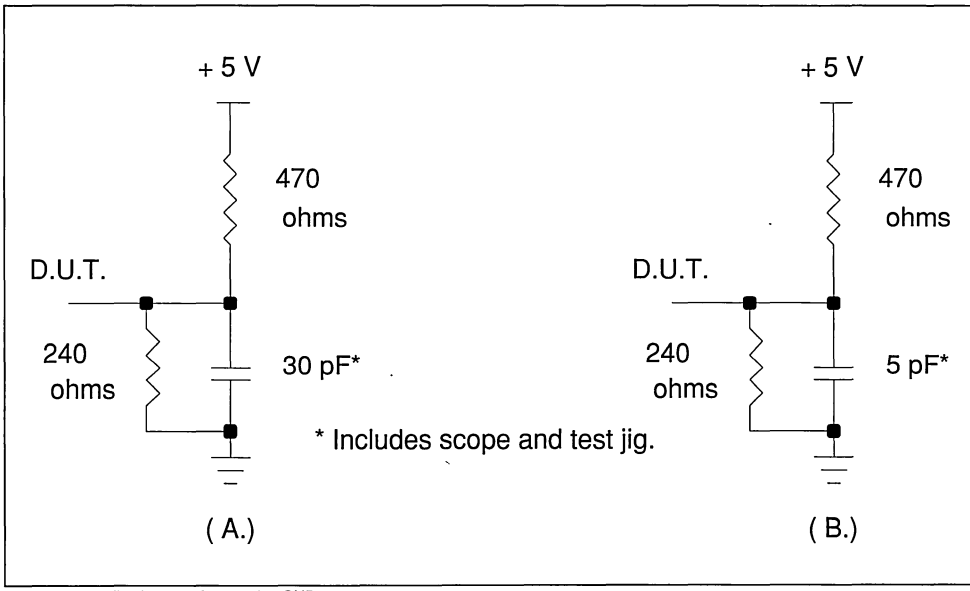
AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
C_1	Capacitance on any Input Pin		4	5	pF	2
C_2	Capacitance on any Output Pin		8	10	pF	2

AC TEST CONDITIONS

Input Levels ..... GND to 3.0V
Transition Times 5ns
Input and Output Signal Timing Reference Level 1.5V
Ambient Temperature ..... 0°C to 70°C
V_{CC} ..... 5.0V ± 10 percent

Figure 3 : Output Load Circuits.



Notes : 1. All voltages referenced to GND.
2. Measured with GND ≤ V ≤ V_{CC}. Outputs are deselected with exception to MATCH which is always enabled.
3. Measured with load as shown in Figure 3A.
4. Measured with load as shown in Figure 3B.
5. I_{CC1} measured with outputs open, V_{CC} max, f = min. cycle.
6. Output buffer is deselected.
7. Capacitances are sampled, and not 100% tested.

COMPARE, WRITE AND READ TIMING

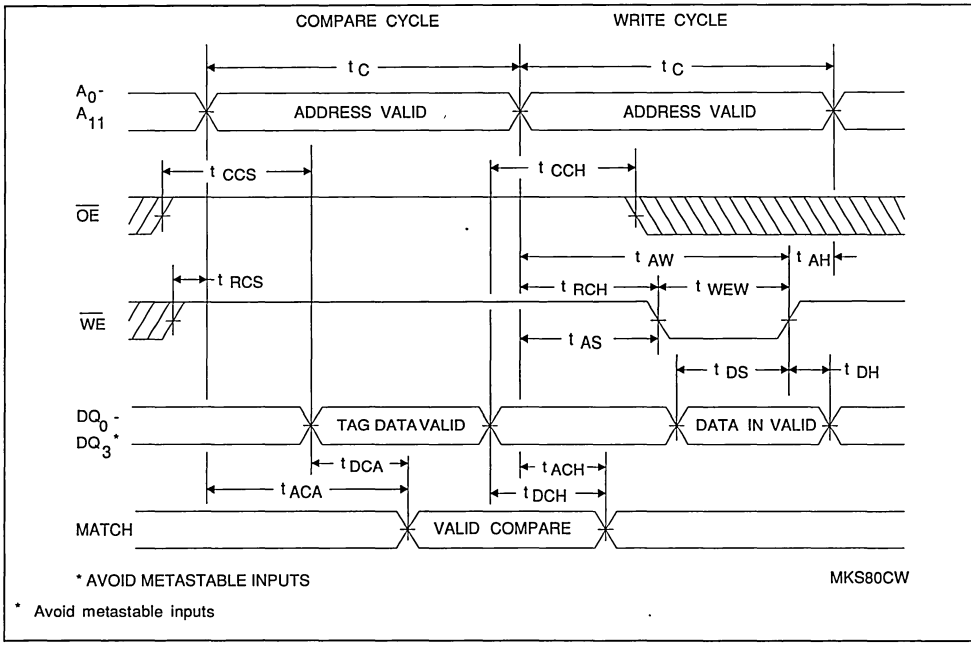
The MK41H80 employs three signals for device control. The Write Enable ($\overline{WE}$) pin enables a Write Cycle if low and either a Compare Cycle or a Read Cycle when high. The $\overline{OE}$ pin enables a Read Cycle if low or a Compare Cycle if high. The $\overline{CLR}$ pin enables a Flash Clear Cycle when brought low.

The MK41H80 begins a Compare Cycle with the application of a valid address (see figure 4). A valid MATCH is enabled when $\overline{OE}$ and $\overline{WE}$ go high in conjunction with their respective Set Up and Hold times. MATCH will occur t_{ACA} after a valid address, and t_{DCA} after valid Data In. MATCH will then go invalid t_{ACH} after the address changes.

The MK41H80 starts a Write Cycle with stable addresses (see figure 4). $\overline{OE}$ may be in either logic state. $\overline{WE}$ may fall with stable addresses, and must remain low until t_{AW} with a duration of t_{WEW}. Data in must be held valid t_{DS} before and t_{DH} after $\overline{WE}$ goes high. MATCH will be invalid during this cycle.

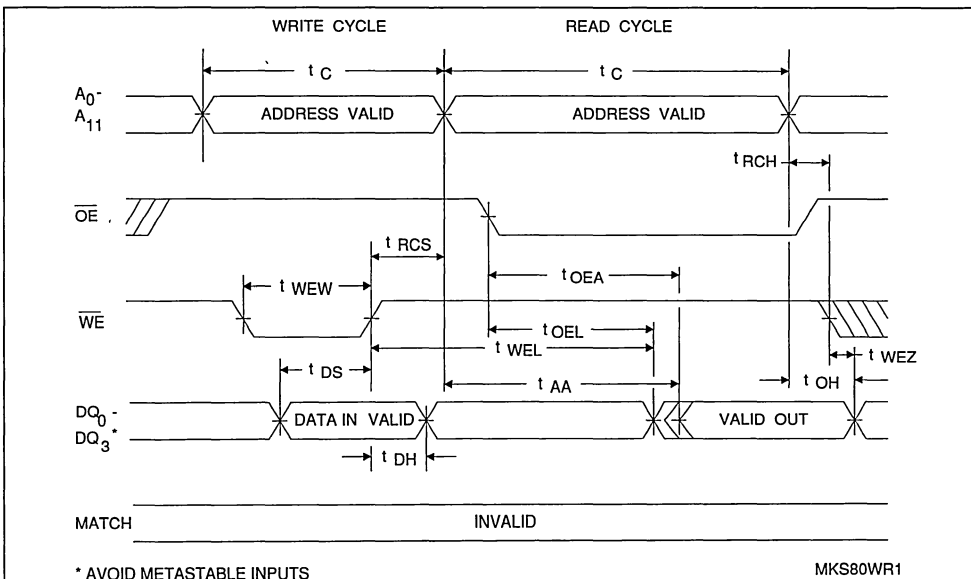
The MK41H80 begins a Read Cycle with stable addresses and $\overline{WE}$ high (see figure 4). DQ becomes valid t_{AA} after a valid address, and t_{OEA} after the fall of $\overline{OE}$. DQ outputs become invalid t_{OH} after the address becomes invalid or t_{OEZ} after OE is brought high. Ripple through data access may be accomplished by holding $\overline{OE}$ active low while strobing addresses A_0-A_{11}, and holding $\overline{CLR}$ and $\overline{WE}$ high. The MATCH output will be invalid during the Read cycle.

Figure 4 : Compare and Write Cycle.



* Avoid metastable inputs

Figure 5 : Write and Read Cycle.



* Avoid metastable inputs

ELECTRICAL CARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$) Units = ns

Symbol	Parameter	- 20		- 22		- 25		- 35		Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_C	Cycle Time	20		25		25		35		
t_{CCS}	Compare Command Set Up Time	7		8		8		10		
t_{CCH}	Compare Command Hold Time	0		0		0		0		
t_{RCS}	Read Command ($\overline{WE}$) Set Up Time	0		0		0		0		
t_{RCH}	Read Command ($\overline{WE}$) Hold Time	0		0		0		0		
t_{AS}	Address Set-up Time	0		0		0		0		
t_{AW}	Address Stable to End of Write Command ($\overline{WE}$)	16		18		20		30		
t_{AH}	Address Hold Time after End of Write	0		0		0		0		
t_{WEW}	Write Command ($\overline{WE}$) to End of Write	16		18		20		30		
t_{DS}	Data Set Up Time	12		13		13		14		
t_{DH}	Data Hold Time	0		0		0		0		
t_{DCA}	Data Compare Access Time		12		15		15		20	3
t_{ACA}	Address Compare Access Time		20		22		25		35	3
t_{ACH}	Address Compare Hold Time	5		5		5		5		3
t_{DCH}	Data Compare Hold Time	3		3		3		3		3
t_{OEA}	Output Enable ($\overline{OE}$) Access Time		10		10		12		15	3
t_{OH}	Valid Data Out ($\overline{DQ}$) Hold Time	5		5		5		5		3
t_{AA}	Address Access Time		20		22		25		35	3
t_{OEZ}	Output Enable ($\overline{OE}$) to High-Z		7		8		8		10	4
t_{OEL}	Output Enable ($\overline{OE}$) to Low-Z	2		2		2		2		4
t_{WEZ}	Write Enable ($\overline{WE}$) to High-Z		8		10		10		13	4
t_{WEL}	Write Enable ($\overline{WE}$) to Low-Z	5		5		5		5		4

APPLICATION

The MK41H80 operates from a 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the MK41H80 can also interface to 5 volt CMOS on all inputs and outputs. Refer to the normalized performance curves that follow.

The MK41H80 compares contents of addressed RAM locations to the current data inputs. A logic one (1) output on the MATCH pin indicates that the input data and the RAM contents match. Conversely, a logic zero (0) on the MATCH pin indicates at least one bit difference between the RAM contents and input data generating a miss.

The MATCH output is always at either an active high or low logic level, and does not exhibit a three-state or high impedance characteristic. Since the comparator circuitry is always enabled, metastable data input levels can result in excessive MATCH output activity. Therefore, the use of pull-up or pull-down resistors is recommended on the data bus.

A pull-up resistor is also recommended for the $\overline{CLR}$ input. This will ensure that any low going system noise, coupled onto the input, does not drive $\overline{CLR}$ below V_{IH} minimum specifications.

Because high frequency current transients will be associated with the operation of the MK41H80, power lines inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance.

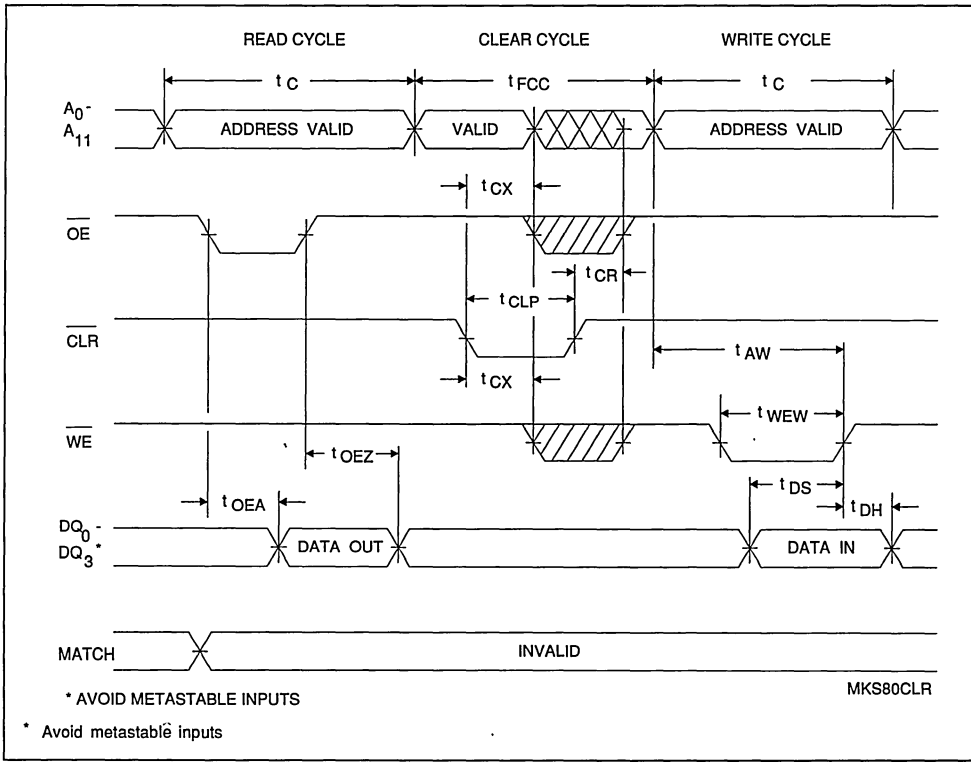
Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve

driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

FLASH CLEAR CYCLE

A Flash Clear Cycle begins as $\overline{CLR}$ is brought low (see figure 5). A Flash Clear sets all 16,384 bits in the RAM to logic zero. Control Inputs will not be recognized from t_{CX} after $\overline{CLR}$ falls to t_{CR} after $\overline{CLR}$ is brought high. $\overline{OE}$ and $\overline{WE}$ are Don't Cares and DQ is High-Z. MATCH will be invalid while $\overline{CLR}$ is low.

Figure 6 : Read–flash Clear–write Cycle.



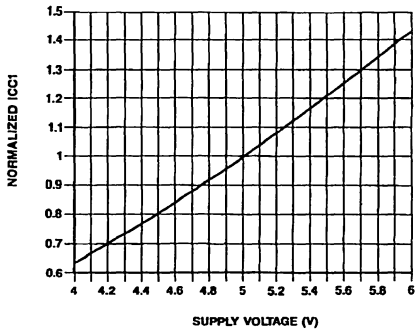
AC ELECTRICAL CARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$) ($V_{CC} = 5.0V \pm 10\%$) Units = ns.

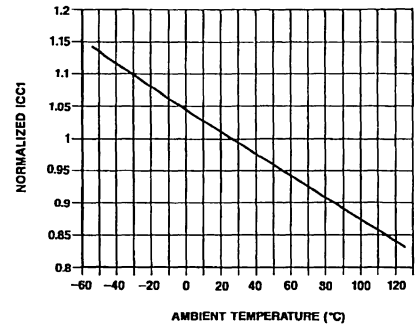
Symbol	Parameter	- 20		- 22		- 25		- 35		Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{FCC}	Flash Clear Cycle Time	40		50		50		70		
t_{CX}	Clear ($\overline{CLR}$) to Inputs Don't Care	0		0		0		0		
t_{CR}	End of Clear ($\overline{CLR}$) to Inputs Recognized	0		0		0		0		
t_{CLP}	Flash Clear ($\overline{CLR}$) Pulse Width	36		36		60		60		

NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

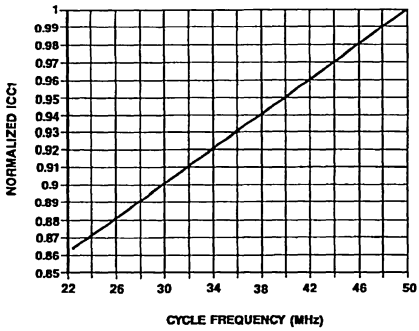
NORMALIZED SUPPLY CURRENT VS.
SUPPLY VOLTAGE T_A = 0°C



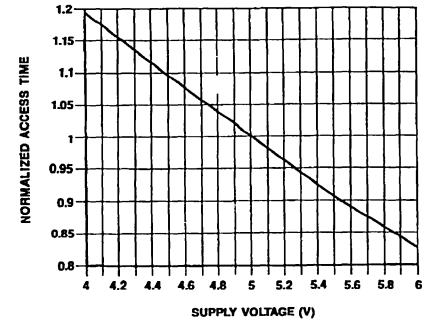
NORMALIZED SUPPLY CURRENT VS.
AMBIENT TEMPERATURE V_{CC} = 5.0V



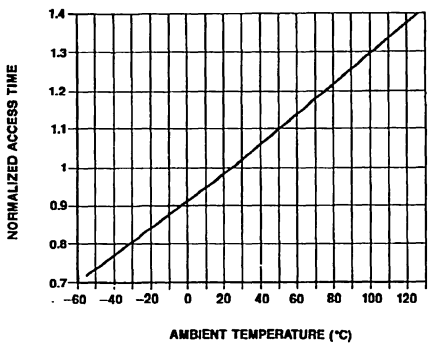
NORMALIZED SUPPLY CURRENT VS.
CYCLE TIME V_{CC} = 5.0V T_A = 25°C



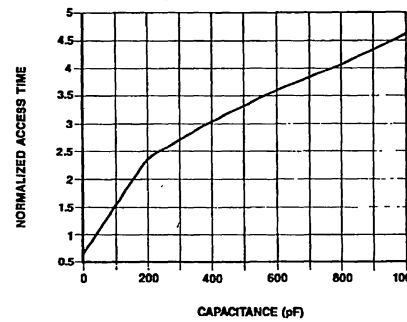
NORMALIZED ACCESS TIME VS.
SUPPLY VOLTAGE T_A = 25°C



NORMALIZED ACCESS TIME VS.
AMBIENT TEMPERATURE V_{CC} = 5.0V

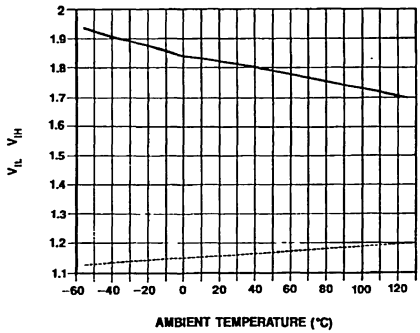


NORMALIZED ACCESS TIME VS.
OUTPUT LOADING V_{CC} = 5.0V T_A = 25°C

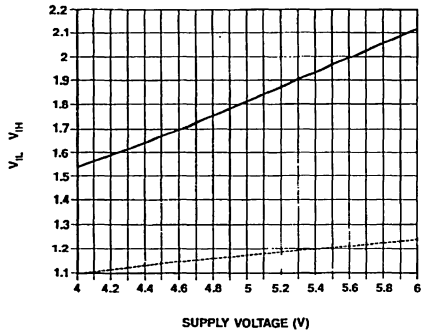


NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

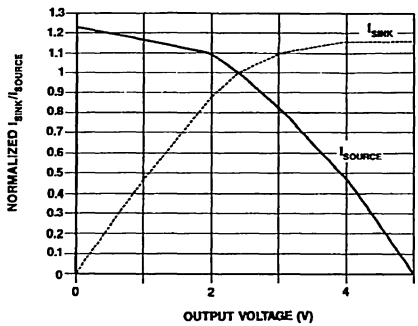
LOGIC THRESHOLD VOLTAGE VS.
AMBIENT TEMPERATURE V_{CC} = 5.0V



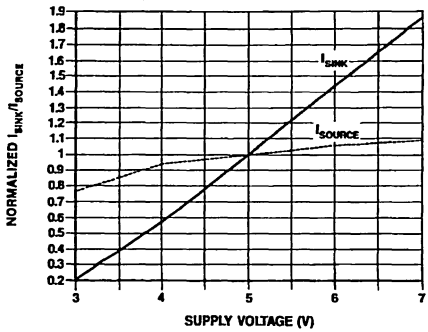
LOGIC THRESHOLD VOLTAGE VS.
SUPPLY VOLTAGE T_A = 25°C



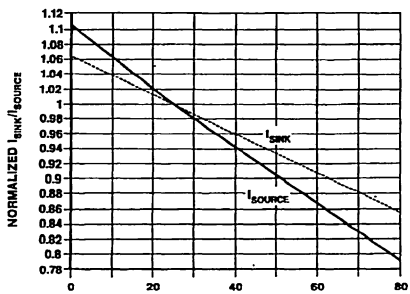
NORMALIZED SOURCE AND SINK CURRENTS VS.
OUTPUT VOLTAGE V_{CC} = 5.0V, T_A = 25°C

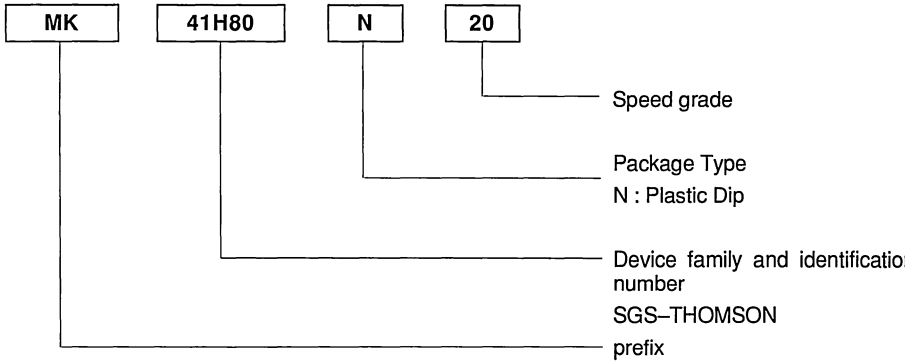


NORMALIZED SOURCE AND SINK CURRENTS VS.
SUPPLY VOLTAGE T_A = 25°C



NORMALIZED SOURCE AND SINK CURRENTS VS.
AMBIENT TEMPERATURE V_{CC} = 5.0V



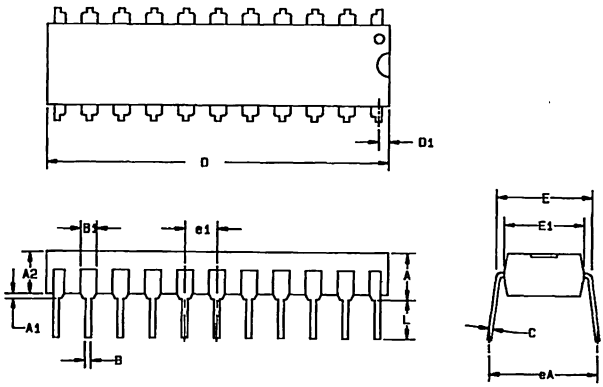


ORDER CODES

Part Number	Access Time	Package Type	Temperature Range
MK41H80N-20	20ns	22 Pin Plastic DIP	0°C to 70°C
MK41H80N-22	22ns	22 Pin Plastic DIP	0°C to 70°C
MK41H80N-25	25ns	22 Pin Plastic DIP	0°C to 70°C
MK41H80N-35	35ns	22 Pin Plastic DIP	0°C to 70°C

PACKAGE DESCRIPTION

22 PIN "N" PACKAGE PLASTIC DIP



Dim.	mm		Inches		Notes
	Min.	Max.	Min.	Max.	
A		5.334		.210	2
A1	0.381		.015		2
A2	3.048	3.556	.120	.140	
B	0.381	0.533	.015	.021	3
B1	1.27	1.778	.050	.070	
C	0.203	0.304	.0008	.012	3
D	25.908	26.67	1.020	1.050	1
D1	0.254	0.635	.010	.025	
E	7.62	8.255	.300	.325	
E1	6.096	6.858	.240	.270	
e1	2.286	2.794	.090	.110	
eA	7.62	10.16	.300	.400	
L	3.048		.120		

Notes : 1. Overall length includes 010 in flash on either end of the package.
2. Package standoff to be measured per jedec requirements.
3. The maximum limit shall be increased by 003 in when solder lead finish is specified.

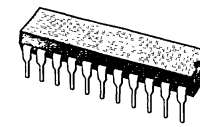
SGS-THOMSON MICROELECTRONICS

MK41S80(N,X) -12/15

4K x 4 CMOS TAGRAM™

ADVANCED DATA

- 4K x 4 FAST HCMOS CACHE TAGRAM
- 12,15ns ADDRESS TO COMPARE ACCESS
- EQUAL ACCESS, READ/WRITE CYCLE TIMES
- FLASH CLEAR FUNCTION
- 22-PIN 300 MIL PLASTIC DIP
  24-PIN 300 MIL SOJ



22-Pin
(300 MIL Plastic Dip)

DESCRIPTION

The MK41S80 is a member of SGS-THOMSON Microelectronics 4K x 4 CMOS Static RAM family featuring fully static operation requiring no external clocks or timing strobes. Cycle Time and Compare Access Time are equal. The MK41S80 is powered by a single + 5V ± 10% power supply and the inputs and outputs are fully TTL compatible.

The MK41S80 features an onboard 4 bit comparator that compares RAM contents and current input data. The result is an active high match on the MATCH pin or an active low miss on the MATCH pin. The MATCH pins of several MK41S80's can be nanded together to provide enabling or acknowledging signals to the data cache or processor.

Tag data can be read from the data pins by bringing Output Enable ($\overline{OE}$) low. This will allow data stored in the memory array to be displayed at the Outputs (DQ_0-DQ_3).

Flash Clear operation is provided on the MK41S80 via the ($\overline{CLR}$) pin. A low applied to the $\overline{CLR}$ pin clears all RAM bits to a logic zero.

PIN NAMES

A_0 - A_{11}	Address Inputs
DQ_0 - DQ_3	Data I/O_{0-3}
MATCH	Comparator Output
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{CLR}$	RAM Flash Clear
V_{CC}, V_{SS}	+ 5V, GND

Figure 1 : Pin Connections.

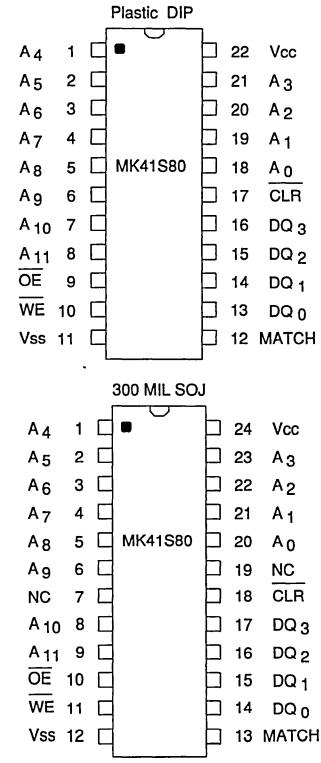
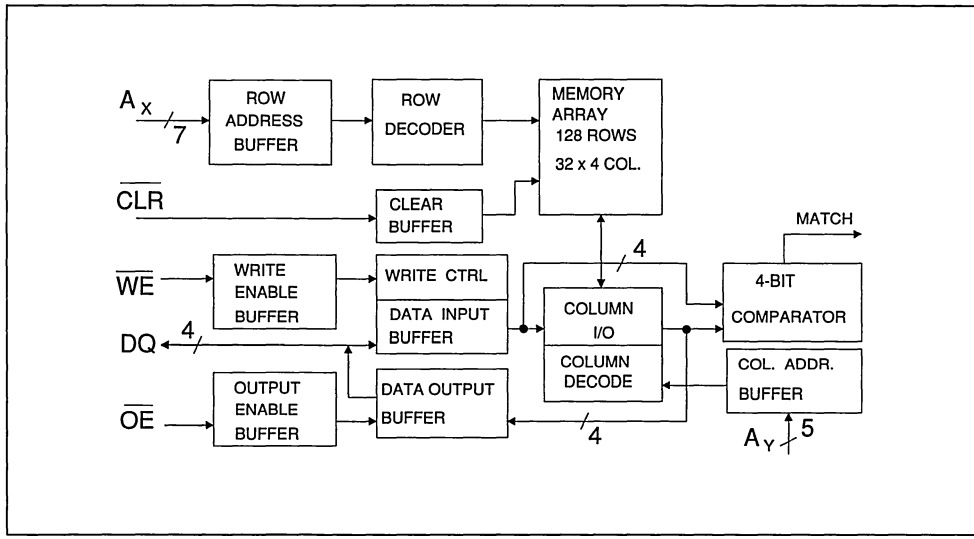


Figure 2 : MK41S80 Block Diagram.



ABSOLUTE MAXIMUM RATINGS*

Parameter	Value	Unit
Voltage on any Pin Relative to Ground	– 0.3 to 7.0	V
Operating Temperature	0 to 70	°C
Storage Temperature	– 55 to + 125	°C
Power Dissipation	1	W
Output Current	50	mA

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sectionsof this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time

TRUTH TABLE (MK41S80)

$\overline{WE}$	$\overline{OE}$	$\overline{CLR}$	Match	Mode
H	H	H	Valid	Compare Cycle
L	X	H	Invalid	Write Cycle
H	L	H	Invalid	Read Cycle
X	X	L	Invalid	Flash Clear Cycle

X = Don't Care

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{CC}	Supply Voltage	4.5	5.5	V	1
V_{SS}	Supply Voltage, GND	0	0	V	1
V_{IH}	Logic 1 All Inputs	2.2	V_{CC} + 0.3	V	1
V_{IL}	logic 0 All Inputs	- 0.3	0.8	V	1

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Min.	Max.	Unit	Notes
I_{CC1}	Average Vcc Power Supply Current		120	mA	
I'_{IL}	Input Leakage Current, (Any Input)	- 1	1	µA	2
I_{OL}	Output Leakage Current	- 10	10	µA	2
V_{OH}	Output logic 1 Voltage (I_{OUT} = - 4.0mA)	2.4		V	1
V_{OL}	Output logic 0 Voltage (I_{OUT} = 8.0mA)		0.4	V	1

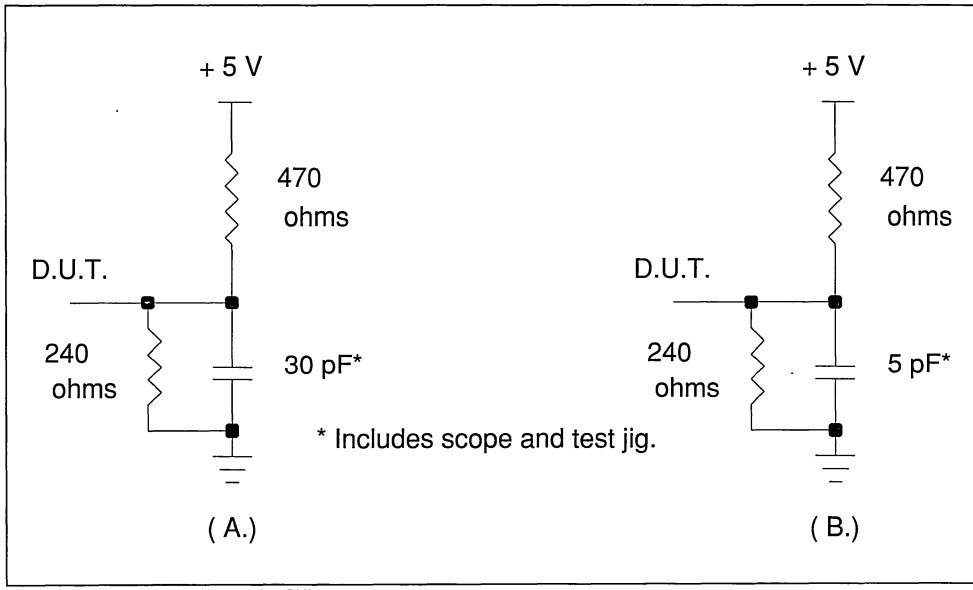
AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
C_1	Capacitance on any Input Pin		4	5	pF	2
C_2	Capacitance on any Output Pin		8	10	pF	2

AC TEST CONDITIONS

Input Levels ..... GND to 3.0V
Transition Times 1.5ns
Input and Output Signal Timing Reference Level 1.5V
Ambient Temperature ..... 0°C to 70°C
Vcc ..... 5.0V ± 10 percent

Figure 3 : Output Load Circuits.



Notes : 1. All voltages referenced to GND.
2. Measured with GND ≤ V ≤ V_{CC}. Outputs are deselected with exception to MATCH which is always enabled.
3. Measured with load as shown in Figure 7A.
4 Measured with load as shown in Figure 7B.
5. I_{CC1} measured with outputs open, V_{CC} max, f = min. cycle.
6. Output buffer is deselected.
7. Capacitances are sampled, and not 100% tested.

COMPARE, WRITE AND READ TIMING

The MK41S80 employs three signals for device control. The Write Enable ($\overline{WE}$) pin enables a Write Cycle if low and either a Compare Cycle or a Read Cycle when high. The $\overline{OE}$ pin enables a Read Cycle if low or a Compare Cycle if high. The $\overline{CLR}$ pin enables a Flash Clear Cycle when brought low.

The MK41S80 begins a Compare Cycle with the application of a valid address (see figure 4). A valid MATCH is enabled when $\overline{OE}$ and $\overline{WE}$ go high in conjunction with their respective Set Up and Hold times. MATCH will occur t_{ACA} after a valid address, and t_{DCA} after valid Data In. MATCH will then go invalid t_{ACH} after the address changes.

The MK41S80 starts a Write Cycle with stable addresses (see figure 4). $\overline{OE}$ may be in either logic state. $\overline{WE}$ may fall with stable addresses, and must remain low until t_{AW} with a duration of t_{WEW}. Data in must be held valid t_{DS} before and t_{DH} after $\overline{WE}$ goes high. MATCH will be invalid during this cycle.

The MK41S80 begins a Read Cycle with stable addresses and $\overline{WE}$ high (see figure 4). DQ becomes valid t_{AA} after a valid address, and t_{OEA} after the fall of $\overline{OE}$. DQ outputs become invalid t_{OH} after the address becomes invalid or t_{OEZ} after OE is brought high. Ripple through data access may be accomplished by holding $\overline{OE}$ active low while strobing addresses A_0-A_{11}, and holding $\overline{CLR}$ and $\overline{WE}$ high. The MATCH output will be invalid during the Read cycle.

Figure 4 : Compare and Write Cycle.

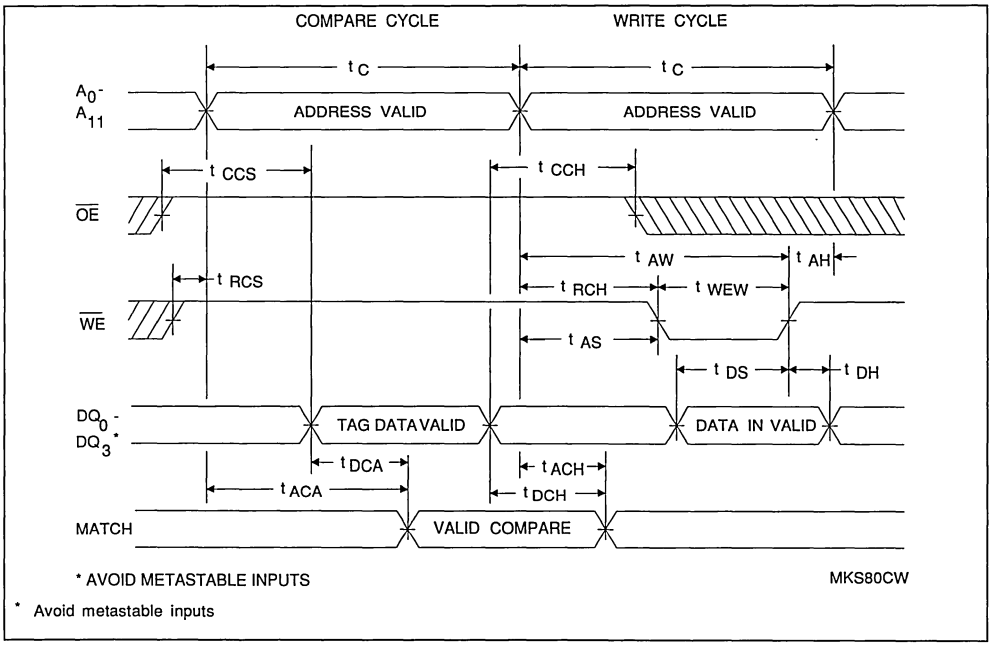
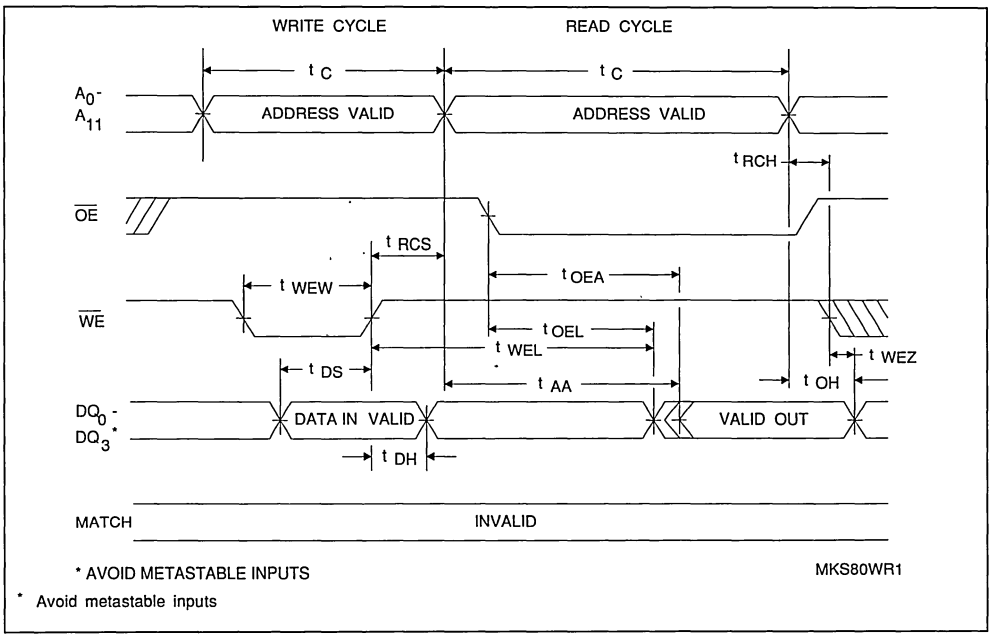


Figure 5 : Write and Read Cycle.



ELECTRICAL CARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$) Units = ns

Symbol	Parameter	- 12		- 15		Notes
		Min.	Max.	Min.	Max.	
t_C	Cycle Time	15		20		
t_{CCS}	Compare Command Set Up Time	5		6		
t_{CCH}	Compare Command Hold Time	0		0		
t_{RCS}	Read Command ($\overline{WE}$) Set Up Time	0		0		
t_{RCH}	Read Command ($\overline{WE}$) Hold Time	0		0		
t_{AS}	Address Set-up Time	0		0		
t_{AW}	Address Stable to End of Write Command ($\overline{WE}$)	10		12		
t_{AH}	Address Hold Time after End of Write	1		1		
t_{WEW}	Write Command ($\overline{WE}$) to End of Write	10		12		
t_{DS}	Data Set Up Time	10		12		
t_{DH}	Data Hold Time	0		0		
t_{DCA}	Data Compare Access Time		8		10	3
t_{ACA}	Address Compare Access Time		12		15	3
t_{ACH}	Address Compare Hold Time	2		2		3
t_{DCH}	Data Compare Hold Time	0		0		3
t_{OEA}	Output Enable ($\overline{OE}$) Access Time		8		10	3
t_{OH}	Valid Data Out ($\overline{DQ}$) Hold Time	2		2		3
t_{AA}	Address Access Time		15		20	3
t_{OEZ}	Output Enable ($\overline{OE}$) to High-Z		7		7	4
t_{OEL}	Output Enable ($\overline{OE}$) to Low-Z	0		0		4
t_{WEZ}	Write Enable ($\overline{WE}$) to High-Z		7		7	4
t_{WEL}	Write Enable ($\overline{WE}$) to Low-Z	1		1		4

APPLICATION

The MK41S80 operates from a 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the MK41S80 can also interface to 5 volt CMOS on all inputs and outputs. Refer to the normalized performance curves that follow.

The MK41S80 compares contents of addressed RAM locations to the current data inputs. A logic one (1) output on the MATCH pin indicates that the input data and the RAM contents match. Conversely, a logic zero (0) on the MATCH pin indicates at least one bit difference between the RAM contents and input data generating a miss.

The MATCH output is always at either an active high or low logic level, and does not exhibit a three-state or high impedance characteristic. Since the comparator circuitry is always enabled, metastable data input levels can result in excessive MATCH output activity. Therefore, the use of pull-up or pull-down resistors is recommended on the data bus.

A pull-up resistor is also recommended for the $\overline{CLR}$ input. This will ensure that any low going system noise, coupled onto the input, does not drive $\overline{CLR}$ below V_{IH} minimum specifications.

Because high frequency current transients will be associated with the operation of the MK41S80, power lines inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance.

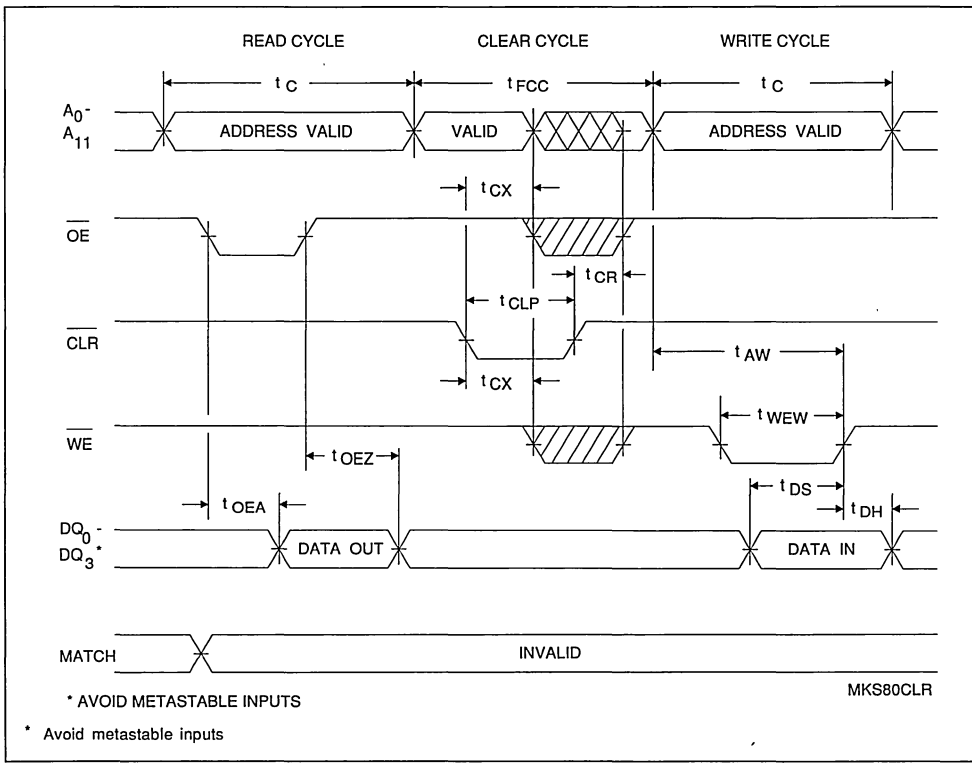
Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve

driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

FLASH CLEAR CYCLE

A Flash Clear Cycle begins as $\overline{CLR}$ is brought low (see figure 5). A Flash Clear sets all 16,384 bits in the RAM to logic zero. Control Inputs will not be recognized from t_{CX} after $\overline{CLR}$ falls to t_{CR} after $\overline{CLR}$ is brought high. $\overline{OE}$ and $\overline{WE}$ are Don't Cares and DQ is High-Z. MATCH will be invalid while $\overline{CLR}$ is low.

Figure 6 : Read–flash Clear–write Cycle.



* Avoid metastable inputs

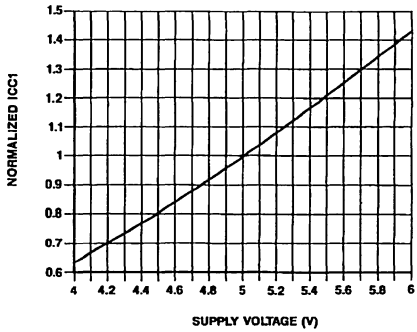
AC ELECTRICAL CARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ±10%) Units = ns.

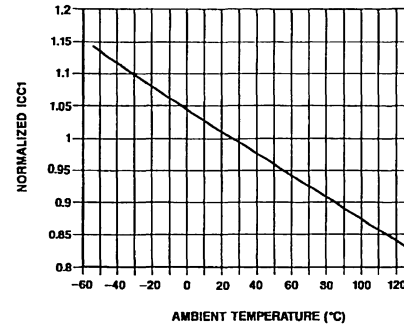
Symbol	Parameter	- 12		- 15		Notes
		Min.	Max.	Min.	Max.	
t_{FCC}	Flash Clear Cycle Time	50		50		
t_{CX}	Clear ($\overline{CLR}$) to Inputs Don't Care	0		0		
t_{CR}	End of Clear ($\overline{CLR}$) to Inputs Recognized	0		0		
t_{CLP}	Flash Clear ($\overline{CLR}$) Pulse Width	35		35		

NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

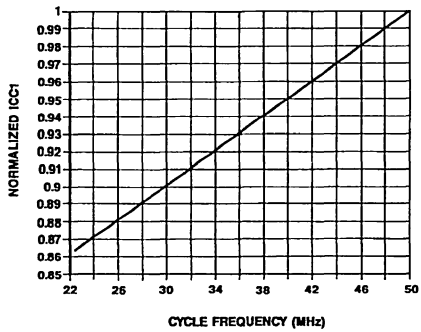
NORMALIZED SUPPLY CURRENT VS.
SUPPLY VOLTAGE T_A = 0°C



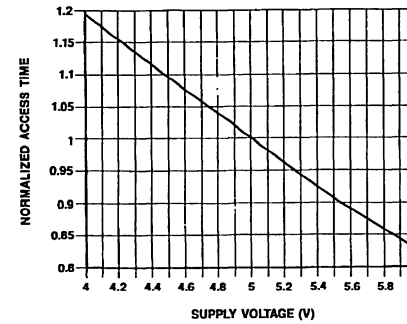
NORMALIZED SUPPLY CURRENT VS.
AMBIENT TEMPERATURE V_{CC} = 5.0V



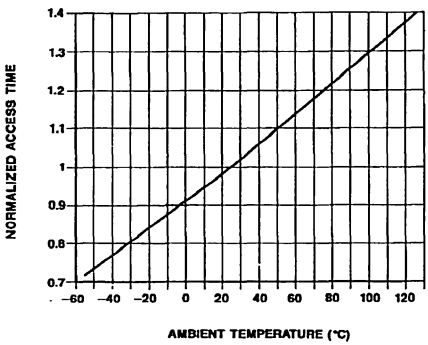
NORMALIZED SUPPLY CURRENT VS.
CYCLE TIME V_{CC} = 5.0V T_A = 25°C



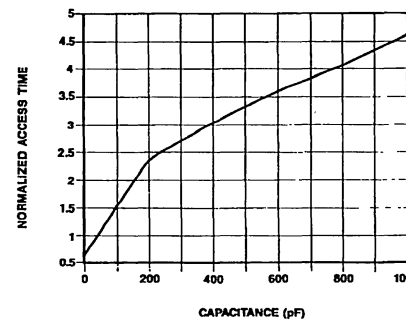
NORMALIZED ACCESS TIME VS.
SUPPLY VOLTAGE T_A = 25°C



NORMALIZED ACCESS TIME VS.
AMBIENT TEMPERATURE V_{CC} = 5.0V

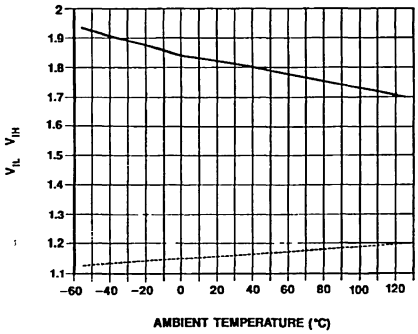


NORMALIZED ACCESS TIME VS.
OUTPUT LOADING V_{CC} = 5.0V T_A = 25°C

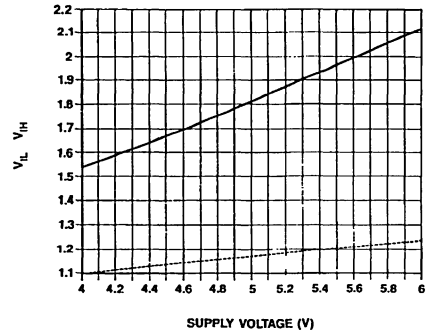


NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

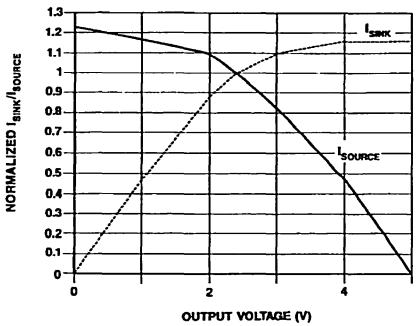
LOGIC THRESHOLD VOLTAGE VS.
AMBIENT TEMPERATURE V_{CC} = 5.0V



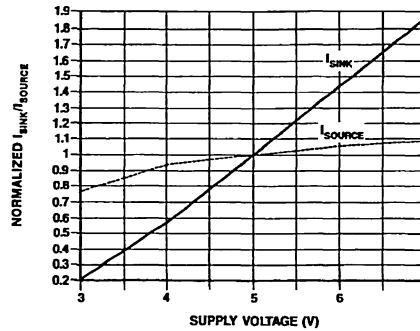
LOGIC THRESHOLD VOLTAGE VS.
SUPPLY VOLTAGE T_A = 25°C



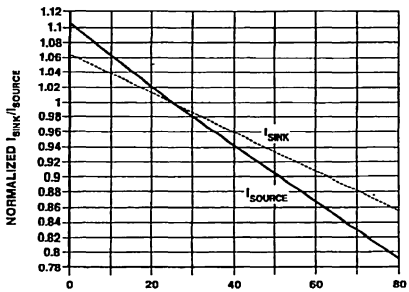
NORMALIZED SOURCE AND SINK CURRENTS VS.
OUTPUT VOLTAGE V_{CC} = 5.0V, T_A = 25°C

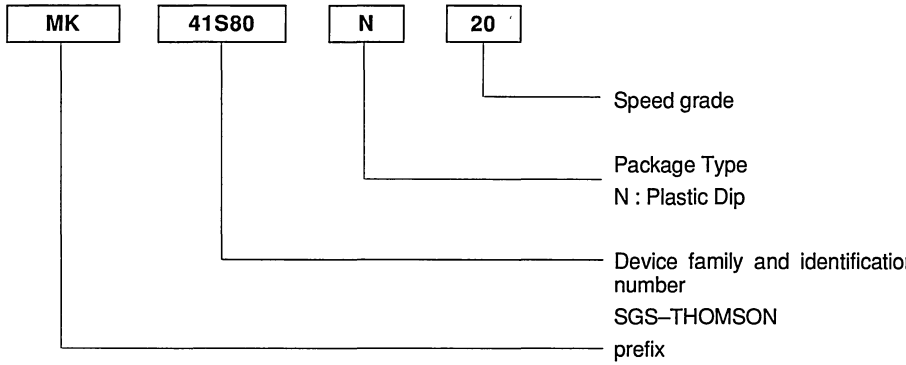


NORMALIZED SOURCE AND SINK CURRENTS VS.
SUPPLY VOLTAGE T_A = 25°C



NORMALIZED SOURCE AND SINK CURRENTS VS.
AMBIENT TEMPERATURE V_{CC} = 5.0V



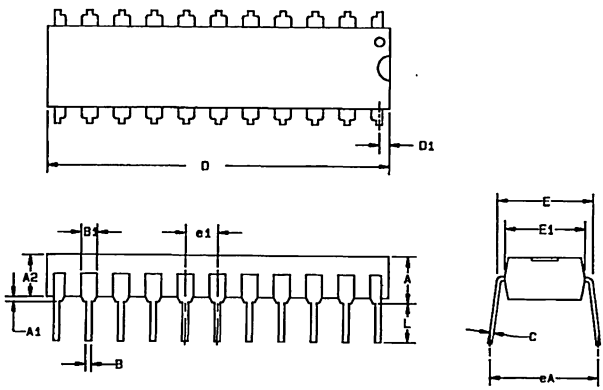


ORDER CODES

Part Number	Access Time	Package Type	Temperature Range
MK41S80N12	12ns	300 MIL Plastic DIP	0°C to 70°C
MK41S80N15	15ns	300 MIL Plastic DIP	0°C to 70°C
MK41S80X12	12ns	300 MIL Plastic SOJ	0°C to 70°C
MK41S80X15	15ns	300 MIL Plastic SOJ	0°C to 70°C

PACKAGE DESCRIPTION

22 PIN "N" PACKAGE PLASTIC DIP



Dim.	mm		Inches		Notes
	Min.	Max.	Min.	Max.	
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A1	0.381		.015		2
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B	0.381	0.533	.015	.021	3
B1	1.27	1.778	.050	.070	
C	0.203	0.304	.0008	.012	3
D	25.908	26.67	1.020	1.050	1
D1	0.254	0.635	.010	.025	
E	7.62	8.255	.300	.325	
E1	6.096	6.858	.240	.270	
e1	2.286	2.794	.090	.110	
eA	7.62	10.16	.300	.400	
L	3.048		.120		

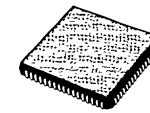
Notes : 1. Overall length includes 010 in flash on either end of the package.
2. Package standoff to be measured per jedec requirements.
3. The maximum limit shall be increased by 003 in when solder lead finish is specified.

SGS-THOMSON MICROELECTRONICS

MK4202(Q)-20/22/25

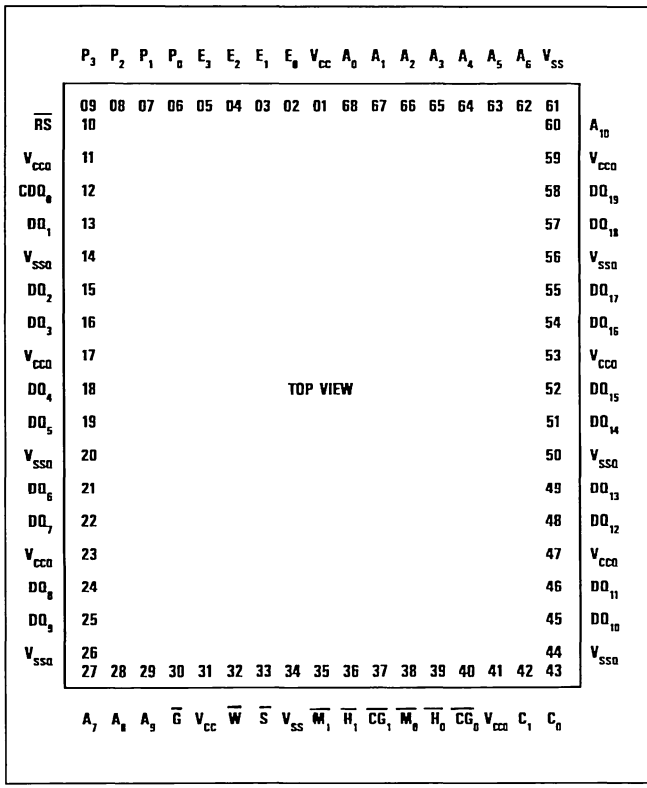
2048 x 20 CMOS TAGRAM™

- 2048 x 20 CMOS SRAM WITH ONBOARD COMPARATOR
- MATCH ACCESS TIME = 20ns (max)
- READ ACCESS TIME = 25ns (max)
- RESET CYCLE = 25ns (max)
- I_{CC} (outputs deselected) = 250mA (max)
- STANDBY = 50mA (max)
- FLASH CLEAR VALID BIT FUNCTION
- TARGET APPLICATION :
- 68020-25, 68030-33 AND 80386 CACHE



Q
PLCC68
(Plastic Chip Carrier)

Figure 1 : Pinout for 68 Pin PLCC Package.



PIN NAMES

V_{CC}, V_{SS}	+ 5V Supply, Ground
V_{CCQ}, V_{SSQ}	+ 5V Output Supply, Output Ground
A_0-A_{10}	Index Address Input
CDO_O	Clearable Tag Data I/O
DQ_1-DQ_{19}	Tag Data I/O
E_0-E_3	Chip Enable (programmable active low or high)
P_0-P_3	Chip Enable Program Inputs
$\overline{RS}$	Reset Input (active low)
$\overline{S}$	Chip Select Input (active low)
$\overline{W}$	Write Enable (active low)
$\overline{G}$	Data Output Enable (active low)
C_O	Compare 0 Output (3-state) Hit = High, Miss = Low
C_1	Compare 1 Output (3-state) Hit = High, Miss. = Low
$\overline{H_0}$	Force hit 0 Input (active low)
$\overline{H_1}$	Force hit 1 Input (active low)
$\overline{M_0}$	Force Miss 0 Input (active low)
$\overline{M_1}$	Force Miss 1 Input (active low)
$\overline{CG_0}$	Compare 0 Output Enable (active low)
$\overline{CG_1}$	Compare 1 Output Enable (active low)

DEVICE DESCRIPTION AND FEATURES

The MK4202 is designed to be connected DIRECTLY to a high performance 32 bit microprocessor, allowing the elimination of the logic delays associated with collecting HIT or Miss outputs into a subsequent gate or the RC delays associated with wired-OR open collector match outputs.
The MK4202 TAGRAM has four major features that allow direct connection :

1. Wide enough for almost any TAGRAM application without requiring multiple chip width expansion and the delays that would result.
2. Four (4) programmable CHIP ENABLE inputs, allowing DEPTH EXPANSION without any of the attendant chip enable decode delays that would otherwise be required.
   P_0-P_3 should be tied directly to V_{CC} or V_{SS}, or through pull-up or pull-down resistors. The MK4202 is selected when E_0-E_3 equals P_0-P_3 in a binary match.
   (Example : E_0-E_1 = 0110, P_0-P_3 = 0110.)
3. 3-STATE COMPARE OUTPUTS, allowing all Compare outputs to be bused together so the Address-to-Compare access time for a depth expanded application is identical to that of a single device. The Programmable Chip Enables prevent bus contention by assuring that only one TAGRAM at a time drives each Compare bus when in Compare mode.
4. DUAL COMPARE OUTPUTS (C_0 and C_1) and FORCED HIT ($\overline{H_0}$ and $\overline{H_1}$) and FORCED MISS ($\overline{M_0}$ and $\overline{M_1}$) inputs for each. The arrangement allows direct connection of the TAGRAM to two separate processor inputs (such as $\overline{BERR}$ and $\overline{HALT}$ on the 68030), and connection of all signals that would otherwise have been connected to those processor inputs to be passed THROUGH the TAGRAM ; eliminating the need for a subsequent gate to collect the COMPARE output and other $\overline{BERR}$ or $\overline{HALT}$ signal sources to the processor. The net effect is that the Address-to-Compare access time demonstrated by the MK4202 is all of the delay the user must consider. The alternative approach, using narrow TAGRAMs with open collector outputs or narrow TAGRAMs with 2-state outputs and a 10ns programmable logic device, requires that the narrow TAGRAMs demonstrate a 10ns Address-to-Compare access time to yield the same performance in a user's system that the MK4202 provides.

TRUTH TABLE (MK4202Q)

$\overline{RS}$	$\overline{S}$	E	$\overline{W}$	$\overline{G}$	$\overline{M_X}$	$\overline{H_X}$	$\overline{CG_X}$	Mode	C_X	DQ	Notes
Hi	–	X	–	–	Lo	X	X	Force Miss	Low	–	1
Hi	–	X	–	–	Hi	Lo	X	Force Hit	High	–	1
Hi	–	X	–	–	Hi	Hi	Hi	Comp Disable	Hi-Z	–	1
Hi	X	F	X	X	Hi	Hi	X	Standby	Hi-Z	Hi-Z	
Hi	X	T	Hi	Hi	Hi	Hi	Hi	Compare	Hi-Z	D in	
Hi	X	T	Hi	Hi	Hi	Hi	Lo	Compare	Hi or Lo	D in	
Hi	Hi	T	Lo	X	Hi	Hi	Lo	Hit	High	Hi-z	
Hi	Hi	T	X	Lo	Hi	Hi	Lo	Hit	High	Hi-Z	
Hi	Lo	T	Lo	X	Hi	Hi	Lo	Write	High	D in	
Hi	Lo	T	Hi	Lo	Hi	Hi	Lo	Read	High	D Out	
Lo	Hi	X	X	X	–	–	–	Reset	–	Hi-Z	
Lo	X	F	X	X	–	–	–	Reset	–	Hi-Z	
Lo	X	X	Hi	Hi	–	–	–	Reset	–	Hi-Z	
Lo	X	X	Hi	Lo	–	–	–	Reset	–	Lo-Z	
Lo	Lo	T	Lo	X	–	–	–	Not Allowed	–	Hi-Z	2
Lo	X	T	Hi	Hi	Hi	Hi	Lo	Reset	Lo	D in	3

Key : X = Don't Care
$\overline{H_X}$ = $\overline{H_0}$ or $\overline{H_1}$
$\overline{M_X}$ = $\overline{M_0}$ or $\overline{M_1}$
$\overline{CG_x}$ = $\overline{CG_0}$ or $\overline{CG_1}$
F = (False) E_0-E_3 pattern DOES NOT match P_0-P_3 pattern.
T = (True) E_0-E_3 pattern DOES match P_0-P_3 pattern.
— = Not related to identified mode of operation.

Notes : 1. Force hit/miss operations independent of other RAM operations.
2. May disrupt Reset, will not damage device.
3. Reset will force C_X low during a valid compare when CDQ_0 is D_{IN} = HIGH.

Figure 2 : MK4202 Block Diagram.

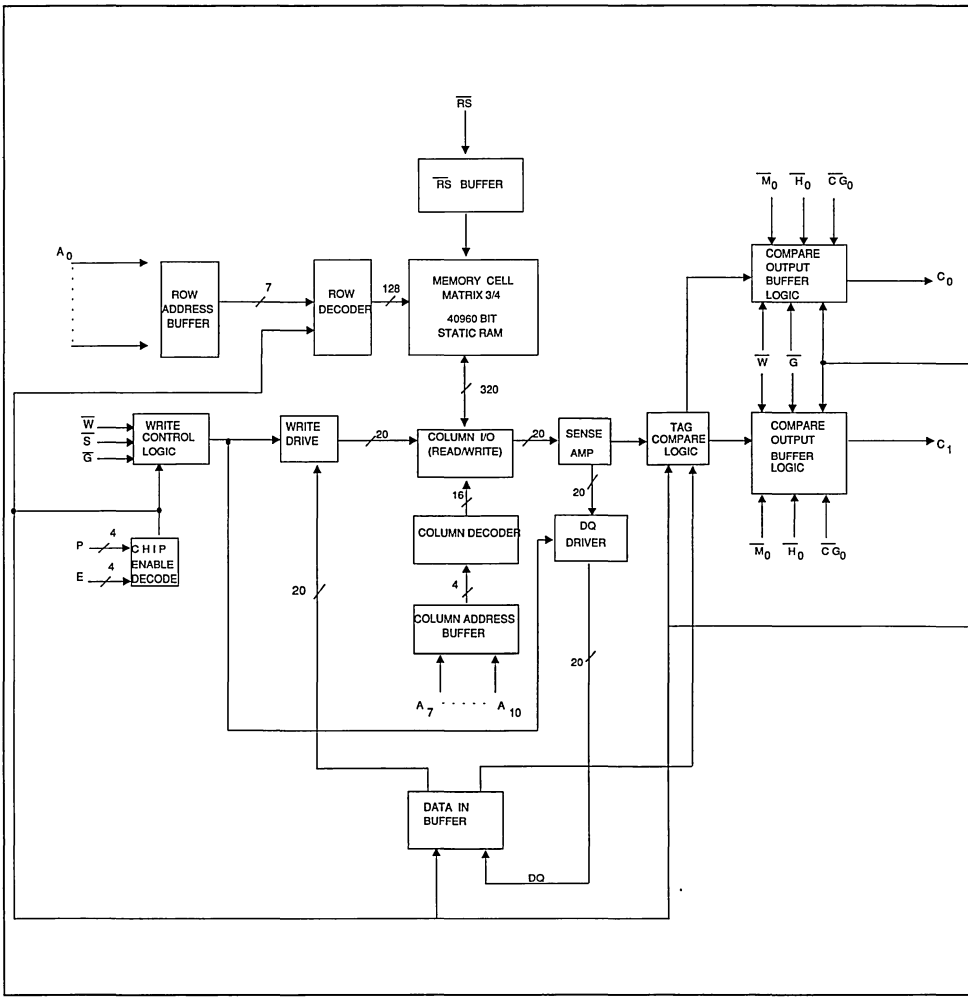
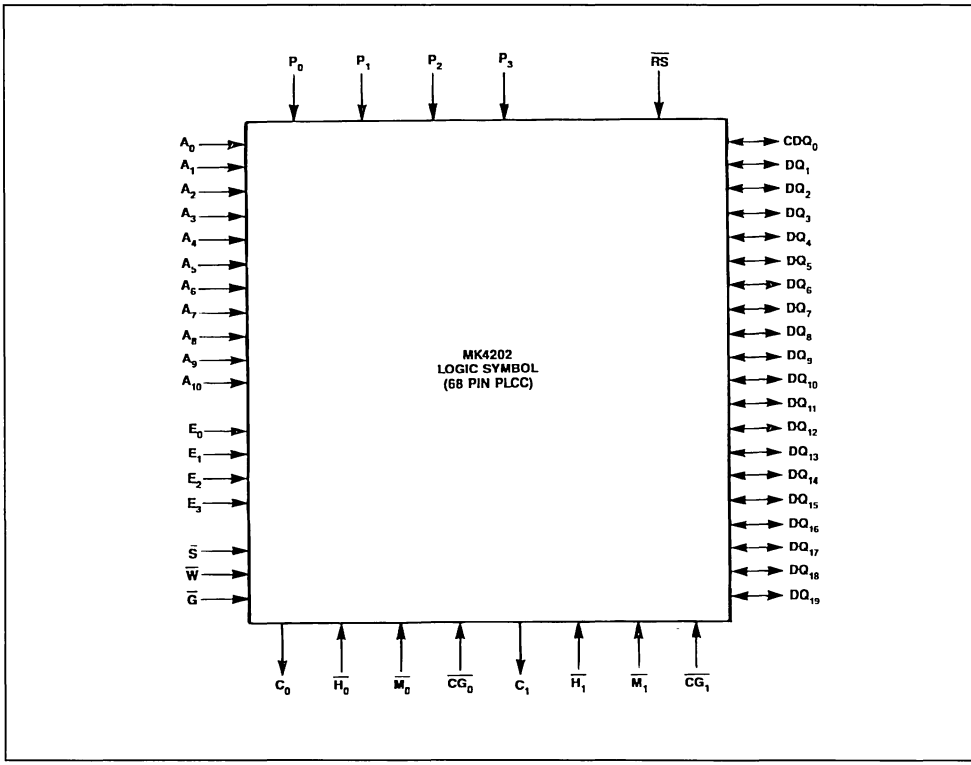


Figure 3 : Device Logic Symbol.

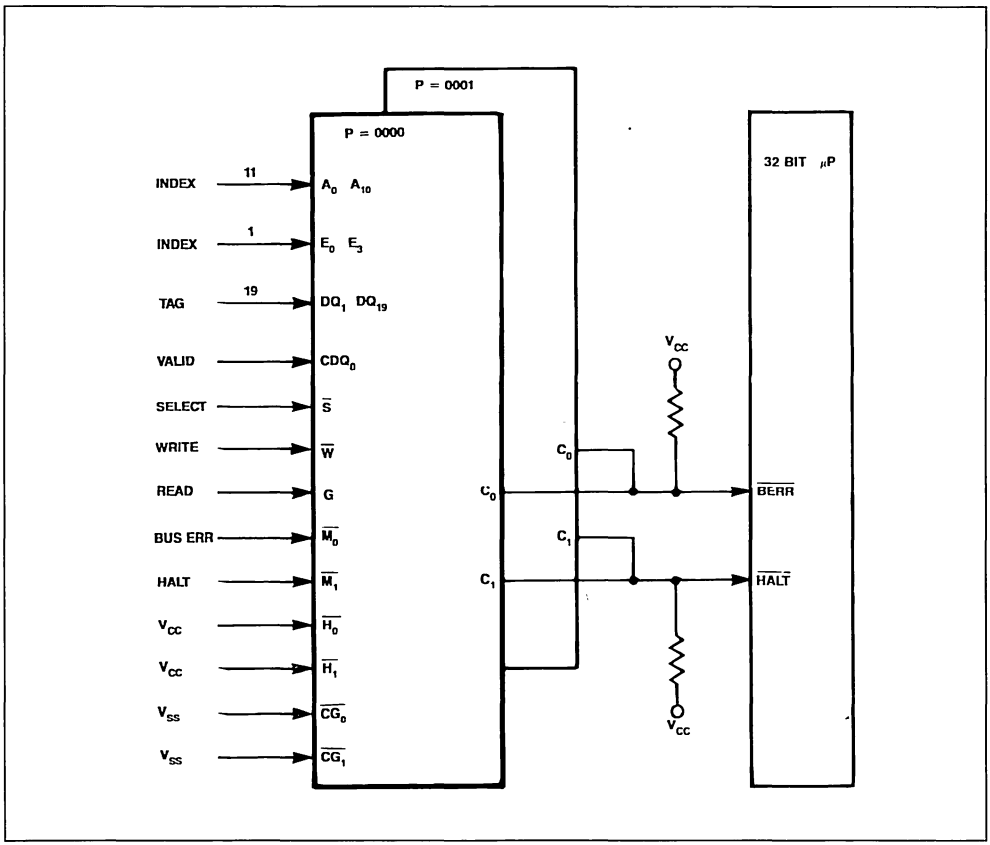


POWER DISTRIBUTION

The MK4202, being a 20 output device, obviously requires the use of good power bussing techniques. MK4202 has been designed in such a way as to allow the user to minimize the effects of switching transients on overall circuit operation. Of particular interest is the separate bussing of the V_{CC} and V_{SS} lines to the output drivers. The advantage provided by these separate power pins, designated V_{CCQ} and V_{SSQ}, is that voltage sags and ground bumps seen on these pins are not reflected into the other portions of the chip, particularly the input structures. As a result, switching noise in the supply has much less effect on input levels, providing the user with more noise margin than would otherwise be available.

Of course V_{CC} and V_{CCQ} must always be at the same DC potential. V_{SS} and V_{SSQ} must match as well. Differences between them due to AC effects are expected, but must be minimized through the adequate use of bussing and bypassing. All specifications and testing are done with $V_{SS} = V_{SSQ} \pm 10mV$ RMS, $V_{CC} = V_{CCQ} \pm 10mV$ RMS with instantaneous peak differences not exceeding 50mV.

Figure 4 : Application Block Schematic.



ABSOLUTE MAXIMUM RATINGS*

Parameter	Value	Unit
Voltage on any Pin Relative to V_{SS}	– 0.3 to7.0	V
Ambient Operating Temperature (T_A)	0 to 70	°C
Ambient Storage Temperature (plastic)	– 55 to 125	°C
Total Device Power Dissipation	2.5	Watts
RMS Output Current per Pin	25	mA

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A = 0 to 70°C)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage, GND	0	0	0	V	
V_{IH}	Logic 1 All Inputs	2.2		V_{CC} + 0.3	V	5
V_{IL}	Logic 0 All Inputs	– 0.3		0.8	V	5

Note : All voltages referenced to V_{SS}.

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = ± 10%)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
I_{CC}	Average Power Supply Current			250	mA	1
I_{CCA}	Active Power Supply Current (f = 0)			200	mA	1
I_{SB1}	TTL Standby Current			50	mA	1
I_{IL}	Input Leakage Current	– 1		+ 1	µA	2
I_{OL}	Output Leakage Current	– 10		+ 10	µA	3
V_{OH}	Logic 1 Output Voltage (I_{OUT} = – 4mA)	2.4			V	4
V_{OL}	Logic 0 Output Voltage (I_{OUT} = 8mA)			0.4	V	4

Notes : 1. Measured with outputs open. V_{CC} max.
2. Measured with V_{IN} = 0.0V to V_{CC}.
3. Measured at CDQ_0, DQ_1-DQ_{19}, C_0 and C_1.
4. All voltages referenced to V_{SSQ}.
5. Inputs (P_0-P_3) require V_{IH} min. = 4.5 volts and V_{IL} max. = 0.5 volts.
6. Sampled, not 100% tested. Measured at 1 MHz.
7. Measured at all data I/O's, C_0 and C_1.

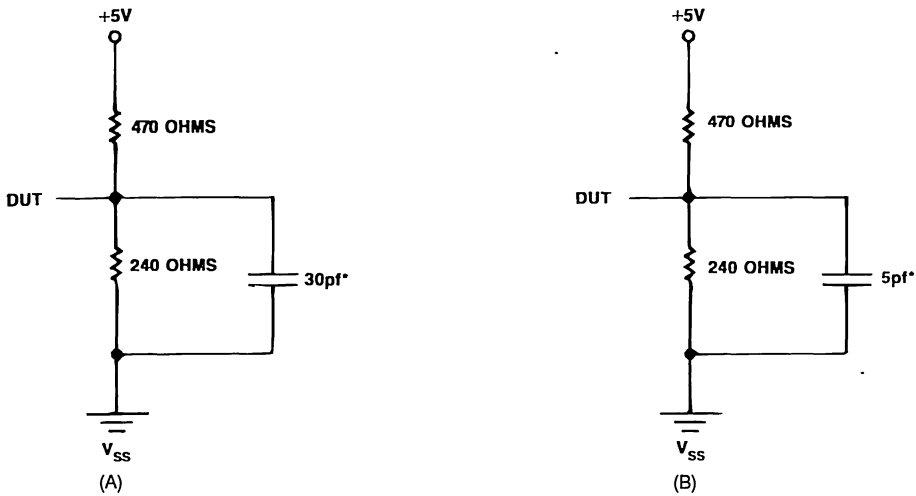
CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
C_I	Input Capacitance	4		4	pF	6
C_O	Output Capacitance	8		10	pF	6.7

AC TEST CONDITIONS

Input Levels ..... GND to 3V
Transition Time 5ns
Input and Output Timing Reference Level 1.5V
Ambient Temperature ..... 0° to 70°C
V_{CC} ..... 5.0V ± 10%

Figure 5 : Equivalent Output Load Circuit.



* Includes scope and test JIG.

READ MODE

The MK4202 is in the Read mode whenever $\overline{W}$ is HIGH, and $\overline{G}$ is LOW provided Chip Select ($\overline{S}$) is LOW and a true Chip Enable pattern (E_0-E_3) is applied. The 11 address inputs (A_0-A_{10}) define a unique index address giving access to 20 of 40,960 bits of data in the static memory array. Valid data will be present at the 20 output pins within t_{AVQV} of the last stable address provided Chip Enable, Chip Select ($\overline{S}$), and Output Enable ($\overline{G}$) access times have been met. If Chip Enable, $\overline{S}$, or $\overline{G}$ access times are not met, data access will be measured from the latter falling edge or limiting parameter (t_{EVQV}, t_{SLQV}, or t_{GLQV}). The state of the tag data I/O pins is controlled by the (E_0-E_3), $\overline{S}$, $\overline{G}$, and $\overline{W}$ input pins. The data lines may be indeterminate at t_{EVQX}, or t_{SLQX}, or t_{GLQX}, but will always have valid data at t_{AVQV}.

ELECTRICAL CHARACTERISITCS AND RECOMMENDED AC OPERATING CONDITIONS

(read cyle timing) (0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 ± 5%)

STD Symbol	ALT Symbol	Parameter	- 20		- 22		- 25		Units	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVAV}	t_C	Cycle Time	25		25		30		ns	
t_{AVQV}	t_{AA}	Address Access Time		25		25		30	ns	
t_{AXQX}	t_{AOH}	Address Output Hold Time	5		5		5		ns	
t_{AEQV}	t_{EA}	Chip Enable Access Time		25		25		30	ns	
t_{EXQX}	t_{EOH}	Chip Enable Output Hold Time	4		4		4		ns	
t_{EVQX}	t_{ELZ}	Chip Enable TRUE to Low-Z	4		4		4		ns	
t_{EXQZ}	t_{EHZ}	Chip Enable FALSE to high-Z		8		8		10	ns	
t_{SLQV}	t_{SA}	Chip Select Access Time		15		15		18	ns	
t_{SHQX}	t_{SOH}	Chip Select Output Hold Time	2		2		2		ns	
t_{SLQX}	t_{SLZ}	Chip Select to Low-Z	3		3		3		ns	
t_{SHQZ}	t_{SHZ}	Chip Select to High-Z		4		4		6	ns	
t_{GLQV}	t_{GA}	Output Enable Access Time		13		13		15	ns	
t_{GHQX}	t_{GOH}	Output Enable Output Hold Time	2		2		2		ns	
t_{GLQX}	t_{GLZ}	Output Enable to Low-Z	2		2		2		ns	
t_{GHQZ}	t_{GHZ}	Output Enable to high-Z		5		5		8	ns	

Figure 6 : Read Cycle.

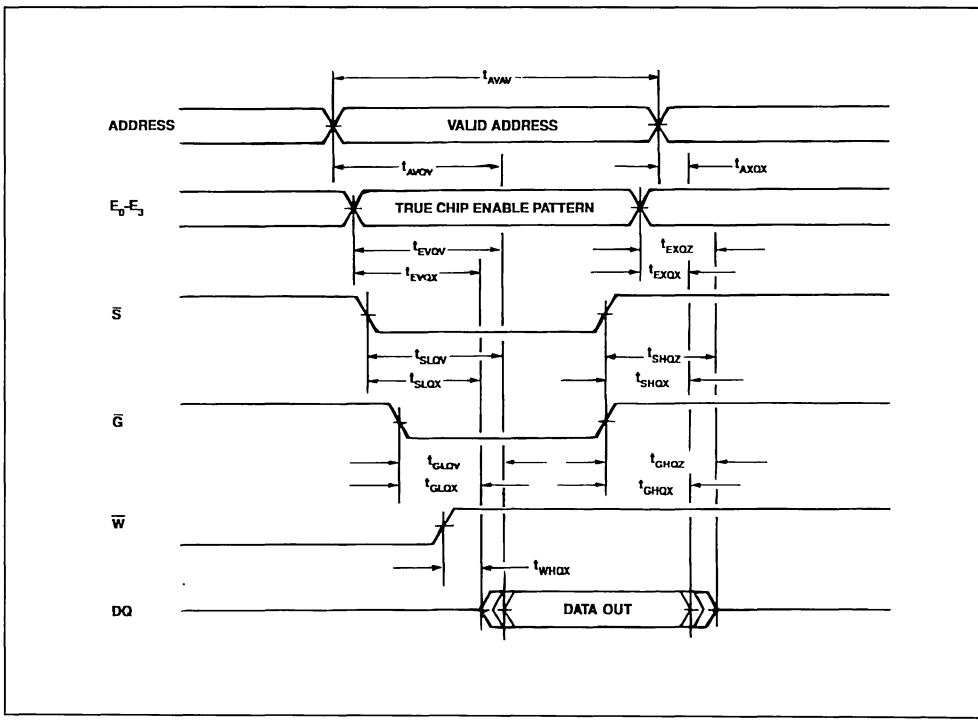


Figure 7 : Address Read Cycle.

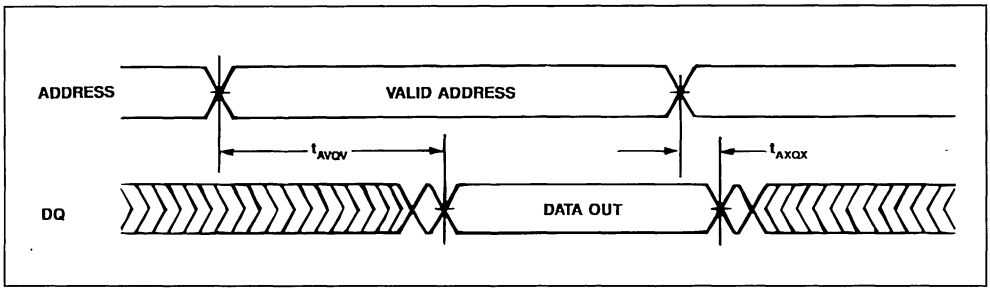


Figure 8 : Chip Enable Read Cycle.

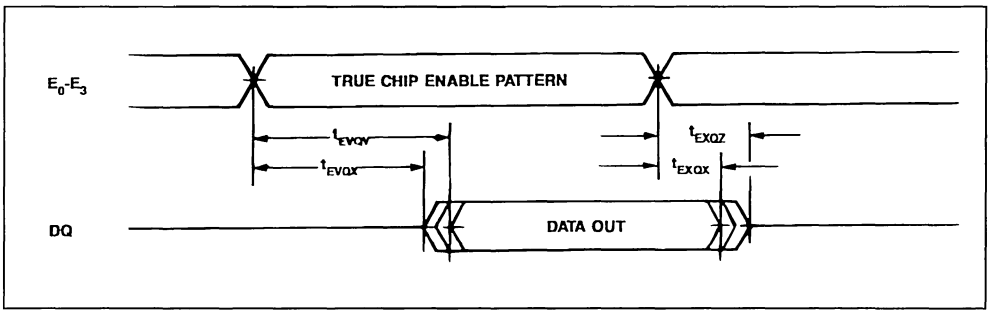


Figure 9 : Chip Select Read Cycle.

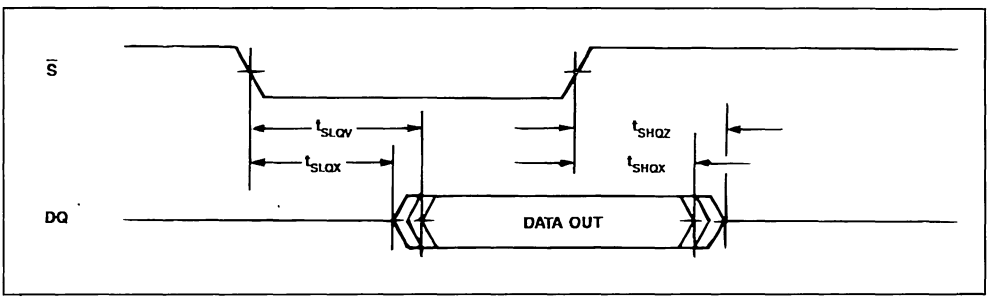
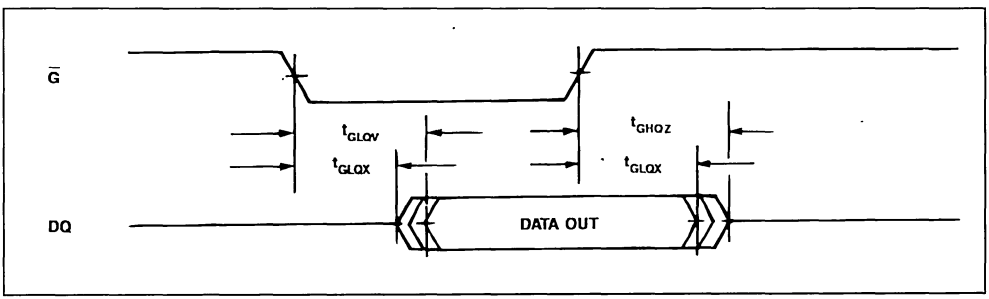


Figure 10 : Output Enable Read Cycle.



WRITE MODE

The MK4202 is in the Write mode whenever $\overline{W}$ is LOW provided Chip Select ($\overline{S}$) is LOW and a true Chip Enable pattern (E_0-E_3) is applied ($\overline{G}$ may be in either logic state). Addresses must be held valid throughout a write cycle, with either $\overline{W}$ or $\overline{S}$ inactive HIGH during address transitions. $\overline{W}$ may fall with stable addresses, but must remain valid for t_{WLWH}. Since the write begins with the concurrence of $\overline{W}$ and $\overline{S}$, should $\overline{W}$ become active first, then t_{SLSH} must be satisfied. Either $\overline{W}$ or $\overline{S}$ can terminate the write cycle, therefore t_{DVWH} or t_{DVSH} must be satisfied before the earlier rising edge, and t_{WHDX} or t_{SHDX} after the earlier rising edge. If the outputs are active with $\overline{G}$ and $\overline{S}$ asserted LOW and with true Chip Enable, then $\overline{W}$ will return the outputs to high impedance within t_{WLHZ} of its falling edge.

ELECTRICAL CHARACTERISITICS AND RECOMMENDED AC OPERATING CONDITIONS

(write cycle timing) ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0 \pm 10\%$)

STD Symbol	ALT Symbol	Parameter	- 20		- 22		- 25		Units	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVAV}	t_C	Cycle Time	25		25		30		ns	
t_{AVWL}	t_{AS}	Address Set-up Time to $\overline{W}$ LOW	0		0		0		ns	
t_{WHAX}	t_{AH}	Address Hold Time from $\overline{W}$ HIGH	0		0		0		ns	
t_{AVSL}	t_{AS}	Address Set-up Time to $\overline{S}$ LOW	0		0		0		ns	
t_{SHAX}	t_{AH}	Address Hold Time from $\overline{S}$ HIGH	0		0		0		ns	
t_{EVWL}	t_{ES}	Chip Enable Set-up Time to $\overline{W}$ LOW	3		3		3		ns	
t_{WHEX}	t_{EH}	Chip Enable Hold Time from $\overline{W}$ HIGH	0		0		0		ns	
t_{EVSL}	t_{ES}	Chip Enable Set-up Time to $\overline{S}$ LOW	3		3		3		ns	
t_{SHEX}	t_{EH}	Chip Enable Hold Time to $\overline{S}$ HIGH	0		0		0		ns	
t_{WLWH}	t_{WW}	Write Pulse Width	15		15		18		ns	
t_{SLSH}	t_{SW}	Chip Select Pulse Width	16		16		20		ns	
t_{DVWH}	t_{DS}	Data Set-up Time to $\overline{W}$ HIGH	12		12		15		ns	
t_{WHDX}	t_{DH}	Data Hold Time from $\overline{W}$ HIGH	0		0		0		ns	
t_{DVSH}	t_{DS}	Data Set-up Time to $\overline{S}$ HIGH	12		12		15		ns	
t_{SHDX}	t_{DH}	Data Hold Time from $\overline{S}$ HIGH	0		0		0		ns	
t_{WLQZ}	t_{WZ}	Outputs Hi-Z from $\overline{W}$ LOW		8		8		10	ns	
t_{WHQX}	t_{WL}	Outputs Low-Z from $\overline{W}$ HIGH	5		5		5		ns	

Figure 11 : $\overline{W}$ Write Cycle.

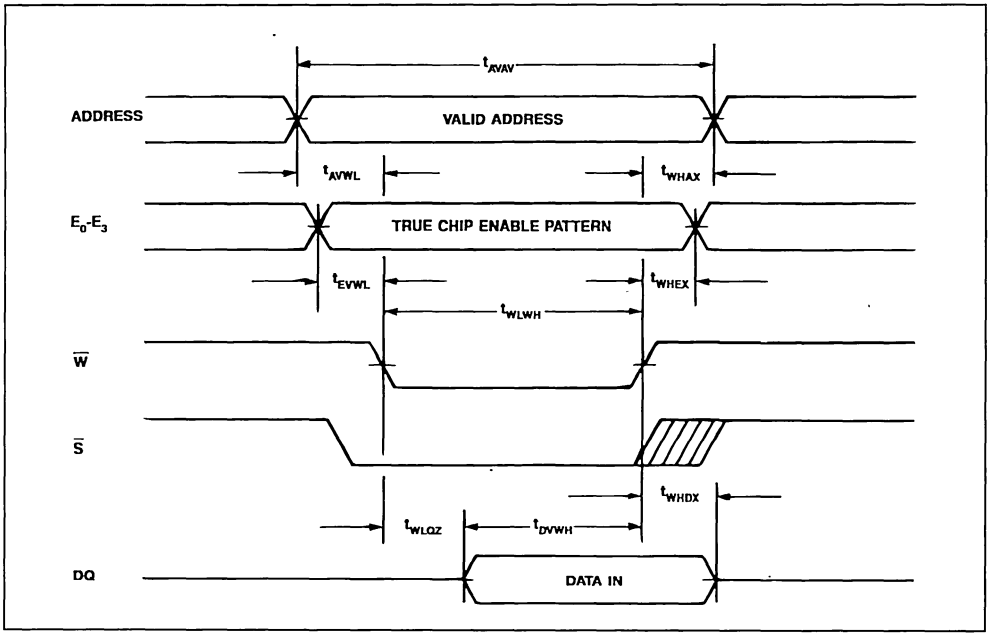
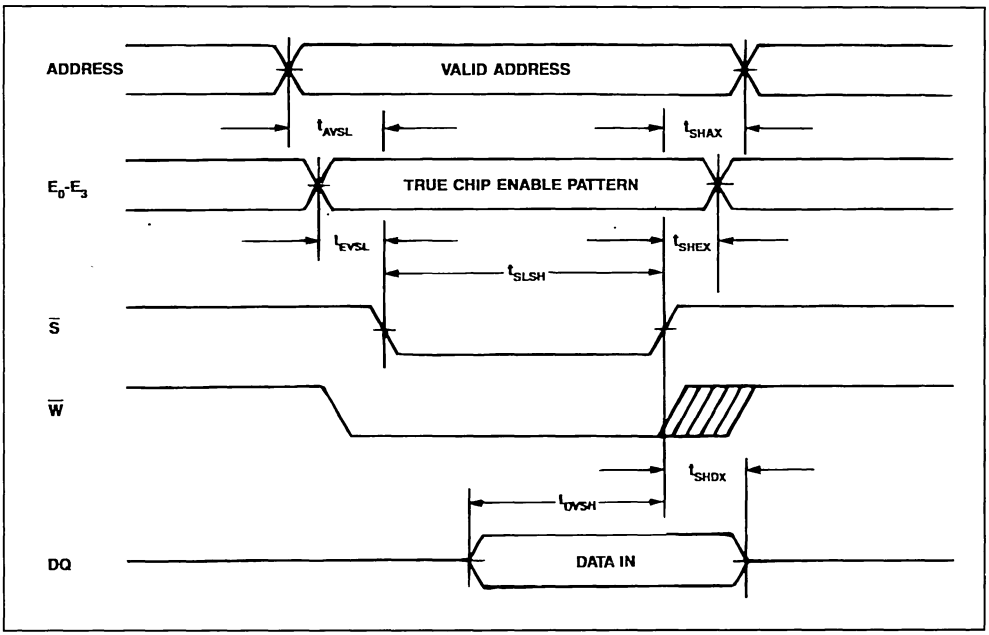


Figure 12 : $\overline{S}$ Write Cycle.



COMPARE MODE

The MK4202 is in the Compare mode whenever $\overline{W}$ and $\overline{G}$ are HIGH provided a true Chip Enable (E_0-E_3) pattern is applied. Chip Select (S) is reguarded as a don't care since the user is not concerned with the data outputs, but only with the Compare (C_X) outputs. M_X and H_X must be HIGH, and CG_X active LOW to enable the Compare outputs for a valid compare hit or miss.

The 11 index address inputs (A_0-A_{10}) define a unique location in the static RAM array. The data presented on the Data Inputs (DQ_1-DQ_{19} and CDQ_0) as Tag Data is compared to the internal RAM data as specified by the index. If all bits are equal (match) then a hit condition occurs (C_X = HIGH). If at least one bit is not equal, then a miss occurs (C_X = LOW).

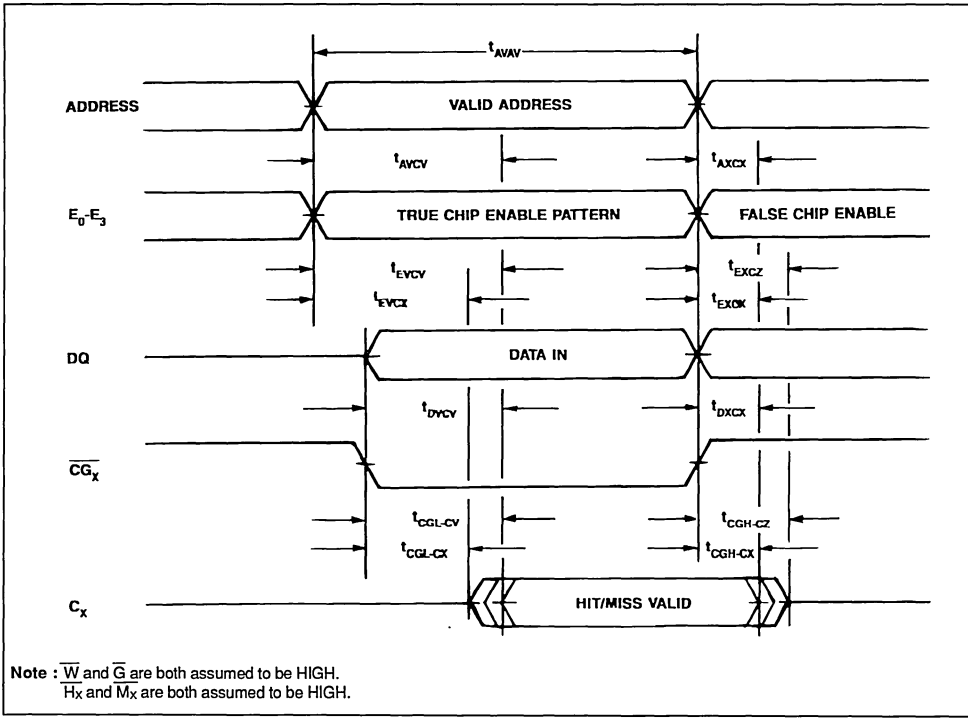
The Compare output will be valid t_{AVCV} from stable address, or t_{DVCV} from valid tag data provided Chip Enable is true, and CG_X is active LOW. Should the address be stable with valid tag data, and Chip Enable false, then compare access will be within t_{EVCV} from true Chip Enable. When executing a write-to-compare cycle ($\overline{W}$ = LOW, and $\overline{G}$ = LOW or HIGH), C_X will be valid t_{WHCV} or t_{GHCV} from the latter rising edge of W or G respectively. Finally, when gating the C_X output in the compare mode with CG_X, the compare output will be valid $t_{CGL\text{-}CV}$ from the falling edge of CG_X.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(compare cycle timing) (0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 ± 10%)

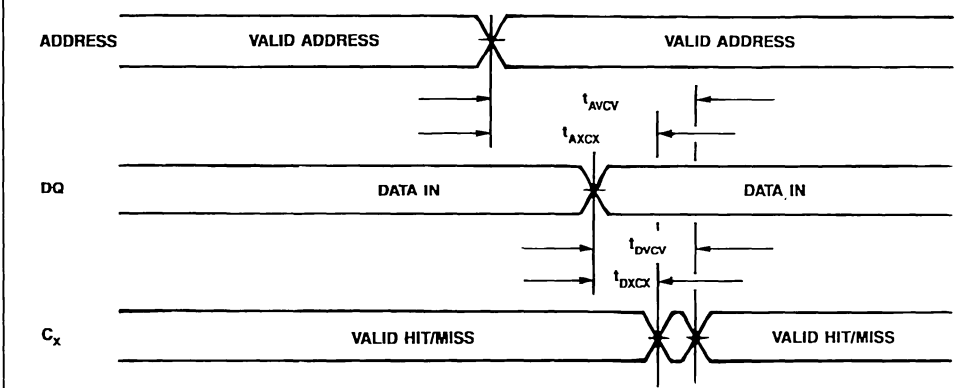
STD Symbol	ALT Symbol	Parameter	- 20		- 22		- 25		Units	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVCV}	t_{ACA}	Address Compare Access Time		20		22		25	ns	
t_{AXCX}	t_{ACOH}	Address Compare Output Hold Time	5		5		5		ns	
t_{DVCV}	t_{DCA}	Tag Data Compare Acccess Time		16		18		20	ns	
t_{DXCX}	t_{DCH}	Tag Data Compare Hold Time	2		2		2		ns	
t_{WLCH}	t_{WCH}	$\overline{W}$ LOW to Compare HIGH		10		11		12	ns	
t_{WHCX}	t_{WCOH}	$\overline{W}$ Compare Output hold Time	3		3		3		ns	
t_{WLCX}	t_{WLCZ}	$\overline{W}$ to Compare HOLD	3		3		3		ns	
t_{WHCV}	t_{WCV}	$\overline{W}$ to Compare Valid		10		10		12	ns	
t_{GLCH}	t_{GCH}	$\overline{G}$ Low to Compare HIGH		10		11		12	ns	
t_{GHCX}	t_{CGOH}	$\overline{G}$ Compare Output Hold Time	3		3		3		ns	
t_{GLCX}	t_{GLCZ}	$\overline{G}$ to Compare to HOLD	3		3		3		ns	
t_{GHCV}	t_{GCV}	$\overline{G}$ to Compare Valid		10		10		12	ns	
t_{EVCV}	t_{ECA}	E True to Compare Access Time		20		22		25	ns	
t_{EXCX}	t_{ECOH}	E False Compare Hold Time	4		4		4		ns	
t_{EVCX}	t_{ECLZ}	E True to Compare Low-Z	4		4		4		ns	
t_{EXCZ}	t_{ECHZ}	E False to Compare high-Z		8		8		10	ns	
$t_{CGL\text{-}CV}$	t_{CGA}	$\overline{CG}_X$ to Compare Access Time		8		8		10	ns	
$t_{CGH\text{-}CX}$	t_{CGOH}	$\overline{CG}_X$ Compare Hold time	2		2		2		ns	
$t_{CGL\text{-}CX}$	t_{CGLZ}	$\overline{CG}_X$ LOW to Compare low-Z	2		2		2		ns	
$t_{CGH\text{-}CZ}$	t_{CGHZ}	$\overline{CG}_X$ HIGH to Compare High-Z		8		8		10	ns	

Figure 12 : Summary Compare Cycle.



Note : $\overline{W}$ and $\overline{G}$ are both assumed to be HIGH.
$\overline{H_X}$ and $\overline{M_X}$ are both assumed to be HIGH.

Figure 13 : Compare Cycle.



Note : $\overline{W}$ and $\overline{G}$ are both HIGH, $\overline{CG_X}$ is LOW, and a true Chip Enable pattern is present. H_X and M_X are both assumed to be HIGH.

RESET MODE

The MK4202 allows an asynchronous reset whenever $\overline{RS}$ is LOW regardless of the logic state on the other input pins. Reset clears all internal RAM bits in CDQ_0 (2048 bits) to a logic zero. This output can be used as a valid tag bit to insure a valid compare miss or hit . It should be noted that a valid write cycle is not allowed during a reset cycle ($\overline{W}$ = LOW, $\overline{S}$ = LOW, $\overline{RS}$ = LOW, and Chip Enable is true). The state of the data outputs is determined by the input control logic pins : Chip Enable, $\overline{S}$, $\overline{G}$, and $\overline{W}$ (see truth table). Should a reset occur during a valid compare cycle, and the CDQ_0 valid tag bit is set to a logic (1), then C_X will go LOW at t_{RSL-CL} from the falling edge of $\overline{RS}$.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(reset cycle timing) (0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 ± 10%)

STD Symbol	ALT Symbol	Parameter	- 20		- 22		- 25		Units	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
$t_{RLSL-AV}$	t_{RSC}	Reset Cycle Time	20		25		30		ns	
$t_{RSL-RSH}$	t_{RSW}	Reset pulse Width	25		25		30		ns	
t_{RSL-CL}	t_{RSCL}	$\overline{RS}$ LOW to Compare Output LOW		25		25		30	ns	
t_{RSH-AV}	t_{RSR}	Address Recovery Time	0		0		0		ns	
t_{RSH-EV}	t_{RSR}	Chip Enable Recovery Time	0		0		0		ns	

FORCE HIT AND FORCE MISS

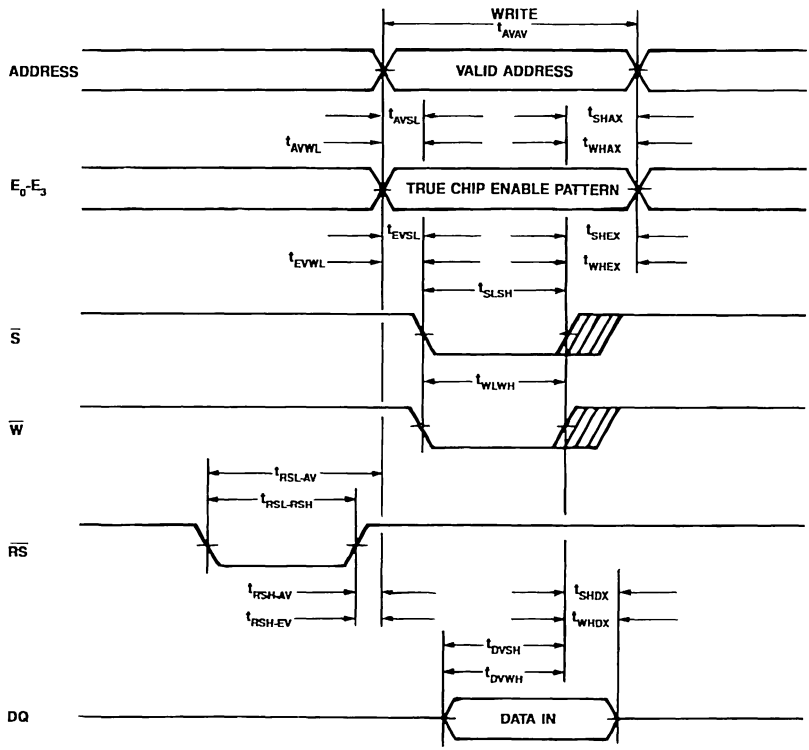
The MK4202 can force either a miss or hit condition on the C_X output by asserting $\overline{M_X}$ or $\overline{H_X}$ LOW. A Force Miss overrides a Force Hit condition and is not dependent upon Compare Output Enable ($\overline{CG_X}$) (see truth table). The $C_{\overline{X}}$ output will go HIGH within $t_{\overline{HLCH}}$ from the falling edge of $\overline{H_X}$ or $C_{\overline{X}}$ will go LOW within $t_{\overline{MLCL}}$ from the falling edge of $M_{\overline{X}}$. All $M_{\overline{X}}$ and $H_{\overline{X}}$ inputs must be HIGH during a valid compare cycle.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(force hit or miss cycle timing) (0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 ± 10%)

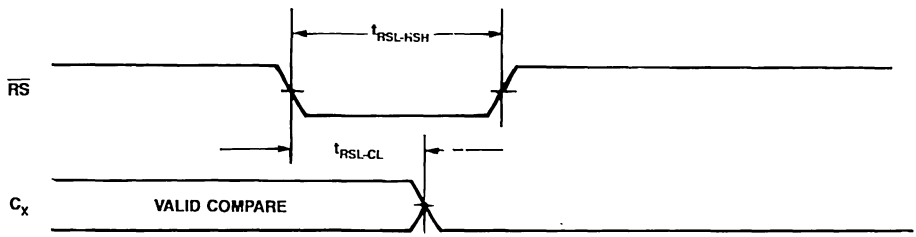
STD Symbol	ALT Symbol	Parameter	- 20		- 22		- 25		Units	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{HLCH}	t_{HA}	$\overline{H_X}$ to Force Hit Access Time		8		8		10	ns	
t_{HHCZ}	t_{HHZ}	$\overline{H_X}$ to Compare High-Z		5		5		8	ns	
t_{HL-CGX}	t_{HS}	Force hit to $\overline{CG}_X$ don't care	2		2		2		ns	
t_{HH-CGH}	t_{HR}	Force hit to $\overline{CG}_X$ recognized	2		2		2		ns	
t_{MLCL}	t_{MA}	$\overline{M_X}$ to Force Miss Access Time		8		8		10	ns	
t_{MHCZ}	t_{MHZ}	$\overline{M_X}$ to Compare to high-Z		5		5		8	ns	
t_{ML-CGX}	t_{MS}	Force Miss to $\overline{CG}_X$ don't care	2		2		2		ns	
t_{MH-CGH}	t_{MR}	Force Miss to $\overline{CG}_X$ Recognized	2		2		2		ns	
t_{MLHX}	t_{MHS}	Force Miss to $\overline{H}_X$ don't care	2		2		2		ns	
t_{MHHH}	t_{MHR}	Force Miss to $\overline{H}_X$ Recognized	2		2		2		ns	

Figure 14 : Reset Cycle.



Note : Reset during an active write cycle is not allowed. A write cycle may disrupt Reset, but will not damage device.

Figure 15 : Valid Compare - Reset.



Note : CDQ_0 is presumed to be HIGH.

Figure 16 : Force Hit and Force Miss.

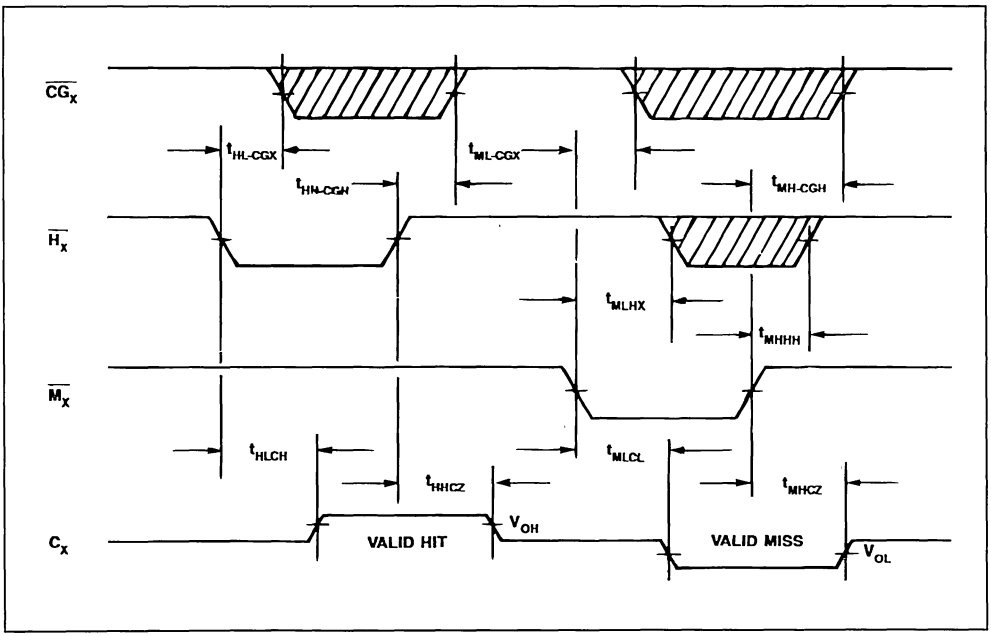
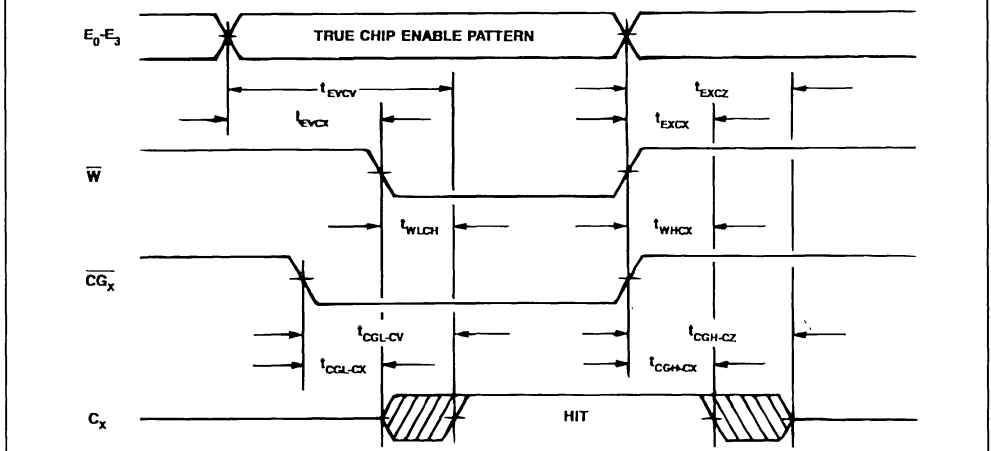
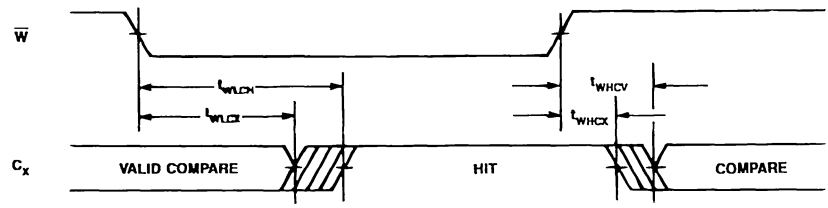


Figure 17 : Late Write - Hit Cycle.



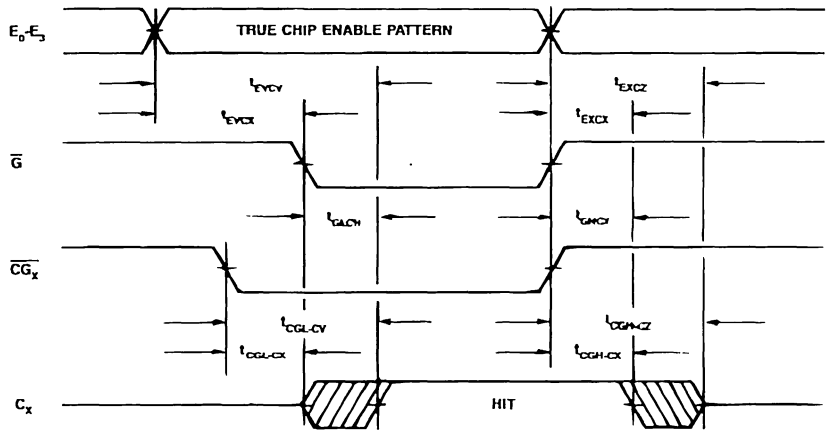
Note : $\overline{G}$ is HIGH and a Valid Address is present, H_X and M_X are both assumed to be HIGH, with CG_X LOW.

Figure 18 : Compare - Write Hit - Compare Cycle.



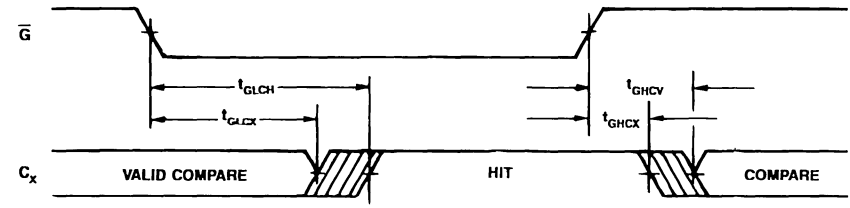
Note : $\overline{G}$ is HIGH and a Valid Address is present, $\overline{H_X}$ and $\overline{M_X}$ are both assumed to be HIGH, with CG_X LOW, with $\overline{CG_X}$ LOW.

Figure 19 : Late Read - Hit Cycle.



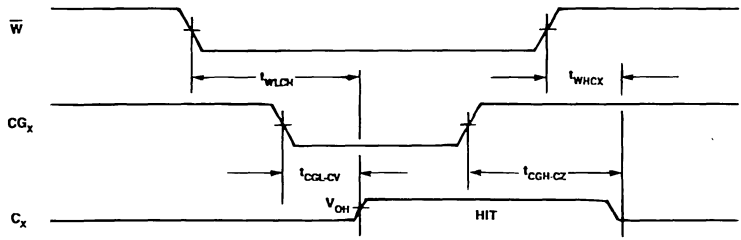
Note : $\overline{W}$ is HIGH and a Valid Address is present, $\overline{H_X}$ and $\overline{M_X}$ are both assumed to be HIGH, (with $\overline{CG_X}$ LOW.)

Figure 20 : Compare - Read Hit - Compare Cycle.



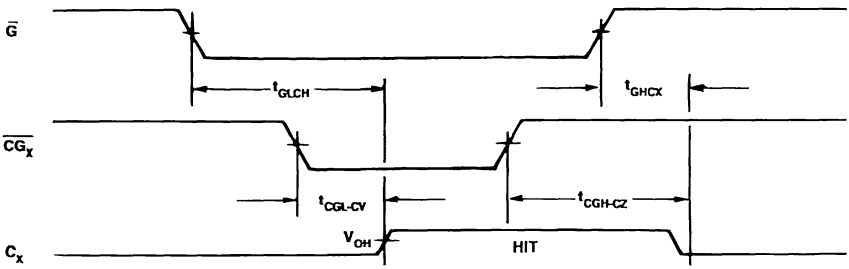
Note : $\overline{W}$ is HIGH and a Valid Address is present, $\overline{H_X}$ and $\overline{M_X}$ are both assumed to be HIGH, with CG_X LOW.

Figure 21 : Early Write - Hit Cycle.



Note : $\overline{G}$ is HIGH and a Valid Address is present, with $(E_0 - E_3) = \overline{True}$. H_X and M_X are both assumed to be HIGH.

Figure 22 : Early Read - Hit Cycle.

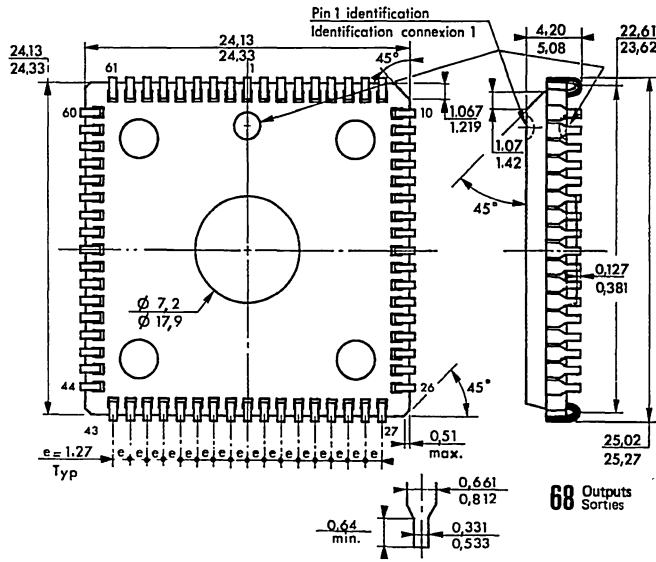


Note : $\overline{W}$ is HIGH and a Valid Address is present, with $(E_0 - E_3) = \overline{True}$. H_X and M_X are both assumed to be HIGH.

ORDER CODE

Part Number	Access Time	Cycle Time	Package Type	Temperature
MK4202(Q)-20	20ns	25ns	68 Pin PLCC	0°C to 70°C
MK4202(Q)-22	22ns	25ns	68 Pin PLCC	0°C to 70°C
MK4202(Q)-25	25ns	30ns	68 Pin PLCC	0°C to 70°C

PACKAGE DIMENSIONS



SGS-THOMSON MICROELECTRONICS

MK44S80(N,X) -15/17/20

65,536-BIT FAST CMOS 16 K X 4 CACHE TAGRAM™

ADVANCE DATA

FEATURES

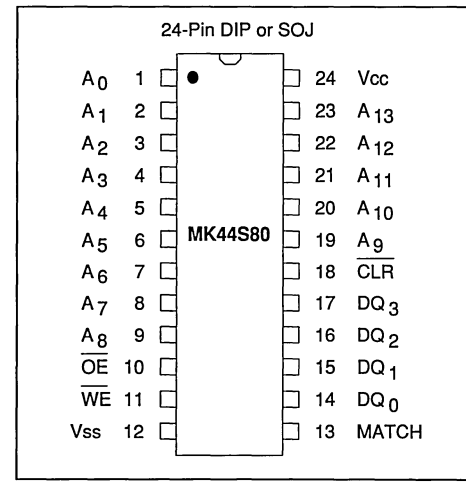
- 16K x 4 FAST CMOS CACHE TAGRAM
- 15,17,20ns ADDRESS TO COMPARE ACCESS
- 10,12,14ns TAG DATA TO COMPARE ACCESS
- EQUAL ACCESS, READ/WRITE CYCLE TIMES
- FLASH CLEAR FUNCTION
- 24-PIN 300 MIL STANDARD PLASTIC DIP

DESCRIPTION

The MK44S80 is a 65,536-bit CMOS Static TAGRAM, organized as 16Kx4 using SGS-THOMSON Microelectronics' advanced fast HCMOS process technology. This device is functionally compatible with the industry standard MK41S80 4Kx4 TAGRAM. All inputs and outputs are TTL compatible using a single 5V supply.

The MK44S80 provides full static operation, requiring no external clocks or refresh operations, and features a MATCH output for indicating either a cache hit or miss condition. The on-board 4-bit comparator compares RAM contents with current input (tag) data. The result on the MATCH pin is an active high match ("hit"), or active low for a "miss" condition. The MK44S80 offers a totem-pole MATCH output design for fast access times, allowing the MATCH pins of several devices to be gated together to provide an enable or acknowledge to the data cache or cache control logic (refer to Figure 2).

PIN CONNECTION



MK44S80 TRUTH TABLE

$\overline{WE}$	$\overline{OE}$	$\overline{CLR}$	MATCH	MODE
H	H	H	Valid	Compare
L	X	H	Invalid	Write
H	L	H	Invalid	Read
X	X	L	Invalid	Clear

PIN NAMES

A_0-A_{13}	Address Inputs
DQ_0-DQ_3	Data I/O_{0-3}
MATCH	Comparator Output
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{CLR}$	Ram Flash Clear
V_{CC}, V_{SS}	+5V, GND

TAGRAM FUNCTION

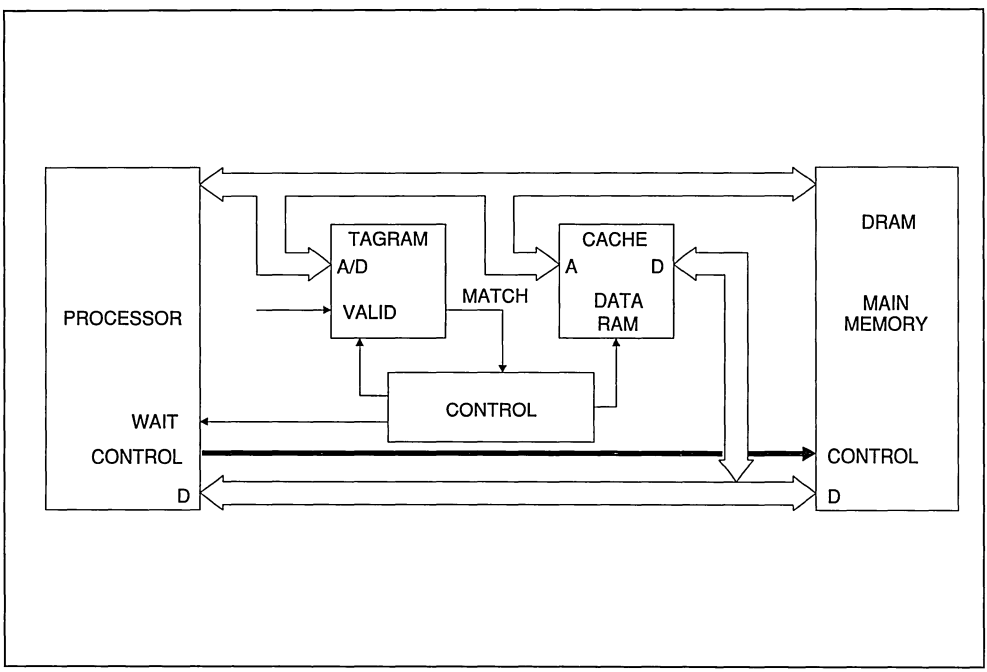
The MK44S80 is an SRAM based Cache Tag directory (hence the name TAGRAM). Figure 2 shows a general block diagram using a cache tag directory (TAGRAM) in a cache subsystem application. The system must detect whether the requested data resides in the cache data RAM, or if extended read cycles to main memory are necessary.

The MK44S80 features four modes of operation: Write, Read, Compare, and Clear. The MK44S80 incorporates an on-board 4 bit comparator that compares internal RAM contents with current (tag) input data. If the device is in the compare mode, and the comparator detects a "match", then the MATCH pin will go high for a hit condition. If a match is not detected by the comparator, then the MATCH pin drives low to denote a "miss" condition. Standard write/read operations are performed with Write ($\overline{WE}$) and Output ($\overline{OE}$) Enable inputs. Additionally, the device provides a Flash Clear operation via the $\overline{CLR}$ pin.

When a low level (V_{IL}) is applied to the $\overline{CLR}$ input pin for the specified t_{CLP} time, all RAM bits are set to a logic zero.

Compare data (internal RAM) can be read from the data pins by bringing Output Enable ($\overline{OE}$) low. This will allow data stored in the memory array to be displayed at the Outputs (DQ_0 - DQ_3).

GENERAL CACHE SUB SYSTEM BLOCK DIAGRAM



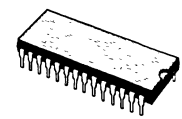
SGS-THOMSON MICROELECTRONICS

MK4501(N,K) -65/80/10/12/15/20

512 x 9 CMOS BiPORT FIFO

ADVANCE DATA

- FIRST-IN, FIRST-OUT MEMORY BASED ARCHITECTURE
- FLEXIBLE 512 x 9 ORGANIZATION
- LOW POWER HCMOS TECHNOLOGY
- ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE
- BIDIRECTIONAL APPLICATIONS
- FULLY EXPANDABLE BY WORD WIDTH OR DEPTH
- EMPTY AND FULL WARNING FLAGS
- RETRANSMIT CAPABILITY
- HIGH PERFORMANCE



N
DIP–28
(Plastic Package)

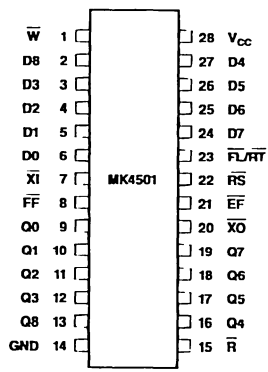
K
PLCC32
(Plastic Chip Carrier)

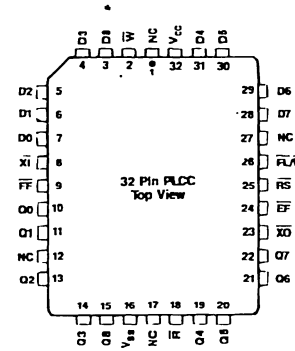
Part No	Access Time	R/W Cycle Time
MK4501-65	65ns	80ns
MK4501-80	80ns	100ns
MK4501-10	100ns	120ns
MK4501-12	120ns	140ns
MK4501-15	150ns	175ns
MK4501-20	200ns	235ns

PIN NAMES

$\overline{W}$	= Write	$\overline{XI}$	= Expansion In
$\overline{R}$	= Read	$\overline{XO}$	= Expansion Out
$\overline{RS}$	= Reset	$\overline{FF}$	= Full Flag
$\overline{FL}/\overline{RT}$	= First Load/ Retransmit	$\overline{EF}$	= Empty Flag
		V_{CC}	= 5V
D	= Data In	GND	= Ground
Q	= Data Out		

Figure 1 : Pin Connections.





DESCRIPTION

The MK4501 is a member of the BiPORT™ Memory Series, which utilizes special two-port cell techniques. Specifically, this device implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full and empty flags, and unlimited expansion capability in both word size and depth. The main application of the MK4501 is as a rate buffer, sourcing and absorbing data at different rates, (e.g., interfacing fast processors and slow peripherals). The full and empty flags are provided to prevent data overflow and underflow. The data is loaded and emptied on a First-In, First-Out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the writes and reads are internally sequential, thereby requiring no address information, the pinout definition will serve this and future high-density devices. The ninth bit is provided to support control or parity functions.

FUNCTIONAL DESCRIPTION

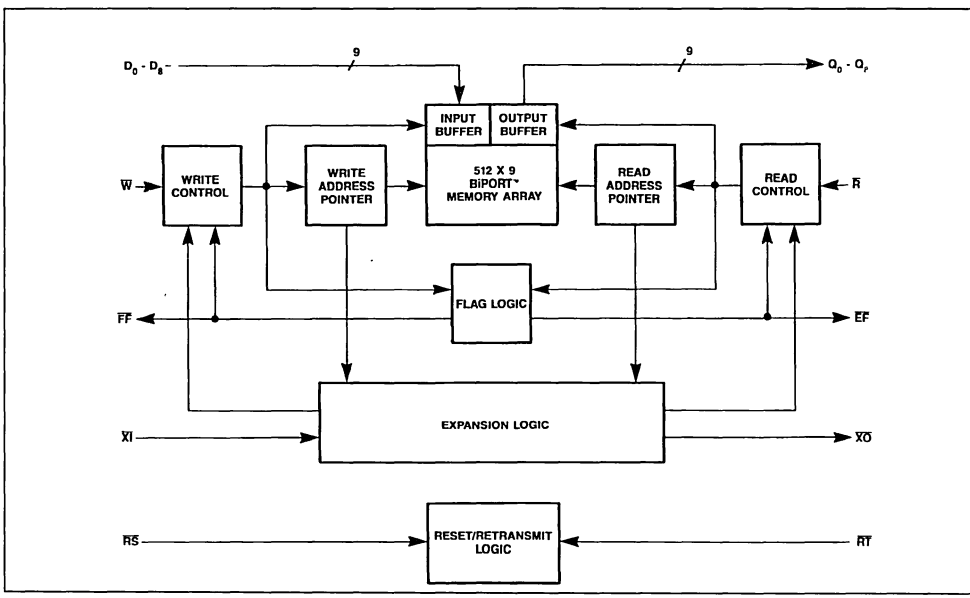
Unlike conventional shift register based FIFOs, the MK4501 employs a memory-based architecture wherein a byte written into the device does not "ripple-through". Instead, a byte written into the MK4501 is stored at a specific location, where it remains until over-written. The byte can be read and re-read as often as desired.

Twin address pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written. Address pointers automatically loop back to address zero after reaching address 511. The empty/full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

Resetting the FIFO simply resets the address pointers to address zero. Pulsing retransmit resets the read address pointer without affecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading the individual FIFOs. The penalty of cascading is often unacceptable ripple-through delays. The 4501 allows implementation of very large FIFOs with no timing penalties. The memory-based architecture of the MK4501 allows connecting the read, write, data in, and data out lines of the MK4501s in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in and expansion-out pins as appropriate (see the Expansion Timing section for a more complete discussion).

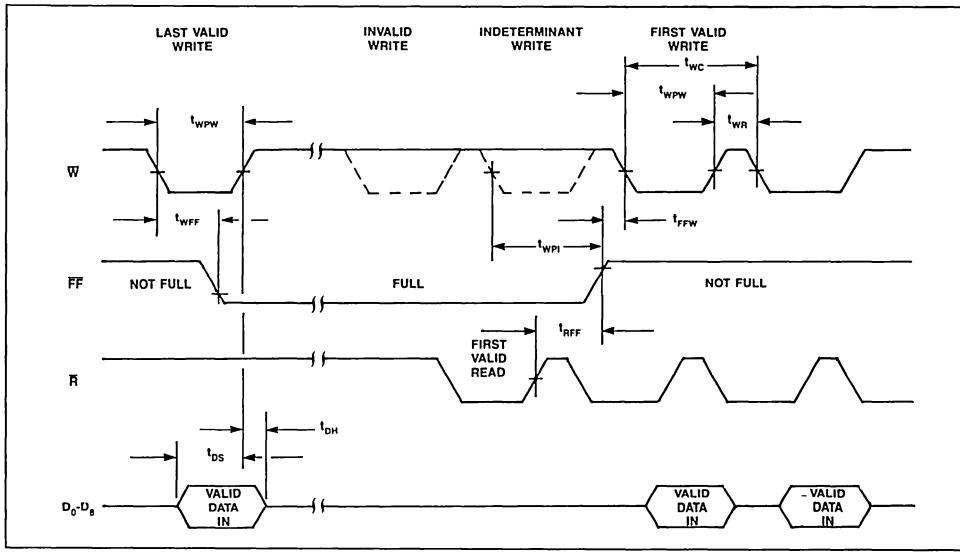
Figure 2 : MK4501 Block Diagram.



WRITE MODE

The MK4501 initiates a Write Cycle (see Figure 3A) on the falling edge of the Write Enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not asserted. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing Read operations. $\overline{FF}$ is asserted during the last valid write as the MK4501 becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go high t_{RFF} after completion of a valid READ operation. $\overline{FF}$ will again go low t_{WFF} from the beginning of a subsequent WRITE operation, provided that a second READ has not been completed (see Figure 4A). Writes beginning t_{FFW} after $\overline{FF}$ goes high are valid. Writes beginning after $\overline{FF}$ goes low and more than t_{WPI} before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on internal flag status.

FIGURE 3A. WRITE AND FULL FLAG TIMING



AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

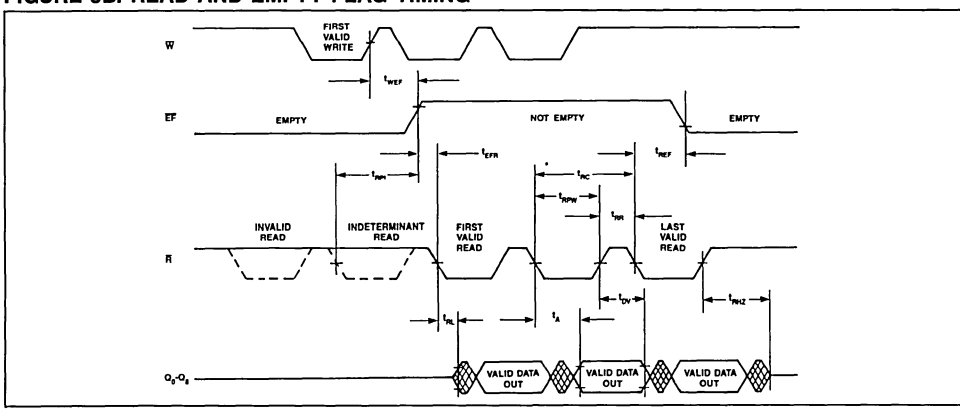
		4501-65		4501-80		4501-10		4501-12		4501-15		4501-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	Write Cycle Time	80		100		120		140		175		235		ns	
t_{WPW}	Write Pulse Width	65		80		100		120		150		200		ns	1
t_{WR}	Write Recovery Time	15		20		20		20		25		35		ns	
t_{DS}	Data Set Up Time	20		25		35		40		50		65		ns	
t_{DH}	Data Hold Time	10		10		10		10		10		10		ns	
t_{WFF}	$\overline{W}$ Low to $\overline{FF}$ Low		60		75		95		115		145		195	ns	2
t_{FFW}	$\overline{FF}$ High to Valid Write	10		10		10		10		10		10		ns	2
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High		60		75		95		110		140		190	ns	2
t_{WPI}	Write Protect Indeterminant		35		35		35		35		35		35	ns	2

READ MODE

The MK4501 initiates a Read Cycle (see Figure 3B) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not asserted. In the Read mode of operation, the MK4501 provides a fast access to data from 9 of 4608 locations in the static storage array. The data is accessed on a FIFO basis independent of any ongoing WRITE operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next Read operation.

In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further Read operations will be inhibited (the data outputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid Write operation. $\overline{EF}$ will again go low t_{REF} from the beginning a subsequent READ operation, provided that a second WRITE has not been completed (see Figure 4B). Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more than t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less than t_{EFR} later may or may not occur (be valid) depending on internal flag status.

FIGURE 3B. READ AND EMPTY FLAG TIMING



AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

		4501-65		4501-80		4501-10		4501-12		4501-15		4501-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	80		100		120		140		175		235		ns	
t_A	Access Time		65		80		100		120		150		200	ns	2
t_{RR}	Read Recovery Time	15		20		20		20		25		35		ns	
t_{RPW}	Read Pulse Width	65		80		100		120		150		200		ns	1
t_{RL}	$\overline{R}$ Low to Low Z	0		0		0		0		0		0		ns	2
t_{DV}	Data Valid from High$\overline{R}$	5		5		5		5		5		5		ns	2
t_{RHZ}	$\overline{R}$ High to High Z		25		25		25		35		50		60	ns	2
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low		60		75		95		115		145		195	ns	2
t_{EFR}	$\overline{EF}$ High to Valid Read	10		10		10		10		10		10		ns	2
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High		60		75		95		110		140		190	ns	2
t_{RPI}	Read Protect Indeterminant		35		35		35		35		35		35	ns	2

FIGURE 4A. READ/WRITE TO FULL FLAG

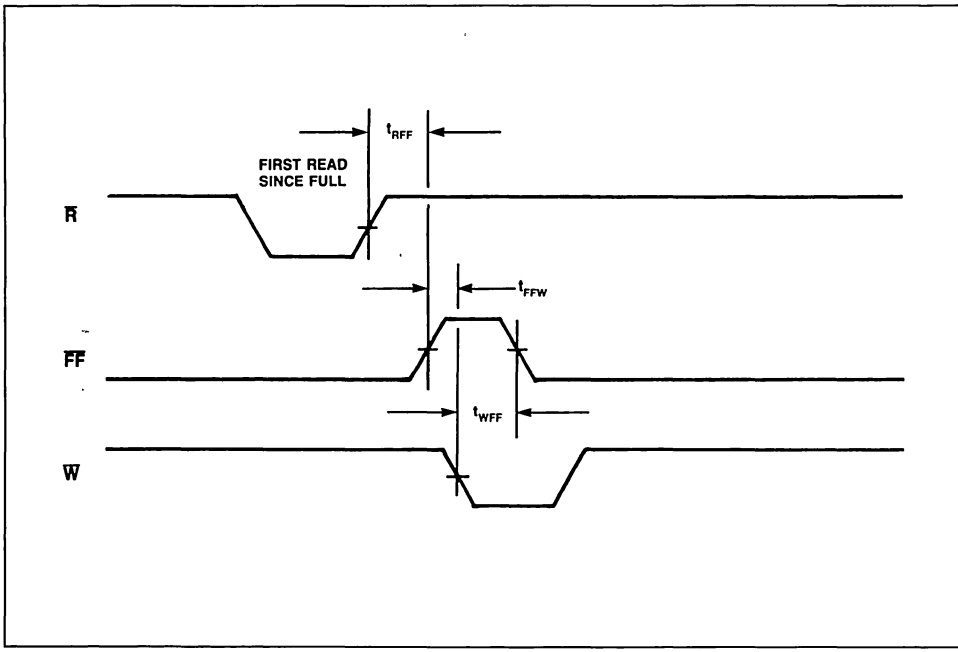
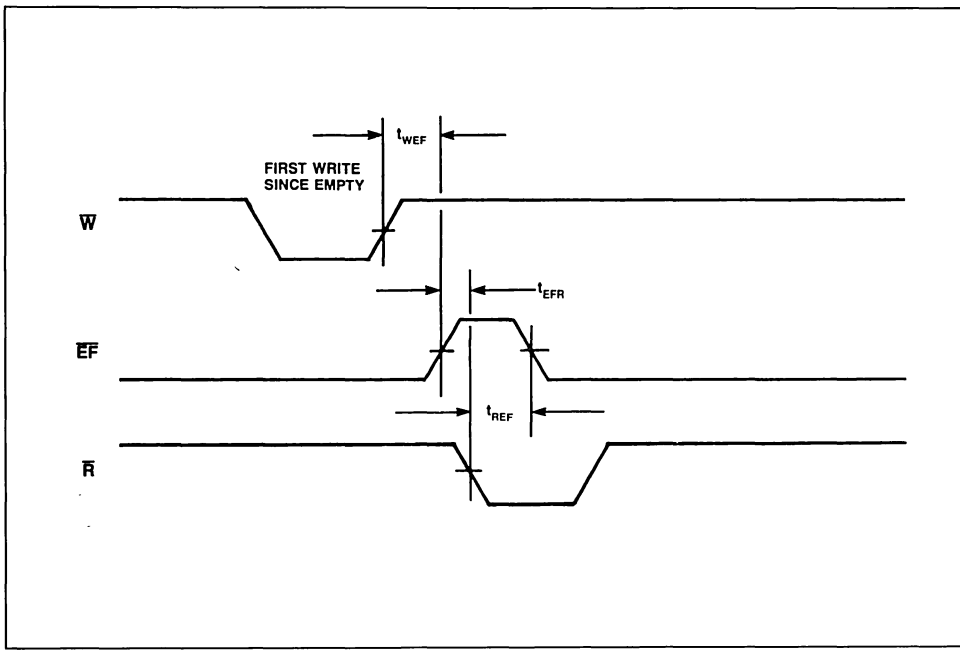


FIGURE 4B. WRITE/READ TO EMPTY FLAG

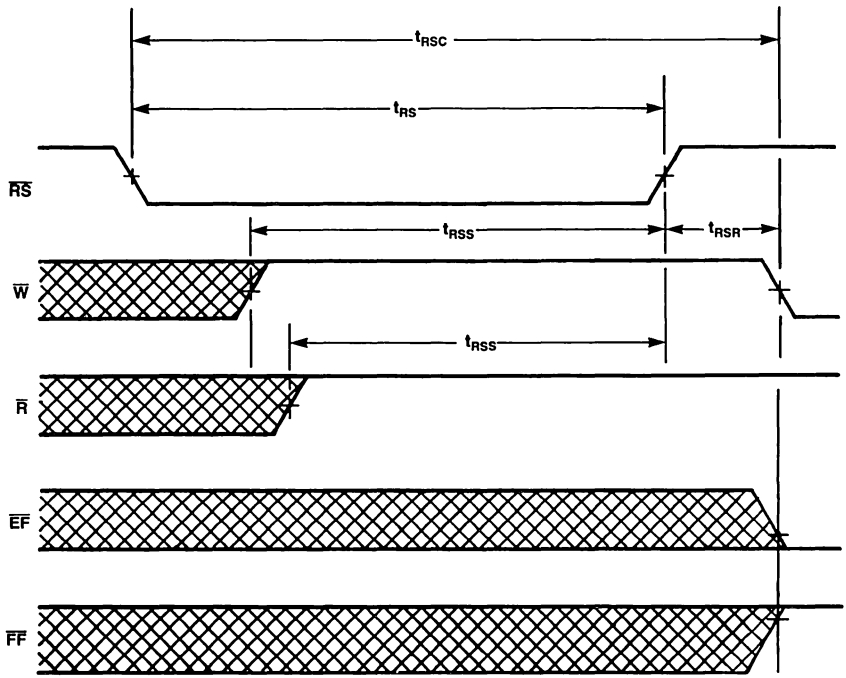


RESET

The MK4501 is reset (see Figure 5) whenever the Reset pin ($\overline{RS}$) is in the low state. During a Reset, both the internal read and write pointers are set to the first location. Reset is required after power up, before a Write operation can begin.

Although neither $\overline{W}$ or $\overline{R}$ need be high when $\overline{RS}$ goes low, both $\overline{W}$ and $\overline{R}$ must be high t_{RSS} before $\overline{RS}$ goes high, and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of $\overline{FL}/\overline{RT}$ and $\overline{XI}$ during Reset.

FIGURE 5. RESET



NOTE
$\overline{EF}$ and $\overline{FF}$ may change status during Reset, but flags will be valid at t_{RSC}.

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

		4501-65		4501-80		4501-10		4501-12		4501-15		4501-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RSC}	Reset Cycle Time	80		100		120		140		175		235		ns	
t_{RS}	Reset Pulse Width	65		80		100		120		150		200		ns	1
t_{RSR}	Reset Recovery Time	15		20		20		20		25		35		ns	
t_{RSS}	Reset Set Up Time	45		60		80		100		130		180		ns	

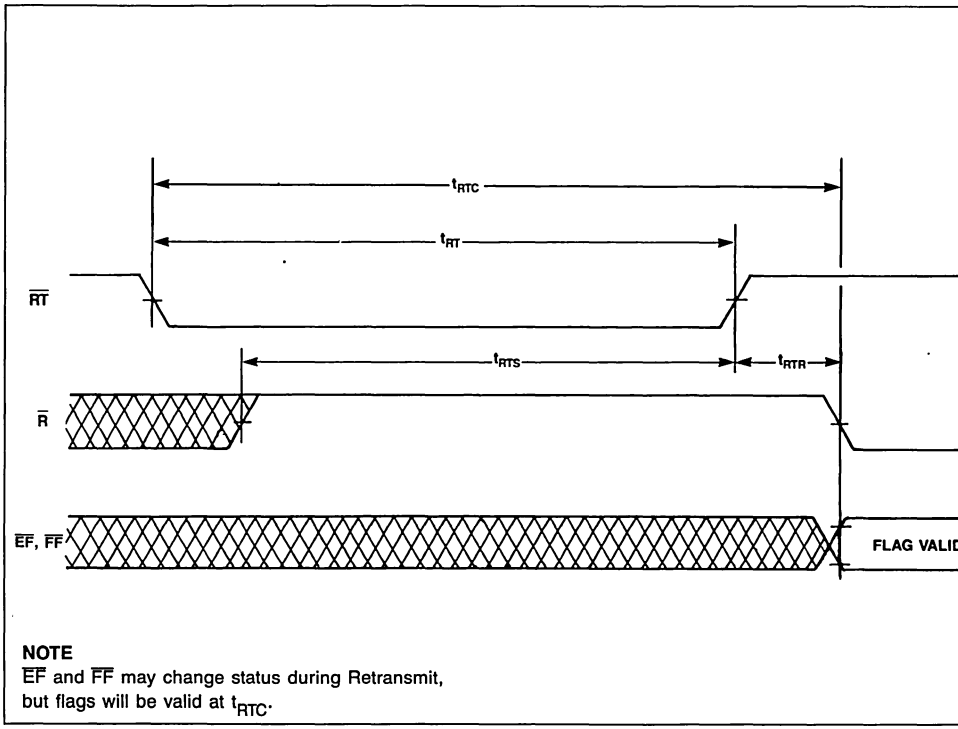
RETRANSMIT

The MK4501 can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low. (See Figure 6).

A Retransmit operation sets the internal read pointer to the first physical location in the array, but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high, and must remain high for t_{RTR} afterwards.

The Retransmit function is particularly useful when blocks of less than 512 Writes are performed between Resets. The Retransmit feature is not compatible with Depth Expansion.

FIGURE 6. RETRANSMIT



NOTE
$\overline{EF}$ and $\overline{FF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

AC ELECTRICAL CHARACTERISTICS
(0°C≤T_A≤ +70°C) (V_{CC} = +5.0 volts ± 10%)

		4501-65		4501-80		4501-10		4501-12		4501-15		4501-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RTC}	Retransmit Cycle Time	80		100		120		140		175		235		ns	
t_{RT}	Retransmit Pulse Width	65		80		100		120		150		200		ns	1
t_{RTR}	Retransmit Recovery Time	15		20		20		20		25		35		ns	
t_{RTS}	Retransmit Setup Time	45		60		80		100		130		180		ns	

SINGLE DEVICE CONFIGURATION

A single MK4501 may be used when application requirements are for 512 words or less. The MK4501 is placed in Single Device Configuration mode when the chip is Reset with the Expansion In pin ($\overline{XI}$) grounded (see Figure 7).

WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 8 demonstrates an 18-bit word width by using two MK4501s. Any word width can be attained by adding additional MK4501s.

FIGURE 7. A SINGLE 512 x 9 FIFO CONFIGURATION

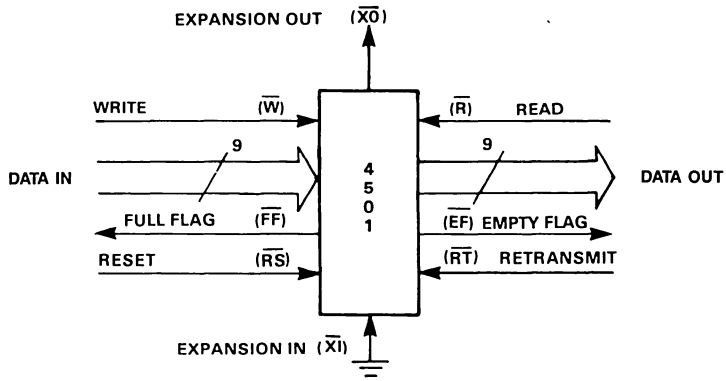
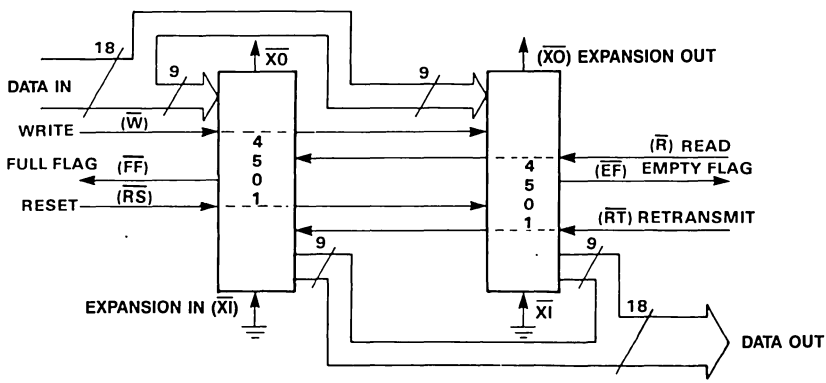


FIGURE 8. A 512 x 18 FIFO CONFIGURATION (WIDTH EXPANSION)



NOTE
Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$ signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

DEPTH EXPANSION (DAISY CHAIN)

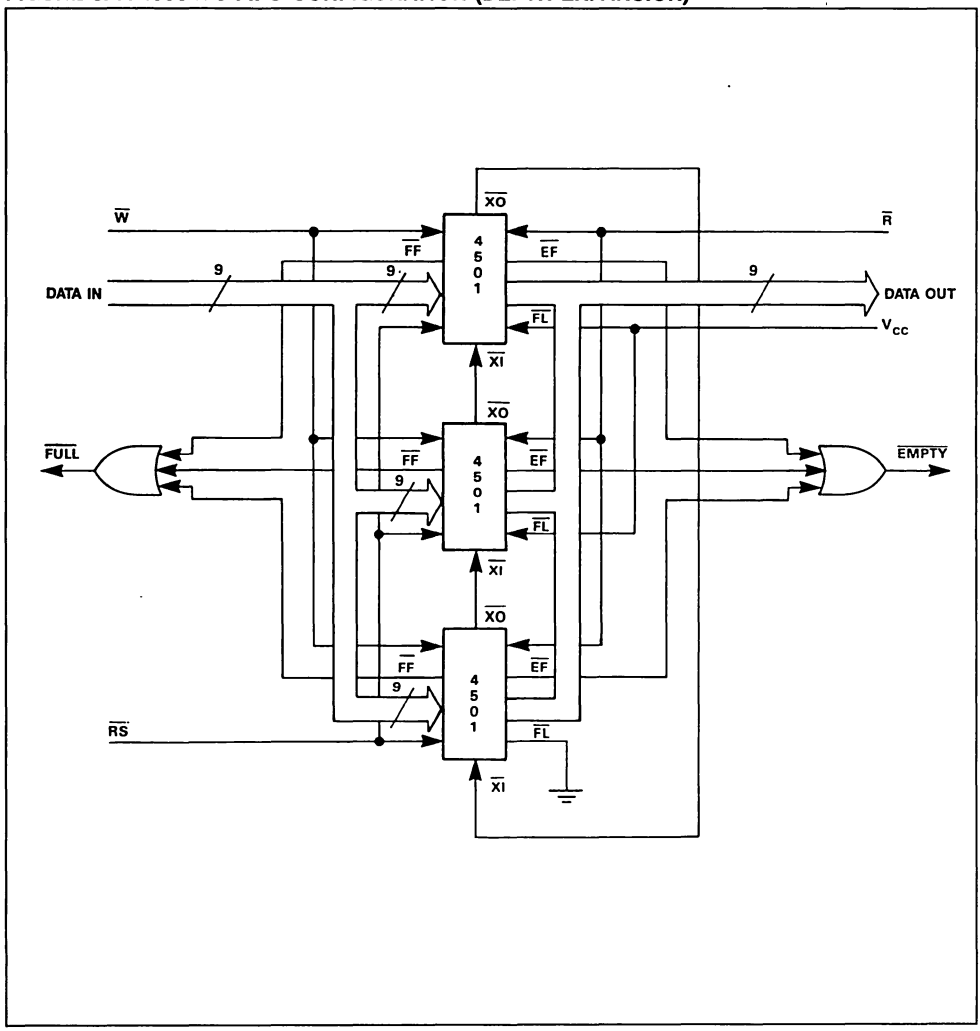
The MK4501 can easily be adapted to applications when the requirements are for greater than 512 words. Figure 9 demonstrates Depth Expansion using three MK4501s. Any depth can be attained by adding additional MK4501s.

External logic is needed to generate a composite Full Flag and Empty Flag. This requires the ORing of all $\overline{EF}$s and the ORing of all FFs (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).

The MK4501 operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions.

1. The first device must be designated by grounding the First Load pin ($\overline{FL}$). The Retransmit function is not allowed in the Depth Expansion Mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device.

FIGURE 9. A 1536 x 9 FIFO CONFIGURATION (DEPTH EXPANSION)

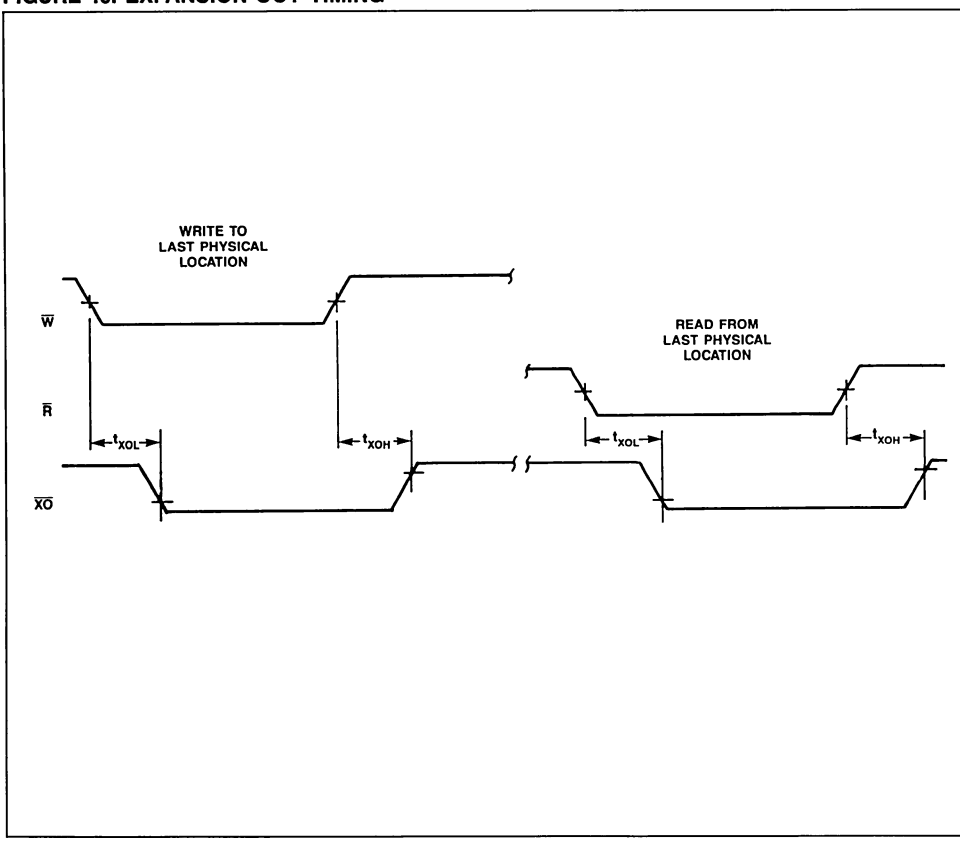


EXPANSION TIMING

Figures 10 and 11 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. Inasmuch as Expansion Out pins are generally connected only to Expansion In pins, the user need not be concerned with actual timing in a normal Depth Expanded application unless extreme propagation delays exist between the $\overline{XO}/\overline{XI}$ pin pairs.

Expansion Out pulses are the image of the WRITE and READ signals that cause them; delayed in time by t_{XOL} and t_{XOH}. The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and Empty Flags are activated, which is in response to writing and reading a last available location.

FIGURE 10. EXPANSION OUT TIMING



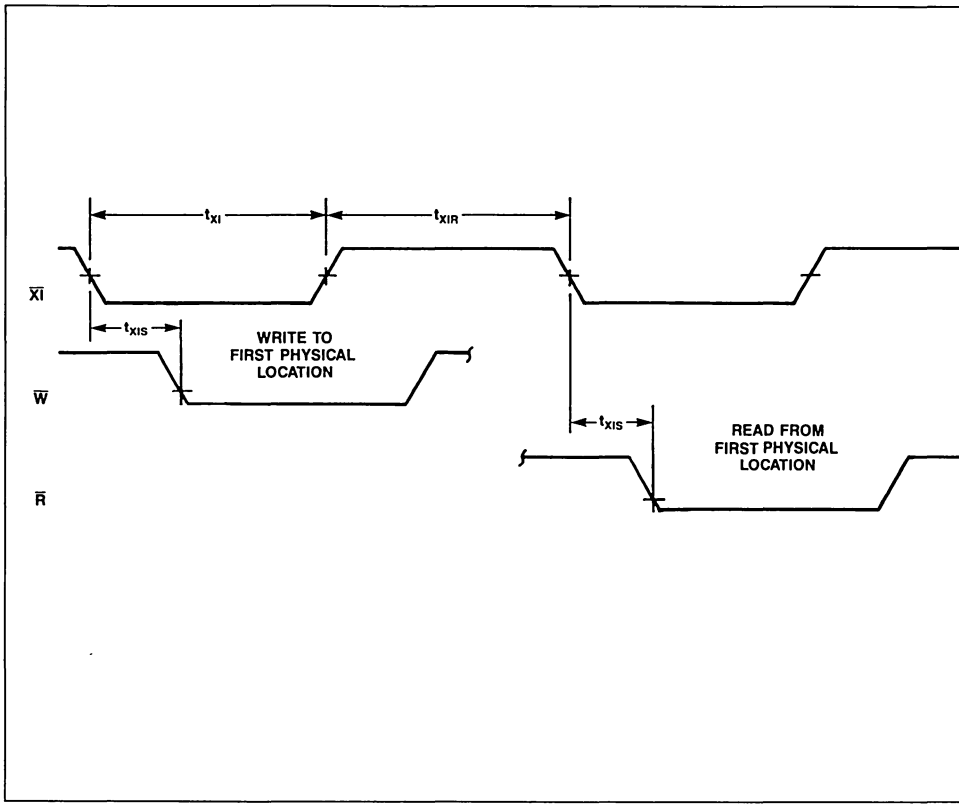
AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

		4501-65		4501-80		4501-10		4501-12		4501-15		4501-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{XOL}	Expansion Out Low		55		70		75		90		115		150	ns	
t_{XOH}	Expansion Out High		60		80		90		100		125		155	ns	

When in Depth Expansion mode, a given MK4501 will begin writing and reading as soon as valid WRITE and READ signals begin, provided $\overline{FL}$ was grounded at RESET time. A MK4501 in Depth Expansion mode with $\overline{FL}$ high at RESET will not begin writing until after an Expansion In pulse occurs. It will not begin reading until a second Expansion In pulse occurs and the Empty Flag has gone high. Expansion In pulses must occur t_{XIS} before the WRITE and READ signals they are intended to enable. Minimum Expansion In pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

FIGURE 11. EXPANSION IN TIMING



AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C) (V_{CC} = +5.0 volts ± 10%)

		4501-65		4501-80		4501-10		4501-12		4501-15		4501-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{XI}	Expansion In Pulse Width	60		75		95		115		145		195		ns	1
t_{XIR}	Expansion In Recovery Time	15		20		20		20		25		35		ns	
t_{XIS}	Expansion In Setup Time	25		30		45		50		60		85		ns	

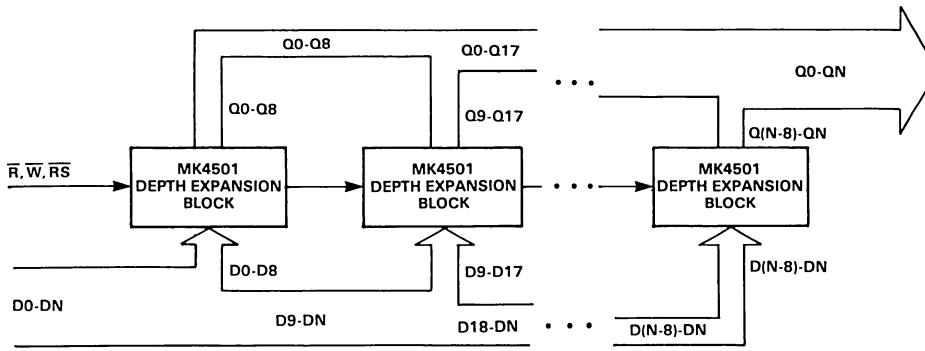
COMPOUND EXPANSION

The two expansion techiques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 12).

BIDIRECTIONAL APPLICATIONS

Applications, which require data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing MK4501s, as shown in Figure 13. Care must be taken to assure that the appropriate flag is monitored by each system. (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used.) Both Depth Expansion and Width Expansion may be used in this mode.

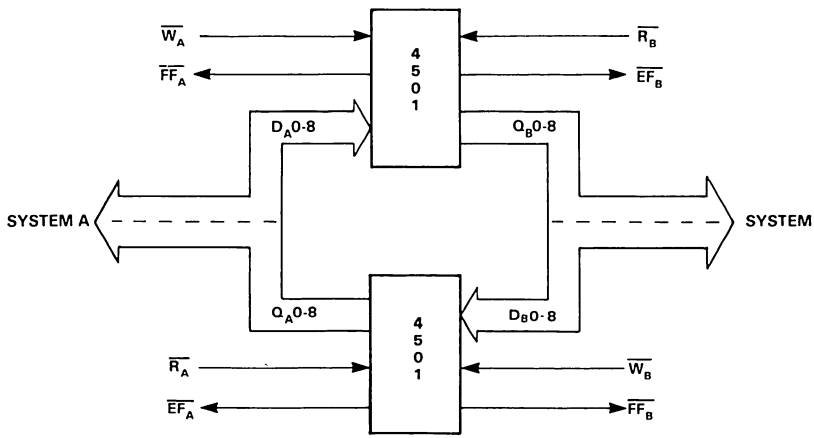
FIGURE 12. COMPOUND FIFO EXPANSION



NOTES

1. For depth expansion block see DEPTH EXPANSION Section and Figure 9.
2. For Flag operation see WIDTH EXPANSION Section and Figure 8.

FIGURE 13. BIDIRECTIONAL FIFO APPLICATION



ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND ..... -0.5 V to + 7.0 V
Operating Temperature T_A (Ambient) ..... 0°C to + 70°C
Storage Temperature ..... -55°C to + 125°C
Total Device Power Dissipation ..... 1 Watt
Output Current per Pin ..... 20 mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions above those indicated in the operational sections of this specification, is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	3
GND	Ground	0	0	0	V	
V_{IH}	Logic "1" Voltage All Inputs	2.0		V_{CC} + 1	V	3
V_{IL}	Logic "0" Voltage All Inputs	-0.3		0.8	V	3, 4

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = 5.0 volts ± 10%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{IL}	Input Leakage Current (Any Input)	-1	1	μA	5
I_{OL}	Output Leakage Current	-10	10	μA	6
V_{OH}	Output Logic "1" Voltage I_{OUT} = -1 mA	2.4		V	3
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4 mA		0.4	V	3
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	7
I_{CC2}	Average Standby Current ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL/RT} = V_{IH}$)		8	mA	7
I_{CC3}	Power Down Current (All Inputs ≥ V_{CC} -0.2 V)		500	μA	7

AC ELECTRICAL CHARACTERISTICS

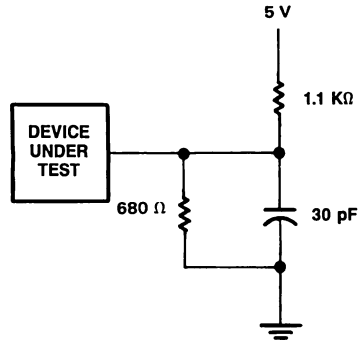
(T_A = 25°C, f = 1.0 MHz)

SYM	PARAMETER	TYP	MAX	NOTES
C_I	Capacitance on Input Pins		7 pF	
C_Q	Capacitance on Output Pins		12 pF	8

NOTES

1. Pulse widths less than minimum values are not allowed.
2. Measured using output load shown in Output Load Diagram.
3. All voltages are referenced to ground.
4. −1.5 volt undershoots are allowed for 10 ns once per cycle.
5. Measured with $0.4 \leq V_{IN} \leq V_{CC}$.
6. $\overline{R} \geq V_{IH}$, $0.4 \geq V_{OUT} \leq V_{CC}$.
7. I_{CC} measurements are made with outputs open.
8. With output buffer deselected.

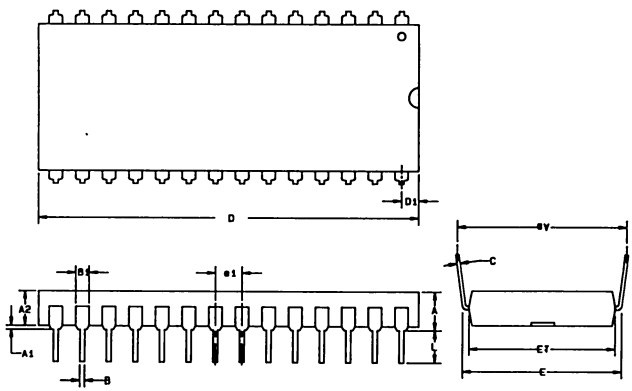
FIGURE 14. OUTPUT LOAD



AC TEST CONDITIONS:

Input Levels ..... GND to 3.0 V
Transition Times ..... 5 ns
Input Signal Timing Reference Level ..... 1.5 V
Output Signal Timing Reference Level 0.8 V and 2.2 V
Ambient Temperature ..... 0°C to 70°C
V_{CC} ..... 5.0 V ± 10%

FIGURE 15. MK4501 PLASTIC (N TYPE) DUAL-IN-LINE, 28 PINS

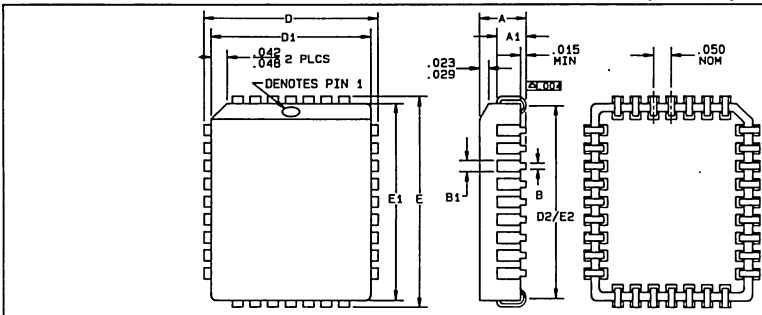


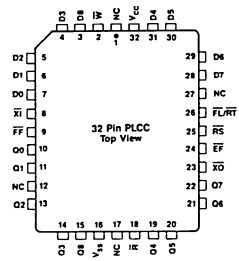
Dim.	mm		inches		Notes
	Min	Max	Min	Max	
A	—	5.334	—	210	2
A1	0.381	—	.015	—	2
A2	3.556	4.064	.140	.160	
B	0.381	0.533	.015	.021	3
B1	1.27	1.778	.050	.070	
C	0.203	0.304	.008	.012	3
D	36.576	37.338	1.440	1.470	1
D1	1.651	2.159	.065	.085	
E	15.24	15.875	.600	.625	
E1	13.462	14.224	.530	.560	
e1	2.286	2.794	.090	.110	
eA	15.24	17.78	.600	.700	
L	3.048	—	.120	—	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

FIGURE 16. MK4501 PLASTIC LEADED CHIP CARRIER, 32 PIN (K TYPE)





Dim.	mm		inches	
	Min	Max	Min	Max
A	3.048	3.556	.120	.140
A1	1.981	2.413	.078	.095
B	0.330	0.533	.013	.021
B1	0.660	0.812	.026	.032
D	12.319	12.573	.485	.495
D1	11.353	11.506	.447	.453
D2	9.906	10.922	.390	.430
E	14.859	15.113	.585	.595
E1	13.893	14.046	.547	.553
E2	12.446	13.462	.490	.530

ORDERING INFORMATION

PART NO.	ACCESS TIME	R/W CYCLE TIME	CLOCK FREQ.	PACKAGE TYPE	TEMPERATURE RANGE
MK4501N-65	65 ns	80 ns	12.5 MHz	28 Pin Plastic DIP	0° to 70°C
MK4501N-80	80 ns	100 ns	10.0 MHz	28 Pin Plastic DIP	0° to 70°C
MK4501N-10	100 ns	120 ns	8.3 MHz	28 Pin Plastic DIP	0° to 70°C
MK4501N-12	120 ns	140 ns	7.1 MHz	28 Pin Plastic DIP	0° to 70°C
MK4501N-15	150 ns	175 ns	5.7 MHz	28 Pin Plastic DIP	0° to 70°C
MK4501N-20	200 ns	235 ns	4.2 MHz	28 Pin Plastic DIP	0° to 70°C
MK4501K-65	65 ns	80 ns	12.5 MHz	32 Pin Plastic LCC	0° to 70°C
MK4501K-80	80 ns	100 ns	10.0 MHz	32 Pin Plastic LCC	0° to 70°C
MK4501K-10	100 ns	120 ns	8.3 MHz	32 Pin Plastic LCC	0° to 70°C
MK4501K-12	120 ns	140 ns	7.1 MHz	32 Pin Plastic LCC	0° to 70°C
MK4501K-15	150 ns	175 ns	5.7 MHz	32 Pin Plastic LCC	0° to 70°C
MK4501K-20	200 ns	235 ns	4.2 MHz	32 Pin Plastic LCC	0° to 70°C

MK — SGS-THOMSON Prefix

4501 — Device family and number identification

N — Package type
N: Plastic DIP
K: Plastic LCC

65 — Speed grade Access Time

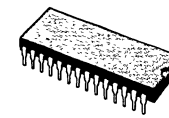
SGS-THOMSON MICROELECTRONICS

MK4503(N) 65/80/10/12/15/20

2048 x 9 CMOS BiPORT FIFO

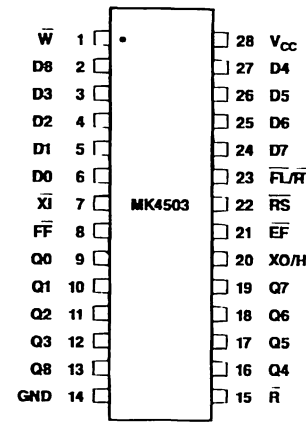
ADVANCE DATA

- FIRST-IN, FIRST-OUT MEMORY BASED ARCHITECTURE
- FLEXIBLE 2048 x 9 ORGANIZATION
- LOW POWER HCMOS TECHNOLOGY
- ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE
- BIDIRECTIONAL APPLICATIONS
- FULLY EXPANDABLE BY WORD WIDTH OR DEPTH
- EMPTY AND FULL WARNING FLAGS
- RETRANSMIT CAPABILITY
- HIGH PERFORMANCE
- HALF FULL FLAG IN SINGLE DEVICE MODE



N
DIP–28
(Plastic Package)

Figure 1 : Pin Connections.



DESCRIPTION

The MK4503 is a member of the BiPORT™ Memory Series, which utilizes special two-port cell techniques. Specifically, this device implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full, half full and empty flags, and unlimited expansion capability in both word size and depth. The main application of the MK4503 is as a rate buffer, sourcing and absorbing data at different rates, (e.g., interfacing fast processors and slow peripherals). The full, half full and empty flags are provided to prevent data overflow and underflow. The data is loaded and emptied on a First-In, First-Out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the writes and reads are internally sequential, thereby requiring no address information, the pinout definition will serve this and future high-density devices. The ninth bit is provided to support control or parity functions.

PIN NAMES

$\overline{W}$	= Write	$\overline{XI}$	= Expansion in
$\overline{R}$	= Read	$\overline{XO/HF}$	= Expansion out Half Full Flag
$\overline{RS}$	= Reset	$\overline{FF}$	= Full Flag
$\overline{FL/RT}$	= First Load/ Retransmit	$\overline{EF}$ V_{CC}	= Empty Flag = 5V
D	= Data in	GND	= Ground
Q	= Data out	NC	= No Connection

FUNCTIONAL DESCRIPTION

Unlike conventional shift register based FIFOs, the MK4503 employs a memory-based architecture wherein a byte written into the device does not "ripple-through". Instead, a byte written into the MK4503 is stored at a specific location, where it remains until over-written. The byte can be read and re-read as often as desired in the single device configuration.

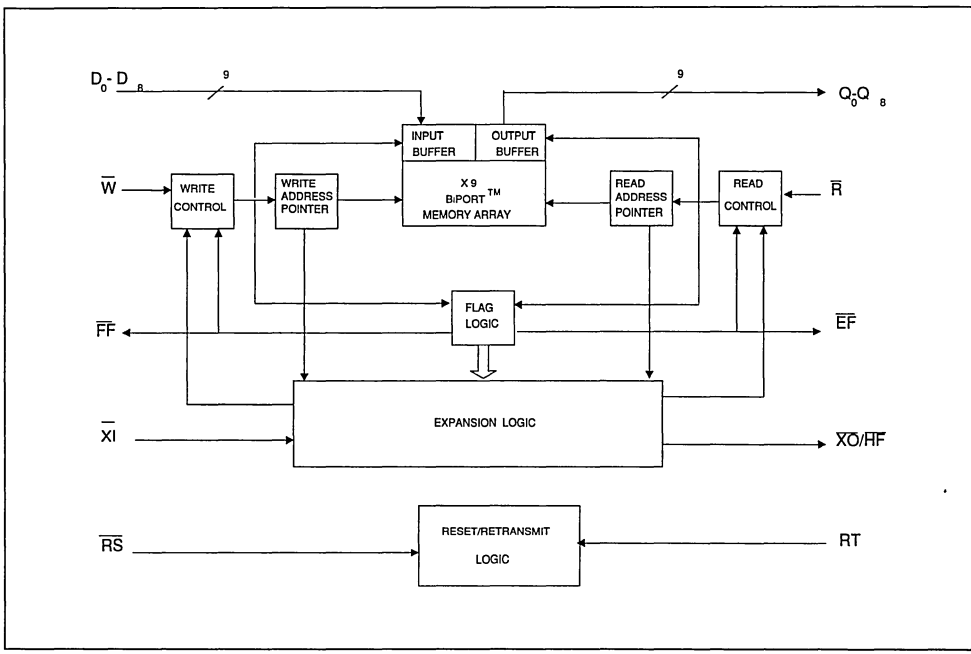
Twin internal pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written.

The address pointers automatically loop back to address zero after reaching address 2047. The empty/half full and full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

Resetting the FIFO simply resets the write and read pointers to location zero. Pulsing retransmit resets the read address pointer without affecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading the individual FIFOs. The penalty of cascading is often unacceptable ripple-through delays. The 4503 allows implementation of very large FIFOs with no timing penalties. The memory-based architecture of the MK4503 allows connecting the read, write, data in, and data out lines of the MK4503s in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in and expansion-out pins.

Figure 2 : MK4503 Block Diagram.



ABSOLUTE MAXIMUM RATINGS*

Parameter	Value	Unit
Voltage on any Pin Relative to GND	- 0.5 to + 7.0	V
Operating Temperature T_A (ambient)	0 to + 70	°C
Storage Temperature	- 55 to + 125	°C
Total Device Power Dissipation	1	Watt
Output Current per Pin	20	mA

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions above those indicated in the operational sections of this specification, is not implied. Exposure to absolute maximum ratings for extended periods may affect device

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq + 70°C$)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	3
GND	Ground	0	0	0	V	
V_{IH}	Logic "1" Voltage all Inputs	2.0		V_{CC} + .3	V	3, 9
V_{IL}	Logic "0" Voltage all Inputs	- 0.3		0.8	V	3, 4, 9

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq + 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
I_{IL}	Input Leakage Current (any input)	- 1		1	µA	5
I_{OL}	Output Leakage Current	- 10		10	µA	6
V_{OH}	Output Logic "1" Voltage I_{OUT} = - 1mA	2.4			V	3
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4mA			0.4	V	3
I_{CC1}	Average V_{CC} Power Supply Current			120	mA	7
I_{CC2}	Average Standby Current ($\overline{R} = W = \overline{RS} = FL/\overline{RT} = V_{IH}$)			12	mA	7
I_{CC3}	Power Down Current (all inputs ≥ V_{CC} - 0.2V)			4	µA	7

AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq + 70°C$) ($V_{CC} = + 5.0V \pm 10\%$)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
C_I	Capacitance on Input Pins			7	pF	
C_O	Capacitance on Output Pins			12	pF	8

Notes : 1. Pulse widths less than minimum values are not allowed.
2. Measured using output load shown in Output Load Circuit.
3. All voltages are referenced to ground.
4. – 1.5 volt undershoots are allowed for 10ns once per cycle.
5. Measured with $0.0 \leq V_{IN} \leq V_{CC}$.
6. $\overline{R} \geq V_{IH}$, $0.0 \geq V_{OUT} \leq V_{CC}$.
7. I_{CC} measurements are made with outputs open.
8. With output buffer deselected.
9. Input levels tested at 500ns cycle time.

AC TEST CONDITIONS :

Input Levels..... GND to 3.0V

Transition Times..... 5ns

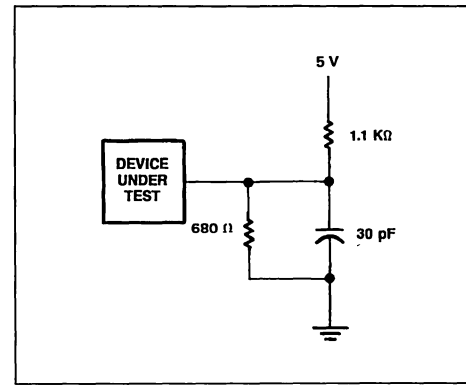
Input Signal Timing
Reference Level..... .5

Output Signal Timing
Reference Level..... 0.8V and 2.2V

Ambient Temperature..... 0°C to 70°C

V_{CC} ..... 5.0V ± 10%

Figure 3 : Output Load Circuit.

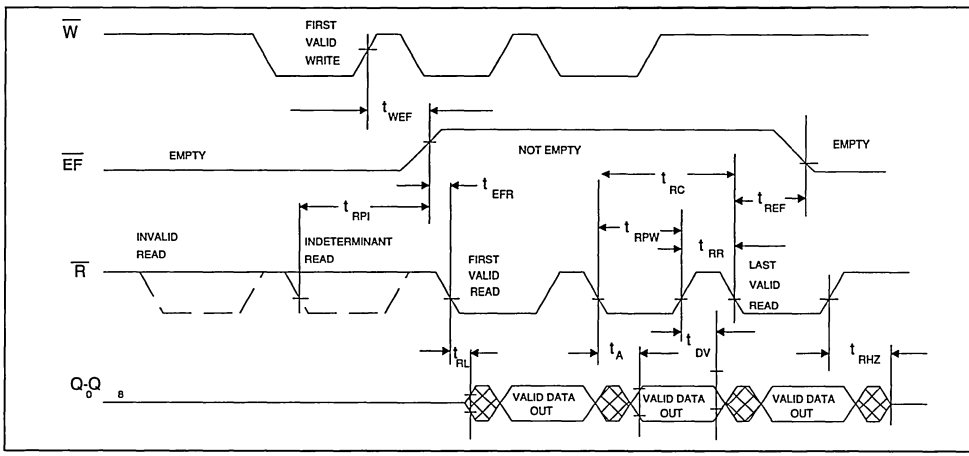


READ MODE

The MK4503 initiates a Read Cycle (see figure 4) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not asserted. In the Read mode of operation, the MK4503 provides a fast access to data from 9 of 18432 locations in the static storage array. The data is accessed on a FIFO basis independent of any on-going WRITE operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next Read operation.

In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further Read operations will be inhibited (the data outputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid Write operation. $\overline{EF}$ will again go low t_{REF} from the beginning a subsequent READ operation, provided that a second WRITE has not been completed (see figure 6B). Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more than t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less than t_{EFR} later may or may not occur (be valid) depending on internal flag status.

Figure 4 : Read And Empty Flag Timing.



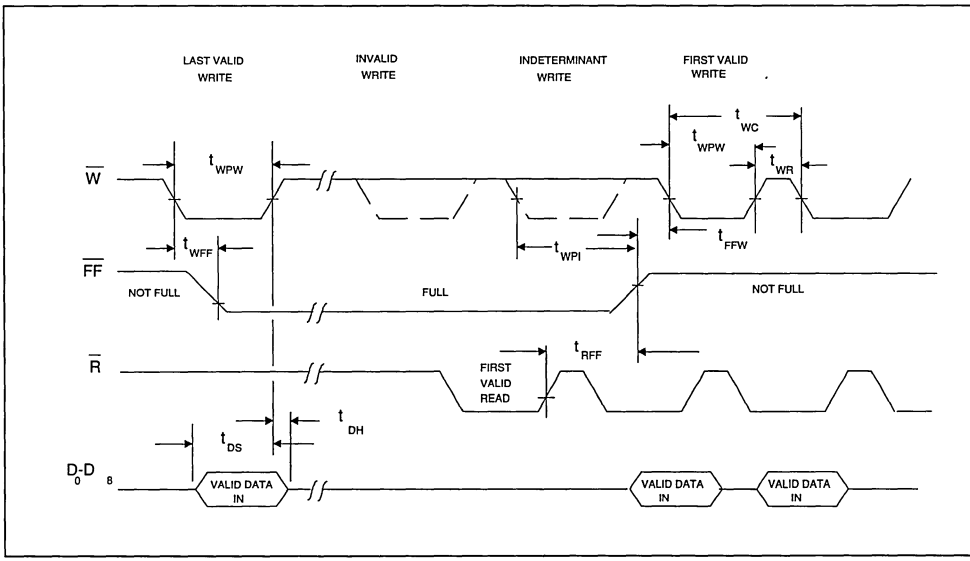
AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = +5.0volts \pm 10\%$)

Sym.	Parameter	4503-65		4503-80		4503-10		4503-12		4503-15		4503-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	80		100		120		140		175		235		ns	
t_A	Access Time		65		80		100		120		150		200	ns	2
t_{RR}	Read Recovery Time	15		20		20		20		25		35		ns	
t_{RPW}	Read Pulse Width	65		80		100		120		150		200		ns	1
t_{RL}	$\overline{R}$ Low to Low Z	0		0		0		0		0		0		ns	2
t_{DV}	Data Valid from $\overline{R}$ High	5		5		5		5		5		5		ns	2
t_{RHZ}	$\overline{R}$ High to High Z		25		25		25		35		50		60	ns	2
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low		60		75		95		115		145		195	ns	2
t_{EFR}	$\overline{EF}$ High to Valid Read	10		10		10		10		10		10		ns	2
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High		60		75		95		110		140		190	ns	2
t_{RPI}	Read Protect Indeterminant		35		35		35		35		35		35	ns	2

WRITE MODE

The MK4503 initiates a Write Cycle (see figure 5) on the falling edge of the Write Enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not asserted. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing Read operations. $\overline{FF}$ is asserted during the last valid write as the MK4503 becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go high t_{RFF} after completion of a valid READ operation. $\overline{FF}$ will again go low t_{WFF} from the beginning of a subsequent WRITE operation, provided that a second READ has not been completed (see figure 6A). Writes beginning t_{FFW} after $\overline{FF}$ goes high are valid. Writes beginning after $\overline{FF}$ goes low and more than t_{WPI} before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on internal flag status.

Figure 5 : Write And Full Flag Timing.



AC ELECTRICAL CHARACTERISTICS ($0°C \le T_A \le +70°C$) ($V_{CC} = +5.0$volts $\pm 10\%$)

Sym.	Parameter	4503-65		4503-80		4503-10		4503-12		4503-15		4503-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	80		100		120		140		175		235		ns	
t_{WPW}	Write Pulse Width	65		80		100		120		150		200		ns	1
t_{WR}	Write Recovery Time	15		20		20		20		25		35		ns	
t_{DS}	Data Set Up Time	30		40		40		40		50		65		ns	
t_{DH}	Data Hold Time	10		10		10		10		10		10		ns	
t_{WFF}	$\overline{W}$ Low to $\overline{FF}$ Low		60		70		95		115		145		195	ns	2
t_{FFW}	$\overline{FF}$ High to Valid Write	10		10		10		10		10		10		ns	2
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High		60		70		95		110		140		190	ns	2
t_{WPI}	Write Protect Indeterminant		35		35		35		35		35		35	ns	2

Figure 6a : Read/write To Full Flag.

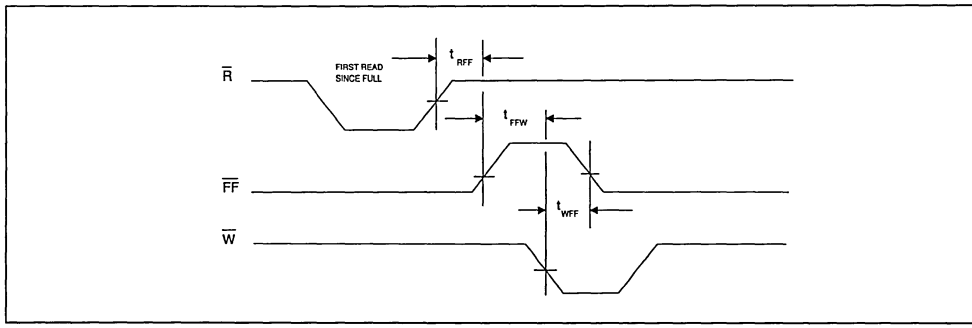
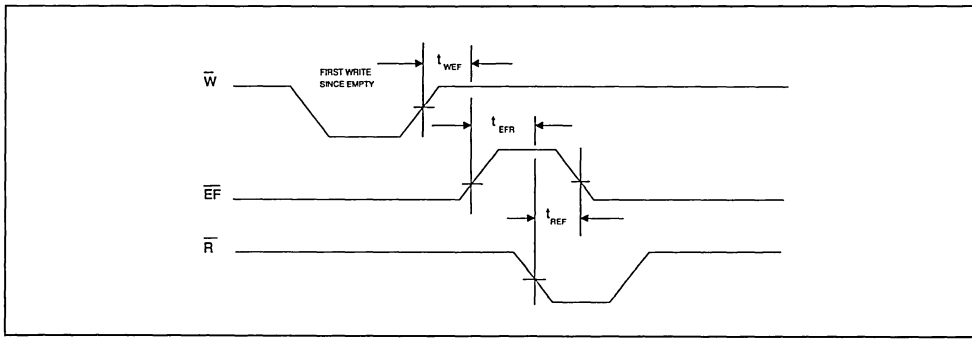


Figure 6b : Write/read To Empty Flag.

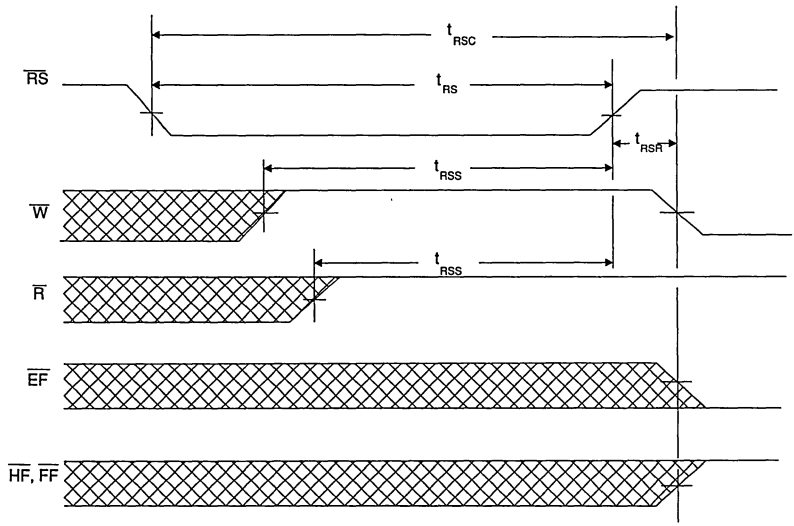


RESET

The MK4503 is reset (see figure 7) whenever the Reset pin ($\overline{RS}$) is in the low state. During a Reset, both the internal read and write pointers are set to the first location. Reset is required after power up, before a Write operation can begin.

Although neither $\overline{W}$ or $\overline{R}$ need be high when $\overline{RS}$ goes low, both $\overline{W}$ and $\overline{R}$ must be high t_{RSS} before $\overline{RS}$ goes high, and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of $\overline{FL}/\overline{RT}$ and $\overline{XI}$ during Reset.

Figure 7 : Reset.



Note : $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Reset, but flags will be valid at t_{RSC}.

AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = +5.0volts \pm 10\%$)

Sym.	Parameter	4503-65		4503-80		4503-10		4503-12		4503-15		4503-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RSC}	Reset Cycle Time	80		100		120		140		175		235		ns	
t_{RS}	Reset Pulse Width	65		80		100		120		150		200		ns	1
t_{RSR}	Reset Recovery Time	15		20		20		20		25		35		ns	
t_{RSS}	Reset Set Up Time	45		60		80		100		130		180		ns	

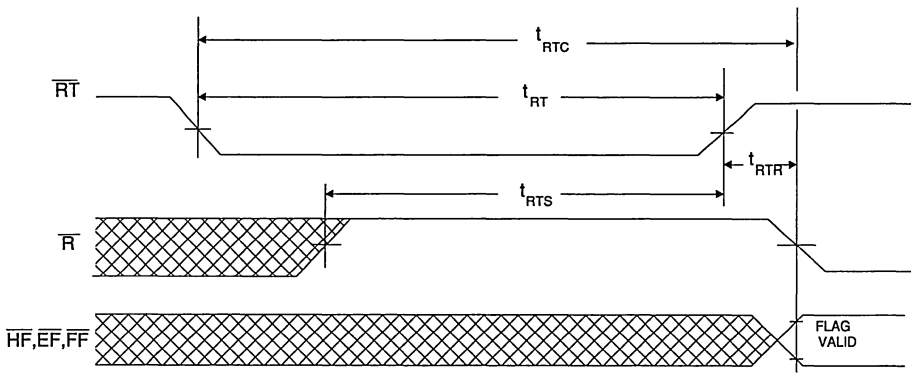
RETRANSMIT

The MK4503 can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low. (See figure 8).

A Retransmit operation sets the internal read pointer to the first physical location in the array, but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high, and must remain high for t_{RTR} afterwards.

The Retransmit function is particularly useful when blocks of less than 2048 Writes are performed between Resets. The Retransmit feature is not compatible with Depth Expansion.

Figure 8 : Retransmit.



Note : $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = +5.0volts \pm 10\%$)

Sym.	Parameter	4503-65		4503-80		4503-10		4503-12		4503-15		4503-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RTC}	Retransmit Cycle Time	80		100		120		140		175		235		ns	
t_{RT}	Retransmit Pulse Width	65		80		100		120		150		200		ns	1
t_{RTR}	Retransmit Recovery Time	15		20		20		20		25		35		ns	
t_{RTS}	Retransmit Setup Time	45		60		80		100		130		180		ns	

SINGLE DEVICE CONFIGURATION

A single MK4503 may be used when application requirements are for 2048 words or less. The MK4503 is placed in Single Device Configuration mode when the chip is Reset with the Expansion In pin ($\overline{XI}$) grounded (see figure 9).

WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 10 demonstrates an 18-bit word width by using two MK4503s. Any word width can be attained by adding additional MK4503s. The half full flag ($\overline{HF}$) operates the same as in the single device configuration.

Figure 9 : A Single 2047 x 9 FIFO Configuration.

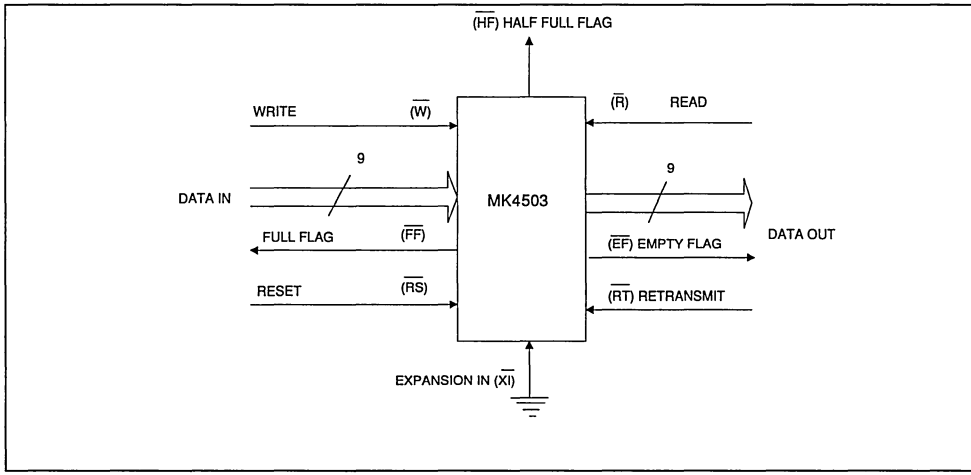
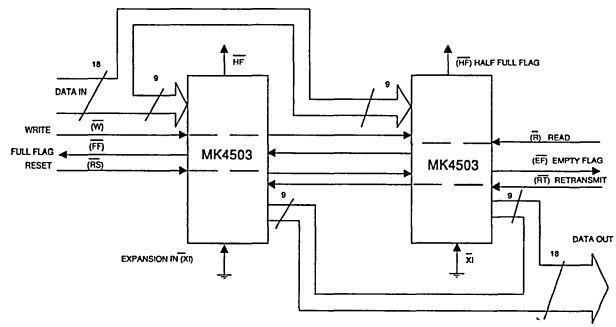


Figure 10 : A 2048 x 18 FIFO Configuration (width expansion).

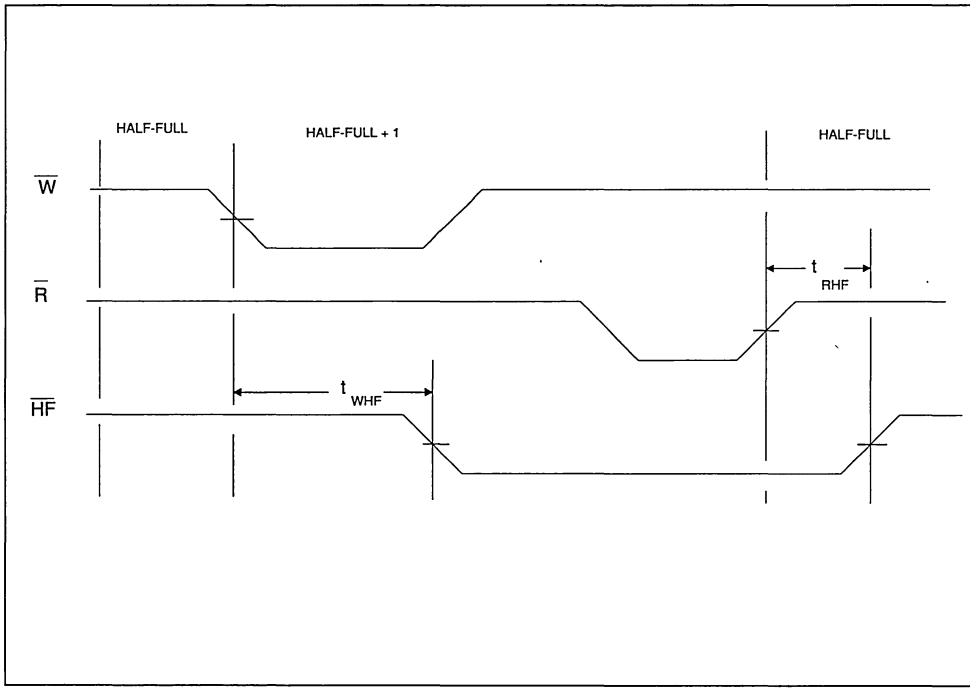


Note : Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$ signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

HALF FULL FLAG LOGIC

When in single device configuration, the ($\overline{HF}$) output acts as an indication of a half full memory. After half of the memory is filled, and at the falling edge of the next write operation, the half full flag ($\overline{HF}$) will be set low and remain low until the difference between the write pointer and read pointer is less than or equal to one half the total memory. The half full flag ($\overline{HF}$) is then reset by the rising edge of the read operation (see figure 11).

Figure 11 : Half Full Flag Timing.



AC CHARACTERISTICS (0°C ≤ T_A ≤ + 70°C) (V_{CC} = + 5volts ± 10%)

Sym.	Parameter	4503-65		4503-80		4503-10		4503-12		4503-15		4503-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WHF}	Write Low to Half Full Flag Low		80		100		120		140		175		235	ns	
t_{RHF}	Read High to Half Full Flag High		80		100		120		140		175		235	ns	

DEPTH EXPANSION (daisy chain)

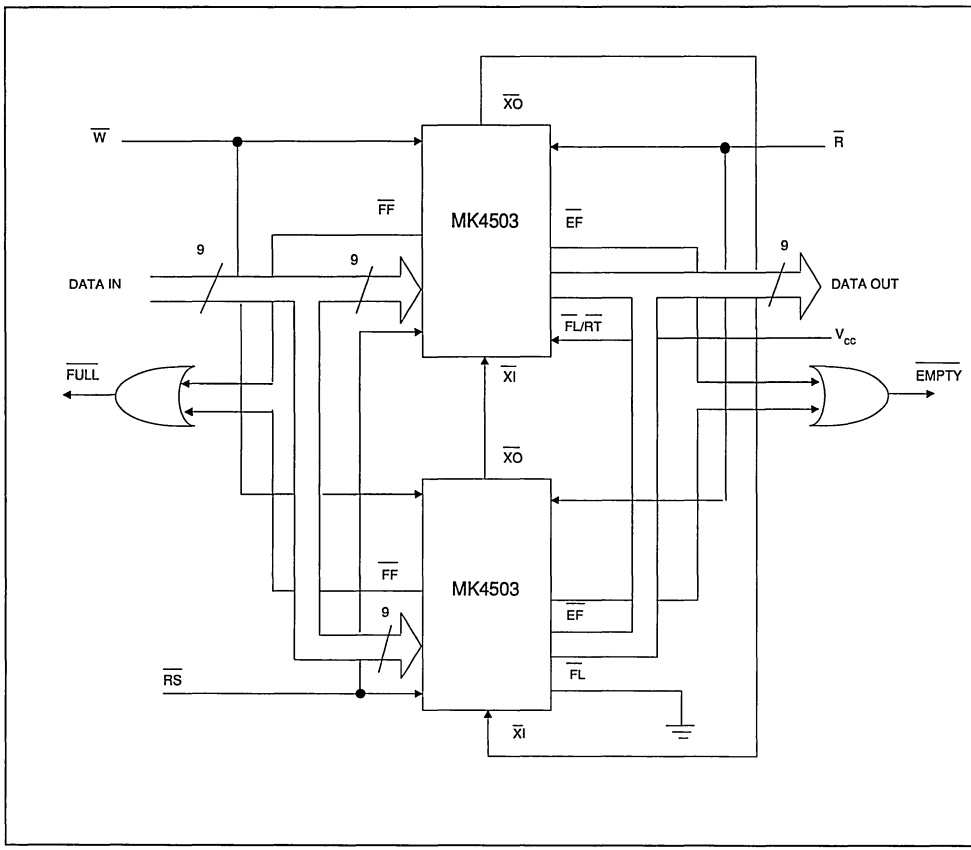
The MK4503 can easily be adapted to applications when the requirements are for greater than 2048 words. Figure 12 demonstrates Depth Expansion using the MK4503s. Any depth can be attained by adding additional MK4503s.

External logic is needed to generate a composite Full Flag and Empty Flag. This requires the ORing of all $\overline{EF}$s and the ORing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).

The MK4503 operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions.

1. The first device must be designated by grounding the First Load pin ($\overline{FL}$). The Retransmit function is not allowed in the Depth Expansion Mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. The Half Full Flag ($\overline{HF}$) is disabled in this

Figure 12 : A 4K x 9 FIFO Configuration (depth expansion).

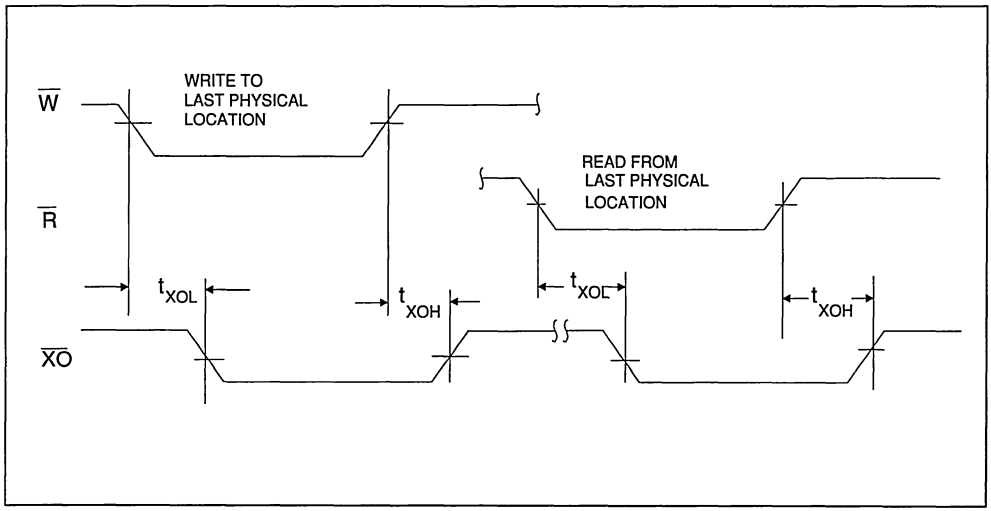


EXPANSION TIMING

Figures 13 and 14 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. Inasmuch as Expansion Out pins are generally connected only to Expansion In pins, the user need not be concerned with actual timing in a normal Depth Expanded application unless extreme propagation delays exist between the $\overline{XO}/\overline{XI}$ pin pairs.

Expansion Out pulses are the image of the WRITE and READ signals that cause them ; delayed in time by t_{XOL} and t_{XOH}. The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and Empty Flags are activated, which is in response to writing and reading a last available location.

Figure 13 : Expansion Out timing.



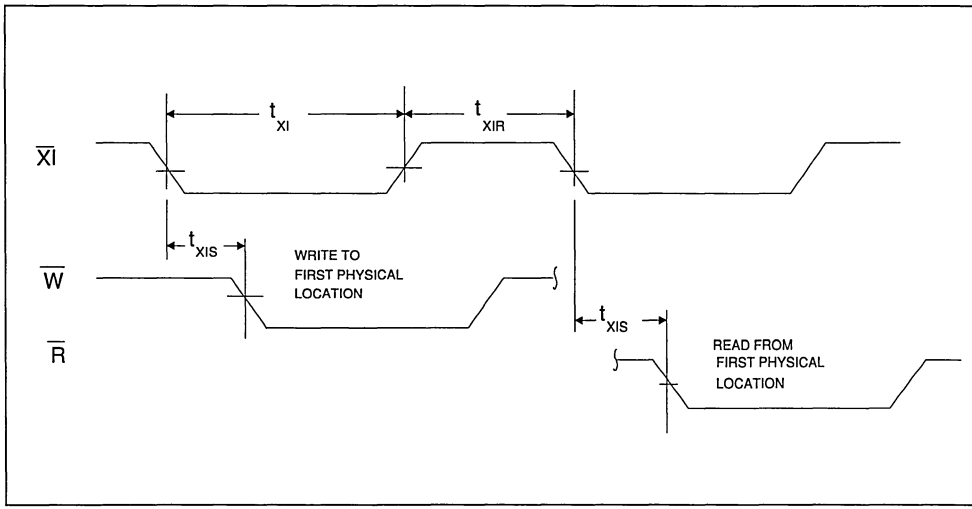
AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = +5.0$volts $\pm 10\%$)

Sym.	Parameter	4503-65		4503-80		4503-10		4503-12		4503-15		4503-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XOL}	Expansion Out Low		55		70		75		90		115		150	ns	
t_{XOH}	Expansion Out High		60		80		90		100		125		155	ns	

When in Depth Expansion mode, a given MK4503 will begin writing and reading as soon as valid WRITE and READ signals begin, provided $\overline{FL}$ was grounded at RESET time. A MK4503 in Depth Expansion mode with $\overline{FL}$ high at RESET will not begin writing until after an Expansion In pulse occurs.

It will not begin reading until a second Expansion In pulse occurs and the Empty Flag has gone high. Expansion In pulses must occur t_{XIS} before the WRITE and READ signals they are intended to enable. Minimum Expansion In pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

Figure 14 : Expansion In Timing.



AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = +5.0volts \pm 10\%$)

Sym.	Parameter	4503-65		4503-80		4503-10		4503-12		4503-15		4503-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XI}	Expansion in Pulse Width	60		75		95		115		145		195		ns	1
t_{XIR}	Expansion in Recovery Time	15		20		20		20		25		35		ns	
t_{XIS}	Expansion in Setup Time	25		30		45		50		60		85		ns	

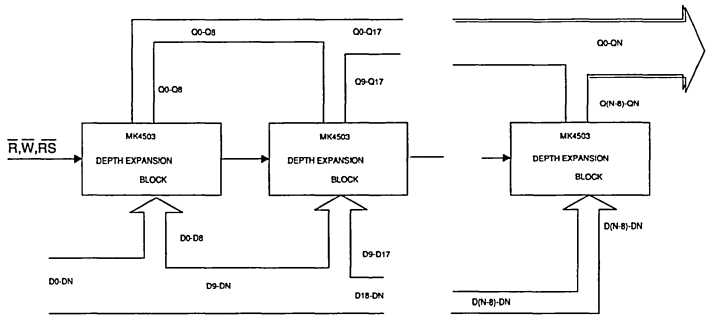
COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see figure 15).

BIDIRECTIONAL APPLICATIONS

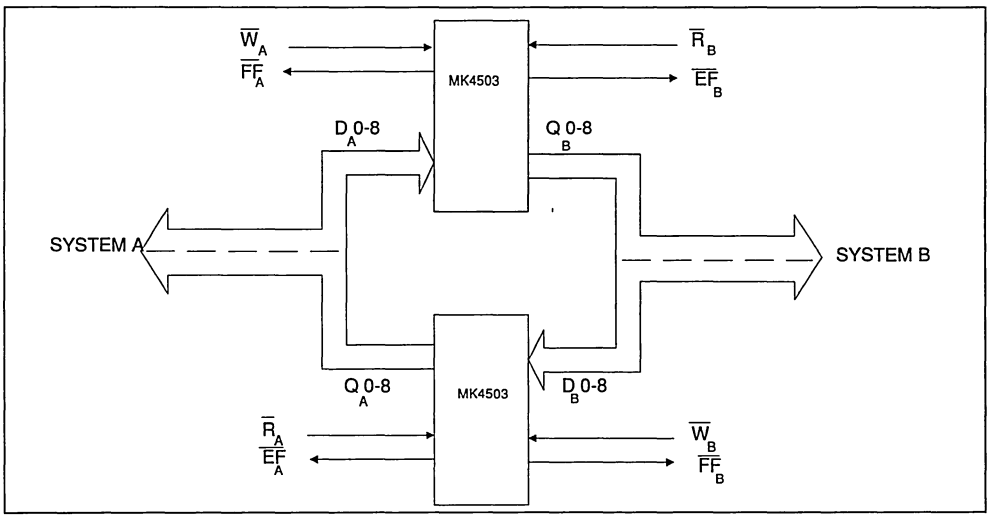
Applications, which require data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing MK4503s, as shown in figure 16. Care must be taken to assure that the appropriate flag is monitored by each system. (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used ; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

Figure 15 : Compound Fifo Expansion.



Notes : 1. For depth expansion block see DEPTH EXPANSION Section and Figure 12.
2. For Flag operation see WIDTH EXPANSION Section and Figure 10.

Figure 16 : Bidirectional Fifo Application.



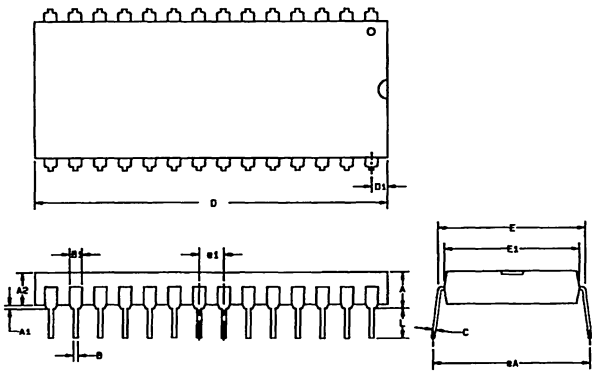
ORDER CODES

Part No	Access Time	R/W Cycle Time	Clock Freq.	Package Type	Temperature Range
MK4503N-65	65ns	80ns	12.5MHz	28 Pin Plastic DIP	0° to 70°C
MK4503N-80	80ns	100ns	10.0MHz	28 Pin Plastic DIP	0° to 70°C
MK4503N-10	100ns	120ns	8.3MHz	28 Pin Plastic DIP	0° to 70°C
MK4503N-12	120ns	140ns	7.1MHz	28 Pin Plastic DIP	0° to 70°C
MK4503N-15	150ns	175ns	5.7MHz	28 Pin Plastic DIP	0° to 70°C
MK4503N-20	200ns	235ns	4.2MHz	28 Pin Plastic DIP	0° to 70°C

Part No	Access Time	R/W Cycle Time
MK4503-65	65ns	80ns
MK4503-80	80ns	100ns
MK4503-10	100ns	120ns
MK4503-12	120ns	140ns
MK4503-15	150ns	175ns
MK4503-20	200ns	235ns

PACKAGE DESCRIPTION

MK4503 PLASTIC (N TYPE) DUAL–IN–LINE, 28 PINS



Dim.	mm		Inches		Notes
	Min.	Max.	Min.	Max.	
A		5.334		210	2
A1	0.381		.015		2
A2	3.556	4.064	.140	.160	
B	0.381	0.534	.015	.021	3
B1	1.27	1.778	.050	.070	
C	0.203	0.304	.008	.012	3
D	36.576	37.338	1.440	1.470	1
D1	1.651	2.159	.065	.085	
E	15.24	15.875	.600	.625	
E1	13.462	14.224	.530	.560	
e1	2.286	2.794	.090	.110	
eA	15.24	17.78	.600	.700	
L	3.048		.120		

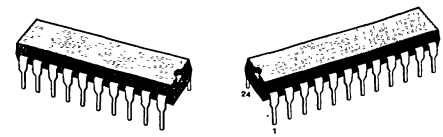
Notes : 1. Overall length includes 010 in flash on either end of the package.
2. Package standoff to be measured per jedec requirements.
3. The maximum limit shall be increased by 003 in when solder lead finish is specified.

VERY HIGH-SPEED CMOS CLOCKED FIFO

- 1024 x 5 ORGANIZATION
- VERY HIGH PERFORMANCE

Part No	Cycle Time	Cycle Frequency	Access Time
4505-25	25ns	40MHz	15ns
4505-33	33ns	30MHz	20ns
4505-50	50ns	20MHz	25ns

- RISING EDGE TRIGGERED CLOCK INPUTS
- SUPPORTS FREE-RUNNING 40% TO 60% DUTY CYCLE CLOCK INPUTS
- SEPARATE READ AND WRITE ENABLE INPUTS
- BiPORT™ RAM ARCHITECTURE ALLOWS FULLY ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE OPERATION
- CASCADABLE TO ANY DEPTH WITH NO ADDITIONAL LOGIC
- WIDTH EXPANDABLE TO MORE THAN 40 BITS WITH NO ADDITIONAL LOGIC
- HALF FULL STATUS FLAG
- FULL AND EMPTY FLAGS, ALMOST FULL, ALMOST EMPTY, INPUT READY, OUTPUT VALID STATUS FLAGS (4505M)
- FULLY TTL COMPATIBLE

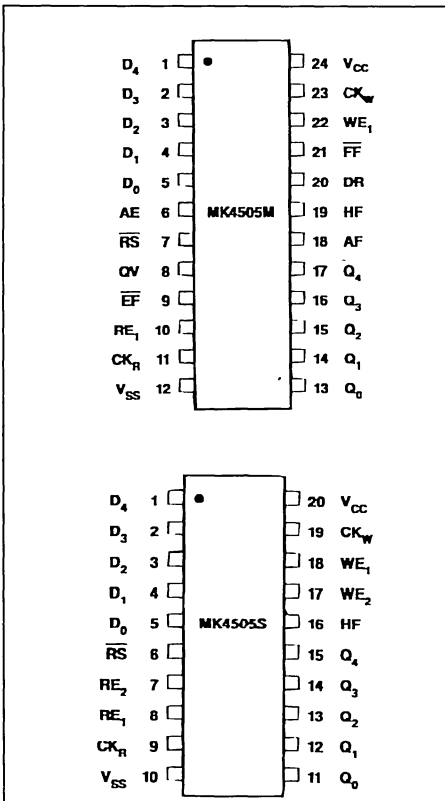


N
PDIP20
(300-Mil PDIP)

N
PDIP24
(300-Mil PDIP)

(Ordering Information at the end of the datasheet)

Figure 1 : Pin Configurations.



DESCRIPTION

The MK4505 is a Very High Speed 1K x 5 Clocked FIFO memory. It achieves its high performance through the use of a pipelined architecture, a 1.2µ full CMOS, single poly, double level metal process, and a memory array constructed using SGS-THOMSON'S 8 transistor BiPORT memory cell.

The device is designed for use in applications where data is moving through a system on a square wave clock ; applications such as digitized video and audio, image processing, A-to-D and D-to-A conversions, high speed data links, Radar return sampling or data tracing.

The device is available in two versions ; a Master, the MK4505M, and a Slave, the MK4505S. The Master provides all of the control signals necessary for reliable, full speed, fully asynchronous width expansion and/or depth expansion. The Master also provides a full compliment of status flags, including Output Valid, Empty, Almost Empty, Half Full, Al-

most Full, Full, and Input Ready. The Master cannot be written while Full or read while Empty. The Slave, in contrast, can be forced to write and/or read continuously regardless of device status ; a feature useful in triggered data acquisitions, or for retransmit (repeat reading) applications.

PIN NAMES

D_0 - D_4	– Data Input
Q_0 - Q_4	– Data Output
CK_W, CK_R	– Write and Read Clock
WE_1	– Write Enable Input 1
RE_1	– Read Enable Input 1
$\overline{RS}$	– Reset (active low)
HF	– Half Full Flag
V_{CC}, V_{SS}	– + 5 Volt, Ground

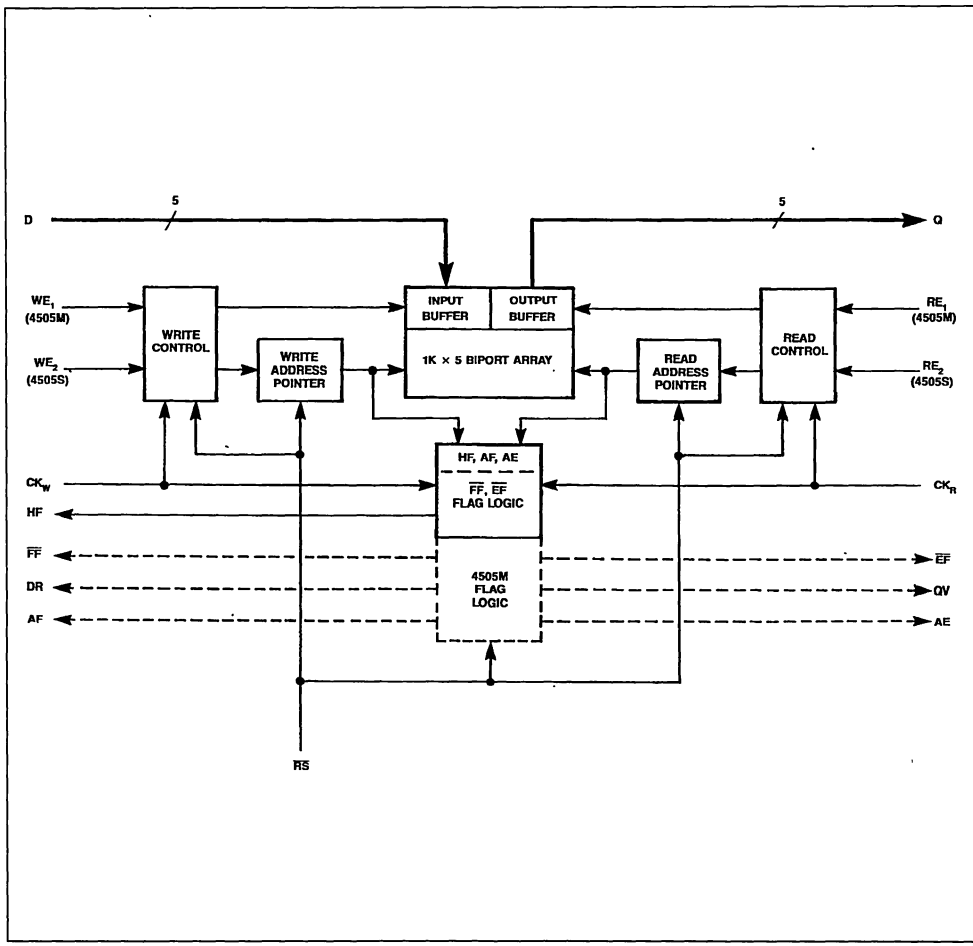
4505M only

$\overline{FF}$, $\overline{EF}$	– Full and Empty Flag (active low)
AF, AE	– Almost Full, Almost Empty Flag
DR, QV	– Input Ready, Output Valid

4505S only

WE_2	– Write Enable Input 2
RE_2	– Read Enable Input 2 (rising edge triggered 3 state control)

Figure 2 : Block Diagram.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to GND	– 1.0 to 7.0	V
T_A	Ambient Operating Temperature	0 to + 70	°C
T_{stg}	Ambient Storage Temperature (plastic)	– 55 to + 125	°C
P_D	Total Device Power Dissipation	1	Watt
I_P	Output Current per Pin	. 25	mA

Note : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Value			Unit	Note
		Min.	Typ.	Max.		
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic 1 Input	2.2		V_{CC} + 1.0	V	1
V_{IL}	Logic 0 Input	– 0.3		0.8	V	1

Note : 1. All voltages referenced to GND.

DC ELECTRICAL CHARACTERISTICS
(T_A = 0°C to 70°C, V_{CC} = 5.0 ± 10%)

Symbol	Parameter	4505-25			4505-33			4505-50			Unit	Note
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{CC}	Average Power Supply Current		115	140		95	140		75	140	mA	1

Symbol	Parameter	Min.	Max.	Unit	Note
I_{IL}	Input Leakage Current	– 1	+ 1	µA	2
I_{OL}	Output Leakage Current	– 10	+ 10	µA	2, 3
V_{OH}	Logic 1 Output Voltage (I_{OUT} = – 4 mA)	2.4		V	4
V_{OL}	Logic 0 Output Voltage (I_{OUT} = 8 mA)		0.4	V	4

Notes : 1. Measured with both ports operating at t_{CK} Min, 50% duty cycle, outputs open, V_{CC} max. Typical values reflect t_{CK} Min, outputs open, with V_{CC} = 5.0, 25°C, with 50% duty cycle.
2. Measured with V = 0.0V to V_{CC}.
3. Measured at $Q_0 - Q_4$, with QV = Low (4505M) ; after clocking with RE_2 = Low (4505S).
4. All voltages referenced to GND.

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

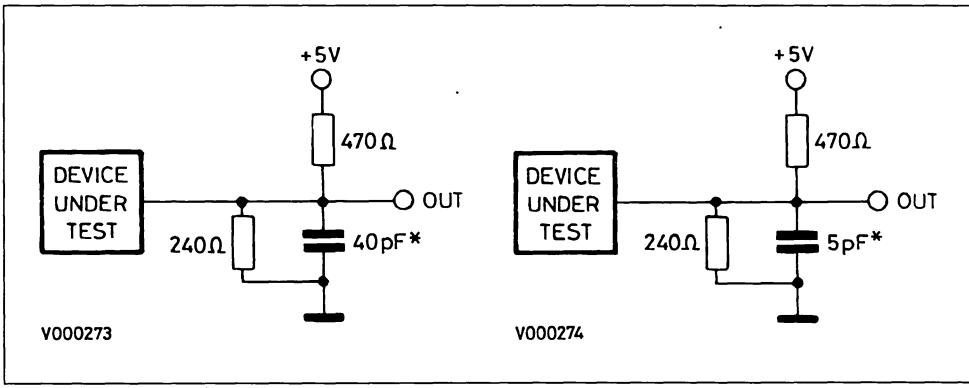
Symbol	Parameter	Value			Unit	Note
		Min.	Typ.	Max.		
C_I	Input Capacitance	4		5	pF	1
CO_1	Output Capacitance	8		10	pF	1, 2
CO_2	Output Capacitance	12		15	pF	1, 3

Notes : 1. Sampled, not 100% tested. Measured at 1MHz.
2. Measured at all data and flag outputs except $\overline{EF}$ and $\overline{FF}$.
3. Measured at $\overline{EF}$ and $\overline{FF}$.

AC TEST CONDITIONS

Parameter	Value	Unit
Input Levels	0 to 3	V
Transition Times	5	ns
Input and Output Timing Reference Levels	1.5	V
Ambient Temperature	0 to 70	°C
V_{CC}	5.0 ± 10%	V

Figure 3 : Output Load Circuit.



Note : Includes scope and test Fig.

READ AND HOLD OPERATIONS

The device will perform a Read on the next rising edge of the Read Clock (CK_R) whenever (see figure 4) :

- (4505S) RE_1 and RE_2 are high at the rising edge of the clock.
- (4505M) RE_1 and $\overline{EF}$ are high at the rising edge of the clock.

Because the device only re-evaluates and updates the Empty Flag ($\overline{EF}$) on the rising edge of CK_R, the appearance of an active Empty Flag at valid flag access time, t_{F1A}, assures the user that the next rising edge of CK_R will generate an inhibit condition. All Q outputs will be High Z at t_{QZ} from the rising edge of CK_R. $\overline{EF}$ is latched between subsequent read clocks.

The device will perform a Hold Cycle (hold over previous data) if RE_1 is low at the rising edge of the clock (CK_R). If $\overline{EF}$ (4505M) or RE_2 (4505S) is low at the rising edge of the clock, then the outputs will go to High-Z.

WRITE OPERATIONS

The device will perform a Write on the next rising edge of the Write Clock (CK_W) whenever (see figure 5) :

- (4505S) WE_1 and WE_2 are high at the rising edge of the clock.
- (4505M) WE_1 and $\overline{FF}$ are high at the rising edge of the clock.

Because the device only re-evaluates and updates the Full Flag ($\overline{FF}$) on the rising edge of CK_W, the appearance of an active Full Flag at valid flag access time, t_{F1A}, assures the user that the next rising edge of CK_W will generate a No-Op condition. $\overline{FF}$ is latched between subsequent write clocks.

MK4505M (Master) WRITE TRUTH TABLE

CK_W	Present State			Operation	Next State	
	$\overline{RS}$	WE_1	$\overline{FF}$		$\overline{FF}$	Data In
X	0	X	X	Reset	1	Don't Care
↑	1	0	0	No-Op	?	Don't Care
↑	1	0	1	No-Op	1	Don't Care
↑	1	1	0	No-Op	?	Don't Care
↑	1	1	1	Write	?	Data In

? = Device Status is referenced to the "next state" logic conditions.
The "next state" flag logic level is unknown due to the possible occurence of a read operation.

MK4505M (Master) READ TRUTH TABLE

CK_R	Present State			Operation	Next State	
	$\overline{RS}$	RE_1	$\overline{EF}$		$\overline{EF}$	Q_{OUT}
X	0	X	X	Reset	0	Hi Z
↑	1	0	0	Inhibit	?	Hi Z
↑	1	0	1	Hold	1	Previous Q
↑	1	1	0	Inhibit	?	Hi Z
↑	1	1	1	Read	?	Data Out

? = Device Status is referenced to the "next state" flag logic and Q_{OUT} conditions.
The "next state" flag logic level is unknown due to the possible occurrence of a write operation.

MK4505S (Slave) WRITE TRUTH TABLE

CK_W	Present State			Operation	Next State
	$\overline{RS}$	WE_1	WE_2		Data
X	0	X	X	Reset	Don't Care
↑	1	0	0	No-Op	Don't Care
↑	1	0	1	No-Op	Don't Care
↑	1	1	0	No-Op	Don't Care
↑	1	1	1	Write	Data In

MK4505S (Slave) READ TRUTH TABLE

CK_W	Present State			Operation	Next State
	$\overline{RS}$	RE_1	RE_2		Q_{OUT}
X	0	X	X	Reset	Hi Z
↑	1	0	0	Inhibit	Hi Z
↑	1	0	1	Hold	Previous Q
↑	1	1	0	Inhibit	Hi Z
↑	1	1	1	Read	Data Out

RESET

$\overline{RS}$ is an asynchronous master reset input. A Reset is required after power-up, before first write. Reset commences on the falling edge of $\overline{RS}$ irrespective of the state of any other input or output. The user is required to observe Reset Set Up Time (t_{RSS}) only if the device is enabled (see figure 7). The t_{RSS} specification is a don't care if the device remains disabled ($WE_1 = RE_1 = LOW$). All status flag outputs will be valid t_{RSA} from the falling edge of $\overline{RS}$, and all Q data outputs will be high impedance t_{RSQZ} from the same falling edge.

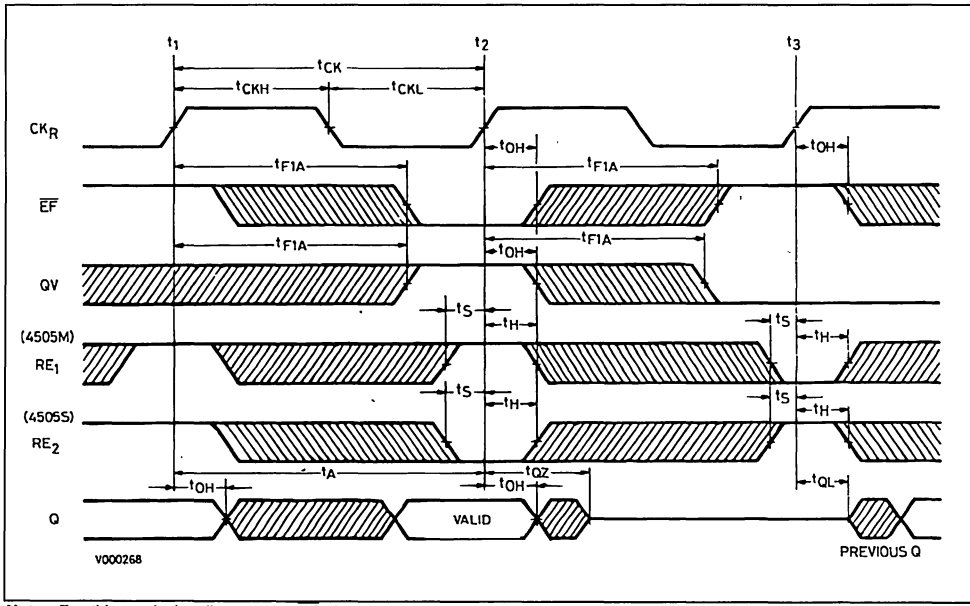
After Reset, if no valid Read operations have been performed since Reset, the "previous data" that will be output when executing the first Hold cycle will be all zeros (see figure 8).

AC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	4505-25		4505-33		4505-50		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CK}	Clock Cycle Time	25		33		50		ns	1
t_{CKH}	Clock High Time	10		13		20		ns	1
t_{CKL}	Clock Low Time	10		13		20		ns	1
t_S	Set Up Time	10		13		16		ns	1
t_H	Hold Time	0		0		0		ns	
t_A	Output (Q) Access Time		15		20		25	ns	1, 2
t_{F1A}	Flag 1 Access Time(7)		15		20		25	ns	1, 2
t_{F2A}	Flag 2 Access Time(8)		20		25		30	ns	1, 2
t_{OH}	Output Hold Time	5		5		5		ns	1, 2
t_{OZ}	Clock to Outputs High-Z		15		20		25	ns	1, 3
t_{OL}	Clock to Outputs Low-Z	5		5		5		ns	1, 3
t_{RSS}	Reset Set Up Time	12		16		25		ns	1, 4
t_{RS}	Reset Pulse Width	25		33		50		ns	
t_{RSA}	Reset Flag Acces Time		50		66		100	ns	1, 3
t_{RSQZ}	Reset to Outputs High-Z		25		33		50	ns	1, 3
t_{FRL}	First Read Latency	50		66		100		ns	1, 5
t_{FFL}	First Flag Cycle Latency	25		33		50		ns	1, 6

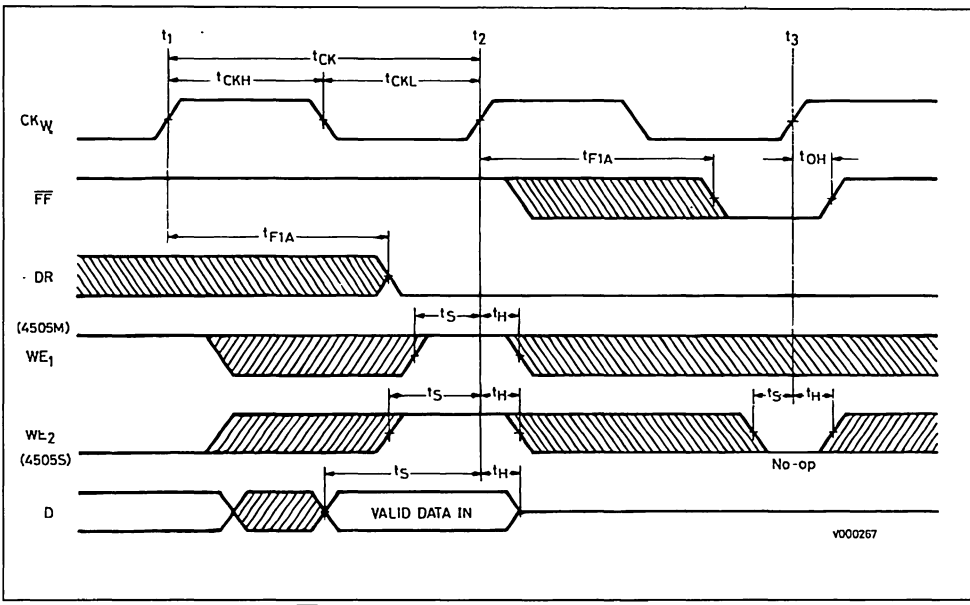
Notes : 1. All AC Electrical Characteristics measured under conditions specified in "AC Test Conditions".
2. Measured w/40pf Output Load (figure 3A).
3. Measured w/5pf Output Load (figure 3B).
4. Need not be met unless device is Read and/or Write Enabled.
5. Minimum first Write to first Read delay required to assure valid first Read.
6. Minimum first Write to first Read Clock delay required to assure clearing the Empty Flag.
7. Flag 1 = $\overline{EF}$, $\overline{FF}$, QV, DR.
8. Flag 2 = AE, AF, HF.

Figure 4 : Read Cycle Timing.



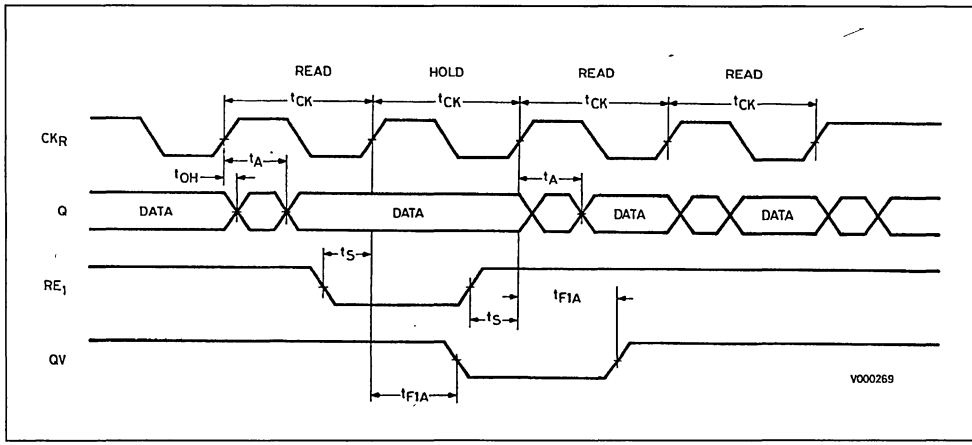
Note : For this particular diagram the $\overline{EF}$ changes logic states presuming that a valid WRITE operation has occured prior to the rising edge of CK_R at t_2.

Figure 5 : Write Cycle Timing.



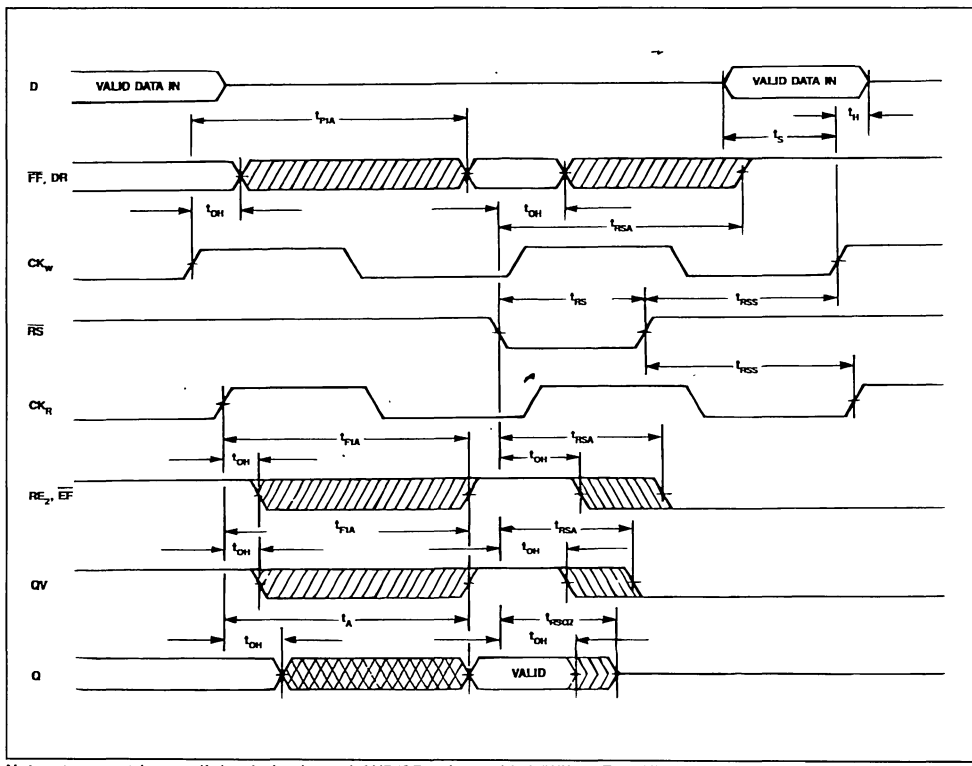
Note : For this particular diagram the $\overline{FF}$ changes logic states presuming that a valid READ operation has occured prior to the rising edge of CK_W at t_3.

Figure 6 : Hold Cycle Timing.



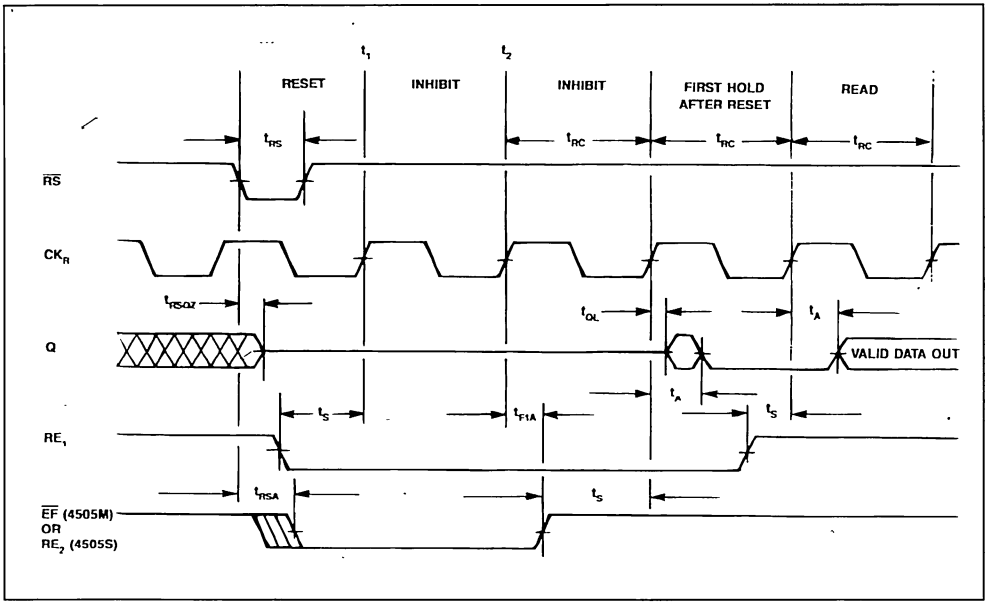
Note : $\overline{EF}$ = HIGH (master)
RE_2 = HIGH (slave)

Figure 7 : Reset Cycle Timing.



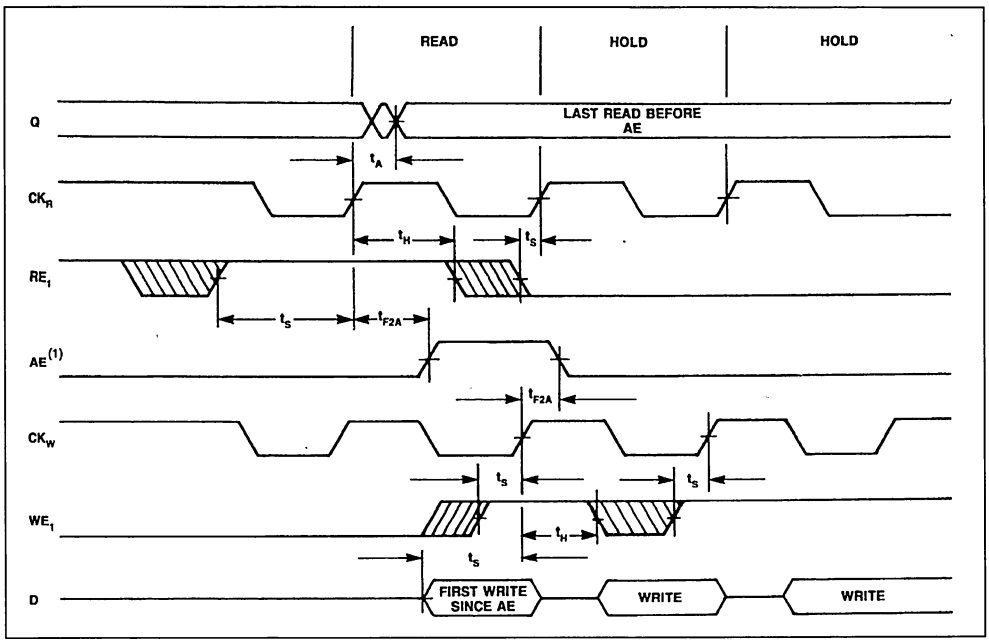
Note : t_{RSS} must be met if the device is read AND/OR write enabled (WE_1, RE_1 = High).

Figure 8 : First Hold After Reset.



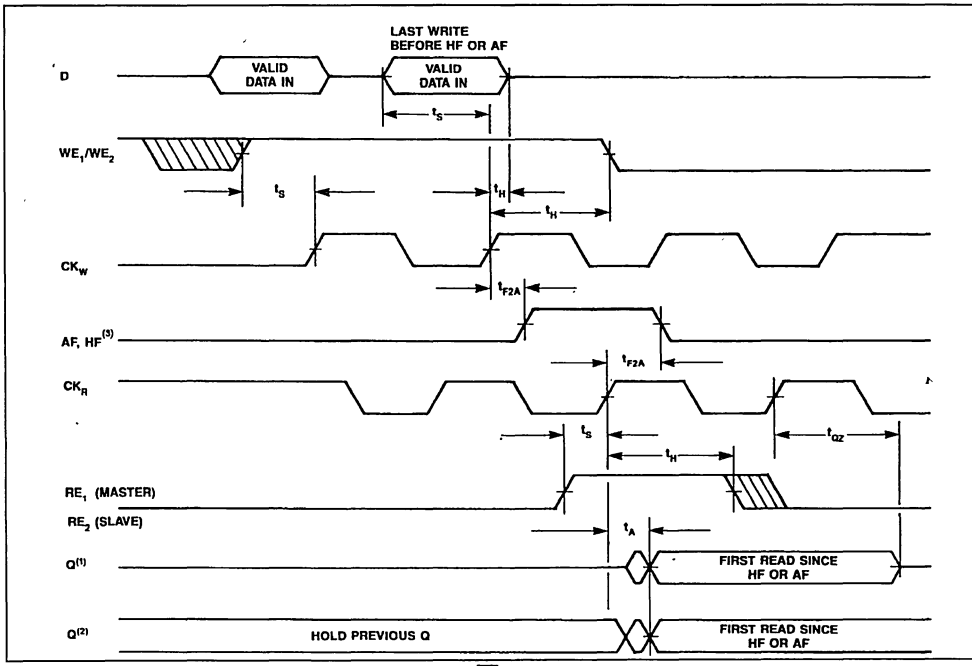
Note : A valid write operation is presumed between t_1 and t_2.

Figure 9 : Almost Empty Flag Timing (4505M only).



Note : 1. This example does not show the hysterisis in the ALMOST FLAGS.

Figure 10 : Almost Full, Half Full Flag Timing.



Notes : 1. Q outputs in Master/Slave Width Expansion ($RE_2 = \overline{EF}$), or when using MK4505S Slave separately.
2. Q outputs in Master-to-Master Depth Expansion (RE_1 with $\overline{EF}$ = HIGH), or when using the MK4505M separately.
3. This example does not show the hysterisis in the ALMOST FLAGS.

FLAG INTERPRETATION KEY

Gating Clock		Gating Operation	Flag Affected	Flag Transition	Read Locations Remaining to Empty	Write Locations Available to Full
CK_R	CK_W					
↑	–	Read	AE		8*	1016
–	↑	Write	AE		10	1014
↑	–	Read	AE		9	1015
–	↑	Write	AE		11	1013
↑	–	Read	AF		1014	10
–	↑	Write	AF		1016	8*
↑	–	Read	AF		1013	11
–	↑	Write	AF		1015	9
↑	–	Read	HF		510	514
–	↑	Write	HF		512	512*
↑	–	Read	HF		509	515
–	↑	Write	HF		511	513

Notes : *. Flag definition to the respective operation and clock.
1. All examples are given in reference to the flag transition point, in the direction shown, for the given clock edge and operation. The flag remains stable as long as the condition that set or cleared the flag exists in the device.
2. The table describes the number of the cycles that can be performed, including the next rising edge.
3. Remaining Read or Available Write locations at the flag transition point reflects the hysterisis inherent to the internal scheme that detects the flag status.
4. Asynchronous or simultaneous dual port operations at the flag transition point may result in a false flag status. When this occurs, the flag is evaluated and updated on the subsequent clock.

Figure 11 : Simultaneous Write/Read Timing (4505M only).

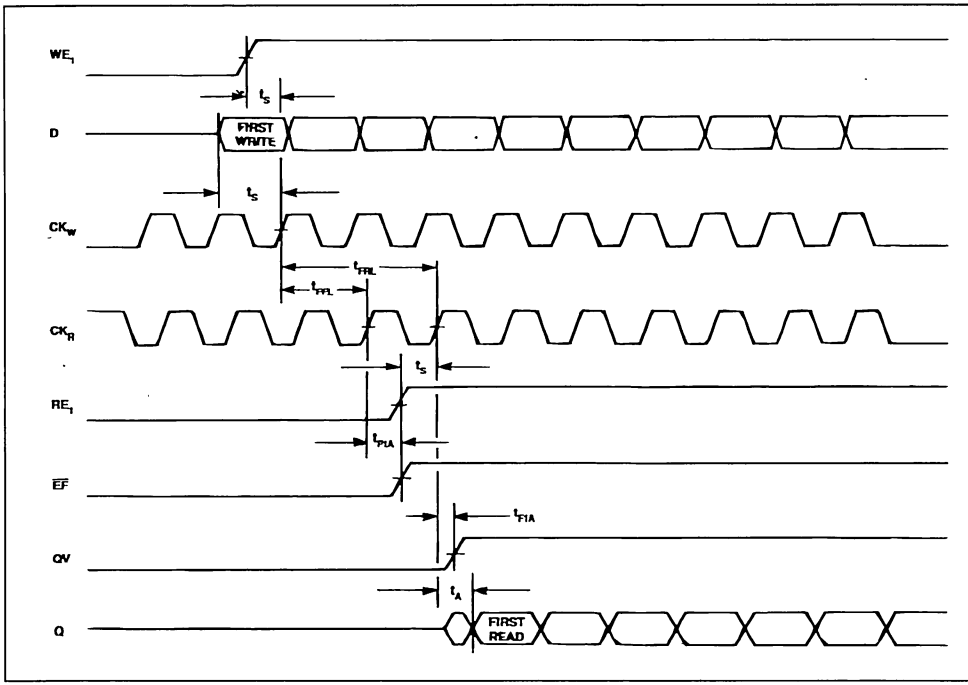
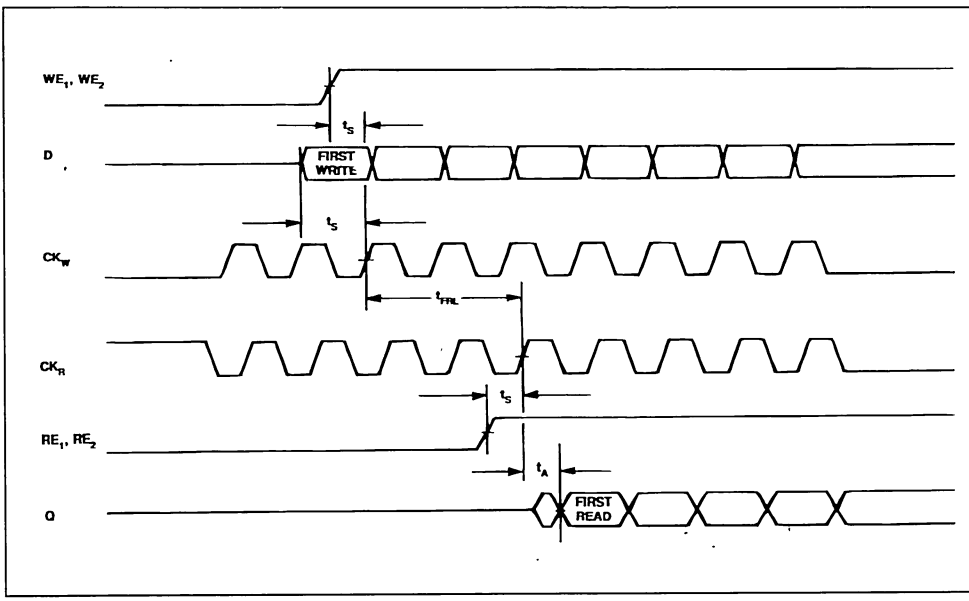


Figure 12 : Simultaneous Write/Read Timing (4505S only).



SIMULTANEOUS WRITE/READ TIMING

The Empty Flag ($\overline{EF}$) is guaranteed to clear (go HIGH) in response to the first rising edge of the read clock (CK_R) to occur t_{FFL} (First Flag Latency) after a valid First Write (from the rising edge of CK_W). Read clocks occurring less than t_{FFL} after a First Write may clear the $\overline{EF}$, but are not guaranteed (see figure 10). As always, reads attempted in conjunction with an active Empty Flag are inhibited. Therefore, the next rising edge of CK_R following t_{FFL} will produce the first valid read. This is the t_{FRL} (First Read Latency) parameter, and must be observed for proper system operation with the latched $\overline{EF}$. Coming from an empty condition, the First Read operation should be accomplished by enabling RE_1 no less than t_S before the rising edge of CK_R at t_{FRL}. The Q outputs will present valid data t_A from the rising edge of CK_R.

When using the MK4505S (Slave) separately, the user must observe the t_{FRL} (First Read Latency) parameter to ensure first-write-to-first-read valid data. Referring to figure 12, the first rising edge of CK_R to occur t_{FRL} after a First Write clock will guarantee valid data t_A from the rising edge of CK_R. Read operations attempted before t_{FRL} is satisfied may result in reading RAM locations not yet written. Careful observance of t_{FRL} by the user is a must when using free running asynchronous read/write clocks on the MK4505S ; there is no automatic read and write protection circuitry in the Slave.

It should also be noted that the MK4505M/S has an expected "fall-through delay time" described as First Write data presented to the FIFO and clocked out to the outside world. This can be calculated as : $t_S + t_{FRL} + t_A$ (from figure 11 or 12). Further occurring valid read clocks will present data to the Q outputs t_A from the rising edge of CK_R.

WIDTH AND DEPTH EXPANSION

A single Master (MK4505M) is required for each 1K of depth configured. The number of Slaves that can be driven by a single Master is limited only by the effects of adding extra load capacitance (Write and Read Enable Input Capacitance) onto the Input Ready (DR), Output Valid (QV), Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$) outputs. However, even 40 bits of width (8 devices) results in only 40pf of loading, which corresponds to the amount of load called out in the AC Test Conditions. Additional loading will slow the flags down, but as long as Enable Set Up time (t_S) is met, slowing the flags has no negative consequences.

DEPTH EXPANSION HANDSHAKE PROTOCOL

The depth expansion handshake device connections are shown in figure 13. The expansion interface signals can be considered transparent to the user, as long as the expansion clock continues to run. The Output Ready (QV) flag, and the Data Ready (DR) flag logic descriptions are detailed in the following charts. Since the expansion clock is the read clock for the sending FIFO, as well as the write clock for the receiving FIFO, these two signals prevent data loss during depth expansion applications where the receiving bank (bank B, figure 13) goes full simultaneously as the sending bank goes empty (bank A, figure 13).

QV Definition Table.

Before Read Clock				Operation at CK_R	After Read Clock		Note
RE_1	$\overline{EF}$	QV	Reads Remaining		QV	Status	
X	0	X	0	Inhibit	0	Empty	1
0	1	1	≥ 1	Hold	0	Active	2
1	1	0	1	Read	1	Empty	3
1	1	X	≥ 2	Read	1	Active	4

Notes : 1. Whenever EF is active low, further attempted read cycles are inhibited.
2. QV is gated by RE_1 such that the QV flag will be latched low t_{f1A} from the rising edge of CK_R when RE_1 is low. The RE1 input must meet the set-up time (t_S) prior to the read clock edge. QV does not logically allow or prevent a read operation.
3. Whenever RE_1 is active high, QV will always follows the $\overline{EF}$ signal by one read clock cycle.
4. This condition displays a typical read operation when remaining memory locations (prior to the read operation) are from 2 to 1024. $\overline{EF}$ and QV continue to acknowledge that the FIFO has more data available.

DR Definition Table.

Before Write Clock				Operation at CK_W	After Write Clock		Note
WE_1	$\overline{FF}$	DR	Write Available		DR	Status	
X	0	0	0	No-Op	0	Full	1
0	1	0	1	No-Op	1	Full-1	2
0	1	1	1	No-Op	0	Full-1	2
1	1	X	1	Write	0	Full	1
0	1	X	2	No-Op	1	Active	3
1	1	1	2	Write	0	Full-1	4
0	1	1	≥ 3	No-Op	1	Active	
1	1	1	≥ 3	Write	1	Active	5

Notes : 1. DR can be low only when the MK4505M is full or (full-1). Whenever the device goes full ($\overline{FF}$ = low), then DR will be latched low t_{F1A} from the same write clock edge (CK_W) regardless of the logic state of the DR flag at the clock transition. Further attempted write operations are blocked since FF is low.

2. If DR changes logic states after the write clock, then this example reflects the condition when the MK4505M has one (1) memory location available (full-1). DR will presume the opposite logic state of the previous cycle for subsequent write clocks if WE_1 is disabled (low) and one memory location is available. Whenever the MK4505M goes full ($\overline{FF}$ = low), DR will be latched low in the same clock cycle. (This is part of the Depth Expansion Protocol, and acts to notify the sending unit that space is available.) The DR flag does not logically allow or prevent a write operation.
3. If DR is a logic 1 before and after the write clock, then this example signifies that the available memory locations in the MK4505M are greater than or equal to 2, after the completed write operation.
4. During a valid write cycle, the DR flag will go inactive low t_{F1A} from the rising edge of CK_W if the write counter is (full-2) at the clock transition. This results is a (full-1) condition. (Refer to notes 1 and 2.)
5. This condition displays a typical write cycle, where available memory locations (prior to the write operation) are from 3 to 1024. DR and $\overline{FF}$ continue to acknowledge that the FIFO is ready to accept more data.

In summary, the QV flag follows the $\overline{EF}$ signal by one read clock cycle (in all instances) when RE_1 is active high at the rising edge of CK_R. Whenever RE_1 is disabled (low), the QV flag will go low t_{F1A} from the rising edge of CK_R. Of course, the RE_1 input must satisfy the set-up time (t_S) prior to CK_R. The QV flag does not enable or inhibit read operations. Read protection is provided by the EF signal.

The DR flag will go low one cycle prior to a full condition (full-1), or DR will go high at (full-2) from the rising edge of CK_W. However, if WE_1 is disabled (low), and the device has one location available, then DR will toggle each subsequent write cycle until full. This way the device notifies the sending unit that at least one more byte of data can be accepted. When the device goes full, the DR flag will be latched low t_{F1A} from the clock edge (during the same write cycle), regardless of its previous logic state. As with all valid write cycles, the WE_1 input must satisfy the set-up time (t_S) prior to CK_W. The DR flag does not enable or inhibit write operations. Write protection is provided by the $\overline{FF}$ signal.

WIDTH AND DEPTH EXPANSION EXAMPLES

The width and depth expansion interface timing diagrams (figures 14 and 15) are in reference to the width and depth expansion schematic in figure 13 (For simplicity all clocks have the same frequency and transition rate).

Example 1 - First Write Since Empty - Reading the timing diagram from the top left to bottom right, one can determine that figure 13 illustrates the effects of the first WRITE/READ cycles from an EMPTY array of FIFOs. Both of the $\overline{EF}$ pins are initially low ($\overline{EF}_X$, $\overline{EF}$ and RE_2). As data is written into Bank A, the expansion clock reads data from Bank A and writes it to Bank B, the interface $\overline{EF}$ ($\overline{EF}$ and RE_2) and the external $\overline{EF}$ ($\overline{EF}_X$) go inactive (logic 1) while data is shifted through the FIFO array from Bank A through Bank B to the external output (Q_X). The $\overline{EF}$ logic goes valid (logic 0) once data is shifted out of its respective bank.

Example 2 - First Read Since Full - Reading the timing diagram from the bottom left to top right, one can determine that figure 15 illustrates the effects of the first READs from a FULL array of FIFOs. As data is read out of the system (Q_X), it allows Bank B to receive data (Q_{EXP}) shifted from Bank A. As Bank B shifts data out via Q_X, allowing Bank A to shift data into Bank B, both banks will show a cleared $\overline{FF}$ status (logic 1) on the expansion $\overline{FF}$ ($\overline{FF}$ and WE_2) as well as the internal $\overline{FF}$ ($\overline{FF}_X$). When Bank A is no longer considered FULL, Data In from the system (D_X) is now written into Bank A. The FIFO array is again completely Full.

APPLICATION

The MK4505 operates from a 5V supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the MK4505 can also interface to 5V CMOS on all inputs and outputs.

Since very high frequency current transients will be associated with the operation of the MK4505, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. A high frequency decoupling capacitor should be placed next to each FIFO. The capacitor should be 0.1µF or larger. Also, a pull-up resistor in the range of 1KΩ is recommended for the $\overline{\text{RESET}}$ input pin to improve proper operation.

Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10Ω to 33Ω often prove most suitable.

Figure 13 : MK4505M/S 2K x 10 Width and Depth Expansion Schematic.

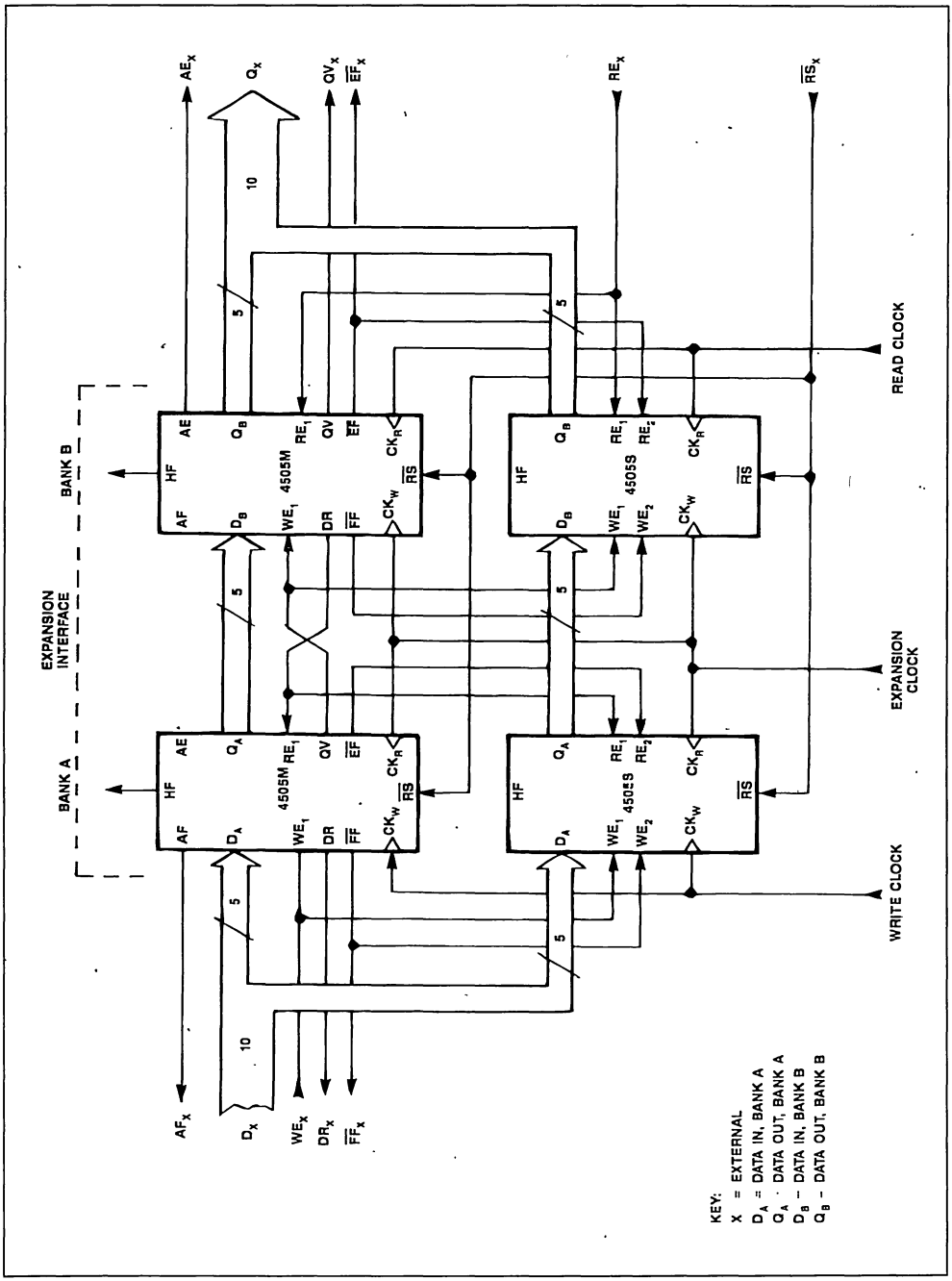
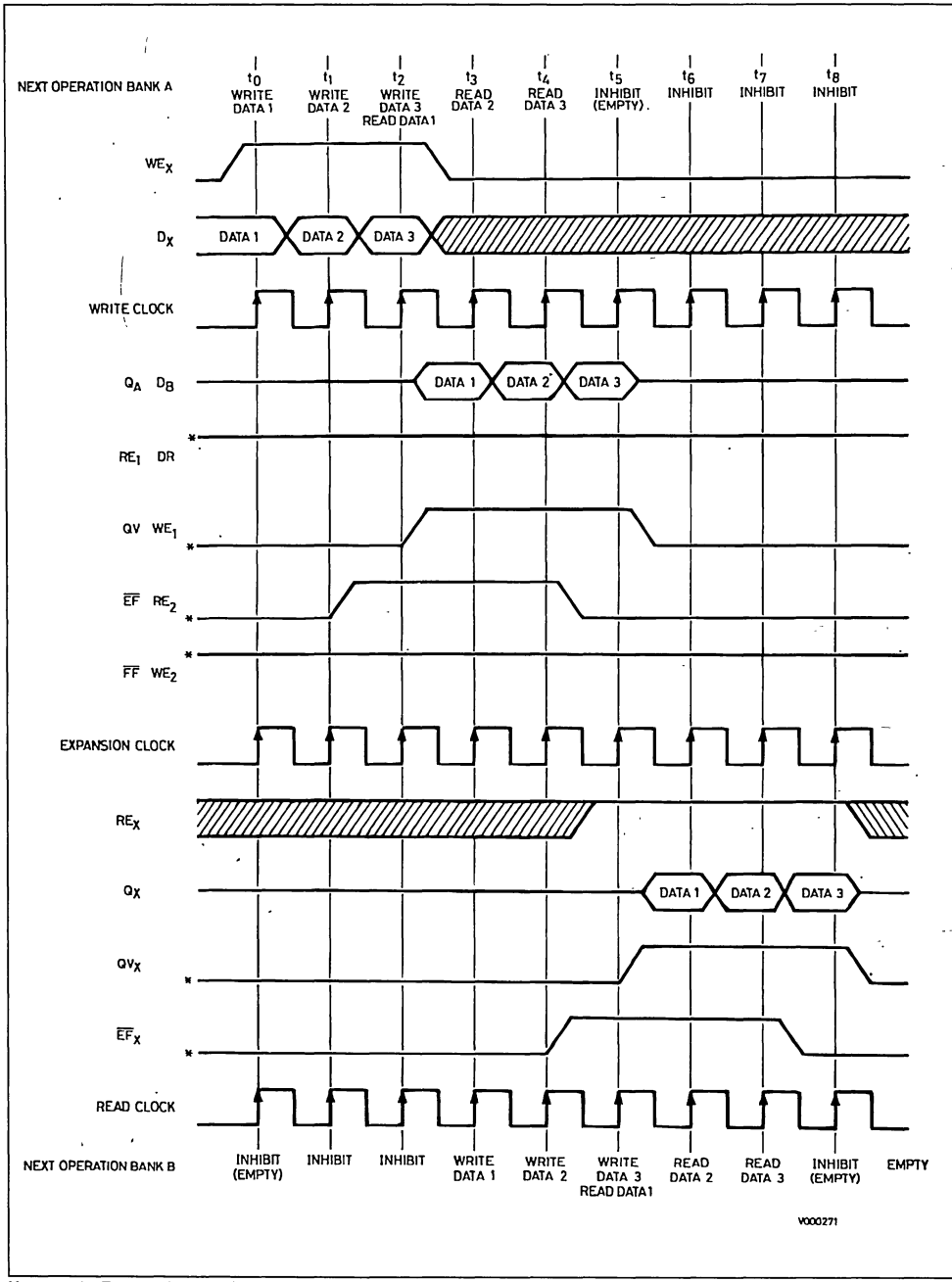
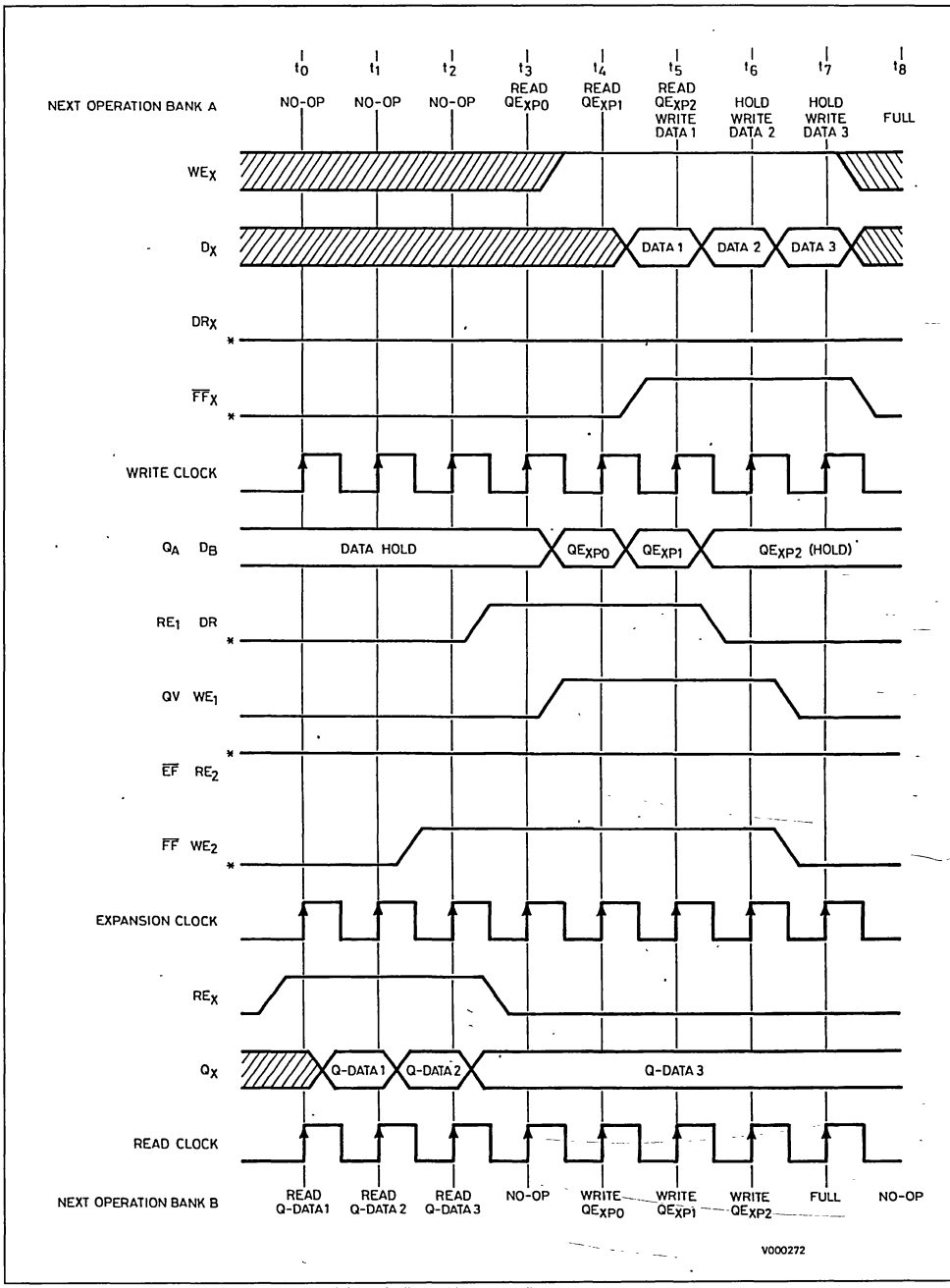


Figure 14 : Example 1 - Width and Depth Expansion Interface Timing.



Note : *. Example begins with both banks empty, as status flags indicate.

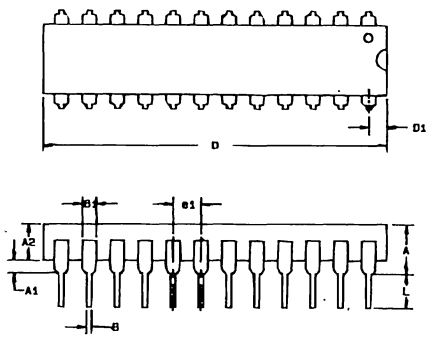
Figure 15 : Example 2 - Width and Depth Expansion Interface Timing.



Note : *. Example begins with both banks full, as indicated by status flags.

PACKAGES MECHANICAL DATA

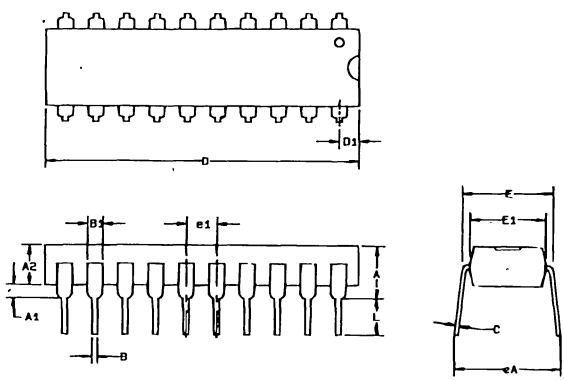
Figure 16 : MK4505M 24-Pin Plastic DIP (N), 300-Mil.



Dim.	mm		Inches		Notes
	Min.	Max.	Min.	Max.	
A	–	5.334	–	210	2
A1	0.381	–	.015	–	2
A2	3.048	3.556	.120	.140	
B	0.381	0.533	.015	.021	3
B1	1.143	1.778	.045	.070	
C	0.203	0.304	.008	.012	3
D	–	32.258	–	1.270	1
D1	1.524	2.286	.060	.075	
E	7.62	8.255	.300	.325	
E1	6.906	6.858	.240	.270	
e1	2.286	2.794	.090	.110	
eA	7.62	9.271	.300	.365	
L	3.175	–	.125	–	

Notes : 1. Overall Length includes .010 IN.Flash on either end of the package.
2. Package standoff to be measured per Jedec requirements.
3. The maximum limit shall be increased by .003 IN. when solder lead finish is specified.

Figure 17 : MK4505S 20-Pin Plastic DIP (N), 300-Mil.



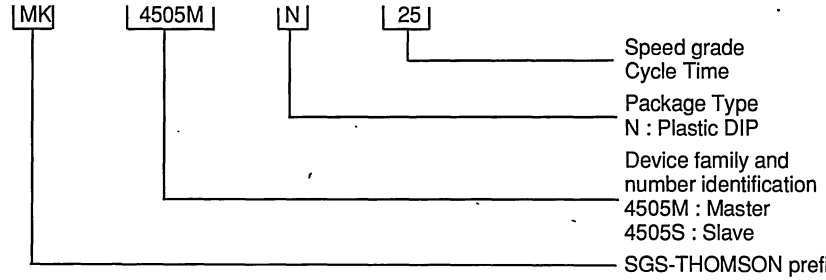
Dim.	mm		Inches		Notes
	Min.	Max.	Min.	Max.	
A	–	5.334	–	210	2
A1	0.381	–	015	–	2
A2	3.048	3.556	.120	.140	
B	0.381	0.533	.015	.021	3
B1	1.143	1.778	.045	.070	
C	0.203	0.304	.008	.012	3
D	25.908	26.67	1.020	1.050	1
D1	1.524	1.905	.060	.075	
E	7.62	8.255	.300	.325	
E1	6.906	6.858	.240	.270	
e1	2.286	2.794	.090	.110	
eA	7.62	9.271	.300	.365	
L	3.175	–	.125	–	

Notes : 1. Overall Length includes .010 IN. Flash on either end of the package.
2. Package standoff to be measured per Jedec requirements.
3. The maximum limit shall be increased by .003 IN. when solder lead finish is specified.

ORDERING INFORMATION

Part Number	Access Time	Cycle Time	Cycle Frequency	Temperature Range	Package Type
MK4505MN-25	15ns	25ns	40MHz	0°C to 70°C	PDIP24 300-MIL
MK4505MN-33	20ns	33ns	30MHz	0°C to 70°C	PDIP24 300-MIL
MK4505MN-50	25ns	50ns	20MHz	0°C to 70°C	PDIP24 300-MIL
MK4505SN-25	15ns	25ns	40MHz	0°C to 70°C	PDIP20 300-MIL
MK4505SN-33	20ns	33ns	30MHz	0°C to 70°C	PDIP20 300-MIL
MK4505SN-50	25ns	50ns	20MHz	0°C to 70°C	PDIP20 300-MIL

Note : PDIP = Plastic DIP.



SGS-THOMSON MICROELECTRONICS

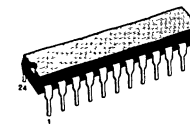
MK45264/45265(N) -55/70

(64 x 5) x 2 CMOS BIDERECTIONAL BiPORT FIFO/TRANSCEIVER

- DUAL 64 x 5 FIFOs PLUS A '245-TYPE TRANSCEIVER FUNCTION
- FULLY ASYNCHRONOUS DUAL PORT OPERATION
- EMPTY, FULL, ALMOST FULL AND ALMOST EMPTY STATUS FLAGS
- SPARE BITS FOR PARITY AND BEGINNING/END-OF-MESSAGE FLAGS
- ± 12mA OUTPUT DRIVE CAPABILITY
- DUAL V_{CC} AND V_{SS} FOR IMPROVED MARGIN AND DRIVE
- 300 MIL DIP PACKAGE
- APPLICATION : ARBITRATION-FREE µP-TO-µP MESSAGE PASSING

PIN NAMES

V_{CC}, V_{SS}	+ 5V, GND
DQ_{X0}-DQ_{X4}	X Port Data I/O
DQ_{Y0}-DQ_{Y4}	Y Port Data I/O
$\overline{W}_X$, $\overline{W}_Y$	X & Y Port Write Enables
$\overline{R}_X$/DIR	X Port Read Enable and Transceiver Direction Control
$\overline{G}$	Transceiver Enable
$\overline{R}_Y$	Y Port Read Enable
$\overline{RS}$	Master Reset
$\overline{EF}_X$, $\overline{FF}_Y$	Y-to-X FIFO Empty/full Flag
$\overline{EF}_Y$, $\overline{FF}_X$	X-to-Y FIFO Empty/full Flag
$\overline{AE}_Y$, $\overline{AF}_X$	X-to-Y FIFO Almost Empty/full
$\overline{AE}_X$, $\overline{AF}_Y$	Y-to-X FIFO Almost Empty/full



N
DIP-24
(Plastic Package)

Part No	Access Time	Cycle Time	Cycle Rate
MK45264N-55	55ns	75ns	13.3MHz
MK45265N-55	55ns	75ns	13.3MHz
MK45264N-70	70ns	95ns	10.5MHz
MK45265N-70	70ns	95ns	10.5MHz

Figure 1 : Pin Connections.

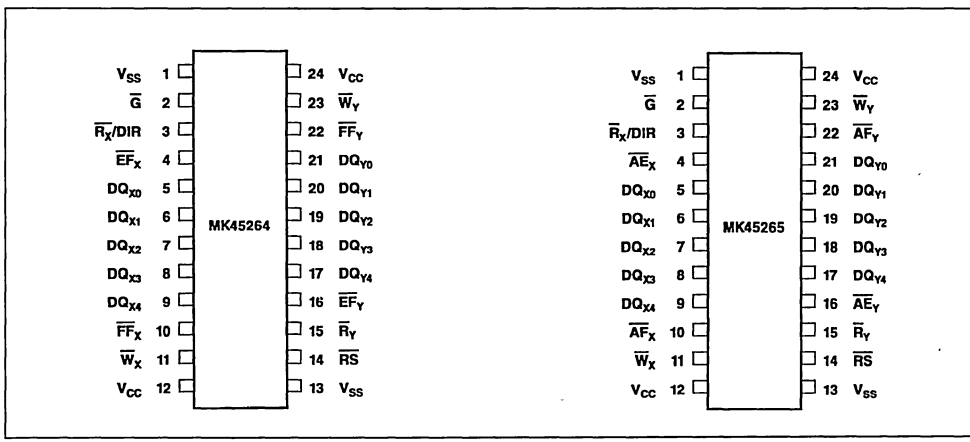
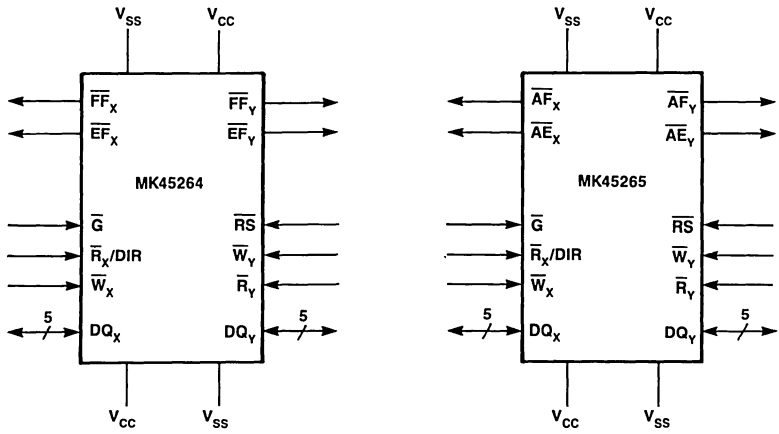


FIGURE 2. DEVICE LOGIC SYMBOL



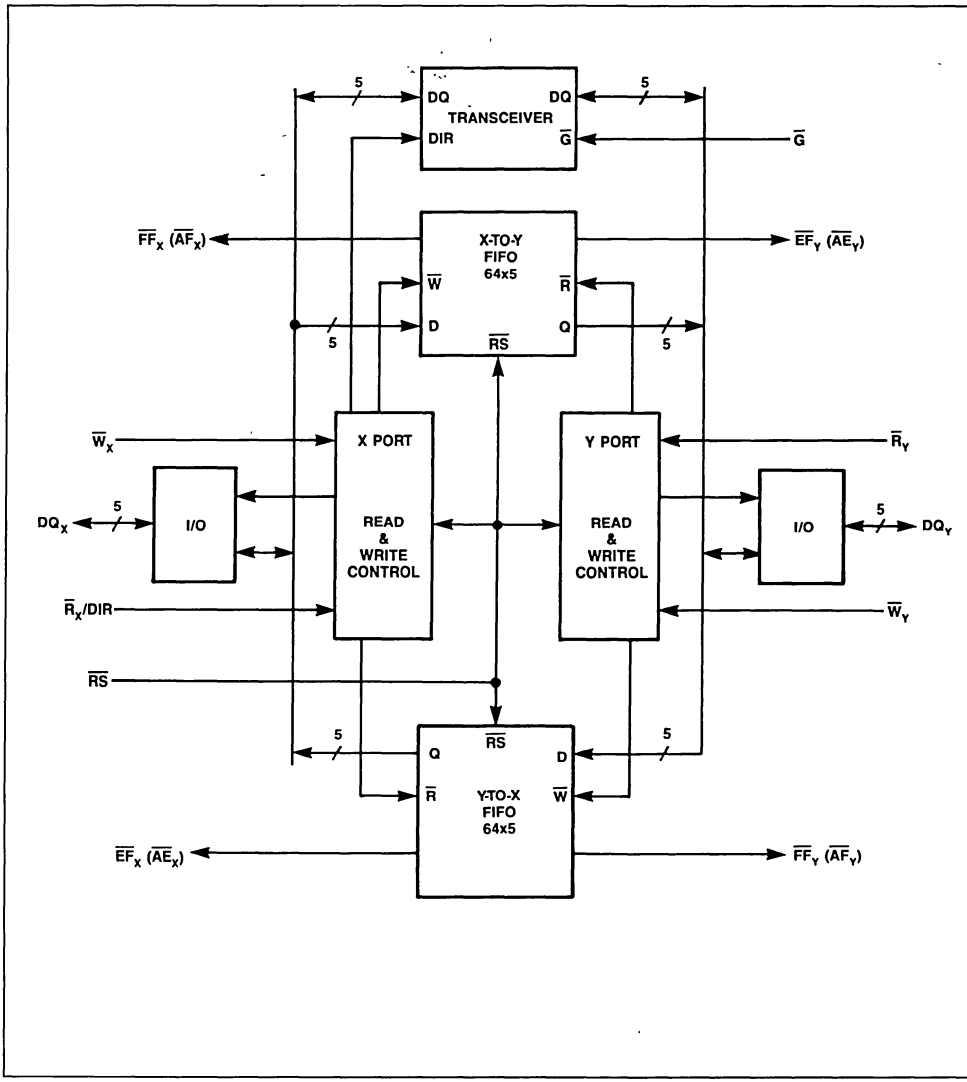
TRUTH TABLE

$\overline{RS}$	$\overline{G}$	$\overline{R_X}$/DIR	$\overline{W_X}$	$\overline{R_Y}$	$\overline{W_Y}$	MODE	DQ_X	DQ_Y
Lo	X	X	X	X	X	Master Reset	High Z	High Z
Hi	Lo	Hi	X	X	X	Transparent X-Y	Data In	DQ_X
Hi	Lo	Lo	X	X	X	Transparent Y-X	DQ_Y	Data In
Hi	Hi	Hi	Hi	Hi	Hi	Sby X / Sby Y	High Z	High Z
Hi	Hi	Hi	Hi	Lo	Hi	Sby X / Read Y	High Z	Data Out
Hi	Hi	Hi	Hi	X	Lo	Sby X / Write Y	High Z	Data In
Hi	Hi	Lo	Hi	Hi	Hi	Read X / Sby Y	Data Out	High Z
Hi	Hi	Lo	Hi	Lo	Hi	Read X / Read Y	Data Out	Data Out
Hi	Hi	Lo	Hi	X	Lo	Read X / Write Y	Data Out	Data In
Hi	Hi	X	Lo	Hi	Hi	Write X / Sby Y	Data In	High Z
Hi	Hi	X	Lo	Lo	Hi	Write X / Read Y	Data In	Data Out
Hi	Hi	X	Lo	X	Lo	Write X / Write Y	Data In	Data In

X = Don't Care

NOTE: Truth Table logic states presume all status flags to be inactive.

FIGURE 3. BLOCK DIAGRAM



DEVICE APPLICATION/FUNCTION

The MK45264/65 contains two independent single direction FIFOs, and a bidirectional transceiver, connected via two internal three state busses to I/O drive circuits. One FIFO is pointed X-to-Y, and the other pointed Y-to-X. Either port's FIFOs can be read or written asynchronous with FIFO read or write operations on the other port. The transceiver is activated with a low on $\overline{G}$.

Once the transceiver is activated, direction is controlled by the R_X/DIR pin. A high on R_X/DIR points the transceiver X-to-Y; a low points it Y-to-X. A low on $\overline{G}$ disables FIFO operations. Activating the Transceiver during FIFO operations may result in invalid or unpredictable FIFO operation.

AC ELECTRICAL CHARACTERISTICS

(T_A = 0° to 70°C, V_{CC} = 5.0 ±10%)

ALT. SYMBOL	STD. SYMBOL	PARAMETER	55		70		UNITS	NOTES
			MIN	MAX	MIN	MAX		
t_P	t_{RL-RH}	Read Pulse Width	55		70		ns	
t_P	t_{WL-WH}	Write Pulse Width	55		70		ns	
t_P	t_{GH-RH}	X-ceiver Disable to end of Read	55		70		ns	
t_P	t_{GH-WH}	X-ceiver Disable to end of Write	55		70		ns	
t_R	t_{RH-RL}	Read Recovery Time	20		25		ns	
t_R	t_{WH-WL}	Write Recovery Time	20		25		ns	
t_R	t_{RH-WL}	Read Write Recovery Time	20		25		ns	
t_R	t_{WH-RL}	Write Read Recovery Time	20		25		ns	
t_C	t_{RL-RL}	Read Cycle Time	75		95		ns	
t_C	t_{WL-WL}	Write Cycle Time	75		95		ns	
t_{DS}	t_{DV-WH}	Data Set Up Time	20		25		ns	
t_{DH}	t_{WH-DX}	Data Hold Time	5		5		ns	
t_{QL}	t_{RL-QL}	$\overline{R}$ Low to Outputs Low-Z	5		5		ns	2
t_A	t_{RL-QV}	Read Access Time		55		70	ns	3
t_{OH}	t_{RH-QX}	Output Hold Time	5		5		ns	3
t_{OH}	t_{WL-QX}	Output Hold Time	5		5		ns	3
t_{QZ}	t_{RH-QZ}	$\overline{R}$ High to Outputs High-Z		30		40	ns	2
t_{WQZ}	t_{WL-QZ}	$\overline{W}$ Low to Outputs High-Z		45		55	ns	2
t_{FL1}	t_{WL-FFL}	$\overline{W}$ Low to Full Flag Low		60		80	ns	4
t_{FL1}	t_{RL-EFL}	$\overline{R}$ Low to Empty Flag Low		60		80	ns	4
t_{FH1}	t_{WH-EFH}	$\overline{W}$ Hi to Empty Flag High		50		65	ns	4
t_{FH1}	t_{RH-FFH}	$\overline{R}$ Hi to Full Flag High		50		65	ns	4
t_{FL2}	t_{WL-AFL}	$\overline{W}$ Low to Almost Full Flag Low		60		80	ns	5
t_{FL2}	t_{RL-AEL}	$\overline{R}$ Low to Almost Empty Flag Low		60		80	ns	5
t_{FH2}	t_{WH-AEH}	$\overline{W}$ Hi to Almost Empty Flag High		75		95	ns	5
t_{FH2}	t_{RH-AFH}	$\overline{R}$ Hi to Almost Full Flag High		75		95	ns	5
t_I	t_{WL-FFH}	Write Protect Indeterminate		25		30	ns	6
t_I	t_{RL-EFH}	Read Protect Indeterminate		25		30	ns	7
t_{FR}	t_{FFH-WL}	Full Flag Recovery	0		0		ns	6
t_{FR}	t_{EFH-RL}	Empty Flag Recovery	0		0		ns	7
t_{RS}	$t_{RSL-RSH}$	Reset Pulse Width	55		70		ns	

AC ELECTRICAL CHARACTERISTICS

(T_A = 0° to 70°C, V_{CC} = 5.0 ±10%)

ALT. SYMBOL	STD. SYMBOL	PARAMETER	55		70		UNITS	NOTES
			MIN	MAX	MIN	MAX		
t_{RSR}	t_{RSH-WH}	Reset Recovery Time	75		95		ns	
t_{RFV}	$t_{RSL-FFH}$	Reset to Full Flag Valid		70		90	ns	3
t_{RFV}	$t_{RSL-AFH}$	Reset to $\overline{AF}$ Flag Valid		70		90	ns	3
t_{RFV}	$t_{RSL-EFL}$	Reset to Empty Flag Valid		70		90	ns	3
t_{RFV}	$t_{RSL-AEL}$	Reset to $\overline{AE}$ Flag Valid		70		90	ns	3
t_{RQX}	t_{RSL-QX}	Outout Hold from $\overline{RS}$ Low	0		0		ns	3
t_{RQZ}	t_{RSL-QZ}	RS Low to Output High Z		40		50	ns	2
t_{FG}	t_{WH-GL}	FIFO Mode to X-ceiver Mode	0		0		ns	
t_{FG}	t_{RH-GL}	FIFO Mode to X-ceiver Mode	0		0		ns	
t_{GF}	t_{GH-WL}	X-ceiver Mode to FIFO Mode	5		5		ns	
t_{GF}	t_{GH-RL}	X-ceiver Mode to FIFO Mode	5		5		ns	
t_{GQL}	t_{GL-QL}	$\overline{G}$ to Output Low Z	0		0		ns	2
t_{GQV}	t_{GL-QV}	$\overline{G}$ to Output Valid		75		95	ns	3
t_{GQX}	t_{GH-QX}	Output Hold from $\overline{G}$	0		0		ns	3
t_{GQZ}	t_{GH-QZ}	$\overline{G}$ to Output High Z		40		50	ns	2
t_{DVQV}	t_{DV-QV}	Input to Output Valid		55		70	ns	3
t_{DXQX}	t_{DX-QX}	Input to Output Invalid	10		10		ns	3
t_{DQL}	$t_{DIRV-QL}$	$\overline{R}_X$/DIR to Output Low Z	0		0		ns	2
t_{DQV}	$t_{DIRV-QV}$	$\overline{R}_X$/DIR to Output Valid		55		70	ns	3
t_{DQX}	$t_{DIRV-QX}$	Output Hold from $\overline{R}_X$/DIR	0		0		ns	3
t_{DQZ}	$t_{DIRV-QZ}$	$\overline{R}_X$/DIR to Output High Z		40		50	ns	2

NOTES

1. All AC Electrical Characteristics measured under conditions specified in "AC Test Conditions".
2. Measured w/5pf Output Load. See Equivalent Load Circuit B.
3. Measured w/30pf Output Load. See Equivalent Load Circuit A.
4. Applies to $\overline{EF}_X$, $\overline{FF}_X$, $\overline{FF}_Y$, $\overline{EF}_Y$. Measured w/30pf Output Load. See Equivalent Load Circuit C.
5. Applies to $\overline{AE}_X$, $\overline{AF}_X$, $\overline{AE}_Y$, $\overline{AF}_Y$. Measured w/30pf Output Load. See Equivalent Load Circuit C.
6. Writes beginning a) more than t_I (max) before $\overline{FF}$ goes high will be blocked. b) less than t_I (max) before and less than t_{FR} (min) after $\overline{FF}$ goes high may be performed. c) t_{FR} (min) after $\overline{FF}$ goes high will be performed.
7. Reads beginning a) more than t_I (max) before $\overline{EF}$ goes high will be blocked. b) less than t_I (max) before and less than t_{FR} (min) after $\overline{EF}$ goes high may be performed. c) t_{FR} (min) after $\overline{EF}$ goes high will be performed.

Read/Write

The FIFOs utilize separate Read and Write enable inputs to control port activity and direction. A low on a Read Enable reads a port's receive FIFO. A high on a Read Enable or a low on a Write Enable disables a port's data outputs to a high impedance state. A low on a Write Enable initiates a write to a port's transmit FIFO, regardless of the state of Read Enable. Input data is latched into the FIFO on the rising edge of a Write Enable.

Full/Empty Flags

An active Full Flag indicates that a port's transmit FIFO is full and will accept no more data. Writes done to a FIFO while full are blocked. Once a read has occurred on a full FIFO, clearing a location in the FIFO, the Full Flag will go inactive, allowing another write to begin on the next falling edge of Write Enable.

An active Empty Flag indicates a port's receive FIFO is empty and can send no more data. Any reads done on a FIFO while empty are blocked. Once a write to an empty FIFO has occurred, the Empty Flag will go inactive, allowing another read to begin on the next falling edge of Read Enable.

Almost Flags

An inactive Almost Full flag indicates a port's transmit FIFO has room for at least four (4) more bytes, which is to say the flag will go active during the fourth write from full and stay active until after the fourth location from full has been vacated (read). An inactive Almost Empty flag indicates a port's receive FIFO has at least four (4) bytes of data in memory, ready to be read, which is to say that the flag will go active while reading the fourth remaining byte and remain active until after the fourth byte has been stored (written).

Reset

Reset is initiated by a low on the Master Reset ($\overline{RS}$) input. A reset returns all data outputs to a high impedance state, taking precedence over the read strobes ($\overline{R_X}$/DIR and $\overline{R_Y}$) and $\overline{G}$. The states of the FIFO control inputs ($\overline{R_X}$/DIR, $\overline{W_X}$, $\overline{R_Y}$ and $\overline{W_Y}$) are a Don't Care throughout reset. The read strobes are a Don't Care at the end of reset because the Empty Flag becomes active (goes low) during reset, blocking any attempted reads. The write strobes ($\overline{W_X}$ and $\overline{W_Y}$) may fall any time during or after reset, but must not go high until t_{RSR} after $\overline{RS}$ goes high.

FIGURE 4. WRITE TIMING

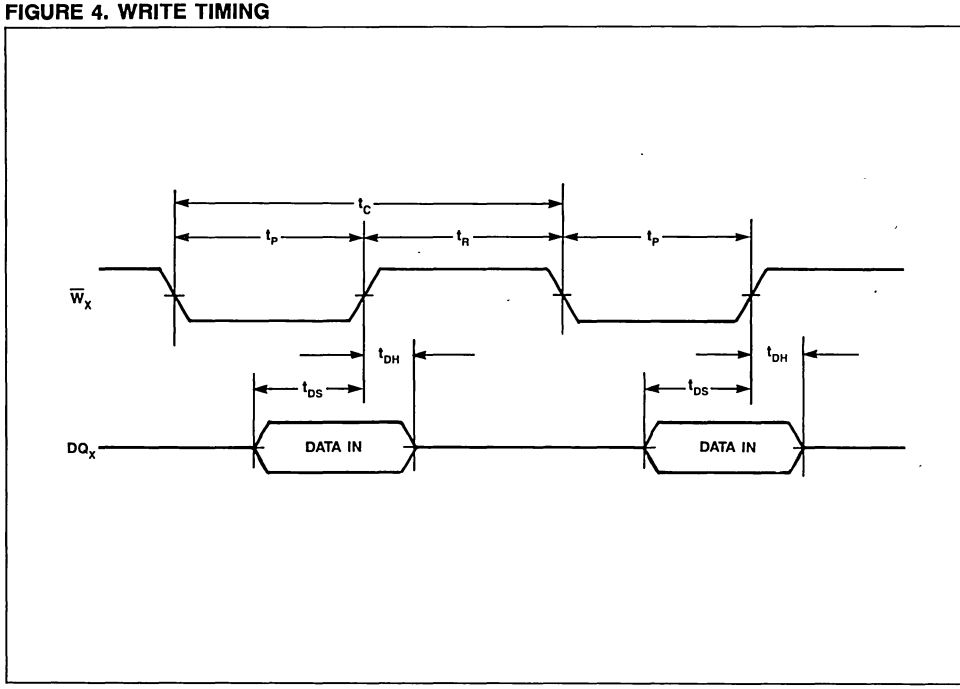


FIGURE 5. READ TIMING

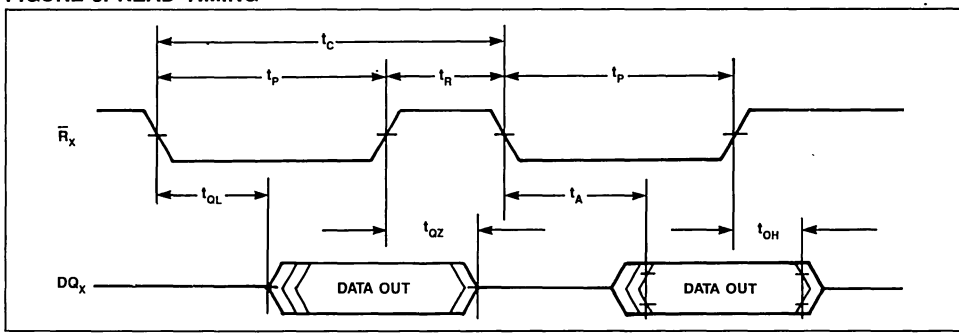


FIGURE 6. WRITE/READ TIMING

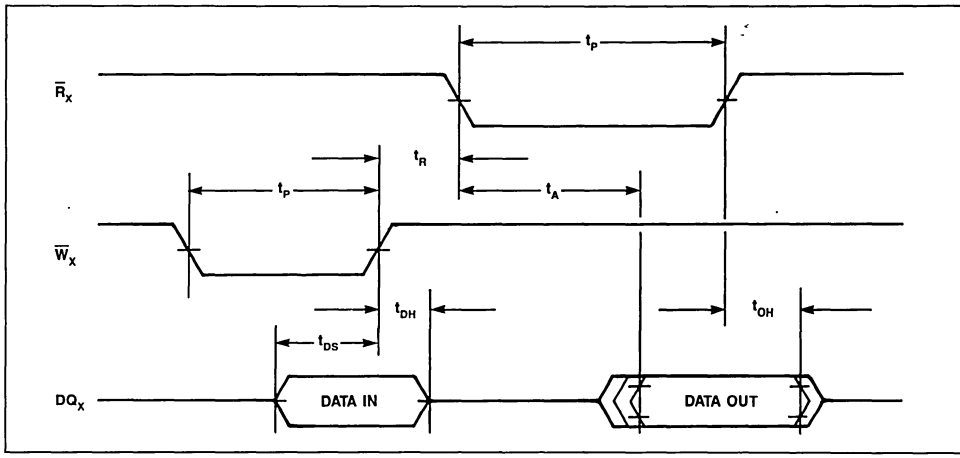


FIGURE 7. READ/WRITE TIMING

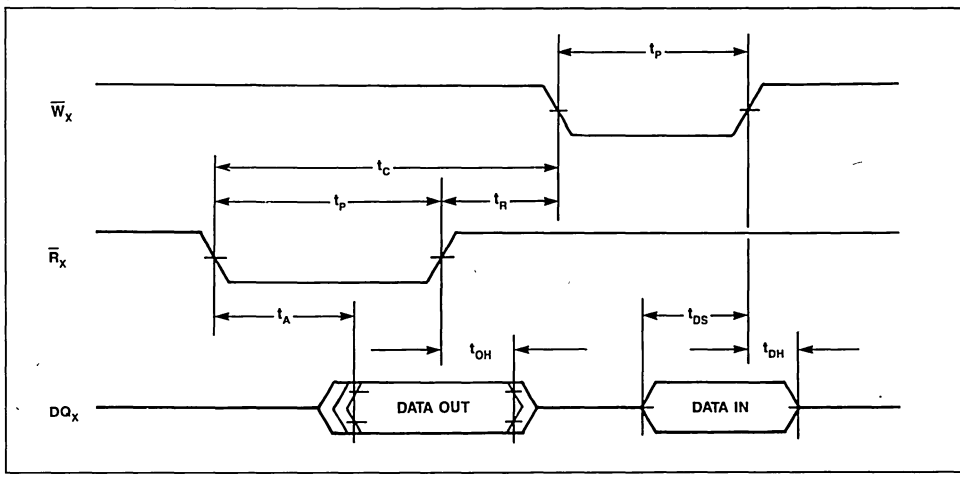


FIGURE 8. FULL (ALMOST FULL) FLAG TIMING

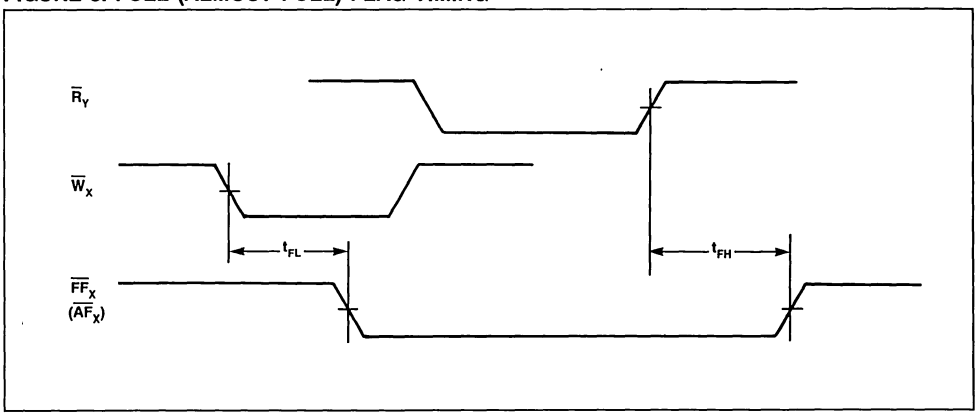


FIGURE 9. EMPTY (ALMOST EMPTY) FLAG TIMING

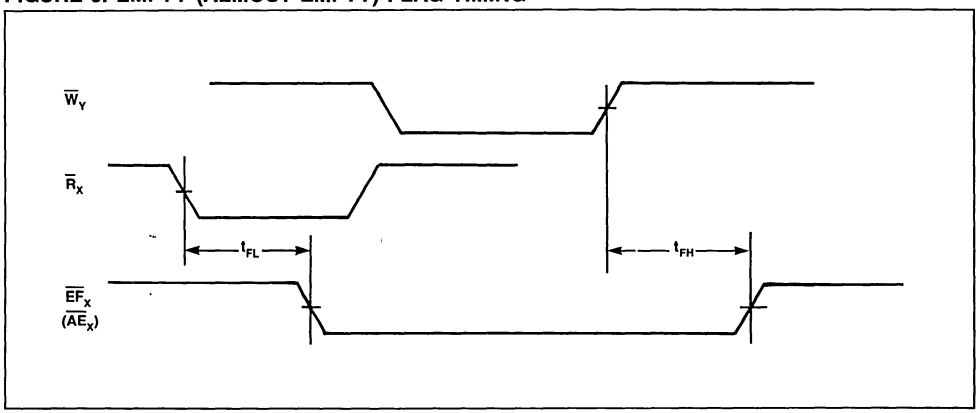


FIGURE 10. FIRST WRITE AFTER FULL TIMING

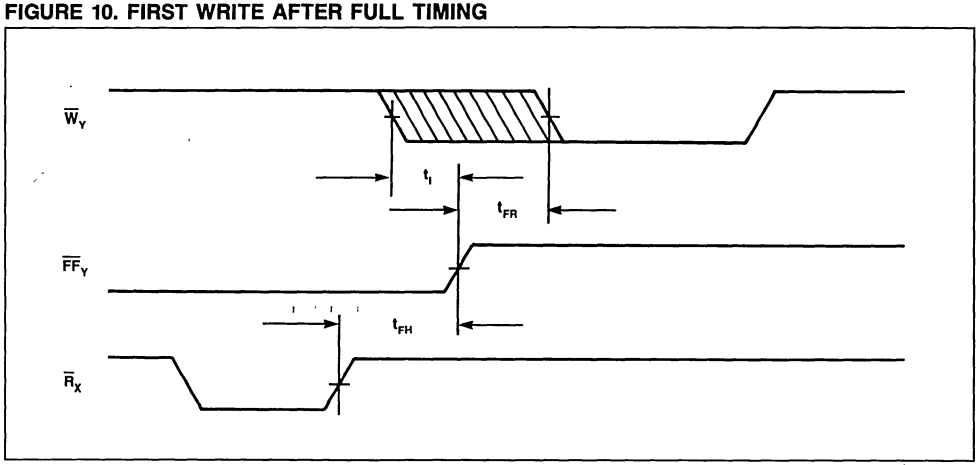


FIGURE 11. FIRST READ AFTER EMPTY TIMING

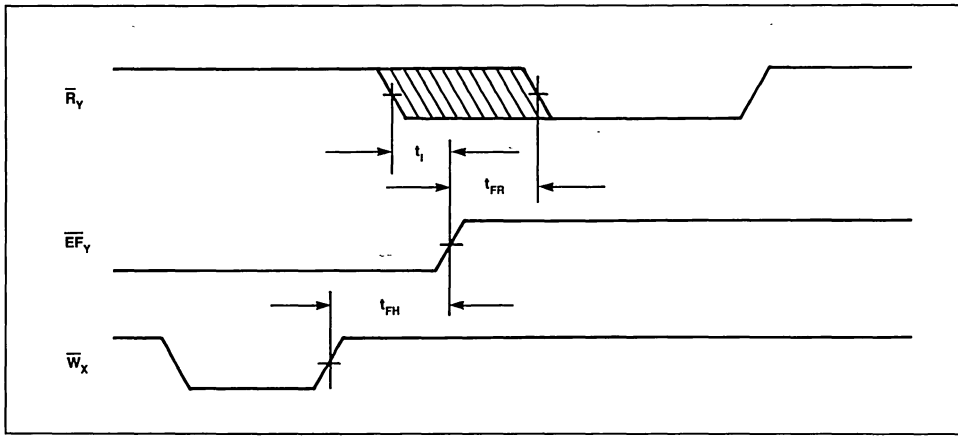


FIGURE 12. FIFO RESET TIMING

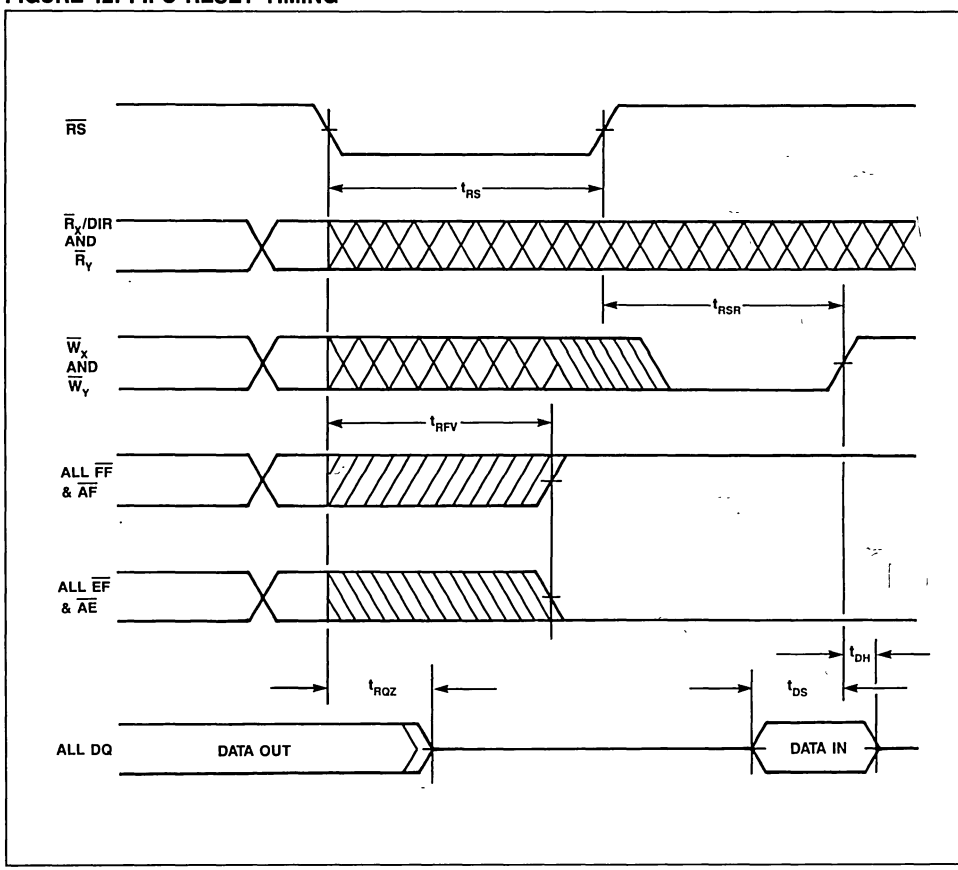


FIGURE 13. TRANSCEIVER RESET TIMING (EXAMPLE SHOWN WITH $\overline{R_X}$/DIR HIGH)

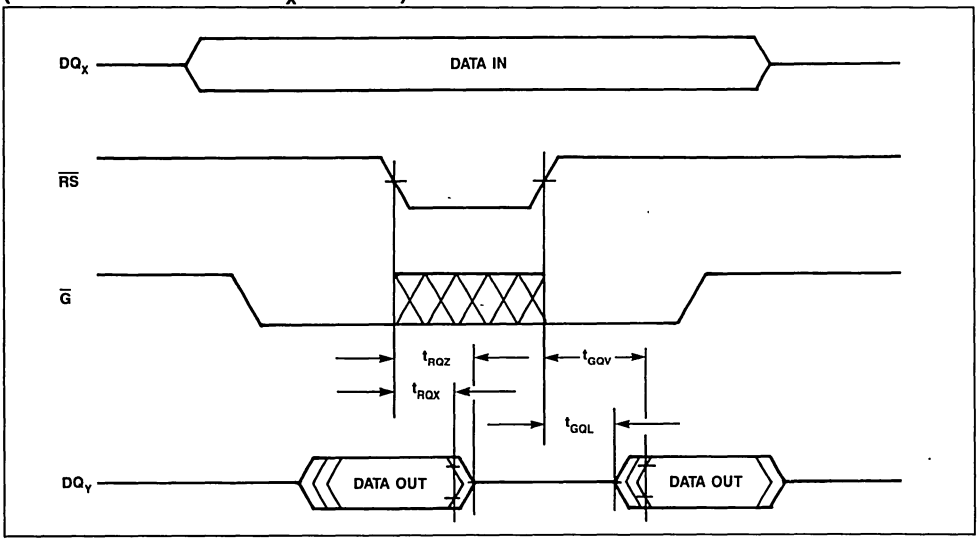


FIGURE 14. FIFO MODE/TRANSCEIVER MODE TRANSITION

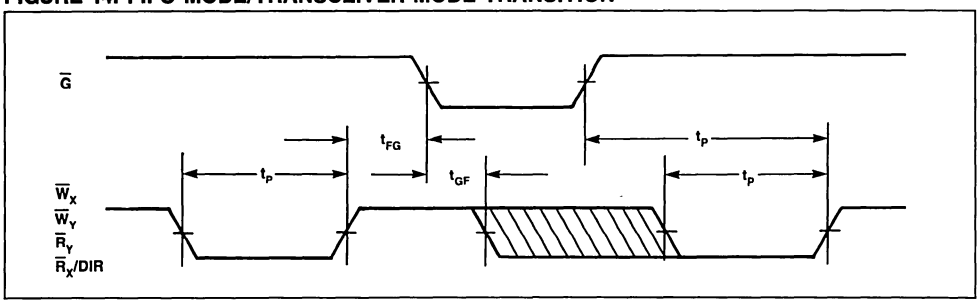


FIGURE 15. TRANSCEIVER $\overline{G}$ TIMING (EXAMPLE SHOWN WITH $\overline{R_X}$/DIR HIGH)

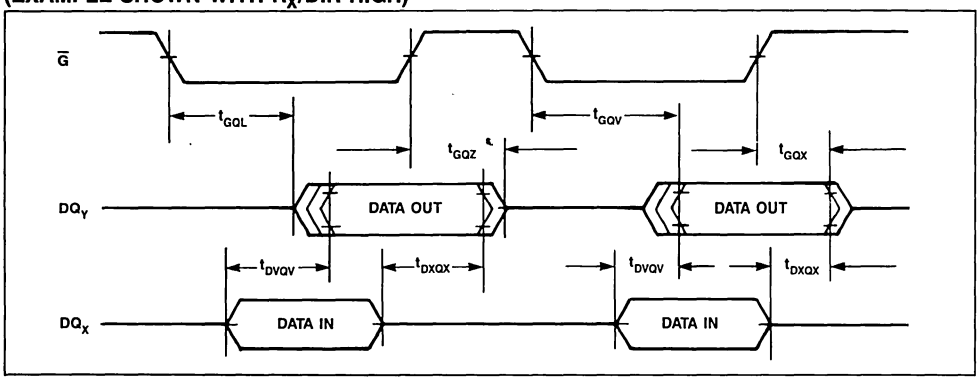


FIGURE 16. TRANSCEIVER $\overline{R_X}$/DIR TIMING
(EXAMPLE SHOWN WITH $\overline{G}$ LOW)

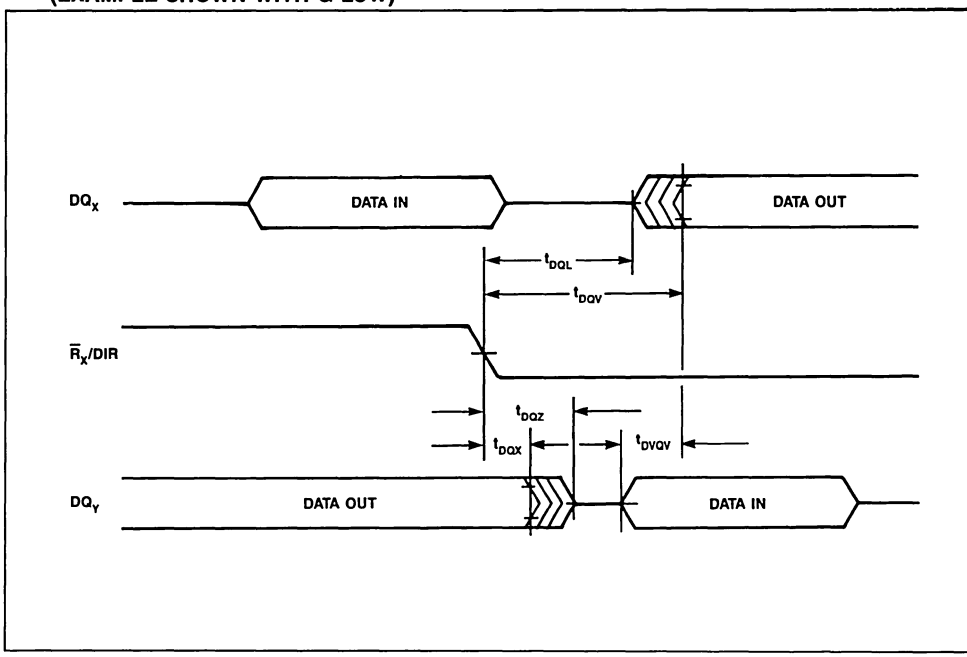


FIGURE 17. WRITE/ALMOST FULL/FULL FLAG TIMING SUMMARY

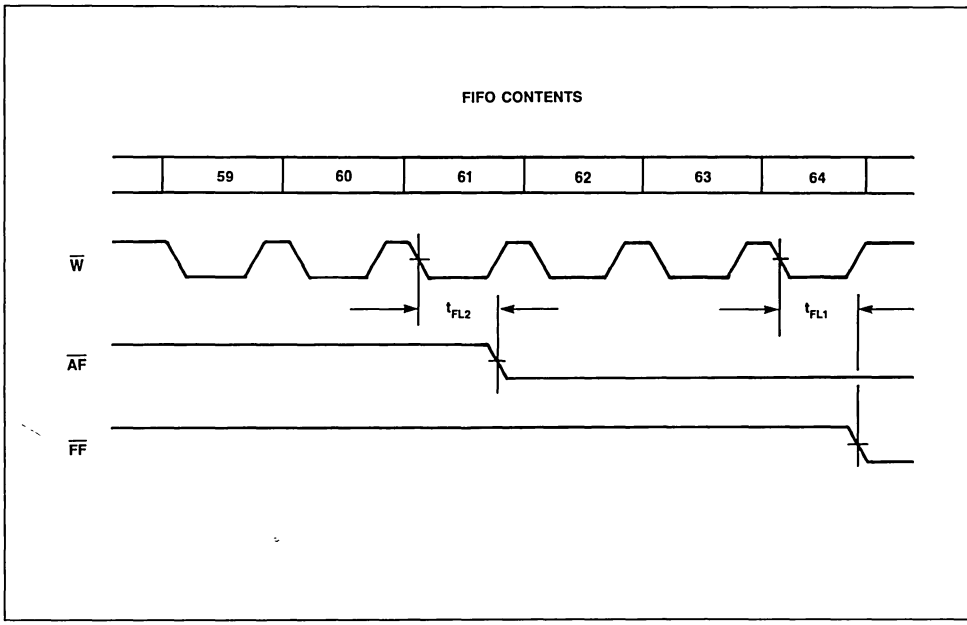


FIGURE 18. WRITE/ALMOST EMPTY/EMPTY FLAG TIMING SUMMARY

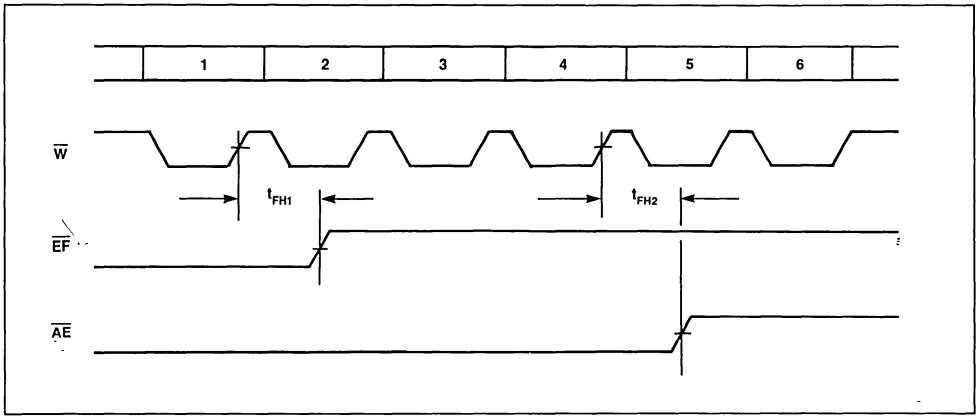


FIGURE 19. READ/ALMOST EMPTY/EMPTY FLAG TIMING SUMMARY

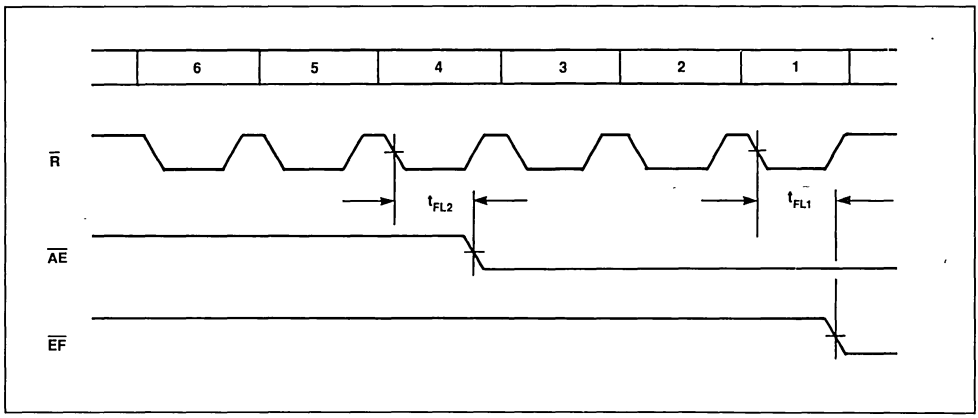
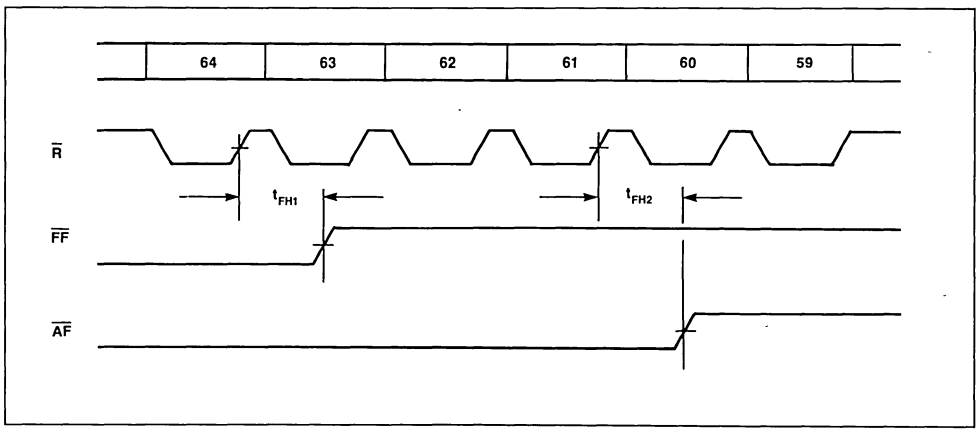


FIGURE 20. READ/ALMOST FULL/FULL FLAG TIMING SUMMARY



ABSOLUTE MAXIMUM RATINGS*

Parameter	Value	Unit
Voltage on any Pin Relative to V_{SS}	− 1.5 to + 7.0	V
Ambient Operating Temperature (T_A)	0 to + 70	°C
Ambient Temperature under Bias	− 55 to + 125	°C
Ambient Storage Temperature (plastic)	− 55 to + 125	°C
Allowable Total Device Power Dissipation	1	W
Allowable RMS Output Current per Pin	80	mA

* Stresses greater than those listed "Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A = 0° to + 70°C)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic 1 Input	2.2		V_{CC} + 0.3	V	1
V_{IL}	Logic 0 Input	− 0.3		0.8	V	1

DC ELECTRICAL CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 5.0 ± 10%)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
I_{CCQ}	Quiescent Power Supply Current, per Port			25	mA	1,2
I_{CCA}	Active Power Supply Current, per Port			40	mA	1,3
I_{CCD}	Dynamic Power Supply Current, per Port			1.2	mA/MHz	1,4
I_{CCT}	Total Power Supply Current, both Ports			100	mA	1,5
I_{IL}	Input Leakage Current	− 1		+ 1	µA	6
I_{OL}	Output Leakage Current	− 10		+ 10	µA	7
V_{OH}	Logic 1 Output Voltage	2.4			V	7,8
V_{OL}	Logic 0 Output Voltage			0.4	V	7,9

Notes : 1. Measured with outputs open.
2. Measured with opposite port quiescent ; $\overline{R}$, $\overline{W}$ and $\overline{G}$ ≥ V_{IH} (Min).
3. Measured with opposite port quiescent ; $\overline{R}$ or $\overline{W}$ ≤ V_{IL} (Max) and $\overline{G}$ ≥ V_{IH} (Min).
4. Measured with opposite port quiescent ; R or W toggling and G ≥ V_{IH} (Min).
5. Measured with both ports operating at t_C (min.).
6. Measured with V_{IN} = 0.0V to V_{CC}.
7. All voltages referenced to V_{SS}.
8. Data Output Pins (DQ_{X0}-DQ_{X4} and DQ_{Y0}-DQ_{Y4}) I_{OUT} = - 12mA ; Flag Output Pins $\overline{EF_X}$, $\overline{EF_Y}$, $\overline{FF_X}$, $\overline{FF_Y}$, $\overline{AE_X}$, $\overline{AE_Y}$, $\overline{AF_X}$, $\overline{AF_Y}$) I_{OUT} = −1mA.
9. Data Outputs (DQ_{X0}-DQ_{X4} and DQ_{Y0}-DQ_{Y4}) I_{OUT} = 12mA , Flag Output Pins $\overline{EF_X}$, $\overline{EF_Y}$, $\overline{FF_X}$, $\overline{FF_Y}$, $\overline{AE_X}$, $\overline{AE_Y}$, $\overline{AF_X}$, $\overline{AF_Y}$) I_{OUT} = 4mA.

CAPACITANCE (T_A = 0° to 70°C, V_{CC} = 5.0 ± 10%)

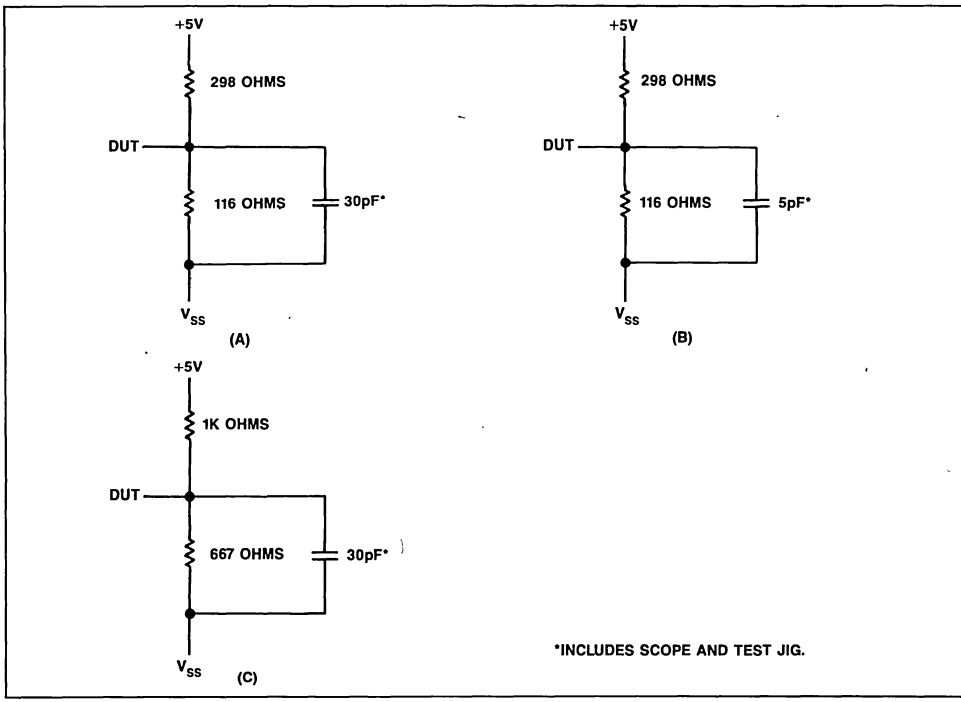
Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
C_I	Input Capacitance		4	5	pF	1
C_O	Output Capacitance		8	10	pF	1

Note : 1. Sampled, not 100% tested. Measured at 1 MKz.

AC TEST CONDITIONS

Input Levels ..... 0 to 3 Volts
Transition Times ..... 5 ns
Input and Output Reference Levels ..... 1.5 Volts
Ambient Temperature ..... 0° to 70°C
V_{CC} = 5.0 Volts ± 10%

FIGURE 21. EQUIVALENT OUTPUT LOAD CIRCUIT



APPLICATION ISSUES

Width Expansion

The MK45264/65 is designed to be used in sets of two or more, as shown below. The MK45264/65 is supplied in two configurations, MK45264 and MK45265; the MK45264 having Empty and Full Flags, the MK45265 having Almost Empty and Almost Full Flags. This scheme allows a pair of devices to be connected in such a way as to assure that the PAIR present a full complement of status flags in BOTH directions, that is, both to the left and to the right.

The resulting 10 bit wide configuration allows both parity AND beginning or end of message flag bits to be carried along with an 8 bit byte of data. The 20 bit wide configuration allows carrying 2 bits of parity AND separate message start and stop bits in 16 bit applications.

The MK45264/65 was designed as a 5 bit wide device in order to allow the use of a 300 mil DIP package; allowing the MK45264/65 to: a) achieve the highest function/board space ratio possible for a fully featured bidirectional BiPORT FIFO, b) provide higher performance with improved noise margins than would be possible in higher pin count packages, and c) provide greater flexibility to users of various bus widths.

FIGURE 22. (64x10)x2 WIDTH EXPANSION

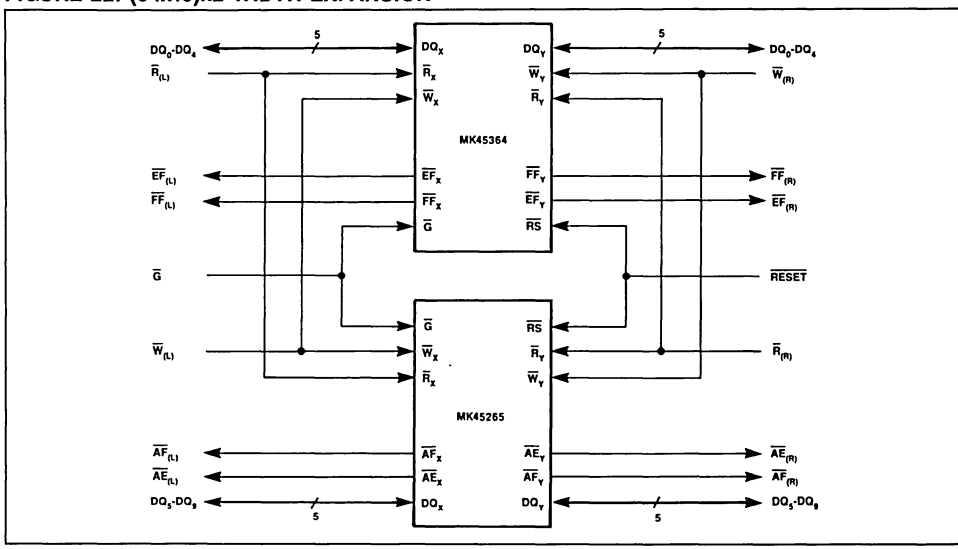
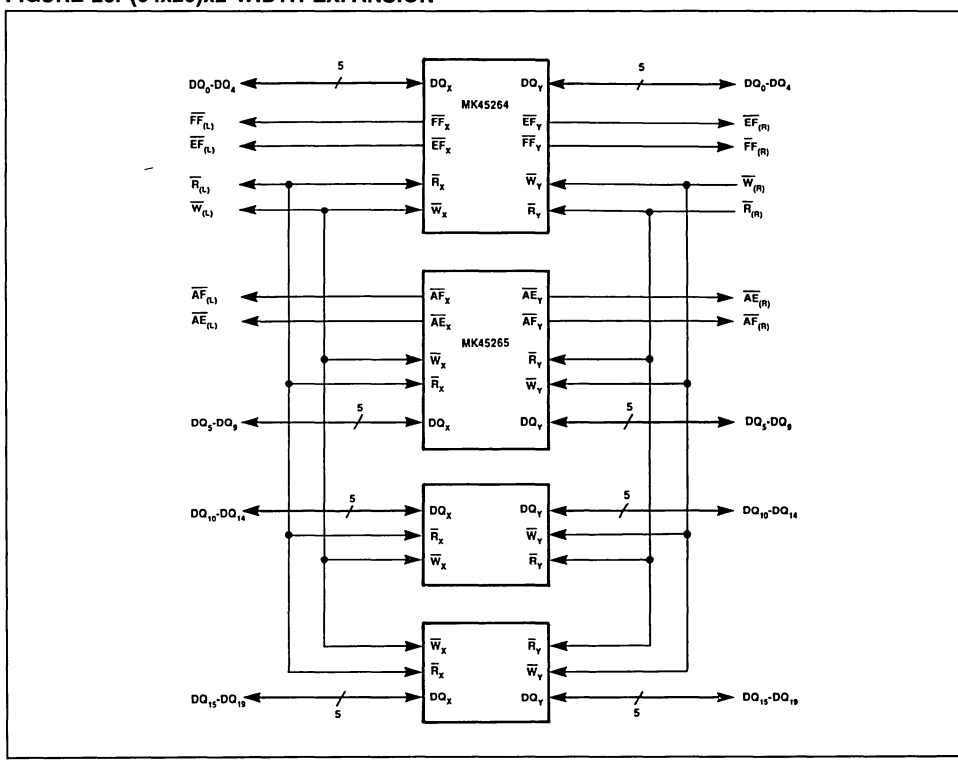


FIGURE 23. (64x20)x2 WIDTH EXPANSION



Width Expansion and Word-Skew

Word-skew, in this context, is defined as what happens when FIFOs that are wired in parallel for width expansion get out of sync with one another. Halting writes when full and reads when empty circumvents the problems altogether. Reading while empty and writing while full should, therefore, be avoided. The problem of word-skew can emerge if one is using the MK45264/65 in width expansion mode AND writing (or reading) WHILE full (or WHILE empty).

Slight differences in Full (or Empty) Flag response delays between different devices may result in "disagreements" between adjacent devices as they go from Full to Not Full or from Empty to Not Empty; resulting in one device accepting an attempted write (or read) while an adjacent device blocks the cycle. The simplest approach to avoiding word skew is configuring the system using the FIFOs to begin reading only when the Almost Empty flag has gone high, rather than right after the Empty flag has gone high. In like manner, waiting to write until the Almost Full flag goes high, rather than right after the Full flag goes high will prevent the problem, which is why the Almost flags are provided. However, should such a scheme prove unworkable in a particular appication, the addition of an external flag latching circuit can also solve the problem.

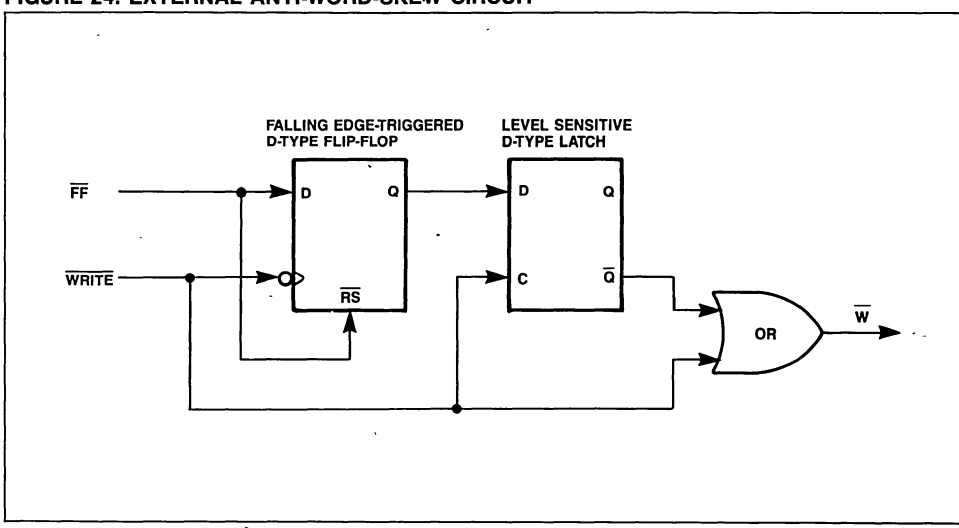
The circuit shown below, when connected to the Write strobe and Full Flag, latches the status of the flag at the beginning of a write. If the flag is inactive, the Write strobe is passed through to the FIFO. When the flag goes active (low) the falling-edge triggered flop is reset. The reset flop, in concert with the level-sensitive latch and the OR gate block the write strobe.

Tying the Flag to the Reset input of the edge-triggered flop assures that the Write strobe is blocked on the first write attempted after the flag falls. The level sensitive latch also prevents transitions in the flag from disturbing cycles that are already in progress. In the event that a write is begun just as the flag is going inactive (high) the falling edge-triggered flop will latch its interpretation of the metastable flag. If it interprets the metastable input as being low, the present and next cycle are blocked, as were their predecessors. If it interprets the flag as being high, the present cycle is still blocked, because the level sensitive latch was still seeing an active flag as the cycle began. However, the next attempted cycle is passed through.

Although "throwing away" write cycles goes against the grain conceptually, it does not actually present a problem in this situation. It must be assumed that Writing while Full or Reading while Empty would only be allowed in applications where the write and/or read strobes are proceeding regardless of FIFO status anyway. "Throwing away" reads or writes cannot, by definition, be considered an error.

Remember, overall signal timing must comprehend the delays of the particular components chosen to implement the external circuit.

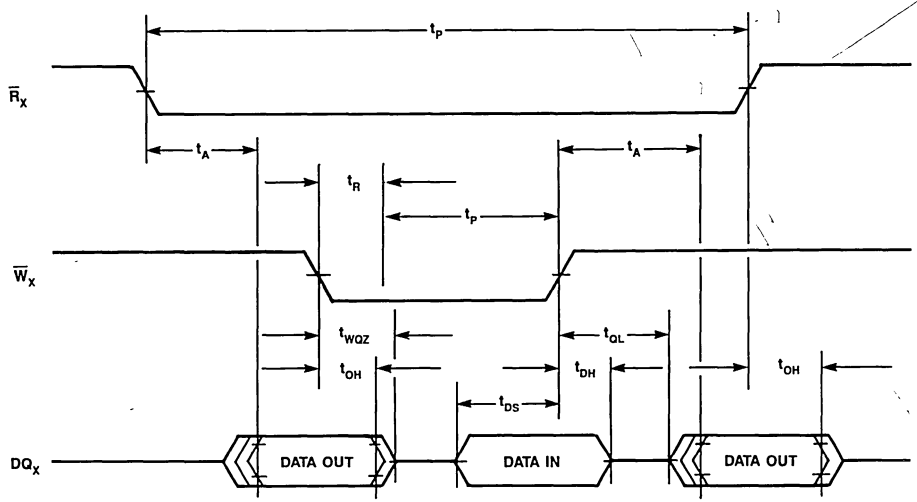
FIGURE 24. EXTERNAL ANTI-WORD-SKEW CIRCUIT



Overlapping Read and Write Strobes

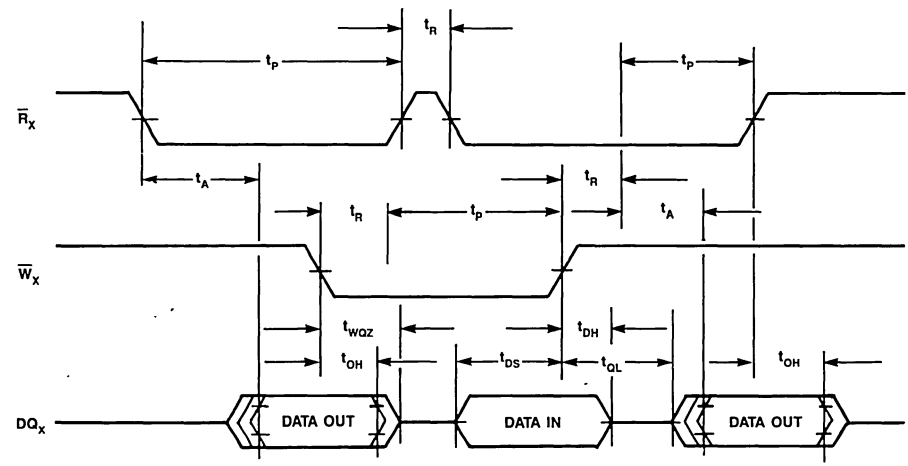
Overlapping Read and Write strobes on a given port is neither tested nor recommended. The following timing diagrams are provided only to illustrate the relationship between the control functions.

FIGURE 25. OVERLAPPING READ/WRITE TIMING



NOTE: THE SECOND D OUT IS THE SAME AS THE FIRST. A OVERLAPPING WRITE DOES NOT INCREMENT THE READ ADDRESS COUNTER.

FIGURE 26. OVERLAPPING READ/WRITE TIMING



NOTE: THE SECOND D OUT IS NOT THE SAME AS THE FIRST. IT IS, IN FACT, THE NEXT READ DATA. AN OVERLAPPING WRITE DOES NOT BLOCK THE READ STROBE FROM INCREMENTING THE READ ADDRESS COUNTER.

ORDERING INFORMATION

PART NO.	ACCESS TIME	R/W CYCLE TIME	CLOCK FREQ.	PACKAGE TYPE	TEMPERATURE RANGE
MK45264N-55	55 ns	75 ns	13.3 MHz	24 Pin Plastic DIP	0° to 70°C
MK45265N-55	55 ns	75 ns	13.3 MHz	24 Pin Plastic DIP	0° to 70°C
MK45264N-70	70 ns	95 ns	10.5 MHz	24 Pin Plastic DIP	0° to 70°C
MK45265N-70	70 ns	95 ns	10.5 MHz	24 Pin Plastic DIP	0° to 70°C

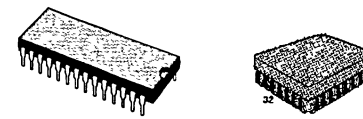
SGS-THOMSON MICROELECTRONICS

MK45H01/02/03(N,K) -25/35/50/65/12

HIGH SPEED 512/1K/2K x 9 CMOS BiPORT™ FIFO

ADVANCE DATA

- FIRST-IN-FIRST-OUT MEMORY BASED ARCHITECTURE
- FLEXIBLE x 9 ORGANIZATIONS : MK45H01 (512 x 9), MK45H02 (1K x 9), MK45H03 (2K x 9)
- LOW POWER, HIGH SPEED HCMOS TECHNOLOGY
- ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE
- FULLY EXPANDABLE IN WORD WIDTH AND DEPTH
- EMPTY AND FULL WARNING FLAGS
- RETRANSMIT CAPABILITY
- HALF-FULL FLAG IN SINGLE DEVICE MODE



N
DIP–28
(Plastic Package)

K
PLCC32
(Plastic Chip Carrier)

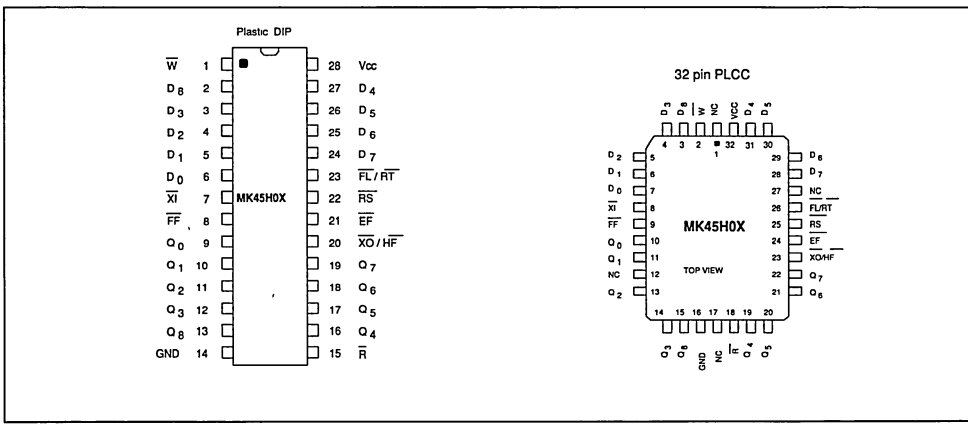
DESCRIPTION

The MK45H01, MK45H02, and MK45H03 are members of the BiPORT FIFO Family from SGS-THOMSON Microelectronics, which utilize special two-port memory cell techniques. Specifically, these devices implement a First-In-First-Out (FIFO) algorithm, featuring asynchronous read/write operations, full, empty, and half full status flags, and unlimited expansion capability in both word size and depth. The full and empty flags are provided to prevent data overflow and underflow. The data is loaded and emptied on a first-in-first-out basis, and the latency for retrieval of data is approximately one load (write) cycle. These devices feature a read/write cycle time of only 35ns (28.5MHz).

PIN NAMES

$\overline{W}$	= Write	$\overline{XI}$	= Expansion In
$\overline{R}$	= Read	$\overline{XO}$	= Expansion Out
$\overline{RS}$	= Reset	$\overline{FF}$	= Full Flag
$\overline{FL/RT}$	= First Load/ Retransmit	$\overline{EF}$ $\overline{HF}$	= Empty Flag = Half-full Flag
D_{0-8}	= Data In	V_{CC}	Power, +5 V
Q_{0-8}	= Data Out	GND	= Ground

Figure 1 : Pin Connections.



DESCRIPTION (continued)

The reads and writes are internally sequential through the use of separate read and write pointers in a ring counter fashion. Therefore, no address information is required to load or unload data. Data is loaded and unloaded with the use of W (write), and R (read) input pins. Separate data in (D_0-D_8) and data out (Q_0-Q_8) pins allow simultaneous and asynchronous read/write operations, provided the status flags are not protecting against data underflow or overflow.

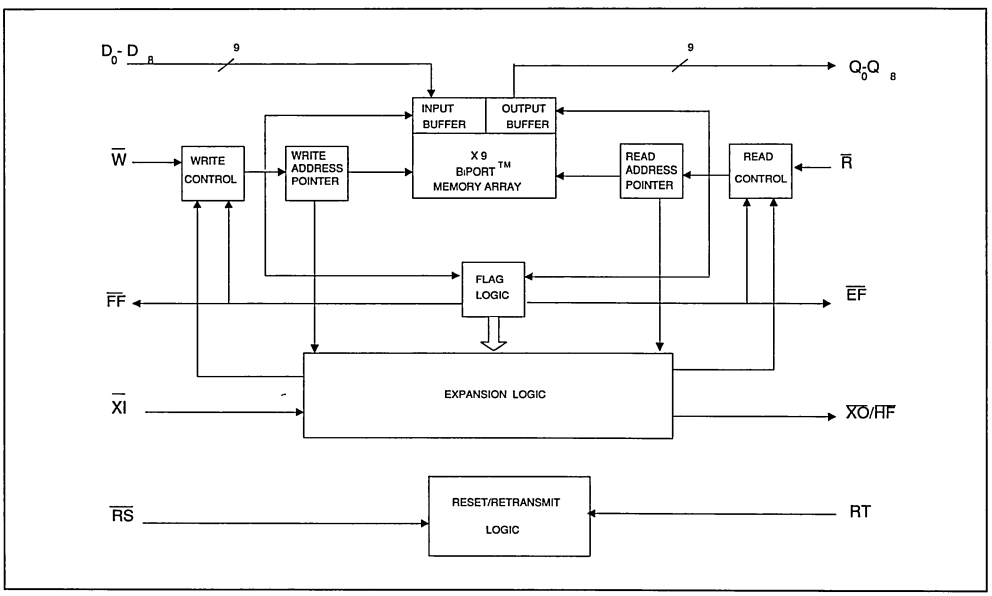
The main application of these devices is a buffer for sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The MK45H01, MK45H02, and MK45H03 incorporate 9-bit wide data arrays that provide for support control or parity bit functions. This feature is helpful in data communications where the extra parity bit is used for transmission and reception error checking. These devices also offer retransmit (RT) and half-full features in single device or width expansion modes. The retransmit function allows data to be re-read by resetting the read pointer while not disturbing the write pointer. This is for applications where the FIFO is not full, or is written with less than 512, 1024, or 2048 words. The MK45H01, MK45H02, and MK45H03 continue our 28-pin industry standard pin-out assignment.

FUNCTIONAL DESCRIPTION

Unlike conventional shift register based FIFOs, the MK45H01, MK45H02, and MK45H03 employ a memory-based architecture wherein a byte written into the device does not "ripple through". Instead, a byte written into the device is stored in a specific location, where it remains until over-written. The byte can be read and re-read as often as desired in the single device configuration.

Two internal pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written. The address pointers automatically loop back to address zero after reaching the final address in the FIFO (512, 1024, or 2048). The empty, half full, and full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

Figure 2 : MK45H0X Block Diagram.



ABSOLUTE MAXIMUM RATINGS*

Parameter	Value	Unit
Voltage on any Pin Relative to Ground	- 0.3 to + 7.0	V
Operating Temperature	0 to + 70	°C
Storage Temperature	- 55 to + 125	°C
Power Dissipation	1	Watt
Output Current	20	mA

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq + 70°C$)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{CC}	Supply Voltage	4.5		5.5	V	3
GND	Ground	0		0	V	
V_{IH}	Logic "1" Voltage all Inputs	2.0		V_{CC} + 1.0	V	3
V_{IL}	Logic "0" Voltage all Inputs	- 0.3		0.8	V	3

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq + 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Value			Units	Notes
		Min.	Typ.	Max.		
I_{CC1}	Average VCC Power Supply Current			120	mA	6
I_{CC2}	Average Standby Current (R = W = RS = FL/RT = VIH)			12	mA	6
I_{CC3}	Power Down Current (Inputs ≥ VCC – 0.2V)			2	mA	6
I_{IL}	Input Leakage Current (Any Input)	– 1.0		1.0	µA	4
I_{OL}	Output Leakage Current	– 10.0		10.0	µA	5
V_{OH}	Output Logic 1 Voltage (IOUT = – 4.0mA)	2.4			Volts	3
V_{OL}	Output Logic 0 Voltage (IOUT = 8.0mA)			0.4	Volts	3

Notes : 1. Pulse widths less than minimum values are not allowed.
2. Measured using output load shown in Output Load Circuit.
3. All voltages are referenced to ground.
4. Measured with $0.4 \leq V_{IN} \leq V_{CC}$.
5. $\overline{R} \geq V_{IH}$, $0.4 \geq V_{OUT} \leq V_{CC}$.
6. I_{CC} measurements are made with outputs open.

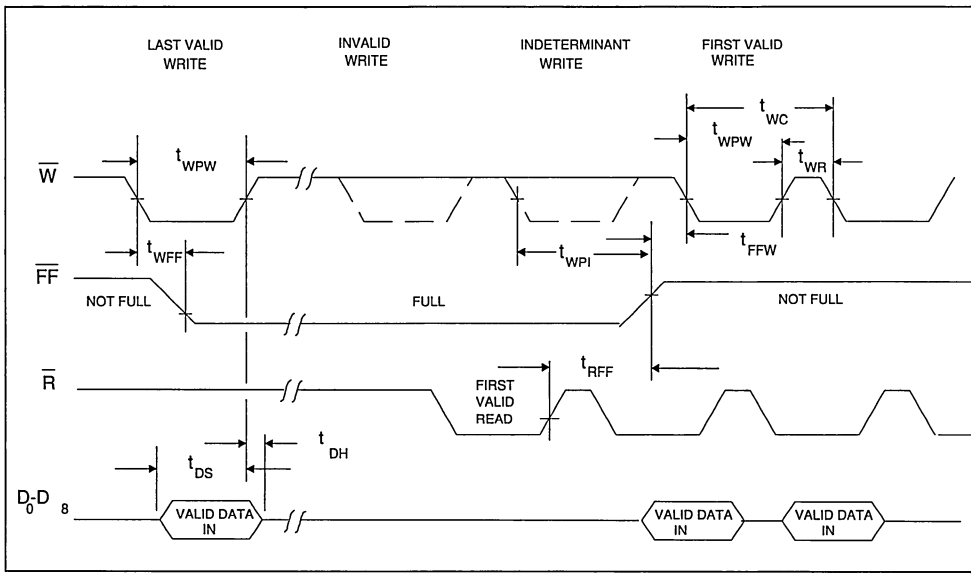
Resetting the FIFO simply resets the write and read pointers to location zero. Pulsing retransmit resets the read address pointer without effecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading individual FIFOs. The penalty of cascading is often unacceptable ripple through delays. The MK45H01, MK45H02, and MK45H03 allow implementation of very large FIFOs with no timing penalties. The memory-based architecture of the device allows connecting the read, write, data in, and data out lines of the device in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in and expansion-out pins.

WRITE MODE

The MK45H0X initiates a Write Cycle (see figure 3A) on the falling edge of the Write Enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not asserted. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of W. The data is stored sequentially and independent of any ongoing Read operations. FF is asserted during the last valid write as the MK45H0X becomes full. Write operations begun with FF low are inhibited. FF will go high t_{RFF} after completion of a valid READ operation. FF will again go low t_{WFF} from the beginning of a subsequent WRITE operation, provided that a second READ has not been completed (see figure 4A). Writes beginning t_{FFW} after FF goes high are valid. Writes beginning after FF goes low and more than t_{WPI} before FF goes high are invalid (ignored). Writes beginning less then t_{WPI} before FF goes high and less then t_{FFW} later may or may not occur (be valid), depending on internal flag status.

Figure 3A : Write and Full Flag Timing.



AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = +5.0V \pm 10\%$)

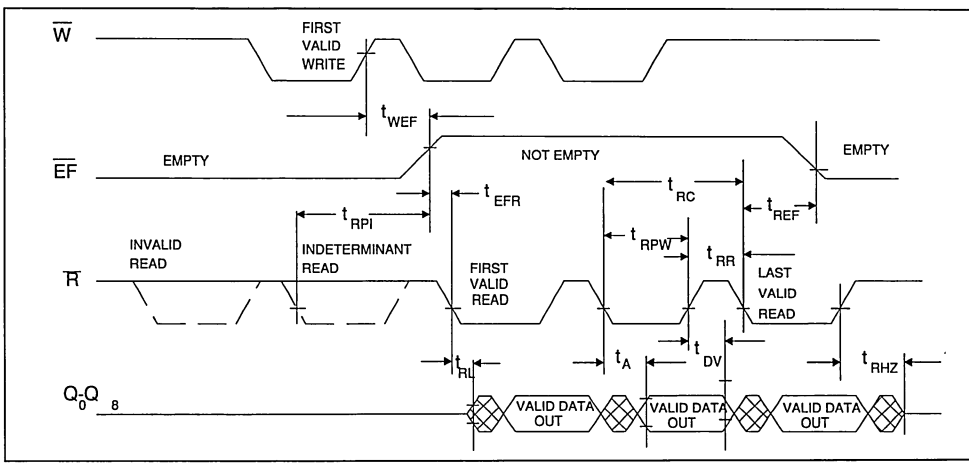
Sym.	Parameter	-25		-35		-50		-65		-120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	35		45		65		80		140		ns	
t_{WPW}	Write Pulse Width	25		35		50		65		120		ns	1
t_{WR}	Write Recovery Time	10		10		15		15		20		ns	
t_{DS}	Data Set Up Time	15		18		30		30		40		ns	
t_{DH}	Data Hold Time	0		0		0		0		0		ns	
t_{WFF}	$\overline{W}$ Low to $\overline{FF}$ Low		30		35		45		60		60	ns	2
t_{FFW}	$\overline{FF}$ High to Valid Write		10		10		10		10		10	ns	2
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High		30		35		45		60		60	ns	2
t_{WPI}	Write Protect Indeterminant	10		10		10		10		10		ns	2

READ MODE

The MK45H0X initiates a Read Cycle (see figure 3B) on the falling edge of Read Enable control input (R), provided that the Empty Flag (EF) is not asserted. In the read mode of operation, the MK45H0X provides a fast access to data from 9 of the locations in the static storage array. The data is accessed on a FIFO basis independent of any ongoing WRITE operations. After R goes high, data outputs will return to a high impedance condition until the next read operation.

In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further READ operations will be inhibited (the data inputs will remain in high impedance). EF will go high t_{WEF} after completion of a valid WRITE operation. EF will again go low t_{REF} from the beginning a subsequent read operation, provided that a second WRITE has not been completed (see figure 4B). Reads beginning t_{EFR} after EF goes high are valid. Reads begun after EF goes high are invalid (ignored). Reads beginning less than t_{RPI} before EF goes high and less then t_{EFR} later may or may not occur (be valid) depending on internal flag status.

Figure 3B : Read and Empty Flag Timing.



AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = +5.0V \pm 10\%$)

Sym.	Parameter	-25		-35		-50		-65		-120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	35		45		65		80		140		ns	
t_A	Access Time		25		35		50		65		120	ns	2
t_{RR}	Read Recovery Time	10		10		15		15		20		ns	
t_{RPW}	Read Pulse Width	25		35		50		65		120		ns	1
t_{RL}	$\overline{R}$ Low to Low Z	0		0		0		0		0		ns	2
t_{DV}	Data Valid from $\overline{R}$ High	5		5		5		5		5		ns	2
t_{RHZ}	$\overline{R}$ High to High Z		18		20		25		25		35	ns	2
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low		30		35		40		60		60	ns	2
t_{EFR}	$\overline{EF}$ High to Valid Read		10		10		10		10		10	ns	2
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High		30		35		45		60		60	ns	2
t_{RPI}	Read Protect Indeterminant	10		10		10		10		10		ns	2

Figure 4A : Read/Write to Full Flag.

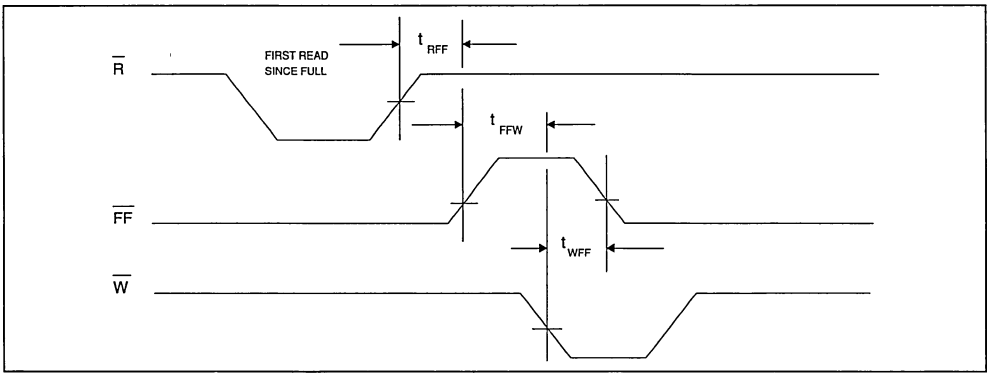
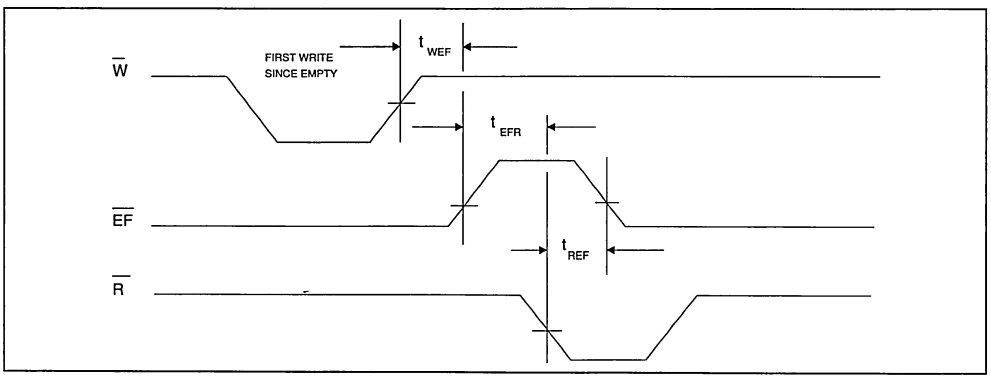


Figure 4B : Write/Read to Empty Flag.

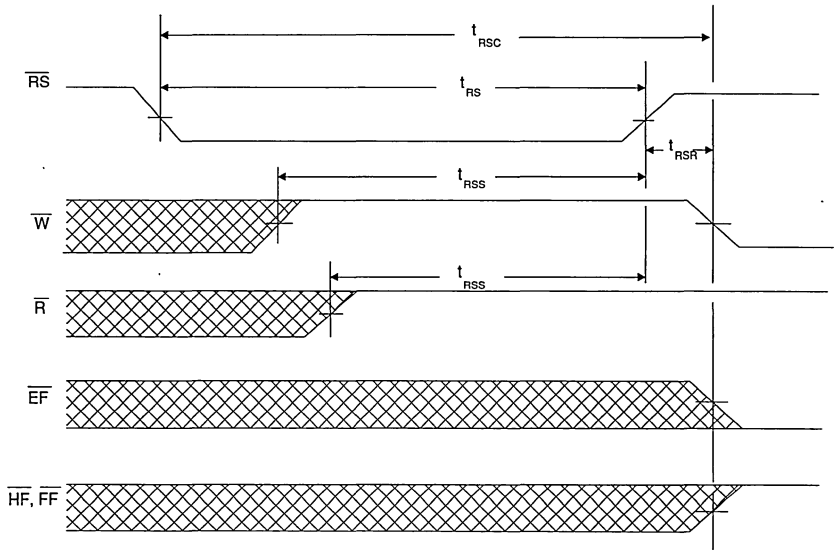


RESET

The MK45H0X is reset (see figure 5) whenever the Reset pin (RS) is in the low state. During a reset, both the internal read and write pointers are set to the first location. Reset is required after power up, before a WRITE operation can begin.

Although neither $\overline{W}$ or $\overline{R}$ need be high when $\overline{RS}$ goes low, both R and W must be high t_{RSS} before RS goes high, and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of FL/RT and XI during Reset.

Figure 5 : Reset.



Note : $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Reset, but flags will be valid at t_{RSC}.

AC ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ + 70°C) (V_{CC} = + 5.0V ± 10%)

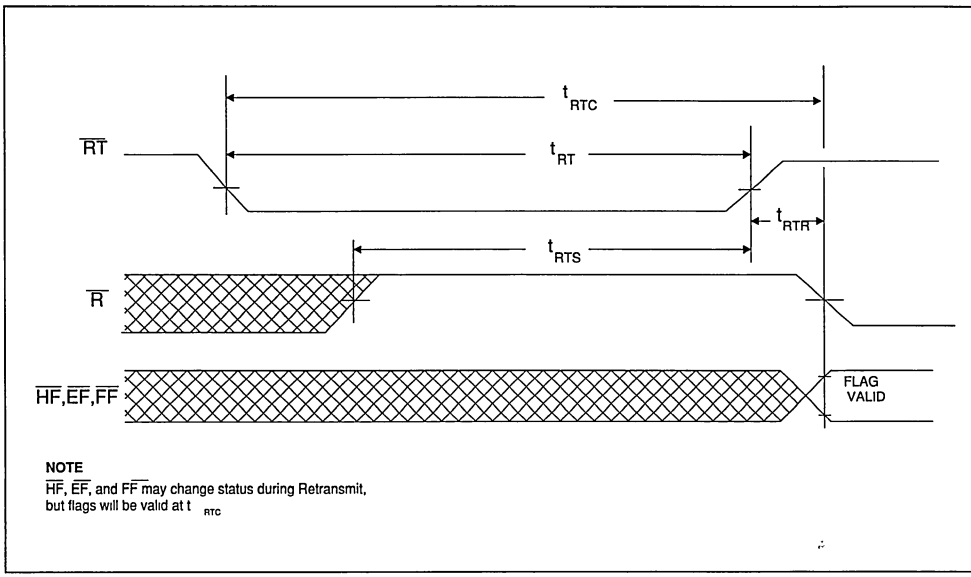
Sym.	Parameter	-25		-35		-50		-65		-120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RSC}	Reset Cycle Time	35		45		65		80		140		ns	
t_{RS}	Reset Pulse Width	25		35		50		65		120		ns	1
t_{RSR}	Reset Recovery Time	10		10		15		15		20		ns	
t_{RSS}	Reset Set Up Time	25		30		30		45		100		ns	

RETRANSMIT

The MK45H0X can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low. (See figure 6). A Retransmit operation sets the internal read pointer to the first location in the array, but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high, and must remain high for t_{RTR} afterwards.

The Retransmit function is particularly useful when blocks of less than the total FIFO depth are performed bet-ween Resets. The Retransmit feature is not compatible with Depth Expansion.

Figure 6 : Retransmit.



AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = +5.0V \pm 10\%$)

Sym.	Parameter	-25		-35		-50		-65		-120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RTC}	Retransmit Cycle Time	35		45		65		80		140		ns	
t_{RT}	Retransmit Pulse Width	25		35		10		65		120		ns	1
t_{RTR}	Retransmit Recovery Time	10		10		15		15		20		ns	
t_{RTS}	Retransmit Setup Time	25		30		30		45		100		ns	

SINGLE DEVICE CONFIGURATION

A single MK45H0X may be used when application requirements are for a depth of the device depth or less. The MK45H0X is placed in the Single Device Configuration mode when the chip is Reset with the Expansion In pin (XI) grounded (see figure 7).

WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags (EF and FF) can be detected from any one device. Figure 8 demonstrates an 18-bit word width by using two MK45H0Xs. Any word width can be attained by adding additional MK45H0Xs. The half full flag (HF) operates the same as in single device configuration.

Figure 7 : A Single MK45H0X FIFO Configuration.

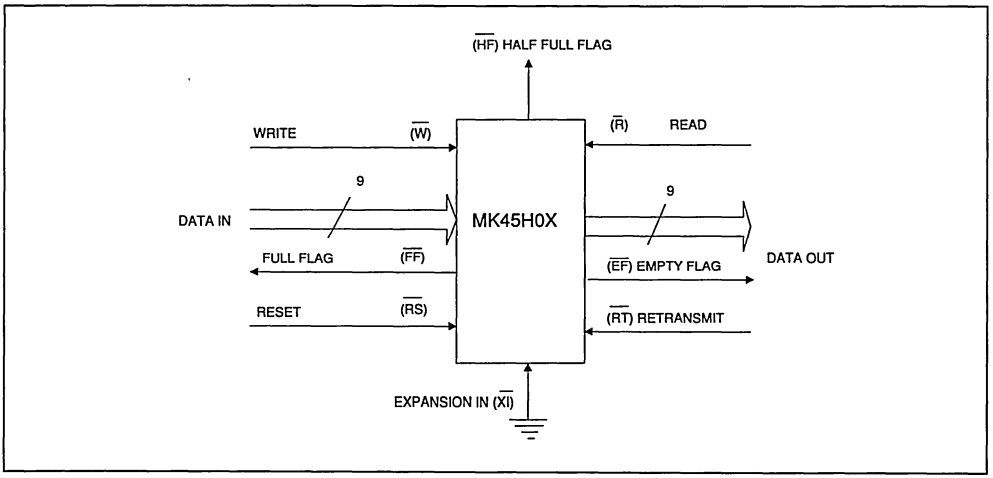
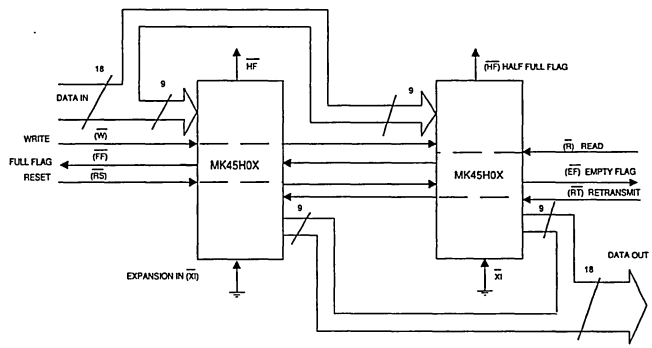


Figure 8 : MK45H0X Width Expansion FIFO Configuration.

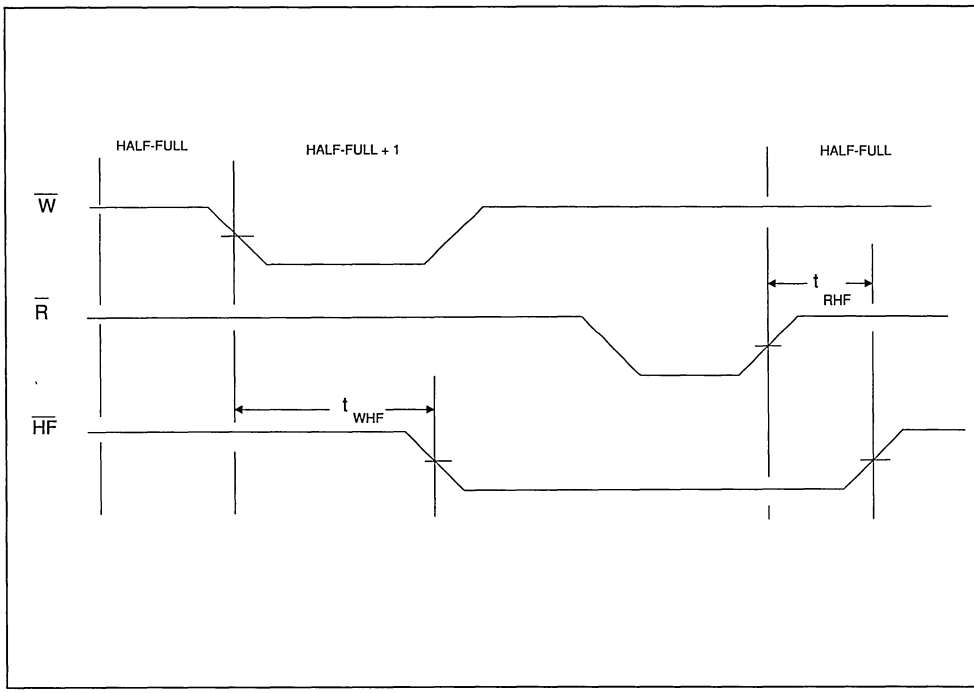


Note : Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$ signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

HALF FULL FLAG LOGIC

When in single device configuration, the ($\overline{HF}$) output acts as an indication of a half full memory. After half of the memory is filled, and at the falling edge of the next write operation, the half full flag (HF) will be set low and remain low until the difference between the write pointer and read pointer is less than or equal to one half the total memory. The half full flag (HF) is then reset by the rising edge of the read operation (see figure 9).

Figure 9 : Half Full Flag Timing.



AC CHARACTERISTICS (0°C ≤ T_A ≤ + 70°C) (V_{CC} = + 5V ± 10%)

Sym.	Parameter	-25		-35		-50		-65		-120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WHF}	Write Low to Half Full Flag Low		30		35		45		60		60	ns	
t_{RHF}	Read High to Half Full Flag High		30		35		45		60		60	ns	

DEPTH EXPANSION (daisy chain)

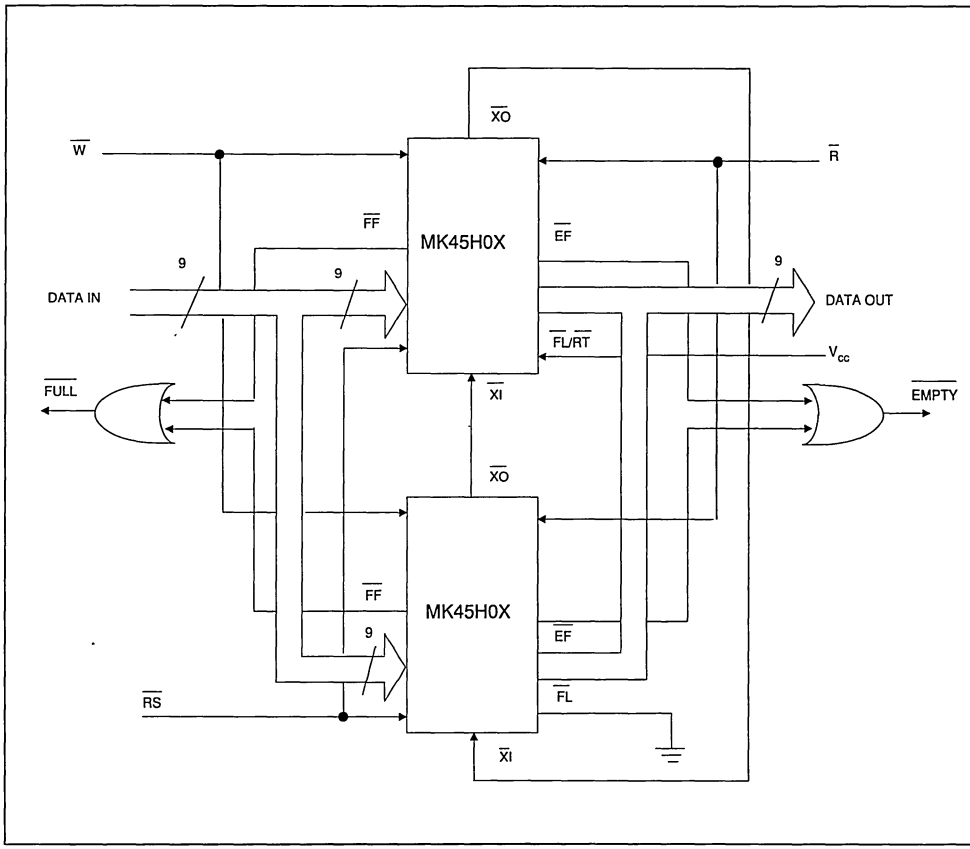
The MK45H0X can be easily adapted to applications when the requirements are greater than the individual device word depth. Figure 10 demonstrates Depth Expansion using two MK45H0Xs. Any depth can be attained by adding additional MK45H0Xs.

External logic is needed to generate a composite Full and Empty Flag. This requires the ORing of all the EFs and the ORing of all the FFs (i.e., all must be set to generate the composite FF or EF).

The MK45H0X operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions :

1. The first device must be designated by grounding the First Load pin (FL). The Retransmit function is not allowed in the Depth Expansion Mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. The Half Full Flag ($\overline{HF}$) is disabled in this mode.

Figure 10 : A Two Device Depth Expansion Configuration.

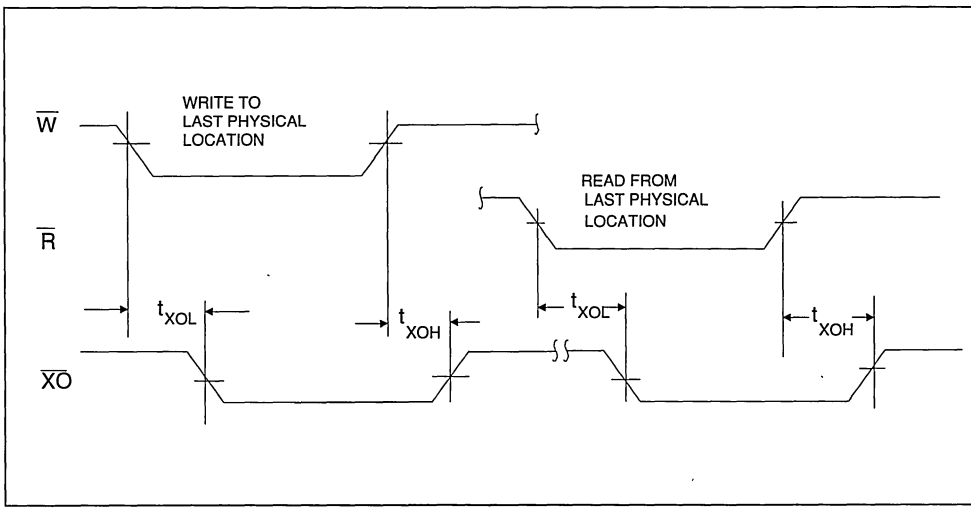


EXPANSION TIMING

Figures 11 and 12 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. In asmuch as Expansion Out pins are generally connected only to Expansion In pins, the user need not be concerned with the actual timing in a normal Depth Expanded application unless extreme propagation delays exist between the XO/XI pin pairs.

Expansion Out pulses are the image of the WRITE and READ signals that cause them ; delayed in time by t_{XOL} and t_{XOH}. The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and Empty Flags are activated, which is in response to writing and reading a last available location.

Figure 11 : Expansion Out Timing.



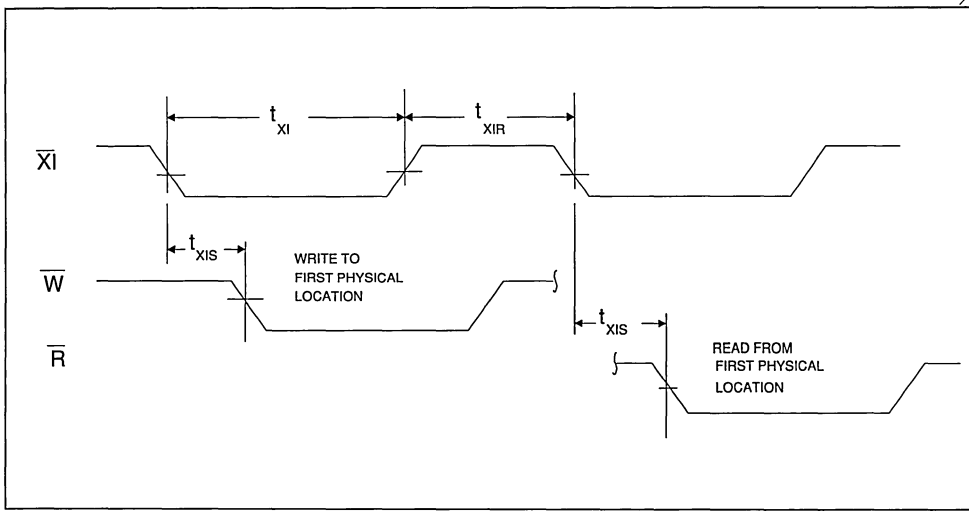
AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = +5.0V \pm 10\%$)

Sym.	Parameter	-25		-35		-50		-65		-120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XOL}	Expansion Out Low		25		35		40		55		90	ns	
t_{XOH}	Expansion Out High		25		35		40		55		90	ns	

When in Depth Expansion mode, a given MK45H0X will begin writing and reading as soon as valid WRITE and READ signals begin, provided FL was grounded at RESET time. A MK45H0X in Depth Expansion mode with FL high at RESET will not begin writing until after an Expansion in pulse occurs.

It will not begin reading until a second Expansion In pulse and the Empth Flag has gone high. Expansion In pulses must occur t_{XIS} before the WRITE and READ signals they are intended to enable. Minimum Expansion In pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

Figure 12 : Expansion In Timing.



AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = +5.0V \pm 10\%$)

Sym.	Parameter	-25		-35		-50		-65		-120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XI}	Expansion in Pulse Width	25		35		45		60		115		ns	1
t_{XIR}	Expansion in Recovery Time	10		10		10		10		10		ns	
t_{XIS}	Expansion in Setup Time	15		15		15		15		15		ns	

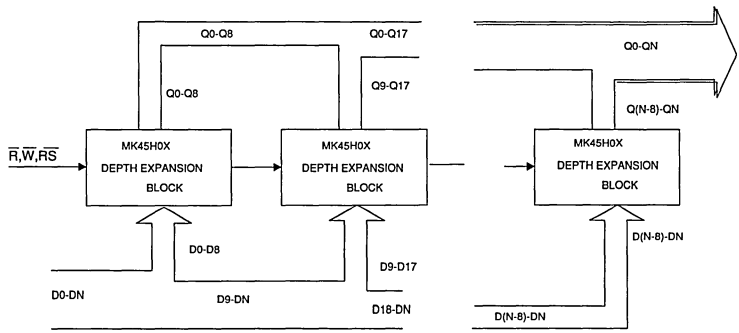
COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see figure 13).

BIDIRECTIONAL APPLICATIONS

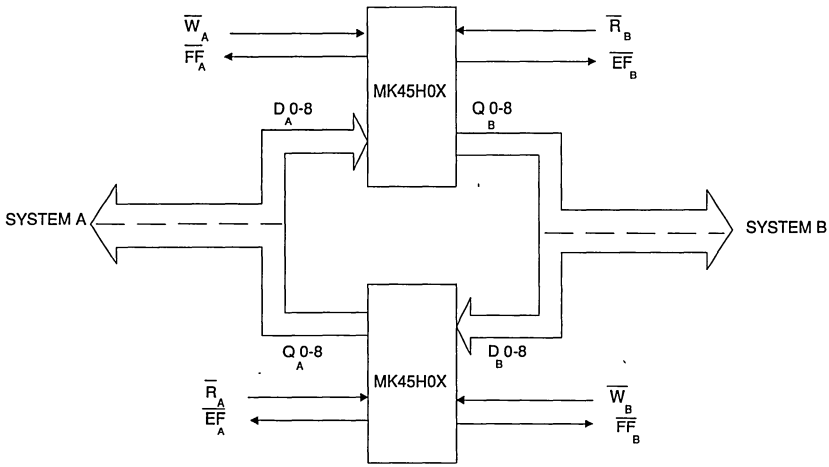
Applications, which require data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing MK45H0Xs, as shown in figure 14. Care must be taken to assure that the appropriate flag is monitored by each system. (i.e., FF is monitored on the device where W is used ; EF is monitored on the device where R is used). Both Depth Expansion and Width Expansion may be used in this mode.

Figure 13 : Compound FIFO Expansion.



Notes : 1. For depth expansion block see DEPTH EXPANSION Section and Figure 10.
2. For Flag operation see WIDTH EXPANSION Section and Figure 8.

Figure 14 : Bidirectional FIFO Application.



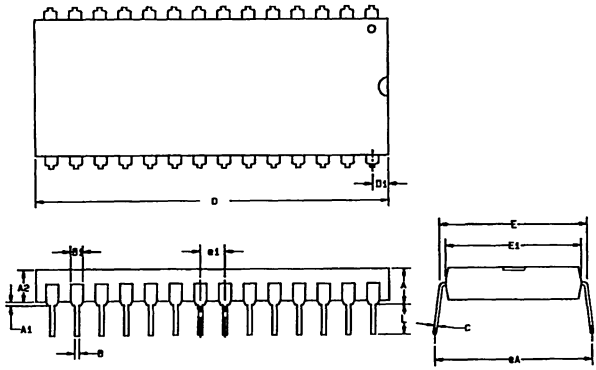
ORDER CODES

Part No	Access Time	Cycle Time	Package Type	Temperature
MK45H01N-25	25ns	35ns	600 MIL Plastic DIP	0° to 70°C
MK45H01N-35	35ns	45ns	600 MIL Plastic DIP	0° to 70°C
MK45H01N-50	50ns	65ns	600 MIL Plastic DIP	0° to 70°C
MK45H01N-65	65ns	80ns	600 MIL Plastic DIP	0° to 70°C
MK45H01N-12	120ns	140ns	600 MIL Plastic DIP	0° to 70°C
MK45H01K-25	25ns	35ns	32 PLCC	0° to 70°C
MK45H01K-35	35ns	45ns	32 PLCC	0° to 70°C
MK45H01K-50	50ns	65ns	32 PLCC	0° to 70°C
MK45H01K-65	65ns	80ns	32 PLCC	0° to 70°C
MK45H01K-12	120ns	140ns	32 PLCC	0° to 70°C
MK45H02N-25	25ns	35ns	600 MIL Plastic DIP	0° to 70°C
MK45H02N-35	35ns	45ns	600 MIL Plastic DIP	0° to 70°C
MK45H02N-50	50ns	65ns	600 MIL Plastic DIP	0° to 70°C
MK45H02N-65	65ns	80ns	600 MIL Plastic DIP	0° to 70°C
MK45H02N-12	120ns	140ns	600 MIL Plastic DIP	0° to 70°C
MK45H02K-25	25ns	35ns	32 PLCC	0° to 70°C
MK45H02K-35	35ns	45ns	32 PLCC	0° to 70°C
MK45H02K-50	50ns	65ns	32 PLCC	0° to 70°C
MK45H02K-65	65ns	80ns	32 PLCC	0° to 70°C
MK45H02K-12	120ns	140ns	32 PLCC	0° to 70°C
MK45H03N-25	25ns	35ns	600 MIL Plastic DIP	0° to 70°C
MK45H03N-35	35ns	45ns	600 MIL Plastic DIP	0° to 70°C
MK45H03N-50	50ns	65ns	600 MIL Plastic DIP	0° to 70°C
MK45H03N-65	65ns	80ns	600 MIL Plastic DIP	0° to 70°C
MK45H03N-12	120ns	140ns	600 MIL Plastic DIP	0° to 70°C
MK45H03K-25	25ns	35ns	32 PLCC	0° to 70°C
MK45H03K-35	35ns	45ns	32 PLCC	0° to 70°C
MK45H03K-50	50ns	65ns	32 PLCC	0° to 70°C
MK45H03K-65	65ns	80ns	32 PLCC	0° to 70°C
MK45H03K-12	120ns	140ns	32 PLCC	0° to 70°C
MK45H13N-25	25ns	35ns	300 MIL Plastic DIP	0° to 70°C
MK45H13N-35	35ns	45ns	300 MIL Plastic DIP	0° to 70°C
MK45H13N-50	50ns	65ns	300 MIL Plastic DIP	0° to 70°C
MK45H13N-65	65ns	80ns	300 MIL Plastic DIP	0° to 70°C
MK45H13N-12	120ns	140ns	300 MIL Plastic DIP	0° to 70°C

Part No	Access Time	R/W Cycle Time
MK45H01/2/3-25	25ns	35ns, 28.5MHz
MK45H01/2/3-35	35ns	45ns, 22.2MHz
MK45H01/2/3-50	50ns	65ns, 15.3MHz
MK45H01/2/3-65	65ns	80ns, 12.5MHz
MK45H01/2/3-12	120ns	140ns, 7.14MHz

PACKAGE DESCRIPTION

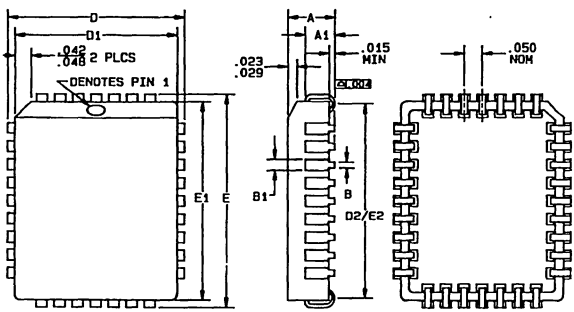
MK45H0X PLASTIC (N TYPE) DUAL–IN–LINE, 28 PINS



Dim.	mm		Inches		Notes
	Min.	Max.	Min.	Max.	
A		5.334		210	2
A1	0.381		.015		2
A2	3.556	4.064	.140	.160	
B	0.381	0.534	.015	.021	3
B1	1.27	1.778	.050	.070	
C	0.203	0.304	.008	.012	3
D	36.576	37.338	1.440	1.470	1
D1	1.651	2.159	.065	.085	
E	15.24	15.875	.600	.625	
E1	13.462	14.224	.530	.560	
e1	2.286	2.794	.090	.110	
eA	15.24	17.78	.600	.700	
L	3.048		.120		

Notes : 1. Overall length includes 010 in flash on either end of the package.
2. Package standoff to be measured per jedec requirements.
3. The maximum limit shall be increased by 003 in when solder lead finish is specified.

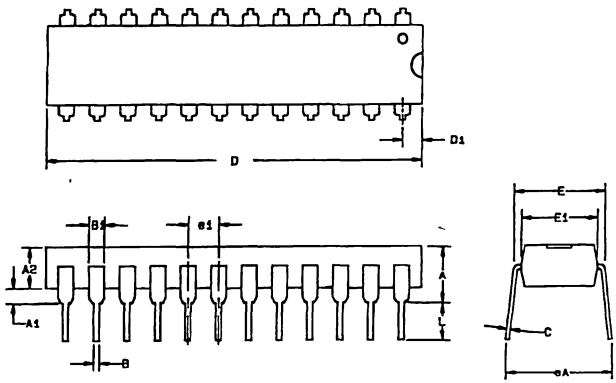
MK45H0X PLASTIC LEADED CHIP CARRIER, 32 PIN (K TYPE)



Dim.	mm		Inches	
	Min.	Max.	Min.	Max.
A	3.048	3.556	.120	.140
A1	1.981	2.413	.078	.095
B	0.330	0.533	.013	.021
B1	0.660	0.812	.026	.032
D	12.319	12.573	.485	.495
D1	11.353	11.506	.447	.453
D2	9.906	10.922	.390	.430
E	14.859	15.113	.585	.595
E1	13.893	14.046	.547	.553
E2	12.446	13.462	.490	.530

PACKAGE DESCRIPTION

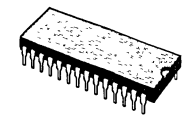
MK45H0X PLASTIC DIP (N), 28 PINS



Dim.	Inches	
	Min.	Max.
A		.210
A1	.015	
A2	.120	.140
B	.015	.021
B1	.045	.070
C	.008	.012
D		1.270
D1	.060	.090
E	.300	.325
E1	.240	.270
e1	.090	.110
eA	.300	.365
L	.125	

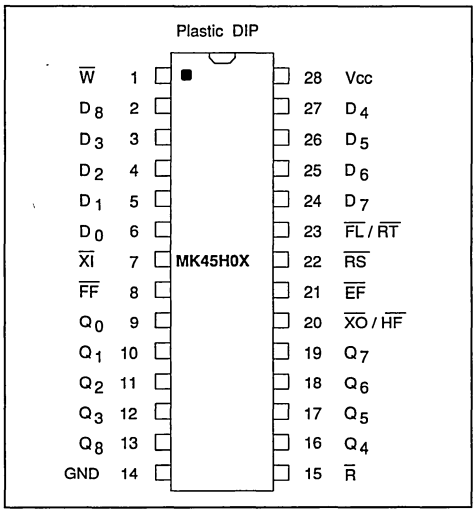
HIGH SPEED 4K x 9 / 8K x 9 CMOS BIPORT™ FIFO

- FIRST-IN-FIRST-OUT MEMORY BASED ARCHITECTURE
- FLEXIBLE 4K x 9, 8K x 9 ORGANIZATIONS
- LOW POWER, HIGH PERFORMANCE HCMOS TECHNOLOGY
- ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE
- BIDIRECTIONAL AND RATE BUFFER APPLICATIONS
- FULLY EXPANDABLE IN WORD WIDTH AND DEPTH
- EMPTY AND FULL WARNING FLAGS
- RETRANSMIT CAPABILITY
- HALF-FULL FLAG IN SINGLE DEVICE MODE



N
DIP–28
(Plastic Package)

Figure 1 : Pin Connections.



DESCRIPTION

The MK45H04 and MK45H08 are members of the BiPORT FIFO Family from SGS-THOMSON Microelectronics, which utilize special two-port memory cell techniques. Specifically, these devices implement a First-In-First-Out (FIFO) algorithm, featuring asynchronous read/write operations, full, empty, and half-full status flags, and unlimited expansion capability in both word size and depth. The full and empty flags are provided to prevent data overflow and underflow. The data is loaded and emptied on a first-in-first-out basis, and the latency for retrieval of data is approximately one load (write) cycle. These devices feature a read/write cycle time of only 35ns (28.5MHz).

The reads and writes are internally sequential through the use of separate read and write pointers in a ring counter fashion. Therefore, no address information is required to load or unload data. Data is loaded and unloaded with the use of $\overline{W}$ (write), and $\overline{R}$ (read) input pins. Separate data in (D_0-D_8) and data out (Q_0-Q_8) pins allow simultaneous and asynchronous read/write operations, provided the status flags are not protecting against data underflow or overflow.

The main application of these devices is as a rate buffer for sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The MK45H04 and MK45H08 incorporate 9-bit wide data arrays that provide for support control or parity bit functions.

PIN NAMES

$\overline{W}$	= Write	$\overline{XI}$	= Expansion in
$\overline{R}$	= Read	$\overline{XO}$	= Expansion out
$\overline{RS}$	= Reset	$\overline{FF}$	= Full Flag
$\overline{FL/RT}$	= First Load/ Retransmit	$\overline{EF}$ $\overline{HF}$	= Empty Flag = Half-full Flag
D_{0-8}	= Data in	V_{CC}	Power, + 5 Volts
Q_{0-8}	= Data out	GND	= Ground

This feature is helpful in data communications where the extra parity bit is used for transmission and reception error checking. These devices also offer retransmit ($\overline{RT}$) and half-full features in single device or width expansion modes. The retransmit function allows data to be re-read by resetting the read pointer while not disturbing the write pointer. This is for applications where the FIFO is not full, or is written with less than 4096, or 8192 words. The MK45H04 and MK45H08 continue our 28-pin industry standard pin-out assignment.

FUNCTIONAL DESCRIPTION

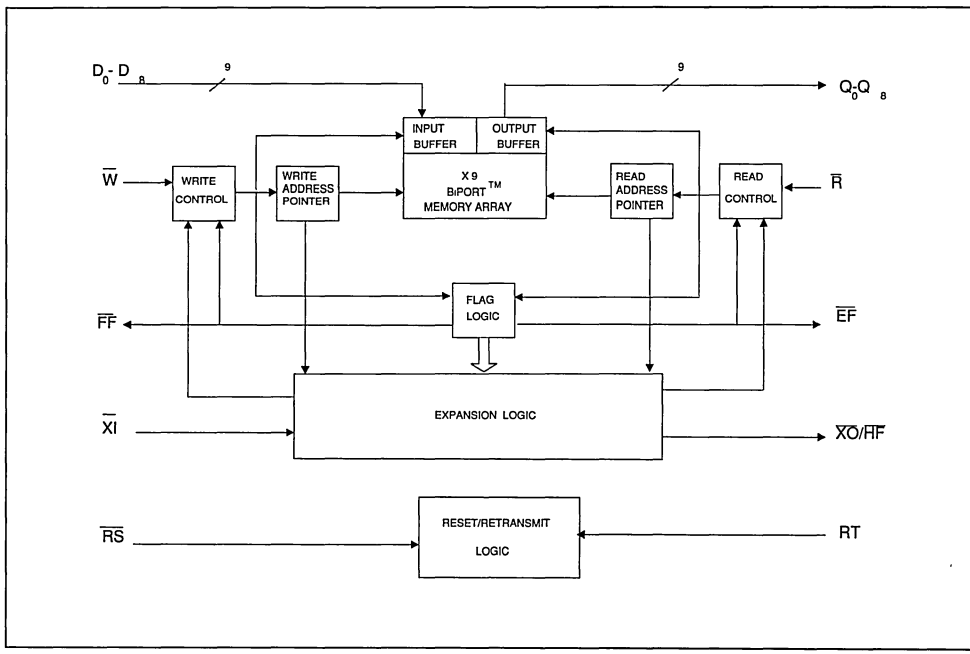
Unlike conventional shift register based FIFOs, the MK45H04 and MK45H08 employ a memory-based architecture wherein a byte written into the device does not "ripple through". Instead, a byte written into the device is stored in a specific location, where it remains until over-written. The byte can be read and re-read as often as desired in the single device configuration.

Two internal pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading unwritten bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written. The address pointers automatically loop back to address zero after reaching the final address in the FIFO (4096 or 8192). The empty, half full, and full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

Resetting the FIFO simply resets the write and read pointers to location zero. Pulsing retransmit resets the read pointer without effecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading individual FIFOs. The penalty of cascading is often unacceptable in ripple through delays. The MK45H04 and MK45H08 allow implementation of very large FIFOs with no timing penalties. The memory-based architecture of the device allows connecting the read, write, data in, and data out lines of the device in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in ($\overline{XI}$) and expansion-out ($\overline{XO}$) pins.

Figure 2 : MK45HOX Block Diagram.



ABSOLUTE MAXIMUM RATINGS*

Parameter	Value	Unit
Voltage on any Pin Relative to GND	– 0.3 to + 7.0	V
Operating Temperature	0 to + 70	°C
Storage Temperature	– 55 to + 125	°C
Power Dissipation	1	Watt
Output Current	20	mA

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Min.	Max.	Units	Notes
V_{CC}	Supply Voltage	4.5	5.5	V	3
GND	Ground	0.0	0.0	V	
V_{IH}	Logic 1 all Inputs	2.0	VCC + 1.0	V	3
V_{IL}	Logic 0 all Inputs	– 0.3	0.8	V	3

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = 5.0 \pm 10\%$)

Symbol	Parameter	Min.	Max.	Units	Notes
I_{CC1}	Average VCC power Supply Current		120	mA	6
I_{CC2}	Average Standby Current ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL/RT} = V_{IH}$)		12	mA	6
I_{CC3}	Power Down Current (Inputs $\geq V_{CC}$ - 0.2V)		2	mA	6
I_{IL}	Input Leakage Current (any input)	– 1.0	1.0	µA	4
I_{OL}	Output Leakage Current	– 10.0	10.0	µA	5
V_{OH}	Output Logic 1 Voltage ($I_{OUT} = -4.0$mA)	2.4		V	3
V_{OL}	Output Logic 0 Voltage ($I_{OUT} = 8.0$mA)		0.4	V	3

AC ELECTRICAL CHARACTERISTICS (TA = 25°C, f = 1.0MHz)

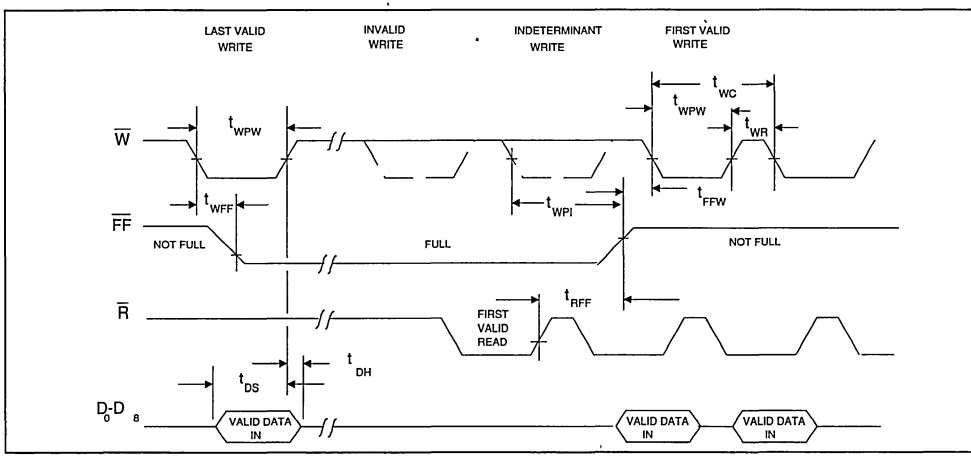
Symbol	Parameter	Typ.	Max.	Unit	Notes
C_I	Capacitance on Input Pins		8	pF	8
C_O	Capacitance on Output Pins		12	pF	8,9

Notes : 8. Sampled : not 100% tested.
9. Output buffer deselected.

WRITE MODE

The MK45H0X initiates a Write Cycle (see Figure 3A) on the falling edge of the Write Enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not asserted. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing Read operations. $\overline{FF}$ is asserted during the last valid write as the MK45H0X becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go high t_{RFF} after completion of a valid READ operation. $\overline{FF}$ will again go low t_{WFF} from the beginning of a subsequent WRITE operation, provided that the second READ has not been completed (see Figure 4A). Writes beginning t_{FFW} after $\overline{FF}$ goes high are valid. Writes beginning after $\overline{FF}$ goes low and more then t_{WPI} before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on the internal flag status.

Figure 3A : Write and Full Flag Timing.



AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = +5.0$volts $\pm 10\%$)

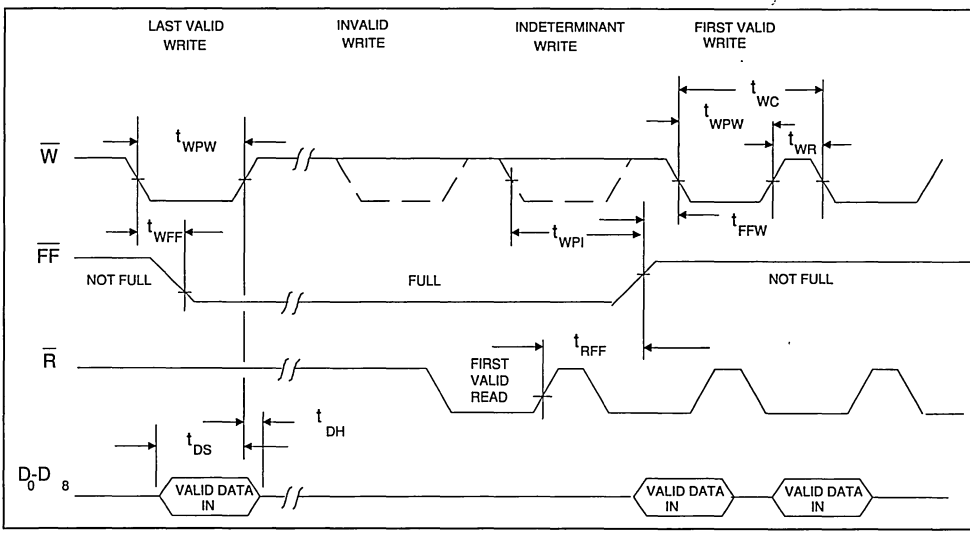
Sym.	Parameter	- 25		- 35		- 50		- 65		- 120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	35		45		65		80		140		ns	
t_{WPW}	Write Pulse Width	25		35		50		65		120		ns	1
t_{WR}	Write Recovery Time	10		10		15		15		20		ns	
t_{DS}	Data Set Up Time	15		18		30		30		40		ns	
t_{DH}	Data Hold Time	0		0		0		0		0		ns	
t_{WFF}	$\overline{W}$ Low to $\overline{FF}$ Low		30		35		45		60		60	ns	2
t_{FFW}	$\overline{FF}$ High to Valid Write		10		10		10		10		10	ns	2
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High		30		35		45		60		60	ns	2
t_{WPI}	Write Protect Indeterminant	10		10		10		10		10		ns	2

READ MODE

The MK45H0X initiates a Read Cycle (see Figure 3B) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not asserted. In the read mode of operation, the MK45H0X provides a very fast access to data from 9 of the locations in the static storage array. The data is accessed on a FIFO basis independent of any ongoing WRITE operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next read operation.

In the event that all the data has been read from the FIFO, the $\overline{EF}$ will go low, and further READ operations will be inhibited (the data outputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid WRITE Operation. $\overline{EF}$ will again go low t_{REF} from the beginning of a subsequent read operation, provided that a second WRITE has not been completed (see Figure 4B). Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more then t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less than t_{EFR} later may or may not occur (be valid) depending on internal flag status.

Figure 3B : Write And Full Flag Timing.



AC ELECTRICAL CHARACTERISTICS ($0°C \le T_A \le +70°C$) ($V_{CC} = +5.0volts \pm 10\%$)

Sym.	Parameter	- 25		- 35		- 50		- 65		- 120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	35		45		65		80		140		ns	
t_A	Access Time		25		35		50		65		120	ns	2
t_{RR}	Read Recovery Time	10		10		15		15		20		ns	
t_{RPW}	Read Pulse Width	25		35		50		65		120		ns	1
t_{RL}	$\overline{R}$ Low to Low Z	0		0		0		0		0		ns	2
t_{DV}	Data Valid from $\overline{R}$ High	5		5		5		5		5		ns	2
t_{RHZ}	$\overline{R}$ High to High Z		18		20		25		25		35	ns	2
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low		60		75		95		115		145	ns	2
t_{EFR}	$\overline{EF}$ High to Valid Read		10		10		10		10		10	ns	2
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High		30		35		45		60		60	ns	2
t_{RPI}	Read Protect Indeterminant	10		10		10		10		10		ns	2

Figure 4A : Read/write To Full Flag.

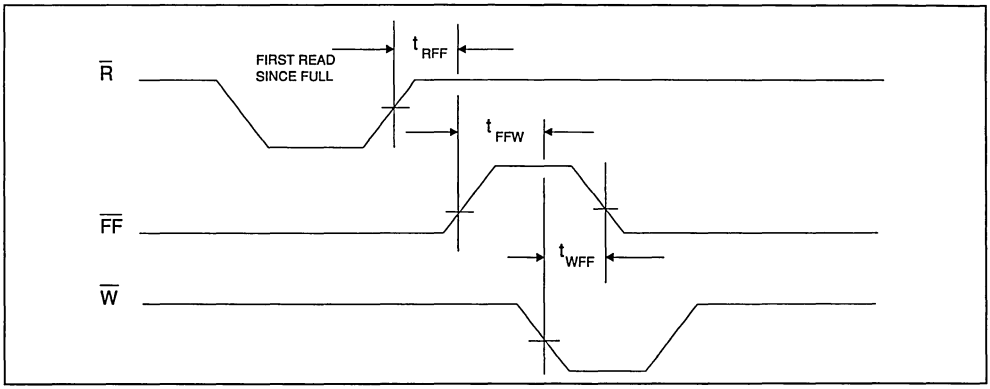
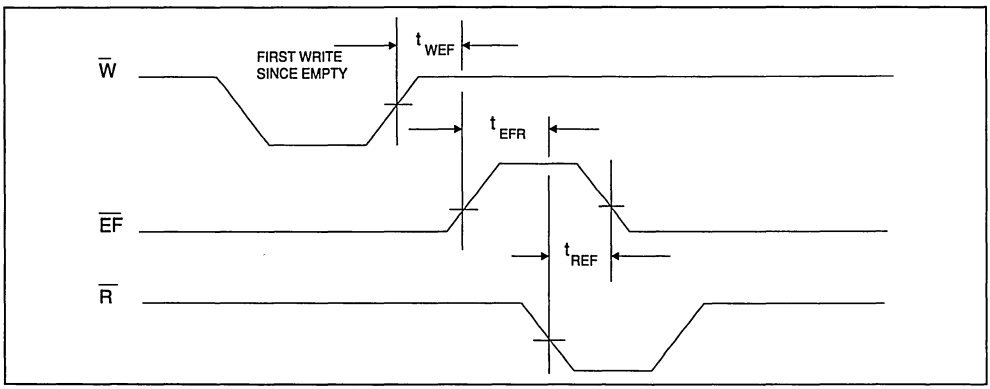


Figure 4B : Write/read To Empty Flag.

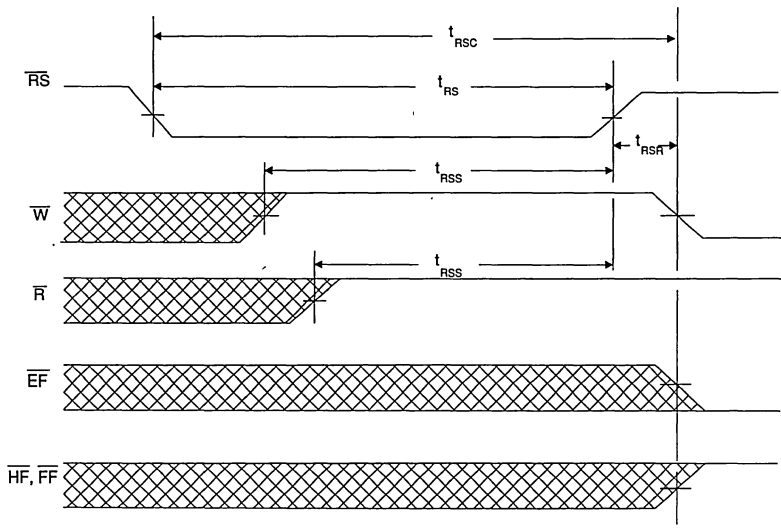


RESET

The MK45H0X is reset (see Figure 5) whenever the Reset pin ($\overline{RS}$) is in the low state. During a reset, both the internal read and write pointers are set to the first location. Reset is required after power up, before a WRITE operation can begin.

Although neither $\overline{W}$ or $\overline{R}$ need to be high when $\overline{RS}$ goes low, both $\overline{R}$ and $\overline{W}$ must be high t_{RSS} before $\overline{RS}$ goes high, and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of $\overline{FL}/\overline{RT}$ and $\overline{XI}$ during Reset.

Figure 5 : Reset.



Note : $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Reset, but flags will be valid at t_{RSC}.

AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = +5.0volts \pm 10\%$)

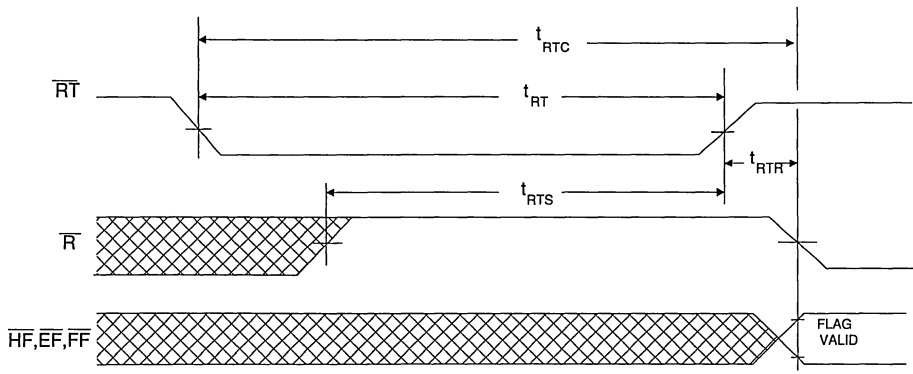
Sym.	Parameter	- 25		- 35		- 50		- 65		- 120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RSC}	Reset Cycle Time	35		45		65		80		140		ns	
t_{RS}	Reset Pulse Width	25		35		50		65		120		ns	1
t_{RSR}	Reset Recovery Time	10		10		15		15		20		ns	
t_{RSS}	Reset Set Up Time	25		30		30		45		100		ns	

RETRANSMIT

The MK45H0X can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low. (see Figure 6). A Retransmit operation sets the internal read pointer to the first location in the array, but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high, and must remain high for t_{RTR} afterwards.

The Retransmit function is particualrly useful when blocks of less than the total FIFO depth are performed between Resets. The Retransmit feature is not compatible with Depth Expansion.

Figure 6 : Retransmit.



Note : $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = +5.0volts \pm 10\%$)

Sym.	Parameter	- 25		- 35		- 50		- 65		- 120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RTC}	Retransmit Cycle Time	35		45		65		80		140		ns	
t_{RT}	Retransmit Pulse Width	25		35		50		65		120		ns	1
t_{RTR}	Retransmit Recovery Time	10		10		15		15		20		ns	
t_{RTS}	Retransmit Setup Time	25		30		30		45		100		ns	

SINGLE DEVICE CONFIGURATION

A single MK45H0X may be used when application requirements are for a depth of the device depth or less. The MK45H0X is placed in the Single Device Configuration mode when the chip is Reset with the Expansion In pin ($\overline{XI}$) grounded (see Figure 7).

WIDTH EXPANSION

Word width may be increased simpy by connecting the corresponding input control signals of multiple devices. Status Flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 8 demonstrates an 18-bit word width by using two MK45H0Xs. Any word width can be attained by adding additional MK45H0Xs. The half full flag ($\overline{HF}$) operates the same as in single device configuration.

HALF FULL FLAG LOGIC

When in single device configuration, the ($\overline{HF}$) output acts as an indication of a half full memory. After half of the memory is filled, and at the falling edge of the next write operation, the half full flag ($\overline{HF}$) will be set low and remain low until the difference between the write pointer and the read pointer is less than or equal to one half the total memory. The half full flag ($\overline{HF}$) is then reset by the rising edge of the read operation. See Figure 9.

Figure 7 : A Single MK45H0X FIFO Configuration.

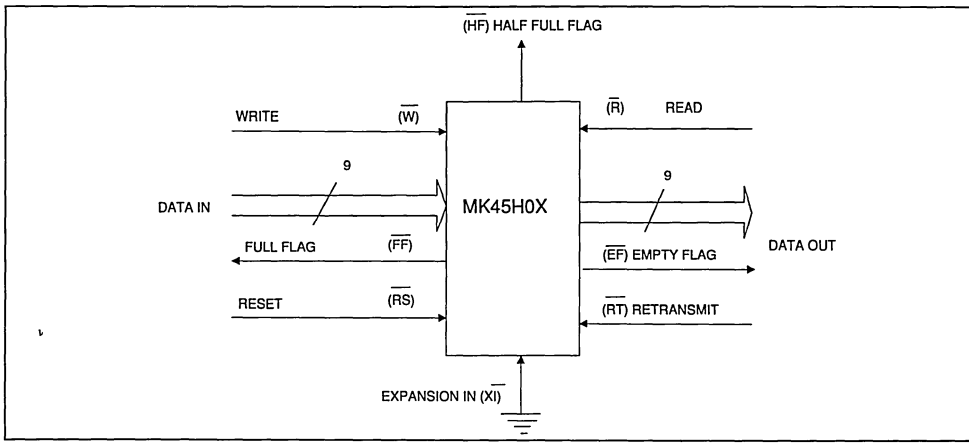
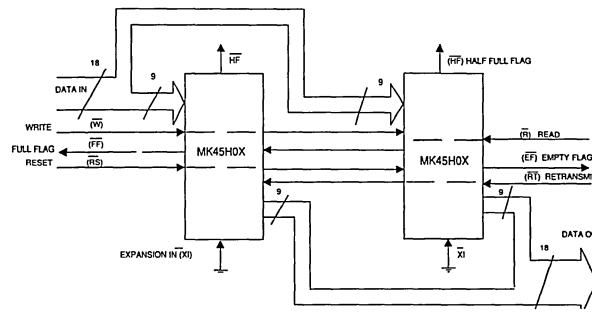


Figure 8 : MK45H0X Width Expansion FIFO Configuration.



Note : Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$ signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

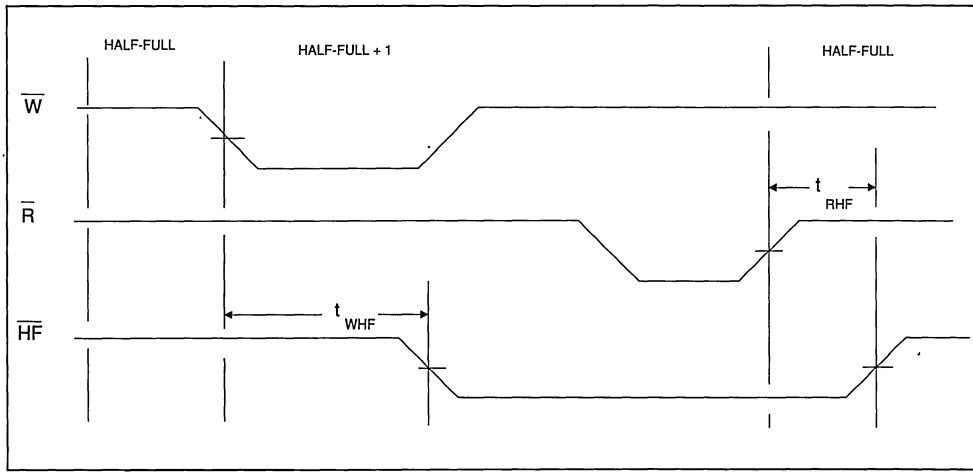
DEPTH EXPANSION (DAISY CHAIN)

The MK45H0X can be easily adapted to applications when the requirements are greater than the individual device word depth. Figure 10 demonstrates Depth Expansion using two MK45H0Xs. Any depth can be attained by adding additional MK45H0Xs.

External logic is needed to generate a composite Full and Empty Flag. This requires the ORing of all the $\overline{EF}$s and the ORing of all the $\overline{FF}$s (i.e., all must be set to generate the composite $\overline{FF}$ or EF).

The MK45H0X operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions:

Figure 9 : Half Full Flag Timing.



AC CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = +5volts \pm 10\%$)

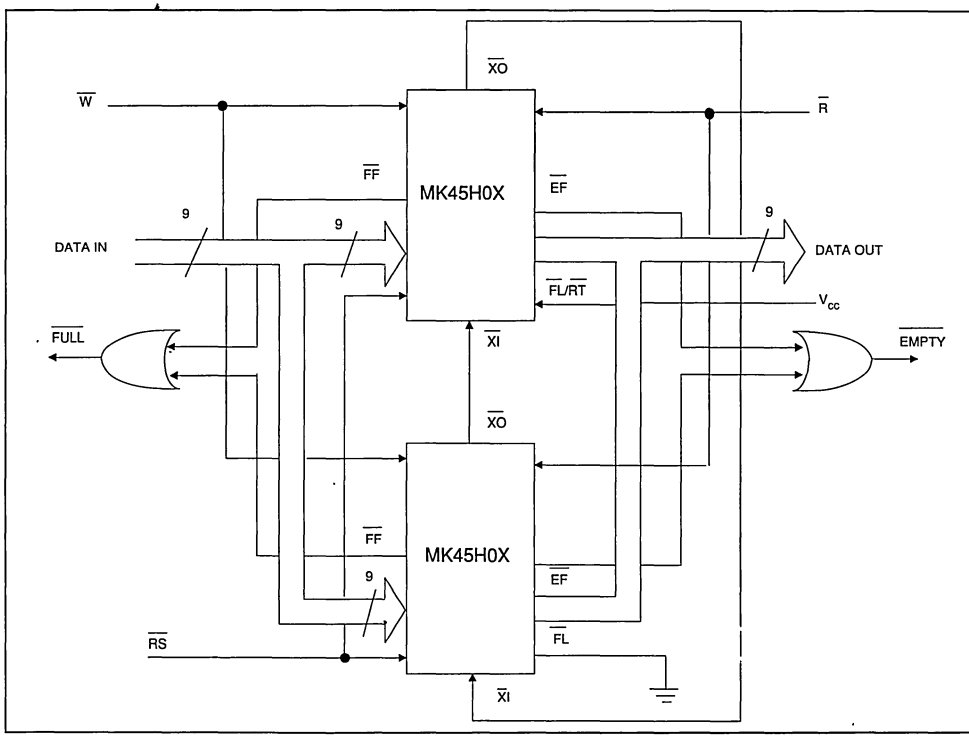
Sym.	Parameter	- 25		- 35		- 50		- 65		- 120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WHF}	Write Low to Half Full Flag Low		30		35		45		60		60	ns	
t_{RHF}	Read High to Half Full Flag High		30		35		45		60		60	ns	

1. The first device must be designated by grounding the First Load pin ($\overline{FL}$). The Retransmit function is not allowed in the Depth Expansion Mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. The Half Full Flag ($\overline{HF}$) is disabled in this mode.

EXPANSION TIMING

Figure 11 and 12 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. In asmuch as Expansion Out pins are generally connected only to Expansion In pins, the user need not be concerned with the actual timing in the normal Depth Expanded application unless extreme propagation delays exist between the $\overline{XO}/\overline{XI}$ pin pairs.

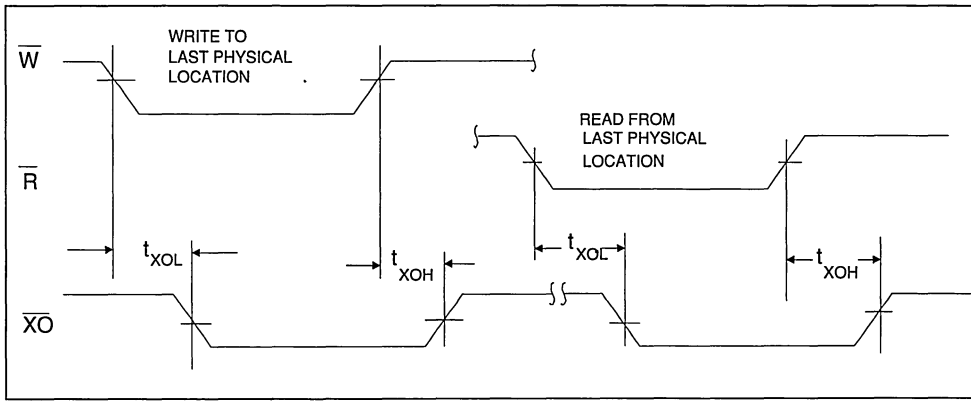
Figure 10 : A two Device Depth Expansion Configuration.



Expansion Out pulses are the image of the WRITE and READ signals that cause them; delayed in time by t_{XOL} and t_{XOH}. The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and Empty Flags are activated, which is in response to writing and reading a last available location.

When in Depth Expansion mode, a given MK45H0X will begin writing and reading as soon as valid WRITE and READ signals begin, provided $\overline{FL}$ was grounded at RESET time.

Figure 11 : Expansion Out timing.



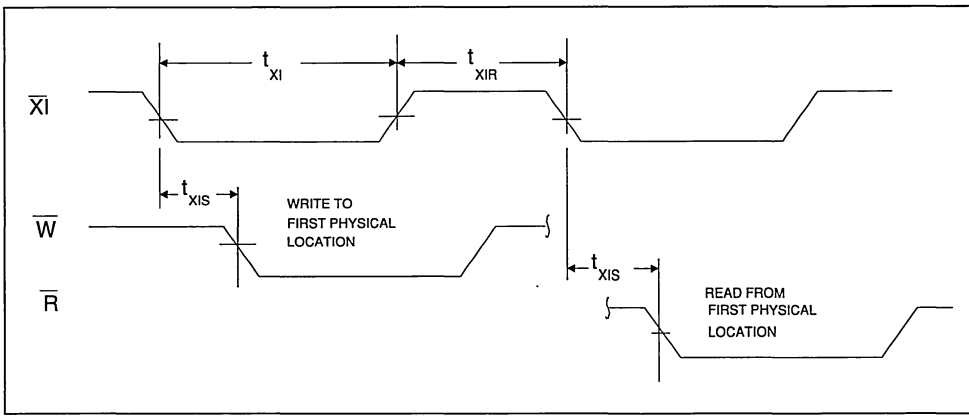
AC ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ + 70°C) (V_{CC} = + 5.0volts ± 10%)

Sym.	Parameter	- 25		- 35		- 50		- 65		- 120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XOL}	Expansion Out Low		25		35		40		55		90	ns	
t_{XOH}	Expansion Out High		25		35		40		55		90	ns	

A MK45H0X in Depth Expansion mode with $\overline{FL}$ high at RESET will not begin writing until after an expansion in pulse occurs.

It will not begin reading until a second Expansion In pulse and the Empth Flag has gone high. Expansion In pulses must occur t_{XIS} before the WRITE and READ signals they are intended to enable. Minimum Expansion In pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

Figure 12 : Expansion In Timing.



AC ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ + 70°C) (V_{CC} = + 5.0volts ± 10%)

Sym.	Parameter	- 25		- 35		- 50		- 65		- 120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XI}	Expansion in Pulse Width	25		35		45		60		115		ns	1
t_{XIR}	Expansion in Recovery Time	10		10		10		10		10		ns	
t_{XIS}	Expansion in Setup Time	15		15		15		15		15		ns	

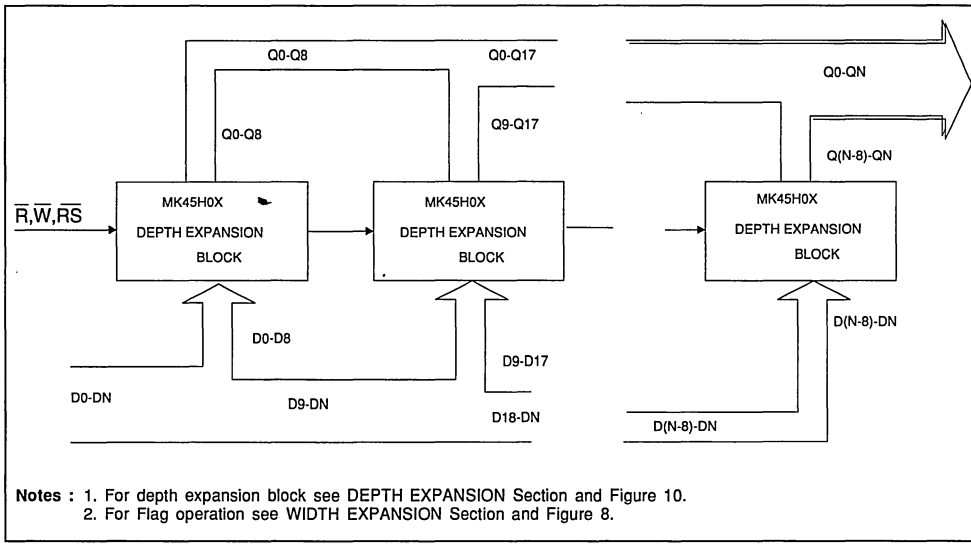
COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 13).

BIDIRECTIONAL APPLICATIONS

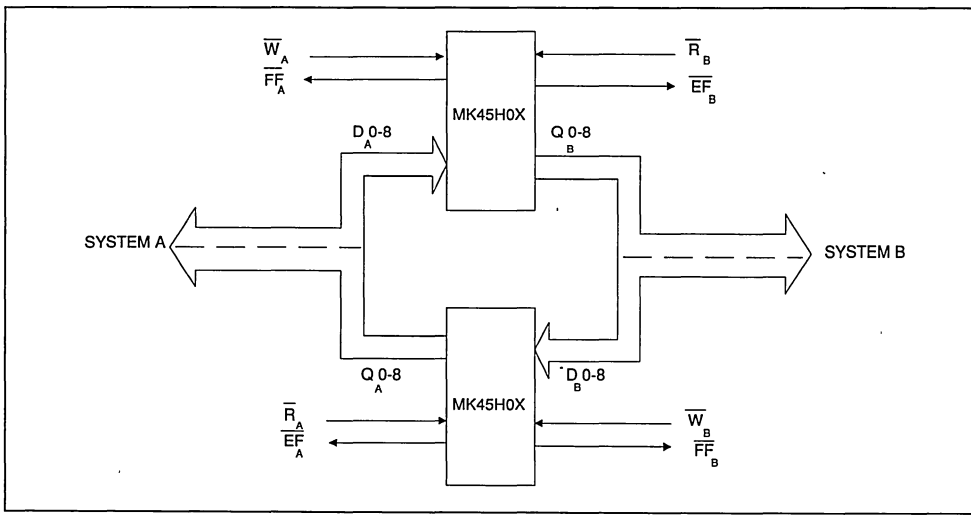
Applications which require data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairng MK45H0Xs as shown in Figure 14. Care must be taken to assure that the appropriate flag is monitored by each system. (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used.) Both Depth Expansion and Width Expansion may be used in this mode.

Figure 13 : Compound Fifo Expansion.



Notes : 1. For depth expansion block see DEPTH EXPANSION Section and Figure 10.
2. For Flag operation see WIDTH EXPANSION Section and Figure 8.

Figure 14 : Bidirectional Fifo Application.



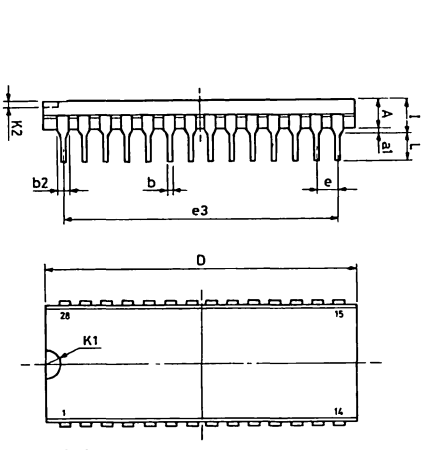
ORDER CODES

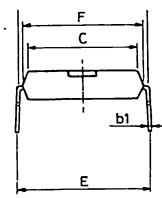
Part No	Access Time	Cycle Time	Package Type	Temperature
MK45H04N25	25ns	35ns	600 MIL Plastic DIP	0° to 70°C
MK45H04N35	35ns	45ns	600 MIL Plastic DIP	0° to 70°C
MK45H04N50	50ns	65ns	600 MIL Plastic DIP	0° to 70°C
MK45H04N65	65ns	80ns	600 MIL Plastic DIP	0° to 70°C
MK45H04N12	120ns	140ns	600 MIL Plastic DIP	0° to 70°C
MK45H14N25	25ns	35ns	600 MIL Plastic DIP	0° to 70°C
MK45H14N35	35ns	45ns	600 MIL Plastic DIP	0° to 70°C
MK45H14N50	50ns	65ns	600 MIL Plastic DIP	0° to 70°C
MK45H14N65	65ns	80ns	600 MIL Plastic DIP	0° to 70°C
MK45H14N12	120ns	140ns	600 MIL Plastic DIP	0° to 70°C
MK45H08N25	25ns	35ns	600 MIL Plastic DIP	0° to 70°C
MK45H08N35	35ns	45ns	600 MIL Plastic DIP	0° to 70°C
MK45H08N50	50ns	65ns	600 MIL Plastic DIP	0° to 70°C
MK45H08N65	65ns	80ns	600 MIL Plastic DIP	0° to 70°C
MK45H08N12	120ns	140ns	600 MIL Plastic DIP	0° to 70°C

Part No	Access Time	R/W Cycle Time
MK45H04/08-25	25ns	35ns, 28.5MHz
MK45H04/08-35	35ns	45ns, 22.2MHz
MK45H04/08-50	55ns	65ns, 15.3MHz
MK45H04/08-65	65ns	80ns, 12.5MHz
MK45H04/08-12	120ns	140ns, 7.14MHz

PACKAGE MECHANICAL DATA

Figure 15 : MK45H04 28 Pin Plastic DIP (N) 600 MIL.





Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A						
a1		0.63			.025	
B		0.45			.018	
b1	0.23		0.31	0.009		.012
b2		1.27			.050	
C						
D			37.34			1 470
E	15.20		16.68	0.598		.657
e		2.54			.100	
e3		33.02			1.300	
e4						
F			14.10			.555
I		4.45			.175	
L		3.30			.130	
K1						
K2						

SGS-THOMSON MICROELECTRONICS

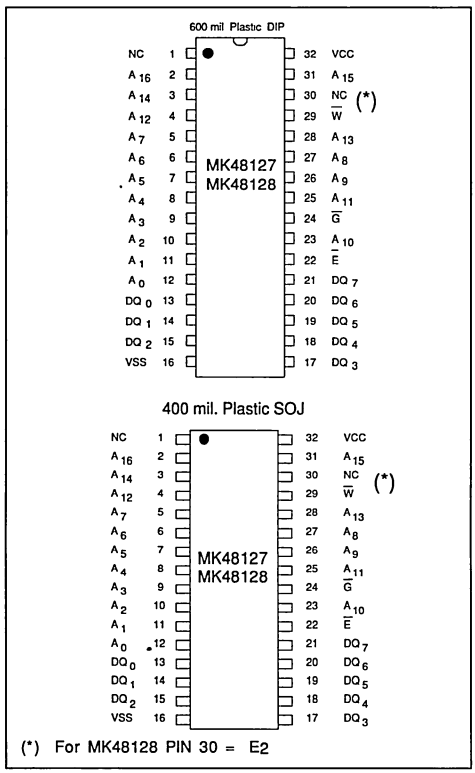
MK48127/128(N,X) -55/70/85

1 MEG (1,048,576-BIT) 128 K X 8 CMOS SRAM

ADVANCE DATA

- BYTEWYDE™ 128K X 8 CMOS SRAM
- EQUAL CYCLE/ACCESS TIMES, 55,70,85NS MAX.
- LOW V_{CC} DATA RETENTION 2 VOLTS
- THREE STATE OUTPUT
- JEDEC STANDARD 32-PIN PACKAGE IN 600 MIL PLASTIC DIP, 400 MIL PLASTIC SOJ

PIN CONNECTION



DESCRIPTION

The MK48127 is a Mega-bit (1,048,576-bit) CMOS SRAM, organized as 131,072 words x 8 bits. It is fabricated using SGS-Thomson's low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single +5V ± 10% supply, and all inputs and outputs are TTL compatible.

PIN NAMES

A_0-A_{16}	Address Inputs
DQ_0-DQ_7	Data I/O_{0-7}
$\overline{E}_1$	Chip Enable 1, Active Low
E_2 (*)	Chip Enable 2, Active High
$\overline{G}$	($\overline{OE}$) Output Enable
$\overline{W}$	Write/read Enable
V_{CC},V_{SS}	+5V, GND
NC	No Connection

NOTES :
(*) For MK48128 ONLY

MK48127/128 THRUTH TABLE

$\overline{W}$	$\overline{E}_1$	E_2(*)	$\overline{G}$	MODE	DQ	POWER
X	H	X	X	Deselect	Hi-Z	Standby
X	X	L	X	Deselect	Hi-Z	Standby
H	L	H	H	Read	Hi-Z	Active
H	L	H	L	Read	Q_{OUT}	Active
L	L	H	X	Write	D_{IN}	Active

NOTES :
(*) For MK48128 ONLY

READ MODE

The MK48127 is in the Read mode whenever Write Enable ($\overline{W}$) is high with Output Enable ($\overline{G}$) low, and Chip Enable ($\overline{E}$) is active low. This provides access to data from eight of 1,048,576 locations in the static memory array, specified by the 17 address inputs. Valid data will be available at the eight Output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is low, and $\overline{E}$ is low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{ELQV}, or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{ELQX}, and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

WRITE MODE

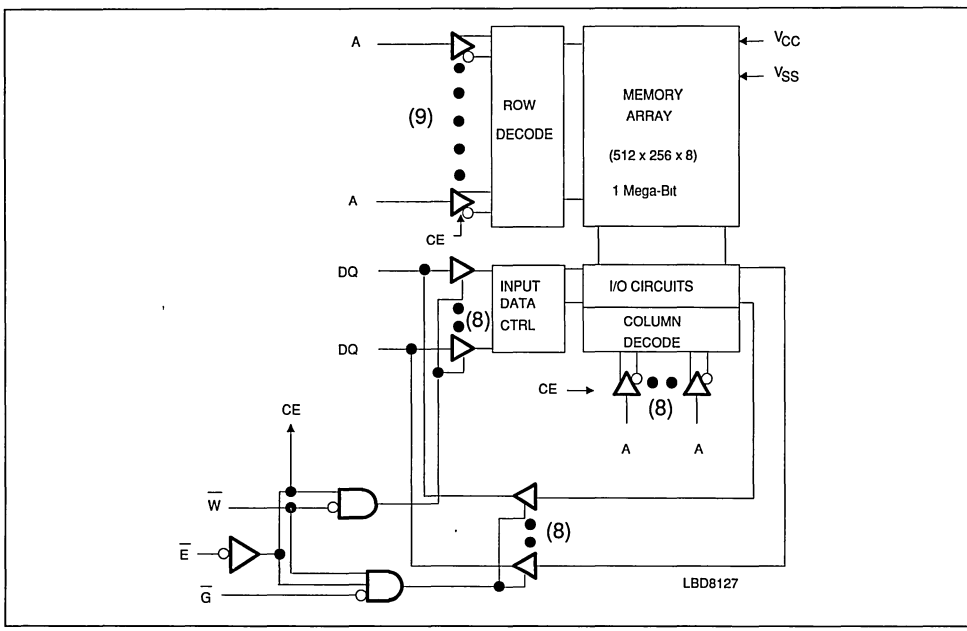
The MK48127 is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ pins are low. Either Chip Enable or $\overline{W}$ must be inactive during Address transitions. The Write begins with the concurrence of Chip Enable being low with $\overline{W}$ low. Therefore, address setup times are referenced to Write Enable and Chip Enable as t_{AVWL}, and t_{AVEL} respectively, and is determined to the latter occuring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{W}$ or Chip Enable ($\overline{E}$).

If the Output is enabled ($\overline{E}$ = low, $\overline{G}$ = low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DVWH} to the rising edge of Write Enable, or to the rising edge of $\overline{E}$, whichever occurs first, and remain valid t_{WHDX}.

OPERATIONAL MODES

The MK48127 has a Chip Enable power down feature which sustains an automatic standby mode whenever Chip Enable ($\overline{E}$) goes inactive high. An Output Enable ($\overline{G}$) pin provides a high speed tristate control, allowing fast read/write cycles to be achieved with the common-I/O data bus. Operational modes are determined by device control inputs $\overline{W}$, $\overline{G}$, and $\overline{E}$, as summarized in the truth table.

MK48127/128 BLOCK DIAGRAM

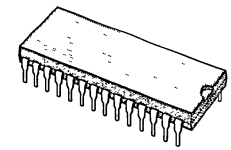


SGS-THOMSON MICROELECTRONICS

MK4832(N)/ MK4832L(N)-70/120

256 K (262, 144-bit) 32 K X 8 CMOS SRAM

- BYTEWYDE™ 32K X 8 CMOS SRAM
- EQUAL CYCLE/ACCESS TIMES, 70, 120NS MAX.
- LOW V_{CC} DATA RETENTION 2 VOLTS
- THREE STATE OUTPUT
- JEDEC STANDARD 28-PIN PACKAGE IN 600 MIL PLASTIC DIP



B
DIP-28
(Plastic Package)

DESCRIPTION

The MK4832 is a 256K (262,144-bit) CMOS SRAM, organized as 32,768 words x 8 bits. It is fabricated using SGS-Thomson's low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single +5V ± 10% supply, and all inputs and outputs are TTL compatible.

OPERATIONAL MODES

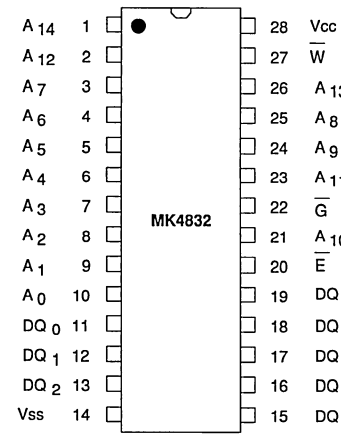
The MK4832 has a Chip Enable power down feature wich sustains an automatic standby mode whenever Chip Enable ($\overline{E}$) goes inactive high. An Output Enable (G) pin provide as high speed tri-state control, allowing fast read/write cycles to be achieved with the common-I/O data bus. Operational modes are determined by device control inputs $\overline{W}$, G and $\overline{E}$, as summurarized in the thruth table.

PIN NAMES

A0-A14	Address Inputs
DQ0-DQ7	Data In/Data Out
E	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write/Read Enable
Vcc	+ 5V
Vss	GROUND

PIN CONNECTIONS

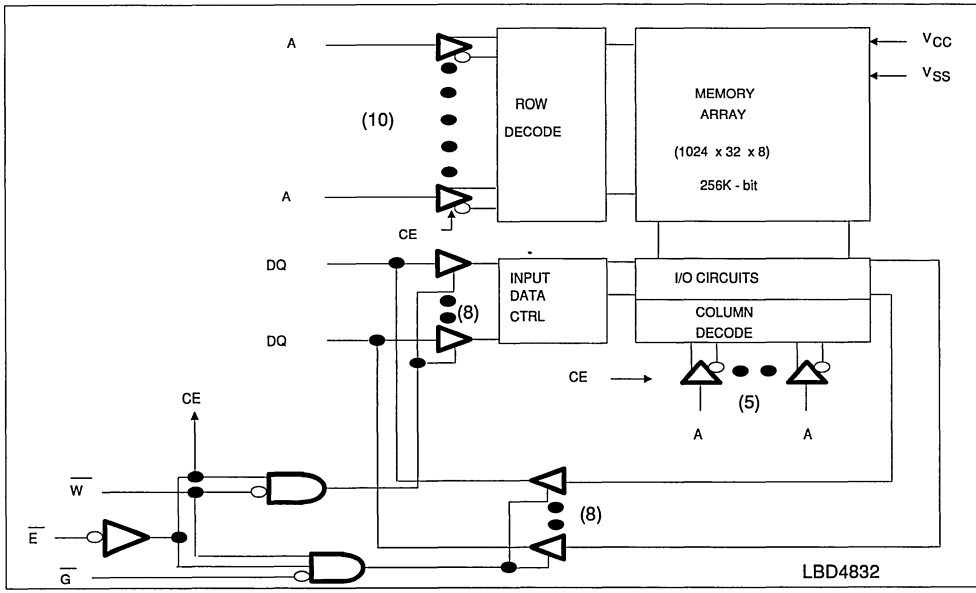
600 mil. Plastic DIP



MK4832 THRUTH TABLE

E	W	G	MODE	DQ	POWER
H	X	X	Deselect	Hi-Z	Standby
L	H	H	Read	Hi-Z	Active
L	H	L	Read	D_{OUT}	Active

FIGURE 1 : MK4832 BLOCK DIAGRAM



READ MODE

The MK4832 is in the Read mode whenever Write Enable (W) is high with Output Enable (G) low, and Chip Enable (E) is active low. This provides access to data from eight of 262,144 locations in the static memory array, specified by the 15 address inputs. Valid data will be available at the eight Output pins within t_{AVQV} after the last stable address, providing G is low, and E is low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{ELQV}, or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{ELQX}, and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

AC ELECTRICAL CHARACTERISTICS (READ CYCLE) (0°C ≤ TA ≤ +70°C, V_{CC} = 5. V ± 10%)

SYMBOL	PARAMETER	4832-70/70L		4832-120/120L		UNIT	NOTE
		MIN	MAX	MIN	MAX		
t_{ELQX}	Chip Enable to Q Low-Z	10		10		ns	5
t_{AXQX}	Output Hold from Address Change	10		10			4
t_{GLQX}	Ouput Enable Access Time	5		5			5
t_{AVAV}	Read Cycle Time	70		120			
t_{AVQV}	Address Access Time		70		120		4
t_{ELQV}	Chip Enable Access Time		70		120		4
t_{GLQV}	Output Enable Access Time		35		60		4
t_{EHQZ}	Chip Enable ($\overline{E}$) to Q High-Z	0	30	0	35		5
t_{GHQZ}	Output Disable ($\overline{G}$)to Q High-Z	0	30	0	35		5

FIGURE 2 : READ TIMING N°.1 (ADDRESS ACCESS)

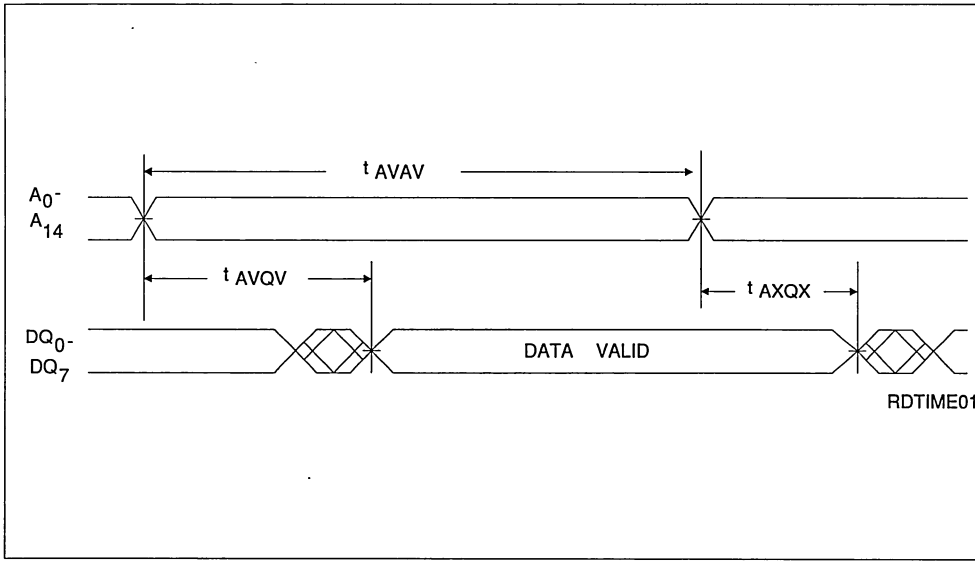
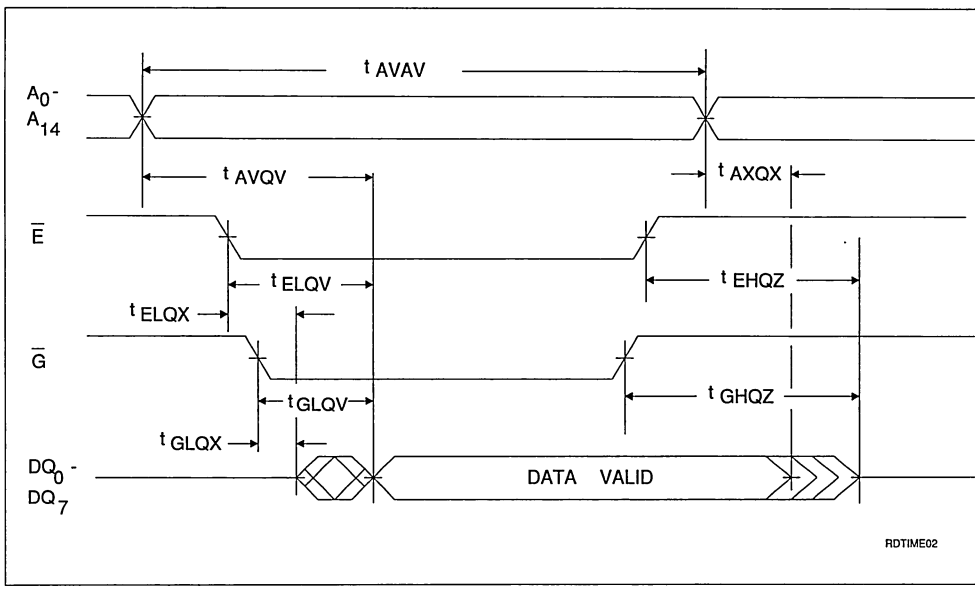


FIGURE 3 : READ TIMING N°.2



WRITE MODE

The MK4832 is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ pins are low. Either Chip Enable or $\overline{W}$ must be inactive during Address transitions. The Write begins with the concurrence of Chip Enable being low with $\overline{W}$ low. Therefore, address setup times are referenced to Write Enable and Chip Enable as t_{AVWL}, and t_{AVEL} respectively, and is determined to the latter occuring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{W}$ or Chip Enable ($\overline{E}$).

If the Output is enabled ($\overline{E}$ = low, $\overline{G}$ = low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DVWH} to the rising edge of Write Enable, or to the rising edge of $\overline{E}$, whichever occurs first, and remain valid t_{WHDX}.

AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE)

SYMBOL	PARAMETER	MK4832-70/70L		MM4832-120/120L		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{AVAV}	Write Cycle Time	70		120		ns	
t_{AVWL}	Address Set-up Time to $\overline{W}$ Low	0		0			
t_{AVEL}	Address Set-up Time to $\overline{E}$ Low	0		0			
t_{AVWH}	address valid to $\overline{W}$ HiGh	60		85			
t_{WLWH}	Write Pulse Width	45		65			
t_{WHAX}	Address Hold After End Of Write	5		5			
t_{ELEH}	Chip Enable Active To End Of Write	60		85			
t_{EHAX}	Address Hold Time From Chip Enable	5		5			
t_{DVWH}	Data Valid To End Of Write	25		45			
t_{WHDX}	Data Hold Time	0		0			
t_{WHQX}	$\overline{W}$ High to Q Active	5		5			5
t_{WLQZ}	$\overline{W}$ Low to Q High-Z	0	40	0	40		5

FIGURE 4 : WRITE CONTROL CYCLE TIMING

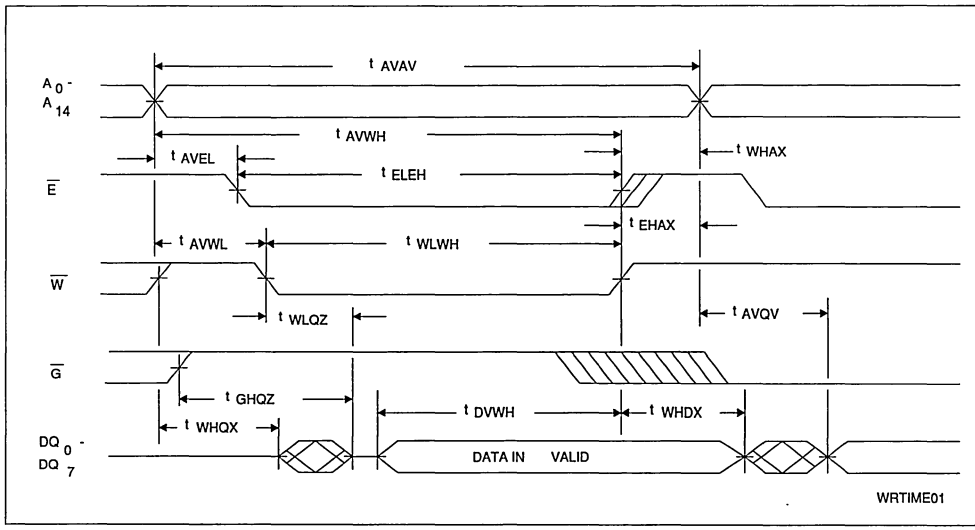
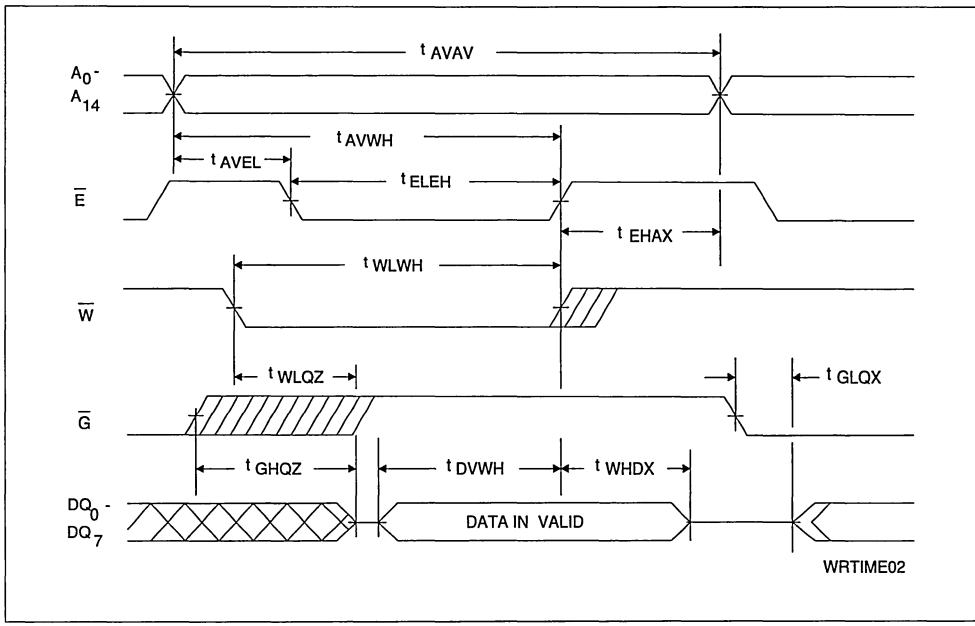


FIGURE 5 : CHIP ENABLE CONTROL WRITE CYCLE TIMING

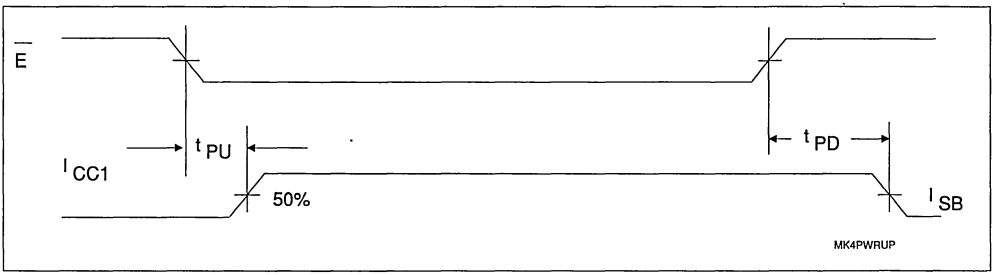


STANDBY MODE CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C, VCC = 5.0V ± 10%)

SYMBOL	PARAMETERS	MK4832/4832L- 70		MK4832/4832L-120		UNITS
		MAX	MIN	MAX	MIN	
t_{PU}	Chip Enable to Power-Up	0		0		ns
t_{PD}	Chip Enable to Power-Down		70		120	ns

FIGURE 6 : STANDBY MODE TIMING

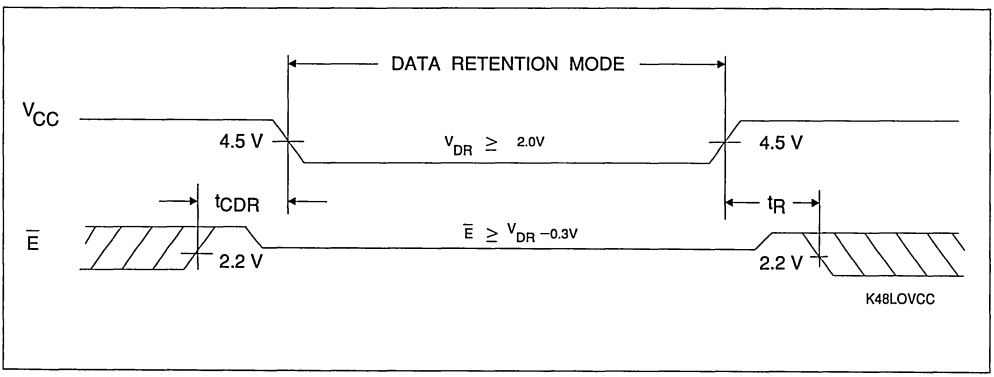


LOW VCC DATA RETENTION CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C, VCC = 5.0 ± 10%)

SYMBOL	PARAMETERS		MAX	MAX	UNIT	NOTE
V_{DR}	V_{CC} Data Retentionmode		2.0		V	9
I_{CCDR}(1)	Data Retention Pwr.supply Current Test Condition: Vcc = 3.0	MK4832		500	µA	9
		MK4832L		20	µA	9
t_{CDR}	Chip Deselect To Data Retention Mode		0		nS	9
t_R	Operation Recovery Time		t_{AVAV} (2)		nS	9

FIGURE 7 : LOW V_{CC} DATA RETENTION



ABSOLUTE MAXIMUM RATINGS *

SYMBOL	PARAMETER	VALUE	UNIT
V_I	Voltage On Any Pin Relative to Ground	-0.5 to +7.0	V
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-65 to 150	°C
P_D	Power Dissipation	1	Watt
I_O	Output Current (1)	50	mA

* This is a stress rating only and functional operation of the device at these or any other conditions above thoseindicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may effact reliability.
(1) Output current absolute maximum rating is specified for one output at atime, not to exceed a duration of 1 second.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq +70°C$)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Vcc	Supply Voltage	4.75	5.0	5.5	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2		Vcc + 0.3v	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3		0.8	V	1

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$)

SYMBOL	PARAMETER		MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current			70	mA	6
I_{SB}	TTL Standby Current ($\overline{E}= V_{IH}$)			3	mA	7
I_{SB1}	CMOS Standby Current ($\overline{E}=$ Vcc -0.2v)	MK4832		1	mA	8
		MK4832L		50	µA	8
I_{LI}	Input Leakage Current (Any Input)		-1	+1	µA	2
I_{LO}	Ouput Leakage Current		-2	+2	µA	2
V_{OH}	Output Logic "1" Voltage (I_{OUT} =-4.0 mA)		2.4		V	1
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +8.0 mA)			0.4	V	1

NOTES :

1. All voltages referenced to GND.
2. Negative spikes of -1.0 volts allowed for up to 10 nS once per Cycle.
3. I_{CC1} measured with outputs open.
4. 1mA typical.
5. Measured with $Vcc \geq V_I \geq$ GND and outputs deselected.

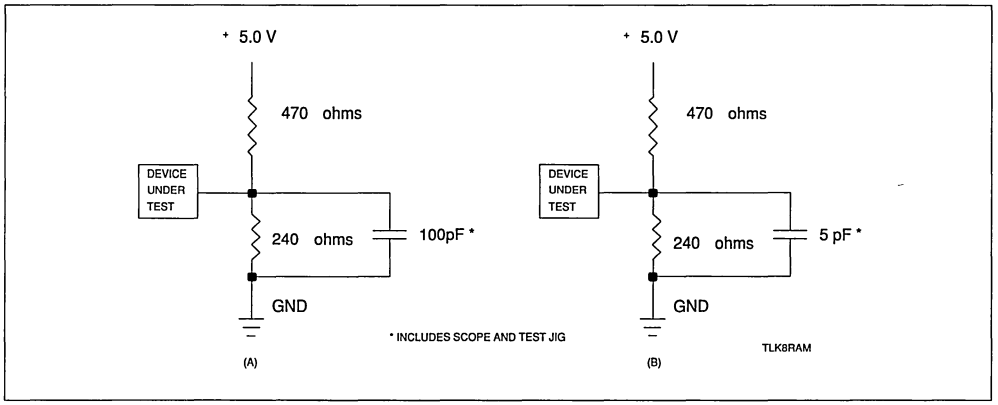
AC TEST CONDITIONS

Inputs Levels. . . . . .0.0v to 3.0v

Transition Time 5ns

Input And Output TimingReference Levels 1.5v

FIGURE 8 : OUPUT LOAD DIAGRAM



CAPACITANCE

(T_A = 25°C, f = 1.0MHz)

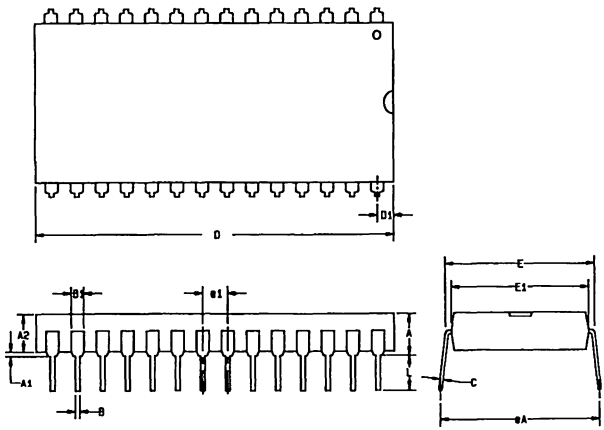
SYMBOL	PARAMETERS	MAX	UNITS	NOTES
CI	capacitance on all pins (except dQ)	8.0	pF	10
CDQ	capacitance on DQ pins	10.0	pF	3,10

ORDERING I NFORMATION

PART NUMBER	ACCESS TIME	PLACKGE TYPE	TEMPERATURE RANGE
MK4832N-70	70ns	28 PIN 600 Mil. Pllastic DIP	0°C to 70°C
MK4832N-120	120ns	28 PIN 600 Mil. Pllastic DIP	0°C to 70°C
MK4832LN-70	70ns	28 PIN 600 Mil. Pllastic DIP	0°C to 70°C
MK4832LN-120	120ns	28 PIN 600 Mil. Pllastic DIP	0°C to 70°C

MK	SGS-THOMSON PREFIX
4832	DEVICE INDENTIFICATION NUMBER
L	LOW POWER
N	PLASTIC PACKAGE
70/120	SPEED GRADE

FIGURE 9 : PACKAGE MECHANICAL DATA



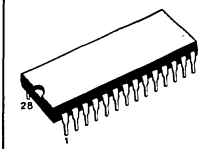
Dim.	mm		Inches		Note
	Min.	Max.	Min.	Max.	
A		5.334		210	2
A1	0.381		.015		2
A2	3.556	4.064	.140	.160	
B	0.381	0.533	.015	.021	3
B1	1.27	1.778	.050	.070	
C	0.203	0.304	.008	.012	3
D	36.57	37.338	1.440	1.470	1
D1	1.651	2.159	.065	.085	
E	15.24	15.875	.600	.625	
E1	13.46	14.224	.530	.560	
e1	2.286	2.794	.090	.110	
eA	15.24	17.78	.600	.700	
L	3.048		.120		

NOTES :

1. Overall length includes 0.10 in flash on either end of the package.
2. Package standoff to be measured per Jedec requirments.
3. The maximum limit shall be increased by .0003 In. when solder laed is specified.

2K × 8 ZEROPOWER™ RAM

- LOW CURRENT (1 μA @ 70°C) BATTERY INPUT FOR DATA RETENTION IN THE ABSENCE OF POWER
- DATA SECURITY PROVIDED BY AUTOMATIC WRITE PROTECTION DURING POWER FAILURE
- +5 VOLT ONLY READ/WRITE
- CONVENTIONAL SRAM WRITE CYCLES
- LOW POWER 440 mW ACTIVE; 5.5 mW STANDBY
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME
- LOW-BATTERY WARNING
- TWO POWER-FAIL DESELECT TRIP POINTS AVAILABLE
  MK48C02A 4.75V ≥ V_{PFD} ≥ 4.50V
  MK48C12A 4.50V ≥ V_{PFD} ≥ 4.20V
- POWER FAIL INTERRUPT OUTPUT

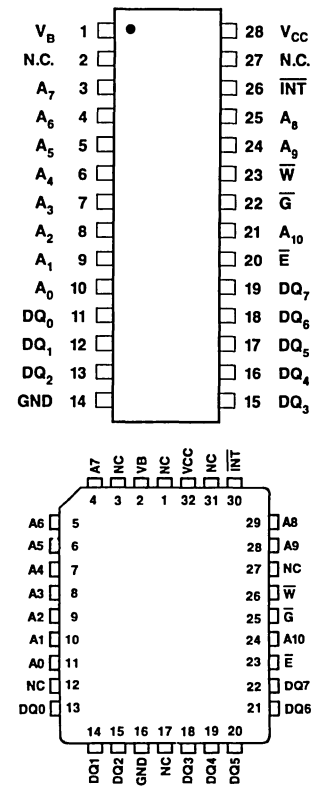


N
DIP-28
(Plastic Package)

K
PLCC32
(Plastic Chip Carrier)

Part Number	Access Time	R/W Cycle Time
MK48CX2A-15	150 ns	150 ns
MK48CX2A-20	200 ns	200 ns
MK48CX2A-25	250 ns	250 ns

FIGURE 1. PIN CONNECTIONS



PIN NAMES

A_0 - A_{10} Address Inputs	V_{CC} System Power (+5 V)
$\overline{E}$ Chip Enable	$\overline{W}$ Write Enable
GND Ground	$\overline{G}$ Output Enable
DQ_0-DQ_7 Data In/Data Out	V_B Battery Input
$\overline{INT}$ Power Fail Interrupt (Open Drain Type)	
NC No Connection	

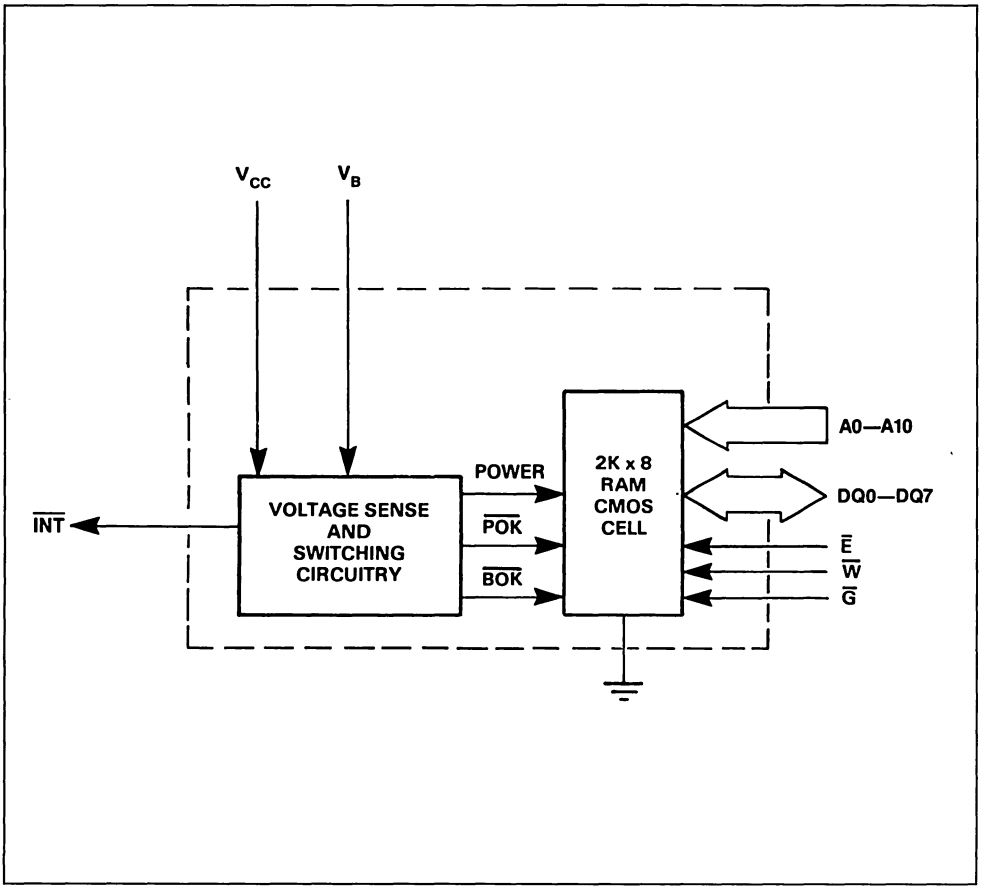
TRUTH TABLE (MK48C02A/12A)

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ
	V_{IH}	X	X	Deselect	High-Z
$<V_{CC}$ (Max)	V_{IL}	X	V_{IL}	Write	D_{IN}
$>V_{CC}$ (Min)	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
	V_{IL}	V_{IH}	V_{IH}	Read	High-Z
$<V_{PFD}$ (Min) $>V_{SO}$	X	X	X	Power-Fail Deselect	High-Z
$\leq V_{SO}$	X	X	X	Battery Back-up	High-Z

DESCRIPTION

The MK48C02A/12A is a CMOS RAM with internal power fail support circuitry for battery backup applications. The fully static RAM uses an HCMOS six transistor cell and is organized 2K x 8. Included in the device is a feature to conserve battery energy and a method of providing data security during V_{CC} transients. A precision voltage detector write-protects the RAM to prevent inadvertent loss of data when V_{CC} falls out of tolerance. In this way, all input and output pins (including $\overline{E}$ and $\overline{W}$) become "don't care". The device permits full functional ability of the RAM for V_{CC} above 4.75V (MK48C02A) and 4.5V (MK48C12A). Data protection is provided for V_{CC} below 4.5V (MK48C02A) and 4.2V (MK48C12A), and maintains data in the absence of V_{CC} with no additional support circuitry other than a primary cell. The current supplied by the battery during data retention is for junction leakage only (typically less than 5na) because all power-consuming circuitry is turned off. The low battery drain allows use of a long life Lithium primary cell.

FIGURE 2. BLOCK DIAGRAM



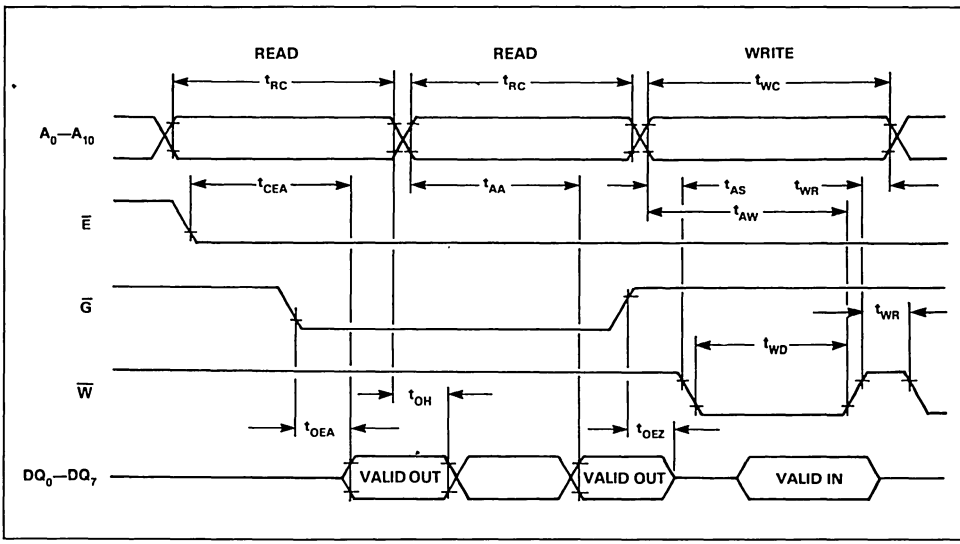
OPERATION

Read Mode

The MK48C02A/12A is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low, providing a ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_n) defines which one of 2,048 bytes of data is to be accessed.

Valid data will be available to the eight data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are satisfied. If $\overline{E}$ or $\overline{G}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}), rather than the address. The state of the eight Data I/O signals is controlled by the $\overline{E}$ and $\overline{G}$ control signals. The data lines may be in an indeterminate state between t_{OH} and t_{AA}, but the data lines will always have valid data at t_{AA}.

FIGURE 3. READ-READ-WRITE TIMING



AC ELECTRICAL CHARACTERISTICS (READ CYCLE TIMING)
($0°C \le T_A \le 70°C$) (V_{CC} (Max) $\ge V_{CC} \ge V_{CC}$ (Min))

		MK48CX2A-15		MK48CX2A-20		MK48CX2A-25			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	150		200		250		ns	
t_{AA}	Address Access Time		150		200		250	ns	1
t_{CEA}	Chip Enable Access Time		150		200		250	ns	1
t_{OEA}	Output Enable Access Time		75		80		90	ns	1
t_{CEZ}	Chip Enable Hi to High-Z		35		40		50	ns	
t_{OEZ}	Output Enable Hi to High-Z		35		40		50	ns	
t_{OH}	Valid Data Out Hold Time	15		15		15		ns	1

NOTE
1. Measured using the Output Load Diagram shown in Figure 7.

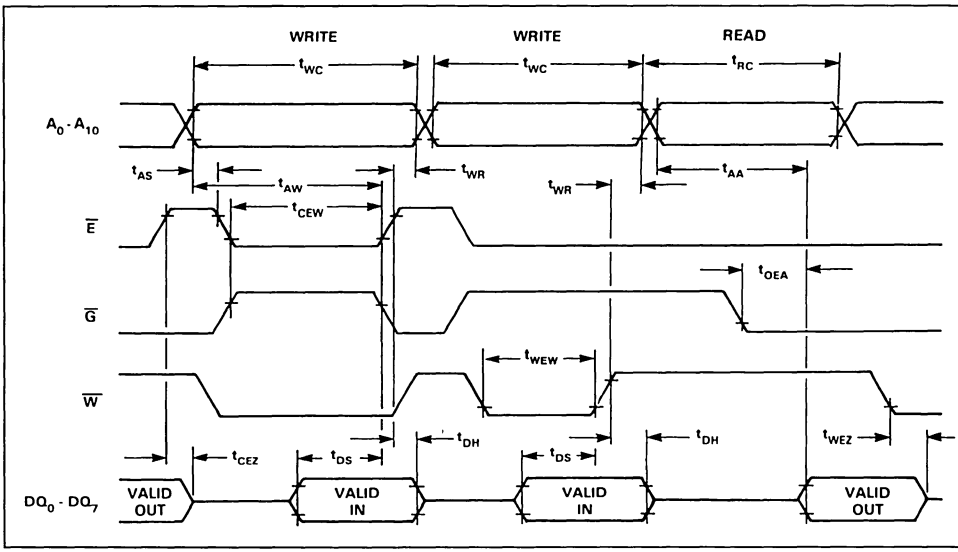
WRITE MODE

The MK48C02A/12A is in Write Mode whenever the $\overline{W}$ and $\overline{E}$ inputs are held low. The start of a Write is referenced to the latter occurring falling edge of either $\overline{W}$ or $\overline{E}$. A Write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{W}$ or $\overline{E}$ must return high, for a minimum of t_{WR} prior to the initiation of another Read or Write Cycle. Data-in must be valid for t_{DS} prior to the End of Write and remain valid for t_{DH} afterward.

Some processors thrash producing spurious Write Cycles during power-up, despite application of a power-on reset. Users should force $\overline{W}$ or $\overline{E}$ high during power-up to protect memory after V_{CC} reaches V_{CC} (min) but before the processor stablizes.

The MK48C02A/12A $\overline{G}$ input is a DON'T CARE in the write mode. $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WEZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

FIGURE 4. WRITE-WRITE-READ TIMING



AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE TIMING)

(0°C ≤ T_A ≤ 70°C) (V_{CC} (Max) ≥ V_{CC} ≥ V_{CC} (Min))

		MK48CX2A-15		MK48CX2A-20		MK48CX2A-25			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	Write Cycle Time	150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AW}	Address Valid to End of Write	120		140		180		ns	
t_{CEW}	Chip Enable to End of Write	90		120		160		ns	
t_{WEW}	Write Enable to End of Write	90		120		160		ns	
t_{WR}	Write Recovery Time	10		10		10		ns	
t_{DS}	Data Setup Time	40		60		100		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WEZ}	Write Enable Low to High-Z		50		60		80	ns	

DATA RETENTION MODE

With V_{CC} applied, the MK48C02A/12A operates as a conventional BYTEWIDE static ram. However, V_{CC} is being constantly monitored. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. The MK48C02A has a V_{PFD} (max) -V_{PFD} (min) window of 4.75 volts to 4.5 volts, providing very high data security, particularly when all of the other system components are specified to 5.0 volts plus and minus 10%. The MK48C12A has a V_{PFD} (max) -V_{PFD} (min) window of 4.5 volts to 4.2 volts, allowing users constrained to a 10% power supply specification to use the device.

Note: A mid-write cycle power failure may corrupt data at the current address location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time does not exceed t_F. The MK48C02A/12A may respond to transient noise spikes that reach into the deselect window if they should occur during the time the device is sampling V_{CC}. Therefore decoupling of power supply lines is recommended.

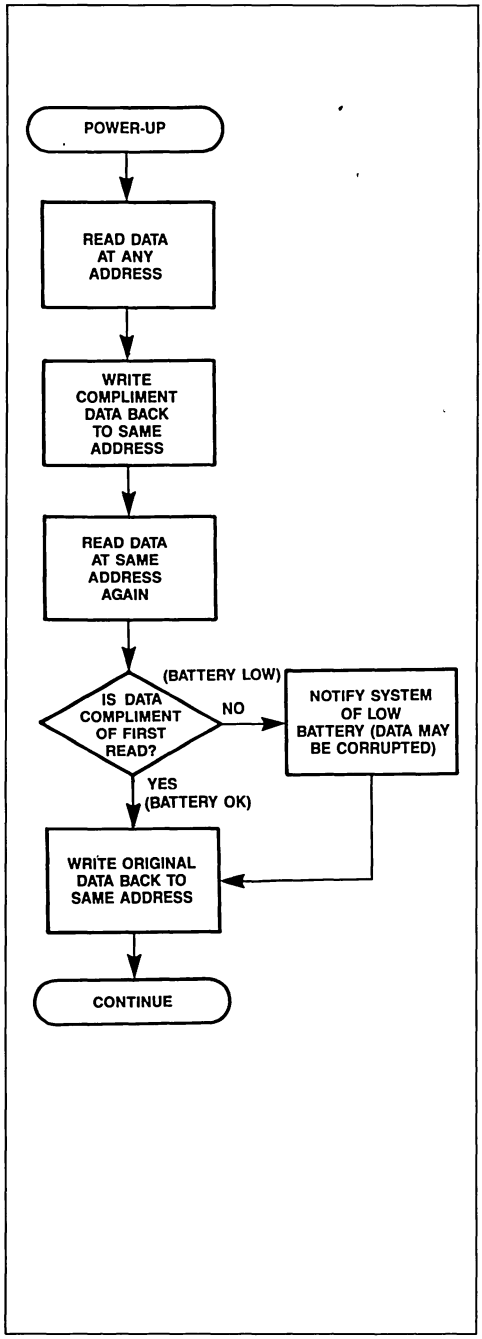
The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{BOK}$) flag will be set. The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after first write, and normal RAM operation resumes. Figure 5 illustrates how a $\overline{BOK}$ check routine could be structured.

Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD} (Max). Caution should be taken to keep $\overline{E}$ or $\overline{W}$ high as V_{CC} rises past V_{PFD} (Min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

INTERRUPT FUNCTION

The MK48C02A/12A provides a power-fail interrupt output labeled $\overline{INT}$. The $\overline{INT}$ pin eliminates the need for external power sensing components in applications where an orderly shut down of the system is necessary. The $\overline{INT}$ pin is open drain for "wire or" applications and provides the user with 10 μs to 40 μs advanced warning of an impending power-fail write protect.

FIGURE 5. CHECKING THE $\overline{BOK}$ FLAG STATUS



AC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TIMING)
(0°C≤T_A≤+70°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_F	V_{PFD} (Max) to V_{PFD} (Min) V_{CC} Fall Time	300		μs	2
t_{FB}	V_{PFD} (Min) to V_{SO} V_{CC} Fall Time	10		μs	3
t_{RB}	V_{SO} to V_{PFD} (Min) V_{CC} Rise Time	1		μs	
t_R	V_{PFD} (Min) to V_{PFD} (Max) V_{CC} Rise Time	0		μs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after V_{PFD} (max)	120		μs	
t_{PFX}	$\overline{INT}$ Low to Auto Deselect	10	40	μs	
t_{PFH}	V_{PFD} (Max) to $\overline{INT}$ High		120	μs	4
t_{FB}	V_{PFD} (Min) to V_{SO}	10		μs	

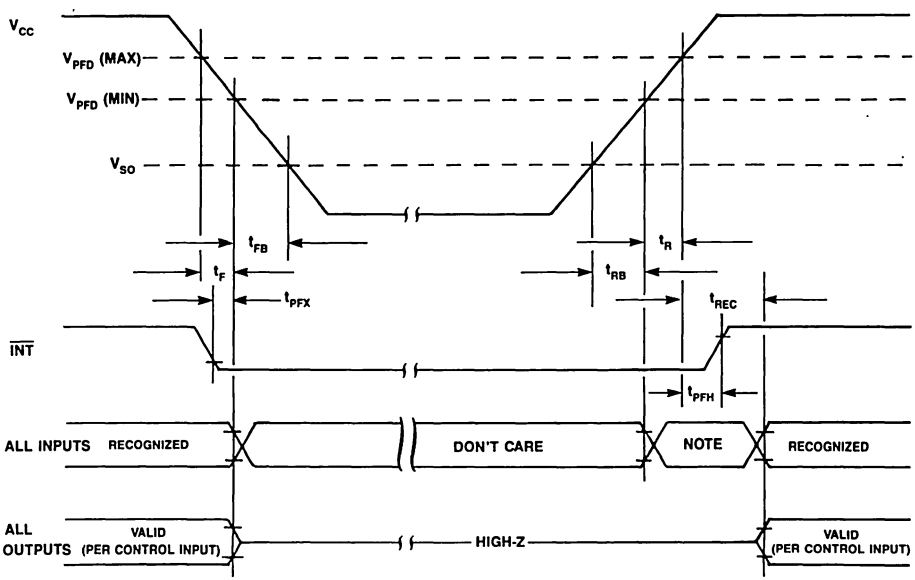
DC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TRIP POINT VOLTAGES)
(0°C≤T_A≤+70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{PFD}	Power-fail Deselect Voltage (MK48C02A)	4.50	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MK48C12A)	4.20	4.3	4.50	V	1
V_{SO}	Battery Back-up Switchover Voltage		3		V	1

NOTES:
1. All voltages referenced to GND.
2. V_{PFD} (Max) to V_{PFD} (Min) fall times of less t_F may result in deselection/write protection not occurring until 40 μs after V_{CC} passes V_{PFD} (Min). V_{PFD} (Max) to (Min) fall times of less than 10 μs may cause corruption of RAM data.
3. V_{PFD} (Min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data.
4. INT may go high anytime after V_{CC} exceeds V_{PFD} (min) and is guaranteed to go high t_{PFH} after V_{CC} exceeds V_{PFD} (max).

CAUTION
Negative Undershoots Below −0.3 volts are not allowed on any pin while in Battery Back-up mode.

FIGURE 6. POWER DOWN/POWER-UP TIMING



NOTE:
Inputs may or may not be recognized at this time.
Caution should be taken to keep $\overline{E}$ or $\overline{W}$ in the high state V_{CC} rises past V_{PFD} (min). Some systems may perform inadvertant write cycles after V_{CC} rises but before normal system operation begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Pin Relative To GND ..... −0.3 V to +7.0 V
Ambient Operating (V_{CC} On) Temperature (T_A) ..... 0°C to +70°C
Ambient Storage (V_{CC} Off) Temperature ..... −55°C to +125°C
Total Device Power Dissipation ..... 1 Watt
Output Current Per Pin ..... 20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

CAUTION: Under no conditions can the "Absolute Maximum Rating" for the voltage on any pin be exceeded since it will cause permanent damage. Specifically, do not perform the "standard" continuity test on any input or output pin, i.e do not force these pins below −0.3 V DC.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage (MK48C02A)	4.75	5.50	V	1
V_{CC}	Supply Voltage (MK48C12A)	4.50	5.50	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3 V	V	1
V_{IL}	Logic "0" Voltage All Inputs	−0.3	0.8	V	1,2
V_B	Battery Voltage	1.8	4.0	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C) (V_{CC} (max) ≥ V_{CC} ≥ V_{CC} (min))

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	3
I_{CC2}	TTL Standby Current ($\overline{E}$ = V_{IH})		3	mA	
I_{CC3}	CMOS Standby Current ($\overline{E}$ ≥ V_{CC} −0.2 V)		1	mA	
I_{IL}	Input Leakage Current (Any Input)	−1	+1	µA	4
I_{OL}	Output Leakage Current	−5	+5	µA	4
V_{OH}	Output Logic "1" Voltage (I_{OUT} = −1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 2.1 mA)		0.4	V	
V_{PFL}	INT Logic "0" Voltage (I_{OUT} = 0.5 mA)		0.4	V	
I_{BATT}	Battery Backup Current V_B = 4.0 V		1	µA	
I_{CHG}	Battery Charging Current V_{CC} = 5.5 V	−5	+5	nA	
V_{LB}	Battery OK Flag	1.8	2.6	V	

CAPACITANCE (T_A = 25°C)

SYM	PARAMETER	MAX	NOTES
C_I	Capacitance on all pins (except D/Q)	7 pF	5
$C_{D/Q}$	Capacitance on D/Q pins and $\overline{INT}$	10 pF	4,5

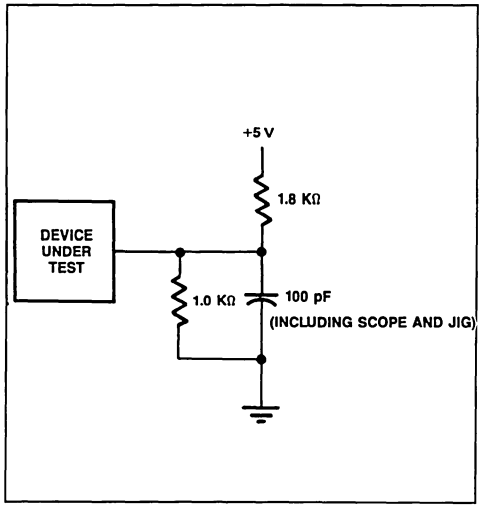
NOTES

1. All voltages referenced to GND.
2. Negative spikes of −1.0 volts allowed for up to 10 ns once per cycle.
3. I_{CC1} measured with outputs open.
4. Measured with GND ≤ V_I ≤ V_{CC} and outputs deselected.
5. Effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3 volts and power supply at nominal level.

AC TEST CONDITIONS

Input Levels:	0.6 V to 2.4 V
Transition Times:	5 ns
Input and Output Timing Reference Levels	0.8 V or 2.2 V
Ambient Temperature	0°C to 70°C
V_{CC} (MK48C02A)	4.75 V to 5.5 V
V_{CC} (MK48C12A)	4.5 V to 5.5 V

FIGURE 7. OUTPUT LOAD DIAGRAM



ORDERING INFORMATION

MK48C X 2A X -XX

DEVICE FAMILY

V_{CC} RANGE

PACKAGE

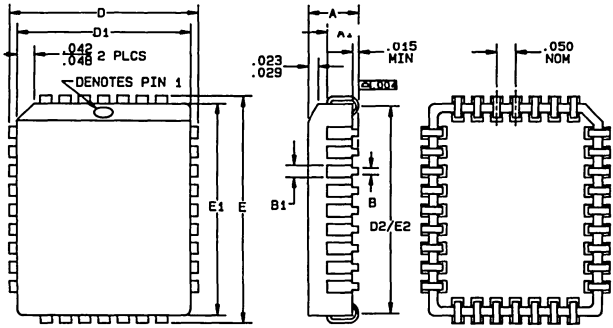
SPEED

-15 150 NS ACCESS TIME
-20 200 NS ACCESS TIME
-25 250 NS ACCESS TIME

K 32 PIN PLCC
N 28 PIN DIP

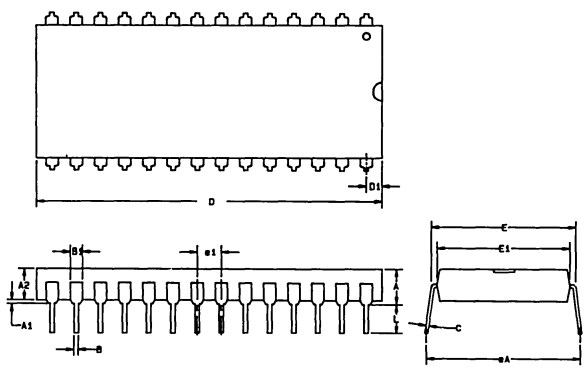
0 +10%/−5%
1 +10%/−10%

FIGURE 8. MK48C02A/12A PLASTIC LEADED CHIP CARRIER, 32 PIN (K TYPE)



Dim.	mm		inches	
	Min	Max	Min	Max
A	3.048	3.556	.120	.140
A1	1.981	2.413	.078	.095
B	0.330	0.533	.013	.021
B1	0.660	0.812	.026	.032
D	12.319	12.573	.485	.495
D1	11.353	11.506	.447	.453
D2	9.906	10.922	.390	.430
E	14.859	15.113	.585	.595
E1	13.893	14.046	.547	.553
E2	12.446	13.462	.490	.530

FIGURE 9. MK48C02A/12A PLASTIC (N TYPE) DUAL-IN-LINE, 28 PINS



NOTES

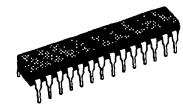
1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

Dim.	mm		inches		Notes
	Min	Max	Min	Max	
A	—	5.334	—	.210	2
A1	0.381	—	.015	—	2
A2	3.556	4.064	.140	.160	
B	0.381	0.533	.015	.021	3
B1	1.27	1.778	.050	.070	
C	0.203	0.304	.008	.012	3
D	36.576	37.338	1.440	1.470	1
D1	1.651	2.159	.065	.085	
E	15.24	15.875	.600	.625	
E1	13.462	14.224	.530	.560	
e1	2.286	2.794	.090	.110	
eA	15.24	17.78	.600	.700	
L	3.048	—	.120	—	

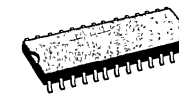
MK48H64(N,S)70/120
MK48H64L(N,S)70/120

64K (8K x 8-BIT) CMOS FAST STATIC RAM

- 70 AND 120ns ADDRESS ACCESS TIME
- EQUAL ACCESS AND CYCLE TIMES
- STATIC OPERATION - NO CLOCKS OR TIMING STROBES REQUIRED
- LOW V_{CC} DATA RETENTION 2 VOLTS
- ALL INPUTS AND OUTPUTS ARE CMOS AND TTL COMPATIBLE
- LOW POWER OPERATION, 10µA CMOS STAND-BY CURRENT UTILIZING FULL CMOS 6-T CELL
- THREE STATE OUTPUT
- STANDARD 28-PIN PACKAGE IN 600 MIL PLASTIC DIP OR 330 MIL SOIC PACKAGE

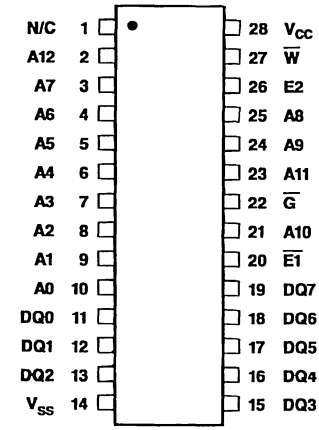


N
DIP-28
(Plastic Package)



S
SOIC-28
(Surface Mount)

Figure 1 : Pin Connections.



DESCRIPTION

The MK48H64 is 65,536-bit organized as 8K x 8 bits. It is fabricated using SGS-THOMSON's low power, high performance, CMOS technology. The device feature fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. They require a single + 5V ± 10% supply, and are fully TTL compatible.

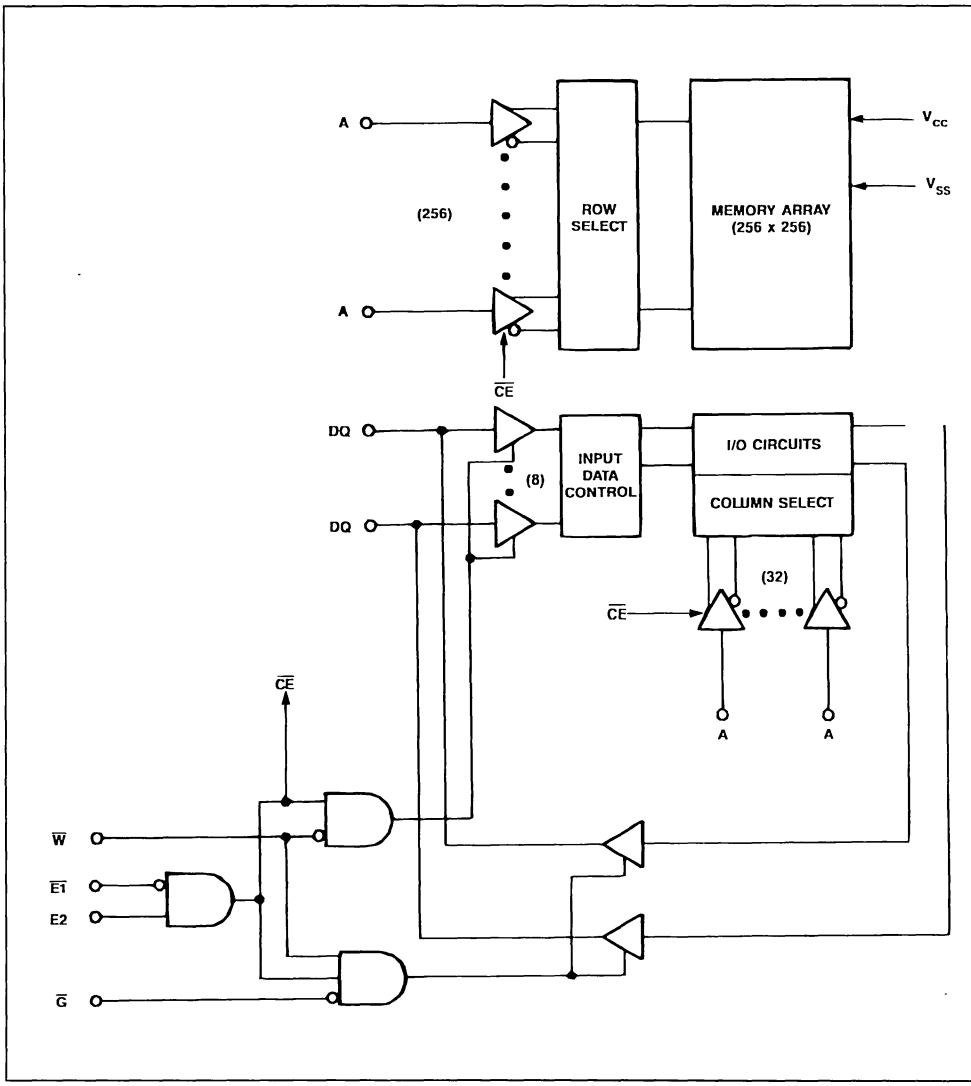
The MK48H64 have a Chip Enable power down feature which sustains an automatic standby mode whenever either Chip Enable goes inactive ($\overline{E1}$ goes high or E2 goes low). An Output Enable ($\overline{G}$) pin provides a high speed tristate control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs $\overline{W}$, $\overline{G}$, $\overline{E1}$, and E2, as summarized in the truth table.

The MK48H64 is available in a 600 Mil Plastic DIP, or a 330 Mil SOIC Package.

PIN NAMES

A_0 - A_{12}	Address Inputs
DQ_0 - DQ_7	Data Input/Output
$\overline{E1}$, E2	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
V_{CC}	+ 5V
V_{SS}	Ground
N/C	No Connection

Figure 2 : Block Diagram.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to GND	– 1.0 to + 7.0	V
T_A	Ambient Operating Temperature	0 to + 70	°C
T_{stg}	Storage Temperature	– 55 to + 125	°C
P_D	Power Dissipation	1	W
I_O	Output Current per Pin	50	mA

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

TRUTH TABLE

$\overline{W}$	$\overline{E1}$	E2	$\overline{G}$	Mode	DQ	Power
X	H	X	X	Deselect	High-Z	Standby
X	X	L	X	Deselect	High-Z	Standby
H	L	H	H	Read	High-Z	Active
H	L	H	L	Read	Q_{OUT}	Active
L	L	H	X	Write	D_{IN}	Active

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	4
GND	Supply Voltage	0	0	0	V	
V_{IH}	Logic 1 Voltage, All Inputs	2.2		V_{CC} + 0.3	V	4
V_{IL}	Logic 0 Voltage, All Inputs	- 0.3		0.8	V	4

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10$ percent)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
I_{CC1}	Average Power Supply Current -120 f = min Cycle -70			90 100	mA	5
I_{SB1}	TTL Standby Current			5	mA	6
I_{SB2}	CMOS Standby Current, MK48H64			1	mA	7
I_{SB2}	CMOS Standby Current, MK48H64L			50	µA	7
I_{IL}	Input Leakage Current (any input pin)	- 1		+ 1	µA	8
I_{OL}	Output Leakage Current (any output pin)	- 10		+ 10	µA	9
V_{OH}	Output Logic 1 Voltage (I_{OUT} = – 4mA)	2.4			V	4
V_{OL}	Output Logic 0 Voltage (I_{OUT} = + 8mA)			0.4	V	4

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

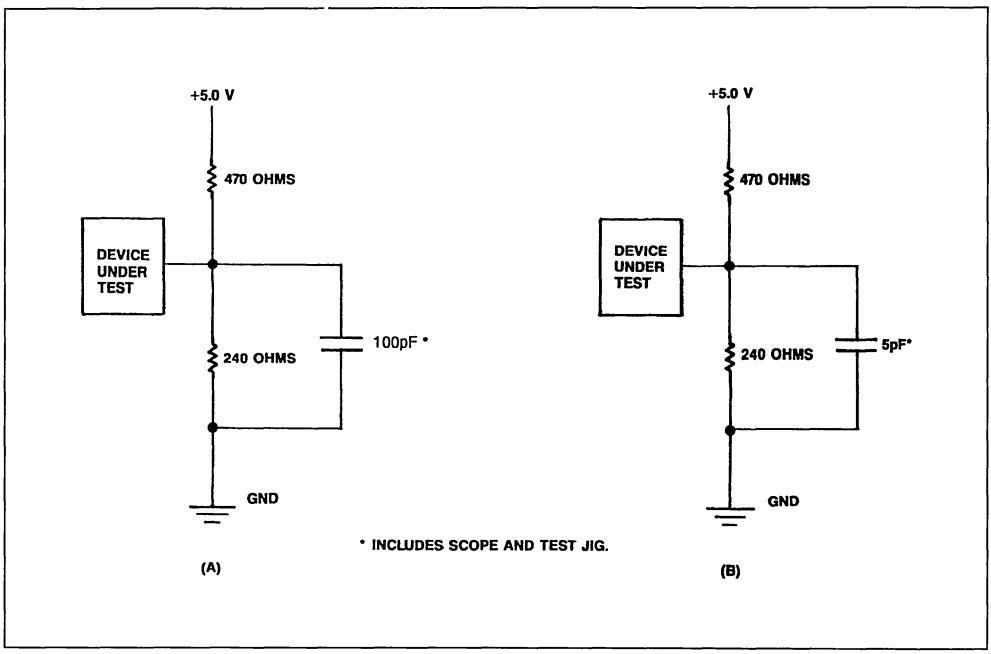
Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
C_1	Capacitance on Input Pins		4	5	pF	10
C_2	Capacitance on DQ Pins		8	10	pF	10

Notes :
1. Measured with load shown in Figure 8(A).
2. Measured with load shown in Figure 8(B).
3. V_{CC} = 3.0V.
4. All voltages referenced to GND.
5. I_{CC1} is measured as the average AC current with V_{CC} = V_{CC} (max) and with the outputs open circuit. t_{AVAV} = t_{AVAV} (min) duty cycle 100%.
6. $\overline{E1}$ = V_{IH}, all other Inputs = Don't Care.
7. V_{CC} (max), and E2 ≤ V_{SS} + 0.3V, all other Inputs = Don't Care.
8. Input leakage current specifications are valid for all V_{IN} such that 0V < V_{IN} < V_{CC}. Measured at V_{CC} = V_{CC} (max).
9. Output leakage current specifications are valid for all V_{OUT} such that 0V < V_{OUT} < V_{CC}, $\overline{E1}$ = V_{IH} or E2 = V_{IL}, and V_{CC} in valid operating range.
10. Capacitances are sampled and not 100% tested.

AC TEST CONDITIONS

Input Levels ..... GND to 3.0V
Transition Times 5ns
Input and Output Signal Timing Reference Level 1.5V
Ambient Temperature ..... 0°C to 70°C
V_{CC} ..... 5.0V ± 10%

Figure 3 : Output Load Circuits.



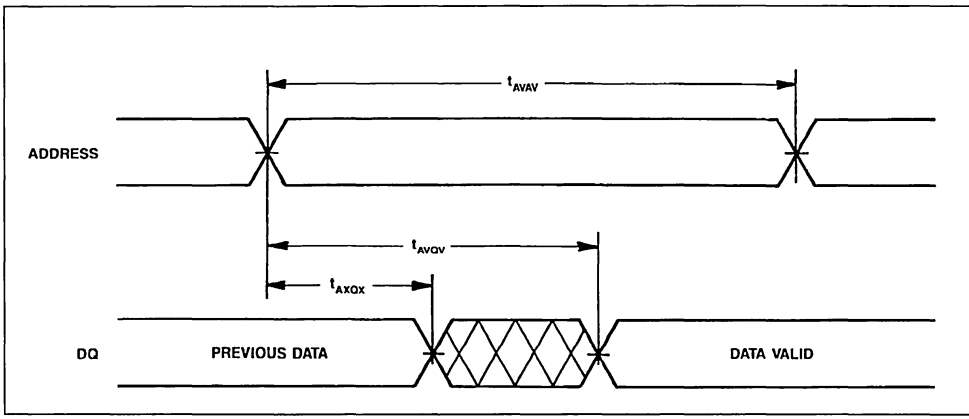
OPERATIONS

READ MODE

The MK48H64 is in the Read mode whenever Write Enable ($\overline{W}$) is high with Output Enable ($\overline{G}$) low, and both Chip Enables (E1 and E2) are active. This provides access to data from eight of 65,536 locations in the static memory array. The unique address specified by the 13 Address Inputs defines which one of the 8192 8-bit bytes is to be accessed.

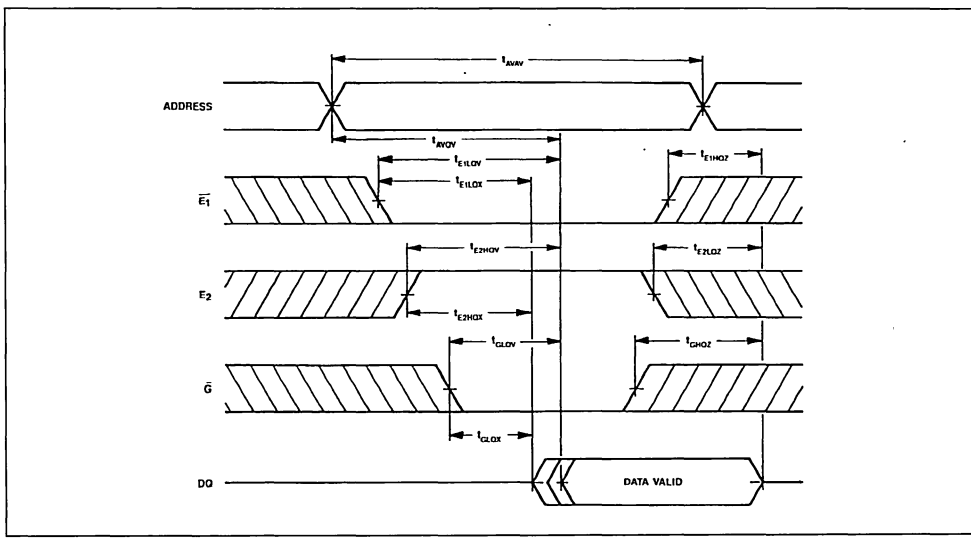
Valid data will be available at the eight Output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is low, E1 is low, and E2 is high. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{E1LQV}, t_{E2HQV}, or t_{GLQV}) rather than the address. The state of the DQ pins is controlled by the $\overline{E1}$, E2, $\overline{G}$, and $\overline{W}$ control signals. Data out may be indeterminate at t_{E1LQX}, t_{E2HQX}, and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

Figure 4 : Read Timing N°1 (Address Access).



Note : Chip Enable and Output Enable are presumed valid.

Figure 5 : Read Timing N° 2 ($\overline{W}$ = V_{IH}).



READ CYCLE TIMING

Symbol		Parameter	48H64-70 48H64L-70		48H64-120 48H64L-120		Unit	Notes
ALT.	STD.		Min.	Max.	Min.	Max.		
t_{RC}	t_{AVAV}	Read Cycle Time	70		120		ns	
t_{AA}	t_{AVQV}	Address Access Time		70		120	ns	1
t_{CEA} 1 & 2	t_{E1LQV} t_{E2HQV}	Chip Enable 1 & 2 Access Time		70 70		120 120	ns ns	1
t_{OEA}	t_{GLQV}	Output Enable Access Time		35		50	ns	1
t_{CEL} 1 & 2	t_{E1LQX} t_{E2HQV}	Chip Enable 1 & 2 to Output Low-Z	5 5		5 5		ns ns	2
t_{OEL}	t_{GLQX}	Output Enable to Low-Z	0		0		ns	2
t_{CEZ} 1 & 2	t_{E1HQZ} t_{E2LQZ}	Chip Enable 1 & 2 to High-Z		30 30		40 40	ns ns	2
t_{OEZ}	t_{GHQZ}	Output Enable to High-Z		30		40	ns	2
t_{OH}	t_{AXQX}	Output Hold From Address Change	5		5		ns	1

WRITE MODE

The MK48H64 and MK48H65 are in the Write mode whenever the $\overline{W}$ and $\overline{E1}$ pins are low, with E2 high. Either Chip Enable pin or $\overline{W}$ must be inactive during Address transitions. The Write begins with the concurrence of both Chip Enables being active with $\overline{W}$ low. Therefore address setup times are referenced to Write Enable and both Chip Enables as t_{AVWL}, t_{AVE1L}, and t_{AVE2H} respectively, and is determined to the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{E1}$ or $\overline{W}$, or the falling edge of E2.

If the Output is enabled ($\overline{E1}$ = low, E2 = high, $\overline{G}$ = low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DVWH} to the rising edge of Write Enable, or to the rising edge of $\overline{E1}$ or the falling edge of E2, whichever occurs first, and remain valid t_{WHDX} after the rising edge of $\overline{E1}$ or $\overline{W}$, or the falling edge of E2.

Figure 6 : Write Timing N° 1 ($\overline{W}$ control).

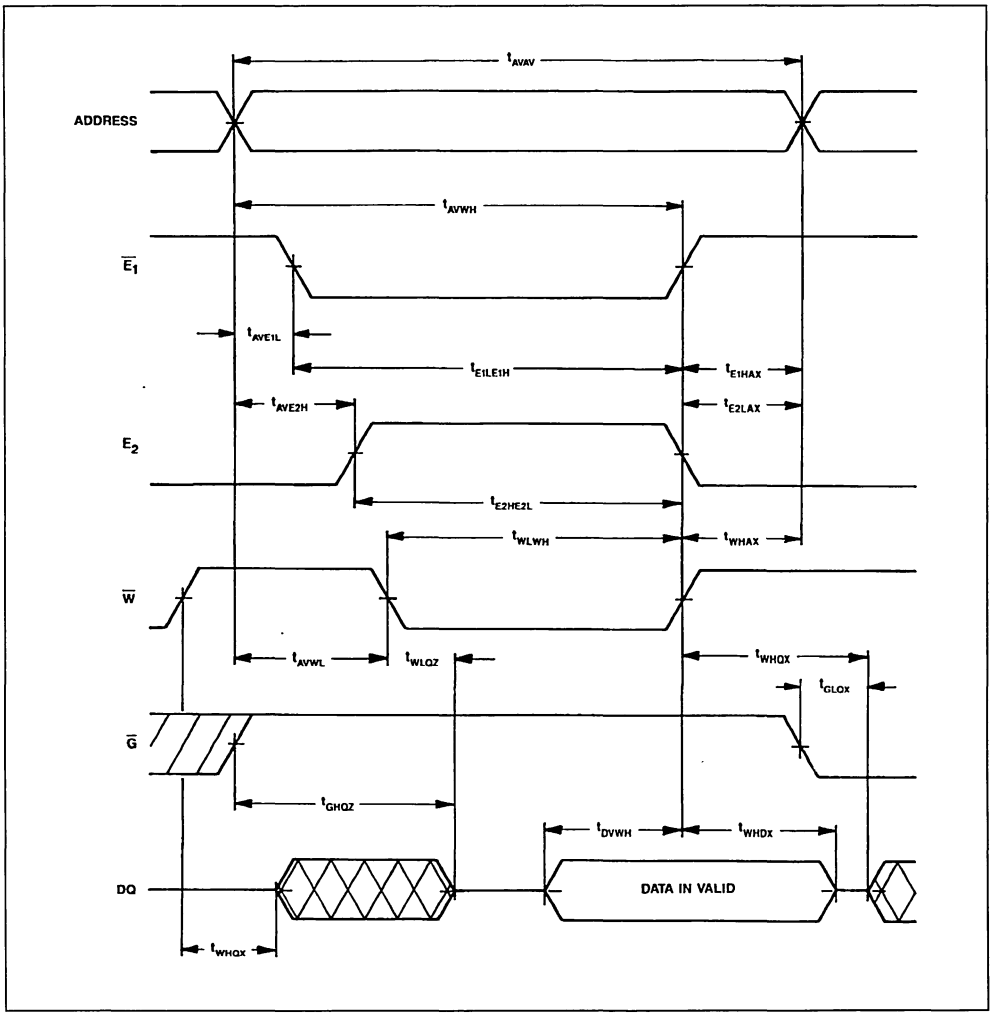
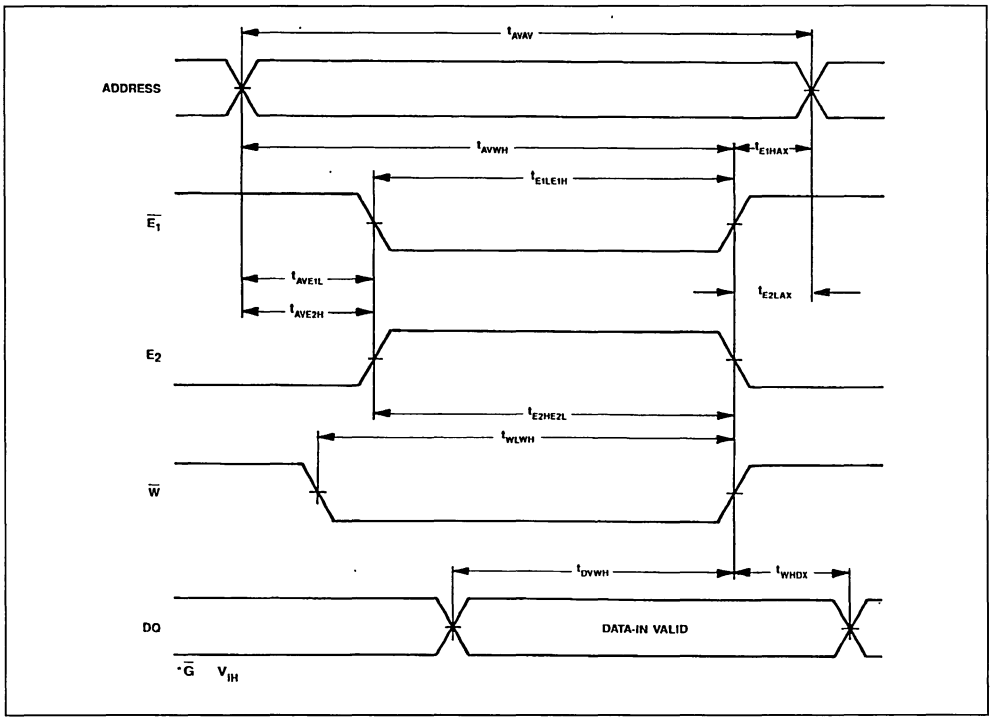


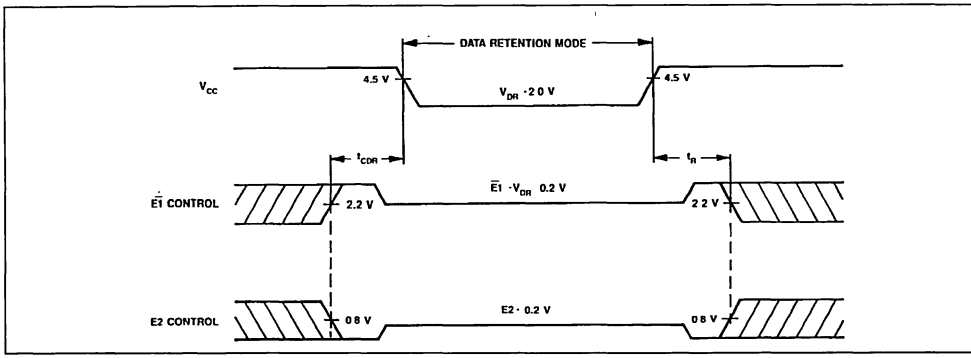
Figure 7 : Write Timing N° 2 ($\overline{E}_1$).



WRITE CYCLE TIMING

Symbol		Parameter	48H64-70 48H64L-70		68H64-120 68H64L-120		Unit	Notes
ALT.	STD.		Min.	Max.	Min.	Max.		
t_{WC}	t_{AVAV}	Write Cycle Time	70		70		ns	
t_{AS}	t_{AVWL}	Address Set-up Time to Write Enable Low	0		0		ns	
t_{AS}	t_{AVE1L} t_{AVE2H}	Address Set-up Time to Chip Enable	0		0		ns	
t_{AW}	t_{AVWH}	Address Valid to End of Write	60		85		ns	
t_{WEW}	t_{WLWH}	Write Pulse Width	60		70		ns	
t_{AH}	t_{WHAX}	Address Hold Time after End of Write	10		10		ns	
t_{CEW}	t_{E1LE1H} t_{E2HE2L}	Chip Enable to End of Write	60		70		ns	
t_{WR}	t_{E1HAX} t_{E2LAX}	Write Recovery Time to Chip Disable	10		10		ns	
t_{DW}	t_{DVWH}	Data Valid to End of Write	40		40		ns	
t_{DH}	t_{WHDX}	Data Hold Time	0		0		ns	
t_{WEL}	t_{WHDX}	Write High to Output Low-Z (active)	0		0		ns	2
t_{WEZ}	t_{WLQZ}	Write Enable to Output High-Z		30		35	ns	2

Figure 8 : Low V_{CC} Data Retention Timing.



LOW V_{CC} DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Value		Unit	Notes
		Min.	Max.		
VDR	V_{CC} Data Retention	2.0	$V_{CC(min)}$	V	
$I_{CC}DR$	Data Retention Power Supply Current, MK48H64		500	µA	3
$I_{CC}DR$	Data Retention Power Supply Current, MK48H64L		25	µA	3
t_{CDR}	Chip Deselection to Data Retention Time	0		ns	
t_R	Operation Recovery Time	t_{AVAV}		ns	

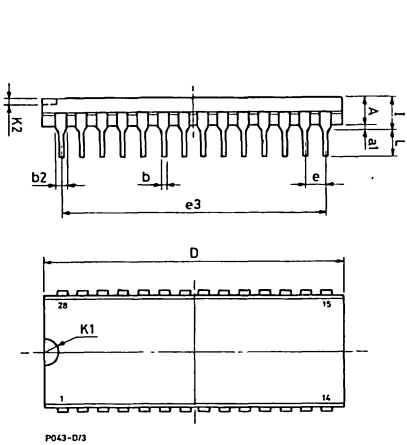
Note : t_{AVAV} = Read Cycle Time.

ORDER CODES

Part Number	Access Time	Package Type	Temperature Range
MK48H64N-70	70ns	28 pin 600 mil Plastic DIP	0°C to 70°C
MK48H64N-120	120ns	28 pin 600 mil Plastic DIP	0°C to 70°C
MK48H64S-70	70ns	28 pin 330 mil SOIC	0°C to 70°C
MK48H64S-120	120ns	28 pin 330 mil SOIC	0°C to 70°C
MK48H64LN-70	70ns	28 pin 600 mil Plastic DIP	0°C to 70°C
MK48H64LN-120	120ns	28 pin 600 mil Plastic DIP	0°C to 70°C
MK48H64LS-70	70ns	28 pin 330 mil SOIC	0°C to 70°C
MK48H64LS-120	120ns	28 pin 330 mil SOIC	0°C to 70°C

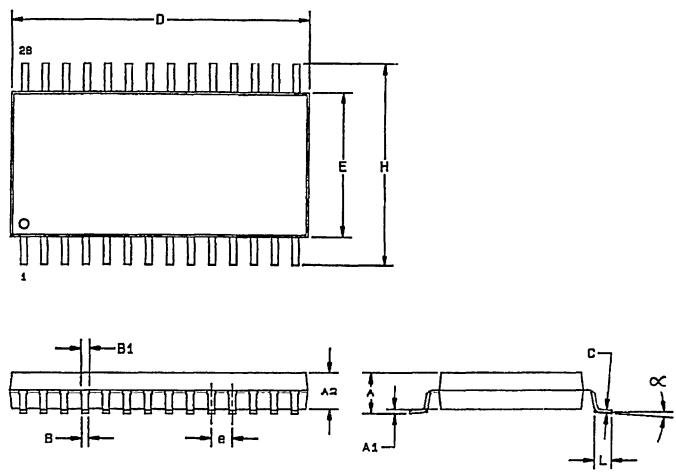
MECHANICAL DATA

Figure 7 : MK48H64 28-Pin Plastic DIP (N), 600-Mil.



Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A						
a1		0 63			.025	
B		0.45			.018	
b1	0.23		0 31	0 009		.012
b2		1.27			.050	
C						
D			37.34			1.470
E	15.20		16.68	0.598		.657
e		2.54			100	
e3		33.02			1.300	
e4						
F			14.10			.555
I		4.45			.175	
L		3.30			.130	
K1						
K2						

Figure 8 : MK48H64 28-Lead Plastic Micropackage (S), 300-Mil.



Dim.	Inches	
	Min.	Max.
A		.120
A1	.002	.014
A2	.092	.106
B	.014	.020
B1	.014	.024
C	.006	.0125
D	.697	.728
E	.324	.350
e	.050 Basic	
H	.453	.500
L	.016	.050
α	0°	8°

SGS-THOMSON MICROELECTRONICS

MK48H89(N) -20/25/35

73,728-BIT 8K X 9 CMOS FAST SRAM

ADVANCE DATA

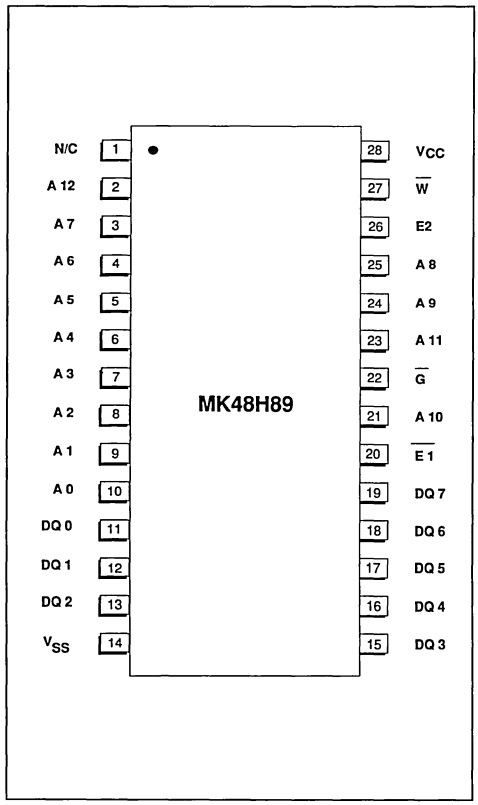
- BYTEWYDE 8K X 9 CMOS FSRAM
- FAST ACCESS TIMES, 20,25,35NS MAX.
- EQUAL ACCESS AND CYCLE TIMES
- LOW V_{CC} DATA RETENTION 2 VOLTS
- THREE STATE OUTPUT
- STANDARD 28-PIN PACKAGE IN 300 MIL PLASTIC DIP

DESCRIPTION

The MK48H89 is a 73,728-bit static RAM, organized as 8K X 9 bits. It is fabricated using SGS-Thomson's low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single + 5V ± 10% supply, and all inputs and outputs are TTL compatible.

The MK48H89 has a Chip Enable power down feature which sustains an automatic standby mode whenever either Chip Enable goes inactive ($\overline{E}_1$ goes high or E_2 goes low). An Output Enable ($\overline{G}$) pin provides a high speed tristate control, allowing fast read/write cycles to be achieved with the common-I/O data bus. Operational modes are determined by device control inputs $\overline{W}$, $\overline{G}$, $\overline{E}_1$ and E_2, as summarized in the truth table.

PIN CONNECTION



PIN NAMES

A_0-A_{12}	Address Inputs
DQ_0-DQ_8	Data I/O_{0-8}
$\overline{E}_1$	Chip Enable 1, Active Low
E_2	Chip Enable 2, Active High
$\overline{G}$	($\overline{OE}$) Output Enable
$\overline{W}$	Write/read Enable
V_{CC},V_{SS}	+5V, GND

MK48H89 TRUTH TABLE

$\overline{W}$	$\overline{E}_1$	E_2	$\overline{G}$	MODE	DQ	POWER
X	H	X	X	Deselect	Hi-Z	Standby
X	X	L	X	Deselect	Hi-Z	Standby
H	L	H	H	Read	Hi-Z	Active
H	L	H	L	Read	Q_{OUT}	Active
L	L	H	X	Write	D_{IN}	Active

READ MODE

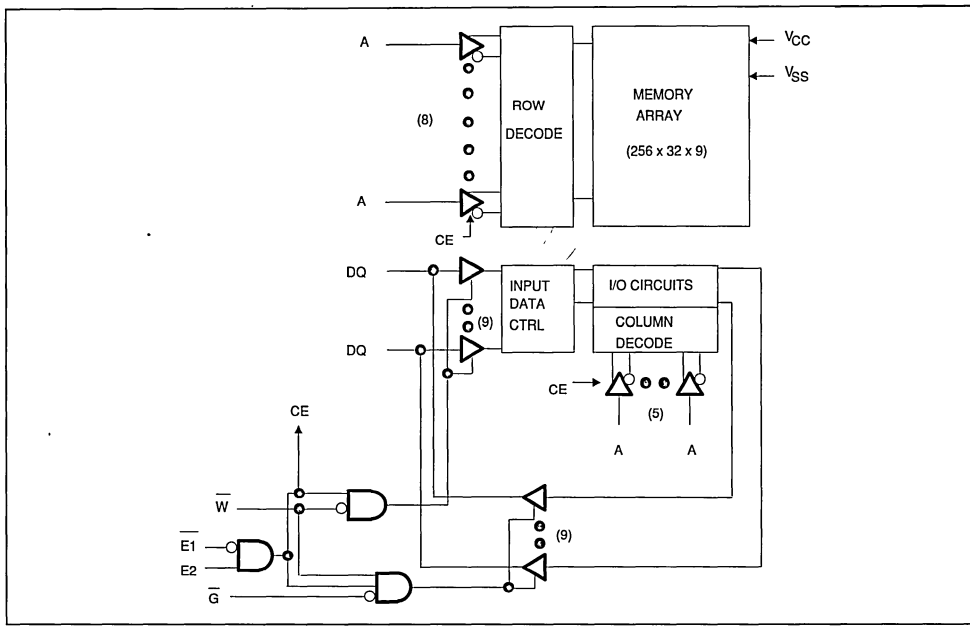
The MK48H89 is in the Read mode whenever Write Enable ($\overline{W}$) is high with Output Enable ($\overline{G}$) low, and both Chip Enables ($\overline{E1}$ and E2) are active. This provides access to data from nine of 73,728 locations in the static memory array, specified by the 13 address inputs . Valid data will be available at the nine Output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is low, $\overline{E_1}$ is low, and E_2 is high. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{E1LQV}, t_{E2HQV}, or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{E1LQX}, t_{E2HQX}, and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

WRITE MODE

The MK48H89 is in the Write mode whenever the $\overline{W}$ and $\overline{E_1}$ pins are low, with E_2 high. Either Chip Enable pin or $\overline{W}$ must be inactive during Address transitions. The Write begins with the concurrence of both Chip Enables being active with $\overline{W}$ low. Therefore, address setup times are referenced to Write Enable and both Chip Enables as t_{AVWL}, t_{AVE1L} and t_{AVE2H} respectively, and is determined to the latter occuring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{E_1}$, $\overline{W}$, or the falling edge of E_2.

If the Output is enabled ($\overline{E_1}$ = low, E_2 = high, $\overline{G}$ = low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DVWH} to the rising edge of Write Enable, or to the rising edge of $\overline{E_1}$ or the falling edge of E_2, whichever occurs first, and remain valid t_{WHDX}.

MK48H89 BLOCK DIAGRAM



SGS-THOMSON MICROELECTRONICS

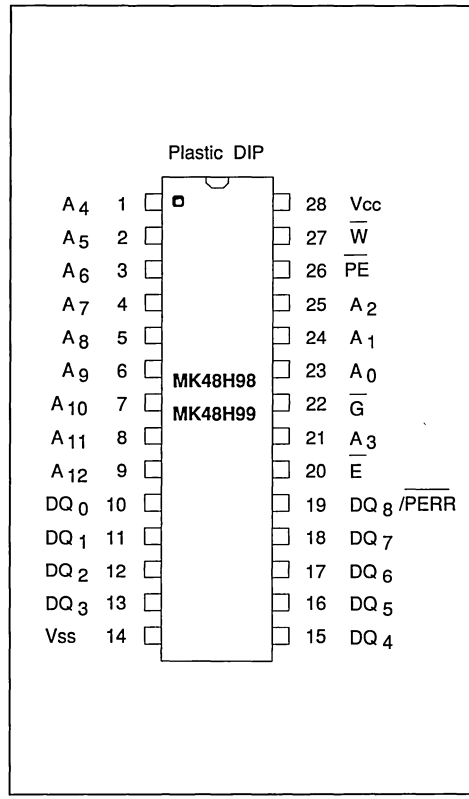
MK48H98/99(N) -20/30/40

73,728-BIT 8 K X 8/9 CMOS PARITY SRAM

ADVANCE DATA

- BYTEWYDE 8K x 9 CMOS STATIC RAM
- CONFIGURABLE: x9/ or x8 plus PARITY
- 20,30,40ns DATA ACCESS TIMES
- 25,35,45ns PARITY ERROR ACCESS TIMES
- FAST CYCLE TIMES = 25,35,45ns
- 28-PIN 300 MIL PLASTIC DIP

PIN CONNECTION



DESCRIPTION

The MK48H98/99 is a 73,728-bit CMOS Parity SRAM, organized 8K x 9 using SGS-THOMSON Microelectronics' advanced HCMOS process technology. The MK48H98/99 has a Chip Enable power down feature which sustains an automatic standby mode whenever Chip Enable ($\overline{E}$) goes inactive high. An Output Enable ($\overline{G}$) pin provides a fast high impedance control, allowing fast read/write cycles to be achieved with the common-I/O data bus.

This device offers a high performance CMOS static RAM with a parity generator/checker option on chip. The $\overline{PE}$ input allows the device to be configured with or without the parity function. When parity is enabled, true parity is generated and stored internally during write operations. Parity data is accessed and checked during read operations. The MK48H98 employs an internal **even** parity scheme, while the MK48H99 employs an **odd** parity scheme. The $\overline{PERR}$ pin is an open-collector output for parity error detection, and easy wired-OR system implementation. If parity is disabled, then DQ_8 is simply another data I/O buffer with a totem-pole configuration. The Parity SRAM requires a single +5 volt supply ± 10%, and all inputs and outputs are TTL compatible.

PIN NAMES

A_0-A_{12}	Address Inputs
DQ_0-DQ_7	Data I/O_{0-7}
$DQ_8/\overline{PERR}$	Data I/O_8, Parity Error
$\overline{E}_1$	Chip Enable
$\overline{PE}$	Parity Enable
$\overline{G}$	($\overline{OE}$) Output Enable
$\overline{W}$	Write/read Enable
V_{CC},V_{SS}	+5V, GND

MODES OF OPERATION

As previously mentioned, the $\overline{PE}$ input can configure the MK48H98/99 to internally generate and check true parity. When the $\overline{PE}$ input is a logic zero (V_{IL}), the parity function (parity generator/checker) is enabled. If $\overline{PE}$ is a logic one (V_{IH}), the device is configured as a standard 8K x 9 SRAM. The device configuration can be accomplished by tying the $\overline{PE}$ input either high or low, depending upon the desired mode of operation. For diagnostic purposes, a parity error can be forced by writing a false parity bit pattern ($\overline{PE}$= V_{IH}), and reading with parity true ($\overline{PE}$= V_{IL}). This defines a dynamic approach for **mix-mode** operation in addition to the basic device modes.

The mix-mode operation allows the parity function to be enabled while Writing ($\overline{PE}$ = V_{IL}), and disabled during Read operations ($\overline{PE}$ = V_{IH}). This provides the user with self-generated parity from the Parity SRAM, with an external system parity bit. Conversely, parity can be disabled while Writing ($\overline{PE}$ = V_{IH}), and true parity checked internally with a device parity error detection ($\overline{PERR}$) during Read operations ($\overline{PE}$ = V_{IL}). This mode allows the device to check system generated parity without designing external parity logic. However, transceiver logic is required for DQ_8/$\overline{PERR}$ in this mode. The MK48H98/99 Truth table depicts all modes of operation. This includes either static or dynamic mode operations.

MK48H98/99 TRUTH TABLE

$\overline{E}$	$\overline{W}$	$\overline{G}$	$\overline{PE}$	MODE	DQ
H	X	X	X	Standby	Hi-Z
L	L	X	H	Write X 9(1)	D_{IN}
L	H	L	H	Read X 9(1)	D_{OUT}
L	H	H	H	Read X 9(1)	Hi-Z
L	L	X	L	Write X 8(2)	D_{IN}
L	H	L	L	Read X 8(2)	D_{OUT}
L	H	H	L	Read X 8(2)	Hi-Z

NOTES :

(1) Operation and configuration as an 8K X 9 SRAM ($\overline{PE}$= High)

(2) Generate and store true parity during Write Cycles; $\overline{PERR}$ enabled and valid during Read Cycles ($\overline{PE}$= Low)

READ MODE

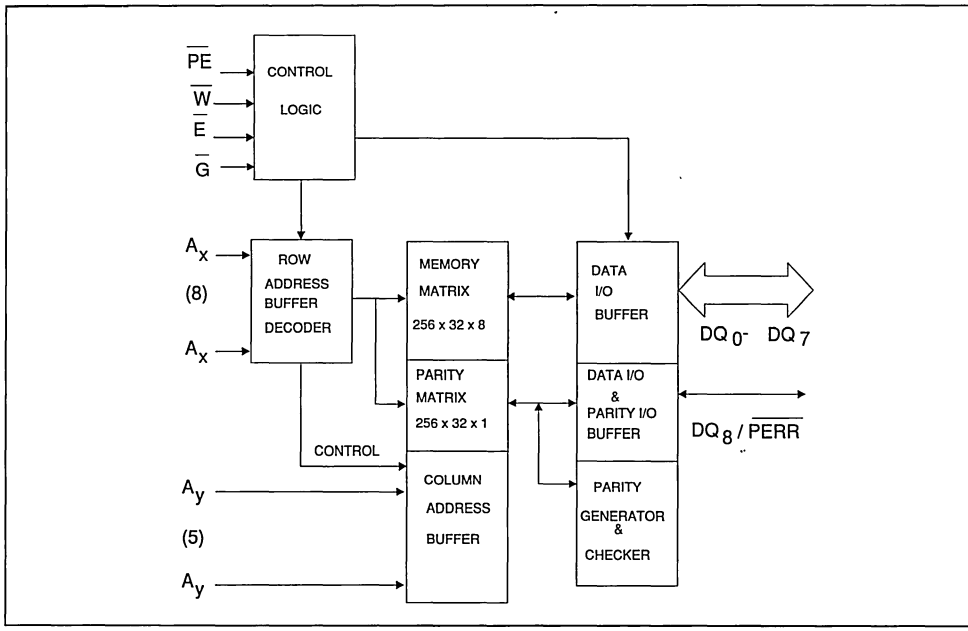
The MK48H98/99 is in the Read mode whenever Write Enable ($\overline{W}$) is high and Chip Enable ($\overline{E}$) is low. This provides access to data from nine of 73,728 locations in the static memory array. If Parity Enable ($\overline{PE}$) is high, data is accessed as a 9-bit word; if $\overline{PE}$ is low data is accessed as an 8-bit word plus parity error ($\overline{PERR}$). The unique address is specified by the 13 address inputs. Valid data will be available at the DQ Output pins within t_{AVQV} after the last stable address, and $\overline{PERR}$ will be valid within t_{AVPV} of the last stable address providing $\overline{G}$, $\overline{E}$, and $\overline{PE}$ are low (see truth table for logic options). If $\overline{E}$, $\overline{PE}$, or $\overline{G}$ access times are not met, data access and parity error access times will be measured from the limiting parameter t_{ELQV}, t_{ELPV}, t_{PELPV}, t_{PEHQV}, t_{GLQV}, or t_{GLPV} rather than the address.

WRITE MODE

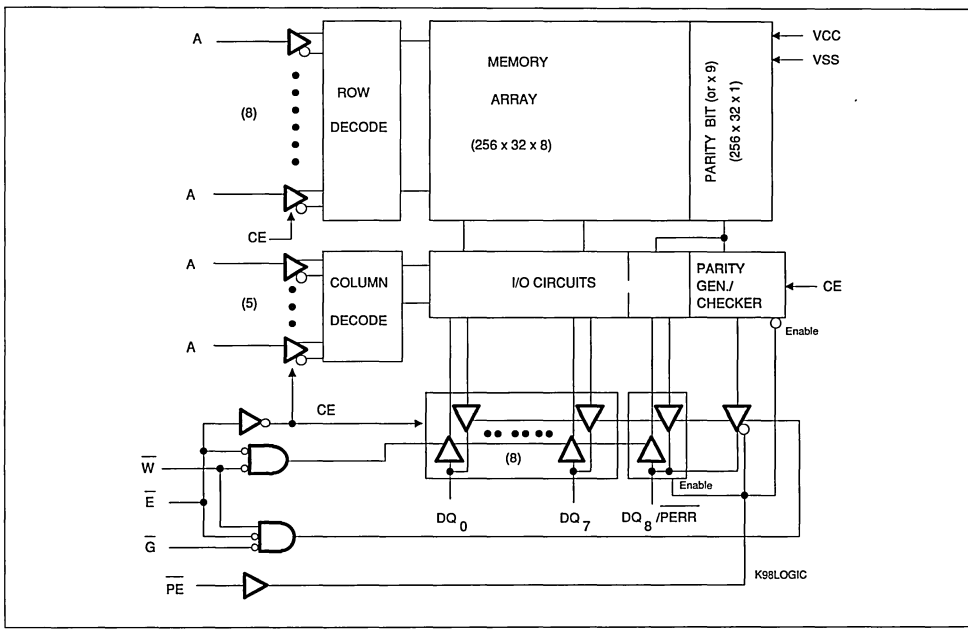
The MK48H98/99 is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ pins are low. Either $\overline{E}$ or $\overline{W}$ must be inactive during Address transitions. The Write begins with the concurrence of $\overline{E}$ and $\overline{W}$ being active low. Therefore, address setup times are referenced to $\overline{W}$, $\overline{E}$, and/or $\overline{PE}$ as t_{AVWL}, t_{AVEL} and t_{AVPEL} respectively, and is determined to the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of Write Enable or Chip Enable. Parity Enable ($\overline{PE}$) allows the on-board parity function to generate true parity if active low, but cannot terminate a write cycle by going high.

If the Output is enabled ($\overline{E}$ = low, and $\overline{G}$ = low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DVWH} to the rising edge of $\overline{W}$, $\overline{E}$ or $\overline{PE}$, whichever occurs first, and remain valid t_{WHDX}.

MK48H98/99 BLOCK DIAGRAM N°. 1



BLOCK DIAGRAM N°. 2

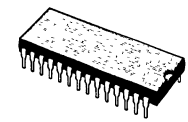


MK48S74(N,X)-20/22/25
MK48S75(N)-20/22/25

64K (8K x 8-BIT) FAST CMOS TAGRAM™

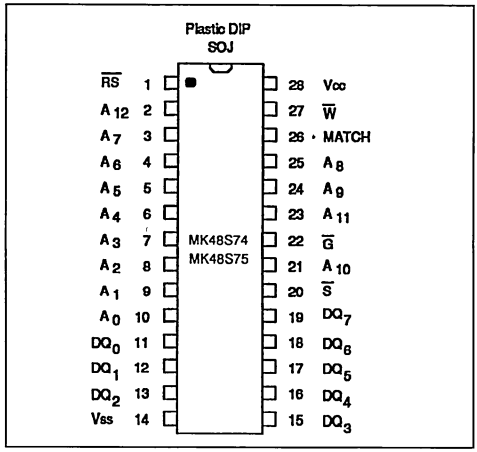
ADVANCE DATA

- 8K x 8 CMOS SRAM WITH ONBOARD COMPARATOR
- ADDRESS TO COMPARE ACCESS 20/22/25ns
- FAST CHIP SELECT TO COMPARE ACCESS 15ns
- MATCH OUTPUT WITH FAST TAG DATA TO COMPARE ACCESS OF 12/15ns (max.)
- STATIC OPERATION - NO CLOCKS OR TIMING STROBES REQUIRED
- ALL INPUTS AND OUTPUTS ARE FULLY TTL COMPATIBLE
- FULL CMOS FOR LOW POWER OPERATION
- OPEN DRAIN MATCH OUTPUT
- THREE-STATE OUTPUT
- 28 PIN 300/600 MIL DIP (MK48S74N/75N)
- 28 PIN 330 MIL SOJ (MK48X74S)
- HIGH SPEED ASYNCHRONOUS RAM CLEAR



N
DIP-28
(Plastic Package)

Figure 1 : Pin Connections.



DESCRIPTION

The MK48S74/75 are a 65,636-bit fast static cache TAGRAM organized as 8K x 8 bits. It is fabricated using SGS-THOMSON Microelectronics low power, high performance, CMOS technology. The MK48S74/75 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The device requires a single + 5V ± 10 percent supply, and is fully TTL compatible.

The MK48S74/75 has a fast Chip Select control for high speed operation to Match Compare valid, and device select/deselect operations. Additionally, the MK48S74/75 provides a Reset Clear, and Match compare pin. The Reset Clear input provides an asynchronous RAM clear control which clears all internal RAM bits to zero in only two cycles. The MATCH output features an open-drain for wired OR operation. During a match compare cycle, an onboard 8-bit comparator compares the Data Inputs (8-bit TAG) at the specified address index (A_0-A_{12}) to the internal RAM data. If a match exists, the MATCH output issues a HIGH match valid signal. If a miss condition exists, where at least one bit of TAG data does not match the internal RAM, then the MATCH output issues a LOW miss signal.

PIN NAMES

A_0 - A_{12}	– Address Inputs
DQ_0 - DQ_7	– Data Input/output
$\overline{S}$	– Chip Select
$\overline{W}$	– Write Enable
$\overline{G}$	– Output Enable
V_{CC}	– + 5V
V_{SS}	– Ground
$\overline{RS}$	Reset Flash Clear
MATCH	Match Output

ABSOLUTE MAXIMUM RATINGS*

Parameter	Value	Unit
Voltage on any Pin Relative to GND	– 1.0 to 7.0	V
Ambient Operating Temperature (T_A)	0 to + 70	°C
Ambient Storage Temperature (plastic)	– 55 to + 125	°C
Ambient Storage Temperature (ceramic)	– 65 to + 150	°C
Total Device Power Dissipation	1	Watt
Output Current per Pin	50	mA

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

TRUTH TABLE (MK48SH74/75)

$\overline{W}$	$\overline{S}$	$\overline{G}$	$\overline{RS}$	Mode	DQ	Match
X	X	X	L	Reset Clear	High-Z	High-Z
X	H	X	H	Deselect	High-Z	High-Z
H	L	H	H	Miss-NOmatch	D_{IN}	Low
H	L	H	H	Match	D_{IN}	High-Z
H	L	L	H	Read	Q_{OUT}	High-Z
L	L	X	H	Write	D_{IN}	High-Z

RECOMMENDED DC OPERATING CONDITIONS (0°C ≤ T_A ≤ + 70°C)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	4
V_{SS}	Supply Voltage	0	0	0	V	4
V_{IH}	Logic 1 Voltage, all Inputs	2.2		V_{CC} + 0.3	V	4
V_{IL}	Logic 0 Voltage, all Inputs	– 0.3		0.8	V	4

DC ELECTRICAL CHARACTERISTICS
(0°C ≤ T_A ≤ + 70°C) (V_{CC} = 5.0 ± 10 percent)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
I_{CC1}	Average Power Supply Current f = min Cycle			150	mA	5
I_{CC2}	Average Power Supply Current f = 0			110	mA	6
I_{IL}	Input Leakage Current (any input pin)	– 1		+ 1	µA	7
I_{OL}	Output Leakage Current (any Q output pin)	– 5		+ 5	µA	8
V_{OH}	Output Logic 1 Voltage (I_{OUT} = – 4mA)	2.4			V	4
V_{OL}	Output Logic 0 Voltage (I_{OUT} = + 8mA)			0.4	V	4
V_{OL}	Match Output Logic 0 Voltage (I_{OUT} = 18mA)			0.4	V	4

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

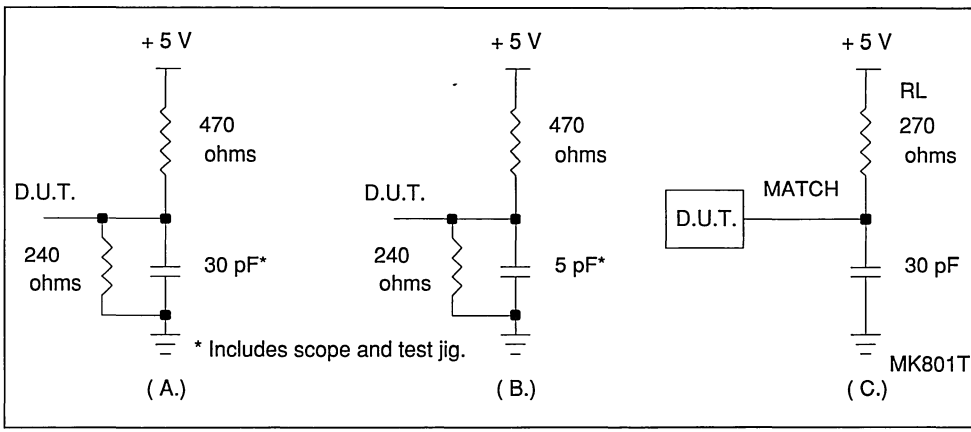
Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
C_1	Capacitance on Input Pins	4		5	pF	9
C_2	Capacitance on DQ Pins	8		10	pF	9

Notes :
1. Measured with load shown in figure 2(A).
2. Measured with load shown in figure 2(B).
3. Measured with load shown in figure 2(C).
4. All voltages referenced to GND.
5. I_{CC1} is measured as the average AC current with V_{CC} = V_{CC} (max) and with the outputs open circuit. t_{AVAV} = t_{AVAV} (min) duty cycle 100%.
6. I_{CC2} is measured with outputs open circuit.
7. Input leakage current specifications are valid for all V_{IN} such that 0V< V_{IN} < V_{CC}. Measured at V_{CC} = V_{CC} (max).
8. Output leakage current specifications are valid for all V_{OUT} such that 0V< V_{OUT} < V_{CC}, $\overline{S}$ = V_{IH}, and V_{CC} in valid operating range.

AC TEST CONDITIONS

Input Levels ..... GND to 3.0V
Transition Times 5ns
Input and Output Signal Timing Reference Level 1.5V
Ambient Temperature ..... 0°C to 70°C
V_{CC} ..... 5.0V ± 10 percent

Figure 2 : Output Load Circuits.



OPERATIONS

READ MODE

The MK48S74/75 are in the read mode whenever Write Enable ($\overline{W}$) is HIGH with Output Enable ($\overline{G}$) LOW, and Chip Select ($\overline{S}$) is active. This provides access to data from eight of 65,536 locations in the static memory array. The unique address specified by the 13 Address Inputs defines which one of the 8192 8-bit bytes is to be accessed.

Valid data will be available at the eight Output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is LOW, and $\overline{S}$ is LOW. If Chip Select or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{SLQV} or t_{GLQV}) rather than the address. The state of the DQ pins is controlled by the $\overline{S}$, $\overline{G}$, and $\overline{W}$ control signals. Data out may be indeterminate at t_{SLQX} and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

Figure 3a : Read Timing N°1 (address access).

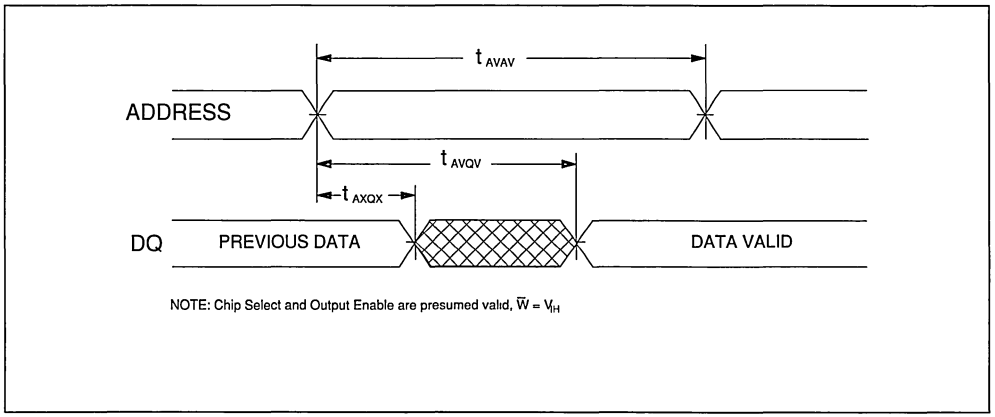
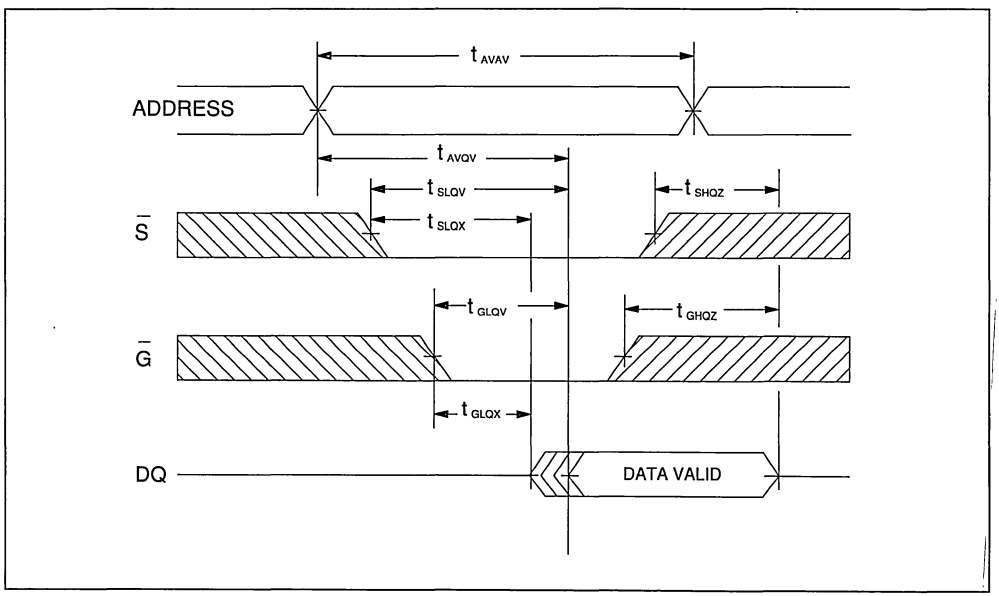


Figure 3b : Read Timing N°2 ($\overline{W}$ = V_{IH}).



AC ELECTRICAL CHARACTERISTICS (read cycle timing)

($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0 \pm 10\%$)

Symbols		Parameter	– 20		– 22		– 25		Unit	Notes
ALT.	STD.		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	t_{AVAV}	Read Cycle Time	20		25		25		ns	
t_{AA}	t_{AVQV}	Address Access Time		20		25		25	ns	1
t_{CSA}	t_{SLQV}	Chip Select Access Time		15		15		15	ns	
t_{OEA}	t_{GLQV}	Output Enable Access Time		10		12		15	ns	1
t_{CSL}	t_{SLQX}	Chip Select to Output Low-Z	0		0		0		ns	
t_{OEL}	t_{GLQX}	Output Enable to Low-Z	0		0		0		ns	
t_{CSZ}	t_{SHQZ}	Chip Select to High-Z	0	10	0	10	0	10	ns	
t_{OEZ}	t_{GHQZ}	Output Enable to High-Z		10		12		15	ns	2
t_{OH}	t_{AXQX}	Output Hold from Address Change	3		3		3		ns	1

WRITE MODE

The MK48S74/75 is in the Write mode whenever the $\overline{W}$ and $\overline{S}$ pins are LOW. Chip Select or $\overline{W}$ must be inactive during Address transitions. The Write begins with the concurrence of Chip Select being active with $\overline{W}$ LOW. Therefore address setup times are referenced to Write Enable and Chip Select as t_{AVWL} and t_{AVSL}, and is determined to the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{S}$ or $\overline{W}$.

If the Output is enabled ($\overline{S}$ = LOW, $\overline{G}$ = LOW), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DVWH} to the rising edge of Write Enable, or to the rising edge of $\overline{S}$, whichever occurs first, and remain valid t_{WHDX} after the rising edge of $\overline{S}$ or $\overline{W}$.

Figure 4a : Writing Timing N°1 ($\overline{W}$ control).

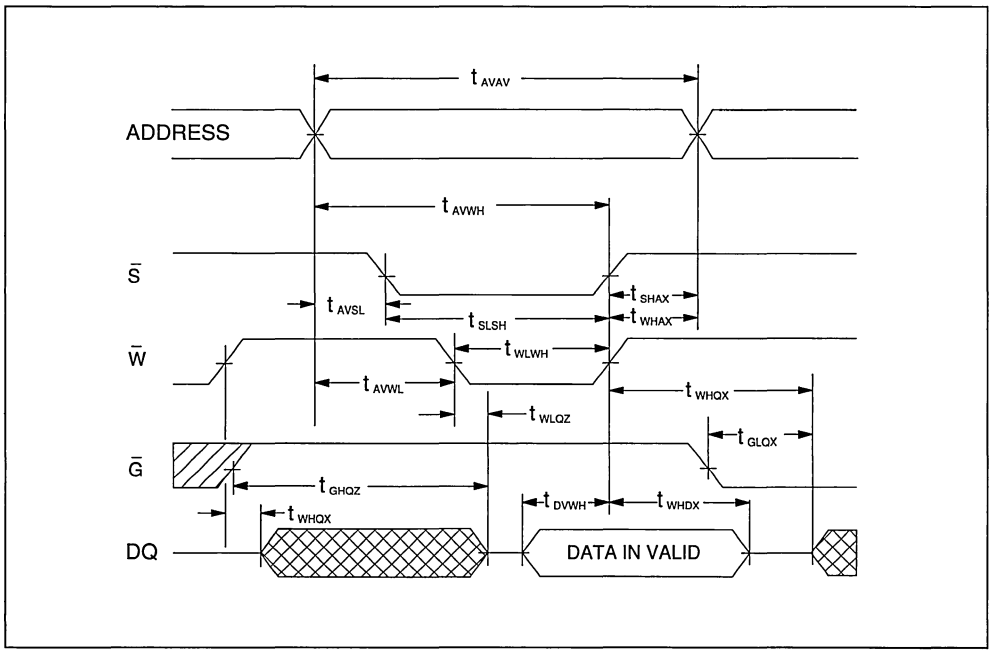
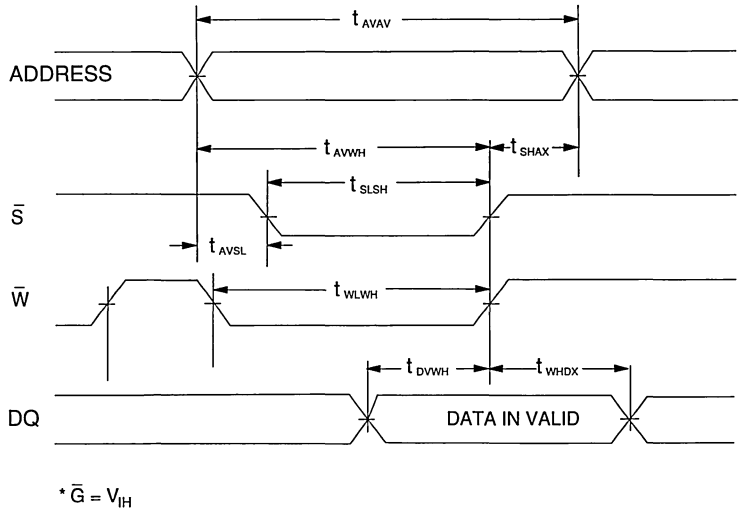


Figure 4b : Write Timing N°2 ($\overline{S}$ control).



AC ELECTRICAL CHARACTERISTICS (write cycle timing)
(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 ± 10%)

Symbols		Parameter	– 20		– 22		– 25		Unit	Notes
ALT.	STD.		Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	t_{AVAV}	Write Cycle Time	20		25		25		ns	
t_{AS}	t_{AVWL}	Address Set-up Time to Write Enable Low	0		0		0		ns	
t_{AS}	t_{AVSL}	Address Set-up Time to Chip Select	0		0		0		ns	
t_{AW}	t_{AVWH}	Address Valid to End of Write	15		20		20		ns	
t_{WEW}	t_{WLWH}	Write Pulse Width	15		20		20		ns	
t_{AH}	t_{WHAX}	Address Hold Time after End of Write	0		0		0		ns	
t_{CSW}	t_{SLSH}	Chip Select to End of Write	15		20		20		ns	
t_{WR}	t_{SHAX}	Write Recovery Time to Chip Deselect	0		0		0		ns	
t_{DW}	t_{DVWH}	Data Valid to End of Write	10		13		30		ns	
t_{DH}	t_{WHDX}	Data Hold Time	0		0		0		ns	
t_{WEL}	t_{WHQX}	Write High to Output Low-Z (active)	0		0		0		ns	2
t_{WEZ}	t_{WLQZ}	Write Enable to Output High-Z		5		7		7	ns	2

COMPARE MODE

The MK48S74/75 are in the Compare mode whenever W and G are HIGH provided Chip Select (S) is active LOW. The 13 index address inputs (A_0-A_{12}) define a unique location in the static RAM array. The data presented on the Data Inputs (DQ_0-DQ_7) as Tag Data is compared to the internal RAM data as specified by the index. If all bits are equal (match) then a hit condition occurs (MATCH = HIGH). When at least one bit is not equal, then MATCH will go LOW signifying a miss condition.

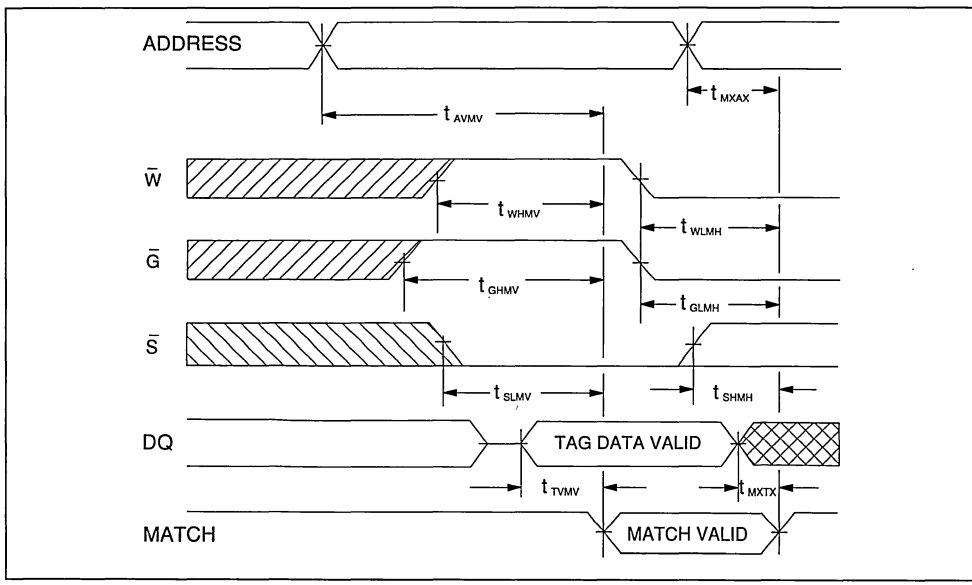
The MATCH output will be valid t_{AVMV} from stable address, or t_{TVMV} from valid Tag Data when S is LOW. Should the address be stable with valid Tag Data, and the device is deselected (S = HIGH), then MATCH will be valid t_{SLMV} from the falling edge of Chip Select (S). When executing a write-to-compare cycle (W = LOW, and G = LOW or HIGH), MATCH will be valid t_{WHMV} or t_{GHMV} from the latter rising edge of W or G respectively.

AC ELECTRICAL CHARACTERISTICS (match compare cycle timing)

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 ± 10%)

Symbols		Parameter	– 20		– 22		– 25		Unit	Notes
ALT.	STD.		Min.	Max.	Min.	Max.	Min.	Max.		
t_{AMA}	t_{AVMV}	Address to MATCH Valid	–	20	–	22	-	25	ns	2
t_{CSM}	t_{SLMV}	Chip Select to MATCH Valid	–	15	–	15	–	15	ns	2
t_{CSMH}	t_{SHMH}	Chip Deselect to MATCH High	–	10	–	12	–	12	ns	2
t_{DMA}	t_{TVMV}	Tag Data to MATCH Valid	–	12	–	15	–	15	ns	2
t_{OEM}	t_{GHMV}	$\overline{G}$ High to MATCH Valid	–	15	–	15	–	15	ns	3
t_{OEMH}	t_{GLMH}	$\overline{G}$ Low to MATCH High	–	10	–	12	–	12	ns	3
t_{WEM}	t_{WHMV}	$\overline{W}$ High to MATCH Valid	–	15	–	15	–	20	ns	3
t_{WEMH}	t_{WLMH}	$\overline{W}$ Low to MATCH High	–	12	–	12	–	15	ns	3
t_{MHA}	t_{AHMV}	MATCH Hold from Address	3	–	3	–	3	–	ns	3
t_{MHD}	t_{DHMV}	MATCH Hold from Tag Data	0	–	0	–	0	–	ns	3

Figure 5 : Match Compare Timing.



RESET MODE

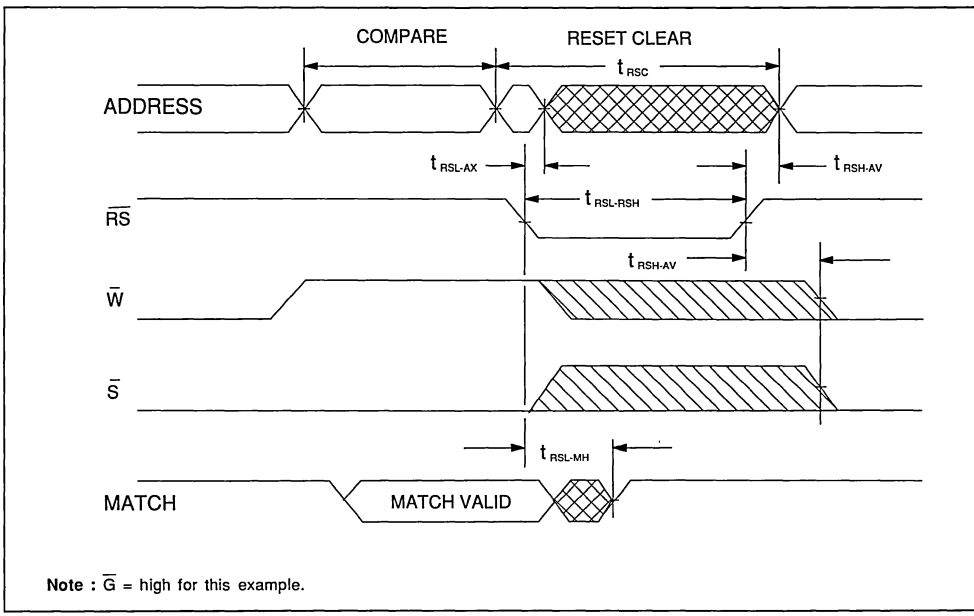
The MK48S74/75 allows an asynchronous reset clear whenever $\overline{RS}$ is LOW regardless of the logic state on the other input pins. Reset clears all internal RAM bits (65536 bits) to a logic zero as long as $t_{RSL-RSH}$ is satisfied. The state of the outputs is determined by the control logic input pins $\overline{S}$, $\overline{W}$, and $\overline{G}$ during reset (see truth table). The MATCH output will go HIGH t_{RSL-MH} from the falling edge of $\overline{RS}$, and all inputs will not be recognized until t_{RSH-AV} from the rising edge of reset ($\overline{RS}$).

AC ELECTRICAL CHARACTERISTICS (reset clear cycle timing)

($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0 \pm 10\%$)

Symbols		Parameter	-20		-22		-25		Unit	Notes
ALT.	STD.		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	t_{RSC}	Flash Clear Cycle Time	40		0		50		ns	
t_{RSX}	t_{RSL-AX}	Reset Clear ($\overline{RS}$) to Inputs Don't Care	0		0		0		ns	
t_{RSV}	t_{RSH-AV}	$\overline{RS}$ to Inputs Valid	5		5		5		ns	
t_{RSP}	$t_{RSL-RSH}$	Reset ($\overline{RS}$) Pulse Width	35		40		40		ns	
t_{RSM}	t_{RSL-MH}	Reset ($\overline{RS}$) to MATCH High		15		15		15	ns	

Figure 6 : Reset Timing.



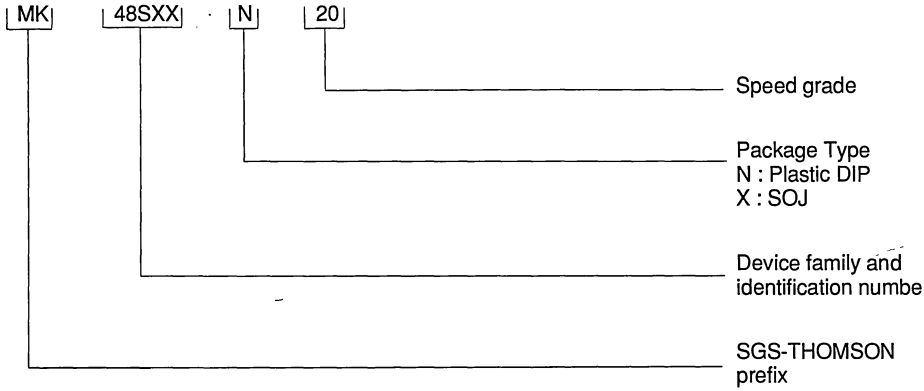
Note : $\overline{G}$ = high for this example.

APPLICATION

The MK48S74/75 operates from a 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. A pull-up resistor is also recommended for the RS input. This will ensure that any low going system noise, coupled onto the input, does not drive RS below V_{IH} minimum specifications. This will enhance proper device operation, and avoid possible partial flash clear cycles. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the MK48S74/75 can also interface to 5 volt CMOS on all inputs and outputs. The MK48S74/75 provides the system designer with 64K fast static memory, a MATCH output, and a BYTEWIDE™ on-board comparator - all in one chip. The MK48S74/75 compares contents of addressed RAM locations to the current data inputs. A logic one (1) output on the MATCH pin indicates that the input data and the RAM contents match. Conversely, a logic zero (0) on the MATCH pin indicates at least one bit difference between the RAM contents and input TAG data generating a miss. The MATCH output is constructed with an open drain arrangement. This provides easy wired-OR implementation when generating a composite MATCH signal.

In a cache subsystem, the MATCH signal provides the processor or CPU with the necessary information concerning wait state conditions. The purpose of a cache subsystem is to maintain a duplicate copy of a portion of the main memory. When a valid match occurs, the system processor uses data from the fast cache memory, and avoids longer cycles to the main memory. Therefore, implementing cache subsystems with the MK48S74/75, and providing good hit or match ratio designs will enhance overall system performance.

Because high frequency current transients will be associated with the operation of the MK48S74/75, power lines inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

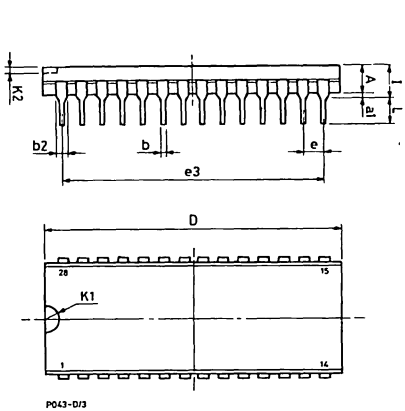


ORDER CODES

Part No.	Match Access Time	Cycle Time	Package Type	Temperature
MK48S74N20	20ns	20ns	28 pin 300 mil DIP	0°C to 70°C
MK48S74N22	22ns	25ns	28 pin 300 mil DIP	0°C to 70°C
MK48S74N25	25ns	25ns	28 pin 300 mil DIP	0°C to 70°C
MK48X74X20	20ns	20ns	28 pin 330 mil SOJ	0°C to 70°C
MK48X74X22	22ns	25ns	28 pin 330 mil SOJ	0°C to 70°C
MK48X74X25	25ns	25ns	28 pin 330 mil SOJ	0°C to 70°C
MK48S75N20	20ns	20ns	28 pin 600 mil DIP	0°C to 70°C
MK48S75N22	22ns	25ns	28 pin 600 mil DIP	0°C to 70°C
MK48S75N25	25ns	25ns	28 pin 600 mil DIP	0°C to 70°C

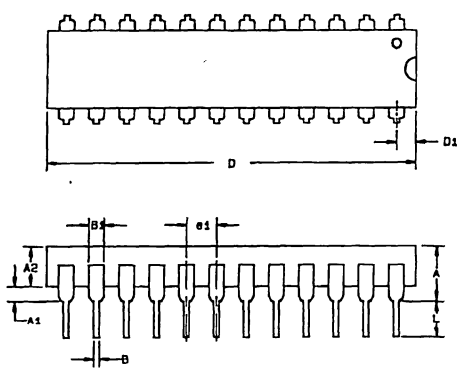
MECHANICAL DATA

Figure 7 : MK48S75 28 Pin Plastic DIP (N) 600 MIL.



Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A						
a1		0 63			.025	
B		0 45			.018	
b1	0 23		0 31	0 009		.012
b2		1 27			.050	
C						
D			37 34			1 470
E	15 20		16 68	0.598		657
e		2 54			100	
e3		33 02			1 300	
e4						
F			14.10			.555
I		4 45			175	
L		3 30			.130	
K1						
K2						

Figure 8 : MK48S74 28 Pin Plastic DIP (N) 300 MIL.



Dim.	Inches	
	Min.	Max.
A		.210
A1	.015	
A2	.120	.140
B	.015	.021
B1	.045	.070
C	.008	.012
D		1.270
D1	.060	.090
E	.300	.325
E1	.240	.270
e1	.090	.110
eA	.300	.365
L	.125	

SGS-THOMSON MICROELECTRONICS

MK48S80(N,X) -15/17/20

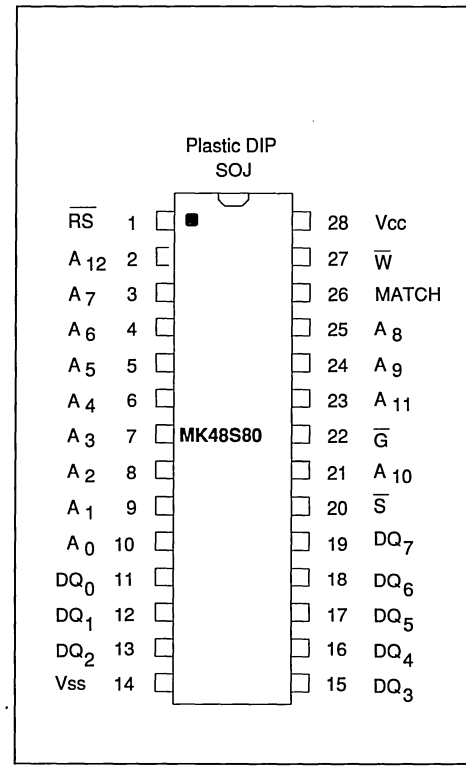
65,536 BIT FAST CMOS 8K X 8 CACHE TAGRAM™

ADVANCE DATA

FEATURES

- 8K X 8 CMOS SRAM WITH ONBOARD COMPARATOR.
- ADDRESS TO COMPARE ACCESS 15/17/20.
- FAST CHIP SELECT COMPARE ACCESS 10ns
- MATCH OUTPUT WITH FAST TAG DATA TO COMPARE ACCESS OF 10/12/14NS (MAX).
- STATIC OPERATION-NO CLOCKS OR TIMING STROBES REQUIRED.
- ALL INPUTS AND OUTPUTS ARE FULLY TTL COMPATIBLE.
- FULL CMOS FOR LOW POWER OPERATION.
- TOTEM-POLE MATCH OUTPUT.
- THREE-STATE OUTPUT.
- 28 PIN 300 MIL DIP & 28 PIN 330 MIL SOJ.
- HIGH SPEED ASYNCHRONOUS RAM CLEAR.

PIN CONNECTION



DESCRIPTION

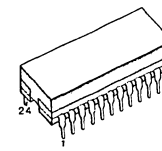
The MK48S80 IS 65,536 fast static cache TAGRAM organized as 8K X 8 bits. It is fabricated using SGS-THOMSON's low power, high performance HCMPOS4 technology. The MK48S80 features fully dtztic opeation requiring no external clocks or timing strobes, and equal access and cycles times. The device requires a single +5v ± 10% supply and is fully TTL compatible. The MK48S80 has a fast Chip Select control for high sped operation to the match compare valid, and device select/deselect operations. Additionally, the MK48S80 provides a Reset Clear, and MATCH compare pin. The RESET CLEAR, input provides an asynchronous RAM clear control which clears all internal RAM bits to zero in only 2 cycles. The MATCH output is in a totem-pole configuration to minimize switching delays associated with open-drain devices. During a MATCH compare cycle, and on-board 8-bit comparator compares the Data Input (8-bit TAG) to the internal RAM data. If a miss condition exists, where at least one bit of TAG data does not match the internal RAM, then the MATCH output issues a LOW miss signal.

MK48S80 TRUTH TABLE

$\overline{W}$	$\overline{S}$	$\overline{G}$	$\overline{RS}$	MODE	DQ	MATCH
X	X	X	L	Reset Clear	High-Z	Invalid
X	H	X	H	Deselect	High-Z	Invalid
H	L	H	H	Miss	D_{IN}	Low
H	L	H	H	Match	D_{IN}	Invalid
H	L	L	H	Read	Q_{OUT}	Invalid

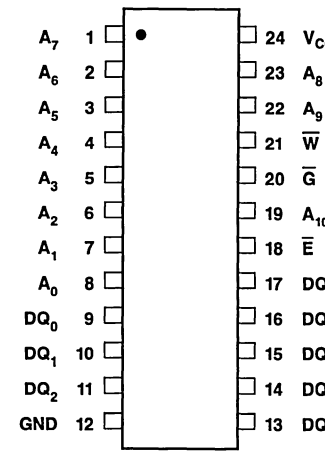
2K × 8 ZEROPOWER™/TIMEKEEPER™ RAM

- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK, CRYSTAL, POWER-FAIL CONTROL CIRCUIT AND BATTERY
- BYTEWIDE™ RAM-LIKE CLOCK ACCESS
- BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES AND SECONDS
- SOFTWARE CONTROLLED CLOCK CALIBRATION FOR HIGH ACCURACY APPLICATIONS
- PREDICTED WORST CASE BATTERY STORAGE LIFE OF 11 YEARS @ 70°C
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 2K × 8 SRAMS
- AUTOMATIC POWER-FAIL CHIP DESELECT/WRITE PROTECTION
- TWO POWER-FAIL DESELECT TRIP POINTS AVAILABLE
  MK48T02 4.75V ≥ V_{PFD} ≥ 4.50V
  MK48T12 4.50V ≥ V_{PFD} ≥ 4.20V



B
DIP-24
(Plastic with Battery Top Alt)

FIGURE 1. PIN CONNECTIONS



Part Number	Access Time	R/W Cycle Time
MK48TX2-12	120 ns	120 ns
MK48TX2-15	150 ns	150 ns
MK48TX2-20	200 ns	200 ns
MK48TX2-25	250 ns	250 ns

TRUTH TABLE (MK48T02/12)

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ
<V_{CC} (Max)	V_{IH}	X	X	Deselect	High-Z
>V_{CC} (Min)	V_{IL}	X	V_{IL}	Write	D_{IN}
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
	V_{IL}	V_{IH}	V_{IH}	Read	High-Z
<V_{PFD} (Min)	X	X	X	Power-Fail	High-Z
>V_{SO}				Deselect	
≤V_{SO}	X	X	X	Battery Back-up	High-Z

PIN NAMES

A_0 - A_{10}	Address Inputs	V_{CC}	+5 V
$\overline{E}$	Chip Enable	$\overline{W}$	Write Enable
GND	Ground	$\overline{G}$	Output Enable
DQ_0—DQ_7 Data In/Data Out			

DESCRIPTION

The MK48T02/12 combines a 2K × 8 full CMOS SRAM, a BYTEWIDE accessible real time clock, a crystal and a long life lithium carbon mono-fluoride battery, all in a single plastic DIP package. The MK48T02/12 is a non-volatile pin and function equivalent to any JEDEC standard 2K × 8 SRAM, such as the 6116 or 5517. It also easily fits into many EPROM AND EEPROM sockets, providing the non-volatility of the PROMs without any requirement for special write timing, or limitations on the number of writes that can be performed.

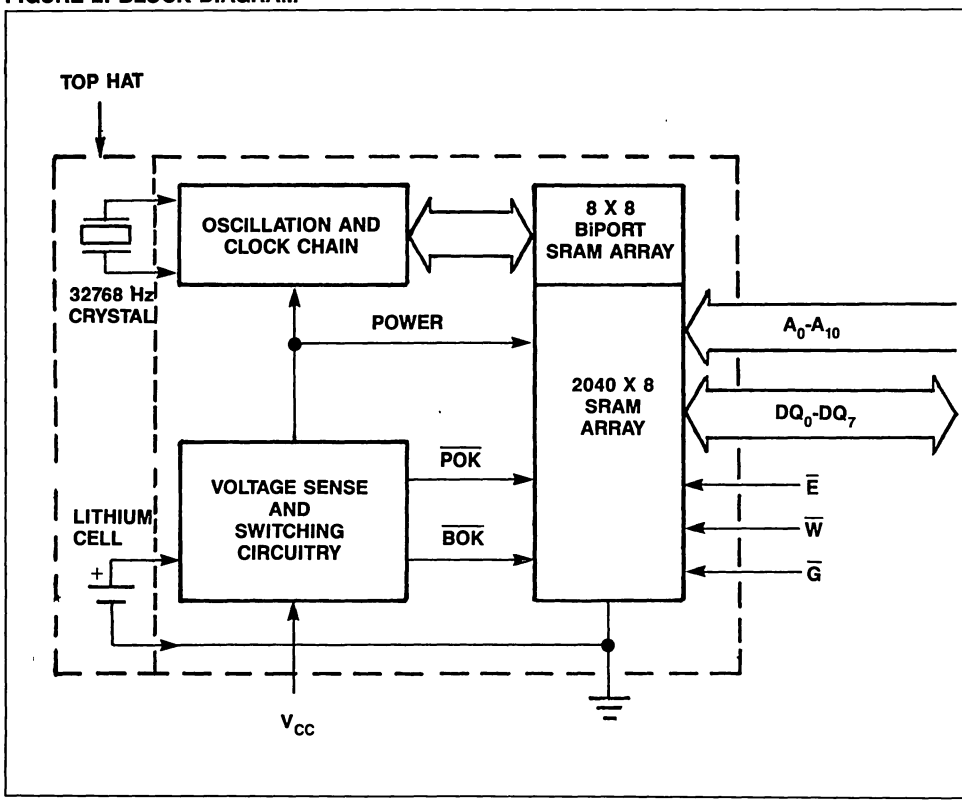
Access to the clock is as simple as conventional BYTEWIDE RAM access because the RAM and the Clock are combined on the same die. As Figure 2 indicates, the TIMEKEEPER registers are located in the upper eight locations of the RAM. The registers contain, beginning at the top; year, month, date, day, hour, minutes, and seconds data in 24 Hour BCD format. Corrections for 28, 29 (Leap Year), 30 and 31 day months are made automatically. The eighth location is a Control register. These registers are not the actual clock counters; they are BiPORT read/write Static RAM memory locations. The MK48T02/12 includes a clock control circuit that, once every second, dumps the counters into the BiPORT RAM.

Because the Clock Registers are constructed using BiPORT memory cells, access to the rest of the RAM proceeds unhindered by updates to the TIMEKEEPER registers, even if the TIMEKEEPER registers are being updated at the very moment another location in the memory array is accessed.

The MK48T02/12 also has its own Power-fail Detect circuit. The circuit deselects the device whenever V_{CC} is out of range, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}.

BiPORT, BYTEWIDE, TIMEKEEPER and ZEROPOWER are trademarks of SGS-THOMSON Microelectronics, Inc..

FIGURE 2. BLOCK DIAGRAM



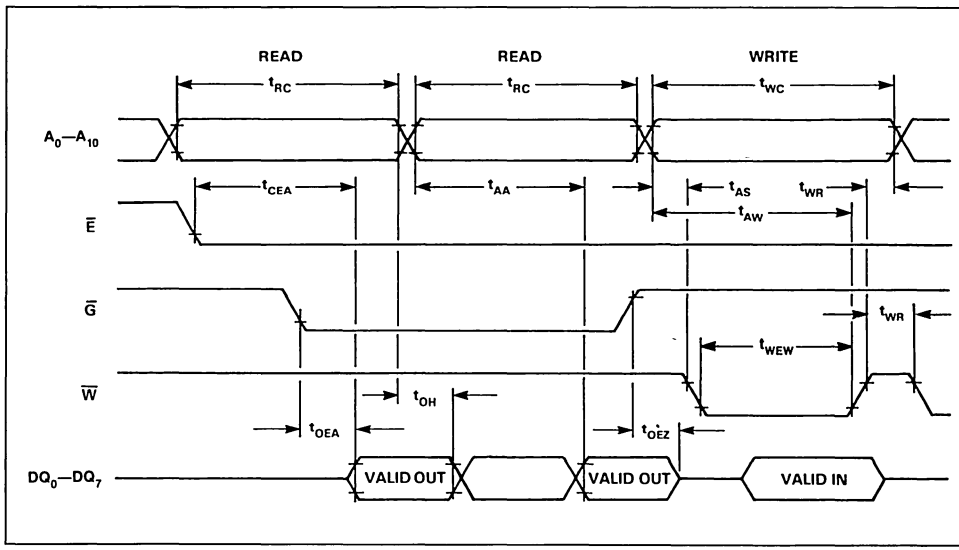
OPERATION

READ MODE

The MK48T02/12 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access (changing Addresses without removing Chip Enable) to any of the 2048 address locations in the static storage array. Valid data will be available at the Data I/O pins within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are satisfied.

If $\overline{E}$ or $\overline{G}$ access times are not yet met, valid data will be available at the latter of Chip Enable Access Time (t_{CEA}) or at Output Enable Access Time (t_{OEA}). The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the Outputs are activated before t_{AA}, the data lines will be driven to an indeterminate state until t_{AA}. If the Address inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for Output Data Hold Time (t_{OH}) but will go indeterminant until the next t_{AA}.

FIGURE 3. READ-READ-WRITE TIMING



AC ELECTRICAL CHARACTERISTICS (READ CYCLE TIMING)
($0°C \le T_A \le 70°C$) (V_{CC} (Max) $\ge V_{CC} \ge V_{CC}$ (Min))

		MK48TX2-12		MK48TX2-15		MK48TX2-20		MK48TX2-25			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	120		150		200		250		ns	
t_{AA}	Address Access Time		120		150		200		250	ns	1
t_{CEA}	Chip Enable Access Time		120		150		200		250	ns	1
t_{OEA}	Output Enable Access Time		75		75		80		90	ns	1
t_{CEZ}	Chip Enable Hi to High-Z		30		35		40		50	ns	
t_{OEZ}	Output Enable Hi to High-Z		30		35		40		50	ns	
t_{OH}	Valid Data Out Hold Time	15		15		15		15		ns	1

NOTE
1. Measured using the Output Load Diagram shown in Figure 13.

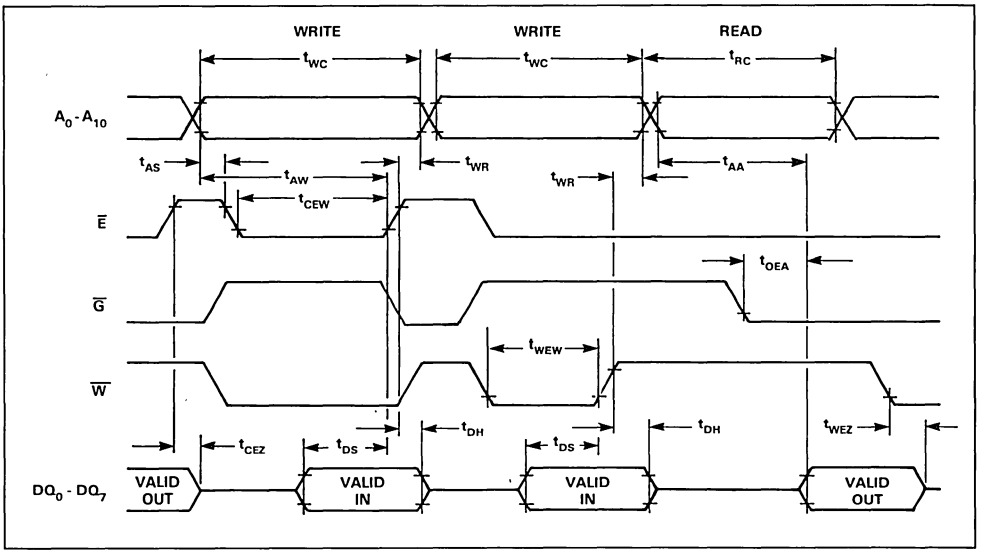
WRITE MODE

The MK48T02/12 is in Write Mode whenever the $\overline{W}$ and $\overline{E}$ inputs are held low. The start of a Write is referenced to the latter occurring falling edge of either $\overline{W}$ or $\overline{E}$. A Write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{W}$ or $\overline{E}$ must return high for a minimum of t_{WR} prior to the initiation of another Read or Write Cycle. Data-in must be valid for t_{DS} prior to the End of Write and remain valid for t_{DH} afterward.

Some processors thrash producing spurious Write Cycles during power-up, despite application of a power-on reset. Users should force $\overline{W}$ or $\overline{E}$ high during power-up to protect memory after V_{CC} reaches V_{CC} (min) but before the processor stablizes.

The MK48T02/12 $\overline{G}$ input is a DON'T CARE in the write mode. $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WEZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

FIGURE 4. WRITE-WRITE-READ TIMING



AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE TIMING)

($0°C \le T_A \le 70°C$) (V_{CC} (Max) $\ge V_{CC} \ge V_{CC}$ (Min))

		MK48TX2-12		MK48TX2-15		MK48TX2-20		MK48TX2-25			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	Write Cycle Time	120		150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		0		ns	
t_{AW}	Address Valid to End of Write	90		120		140		180		ns	
t_{CEW}	Chip Enable to End of Write	75		90		120		160		ns	
t_{WEW}	Write Enable to End of Write	75		90		120		160		ns	
t_{WR}	Write Recovery Time	10		10		10		10		ns	
t_{DS}	Data Setup Time	35		40		60		100		ns	
t_{DH}	Data Hold Time	0		0		0		0		ns	
t_{WEZ}	Write Enable Low to High-Z		40		50		60		80	ns	

CLOCK OPERATIONS

Reading the Clock

Updates to the TIMEKEEPER registers should be Halted before clock data is read to prevent reading of data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual counters, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a "1" is written into the "Read" bit, the seventh most significant bit in the Control register. As long as a "1" remains in that position, updating is halted. After a Halt is issued, the registers reflect the count, that is day, date, and time that were current at the moment the Halt command was issued. All of the TIMEKEEPER registers are updated simultaneously. A Halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a "0".

Setting the Clock

The eighth bit of the Control register is the "Write" bit. Setting the Write bit to a "1", like the Read Bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date and time data in 24 Hour BCD format. Resetting the Write bit to a "0" then transfers those values the actual TIMEKEEPER counters and allows normal operation to resume. The KS bit, FT bit and the bits marked with zeroes in Figure 5 must be written with zeroes to allow normal TIMEKEEPER and RAM operation.

FIGURE 5. THE MK48T02/12 REGISTER MAP

ADDRESS	DATA								FUNCTION	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
7FF	—	—	—	—	—	—	—	—	YEAR	00-99
7FE	0	0	0	—	—	—	—	—	MONTH	01-12
7FD	0	0	—	—	—	—	—	—	DATE	01-31
7FC	0	FT	0	0	0	—	—	—	DAY	01-07
7FB	KS	0	—	—	—	—	—	—	HOUR	00-23
7FA	0	—	—	—	—	—	—	—	MINUTES	00-59
7F9	ST	—	—	—	—	—	—	—	SECONDS	00-59
7F8	W	R	S	—	—	—	—	—	CONTROL	

KEY: ST = STOP BIT R = READ BIT FT = FREQUENCY TEST
W = WRITE BIT S = SIGN BIT KS = KICK START

Calibrating the Clock

The MK48T02/12 is driven by a quartz crystal controlled oscillator with a nominal frequency of 32768 Hz.The crystal is mounted in the tophat along with the battery. A typical MK48T02/12 is accurate within ±1 minute per month at 25°C without calibration. The devices are tested not to exceed ± 35 ppm (Parts Per Million) oscillator frequency error at 25°C, which comes to about ±1.53 minutes per month. Of course the oscillation rate of any crystal changes with temperature. Figure 6 shows the frequency error that can be expected at various temperatures.

Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The MK48T02/12 design, however, employs periodic counter correction. The calibration circuit adds or subtracts count from the oscillator divider circuit at the divide by 256 stage, as shown in Figure 7. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control register. Adding count speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits in the Control register. The byte can be set to represent any value between 0 and 31 in binary form. The sixth bit is a sign bit; "1" indicates positive calibration, "0" indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened or lengthened by 128 oscillator cycles, that is one tick of the divide by 256 stage. If a binary 1 is loaded into the register, only the first two minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

FIGURE 6. THE MK48T02/12 OSCILLATOR FREQUENCY VS. TEMPERATURE

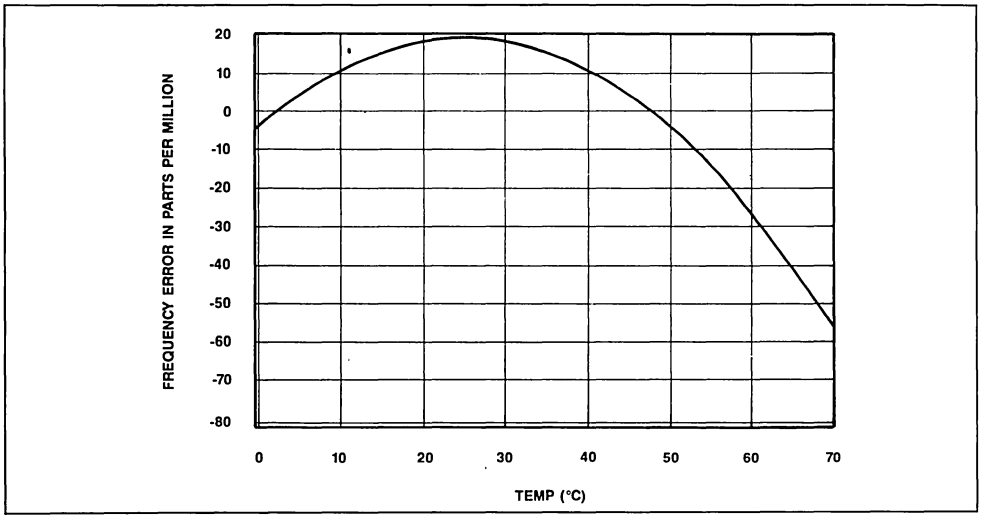
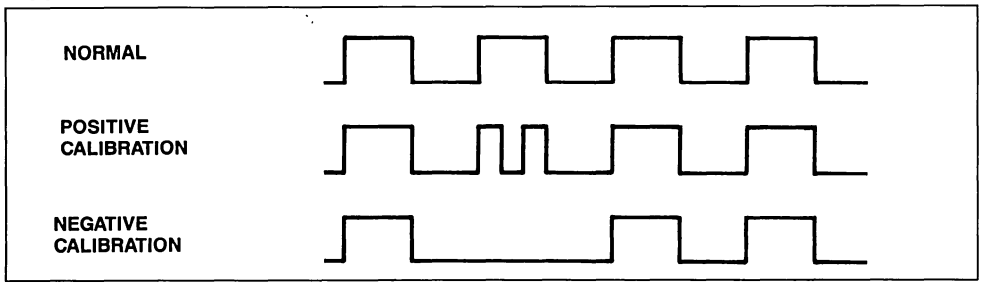


FIGURE 7. ADJUSTING THE DIVIDE BY 256 PULSE TRAIN



Therefore, each calibration step has the effect of adding or subtracting 256 oscillator cycles for every 125,829,120 (32768 x 60 x 64) actual oscillator cycles, that is 2.034 ppm of adjustment per calibration step; giving the user a ± 63.07 ppm calibration range. Assuming that the oscillator is in fact running at exactly 32768 Hz, each of the 31 increments in the Calibration byte would represent 5.35 seconds per month.

Two methods are available for ascertaining how much calibration a given MK48T02/12 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user servioeable enclosure. All the designer has to do is provide a simple utility that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the Day register, is set to a "1", and the oscillator is running at 32768 Hz, the LSB (DQ_0) of the Seconds register will toggle at a 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.00512 Hz would indicate a +10 ppm (1−(512/512.00512)) oscillator frequency error, requiring a −5 (000101_2) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency Test output frequency. The device must be selected and addresses must be stable at Address 7F9 when reading the 512 Hz on DQ_0.

The FT bit must be set using the same method used to set the clock, using the Write bit. The LSB of the Seconds register is monitored by holding the MK48T02/12 in an extended read of the Second register, without having the Read bit set. The FT bit MUST be reset to a "0" for normal clock operations to resume.

Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain from the battery. The "Stop" bit is the MSB of the Seconds register. Setting it to a "1" stops the oscillator. In order to make the oscillator as stingy with current as possible, the oscillator is designed to require an extra "kick" to begin oscillation again. The extra kick is provided by the Kick Start (KS) bit, the MSB of the Hours register. To start the oscillator, implement the following procedure.

1. Set the Write Bit to "1".
2. Reset the Stop Bit to "0".
3. Set the Kick Start Bit to "1".
4. Reset the Write Bit to "0".
5. Wait 2 seconds.
6. Set the Write Bit to "1".
7. Reset the Kick Start Bit to "0".
8. Set the Correct time and date.
9. Reset the Write Bit to "0".

Note: Leaving the KS bit set will cause the Clock to draw excessive current and will shorten battery life.

DATA RETENTION MODE

With V_{CC} applied, the MK48T02/12 operates as a conventional BYTEWIDE static ram. However, V_{CC} is being constantly monitored. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. The MK48T02 has a V_{PFD} (max) -V_{PFD} (min) window of 4.75 volts to 4.5 volts, providing very high data security, particularly when all of the other system components are specified to 5.0 volts plus and minus 10%. The MK48T12 has a V_{PFD} (max) -V_{PFD} (min) window of 4.5 volts to 4.2 volts, allowing users constrained to a 10% power supply specification to use the device.

Note: A mid-write cycle power failure may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time does not exceed t_F. The MK48T02/12 may respond to transient noise spikes that reach into the deselect window if they should occur during the time the device is sampling V_{CC}. Therefore decoupling of power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{BOK}$) flag will be set. The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after first write, and normal RAM operation resumes. Figure 8 illustrates how a $\overline{BOK}$ check routine could be structured.

Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD} (Max). Caution should be taken to keep $\overline{E}$ or $\overline{W}$ high as V_{CC} rises past V_{PFD} (Min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

FIGURE 8. CHECKING THE $\overline{BOK}$ FLAG STATUS

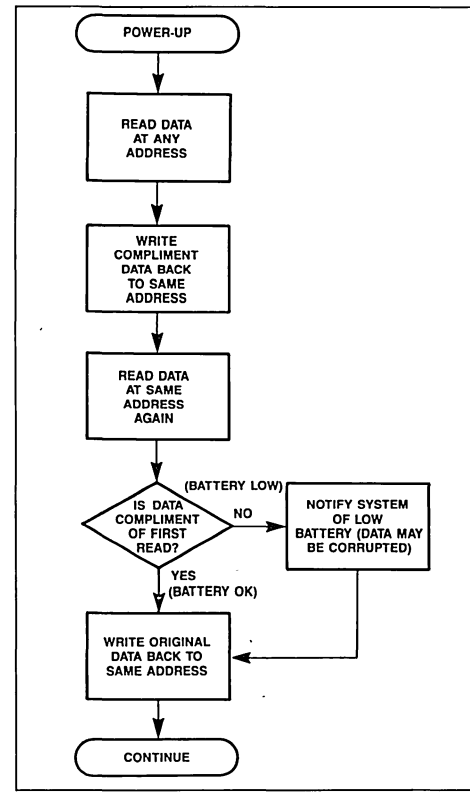
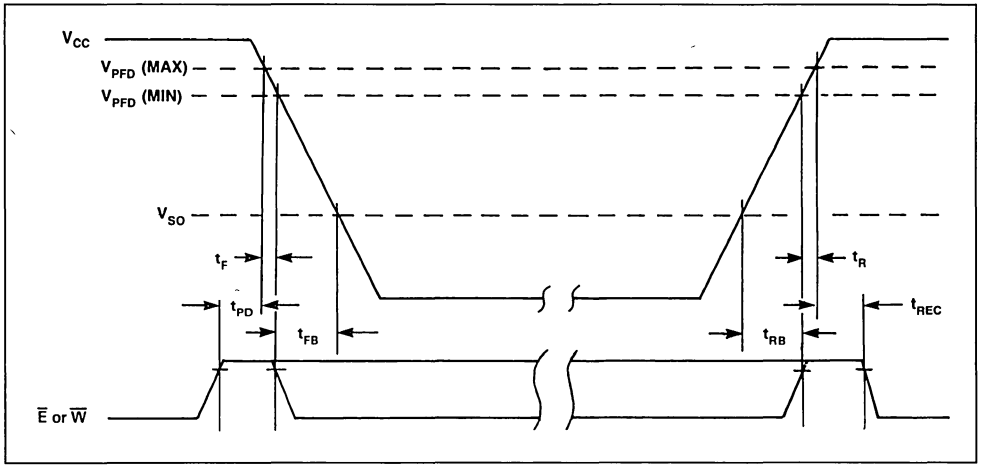


FIGURE 9. POWER-DOWN/POWER-UP TIMING



DC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TRIP POINT VOLTAGES)
($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{PFD}	Power-fail Deselect Voltage (MK48T02)	4.50	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MK48T12)	4.20	4.3	4.50	V	1
V_{SO}	Battery Back-up Switchover Voltage		3		V	1

AC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TIMING)
($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		ns	
t_F	V_{PFD} (Max) to V_{PFD} (Min) V_{CC} Fall Time	300		µs	2
t_{FB}	V_{PFD} (Min) to V_{SO} V_{CC} Fall Time	10		µs	3
t_{RB}	V_{SO} to V_{PFD} (Min) V_{CC} Rise Time	1		µs	
t_R	V_{PFD} (Min) to V_{PFD} (Max) V_{CC} Rise Time	0		µs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	2		ms	

NOTES:
1. All voltages referenced to GND.
2. V_{PFD} (Max) to V_{PFD} (Min) fall times of less t_F may result in deselection/write protection not occurring until 50 µs after V_{CC} passes V_{PFD} (Min). V_{PFD} (Max) to (Min) fall times of less than 10 µs may cause corruption of RAM data or stop the clock.
3. V_{PFD} (Min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data or stop the clock.

CAUTION

Negative undershoots below −0.3 volts are not allowed on any pin while in Battery Back-up mode.

PREDICTING BACK-UP SYSTEM LIFE

The useful life of the battery in the MK48T02/12 is expected to ultimately come to an end for one of two reasons; either because it has been discharged while providing current to an external load; or because the effects of aging render the cell useless before it can actually be discharged. Fortunately, these two effects are virtually unrelated, allowing discharge, or Capacity Consumption and the effects of aging, or Storage Life to be treated as two independent but simultaneous mechanisms, the earlier of which defines Back-up System life.

The current drain that is responsible for Capacity Consumption can be reduced either by applying V_{CC} or turning off the oscillator. With the oscillator off, only the leakage currents required to maintain data in the RAM are flowing. With V_{CC} on, the battery is disconnected from the RAM. Because the leakage currents of the MK48T02/12 are so low, they can be neglected in practical Storage Life calculations. Therefore, application of V_{CC} or turning off the oscillator can extend the effective Back-up System life.

Predicting Storage Life

Figure 10 illustrates how temperature affects Storage Life of the MK48T02/12 battery. As long as V_{CC} is applied or the oscillator is turned off, the life of the battery is controlled by temperature and is virtually unaffected by leakage currents drawn by the MK48T02/12.

Storage Life predictions presented in Figure 10 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's on going battery testing since it began in 1982, we believe the chance of such failure mechanisms surfacing is extremely small. For the purpose of this testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.0 volt closed-circuit voltage across a 250K ohm load resistance.

A Special Note: The summary presented in Figure 10 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final; they can be expected to change as yet more data becomes available. We believe that future read-points of life tests presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 10. They are labeled "Average" ($t_{50\%}$) and ($t_{1\%}$). These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure 10 indicates that a particular MK48T02/12 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience battery failure within 11 years; 50% of them can be expected to fail within 20 years.

The $t_{1\%}$ figure represents the practical onset of wear out, and is therefore suitable for use in what would normally be thought of as a worst-case analysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning on the date of manufacture. Each MK48T02/12 is marked with a four digit manufacturing date code in the form YYWW (Example: 8625 = 1986, week 25).

Calculating Predicted Storage Life of the Battery

As Figure 10 indicates, the predicted Storage Life of the battery in the MK48T02/12 is a function of temperature.

Because the ambient temperature profile is dependent upon application controlled variables, only the user can estimate predicted Storage Life in a given design. As long as ambient temperature is held reasonably constant, expected Storage Life can be read directly from Figure 10. If the MK48T02/12 spends an appreciable amount of time at a variety of temperatures, the following equation should be used to estimate Storage Life.

$$\text{Predicted Storage Life} = \frac{1}{[(TA_1/TT)/SL_1]+[(TA_2/TT)/SL_2]+\ldots+[(TA_n/TT)/SL_n]}$$

Where TA_1, TA_2, TA_n = Time at Ambient Temperature 1, 2, etc.

TT = Total Time = $TA_1 + TA_2 + \ldots + TA_n$

SL_1, SL_2, SL_n = Predicted Storage Life at Temp 1, Temp 2, etc. (See Figure 10).

Example Predicted Storage Life Calculation

A cash register/terminal operates in an environment where the MK48T02/12 is exposed to temperatures of 30°C (86°F) or less for 4672 hrs/yr; temperatures greater than 25°C, but less than 40°C (104°F), for 3650 hrs/yr; and temperatures greater than 40°C, but less than 70°C (158°F), for the remaining 438 hrs/yr.

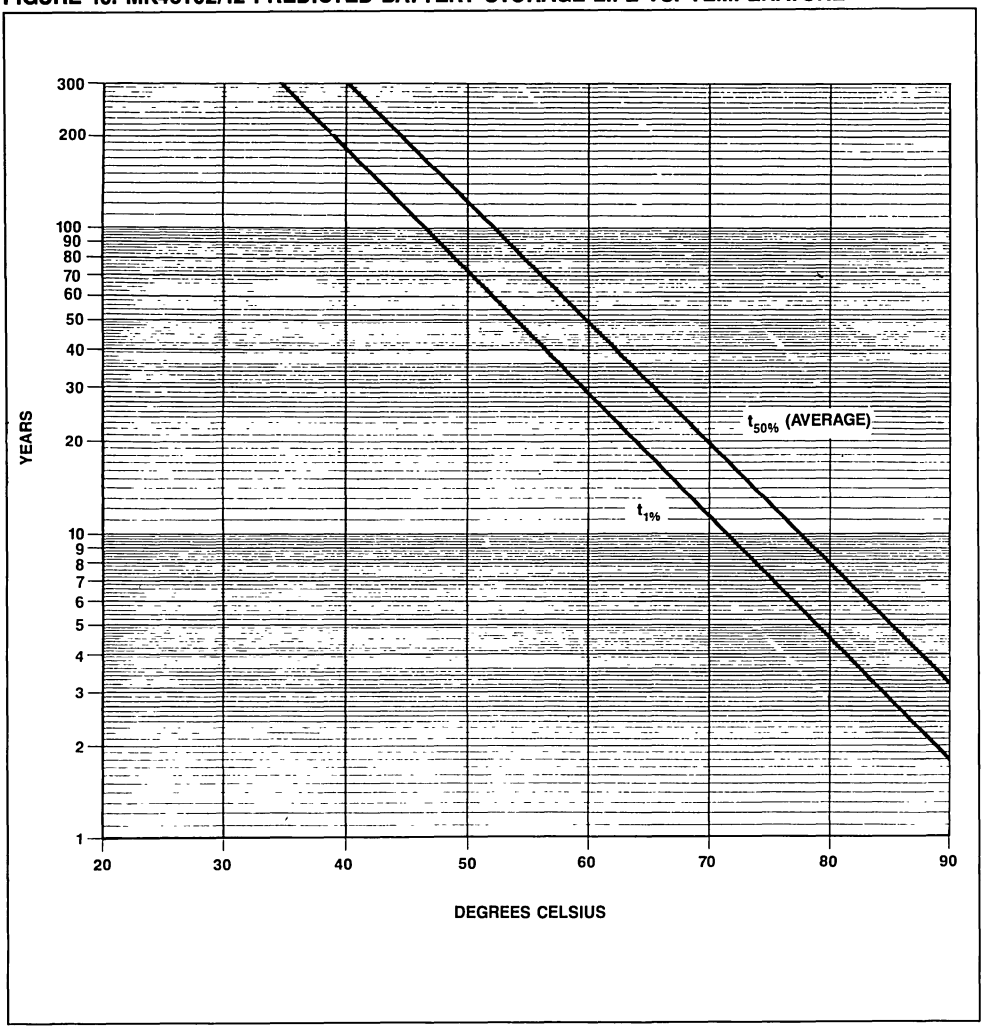
Reading predicted $t_{1\%}$ values from Figure 10; SL_1 = 456 yrs., SL_2 = 175 yrs., SL_3 = 11.4 yrs.

Total Time (TT) = 8760 hrs./yr. TA_1 = 4672 hrs./yr. TA_2 =3650 hrs./yr. TA_3 = 438 hrs./yr.

$$\text{Predicted Typical Storage Life} \geq \frac{1}{[(4672/8760)/456]+[(3650/8760)/175]+[(438/8760)/11.4]}$$

$$\geq 126 \text{ yrs.}$$

FIGURE 10. MK48T02/12 PREDICTED BATTERY STORAGE LIFE VS. TEMPERATURE



Predicting Capacity Consumption Life

The MK48T02/12 internal cell has a minimum rated capacity of 35 mAh. The device places a nominal combined RAM and TIMEKEEPER load of 1.2 μA on a typical internal 37 mAh lithium battery when the clock is running and the device is in Battery Back-up mode. At that rate, the MK48T02/12 will consume the cell's capacity in 29,166 hours, or about 3.3 years. But, as Figure 11 shows, Capacity Consumption can be spread over a much longer period of time.

Naturally, Back-up current varies with temperature. As Figure 12 indicates, the rate of Current Consumption by the MK48T02/12 with the clock running in Battery Back-up mode is a function of temperature.

Because the ambient temperature profile is dependent upon application controlled variables, only the user can estimate consumption rates in a given design. As long as ambient temperature is held reasonably constant, expected Capacity Consumption life can be estimated by reading 0% V_{CC} Duty Cycle Capacity Consumption life directly from Figure 12, and dividing by the expected V_{CC} Duty Cycle (i.e. at 25°C with a 66% Duty Cycle, Capacity Consumption Life = 3.3/(1-.66) = 9.5 years).

If the MK48T02/12 spends an appreciable amount of time at a variety of temperatures, the same equation provided in the previous Storage Life section should be used to estimate Capacity Consumption life.

Example Consumption Life Calculation

Taking the same cash register/terminal used earlier, let's assume that the high and low temperature periods are the non-operating, Battery Back-up mode periods, and that the register is turned on 10 hours a day seven days per week. The two points of interest on the curves in Figure 12 will be the 25°C and the 70°C points.

Reading Capacity Life values from Figure 12; CL_1 = 3.3 yrs., CL_2 = 3.55 yrs.

Total Time (TT) = 8760 hrs./yr. TA_1 = 4672 hrs./yr. TA_2 = 438 hrs./yr.

$$\text{Capacity Life} \geq \frac{1}{[(4672/8760)/3.3]+[(438/8760)/3.55]}$$

$$\geq 5.69 \text{ yrs.}$$

Estimating Back-up System Life

The procedure for estimating Back-up System Life is simple. Pick the lower of the two numbers. In the case calculated in the examples, that would be 5.69 years.

The fact is, since either mechanism, Storage Life or Capacity Consumption, can end the system's life, the end is marked by whichever occurs first.

FIGURE 11. TYPICAL CAPACITY CONSUMPTION LIFE AT 25°C VS. V_{CC} DUTY CYCLE

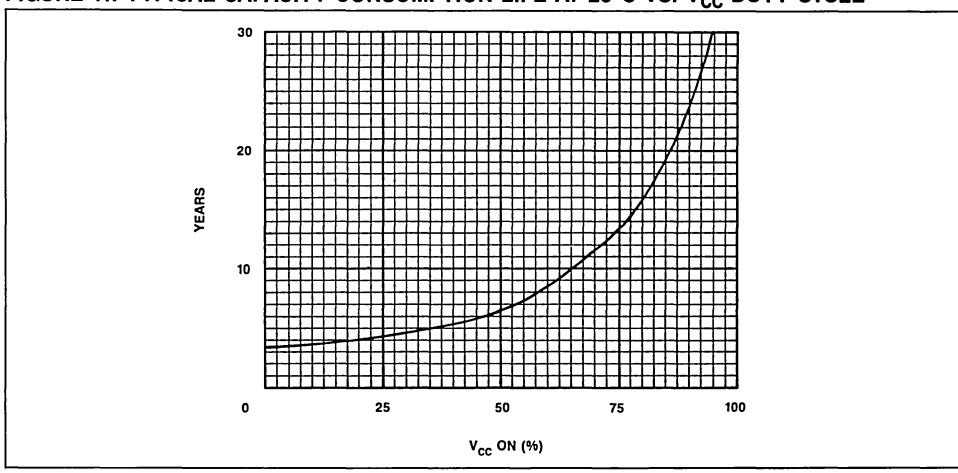
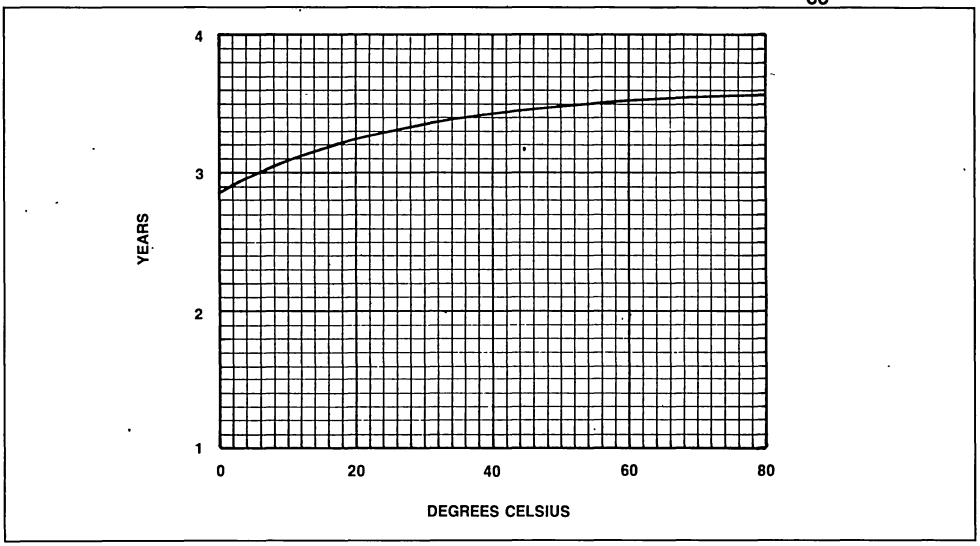


FIGURE 12. CURRENT CONSUMPTION LIFE OVER TEMPERATURE WITH 0% V_{CC} DUTY CYCLE



APPLICATION NOTE:

BINARY TO BCD, AND BCD TO BINARY CONVERSION

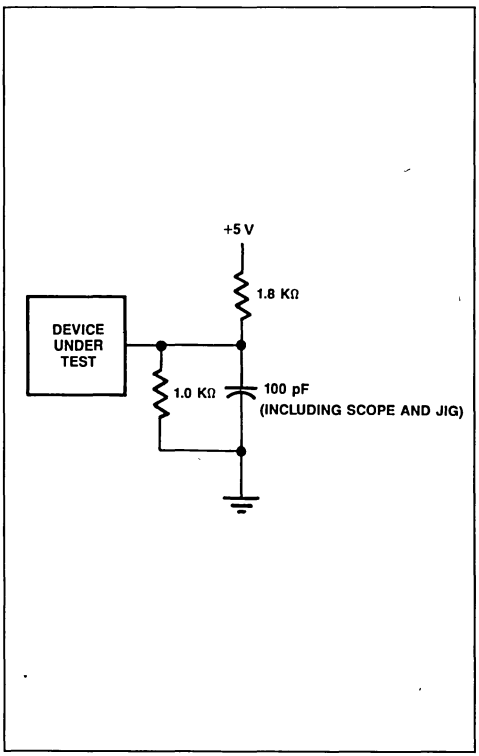
The MK48T02/12 presents and accepts TIMEKEEPER data in BCD format. Conversion to or from other formats can be executed in a single line of code, as the following example BASIC program demonstrates.

```
10 REM  BINARY TO BCD
20 DEF  FNA (X)=INT (X/10)*16+X-INT
        (X/10)*10
30 REM  BCD TO BINARY
40 DEF  FNB (X)=INT (X/16)*10+(XAND15)
```

AC TEST CONDITIONS

Input Levels:	0.6 V to 2.4 V
Transition Times:	5 ns
Input and Output Timing Reference Levels	0.8 V or 2.2 V

FIGURE 13. EQUIVALENT OUTPUT LOAD DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Pin Relative To GND ..... −0.3 V to +7.0 V
Ambient Operating (V_{CC} On) Temperature (T_A) ..... 0°C to +70°C
Ambient Storage (V_{CC} Off, Oscillator Off) Temperature ..... −20°C to +70°C
Total Device Power Dissipation ..... 1 Watt
Output Current Per Pin ..... 20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS
($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage (MK48T02)	4.75	5.50	V	1
V_{CC}	Supply Voltage (MK48T12)	4.50	5.50	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3 V	V	1
V_{IL}	Logic "0" Voltage All Inputs	−0.3	0.8	V	1,2

DC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq +70°C$) (V_{CC} (Max) $\geq V_{CC} \geq V_{CC}$ (Min))

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	3
I_{CC2}	TTL Standby Current ($\overline{E} = V_{IH}$)		5	mA	4
I_{CC3}	CMOS Standby Current ($\overline{E} = V_{CC}-0.2$ V)		3	mA	4
I_{IL}	Input Leakage Current (Any Input)	−1	+1	µA	5
I_{OL}	Output Leakage Current	−5	+5	µA	5
V_{OH}	Output Logic "1" Voltage (I_{OUT} = −1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 2.1 mA)		0.4	V	

CAPACITANCE (T_A = 25°C)

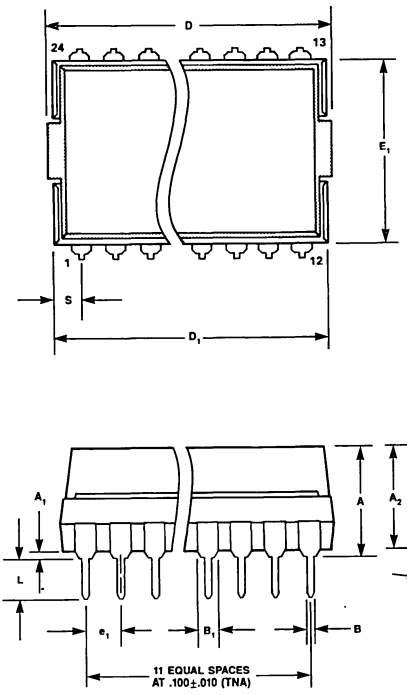
SYM	PARAMETER	MAX	NOTES
C_I	Capacitance on all pins (except D/Q)	7 pF	6
$C_{D/Q}$	Capacitance on D/Q pins	10 pF	6,7

NOTES
1. All voltages referenced to GND.
2. Negative spikes of −1.0 volts allowed for up to 10 ns once per cycle.
3. I_{CC1} measured with outputs open.
4. Measured with Control Bits set as follows: R = 1; W, ST, KS, FT = 0.
5. Measured with $GND \leq V_I \leq V_{CC}$ and outputs deselected.
6. Effective capacitance calculated from the equation $C = \frac{I\Delta t}{V\Delta}$ with ΔV = 3 volts and power supply at 5.0 V.
7. Measured with outputs deselected.

PACKAGE DESCRIPTION

B PACKAGE 24 PIN

	Dim.	mm		inches		Notes
		Min	Max	Min	Max	
BATTERY ONLY	D	—	32.893	—	1.295	
	Z	13.97	14.478	.550	.570	
	A	8.128	9.652	.320	.380	
	A_2	7.62	9.144	.300	.360	
	E_1	13.462	13.97	.530	.550	
	B	0.381	0.533	.015	.021	4
	B_1	1.143	1.778	.045	.070	
	C	0.203	0.355	.008	.014	4
24 PIN PLASTIC D.I.P. ONLY	D_1	—	32.258	—	1.270	1
	E	13.462	16.256	.530	.640	
	e_A	15.24	17.78	.600	.700	3
	e_1	2.286	2.794	.090	.110	
	L	3.048	3.81	.120	.150	
	A_1	0.381	0.762	.015	.030	2
	S	1.524	2.286	.060	.090	.



NOTES:
1 Overall length includes .010 in flash on either end of the package
2 Package standoff to be measured per JEDEC requirements
3 Measured from centerline to centerline at lead tips
4 When the solder lead finish is specified, the maximum limit shall be increased by .003 in

ORDERING INFORMATION

MK48T	X	2	B	-XX
DEVICE FAMILY	V_{CC} RANGE		PACKAGE	SPEED

-12 120 NS ACCESS TIME
-15 150 NS ACCESS TIME
-20 200 NS ACCESS TIME
-25 250 NS ACCESS TIME

B PLASTIC WITH BATTERY TOP HAT

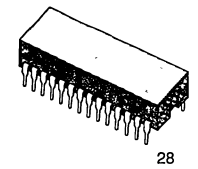
0 +10%/–5%
1 +10%/–10%

SGS-THOMSON MICROELECTRONICS

MK48T08/18(B) -10/15/20

TIMEKEEPER™ 8 K X 8 ZEROPOWER™ RAM

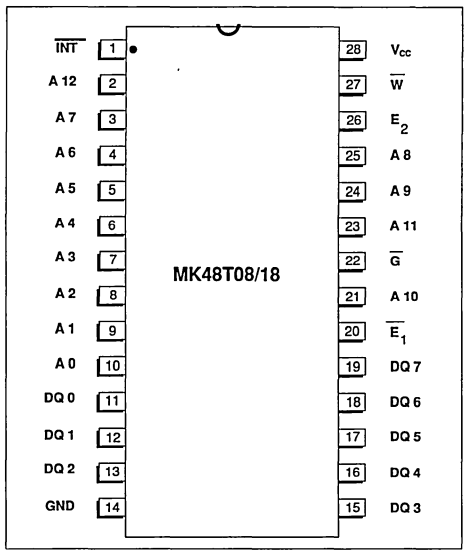
- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK, CRYSTAL, POWER-FAIL CONTROL CIRCUIT AND BATTERY.
- BYTEWIDE™ RAM-LIKE CLOCK ACCESS.
- BCD CODED YEAR, MONTH, DAY DATE, HOURS, MINUTES AND SECONDS.
- SOFTWARE CONTROLLED CLOCK CALIBRATION FOR HIGH ACCURACY APPLICATIONS.
- PREDICTED WORST CASE BATTERY LIFE OF 10 YEARS @ 70°C.
- PIN FUNCTION COMPATIBLE WITH JEDEC STANDARD 8K X 8 SRAMS.
- AUTOMATIC POWER-FAIL CHIP DESELECT/WRITE PROTECTION.
- CHOICE OF TWO WRITE PROTECT VOLTAGES:
  MK48T08 - $4.50 \leq V_{PFD} \leq 4.70$
  MK48T18 - $4.20 \leq V_{PFD} \leq 4.50$



B

DIP-28
(Plastic with Battery Top Hat)

PIN CONNECTIONS



PIN NAMES

A0-A12	Address Input	Vcc	+5Volts
$\overline{E1}$	Chip Enable	$\overline{W}$	Write Enable
E2	Chip Enable	$\overline{G}$	Output Enable
GND	Ground	DQ0-DQ7	Data In/Data Out
NC	No Connection	$\overline{INT}$	Power Fail Interrupt

Part Number	Access Time	R/W Cycle Time
MK48TX8-10	100 ns	100 ns
MK48TX8-15	150 ns	150 ns
MK48TX8-20	200 ns	200 ns

DESCRIPTION

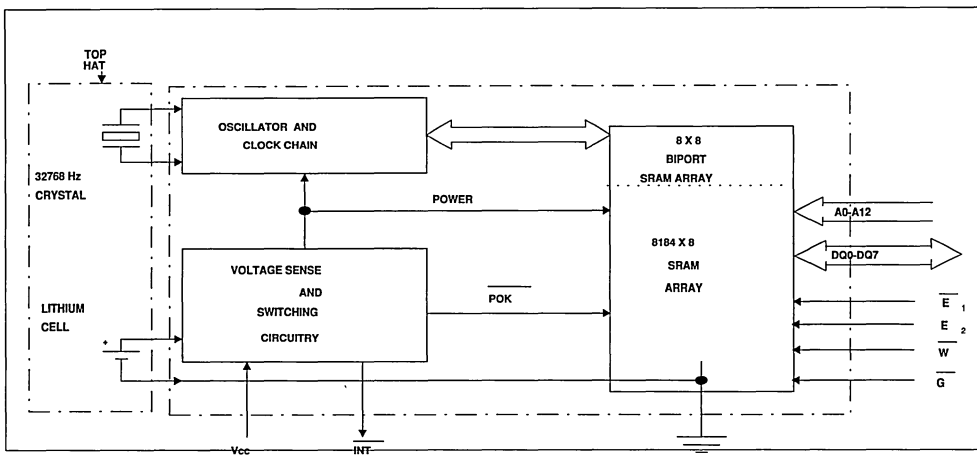
The MK48T08/18 combines an 8K x 8 full CMOS SRAM, a BYTEWIDE accessible real time clock, a crystal and a long life lithium carbon mono-fluoride battery in a single plastic DIP package. The MK48T08/18 is a non-volatile pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many EPROM and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing, or limitations on the number of writes that can be performed.

Access to the clock is as simple as conventional BYTEWIDE RAM access because the RAM and the clock are combined on the same die. As Figure 1 indicates, the TIMEKEEPER registers are located in the upper eight locations of the RAM. The registers contain, beginning at the top; year, month, date, day, hour, minutes, and seconds data in 24 hour BCD format. Corrections for 28, 29 (Leap Year), 30 and 31 day months are made automatically. The eighth location is a control register. These registers are not the actual clock counters; they are BiPORT read/write Static RAM memory locations. The MK48T08/18 includes a clock control circuit that, once every second, dumps the counters into the BiPORT RAM.

Because the Clock Registers are constructed using BiPORT memory cells, access to the rest of the RAM proceeds unhindered by updates to the TIMEKEEPER registers, even if the TIMEKEEPER registers are being updated a the very moment another location in the memory array is accessed.

The MK48T08/18 also has its own Power-fail Detect circuit. The circuit deselects the device when ever Vcc below tolerance, providing a high degree of data security in the midst of unpredictable system operations brought on by low Vcc.

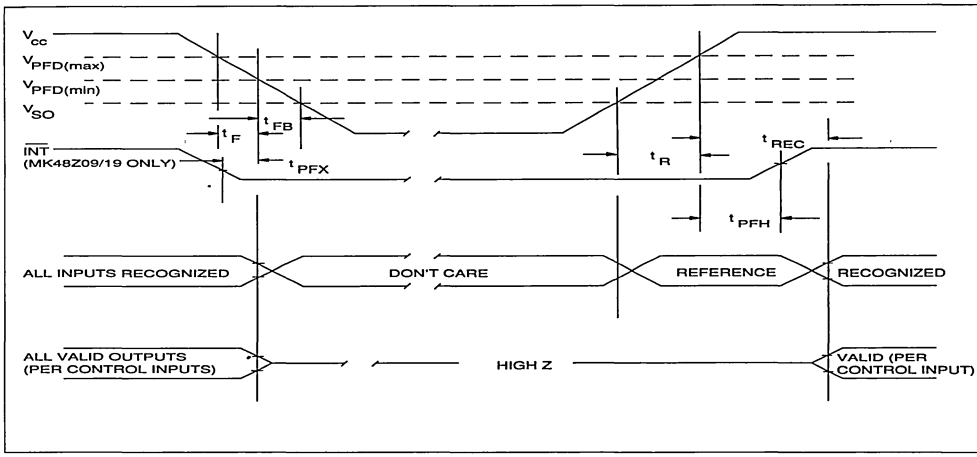
FIGURE 1 : MK48T08 BLOCK DIAGRAM



TRUTH TABLE (MK48T08/18)

Vcc	$\overline{E}_1$	E_2	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
< Vcc (Max)	V_{IH}	X	X	X	Deselect	High Z	Standby
	X	V_{IL}	X	X	Deselect	High Z	Active
	V_{IL}	V_{IH}	X	V_{IL}	Write	DIN	Active
> Vcc (Min)	V_{IL}	V_{IH}	V_{IL}	VIH	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD} (Min) > V_{SO}	X	X	X	X	Deselect	High Z	CMOS Standby
≤ V_{SO}	X	X	X	X	Deselect	High Z	Battery Back-up Mode

FIGURE 2 : POWER DOWN/POWER UP TIMING.



AC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TIMING) (0°C ≤ T_A ≤ + 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		µS	
t_F	V_{PFD} (Max) to V_{PFD} (Min) Vcc Fall Time	300		µS	2
t_{FB}	V_{PFD} (Min) to V_{SO} V_{CC} Fall Time	10		µS	3
t_R	V_{SO} to V_{PFD} (Max) V_{CC} Rise Time	1		µS	
t_{REC}	$\overline{E_1}$ or $\overline{W}$ at V_{IH} or E_2 at V_{IL} after Power Up	1		mS	
t_{PFX}	$\overline{INT}$ Low to Auto Deselect	10	40	µS	
t_{PFH}	V_{PFD} (Max) to $\overline{INT}$ High		120	µS	4

DC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TRIP POINTS) (0°C ≤ T_A ≤ +70°C)

		VALUE				
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{PFD}	Power-fail Deselect Voltage (MK48T08/09)	4.5	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MK48T18/19)	4.2	4.3	4.5	V	1
V_{SO}	Battery Back-up Switchover Voltage		3.0		V	1
t_{DR}	Expected Data Retention Time	11			YEARS	

NOTES :

1. All voltages referenced to GND.

2. V_{PFD} (MAX) to V_{PFD} (MIN) fall time of less than $t_F$may result in deselection/write protection not occuring until 200 µS after Vcc passes V_{PFD} (MIN). V_{PFD} (MAX) to (MIN) fall times of less than 10 µS may cause coruuption of RAM data.

3.V_{PFD} (MIN) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

4. $\overline{INT}$ may go high anytime after Vcc exceeds V_{SO} and is guaranteed to go high t_{PFH} after Vcc exceeds V_{PFD} (MAX).

READ MODE

The MK48T08/18 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high, $\overline{E}_1$ is low, and E_2 is high. Access Time (t_{GLQV}). The state of the eight three-state Data I/O signals is controlled by Chip Enable and $\overline{G}$. If the Outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address inputs are changed while Chip Enable and $\overline{G}$ remain low, output data will remain valid for Output Hold from Address (t_{AXQX}) but will go indeterminate until the next Address Access.

The device architecture allows ripple through access of data from eight of 65,536 locations in the static storage array. Thus, the unique address specified by the 13 Address inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} after the last address input signal is stable, providing that the Chip Enable and $\overline{G}$ access times are satisfied.

If Chip Enable or $\overline{G}$ access times are not yet met, valid data will be available at the latter of Chip Enable Access Time (t_{ELQV}) or at Output Enable

AC ELECTRICAL CHARACTERISTICS (READ CYCLE) (0°C ≤ T_A ≤ +70°C (Vcc (min) ≤ Vcc≤ Vcc(Max))

		48TX8-10		48TX8-15		48TX8-20			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT	NOTE
t_{E1LQX}	Chip Enable 1 to Q low-Z	10		10		10		ns	
t_{E2HQX}	Chip Enable 2 to Q low-Z	10		10		10			
t_{AXQX}	Output Hold from Address	5		5		5			
t_{GLQX}	Ouput Enable 1 to Q low-Z	5		5		5			
t_{AVAV}	Read Cycle Time	100		150		200			
t_{AVQV}	Address Access Time		100		150		200		
t_{E1LQV}	Chip, Enable 1 Access Time		100		150		200		
t_{E2HQV}	Chip, Enable 2 Access Time		100		150		200		
t_{GLQV}	Output Enable Access Time		50		75		100		
t_{E1HQZ}	Chip Enable 1 to Q High-Z		50		75		100		
t_{E2LQZ}	Chip Enable 2 to Q High-Z		50		75		80		
t_{GHQZ}	Output Disable to Q High-Z		40		60		80		

FIGURE 3 : READ TIMING N° .1 (ADDRESS ACCES)

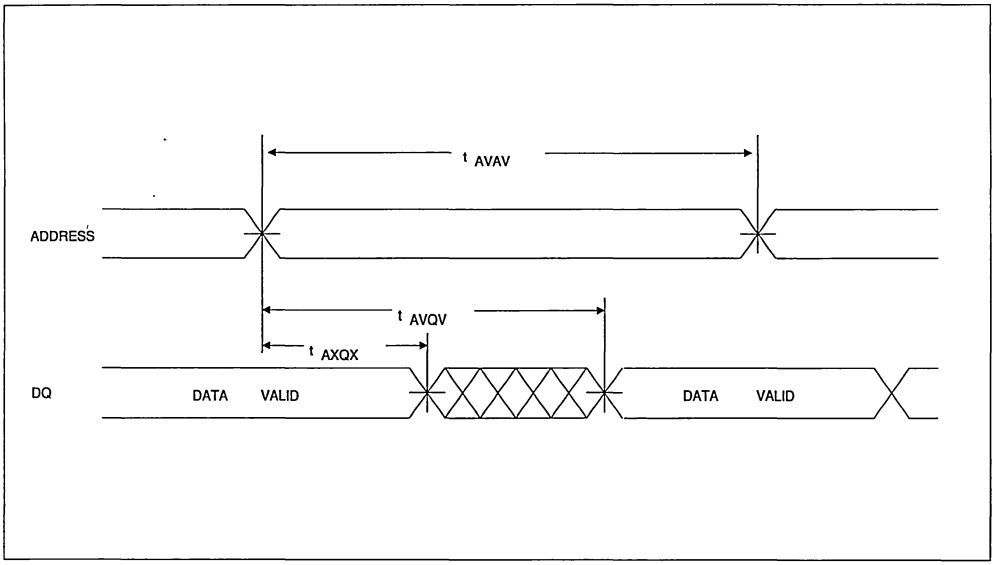
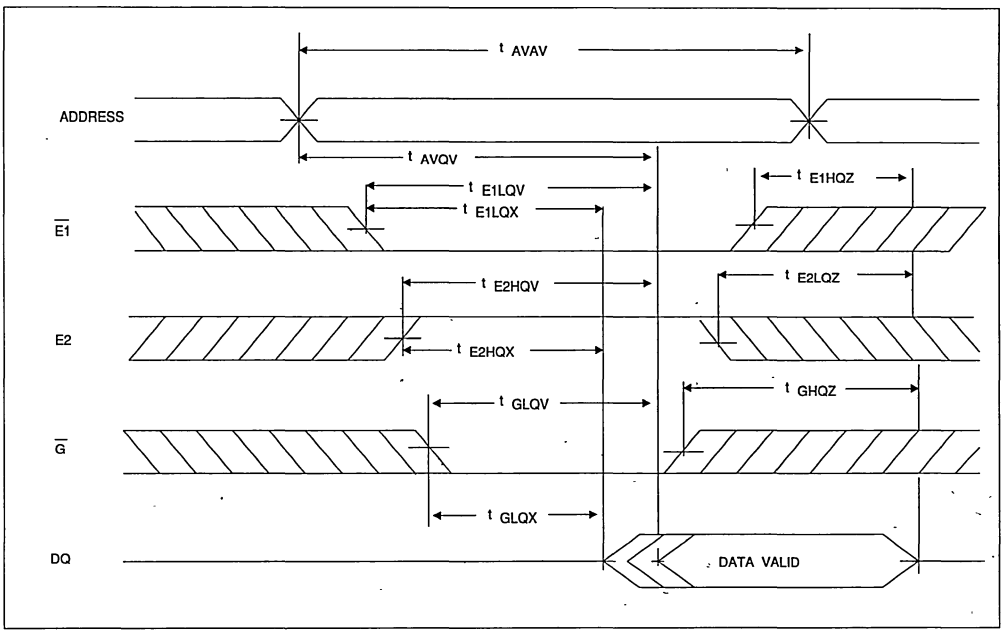


FIGURE 4 : aREAD TIMING N°.2



WRITE MODE

The MK48T08/18 is in the Write Mode whenever Write Enable and Chip Enable are active. The start of a write is referenced to the latter occurring falling edge of w or e1 or rising edge of e2 . a write is terminated by the earlier rising edge of w or e1, or the falling edge of e2. the addresses must be held valid throughout the cycle. e1 or wmust return high or e2 low for minimum of te1hax or t_{E2LAX} prior to the initiation of another read or write cycle. Data-in must be valid t_{DVEH} prior to the end of write and remain valid for t_{WHDX} afterward.

Because $\overline{G}$ is a Don't Care in the Write Mode and a low on $\overline{W}$ will return the outputs to High-Z, $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE) (0°C ≤ T_A ≤ +70°C (Vcc (min) ≤ Vcc ≤ Vcc (max))

		48TX8-10		48TX8-15		48TX8-20			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTE
t_{AVWL}	Address Set-Up Time	0		0		0		ns	
t_{AVE1L}	Address Set-Up Time to ChipEnable	0		0		0			
t_{AVE2H}		0		0		0			
t_{E1HAX}	Write recovery from Chip Enable (Address Hold Time)	10		10		10			2
t_{E2LAX}		10		10		10			2
t_{WHDX}	Data Hold Time	5		5		5			1,2
t_{AVAV}	WriteCycle Time	100		150		200			
t_{AVWH}	Address Valid to $\overline{W}$ High	80		130		180			
t_{WLWH}	Write Pulse Width	80		100		150			
t_{WHAX}	Address Hold after End of Write	10		13		10			1
t_{E1L1H}	Chip Enable Active to End of Write (W High)	80		130		180			2
t_{E2HE2L}		80		130		180			2
t_{DVWH}	Data Valid to End of Write	50		70		80			1,2
t_{WLQZ}	$\overline{W}$ Low to Q High-Z		50		75		100		

NOTES :

1. In a $\overline{W}$ Controlled Cycle
2. In a $\overline{E}_1$, E2 Controlled Cycle

FIGURE 5 : WRITE CONTROL CYCLE TIMING

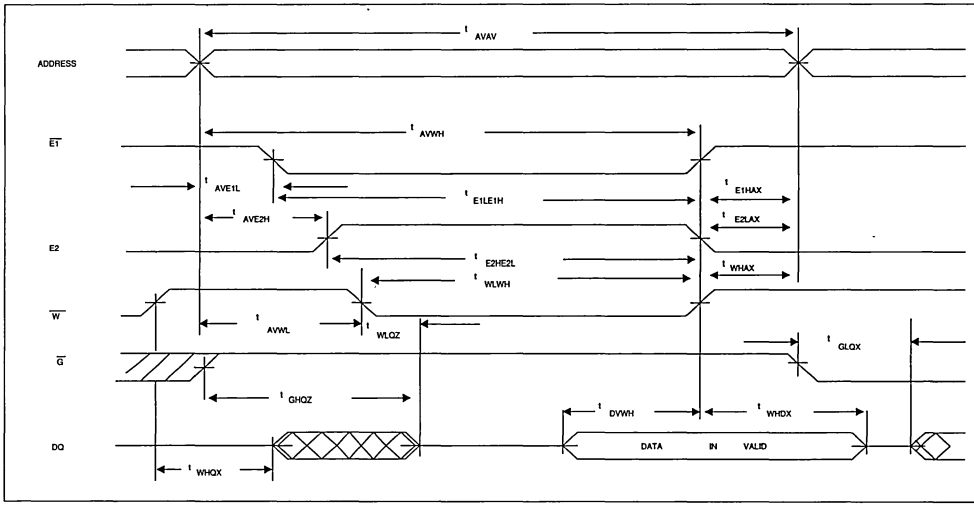
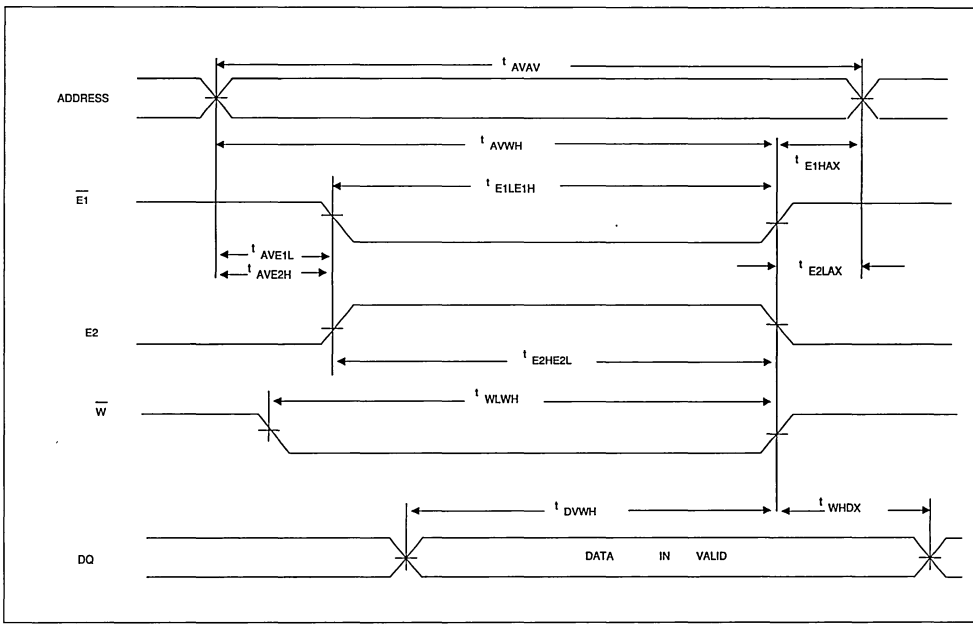


FIGURE 6 : CHIP ENABLE CONTROL WRITE CYCLE TIMING



DATA RETENTION MODE

With V_{CC} applied, the MK48T08/18 operates as a conventional BYTEWIDE static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window.

Note: A mid-write cycle power failure may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The MK48T08/18 may respond to transient noise spikes that reach into the deselect window if this should occur during the time the device is sampling V_{CC}. Therefore decoupling of the power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max). Caution should be taken to keep E_1 high or E_2 low as Vcc rises past V_{PFD} (Min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

POWER FAIL INTERRUPT

The MK48T08/18continuously monitors Vcc. When Vcc fall to the power fail detect trip point of the MK48Z09/19 an interrupt is immediatly generated. An internal clock provides a delay no less than 10µS but no greater than 40µS before automatically deselecting the MK48T08/18.

PREDICTING BACK-UP SYSTEM LIFE

The useful life of the battery in the MK48T08/18 is expected to ultimately come to an end for one of two reasons: either because it has been discharged while providing current to an external load; or because the effects of aging render the cell useless before it can actually be discharged. Fortunately, these two effects are virtually unrelated, allowing discharge, or Capacity Consumption, and the effects of aging, or Storage Life, to be treated as two independent but simultaneous mechanisms, the earlier of which defines Back-up System life.

With V_{CC} on, the battery is disconnected from the RAM and aging effects become the determining factor in battery life. With V_{CC} off, leakage currents in the RAM provide the only load on the Battery during battery back-up. For the MK48T08/18the leakage currents are so low that the Back-up System life of the device is simply the Storage Life of the cell. The Storage Life of the cell is a function of temperature.

PREDICTING STORAGE LIFE

Figure 7 illustrates how temperature affects Storage Life of the MK48T08/18 battery. The life of the battery is controlled by temperature and is virtually unaffected by leakage currents drawn by the MK48T08/18.

Storage Life predictions presented in Figure 7 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's on going battery testing since it began in 1982, we believe the chance of such failure mechanisms surfacing is extremely small. For the purpose of the testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.4 volt closed-circuit voltage across a 250K load resistance.

A Special Note: The summary presented in Figure 7 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final; they can be expected to change as yet more data becomes available. We believe that future read points of life test presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 7. The are labeled "Average" ($t_{50\%}$) and ($t_{1\%}$). These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure 7 indicates that a particular MK48T08 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience a battery failure within 11 years; 50% of them can be expected to experience a failure within 20 years.

The $t_{1\%}$ figure represents the practical onset of wear out, and is therefore suitable for use in what would normally be thought of as a worst-case analysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning at the date of manufacture. Each MK48T08/18 is marked with a five digit manufacturing date code in the form XYYWW. The first digit is the assembly location code (example: 98625= assembled in Muar Malasia, 1986, week 25).

Calculating Predicted Storage Life of the Battery

As Figure 7 indicates, the predicted Storage Life of the battery in the MK48T08/18 is a function of temperature.

Because the ambient temperature profile is dependent upon application controlled variables, only the user can estimate predicted Storage Life in a given design. As long as ambient temperature is held reasonably constant, expected Storage Life can be read directly from Figure 7. If the MK48T08/18 spends an appreciable amount of time at a variety

Example Predicted Storage Life Calculation

Predicted Storage Life = $1 \div \{ [(TA_1 \div TT) \div SL_1] + [(TA_2 \div TT) \div SL_2] + ... + [(TA_N \div TT) \div SL_N] \}$

Where TA_1, TA_2, TA_N, = Time at Ambient Temperature 1, 2, etc.

$TT = \text{Total Time} = TA_1 + TA_2 + ... + TA_N$

SL_1, SL_2, SL_N = Predicted Storage Life at Temp. 1, Temp. 2, etc. (See Figure 7)

Example Predicted Storage Life Calculation

A cash register/terminal operates in an environment where the MK48T08 is exposed to temperatures of 55°C or less for 8322 hrs./yr.; and temperatures greater than 60°C, but less than 70°C, for the remaining 438 hrs./yr.

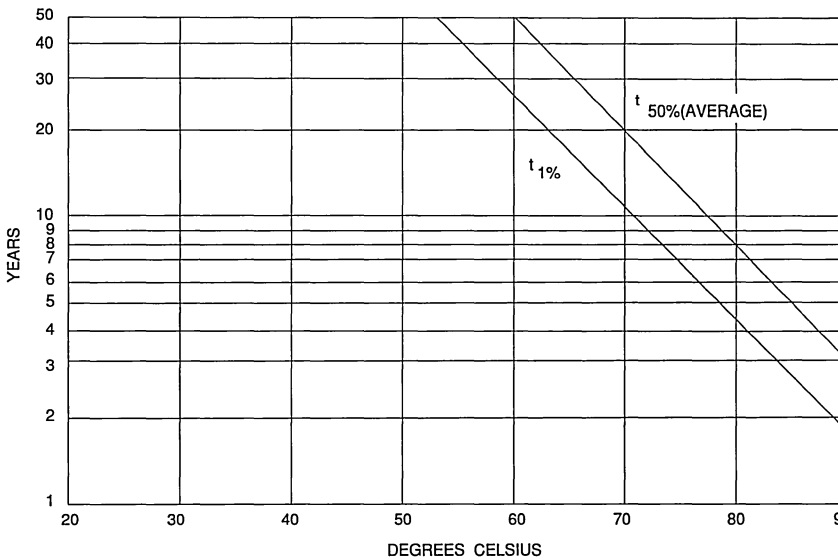
Reading Predicted $t_{1\%}$ values from Figure 7; $SL_1 = 41$ yrs., $SL_2 = 11.4$ yrs.,

Total Time (TT) = 8760 hrs./yr. $TA_1 = 8322$ hrs./yr. $TA_2 = 438$ hrs./yr. .

Predicted Typical Storage Life $\geq 1 \div \{ [(8322 \div 8760) \div 41] + [(438 \div 8760) \div 11.4]$

Predicted Typical Storage Life $\geq$ 36 years

FIGURE 7 : PREDICTED BATTERY STORAGE LIFE VS. TEMP.



Calculing Predicted Capacity Consumption

The MK48T08/18 internal cell has a minimum rated capatity of 35MAh.The device places a nominal RAM and TIMEKEEPER load pof less than 400nA over the operating temperature range. At this rate, the Capacity Consumption life is 35E-3/400E-9=87500 hours or about 10 Years.The Capacity Consumption life can be extended by applying Vcc or turning off the oscillator run 100% of the time butr Vcc is applied 60% of the time, the Capacity Consumption life is 10/(1-.6) = 25 years.

Estimated back-up System Life

Since either Storahge or Capacity Consumption can end the Battery's life, System Life is marked which-ever occurs first.

CLOCK OPERATIONS

Reading the Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading of data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual counter, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a "1" is written into the "Read" bit, the seventh most significant bit in the Control Register. As long as a "1" remains in that position, updating is halted. After a Halt is issued, the registers reflect the count, that is the day, date, and time that were current at the moment the Halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A Halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a "0".

Setting the Clock

The eighth bit of the Control register is the "Write" bit. Setting the Write bit to a "1", like the Read bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date and time data in 24 Hour BCD format. Resetting the Write bit to a "0" then transfers those values to the actual TIMEKEEPER counters and allows normal operation to resume.

Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain from the battery. The "Stop" bit is the MSB for the Seconds Register. Setting it to a "1" stops the oscillator.

FIGURE 8 : THE MK48T08/18 REGISTER MAP

ADDRESS	DATA								FUNCTION	
	D7	D6	D5	D4	D3	D2	D1	D0		
1FFF	--	--	--	--	--	--	--	--	YEAR	00-99
1FFE	X	X	X	--	--	--	--	--	MONTH	01-12
1FFD	X	X	FT	--	--	--	--	--	DATE	01-31
1FFC	X	X	X	X	X	--	--	--	DAY	01-07
1FFB	X	X	--	--	--	--	--	--	HOUR	00-23
1FFA	X	--	--	--	--	--	--	--	MINUTES	00-59
1FF9	ST	--	--	--	--	--	--	--	SECONDS	00-59
1FF8	W	R	S	--	--	--	--	--	CONTROL	

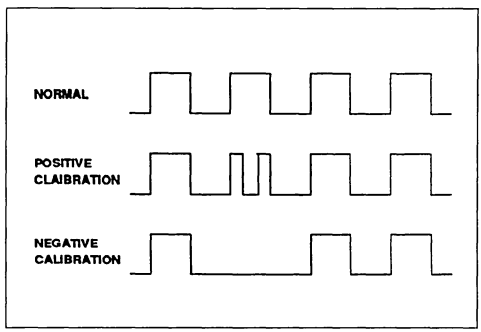
ST = STOP BIT
W = WRITE BIT
R = READ BIT
S = SIGNBIT
FT = FREQUENCY TEST
X = UNUSED

Calibrating the Clock

The MK48T08/18 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The crystal is mounted in the tophat along with the battery. A typical MK48T08/18 is accurate within ±1 minute per month at 25°C without calibration. The devices are tested not to exceed 35 PPM (parts per million) oscillator frequency error at 25°C, which equates to about ± 1.53 minutes per month. Of course the oscillation rate of any crystal changes with temperature. Figure 8 shows the frequency error that can be expected at various temperatures.

Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The MK48T08/18 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 128 stage, as shown in Figure 7. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

FIGURE 9



The Calibration byte occupies the five lower order bits in the Control register. This byte can be set to represent any value between 0 and 31 in binary form. The sixth bit is a sign bit; "1" indicates positive calibration, "0" indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary "1" is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

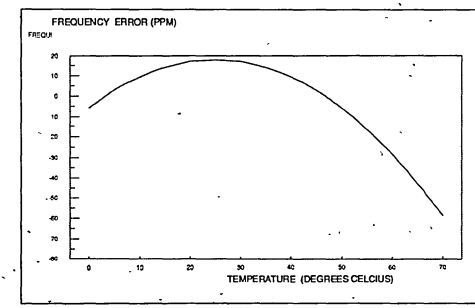
Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or -2.034 PPM of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or - 5.35 seconds per month.

Two methods are available for ascertaining how much calibration a given MK48T08/18 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the day Register, is set to a "1", and the oscillator is running at 32,768 Hz, the LSB (DQ0) of the Seconds Register will toggle at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 PPM oscillator frequency error, requiring a -10(001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency. The device must be selected and addresses must stable at Address 1FF9 when reading the 512 Hz on DQ0.

The FT bit must be set using the same method used to set the clock, using the write bit. The LSB of the Seconds Register is monitored by holding the MK48T08/18 in an extended read of the Seconds Register, without having the Read bit set. The FT bit MUST be reset to "0" for normal clock operations to resume.

FIGURE 10 : FREQUENCY ERROR



ABSOLUTE MAXIMUM RATINGS *

PARAMETER	VALUE	UNIT
Total Power Dissipation	1.0	W
Output Current per Pin	20	mA
Voltage on any Pin Relative to GND	-0.3 to + 7.0	V
Ambient Operating (Vcc on) Temperature (T_A)	0 to 70	°C
Ambient Storage (Vcc off) Temperature	-40 to +85	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is net implied. Exposure to the absolute maximum ratings conditions for extended periods of t ime may affect reliability.

CAUTION
Negative undershoots below -0.3 volts are not allowed on any pin while in the Battery Back-up mode.

RECOMMENDED DC OPERATING CONDITIONS (0°C≤ T_A ≤ +70°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
Vcc	Supply Voltage (MK48T08/09)	4.75	5.5	V	1
Vcc	Supply Voltage (MK48T18/19)	4.5	5.5	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	Vcc + 0.3v	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3	0.8	V	1,2

DC ELECTRICAL CHARACTERISTICS (0°C≤ T_A ≤+70°C) (Vcc (min) ≤ Vcc ≤ Vcc (max))

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
Icc1	Average Vcc Power Supply Current		80	mA	3
Icc2	TTL Standby Current ($\overline{E}_1$= V_{IH} or $\overline{E}$2=V_{IL})		3	mA	
Icc3	CMOS Standby Current ($\overline{E}_1$= Vcc -0.2v)		3	mA	4
I_{IL}	Input Leakage Current (Any Input)	-1	+1	µA	5
I_{OL}	Ouput Leakage Current	-5	+5	µA	5
V_{OH}	Output Logic "1" Voltage (I_{OUT} =-1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +2.1 mA)		0.4	V	
V_{INT}	$\overline{INT}$ Logic "0" Voltage (I_{OUT} = +0.5 mA)		0.4	V	

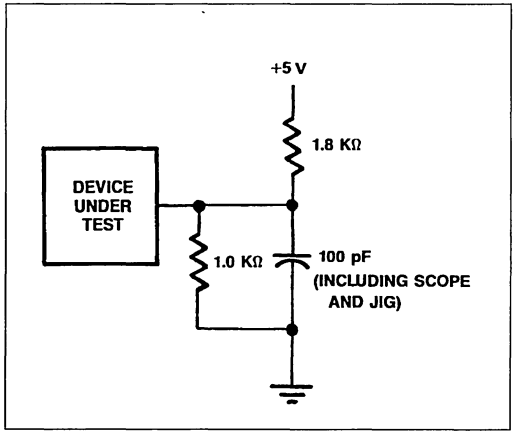
NOTES :

1. All voltages referenced to GND.
2. Negative spikes of -1.0 volts allowed for up to 10 ns once per Cycle.
3. I_{CC1} measured with outputs open.
4. 1mA typical.
5. Measured with Vcc ≥ V_I ≥ GND and outputs deselected.

AC TEST CONDITIONS

INPUT LEVELS	0.0v to 3.0v
TRANSITION TIMES:	5nS
INPUT AND OUTPUT TIMING REFERENCE LEVELS	1.5v

FIGURE 11 : OUPUT LOAD DIAGRAM



CAPACITANCE (T_A = 25°C)

SYMBOL	PARAMETER	MAX	UNITS	NOTES
CI	capacitance on all pins (except DQ)	10.0	pF	1
CDQ	capacitance on DQ pins	10.0	pF	1,2

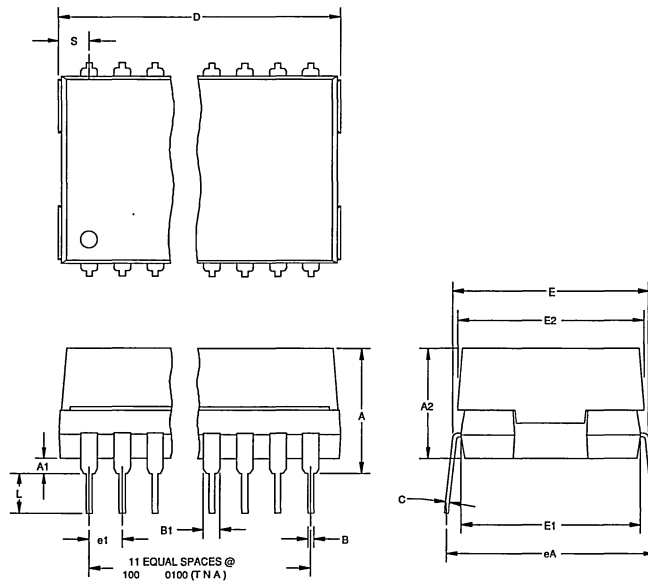
NOTES :

1. Effective capacitance calculated from the equation C

ORDERING INFORMATION

PART NUMBER	ACCESS TIME (ns)	SUPPLY VOLTAGE
MK48T08B10	100	5V±10%
MK48T08B15	150	5V±10%
MK48T08B20	200	5V±10%
MK48T18B10	100	5V +10% -5%
MK48T18B15	150	5V +10% -5%
MK48T18B20	200	5V +10% -5%

FIGURE 12 : PACKAGE MECHANICAL DATA



DIM	INCHES		NOTES
	MIN	MAX	
A	.320	.380	2
A1	.015	.030	2
A2	.300	.360	
B	.015	.021	3
B1	.045	.070	
C	.008	.012	3
D	-	1.495	1
E	.530	640	
E1	.530	.550	
E2	.550	.570	
e1	.090	.110	
eA	.600	.700	
L	.120	.150	
S	.060	090	

NOTES

1. OVERALL LENGTH INCLUDES FLASH AND PROJECTIONS ON EITHER END OF PACKAGE
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN WHEN SOLDER LEAD FINISH IS SPECIFIED

SGS-THOMSON MICROELECTRONICS

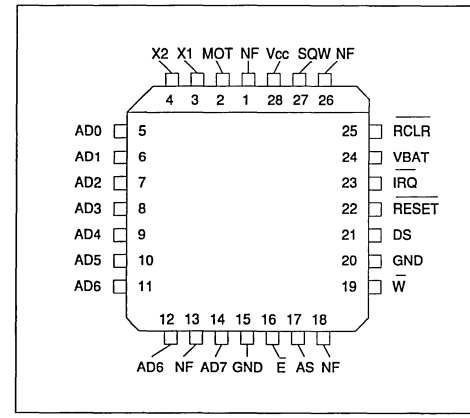
MK48T85Q

ADDRESS / DATA MULTIPLEX TIMEKEEPER™ RAM

ADVANCE DATA

- DROP-IN REPLACEMENT FOR IBM AT COMPUTER CLOCK/CALENDAR
- PIN COMPATIBLE WITH THE DS1285Q
- EXTERNAL BATTERY AND CRYSTAL PINS
- COUNTS SECONDS, MINUTES, HOURS, DAYS, DAY OF THE WEEK, DATE, MONTH AND YEAR WITH LEAP YEAR COMPENSATION
- BINARY OR BCD REPRESENTATION OF TIME, CALENDAR AND ALARM
- 12 OR 24 HOUR CLOCK WITH AM AND PM IN 12 HOUR MODE
- SELECTABLE BETWEEN MOTOROLA AND INTEL BUS TIMING
- MULTIPLEX BUS FOR PIN EFFICIENCY
- INTERFACED WITH SOFTWARE AS 64 RAM LOCATIONS
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose ram
- PROGRAMMABLE SQUARE WAVE OUTPUT SIGNAL
- BUS COMPATIBLE INTERRUPT SIGNALS (IRQ)
- THREE INTERRUPTS ARE SEPARATELY SOFTWARE-MASKABLE AND TESTABLE
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 us to 500 ms
  - End of clock update cycle

PIN CONNECTIONS



PIN NAMES

A/D0 - A/D7	ADDRESS / DATA
MOT	BUS TYPE SELECTION
$\overline{E}$	CHIP SELECT
AS	ADDRESS STROBE
$\overline{W}$	READ / WRITE
SQW	SQUARE WAVE OUT
$\overline{IRQ}$	INTERRUPT REQUEST
$\overline{RESET}$	RESET
DS	DATA STROBE
V_{CC}	+5 VOLTS
GND	GROUND
$\overline{RCLR}$	RAM CLEAR
X1, X2	32.768 KHz CRYSTAL
VBAT	+3 VOLT BATTERY INPUT
NF*	NO FUNCTION

* This pin serves no function and may be connected to other signals without affecting device operation. The electrical characteristics are the same as the other inputs pins.

DESCRIPTION

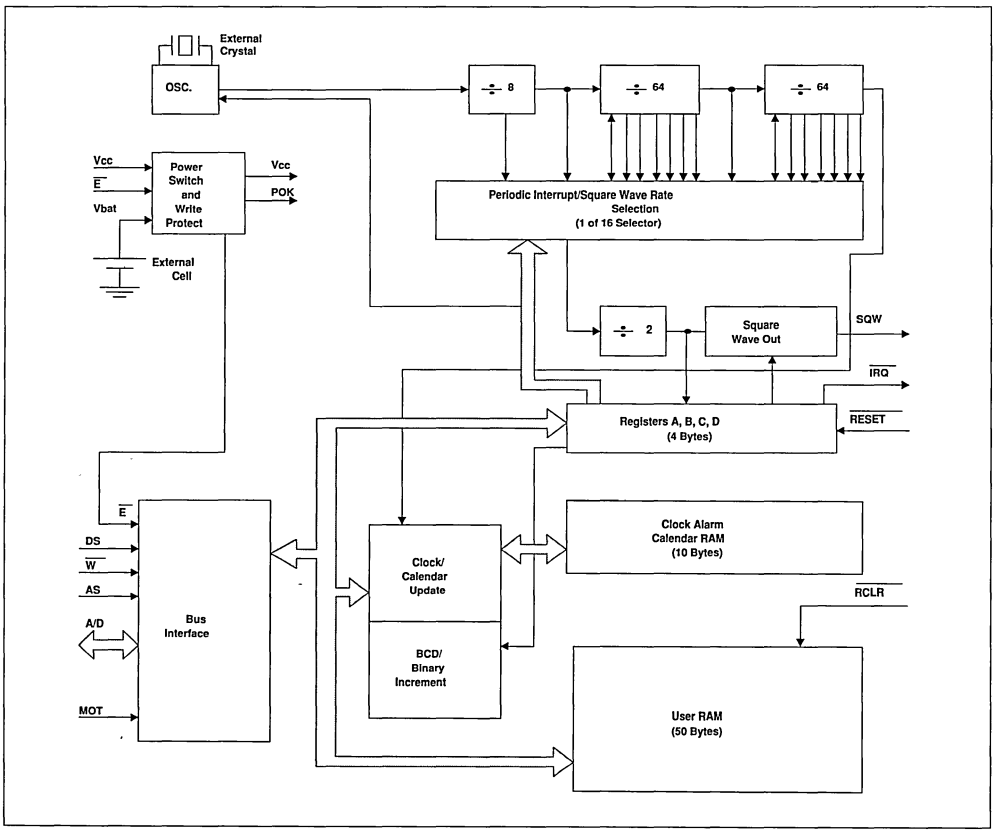
The MK48T85 RealTime Clock and RAM is designed to be a functional replacement for the DS1285. The functions available to the user include a time-of-day clock, an alarm, a one-hundred-year calendar, programmable interrupts, a square wave generator, and 50 bytes of static RAM. The MK48T85 provides connections for a battery and a 32.768 KHz crystal. The battery connection allows the user to back-up the RAM and clock functions in the absence of system voltage.

Automatic deselection of the device provides insurance that data integrity is not compromised should V_{CC} fall below specified (V_{PFD}) levels. The automatic deselection of the device remains in effect upon power up for a period of 100ms after V_{CC} rises above V_{PFD}, provided the Real Time Clock is running and the count down chain is not in reset, allowing sufficient time for V_{CC} to stabilize and giving the system clock a wake up period so that a valid system reset can be established.

OPERATION

The block diagram in Figure 1 shows the pin connection with the major functions of MK48T85 (Real Time Clock/RAM). For a complete description of operating conditions, electrical characteristics, bus timing, and pin descriptions other than X1, X2, VBAT, and $\overline{RCLR}$ see the MK48T87(B) datasheet.

FIGURE 1 . BLOCK DIAGRAM



SIGNAL DESCRIPTIONS

X1, X2 - The X1 and X2 pins are the connections for a standard 32.768 KHz quartz crystal.

VBAT - The VBAT pin is the battery input for any standard 3V lithium cell or other energy source.

RCLR - the $\overline{RCLR}$ pin is used to clear (set to logic "1") all 50 bytes of the general purpose RAM associated with the Real Time Clock. In order to clear the RAM, $\overline{RCLR}$ must be forced to an input logic "0" (-0.3 to 0.8 volts) for a minimun of 100 ms when VCC is applied

FOR COMPLETE DESCRIPTION OF OPERATING CONDITIONS, ELECTRICAL CHARACTERISTICS, BUS TIMING, PACKAGE DIMENSION, AND PIN DESCRIPTIONS, SEE THE MK48T87(B) DATASHEET. .

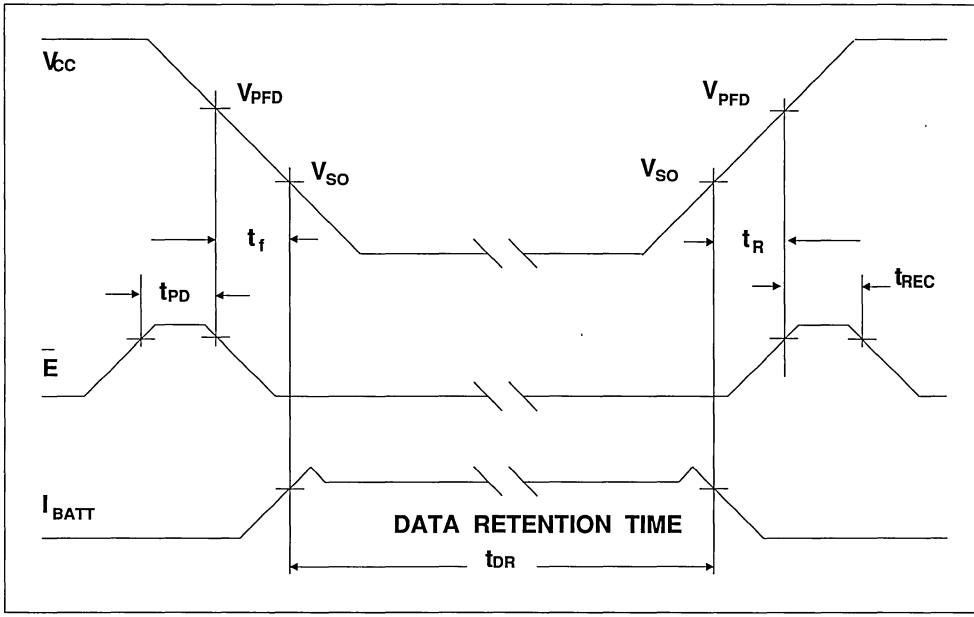
DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) ($V_{CC\ (Max)} \leq V_{CC} \leq V_{CC(\ Min)}$)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		15	mA	
I_{mot}	Input Current	-1.0	500	µA	
I_{IL}	Input Leakage Current	-1	+1	µA	
I_{OL}	Output Leakage Current	-5	+5	µA	
V_{OH}	Output Logic "1" Voltage (I_{OUT} = -1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 4.0 mA)		0.4	V	
VBAT	Battery Voltage	2.4	3.5	V	

CRYSTAL ELECTRICAL CHARACTERISTICS (externally supplied)

SYMBOL	PARAMETER	TEST CONDITIONS	VALUES			UNITS
			MIN	TYP	MAX	
f_O	Resonant Frequancy			32.768		KHz
r_S	Series Resistance				30	KΩ
c_L	load Capacitance		12.5			pf

FIGURE 2 . POWER-UP / POWER-DOWN CONDITIONS



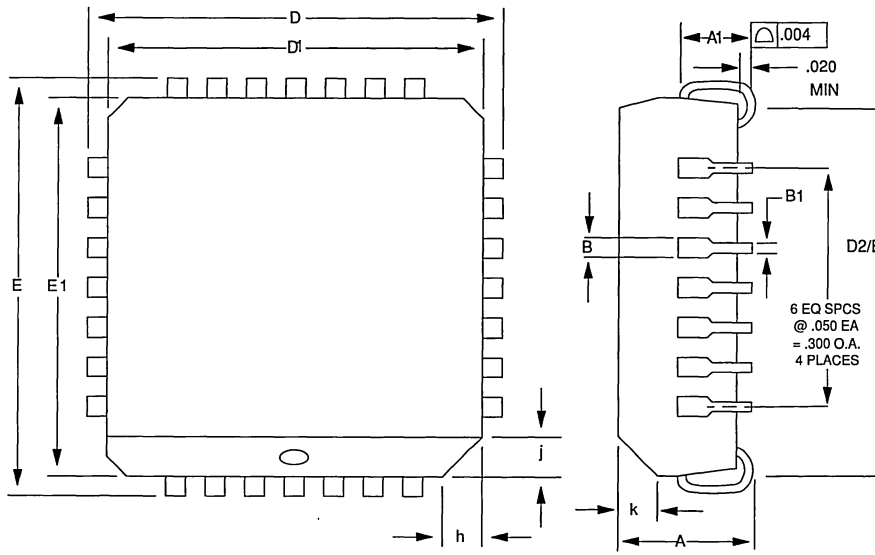
AC ELECTRICAL CHARACTERISTICS (POWER-UP / DOWN TIMING)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} Before Power Down	0		ns	
t_F	V_{PFD} to V_{SO} V_{CC} Fall Time	310		µs	
t_R	V_{SO} to V_{PFD} V_{CC} Rise Time	100		µs	

DC ELECTRICAL CHARACTERISTICS (POWER-UP/ DOWN TRIP POINTS)(0°C ≤ T_A ≤ 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{PFD}	Power-fail Deselect Voltage		1.29 V_{BAT}		V	
V_{SO}	Battery Back-up Swithover Voltage		V_{BAT}		V	

FIGURE 3 . PACKAGE DESCRIPTION 28 PIN PLCC



DIM	INCHES		NOTES
	MIN	MAX	
A	0.165	0.185	2
A1	0.090	0.120	2
B	0.026	0.032	2
B1	0.013	0.021	2
D	0.485	0.495	
D1	0.450	0.456	
D2	0.390	0.430	
E	0.485	0.495	
E1	0.450	0.456	
E2	0.390	0.430	
h	0.042	0.060	
j	0.042	0.060	
k	0.042	0.056	

NOTES:

1. Lead finish to be solder dip or tin/lead plate.

2. The maximun limit shall be increased by 0.003 inche when solder lead finish is specified.

SGS-THOMSON MICROELECTRONICS

MK48T87A(B)

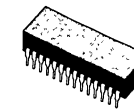
ADDRESS / DATA MULTIPLEX TIMEKEEPER™ RAM

ADVANCE DATA

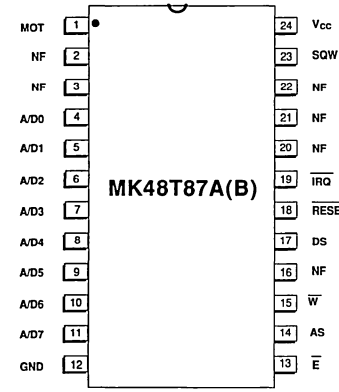
- DROP-IN REPLACEMENT FOR IBM AT COMPUTER CLOCK/CALENDAR
- PIN COMPATIBLE WITH THE MC146818 A
- TOTALLY NONVOLATILE WITH OVER 10 YEARS OF OPERATION IN THE ABSENCE OF POWER
- SELF-CONTAINED SUBSYSTEM INCLUDES LITHIUM BATTERY, QUARTZ CRYSTAL AND SUPPORT CIRCUITRY
- COUNTS SECONDS, MINUTES, HOURS, DAYS, DAY OF THE WEEK, DATE, MONTH AND YEAR WITH LEAP YEAR COMPENSATION
- BINARY OR BCD REPRESENTATION OF TIME, CALENDAR AND ALARM
- 12 OR 24 HOUR CLOCK WITH AM AND PM IN 12 HOUR MODE
- SELECTABLE BETWEEN MOTOROLA AND INTEL BUS TIMING
- MULTIPLEX BUS FOR PIN EFFICIENCY
- INTERFACED WITH SOFTWARE AS 64 RAM LOCATIONS
  - 14 Bytes Of Clock And Control Registers
  - 50 Bytes Of General Purpose Ram
- PROGRAMMABLE SQUARE WAVE OUTPUT SIGNAL
- BUS COMPATIBLE INTERRUPT SIGNALS (IRQ)
- THREE INTERRUPTS ARE SEPARATELY SOFTWARE-MASKABLE AND TESTABLE
  - Time-of-day Alarm Once/second To Once/day
  - Periodic Rates From 122 us To 500 ms
  - End Of Clock Update Cycle

* This pin serves no function and may be connected to other signals without affecting device operation. The electrical characteristics are the same as the other inputs pins.

B
DIP-24
(Plastic with battery top Hat)



PIN CONNECTIONS



PIN NAMES

A/D0 - A/D7	ADDRESS / DATA
MOT	BUS TYPE SELECTION
$\overline{E}$	CHIP SELECT
AS	ADDRESS STROBE
$\overline{W}$	READ / WRITE
SQW	SQUARE WAVE OUT
$\overline{IRQ}$	INTERRUPT REQUEST
$\overline{RESET}$	RESET
DS	DATA STROBE
V_{CC}	+5 VOLTS
GND	GROUND
$\overline{RCLR}$	RAM CLEAR
NF*	NO FUNCTION

DESCRIPTION

The MK48T87 Real Time Clock and RAM is designed to be a compatable replacement for the MC146818. A lithium energy source, a quartz crystal and write-protection circuitry are contained within a 24-pin dual in-line package. The MK48T87 is, therefore, a complete subsystem replacing as many as 16 components in a typical application. The functions available to the user include a nonvolatile time-of-day clock, an alarm, a one-hundred-year calendar, programmable interrupt, square wave generator, and 50 bytes of nonvolatile static RAM. The Real Time Clock/RAM is unique in that the time-of-day and memory are maintained even in the absence of power.

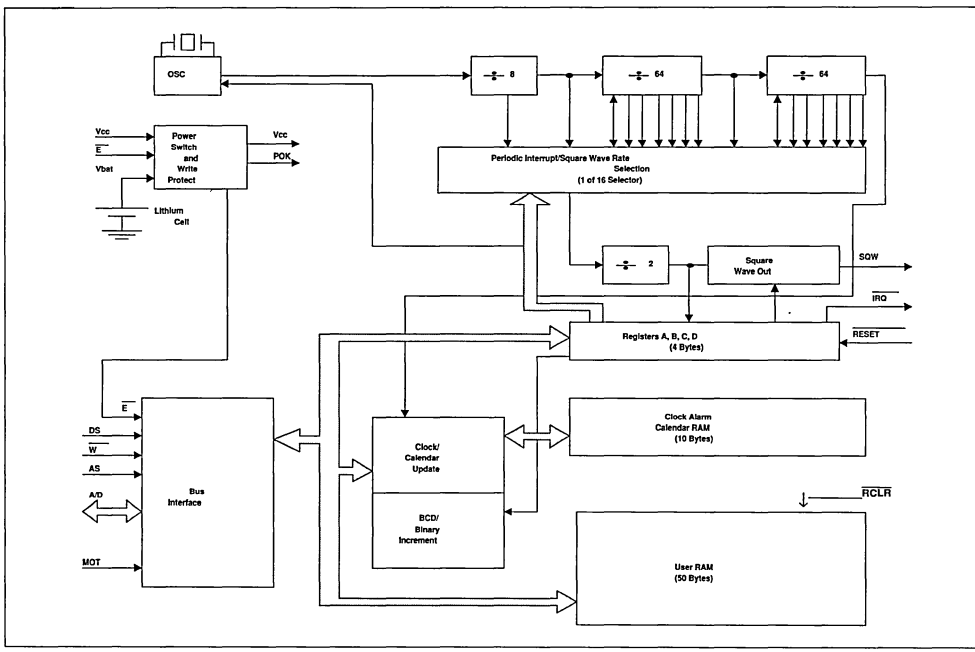
Automatic deselection of the device provides insurance that data integrity is not compromised should V_{CC} fall below specified (V_{PFD}) levels. The automatic deselection of the device remains in effect upon power up for a period of 100ms after V_{CC} rises above V_{PFD}, provided the Real Time Clock is running and the count down chain is not in reset, allowing sufficient time for V_{CC} to stabilize and giving the system clock a wake up period so that a valid system reset can be established.

The block diagram in Figure 1 shows the pin connection with the major internal functions of MK48T87 (Real Time Clock/RAM). **FOR COMPLETE DESCRIPTION OF OPERATING CONDITIONS, ELECTRICAL CHARACTERISTICS, BUS TIMING, PACKAGE DIMENSION, AND PIN DESCRIPTIONS OTHER THAN RLCR, SEE THE MK48T87(B) DATASHEET.**

SIGNAL DESCRIPTIONS

RCLR - The $\overline{RCLR}$ pin is used to clear (set to logic "1") all 50 bytes of general purpose RAM but does not affect the RAM associated with the Real Time Clock. In order to clear the RAM, $\overline{RCLR}$ must be forced to an input Logic "0" (-0.3 to 0.8 volts) for a minimun of 100 ms when V_{CC} is applied.

FIGURE 1 . BLOCK DIAGRAM



SGS-THOMSON MICROELECTRONICS

MK48T87(B)

ADDRESS / DATA MULTIPLEX TIMEKEEPER™ RAM

ADVANCE DATA

- DROP-IN REPLACEMENT FOR IBM AT COMPUTER CLOCK/CALENDAR
- PIN COMPATIBLE WITH THE MC146818 A
- TOTALLY NONVOLATILE WITH OVER 10 YEARS OF OPERATION IN THE ABSENCE OF POWER
- SELF-CONTAINED SUBSYSTEM INCLUDES LITHIUM BATTERY, QUARTZ CRYSTAL AND SUPPORT CIRCUITRY
- COUNTS SECONDS, MINUTES, HOURS, DAYS, DAY OF THE WEEK, DATE, MONTH AND YEAR WITH LEAP YEAR COMPENSATION
- BINARY OR BCD REPRESENTATION OF TIME, CALENDAR AND ALARM
- 12 OR 24 HOUR CLOCK WITH AM AND PM IN 12 HOUR MODE
- SELECTABLE BETWEEN MOTOROLA AND INTEL BUS TIMING
- MULTIPLEX BUS FOR PIN EFFICIENCY
- INTERFACED WITH SOFTWARE AS 64 RAM LOCATIONS

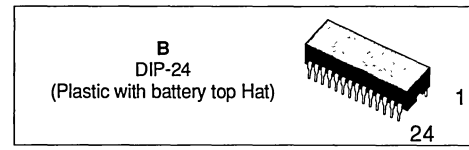
  14 Bytes Of Clock And Control Registers

  50 Bytes Of General Purpose Ram
- PROGRAMMABLE SQUARE WAVE OUTPUT SIGNAL
- BUS COMPATIBLE INTERRUPT SIGNALS (IRQ)
- THREE INTERRUPTS ARE SEPARATELY SOFTWARE-MASKABLE AND TESTABLE

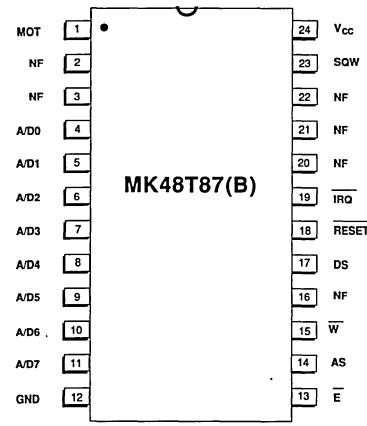
  Time-of-day Alarm Once/second To Once/day

  Periodic Rates From 122 us To 500 ms

  End Of Clock Update Cycle



PIN CONNECTIONS



PIN NAMES

A/D0 - A/D7	ADDRESS / DATA
MOT	BUS TYPE SELECTION
$\overline{E}$	CHIP SELECT
AS	ADDRESS STROBE
$\overline{W}$	READ / WRITE
SQW	SQUARE WAVE OUT
$\overline{IRQ}$	INTERRUPT REQUEST
$\overline{RESET}$	RESET
DS	DATA STROBE
V_{CC}	+5 VOLTS
GND	GROUND
NF*	NO FUNCTION

* This pin serves no function and may be connected to other signals without affecting device operation. The electrical characteristics are the same as the other inputs pins.

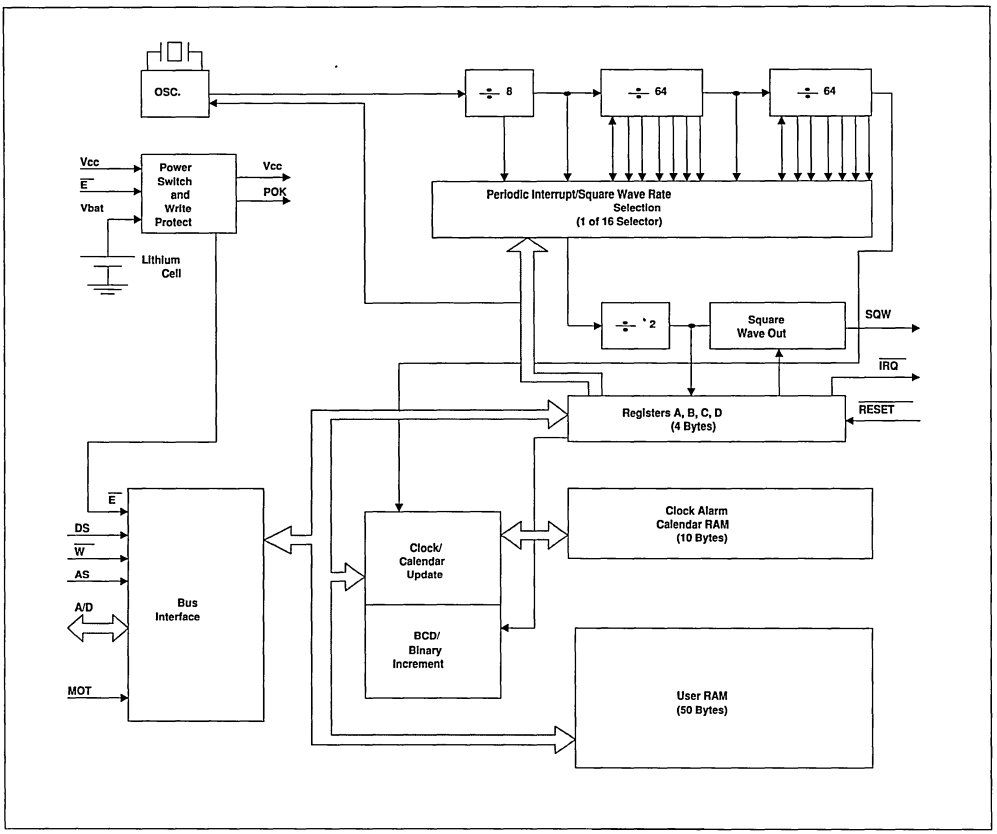
DESCRIPTION

The MK48T87 RealTime Clock and RAM is designed to be a compatable replacement for the MC146818. A lithium energy source, a quartz crystal and write-protection circuitry are contained within a 24-pin dual in-line package. The MK48T87 is, therefore, a complete subsystem replacing as many as 16 components in a typical application. The functions available to the user include a nonvolatile time-of-day clock, an alarm, a one-hundred-year calendar, programmable interrupt, square wave generator, and 50 bytes of nonvolatile static RAM. The Real Time Clock/RAM is unique in that the time-of-day and memory are maintained even in the absence of power.

Automatic deselection of the device provides insurance that data integrity is not compromised should V_{CC} fall below specified (V_{PFD}) levels. The automatic deselection of the device remains in effect upon power up for a period of 100ms after V_{CC} rises above V_{PFD}, provided the Real Time Clock is running and the count down chain is not in reset, allowing sufficient time for V_{CC} to stabilize and giving the system clock a wake up period so that a valid system reset can be established.

The block diagram in Figure 1 shows the pin connection with the major internal functions of MK48T87 (Real Time Clock/RAM). The following paragraphs describe the function of each pin.

FIGURE 1 . BLOCK DIAGRAM



SIGNAL DESCRIPTIONS

GND, V_{CC} - D.C. power is provided to the device on these pins. V_{CC} is the +5 volt input. When V_{CC} is applied and is above V_{PFD}, the device is fully accessible and the data can be written and read. When V_{CC} is below V_{PFD}, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below V_{SO}, the RAM and timekeeper are switched over to an internal Lithium energy source. The timekeeping function maintains an accuracy of ± 1 minute per month at 25 ° C regardless of the voltage input on the V_{CC} pin.

MOT (Mode Select) - The MOT pin offers the flexibility to choose between two bus types. When connected to V_{CC}, Motorola bus timing is selected. When connected to GND or left disconnected, Intel bus timing is selected. The pin has an internal pull-down resistance of approximately 20 K .

SQW (Square Wave Output) - The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the Real Time Clock. The frequency of the SQW pin may be changed by programming Register A. As shown in Table 1, the SQW signal may be turned on and off using the SQWE bit in Register B. The SQW signal is not available when V_{CC} is less than V_{PFD}.

TABLE 1 . PERIODIC INTERRUPT RATE AND SQUARE WAVE FREQUENCY

SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 µs	8.192 KHz
0	1	0	0	244.141 µs	4.096 KHz
0	1	0	1	488.281 µs	2.048 KHz
0	1	1	0	976.5625 µs	1.024 KHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

AD0-AD7 (Multiplexed Bi-Directional Address/Data Bus) - Multiplexing the bus reduces the device pin count because address information and data information time share the same signal paths. The addresses are presented during the first portion of the bus cycle and the same pins and signal paths are used for data transfer during the second portion of the cycle. Address/data multiplexing does not slow the access time of the MK48T87 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the falling edge of AS/ALE, at which time the MK48T87 latches the address from ADO toAD5. Valid write data must be present and held stable during the latter portion of the DS or RD pulses. The read cycle is terminated and the bus returns to a high impedance state as DS transitions low in the case of Motorola timing or as RD transitions high in the case of Intel timing.

AS (Address Strobe Input) - A positive going address strobe pulse serves to demultiplex the bus. The falling edge of AS/ALE causes the address to be latched within the MK48T87.

DS (Data Strobe or Read Input) - The DS/RD pin has two modes of operation depending on the level of the MOT pin. When the MOT pin is connected to V_{CC}, Motorola bus timing is selected. In this mode DS is a positive pulse during the latter portion of the bus cycle and is called Data Strobe. During read cycles, DS signifies the time that the MK48T87 is to drive the bi-directional bus. In write cycles the trailing edge of DS causes the MK48T87 to latch the written data. When the MOT pin is connected to GND, Intel bus timing is selected. In this mode the DS pin is called Read (RD). RD identifies the time period when the MK48T87 drives the bus with read data. The RD signal is the same definition as the Output Enable ($\overline{G}$) signal on a typical memory.

W (Read/Write Input) - The $\overline{W}$ pin also has two modes of operation. When the MOT pin is connected to V_{CC} for Motorola timing, $\overline{W}$ is a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on $\overline{W}$ while DS is high. A write cycle is indicated when $\overline{W}$ is low during DS. When the MOT pin is connected to GND for Intel timing, the $\overline{W}$ signal is an active low signal called WR. In this mode the $\overline{W}$ pin has the same meaning as the Write Enable signal ($\overline{W}$) on generic RAMs.

E (Chip Select Input) - The Chip Select signal ($\overline{E}$) must be asserted low for a bus cycle in which the MK48T87 is to be accessed. $\overline{E}$ must be kept in the active state during DS and AS for Motorola timing and during RD and $\overline{W}$ for Intel timing. Bus cycles which take place without asserting $\overline{E}$ will latch addresses but no access will occur. When V_{CC} is below V_{PFD}, the MK48T87 internally inhibits access cycles by internally disabling the $\overline{E}$ input. This action protects both the Real Time Clock data and RAM data during power outages.

IRQ (Interrupt Request Output) - The $\overline{IRQ}$ pin is an active low output of the MK48T87 that may be used as an interrupt input to a processor. The IRQ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt- enable bit is set. To clear the $\overline{IRQ}$ pin the processor program normally reads the C register. The $\overline{RESET}$ pin also clears pending interrupts. When no interrupt conditions are present, the IRQ level is in the high impedance state. Multiple interrupt devices may be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ bus is an open drain output and requires an external pull-up resistor.

RESET (Reset Input) - The $\overline{RESET}$ pin has no effect on the clock, calendar, or RAM. On power-up the $\overline{RESET}$ pin may be held low for a time in order to allow the power supply to stabilize. The amount of time that $\overline{RESET}$ is held low is dependent on the application. However, if $\overline{RESET}$ is used on power up, the time $\overline{RESET}$ is low should exceed 200 ms to make sure that the internal timer which controls the MK48T87 on power-up has timed out. When $\overline{RESET}$ is low and V_{CC} is above V_{PFD}, the following occurs:

A. Periodic Interrupt Enable (PIE) bit is cleared to zero.

B. Alarm Interrupt Enable (AIE) bit is cleared to zero.

C. Update Ended Interrupt Flag (UF) bit is cleared to zero.

D. Interrupt Request Status Flag (IRQF) bit is cleared to zero.

E. Periodic Interrupt Flag (PF) bit is cleared to zero.

F. The device is not accessible until $\overline{RESET}$ is returned high.

G. Alarm Interrupt Flag (AF) bit is cleared to zero.

H. $\overline{IRQ}$ pin is in the high impedance state.

I. Square Wave Output Enable (SQWE) bit is cleared to zero.

J. Updated Ended Interrupt Is Cleared To Zero.

In a typical application $\overline{RESET}$ may be connected to Vcc. This connection will allow the MK48T87 to go in and out of power fail without affecting any of the control registers.

ADDRESS MAP

The Address Map of the MK48T87 is shown in Figure 2. The address map consists of 50 bytes of user RAM, 10 bytes of RAM which contain the RTC time, calendar and alarm data, and 4 bytes which are used for control and status. All 64 bytes can be directly written or read except for the following:

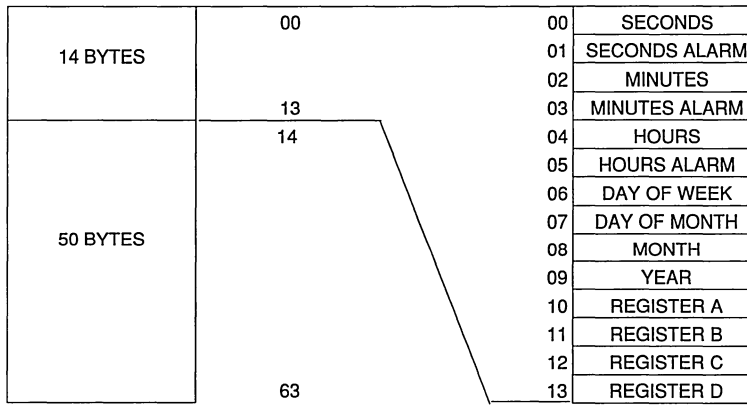
1. Registers C and D are read-only.

2. Bit 7 of Register A is read-only.

3. The high order bit of the seconds byte is read-only.

The contents of four control registers (A,B,C,D) are described in the "Register" section.

FIGURE 2 . ADDRESS MAP



TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate memory bytes. The time, calendar and alarm are set or initialized by writing the appropriate RAM bytes. The contents of the ten time, calendar and alarm bytes may be either Binary or Binary-Coded (BCD) format. Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a Logic one to prevent updates from occuring while access is being attempted. In addition to writing the ten time, calendar and alarm registers in a selected format (Binary or BCD), the data mode bit (DM) of Register B must be set to the appropriate logic level. All ten time, calendar and alarm bytes must be used the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the Real Time Clock to update the time and calendar bytes. Once initialized, the Real Time Clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. Table 2 shows the Binary and BCD formats of the ten time, calendar and alarm locations. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exits that seconds, minutes, hours, etc., may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

TABLE 2 . CALANDAR AND ALARM DATA MODES

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	SECONDS	00 - 59	00 - 3B	00 - 59
1	SECONDS ALARM	00 - 59	00 - 3B	00 - 59
2	MINUTES	00 - 59	00 - 3B	00 - 59
3	MINUTES ALARM	00 - 59	00 - 3B	00 - 59
4	HOURS - 12hrs MODE	1 - 12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	HOURS - 24hrs MODE	0 - 23	00 - 17	00 - 23
5	HOURS ALARM - 12hrs	1 - 12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	HOURS ALARM - 24hrs	0 - 23	00 - 17	00 - 23
6	DAY OF THE WEEK (SUNDAY=1)	1 - 7	01 - 07	01 - 07
7	DAY OF THE MONTH	1 - 31	01 - 1F	01 - 31
8	MONTH	1 - 12	01 - 0C	01 - 12
9	YEAR	0 - 99	00 - 63	00 - 99

The three alarm bytes may be used in two ways. First, when the alarm time is written in the appropriate hours, minutes and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second use condition is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at Logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

NONVOLATILE RAM

The 50 general purpose nonvolatile RAM bytes are not dedicated to any special function within the MK48T87. They can be used by the processor program as nonvolatile memory and are fully available during the update cycle.

INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt may be programmed to occur at rates from once per second to once per day. The periodic interrupt may be selected for rates from 122 us to 500 ms. The update-ended interrupt may be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The processor program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a Logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A "0" in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to Logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. The interrupt flag bit is a status bit which software can interrogate as necessary.

When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read; however, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two or three bits may be set when reading Register C. Each utilized flag bit should be examined when read to insure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the $\overline{IRQ}$ pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in Bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the MK48T87. The act of reading Register C clears all active flag bits and the IRQF bit.

OSCILLATOR CONTROL BITS

When the MK48T87 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium energy cell from being used until it is installed in system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 1. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin may be turned on and off under program control with the square wave enable bit (SQWE).

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the IRQ pin to go to an active state from once every 500 ms to once every 122 us. This function is separate from the alarm interrupt which may be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

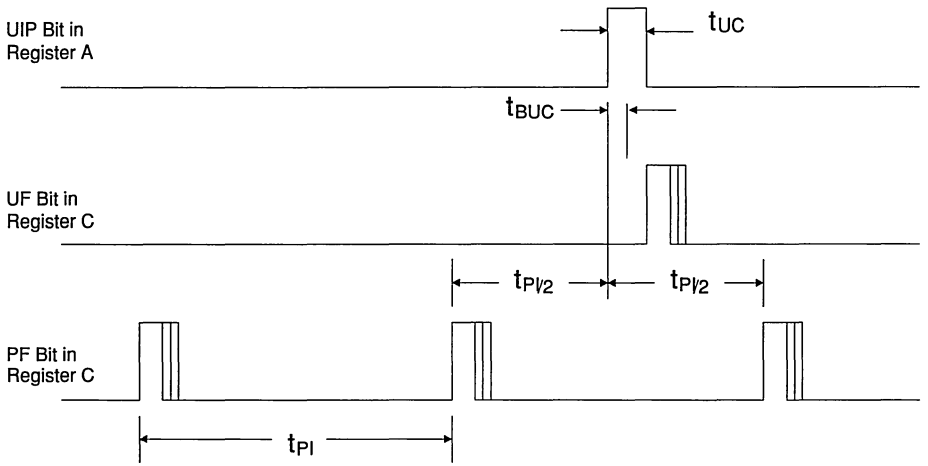
The MK48T87 executes an update cycle once per second regardless of the set bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar and alarm bytes if frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy indep endent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information are consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues and alarm if a match or if a "don't care" code is present in all three positions.

There are three methods which can be employed to handle access of the Real Time Clock which avoids any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 998 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 us later. If a low is read on the UIP bit, the user has at least 244 us before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 us.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within ($T_{PI/2}+t_{BUC}$) to insure that data is not read during the update cycle.

FIGURE 3 . UPDATE ENDED AND PERIODIC INTERRUPT RELATIONSHIP



PI = Periodic Interrupt Time Interval Per Table 1.

t_{BUC} = Delay Time Before Update Cycle = 244 µs.

t_{UC} = 2 ms.

REGISTERS:

REGISTER A

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP

The Update in Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is one. the update transfer will soon occur. The UIP is a zero, the update transfer will not occur for at least 244 us. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only and is not affected by $\overline{\text{RESET}}$. Writing the SET bit in Register B to a "1" inhibits any update transfer and clears the UIP status bit.

DVO, DV1, DV2

These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits which will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 1second after a pattern of 010 is written to DV0, DV1 and DV2.

RS3, RS2, RS1, RS0

These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected may be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user may do one of the following:

1. Enable the interrupt with the PIE bit;

2. Enable the SQW output pin with the $\overline{\text{SQWE}}$ bit;

3. Enable both at the same time and the same rate; or

4. Enable neither.

REGISTER B

MSB							LSB
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET

When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit which is not modified by RESET or internal functions of the MK48T87.

PIE

The periodic interrupt enable PIE bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to cause the IRQ pin to be driven low. When the PIE bit is set to one, periodic interrupts are generated by driving the IRQ pin low at a rate specified by the RS3 through RS0 bits of Register A. A zero in the PIE bit blocks the IRQ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal MK48T87 functions, but is cleared to zero on RESET.

AIE

The Alarm Interrupt Enable (AIE) bit is a read/write bit which when set to a one permits the Alarm Flag (AF) bit in register C to assert IRQ. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a "don't care" alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the IRQ signal. The RESET pin clears AIE to zero. The internal functions of the MK48T87 do not affect the AIE bit.

UIE

The Update Ended Interrupt Enable (UIE) bit is a read/write bit which enables the Update End Flag (UF) bit in Register C to assert IRQ. The RESET pin going low or the SET bit going high clears the UIE bit.

SQWE

When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on the SQW pin. When the SQWE bit is set to zero, the SQW pin is held low; the state of SQWE is cleared by the RESET pin. SQWE is a read/write bit.

DM

The Data Mode (DM) bit indicates whether time and calendar information are in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions or RESET. A one in DM signifies binary data and a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12

The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is a read/write and is not affected by internal functions or RESET.

DSE

The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions or RESET.

REGISTER C

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF

The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF=PIE=1

AF=AIE=1

UF=UIE=1

i.e.,IRQF=PF•PIE+AF•AIE+UF•UIE

Any time the IRQF bit is a one the $\overline{IRQ}$ pin is driven low. All flag bits are cleared after Register C is read by the program or when the $\overline{RESET}$ pin is low.

PF

The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are one, the $\overline{IRQ}$ signal is active and will set the IRQF bit. The PF bit is cleared by a $\overline{RESET}$ or a software read of Register C.

AF

A one in the AF (Alarm Interrupt Flag) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{IRQ}$ pin will go low and a one will appear in the IRQF bit. A $\overline{RESET}$ or a read of Register C will clear AF.

UF

The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in the UF bit causes the IRQF bit to be a one which will assert the $\overline{IRQ}$ pin. UF is cleared by reading Register C or a $\overline{RESET}$.

BIT 0 THROUGH BIT 3

These are unused bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT

The Valid RAM and Time (VRT) bit is set to the one state by SGS-THOMSON prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable. This bit is unaffected by $\overline{RESET}$.

BIT 6 THROUGH BIT 0

The remaining bits of Register D are not usable. They cannot be written and when read, they will always read zero.

ABSOLUTE MAXIMUM RATING*

PARAMETER	VALUE	UNIT
Voltage On Any Pin Relative To GND	-0.3 to +7.0	V
Ambient Operating (V_{CC} Off, Oscilator Off) Temperature	0 to +70	°C
Ambient Storage (V_{CC} Off, Oscilator Off) Temperature	-40 to +85	°C
Total Device Power Dissipation	1	W

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanrnt damage to the device. This is a stress rating only and functional operation of the device at these or any conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMENDED DC OPERATIONING CONDITIONS (0°C ≤ TA ≤ 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.5	V	
GND	Supply Voltage	0	0	V	
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3	V	

DC ELECTRICAL CHARACTERISTICS (0°C ≤ TA ≤ 70°C) ($V_{CC(MAX)} \leq V_{CC} \leq V_{CC(MIN)}$)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		15	mA	
I_{mot}	Input Current	-1.0	500	µA	
I_{IL}	Input Leakage Current	-1	+1	µA	
I_{OL}	Output Leakage Current	-5	+5	µA	
V_{OH}	Output Logic "1" Voltage (I_{OUT}=1.0 mA)	2.4		V	

CAPACITANCE (TA = 25°C)

SYMBOL	PARAMETER	MIN	MAX	NOTES
C_L	Capacitance on All Pins (Except DQ)	5.0	pF	
C_{DQ}	Capacitance on DQ Pins	7.0	pF	

AC ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.5V to 5.5 V)

		SYMBOL	MIN	MAX	UNITS	NOTES
1	Cycle Time	t_{CYC}	953	D.C.	ns	
2	Pulse Width, DS/E Low or $\overline{RD}/\overline{WR}$ High	PW_{EL}	300		ns	
3	Pulse Width, DS/E High or $\overline{RD}/\overline{WR}$ Low	PW_{EH}	325		ns	
4	Input Rise and Fall Time	t_R, t_F		30	ns	
8	R/$\overline{W}$ Hold Time	t_{RWH}	10		ns	
13	R/$\overline{W}$ Set-up Time Before DS/E	t_{RWS}	80		ns	
14	Chip Select Set-up Time Before DS, $\overline{WR}$ or $\overline{RD}$	t_{CS}	25		ns	
15	Chip Select Hold Time	t_{CH}	0		ns	
18	Read Data Hold Time	t_{DHR}	10	100	ns	
21	Write Data Hold Time	t_{DWH}	0		ns	
24	Muxed Address Valid Time to AS/ALE Fall	t_{ASL}	50		ns	
25	Muxed Address Hold Time	t_{AHL}	20		ns	
26	Delay Time DS/E to AS/ALE Fall	t_{ASD}	50		ns	
27	Pulse Width AS/ALE High	PW_{ASH}	135		ns	
28	Delay Time, AS/ALE to DS/E Rise	t_{ASED}	60		ns	
30	Output Data Delay Time From DS/E or $\overline{RD}$	t_{DDR}	20	240	ns	
31	Data Set-up Time	t_{DSW}	200		ns	
32	Reset Pulse Width	t_{RWL}	5		µs	
33	$\overline{IRQ}$ Release from DS	t_{IRDS}		2	µs	
34	$\overline{IRQ}$ Release from $\overline{RESET}$	t_{IRR}		2	µs	

FIGURE 4 . BUS TIMING FOR MOTOROLA INTERFACE

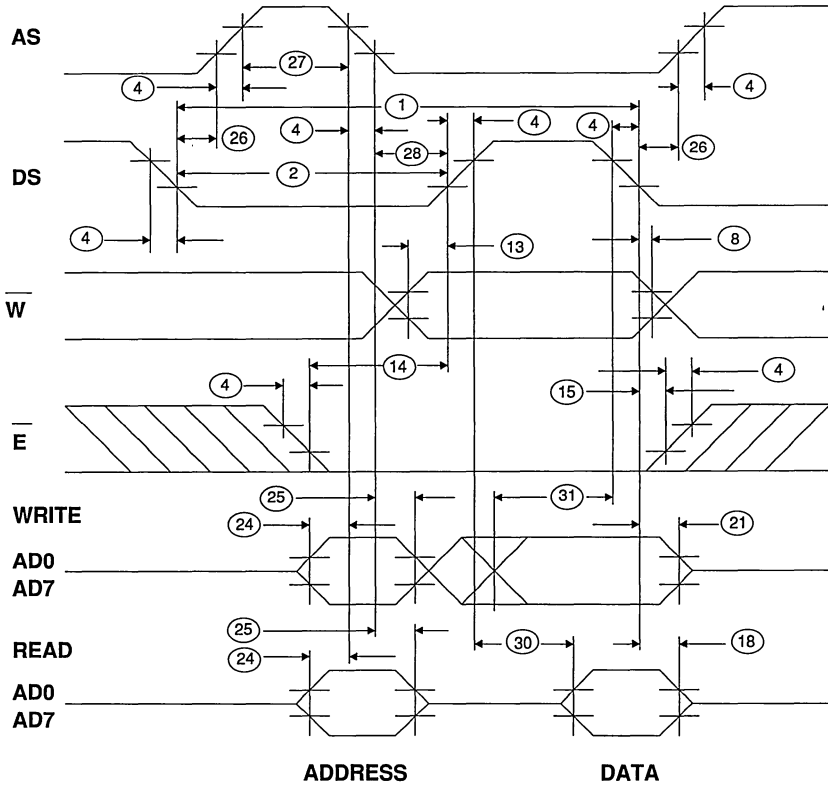


FIGURE 5 . BUS TIMING FOR INTEL INTERFACE READ CYCLE

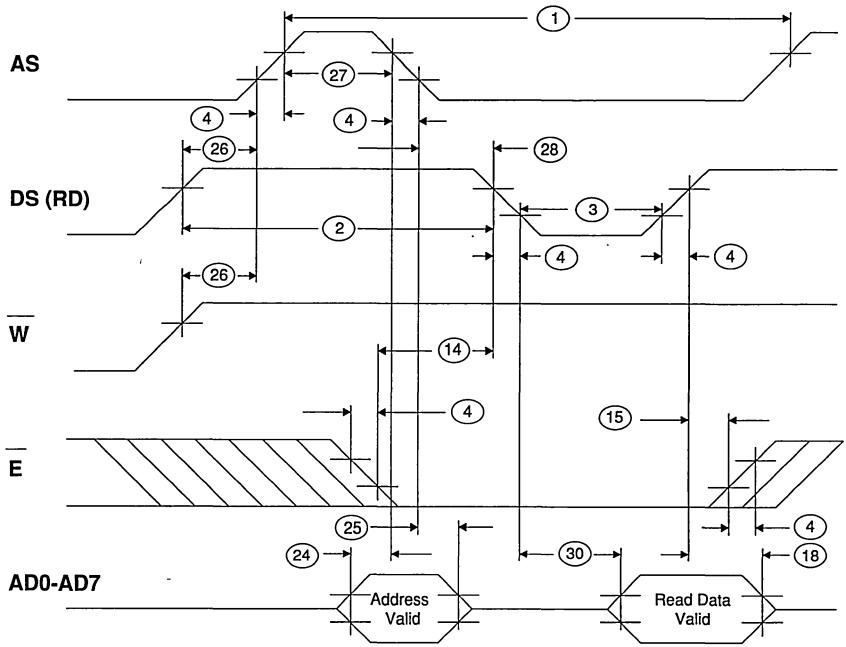


FIGURE 6 . BUS TIMING FOR INTEL INTERFACE WRITE CYCLE

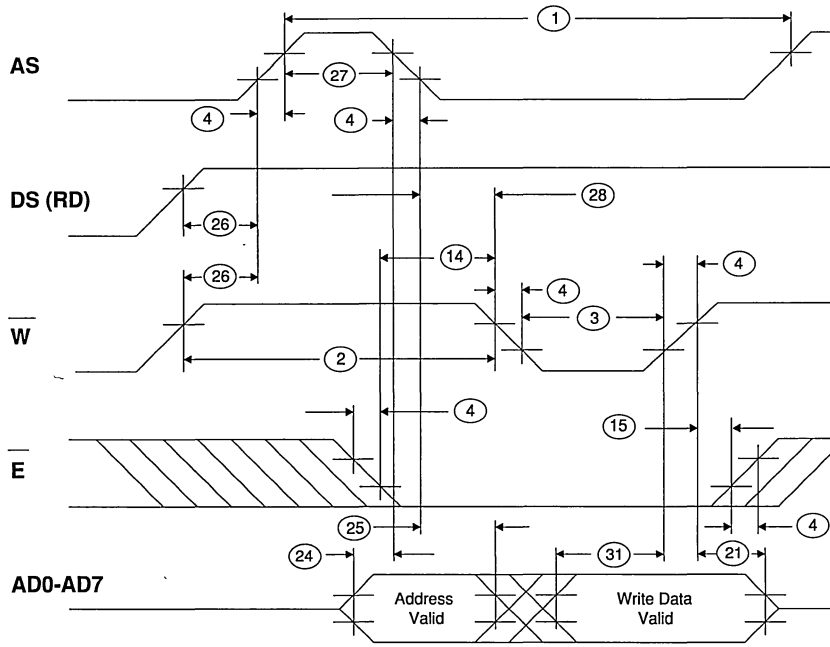


FIGURE 7 . IRQ RELEASE TIMING

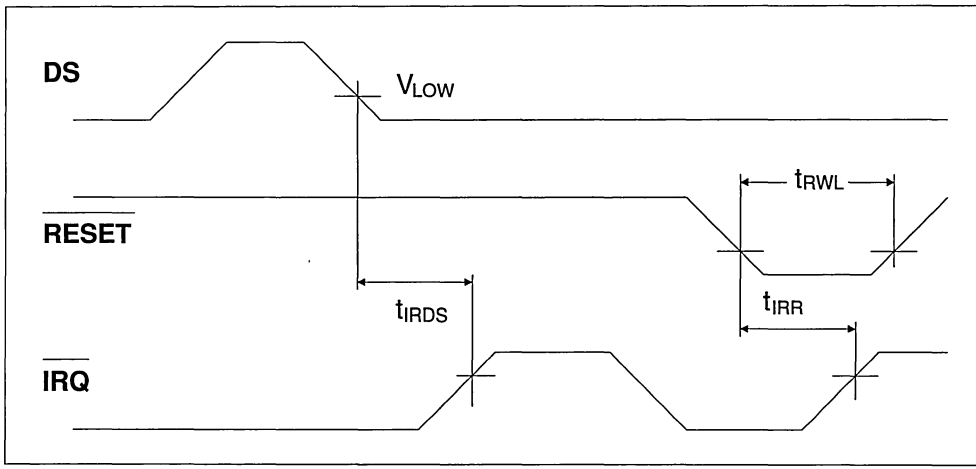
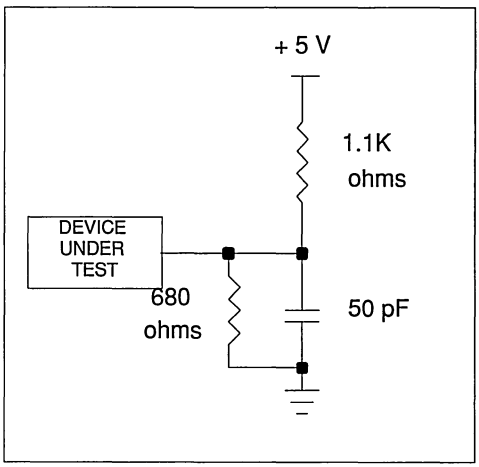


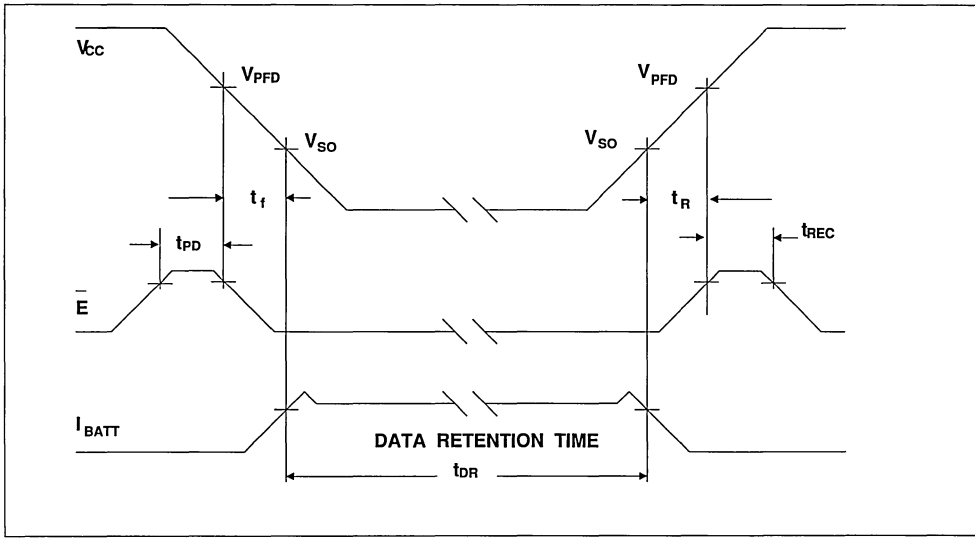
FIGURE 8 . OUTPUT LOAD



NOTES:

1. All voltages are referenced to ground.
2. All outputs are open.
3. The MOT pin has an internal pull-down of 20K
4. Applies to the AD0-AD7 pins, the IRQ pin and the SQW pin when each is in the high impedance state.
5. The IRQ pin is open drain.
6. Measured with a load as shown in Figure 8.

FIGURE 9 . POWER-UP / POWER-DOWN CONDITIONS



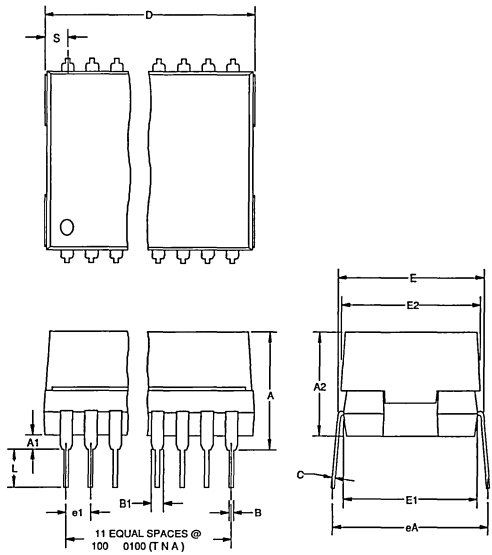
AC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TIMING) (0°C ≤ T_A ≤ +70°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} Before Power Down	0		ns	
t_F	V_{PFD} to V_{SO} V_{CC} Fall Time	310		µs	
t_R	V_{SO} to V_{PFD} V_{CC} Rise Time	100		µs	

DC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TRIP POINTS) (0°C≤T_A≤ +70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{PFD}	Power-fail Deselect Voltage		4.25		V	
V_{SO}	Battery Back-up Switchover Voltage		3.2		V	

FIGURE 10 . PACKAGE DESCRIPTION 24 PIN "B" PACKAGE



DIM	INCHES		NOTES
	MIN	MAX	
A	320	.380	2
A1	015	030	2
A2	300	.360	
B	015	021	3
B1	.045	.070	
C	.008	012	3
D	-	1 295	1
E	.530	640	
E1	.530	550	
E2	.550	570	
e1	090	110	
eA	600	.700	
L	.120	150	
S	060	090	

NOTES

1. OVERALL LENGTH INCLUDES FLASH AND PROJECTIONS ON EITHER END OF PACKAGE
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY 003 IN WHEN SOLDER LEAD FINISH IS SPECIFIED

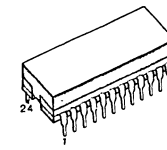
2K × 8 ZEROPOWER™ RAM

- PREDICTED WORST CASE BATTERY LIFE OF 11 YEARS @ 70°C
- DATA RETENTION IN THE ABSENCE OF POWER
- DATA SECURITY PROVIDED BY AUTOMATIC WRITE PROTECTION DURING POWER FAILURE
- +5 VOLT ONLY READ/WRITE
- CONVENTIONAL SRAM WRITE CYCLES
- FULL CMOS-440 mW ACTIVE; 5.5 mW STANDBY
- 24-PIN DUAL IN LINE PACKAGE, JEDEC PINOUTS
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME
- LOW-BATTERY WARNING
- TWO POWER-FAIL DESELECT TRIP POINTS AVAILABLE
  MK48Z02 $4.75V \geq V_{PFD} \geq 4.50V$
  MK48Z12 $4.50V \geq V_{PFD} \geq 4.20V$

Part Number	Access Time	R/W Cycle Time
MK48ZX2-12	120 ns	120 ns
MK48ZX2-15	150 ns	150 ns
MK48ZX2-20	200 ns	200 ns
MK48ZX2-25	250 ns	250 ns

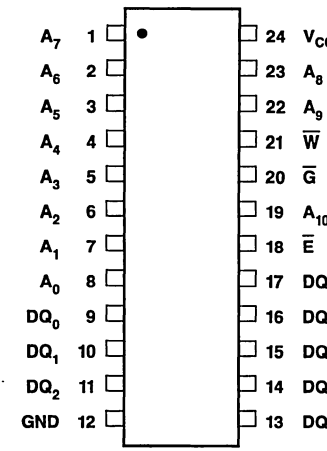
TRUTH TABLE (MK48Z02/12)

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ
$<V_{CC}$ (Max)	V_{IH}	X	X	Deselect	High-Z
$>V_{CC}$ (Min)	V_{IL}	X	V_{IL}	Write	D_{IN}
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
	V_{IL}	V_{IH}	V_{IH}	Read	High-Z
$<V_{PFD}$ (Min) $>V_{SO}$	X	X	X	Power-Fail Deselect	High-Z
$\leq V_{SO}$	X	X	X	Battery Back-up	High-Z



B
DIP-24
(Plastic with Battery Top Hat)

FIGURE 1. PIN CONNECTIONS



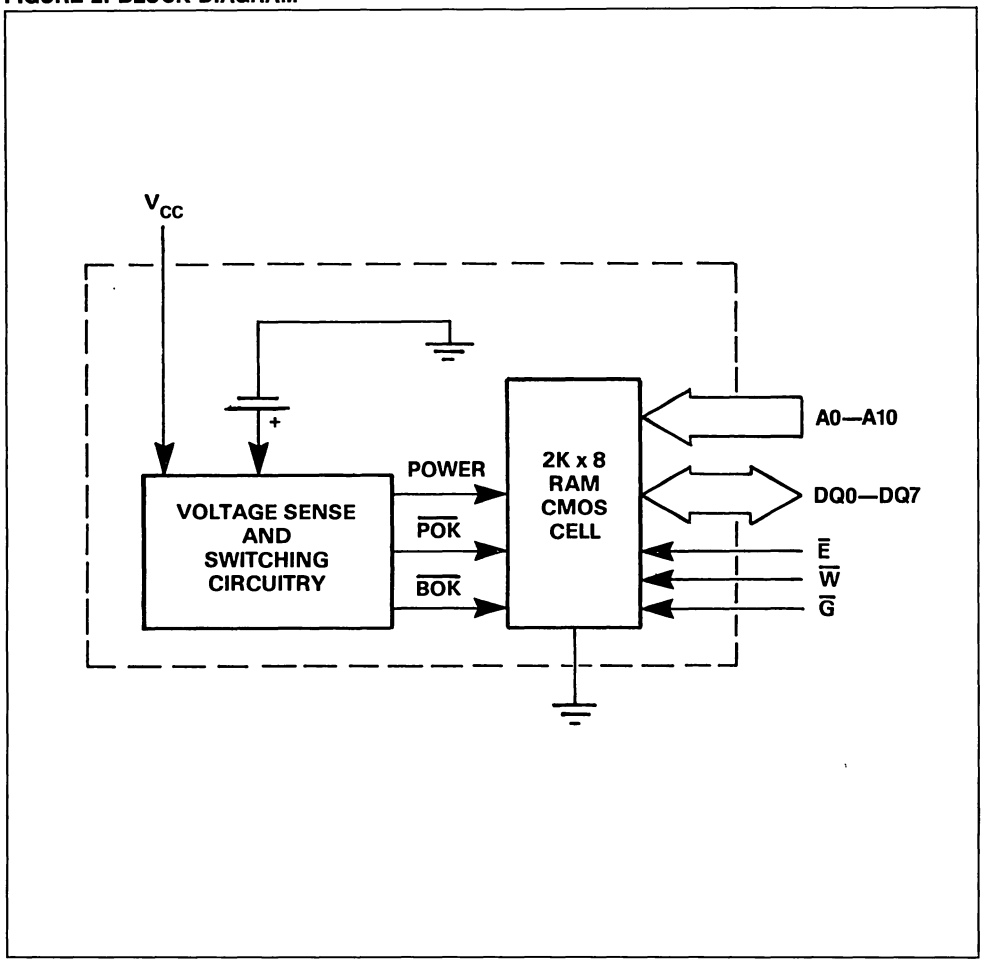
PIN NAMES

A_0 - A_{10}	Address Inputs	V_{CC}	System Power (+5 V)
$\overline{E}$	Chip Enable	$\overline{W}$	Write Enable
GND	Ground	$\overline{G}$	Output Enable
DQ_0—DQ_7 Data In/Data Out			

DESCRIPTION

The MK48Z02/12 is a 16,384-bit, Non-Volatile Static RAM, organized 2K x 8 using CMOS and an integral Lithium energy source. The ZEROPOWER™ RAM has the characteristics of a CMOS static RAM, with the important added benefit of data being retained in the absence of power. Data retention current is so small that a miniature Lithium cell contained within the package provides an energy source to preserve data. Low current drain has been attained by the use of a full CMOS memory cell, novel analog support circuitry, and carefully controlled junction leakage by an all implanted CMOS process. Safeguards against inadvertent data loss have been incorporated to maintain data integrity in the uncertain operating environment associated with power-up and power-down transients. The ZEROPOWER RAM can replace existing 2K x 8 static RAM, directly conforming to the popular Byte Wide 24-pin DIP package (JEDEC). MK48Z02/12 also matches the pinning of 2716 EPROM and 2K x 8 EEPROM. Like other static RAMs, there is no limit to the number of write cycles that can be performed. Since the access time, read cycle, and write cycle are less than 250 ns and require only +5 volts, no additional support circuitry is needed for interface to a microprocessor.

FIGURE 2. BLOCK DIAGRAM



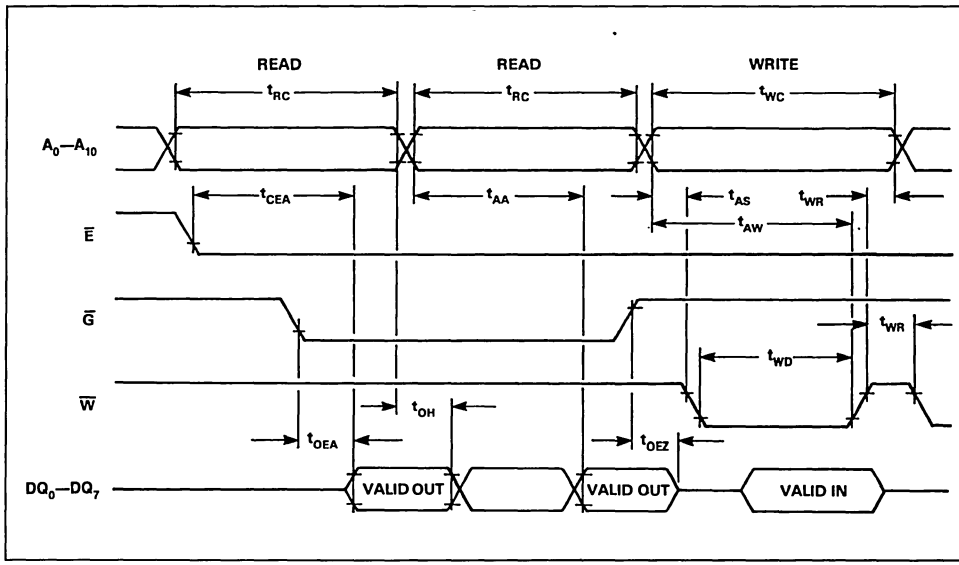
OPERATION

Read Mode

The MK48Z02/12 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low, providing a ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_n) defines which one of 2,048 bytes of data is to be accessed.

Valid data will be available to the eight data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are satisfied. If $\overline{E}$ or $\overline{G}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}), rather than the address. The state of the eight Data I/O signals is controlled by the $\overline{E}$ and $\overline{G}$ control signals. The data lines may be in an indeterminate state between t_{OH} and t_{AA}, but the data lines will always have valid data at t_{AA}.

FIGURE 3. READ-READ-WRITE TIMING



AC ELECTRICAL CHARACTERISTICS (READ CYCLE TIMING)
($0°C \le T_A \le 70°C$) (V_{CC} (Max) $\ge V_{CC} \ge V_{CC}$ (Min))

		MK48ZX2-12		MK48ZX2-15		MK48ZX2-20		MK48ZX2-25			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	120		150		200		250		ns	
t_{AA}	Address Access Time		120		150		200		250	ns	1
t_{CEA}	Chip Enable Access Time		120		150		200		250	ns	1
t_{OEA}	Output Enable Access Time		75		75		80		90	ns	1
t_{CEZ}	Chip Enable Hi to High-Z		30		35		40		50	ns	
t_{OEZ}	Output Enable Hi to High-Z		30		35		40		50	ns	
t_{OH}	Valid Data Out Hold Time	15		15		15		15		ns	1

NOTE
1. Measured using the Output Load Diagram shown in Figure 8.

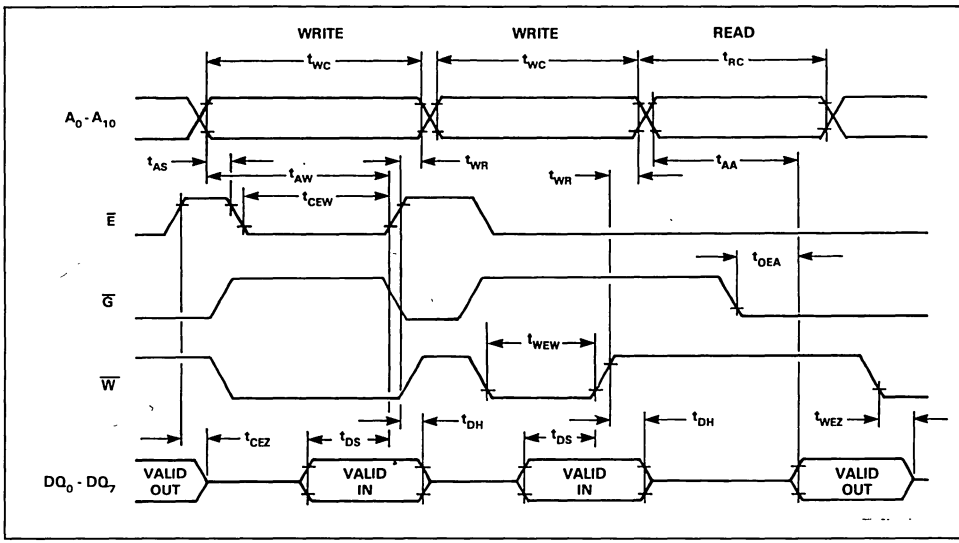
WRITE MODE

The MK48Z02/12 is in Write Mode whenever the $\overline{W}$ and $\overline{E}$ inputs are held low. The start of a Write is referenced to the latter occurring falling edge of either $\overline{W}$ or $\overline{E}$. A Write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{W}$ or $\overline{E}$ must return high for a minimum of t_{WR} prior to the initiation of another Read or Write Cycle. Data-in must be valid for t_{DS} prior to the End of Write and remain valid for t_{DH} afterward.

Some processors thrash producing spurious Write Cycles during power-up, despite application of a power-on reset. Users should force $\overline{W}$ or $\overline{E}$ high during power-up to protect memory after V_{CC} reaches V_{CC} (min) but before the processor stablizes.

The MK48Z02/12 $\overline{G}$ input is a DON'T CARE in the write mode. $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WEZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

FIGURE 4. WRITE-WRITE-READ TIMING



AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE TIMING)

(0°C ≤ T_A ≤ 70°C) (V_{CC} (Max) ≥ V_{CC} ≥ V_{CC} (Min))

		MK48ZX2-12		MK48ZX2-15		MK48ZX2-20		MK48ZX2-25			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	Write Cycle Time	120		150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		0		ns	
t_{AW}	Address Valid to End of Write	90		120		140		180		ns	
t_{CEW}	Chip Enable to End of Write	75		90		120		160		ns	
t_{WEW}	Write Enable to End of Write	75		90		120		160		ns	
t_{WR}	Write Recovery Time	10		10		10		10		ns	
t_{DS}	Data Setup Time	35		40		60		100		ns	
t_{DH}	Data Hold Time	0		0		0		0		ns	
t_{WEZ}	Write Enable Low to High-Z		40		50		60		80	ns	

DATA RETENTION MODE

With V_{CC} applied, the MK48Z02/12 operates as a conventional BYTEWIDE static ram. However, V_{CC} is being constantly monitored. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. The MK48Z02 has a V_{PFD} (max) -V_{PFD} (min) window of 4.75 volts to 4.5 volts, providing very high data security, particularly when all of the other system components are specified to 5.0 volts plus and minus 10%. The MK48Z12 has a V_{PFD} (max) -V_{PFD} (min) window of 4.5 volts to 4.2 volts, allowing users constrained to a 10% power supply specification to use the device.

Note: A mid-write cycle power failure may corrupt data at the current address location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time does not exceed t_F. The MK48Z02/12 may respond to transient noise spikes that reach into the deselect window if they should occur during the time the device is sampling V_{CC}. Therefore decoupling of power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{BOK}$) flag will be set. The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after first write, and normal RAM operation resumes. Figure 5 illustrates how a $\overline{BOK}$ check routine could be structured.

Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD} (Max). Caution should be taken to keep $\overline{E}$ or $\overline{W}$ high as V_{CC} rises past V_{PFD} (Min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

FIGURE 5. CHECKING THE $\overline{BOK}$ FLAG STATUS

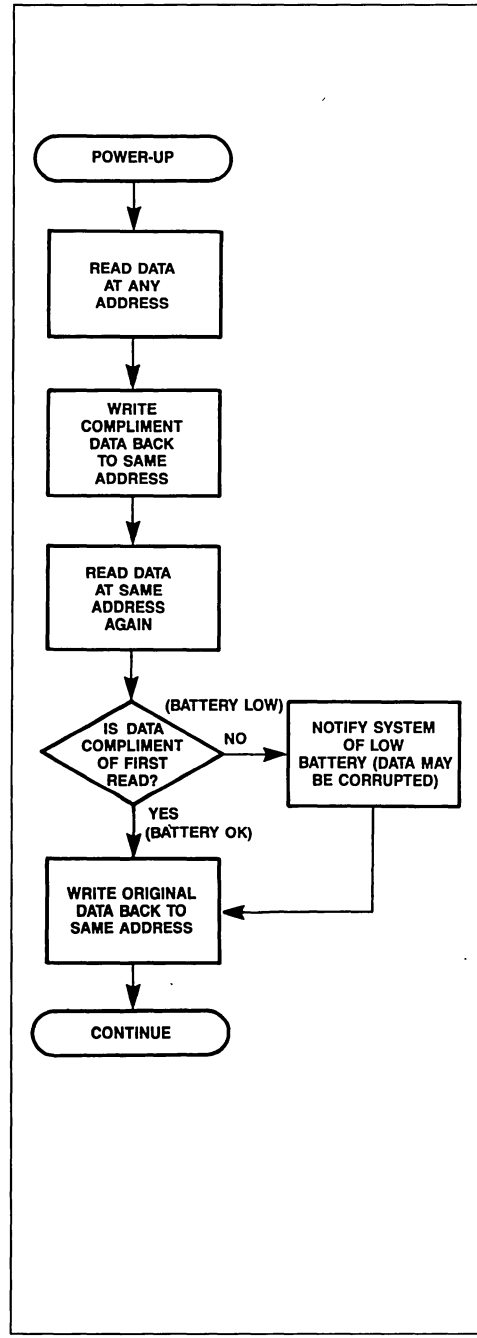
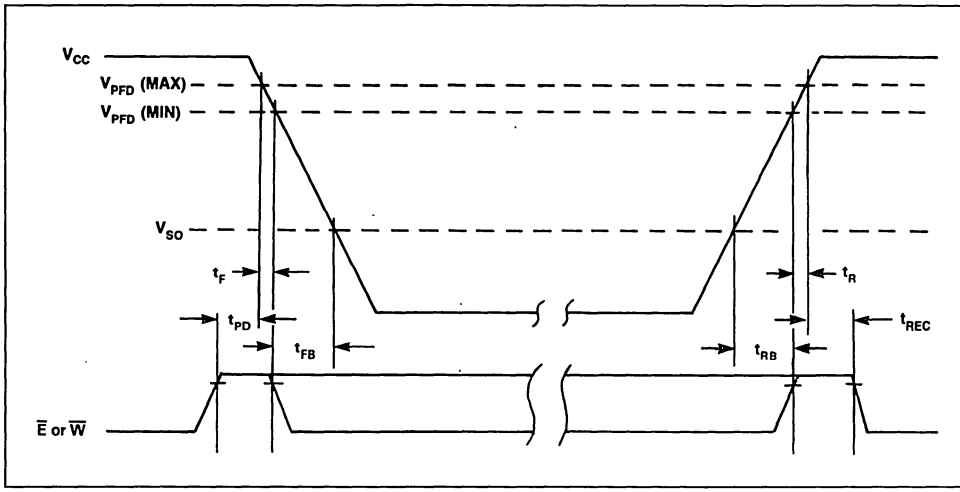


FIGURE 6. POWER-DOWN/POWER-UP TIMING



DC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TRIP POINT VOLTAGES)
(0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{PFD}	Power-fail Deselect Voltage (MK48Z02)	4.50	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MK48Z12)	4.20	4.3	4.50	V	1
V_{SO}	Battery Back-up Switchover Voltage		3		V	1

AC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TIMING)
(0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		ns	
t_F	V_{PFD} (Max) to V_{PFD} (Min) V_{CC} Fall Time	300		µs	2
t_{FB}	V_{PFD} (Min) to V_{SO} V_{CC} Fall Time	10		µs	3
t_{RB}	V_{SO} to V_{PFD} (Min) V_{CC} Rise Time	1		µs	
t_R	V_{PFD} (Min) to V_{PFD} (Max) V_{CC} Rise Time	0		µs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	2		ms	

NOTES:
1. All voltages referenced to GND.
2. V_{PFD} (Max) to V_{PFD} (Min) fall times of less t_F may result in deselection/write protection not occurring until 50 µs after V_{CC} passes V_{PFD} (Min). V_{PFD} (Max) to (Min) fall times of less than 10 µs may cause corruption of RAM data.
3. V_{PFD} (Min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data.

CAUTION

Negative undershoots below −0.3 volts are not allowed on any pin while in Battery Back-up mode.

DATA RETENTION TIME

About Figure 7

Figure 7 illustrates how expected MK48Z02/12 battery life is influenced by temperature. The life of the battery is controlled by temperature and is virtually independent of the percentage of time the MK48Z02/12 spends in battery back-up mode.

Battery life predictions presented in Figure 7 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's ongoing battery testing since it began in 1982, we believe the likelihood of such failure mechanisms surfacing is extremely poor. For the purpose of this testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.0 volt closed-circuit voltage across a 250K ohm load resistance.

A Special Note: The summary presented in Figure 7 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final; they can be expected to change as yet more data becomes available. We believe that future read-points of life tests presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 7. They are labeled "Average ($t_{50\%}$)" and "($t_{1\%}$)". These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure 7 indicates that a particular MK48Z02/12 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience battery failure within 11 years; 50% of them can be expected to fail within 20 years.

The $t_{1\%}$ figure represents the practical onset of wear-out, and is therefore suitable for use in what would normally be though of as a worst-case analysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning on the date of manufacture. Each MK48Z02/12 is marked with a four digit manufacturing date code in the form YYWW (Example: 8502 = 1985, week 2).

Calculating Predicted Battery Life

As Figure 7 indicates, the predicted life of the battery in the MK48Z02/12 is a function of temperature. The back-up current required by the memory matrix in the MK48Z02/12 is so low that it has negligible influence on battery life.

Because predicted battery life is dependent upon application controlled variables, only the user can estimate predicted battery life in a given design. As long as ambient temperature is held reasonably constant, expected life can be read directly from Figure 7. if the MK48Z02/12 spends an appreciable amount of time at a variety of temperatures, the following equations should be used to estimate battery life.

$$\text{Predicted Battery Life} = \frac{1}{[(TA_1/TT)/BL_1)]+[(TA_2/TT)/BL_2]+\ldots+[(TA_n/TT)/BL_n)]}$$

Where TA_1, TA_2, TA_n = Time at Ambient Temperature 1, 2, etc.

$$TT = \text{Total Time} = TA_1 + TA_2 + \ldots + TA_n$$

BL_1, BL_2, BL_n = Predicted Battery Lifetime at Temp 1, Temp 2, etc. (see Figure 7).

EXAMPLE PREDICTED BATTERY LIFE CALCULATION

A cash register/terminal operates in an environment where the MK48Z02/12 is exposed to temperatures of 30°C (86°F) or less for 3066 hrs/yr; temperatures greater than 25°C, but less than 40°C (104°F), for 5256 hrs/yr; and temperatures greater than 40°C, but less than 70°C (158°F), for the remaining 438 hrs/yr.

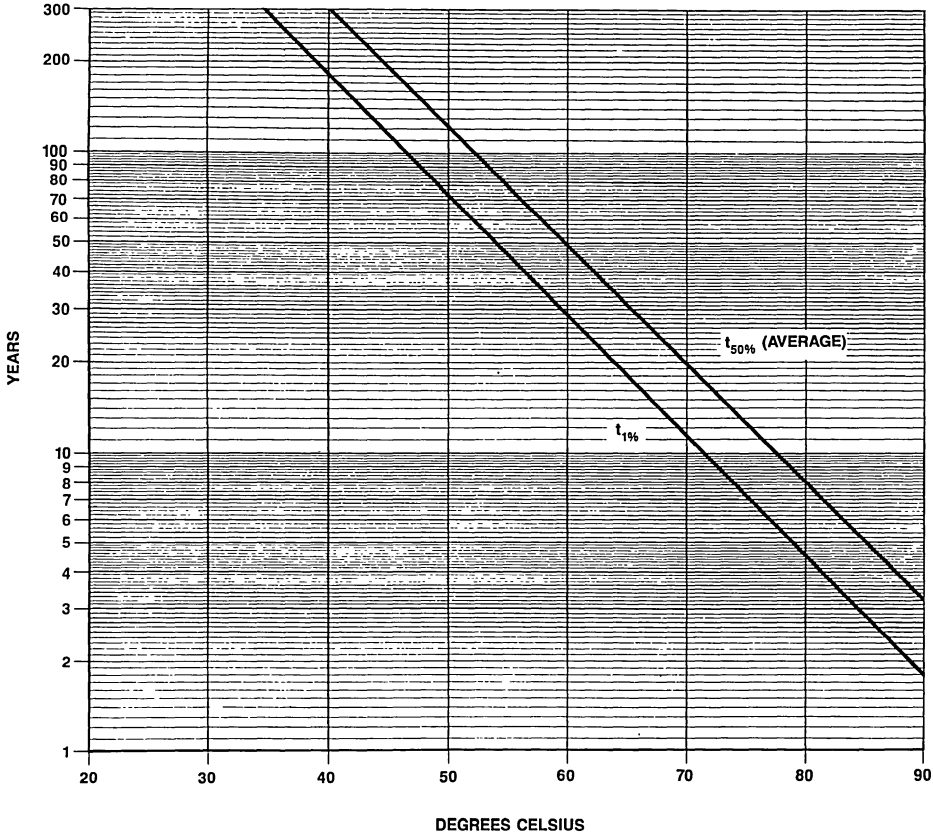
Reading predicted typical life values from Figure 7; BL_1 = 456 yrs., BL_2 = 175 yrs., BL_3 = 11.4 yrs.

Total Time (TT) = 8760 hrs./yr. TA_1 = 3066 hrs./yr. TA_2 =5256 hrs./yr. TA_3 = 438 hrs./yr.

$$\text{Predicted Typical Battery Life} \geq \frac{1}{[(3066/8760)/456]+[(5256/8760)/175]+[(438/8760)/11.4]}$$

$$\geq 116.5 \text{ yrs.}$$

FIGURE 7. MK48Z02/12 PREDICTED BATTERY STORAGE LIFE VS TEMPERATURE



ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Pin Relative To GND ..... −0.3 V to +7.0 V
Ambient Operating (V_{CC} On) Temperature (T_A) ..... 0°C to +70°C
Ambient Storage (V_{CC} Off) Temperature ..... −40°C to +85°C
Total Device Power Dissipation ..... 1 Watt
Output Current Per Pin ..... 20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

CAUTION: Under no conditions can the "Absolute Maximum Rating" for the voltage on any pin be exceeded since it will cause permanent damage. Specifically, do not perform the "standard" continuity test on any input or output pin, i.e do not force these pins below −0.3 V DC.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage (MK48Z02)	4.75	5.50	V	1
V_{CC}	Supply Voltage (MK48Z12)	4.50	5.50	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3 V	V	1
V_{IL}	Logic "0" Voltage All Inputs	−0.3	0.8	V	1,2

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le +70°C$) (V_{CC} (max) $\ge V_{CC} \ge V_{CC}$ (min))

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	3
I_{CC2}	TTL Standby Current ($\overline{E} = V_{IH}$)		3	mA	
I_{CC3}	CMOS Standby Current ($\overline{E} \ge V_{CC}-0.2$ V)		1	mA	
I_{IL}	Input Leakage Current (Any Input)	−1	+1	µA	4
I_{OL}	Output Leakage Current	−5	+5	µA	4
V_{OH}	Output Logic "1" Voltage (I_{OUT} = −1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 2.1 mA)		0.4	V	

CAPACITANCE (T_A = 25°C)

SYM	PARAMETER	MAX	NOTES
C_I	Capacitance on all pins (except D/Q)	7 pF	5
$C_{D/Q}$	Capacitance on D/Q pins	10 pF	4,5

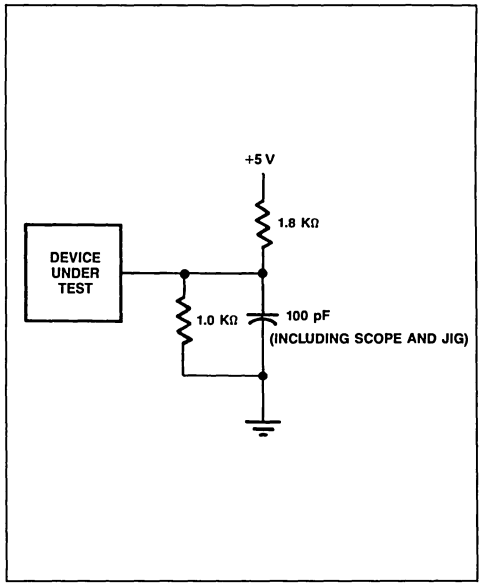
NOTES

1. All voltages referenced to GND.
2. Negative spikes of −1.0 volts allowed for up to 10 ns once per cycle.
3. I_{CC1} measured with outputs open.
4. Measured with $GND \le V_I \le V_{CC}$ and outputs deselected.
5. Effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3 volts and power supply at nominal level.

AC TEST CONDITIONS

Input Levels:	0.6 V to 2.4 V
Transition Times:	5 ns
Input and Output Timing Reference Levels	0.8 V or 2.2 V
Ambient Temperature	0°C to 70°C
V_{CC} (MK48Z02)	4.75 V to 5.5 V
V_{CC} (MK48Z12)	4.5 V to 5.5 V

FIGURE 8. OUTPUT LOAD DIAGRAM



ORDERING INFORMATION

MK48Z X 2 B -XX

DEVICE FAMILY

V_{CC} RANGE

PACKAGE

SPEED

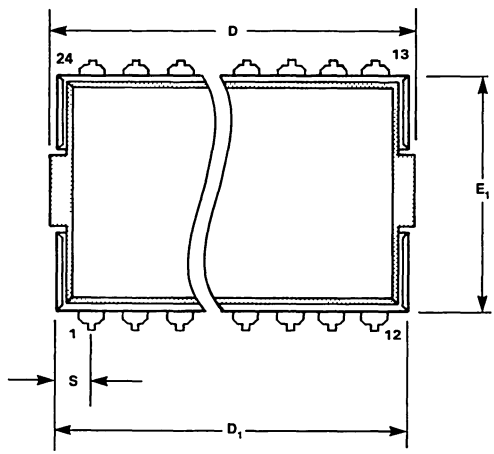
-12 120 NS ACCESS TIME
-15 150 NS ACCESS TIME
-20 200 NS ACCESS TIME
-25 250 NS ACCESS TIME

B PLASTIC WITH BATTERY TOP HAT

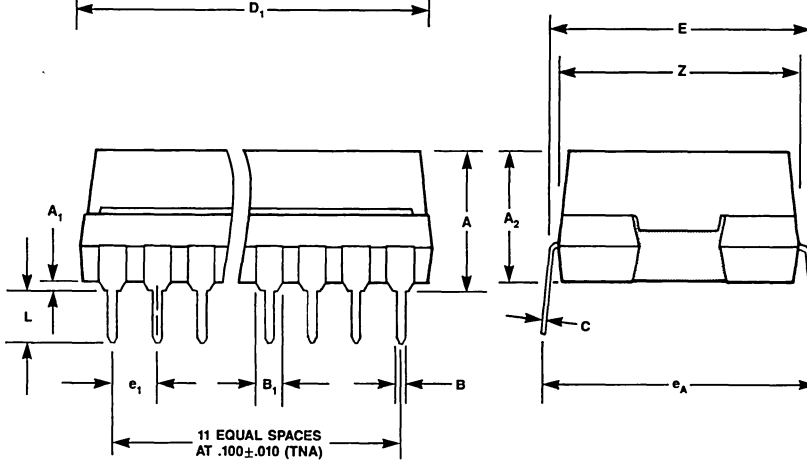
0 +10%/−5%
1 +10%/−10%

PACKAGE DESCRIPTION

B PACKAGE 24 PIN



	Dim.	mm		inches		Notes
		Min	Max	Min	Max	
BATTERY	D	—	32.893	—	1.295	
ONLY	Z	13.97	14.478	.550	.570	
	A	8.128	9.652	.320	.380	
	A_2	7.62	9.144	.300	.360	
	E_1	13.462	13.97	.530	.550	
	B	0.381	0.533	.015	.021	4
	B_1	1.143	1.778	.045	.070	
	C	0.203	0.355	.008	.014	4
24 PIN	D_1	—	32.258	—	1.270	1
PLASTIC	E	13.462	16.256	.530	.640	
D.I.P.	e_A	15.24	17.78	.600	.700	3
ONLY	e_1	2.286	2.794	.090	.110	
	L	3.048	3.81	.120	.150	
	A_1	0.381	0.762	.015	.030	2
	S	1.524	2.286	.060	.090	



NOTES:
1. Overall length includes .010 in. flash on either end of the package
2. Package standoff to be measured per JEDEC requirements
3 Measured from centerline to centerline at lead tips
4. When the solder lead finish is specified, the maximum limit shall be increased by 003 in.

8 K X 8 ZEROPOWER™ SRAM

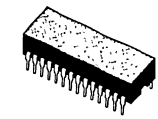
FEATURES

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT AND BATTERY.
- UNLIMITED WRITE-CYCLES.
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME.
- PREDICTED WORST CASE BATTERY LIFE OF 11 YEARS @ 70°C.
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 8K X 8 SRAMS.
- AUTOMATIC POWER-FAIL CHIP DESELECT/WRITE PROTECTION.
- CHOICE OF TWO WRITE PROTECT VOLTAGES
  MK48Z08/09 - 4.50V ≤ V_{PFD} ≤ 4.75
  MK48Z18/19 - 4.20V ≤ V_{PFD} ≤ 4.50 .

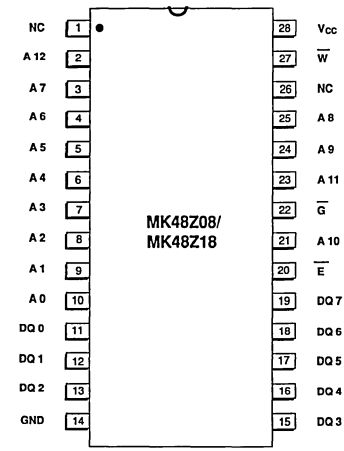
B

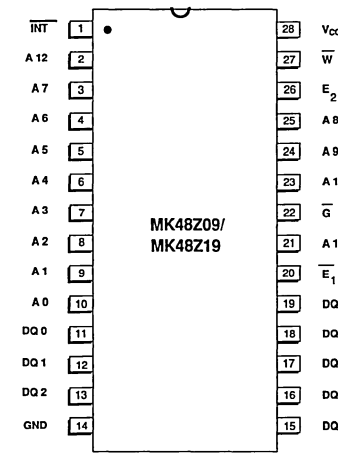
DIP-28

(Plastic with BatteryTop Hat)



PIN CONNECTIONS





DESCRIPTION

Part Number	Access Time	R/W Cycle Time
MK48ZXX-55	55 ns	55 ns
MK48ZXX-70	70 ns	70 ns
MK48ZXX-10	100 ns	100 ns
MK48ZXX-15	150 ns	150 ns
MK48ZXX-20	200 ns	200 ns

PIN NAMES

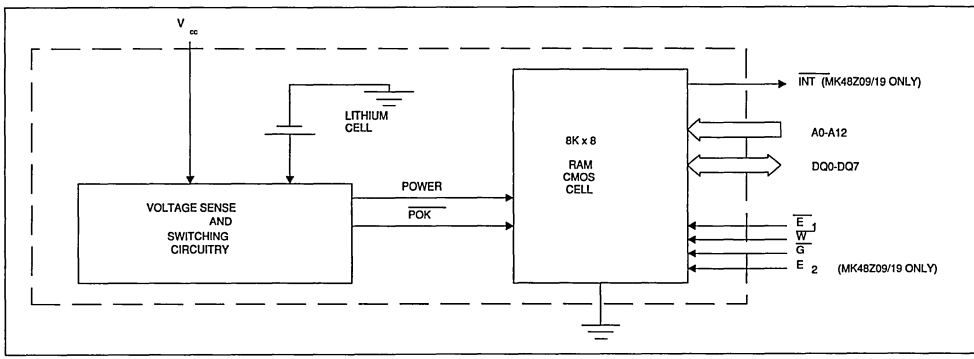
A0-A12	Address Input	Vcc	+5Volts
$\overline{E}$1	Chip Enable	$\overline{W}$	Write Enable
E2	Chip Enable	$\overline{G}$	Output Enable
GND	Ground	DQ0-DQ7	Data In/Data Out
NC	No Connection	$\overline{INT}$	Power Fail Interrupt

DESCRIPTION

The MK48Z08/18/09/19 combines an 8K x 8 full CMOS SRAM and a long life lithium carbon monofluoride battery in a single plastic DIP package. The MK48Z08/18/09/19 is a nonvolatile pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many EPROM and EEPROM sockets, providing the non-volatility of the PROMs without any requirement for special write timing, or limitations on the number of writes that can be performed.

In addition, the MK48Z08/18/09/19 has its own Power-fail Detect circuit. The circuit deselects the device whenever V_{CC} is below tolerance, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}.

FIGURE 1 : MK48Z08 BLOCK DIAGRAM



TRUTH TABLE (MK48Z08/18)

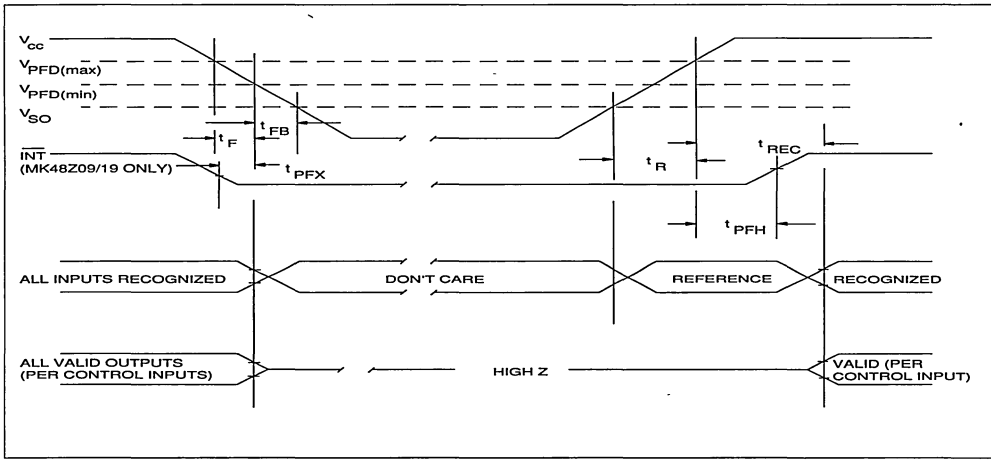
Vcc	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
< Vcc	V_{IH}	X	X	Deselect	High Z	Standby
(Max)	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
> Vcc	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
(MIn)	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD}(MIn)	X	X	X	Deselect	High Z	CMOS
> V_{SO}						Standby
≤ V_{SO}	X	X	X	Deselect	High Z	Battery
						Back-up

TRUTH TABLE (MK48Z09/19)

Vcc	$\overline{E}_1$	E_2	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
< Vcc	V_{IH}	X	X	X	Deselect	High Z	Standby
(Max)	X	V_{IL}	X	X	Deselect	High Z	Standby
	V_{IL}	V_{IH}	X	V_{IL}	Write	DIN	Active
> Vcc	V_{IL}	V_{IH}	V_{IL}	VIH	Read	D_{OUT}	Active
(MIn)	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD}(MIn)	X	X	X	X	Deselect	High Z	CMOS
> V_{SO}							Standby
≤ V_{SO}	X	X	X	X	Deselect	High Z	Battery
							Back-up

NOTE 1 : Refer to Figure 2

FIGURE 2 : POWER DOWN/POWER UP TIMING.



REFERENCE :

Inputs may not be recognized at this time. Caution should be taken to keep $\overline{E}_1$ high or $\overline{E}_2$ low as VCC rises past VSO. **Some system may performs inadvernant write cycles** after V_{CC} rises above normal system operations begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

AC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TIMING) (0°C ≤ T_A ≤ + 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		µs	
t_F	V_{PFD} (Max) to V_{PFD} (Min) Vcc Fall Time	300		µs	2
t_{FB}	V_{PFD} (Min) to V_{SO} V_{CC} Fall Time	10		µs	3
t_R	V_{SO} to V_{PFD} (Max) V_{CC} Rise Time	1		µs	
t_{REC}	$\overline{E}_1$ or $\overline{W}$ at V_{IH} or E_2 at V_{IL} after Power Up	1		ms	
t_{PFX}	$\overline{INT}$ Low to Auto Deselect	10	40	µs	
t_{PFH}	V_{PFD} (Max) to $\overline{INT}$ High		120	µs	4

DC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TRIP POINTS) (0°C ≤ T_A ≤ + 70°C)

		VALUE				
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{PFD}	Power-fail Deselect Voltage (MK48Z08/09)	4.5	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MK48Z18/19)	4.2	4.3	4.5	V	1
V_{SO}	Battery Back-up Switchover Voltage		3.0		V	1
t_{DR}	Expected Data Retention Time	11			YEARS	

NOTES :

1. All voltages referenced to GND.

2. V_{PFD} (MAX) to V_{PFD} (MIN) fall time of less than t_F may result in deselection/write protection not occuring until 200 µs after Vcc passes V_{PFD} (MIN). V_{PFD} (MAX) to (MIN) fall times of less than 10 µs may cause corruption of RAM data.

3. V_{PFD} (MIN) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

4. $\overline{INT}$ may go high anytime after Vcc exceeds V_{SO} and is guaranteed to go high t_{PFH} after Vcc exceeds V_{PFD} (MAX).

READ MODE

The MK48Z08/18/09/19 is in the Read Mode whenever W (Write Enable) is high, $\overline{E}_1$ is low, and E_2 is high (MK48Z09/19). The device architecture allows ripple-through access of data from eight of 65,536 locations in the static storage array. Thus, the unique address specified by the 13 Address inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} after the last address input signal is stable, providing that the Chip Enable and G access times are satisfied.

If Chip Enable or $\overline{G}$ access times are not yet met, valid data will be available at the latter of Chip Enable Access Time (t_{ELQV}) or at Output Enable Access Time (t_{GLQV}). The state of the eight three-state Data I/O signals is controlled by Chip Enable and G. If the Outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address inputs are changed while Chip Enable and G remain low, output data will remain valid for Output Hold from Address (t_{AXQX}) but will go indeterminate until the next Address Access.

AC ELECTRICAL CHARACTERISTICS (READ CYCLE) ($0°C \le T_A \le +70°C$ (Vcc (min) ≤ Vcc ≤ Vcc(max))

		48ZXX-55/70/10/15/20		48ZXX-55		48ZXX-70			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTE
t_{E1LQX}	Chip Enable 1 to Q Low-Z	10						ns	
t_{E2HQX}	Chip Enable 2 to Q Low-Z	10							
t_{AXQX}	Output Hold from Address	5							
t_{GLQX}	Ouput Enable 1 to Q Low-Z	5							
t_{AVAV}	Read Cycle Time			55		70			
t_{AVQV}	Address Access Time				55		70		
t_{E1LQV}	Chip Enable 1 Access Time				55		70		
t_{E2HQV}	Chip Enable 2 Access Time				55		70		
t_{GLQV}	Ouput Enable Access Time				55		70		
t_{E1HQZ}	Chip Enable 1 to Q High-Z				20		20		
t_{E2LQZ}	Chip Enable 2 to Q High-Z				20		20		
t_{GHQZ}	Output Disable to QHigh-Z				15		15		

		48ZXX-10		48ZXX-15		48ZXX-20			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT	NOTE
t_{AVAV}	Read Cycle Time	100		150		200		ns	
t_{AVQV}	Address Access Time		100		150		200		
t_{E1LQV}	Chip Enable 1 Access Time		100		150		200		
t_{E2HQV}	Chip Enable 2 Access Time		100		150		200		
t_{GLQV}	Output Enable Access Time		50		75		100		
t_{E1HQZ}	Chip Enable 1 to Q High-Z		50		75		100		
t_{E2LQZ}	Chip Enable 2 to Q High-Z		50		75		80		
t_{GHQZ}	Output Disable to Q High-Z		40		60		80		

FIGURE 3 : READ TIMING N°.1 (ADDRESS ACCESS)

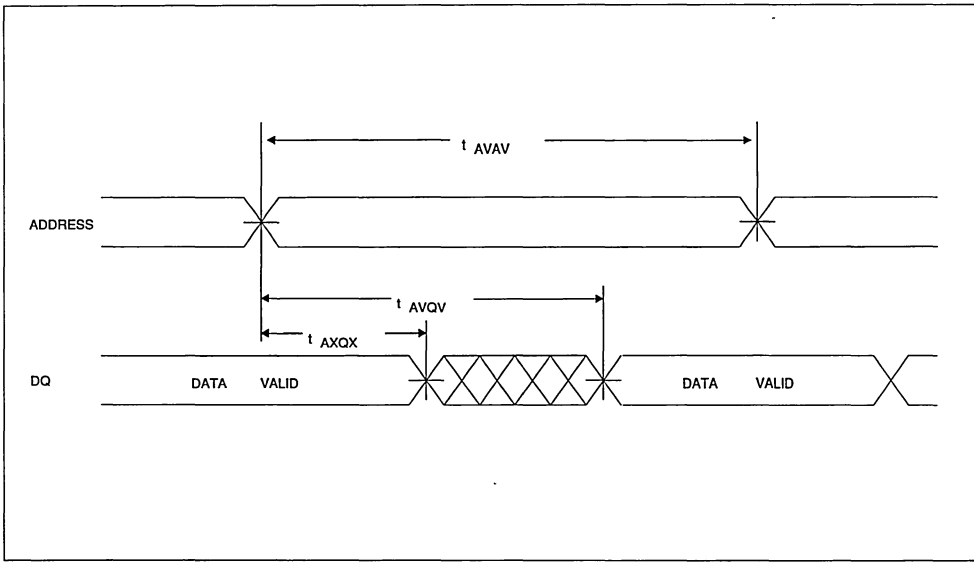
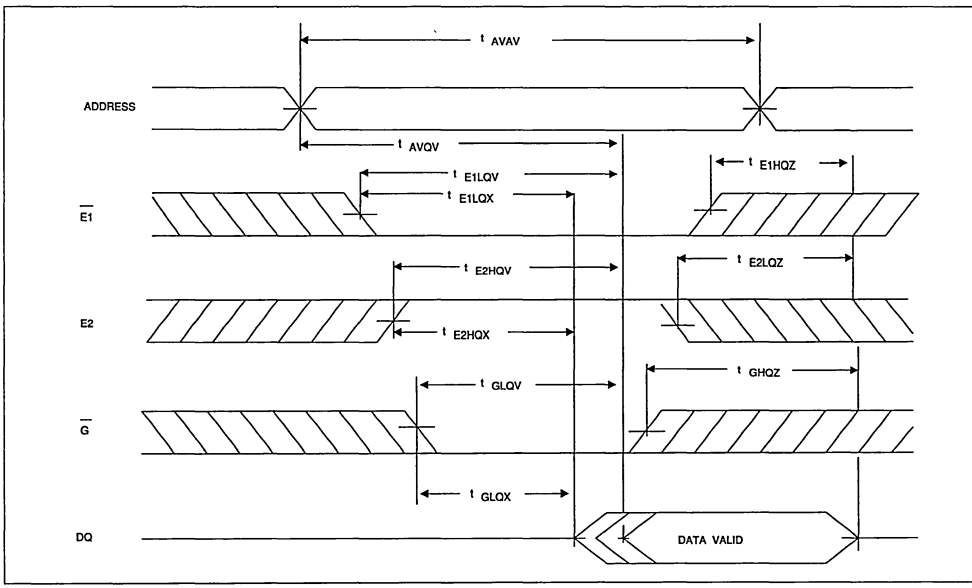


FIGURE 4 : READ TIMING N°.2



WRITE MODE

The MK48Z08/18/09/19 is in the Write Mode whenever Write Enable and Chip Enable are active. The start of a write is referenced to the latter occurring falling edge of $\overline{W}$ or $\overline{E}_1$ or rising edge of E_2 (MK48Z09/19). A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}_1$ or the falling edge of E_2 (MK48Z09/19). The addresses must be held valid throughout the cycle. $\overline{E}_1$ or $\overline{W}$ must return high or E_2 low for minimum of t_{E1HAX} or t_{E2LAX} prior to the initiation of another read or write cycle. Data-in must be valid t_{DVEH} prior to the end of write and remain valid for t_{WHDX} afterward. Because G is a Don't Care in the Write Mode and a low on $\overline{W}$ will return the outputs to High-Z, G can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

AC ELECTRICAL CHARACTERISTICS(WRITE CYCLE)(0°C ≤ T_A ≤ +70°C (Vcc (min) ≤ Vcc ≤ Vcc(max))

		48ZXX-55/70/10/15/20		48ZXX-55		48ZXX-70			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTE
t_{AVWL}	Address Set-Up Time to $\overline{W}$ Low	0							
t_{AVE1L}	Address Set-Up Time to ChipEnable Active	0							
t_{AVE2H}		0							
t_{E1HAX}	Write Recovery from Chip Enable (Address Hold Time)	10							2
t_{E2LAX}		10							2
t_{WHDX}	Data Hold Time	5							1,2
t_{AVAV}	Write Cycle Time			55		70		ns	
t_{AVWH}	Address Valid to $\overline{W}$ High			35		50			
t_{WLWH}	Write Pulse Width			35		50			
t_{WHAX}	Address Hold after End of Write			10		10			1
t_{E1LE1H}	Chip Enable Active to End of Write (W High)			35		50			2
t_{E2HE2L}				35		50			2
t_{DVWH}	Data Valid to End of Write			25		40			1,2
t_{WLQZ}	$\overline{W}$ Low to Q High-Z				30		40		

		48ZXX-10		48ZXX-15		48ZXX-20			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTE
t_{AVAV}	WriteCycle Time	100		150		200			
t_{AVWH}	Address Valid to $\overline{W}$ High	80		130		180			
t_{WLWH}	Write Pulse Width	80		100		150			
t_{WHAX}	Address Hold after End of Write	10		10		10		ns	1
t_{E1LE1H}	Chip Enable Active to End of Write (W High)	80		130		180			2
t_{E2HE2L}		80		130		180			2
t_{DVWH}	Data Valid to End of Write	50		70		80			1,2
t_{WLQZ}	$\overline{W}$ Low to Q High-Z		50		75		100		

NOTES : **1.** In a $\overline{W}$ Controlled Cycle / **2.** In a $\overline{E}_1$, E2 Controlled Cycle

FIGURE 5 : WRITE CONTROL WRITE CYCLE TIMING

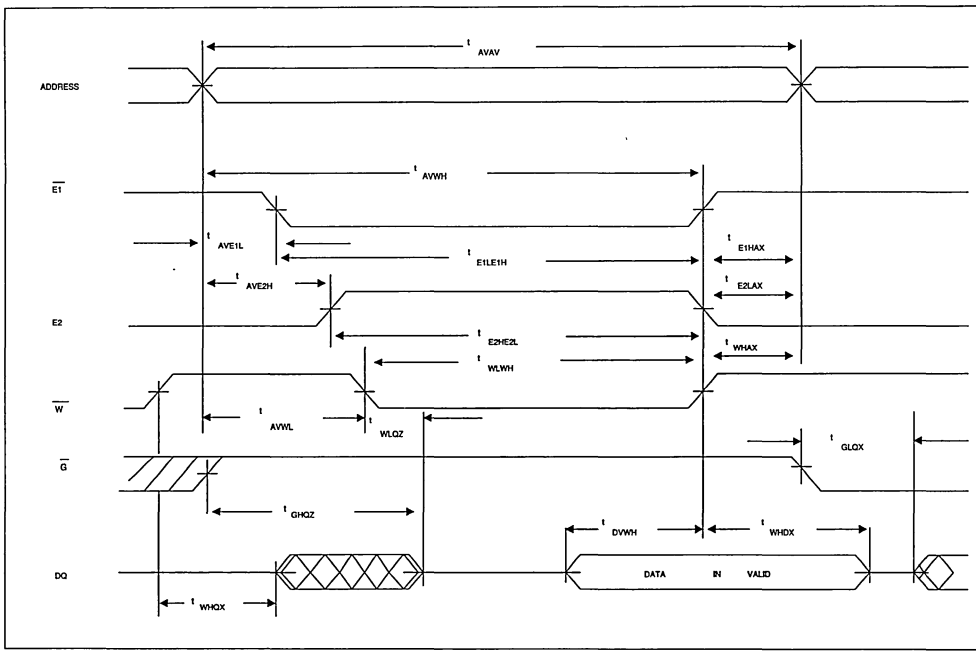
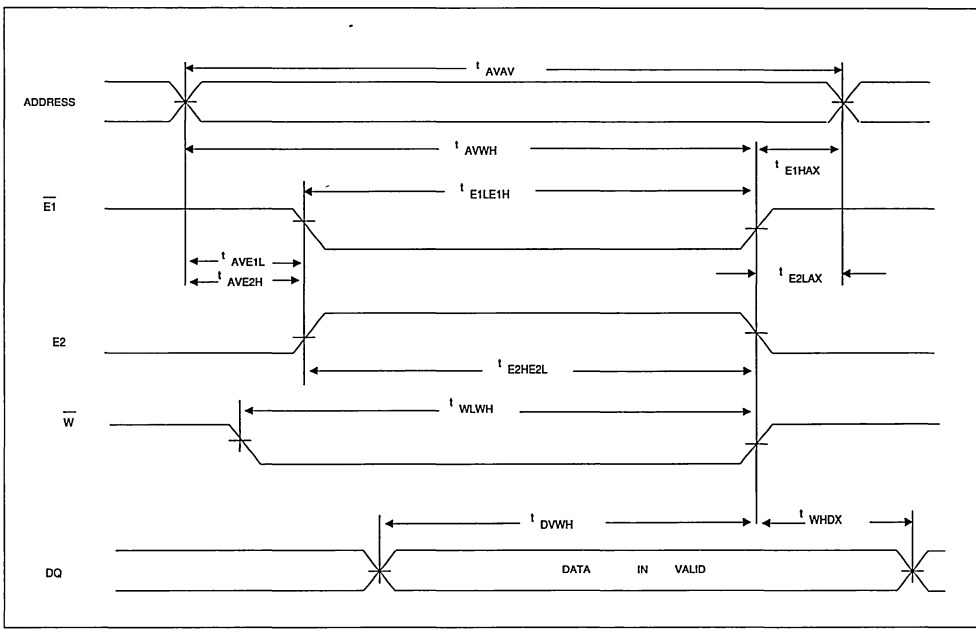


FIGURE 6 : CHIP ENABLE CONTROL WRITE CYCLE TIMING



DATA RETENTION MODE

With V_{CC} applied, the MK48Z08/18/09/19 operates as a conventional BYTEWIDE static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window.

Note: A mid-write cycle power failure may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The MK48Z08/18/09/19 may respond to transient noise spikes that reach into the deselect window if this should occur during the time the device is sampling V_{CC}. Therefore decoupling of the power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max). Caution should be taken to keep $\overline{E}_1$ high (MK48Z08/18) or E_2 low (MK48Z09/19) as V_{CC} rises past V_{SO} as some systems may perform inadvertant write cycles after V_{CC} rises but before normal system operation begins.

POWER FAIL INTERRUPT

The MK48Z09/19 continuously monitors Vcc. When Vcc fall to the power fail detect trip point of the MK48Z09/19 an interrupt is immediatly generated. An internal clock provides a delay no less than 10µS but no greater than 40µS before automatically deselecting the MK48Z09/19.

PREDICTING BACK-UP SYSTEM LIFE

The useful life of the battery in the MK48Z08/18/09/19 is expected to ultimately come to an end for one of two reasons: either because it has been discharged while providing current to an external load; or because the effects of aging render the cell useless before it can actually be discharged. Fortunately, these two effects are virtually unrelated, allowing discharge, or Capacity Consumption, and the effects of aging, or Storage Life, to be treated as two independent but simultaneous mechanisms, the earlier of which defines Back-up System life.

With V_{CC} on, the battery is disconnected from the RAM and aging effects become the determining factor in battery life. With V_{CC} off, leakage currents in the RAM provide the only load on the Battery during battery back-up. For the MK48Z08/18/09/19, the leakage currents are so low that the Back-up System life of the device is simply the Storage Life of the cell. The Storage Life of the cell is a function of temperature.

PREDICTING STORAGE LIFE

Figure 7 illustrates how temperature affects Storage Life of the MK48Z08/18/09/19 battery. The life of the battery is controlled by temperature and is virtually unaffected by leakage currents drawn by the MK48Z08/18/09/19.

Storage Life predictions presented in Figure 7 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's on going battery testing since it began in 1982, we believe the chance of such failure mechanisms surfacing is extremely small. For the purpose of the testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.4 volt closed-circuit voltage across a 250K load resistance.

A Special Note: The summary presented in Figure 8 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final; they can be expected to change as yet more data becomes available. We believe that future read points of life test presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 7. The are labeled "Average" ($t_{50\%}$) and ($t_{1\%}$). These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure 7 indicates that a particular MK48Z08/18/09/19 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience a battery failure within 11 years; 50% of them can be expected to experience a failure within 20 years.
The $t_{1\%}$ figure represents the practical onset of wear out, and is therefore suitable for use in what would normally be thought of as a worst-case analysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning at the date of manufacture. Each MK48Z08/18/09/19 is marked with a five digit manufacturing date code in the form XYYWW. The first digit is the assembly location code (example: 98625= assembled in Muar Malasia, 1986, week 25).

Calculating Predicted Storage Life of the Battery

As Figure 7 indicates, the predicted Storage Life of the battery in the MK48Z08/18/09/19 is a function of temperature.

Because the ambient temperature profile is dependent upon application controlled variables, only the user can estimate predicted Storage Life in a given design. As long as ambient temperature is held reasonably constant, expected Storage Life can be read directly from Figure 7. If the MK48Z08/18/09/19 spends an appreciable amount of time at a variety of temperatures, the following equation should be used to estimate Storage Life.

Example Predicted Storage Life Calculation

Predicted Storage Life = $1 \div \{ [(TA_1 \div TT) \div SL_1] + [(TA_2 \div TT) \div SL_2] + ... + [(TA_N \div TT) \div SL_N] \}$

Where TA_1, TA_2, TA_N, = Time at Ambient Temperature 1, 2, etc.

$TT = Total\ Time = TA_1 + TA_2 + ... + TA_N$

SL_1, SL_2, SL_N = Predicted Storage Life at Temp. 1, Temp. 2, etc. (See Figure 7)

Example Predicted Storage Life Calculation

A cash register/terminal operates in an environment where the MK48Z08 is exposed to temperatures of 55°C or less for 8322 hrs./yr.; and temperatures greater than 60°C, but less than 70°C, for the remaining 438 hrs./yr.

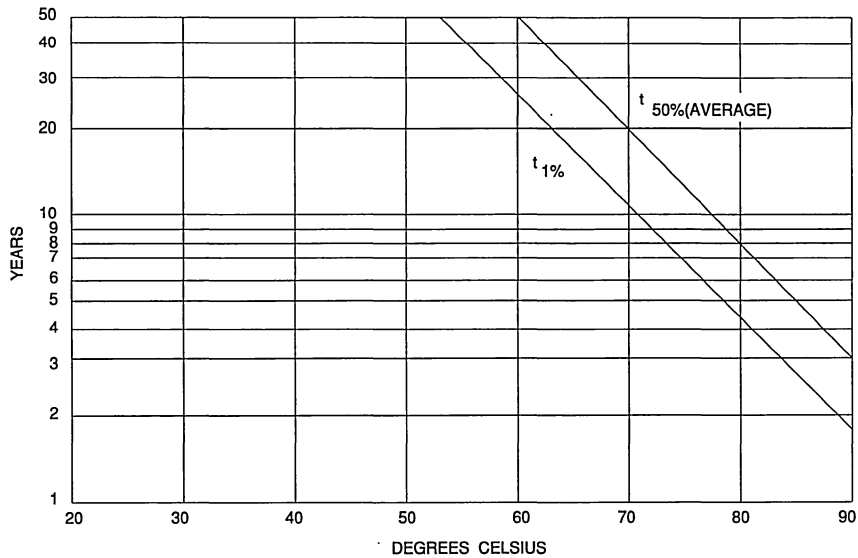
Reading Predicted $t_{1\%}$ values from Figure 7; SL_1 = 41 yrs., SL_2 = 11.4 yrs.,

Total Time (TT) = 8760 hrs./yr. TA_1 = 8322 hrs./yr. TA_2 = 438 hrs./yr. .

Predicted Typical Storage Life $\geq 1 \div \{ [(8322 \div 8760) \div 41] + [(438 \div 8760) \div 11.4]$

Predicted Typical Storage Life $\geq$ 36 years

FIGURE 7 : PREDICTED BATTERY STORAGE LIFE VS. TEMP.



ABSOLUTE MAXIMUM RATINGS *

PARAMETER	VALUE	UNIT
Total Power Dissipation	1.0	W
Output Current per Pin	20	mA
Voltage on any Pin Relative to GND	-0.3 to + 7.0	V
Ambient Operating (Vcc on) Temperature (T_A)	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION
Negative undershoots below -0.3 volts are not allowed on any pin while in the Battery Back-up mode.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
Vcc	Supply Voltage (MK48Z08/09)	4.75	5.5	V	1
Vcc	Supply Voltage (MK48Z18/19)	4.5	5.5	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	Vcc + 0.3v	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3	0.8	V	1,2

DC ELECTRICAL CHARACTERISTICS(0°C≤ T_A ≤+70°C) (Vcc (min) ≤ Vcc ≤ Vcc (max))

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
Icc1	Average Vcc Power Supply Current		80,125	mA	3,6
Icc2	TTL Standby Current ($\overline{E}_1$= V_{IH} or E_2=V_{IL})		3	mA	
Icc3	CMOS Standby Current ($\overline{E}_1$= Vcc -0.2v)		3	mA	4
I_{IL}	Input Leakage Current (Any Input)	-1	+1	µA	5
I_{OL}	Ouput Leakage Current	-5	+5	µA	5
V_{OH}	Output Logic "1" Voltage (I_{OUT} =-1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +2.1 mA)		0.4	V	
V_{INT}	$\overline{INT}$ Logic "0" Voltage (I_{OUT} = +0.5 mA)		0.4	V	

NOTES :

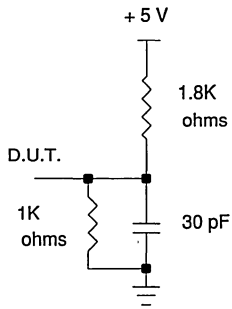
1. All voltages referenced to GND.
2. Negative spikes of -1.0 volts allowed for up to 10 ns once per Cycle.
3. I_{CC1} measured with outputs open.
4. 1mA typical.
5. Measured with Vcc ≥ V_I ≥ GND and outputs deselected.
6. 80mA@ 100,150,200ns, & 125mA@ 55,70ns

AC TEST CONDITIONS

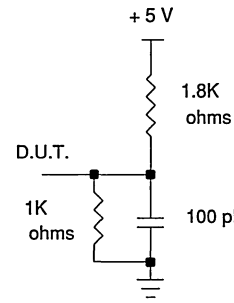
INPUT LEVELS _____ 0.0v to 3.0v
TRANSITION TIMES _____ 5ns
INPUT AND OUTPUT TIMING
REFERENCE LEVELS _____ 1.5v

FIGURE 8 : OUPUT LOAD DIAGRAM

MK48Z08/18/09/19-55/70



MK48Z08/18/09/19-10/15/20



CAPACITANCE (T_A = 25°C)

SYMBOL	PARAMETER	MAX	UNITS	NOTES
CI	Capacitance On All Pins (except DQ)	10.0	pF	1
CQ	Capacitance On DQ Pins	10.0	pF	1,2

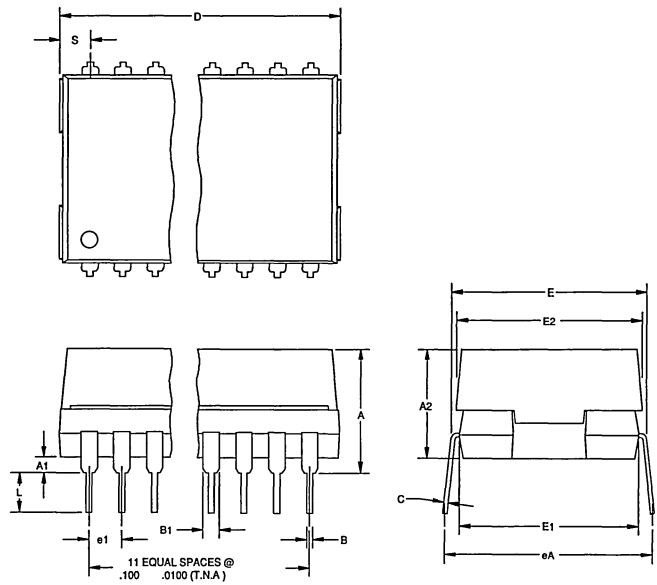
NOTE :

1. Effective capacitance calculated from the equation $C = I \Delta t/\Delta V$ with ΔV = 3 volts and power supply at 5.0V 2.
Measured with outputs deselected.

ORDERING INFORMATION

PART NUMBER	ACCESS TIME (ns)	SUPPLY VOLTAGE
MK48Z08-B55	55	5V ±10%
MK48Z08-B70	70	5V ±10%
MK48Z08-B10	100	5V ±10%
MK48Z08-B15	150	5V ±10%
MK48Z08-B20	200	5V ±10%
MK48Z18-B55	55	5V +10 -5%
MK48Z18-B70	70	5V +10 -5%
MK48Z18-B12	100	5V +10 -5%
MK48Z18-B15	150	5V +10 -5%
MK48Z18-B20	200	5V +10 -5%
MK48Z09-B55 (PFI)	55	5V ±10%
MK48Z09-B70 (PFI)	70	5V ±10%
MK48Z09-B10 (PFI)	100	5V ±10%
MK48Z09-B12 (PFI)	150	5V ±10%
MK48Z09-B20 (PFI)	200	5V ±10%
MK48Z19-B55 (PFI)	55	5V +10 -5%
MK48Z19-B70 (PFI)	70	5V +10 -5%
MK48Z19-B10 (PFI)	100	5V +10 -5%
MK48Z19-B15 (PFI)	150	5V +10 -5%
MK48Z19-B20 (PFI)	200	5V +10 -5%

FIGURE 9 : PACKAGE MECHANICAL DATA



DIM	INCHES		NOTES
	MIN	MAX	
A	.320	.380	2
A1	.015	.030	2
A2	.300	.360	
B	.015	.021	3
B1	.045	.070	
C	.008	.012	3
D	-	1.495	1
E	.530	.640	
E1	.530	.550	
E2	.550	.570	
e1	.090	.110	
eA	.600	.700	
L	.120	.150	
S	.060	.090	

NOTES

1 OVERALL LENGTH INCLUDES FLASH AND PROJECTIONS ON EITHER END OF PACKAGE

2 PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS

3 THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED

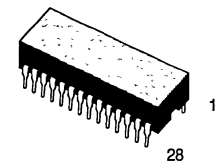
SGS-THOMSON MICROELECTRONICS

MK48Z30/30A(B) -10/12/15

32 K X 8 ZEROPOWER™ RAM

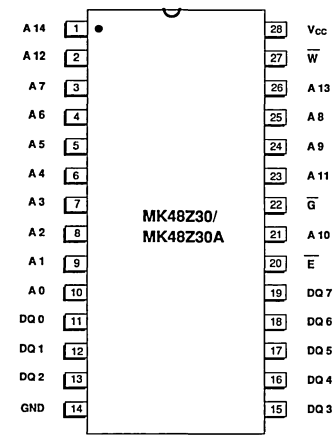
ADVANCE DATA

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT AND BATTERY.
- UNLIMITED WRITE-CYCLES.
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME.
- PREDICTED BATTERY BACK-UP OF 10 YEARS @ 25°C.
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 32K X 8 SRAMS.
- AUTOMATIC POWER-FAIL CHIP DESELECT / WRITE PROTECTION.
- DUAL WRITE PROTECT VOLTAGE: MK48Z30:4.75VOLTS. MK48Z30A: 4.50 VOLTS.



B
28-DIP
Plastic Package

PIN CONNECTIONS



DESCRIPTION

Part Number	Access Time	R/W Cycle Time	Vcc
MK48Z30B - 10	100 ns	100 ns	+10 / -5 %
MK48Z30 B - 12	120 ns	120 ns	+10 / -5 %
MK48Z30 B - 15	150 ns	150 ns	+10 / -5 %
MK48Z30AB-10	100 ns	100 ns	+10 / -10%
MK48Z30AB-12	120 ns	120 ns	+10 / -10%
MK48Z30AB-15	150 ns	150 ns	+10 / -10%

PIN NAMES

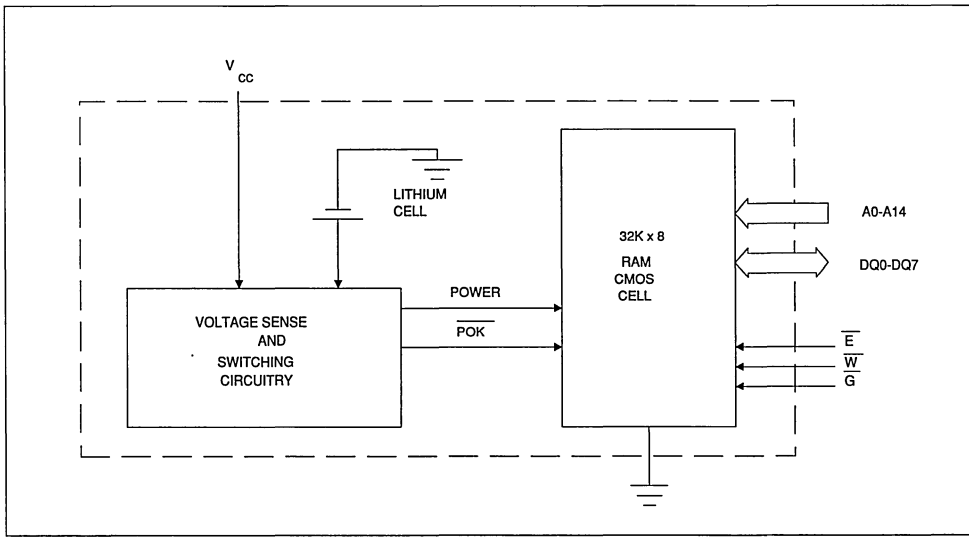
A0-A14	Address Input	Vcc	+5Volts
$\overline{E}$	Chip Enable	$\overline{W}$	Write Enable
		$\overline{G}$	Output Enable
GND	Ground	DQ0-DQ7	Data IN/Data Out

DESCRIPTION

The MK48Z30/30A combines an 32K x 8 full CMOS S RAM and 2 long life carbon mono-fluoride batteries in a single plastic DIP package.The MK48Z30/30A is a nonvolatille pin and function equivalent to any JEDEC standard 32Kx 8 SRAM. it also easily fits into many EPROM and EEPROM sockets, providing the non-volatility of the PROM s without any requiment for special writetiming,or limitations on the number of writes that can be performed.

In addition,the MK48Z30/30A has its own Powerfail Dectect Circuit. The circuit deselect s the device whenever V_{CC} is below tolerance, providing a hight degree of data security in the midst of unpredictable system operations brought on by low V_{CC}.

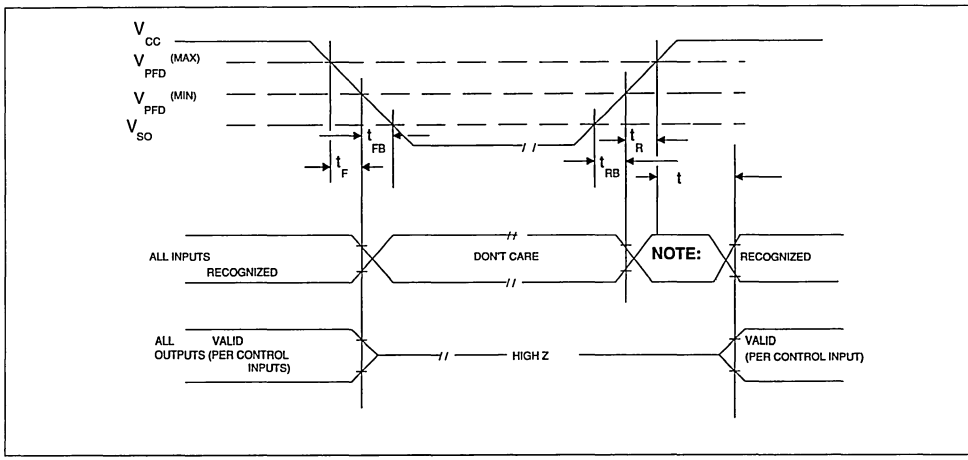
FIGURE 1 : MK48Z30/30A BLOCK DIAGRAM



TRUTH TABLE (MK48Z30/30A)

Vcc	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
< Vcc	V_{IH}	X	X	Deselect	High Z	Standby
(Max)	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
Vcc	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
(Mln)	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD} (Mln) > V_{SO}	X	X	X	Deselect	High Z	CMOS Standby
≤ V_{SO}	X	X	X	Deselect	High Z	Battery Back-up Mode

FIGURE 2 : POWER UP/DOWN TIMING



AC ELECTRICAL CHARACTERISTICS (POWER -UP/DOWN TIMING) (0°C ≤ T_A ≤ +70°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} Before Power Down	0		ns	
t_F	V_{PFD} (Max) to V_{PFD} (Min) V_{CC} FallTime	300		µs	2
t_{FB}	V_{PFD} (Min) to V_{SO} V_{CC} FallTime	10		µs	3
t_{RB}	V_{SO} to V_{PFD} (Min) V_{CC} Rise Time	1		µs	
t_R	V_{PFD} (Min) to V_{PFD} (Max) V_{CC} Rise Time	0		µs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} After Power Up	5		ms	

DC ELECTRICAL CHARACTERISTICS (POWER-UP/ DOWN TRIP POINTS) (0°C ≤ T_A ≤ +70°C)

SYMBOL	PARAMETER	VALUES			UNITS	NOTES
		MIN	TYP	MAX		
V_{PFD}	Power- Fail Deselect Voltage (MK48Z30)	4.5	4.6	4.75	V	1
V_{PFD}	Power- Fail Deselect Voltage (MK48Z30A)	4.2	4.3	4.5	V	1
V_{SO}	Battery Back-Up Switchover Voltage		3.0		V	1
t_{DR}	Expected Data Retention Time	10			YEARS	4

NOTES:

1 . All voltages referenced to GND.

2 . V_{PFD}(Max) to V_{PFD}(Min) fall times of less $t_F$may result in deselection/write protection not occuring until 40 µs after V_{CC} passes V_{PFD} (Min). V_{PFD} (Max)to (Min) fall times of less than 10 µs may cause corruption of RAM data.

3 . V_{PFD}(Min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data.

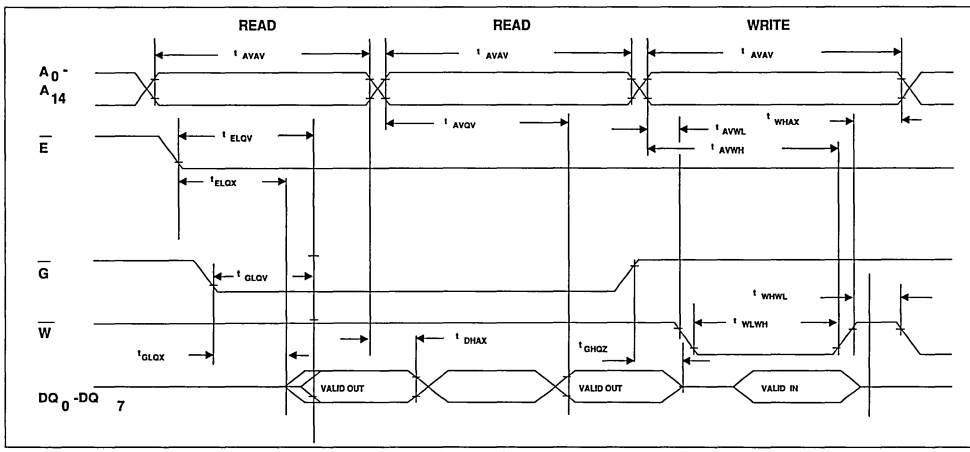
4 . 25 °C ambient condition.

READ MODE

The MK48Z30/30A is in the Read Mode whenever W (Write Enable) is high and E is low. The device architecture allows ripple-through access of data from eight of 262,144 locations in the static storage array. Thus, the unique address specified by the 14 Address inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} after the last address input signal is stable, providing that the Chip Enable and G access times are satisfied. If Chip Enable or G access times are not met, valid data will be available at the Chip Enable Access Time (t_{ELQV}) or at Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by Chip Enable and G. If the Outputs are activated before t_{AA}, the data lines will be driven to an indeterminate state until tAVQV. If the Address inputs are changed while Chip Enable and G remain low, output data will remain valid for Output Data Hold Time (t_{DHAX}) but will go indeterminate until the next Address Access.

FIGURE 3 : READ CYCLE TIMING



AC ELECTRICAL CHARACTERISTICS (READ CYCLE)

(0°C≤T_A≤ + 70°C, VCC = 5.0 V +10% / -5%or -10%)

ALT. SYMBOL	STD. SYMBOL	PARAMETER	48ZXX-10		48ZXX-12		48ZXX-15		UNIT	NOTE
			MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	t_{AVAV}	Read Cycle Time	100		120		150		ns	
t_{AA}	t_{AVQV}	Address Access Time		100		120		150		
t_{CEA1}	t_{ELQV}	$\overline{E}_1$ Access Time		100		120		150		
t_{CEZ}	t_{EHQZ}	Chip Enable Off Time		50		60		75		
t_{OEA}	t_{GLQV}	Output Enable Access Time		50		60		75		
t_{OEZ}	t_{GHQZ}	Output Enable Data Off Time		40		50		60		
t_{OEL}	t_{GLQX}	Output Enable To Q Low-z	5		5		5			
t_{CEL}	t_{ELQX}	Chip Enable To Q Low-z	10		10		10			
t_{OH}	t_{DHAX}	Output Hold From Address	5		5		5			

WRITE MODE

The MK48Z30/30A is in the Write Mode whenever Write Enable and Chip select are active. The start of a write is referenced to the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high or for minimum of t_{WR} prior to the initiation of another read or write cycle. Data-in must be valid t_{DVEH} prior to the end of write and remain valid for t_{WHDX} afterward.

AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE)

(0°C≤T_A≤+ 70°C, V_{CC} = 5.0 V +10% / -5% or -10%)

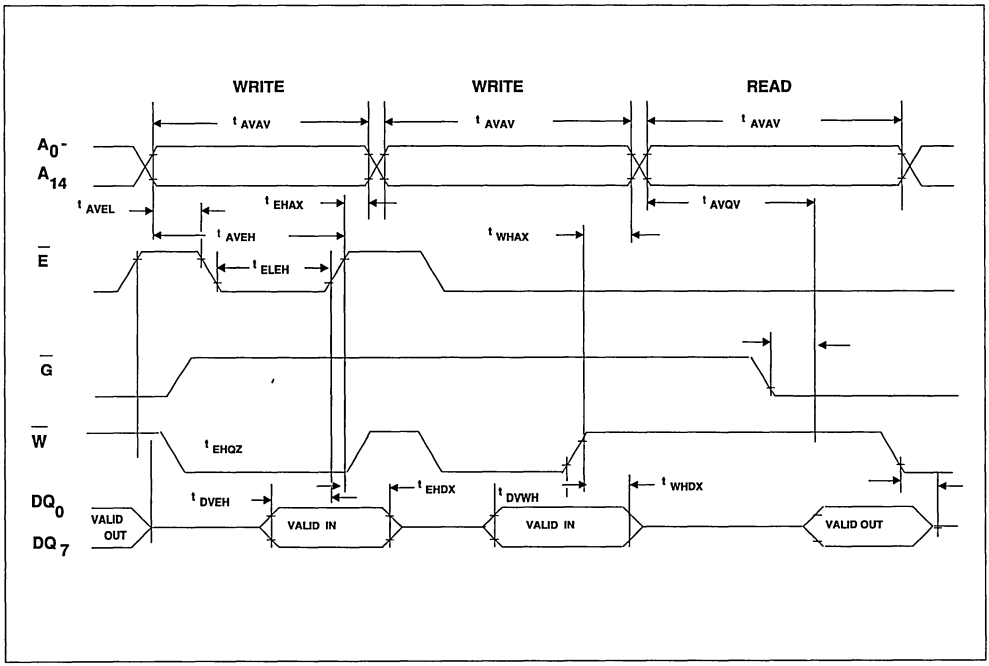
ALT. SYMBOL	STD. SYMBOL	PARAMETER	48ZXX-10		48ZXX-12		48ZXX-15		UNITS	NOTE
			MIN	MAX	MIN	MAX	MIN	MAX		
t_{WC}	t_{AVAV}	Write Cycle Time	100		120		150		ns	
t_{AS}	t_{AVWL}	Address Setup Time $\overline{W}$ Low	0		0		0			
t_{AS}	t_{AVEL}	Address Setup Time $\overline{E}$ Low	0		0		0			
t_{CEW}	t_{ELEH}	Chip Enable to End Of Write	80		100		130			
t_{AW}	t_{AVWH}	Address Valid to End Off Write	80		100		130			
t_{AW}	t_{AVEH}	Address Valid to End Off Write	80		100		130			
t_{WEW}	t_{WLWH}	Write Pulse Width	50		70		100			
t_{TCEZ}	t_{EHQZ}	$\overline{E}$ Data of Time		50		60		75		
t_{WEZ}	t_{WLQZ}	$\overline{W}$ Data of Time		50		60		75		
t_{WR}	t_{WHAX}	$\overline{W}$ High to Address Change	10		10		10			1
t_{WR}	t_{EHAX}	$\overline{E}$ High to Address Change	10		10		10			2
t_{WR}	t_{WHWL}	$\overline{W}$ High to $\overline{W}$ Low Next Cycle	10		10		10			
t_{DS}	t_{DVWH}	Data Setup Time to $\overline{W}$ High	50		60		70			1
t_{DS}	t_{DVEH}	Data Setup Time to $\overline{E}$ High	50		60		70			2
t_{DH}	t_{WHDX}	Data Hold Time $\overline{W}$ High	5		5		5			1
t_{DH}	t_{EHDX}	Data Hold Time $\overline{E}$ High	5		5		5			2

NOTES:

1 . In a $\overline{W}$ Controlled Cycle.

2 . In a $\overline{E}$ Controlled Cycle.

FIGURE 4 : WRITE CYCLE TIMING



DATA RETENTION MODE

With V_{CC} applied, the MK48Z30/30A operates as a conventional BYTEWIDE static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window.

A mid-write cycle power failure may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F.

The power switching circuit connects external V_{CC} to the RAM and disconnects the batteries when V_{CC} rises above V_{SO}. Normal RAM opetration can resume t_{REC} after V_{CC} exceeds V_{PFD}(max). Cuation should be taken to kepp $\overline{E}$ or W hight as V_{CC} rises past V_{PFD}(min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

BATTERY LONGIVITY

The useful life of the MK48Z30/30A is expected to ultimately come to an end for one of two reasons: either because the effects of aging render the cell useless before it can actually be discharged; or because they have been discharged while providing current to an external load.

With V_{CC} on, the batteries are disconnected from the RAM and aging effects become th determining factor in battery-Storage Life.

With V_{CC} off, the MK48Z30/30A initates back-up mode by swithching power from V_{CC}input to the batteries.The leakage current drawn by the RAM represents the only load on the batteries and is referred as the Capacity Consomption

* Storage Life

Figure 5 illustrates how temperature affects Storazge Life of the MK48Z30 batteries. The figure graphs the battery life as a function of temperature and the percentage of time VCC remains on.

Note that regardless off V_{CC} Duty Cycle, Storage Life always decrases with an increase in temperature.

With V_{CC} continuously off, representing a 0% Duty Cycle, the Storage Life of the batteries is short due to the load of the RAM which draws current (consumes batteries capacity).

.With V_{CC} continously on, representing a 100% Duty Cycle (t1%), the Storage Life of the batteries is long due to the RAM being disconnected from the batteries and drawning no current.

Two End-of- Life curves are presented in the Figure 6. They are labeled "100% Duty Cycle - Storage " (t1%), and "Average" (t50%). These terms are related to probability that a given number of failures will have accumulated by a particular point in time. If, for example, the batteries expected life at 70°C is an issue, Figure 5 indicates that an MK48Z30/30A has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year time.

Back-Up Life Calculation

$$\text{Back-Up Life} = \frac{1}{\{[(TA_1 \div TT) \div BL_1] + [(TA_2 \div TT) \div BL_2] + \ldots + [(TAN \div TT) \div BL_N]\}}$$

Where TA_1, TA_2, TA_N, = Time at Ambient Temperature 1, 2, ect....

TT = Total Time = $TA_1 + TA_2 + \ldots + TA_N$

BL_1, BL_2, BL_N = Back-Up System Life at Temp.1, Temp.2, ect... (See Figure 5)

Example Back-Up Life Calculation

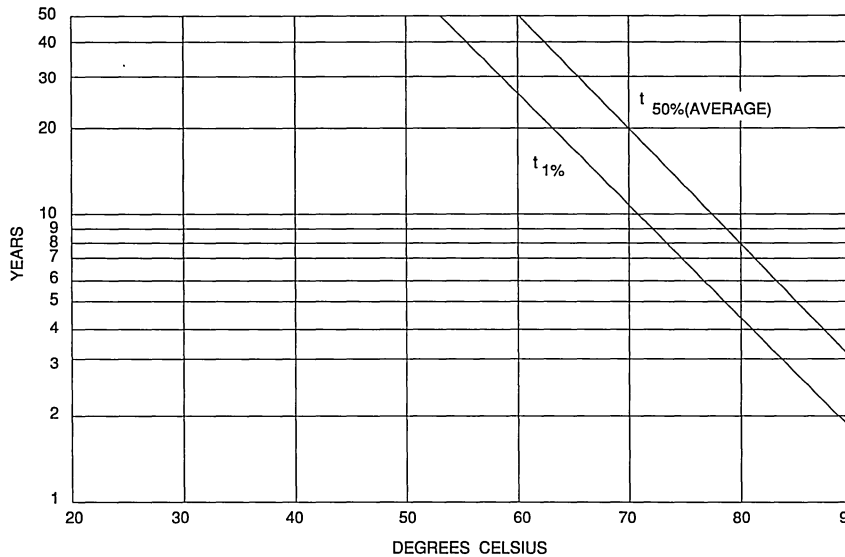
A cash register operates in an environment where the MK48Z30/30A is exposed to a 40°Ctemperatures at 50% power Duty Cycle for 5 days. The 6th day, the MK48Z30/30A is exposed to a 55°C temperature at 100% Duty Cycle. The 7th day, the regester is not used and is exposed to 25°C at 0% Duty Cycle.

Reading Predicted values from Figure 6 ; BL_1 = 4 yrs, BL_2 = 40 yrs, BL_3 = 5 yrs.
Total Time (TT) = 8760 hrs./yr. TA_1 = 6264 hrs/yr, TA_2 = 1248 hrs/yr, TA_3 = 1248 hrs/yr.

$$\text{Back-Up Life} = \frac{1}{\{[(6264/8760) \div 8] + [(1248/8760) \div 40] + [(1248/8760) \div 10]\}}$$

$$= 9.3 \text{ years}$$

FIGURE 5 : PREDICTED BATTERY STORAGE LIVE VS. TEMPERATURE AND V_{CC} DUTY CYCLE

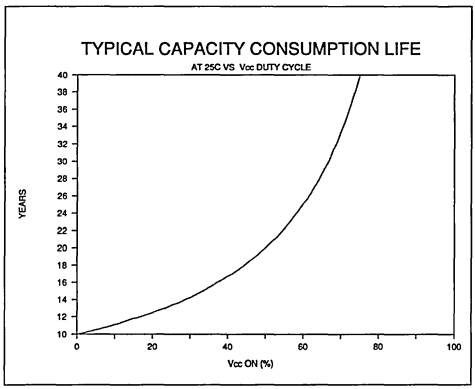


*** Capacity Consumption Life**

The MK48Z30/30A bettery cells have a minimun rated capacity of 35 mAh each. The RAM, battery-backed mode, places a nominal load of 825 nA at 25 °C. At that rate, the MK48Z30/30A will consume the capacity of the battery cells in 84,848 hours or about 10 years. But as Figure 6 Shows, Capacity Consumption can be spread over a much longer period of time whem the V_{CC} Duty Cycle is increased.

Capacity Consumption Life can be estimated by reading 0% V_{CC} Duty Cycle Capacity Consumption Life directly from Figure 6 and dividing by one minus the expected V_{CC} Duty Cycle.

FIGURE 6



For example, the Capacity Consumption Life of an MK48Z30/30A at 25°C and at 20% V_{CC} Duty Cycle is:

10 Years / (1-0.20) = 12.5 Years

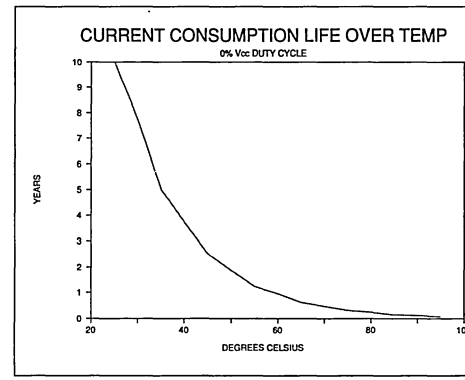
Naturally, battery-backed mode current varies with temperature. As Figure 7 indicates, the Current Consumption Life of the MK48Z30/30A in battery-Backed mode is also function of the temperature. Therefore, to calculate the Capacity Consumption Life of the MK48Z30/30A over temperature, the same equation is used except the corresponding Current Comnsumption Life for a specific temperature, derived from Figure 7 is substituted.

*** Back-Up Life**

The Back-Up Life of the MK48Z30/30A is defined as the combination of the devices'operational factors as previously mentioned. Tha is, the combination of the Storage Life and Capacity Consumption of the batteries. Both of these factors have been graphically represented in the Figure 6 and are a function of the temperature.

Calculations of Back-Up Life begins relative to the first day power is applied to the device. Each MK48Z30/30A RAM is disconnected from the battery at time of manufacture to insure battery longevity. Only after V_{CC} is initially applied is Back-Up Life affected.

FIGURE 7



Because the ambient temperature is dependent upon application controlled variables, only the user can estimate Back-Up Life in a given design. As long as ambient temperature is held reasonably constant, expected Back-Up Life can be read directly from Figure 5 If the MK48Z30/30A spends an appreciable amount of time at a variety of temperatures, the following equation should be used to estimate Back-Up Life.

ABSOLUTE MAXIMUM RATINGS *

PARAMETER	VALUES	UNITS
Voltage on any Pin Relative to GND	-0.3 to + 7.0	V
Ambient Operating (V_{CC} On) Temperature (t_A)	0 to 70	°C
Ambient Storage (V_{CC} Off) Temperature	-40 to +70	°C
Total Device Power Dissipation	1.0	W
Output Current Per Pin (one Output at a Time)	50	mA

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is net implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION

Negative undershoots below -0.3 volts are not allowed on any pin while in the Battery Back-up mode

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage (MK48Z30)	4.75	5.5	V	1
V_{CC}	Supply Voltage (MK48Z30A)	4.5	5.5	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	Vcc + 0.3v	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3	0.8	V	1,2

DC ELECTRICAL CHARACTERISTICS (0°C≤ T_A ≤+70°C) (Vcc (min) ≤ Vcc ≤ Vcc (max))

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		90	mA	3
I_{CC2}	TTL Standby Current ($\overline{E}_1$= V_{IH} or $\overline{E}2$=V_{IL})		5	mA	
I_{CC3}	CMOS Standby Current ($\overline{E}_1$= Vcc -0.2v)		2	mA	4
I_{IL}	Input Leakage Current (Any Input)	-2	2	µA	5
I_{OL}	Onput Leakage Current	-2	2	µA	5
V_{OH}	Output Logic "1" Voltage (I_{OUT} =-1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +2.1 mA)		0.4	V	

NOTES :

1. All voltages referenced to GND.
2. Negative spikes of -1.0 volts allowed for up to 10 ns once per Cycle.
3. I_{CC1} measured with outputs open.
4. 1mA typical.
5. Measured with Vcc ≥ V1 ≥ GND and outputs deselected.

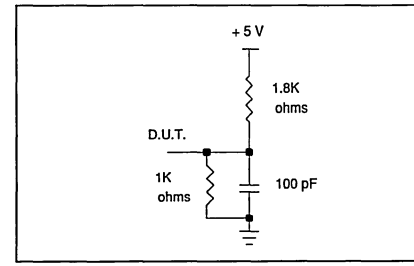
AC TEST CONDITION

Input Levels :. . . . . .0.0V to 3.0V

Transition Times :. . . . . .5 ns

Input and Output Timing
Reference Levels :. 1.5V

FIGURE 8 : OUPUT LOAD DIAGRAM



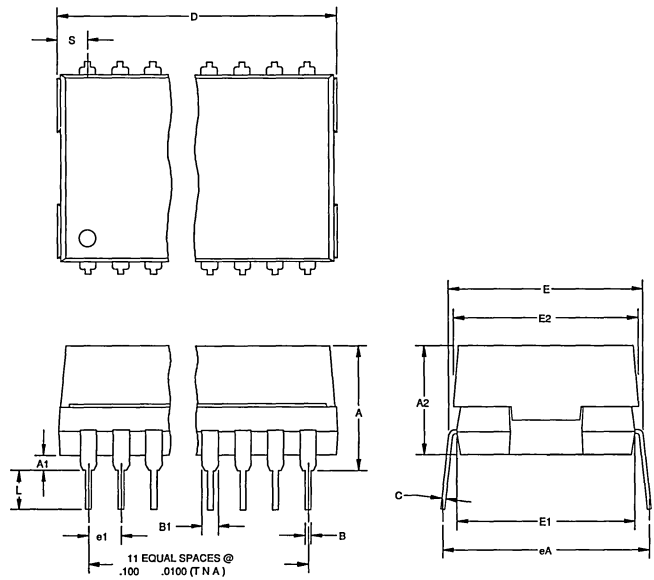
CAPACITANCE (T_A = 25°C)

SYMBOL	PARAMETER	MAX	UNITS	NOTES
C_I	Capacitance on All Pins (except DQ)	10.0	pF	1
C_{DQ}	Capacitance on DQ Pins	10.0	pF	1,2

ORDERING INFORMATION

PART NUMBER	ACCESS TIME (ns)	SUPPLY VOLTAGE	TEMPERATURE RANGE
MK48Z30-B10	100	5V+10%/-5%	0°C-70°C
MK48Z30-B12	120	5V+10%/-5%	0°C-70°C
MK48Z30-B15	150	5V+10%/-5%	0°C-70°C
MK48Z30A-B10	100	5V+10%/-10%	0°C-70°C
MK48Z30A-B12	120	5V+10%/-10%	0°C-70°C
MK48Z30A-B15	150	5V+10%/-10%	0°C-70°C

FIGURE 9 : 28 PIN BATTERY PACKAGE DESCRIPTION



DIM	INCHES		NOTES
	MIN	MAX	
A	.320	.380	2
A1	.015	.030	2
A2	.300	.360	
B	.015	.021	3
B1	.045	.070	
C	.008	.012	3
D	-	1.495	1
E	.530	640	
E1	.530	.550	
E2	.550	.570	
e1	.090	.110	
eA	.600	.700	
L	.120	.150	
S	.060	.090	

NOTES

1 OVERALL LENGTH INCLUDES FLASH AND PROJECTIONS ON EITHER END OF PACKAGE

2 PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS

3 THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN WHEN SOLDER LEAD FINISH IS SPECIFIED

SGS-THOMSON MICROELECTRONICS

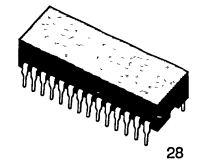
MK48Z32/32A(B) -10/12/15

32 K X 8 ZEROPOWER™ RAM

ADVANCE DATA

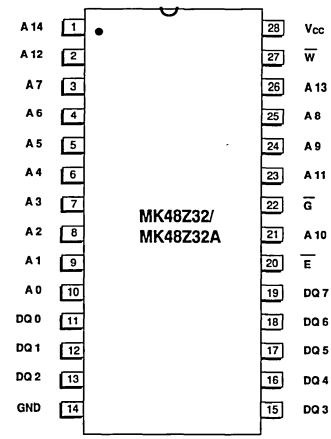
FEATURES

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT AND BATTERY.
- UNLIMITED WRITE-CYCLES.
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME.
- PREDICTED BATTERY BACK-UP OF 10 YEARS @ 25°C.
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 32K X 8 SRAMS.
- AUTOMATIC POWER-FAIL CHIP DESELECT / WRITE PROTECTION.
- DUAL WRITE PROTECT VOLTAGE:
  MK48Z30:4.75VOLTS.
  MK48Z30A: 4.50 VOLTS.



B
28-DIP
Plastic Package

PIN CONNECTIONS



DESCRIPTION

Part Number	Access Time	R/W Cycle Time	Vcc
MK48Z32 B - 10	100 ns	100 ns	+10 / -5 %
MK48Z32 B - 12	120 ns	120 ns	+10 / -5 %
MK48Z32 B - 15	150 ns	150 ns	+10 / -5 %
MK48Z32AB-10	100 ns	100 ns	+10 / -10%
MK48Z32AB-12	120 ns	120 ns	+10 / -10%
MK48Z32AB-15	150 ns	150 ns	+10 / -10%

PIN NAMES

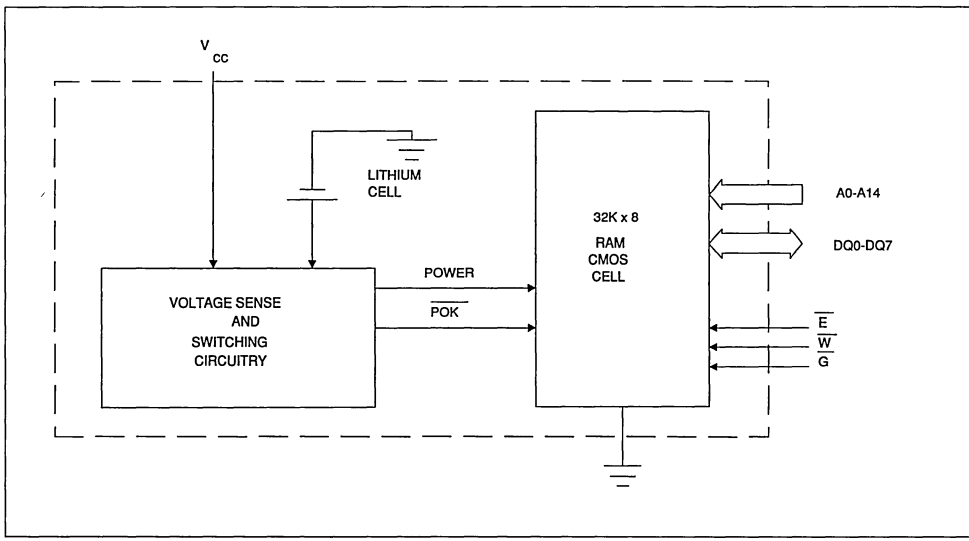
A0-A14	Address Input	Vcc	+5Volts
$\overline{E}$	Chip Enable	$\overline{W}$	Write Enable
		$\overline{G}$	Output Enable
GND	Ground	DQ0-DQ7	Data IN/Data Out

DESCRIPTION

The MK48Z32/32A combines an 32K x 8 full CMOS S RAM and a long life carbon mono-fluoride batteries in a single plastic DIP package.The MK48Z32/32A is a nonvolatille pin and function equivalent to any JEDEC standard 32Kx 8 SRAM. it also easily fits into many EPROM and EEPROM sockets, providing the non-volatility of the PROM s without any requiment for special writetiming,or limitations on the number of writes that can be performed.

In addition,the MK48Z32/32A has its own Powerfail Dectect Circuit. The circuit deselect s the device whenever V_{CC} is below tolerance, providing a hight degree of data security in the midst of unpredictable system operations brought on by low V_{CC}.

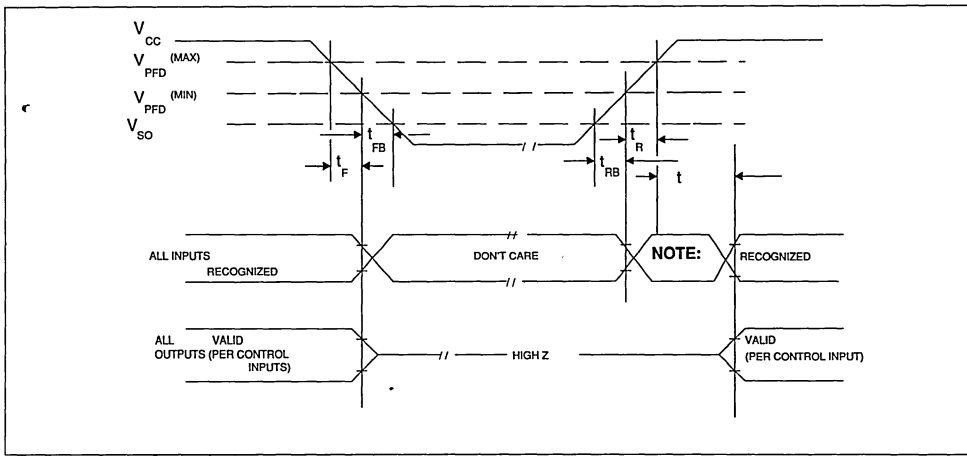
FIGURE 1 : MK48Z32/32A BLOCK DIAGRAM



TRUTH TABLE (MK48Z32/32A)

Vcc	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
< Vcc	V_{IH}	X	X	Deselect	High Z	Standby
(Max)	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
Vcc	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
(Mln)	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD} (Mln) > V_{SO}	X	X	X	Deselect	High Z	CMOS Standby
≤ V_{SO}	X	X	X	Deselect	High Z	Battery Back-up Mode

FIGURE 2 : POWER UP/DOWN TIMING



AC ELECTRICAL CHARACTERISTICS (POWER -UP/DOWN TIMING) (0°C ≤ T_A ≤ +70°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} Before Power Down	0		ns	
t_F	V_{PFD} (Max) to V_{PFD} (Min) V_{CC} FallTime	300		µs	2
t_{FB}	V_{PFD} (Min) to V_{SO} V_{CC} FallTime	10		µs	3
t_{RB}	V_{SO} to V_{PFD} (Min) V_{CC} Rise Time	1		µs	
t_R	V_{PFD} (Min) to V_{PFD} (Max) V_{CC} Rise Time	0		µs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} After Power Up	5		ms	

DC ELECTRICAL CHARACTERISTICS (POWER-UP/ DOWN TRIP POINTS) (0°C ≤ T_A ≤ +70°C)

SYMBOL	PARAMETER	VALUES			UNITS	NOTES
		MIN	TYP	MAX		
V_{PFD}	Power- Fail Deselect Voltage (MK48Z30)	4.5	4.6	4.75	V	1
V_{PFD}	Power- Fail Deselect Voltage (MK48Z30A)	4.2	4.3	4.5	V	1
V_{SO}	Battery Back-Up Switchover Voltage		3.0		V	1
t_{DR}	Expected Data Retention Time	10			YEARS	4

NOTES:

1 . All voltages referenced to GND.

2 . V_{PFD}(Max) to V_{PFD}(Min) fall times of less $t_F$may result in deselection/write protection not occuring until 40 µs after V_{CC} passes V_{PFD} (Min). V_{PFD} (Max)to (Min) fall times of less than 10 µs may cause corruption of RAM data.

3 . V_{PFD}(Min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data.

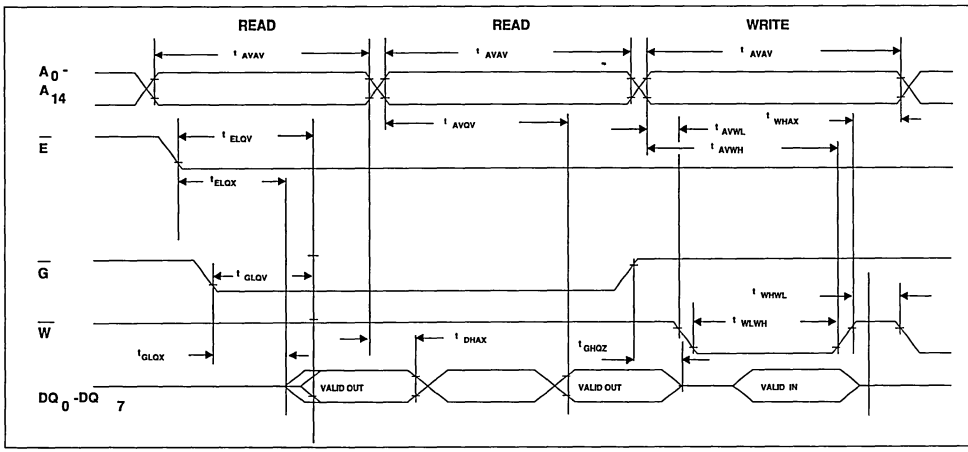
4 . 25 °C ambient condition.

READ MODE

The MK48Z32/32A is in the Read Mode whenever W (Write Enable) is high and E is low. The device architecture allows ripple-through access of data from eight of 262,144 locations in the static storage array. Thus, the unique address specified by the 14 Address inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} after the last address input signal is stable, providing that the Chip Enable and G access times are satisfied. If Chip Enable or G access times are not met, valid data will be available at the Chip Enable Access Time (t_{ELQV}) or at Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by Chip Enable and G. If the Outputs are activated before t_{AA}, the data lines will be driven to an indeterminate state until tAVQV. If the Address inputs are changed while Chip Enable and G remain low, output data will remain valid for

FIGURE 3 : READ CYCLE TIMING



AC ELECTRICAL CHARACTERISTICS (READ CYCLE)

(0°C≤T_A≤ + 70°C, VCC = 5.0 V +10% / -5%or -10%)

ALT. SYMBOL	STD. SYMBOL	PARAMETER	48ZXX-10 MIN	48ZXX-10 MAX	48ZXX-12 MIN	48ZXX-12 MAX	48ZXX-15 MIN	48ZXX-15 MAX	UNIT	NOTE
t_{RC}	t_{AVAV}	Read Cycle Time	100		120		150		ns	
t_{AA}	t_{AVQV}	Address Access Time		100		120		150		
t_{CEA1}	t_{ELQV}	$\overline{E}_1$ Access Time		100		120		150		
t_{CEZ}	t_{EHQZ}	Chip Enable Off Time		50		60		75		
t_{OEA}	t_{GLQV}	Output Enable Access Time		50		60		75		
t_{OEZ}	t_{GHQZ}	Output Enable Data Off Time		40		50		60		
t_{OEL}	t_{GLQX}	Output Enable To Q Low-z	5		5		5			
t_{CEL}	t_{ELQX}	Chip Enable To Q Low-z	10		10		10			
t_{OH}	t_{DHAX}	Output Hold From Address	5		5		5			

Output Data Hold Time (t_{DHAX}) but will go indeterminate until the next Address Access.

WRITE MODE

The MK48Z32/32A is in the Write Mode whenever Write Enable and Chip select are active. The start of a write is referenced to the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high or for minimum of t_{WR} prior to the initiation of another read or write cycle. Data-in must be valid

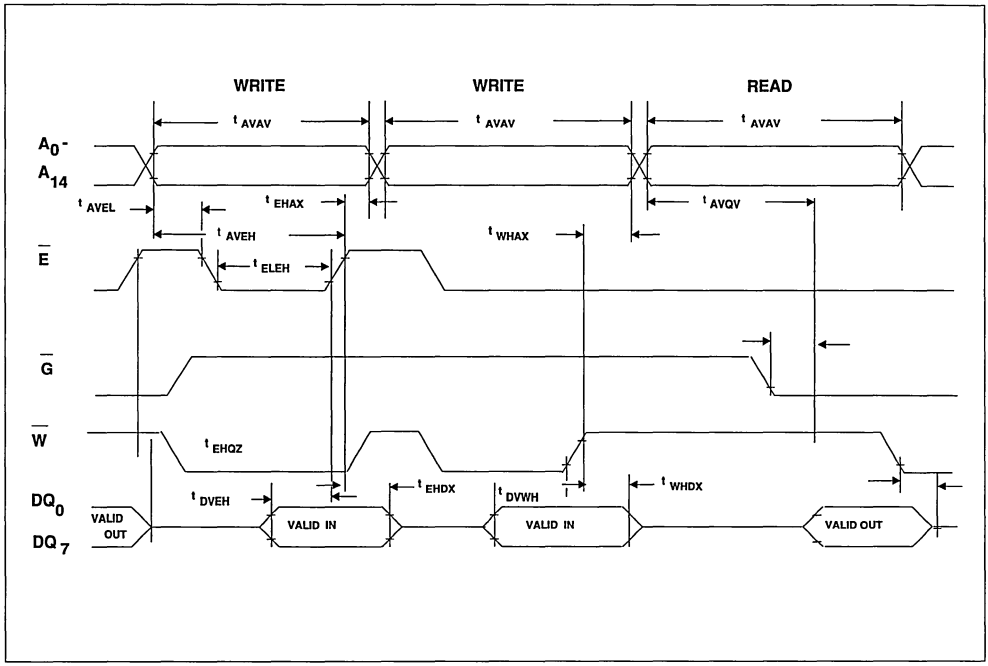
AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE)

($0°C \leq T_A \leq +70°C$, V_{CC} = 5.0 V +10% / -5% or -10%)

ALT. SYMBOL	STD. SYMBOL	PARAMETER	48ZXX-10		48ZXX-12		48ZXX-15		UNITS	NOTE
			MIN	MAX	MIN	MAX	MIN	MAX		
t_{WC}	t_{AVAV}	Write Cycle Time	100		120		150		ns	
t_{AS}	t_{AVWL}	Address Setup Time $\overline{W}$ Low	0		0		0			
t_{AS}	t_{AVEL}	Address Setup Time $\overline{E}$ Low	0		0		0			
t_{CEW}	t_{ELEH}	Chip Enable to End Of Write	80		100		130			
t_{AW}	t_{AVWH}	Address Valid to End Off Write	80		100		130			
t_{AW}	t_{AVEH}	Address Valid to End Off Write	80		100		130			
t_{WEW}	t_{WLWH}	Write Pulse Width	50		70		100			
t_{TCEZ}	t_{EHQZ}	$\overline{E}$ Data of Time		50		60		75		
t_{WEZ}	t_{WLQZ}	$\overline{W}$ Data of Time		50		60		75		
t_{WR}	t_{WHAX}	$\overline{W}$ High to Address Change	10		10		10			1
t_{WR}	t_{EHAX}	$\overline{E}$ High to Address Change	10		10		10			2
t_{WR}	t_{WHWL}	$\overline{W}$ High to $\overline{W}$ Low Next Cycle	10		10		10			
t_{DS}	t_{DVWH}	Data Setup Time to $\overline{W}$ High	50		60		70			1
t_{DS}	t_{DVEH}	Data Setup Time to $\overline{E}$ High	50		60		70			2
t_{DH}	t_{WHDX}	Data Hold Time $\overline{W}$ High	5		5		5			1
t_{DH}	t_{EHDX}	Data Hold Time $\overline{E}$ High	5		5		5			2

NOTES:
1. In a $\overline{W}$ Controlled Cycle.
2. In a $\overline{E}$ Controlled Cycle.

FIGURE 4 : WRITE CYCLE TIMING



ABSOLUTE MAXIMUM RATINGS *

PARAMETER	VALUES	UNITS
Voltage on any Pin Relative to GND	-0.3 to + 7.0	V
Ambient Operating (V_{CC} On) Temperature (t_A)	0 to 70	°C
Ambient Storage (V_{CC} Off) Temperature	-40 to +70	°C
Total Device Power Dissipation	1.0	W
Output Current Per Pin (one Output at a Time)	50	mA

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is net implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION

Negative undershoots below -0.3 volts are not allowed on any pinb while in the Battery Back-up mode

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
Vcc	Supply Voltage (MK48Z30)	4.75	5.5	V	1
Vcc	Supply Voltage (MK48Z30A)	4.5	5.5	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	Vcc + 0.3v	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3	0.8	V	1,2

DC ELECTRICAL CHARACTERISTICS (0°C≤ T_A ≤+70°C) (Vcc (min) ≤ Vcc ≤ Vcc (max))

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
Icc1	Average Vcc Power Supply Current		90	mA	3
Icc2	TTL Standby Current ($\overline{E}_1$= V_{IH} or $\overline{E}$2=V_{IL})		5	mA	
Icc3	CMOS Standby Current ($\overline{E}_1$= Vcc -0.2v)		2	mA	4
I_{IL}	Input Leakage Current (Any Input)	-2	2	µA	5
I_{OL}	Onput Leakage Current	-2	2	µA	5
V_{OH}	Output Logic "1" Voltage (I_{OUT} =-1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +2.1 mA)		0.4	V	

NOTES :

1. All voltages referenced to GND.
2. Negative spikes of -1.0 volts allowed for up to 10 nS once per Cycle.
3. I_{CC1} measured with outputs open.
4. 1mA typical.
5. Measured with Vcc ≥ V1 ≥ GND and outputs deselected.

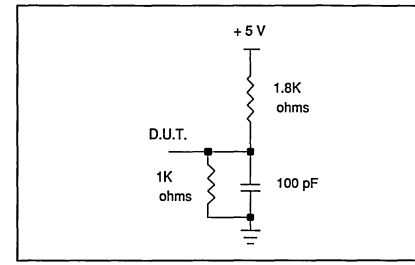
AC TEST CONDITION

Input Levels :. . . . . .0.0V to 3.0V

Transition Times :. . . . . .5 ns

Input and Output Timing
Reference Levels :. 1.5V

FIGURE 5 : OUPUT LOAD DIAGRAM



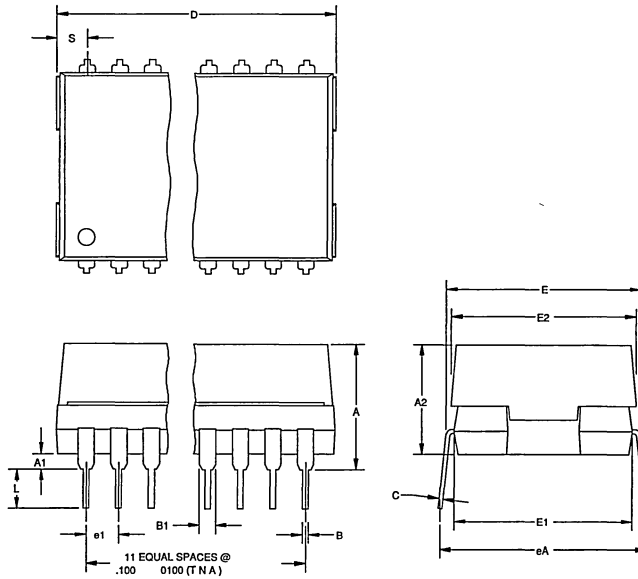
CAPACITANCE (T_A = 25°C)

SYMBOL	PARAMETER	MAX	UNITS	NOTES
C_I	Capacitance on All Pins (except DQ)	10.0	pF	1
C_{DQ}	Capacitance on DQ Pins	10.0	pF	1,2

ORDERING INFORMATION

PART NUMBER	ACCESS TIME (ns)	SUPPLY VOLTAGE	TEMPERATURE RANGE
MK48Z32(B)-10	100	5V+10%/-5%	0°C-70°C
MK48Z32(B)-12	120	5V+10%/-5%	0°C-70°C
MK48Z32(B)-15	150	5V+10%/-5%	0°C-70°C
MK48Z32A(B)-10	100	5V+10%/-10%	0°C-70°C
MK48Z32A(B)-12	120	5V+10%/-10%	0°C-70°C
MK48Z32A(B)-15	150	5V+10%/-10%	0°C-70°C

FIGURE 6 : 28 PIN BATTERY PACKAGE DESCRIPTION



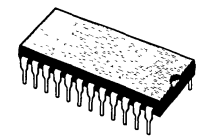
DIM	INCHES		NOTES
	MIN	MAX	
A	.320	.380	2
A1	.015	.030	2
A2	.300	.360	
B	.015	.021	3
B1	.045	.070	
C	.008	.012	3
D	-	1 495	1
E	.530	.640	
E1	.530	.550	
E2	.550	.570	
e1	.090	.110	
eA	.600	.700	
L	.120	.150	
S	.060	.090	

NOTES

1. OVERALL LENGTH INCLUDES FLASH AND PROJECTIONS ON EITHER END OF PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY 003 IN WHEN SOLDER LEAD FINISH IS SPECIFIED.

MK6116, MKI6116, MK6116L, MKI6116L (N/S) - 15/20/25
2 K X 8 CMOS STATIC RAM

- BYTEWYDE™ 2K x 8 CMOS STATIC RAM.
- +5 VOLT ONLY WRITE/READ.
- 24-PIN 600 MIL PLASTIC DIP, JEDEC PINOUT 28-PIN 330 MIL SOIC.
- EQUAL WRITE AND READ CYCLE TIMES.
- HIGH PERFORMANCE WITH LOW CMOS STANDBY POWER.



B
DIP 24
(Plastic Package)

1

24

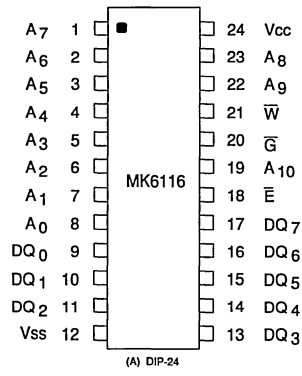
DESCRIPTION

The MK6116 is a 16,384-bit CMOS Static RAM, organized as 2K x 8 usingSGS-THOMSON Microelectronics' advanced HCMOS process technology. This device is directly compatible with the popular 24-pin, three-wire handshake, 16K static CMOS RAM. All inputs and outputs are TTL compatible using a single 5V supply. The MK6116 provides full static operation, requiring no clocks or refresh operations, and has equal access and cycle times. Additionally, whenever $\overline{E}$ (Chip Enable) goes high, the device will maintain a reduced power standby mode until $\overline{E}$ again goes active low. (Refer to the MK6116Truth Table.)

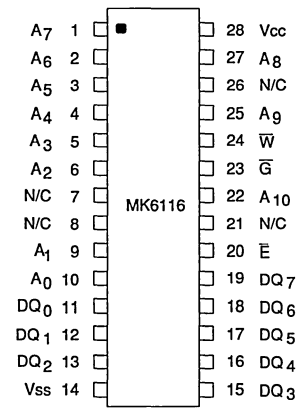
PIN NAMES

A_0 -A_{10}	ADDRESS INPUTS
DQ_0 - DQ_7	DATA I/O
$\overline{E}$	CHIP ENABLE
$\overline{G}$	OUTPUT ENABLE
$\overline{W}$	WRITE ENABLE
V_{CC}, V_{SS}	+5V, GND

PIN CONNECTION

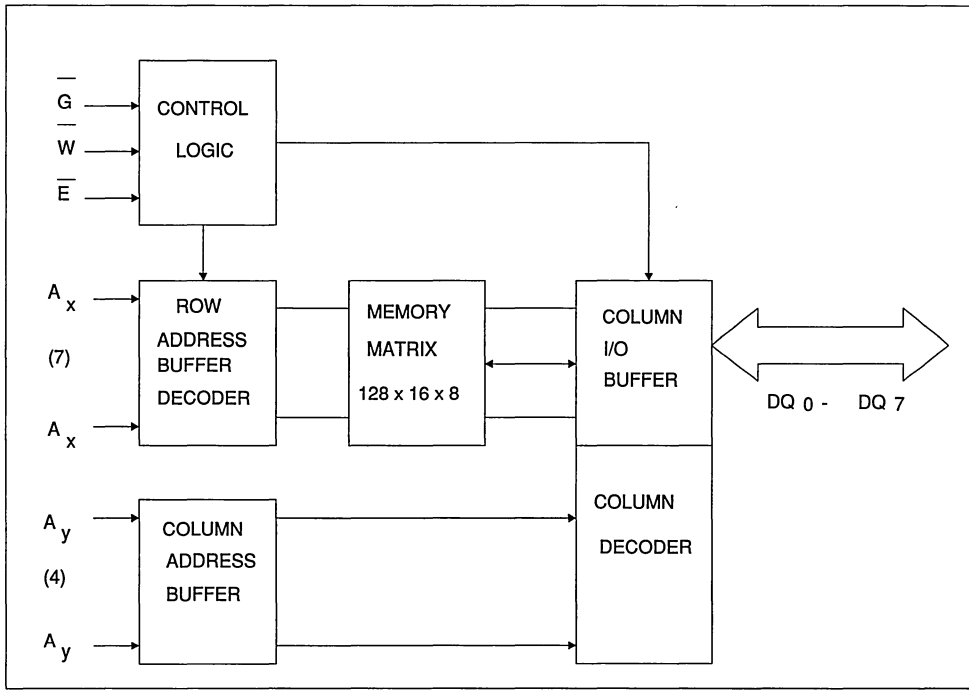


(A) DIP-24



(B) S SOIC-28

FIGURE 1 : BLOCK DIAGRAM



MK6116 TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
V_{IH}	X	X	deselect	Hight Z	Standby
V_{IL}	X	V_{IL}	Write	D_{IN}	Active
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	V_{IH}	Read	Hight Z	Active

READ MODE

The MK6116 is in the read mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low, providing a ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_0-A_{10}) defines which one of 2048 bytes of data is to be accessed.

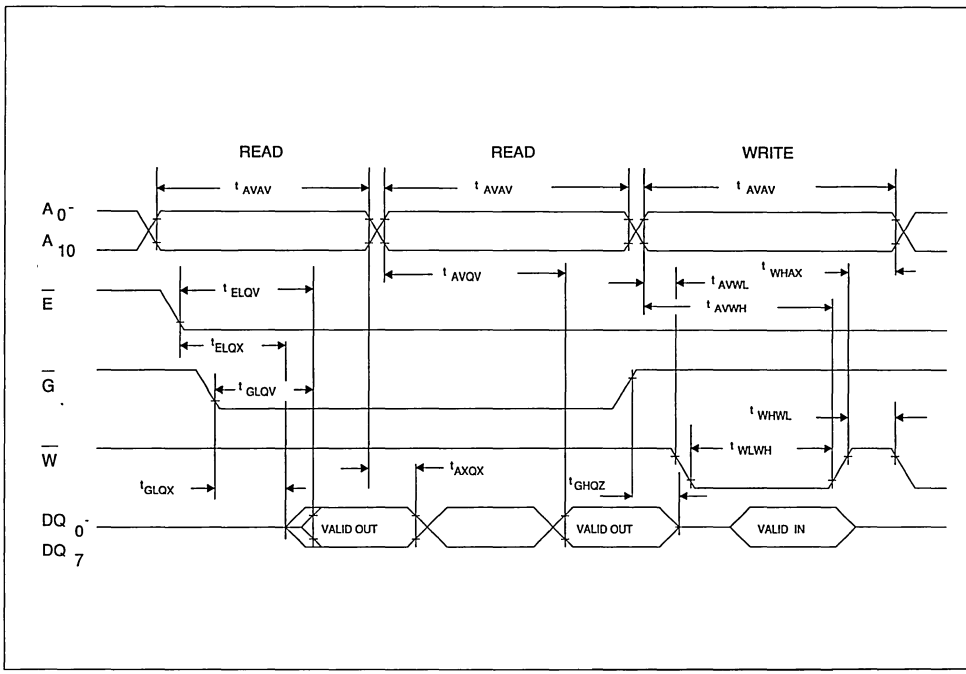
Valid data will be available at the eight Data Outputs Drivers (DQ_0-DQ_7) within t_{AVQV} after the last address input signal is stable, provided that the $\overline{E}$ and G (Out-put Enable) access times are satisfied. If $\overline{E}$ or G access times are not met, data access will be measured from the limiting parameter (t_{ELQV} or t_{GLQV}) rather than address. The state of the eight Data I/O signals is controlled by the $\overline{E}$ and G input signals. Data Out may be indeterminate between t_{AXQX} and t_{AVQV}, but data will always be valid at t_{AVQV}.

AC ELECTRICAL CHARACTERISTIICS (READ CYCLE)

{0°C ≤ TA ≤ +70°C (MK6116/L), -40°C ≤ TA ≤ + 105°C (MKI6116/L), VCC= 5.0 +/ - 10%}

ALT. SYMBOL	STD. SYMBOL	PARAMETER	MK6116 - 15 MKI6116 -15 MK6116L-15 MKI6116L-15		MK6116 - 20 MKI6116 -20 MK6116L-20 MKI6116L-20		MK6116 - 25 MKI6116 -25 MKL6116-25			
			MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	t_{AVAV}	Read Cycle Time	150		200		250		ns	
t_{AA}	t_{AVQV}	Address Access Time		150		200		250	ns	1
t_{CEA}	t_{ELQV}	ChipEnable Access Time		150		200		250	ns	1
t_{CEZ}	t_{EHQZ}	Chip Enable Data OffTime		35		40		50	ns	
t_{OEA}	t_{GLQV}	Output Enable Access Time		75		80		90	ns	1
t_{OEZ}	t_{GLQV}	Output Enable Data Off Time		35		40		50	ns	
t_{OEL}	t_{GLQX}	Out put Enable to Q Low-Z	15		15		15		ns	
t_{CEL}	t_{ELQX}	Chip Enable to Q Low-Z	15		15		15		ns	
t_{OH}	t_{AXQX}	Output Hold from Address	15		15		15		ns	1

FIGURE 2 : READ CYCLE TIMING



WRITE MODE

The MK6116 is in the Write Mode of operation whenever $\overline{W}$ and $\overline{E}$ are active low ($\overline{G}$ is a don't care as noted in the Truth Table). The latter occurring falling edge of either $\overline{W}$ or $\overline{E}$ will determine the start of the write cycle. Therefore, address setup time and write or chip enable pulse width are referenced to the latter occurring edge of $\overline{W}$ or $\overline{E}$. The write cycle can be terminated by either earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{W}$ must return to the high logic state for a minimum write recovery time designated as t_{WHWL} between write cycles. Addresses must remain valid for t_{WHAX} at the termination of the write cycle. The same principles apply for an $\overline{E}$ controlled write cycle.

If the output bus has been enabled ($\overline{E}$ and $\overline{G}$ active low), then $\overline{W}$ will disable the outputs within t_{WLQZ} from its falling edge; however, care must be taken to avoid a potential bus contention. Data-In must be valid t_{DVWH} or t_{DVEH} prior to the earlier rising

AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE)

{0°C ≤ T_A ≤ +70°C (MK6116/L), -40°C≤ T_A ≤ +105°C (MKI6116/L), V_{CC}=5.0 ± 10%}

ALT. SYMBOL	SDT. SYMBOL	PARAMETER	MK6116 - 15 MKI6116 -15 MK6116L-15 MKI6116L-15		MK6116 - 20 MKI6116 -20 MK6116L-20 MKI6116L -20		MK6116 - 25 MKI6116 -25 MKL6116-25			
			MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	t_{AVAV}	Write Cycle Time	150		200		250		ns	
t_{AS}	t_{AVWL}	Address Setup Time $\overline{W}$ Low	0		0		0		ns	
t_{AS}	t_{AVEL}	Address Setup Time $\overline{E}$ Low	0		0		0		ns	
t_{CEW}	t_{ELEH}	Chip Enable to End of Write	90		120		160		ns	
t_{AW}	t_{AVWH}	Address Valid to End of Write	120		140		180		ns	
t_{AW}	t_{AVEH}	Address Valid to End of Write	120		140		180		ns	
t_{WEW}	t_{WLWH}	Write Pulse Width	90		120		160		ns	
t_{AH}	t_{WHAX}	$\overline{W}$ Hight to address Change	10		10		10		ns	
t_{AH}	t_{EHAX}	$\overline{E}$ Hight to address Change	10		10		10		ns	
t_{WR}	t_{WHWL}	$\overline{W}$ Hight to $\overline{W}$ Low Next Cycle	10		10		10		ns	
t_{WEZ}	t_{WLQZ}	$\overline{W}$ Data Off Time		50		60		80	ns	
t_{CEZ}	t_{EHQZ}	$\overline{E}$ Data Off Time		50		60		80	ns	
t_{DS}	t_{DVWH}	Data Setup Time to $\overline{W}$ Hight	40		60		100		ns	
t_{DS}	t_{DVEH}	Data Setup Time to $\overline{E}$ Hight	40		60		100		ns	
t_{DH}	t_{WHDX}	Data Hold Time $\overline{W}$ High	0		0		0		ns	
t_{DH}	t_{EHDX}	Data Hold Time $\overline{E}$ High	0		0		0		ns	

FIGURE 3 : WRITE CYCLE TIMING

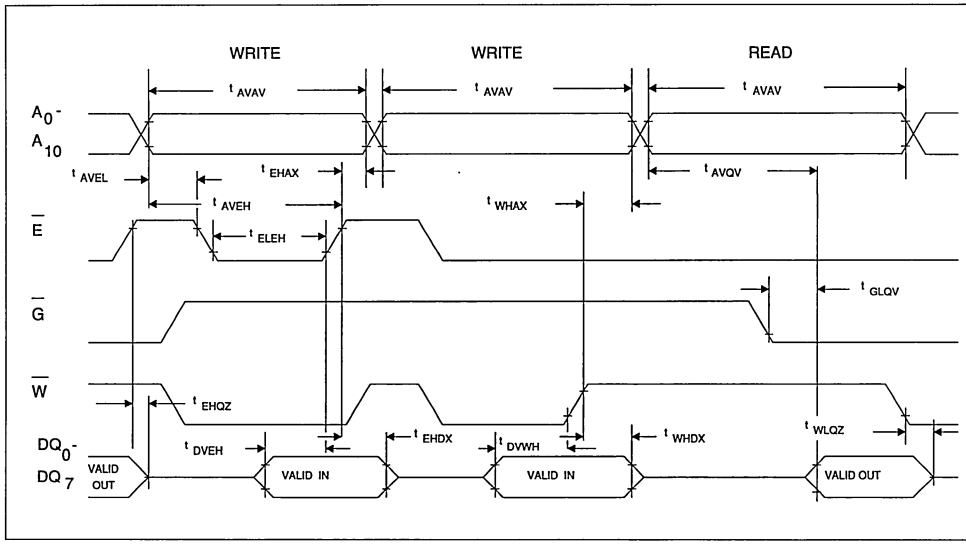
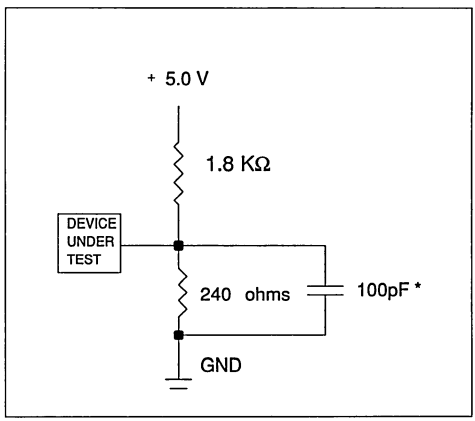


FIGURE 4 : OUTPUT LOAD DIAGRAM



*Notes: Including scope and JIG

AC TEST CONDITION

Input Levels: . . . . . 0.6 V to 2.4 V

Transition Times: . . . . . 5 ns

Input and Output Timing
Reference Levels: . . . . . 0.8V or 2.2 V

ABOLUTE MAXIMUM RATINGS *

PARAMETER	VALUES	UNITS
Voltage on any Pin Relative tro Ground	-0.3 to +7.0	V
Operating Temperature (MK6116L)	0 to +7	°C
Operatting Temperature (MKI6116/L)	-40 to +150	°C
Storage Temperature	-55 to +150	°C
Power Dissipation	1	W
Output Current	† 20	mA

* This is a stress rating only and functional operation of the device at these or any conditions above those indicazted in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

† Output current absolute maximun rating is specified for one output at a time, not to exceed a duration of a1 second.

RECOMMENDED DC OPERATING CONDITIONS

{0°C ≤ T_A ≤ +70°C (MK6116/L), -40°C ≤ T_A ≤ +150°C (MKI6116/L), V_{CC}=5.0 +/- 10%}

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.5.	V	4
V_{SS}	Supply Voltage	0	0	V	4
V_{IH}	Logic 1 All Inputs	2.2	V_{cc} +0.3	V	4
V_{IL}	Logic 1 All Inputs	-0.3	0.8	V	4,5

DC ELECTRICAL CHARACTERISTICS

{0°C ≤ TA ≤ +70°C (MK6116/L), -40°C ≤ T_A ≤ +150°C (MKI6116/L), V_{CC}=5.0 +/- 10%}

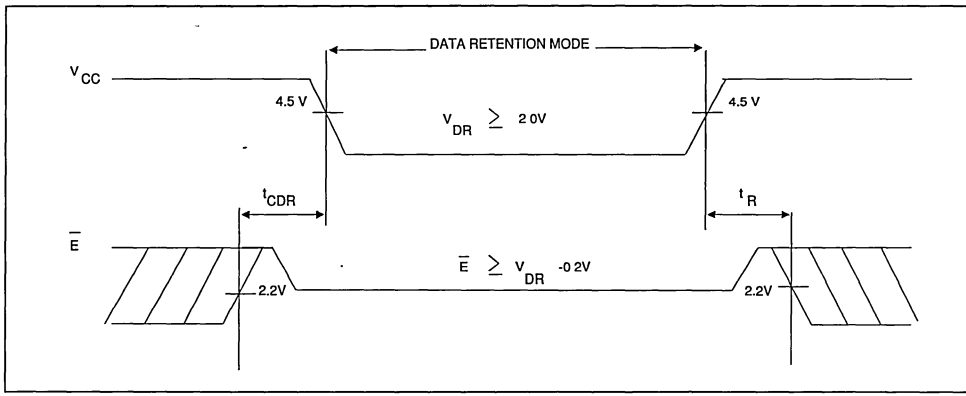
SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC}	Average V_{CC} Power Supply Current ,		70	mA	6
	MK6116, MKI6116				
	MK6116L, MKI6116L		70	mA	
I_{SB1}	TTL Standby Current ($\overline{E}$ = V_{IH})		3	mA	
I_{SB2}	CMOS Standby Current ($\overline{E}$ ≥ V_{CC}-0.2 V)		1	mA	
	MK6116, MKI6116				
	MK6116L			µA	
	MKI6116L		10	µA	
I_{LI}	Input Leakage Current	-1	+1	µA	7
I_{LO}	Output Leakage Current	-5	+5	µA	7
V_{OH}	Output Logic 1 Voltage (I_{OH} = -1.0 mA)	2.4		V	
V_{OL}	Output Logic 2 Voltage (I_{OH} = 2.1 mA)		0.4	V	

LOW V_{CC} Data RETENTION CHARACTERISTICS (MK6116L, MKI6116L)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
V_{DR}	V_{CC} Data retention	2.0	V_{CC} (max)		
$I_{CC}DR$	Data Retention Power Supply Current		1	µA	8
	MK6116L				
	MKI6116L		3	µA	
t_{CDR}	Chip Deselection to Data Retention Time	0		ns	
t_R	Operation Recovery Time	t_{AVAV}*			

* tAVAV = Read Cycle Time

FIGURE 5 . LOW V_{CC} DATA RETENTION TIMING



NOTES:

1 . Measured with load as shown in Figure 4.

2 . Effective capacitance calculated from the equation:
C= IΔt/ΔV, with ΔV = 3 volts and power supply at nominal level

3 . Output is deselected.

4 . All voltages referenced to GND.

5 . Negative spikes of -1.0 volts allowed for up to 10 ns once per cycle.

6 . ICC1 measured with output open.

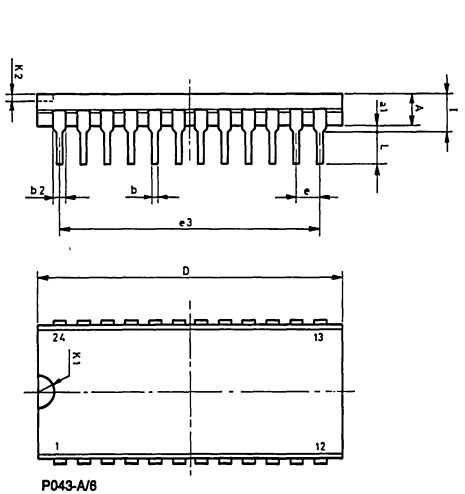
7 . Measured with GND ≤ V ≤ V_{CC} and outputs deselected.

8 . V_{CC} = 2.0 Volts.

CAPACITANCE (TA = 25°C)

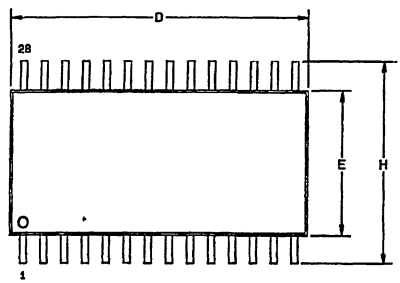
SYMBOL	PARAMETER	MAX	UNITS	NOTES
C_I	Capacitance on all pins (except DQ)	7.0	PF	2
C_{DQ}	Capacitance on DQ pins	10.0	PF	2, 3

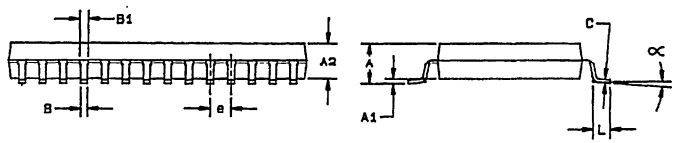
FIGURE 6 . 24-PIN PLASTIC DIP (N)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a 1		0 63			0 024	
B		0 45			0.017	
b 1	0.23		0.31	0.009		0.012
b 2		1.27			0.050	
C						
D			32.20			1.267
E	15 20		16 68	0.598		0.656
e		2 54			0.100	
e3		27.94			1.100	
e4						
F			14.10			0.555
I	4 45		0.175			
L	3.30		0.129			
K1						
K2						

FIGURE 7 . 28-PIN SOIC (S)





Dim.	Inches	
	Min.	Max.
A		.120
A1	.002	.014
A2	.092	.106
B	.014	.020
B1	.014	.024
C	.006	.0125
D	.697	.728
E	.324	.350
e	.050 Basic	
H	.453	.500
L	.016	.050
α	0°	8°

ORDERING INFORMATION

PART NO.	ACCESS TIME	CYCLE TIME	PACKAGE TYPE	TEMPERATURE
MK6116 (N/S)-15	150 ns	150 ns	Plastic DIP/SOIC	0°C to 70°C
MK6116 (N)-20	200 ns	200 ns	Plastic DIP	0°C to 70°C
MK6116 (N) -25	250 ns	250 ns	Plastic DIP	0°C to 70°C
MKI6116 (N/S) -15	150 ns	150 ns	Plastic DIP/SOIC	-40°C to 105°C
MKI6116 (N) -20	200 ns	200 ns	Plastic DIP	-40°C to 105°C
MKI6116 (N) - 25	250 ns	250 ns	Plastic DIP	-40°C to 105°C
MK6116 L(N/S) -15	150 ns	150 ns	Plastic DIP/SOIC	0°C to 70°C
MK6116 L(N) - 20	200 ns	200 ns	Plastic DIP	0°C to 70°C
MK6116 L(N) - 25	250 ns	250 ns	Plastic DIP	0°C to 70°C
MKI6116 L(N/S) - 15	150 ns	150 ns	Plastic DIP/SOIC	-40°C to 105°C
MKI6116L (N) - 20	200 ns	200 ns	Plastic DIP	-40°C to 105°C

MK _____ Commercial Temperature Range (0°C to +70°C)

MKI _____ Industrial Temperature Range (-40°C to +85°C)

6116 _____ Device Family and Identification Number

L _____ Low Power

N _____ Plastic Dip Package

S _____ SOIC Package

15/20/25 _____ Speed Grade

BYTEWYDE is a Trademark of SGS-THOMSON Microelectronics

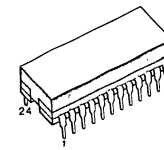
2K × 8 ZEROPOWER™ RAM

- INDUSTRIAL TEMPERATURE RANGE −40°C to +85°C
- PREDICTED WORST CASE BATTERY LIFE OF 6 YEARS @ 85°C
- DATA RETENTION IN THE ABSENCE OF POWER
- DATA SECURITY PROVIDED BY AUTOMATIC WRITE PROTECTION DURING POWER FAILURE
- +5 VOLT ONLY READ/WRITE
- CONVENTIONAL SRAM WRITE CYCLES
- LOW POWER-440 mW ACTIVE; 5.5 mW STANDBY
- 24-PIN DUAL IN LINE PACKAGE, JEDEC 24 PIN MEMORY PINOUT
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME
- ON BOARD LOW-BATTERY WARNING CIRCUITRY
- TWO POWER-FAIL DESELECT TRIP POINTS AVAILABLE
  MKI48Z02 $4.75V \geq V_{PFD} \geq 4.50V$
  MKI48Z12 $4.50V \geq V_{PFD} \geq 4.20V$

Part Number	Access Time	R/W Cycle Time
MKI48ZX2-15	150 ns	150 ns
MKI48ZX2-20	200 ns	200 ns
MKI48ZX2-25	250 ns	250 ns

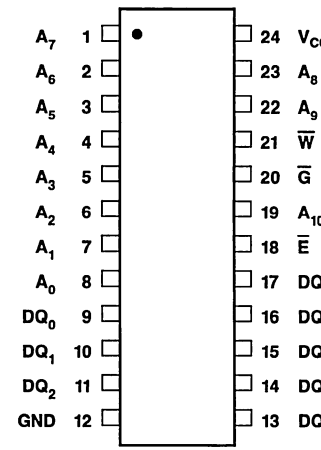
TRUTH TABLE (MKI48Z02/12)

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ
$<V_{CC}$ (Max)	V_{IH}	X	X	Deselect	High-Z
$>V_{CC}$ (Min)	V_{IL}	X	V_{IL}	Write	D_{IN}
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
	V_{IL}	V_{IH}	V_{IH}	Read	High-Z
$<V_{PFD}$ (Min) $>V_{SO}$	X	X	X	Power-Fail Deselect	High-Z
$\leq V_{SO}$	X	X	X	Battery Back-up	High-Z



B
DIP-24
(Plastic with Battery Top Alt)

FIGURE 1. PIN CONNECTIONS



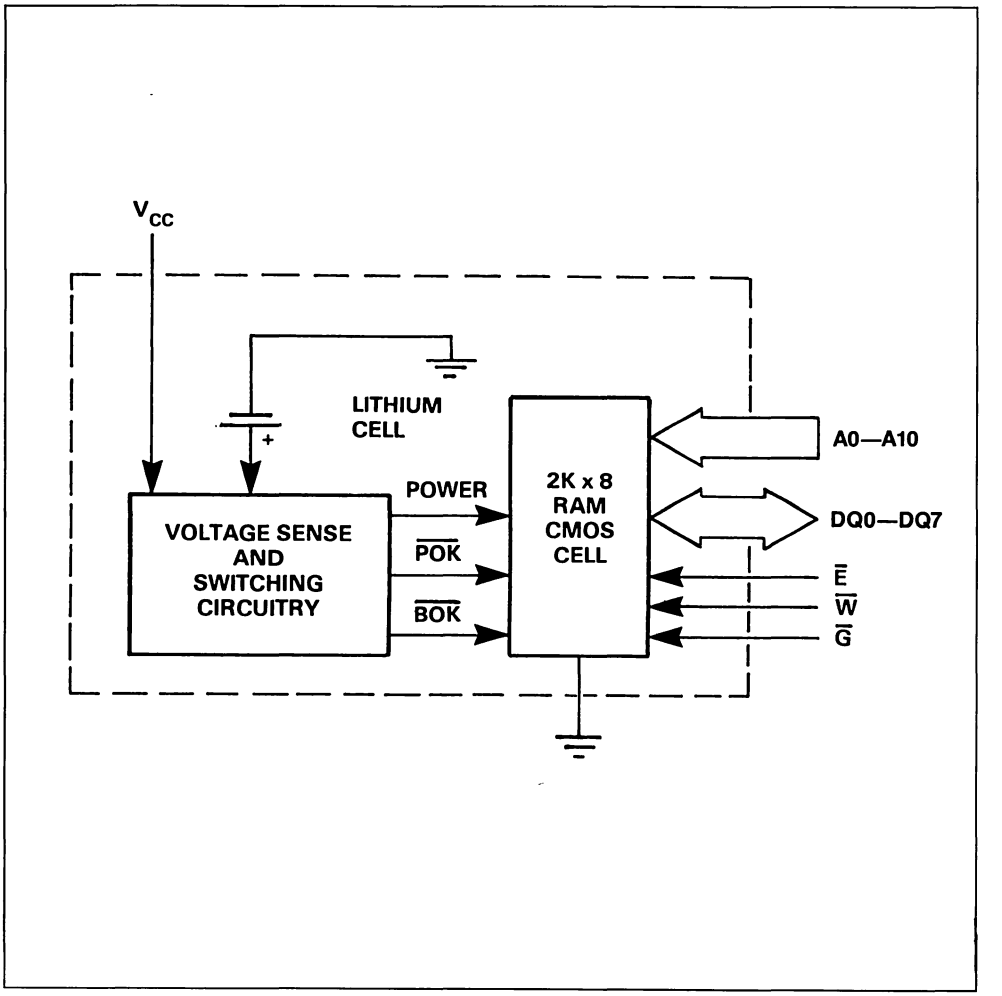
PIN NAMES

A_0 - A_{10}	Address Inputs	V_{CC}	System Power (+5 V)
$\overline{E}$	Chip Enable	$\overline{W}$	Write Enable
GND	Ground	$\overline{G}$	Output Enable
DQ_0—DQ_7 Data In/Data Out			

DESCRIPTION

The MKI48Z02/12 is a 16,384-bit, Non-Volatile Static RAM, organized 2K x 8 using CMOS and an integral Lithium energy source. The ZEROPOWER™ RAM has the characteristics of a CMOS static RAM, with the important added benefit of data being retained in the absence of power. Data retention current is so small that a miniature Lithium cell contained within the package provides an energy source to preserve data. Low current drain has been attained by the use of a full CMOS memory cell, novel analog support circuitry, and carefully controlled junction leakage by an all implanted CMOS process. Safeguards against inadvertent data loss have been incorporated to maintain data integrity in the uncertain operating environment associated with power-up and power-down transients. The ZEROPOWER RAM can replace existing 2K x 8 static RAM, directly conforming to the popular Byte Wide 24-pin DIP package (JEDEC). MKI48Z02/12 also matches the pinning of 2716 EPROM and 2K x 8 EEPROM. Like other static RAMs, there is no limit to the number of write cycles that can be performed. Since the access time, read cycle, and write cycle are less than 250 ns and require only +5 volts, no additional support circuitry is needed for interface to a microprocessor.

FIGURE 2. BLOCK DIAGRAM



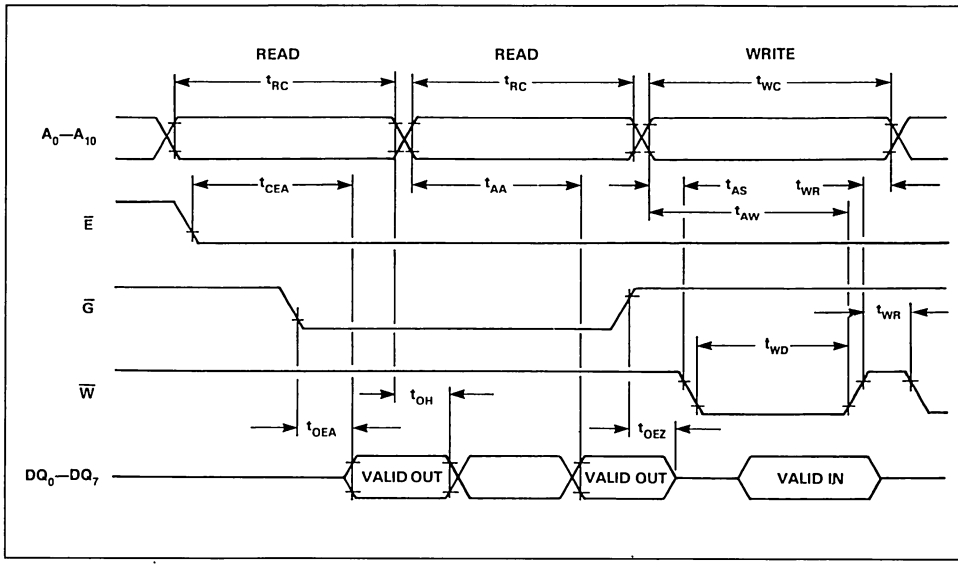
OPERATION

Read Mode

The MKI48Z02/12 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low, providing a ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_n) defines which one of 2,048 bytes of data is to be accessed.

Valid data will be available to the eight data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are satisfied. If $\overline{E}$ or $\overline{G}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}), rather than the address. The state of the eight Data I/O signals is controlled by the $\overline{E}$ and $\overline{G}$ control signals. The data lines may be in an indeterminate state between t_{OH} and t_{AA}, but the data lines will always have valid data at t_{AA}.

FIGURE 3. READ-READ-WRITE TIMING



AC ELECTRICAL CHARACTERISTICS (READ CYCLE TIMING)
($-40°C \leq T_A \leq +85°C$) ($V_{CC}$ (Max) $\geq V_{CC} \geq V_{CC}$ (Min))

SYM	PARAMETER	MKI48ZX2-15		MKI48ZX2-20		MKI48ZX2-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	150		200		250		ns	
t_{AA}	Address Access Time		150		200		250	ns	1
t_{CEA}	Chip Enable Access Time		150		200		250	ns	1
t_{OEA}	Output Enable Access Time		75		80		90	ns	1
t_{CEZ}	Chip Enable Hi to High-Z		35		40		50	ns	
t_{OEZ}	Output Enable Hi to High-Z		35		40		50	ns	
t_{OH}	Valid Data Out Hold Time	15		15		15		ns	1

NOTE
1. Measured using the Output Load Diagram shown in Figure 8.

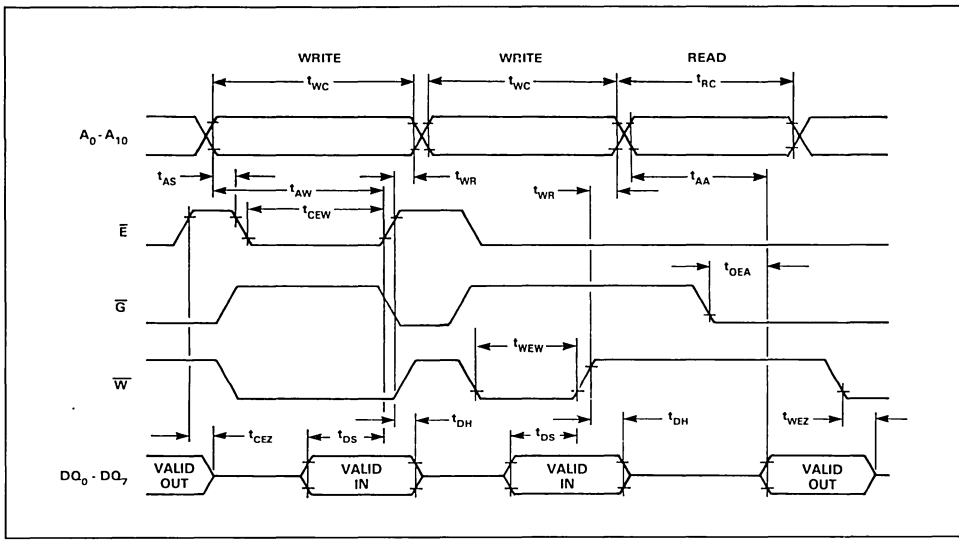
WRITE MODE

The MKI48Z02/12 is in Write Mode whenever the $\overline{W}$ and $\overline{E}$ inputs are held low. The start of a Write is referenced to the latter occurring falling edge of either $\overline{W}$or $\overline{E}$. A Write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{W}$ or $\overline{E}$ must return high for a minimum of t_{WR} prior to the initiation of another Read or Write Cycle. Data-in must be valid for t_{DS} prior to the End of Write and remain valid for t_{DH} afterward.

Some processors thrash producing spurious Write Cycles during power-up, despite application of a power-on reset. Users should force $\overline{W}$ or $\overline{E}$ high during power-up to protect memory after V_{CC} reaches V_{CC} (min) but before the processor stablizes.

The MKI48Z02/12 $\overline{G}$ input is a DON'T CARE in the write mode. $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WEZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

FIGURE 4. WRITE-WRITE-READ TIMING



AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE TIMING)

($-40°C \leq T_A \leq +85°C$) ($V_{CC}$ (Max) $\geq V_{CC} \geq V_{CC}$ (Min))

		MKI48ZX2-15		MKI48ZX2-20		MKI48ZX2-25			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	Write Cycle Time	150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AW}	Address Valid to End of Write	120		140		180		ns	
t_{CEW}	Chip Enable to End of Write	90		120		160		ns	
t_{WEW}	Write Enable to End of Write	90		120		160		ns	
t_{WR}	Write Recovery Time	10		10		10		ns	
t_{DS}	Data Setup Time	40		60		100		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WEZ}	Write Enable Low to High-Z		50		60		80	ns	

DATA RETENTION MODE

With V_{CC} applied, the MKI48Z02/12 operates as a conventional BYTEWIDE static ram. However, V_{CC} is being constantly monitored. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. The MKI48Z02 has a V_{PFD} (max) to V_{PFD} (min) window of 4.75 volts to 4.5 volts, providing very high data security, particularly when all of the other system components are specified to 5.0 volts plus and minus 10%. The MKI48Z12 has a V_{PFD} (max) to V_{PFD} (min) window of 4.5 volts to 4.2 volts, allowing users constrained to a 10% power supply specification to use the device.

Note: A mid-write cycle power failure may corrupt data at the current address location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time does not exceed t_F. The MKI48Z02/12 may respond to transient noise spikes that reach into the deselect window if they should occur during the time the device is sampling V_{CC}. Therefore decoupling of power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{BOK}$) flag will be set. The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after first write, and normal RAM operation resumes. Figure 5 illustrates how a $\overline{BOK}$ check routine could be structured.

Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD} (Max). Caution should be taken to keep $\overline{E}$ or $\overline{W}$ high as V_{CC} rises past V_{PFD} (Min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

FIGURE 5. CHECKING THE $\overline{BOK}$ FLAG STATUS

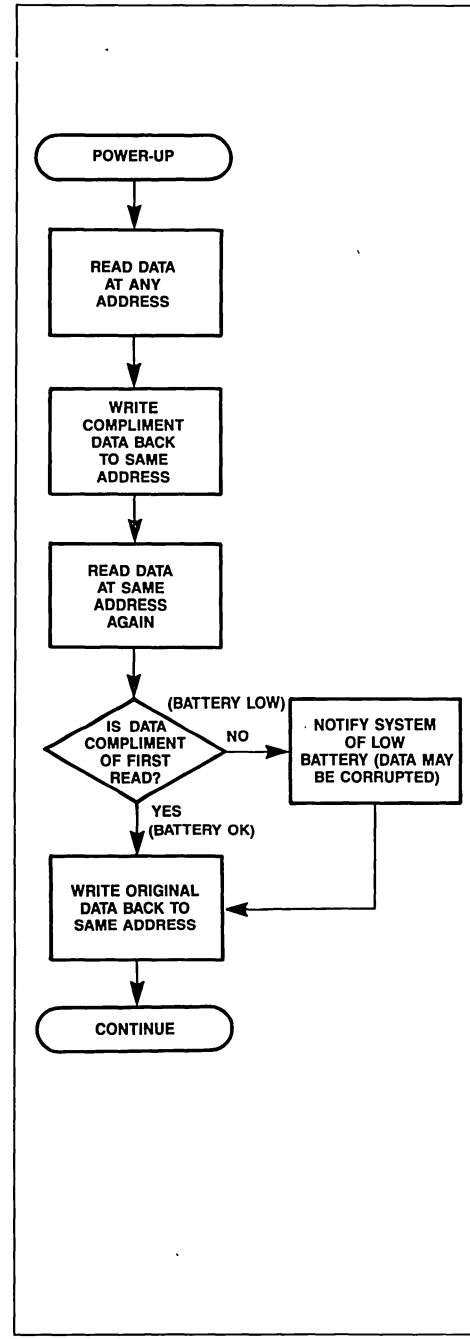
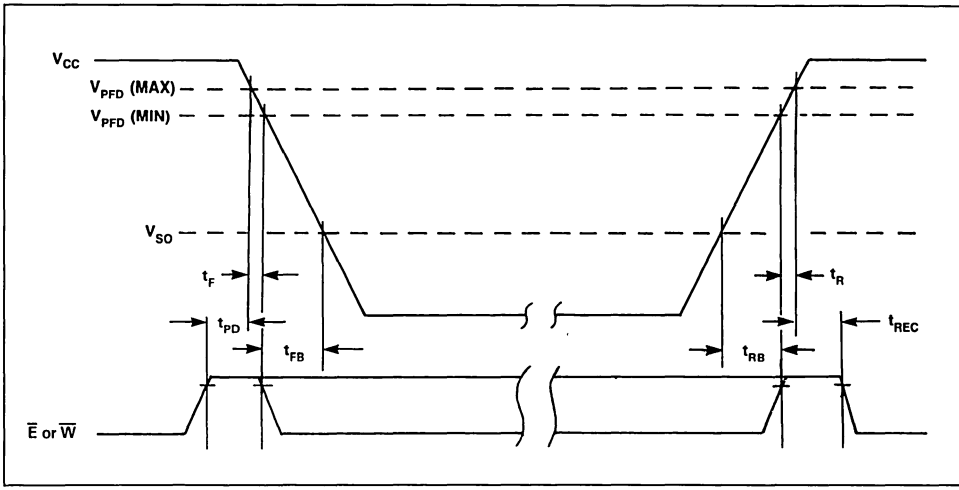


FIGURE 6. POWER-DOWN/POWER-UP TIMING



DC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TRIP POINT VOLTAGES)
$(-40°C \leq T_A \leq +85°C)$

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{PFD}	Power-fail Deselect Voltage (MKI48Z02)	4.50	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MKI48Z12)	4.20	4.3	4.50	V	1
V_{SO}	Battery Back-up Switchover Voltage		3		V	1

AC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TIMING)
$(-40°C \leq T_A \leq +85°C)$

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		ns	
t_F	V_{PFD} (Max) to V_{PFD} (Min) V_{CC} Fall Time	300		µs	2
t_{FB}	V_{PFD} (Min) to V_{SO} V_{CC} Fall Time	10		µs	3
t_{RB}	V_{SO} to V_{PFD} (Min) V_{CC} Rise Time	1		µs	
t_R	V_{PFD} (Min) to V_{PFD} (Max) V_{CC} Rise Time	0		µs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	2		ms	

NOTES:
1. All voltages referenced to GND.
2. V_{PFD} (Max) to V_{PFD} (Min) fall times of less t_F may result in deselection/write protection not occurring until 50 µs after V_{CC} passes V_{PFD} (Min). V_{PFD} (Max) to (Min) fall times of less than 10 µs may cause corruption of RAM data.
3. V_{PFD} (Min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data.

CAUTION

Negative undershoots below −0.3 volts are not allowed on any pin while in Battery Back-up mode.

DATA RETENTION TIME

About Figure 7

Figure 7 illustrates how expected MKI48Z02/12 battery life is influenced by temperature. The life of the battery is controlled by temperature and is virtually independent of the percentage of time the MKI48Z02/12 spends in battery back-up mode.

Battery life predictions presented in Figure 7 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's ongoing battery testing since it began in 1982, we believe the likelihood of such failure mechanisms surfacing is extremely poor. For the purpose of this testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.0 volt closed-circuit voltage across a 250K ohm load resistance.

A Special Note: The summary presented in Figure 7 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final; they can be expected to change as yet more data becomes available. We believe that future read-points of life tests presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 7. They are labeled "Average ($t_{50\%}$)" and "($t_{1\%}$)". These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 80°C is at issue, Figure 7 indicates that a particular MKI48Z02/12 has a 1% chance of having a battery failure 10 years into its life and a 50% chance of failure at the 17 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience battery failure within 10 years; 50% of them can be expected to fail within 17 years.

The $t_{1\%}$ figure represents the practical onset of wear-out, and is therefore suitable for use in what would normally be though of as a worst-case analysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning on the date of manufacture. Each MKI48Z02/12 is marked with a four digit manufacturing date code in the form YYWW (Example: 8502 = 1985, week 2).

Calculating Predicted Battery Life

As Figure 7 indicates, the predicted life of the battery in the MKI48Z02/12 is a function of temperature. The back-up current required by the memory matrix in the MKI48Z02/12 is so low that it has negligible influence on battery life.

Because predicted battery life is dependent upon application controlled variables, only the user can estimate predicted battery life in a given design. As long as ambient temperature is held reasonably constant, expected life can be read directly from Figure 7. If the MKI48Z02/12 spends an appreciable amount of time at a variety of temperatures, the following equations should be used to estimate battery life.

$$\text{Predicted Battery Life} = \frac{1}{[(TA_1/TT)/BL_1)]+[(TA_2/TT)/BL_2]+\ldots+[(TA_n/TT)/BL_n)]}$$

Where TA_1, TA_2, TA_n = Time at Ambient Temperature 1, 2, etc.

$$TT = \text{Total Time} = TA_1 + TA_2 + \ldots + TA_n$$

BL_1, BL_2, BL_n = Predicted Battery Lifetime at Temp 1, Temp 2, etc. (see Figure 7).

EXAMPLE PREDICTED BATTERY LIFE CALCULATION

A process control computer operates in an environment where the MKI48Z02/12 is exposed to temperatures of 50°C or less for 3066 hrs/yr; temperatures greater than 25°C, but less than 60°C, for 5256 hrs/yr; and temperatures greater than 40°C, but less than 85°C, for the remaining 438 hrs/yr.

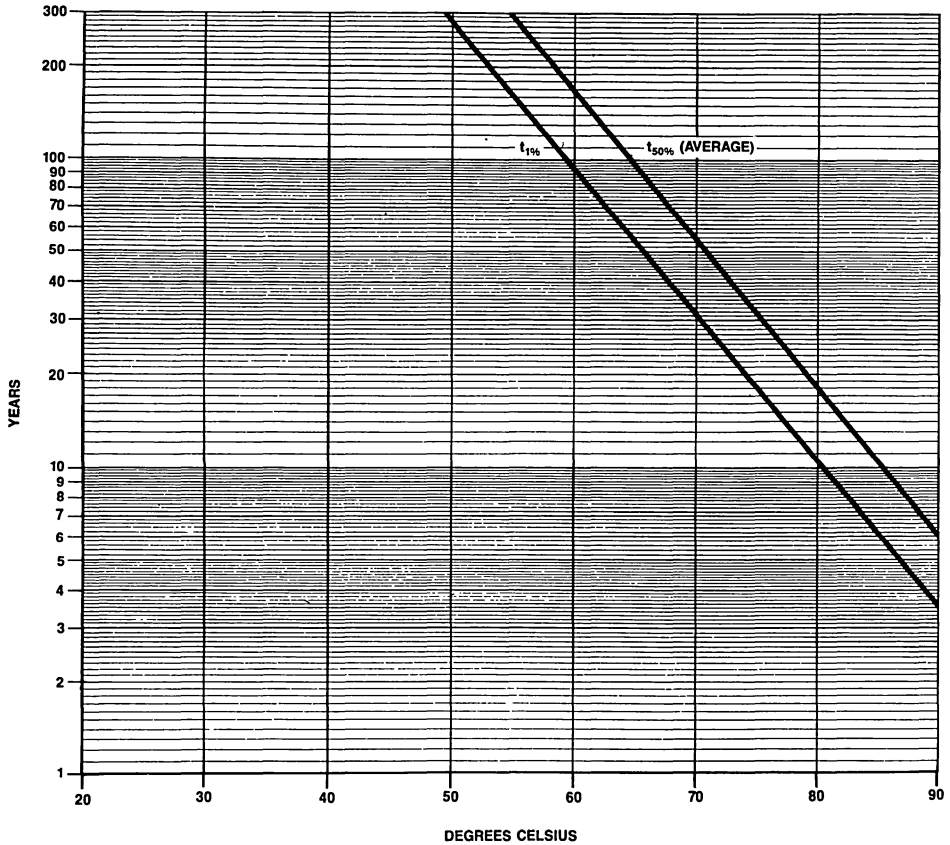
Reading predicted typical life values from Figure 7; BL_1 = 275 yrs., BL_2 = 95 yrs., BL_3 = 32 yrs.

Total Time (TT) = 8760 hrs./yr. TA_1 = 3066 hrs./yr. TA_2 =5256 hrs./yr. TA_3 = 438 hrs./yr.

$$\text{Predicted Typical Battery Life} \geq \frac{1}{[(3066/8760)/275]+[(5256/8760)/95]+[(438/8760)/32]}$$

$$\geq 109.2 \text{ yrs.}$$

FIGURE 7. MKI48Z02/12 PREDICTED BATTERY STORAGE LIFE VS TEMPERATURE



ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Pin Relative To GND ..... −0.3 V to +7.0 V
Ambient Operating (V_{CC} On) Temperature (T_A) ..... −40°C to +85°C
Ambient Storage (V_{CC} Off) Temperature ..... −40°C to +85°C
Total Device Power Dissipation ..... 1 Watt
Output Current Per Pin ..... 20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

CAUTION: Under no conditions can the "Absolute Maximum Rating" for the voltage on any pin be exceeded since it will cause permanent damage. Specifically, do not perform the "standard" continuity test on any input or output pin, i.e do not force these pins below −0.3 V DC.

RECOMMENDED DC OPERATING CONDITIONS

($-40°C \le T_A \le +85°C$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage (MKI48Z02)	4.75	5.50	V	1
V_{CC}	Supply Voltage (MKI48Z12)	4.50	5.5	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3 V	V	1
V_{IL}	Logic "0" Voltage All Inputs	−0.3	0.8	V	1,2

DC ELECTRICAL CHARACTERISTICS

($-40°C \le T_A \le +85°C$) (V_{CC} (max) $\ge V_{CC} \ge V_{CC}$ (min))

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	3
I_{CC2}	TTL Standby Current ($\overline{E} = V_{IH}$)		3	mA	
I_{CC3}	CMOS Standby Current ($\overline{E} \ge V_{CC}-0.2$ V)		1	mA	
I_{IL}	Input Leakage Current (Any Input)	−1	+1	µA	4
I_{OL}	Output Leakage Current	−5	+5	µA	4
V_{OH}	Output Logic "1" Voltage (I_{OUT} = −1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 2.1 mA)		0.4	V	

CAPACITANCE (T_A = 25°C)

SYM	PARAMETER	MAX	NOTES
C_I	Capacitance on all pins (except D/Q)	7 pF	5
$C_{D/Q}$	Capacitance on D/Q pins	10 pF	4,5

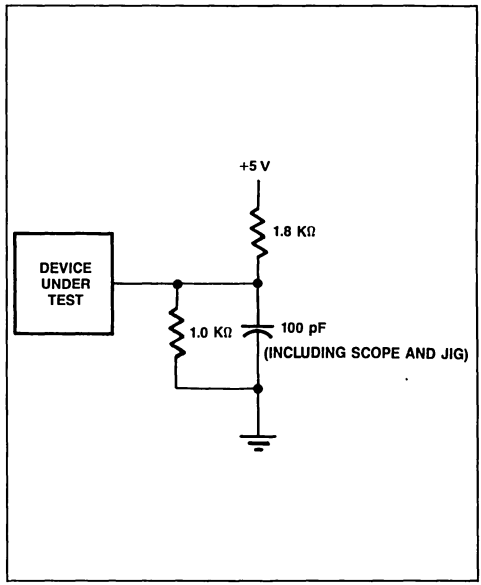
NOTES

1. All voltages referenced to GND.
2. Negative spikes of −1.0 volts allowed for up to 10 ns once per cycle.
3. I_{CC1} measured with outputs open.
4. Measured with $GND \le V_I \le V_{CC}$ and outputs deselected.
5. Effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta V = 3$ volts and power supply at nominal level.

AC TEST CONDITIONS

Input Levels:	0.6 V to 2.4 V
Transition Times:	5 ns
Input and Output Timing Reference Levels	0.8 V or 2.2 V
Ambient Temperature	−40°C to +85°C
V_{CC} (MKI48Z02)	4.75 V to 5.50 V
V_{CC} (MKI48Z12)	4.5 V to 5.50 V

FIGURE 8. OUTPUT LOAD DIAGRAM



ORDERING INFORMATION

MKI48Z	X	2	B	-XX
DEVICE FAMILY	V_{CC} RANGE		PACKAGE	SPEED

-15 150 NS ACCESS TIME
-20 200 NS ACCESS TIME
-25 250 NS ACCESS TIME

B PLASTIC WITH BATTERY TOP HAT

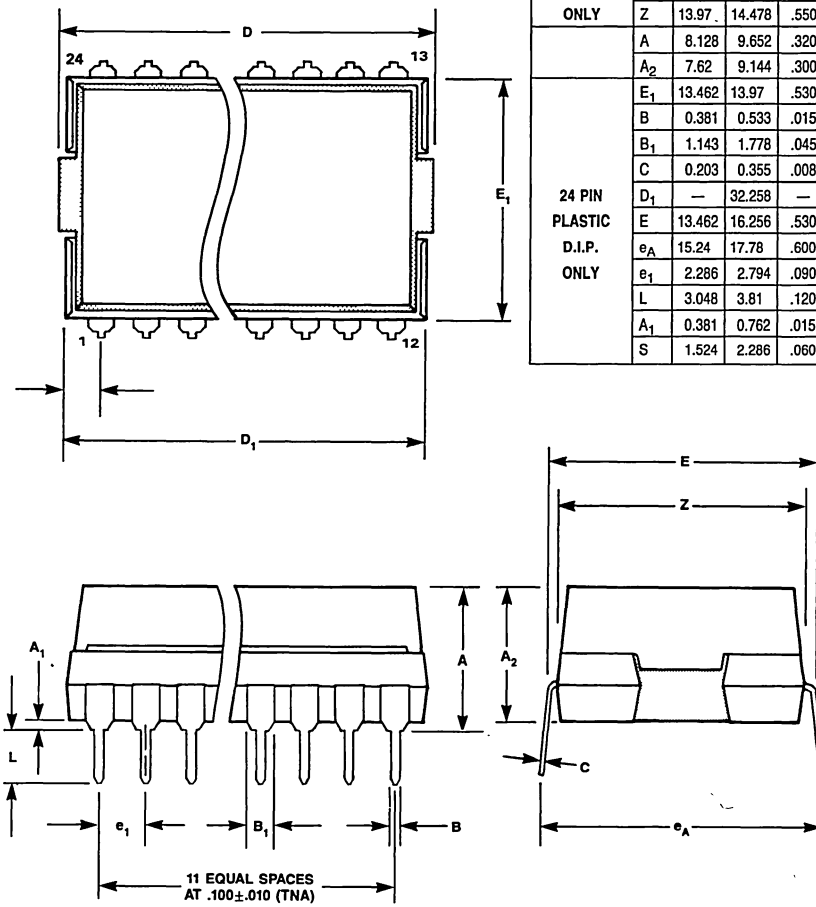
0 +10%/−5%
1 +10%/−10%

MKI Industrial Temp. Range −40°C to +85°C

PACKAGE DESCRIPTION

B PACKAGE 24 PIN

	Dim.	mm		inches		Notes
		Min	Max	Min	Max	
BATTERY ONLY	D	—	32.893	—	1.295	
	Z	13.97	14.478	.550	.570	
	A	8.128	9.652	.320	.380	
	A_2	7.62	9.144	.300	.360	
24 PIN PLASTIC D.I.P. ONLY	E_1	13.462	13.97	.530	.550	
	B	0.381	0.533	.015	.021	4
	B_1	1.143	1.778	.045	.070	
	C	0.203	0.355	.008	.014	4
	D_1	—	32.258	—	1.270	1
	E	13.462	16.256	.530	.640	
	e_A	15.24	17.78	.600	.700	3
	e_1	2.286	2.794	.090	.110	
	L	3.048	3.81	.120	.150	
	A_1	0.381	0.762	.015	.030	2
	S	1.524	2.286	.060	.090	



NOTES:
1. Overall length includes .010 in. flash on either end of the package.
2. Package standoff to be measured per JEDEC requirements
3. Measured from centerline to centerline at lead tips
4. When the solder lead finish is specified, the maximum limit shall be increased by .003 in.

MILITARY SRAMs

IMS1203M
CMOS High Performance 4K x 1 Static RAM MIL-STD-883C

inmos®

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- Specifications guaranteed over full military temperature range (-55° C to + 125° C)
- 4K x 1 Bit Organization
- 25, 35, and 45 nsec Access Times
- Single +5V ± 10% Operation
- Power Down Function
- Fully TTL Compatible
- Separate Data Input and Output
- Three-state Output
- Standard Military Drawing version available
- 18-Pin, 300-mil DIP (JEDEC Std.) and FP

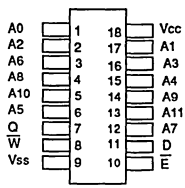
DESCRIPTION

The INMOS IMS1203M is a high speed CMOS 4Kx1 static RAM processed in full compliance to MIL-STD-883C. The IMS1203M provides performance enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1203M features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1203M provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

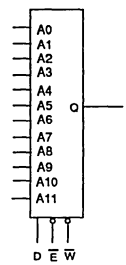
The IMS1203M is a VLSI static RAM intended for military temperature applications that demand superior performance and reliability.

PIN CONFIGURATION

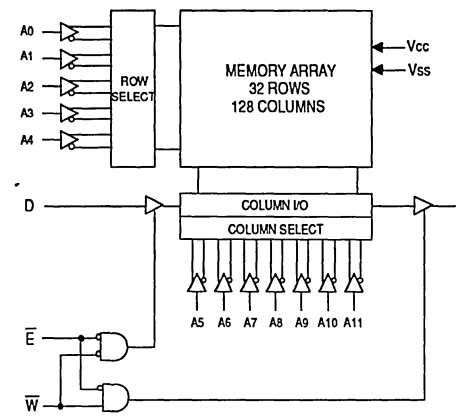


DIP & FLAT PACK

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{11}	ADDRESS INPUTS	Vcc POWER (+5V)
W	WRITE ENABLE	Vss GROUND
D	DATA INPUT	
E	CHIP ENABLE	
Q	DATA OUTPUT	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on Q.....-1.0 to (Vcc+0.5)
Temperature Under Bias... -55° C to 125°C
Storage Temperature .... -55° C to 150°C
Power Dissipation..... .....1W
DC Output Current..... .....25mA
(One Second Duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+0.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	-55	25	125	°C	400 linear ft/min air flow

*V_{IL} min = -3.0 V for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS (-55°C ≤ T_A ≤ 125°C) (V_{CC} = 5.0V ± 10%)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		80	mA	t_{AVAV} = t_{AVAV}(min)
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		15	mA	$\overline{E}$ ≥ V_{IH} . All other inputs at V_{IN} ≤ V_{IL} or ≥ V_{IH}
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		5	mA	$\overline{E}$ ≥ (Vcc - 0.2). All other inputs at V_{IN} ≤ 0.2 or ≥ (Vcc - 0.2V)
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		10	mA	$\overline{E}$ ≥ (Vcc - 0.2) . Inputs cycling at V_{IN} ≤ 0.2 or ≥ (Vcc - 0.2V)
I_{ILK}	Input Leakage Current (Any Input)		± 5	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		± 10	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 12mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels	Vss to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0 MHz)[b]

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	4	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

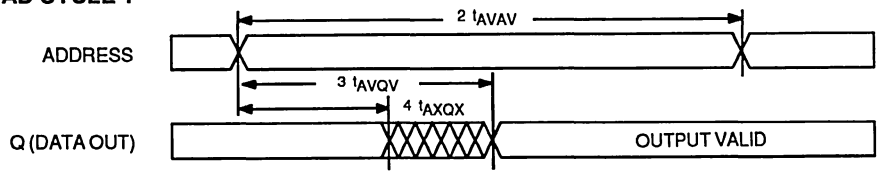
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[g]

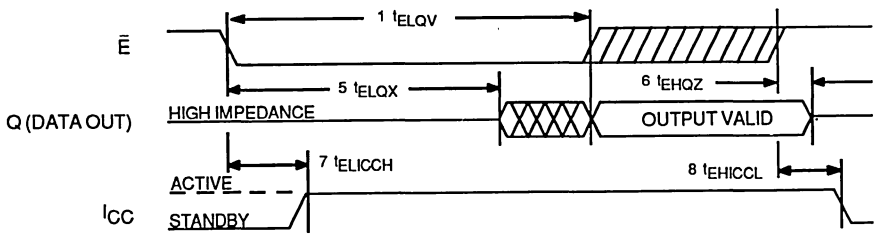
NO.	SYMBOL		PARAMETER	1203M-25		1203M-35		1203M-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	25		35		45		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		25		35		45	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		5		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	j
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive	0	15	0	20	0	20	ns	f, j
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
8	t_{EHICCL}	t_{PD}	Chip Disable to Power Down		30		30		30	ns	j
		t_T	Input Rise and Fall Times		50		50		50	ns	e, j

Note c: For READ CYCLES 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected, $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ± 200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



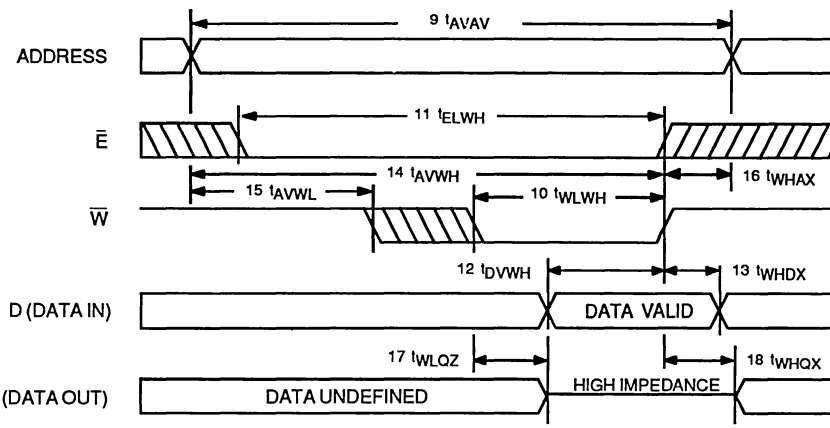
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	IMS1203M-25		IMS1203M-35		IMS1203M-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
9	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns	
10	t_{WLWH}	t_{WP}	Write Pulse Width	15		20		25		ns	
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write	20		30		40		ns	
12	t_{DVWH}	t_{DW}	Data Set-up to End of Write	15		20		20		ns	
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
14	t_{AVWH}	t_{AW}	Address Set-up to End of Write	20		30		40		ns	
15	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	15	0	20	0	20	ns	f, j
18	t_{WHQX}	t_{OW}	Output Active After End of Write	0		0		0		ns	i, j

Note f: Measured ± 200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



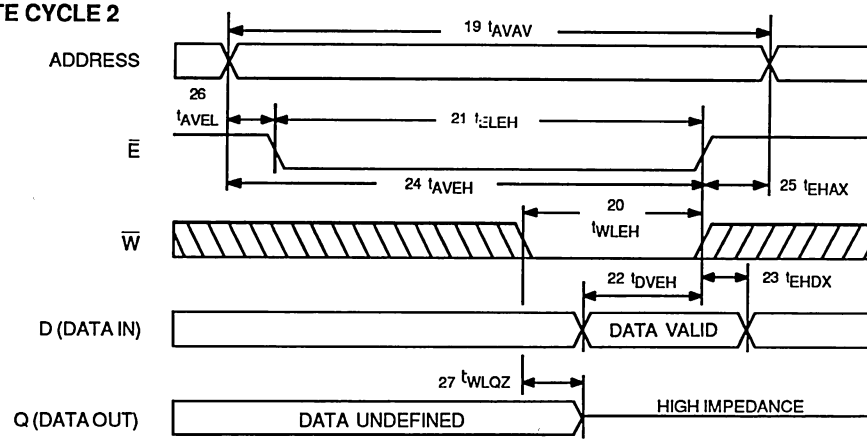
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	IMS1203M-25		IMS1203M-35		IMS1203M-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	15		20		25		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		30		40		ns	
22	t_{DVEH}	t_{DW}	Data Set-up to End of Write	15		20		20		ns	
23	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
24	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		30		40		ns	
25	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
26	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	15	0	20	0	20	ns	f, j

Note f: Measured ± 200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1203M has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), twelve address inputs (A_0-A_{11}), a Data In (D) and a Data Out (Q). The $\overline{E}$ input controls device selection as well as active and standby modes. With $\overline{E}$ low, the device is selected and the twelve address inputs are decoded to select one bit out of 4K bits. Read and Write operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than one-fourth of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The outputs remain active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and as long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable when $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when $\overline{E}$ goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1203M is initiated by the latter of $\overline{E}$ or $\overline{W}$ to transition from a high to low. In the case of $\overline{W}$ falling last, the output buffer will be turned on t_{ELOX} after the falling edge of $\overline{E}$ (just as in a read cycle). The output buffer is then turned off within t_{WLQZ} of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with D and Q connected together in a common I/O configuration. Contention can be avoided in a carefully designed system. During a write cycle, data on the input is written into the selected cells and the output is floating.

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. When $\overline{W}$ goes high at the end of the cycle with $\overline{E}$ active, the output of the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, the outputs remain in the high impedance state.

APPLICATION

It is imperative when designing with any very high speed memory, such as the IMS1203M, that the fundamental rules in regard to memory board layout be followed to ensure proper system operation.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

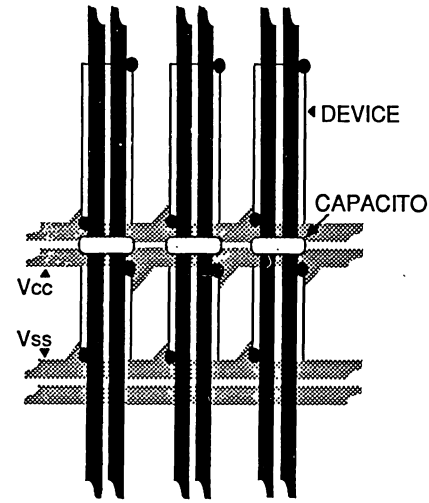
Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1203M. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1203M have very high frequency components, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad, and be placed between each row of devices in the array (see drawing). A larger tantalum capacitor, with a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

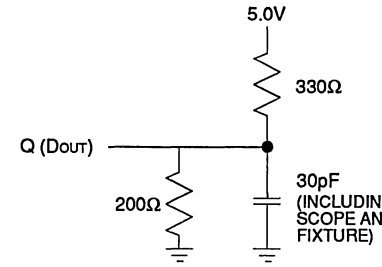
The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

FIGURE 1. OUTPUT LOAD



TRUTH TABLE

$\overline{E}$	$\overline{W}$	Q	MODE
H	X	HI-Z	Standby (Isb)
L	H	Dout	Read
L	L	HI-Z	Write

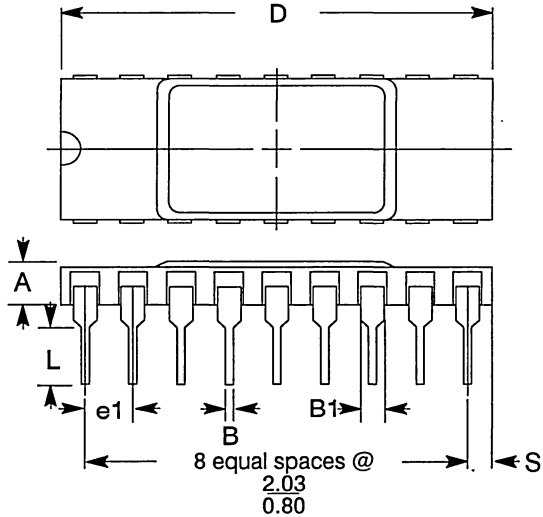
Standard Military Drawing version available, see SMD Reference Guide

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS 1203M	25ns	CERAMIC DIP	IMS1203S-25M
	25ns	FLAT PACK	IMS1203A-25M
	35ns	CERAMIC DIP	IMS1203S-35M
	35ns	FLAT PACK	IMS1203A-35M
	45ns	CERAMIC DIP	IMS1203S-45M
	45ns	FLAT PACK	IMS1203A-45M

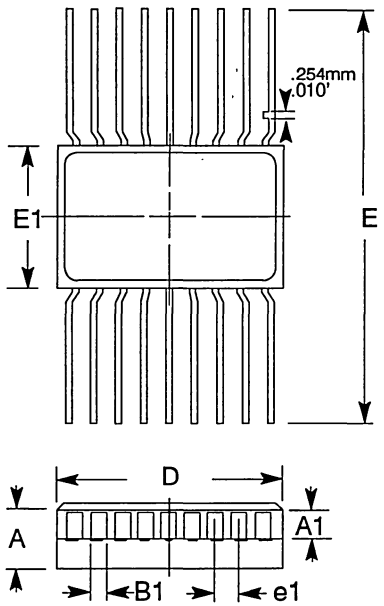
PACKAGING INFORMATION

18 Pin Ceramic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.085	.010	2.18	.230
B	.018	.003	.457	.152
B1	.054	Typ	.137	Typ
D	.900	.011	22.86	.279
E	.310	.010	7.874	.254
E1	.295	.015	7.493	.381
e1	.100	.010	2.54	.254
L	.145	.020	3.683	.508
S	.005		.127	

18 Pin Flat Pack



Dim	Inches		mm		Notes
	Nom	Tol	Nom	Tol	
A	.081	.007	2.057	.178	
A1	.045		1.143		
B1	.028	Ref	.711	Ref	
D	.432	.005	10.973	.127	
C	.005	.002	.127	.051	
E	1.00	Ref	25.40	Ref	
e1	.047		1.194		
eA	.230	.005	5.842	.127	

IMS1223M
CMOS
High Performance
1K x 4 Static RAM
MIL-STD-883C

inmos®

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- Specifications guaranteed over full military temperature range (-55° C to + 125° C)
- 1K x 4 Bit Organization
- 25, 35, and 45 nsec Access Times
- Fully TTL Compatible
- Single +5V ± 10% Operation
- Power Down Function
- Common Data Input and Output
- Three-state Output
- Standard Military Drawing version available
- 18-Pin, 300-mil DIP (JEDEC Std.) and FP

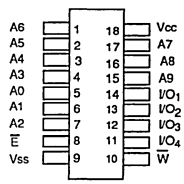
DESCRIPTION

The INMOS IMS1223M is a high speed CMOS 1Kx4 static RAM processed in full compliance to MIL-STD-883C. The IMS1223M provides performance enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1223M features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1223M provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

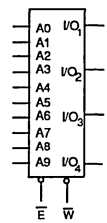
The IMS1223M is a VLSI static RAM intended for military temperature applications that demand superior performance and reliability.

PIN CONFIGURATION

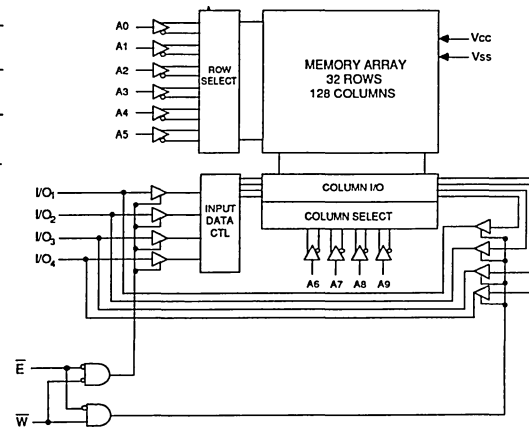


DIP &
FLAT PACK

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_9	ADDRESS INPUTS	Vcc	POWER
W̄	WRITE ENABLE	Vss	GROUND
Ē	CHIP ENABLE		
I/O	DATA IN/OUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on Q.....-1.0 to (Vcc+0.5)
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One Second Duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+0.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	-55	25	70	°C	400 linear ft/min air flow

*V_{IL} min = -3 V for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS (-55°C ≤ T_A ≤ 125°C) (V_{CC} = 5.0V ± 10%)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		110	mA	t_{AVAV} = t_{AVAV}(min)
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		15	mA	E ≥ V_{IH} . All other inputs at V_{IN} ≤ V_{IL} or ≥ V_{IH}
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		5	mA	E ≥ (Vcc - 0.2) . All other inputs at V_{IN} ≤ 0.2 or ≥ (Vcc - 0.2V)
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		10	mA	E ≥ (Vcc - 0.2) . Inputs cycling at V_{IN} ≤ 0.2 or ≥ (Vcc - 0.2V)
I_{ILK}	Input Leakage Current (Any Input)		±5	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		±10	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 8mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels .....V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0MHZ)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	4	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

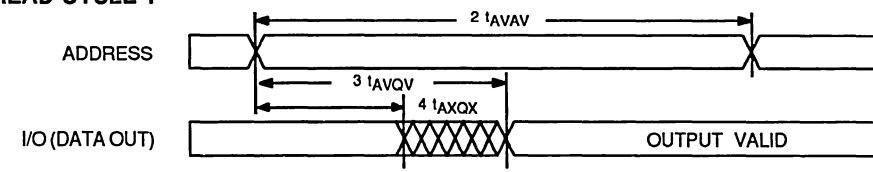
RECOMMENDED AC OPERATING CONDITIONS $-55°C \leq T_A \leq 125°C$) ($V_{CC}$ = 5.0V ± 10%)

READ CYCLE[g]

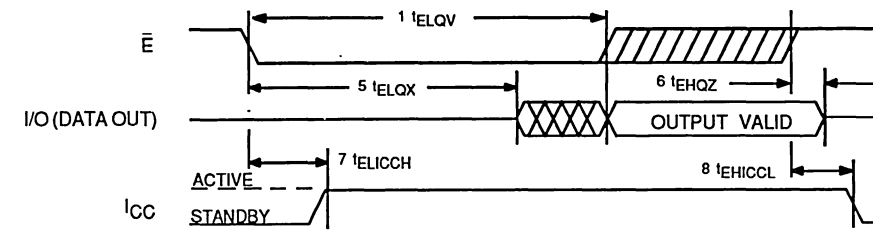
NO.	SYMBOL		PARAMETER	1223M-25		1223M-35		1223M-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	25		35		45		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		25		35		45	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		5		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	j
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive	0	15	0	20	0	20	ns	f, j
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
8	t_{EHICCL}	t_{PD}	Chip Disable to Power Down		30		30		30	ns	j
		t_T	Input Rise and Fall Times		50		50		50	ns	e, j

Note c: For READ CYCLES 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected, $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ± 200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c, d]



READ CYCLE 2[c]



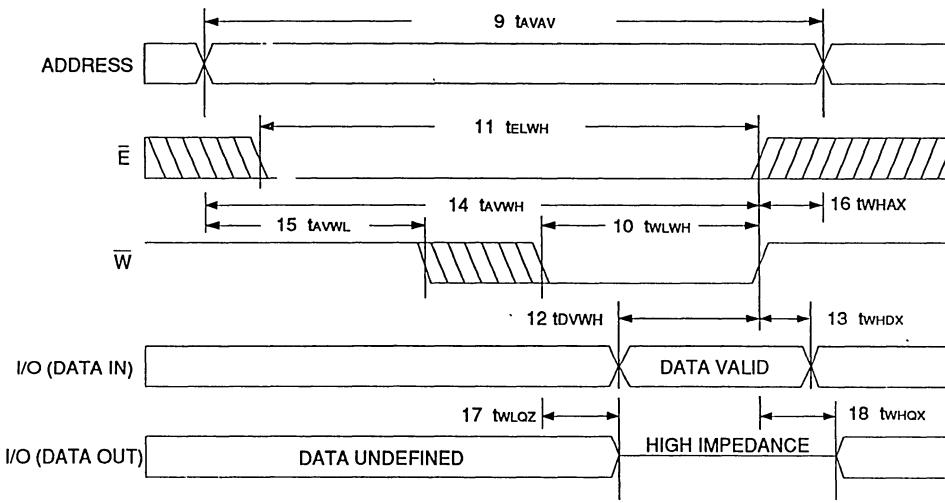
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \le T_A \le 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g,h]

NO.	SYMBOL		PARAMETER	1223M-25		1223M-35		1223M-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
9	tAVAV	twc	Write Cycle Time	20		30		40		ns	
10	tWLWH	twp	Write Pulse Width	15		20		25		ns	
11	tELWH	tcw	Chip Enable to End of Write	20		30		40		ns	
12	tDVWH	tDW	Data Setup to End of Write	15		20		25		ns	
13	tWHDX	tDH	Data Hold after End of Write	0		0		0		ns	
14	tAVWH	taw	Address Setup to End of Write	20		30		40		ns	
15	tAVWL	tAS	Address Setup to Start of Write	0		0		0		ns	
16	tWHAX	twR	Address Hold after End of Write	0		0		0		ns	
17	tWLQZ	twz	Write Enable to Output Disable	0	15	0	20	0	20	ns	f, j
18	tWHQX	tow	Output Active after End of Write	5		5		5		ns	i, j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\ge V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



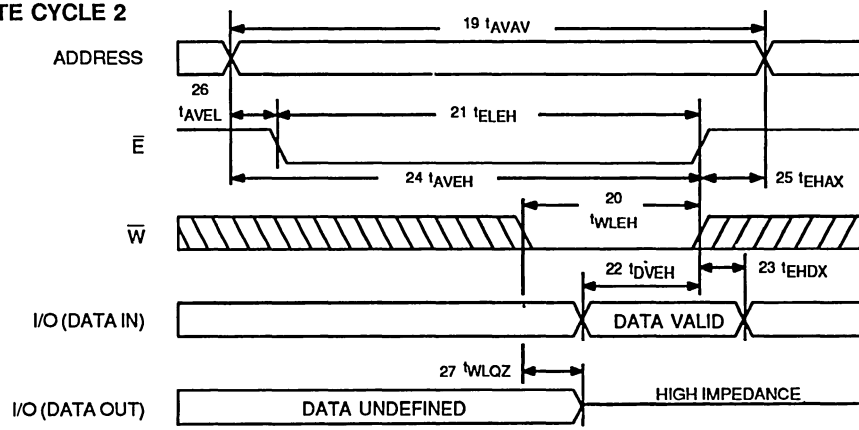
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	1223M-25		1223M-35		1223M-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	20		30		40		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	15		20		25		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		30		40		ns	
22	t_{DVEH}	t_{DW}	Data Set-up to End of Write	10		15		15		ns	
23	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
24	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		30		40		ns	
25	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
26	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
27	t_{WLOZ}	t_{WZ}	Write Enable to Output Disable	0	15	0	20	0	20	ns	f, j

Note f: Measured ± 200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1223M has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), ten address inputs (A_0-A_9), and four Data I/O lines. The $\overline{E}$ input controls device selection as well as active and standby modes. With $\overline{E}$ low, the device is selected and the ten address inputs are decoded to select one four-bit word out of 1K words. Read and Write operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled and the power consumption is reduced to less than one-fourth of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The outputs remain active throughout READ CYCLE 1 and are valid at the specified address access time. The address inputs may change at access time and as long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable when $\overline{E}$ goes low, valid data is at the outputs at the specified Chip Enable Access time. If address is not valid when $\overline{E}$ goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1223M is initiated by the latter of $\overline{E}$ or $\overline{W}$ to transition from a high to a low. In the case of $\overline{W}$ falling last, the output buffers will be turned on t_{ELQX} after the falling edge of $\overline{E}$ (just as in a read cycle). The output buffers are then turned off within t_{WLQZ} of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with common I/O configurations. To avoid bus contention, input data should not become active on the I/O bus until t_{WLQZ}.

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. When $\overline{W}$ goes high at the end of the cycle with $\overline{E}$ active, the output of the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high the outputs remain in the high impedance state.

APPLICATION

It is imperative when designing with any very high speed memory, such as the IMS1223M, that the fundamental rules in regard to memory board layout be followed to ensure proper system operation.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

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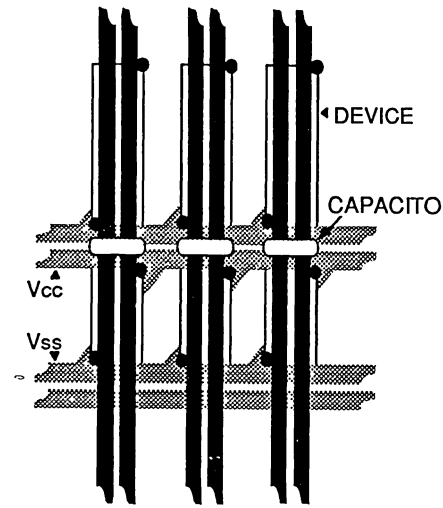
Since the current transients associated with the operation of the high speed IMS1223M have very high frequency components, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad, and be placed between each row of devices in the array (see drawing). A larger tantalum capacitor, with a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

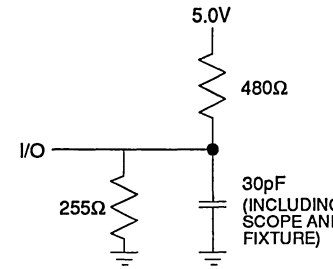
The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

FIGURE 1. OUTPUT LOAD



TRUTH TABLE

$\overline{E}$	$\overline{W}$	Q	MODE
H	X	HI-Z	Standby (Isb)
L	H	Dout	Read
L	L	Din	Write

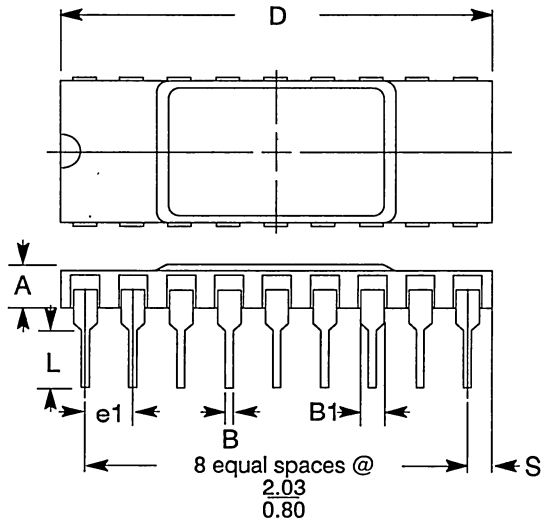
Standard Military Drawing version available, see SMD Reference Guide

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS 1223M	25ns	CERAMIC DIP	IMS1223S-25M
	25ns	FLAT PACK	IMS1223A-25M
	35ns	CERAMIC DIP	IMS1223S-35M
	35ns	FLAT PACK	IMS1223A-35M
	45ns	CERAMIC DIP	IMS1223S-45M
	45ns	FLAT PACK	IMS1223A-45M

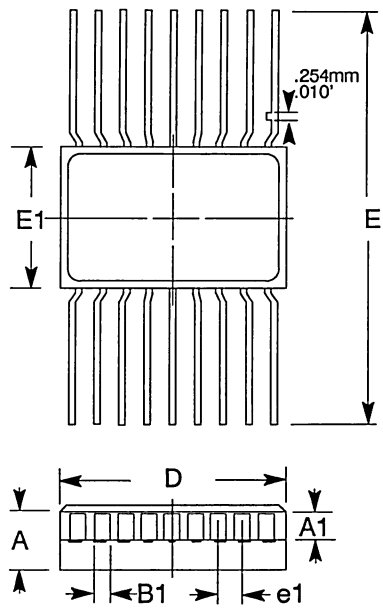
PACKAGING INFORMATION

18 Pin Ceramic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.085	.010	2.18	.230
B	.018	.003	.457	.152
B1	.054	Typ	.137	Typ
D	.900	.011	22.86	.279
E	.310	.010	7.874	.254
E1	.295	.015	7.493	.381
e1	.100	.010	2.54	.254
L	.145	.020	3.683	.508
S	.005		.127	

18 Pin Flat Pack



Dim	Inches		mm		Notes
	Nom	Tol	Nom	Tol	
A	.081	.007	2.057	.178	
A1	.045		1.143		
B1	.028	Ref	.711	Ref	
D	.432	.005	10.973	.127	
C	.005	.002	.127	.051	
E	1.00	Ref	25.40	Ref	
e1	.047		1.194		
eA	.230	.005	5.842	.127	

IMS1400M

High Performance 16K Static RAM MIL-STD-883C

FEATURES

- Full Military Temperature Operating Range (-55°C to +125°C)
- MIL-STD-883C Processing
- 45, 55 and 70 nsec Access Times
- Fully TTL Compatible
- Separate Data Input & Output
- Three-state Output
- Power Down Function
- Single +5V ± 10% Operation
- 20-Pin, 300-mil DIP (JEDEC Std.)
- 20-Pin Ceramic LCC (JEDEC Std.)

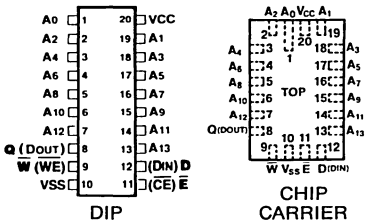
DESCRIPTION

The INMOS IMS1400M is a high performance 16Kx1 Static RAM processed in full compliance to MIL-STD-883C with access times as fast as 45nsec and a maximum power consumption of 660mW. These characteristics are made possible by the combination of innovative circuit design and INMOS' proprietary NMOS technology.

The IMS1400M features fully static operation requiring no external clocks or timing strobes with equal access and cycle times. Additionally, the IMS1400M provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode reducing consumption to less than 165mW.

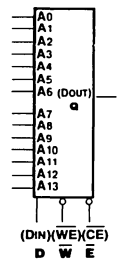
The IMS1400M is a high speed VLSI RAM intended for military applications which demand superior performance and reliability.

PIN CONFIGURATION

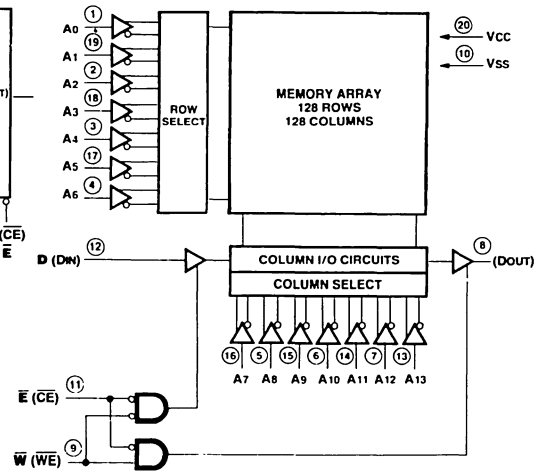


DIP CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A0 - A13	ADDRESS INPUTS	VCC	POWER (+5V)
W (WE)	WRITE ENABLE	VSS	GROUND
E (CE)	CHIP ENABLE		
D (DIN)	DATA INPUT		
Q (DOUT)	DATA OUTPUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −3.5 to 7.0V
Temperature Under Bias . . . . . −65°C to 135°C
Storage Temperature (Ambient) . . . . . −65°C to 150°C
Power Dissipation 1W
DC Output Current 50mA

*Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect reliability

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		6.0	V	All Inputs
V_{IL}	Input Logic "0" Voltage	−2.0		0.8	V	All Inputs
T_A	Ambient Operating Temperature	−55		125	°C	400 Linear ft/min transverse air flow

DC ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current AC		120	mA	$t_C = t_C$ min
I_{CC2}	V_{CC} Power Supply Current (Standby)		30	mA	$\overline{E} \geq V_{IH}$ min
I_{IN}	Input Leakage Current (Any Input)	−10	10	μA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current	−50	50	μA	V_{CC} = max $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage $I_{OUT} = -4mA$	2.4		V	
V_{OL}	Output Logic "0" Voltage $I_{OUT} = 16mA$		0.4	V	

AC TEST CONDITIONS[a]

Input Pulse Levels	V_{SS} to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1 5V
Output Load	See Figure 1

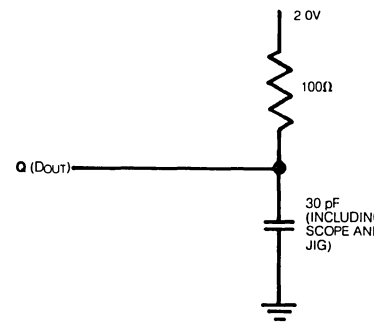
Note a Operation to specifications guaranteed 2ms after V_{CC} applied

CAPACITANCE[b] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNIT	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V
$C_{\overline{E}}$	$\overline{E}$ Capacitance	6	pF	ΔV = 0 to 3V

Note b This parameter is sampled and not 100% tested

FIGURE 1. OUTPUT LOAD



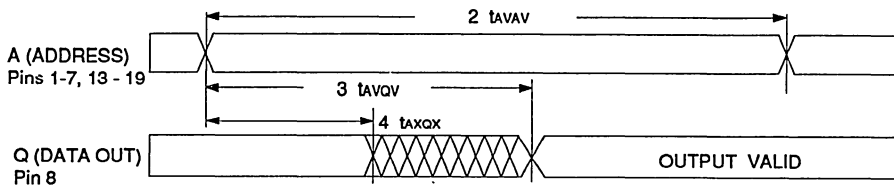
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE

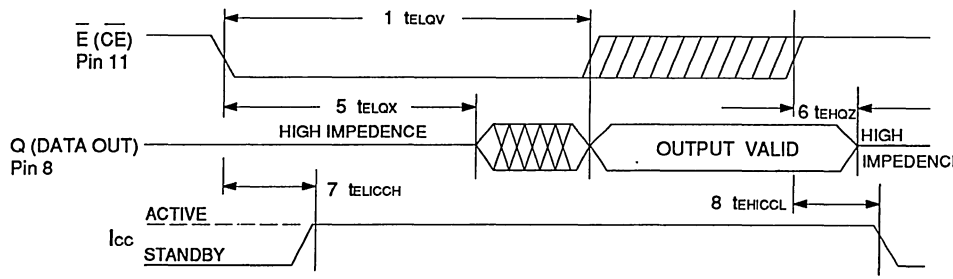
NO.	SYMBOL		PARAMETER	1400M-45		1400M-55		1400M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		45		55		70	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	40		50		65		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		40		50		65	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	3		3		0		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	3		5		5		ns	
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Disable	0	25	0	30	0	40	ns	f
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
8	t_{EHICCL}	t_{PD}	Chip Enable to Power Down	0	45	0	55	0	70	ns	j
		t_T	Input Rise and Fall Times		50		50		50	ns	e

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2 [c]



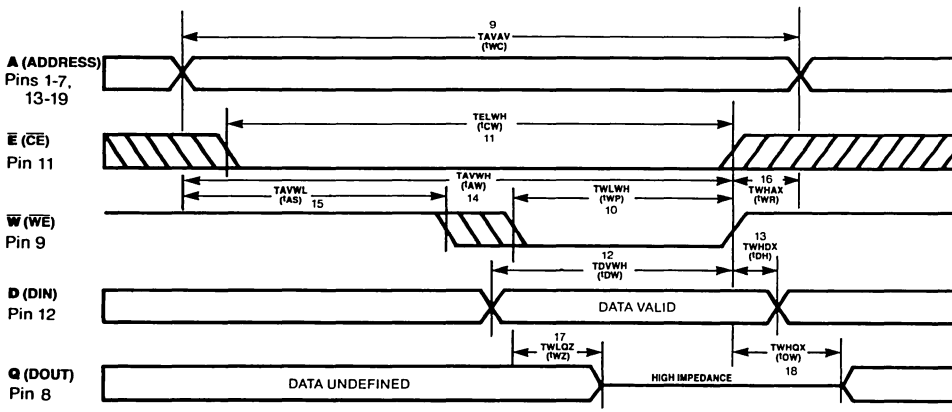
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[h]

NO.	SYMBOL		PARAMETER	1400M-45		1400M-55		1400M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
9	t_{AVAV}	t_{WC}	Write Cycle Time	40		50		65		ns	
10	t_{WLWH}	t_{WP}	Write Pulse Width	20		25		30		ns	
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write	40		50		60		ns	
12	t_{DVWH}	t_{DW}	Data Set-up to End of Write	15		20		23		ns	
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	0		0		8		ns	
14	t_{AVWH}	t_{AW}	Address Set-up to End of Write	40		50		55		ns	
15	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	8		8		8		ns	
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	0		0		10		ns	
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	25	0	28	ns	f
18	t_{WHQX}	t_{OW}	Output Active After End of Write	0	25	0	30	0	40	ns	g, j

Note f: Measured ±200mV from steady state output voltage.
Note g: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



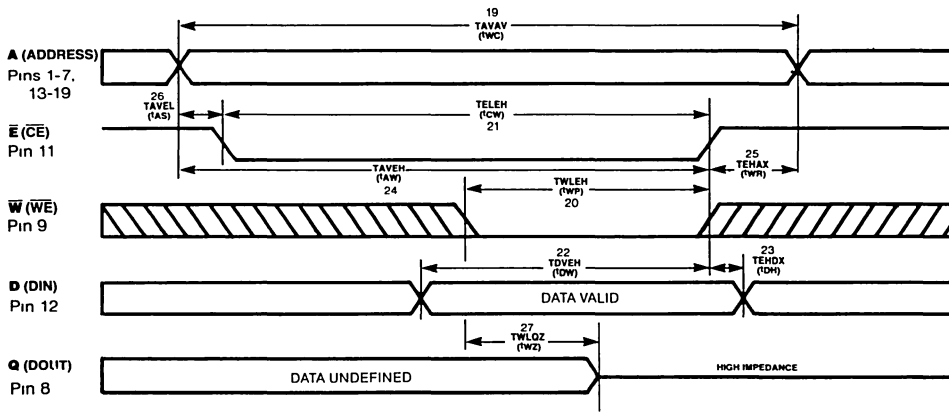
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[h]

NO.	SYMBOL		PARAMETER	1400M-45		1400M-55		1400M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	40		50		65		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	40		50		60		ns	
22	t_{DVEH}	t_{DW}	Data Set-up to End of Write	15		20		23		ns	
23	t_{EHDX}	t_{DH}	Data Hold After End of Write	5		5		10		ns	
24	t_{AVEH}	t_{AW}	Address Set-up to End of Write	40		50		55		ns	
25	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		10		ns	
26	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	−5		−5		−5		ns	
27	t_{WLOZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	25	0	28	ns	f

Note f: Measured ± 200mV from steady state output voltage.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transition.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1400M has two control inputs: Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), 14 address inputs, a data in (D_{IN}) and a data out (D_{OUT}).

When V_{CC} is first applied to pin 20, a circuit associated with the $\overline{E}$ input forces the device into the lower power standby mode regardless of the state of the $\overline{E}$ input. After V_{CC} is applied for 2ms the $\overline{E}$ input controls device selection as well as active and standby modes.

With $\overline{E}$ low, the device is selected and the 14 address inputs are decoded to select one memory cell out of 16,385. READ and WRITE operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than ¼ of the active mode power.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform on page 3 shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low The output remains active throughout a READ CYCLE 1 and is valid at the specified address access time. As long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform on page 3 shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable within 5ns after $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable access time. If address is not valid within 5ns after $\overline{E}$ goes low, the timing is as specified in the READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

A write cycle is initiated by the latter of $\overline{W}$ or $\overline{E}$ going low, and terminated by $\overline{W}$ (WRITE CYCLE 1) or $\overline{E}$ (WRITE CYCLE 2) going high. During the write cycle, data on the input (D_{IN}) is written into the selected cell, and the output (D_{OUT}) is in high impedance.

If a write cycle is initiated by $\overline{W}$ going low, the address must be stable for the WRITE CYCLE 1 set-up time. If a write cycle is initiated by $\overline{E}$ going low, the address must be held stable for the entire write cycle. After $\overline{W}$ or $\overline{E}$ goes high to terminate the cycle, addresses may change. If these address set-up and hold times are not met, contents of other cells may be altered in unpredictable ways.

WRITE CYCLE 1 waveform on page 4 shows a write cycle terminated by $\overline{W}$ going high. D_{IN} set-up and hold times are referenced to the rising edge of $\overline{W}$. With $\overline{W}$ high, D_{OUT} becomes active.

WRITE CYCLE 2 waveform on page 5 shows a write cycle terminated by $\overline{E}$ going high. D_{IN} set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, D_{OUT} remains in the high impedance state.

APPLICATION

To ensure proper operation of the extended temperature IMS1400M in a system environment, it is recommended that the following guidelines on board layout and power distribution be followed.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors. The impedance in the decoupling path from the power pin (20) through the decoupling capacitor, to the ground pin (10) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

To reduce the power line impedance, it is recommended that the power trace and ground trace be gridded or provided by separate power planes. The high frequency decoupling capacitor should have a value of 0.1μF, and be placed between the rows of memory devices in the array (see Figure 2). A larger tantalum capacitor with a value between 22μF and 47μF should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These large capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

Also, to prevent loss of signal margins due to differential ground noise, the ground grid of the memory array should be extended to the TTL drivers in the peripheral circuitry.

TERMINATION

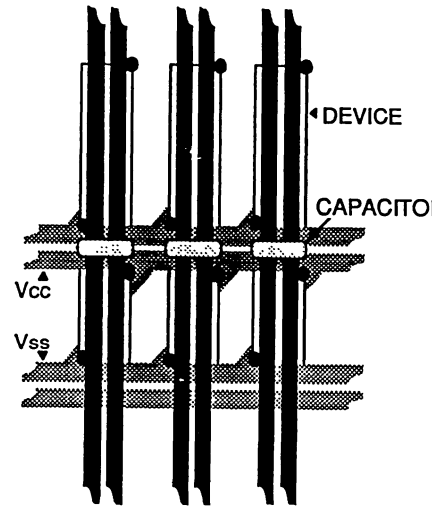
Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals, line termination is recommended. The termination may be either parallel or series but the series termination technique has the advantages of drawing no DC current and using a minimum of components. The recommended technique is to use series termination.

A series resistor in the signal line at the output of the TTL driver to match the source impedance of the TTL driver to the signal line will dampen the reflections on the line. The line should be kept short with the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10Ω to 30Ω range will be required.

The use of proper power distribution techniques, including adequate use of decoupling capacitors, along with proper termination of TTL driver outputs, are some of the most important, yet basic rules to be followed.

The rules are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment relatively free of noise spikes and signal reflections.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

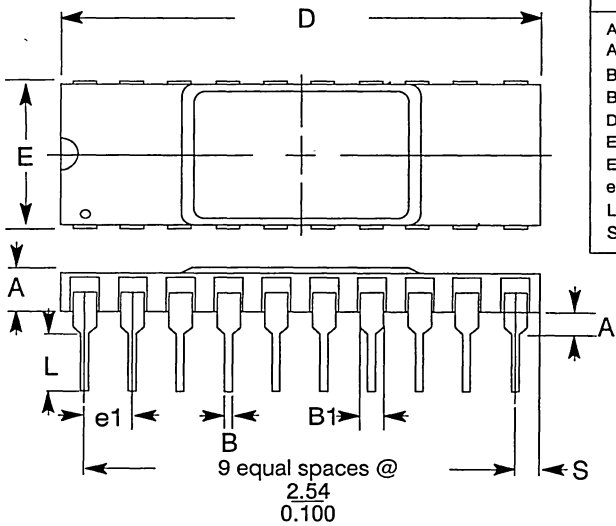
Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS 1400M	45ns	CERAMIC DIP	IMS1400S-45M
	45ns	CERAMIC LCC	IMS1400N-45M
	55ns	CERAMIC DIP	IMS1400S-55M
	55ns	CERAMIC LCC	IMS1400N-55M
	70ns	CERAMIC DIP	IMS1400S-70M
	70ns	CERAMIC LCC	IMS1400N-70M

PACKAGING INFORMATION

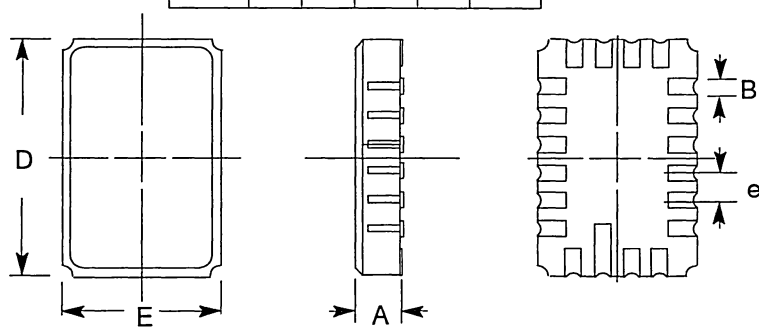
20 Pin Ceramic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.096	.012	2.438	.305
A1	.015		.381	
B	.018	.003	.457	.152
B1	.054	Typ	.137	Typ
D	1.00	.015	25.40	.381
E	.315	.010	8.001	.254
E1	.295	.015	7.493	.381
e1	.100	.010	2.54	.254
L	.125	min	3.175	min
S	.005		.127	

20 Pin Leadless Chip Carrier

Dim	Inches		mm		Notes
	Nom	Tol	Nom	Tol	
A	.071	.007	1.803	.178	
B1	.025	.003	.635	.076	
D	.425	.010	10.795	.254	
E	.290	.010	7.360	.254	
e1	.050	.005	1.270		



IMS1403M
IMS1403LM
CMOS High Performance 16K x 1 Static RAM MIL-STD-883C

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- Specifications guaranteed over full military temperature range (-55° C to +125° C)
- 16K x 1 Bit Organization
- 35, 45, 55 nsec Access Times
- Fully TTL Compatible
- Separate Data Input & Output
- Three-state Output
- Single +5V ± 10% Operation
- Power Down Function
- Pin Compatible with IMS1400M
- Standard Military Drawing version available
- 20-Pin, 300-mil DIP & LCC (JEDEC Std.)
- Battery Backup Operation - 2V Data Retention (L version only)

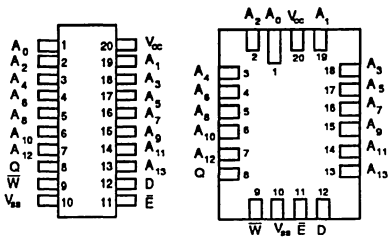
DESCRIPTION

The INMOS IMS1403M is a high speed 16K x 1 CMOS static RAM processed in full compliance to MIL-STD-883C. The IMS1403M provides maximum density and performance enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1403M features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1403M provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

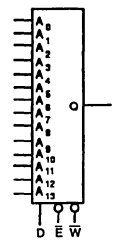
The IMS1403LM is a low power version offering battery backup data retention operating from a 2 volt supply.

PIN CONFIGURATION

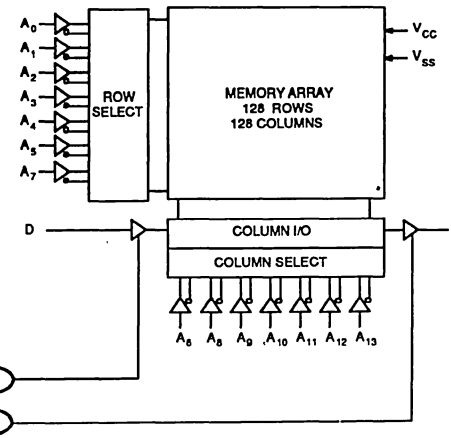


DIP CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{13}	ADDRESS INPUTS	Q	DATA OUTPUT
$\overline{W}$	WRITE ENABLE	V_{CC}	POWER
$\overline{E}$	CHIP ENABLE	V_{SS}	GROUND
D	DATA INPUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS}.....-2.0 to 7.0V
Voltage on Q.....-1.0 to (Vcc+.5)V
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One Second Duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	-55	25	125	°C	400 linear ft/min air flow

* V_{IL} Min = -3.0V for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS ($-55°C \le T_A \le 125°C$) ($V_{CC} = 5.0V \pm 10\%$) [a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		75	mA	$t_{AVAV} = t_{AVAV}$ (min)
I_{CC2}	V_{CC} Power Supply Current (Standby, Stable TTL Input Levels)		15	mA	$\bar{E} \ge V_{IH}$ All other inputs at $V_{IN} \le V_{IL}$ or $\ge V_{IH}$
I_{CC3}	V_{CC} Power Supply Current (Standby, Stable CMOS Input Levels)		5	mA	$\bar{E} \ge (V_{CC} - 0.2)$ All other inputs at $V_{IN} \le 0.2$ or $\ge (V_{CC} - 0.2V)$
I_{CC4}	V_{CC} Power Supply Current (Standby, Cycling CMOS Input Levels)		10	mA	$\bar{E} \ge (V_{CC} - 0.2)$ Inputs cycling at $V_{IN} \le 0.2$ or $\ge (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current (Any Input)		±5	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		±10	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 16mA

Note a: I_{CC} is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels.....V_{SS} to 3V
Input Rise and Fall Times.....5ns
Input and Output Timing Reference Levels.....1.5V
Output Load.....See Figure 1

CAPACITANCE[b] ($T_A = 25°C$, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	4	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

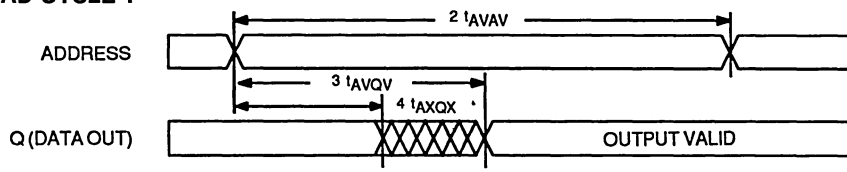
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \le T_A \le 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[g]

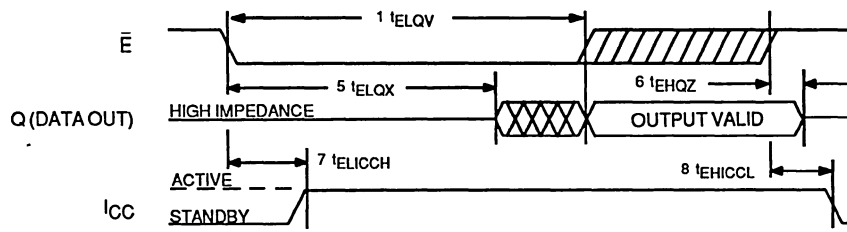
NO.	SYMBOL		PARAMETER	IMS1403M-35		IMS1403M-45		IMS1403M-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		35		45		55	ns	
2	t_{AVAV}	t_{RC}	Read CycleTime	35		40		50		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		35		40		50	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		5		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	j
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive	0	20	0	20	0	25	ns	f, j
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
8	t_{EHICCL}	t_{PD}	Chip Enable to Power Down		30		30		30	ns	j
		t_T	Input Rise and Fall Times		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c, d]



READ CYCLE 2[c]



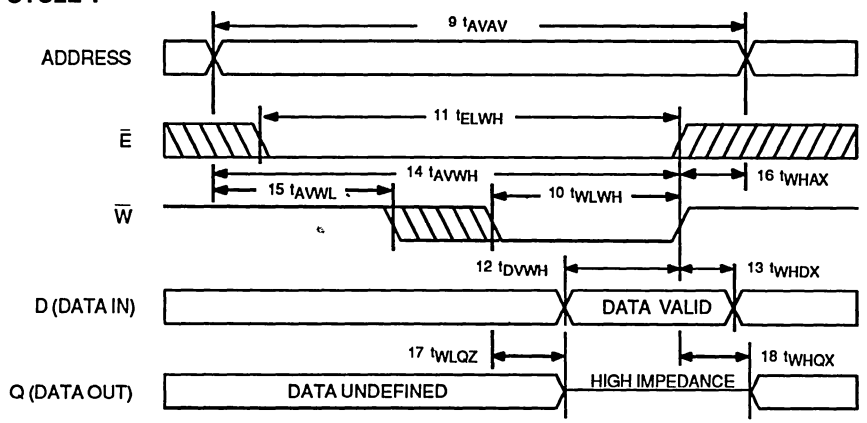
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \le T_A \le 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	IMS1403M-35		IMS1403M-45		IMS1403M-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
9	t_{AVAV}	t_{WC}	Write Cycle Time	30		40		50		ns	
10	t_{WLWH}	t_{WP}	Write Pulse Width	20		20		25		ns	
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write	30		35		45		ns	
12	t_{DVWH}	t_{DW}	Data Set-up to End of Write	15		15		20		ns	
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
14	t_{AVWH}	t_{AW}	Address Set-up to End of Write	30		35		45		ns	
15	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	20	0	25	ns	f, j
18	t_{WHQX}	t_{OW}	Output Active After End of Write	0		0		0			i, j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\ge V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



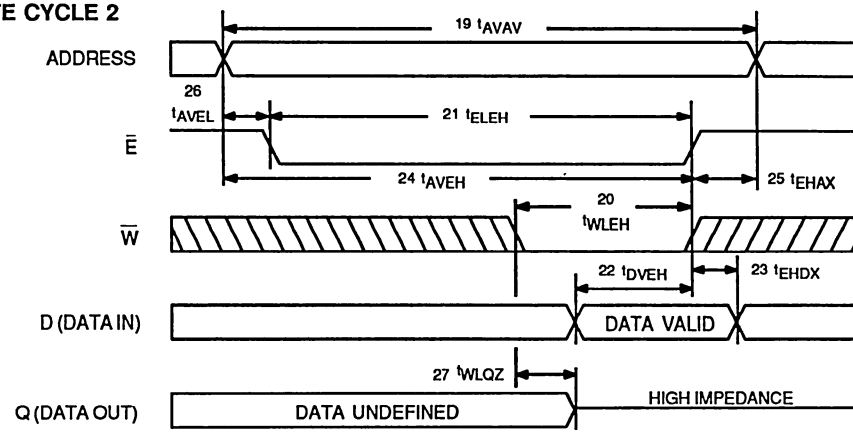
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \le T_A \le 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED [g, h]

NO.	SYMBOL		PARAMETER	IMS1403M-35		IMS1403M-45		IMS1403M-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	30		40		50		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	20		20		25		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	30		35		45		ns	
22	t_{DVEH}	t_{DW}	Data Set-up to End of Write	15		15		20		ns	
23	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
24	t_{AVEH}	t_{AW}	Address Set-up to End of Write	30		35		45		ns	
25	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
26	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	20	0	25	ns	f, j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\ge V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1403M has two control inputs, Chip Enable (/E) and Write Enable (/W), 14 address inputs (A0 -A13), a Data In (D) and a Data Out (Q). The /E input controls device selection as well as active and standby modes. With /E low, the device is selected and the14 address inputs are decoded to select one bit out of 16K bits. Read and Write operations on the memory cell are controlled by the /W input. With /E high, the device is deselected, the outputs are disabled and the power consumption is reduced to less than one-fourth of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as /W ≥ V_{IH} min with /E ≤ V_{IL} max. Read access time is measured from either /E going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while /E is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and long as /E remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by /E going low. As long as address is stable when /E goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when /E goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1403M is initiated by the latter of /E or /W to transition from a high to a low. In the case of /W falling last, the output buffer will be turned on t_{ELQX} after the falling edge of /E (just as in a read cycle). The output buffer is then turned off within t_{WLQZ} of the falling edge of /W. During this interval, it is possible to have bus contention between devices with D and Q connected together in a common I/O configuration. Contention can be avoided in a carefully designed system. During a write cycle, data on the input is written into the selected cells and the output is floating.

WRITE CYCLE 1 waveform shows a write cycle terminated by /W going high. Data set-up and hold times are referenced to the rising edge of /W. When /W goes high at the end of the cycle with /E active, the output of the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by /E going high. Data set-up and hold times are referenced to the rising edge of /E. With /E high the outputs remain in the high impedance state.

APPLICATION

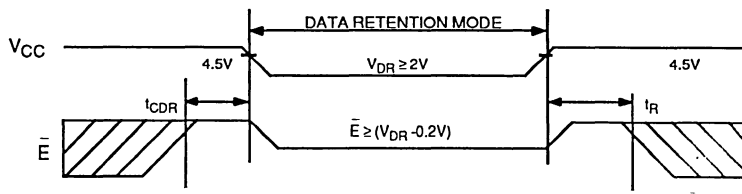
It is imperative when designing with any very high speed memory, such as the IMS1403M, that the fundamental rules in regard to memory board layout be followed to ensure proper system operation.

DATA RETENTION (L version only) (-55°C ≤ T_A ≤ 125°C)

SYMBOL	PARAMETER	MIN	TYP*	MAX	UNITS	NOTES
V_{DR}	Data Retention Voltage	2.0			volts	$V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$ $\bar{E} \geq (V_{CC} - 0.2V)$
I_{CCDR1}	Data Retention Current		3	400	µA	$V_{CC} = 3.0$ volts
I_{CCDR2}	Data Retention Current		2	250	µA	$V_{CC} = 2.0$ volts
t_{EHVCCL}	Deselect Time (t_{CDR})	0			ns	j, k
t_{VCCHEL}	Recovery Time (t_R)	t_{RC}			ns	j, k (t_{RC} = Read Cycle Time)

*Typical data retention parameters at 25°C.
Note j: Parameter guaranteed but not tested.
Note k: Supply recovery rate should not exceed 100mV per µS from V_{DR} to V_{CC} min.

LOW V_{CC} DATA RETENTION



POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1403M. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1403M have very high frequency components, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad, and be placed between each row of devices in the array (see drawing). A larger tantalum capacitor, with a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

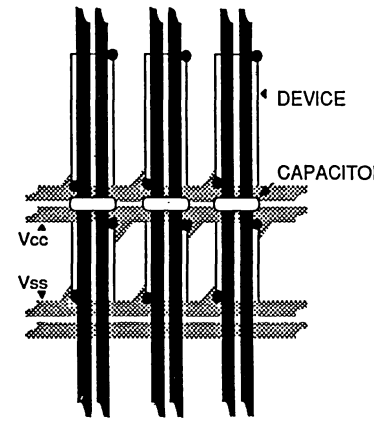
The ground grid of the memory array should extend to the TTL periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

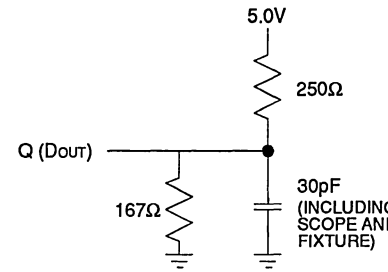
Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.



V_{CC}, V_{SS} GRID SHOWING
DECOUPLING CAPACITORS

Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

FIGURE 1. OUTPUT LOAD



TRUTH TABLE

$\overline{E}$	$\overline{W}$	Q	MODE
H	X	HI-Z	Standby (Isb)
L	H	Dout	Read
L	L	HI-Z	Write

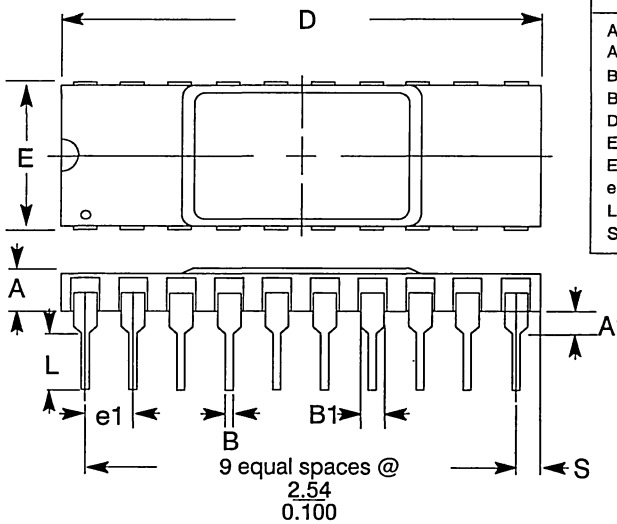
Standard Military Drawing version available, see SMD Reference Guide

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER	
			STANDARD	LOW POWER
IMS 1403M IMS 1403LM	35ns	CERAMIC DIP	IMS1403S-35M	IMS1403LS35M
	35ns	CERAMIC LCC	IMS1403N-35M	IMS1403LN35M
	45ns	CERAMIC DIP	IMS1403S-45M	IMS1403LS45M
	45ns	CERAMIC LCC	IMS1403N-45M	IMS1403LN45M
	55ns	CERAMIC DIP	IMS1403S-55M	IMS1403LS55M
	55ns	CERAMIC LCC	IMS1403N-55M	IMS1403LN55M

PACKAGING INFORMATION

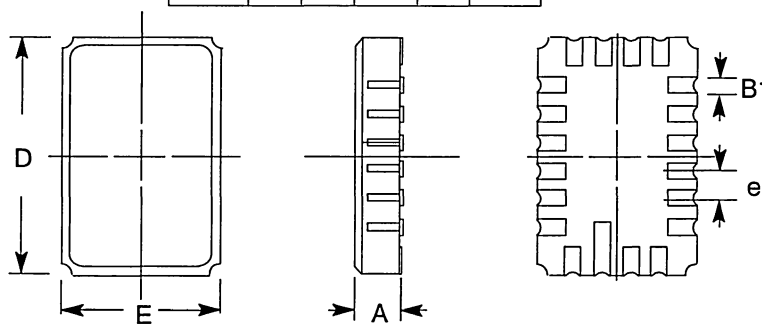
20 Pin Ceramic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.096	.012	2.438	.305
A1	.015		.381	
B	.018	.003	.457	.152
B1	.054	Typ	.137	Typ
D	1.00	.015	25.40	.381
E	.315	.010	8.001	.254
E1	.295	.015	7.493	.381
e1	.100	.010	2.54	.254
L	.125	min	3.175	min
S	.005		.127	

20 Pin Leadless Chip Carrier

Dim	Inches		mm		Notes
	Nom	Tol	Nom	Tol	
A	.071	.007	1.803	.178	
B1	.025	.003	.635	.076	
D	.425	.010	10.795	.254	
E	.290	.010	7.360	.254	
e1	.050	.005	1.270		



IMS1420M
High Performance 4Kx4 Static RAM MIL-STD-883C

inmos®

FEATURES

- Full Military Temperature Operating Range (-55° C to + 125° C)
- MIL-STD-883C Processing
- 4Kx4 Bit Organisation
- 55 and 70 nsec Access Times
- Fully TTL Compatible
- Common Data Input and Output
- Three-state Output
- Power Down Function
- Single +5V ± 10% Operation
- 20-Pin, 300-mil DIP (JEDEC Std.)
- 20-Pin Ceramic LCC (JEDEC Std.)

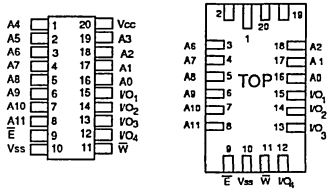
DESCRIPTION

The INMOS IMS1420M is a high performance 4Kx4 Static RAM processed in full compliance to MIL-STD-883C with access times of 55ns and 70ns and a maximum power consumption of 660mW. These characteristics are made possible by the combination of innovative circuit design and INMOS' proprietary NMOS technology.

The IMS1420M features fully static operation requiring no external clocks or timing strobes with equal access and cycle times. Additionally, the IMS1420M provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode reducing consumption to less than 165mW.

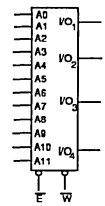
The IMS1420M is a high speed VLSI RAM intended for military applications which demand high performance and reliability.

PIN CONFIGURATION

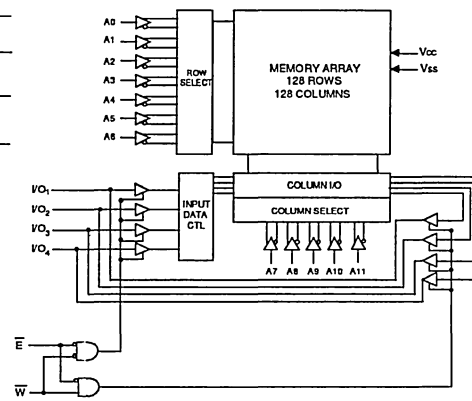


DIP CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{11}	ADDRESS INPUTS	Vcc POWER (+5V)
$\overline{W}$	WRITE ENABLE	Vss GROUND
$\overline{E}$	CHIP ENABLE	
I/O	DATA IN/OUT	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −3.5 to 7.0V
Temperature Under Bias. . . . . −65°C to 135°C
Storage Temperature (Ambient) . −65°C to 150°C
Power Dissipation. 1W
DC Output Current. 50mA

*Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect reliability

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.4		6.0	V	All Inputs
V_{IL}	Input Logic "0" Voltage	−2.0		0.8	V	All Inputs
T_A	Ambient Operating Temperature	−55		125	°C	400 Linear ft/min transverse air flow

DC ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current AC		120	mA	$t_C = t_C$ min
I_{CC2}	V_{CC} Power Supply Current (Standby)		30	mA	$\overline{E} \geq V_{IH}$ min
I_{IN}	Input Leakage Current (Any Input)	−10	10	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current	−50	50	µA	V_{CC} = max $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage $I_{OUT} = -4mA$	2.4		V	
V_{OL}	Output Logic "0" Voltage $I_{OUT} = 8mA$		0.4	V	

AC TEST CONDITIONS[a]

Input Pulse Levels	V_{SS} to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1 5V
Output Load	See Figure 1

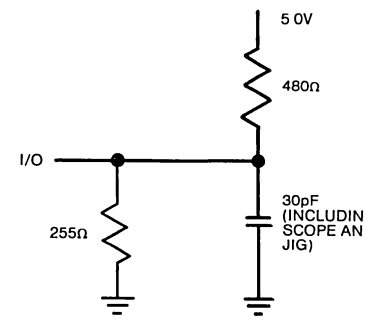
Note a Operation to specifications guaranteed 2ms after V_{CC} applied

CAPACITANCE[b] ($T_A = 25°C$, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNIT	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V
$C_{\overline{E}}$	$\overline{E}$ Capacitance	6	pF	ΔV = 0 to 3V

Note b This parameter is sampled and not 100% tested

FIGURE 1. OUTPUT LOAD



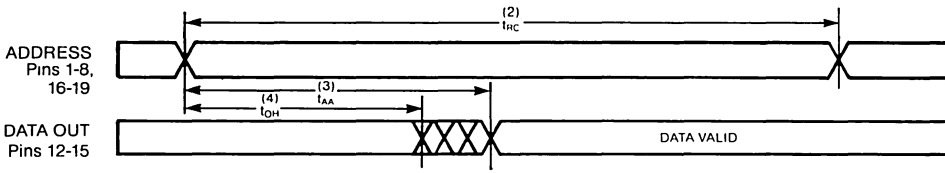
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE

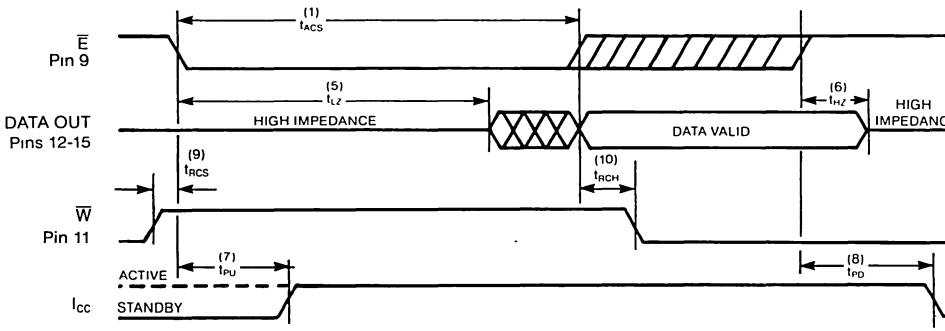
NO.	SYMBOL	PARAMETER	IMS1420M-55		IMS1420M-70		UNITS	NOTES
			MIN	MAX	MIN	MAX		
1	t_{ACS}	Chip Enable Access Time		55		70	ns	
2	t_{RC}	Read Cycle Time	55		70		ns	c
3	t_{AA}	Address Access Time		55		70	ns	d
4	t_{OH}	Output Hold After Address Change	3		3		ns	j
5	t_{LZ}	Chip Enable to Output Active	15		15		ns	j
6	t_{HZ}	Chip Disable to Output Disable		25		30	ns	f
7	t_{PU}	Chip Enable to Power Up	0		0		ns	j
8	t_{PD}	Chip Disable to Power Down	0	55	0	70	ns	j
9	t_{RCS}	Read Command Set-up Time	−5		−5		ns	
10	t_{RCH}	Read Command Hold Time	−5		−5		ns	
	t_T	Input Rise and Fall Times		50		50	ns	e

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1 [c, d]



READ CYCLE 2 [c]



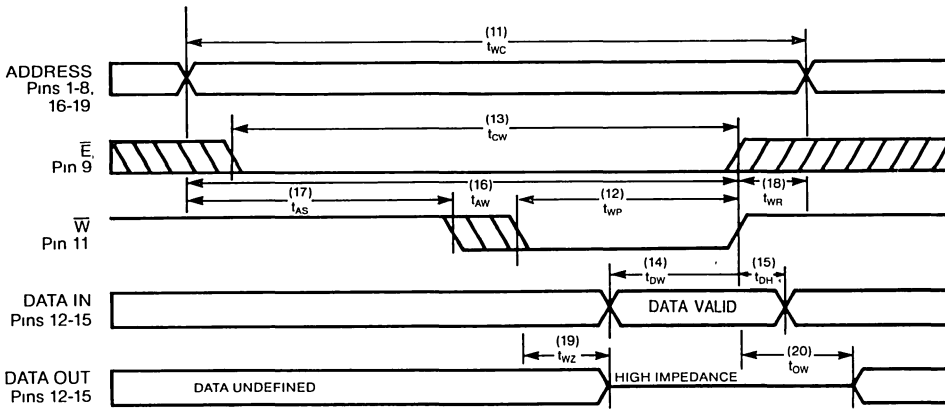
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[h]

NO.	SYMBOL	PARAMETER	IMS1420M-55		IMS1420M-70		UNITS	NOTES
			MIN	MAX	MIN	MAX		
11	t_{WC}	Write Cycle Time	55		70		ns	
12	t_{WP}	Write Pulse Width	45		65		ns	
13	t_{CW}	Chip Enable to End of Write	45		65		ns	
14	t_{DW}	Data Set-up to End of Write	25		30		ns	
15	t_{DH}	Data Hold After End of Write	3		5		ns	
16	t_{AW}	Address Set-up to End of Write	45		65		ns	
17	t_{AS}	Address Set-up to Beginning of Write	0		0		ns	
18	t_{WR}	Address Hold After End of Write	5		5		ns	
19	t_{WZ}	Write Enable to Output Disable	0	25	0	30	ns	f
20	t_{OW}	Output Active After End of Write	0		0		ns	g

Note f. Measured ± 200mV from steady state output voltage.
Note g. If $\overline{E}$ goes high with $\overline{W}$ low, Output remains in HIGH impedance state
Note h. $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.

WRITE CYCLE 1



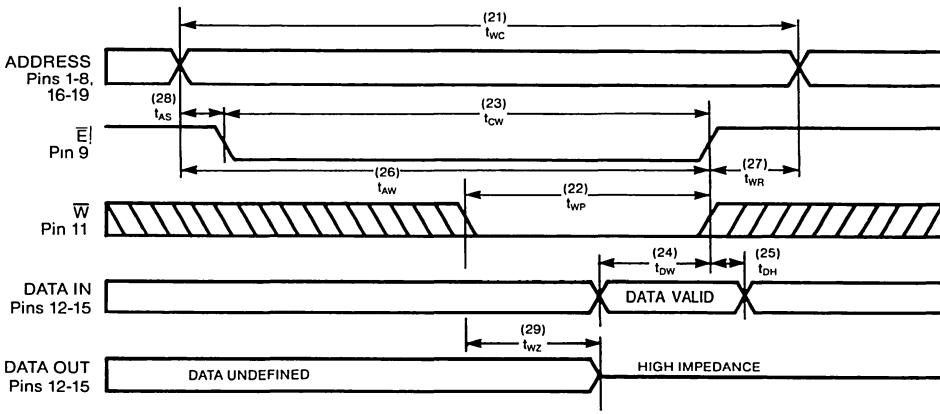
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[h]

NO.	SYMBOL	PARAMETER	IMS1420M-55		IMS1420M-70		UNITS	NOTES
			MIN	MAX	MIN	MAX		
21	t_{WC}	Write Cycle Time	55		70		ns	
22	t_{WP}	Write Pulse Width	45		65		ns	
23	t_{CW}	Chip Enable to End of Write	45		65		ns	
24	t_{DW}	Data Set-up to End of Write	25		30		ns	
25	t_{DH}	Data Hold After End of Write	5		5		ns	
26	t_{AW}	Address Set-up to End of Write	40		60		ns	
27	t_{WR}	Address Hold After End of Write	5		5		ns	
28	t_{AS}	Address Set-up to Beginning of Write	−5		−5		ns	
29	t_{WZ}	Write Enable to Output Disable	0	25	0	30	ns	f

Note f: Measured ± 200mV from steady state output voltage.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1420M has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), twelve address inputs, and four Data I/O lines.

When V_{CC} is first applied to pin 20, a circuit associated with the $\overline{E}$ input forces the device into the lower power standby mode regardless of the state of the $\overline{E}$ input. After V_{CC} is applied for 2ms the $\overline{E}$ input controls device selection as well as active and standby modes.

With $\overline{E}$ low, the device is selected and the twelve address inputs are decoded to select one 4-bit word out of 4096. READ and WRITE operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than one-third of the active mode power.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform on page 3 shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and the output remains valid for a minimum of 3ns. As long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform on page 3 shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable within 5ns after $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable access time. If address is not valid within 5ns after $\overline{E}$ goes low, the timing is as specified in the READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

A write cycle is initiated by the latter of $\overline{W}$ or $\overline{E}$ going low, and terminated by $\overline{W}$ (WRITE CYCLE 1) or $\overline{E}$ (WRITE CYCLE 2) going high. During the write cycle, data on the inputs is written into the selected cells, and the outputs are floating.

If a write cycle is initiated by $\overline{W}$ going low, the address must be stable for the WRITE CYCLE 1 set-up time. If a write cycle is initiated by $\overline{E}$ going low, the address need not be stable until a maximum of 5ns after $\overline{E}$ goes low. The address must be held stable for the entire write cycle. After $\overline{W}$ or $\overline{E}$ goes high to terminate the write cycle, addresses may change. If these address set-up and hold times are not met, contents of other cells may be altered in unpredictable ways.

WRITE CYCLE 1 waveform on page 4 shows a write cycle terminated by $\overline{W}$ going high. D_{IN} set-up and hold times are referenced to the rising edge of $\overline{W}$. With $\overline{W}$ high, the outputs become active. When $\overline{W}$ goes high at the end of a write cycle and the outputs of the memory go active, the data from the memory will be the same as the data just written into the memory. Thus, no data bus contention will occur.

WRITE CYCLE 2 waveform on page 5 shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, the outputs remain in the high impedance state.

APPLICATION

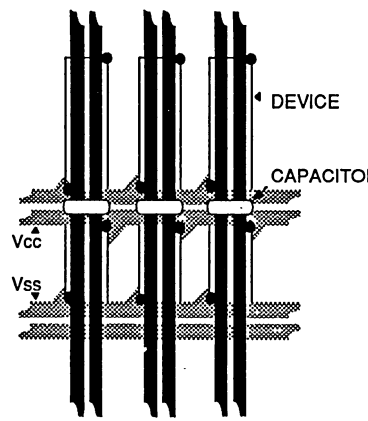
Fundamental rules in regard to memory board layout should be followed to ensure maximum benefit from the features offered by the IMS1420M Static RAM.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1420M. The impedance in the decoupling path from the power pin (20) through the decoupling capacitor, to the ground pin (10) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1420M are high frequency, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor acts as a low impedance power supply located near the memory device. The high frequency decoupling capacitor should have a value of 0.1μF, and be placed between the rows of memory devices in the array (see drawing). A larger tantalum capacitor with a value between 22μF and 47μF should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10Ω to 30Ω range will be required.

Proper power distribution techniques, including adequate use of decoupling capacitors, and proper termination of TTL drive outputs, are some of the most important, yet basic guidelines that need to be followed when designing and building a memory board. The guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment free of noise spikes and signal reflections.

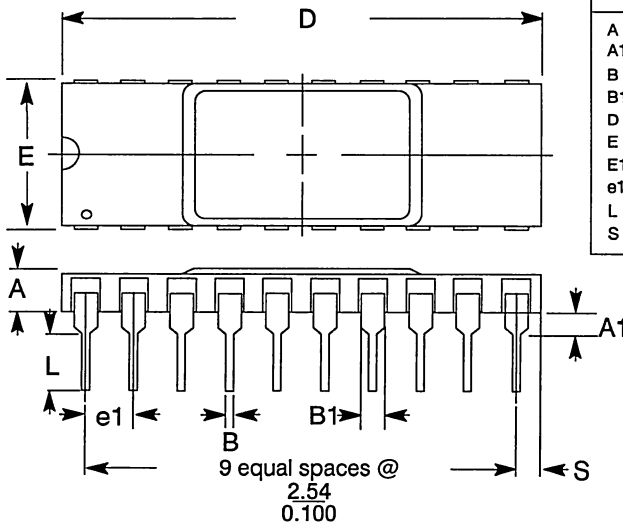
Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS 1420M	55ns	CERAMIC DIP	IMS1420S-55M
	55ns	CERAMIC LCC	IMS1420N-55M
	70ns	CERAMIC DIP	IMS1420S-70M
	70ns	CERAMIC LCC	IMS1420N-70M

PACKAGING INFORMATION

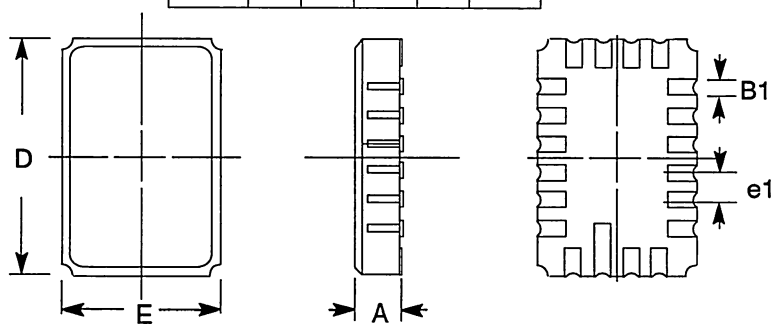
20 Pin Ceramic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.096	.012	2.438	.305
A1	.015		.381	
B	.018	.003	.457	.152
B1	.054	Typ	.137	Typ
D	1.00	.015	25.40	.381
E	.315	.010	8.001	.254
E1	.295	.015	7.493	.381
e1	.100	.010	2.54	.254
L	.125	min	3.175	min
S	.005		.127	

20 Pin Leadless Chip Carrier

Dim	Inches		mm		Notes
	Nom	Tol	Nom	Tol	
A	.071	.007	1.803	.178	
B1	.025	.003	.635	.076	
D	.425	.010	10.795	.254	
E	.290	.010	7.360	.254	
e1	.050	.005	1.270		



IMS1423M
CMOS High Performance 4K x 4 Static RAM MIL-STD-883C

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- Specifications guaranteed over full military temperature range (-55° C to + 125° C)
- 4K x 4 Bit Organization
- 35, 45, and 55 nsec Access Times
- Single +5V ± 10% Operation
- Power Down Function for Low Standby Power
- Fully TTL Compatible
- Common Data Input and Output
- Three-state Output
- Standard Military Drawing version available (refer to page B-7)
- 20-Pin DIP, LCC (JEDEC Std.) and FP
- Pin Compatible with IMS1420M

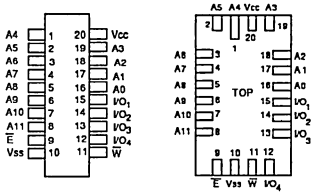
DESCRIPTION

The INMOS IMS1423M is a high speed 4K x 4 CMOS static RAM processed in full compliance to MIL-STD-883C. The IMS1423M provides maximum density and performance enhancements to existing 16K applications.

The IMS1423M features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1423M provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

The IMS1423M is a VLSI static RAM intended for military applications that demand high performance and superior reliability.

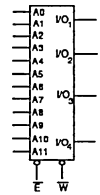
PIN CONFIGURATION



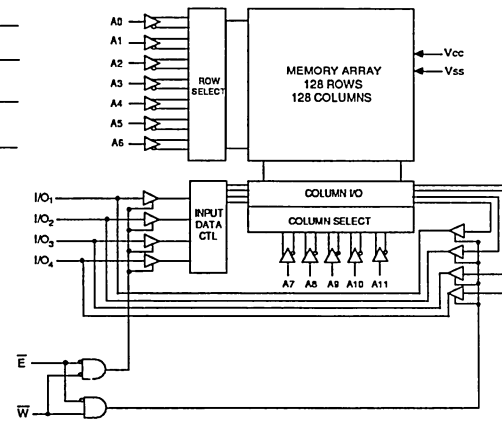
DIP and FLAT PACK

CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{11}	ADDRESS INPUTS	Vcc POWER (+5V)
$\overline{W}$	WRITE ENABLE	Vss GROUND
$\overline{E}$	CHIP ENABLE	
I/O	DATA IN/OUT	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on I/O.....-1.0 to (Vcc+0.5)V
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One output at a time, one second duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+0.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	-55	25	125	°C	400 linear ft/min air flow

*V_{IL} min = -3 volts for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		130 120 110	mA mA mA	t_{AVAV} = 35ns t_{AVAV} = 45ns t_{AVAV} = 55ns
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		20	mA	$\bar{E} \geq V_{IH}$. All other inputs at $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		8	mA	$\bar{E} \geq$ (Vcc - 0.2) . All other inputs at $V_{IN} \leq 0.2$ or $\geq$ (Vcc - 0.2V)
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		15 14 13	mA mA mA	t_{AVAV} = 35ns t_{AVAV} = 45ns t_{AVAV} = 55ns $\bar{E} \geq$ (Vcc - 0.2). all other iInputs cycling at $V_{IN} \leq 0.2$ or $\geq$ (Vcc - 0.2V)
I_{ILK}	Input Leakage Current (Any Input)		±10	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		±50	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OUT} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OUT} = 8mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels .....V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0MHZ)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V
C_E	/E Capacitance	6	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

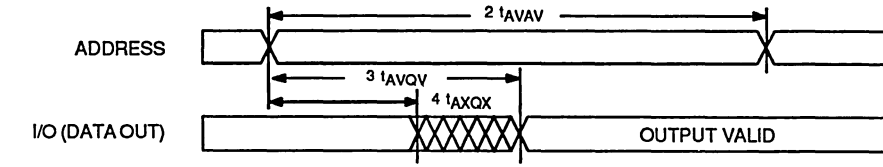
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \le T_A \le 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE [g]

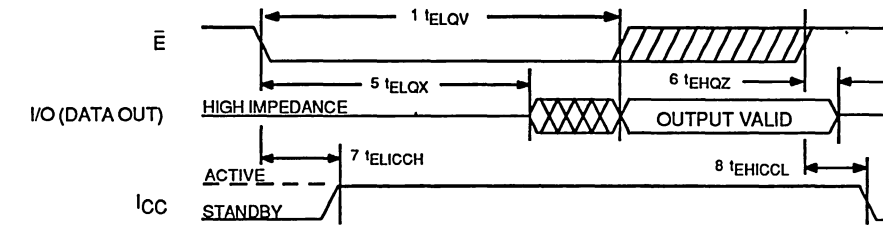
NO.	SYMBOL		PARAMETER	IMS1423M-35		IMS1423M-45		IMS1423M-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		35		45		55	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	35		45		55		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		35		45		55	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	3		3		3		ns	j
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive	0	20	0	20	0	20	ns	f, j
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
8	t_{EHICCL}	t_{PD}	Chip Enable to Power Down		35		45		55	ns	j
		t_T	Input Rise and Fall Times		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c, d]



READ CYCLE 2[c]



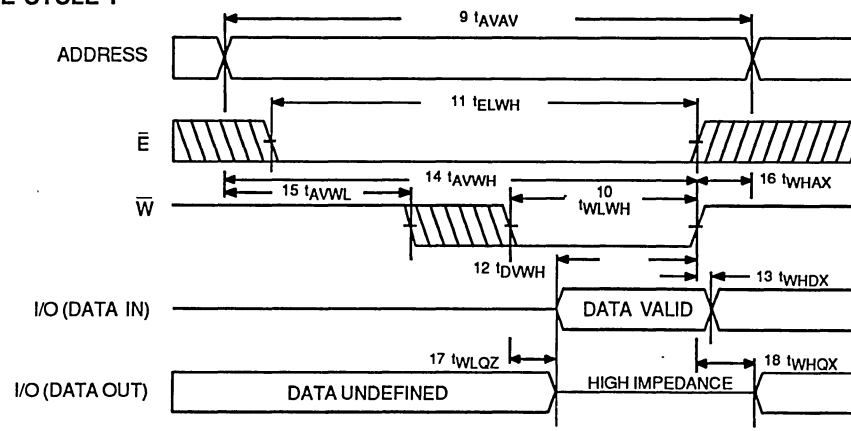
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \le T_A \le 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	IMS1403M-35		IMS1403M-45		IMS1403M-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
9	t_{AVAV}	t_{WC}	Write Cycle Time	35		45		55		ns	
10	t_{WLWH}	t_{WP}	Write Pulse Width	30		40		50		ns	
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write	30		40		50		ns	
12	t_{DVWH}	t_{DW}	Data Set-up to End of Write	15		20		25		ns	
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	3		3		3		ns	
14	t_{AVWH}	t_{AW}	Address Set-up to End of Write	30		40		50		ns	
15	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	5		5		5		ns	
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	15	0	20	0	25	ns	f, j
18	t_{WHQX}	t_{OW}	Output Active After End of Write	5		5		5			i, j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\ge V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



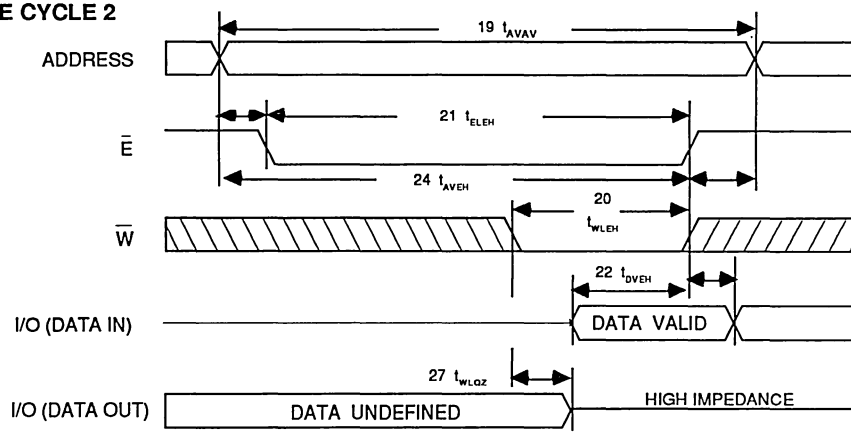
RECOMMENDED AC OPERATING CONDITIONS (-55°C ≤ TA ≤ 125°C) (Vcc = 5.0V ±10%)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

No	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1423M-35 MIN	IMS 1423M-35 MAX	IMS 1423M-45 MIN	IMS 1423M-45 MAX	IMS 1423M-55 MIN	IMS 1423M-55 MAX	UNITS	NOTES
19	tAVAV	tWC	Write Cycle Time	35		45		55		ns	
20	tWLEH	tWP	Write Pulse Width	30		40		50		ns	
21	tELEH	tCW	Chip Enable to End of Write	30		40		50		ns	
22	tDVEH	tDW	Data Setup to End of Write	15		20		25		ns	
23	tEHDX	tDH	Data Hold after End of Write	3		3		3		ns	
24	tAVEH	tAW	Address Setup to End of Write	30		40		50		ns	
25	tEHAX	tWR	Address Hold After End of Write	5		5		5		ns	
26	tAVEL	tAS	Address Setup to Beginning of Write	3		3		3		ns	
27	tWLQZ	tWZ	Write Enable to Output Disable	0	15	0	20	0	25	ns	f,j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1423M has two control inputs, Chip Enable (/E) and Write Enable (/W), 12 address inputs (A0 -A11), and four Data I/O lines. The /E input controls device selection as well as active and standby modes. With /E low, the device is selected and the 12 address inputs are decoded to select one four-bit word out of 4K words. Read and Write operations on the memory cell are controlled by the /W input. With /E high, the device is deselected, the outputs are disabled and the power consumption is reduced to less than one-fourth of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as /W $\geq V_{IH}$ min with /E $\leq V_{IL}$ max. Read access time is measured from either /E going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while /E is low. The outputs remain active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and long as /E remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by /E going low. As long as address is stable when /E goes low, valid data is at the outputs at the specified Chip Enable Access time. If address is not valid when /E goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1423M is initiated by the latter of /E or /W to transition from a high to a low. In the case of /W falling last, the output buffers will be turned on t_{ELQX} after the falling edge of /E (just as in a read cycle). The output buffers are then turned off within t_{WLQZ} of the falling edge of /W. During this interval, it is possible to have bus contention between devices with common I/O configurations. To avoid bus contention, input data should not be active until t_{WLQZ}.

WRITE CYCLE 1 waveform shows a write cycle terminated by /W going high. Data set-up and hold times are referenced to the rising edge of /W. When /W goes high at the end of the cycle with /E active, the outputs of the memory become active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by /E going high. Data set-up and hold times are referenced to the rising edge of /E. With /E high the outputs remain in the high impedance state.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1423M. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1423M have very high frequency components, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad, and be placed between each row of devices in the array (see drawing). A larger tantalum capacitor, with a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

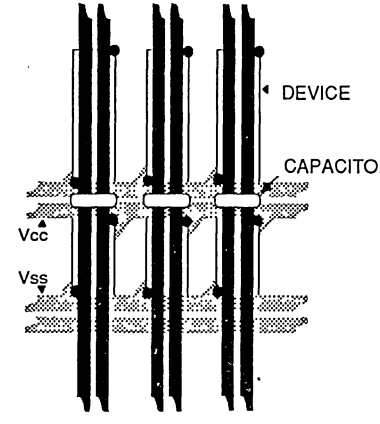
The ground grid of the memory array should extend to the TTL periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

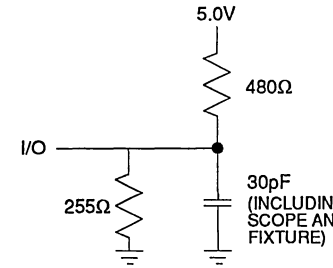
Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

FIGURE 1. OUTPUT LOAD



TRUTH TABLE

$\overline{E}$	$\overline{W}$	Q	MODE
H	X	HI-Z	Standby (Isb)
L	H	Dout	Read
L	L	Din	Write

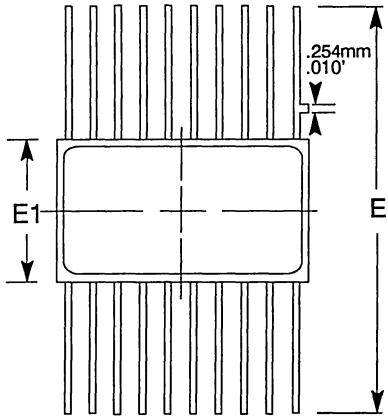
Standard Military Drawing version available, see SMD Reference Guide

ORDERING INFORMATION

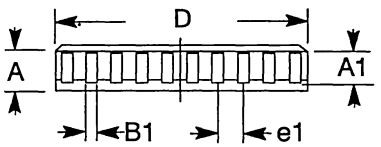
DEVICE	SPEED	PACKAGE	PART NUMBER
IMS 1423M	35ns	CERAMIC DIP	IMS1423S-35M
	35ns	CERAMIC LCC	IMS1423N-35M
	35ns	FLAT PACK	IMS1423Y-35M
	45ns	CERAMIC DIP	IMS1423S-45M
	45ns	CERAMIC LCC	IMS1423N-45M
	45ns	FLAT PACK	IMS1423Y-45M
	55ns	CERAMIC DIP	IMS1423S-55M
	55ns	CERAMIC LCC	IMS1423N-55M
	55ns	FLAT PACK	IMS1423Y-55M

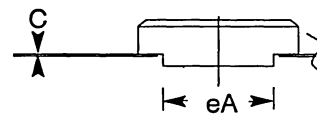
PACKAGING INFORMATION

20 Pin Flat Pack

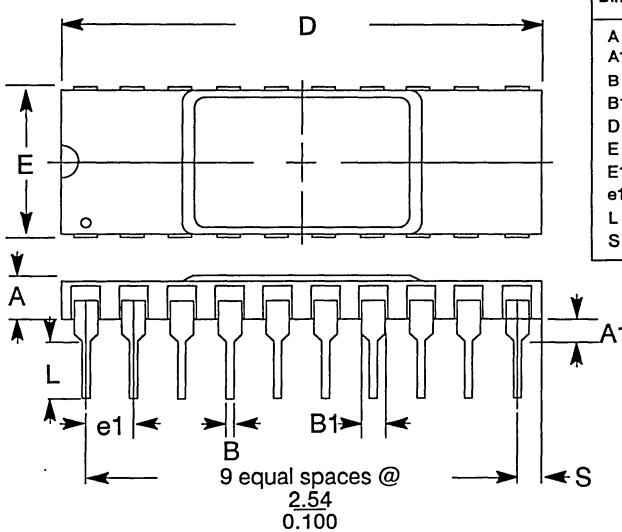


Dim	Inches		mm		Notes
	Nom	Tol	Nom	Tol	
A	.070	.007	1.178	.178	
A1	.050	.007	1.270	.178	
B1	.017	.002	.432	.051	
D	.480	.010	12.192	.254	
C	.005	.002	.127	.051	
E	.895	Ref	22.73	Ref	
e1	.050	.003	1.270	.076	
eA	.215	.006	5.461	.152	

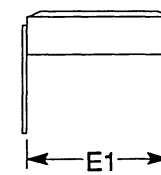




20 Pin Ceramic Dual-In-Line

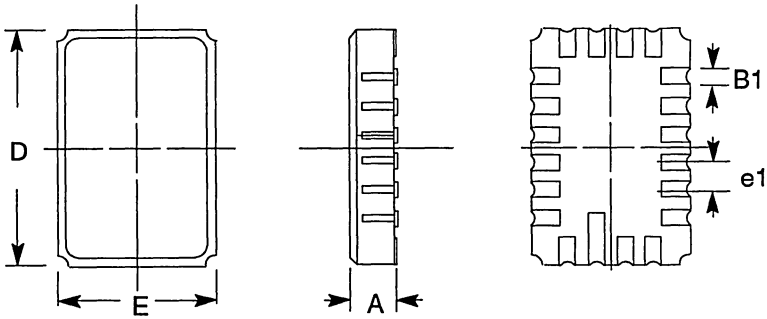


Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.096	.012	2.438	.305
A1	.015		.381	
B	.018	.003	.457	.152
B1	.054	Typ	.137	Typ
D	1.00	.015	25.40	.381
E	.315	.010	8.001	.254
E1	.295	.015	7.493	.381
e1	.100	.010	2.54	.254
L	.125	min	3.175	min
S	.005		.127	



20 Pin Leadless Chip Carrier

Dim	Inches		mm		Notes
	Nom	Tol	Nom	Tol	
A	.071	.007	1.803	.178	
B1	.025	.003	.635	.076	
D	.425	.010	10.795	.254	
E	.290	.010	7.360	.254	
e1	.050	.005	1.270		



IMS1600M
IMS1601LM
CMOS
High Performance
64K x 1 Static RAM
MIL-STD-883C

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- Full Military Temperature Operating Range (-55°C to +125°C)
- MIL-STD-883C Processing
- 45, 55, and 70 nsec Access Times
- Fully TTL Compatible
- Separate Data Input & Output
- Three-state Output
- Power Down Function
- Single +5V ± 10% Operation
- Standard Military Drawing version available
- 22-Pin, 300-mil DIP (JEDEC Std.)
- 22-Pin Ceramic LCC (JEDEC Std.)
- Battery Backup Operation - 2V Data Retention (L version only)

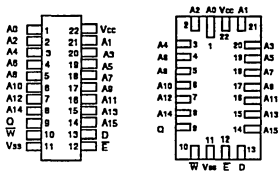
DESCRIPTION

The INMOS IMS1600M is a high performance 64Kx1 CMOS Static RAM processed in full compliance to MIL-STD-883C and guaranteed to operate over the full military temperature range. The IMS1600M provides maximum density and speed enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1600M features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1600M provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

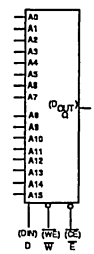
The IMS1601LM is a low power version offering battery backup data retention operating from a 2 volt supply.

PIN CONFIGURATION

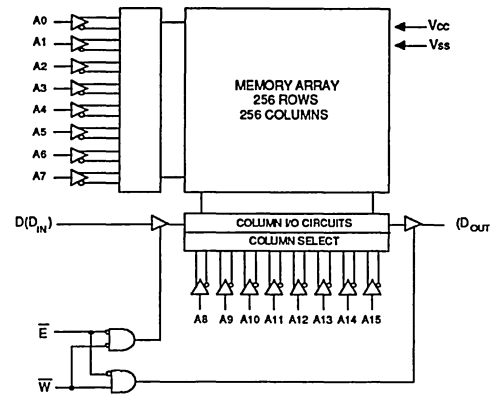


DIP CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{15}	ADDRESS INPUTS	Q	DATA OUTPUT
$\overline{W}$	WRITE ENABLE	Vcc	POWER (+5V)
$\overline{E}$	CHIP ENABLE	Vss	GROUND
D	DATA INPUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on Q.....-1.0 to (Vcc+0.5)
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One Second Duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+0.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	-55	25	125	°C	400 linear ft/min air flow

*V_{IL} min = -3 V for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS (-55°C ≤ T_A ≤ 125°C) (V_{CC} = 5.0V ± 10%)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		70	mA	t_{AVAV} = t_{AVAV}(min)
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		25	mA	$\overline{E}$ ≥ V_{IH} . All other inputs at V_{IN} ≤ V_{IL} or ≥ V_{IH}
	IMS1601L version		20		
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		14	mA	$\overline{E}$ ≥ (Vcc - 0.2) . All other inputs at V_{IN} ≤ 0.2 or ≥ (Vcc - 0.2V)
	IMS1601L version		9		
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		19	mA	$\overline{E}$ ≥ (Vcc - 0.2) . Inputs cycling at V_{IN} ≤ 0.2 or ≥ (Vcc - 0.2V)
	IMS1601L version		15		
I_{ILK}	Input Leakage Current (Any Input)		±5	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		±10	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 8mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels .....Vss to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE (T_A=25°C, f=1.0MHz)[b]

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

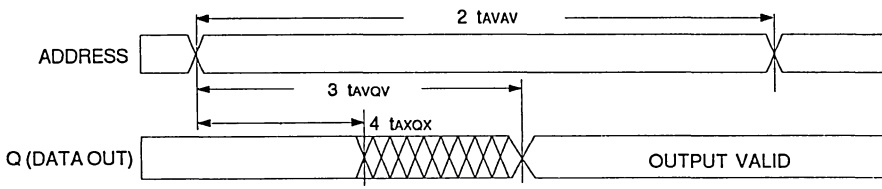
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE [g]

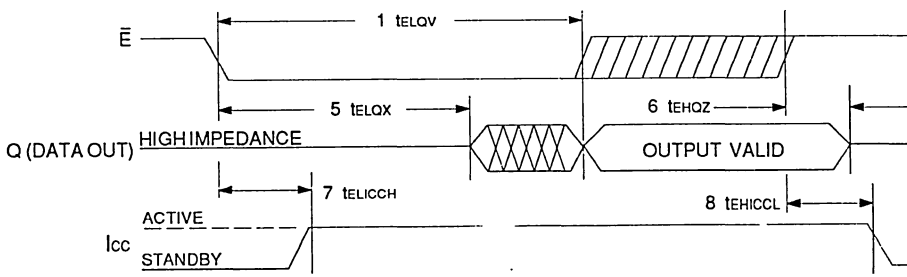
NO.	SYMBOL		PARAMETER	IMS1600M-45		IMS1600M-55		IMS1600M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	tELQV	tACS	Chip Enable Access Time		45		55		70	ns	
2	tAVAV	tRC	Read Cycle Time	45		55		70		ns	c
3	tAVQV	tAA	Address Access Time		45		55		70	ns	d
4	tAXQX	tOH	Output Hold After Address Change	5		5		5		ns	
5	tELQX	tLZ	Chip Enable to Output Active	5		5		5		ns	
6	tEHQZ	tHZ	Chip Disable to Output Inactive	0	25	0	30	0	30	ns	f, j
7	tELICCH	tPU	Chip Enable to Power Up	0		0		0		ns	j
8	tEHICCL	tPD	Chip Enable to Power Down		45		55		70	ns	j
		tT	Input Rise and Fall Times		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



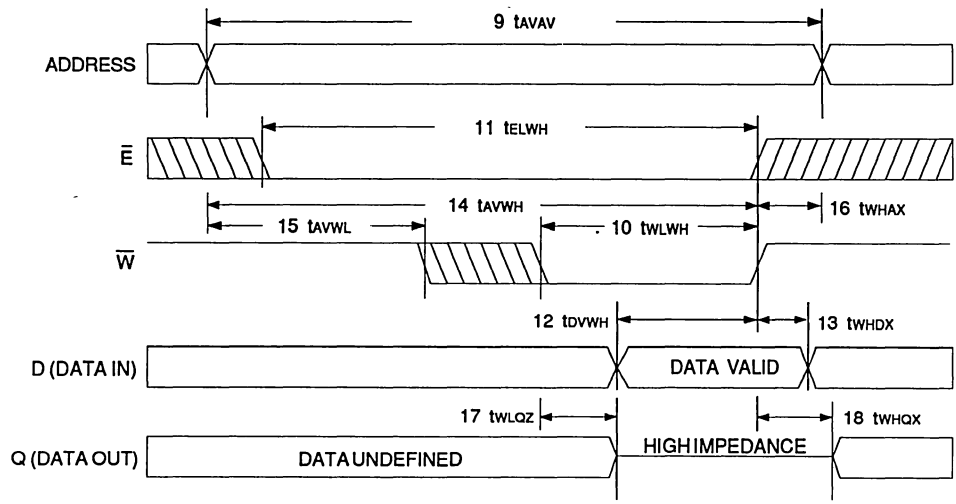
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	IMS1600M-45		IMS1600M-55		IMS1600M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
9	tAVAV	twc	Write Cycle Time	45		55		70		ns	
10	tWLWH	twp	Write Pulse Width	20		25		30		ns	
11	tELWH	tcw	Chip Enable to End of Write	20		30		35		ns	
12	tDVWH	tDW	Data Setup to End of Write	20		20		30		ns	
13	tWHDX	tDH	Data Hold after End of Write	0		5		5		ns	
14	tAVWH	taw	Address Setup to End of Write	27		32		37		ns	
15	tAVWL	tAS	Address Setup to Start of Write	7		7		7		ns	
16	tWHAX	twR	Address Hold after End of Write	5		5		5		ns	
17	tWLQZ	twz	Write Enable to Output Disable	0	20	0	25	0	30	ns	f, j
18	tWHQX	tow	Output Active after End of Write	0		0		0		ns	i, j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



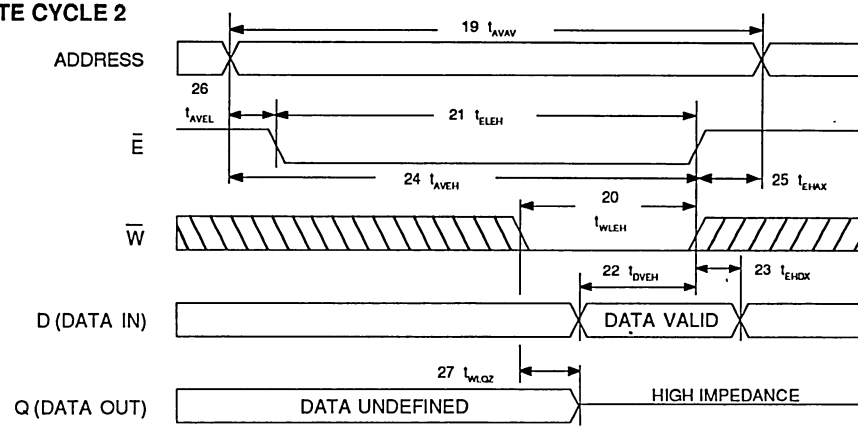
RECOMMENDED AC OPERATING CONDITIONS (-55°C ≤ T_A ≤ +125°C) (Vcc = 5.0V ±10%)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	IMS1600M-45		IMS1600M-55		IMS1600M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	45		55		70		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		30		ns	
22	t_{DVEH}	t_{DW}	Data Setup to End of Write	20		20		30		ns	
23	t_{EHDX}	t_{DH}	Data Hold after End of Write	5		5		5		ns	
24	t_{AVEH}	t_{AW}	Address Setup to End of Write	23		28		33		ns	
25	t_{EHAX}	t_{WR}	Address Hold after End of Write	5		5		5		ns	
26	t_{AVEL}	t_{AS}	Address Setup to Start of Write	3		3		3		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	25	0	30	ns	f, j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1600M has two control inputs, a Chip Enable (/E) and Write Enable (/W), 16 address inputs (A0 -A15), a data in (D) and a data out (Q).

The /E input controls device selection as well as active and standby modes. With /E low, the device is selected and the 16 address inputs are decoded to select one memory cell out of 65,536. Read and Write operations on the memory cell are controlled by the /W input. With /E high, the device is deselected, the output is disabled and the power consumption is reduced to less than one-third of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as /W $\geq$ V_{IH} min with /E $\leq$ V_{IL} max. Read access time is measured from either /E going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while /E is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and long as /E remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by /E going low. As long as address is stable when /E goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when /E goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1600M is initiated by the latter of /E or /W to transition from a high to a low. In the case of /W falling last, the output buffer will be turned on t_{ELQX} after the falling edge of /E (just as in a read cycle). The output buffer is then turned off within t_{WLQZ} of the falling edge of /W. During this interval it is possible to have bus contention between devices with D and Q connected together in a common I/O configuration. To aviod bus contention input data should not be active until t_{WLQZ}.

WRITE CYCLE 1 waveform shows a write cycle terminated by /W going high. Data set-up and hold times are referenced to the rising edge of /W. When /W goes high at the end of the cycle with /E active, the output of the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by /E going high. Data set-up and hold times are referenced to the rising edge of /E. With /E high the output remains in the high impedance state.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1600M. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Current transients associated with the operation of any high speed device have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad and be placed between each row of devices in the array. A larger tantalum capacitor of a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit area This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

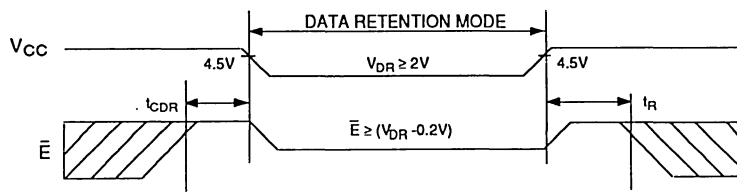
Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.

DATA RETENTION (L version only) ($-55°C \le T_A \le 125°C$)

SYMBOL	PARAMETER	MIN	TYP*	MAX	UNITS	NOTES
V_{DR}	Data Retention Voltage	2.0			volts	$V_{IN} \le 0.2V$ or $\ge (V_{CC}-0.2V)$ $\overline{E} \ge (V_{CC}-0.2V)$
I_{CCDR1}	Data Retention Current		8	1200	µA	V_{CC}= 3.0 volts
I_{CCDR2}	Data Retention Current		5	800	µA	V_{CC}= 2.0 volts
t_{EHVCCL}	Deselect Time (t_{CDR})	0			ns	j, k
t_{VCCHEL}	Recovery Time (t_R)	t_{RC}			ns	j, k (t_{RC}= Read Cycle Time)

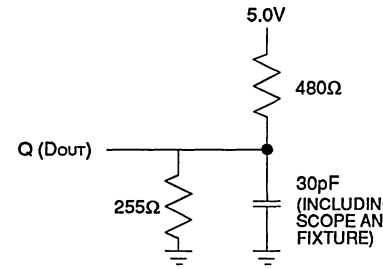
*Typical data retention parameters at 25°C.
Note j: Parameter guaranteed but not tested.
Note k: Supply recovery rate should not exceed 100mV per µS from V_{DR} to V_{CC} min.

LOW V_{CC} DATA RETENTION



Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

FIGURE 1. OUTPUT LOAD



TRUTH TABLE

$\overline{E}$	$\overline{W}$	Q	MODE
H	X	HI-Z	Standby (Isb)
L	H	Dout	Read
L	L	HI-Z	Write

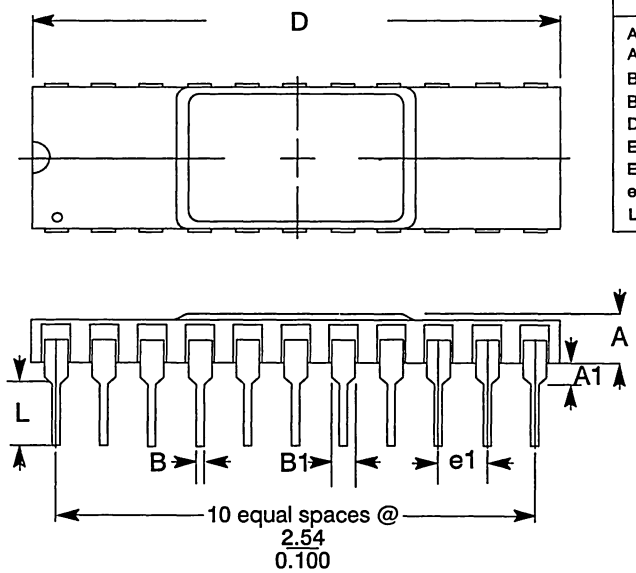
Standard Military Drawing version available, see SMD Reference Guide

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER	
			STANDARD	LOW POWER
IMS 1600M IMS1600LM	45ns	CERAMIC DIP	IMS1600S-45M	IMS1601LS45M
	45ns	CERAMIC LCC	IMS1600N-45M	IMS1601LN45M
	55ns	CERAMIC DIP	IMS1600S-55M	IMS1601LS55M
	55ns	CERAMIC LCC	IMS1600N-55M	IMS1601LN55M
	70ns	CERAMIC DIP	IMS1600S-70M	IMS1601LS70M
	70ns	CERAMIC LCC	IMS1600N-70M	IMS1601LN70M

PACKAGING INFORMATION

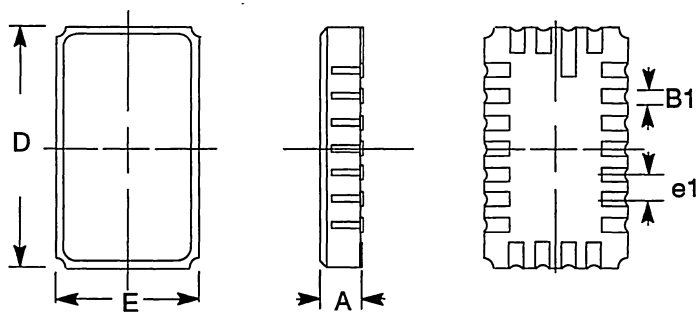
22 Pin Ceramic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.118	.010	2.997	.254
A1	.035	.015	.889	.381
B	.018	.003	.457	.152
B1	.060	Typ	1.524	Max
D	1.10	.013	27.94	.330
E	.315	.010	8.001	.254
E1	.295	.015	7.493	.381
e1	.100	.010	2.54	.254
L	.145	.020	3.683	.508

22 Pin Leadless Chip Carrier

Dim	Inches		mm		Notes
	Nom	Tol	Nom	Tol	
A	.071	.007	1.803	.178	
B1	.025	.003	.635	.076	
D	.490	.006	13.446	.152	
E	.290	.006	7.366	.152	
e1	.050		1.270		



IMS1620M
IMS1620LM
CMOS
High Performance
16K x 4 Static RAM
MIL-STD-883C

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- Full Military Temperature Operating Range (-55°C to + 125°C)
- MIL-STD-883C Processing
- 16K x 4 Bit Organization
- 45, 55 and 70 nsec Access Times
- Fully TTL Compatible
- Common Data Input & Output
- Three-state Output
- Power Down Function
- Single +5V ± 10% Operation
- 22-Pin, 300-mil DIP (JEDEC Std.)
- 22-Pin Ceramic LCC (JEDEC Std.)
- Battery Backup Operation - 2V Data Retention (L version only)

DESCRIPTION

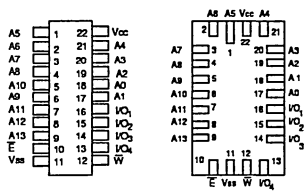
The INMOS IMS1620M is a high performance 16Kx4 CMOS Static RAM processed in full compliance to MIL-STD-883C and guaranteed to operate over the full military temperature range. The IMS1620M provides maximum density and speed enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1620M features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1620M provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

The IMS1620LM is a low power version offering battery backup data retention operating from a 2 volt supply.

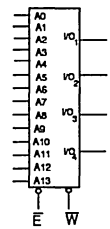
The IMS1624M is the functional equivalent of the IMS1620M with an added Output Enable function.

PIN CONFIGURATION

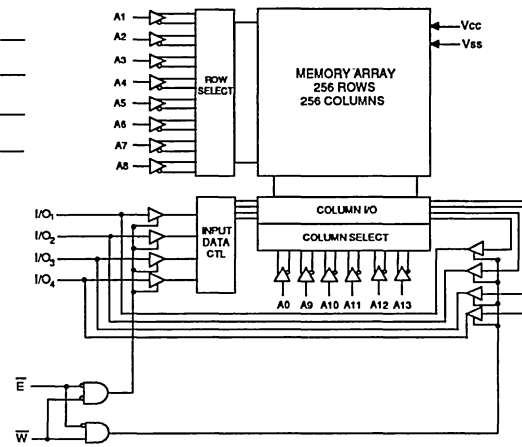


DIP CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{13}	ADDRESS INPUTS	I/O	DATA IN/OUT
$\overline{W}$	WRITE ENABLE	Vcc	POWER
$\overline{E}$	CHIP ENABLE	Vss	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on I/O Pins (13-16).....-1.0 to (Vcc+0.5)
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

(One output at a time, one second duration)

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0	25	70	°C	400 linear ft/min air flow

*V_{IL} min = -3 volts for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		100	mA	t_{AVAV} = t_{AVAV} (min)
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		30	mA	$\overline{E} \geq V_{IH}$. All other inputs at $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$
	IMS1620L version		20		
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		19	mA	$\overline{E} \geq$ (Vcc - 0.2). All other inputs at $V_{IN} \leq 0.2$ or $\geq$ (Vcc - 0.2V)
	IMS1620L version		8		
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		20	mA	$\overline{E} \geq$ (Vcc - 0.2). Inputs cycling at $V_{IN} \leq 0.2$ or $\geq$ (Vcc - 0.2V)
	IMS1620L version		8		
I_{ILK}	Input Leakage Current (Any Input)		±5	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		±10	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 8mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels .....V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

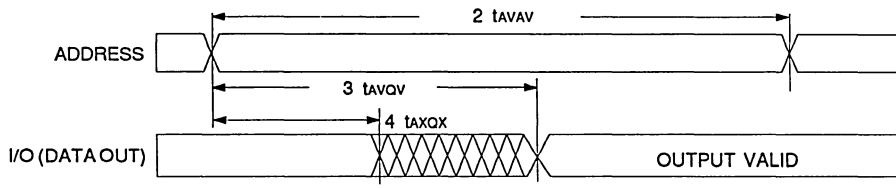
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[g]

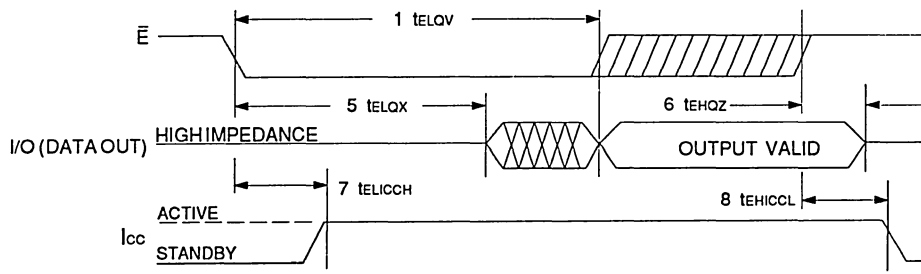
NO.	SYMBOL		PARAMETER	IMS1620M-45		IMS1620M-55		IMS1620M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	tELQV	tACS	Chip Enable Access Time		45		55		70	ns	
2	tAVAV	tRC	Read Cycle Time	45		55		70		ns	c
3	tAVQV	tAA	Address Access Time		45		55		70	ns	d
4	tAXQX	tOH	Output Hold After Address Change	5		5		5		ns	
5	tELQX	tLZ	Chip Enable to Output Active	5		5		5		ns	j
6	tEHQZ	tHZ	Chip Disable to Output Inactive	0	15	0	20	0	25	ns	f, j
7	tELICCH	tPU	Chip Enable to Power Up	0		0		0		ns	j
8	tEHICCL	tPD	Chip Enable to Power Down		45		55		70	ns	j
		tT	Input Rise and Fall Times		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



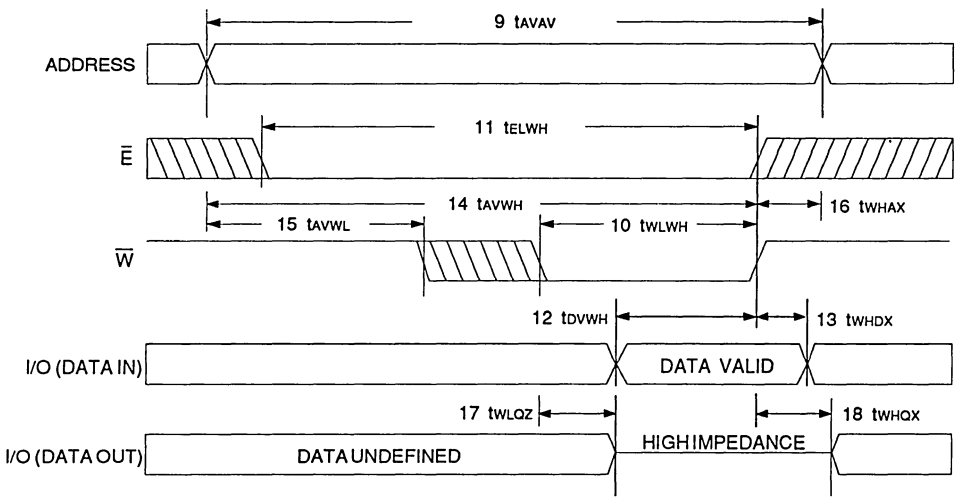
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq +125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g,h]

NO.	SYMBOL		PARAMETER	IMS1620M-45		IMS1620M-55		IMS1620M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
9	tAVAV	twc	Write Cycle Time	40		50		60		ns	
10	tWLWH	twp	Write Pulse Width	30		40		50		ns	
11	tELWH	tcw	Chip Enable to End of Write	30		40		50		ns	
12	tDVWH	tDW	Data Setup to End of Write	20		25		30		ns	
13	tWHDX	tDH	Data Hold after End of Write	0		0		0		ns	
14	tAVWH	taw	Address Setup to End of Write	30		40		50		ns	
15	tAVWL	tAS	Address Setup to Start of Write	0		0		0		ns	
16	tWHAX	twR	Address Hold after End of Write	0		0		0		ns	
17	tWLQZ	twz	Write Enable to Output Disable	0	15	0	20	0	25	ns	f, j
18	tWHQX	tow	Output Active after End of Write	5		5		5		ns	i, j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



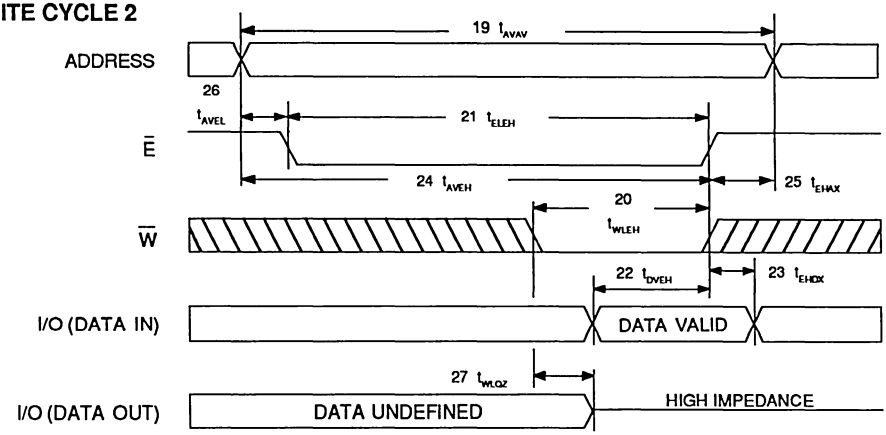
RECOMMENDED AC OPERATING CONDITIONS (-55°C ≤ Ta ≤ 125°C) (Vcc = 5.0V ±10%)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	IMS1620M-45		IMS1620M-55		IMS1620M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	40		50		60		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	30		40		50		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	30		40		50		ns	
22	t_{DVEH}	t_{DW}	Data Setup to End of Write	20		25		30		ns	
23	t_{EHDX}	t_{DH}	Data Hold after End of Write	0		0		0		ns	
24	t_{AVEH}	t_{AW}	Address Setup to End of Write	30		40		50		ns	
25	t_{EHAX}	t_{WR}	Address Hold after End of Write	0		0		0		ns	
26	t_{AVEL}	t_{AS}	Address Setup to Start of Write	0		0		0		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	15	0	20	0	25	ns	f, j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1620M has two control inputs, a Chip Enable (/E) and Write Enable (/W), 14 address inputs (A0 -A13), and four Data I/O pins.

The /E input controls device selection as well as active and standby modes. With /E low, the device is selected and the 14 address inputs are decoded to select one 4-bit word out of 16,384. Read and Write operations on the memory cells are controlled by the /W input. With /E high, the device is deselected, the outputs are disabled and the power consumption is reduced to less than one-third of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as /W $\geq$ V_{IH} min with /E $\leq$ V_{IL} max. Read access time is measured from either /E going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while /E is low. The outputs remain active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and long as /E remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by /E going low. As long as address is stable when /E goes low, valid data is at the outputs at the specified Chip Enable Access time. If address is not valid when /E goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1620M is initiated by the latter of /E or /W to transition from a high to a low. In the case of /W falling last, the output buffers are turned on t_{ELQX} after the falling edge of /E (just as in a read cycle). The output buffers are then turned off within t_{WLQZ} of the falling edge of /W. During this interval it is possible to have bus contention between devices with common I/O configurations. Therefore input data should not be active until t_{WLQZ} to aviod bus contention.

WRITE CYCLE 1 waveform shows a write cycle terminated by /W going high. Data set-up and hold times are referenced to the rising edge of /W. When /W goes high at the end of the cycle with /E active, the output of the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by /E going high. Data set-up and hold times are referenced to the rising edge of /E. With /E high the outputs remain in the high impedance state.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1620M. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Current transients associated with the operation of any high speed device have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad and be placed between each row of devices in the array. A larger tantalum capacitor of a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit area This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

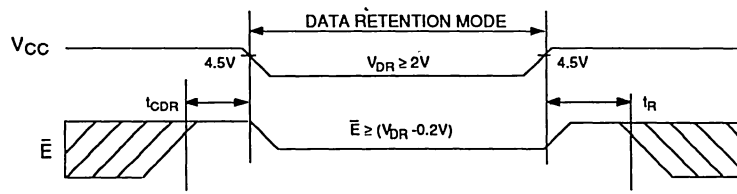
Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.

DATA RETENTION (L version only) ($-55°C \le T_A \le 125°C$)

SYMBOL	PARAMETER	MIN	TYP*	MAX	UNITS	NOTES
V_{DR}	Data Retention Voltage	2.0			volts	$V_{IN} \le 0.2V$ or $\ge (V_{CC}-0.2V)$ $\overline{E} \ge (V_{CC}-0.2V)$
I_{CCDR1}	Data Retention Current		15	1200	µA	V_{CC}= 3.0 volts
I_{CCDR2}	Data Retention Current		10	800	µA	V_{CC}= 2.0 volts
t_{EHVCCL}	Deselect Time (t_{CDR})	0			ns	j, k
t_{VCCHEL}	Recovery Time (t_R)	t_{RC}			ns	j, k (t_{RC}= Read Cycle Time)

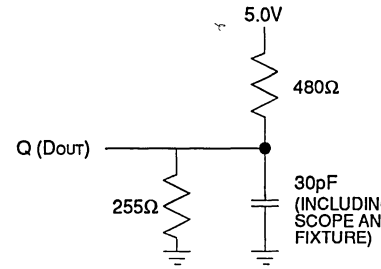
*Typical data retention parameters at 25°C.
Note j: Parameter guaranteed but not tested.
Note k: Supply recovery rate should not exceed 100mV per µS from V_{DR} to V_{CC} min.

LOW V_{CC} DATA RETENTION



Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

FIGURE 1. OUTPUT LOAD



TRUTH TABLE

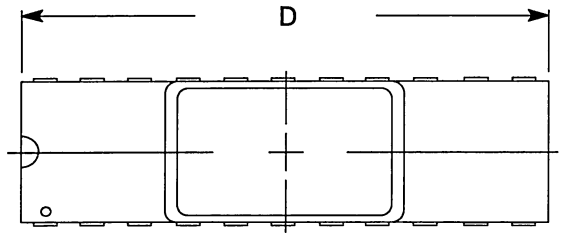
$\overline{E}$	$\overline{W}$	Q	MODE
H	X	HI-Z	Standby (Isb)
L	H	Dout	Read
L	L	HI-Z	Write

ORDERING INFORMATION

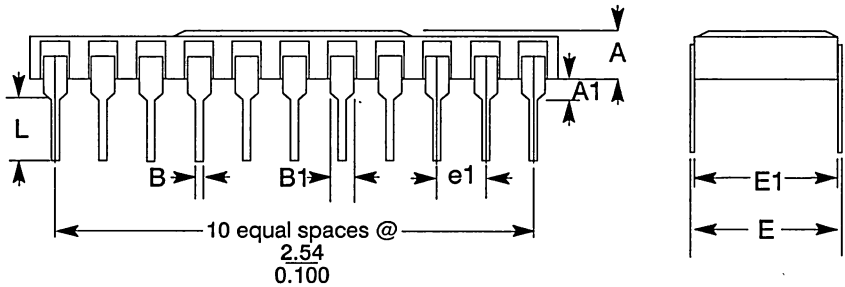
DEVICE	SPEED	PACKAGE	PART NUMBER	
			STANDARD	LOW POWER
IMS 1620M IMS1620LM	45ns	CERAMIC DIP	IMS1620S-45M	IMS1620LS45M
	45ns	CERAMIC LCC	IMS1620N-45M	IMS1620LN45M
	55ns	CERAMIC DIP	IMS1620S-55M	IMS1620LS55M
	55ns	CERAMIC LCC	IMS1620N-55M	IMS1620LN55M
	70ns	CERAMIC DIP	IMS1620S-70M	IMS1620LS70M
	70ns	CERAMIC LCC	IMS1620N-70M	IMS1620LN70M

PACKAGING INFORMATION

22 Pin Ceramic Dual-In-Line

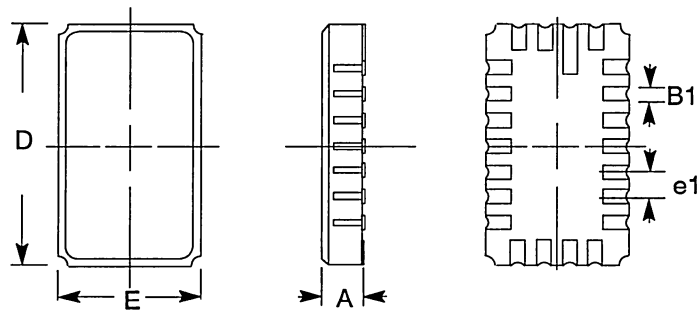


Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.118	.010	2.997	.254
A1	.035	.015	.889	.381
B	.018	.003	.457	.152
B1	.060	Typ	1.524	Max
D	1.10	.013	27.94	.330
E	.315	.010	8.001	.254
E1	.295	.015	7.493	.381
e1	.100	.010	2.54	.254
L	.145	.020	3.683	.508



22 Pin Leadless Chip Carrier

Dim	Inches		mm		Notes
	Nom	Tol	Nom	Tol	
A	.071	.007	1.803	.178	
B1	.025	.003	.635	.076	
D	.490	.006	13.446	.152	
E	.290	.006	7.366	.152	
e1	.050		1.270		



IMS1624M
IMS1624LM
CMOS
High Performance
16K x 4 Static RAM
MIL-STD-883C

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- Full Military Temperature Operating Range (-55°C to +125°C)
- MIL-STD-883C Processing
- 16K x 4 Bit Organization with Output Enable
- 45, 55, and 70 nsec Access Times
- Fully TTL Compatible
- Common Data Input & Output
- Three-state Output
- Power Down Function
- Single +5V ± 10% Operation
- 24-Pin, 300-mil DIP (JEDEC Std.)
- 28-Pin, 300-mil LCC (JEDEC Std.)
- Standard Military Drawing version available
- Battery Backup Operation - 2V Data Retention (L version only)

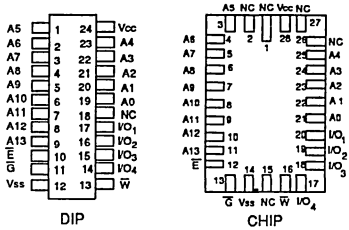
DESCRIPTION

The INMOS IMS1624M is a high performance 16Kx4 CMOS Static RAM processed in full compliance to MIL-STD-883C and guaranteed to operate over the full military temperature range. The IMS1624M provides maximum density and speed enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1624M features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The IMS1624M provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode. The IMS1624M also includes an Output Enable (/G) for fast access to data and enhanced bus contention control.

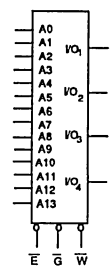
The IMS1624LM is a low power version offering battery backup data retention operating from a 2 volt supply.

PIN CONFIGURATION

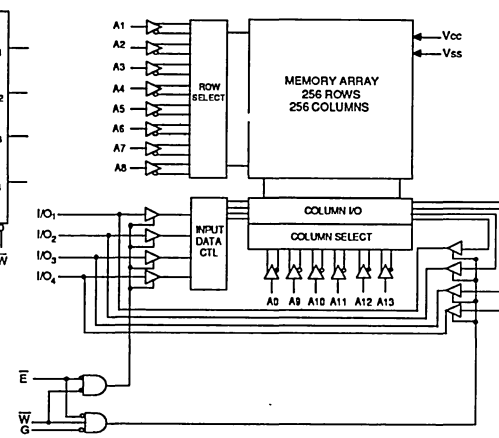


DIP CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{13}	ADDRESS INPUTS	Vcc	POWER (+5V)
$\overline{W}$	WRITE ENABLE	Vss	GROUND
I/O	DATA IN/OUT		
$\overline{E}$	CHIP ENABLE		
$\overline{G}$	OUTPUT ENABLE		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on I/O Pins (13-16).....-1.0 to (Vcc+0.5)
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

(One output at a time, one second duration)

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+0.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	55	25	125	°C	400 linear ft/min air flow

*V_{IL} min = -3 volts for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS (-55°C ≤ T_A ≤ +125°C) (V_{CC} = 5.0V ± 10%)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		100	mA	tAVAV = tAVAV (min)
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		30	mA	$\overline{E}$ ≥ V_{IH} . All other inputs at V_{IN} ≤ V_{IL} or ≥ V_{IH}
	IMS1624L version		20		
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		19	mA	$\overline{E}$ ≥ (Vcc - 0.2) . All other inputs at V_{IN} ≤ 0.2 or ≥ (Vcc - 0.2V)
	IMS1624L version		8		
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		20	mA	$\overline{E}$ ≥ (Vcc - 0.2) . Inputs cycling at V_{IN} ≤ 0.2 or ≥ (Vcc - 0.2V)
	IMS1624L version		8		
I_{ILK}	Input Leakage Current (Any Input)		± 5	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		± 10	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 8mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels .....V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0 MHZ)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

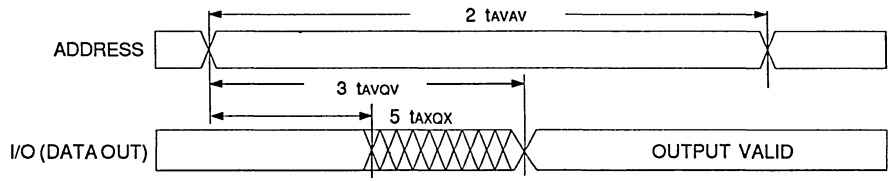
RECOMMENDED AC OPERATING CONDITIONS (-55°C ≤ T_A ≤ 125°C) (V_{CC} = 5.0V ±10%)

READ CYCLE[g]

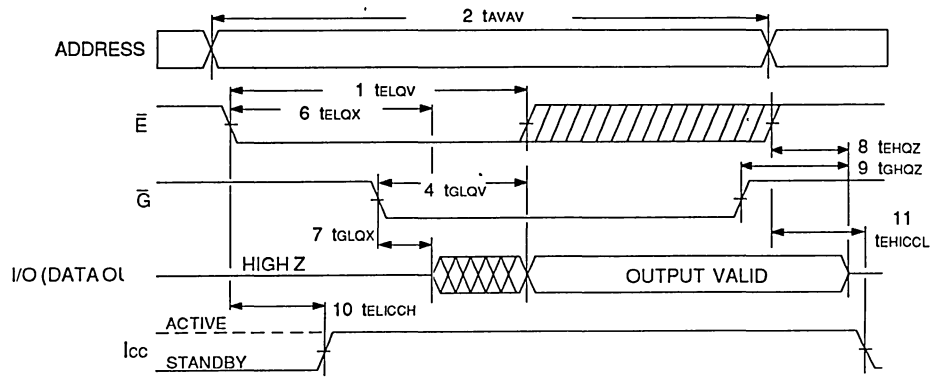
NO.	SYMBOL		PARAMETER	IMS1624M-45		IMS1624M-55		IMS1624M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		45		55		70	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	45		55		70		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		45		55		70	ns	d
4	t_{GLQV}	t_{OE}	Output Enable Access Time		20		25		30	ns	
5	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		5		ns	
6	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	j
7	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	5		5		5		ns	j
8	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive	0	15	0	20	0	25	ns	f, j
9	t_{GHQZ}	t_{OHZ}	Output Disable to Output Inactive	0	15	0	20	0	25	ns	f, j
10	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
11	t_{EHICCL}	t_{PD}	Chip Enable to Power Down		45		55		70	ns	j
		t_T	Input Rise and Fall Times		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



RECOMMENDED AC OPERATING CONDITIONS (-55°C ≤ TA ≤ 125°C) (Vcc = 5.0V ±10%)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g,h]

	SYMBOL		PARAMETER	IMS 1624-45		IMS 1624-55		IMS 1624-70		UNITS	NOTES
No	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
12	tAVAV	tWC	Write Cycle Time	40		50		60		ns	
13	tWLWH	tWP	Write Pulse Width	30		40		50		ns	
14	tELWH	tCW	Chip Enable to End of Write	30		40		50		ns	
15	tDVWH	tDW	Data Setup to End of Write	20		25		30		ns	
16	tWHDX	tDH	Data Hold after End of Write	0		0		0		ns	
17	tAVWH	tAW	Address Setup to End of Write	30		40		50		ns	
18	tAVWL	tAS	Address Setup to Start of Write	0		0		0		ns	
19	tWHAX	tWR	Address Hold after End of Write	0		0		0		ns	
20	tWLQZ	tWZ	Write Enable to Output Disable	0	15	0	20	0	25	ns	f,j
21	tWHQX	tOW	O/P Active after end of Write	0		0		0		ns	i,j

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g,h]

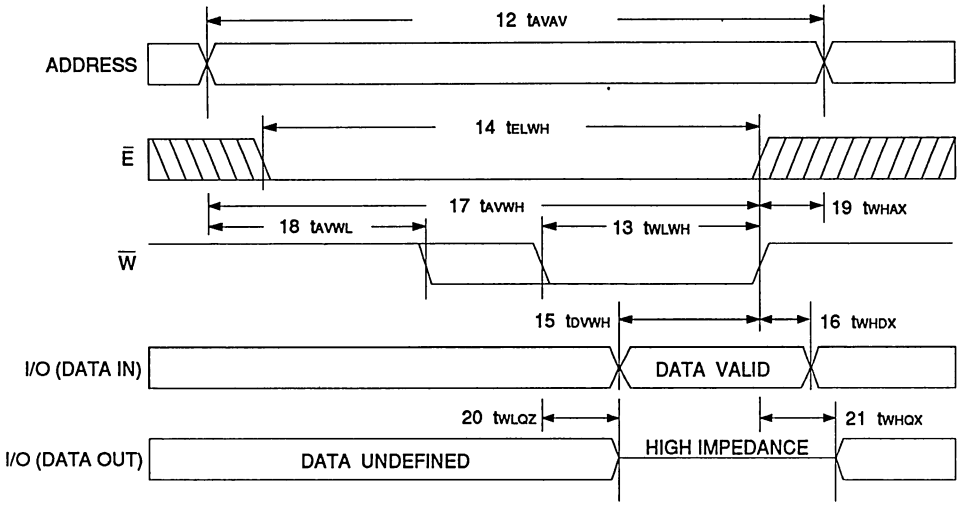
	SYMBOL		PARAMETER	IMS 1624-45		IMS 1624-55		IMS 1624-70		UNITS	NOTES
No	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
22	tAVAV	tWC	Write Cycle Time	40		50		60		ns	
23	tWLEH	tWP	Write Pulse Width	30		40		50		ns	
24	tELEH	tCW	Chip Enable to End of Write	30		40		50		ns	
25	tDVEH	tDW	Data Setup to End of Write	20		25		30		ns	
26	tEHDX	tDH	Data Hold after End of Write	0		0		0		ns	
27	tAVEH	tAW	Address Setup to End of Write	30		40		50		ns	
28	tEHAX	tWR	Address Hold after End of Write	0		0		0		ns	
29	tAVEL	tAS	Address Setup to Start of Write	0		0		0		ns	
30	tWLQZ	tWZ	Write Enable to Output Disable	0	15	0	20	0	25	ns	f,j

WRITE CYCLE 3: Fast Write, Outputs Disabled[g,h]

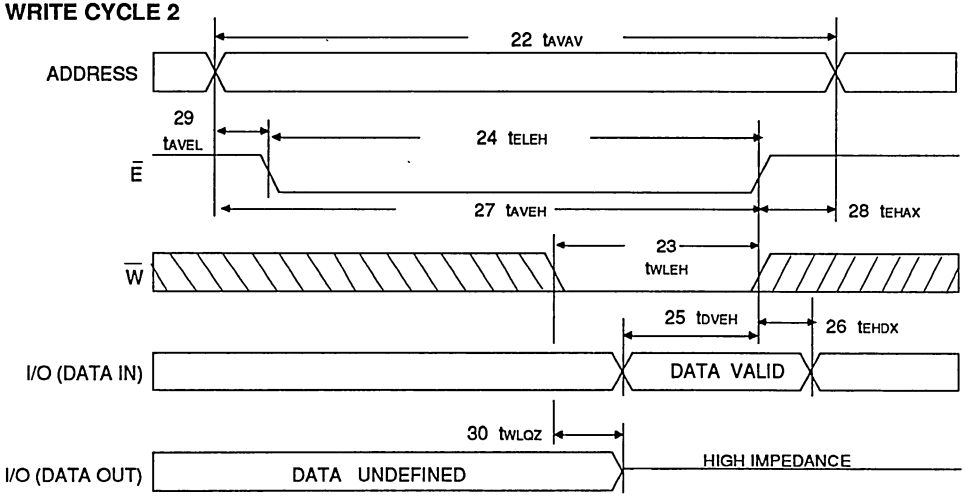
	SYMBOL		PARAMETER	IMS 1624-45		IMS 1624-55		IMS 1624-70		UNITS	NOTES
No	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
31	tAVAV	tWC	Write Cycle Time	25		30		35		ns	
32	tWLWH	tWP	Write Pulse Width	20		25		30		ns	
33	tDVWH	tDW	Data Setup to End of Write	20		25		30		ns	
34	tWHDX	tDH	Data Hold after End of Write	0		0		0		ns	
35	tAVWH	tAW	Address Setup to End of Write	20		25		30		ns	
36	tWHAX	tWR	Address Hold after End of Write	5		5		5		ns	
37	tAVWL	tAS	Address Setup to Start of Write	0		0		0		ns	

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$, $\overline{G}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

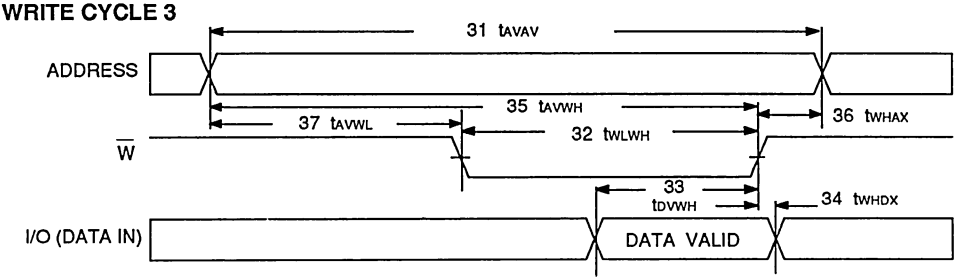
WRITE CYCLE 1



WRITE CYCLE 2



WRITE CYCLE 3



DEVICE OPERATION

The IMS1624M has three control inputs, Chip Enable (/E), Output Enable (/G) and Write Enable (/W), 14 address inputs (A0 -A13), and four Data I/O pins.

The /E input controls device selection as well as active and standby modes. With /E low, the device is selected and the 14 address inputs are decoded to select one 4-bit word out of 16,384. Read and Write operations on the memory cells are controlled by the /W and /G inputs. With /E high, the device is deselected, the outputs are disabled and the power consumption is reduced to less than one-fourth of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as /W $\geq$ V_{IH}min with /E and /G $\leq$ V_{IL}max. Read access time is measured from the latter of either /E or /G going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while /E and /G are low. The outputs remain active throughout READ CYCLE 1 and are valid at the specified address access time. The address inputs may change at access time and long as /E and /G remain low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated bythe latter of /E or /G going low. As long as address is stable when /E goes low, valid data is at the outputs at thelatter of specified Chip Enable Access or Output Enable Access times. If address is not valid when /E goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1624M is initiated by the latter of /E or /W to transition from a high to a low. In the case of /W falling last, the output buffers are turned on t_{ELQX} after the falling edge of /E if /G is already low (just as in a read cycle). The output buffers are then turned off within t_{WLQZ} of the falling edge of /W. During this interval it is possible to have bus contention between devices with common I/O configurations. Therefore input data should not be active until t_{WLQZ}. To aviod bus contention, the /G input can be held high throughout the write operation.

WRITE CYCLE 1 waveform shows a write cycle terminated by /W going high. Data set-up and hold times are referenced to the rising edge of /W. When /W goes high at the end of the cycle with /E active, the output of the memory becomes active (if /G is low). The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by /E going high. Data set-up and hold times are referenced to the rising edge of /E. With /E high the outputs remain in the high impedance state.

WRITE CYCLE 3 waveform shows a write cycle controlled by /W, with /G high and /E low throughout the cycle. As the outputs will not become active during this operation, maximum data bandwidth is provided by allowing very short write cycles and eliminating any bus contention considerations.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1624M. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum.

Current transients associated with the operation of any high speed device have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad and be placed between each row of devices in the array. A larger capacitor to eliminate low frequency ripple should be placed near the edge connection where the power traces meet the backplane power. The larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit area to provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

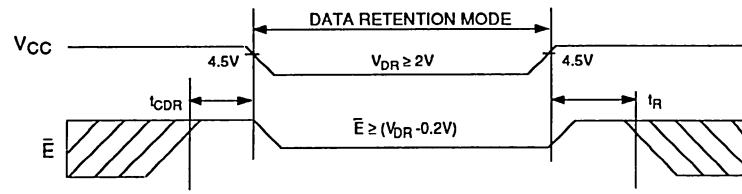
Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.

DATA RETENTION (L version only) ($-55°C \le T_A \le 125°C$)

SYMBOL	PARAMETER	MIN	TYP*	MAX	UNITS	NOTES
V_{DR}	Data Retention Voltage	2.0			volts	$V_{IN} \le 0.2V$ or $\ge (V_{CC}-0.2V)$ $\overline{E} \ge (V_{CC}-0.2V)$
I_{CCDR1}	Data Retention Current		15	1200	µA	V_{CC}= 3.0 volts
I_{CCDR2}	Data Retention Current		10	800	µA	V_{CC}= 2.0 volts
t_{EHVCCL}	Deselect Time (t_{CDR})	0			ns	j, k
t_{VCCHEL}	Recovery Time (t_R)	t_{RC}			ns	j, k (t_{RC}= Read Cycle Time)

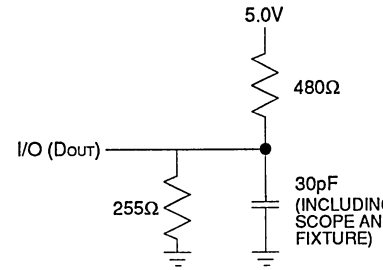
*Typical data retention parameters at 25°C.
Note j: Parameter guaranteed but not tested.
Note k: Supply recovery rate should not exceed 100mV per µS from V_{DR} to V_{CC} min.

LOW V_{CC} DATA RETENTION



Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

FIGURE 1. OUTPUT LOAD



TRUTH TABLE

$\overline{E}$	$\overline{W}$	$\overline{G}$	I/O	MODE
H	X	X	HI-Z	Standby (Isb)
L	H	H	HI-Z	Output Disable
L	H	L	Dout	Read
L	L	X	Din	Write

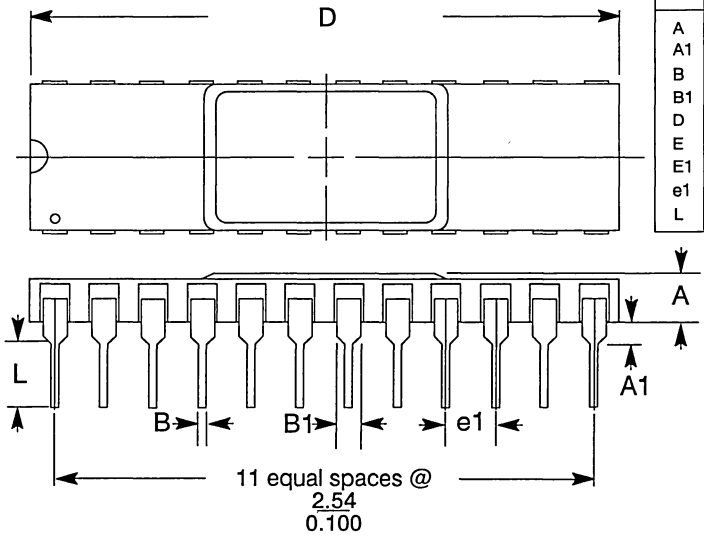
Standard Military Drawing version available, see SMD Reference Guide

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER	
			STANDARD	LOW POWER
IMS 1624M IMS1624LM	45ns	CERAMIC DIP	IMS1624S-45M	IMS1624LS45M
	45ns	CERAMIC LCC	IMS1624N-45M	IMS1624LN45M
	55ns	CERAMIC DIP	IMS1624S-55M	IMS1624LS55M
	55ns	CERAMIC LCC	IMS1624N-55M	IMS1624LN55M
	70ns	CERAMIC DIP	IMS1624S-70M	IMS1624LS70M
	70ns	CERAMIC LCC	IMS1624N-70M	IMS1624LN70M

PACKAGING INFORMATION

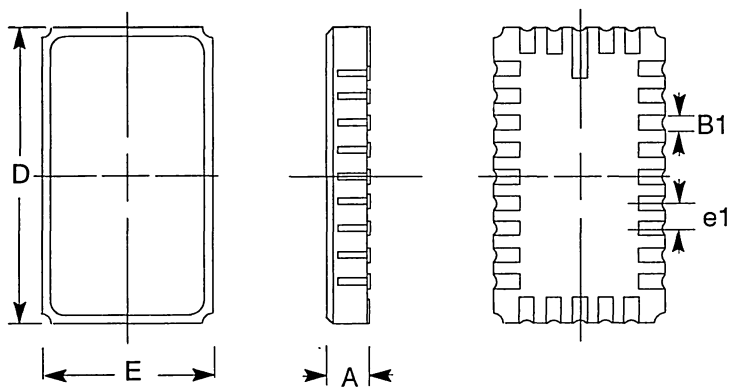
24 Pin Ceramic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.096	.012	2.438	.305
A1	.035	.015	.889	.381
B	.018	.002	.457	.051
B1	.060	Typ	1.524	Max
D	1.20	.012	30.48	.305
E	.315	.010	8.001	.254
E1	.295	.015	7.493	.381
e1	.100	.010	2.54	.254
L	.145	.020	3.683	.508

28 Pin Leadless Chip Carrier

Dim	Inches		mm		Notes
	Nom	Tol	Nom	Tol	
A	.071	.007	1.803	.178	
B1	.025	.003	.635	.076	
D	.550	.010	13.970	.254	
E	.350	.010	8.890	.254	
e1	.050	.002	1.270	.051	



IMS1630M
IMS1630LM
CMOS High Performance 8K x 8 Static RAM MIL-STD-883C

FEATURES

- INMOS' Very High Speed CMOS
- Military Temperature Range (-55°C to 125°C)
- Advanced Process - 1.6 Micron Design Rules
- 8K x 8 Bit Organization
- 45, 55 and 70 ns Address Access Times
- 45, 55 and 70 ns Chip Enable Access Times
- Fully TTL Compatible
- Common Data Inputs and Outputs
- Single +5V ± 10% Operation
- Fast Write Cycle when Outputs Disabled
- Standard Military Drawing version available
- 28 pin DIP, 32 pin LCC (JEDEC Standard)
- Battery Backup Operation - 2V data retention (L version only)

DESCRIPTION

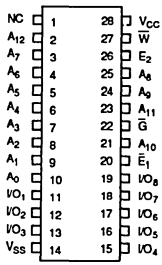
The IMS1630M is a high speed CMOS 8K x 8 Static RAM processed in full compliance to MIL-STD-883C.

The IMS1630M features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The IMS1630M provides two Chip Enable functions (/E1, E2) to place the circuit in a reduced power standby mode.

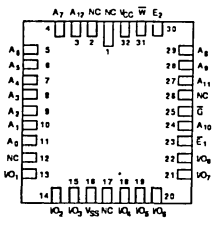
The IMS1630LM is a low power version offering battery backup data retention operating from a 2 volt supply.

The IMS1630M and IMS1630LM are VLSI Static RAMs intended for military applications that demand high performance and superior reliability.

PIN CONFIGURATION

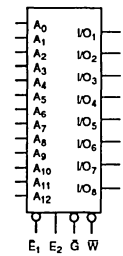


DIP

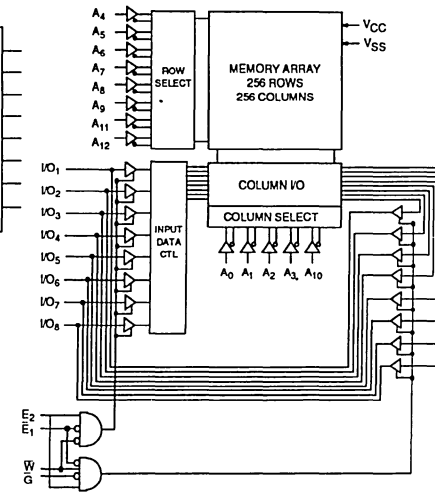


LCC

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_{12}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
I/O_1-I/O_8	DATA IN/OUT		
E_1, E_2	CHIP ENABLE		
$\overline{G}$	OUTPUT ENABLE		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on I/O.....-1.0 to (Vcc+0.5)V
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One output at a time, one second duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+0.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	-55		+125	°C	400 linear ft/min air flow

*V_{IL} min = -3.0 volts for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS (-55°C ≤ T_A ≤ 125°C) (V_{CC} = 5.0V ± 10%)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		85	mA	tAVAV = tAVAV (min)
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		30	mA	$\bar{E}$ ≥ V_{IH} . All other inputs at V_{IN} ≤ V_{IL} or ≥ V_{IH}
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		17	mA	$\bar{E}$ ≥ (Vcc - 0.2) . All other inputs at V_{IN} ≤ 0.2 or ≥ (Vcc - 0.2V)
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		20	mA	$\bar{E}$ ≥ (Vcc - 0.2). All other inputs cycling at V_{IN} ≤ 0.2 or ≥ (Vcc - 0.2V)
I_{ILK}	Input Leakage Current (Any Input)		±5	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		±10	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OUT} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OUT} = 8mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels .....V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0MHZ)[b]

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

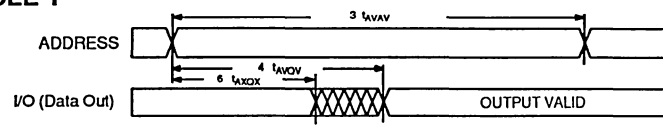
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \le T_A \le 125°C$)($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[g]

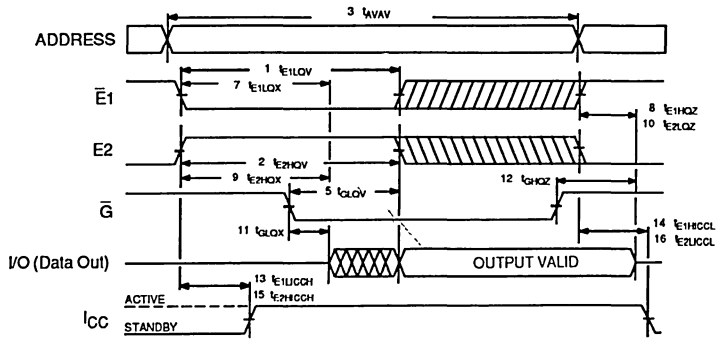
NO.	SYMBOL Standard	SYMBOL Alternate	PARAMETER	1630M-45 MIN	1630M-45 MAX	1630M-55 MIN	1630M-55 MAX	1630M-70 MIN	1630M-70 MAX	UNITS	NOTES
1	t_{E1LQV}	t_{ACS}	Chip Enable Access Time		45		55		70	ns	
2	t_{E2HQV}	t_{ACS}	Chip Enable Access Time		45		55		70	ns	
3	t_{AVAV}	t_{RC}	Read Cycle Time	45		55		70		ns	c
4	t_{AVQV}	t_{AA}	Address Access Time		45		55		70	ns	d
5	t_{GLQV}	t_{OE}	Output Enable to Data Valid		15		20		25	ns	
6	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		5		ns	
7	t_{E1LQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	
8	t_{E1HQZ}	t_{HZ}	Chip Disable to Output Inactive	0	20	0	25	0	25	ns	f, j
9	t_{E2HQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	
10	t_{E2LQZ}	t_{HZ}	Chip Disable to Output Inactive	0	20	0	25	0	25	ns	f, j
11	t_{GLQX}	t_{LZ}	Output Enable to Output Active	5		5		5		ns	
12	t_{GHQZ}	t_{HZ}	Output Disable to Output Inactive	0	20	0	25	0	25	ns	f, j
13	$t_{E1LICCH}$	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
14	$t_{E1HICCL}$	t_{PD}	Chip Enable to Power Down		25		30		35	ns	j
15	$t_{E2HICCH}$	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
16	$t_{E2LICCL}$	t_{PD}	Chip Disable to Power Down		25		30		35	ns	j
		t_T	Input Rise and Fall Times		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected, $\overline{E1}$ low, $\overline{G}$ low and E2 high.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E1}$, E2, $\overline{G}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c, d]



READ CYCLE 2[c]



RECOMMENDED AC OPERATING CONDITIONS (-55°C ≤ T_A ≤ 125°C) (V_{CC} = 5.0V ±10%)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g,h]

No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1630M-45 MIN	IMS 1630M-45 MAX	IMS 1630M-55 MIN	IMS 1630M-55 MAX	IMS 1630M-70 MIN	IMS 1630M-70 MAX	UNITS	NOTES
18	tAVAV	t WC	Write Cycle Time	45		55		70		ns	
19	tWLWH	t WP	Write Pulse Width	35		45		50		ns	
20	tE1LWH	t CW	Chip Enable 1 to End of Write	35		45		50		ns	
21	tE2HWH	t CW	Chip Enable 2 to End of Write	35		45		50		ns	
22	tDVWH	t DW	Data Setup to End of Write	20		25		25		ns	
23	tWHDX	t DH	Data Hold after End of Write	0		0		0		ns	
24	tAVWH	t AW	Address Setup to End of Write	35		45		50		ns	
25	tAVWL	t AS	Address Setup to Start of Write	0		0		0		ns	
26	tWHAX	t WR	Address Hold after End of Write	0		0		0		ns	
27	tWLQZ	t WZ	Write Enable to Output Disable	0	20	0	20	0	25	ns	f,j
28	tWHQX	t OW	Output Active After End of Write	5		5		5		ns	i,j

WRITE CYCLE 2: $\overline{E}$1 OR E2 CONTROLLED[g,h]

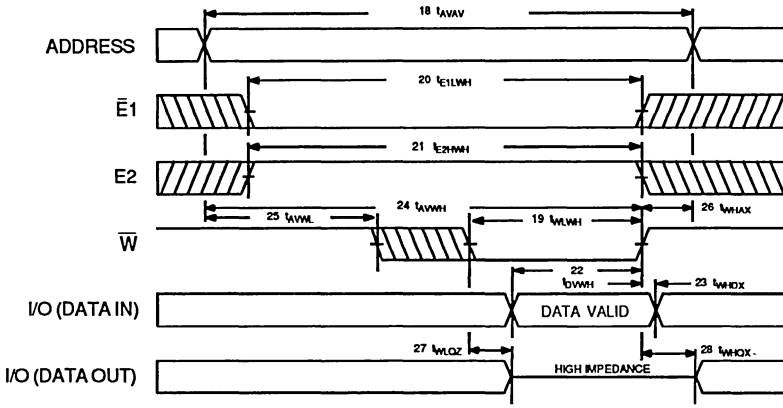
No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1630M-45 MIN	IMS 1630M-45 MAX	IMS 1630M-55 MIN	IMS 1630M-55 MAX	IMS 1630M-70 MIN	IMS 1630M-70 MAX	UNITS	NOTES
29	tAVAV	t WC	Write Cycle Time	45		55		70		ns	
30	tWLE1H	t WP	Write Pulse Width	35		45		50		ns	
31	tE1LE1H	t CW	Chip Enable 1 to End of Write	35		45		50		ns	
32	tE2HE2L	t CW	Chip Enable 2 to End of Write	35		45		50		ns	
33	tDVE1H	t DW	Data Setup to End of Write	20		25		25		ns	
34	tE1HDX	t DH	Data Hold after End of Write	0		0		0		ns	
35	tAVE1H	t AW	Address Setup to End of Write	35		45		50		ns	
36	tE1HAX	t WR	Address Hold after End of Write	0		0		0		ns	
37	tAVE1L	t AS	Address Setup to Start of Write	0		0		0		ns	
38	tWLQZ	t WZ	Write Enable to Output Disable	0	20	0	20	0	25	ns	f,j

WRITE CYCLE 3: FAST WRITE, OUTPUTS DISABLED (DEVICE CONTINUOUSLY SELECTED, $\overline{G}$ HIGH)[g,h]

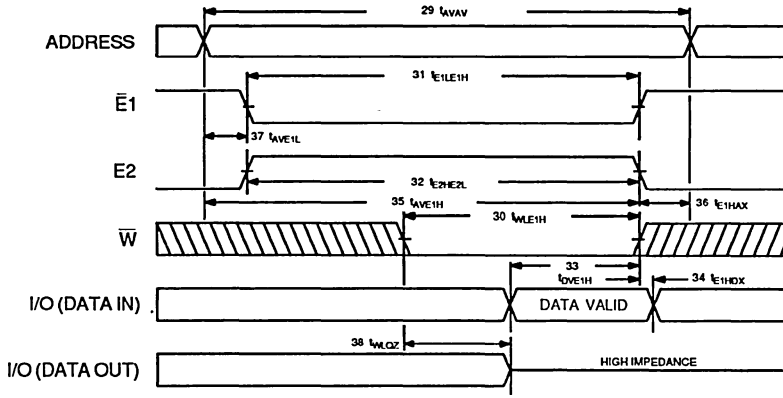
No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1630M-45 MIN	IMS 1630M-45 MAX	IMS 1630M-55 MIN	IMS 1630M-55 MAX	IMS 1630M-70 MIN	IMS 1630M-70 MAX	UNITS	NOTES
39	tAVAV	t WC	Write Cycle Time	25		30		35		ns	
40	tWLWH	t WP	Write Pulse Width	20		25		30		ns	
41	tDVWH	t CW	Data Set-up to End of Write	20		25		30		ns	
42	tWHDX	t CW	Data Hold After End of Write	0		0		0		ns	
43	tAVWH	t DW	Address Set-up to End of Write	20		25		30		ns	
44	tWHAX	t DH	Addres Hold After End of Write	0		0		0		ns	
45	tAVWL	t AS	Address Set-up to Start of Write	0		0		0		ns	

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$1, E2, $\overline{G}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$1, or $\overline{W}$ must be ≥ V_{IH} or E2 must be ≤ V_{IL} during address transitions.
Note i: If $\overline{W}$ is low when the later of $\overline{E}$1 goes low or E2 goes high, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

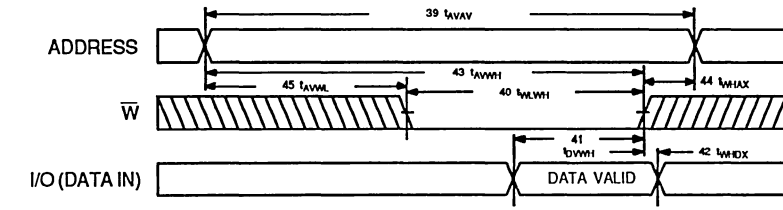
WRITE CYCLE 1



WRITE CYCLE 2



WRITE CYCLE 3



DEVICE OPERATION

The IMS1630M has four control inputs, Chip Enable1 ($\overline{E1}$), Chip Enable 2 (E2), Write Enable ($\overline{W}$) and Output Enable ($\overline{G}$). There are also13 address inputs (A0 -A12) and eight Data I/O lines (I/O 1 to I/O 8). The Enable inputs control device selection as well as active and standby modes. The $\overline{W}$ input controls the mode of operation (Read or Write). The $\overline{G}$ input controls only the state of the eight output drivers.

With both $\overline{E1}$ low and E2 high, the device is selected and the 13 address inputs are decoded to select one 8-bit word out of 8K words. Read and Write operations on the memory cells are controlled by the $\overline{W}$ input. With either $\overline{E1}$ high or E2 low, the device is deselected, the outputs disabled and the power consumption is reduced to less than one-fourth of the active mode power. $\overline{G}$ serves only to control the operation of the output drivers. When $\overline{G}$ is high, the output drivers are in a high impedance state, independant of the $\overline{E1}$, E2 and $\overline{W}$ inputs.

READ CYCLE

A read cycle is defined as $W \geq V_{IH}$ min with $\overline{E1} \leq V_{IL}$ max, $E2 \geq V_{IH}$ min and $\overline{G} \leq V_{IL}$ max. Read access time is measured from the later of either $\overline{E1}$ going low, E2 going high, valid address, or $\overline{G}$ going low.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E1}$ is low and E2 is high (with $\overline{G}$ low). The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and the output remains valid for a minimum of tAXQX. As long as $\overline{E1}$ remains low and E2 is high, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by the later of $\overline{E1}$ going low, E2 going high or $\overline{G}$ going low. As long as address is stable when the later of $\overline{E1}$ goes low or E2 goes high, valid data is at the output at the later of tE1LQV, tE2HQV or tGLQV. If address is not valid when the later of $\overline{E1}$ goes low or E2 goes high, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

The $\overline{G}$ signal controls the output buffer. $\overline{G}$ is required to be low (along with $\overline{E1}$ low and E2 high) in order for I/O1 - I/O 8 to be active.

WRITE CYCLE

The write cycle of the IMS1630M is initiated by the later of $\overline{E1}$ or W to transition from a high to a low or E2 transitioning from low to high. The G control will remove bus contention if held high throughout the duration of the write cycle. If G is low during a W controlled write cycle (Write Cycle 1), the output buffer will be turned on by the later of tE1LQX after the falling edge of E1 or tE2HQX after the rising edge of E2. The output buffer is then turned off within tWLQZ of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with common input/output connections. Therefore the recommended mode of operation is to keep $\overline{G}$ high during the write cycle. During a write cycle, data on the inputs is written into the selected cells and the outputs are floating.

For any write cycle, tAVWL, tAVE1L, or tAVE2H must be met, depending on whether $\overline{E1}$, E2 or $\overline{W}$ is the last to transition. After either $\overline{W}$ or $\overline{E1}$ goes high or E2 goes low to terminate the write cycle, addresses may change. If address set-up and hold times are not met, contents of other cells may be altered in unpredictable ways. The fidelity of the $\overline{W}$ control signal is very important. Excessive ringing on high to low transitions may cause signals to rise above V_{IL} max, violating the minimum $\overline{W}$ pulse width specification - tWLWH.

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. When $\overline{W}$ goes high while $\overline{E1}$ is low and E2 is high, the outputs remain in a high impedance state (unless $\overline{G}$ is low). If $\overline{G}$ is low when $\overline{W}$ goes high at the end of a write cycle the data read from the memory will be the same as the data just written into the memory. Thus, no data bus contention will occur.

WRITE CYCLE 2 waveform shows a write cycle terminated by the later $\overline{E1}$ going high or E2 going low. Data set-up and hold times are referenced to the later of the rising edge of $\overline{E1}$ or the falling edge of E2. With either $\overline{E1}$ high or E2 low the outputs remain in the high impedance state.

When using WRITE CYCLE 1 proper management of the $\overline{G}$ control signal will avoid bus contention. If $\overline{G}$ is low when $\overline{W}$ goes high (with $\overline{E1}$ low and E2 high) the output buffers will be active tWHQX after the rising edge of $\overline{W}$. Data out will be the same as the data just written, unless the address changes. If input data from the previous cycle is still valid after the address changes, contention may result. Contention may also result if the device is selected ($\overline{E1}$ low, E2 high, $\overline{G}$ low) before $\overline{W}$ goes low and input data is valid early in the cycle. The recommended mode of operation is to keep $\overline{G}$ high except when reading data from the device, thus avoiding bus contention.

TTL VS. CMOS INPUTLEVELS

The INMOS 1630M is fully compatible with TTL input levels. The input circuitry of the IMS1630M is designed for maximum speed and also for conversion of TTL level signals to the CMOS levels required for internal operation. The IMS1630M consumes less power when CMOS levels are used instead of TTL levels. The lower CMOS Icc specifications (Icc3 and Icc4) may be achieved by using CMOS levels. The power consumption will be lower at typical TTL levels than at the worst case levels.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1630M. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Current transients associated with the operation of any high speed device have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 µF and be placed between each row of devices in the array. A larger tantalum capacitor of a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit area. This will provide a solid ground reference for the drivers and prevent loss of operating margin due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically. A resistor of predetermined value may not properly terminate the transmission line.

Proper power distribution techniques, including adequate use of decoupling capacitors, and proper termination of TTL drive outputs are some of the most important yet basic guidelines that need to be followed when designing and building a memory board. The guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment free of noise spikes, undershoot, and excessive ringing. It is wise to verify signal fidelity by observation utilising a wideband oscilloscope and probe.

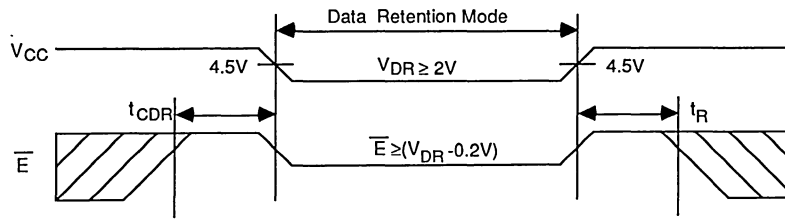
DATA RETENTION (L version only) (-55°C ≤ T_A ≤ 125°C)

SYMBOL	PARAMETER	MIN	TYP*	MAX	UNITS	NOTES
V_{DR}	Data Retention Voltage	2.0			volts	V_{IN} ≤ 0.2V or ≥ (Vcc -0.2V) $\overline{E}$ ≥(Vcc -0.2V)
I_{CCDR1}	Data Retention Current		15	1200	µA	V_{CC} = 3.0 volts
I_{CCDR2}	Data Retention Current		10	800	µA	V_{CC} = 2.0 volts
t_{EHVCCL}	Deselect Time (t_{CDR})	0			ns	j,k
t_{VCCHEL}	Recovery Time (t_R)	t_{RC}			ns	j,k (t_{RC} = Read Cycle Time)

* Typical data retention parameters at 25 °C

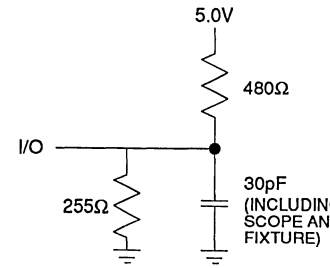
Note j: Parameter guaranteed but not tested

Note k: Supply recovery rate should not exceed 100mV per10µs from V_{DR} to V_{CC} min



Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

FIGURE 1. OUTPUT LOAD



TRUTH TABLE

$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$	I/O	MODE
H	X	X	X	HI-Z	Standby (Isb)
X	L	X	X	HI-Z	Standby (Isb)
L	H	H	H	HI-Z	Output disable
L	H	H	L	Dout	Read
L	H	L	X	Din	Write

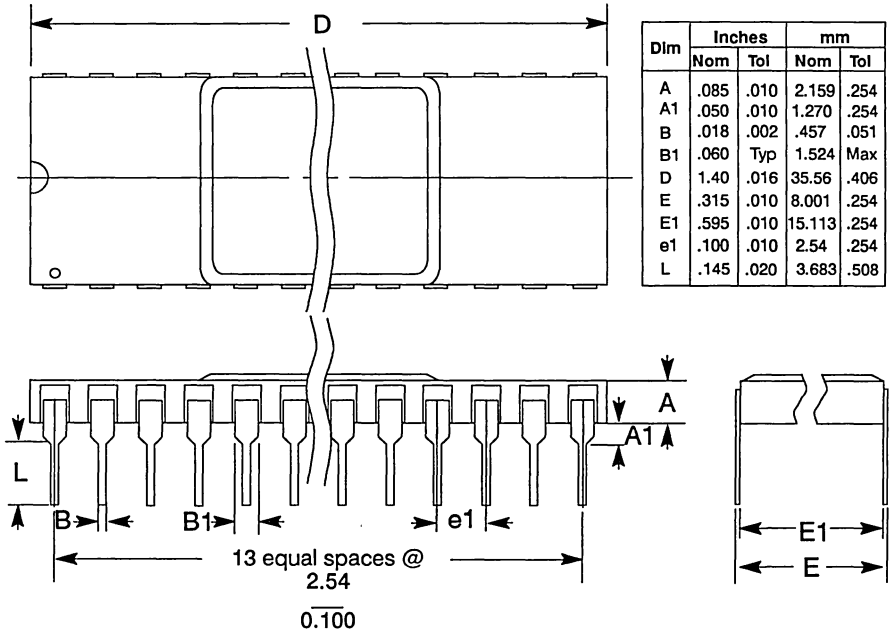
Standard Military Drawing version available, see SMD Reference Guide

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER	
			STANDARD	LOW POWER
IMS 1630M IMS1630LM	45ns	CERAMIC DIP	IMS1630S-45M	IMS1630LS45M
	45ns	CERAMIC LCC	IMS1630N-45M	IMS1630LN45M
	55ns	CERAMIC DIP	IMS1630S-55M	IMS1630LS55M
	55ns	CERAMIC LCC	IMS1630N-55M	IMS1630LN55M
	70ns	CERAMIC DIP	IMS1630S-70M	IMS1630LS70M
	70ns	CERAMIC LCC	IMS1630N-70M	IMS1630LN70M

PACKAGING INFORMATION

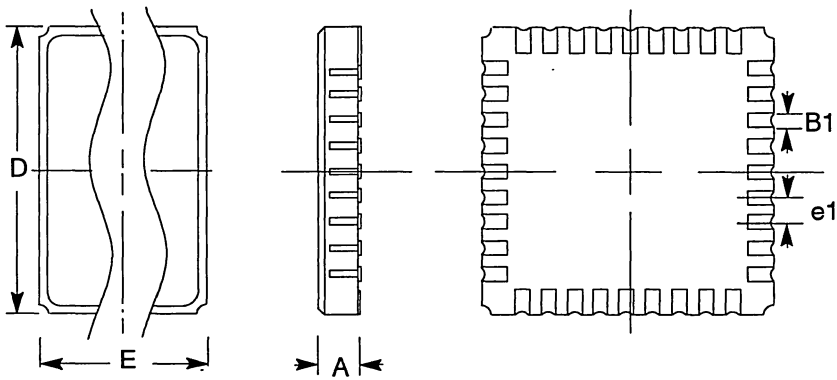
28 Pin Ceramic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.085	.010	2.159	.254
A1	.050	.010	1.270	.254
B	.018	.002	.457	.051
B1	.060	Typ	1.524	Max
D	1.40	.016	35.56	.406
E	.315	.010	8.001	.254
E1	.595	.010	15.113	.254
e1	.100	.010	2.54	.254
L	.145	.020	3.683	.508

32 Pin Leadless Chip Carrier

Dim	Inches		mm		Notes
	Nom	Tol	Nom	Tol	
A	.071	.007	1.803	.178	
B1	.025	.003	.635	.076	
D	.550	.010	13.970	.254	
E	.450	.010	11.43	.254	
e1	.050	.002	1.270	.051	



IMS16X5M series High Performance Memory Products

MIL-STD-883C

IMS 1605M: 64K x 1
IMS 1625M: 16K x 4
IMS 1629M: 16K x 4 with Output Enable
IMS 1626/7M: 16K x 4 with Separate I/Os
IMS 1635M: 8K x 8
IMS 1695M: 8K x 9

Advance Information

FEATURES

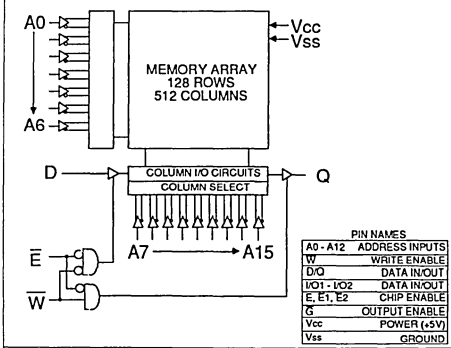
- INMOS' Very High Speed Double Metal CMOS
- Advanced Process-1.2 Micron Design Rules
- 64K Bit Devices
- 20, 25, and 35ns Address Access Times
- 20, 25 and 35 ns Chip Enable Access Times
- Fully TTL Compatible
- Single +5V ± 10% Operation
- Battery Backup Operation - 2V Data Retention, 10µA typical at 25°C
- Packages include: DIP and LCC

DESCRIPTION

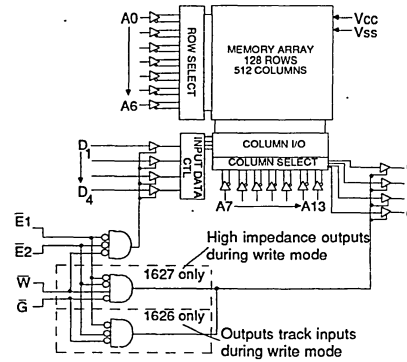
The INMOS IMS16X5M series are high speed advanced 64K double layer metal CMOS Static RAMs.

The range features fully static operation requiring no external clocks or timing strobes, with equal access and cycle times. A chip enable function ($\overline{E}$) that can be used to place the device into a low-power standby mode is available on all organisations. The 8K x 8 organisations provide an additional Chip Enable for reduced low-power standby mode. Output Enable ($\overline{G}$) is an enhancement on organisations requiring fast access to data and enhanced bus contention control. The 16x5M series are intended for military applications that demand high performance and superior reliability.

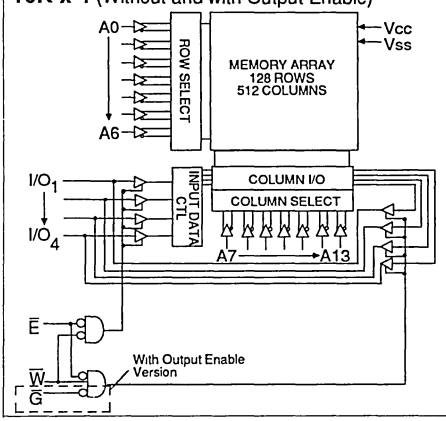
64K x 1



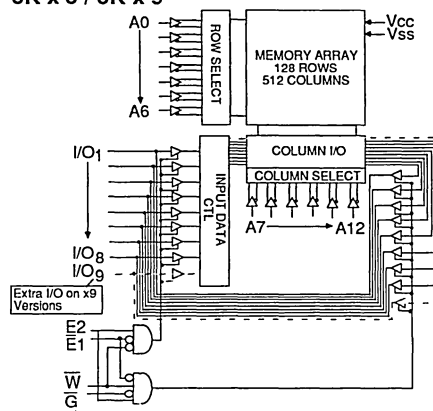
16K x 4 (Separate Inputs and Outputs)



16K x 4 (Without and with Output Enable)



8K x 8 / 8K x 9



IMS1800M CMOS High Performance 256K x 1 Static RAM MIL-STD-883C

Advance Information

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.2 Micron Design Rules
- 256K x 1 Bit Organization
- 30, 35 and 45 ns Address Access Times
- 30, 35 and 45 ns Chip Enable Access Times
- Fully TTL Compatible
- Separate Data Input and Outputs
- Three-state Output
- 24 Pin 300-mil DIP and 28 Pin LCC
- Single +5V ± 10% Operation
- Power Down Function

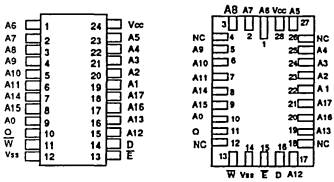
DESCRIPTION

The INMOS IMS1800M is a high performance 256Kx1 CMOS Static RAM. The IMS1800M provides maximum density and speed enhancements with the additional benefits of lower power and superior reliability.

The IMS1800M features fully static operation requiring no external clocks or timing strobes, with equal access and cycle times. Additionally, the IMS1800M provides a Chip Enable function (E) that can be used to place the device into a low power standby mode.

The IMS1800M is a high speed VLSI RAM intended for military applications which require high performance and superior reliability.

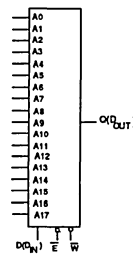
PIN CONFIGURATION



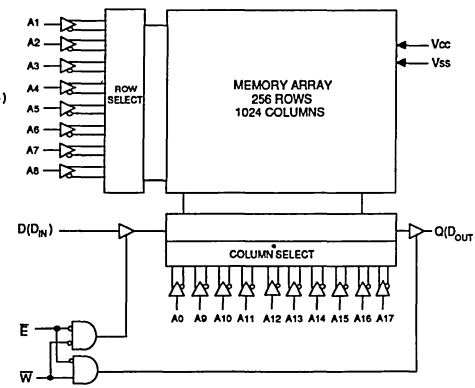
DIP and SOJ

CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{17}	ADDRESS INPUTS	Q	DATA OUT
$\overline{W}$	WRITE ENABLE	Vcc	POWER (+5V)
$\overline{E}$	CHIP ENABLE	Vss	GROUND
D	DATA INPUT		

IMS1820M CMOS High Performance 64K x 4 Static RAM MIL-STD-883C

Advance Information

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.2 Micron Design Rules
- 64K x 4 Bit Organization
- 30, 35 and 45 ns Address Access Times
- 30, 35 and 45 ns Chip Enable Access Times
- Fully TTL Compatible
- Common Data Input and Outputs
- Three-state Output
- 24 Pin 300-mil DIP and 28 Pin LCC
- Single +5V ± 10% Operation
- Power Down Function

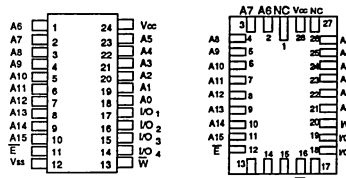
DESCRIPTION

The INMOS IMS1820M is a high performance 64Kx4 CMOS Static RAM. The IMS1820M allows speed enhancements to existing 64K x 4 applications with the additional benefit of reduced power consumption .

The IMS1820M features fully static operation requiring no external clocks or timing strobes, with equal access and cycle times. Additionally, the IMS1820M provides a Chip Enable function (/E) that can be used to place the device into a low power standby mode.

The IMS1820M is a high speed VLSI RAM intended for military applications which require high performance and superior reliability.

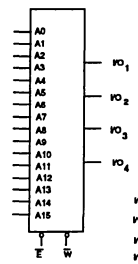
PIN CONFIGURATION



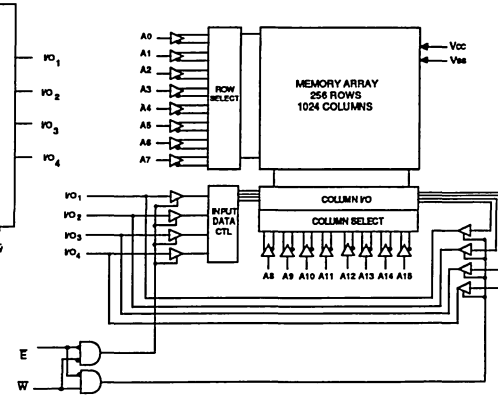
DIP and SOJ

CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{15}	ADDRESS INPUTS	Vcc	POWER (+5V)
W̄	WRITE ENABLE	Vss	GROUND
I/O-I/O	DATA IN/OUT		
Ē	CHIP ENABLE		

NOTES

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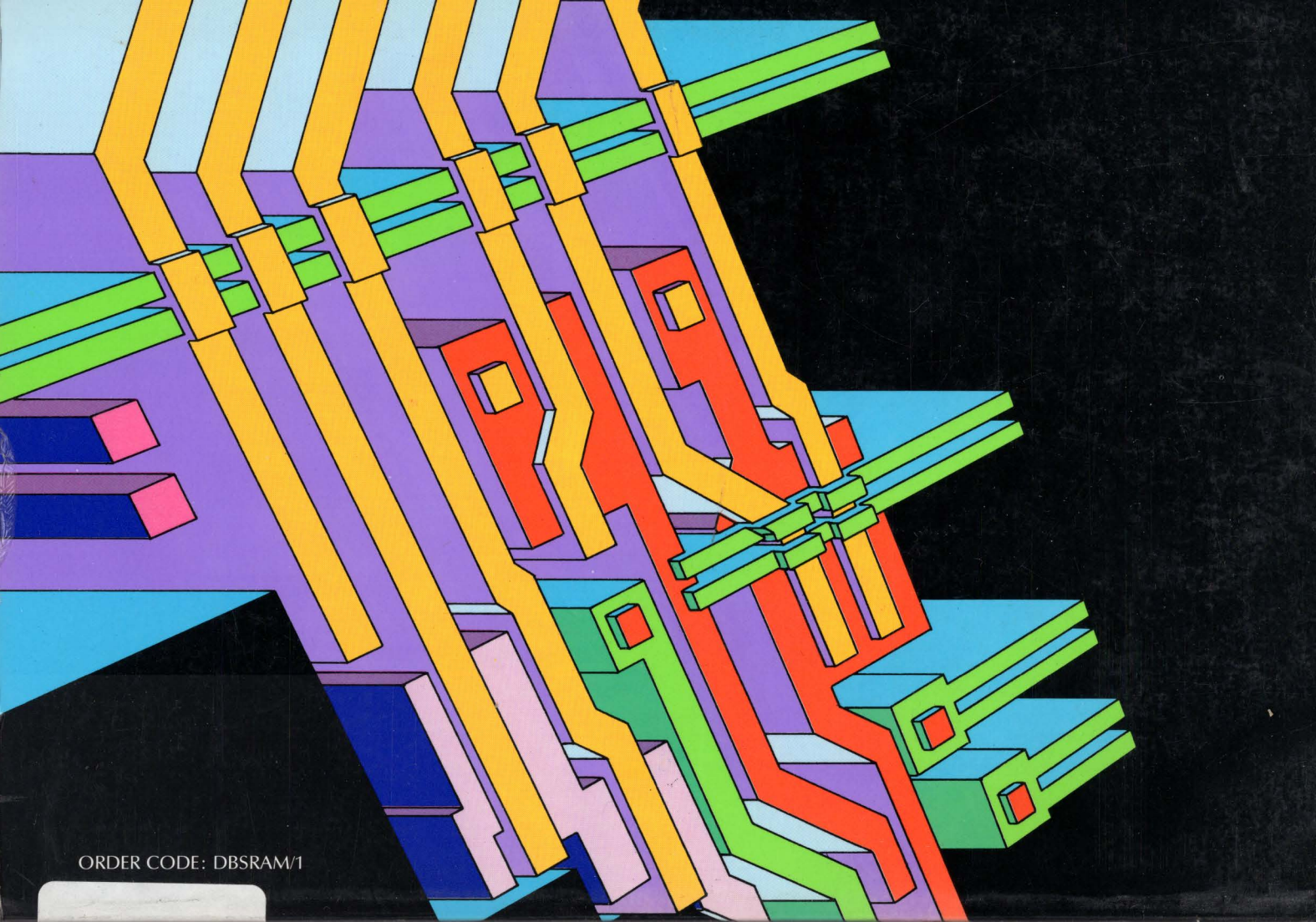

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