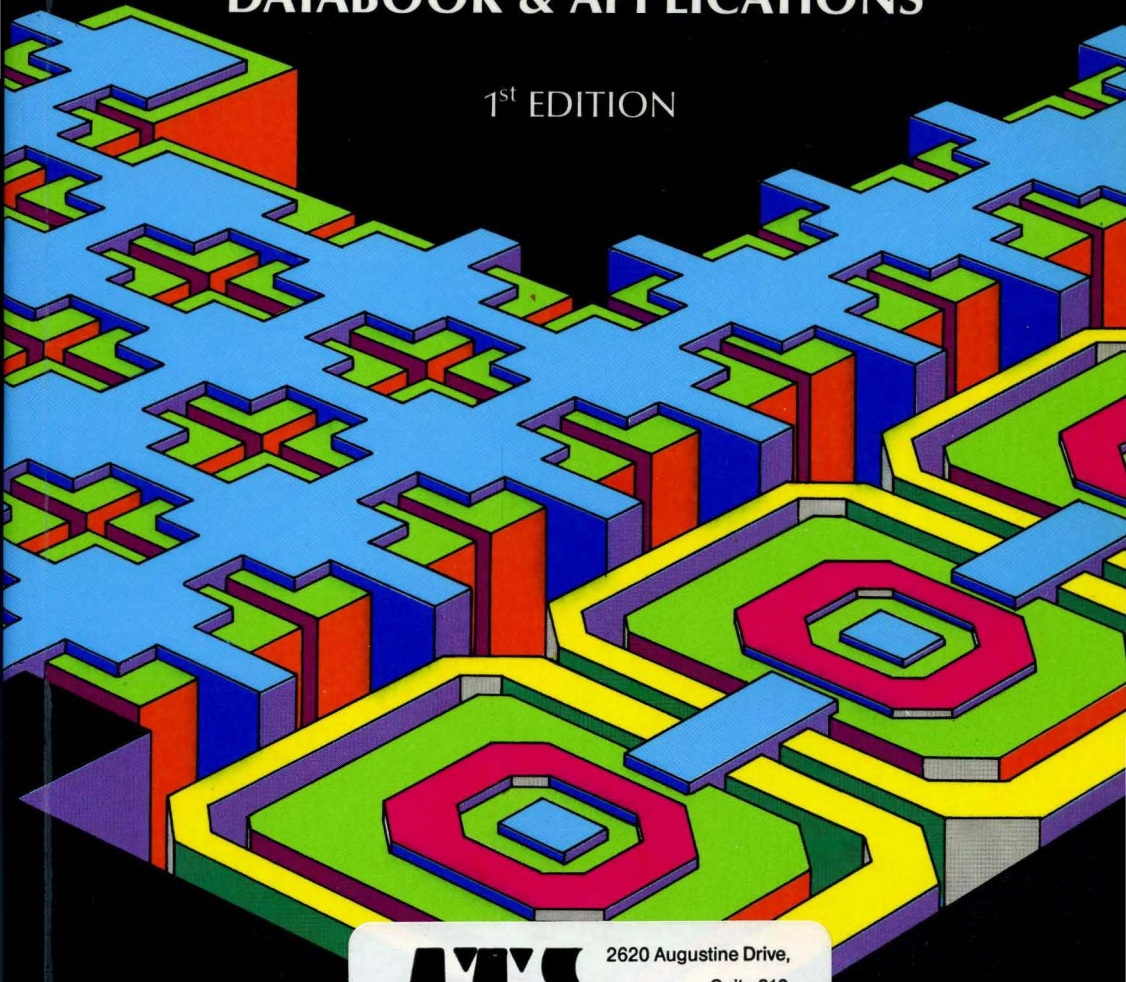
MODEM

DATABOOK & APPLICATIONS

1st EDITION



SGS-THOMSON
MICROELECTRONICS

MODEM

DATABOOK & APPLICATIONS

1st EDITION

MAY 1989

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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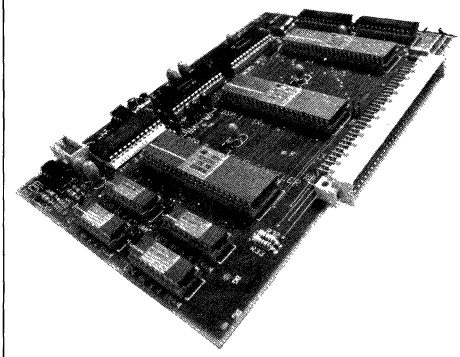
SGS-THOMSON MODEM ICs: A COMMITMENT TO EXCELLENCE

SGS-THOMSON Microelectronics has been a key player in the modem IC market for a long time, accumulating expertise in developing public telephone network modems — V.23, V.22bis, V.32 and others — and exploiting strong manufacturing resources to produce them in quantity.

For this market the company employs technologies that are ideally suited to mixed analog/digital circuits, from a 3 micron double poly to 1.2 micron double metal CMOS processes allowing switched capacitor filtering and high density logic.

Active in a broad spectrum of telecom applications, SGS-THOMSON's design and manufacturing engineers have experience in leading-edge circuits such as the ISDN echo canceller and S Interface transceivers. Moreover, the company is unique in combining expertise in analog conversion and filtering circuits — exemplified by the Analog Front Ends — and in digital signal processing techniques such as automatic adaptive equalization, digital filter carrier recovery and echo cancellation.

In addition to Modem ICs, this databook includes a family of general purpose DSPs that are used in modem datapump design and other telecom applications.



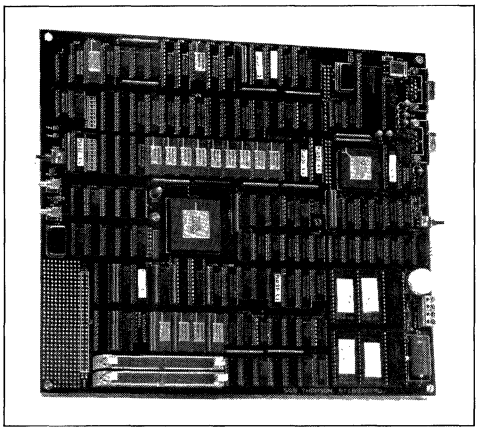
V. 32 - With the SGS-THOMSON TS7532 kit you can build a V. 32 datapump with less than 10 chips. The Kit consist of three DSPs and three Analog Front End ICs.

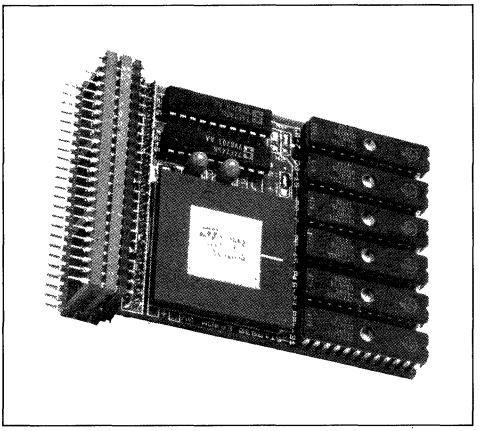
To simplify application software development the DSP family is supported by powerful development tools, including emulators, EPROM modules, cross assemblers simulators, and even a C compiler. Thanks to this set of tools, the users may adapt the SGS-THOMSON application software to suit their own specific needs.

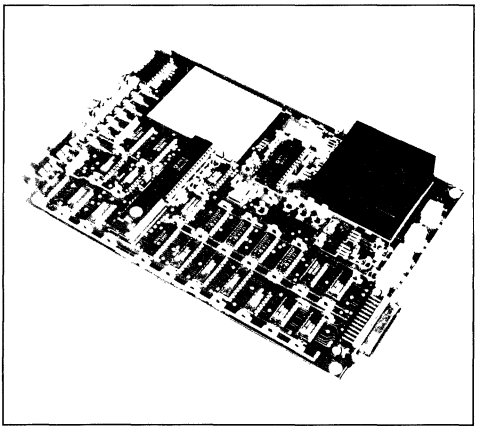
YOUR PARTNER FOR CUSTOMIZED MODEM ICs

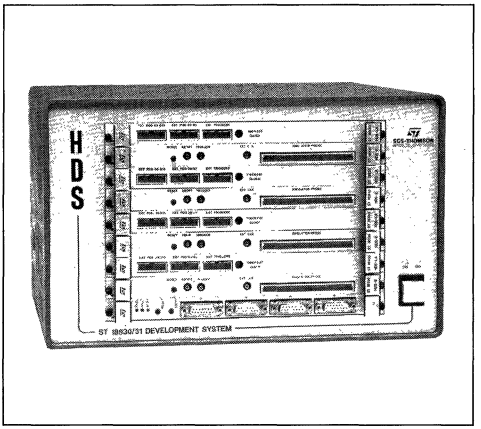
SGS-THOMSON Microelectronics has a long history of close cooperation with major customers in the development of modem ICs, putting the company in an enviable situation for the definition of new dedicated or custom products for this market. This capability is further enhanced by the combination of analog and digital functions on the same chip that is permitted by new generation technologies.

This databook may contains the solution you are looking for, but if you have new ideas or a highly specific application contact SGS-THOMSON to discuss customized solutions.









Development support - SGS-THOMSON's: Digital Signal Processor (DSP) family is supported by a comprehensive range of hardware and software development tools.

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ALPHANUMERICAL INDEX

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POWER SUPPLY MODULE

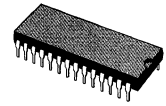
DIGITAL SIGNAL PROCESSORS

DSP APPLICATIONS SUPPORT

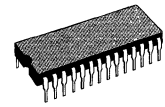
MODEM DATASHEETS

V.21 / V.23 FSK MODEM

- COMPLETE FSK MODEM - JUST ADD LINE INTERFACE
- COMPATIBLE WITH BELL 103/113/108, BELL 202, CCITT V.21, CCITT V.23 SPECIFICATIONS
- NO EXTERNAL FILTERING REQUIRED
- ALL DIGITAL SIGNAL PROCESSING, DIGITAL FILTERS AND ADC/DAC INCLUDED ON-CHIP
- INCLUDES ESSENTIAL RS-232/CCITT V.24 HANDSHAKE SIGNALS
- AUTO-ANSWER CAPABILITY
- LOCAL COPY/TEST MODES
- 1200 BPS FULL DUPLEX ON 4-WIRE LINE
- PIN-PROGRAMMABLE MODE SECTION



P
DIP28
(Plastic Package)



J
CERDIP28
(Cerdip Package)

(Ordering Information at the end of the data-sheet)

DESCRIPTION

The EF7910 is a single-chip asynchronous Frequency Shift Keying (FSK) voiceband modem. It is pin selectable for baud rates of 300, 600, or 1200 bits per second and is compatible with the applicable Bell and CCITT recommended standards for 103/113/108, 202, V.21 and V.23 type modems. Five mode control lines select a desired modem configuration.

Digital signal processing techniques are employed in the EF7910 to perform all major functions such as modulation, demodulation and filtering. The EF7910 contains on-chip analog-to-digital and digital-to-analog converter circuits to minimize the external components in a system. This device includes the essential RS-232/CCITT V.24 terminal control signals with TTL levels.

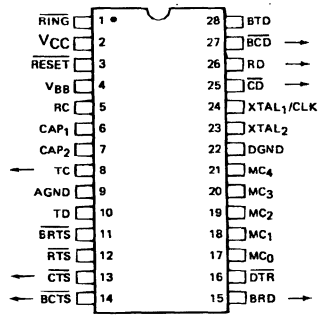
Clocking can be generated by attaching a crystal to drive the internal crystal oscillator or by applying an external clock signal.

A data access arrangement (DAA) or acoustic coupler must provide the phone line interface externally.

The EF7910 is fabricated using HMOS technology. All the digital input and output signals (except the external clock signal) are TTL compatible. Power supply requirements are ± 5 volts.

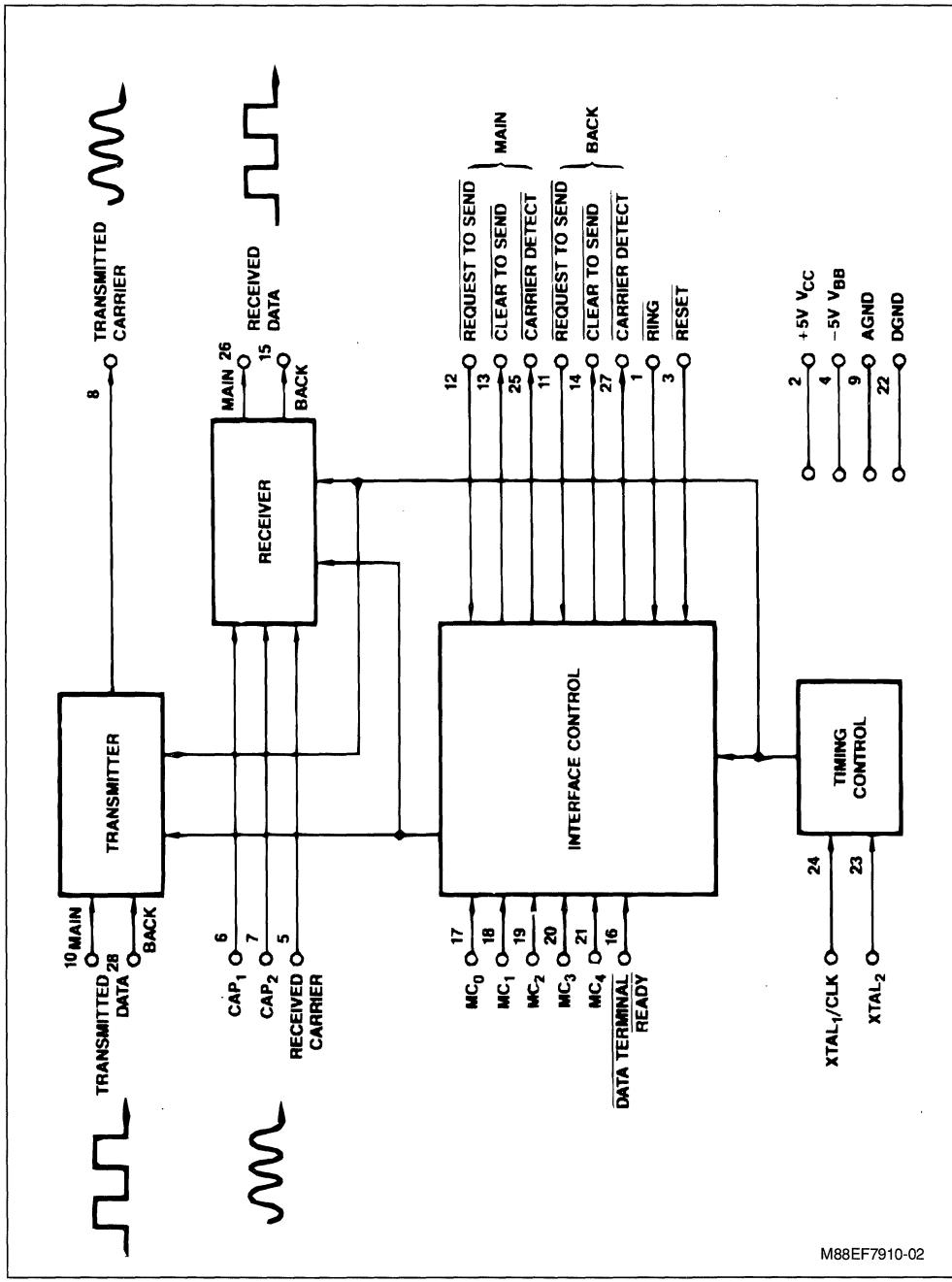
PIN CONNECTIONS

DIP/CERDIP28



M88EF7910-01

BLOCK DIAGRAM



INTERFACE SIGNAL DESCRIPTION

MC_0 - MC_4 (control inputs)

These five inputs select one of thirty-two modem configurations according to the Bell or CCITT specifications listed in table 1. Only 19 of these 32 modes are actually available to the user.

Modes 0-8 are the normal operation modes. The 1200 Baud modes can be selected with or without a compromise equalizer.

Modes 16-25 permit loop back of the EF7910 transmitter and receiver. No internal connection is made. The user must externally connect the TRANSMITTED CARRIER pin (figure 1) to the RECEIVED CARRIER pin if analog loopback is required. For digital loopback, external connection of RECEIVED DATA and TRANSMITTED DATA is required. Whenever a mode in this group is selected, the effect is to set all transmit and receive filters to the same channel frequency band so that loopback can be performed.

Modes 9-15 and 26-31 are reserved and should not be used.

$\overline{\text{DATA TERMINAL READY}}$ ($\overline{\text{DTR}}$)

A LOW level on this input indicates the data terminal desires to send and/or receive data via the modem. This signal is gated with all other TTL inputs and outputs so that a low level enables all these signals as well as the internal control logic to function. A HIGH level disables all TTL I/O pins and the internal logic.

$\overline{\text{REQUEST TO SEND}}$ ($\overline{\text{RTS}}$)

A LOW level on this input instructs the modem to enter transmit mode. This input must remain LOW for the duration of data transmission. The signal has no effect if $\overline{\text{DATA TERMINAL READY}}$ is HIGH (disabled). A HIGH level on this input turns off the transmitter.

$\overline{\text{CLEAR TO SEND}}$ ($\overline{\text{CTS}}$)

This output goes LOW at the end of a delay initiated when $\overline{\text{REQUEST TO SEND}}$ goes LOW. Actual data to be transmitted should not be presented to the TRANSMITTED DATA input until a LOW is indicated on the $\overline{\text{CLEAR TO SEND}}$ output. Normally the user should force the TD input HIGH whenever $\overline{\text{CTS}}$ is off (HIGH). This signal never goes LOW as long as DTR is HIGH (disabled). $\overline{\text{CLEAR TO SEND}}$ goes HIGH at the end of a delay initiated when $\overline{\text{REQUEST TO SEND}}$ goes HIGH.

$\overline{\text{CARRIER DETECT}}$ ($\overline{\text{CD}}$)

A LOW on this output indicates that a valid carrier signal is present at the receiver and has been present for at least a time, t_{CDON}, where t_{CDON} depends upon the selected modem configuration (Table 3b). A HIGH on this output signifies that no valid carrier is being received and has not been received for a time, t_{CDOFF}. $\overline{\text{CARRIER DETECT}}$ remains HIGH when $\overline{\text{DTR}}$ is HIGH. Values for t_{CDON} and t_{CDOFF} are configuration dependent and are listed in table 3b.

TRANSMITTED DATA (TD)

Data bits to be transmitted are presented on this input serially ; HIGH (mark) corresponds to logic 1 and LOW (space) corresponds to logic 0. This data determines which frequency appears at any instant at the TRANSMITTED CARRIER output pin (table 3a). No signal appears at the TRANSMITTED CARRIER output unless $\overline{\text{DTR}}$ is LOW and $\overline{\text{RTS}}$ is LOW.

RECEIVED DATA (RD)

Data bits demodulated from the RECEIVED CARRIER input are available serially at this output. HIGH (mark) indicates logic 1 and LOW (space) indicates logic 0. Under the following conditions this output is forced to logic 1 because the data may be invalid :

1. When $\overline{\text{CARRIER DETECT}}$ is HIGH
2. During the internal squelch delay at half-duplex line turn around (202/V.23 modes only)
3. During soft carrier turnoff at half-duplex line turn around (202 mode only)
4. When $\overline{\text{DTR}}$ is HIGH
5. When $\overline{\text{RTS}}$ ON and $\overline{\text{BRTS}}$ OFF in V.23/202 modes only
6. During auto-answer sequence

$\overline{\text{BACK REQUEST TO SEND}}$ ($\overline{\text{BRTS}}$)

Since the 1200 bps modem configurations, Bell 202 and CCITT V.23, permit only half duplex operation over two-wire lines, a low baud rate "backward" channel is provided for transmission from the main channel receiver to the main channel transmitter. This input signal ($\overline{\text{BRTS}}$) is equivalent to $\overline{\text{REQUEST TO SEND}}$ for the main channel, except it belongs to the backward channel. Note that since the EF7910 contains a single transmitter, $\overline{\text{RTS}}$ and $\overline{\text{BRTS}}$ should not be asserted simultaneously. $\overline{\text{BRTS}}$ is meaningful only when a 202 or V.23 mode is selected by MC_0-MC_4. In all other modes it is ignored.

For V.23 mode the frequency appearing at the transmitted carrier (TC) output pin is determined by a MARK or SPACE at the back transmitted data (BTD) input (table 3a).

For 202 mode a frequency of 387 Hz appears at TC when BRTS is LOW and BTD is HIGH. No energy (0.0 Volt) appears at TC when BRTS is LOW and BTD is HIGH. No energy (0.0 volt) appears at TC when BRTS is HIGH. BTD should be fixed HIGH for 202 back channel transmission. The signal, BRTS, then is equivalent to the signal, Secondary Request-to-Send, for 202 S/T modems, or Supervisory Transmitted Data for 202 C/D modems.

BACK CLEAR TO SEND (BCTS)

This line is equivalent to CLEAR TO SEND for the main channel, except it belongs to the back channel. BCTS is meaningful only when a V.23 mode is selected by MC_0-MC_4. This signal is not used in Bell 202 back mode.

BACK CARRIER DETECT (BCD)

This line is equivalent to CARRIER DETECT for the main channel, except it belongs to the backward channel. BCD is meaningful only when a 202 or V.23 mode is selected by MC_0-MC_4. For V.23 back channel mode, BCD turns on when either the MARK or SPACE frequency appears with sufficient level at the received carrier (RC) input.

For 202 back channel mode, BCD turns on in response to a 387 Hz tone of sufficient level at the RC input. In this case BCD is equivalent to the signal, Secondary Received Line Signal Detector, for 202 S/T modems, or Supervisory Received Data for 202 C/D modems.

BACK TRANSMITTED DATA (BTD)

This line is equivalent to TRANSMITTED DATA for the main channel, except it belongs to the back channel. BTD is meaningful only when a 202 or V.23 mode is selected by MC_0-MC_4. For 202 back transmission of on/off keying, BTD should be fixed at a HIGH level.

BACK RECEIVED DATA (BRD)

This line is equivalent to RECEIVED DATA (except clamping) for the main channel, except it belongs to the back channel. BRD is meaningful only when a V.23 mode is selected by MC_0-MC_4. Under the following conditions this output is forced HIGH :

1. BRD HIGH
2. DTR HIGH
3. V.21/103 mode
4. During auto-answer
5. When BRTS ON and RTS OFF in V.23 modes only

TRANSMITTED CARRIER (TC)

This analog output is the modulated carrier to be conditioned and sent over the phone line.

RECEIVED CARRIER (RC)

This input is the analog signal received from the phone line. The modem extracts the information contained in this modulated carrier and converts it into a serial data stream for presentation at the RECEIVED DATA (BACK RECEIVED DATA) output.

RING

This input signal permits auto-answer capability by responding to a ringing signal from a data access arrangement. If a ringing signal is detected (RING LOW) and DTR is LOW, the modem begins a sequence to generate an answer tone at the TC output.

$XTAL_1$, $XTAL_2$

Master timing of the modem is provided by either a crystal connected to these two inputs or an external clock inserted into $XTAL_1$. The value of the crystal or the external clock frequency must be 2.4576 MHz ± 01 %.

V_{CC}

+ 5 volt power supply (± 5 %)

V_{BB}

– 5 volt power supply (± 5 %).

DGND

Digital signal ground pin.

AGND

Analog signal ground pin (for TRANSMITTED CARRIER and RECEIVED CARRIER).

CAP_1, CAP_2

Connection points of external capacitor/resistor required for proper operation of on-chip analog-to-digital converter.

Recommended values are : C = 2 nF ± 10 %,
R = 100 Ω ± 10 %.

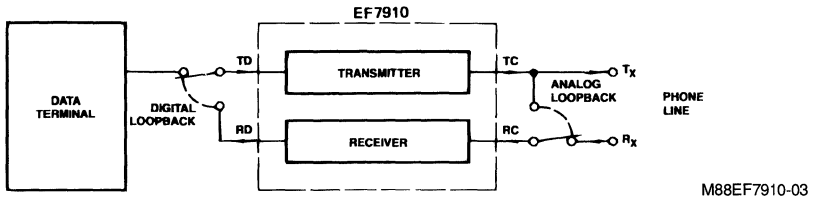
RESET

This input signal is for a reset circuit which operates in either of two modes. It automatically resets when power is applied to the device, or it can be activated by application of an external active low TTL pulse.

Table 1.

MC_4	MC_3	MC_2	MC_1	MC_0	
0	0	0	0	0	Bell 103 Originate 300 bps Full Duplex
0	0	0	0	1	Bell 103 Answer 300 bps Full Duplex
0	0	0	1	0	Bell 202 1200 bps Half Duplex
0	0	0	1	1	Bell 202 with Equalizer 1200 bps Half Duplex
0	0	1	0	0	CCITT V.21 Orig 300 bps Full Duplex
0	0	1	0	1	CCITT V.21 Ans 300 bps Full Duplex
0	0	1	1	0	CCITT V.23 Mode 2 1200 bps Half Duplex
0	0	1	1	1	CCITT V.23 Mode 2 with Equalizer 1200 bps Half Duplex
0	1	0	0	0	CCITT V.23 Mode 1600 bps Half Duplex
0	1	0	0	1	
0	1	0	1	0	
0	1	0	1	1	
0	1	1	0	0	Reserved
0	1	1	0	1	
0	1	1	1	0	
0	1	1	1	1	
1	0	0	0	0	Bell 103 Orig Loopback
1	0	0	0	1	Bell 103 Ans Loopback
1	0	0	1	0	Bell 202 Main Loopback
1	0	0	1	1	Bell 202 with Equalizer Loopback
1	0	1	0	0	CCITT V.21 Orig Loopback
1	0	1	0	1	CCITT V.21 Ans Loopback
1	0	1	1	0	CCITT V.23 Mode 2 Main Loopback
1	0	1	1	1	CCITT V.23 Mode 2 with Equalizer Loopback
1	1	0	0	0	CCITT V.23 Mode 1 Main Loopback
1	1	0	0	1	CCITT V.23 Back Loopback
1	1	0	1	0	
1	1	0	1	1	
1	1	1	0	0	Reserved
1	1	1	0	1	
1	1	1	1	0	
1	1	1	1	1	

Figure 1 : Loopback Configurations.



THEORY OF OPERATION

The EF7910 MODEM consists of three main sections, shown in the block diagram - Transmitter, Receiver, and Interface Control.

TRANSMITTER (modulator)

The transmitter, shown in figure 2 receives binary digital data from a source such as a UART and converts the data to an analog signal using frequency shift keying (FSK) modulation. This analog signal is applied to the phone line through a DAA or acoustic coupler. FSK is a modulation technique which encodes one bit per baud. A logic one applied to the TRANSMITTED DATA (TD) input causes a sine wave at a given frequency to appear at the analog TRANSMITTED CARRIER (TC) output. A logic zero applied to input TD causes a sine wave of a different frequency to appear at the TC output. As the data at the TD input switches between logical one and zero, the TC output switches between the two frequencies. In the EF7910 this switching between frequencies is phase continuous. The frequencies themselves are digitally synthesized sine functions.

The frequencies for each modem configuration available in the EF7910 are listed in table 3a.

The process of switching between two frequencies as in FSK generates energy at many more frequencies than the two used in the modulation. All the transmitted information can be recovered from a frequency band B Hz wide, where B is the bit rate or maximum rate of change of the digital data at the TD input. This band is centered about a frequency, f_C,

where $f_C = f_1 + (f_2 - f_1)/2$

(f_1 = lower of two FSK frequencies)

(f_2 = higher of two FSK frequencies)

In addition to this primary information band, there exist side bands containing redundant information. It is desirable to attenuate these bands for two reasons :

1. The phone companies have specifications on the amount of energy allowed in certain frequency bands on the line.
2. If two independent information channels are present simultaneously on the line (e.g. 300 bps full duplex or 1200 bps half duplex with back), the redundant transmitter components may fall in the frequency band of the local receiver channel and interfere with detection. In the EF7910 these redundant and undesirable components are attenuated by digital bandpass filters.

Following the digital bandpass filters, the filtered FSK signal is converted to an analog signal by an on-chip DAC operating at a high sample rate. This analog FSK signal is finally smoothed by a simple on-chip analog low pass filter.

RECEIVER (demodulator)

A simplified block diagram of the EF7910 FSK receiver is shown in Figure 3. Data transmitted from a remote site modem over the phone line is an FSK-modulated analog carrier. This carrier is applied to the RECEIVED CARRIER (RC) pin via a DAA or acoustic coupler. The first stage of the demodulator is a simple on-chip analog low pass anti-alias filter. The output of this is converted into digital form and filtered by digital bandpass filters to improve the signal to noise ratio and reject other independent channel frequencies associated with the phone line in the case of full duplex configuration. The bandpass filtered output is digitally demodulated to recover the binary data. A carrier detect signal is also digitally extracted from the received line carrier to indicate valid data.

Figure 2 : Transmitter Block Diagram.

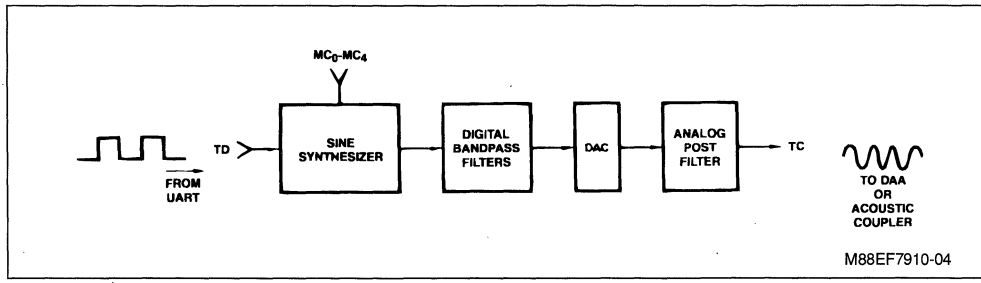
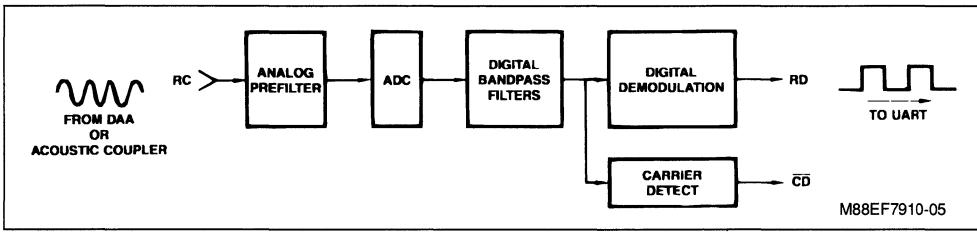


Figure 3 : Receiver Block Diagram.



INTERFACE CONTROL

This section controls the handshaking between the modem and the local terminal. It consists primarily of delay generation counters, two state machines for controlling transmission and reception, and mode control decode logic for selecting proper transmit frequencies and transmit and receive filters according to the selected modem type. Inputs and outputs from this section are as follows :

REQUEST TO SEND (Main and Back)
CLEAR TO SEND (Main and Back)
CARRIER DETECT (Main and Back)
RING
MC0-MC4
DATA TERMINAL READY

Internal logic clamps protocol signals to different levels under certain conditions (e.g., initial conditions).

When Bell 103/113 and V.21 modem configurations are selected, the back channel signals are non-functional.

Figures 6 and 7 depict the sequencing of the two state machines. State machine 1 implements main or back channel transmission and the auto-answer sequence. State machine 2 implements reception on main or back channel.

The state machine powers on to the state labelled INITIAL CONDITIONS. Handshake signals are set to or assumed to be the levels listed in table 2. The machine then waits for DATA TERMINAL READY (DTR) to be turned on. Whenever DTR is turned to the OFF state from an ON condition, each state machine and external signals return to the initial conditions within 25 microseconds. After DTR is turned ON the EF7910 becomes operational as a modem and the state machines proceed as depicted in the flowcharts.

The definitions of the terms Full Duplex and Half Duplex used in these flowcharts are depicted below (figs. 4 and 5). "Full Duplex" applies to all 103/113, V.21 modes. "Hall Duplex" applies to 202 and V.23, both forward and backward channel.

Full Duplex : Data can be transmitted and received simultaneously at a rate of 300 baud. Two independent 300 Hz channels are frequency multiplexed into the 3000 Hz bandwidth of the phone line. The EF7910 configurations for the Bell 103/113 and CCITT V.21 can be operated full duplex.

Half Duplex : In half duplex with back channel, the modem may transmit at 1200/600 baud and receive at 5/75 baud. Alternatively it may transmit at 5/75 baud and receive at 1200/600 baud. Examples are Bell 202 and CCITT V.23.

Table 2 : Initial Conditions

Data Terminal Ready (DTR)	OFF
Request to Send (RTS)	OFF
Clear to Send (CTS)	OFF
Transmitted Data (TD)	Ignored
Back Channel Request to Send (BRTS)	OFF
Back Channel Clear to Send (BCTS)	OFF
Back Channel Transmitted Data (BTD)	Ignored
Ring (RING)	OFF
Carrier Detect (CD)	OFF
Received Data (RD)	MARK
Back Channel Carrier Detect (BCD)	OFF
Back Channel Received Data (BRD)	MARK

Figure 4 : Full Duplex.

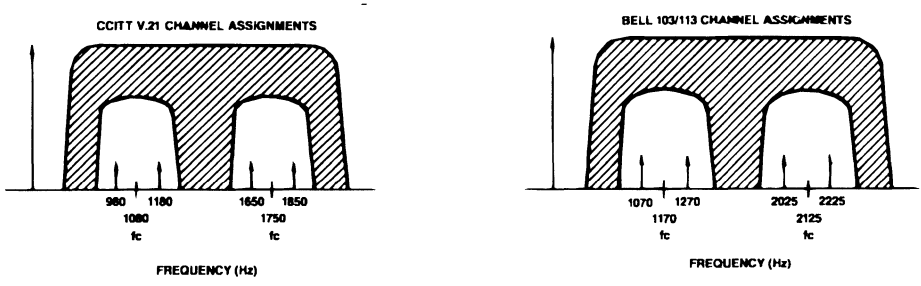


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Figure 5 : Half Duplex.

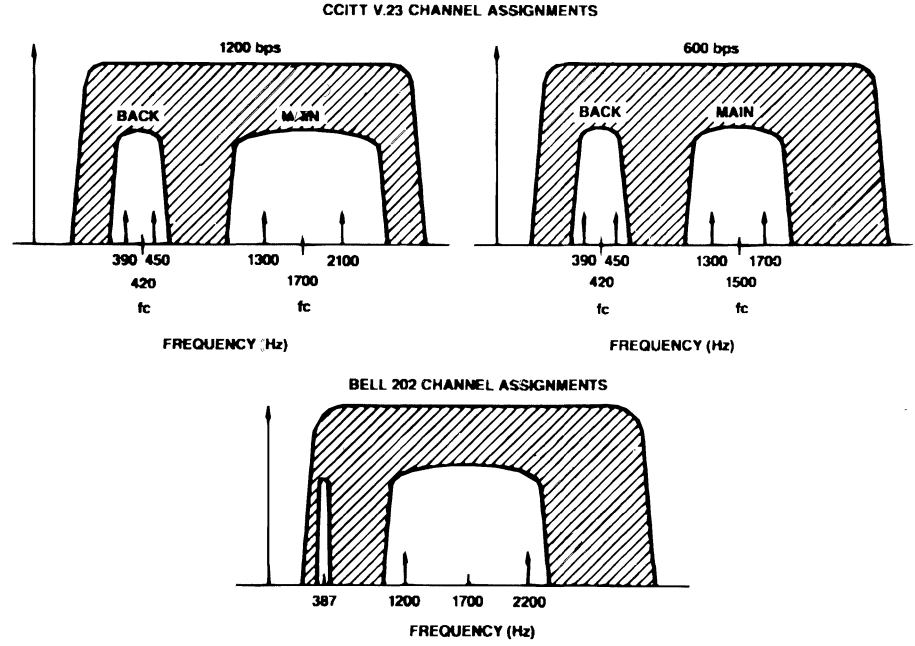

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Table 3 (a) : Frequency Parameters.

Modem	Baud Rate (BPS)	Duplex	Transmit Frequency		Receive Frequency		Answer Tone Freq. Hz
			Space Hz	Mark Hz	Space Hz	Mark Hz	
Bell 103 Orig	300	Full	1070	1270	2025	2225	
Bell 103 Ans	300	Full	2025	2225	1070	1270	2225
CCITT V.21 Orig	300	Full	1180	980	1850	1650	
CCITT V.21 Ans	300	Full	1850	1650	1180	950	2100
CCITT V.23 Mode 1	600	Half	1700	1300	1700	1300	2100
CCITT V.23 Mode 2	1200	Half	2100	1300	2100	1300	2100
CCITT V.23 Mode 2 Equalized	1200	Half	2100	1300	2100	1300	2100
Bell 202	1200	Half	2200	1200	2200	1200	2025
Bell 202 Equalized	1200	Half	2200	1200	2200	1200	2025
CCITT V.23 Back	75		450	390	450	390	
Bell 202 Back	5		*	*	**	**	

* ($\overline{\text{BRTS}}$ LOW) and (BTD HIGH) : 387 Hz at TC
* (BRTS HIGH) or (BTD LOW) : 0 volt at TC
* Meets new CCITT R20 frequency tolerance.
** 387 Hz at RC : $\overline{\text{BCD}}$ LOW
** No 387 Hz at RC : $\overline{\text{BCD}}$ HIGH
Frequency tolerance is less than ± 0.4 Hz with 2.4576 MHz Crystal. Except Bell 202 which is + 1 Hz (1200 Hz, mark).

Table 3 (b): Timing Parameters (refer to figures 9, 10 and 11 for timing diagrams).

Symbol	Description	Bell 103 Orig	Bell 103 Ans	Bell 202	Bell 202 EQ	Bell 202 Back	Unit
$t_{RC\ (on)}$	Request-to-Send to Clear-to-Send ON Delay	208.3	208.3	183.3	183.3		msec ± 0.3 %
$t_{RC\ (off)}$	Request-to-Send to Clear-to-Send OFF Delay	0.5	0.5	0.5	0.5		msec ± 0.25 %
$t_{BRC\ (on)}$	Back Channel Request-to-Send to Clear-to-Send ON Delay						msec ± 0.64 %
$t_{BRC\ (off)}$	Back Channel Request-to-Send to Clear-to-Send OFF Delay						msec ± 25 %
$t_{CD\ (on)}$	Carrier Detect ON Delay	94-106	94-106	18-22	18-22		msec
$t_{CD\ (off)}$	Carrier Detect OFF Delay	21-40	21-40	12.4-23.4	12.4-23.4		msec
$t_{BCD\ (on)}$	Back Channel Carrier Detect ON Delay					17-25	msec
$t_{BCD\ (off)}$	Back Channel Carrier Detect OFF Delay					21-38	msec
t_{AT}	Answer Tone Duration		1.9	1.9	1.9		sec ± 0.44 %
t_{SIL}	Silence Interval before Transmission	1.3	1.3	1.3	1.3		sec ± 0.64 %
t_{SQ}	Receive Squelch Duration			156.3	156.3		msec ± 3.3 %
t_{STO}	Transmitter Soft Turn-Off Duration			24	24		msec ± 2.3 %
t_{RI}	Minimum $\overline{\text{RI}}$ Low Duration		25	25	25		µS

Table 3 (c): (continued).

Symbol	Description	CCITT V.21 Orig	CCITT V.21 Ans	CCITT V.23 Mode 1	CCITT V.23 Mode 2	CCITT V.23 Mode 2 EQ	CCITT V.23 Back	Unit
$t_{RC\ (on)}$	Request-to-Send to Clear-to-Send ON Delay	400	400	208.3	208.3	208.3		msec ± 0.3 %
$t_{RC\ (off)}$	Request-to-Send to Clear-to-Send OFF Delay	0.5	0.5	0.5	0.5	0.5		msec ± 0.25 %
$t_{BRC\ (on)}$	Back Channel Request-to-Send to Clear-to-Send ON Delay						82.3	msec ± 0.64 %
$t_{BRC\ (off)}$	Back Channel Request-to-Send to Clear-to-Send OFF Delay						0.5	msec ± 25 %
$t_{CD\ (on)}$	Carrier Detect ON Delay	301-312	301-312	11.4-15.4	11.4-15.4	11.4-15.4		msec
$t_{CD\ (off)}$	Carrier Detect OFF Delay	21-40	21-40	5.4-13.3	5.4-13.3	5.4-13.3		msec
$t_{BCD\ (on)}$	Back Channel Carrier Detect ON Delay						17-25	msec
$t_{BCD\ (off)}$	Back Channel Carrier Detect OFF Delay						21-38	msec
t_{AT}	Answer Tone Duration		3.0	3.0	3.0	3.0		sec ± 0.44 %
t_{SIL}	Silence Interval before Transmission	1.9	1.9	1.9	1.9	1.9		sec ± 0.64 %
t_{SQ}	Receiver Squelch Duration			156.3	156.3	156.3		msec ± 3.3 %
t_{STO}	Transmitter Soft Turn-Off Duration							msec ± 2.3 %
t_{RI}	Minimum $\overline{RI}$ Low Duration		25	25	25	25		µS

CALL ESTABLISHMENT

Before two modems can exchange data, an electrical connection through the phone system must be established. Although it may assist in call establishment, a modem typically does not play a major role. A call may be originated manually or automatically and it may be answered manually or automatically.

Manual Calling - Manual calling is performed by a person who dials the number, waits for an answer, then places the calling modem into data transmission mode.

Automatic Calling - Automatic calling is typically performed by an automatic calling unit (ACU) which generates the appropriate dialing pulse or dual-tone sequence required to call the remote (called) modem. The ACU also has the ability to detect an answer tone from the called modem and place the calling modem into data transmission mode.

Manual Answering - Manual answering is performed by a person who hears the phone ring, lifts the receiver, causes the called modem to send an answer tone to the calling modem, and places the called modem into data transmission mode.

Automatic Answering - Automatic answering is performed by a called modem with a data access arrangement (DAA). The DAA detects a ringing signal, takes the phone circuit off-hook (corresponding to lifting the receiver) and instructs the called modem to commence the auto-answer sequence. Next the called modem sends out silence on the line, followed by an answer tone. When this tone is detected

by the calling modem, the connection is considered to have been established.

The EF7910 provides assistance for automatic answering through the RING signal as follows. Observe the upper right-hand portion of Figure 6 (a). Assume that DATA TERMINAL READY (DTR) has recently been asserted to cause exit from the initial conditions. Note that if DTR remains OFF, RING is ignored. Assume also that RTS and BRTS are OFF and that the mode control lines (MC0-MC4) select a normal modem configuration, not a loopback mode. Automatic answering is initiated by receipt of a LOW level at the RING input, causing entrance to the auto-answer sequence depicted in Figure 6 (c).

The EF7910 outputs silence (0.0 volt) at its TRANSMITTED CARRIER (TC) output for a time, t_{SIL}, followed by the answer tone for a time, t_{AT}. The CARRIER DETECT (CD) pin is clamped OFF and the RECEIVED DATA (RD) signal is therefore clamped to a MARK (HIGH) during the auto-answer sequence. Upon completion of the answer tone, CD is released. If the mode lines (MC0-MC4) select a 202 or V.23 mode, the transmit filters are set to the forward channel and the receive filters are set to the back channel during the auto answer sequence.

At the end of the auto-answer sequence, return is made to point A in the loop at the upper right-hand portion of Fig. 6 (a). Note that since the answer flag has been set, the auto-answer sequence cannot be entered again unless DTR is first turned OFF, then ON. At this point the phone line connection has been established and data transmission or reception may begin.

The RING input may be activated from a conditioned DAA Ring indicator output for automatic answering or it may be activated by a switch for manual answering. Tying RING HIGH will disable the auto-answer function of the EF7910.

DATA TRANSMISSION

FULL DUPLEX. Following call establishment, full duplex data transmission can be started by either the called or calling modem. In other words, if the connection has been established and the modem is looping through point A in figure 6 (a), it no longer matters which is the called and which is the calling modem. Data transmission is initiated by asserting REQUEST TO SEND (RTS). At this time the TRANSMITTED DATA (TD) input will be released and a modulated carrier can appear at the TRANSMITTED CARRIER (TC) output. Following a delay, t_{RCON}, CLEAR TO SEND (CTS) will turn ON. At this time, data may be transmitted through the TD input. It is a common protocol for the user to always present a MARK at the TD input before RTS is asserted and during the t_{RCON} delay.

Data transmission continues until RTS is turned OFF. Following a short delay, t_{RCOFF}, CTS turns OFF. As soon as RTS goes OFF, the TD input is ignored and the TC output is set to 0.0 volt (silence). After CTS turns OFF, the state machine returns to point A in Figure 6 (a).

HALF DUPLEX. When a half duplex mode is selected (202 or V.23), data transmission can be either on the main channel at 1200/600 baud or on the back channel at 5/75 baud. In normal half duplex operation a single modem is either transmitting on the main and receiving on the back channel or vice versa. In the EF7910 control of the transmitter and receiver filters to the proper channel is performed by RTS. When RTS is asserted, the transmitter filters and synthesizer are set to transmit on the main channel ; the receiver filters are set to receive on the back channel. Therefore, whenever RTS is on, BRTS should not be asserted since the transmitter cannot be used for the back channel. When RTS is OFF and a half duplex mode is selected, the transmitter filters and synthesizer are set to the back channel ; the receiver filters are set to the main channel. If RTS and BRTS are asserted simultaneously, RTS will take precedence. However, if BRTS is asserted before RTS and the back channel data transmission sequence has been entered (Figure 6 (b)), RTS will be ignored until BRTS is turned OFF.

The state machine sequences for main and back channel transmission differ slightly and are depicted in figure 6. Assume the state machine is idling through point A in Figure 6 (a).

MAIN CHANNEL. This transmission sequence is entered if a 202 or V.23 mode is selected and RTS is asserted. Since the receiver is now forced to the back channel, the RECEIVED DATA (RD) signal is clamped to a MARK ; and the CARRIER DETECT signal is clamped OFF. The TRANSMITTED DATA input (TD) is released and a carrier appears at the TRANSMITTED CARRIER output which follows the MARK/SPACE applied to TD. RTS turning ON initiates a delay, t_{RCON}, at the end of which the CLEAR TO SEND (CTS) output goes LOW. When CTS goes LOW data may be transmitted through input TD. Data transmission continues until RTS is turned OFF. At this time several events are initiated. First a delay, t_{RCOFF}, is initiated at the end of which CTS turns OFF. The TD input is ignored as soon as RTS goes OFF. If a 202 mode is selected, a soft turn-off tone appears at the TC output for a time, t_{STO}, followed by silence (0.0 volt). For both 202 and V.23 modes a squelch period, t_{SQ}, is initiated when RTS

goes OFF. During this period the $\overline{CD}$ output is clamped OFF, forcing the RD output to a MARK condition. The squelch period begins as soon as $\overline{RTS}$ goes OFF and thus overlaps both t_{RCOFF} and t_{STO}. At the end of the squelch period, the state machine returns to the idle loop at point A in Figure 6 (a).

The reasons for squelch and soft-turnoff are as follows :

Soft Turn-Off : When $\overline{RTS}$ is turned OFF at the end of a message, transients occur which may cause spurious space signals to be received at a remote modem. During soft turn-off the modem transmits a soft carrier frequency for a period, t_{STO}, after $\overline{RTS}$ is turned OFF. This results in a steady MARK on the RECEIVED DATA (RD) line of the remote modem.

Squelch : The local receiver must be turned OFF after $\overline{RTS}$ is OFF, until the start of carrier detect, so that the line transients are not demodulated. The process of disabling the receiver after $\overline{RTS}$ is turned OFF is called squelching.

BACK CHANNEL. This transmission sequence, shown in Figure 6 (b), is entered if a 202 or V.23 mode is selected, $\overline{RTS}$ is OFF, and $\overline{BRTS}$ is asserted. The BACK CARRIER DETECT (BCD) output is forced OFF and the BACK RECEIVED DATA (BRD) output is clamped to a MARK. The BACK TRANSMITTED DATA input (BTD) is released and a carrier appears at the TC output which follows the MARK/SPACE applied to BTD. Turning on $\overline{BRTS}$ initiates a delay, t_{BRCON}, at the end of which the BACK CLEAR TO SEND ($\overline{BCTS}$) output goes LOW. When $\overline{BCTS}$ goes LOW data may be transmitted through input BTD. Data transmission continues until $\overline{BRTS}$ is turned OFF. The input BTD is immediatly ignored and the TC output is silenced (set to 0.0 volt). Following a short delay, t_{BRCOFF}, the output $\overline{BCTS}$ goes OFF. The signals BCD and BRD are released and the state machine returns to idle at point A of figure 6 (a).

In 202 back channel mode, BTD should be tied HIGH. Then $\overline{BRTS}$ controls the ON/OFF keying modulation. When $\overline{BRTS}$ is LOW, 387 Hz appears at the TC output ; when $\overline{BRTS}$ is HIGH, 0 volt appears at TC.

DATA RECEPTION

Data reception is controlled by state machine 2 and depicted in figure 7. At power on the machine enters initial conditions and remains there until DTR is asserted. If then loops until either CARRIER DETECT (CD) or BACK CARRIER DETECT (BCD) occurs.

FULL DUPLEX. In full duplex data reception, $\overline{CARRIER\ DETECT}$ may appear at any time after the phone connection has been established. Reception is independent of transmission. When the receiver detects a valid carrier for at least a time, t_{CDON}, the output $\overline{CD}$ is turned ON, the RECEIVED DATA (RD) output is released, and valid data can be obtained at RD. Data is received until the receiver detects loss of carrier for at least a time, t_{CDOFF}. At this time the $\overline{CD}$ output is turned OFF and RD is clamped to a MARK. The state machine returns to the idle loop at point E.

HALF DUPLEX. As discussed in the data transmission section above, when a half duplex mode has been selected, the signal $\overline{RTS}$ controls whether the main channel is transmitting or receiving. The back channel can only do the opposite from the main. If $\overline{RTS}$ is OFF, then $\overline{CARRIER\ DETECT}$ may be asserted and the data reception sequence is identical to that discussed above for full duplex reception. As long as $\overline{RTS}$ remains OFF, $\overline{BACK\ CARRIER\ DETECT}$ will never be asserted. If $\overline{RTS}$ is ON, then $\overline{CARRIER\ DETECT}$ will never be asserted. Instead the receiver will look for a valid carrier in the back channel frequency band. If a valid carrier exists for at least a time, t_{BCDON}, the output BACK CARRIER DETECT (BCD) is turned ON, the BACK RECEIVED DATA (BRD) output is released and valid data can be obtained at BRD. Data is received until the receiver detects loss of back channel received signal for at least time, t_{BCDOFF}. At this time the $\overline{BCD}$ output is turned OFF. Data output, $\overline{BRD}$, is clamped to a MARK if a V.23 mode is selected. For 202 back channel mode, $\overline{BCD}$ represents the received data. The BRD output can be ignored. The state machine returns to the idle loop at point E.

LOOPBACK

Ten modes exist to allow both analog and digital loopback for each modem specification met by the EF7910. When a loopback mode is selected, the signal processing (filters, etc.) for both the transmitter and receiver is set to process the same channel or frequency band. This allows the analog output, TRANSMITTED CARRIER, and the analog input, RECEIVED CARRIER, to be connected for local analog loopback. Alternatively the digital data signals, TD and RD or BTD and BRD, can be connected externally, allowing a remote modem to test the local modem with its digital data signals looped back.

When a loopback mode is selected, the state machine sequences are altered slightly. First, autoanswer is disabled. Second, if a half duplex loopback mode is selected (202 or V.23), the local $\overline{CARRIER\ DETECT/BCD}$ is not forced OFF when $\overline{RTS/BRTS}$ is asserted.

Figure 6 (a) : Transmit Main Channel State Diagram.

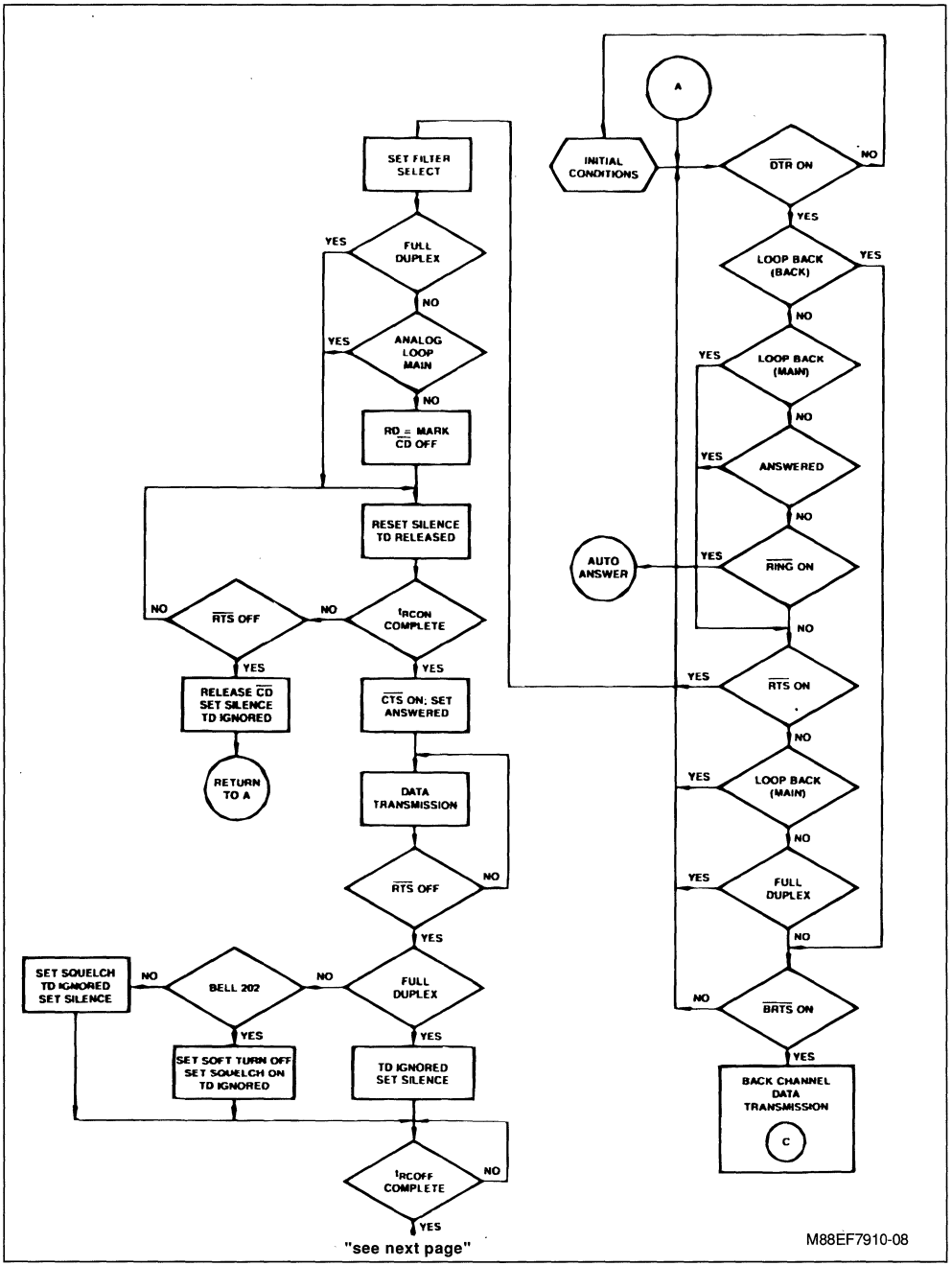

Figure 6 (a) : Transmit Main Channel State Diagram (continued).

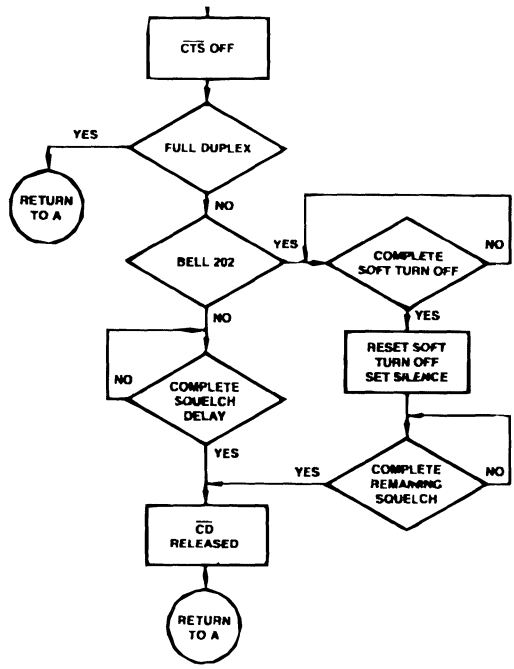

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Figure 6 (b) : Transmit Back Channel State Diagram.

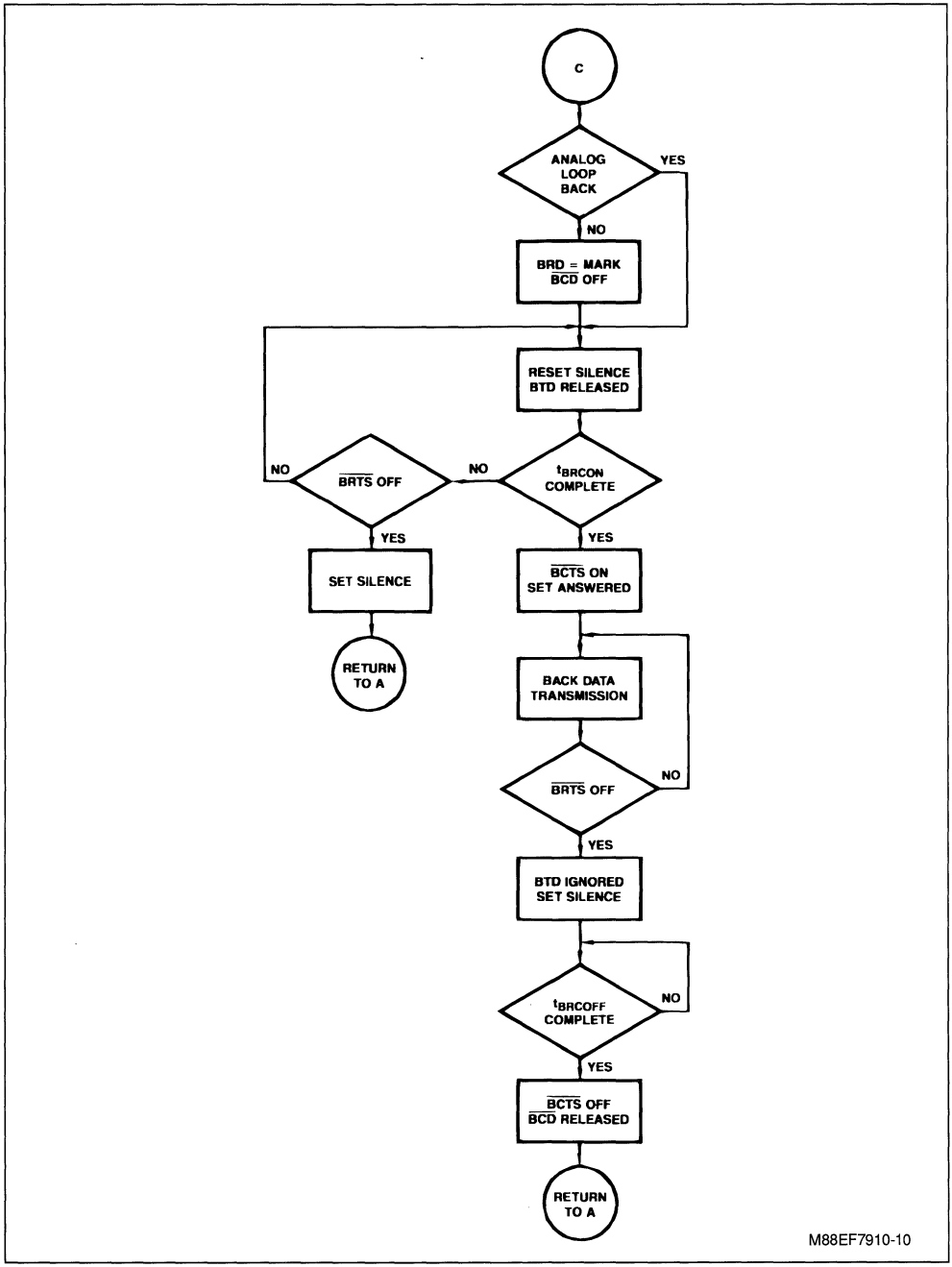

Figure 6 (c) : Auto Answer State Diagram.

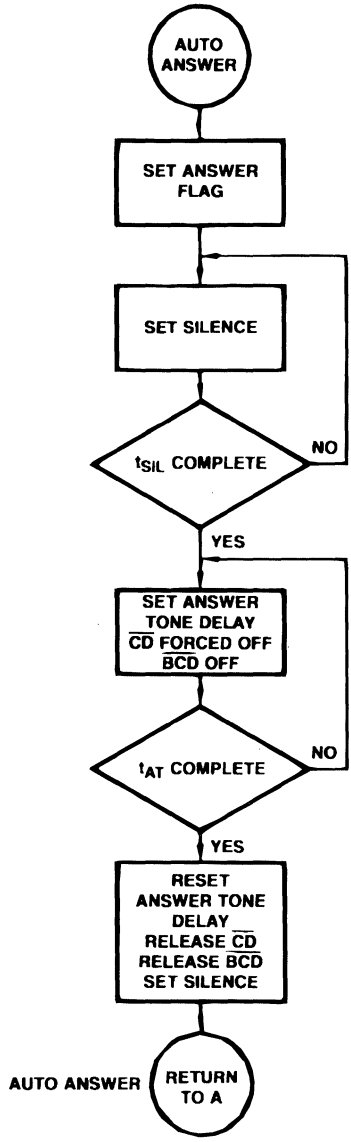

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Figure 7 : Receiver Main/Back Channel State Diagram.

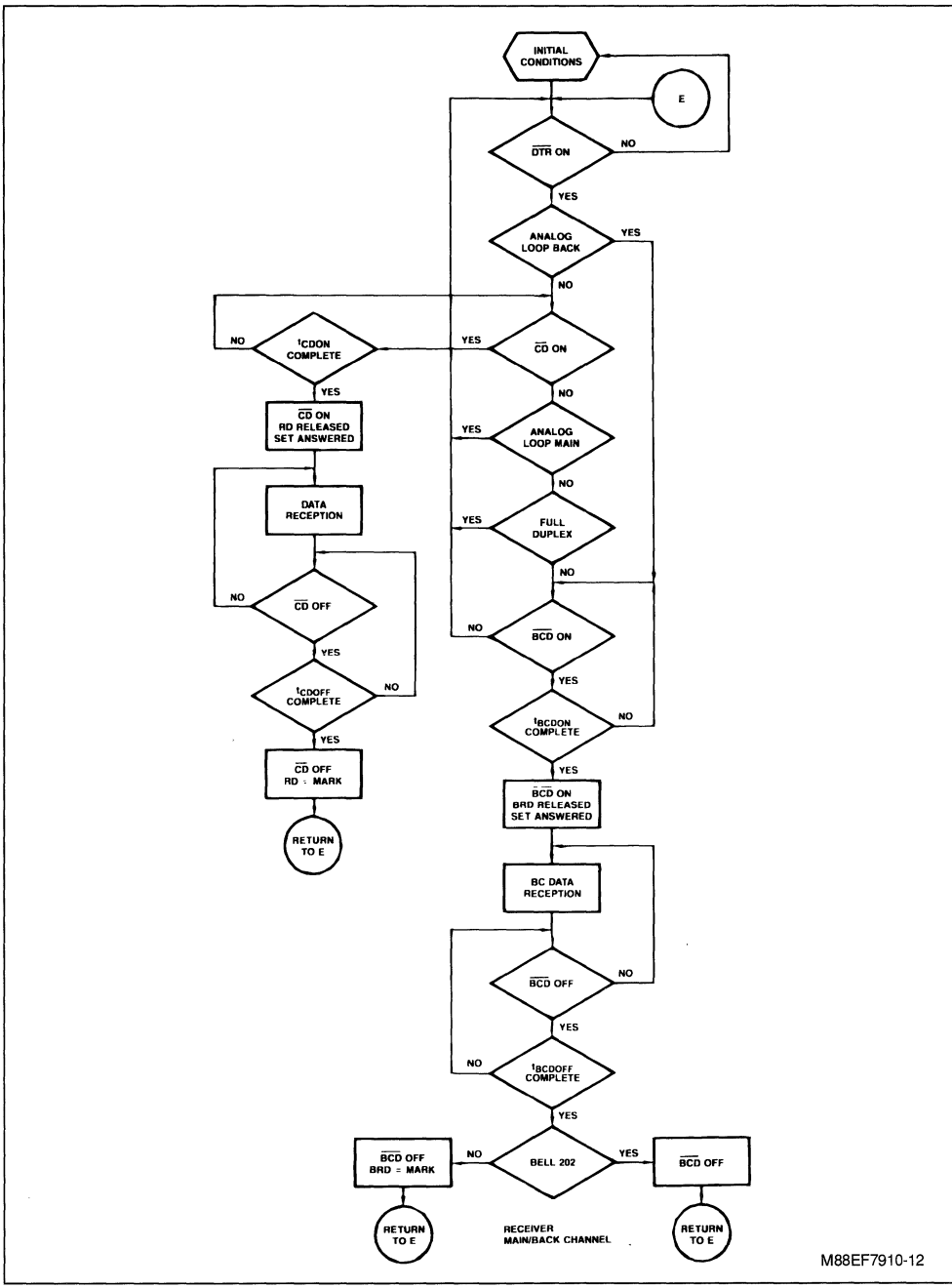


Figure 8 : BELL 202 Handshake Timing.

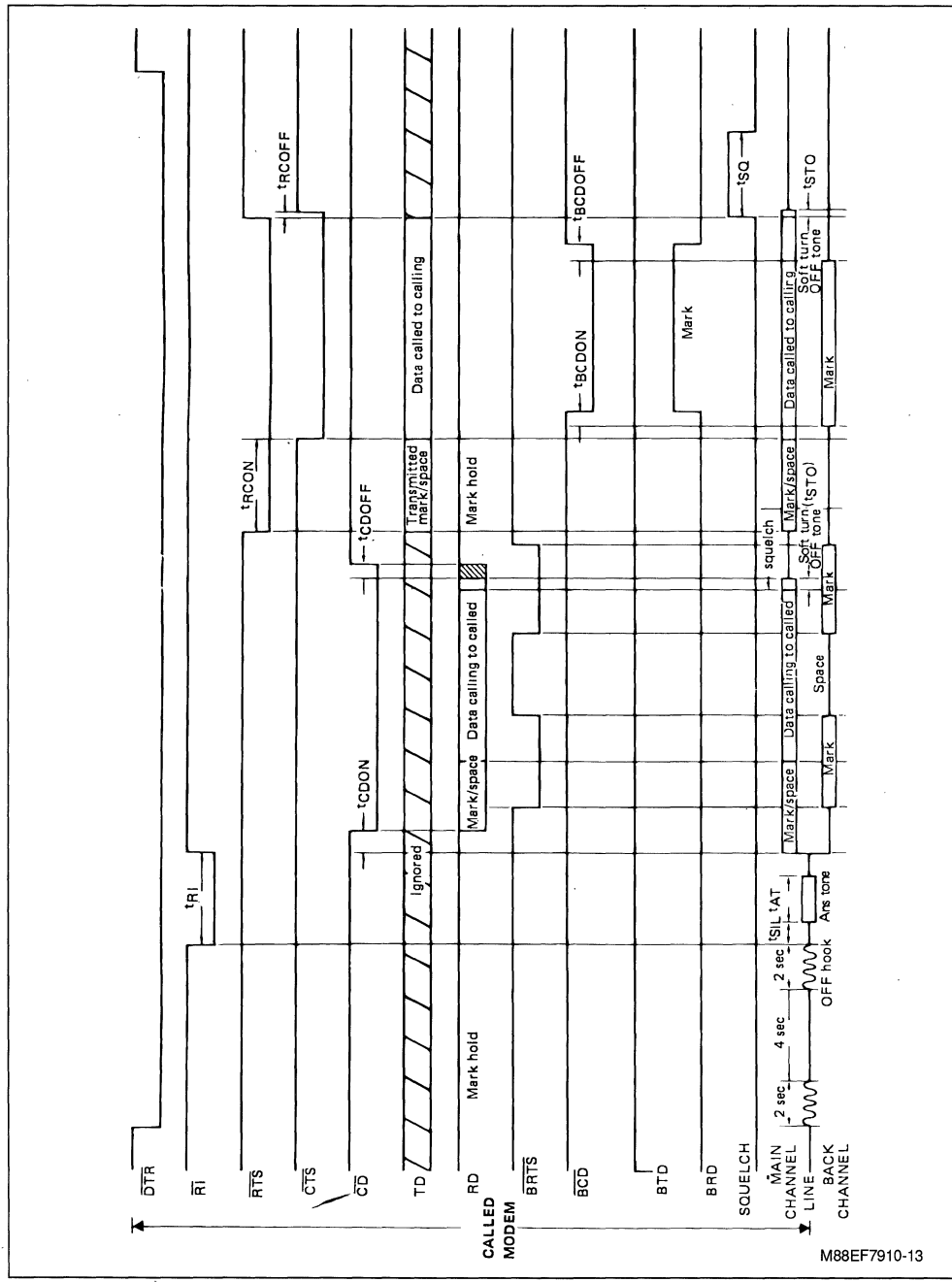


Figure 8 : BELL 202 Handshake Timing (continued).

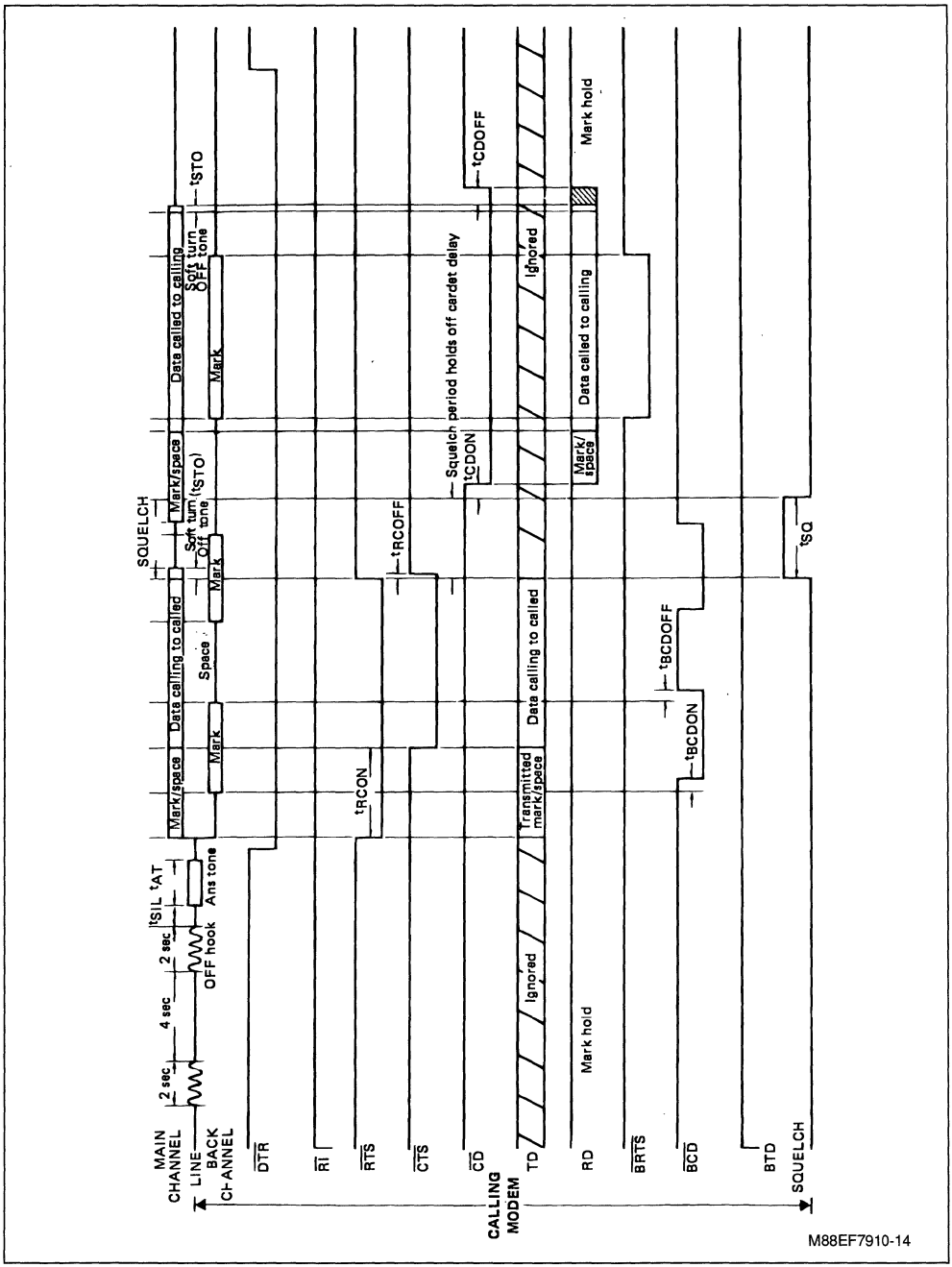


Figure 9 : CCITT V.23 Handshake Timing.

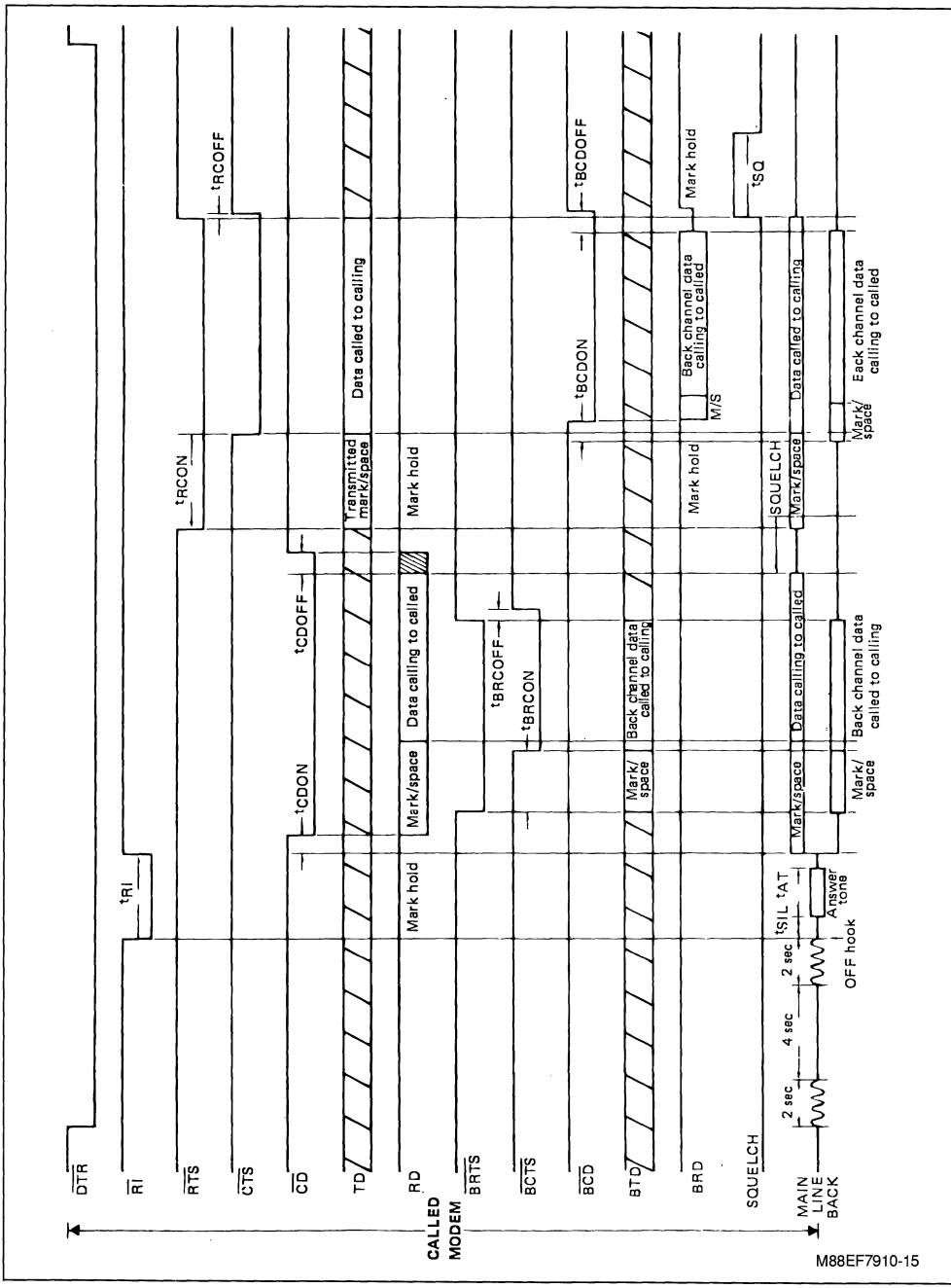


Figure 9 : CCITT V.23 Handshake Timing (continued).

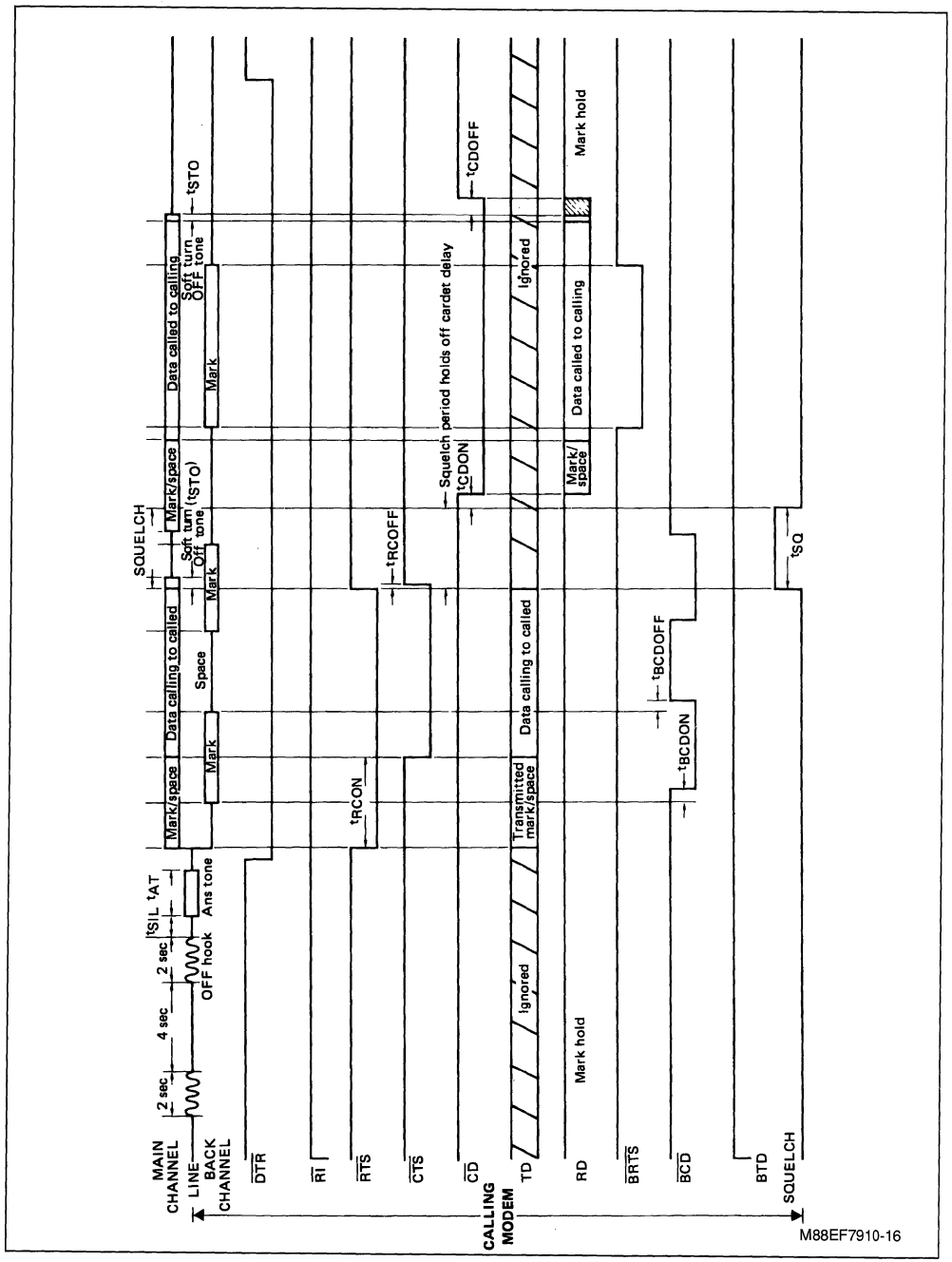
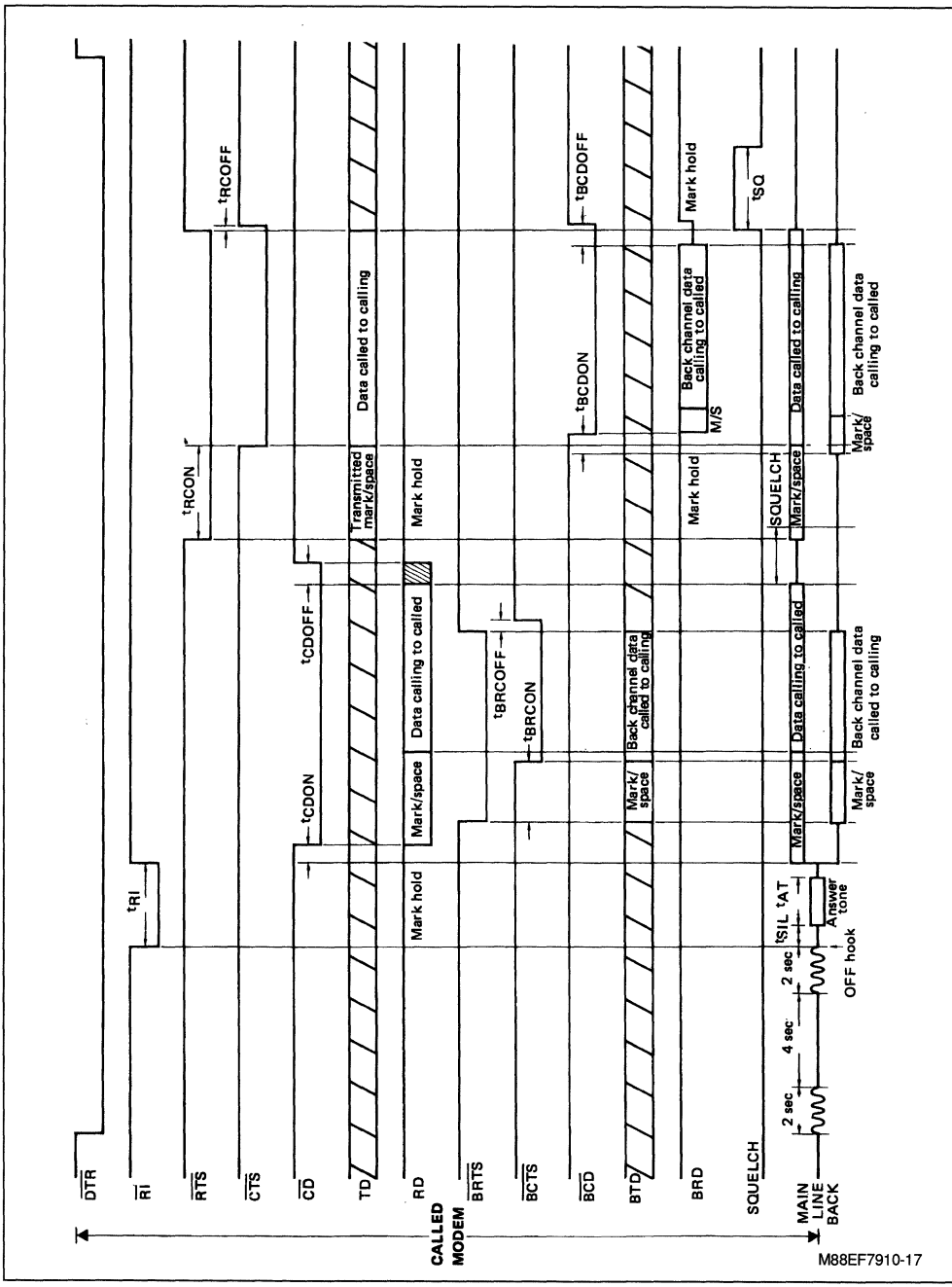


Figure 10 : BELL 103/CCITT V.21 Handshake Timing.



The 202 and V.23 main loopback modes allow use in a 4-wire configuration at 1200 bps.

CLOCK GENERATION

Master timing of the modem is provided by either a crystal connected to the $XTAL_1$ and $XTAL_2$ inputs or an external clock applied to the $XTAL_1$ input.

CRYSTAL.

When a crystal is used it should be connected as shown in figure 11. The crystal should be a parallel resonance type, and its value must be 2.4576 MHz ± 0.01 %. A list of crystal suppliers is shown below.

EXTERNAL CLOCK

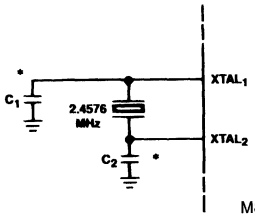
This clock signal could be derived from one of several crystal-driven baud rate generators. It should be connected to the $XTAL_1$ input and the $XTAL_2$ input must be left floating. The timing parameters required of this clock are shown in figure 11 and the values are listed in table 4.

Figure 11 : Clock Generation.

Crystal Information (f_C = 2.4576 MHz)

Manufacturer	P/N	C_1	C_2
M-Tron	MP-2	20 pF	20 pF
Monitor Products	MM-33	20 pF	20 pF

Note : Rise time of V_{CC} must be greater than 5 msec to insure proper crystal oscillator start-up.



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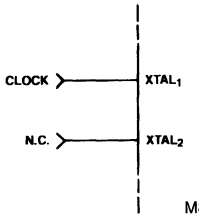

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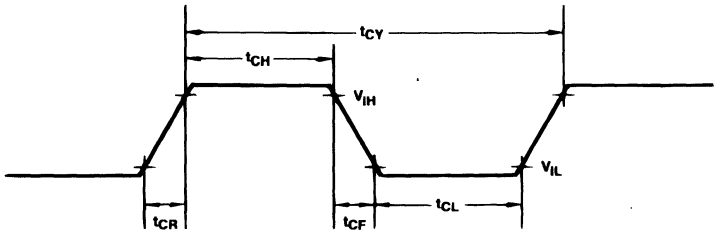
Capacitors values vary with different crystal manufacturers.



(b)

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Table 4 : Clock Parameters.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CY}	Clock Period	406.86	406.9	406.94	ns
t_{CH}	Clock High Time	165			ns
t_{CL}	Clock Low Time	165			ns
t_{CR}	Clock Rise Time			20	ns
t_{CF}	Clock Fall Time			20	ns

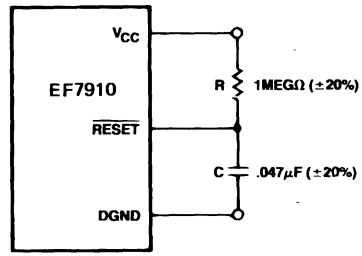
POWER ON RESET

The reset circuit operates in either of two modes.

AUTOMATIC RESET

In this mode an internal reset sequence is automatically entered when power is applied to the device. One resistor and one capacitor must be connected externally as shown in Figure 12. Values shown will work with most power supplies. Power supply (V_{CC}) rise time should be less than one half the RC time constant.

Figure 12 : Automatic Reset.



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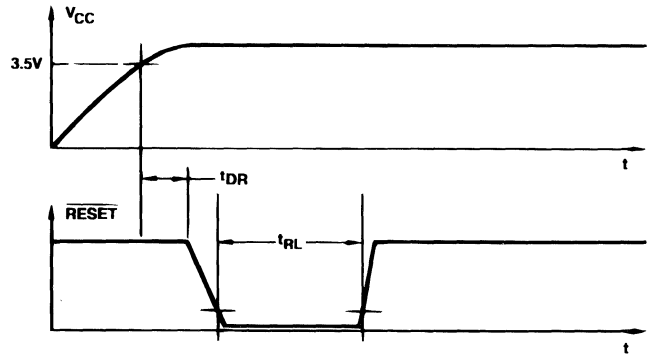
EXTERNAL RESET

In this mode the device may be forced into the reset sequence by application of an active LOW pulse applied to the $\overline{RESET}$ input. The reset must not be applied until the V_{CC} supply has reached at least 3.5 V. Timing is diagrammed in figure 13.

Figure 13 : External Reset.

TIMING DIAGRAMS



t_{DR} = delay from the time V_{CC} reaches 3.5 V and the falling edge of $\overline{RESET}$ signal (> 1 μs)
t_{RL} = $\overline{RESET}$ LOW duration time (> t_{MCK} = 406 ns)

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NOMINAL PERFORMANCE SPECIFICATIONS
TRANSMITTER (all modem types)

Input Data Format : Serial, asynchronous, standard TTL levels Modulation Technique :

Binary, phase-coherent Frequency Shift Keying (FSK)

TC Output Level : - 3 dBm into 600 Ω

Frequency Accuracy :

± 0.4 Hz all modems except Bell 202 (mark)
+ 1.0 Hz Bell 202 (mark)

Harmonics : – 45 dB from fundamental for single tones

Delay uncertainty for TD logic input change to TC frequency change : ≤ 8.3 µs

Out-of-band energy : see figure 14

RECEIVER

Output Data Format : Serial, asynchronous, TTL levels Demodulation Technique : Differential FM Detection
Sensitivity at Receiver Input : 0 dBm to - 48 dBm
Frequency Deviation Tolerance : ± 16 Hz
Carrier Detect Threshold :

ON	> – 40 dBm ± 1 dB
OFF	< – 43 dBm ± 1 dB
Hysteresis	> 2.5 dB

TEST MEASUREMENT SETUP

EF7910 performance is characterized using the test equipment setup shown in Figure 15. The HP1645A data error analyzer is used to generate 511-bit pseudo random binary sequences (PRBS) at D_{OUT} for testing the modem. The 1645A also receives and analyzes the 511-bit digital pattern at D_{IN} after it has progressed around the test loop. A reference transmitter converts the digital sequence generated by the HP1645A into an FSK signal. The FSK signal is typically adjusted to different levels from – 12 to – 45 dBm. The level-adjusted FSK signal or incident signal then passes through three pieces of equipment which comprise the telephone line simulator. The Wandel and Golterman TLN-1 and DLZ-4 simulate amplitude and group delay characteristics typical of a wide variety of phone lines. Line perturbations, such as amplitude hits and phase hits, may be injected by the Bradley 2A/2B.

The summing amplifier which drives the modem under test has three inputs. One of these inputs is the incident FSK signal which has been passed through a simulated phone line. The second input is from an optionally filtered noise source in order to simulate noise conditions which may be encountered on phone lines. The third input is from the transmitter of the EF7910 under test. This third input simulates the adjacent channel signal seen at the input of the EF7910 receiver due to the duplexer used on 2-wire lines. If 4-wire testing is being performed, the adjacent channel would not normally be included.

The HP3551A or HP3552A Transmission Test Set is used for measuring various levels which the modem under test is to receive. The levels of each of the three inputs to the summing amplifier should be measured independently of the other two inputs. For instance, the incident signal level should be measured by the transmission test set with no adjacent channel or noise present. The dashed line from the noise generator shows that the noise may or may not be measured at the output of the noise generator, depending on whether or not an optional filter is used, or on the characteristics of the filter.

Figure 14 : Out-of-band Transmitter Energy.

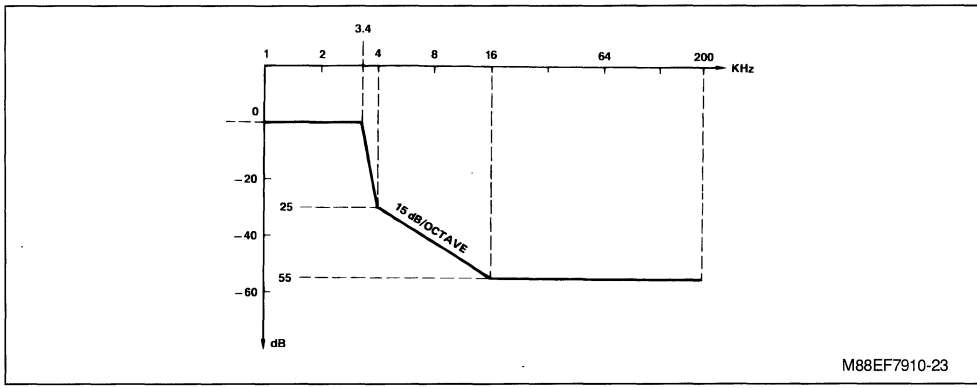
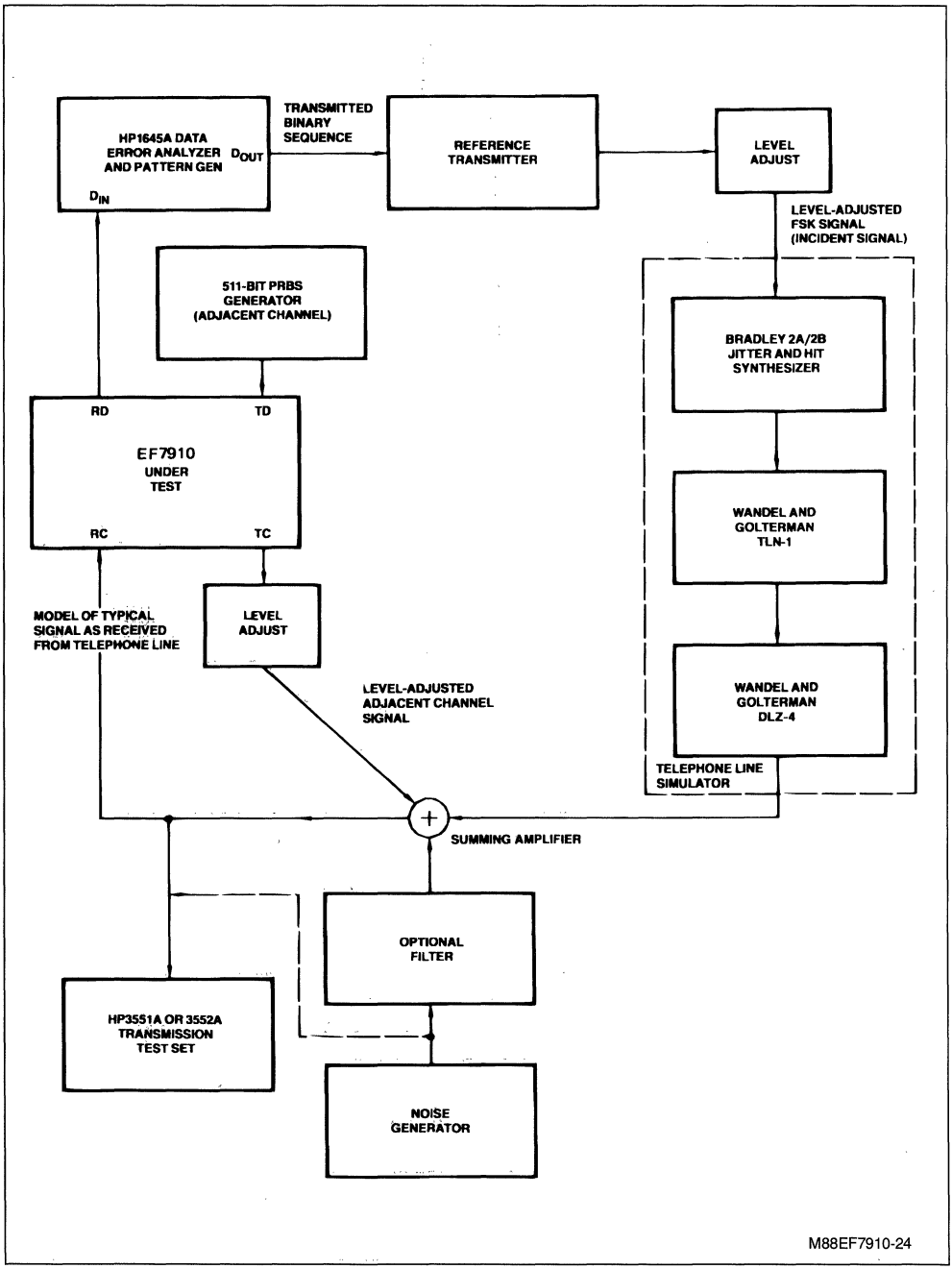
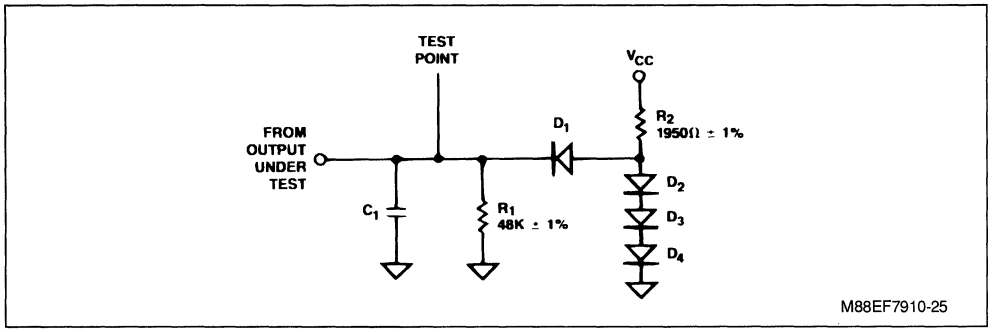


Figure 15 : BER and Distorsion Measurement Test Setup.



STANDARD LOAD CIRCUIT



Notes : 1. C_1 = 50 pF including stray and wiring capacitance.
2. All diodes are 1N3064 or equivalent.
3. All resistors are 1/8 watt.
4. V_{CC} = 5 volts ± 1 %.

APPLICATIONS

Figure 17 depicts a stand-alone EF7910 configuration. An op amp and three resistors provide a duplexor function to put the transmitter output into the line while receiving adjacent channel data from the line. Connection to the line is via a Data Access Arrangement (DAA). Note the lack of external analog filters. The TTL handshake signals may be level converted to RS-232, RS-422, or V.24 using appropriate devices. Mode control lines are hardwired or connected to switches.

Figure 18 depicts an application of the EF7910 with the SGS-THOMSON Microelectronics EF6805CT microcomputer. The duplexor/line interface is identical to the above configuration. However, the handshake signals interface directly with the UART included inside the EF6805CT. The mode control lines might also be controlled by the MCU while keeping the address and data bus of the EF6805CT available for customer applications. The main features of the EF6805CT are given at the end of this data sheet.

Figure 17 : Stand-Alone EF7910 Application.

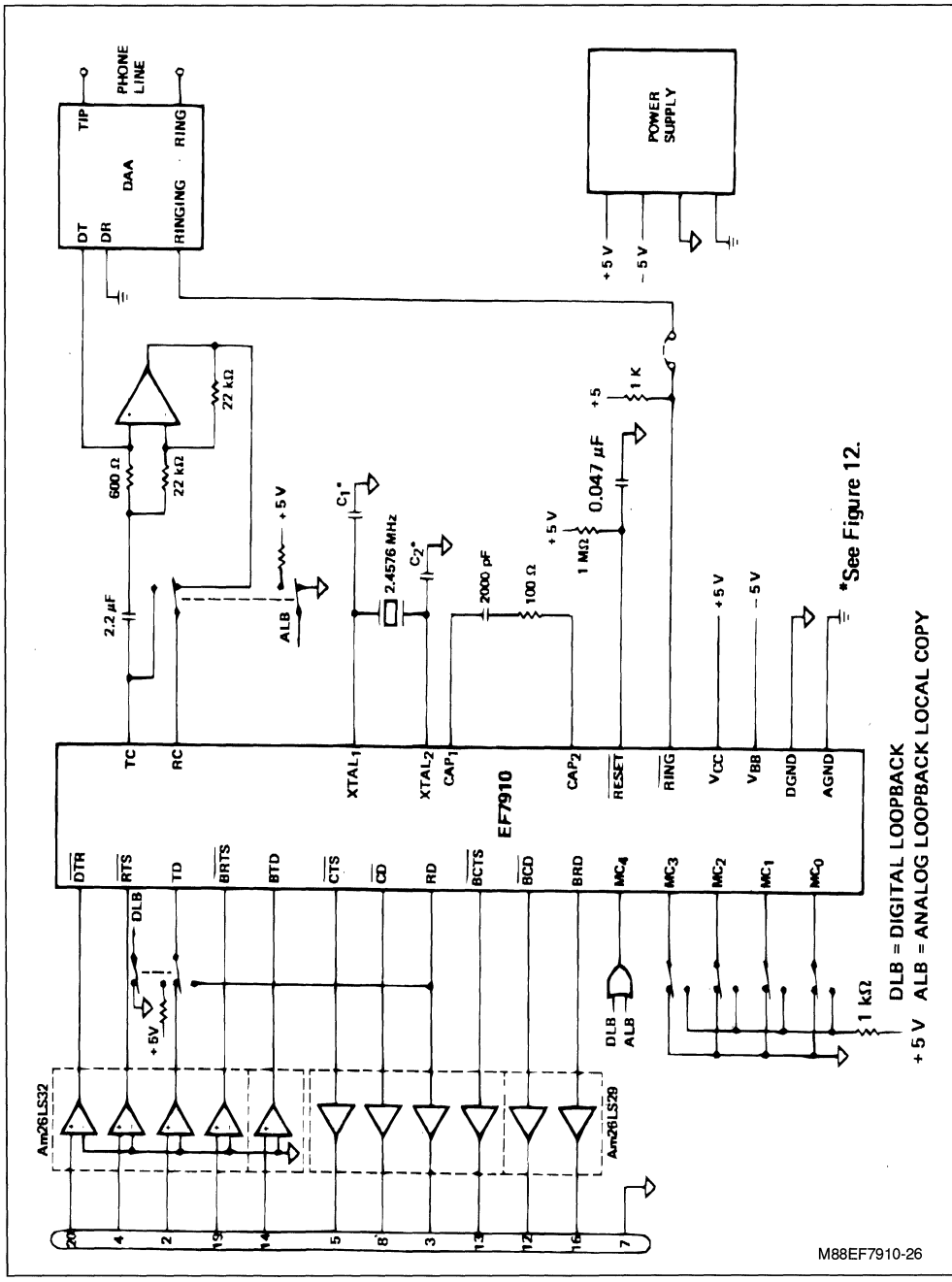
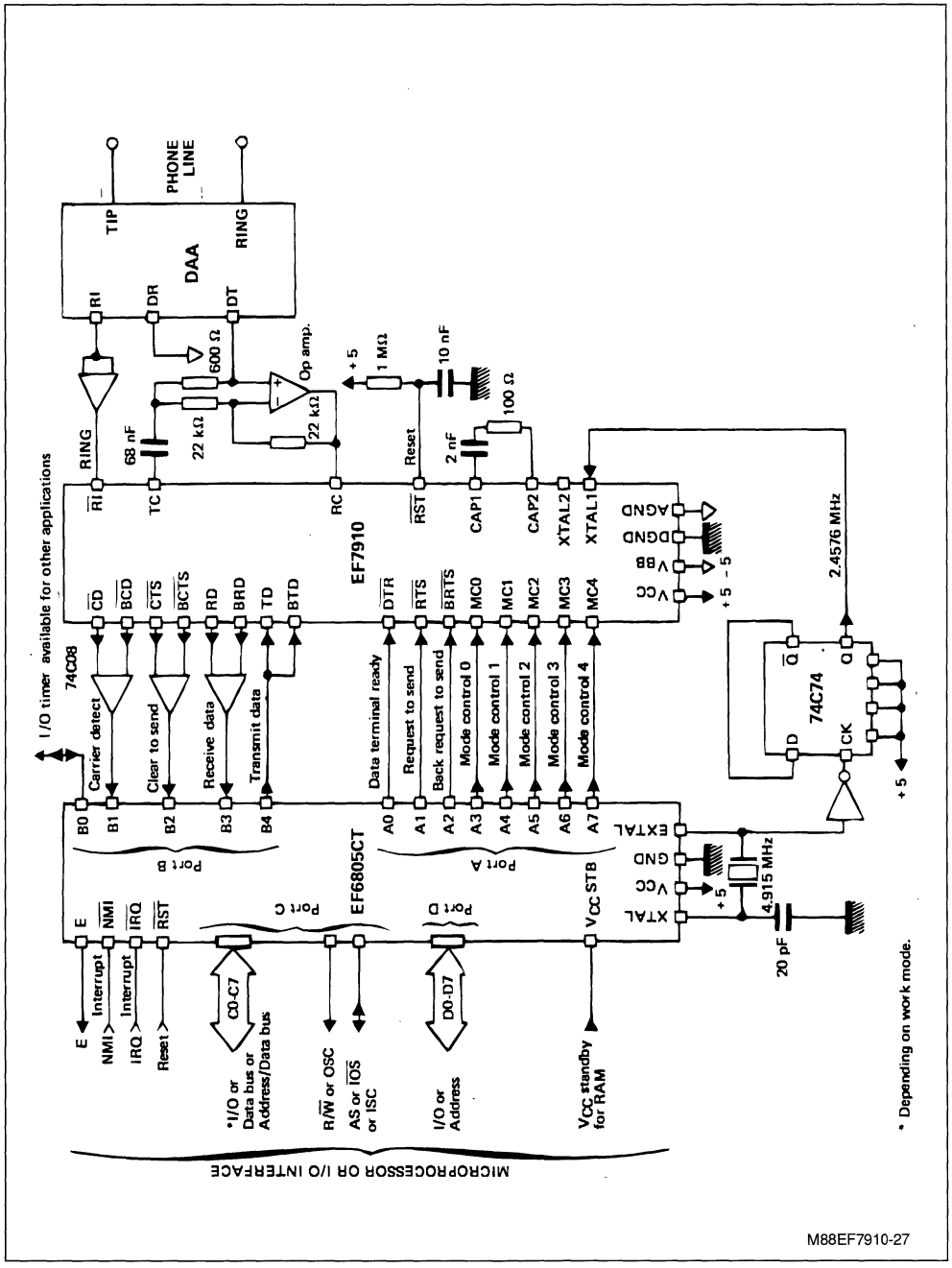


Figure 18 : Microprocessor Typical Application.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
T_{stg}	Storage Temperature	– 65 to + 125	°C
T_{amb}	Ambient Temperature under Bias	0 to + 70	°C
V_{CC}	V_{CC} with Respect to V_{DGND}	+ 6 / – 0.4	V
V_{BB}	V_{BB} with Respect to V_{DGND}	– 6 / + 0.4	V
	All Signal Voltages with Respect to V_{DGND}	± 5	V

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL DC CHARACTERISTICS over operating range, referred to V_{DGND}
$0\ °C \leq T_A \leq +\ 70\ °C$, $V_{CC} = +\ 5.0\ V \pm 5\ \%$, $V_{BB} = -\ 5.0\ V \pm 5\ \%$, $V_{AGND} = 0\ V \pm 50\ mV$, $V_{DGND} = 0\ V$
Digital Inputs : TD, $\overline{RTS}$, MC_0-MC_4, $\overline{DTR}$, $\overline{RING}$, BTD, $\overline{BRTS}$
Digital Outputs : RD, $\overline{CTS}$, $\overline{CD}$, BRD, $\overline{BCTS}$, $\overline{BCD}$

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage ($I_{OH} = -\ 50\ \mu A$, $C_{LD} = 50\ pF$)	2.4			V
V_{OL}	Output LOW Voltage ($I_{OL} = +\ 2\ mA$, $C_{LD} = 50\ pF$)			0.4	V
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V
V_{IL}	Input LOW Voltage	– 0.5		+ 0.8	V
V_{IHC}	External Clock Input HIGH ($XTAL_1$)	3.8		V_{CC}	V
V_{ILC}	External Clock Input LOW ($XTAL_1$)	– 0.5		0.8	V
V_{IHR}	External Reset Input HIGH ($\overline{RESET}$)	3.8		V_{CC}	V
V_{ILR}	External Reset Input LOW ($\overline{RESET}$)	– 0.5		0.8	V
I_{IL}	Digital Input Leakage Current ($0 \leq V_{IN} \leq V_{CC}$)	– 10		+ 10	µA
I_{CC}	V_{CC} Supply Current			125	mA
I_{BB}	V_{BB} Supply Current			25	mA
C_{OUT}	Output Capacitance ($f_C = 1.0\ MHz$)		5	15	pF
C_{IN}	Input Capacitance ($f_C = 1.0\ MHz$)		5	15	pF

ANALOG INPUT (RC) :

R_{IN}	Input Resistance ($-\ 1.6\ V < V_{RC} < +\ 1.6\ V$)	50			kΩ
V_{RC}	Operating Input Signal	– 1.6		+ 1.6	V
V_{RCOS}	Allowed DC Input Offset (REF V_{AGND})	– 30		+ 30	mV

ANALOG OUTPUT (TC) :

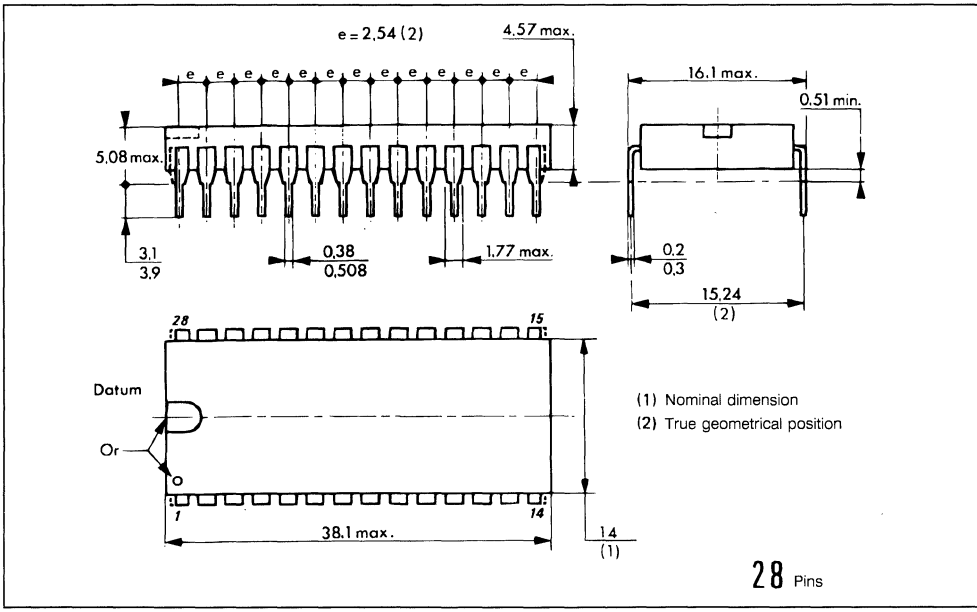
V_{TC}	Output Voltage ($R_L = 600\ \Omega$)	– 1.1		+ 1.1	V
V_{TCOS}	Output DC Offset		± 200		mV

ORDERING INFORMATION

Part Number	Temperature Range	Package
EF7910PL	0 to 70 °C	DIP 28
EF7910JL	0 to 70 °C	CERDIP28

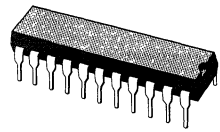
PACKAGE MECHANICAL DATA

28 PINS – PLASTIC PACKAGE



SINGLE CHIP ASYNCHRONOUS FSK MODEM

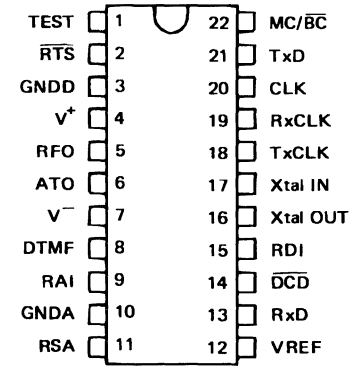
- MONOLITHIC DEVICE INCLUDING BOTH TRANSMIT AND RECEIVE FILTER
- PROGRAMMABLE MODES :
  - 75 BDS TRANSMIT / 1200 BDS RECEIVE
  - 1200 BDS TRANSMIT / 75 BDS RECEIVE
  - 1200 BDS FULL DUPLEX ON 4 WIRE LINE
  - ANALOG LOOPBACK
- FIXED COMPROMISE LINE EQUALIZER
- RECEIVE AND TRANSMIT CLOCKS FOR UART
- STANDARD LOW COST CRYSTAL (3.579 MHz)
- ± 5 % POWER SUPPLIES (+ 5 V, - 5 V)
- DTMF FILTER AND TAX REJECTION NOTCH-FILTER (kit with EFG7189 DTMF)
- 3.579 MHz CLOCK OUTPUT AVAILABLE



P
DIP22
(Plastic Package)

(Ordering Information at the end of the datasheet)

PIN CONNECTIONS



M88TS7513-01

DESCRIPTION

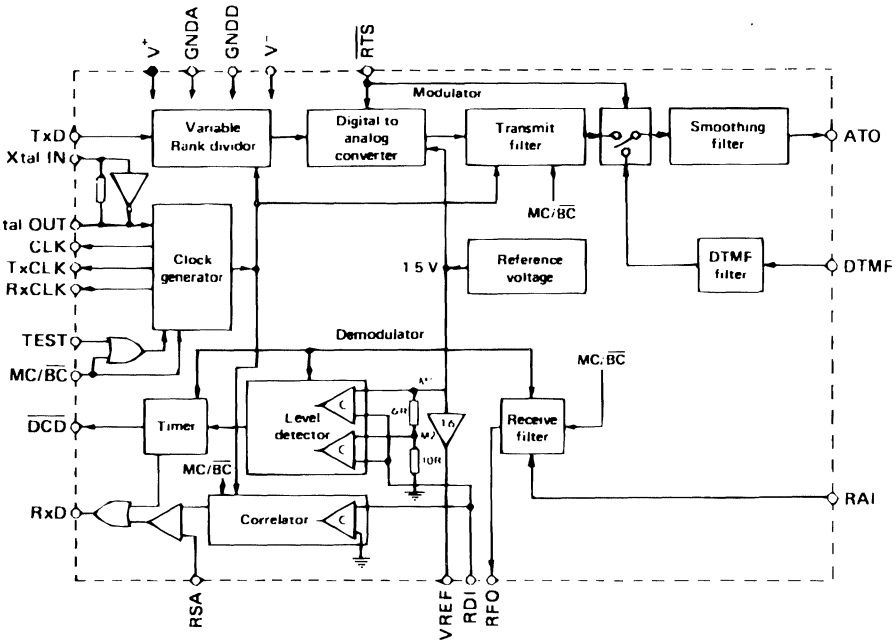
The TS7513 is a single chip asynchronous frequency shift keying voice-band modem. Operating at rates up to 75, 1200 bit per second, it is compatible with the applicable CCITT recommended standards for V.23 type modems. This device provides the essential CCITT V.24, V.25 and V.54 terminal control signals at TTL levels.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V^+	Supply Voltage	+ 7 V	V
V^-	Supply Voltage	− 7 V	V
V_{in}	Analog Input Range	$V^- \leq V_{IN} \leq V^+$	V
V_I	Digital Input Range	$GNDD \leq V_I \leq V^+$	V
T_A	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	− 55 to + 125	°C
	Pin Temperature (soldering, 10 s)	260	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Standard CMOS handling procedures should be employed to avoid possible damage to device.

BLOCK DIAGRAM



M88TS7513-02

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min.	Nom.	Max.	Unit
V^+	Positive Supply Voltage	4.75	5.0	5.25	V
V^-	Negative Supply Voltage	– 5.25	– 5.0	– 4.75	V
I_{CC}	V^+ Operating Current	–	–	20	mA
I_{BB}	V^- Operating Current	– 15	–	–	mA

D.C. AND OPERATING CHARACTERISTICS

(T_A = 0 °C to + 70 °C, V^+ = + 5 V ± 5 %, V^- = − 5 V ± 5 %, GNDA = 0 V, GNDD = 0 V, unless otherwise noted).

DIGITAL INTERFACE (TEST, $\overline{RTS}$, $\overline{DCD}$, RxD, TxCLK, RxCLK, CLK, TxD, MC/$\overline{BC}$)

Symbol	Parameter	Min.	Typ. (1)	Max.	Unit
I_I	Input Current ($V_{IL\ min} \leq V_I \leq V_{IH\ max}$)	–	–	10	µA
I_{OL}	Output Low Level Current (V_{OL} = 0.4 V)	1.6	–	–	mA
I_{OH}	Output High Level Current (V_{OH} = 2.8 V)	–	–	− 250	µA
V_{IL}	Input Low Voltage	GNDD	–	0.8	V
V_{IH}	Input High Voltage	2.4	–	V^+	V

ANALOG INTERFACE, RECEIVE FILTER (DTMF, RAI, RFO)

Symbol	Parameter		Min.	Typ. (1)	Max.	Unit
I_{BRI}	Input Leakage Current, (− 3 V < V_{IN} < 3 V)	DTMF, RAI	–	± 1	± 3	µA
R_{IRI}	Input Resistance,	DTMF, RAI	1	3	–	MΩ
V_{OGSR}	Output Offset Voltage,	RFO	–	–	± 300	mV
V_{ORI}	Output Voltage Swing, (RL ≥ 10 kΩ)	RFO	–	–	± 3	V
C_{LRI}	Load Capacitance,	RFO	–	–	20	pF
R_{LRI}	Load Resistance,	RFO	10	–	–	kΩ
V_{IRI}	Input Voltage Swing,	RAI	− 2	–	+ 2	V
V_{ID}	Input Voltage Swing	DTMF	− 3	–	+ 3	V
C_{DPR}	Signal Frequency Distortion Products at Maximum Signal Level	RFO	–	− 40	–	dB

ANALOG INTERFACE RECEIVE DEMODULATOR INPUT (RDI)

Symbol	Parameter	Min.	Typ. (1)	Max.	Unit
I_{in}	Input Current	− 1	–	1	µA
N_1	Maximum Detection Level to Valid $\overline{DCD}$ Output	1.2	1.4	1.6	V_p
N_2	Minimum Detection Level to Valid $\overline{DCD}$ Output	–	1.0	–	V_p
N_1/N_2	Hysteresis Effect	2.3	3	4	dB

ANALOG INTERFACE, RECEIVE SLICER ADJUST (RSA)

Symbol	Parameter	Min.	Typ. (1)	Max.	Unit
I_{in}	Input Current	− 1	–	+ 1	µA
V_I	Input Voltage	V_{REF}	$V_{REF}/2$	GNDA	V

(1) Typical values are for T_A = 25 °C and nominal power supply values.

D.C. AND OPERATING CHARACTERISTICS (continued)

ANALOG INTERFACE, TRANSMIT OUTPUT (ATO)

Symbol	Parameter	Min.	Typ. (1)	Max.	Unit
V_{OS}	Output DC Offset, ($\overline{RTS}$ connected to V^+)	–	–	± 250	mV
C_L	Load Capacitance	–	–	20	pF
R_L	Load Resistance	10	–	–	kΩ
V_O	Output Voltage Swing 390 Hz (R_L = 10 kΩ, C_L = 20 pF)	2.8	–	3.6	V_{pp}
–	450 Hz/390 Hz Ampl. Ratio	0	–	1	dB
V_O	1300 Hz	2.8	–	3.6	V_{pp}
–	2100 Hz/1300 Hz Ampl. Ratio	0	–	1	dB
–	$\overline{RTS}$ Attenuation Ratio Efficiency	55	–	–	dB

ANALOG INTERFACE, REGULATED VOLTAGE (V_{REF})

Symbol	Parameter	Min.	Typ. (1)	Max.	Unit
V_{OR}	Output Voltage	– 2.6	– 2.2	– 1.8	V
R_{LR}	Load Resistance	10	–	–	kΩ
C_{LR}	Load Capacitance	–	–	20	pF

(1) Typical values for T_A = 25 °C and nominal power supply values.

DYNAMIC CHARACTERISTICS

RECEIVE FILTER TRANSFER CHARACTERISTICS

Symbol	Parameter		Min.	Typ.	Max.	Unit
G_{AR}	Absolute Passband Gain at 1300 Hz	(V_{RFO}, R_L = ∞)	0.9	1.5	2.6	dB
G_{RR}	Gain Relative to Gain at 1300 Hz (maximum input signal) (2)	390 Hz	–	– 60	– 50	dB
		450 Hz	–	– 60	– 48	dB
		2100 Hz	2.8	3.1	4	dB
		2900 Hz	– 30	–	– 17	dB
		12000 Hz	–	– 45	– 40	dB
G_{AR}	Absolute Passband Gain at 390 Hz	(V_{RFO}, R_L = ∞)	0.9	1.5	2.6	dB
G_{RR}	Gain Relative to Gain at 390 Hz (maximum input signal)	450 Hz	1	1.5	2	dB
		800 Hz	– 30	–	20	dB
		1300 Hz	–	– 50	– 48	dB
		2100 Hz	–	– 55	– 50	dB
		12000 Hz	–	– 45	– 40	dB

DTMF FILTER TRANSFER CHARACTERISTICS

Symbol	Parameter		Min.	Typ.	Max.	Unit
G_{AR}	Absolute Passband Gain at 100 Hz		–	0	–	dB
G_{RR}	Gain Relative to Gain at 100 Hz	1000 Hz	– 1	0	+ 1	dB
		3400 Hz	–	– 3	– 2	dB
		10000 Hz	–	–	– 20	dB

DYNAMIC CHARACTERISTICS (continued)

DIGITAL INTERFACE

Symbol	Parameter	Min.	Typ. (1)	Max.	Unit
C_{IB}	Capacitance	–	–	10	pF
t_{THL}, t_{TLH}	Input Rise-time, Fall-time, measured between 0.8 V and 2.4 V	–	–	100	ns
t_{THL}, t_{TLH}	Output Rise-time, Fall-time between 0.4 V and 2.8 V (3)	–	50	–	ns

(1) Typical values are for $T_A = 25°C$ and nominal power supply values
(2) This value refers to the integrated receive filter only, measured at RFO. The rejection value for the complete reception part must take into account the band-pass filter of the peak limiter (refer to CALCULATION OF CIRCUIT ELEMENTS). In this case the maximum gain relative to gain at 1300 Hz is – 60 dB at 16 kHz.
(3) Driving one 74L or 74LS TTL load plus 30 pF.

PIN DESCRIPTION

COMMON SECTION

N°	Name	Function	Description
4 7	V^+ V^-	Positive Power Supply Negative Power Supply	+ 5 V – 5 V
10	GNDA	Analog Ground	Pin 10 serves as the ground return for the analog circuits of the transmit and receive section. The analog ground is not internally connected to the digital ground. The digital and analog grounds should be tied together as close as possible to the system supply ground.
3	GNDD	Digital Ground	Pin 3 serves as the digital ground return for the internal clock. The digital ground is not internally connected to the analog ground. The digital and analog grounds should be tied together as close as possible to the system supply ground.
17	Xtal IN	Oscillator Input	This pin corresponds to the input of the inverter of the oscillator. It is normally connected to an external crystal, but may also be connected to a pulse generator. The nominal frequency of the oscillator is 3.579 MHz.
16	Xtal OUT	Oscillator Output	This pin corresponds to the output of an inverter with sufficient loop gain to start and maintain the crystal oscillating.
12	VREF	Regulated Voltage	This output carries an internally regulated voltage. By means of an external potentiometer connected between VREF and GNDA, an adjustable reference voltage may be applied to RSA. The adjustment of RSA is to optimize the discrimination of high anf low frequencies of the same channel. The voltage applied to RSA is approximately VREF/2.
20	CLK	Clock	This output delivers a clock signal, the frequency of which is 3.579 MHz.
22	MC/$\overline{BC}$	Main Channel/Back Channel	This input selects transmission on the main channel or back channel and defines the modulation rate according to the European standards. (refer to functional description).

PIN DESCRIPTION (continued)

TRANSMIT SECTION

N°	Name	Function	Description
2	$\overline{RTS}$	Request to Send	When a low state is present on input $\overline{RTS}$, the TS7513 delivers on output ATO a sinusoidal signal at a frequency which depends on input TxD. When a high state is present on input $\overline{RTS}$, output ATO is connected to DTMF filter.
21	TxD	Transmit Data	This input selects the high frequency or low frequency at the Analog transmit output pin (ATO) : • a high state selects the low frequency, • a low state selects the high frequency.
18	TxCLK	Transmit Clock	This output delivers a clock signal, the frequency of which is 16 times the modulation rate (± 1 %). The logic state duration is compatible to the UART clock specification.
6	ATO	Analog Transmit Output	When a low state is present on $\overline{RTS}$, the TS7513 delivers on output ATO a sinusoidal signal centered on the analog ground.

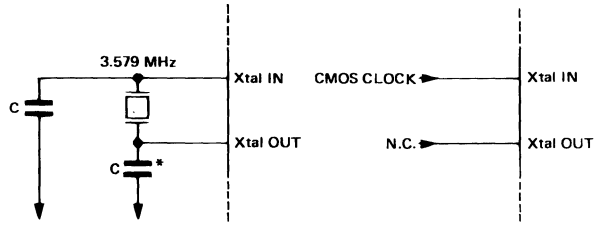
RECEIVE SECTION

N°	Name	Function	Description
1	TEST	Loop Back Mode	When high, the demodulator is tuned on the transmission modulation rate to the loop back mode or to the 4 wires full duplex operation mode. When TEST is low, the modem is in normal operating mode.
5	RFO	Receiver Filter Output	This analog output must be connected to a high-pass filter and slicer, with sufficient gain to satisfy the level detection conditions.
8	DTMF	Dual Tone Multifrequency Input	Analog input receiving a signal from a dual tone multifrequency generator. Transmitted spectrum of DTMF signal matches the gauge in Annex III.
9	RAI	Receive Analog Input	Input for modulated analog signal of amplitude lower than 4 V peak to peak and centered on analog ground.
15	RDI	Receive Demodulator Input	This is input of the demodulator. The analog signals are passed through level detection comparators and zero crossing detector.
11	RSA	Receive Slicer Adjust	Input of the decision comparator optimizing discrimination between high and low frequencies.
14	$\overline{DCD}$	Data Carrier Detect	This output is low when TS7513 receives on input RDI a signal with amplitude higher than N1 This output is high when the TS7513 receives on input RDI a sinusoidal signal with amplitude lower than N2. Within the N1 – N2 range, the detection system presents an hysteresis.
13	RxD	Receive Data	This output is low when a high frequency signal is present on input RDI, and high when a low frequency signal is present on input RDI. Without carrier on pin RAI, this output is high.
19	RxCLK	Receive Clock	This output delivers a clock signal, the frequency of which is 16 times the demodulation rate (± 1 %). The logic state duration is compatible to the UART clock specification.

FUNCTIONAL DESCRIPTION

CLOCK GENERATION

Crystal : NYMPH, NYP 035A – 18



*Capacitor values vary with different crystal manufacturers ; typical value : 12 pF

M88TS7513-03

With a minimum number of external components, the TS7513 performs all the functions of modulation, demodulation and filtering necessary to meet the requirements of CCITT Recommandation V.23.

This circuit is in five parts :

- a modulator
- a demodulator
- a clock generator
- a reference voltage generator
- a DTMF filter.

Note : The description of the demodulator also covers a subsystem, external to the circuit proper and having the following functions (refer to paragraph CALCULATION OF CIRCUIT ELEMENTS).

- Band-pass filter
- amplification
- slicer.

MODULATOR

When input $\overline{RTS}$ is low, output ATO delivers a sinusoidal signal, the frequency of which depends on MC/BC and TxD.

DEMODULATOR

When the analog signal on RDI conforms to certain criteria, output DCD detects it and output RxD delivers a digital signal, the logic state of which depends on the analog signal frequency.

CLOCK GENERATOR

This part of the circuit generates from a 3.579 MHz crystal all the internal clocks necessary to the correct performance of the TS7513 : the clocks for the switched capacitor filters as well as those for the sinewave generator. The circuit delivers on RxCLK and TxCLK, the transmit and receive clocks for the UART. It also delivers on CLK a buffered clock at 3.579 MHz.

REFERENCE VOLTAGE GENERATOR

This part of the circuit generates a regulated voltage on VREF which is used to adjust detection thresholds. It is independent of power supply values.

DTMF FILTER

This part of the circuit receives a signal from a dual tone multi-frequency generator and transmit through ATO a filtered signal when RTS is high.

FUNCTIONAL CHARACTERISTICS

MODULATOR

• Modulation Conditions :

$\overline{RTS}$	ATO
" L "	FSK Modulated Signal
" H "	DTMF Signal

• **Transmitted Frequencies :**
(for details of frequency selection see PIN DESCRIPTION – ATO)

MC/$\overline{BC}$	Modulation Rate	TxD	R.35 and V.23 Recommandations (Hz)	Frequency Generated from a 3.579 MHz Crystal	Error (Hz)
GNDD	75 Bauds	"H" "L"	390 ± 2 450 ± 2	389.52 450.20	– 0.48 + 0.20
V^+	1200 Bauds	"H" "L"	1300 ±10 2100 ± 10	1299.70 2097.40	– 0.34 – 2.61

DEMODULATOR

• **Frequencies Receive on RDI**

Analog signals centered on analog ground are received on input RDI.

RECEIVE DEMODULATION RATE
The receive Demodulation Rate Depends on MC/$\overline{BC}$ and TEST Input as Follows :

MC/BC	TEST	Demodulation Rate	Frequencies (recommendation V 23)
H	H	1200	1300 ± 16 2100 ± 16
L	H	75	390 450
H	L	75	390 450
L	L	1200	1300 ± 16 2100 ± 16

• **Level detection conditions**

Input RDI drives a signal detector the output of which (DCD) is at logic "0" if the level of signal RDI is higher than N1. The output of this detector is at logic "1" if the level of the signal RDI is lower than N2. This detector has an hysteresis effect : N1/N2.

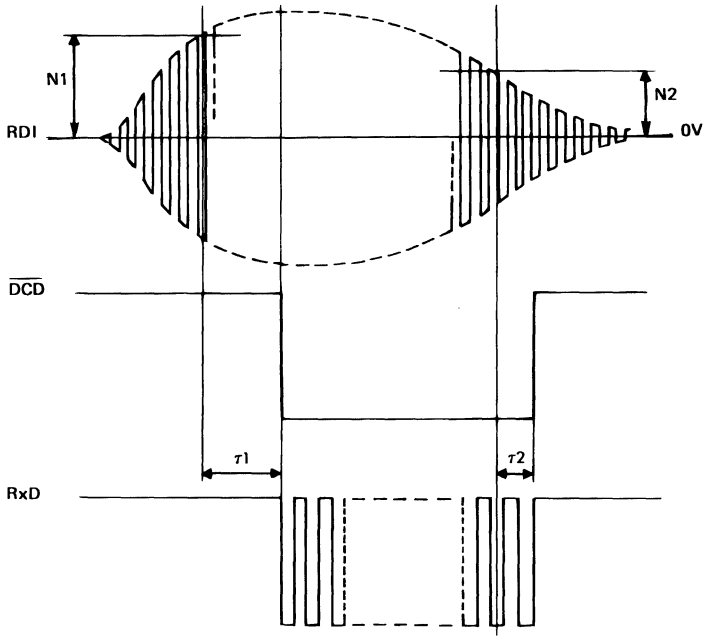
• **Timing detection conditions**

The timing performance of the level detector ($\overline{DCD}$) conforms to CCITT Recommendation V.23.

Under normal working conditions, output $\overline{DCD}$ is :

- low if signal RDI conforms to the level detection condition,
- high if signal RDI does not conform to the level detection conditions.

Output $\overline{DCD}$ goes from high to low when signal RDI conforms to the level detection conditions for 15 ms or more (respectively 15 ms for 75 bauds).
Output $\overline{DCD}$ does not go from high to low when signal RDI conforms to the level detection conditions for 10 ms or less (respectively 10 ms for 75 bauds).
Output $\overline{DCD}$ goes from low to high when signal RDI does not conform to the level detection conditions for 15 ms or more (respectively 30 ms for 75 bauds).
Output $\overline{DCD}$ does not go from low to high when signal RDI does not conform to the level detection conditions for 10 ms or less (respectively 20 ms for 75 bauds).
Note : Each transition on the MC/BC input sets the DCD output to the logical high level and initiate the detection timing.



M88TS7513-04

Modulation Rate	DCD Transition	Min.	Typ. (1)	Max.	Unit
1200 bds	τ 1	10	12	15	ms
	τ 2	10	12	15	ms
75 bds	τ 1	10	15	20	ms
	τ 2	20	30	40	ms

(1) Typical values for T_A = 25 °C and nominal power supply values.

• **Demodulated Signal**

Under Normal Working Conditions, signal RxD Conforms to the Following Table :

Demodulation Rate	Level Received on RDI	DCD	Frequency Received on RAI (Hz)	RxD
1200 bds	> N1	" L "	1300	" H "
	> N1	" L "	2100	" L "
	< N2	" H "	" X "	" H "
75 bds	> N1	" L "	390	" H "
	> N1	" L "	450	" L "
	< N2	" H "	" X "	" H "

REFERENCE VOLTAGE GENERATOR
The VREF output carries a regulated reference voltage.
An external potentiometer, connected between VREF and GNDA, can supply a regulated voltage to input RSA.
Adjustement of RSA optimizes the discrimination between the high and low frequencies.

CALCULATION OF CIRCUIT ELEMENTS

The following factors must be considered in calculating the external components in the TS7513 application :

- Signal amplification introduced by the receive filter is 1.5 dB/1300 Hz.
- The maximum permissible level at RAI input is 4 Vpp (+ 5 dBm).

Note : the reference frequencies are 1300 and 390 Hz.

- A 2.5 dB hysteresis is introduced within the two signal detection level N1 and N2, in accordance with CCITT Recommendation V.23.

To be centered, the two limit values of the CARRIER DETECT signal are therefore :

- Upper : - 43 dBm, or 15.5 mV_{PP}
- Lower : - 48 dBm, or 8.7 mV_{PP}

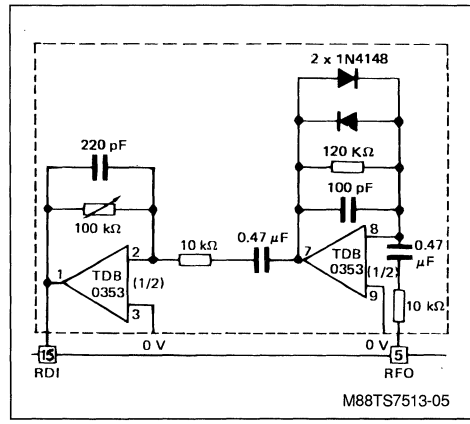
- For a correct operation of the TS7513 signal detector, the peak-limiting filter must remain linear up to - 43 dBm on line.
- At input RDI, the upper threshold level N1 of the signal detector is 2.8 VPP (2.1 dBm), and must correspond to the minimum signal level received from the line transformer. With a duplexer reception gain of + 6 dB, the peak-limiting filter gain is defined by :

A = 43 - 6 - 1.5 + 2.1 = 37.6 dB (a ratio of 76).

Note : The peak-limiting filter gain must be adjusted according to the minimum level on line. With a minimum level of :

- 38 dBm, A = 32.6 dB
- 33 dBm, A = 27.6 dB

Typical Peak-limiting Filter Configuration



ENVIRONMENTAL FUNCTIONAL DESCRIPTION (refer to typical application)

Transmit section

The transmit section comprises a single operational amplifier capable of driving a load of 600Ω , which can also be used to adjust the transmit level.

Duplexer

This amplifier provides the 2 wire/4 wire separation function and enables a low cost standard non differential transformer (ratio 1:1) to be used. The duplexer principlze provides a gain of 6 dB for the received signal.

Peak-limiting filter

This section is made of two operational amplifiers and performs three functions :

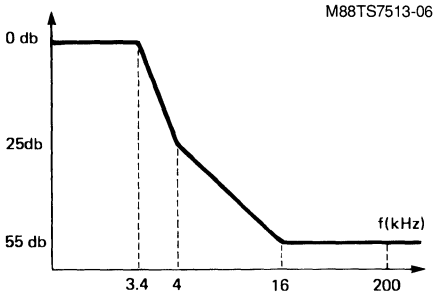
- peak-limiting amplifier, designed to meet the signal detector levels according to the signal received from the phone line.
- High-pass filter (12 dB per octave) to overcome the DC component of the signal to be demodulated.
- Low-pass filter to protect against the inherent noise of the receive filter.

TYPICAL PERFORMANCES

These typical performances are achieved with the measuring equipment described in Annex I.

• **Transmitted spectrum**

On output ATO, the transmitted out of band signal energy must conform to the following specification :



• **Receiver**

Measurement conditions

Local transmit level : - 10 dBm.
Receive level : - 25 dBm, with 511 bit pseudo-random test pattern.

Isochronous distortion

Table below shows the typical isochronous distortion values obtained with the TS7513, which conform to the french CCETT specifications for videotext applications. The characteristics of CCETT lines used for measurements are given in Annex II.

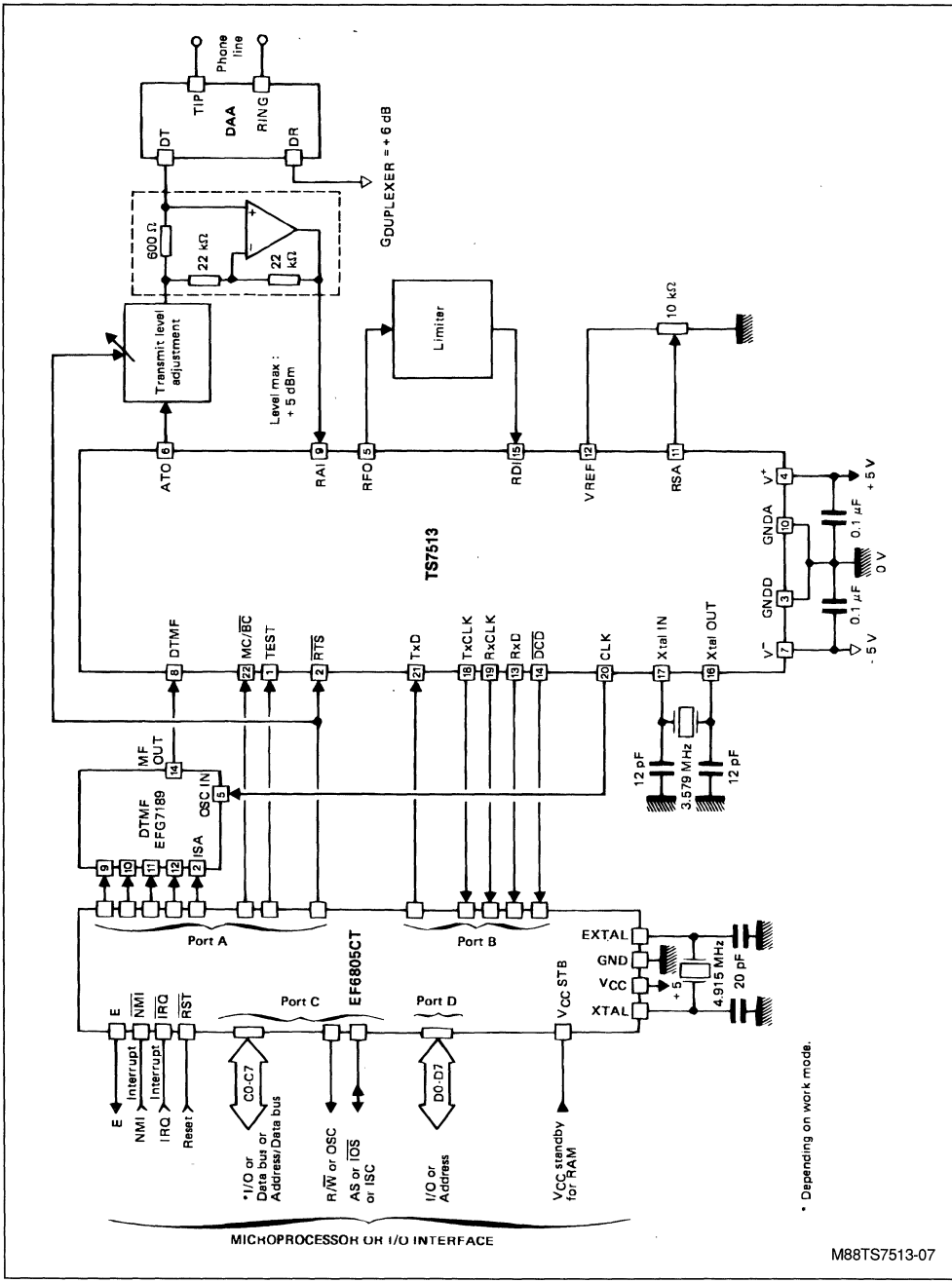
Line	1200 bds Reception	75 bds Reception
Line 1 (flat)	10 %	4 %
Line 2	12 %	4 %
Line 3	18 %	6 %
Line 4	12 %	6 %

BIT ERROR RATE

The typical bit error rates versus white noise are as follows.

	1200 bds Reception		75 bds Reception	
	S/N	BER	S/N	BER
on Line 1	6 dB	2.10^{-3}	– 1 dB	7.10^{-4}
on Line 2	7 dB	5.10^{-4}	– 1 dB	7.10^{-4}
on Line 3	9 dB	5.10^{-4}	0 dB	5.10^{-4}
on Line 4	8 dB	2.10^{-4}	0 dB	5.10^{-4}

TS7513 : Typical Application.

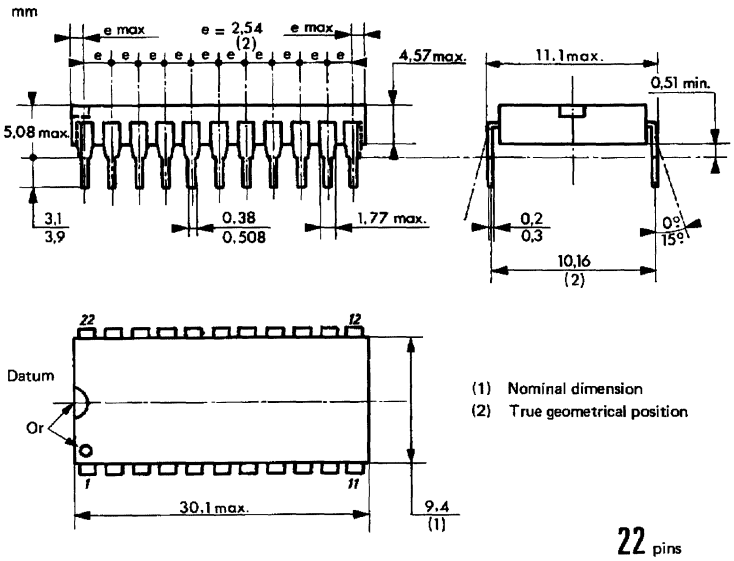


ORDERING INFORMATION

Part Number	Temperature Range	Package
TS7513CP	0 to + 70 °C	DIP 22
TS7513IP	– 40 to + 85 °C	DIP 22

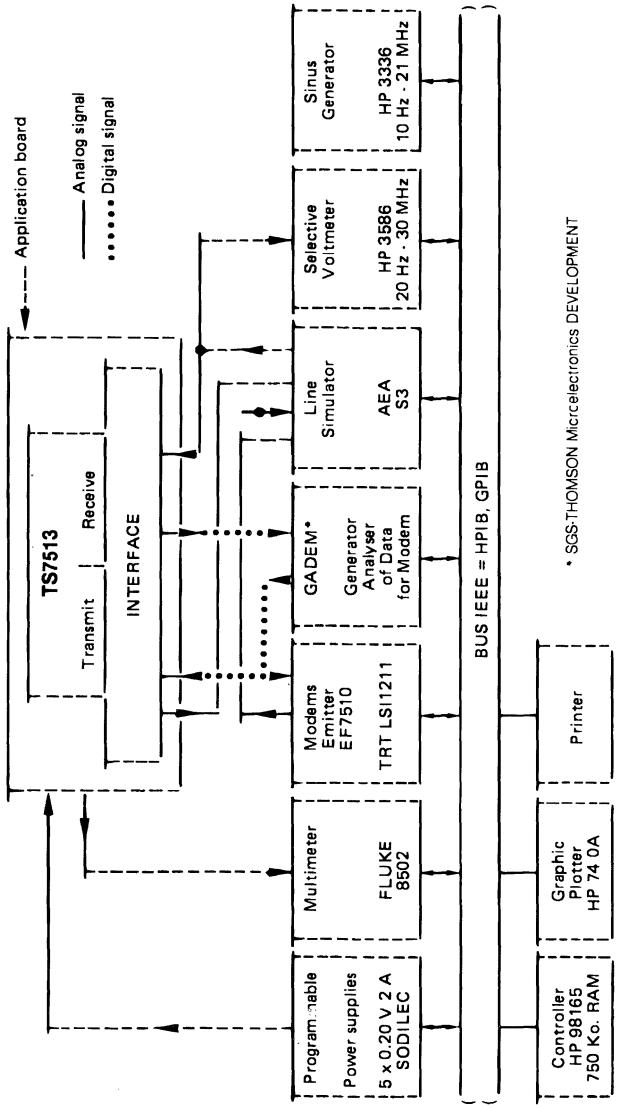
PACKAGE MECHANICAL DATA

22 PINS - PLASTIC DIP



APPENDIX 1

1 – MEASUREMENT SYSTEM



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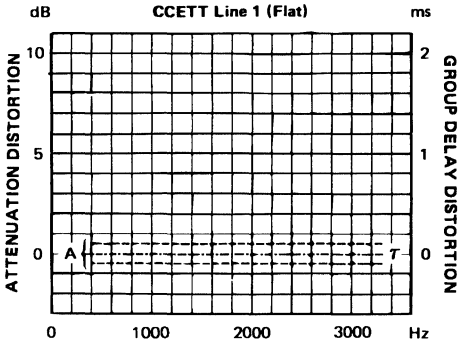
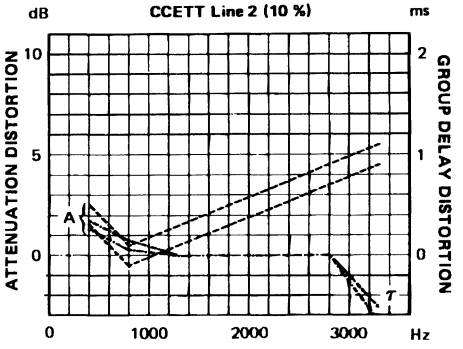
APPENDIX 2

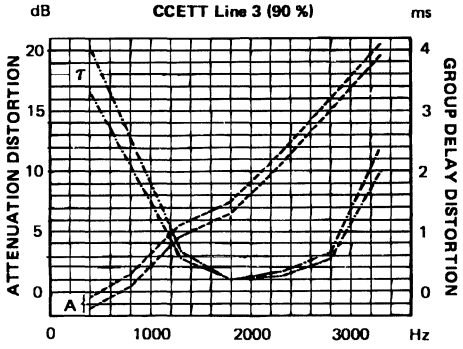
CHARACTERISTICS OF TEST LINES



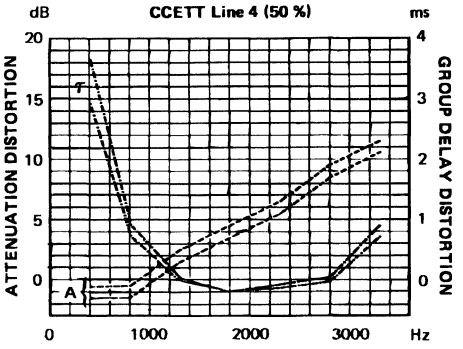
M88TS7513-11



M88TS7513-12

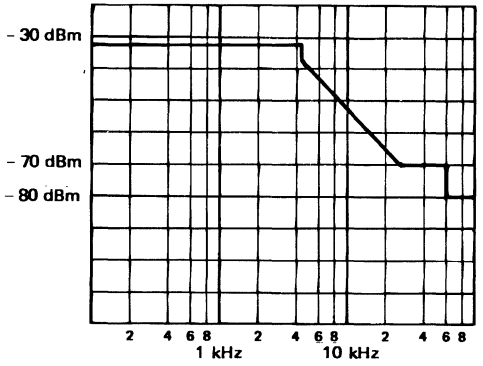


M88TS7513-11



M88TS7513-12

SPECTRUM OF DTMF SIGNAL



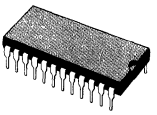
M88TS7513-13

K17 CCITT specification for telephone set gauge

PROGRAMMABLE V.23 MODEM WITH DTMF

ADVANCE DATA

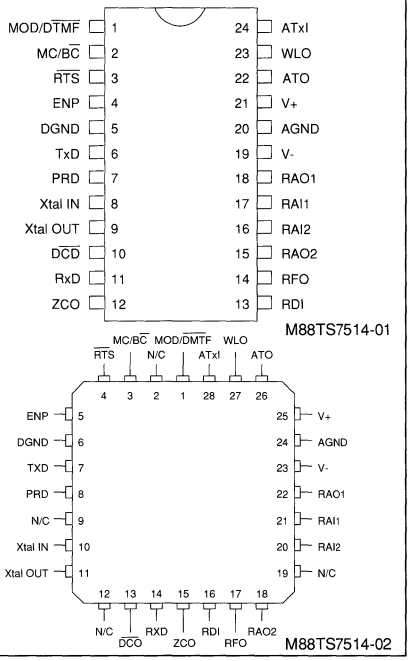
- PROGRAMMABLE MODES :
  - Modem 75 bps transmit, 1200 bps receive
  - Modem 1200 bps transmit, 75 bps receive
  - DTMF dialing
  - Call status tone detection
  - Auxiliary analog transmit input
  - Analog test loopback
- PROGRAMMABLE FUNCTIONS :
  - Transmission level
  - Hysteresis and detection level
  - Filters (reception and transmission)
  - Line monitoring and buzzer
  - DTMF frequencies
- FIXED COMPROMISE LINE EQUALIZER
- AUTOMATIC BIAS ADJUSTMENT
- INTEGRATED DUPLEXER
- STANDARD LOW COST CRYSTAL (3.579 MHZ)
- TAX TONE REJECTION
- POWER-UP INITIALIZATION OF REGISTERS
- OPERATES FROM ± 5 VOLTS



P
DIP24
(Plastic Package)

FN
PLCC28
(Plastic Package)

PIN CONNECTIONS



DESCRIPTION

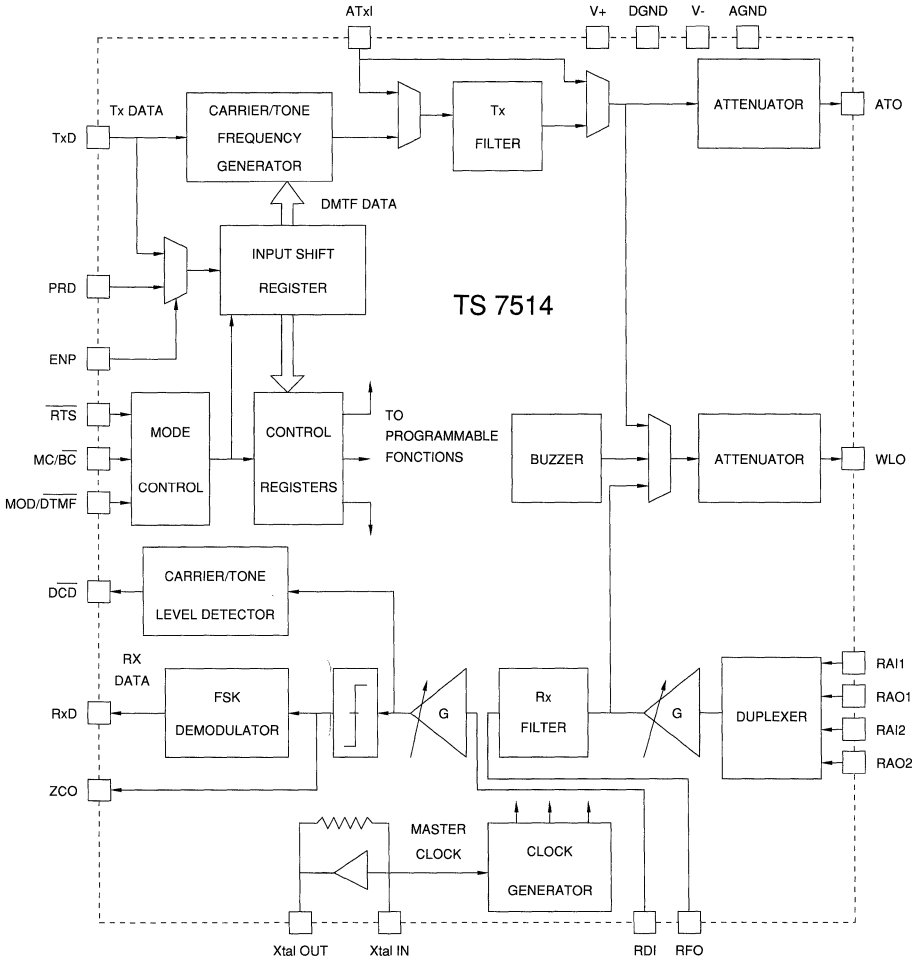
The TS7514 is an FSK modem which can be programmed for asynchronous half-duplex voice-band communications on a 2-wire line or full duplex on a 4-wire line. Its programming concept makes it the ideal component to design low-cost intelligent modems, featuring auto dialing and auto answering.

The TS7514 conforms to CCITT V.23 recommendation.

The chip incorporates DTMF dialing, line monitoring, tone and dialing detection.

ARCHITECTURE

Figure 1 : Simplified Block Diagram.



M88TS7514-03

PIN DESCRIPTION

Name	Pin n° P D I P	Pin n° P L C C	Description
MOD/$\overline{DMTF}$	1	1	MODEM or DMTF Operating Mode Selection Also controls write operations to control registers (if MOD/$\overline{DMTF}$ = 0 and MC/$\overline{BC}$ = 0).
MC/$\overline{BC}$	2	3	Digital Control Input. In MODEM mode, it sets transmission mode to main or back channel. It also permits selection of dialing or control registers programming.
$\overline{RTS}$	3	4	Request to Send When RTS = 0, the circuit sends an analog signal to the ATO output. The signal depends on the operating mode selected. When RTS = 1, the signal sent to ATO is suppressed after its first zero crossing. When MOD/$\overline{DMTF}$ = 0 and MC/$\overline{BC}$ = 0, the RTS pin acts as a clock for serial data loading into the input register.
ENP	4	5	Serial Register Write Select Input. When ENP = 0, the serial register input is connected to TxD. When ENP = 1, the register input is connected to PRD.
DGND	5	6	Digital Ground = 0V. All digital signals are referenced to this pin.
TxD	6	7	Digital Input for Transmit or Control Data
PRD	7	8	Digital Input for Control Data. Selected through ENP
XtalIN	8	10	Crystal Oscillator Input. Can be tied to an external clock generator. F quartz = 3.579 MHz.
XtalOUT	9	11	Crystal Oscillator Output
DCD	10	13	Data Carrier Detect Output
RxD	11	14	Digital Receive Data Output
ZCO	12	15	Zero Crossing Rx Digital Output (ringing detection)
RDI	13	16	Analog Output for the Receive Signal after Filtering or Analog Input for the Amplifier-limiter.
RFO	14	17	Analog Receive Filter Output
RAO2	15	18	A2 Amplifier Output
RAI2	16	20	A2 Amplifier Inverting Input
RAI1	17	21	A1 Amplifier Inverting Input
RAO1	18	22	A1 Amplifier Output
V-	19	23	Negative Supply Voltage : – 5 V ± 5 %
AGND	20	24	Analog Ground = 0 V. Reference Pin for Analog Signals
V+	21	25	Positive Supply Voltage : + 5 V ± 5 %
ATO	22	26	Analog Transmit Output
WLO	23	27	Analog Output for Line Monitoring and Buzzer
ATxI	24	28	Direct Analog Input Transmit Filter

FUNCTIONAL DESCRIPTION

The TS7514 circuit is an FSK modem for half-duplex, voice-band asynchronous transmissions on a 2-wire line according to CCITT recommendation V.23 or full duplex on 4 wire-line.

The circuit features DTMF dialing, call status tone detection and line monitoring in both dialing and automatic answer modes. A signalling frequency is available at the line monitoring output (buzzer).

Ring detection is possible by using the signal detection function and bypassing the receive filter. The receive signal at ZCO output can be filtered in the associated microprocessor.

The TRANSMIT channel (Tx) includes :

- two programmable frequency generators
- one switched capacitor filter (SCF) with low-pass or bandpass configuration and its associated propagation delay corrector.
- one continuous time low-pass smoothing filter
- one attenuator, programmable from 0 to + 13 dB by 1 dB steps
- one programmable analog input

The RECEIVE channel (Rx) includes :

- two operational amplifiers for duplexer implementation
- one continuous time low-pass anti-aliasing filter
- one programmable gain amplifier
- one linear compromise equalizer
- one switched capacitor band pass filter (can be set to either main or back channel)
- one continuous time low pass smoothing filter
- one limiting amplifier
- one correlation demodulator
- one programmable level signal detector

The LINE MONITORING channel includes :

- one buzzer
- one 3-channel multiplexer to select beetwen
  - transmit channel monitoring
  - receive channel monitoring
  - buzzer
- one programmable attenuator

INTERNAL CONTROL

Power up initialization

The TS7514 includes power-up initialization of control registers. This system sets the ATO transmission output to an infinite attenuation position, leaving time for the microprocessor to set up the RPROG input on power up. Control registers are also initialized when V+ is lower than 3 V or V - greater than - 3 V.

Registers

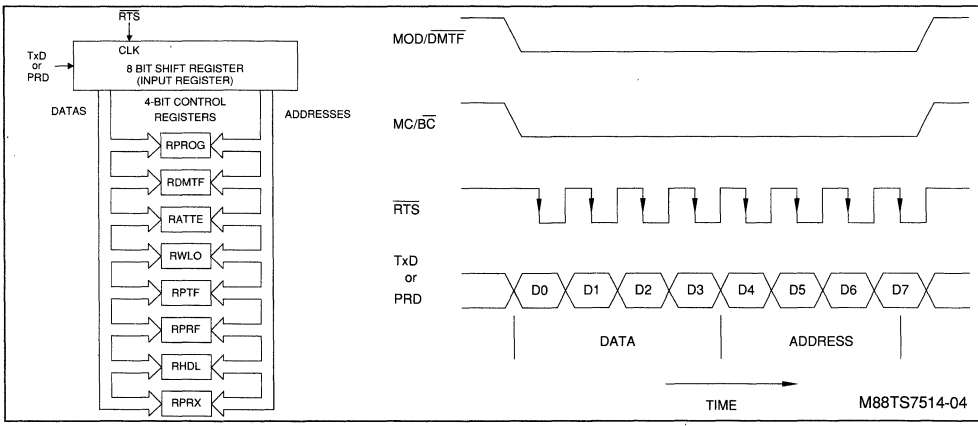
Write access to the DTMF data register and to other control registers is achieved in serial mode through TxD input or PRD input*. Addressing of these 4 bit registers is indirect. They are accessed through an 8 bit shift register addressed when MOD/$\overline{\text{DTMF}}$ = 0 and MC/$\overline{\text{BC}}$ = 0. Data sent to the TxD input is strobed on the RTS signal trailing edge.

Serial data is sent to the TxD input, with Least Significant Bit (LSB) first. The 4 Most Significant Bits (MSB) contain the control register address while the 4 LSB contain associated data.

Data transfer from the input register to the control register (addressed by the MSB's) is started by the operating mode (MODEM or DTMF) selection (MOD/$\overline{\text{DTMF}}$ = 1 or MC/$\overline{\text{BC}}$ = 1).

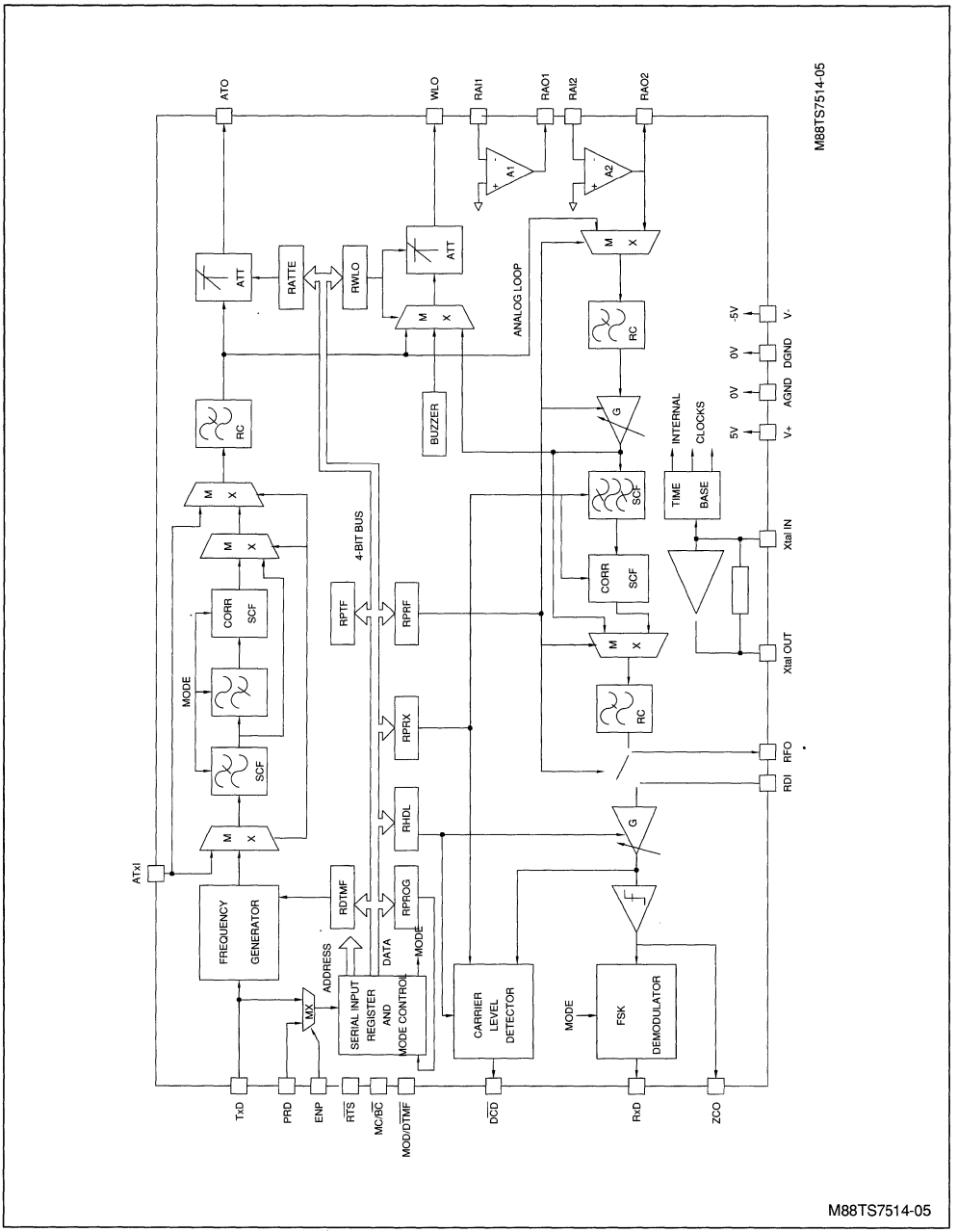
* N.B. PRD input can be used instead of TxD (when ENP = 1).

Figure 2 : Internal Control Register.



FUNCTIONAL DESCRIPTION (continued)

Figure 3 : Detailed Block Diagram.



OPERATING MODES

The various operating modes are defined by MC/$\overline{BC}$ and MOD/$\overline{DTMF}$ inputs, and by the content of a control register RPROG.

The TS7514 includes 8 control registers. Access to each control register is achieved through an auxiliary 8 bit shift register (input register). The input of that shift register is connected either to TxD or PRD, depending upon the status of the ENP control pin (ie when ENP = 0 and ENP = 1 respectively). In both cases, the $\overline{RTS}$ input receives the shift clock and sequentialy transfer is controlled by setting simultaneously MOD/$\overline{DTMF}$ and MC/$\overline{BC}$ to 0. The previous internal status and data are memorized during loading of the input register so that transmission continues properly. That feature allows the user to modify transmission level or line monitoring selection during transmission. The transmit channel operating mode (Modem main or back channel, DTMF) can only be modified when $\overline{RTS}$ = 1. When RTS = 0, the ATO transmit output is enabled and the preselected operating mode is activated. When RTS returns to 1, Modem or DTMF transmission is inhibited after the first zero crossing of the generated signal.

MOD/$\overline{DTMF}$	MC/$\overline{BC}$	**Transmission** (ATO)	**Reception** (RxD, $\overline{DCD}$)
1	1	MODEM, Main Channel	MODEM, Back Channel
1	0	MODEM, Back Channel	MODEM, Main Channel
0	1	DTMF	$\overline{DCD}$ = Active Tone Detection (270 -500 Hz) if $\overline{RTS}$ = 1... $\overline{DCD}$ = 1 if $\overline{RTS}$ = 0
0	0	If $\overline{RTS}$ = 0 when that configuration occurs, transmission and reception are not modified. If $\overline{RTS}$ = 1 (no signal sent on the line), transmission is not modified and reception is set up to detect 2100 Hz tone (note 1).	

Note 1 : The decision threshold of the demodulator output is shifted, so that RxD changes from 0 to 1 at 1950 Hz instead of 1700 Hz.

MODEM TRANSMISSION FREQUENCIES

Modulation Rate	TxD	CCITT R35 AND V.23 Recommendations (Hz)	Frequency Generated with Xtal at 3.579 MHz (Hz)	Error (Hz)
75 bps	1	390 ± 2	390.09	+ 0.09
	0	450 ± 2	450.45	+ 0.45
1200 bps	1	1300 + 10	1299.76	– 0.24
	0	2100 ± 10	2099.12	– 0.88

DTMF TRANSMISSION FREQUENCIES

	Specifications DTMF (Hz)	Frequency Generated with Xtal at 3.579 MHz (Hz)	Dividing Ratio	Error (%)
f1	697 ± 1.8 %	699.13	5120	+ 0.31
f2	770 ± 1.8 %	771.45	4640	+ 0.19
f3	852 ± 1.8 %	853.90	4192	+ 0.22
f4	941 ± 1.8 %	940.01	3808	- 0.10
f5	1209 ± 1.8 %	1209.31	2960	+ 0.03
f6	1336 ± 1.8 %	1335.65	2680	- 0.03
f7	1477 ± 1.8 %	1479.15	2420	+ 0.15
f8	1633 ± 1.8 %	1627.07	2200	+ 0.36

CARRIER LEVEL DETECTOR

- Output Level Detection conditions

The $\overline{DCD}$ signal detector output is set to logic state 0 if the RMS value of the demodulator input signal is greater than N1. The DCD output has logic state 1 if the RMS value is less than N2.

The detector has an hysteresis effect : N1 - N2.

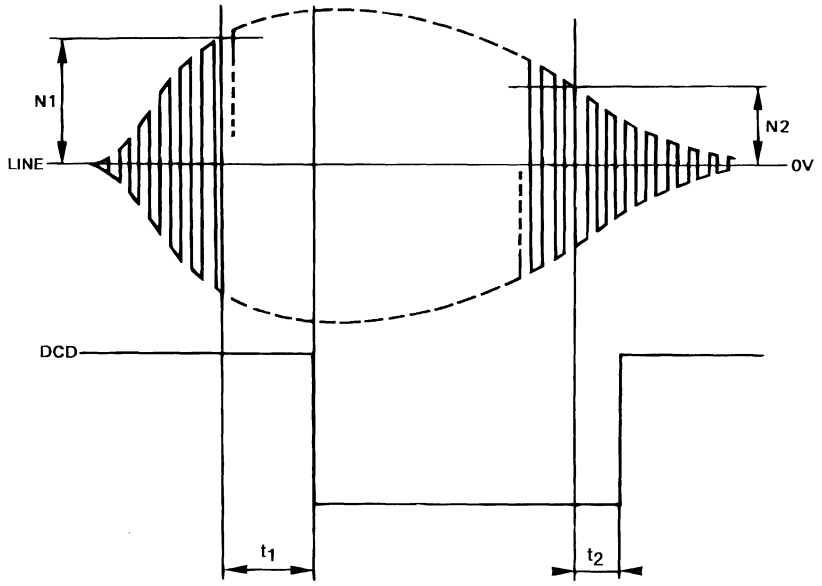
- Timing Detection Requirements

Signal detection time constants at the $\overline{DCD}$ output comply with CCITT Recommendation V.23.

Modulation Ratio	DCD Transition	CCITT V.23 (min)	Min.	Max.	CCITT V.23 (max)	Unit
1200 bps	t1	10	10	20	20	ms
	t2	5	5	15	15	ms
75 bps *	t1	0	15	40	80	ms
	t2	15	15	40	80	ms

* Wide band Rx filter used (Fig 4c.)

Figure 4 : Signal Detection Time Out.



M88TS7514-06

Note : When delays are bypassed (see RPRX register programming) response time ranges from 0 to 5 ms in receive mode at 1200 bps, and from 0 to 10 ms at 75 bps.

PROGRAMMING REGISTER

RPROG

Address				Data				Selected Mode (note 1)
D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	0 0	X X	0 1	0 1	The most significant bit (D 7) is not used when decoding control register addresses.
				0	X	0	1	Control register addressing is enabled when D 7 = 0 (see note 2).
				0	X	1	0	Control register addressing is enabled when D 7 = 1 (see note 2).
				0	0	X	X	Reception positioned in the channel opposite to the transmission channel controlled by MC/BC
				0	1	X	X	Reception positioned in the same channel as transmission (see note 3).
				1	X	X	X	Programming inhibited in normal operating mode. This mode is used for testing purposes.

Note : 1. RPROG is set to 0000 on power-up.
2. Excepted for RPROG register whose address is always 000, regardless of D0 and D1.
3. This mode allows either full duplex operation on a 4-wire line, or circuit testing with external Tx/Rx loopback.

DTMF DIALING DATA REGISTER

RDTMF REGISTER

Address				Data				Tone Frequency (Hz)	
D7	D6	D5	D4	D3	D2	D1	D0	LOW	HIGH
P	0	0	1	X	X	0	0	697	X
				X	X	0	1	770	X
				X	X	1	0	852	X
				X	X	1	1	941	X
				0	0	X	X	X	1209
				0	1	X	X	X	1336
				1	0	X	X	X	1477
				1	1	X	X	X	1633

Note : This register is not initialized on power up.
X : Don't care value.
P : 1,0 or X depending upon RPROG content.

DATA REGISTER FOR THE TRANSMISSION ATTENUATOR

RATE REGISTER

Address				Data				Attenuation (dB)	Output Transmit Level (dBm)	On Line Level (dBm) Coupler Gain (– 6dB)
D7	D6	D5	D4	D3	D2	D1	D0			
P	0	1	0	0	0	0	0	0	+ 4	– 2
				0	0	0	1	1	+ 3	– 3
				0	0	1	0	2	+ 2	– 4
				0	0	1	1	3	+ 1	– 5
				0	1	0	0	4	0	– 6
				0	1	0	1	5	– 1	– 7
				0	1	1	0	6	– 2	– 8
				0	1	1	1	7	– 3	– 9
				1	0	0	0	8	– 4	– 10
				1	0	0	1	9	– 5	– 11
				1	0	1	0	10	– 6	– 12
				1	0	1	1	11	– 7	– 13
				1	1	0	0	12	– 8	– 14
				1	1	0	1	13	– 9	– 15
				1	1	1	0	Infinite	< – 64	< – 70
				1	1	1	1	Infinite*	< – 64 *	< – 70 *

* Power - up configuration.

LINE MONITORING PROGRAMMING REGISTER

RWLO REGISTER

Address				Data				Line Monitoring In Transmit Mode Relative Level (dB)	Line Monitoring In Receive Mode Relative Level (dB)	Signalling Frequency Absolute Level (V_{PP}) Relative Level (dB) (see note)
D7	D6	D5	D4	D3	D2	D1	D0			
P	0	1	1	0	0	0	0	– 10		
				0	0	0	1	– 20		
				0	0	1	0	– 31		
				0	0	1	1	– 42		
				0	1	0	0		0	
				0	1	0	1		– 10	
				0	1	1	0		– 20	
				0	1	1	1		– 31	
				1	0	0	0			0.42 V_{PP}
				1	0	0	1			– 10 dB
				1	0	1	0			– 20 dB
				1	0	1	1			– 31 dB
				1	1	X	X			< – 60 dB*

* Power - up configuration

Note : Signalling frequency is a square wave signal at 2982 Hz.

RECEIVE FILTER SELECTION AND GAIN PROGRAMMING REGISTER

RPRF REGISTER

Address				Data				Reception Gain (dB) (note 1)	Comments
D7	D6	D5	D4	D3	D2	D1	D0		
P	1	0	1	X	X	0	0	0	
				X	X	0	1	+ 6 *	
				X	X	1	0	+ 12	
				X	X	1	1	0	Rx Channel Band = Tx Channel Band Tx to Rx Loopback – 33 dBm ≤ Rx Level ≤ –40dBm
				X	0	X	X	X	Receive Filter Selected
				X	1	X	X	X	Receive Filter Desabled
				1	X	X	X	X	Receive Filter Disconnected from RDI Output and from Demodulator. Offset Disabled.

* Power - up configuration.

Note 1 : Depending on the line length, the received signal can be amplified. Programmable reception gain allows setting a level close to + 3dBm at the filter input to take benefit of the maximum filter dynamic range (S / N ratio). The following requirement must be met : Max line level + prog. gain ≤ + 3 dBm.

TRANSMISSION FILTER PROGRAMMING REGISTER

RPTF REGISTER

Address				Data				ATO Transmission
D7	D6	D5	D4	D3	D2	D1	D0	
P	1	0	0	0	0	0	0	MODEM or DTMF Signal*
				0	0	0	1	ATxI via Smoothing Filter and Attenuator
				0	0	1	0	ATxI via Low-pass Filter and Attenuator
				0	0	1	1	ATxI via Band-pass Filter and Attenuator
				0	1	0	0	In DTMF Mode, Transmision of High Tone Frequency
				1	0	0	0	In DTMF Mode, Transmission of Low Tone Frequency

* Power - up configuration.

HYSTERESIS AND SIGNAL DETECTION LEVEL PROGRAMMING REGISTER

RHDL REGISTER

Address				Data				**N2** (dBm) (note 1) See Figure 4	**N1**/**N2** (dB)
D7	D6	D5	D4	D3	D2	D1	D0		
P	1	1	0	X	0	0	0	– 43 *	X
				X	0	0	1	– 41	X
				X	0	1	0	– 39	X
				X	0	1	1	– 37	X
				X	1	0	0	– 35	X
				X	1	0	1	– 33	X
				X	1	1	0	– 31	X
				X	1	1	1	– 29	X
				0	X	X	X	X	3 *
				1	X	X	X	X	3.5

* Power - up configuration.

Note 1 : Detection low level measured at the demodulator input. The line signal detection level is obtained by reducing the gain ate the filter input.

RECEIVE CHANNEL PROGRAMMING REGISTER

RPRX REGISTER

Address				Data				Configuration
D7	D6	D5	D4	D3	D2	D1	D0	
P	1	1	1	X	X	0	X	Low Frequency Wide Band Selected (fig. 4b)*
				X	X	1	X	Low Frequency Narrow Band Selected (fig. 4c)
				X	X	X	0	Carrier Level Detector Delay Enabled*
				X	X	X	1	Carrier Level Detector Delay Disabled.

Note : In active tone detection mode (MOD/$\overline{\text{DTMF}}$ = Ø, MC/$\overline{\text{BC}}$ = 1, $\overline{\text{RTS}}$ = 1 see op. modes), The low frequency wide band is automatically selected for the receive channel, whatever the RPRX register programming value.
After a switch back to modem mode (MOD/$\overline{\text{DTMF}}$ = 1, MC/$\overline{\text{BC}}$ = Ø or 1) the RPRX register indicates again the value programmed before the active tone detection mode.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
DGND	DGND (digital ground) to AGND (analog ground)	– 0.3 to + 0.3	V
V+	Supply Voltage V+ to DGND ro AGND	– 0.3 to + 7	V
V–	Supply Voltage V- to DGND or AGND	– 7 to + 0.3	V
V_I	Voltage at any Digital Input	DGND - 0.3 to V+ + 0.3	V
V_{in}	Voltage at any Analog Input	V– 0.3 to V + + 0.3	V
I_o	Current at any Digital Output	– 20 to + 20	mA
I_{out}	Current at any Analog Output	– 10 to + 10	mA
P_{tot}	Power Dissipation	500	mW
T_{op}	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_{lead}	Lead Temperature (soldering, 10 s)	+ 260	°C

If the Maximum Ratings are exceeded, permanent damage may be caused to the device. This is a stress rating only, and functional operation of the device under these or any other conditions for extended periods may affect device reliability. Standard CMOS handling procedures should be employed to avoid possible damage to the device.

ELECTRIC OPERATING CHARACTERISTICS

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V+	Positive Supply Voltage	4.75	5	5.25	V
V–	Negative Supply Voltage	– 5.25	– 5.0	– 4.75	V
I+	V+ Operating Current	–	10	15	mA
I-	V- Operating Current	– 15	– 10	–	mA

DC AND OPERATING CHARACTERISTICS

Electrical characteristics are guaranteed over the complete temperature range, with typical load except where otherwise indicated. Typical values are given for :

V+ = +5V, V- = -5V and room temperature = 25°C

DIGITAL INTERFACE (MOD / $\overline{\text{DTMF}}$, $\overline{\text{RTS}}$, $\overline{\text{DCD}}$, RxD, ZCO, TxD, MC / $\overline{\text{BC}}$, ENP, PRD)

Symbol	Characteristic		Min.	Typ.	Max.	Unit
V_{IL}	Input Voltage, Low Level		–	–	0.8	V
V_{IH}	Input Voltage, High Level		– 2.2	–	–	–
I_{IL}	Input Current, Low Level	DGND < Vi < VIL (max)	– 10	–	10	µA
I_{IH}	Input Current, High Level	VIH (min) < V_I < V+	– 10	–	10	µA
I_{OL}	Output Current Low, Level	V_{OL} = 0.4 V	1.6	–	–	mA
I_{OH}	Output Current, High Level	V_{OH} = 2.8 V	–	–	– 250	µA

ANALOG INTERFACE-PROGRAMMABLE (ATxI)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{in}	Input Voltage Range	– 1.8	–	+ 1.8	V
I_{in}	Input Current (filter output selected)	– 10	–	+ 10	µA
C_{in}	Input Capacitance (ATT output selected)	–	–	20	pF
R_{in}	Input Resistance (ATT output selected)	100	–	–	kΩ

ANALOG INTERFACE - TRANSMIT OUTPUT (ATO) (load conditions R_L = 560 Ω, C_L = 100 pF)

Symbol	Characteristic	Min.	Typ.	Max.	Unit.
V_{OS}	Output Offset Voltage	– 250	–	+ 250	mV
C_L	Load Capacitance	–	–	100	pF
R_L	Load Resistance	–	560	–	Ω
V_{out}	Output Voltage Swing	– 1.8	–	+ 1.8	V
R_{out}	Output Resistance	10	–	25	Ω
–	ATO Attenuation Ratio when $\overline{RTS}$ = 1	70	–	–	dB

ANALOG INTERFACE - LINE MONITORING (WLO) (load conditions , R_L = 10 kΩ, C_L = 50 pF)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{OS}	Output Offset Voltage	– 250	–	+ 250	mV
C_L	Load Capacitance	–	–	100	pF
R_L	Load Resistance	10	–	–	kΩ
V_{out}	Output Voltage Swing	– 1.8	–	+ 1.8	V
R_{out}	Output Resistance	–	–	15	Ω
–	WLO Attenuation Ratio	70	–	–	dB

ANALOG INTERFACE - DUPLEXER (RAI +, RAI –, RA0)

Symbol	Characteristic		Min.	Typ.	Max.	Unit
V_{in}	Input Voltage Range RAI+, RAI–		– 2	–	+ 2	V
I_{in}	Input Current RAI+, RAI–		– 10	–	+ 10	µA
C_{in}	Input Capacitance RAI+, RAI–		–	–	10	pF
V_{off}	Input Offset Voltage RAI+, RAI–		– 20	–	+ 20	mV
V_{out}	Output Voltage Swing, RA0	C_L = 100 pF, R_L = 600 Ω R_L = 300 Ω	– 1.8 – 0.9	– –	+ 1.8 + 0.9	V V
C_L	Load Capacitance RAO1	C_L = 100 pF	–	–	100	pF
R_L	Load Resistance RA01		300	–	–	Ω
G	DC Voltage Gain in Large Signals, RA01	R_L = 300 Ω C_L = 100 pF	60	–	–	dB
CMRR	Common Mode Rejection Ratio, RA01, RA02		60	–	–	dB
PSRR	Supply Voltage Rejection Ratio, RA01, RA02		60	–	–	dB
V_{out}	Output Voltage Swing, RA02	C_L = 50 pF, R_L = 10 kΩ	– 2.5	–	2.5	V
C_L	Load Capacitance, RA02		–	–	50	pF
R_L	Load Resistance, RA02		10	–	–	kΩ
AV_O	DC Voltage Gain in Large Signals, RA02		60	–	–	dB

ANALOG INTERFACE-RECEIVE FILTER OUTPUT (RFO)

AMPLIFIER LIMITER INPUT (RDI)

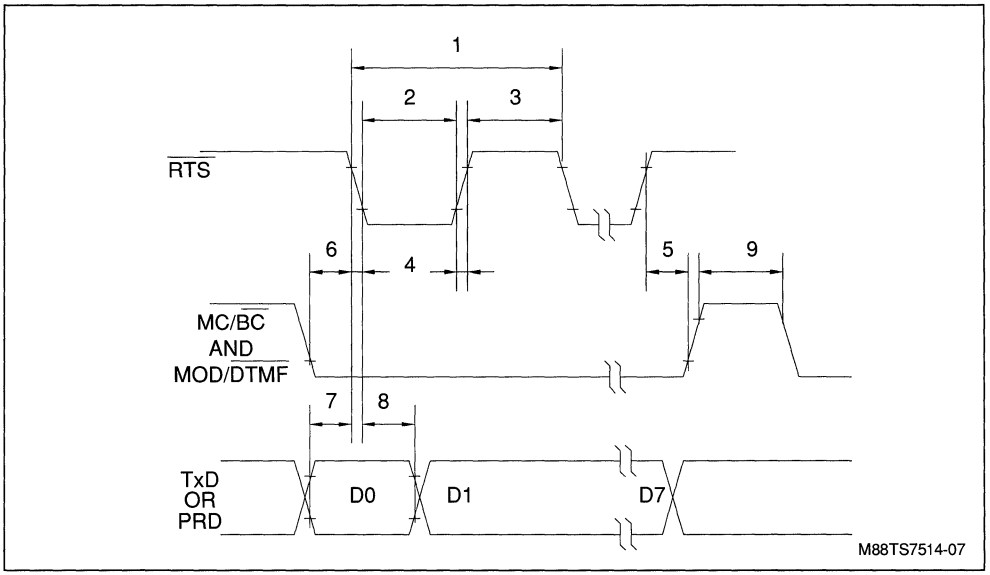
Symbol	Characteristic		Min.	Typ.	Max.	Unit
V_{in}	Input Voltage Range	RPRF = 1 xxx	– 2.2	–	+ 2.2	V
R_{in}	Input Resistance	RPRF = 1 xxx	1.5	–	–	kΩ
C_{in}	Input Capacitance	RPRF = 1 xxx	–	–	20	pF
C_L	Load Capacitance	RPRF = 1 xxx	–	–	50	pF
R_L	Load Resistance		1.5	–	–	kΩ
V_{out}	Output Voltage Swing	R_L = 1.5 kΩ R_L = 50 pF	– 1.8	–	+ 1.8	V
R_{out}	Output Resistance		–	–	15	Ω

DYNAMIC CHARACTERISTICS FOR PROGRAMMING REGISTER ACCESS

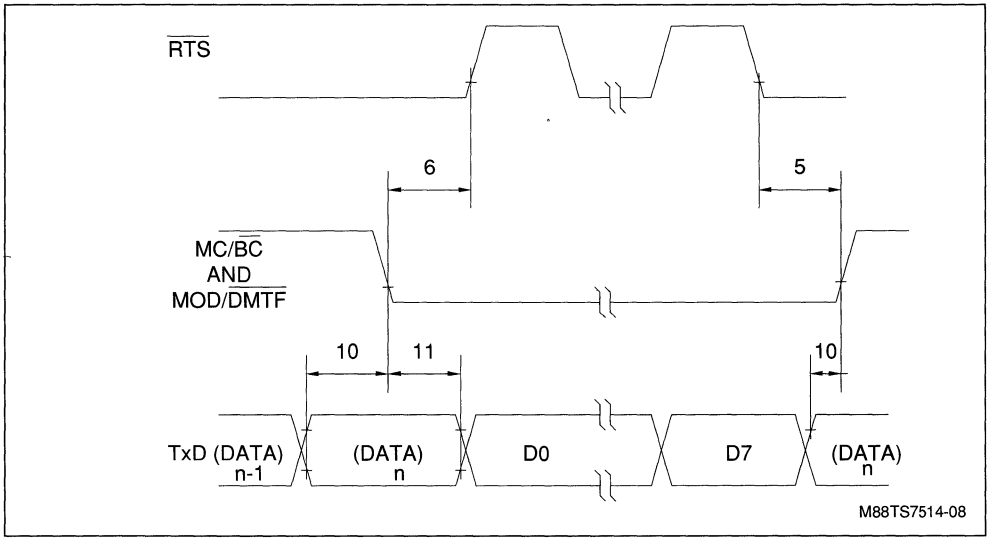
N°	Symbol	Characteristic	Min.	Max.	Unit
1	t_{CYC}	Cycle Time	600	–	ns
2	P_{wel}	Pulse Width, $\overline{RTS}$ Low	300	–	ns
3	P_{Weh}	Pulse Width, $\overline{RTS}$ High	300	–	ns
4	t_r, t_f	$\overline{RTS}$ Rise and Fall Times	–	50	ns
5	t_{HCE}	Control Input Holding Time	100	–	ns
6	t_{SCE}	Control Input Setup Time	300	–	ns
7	t_{SDI}	TxD or PRD Input Setup Time	200	–	ns
8	t_{HDI}	TxD or PRD Input Hold Time	100	–	ns
9	t_{WW}	TWW Input Writing Inpulsion Width (high level)	300	–	ns
10	t_{BD}	TxD Input Setup Time	100	–	ns
11	t_{HD}	TxD Input Hold Time	100	–	ns

INPUT SHIFT REGISTER ACCESS

1st Case : Programmation without Data Transmission.



2st Case : Programmation with TXD During Data Transmission.



TRANSMIT FILTER TRANSFER FUNCTION (load conditions : R_L = 560 Ω, C_L = 100 pF)

Symbol	Parameter		Min.	Typ.	Max.	Unit
G_{AR}	Absolute Gain at 2100 Hz		–	0	–	dB
G_{HH}	Gain Relative to Gain at 1700 Hz					
	Band-pass	< 390 Hz	–	–	– 30	dB
		= 390 Hz	–	–	– 35	dB
		= 450 Hz	–	–	– 35	dB
		= 1100 Hz	– 0.5	–	+ 0.5	dB
	Band-pass or Low-pass	1100 Hz to 2300 Hz	– 0.5	–	+ 0.5	dB
		3300 Hz	–	– 3	–	dB
		5800 Hz	–	–	– 15	dB
		> 16000 Hz	–	–	– 35	dB
D_{AR}	Group Delay : (modem transmission)					
	Main Channel : from 380 to 460 Hz		90	–	110	µs
	Back Channel : from 1100 to 2300 Hz		1.04	–	1.	ms

ATTENUATOR TRANSFER FUNCTION

A_{TT}	Absolute Gain for 0 dB Programmed	0.3	0	0.3	dB
R_{AT}	Attenuation Relative to Programmed Value	- 0.5	-	+ 0.5	dB
	Attenuation for Programmed Value = ∞	70	-		dB
R_{LT}	Relative Attenuation between two Consecutive Steps	0.8	-	1.2	dB

TRANSMIT GENERAL CHARACTERISTICS

Modem Amplitude (Att = 0 dB)				
390 Hz	+ 3.5	–	+ 4.5	dBm
450 Hz	+ 3.5	–	+ 4.5	dBm
1300 Hz	+ 3.5	–	+ 4.5	dBm
2100 Hz	+ 3.5	–	+ 4.5	dBm
DTMF Amplitude (Att = 0 dB) Low Frequency Group	– 3	–	– 1.5	dBm
DTMF Amplitude (Att = 0 dB) Low Frequency Group Versus Low Frequency Group	+ 1.5	–	+ 2.5	dB
Psophometric Noise	–	–	250	µV

RECEIVE FILTER TRANSFER FUNCTION

G_{AR}	Absolute Gain at 1100 Hz - Main Channel (0 dB programmed)	– 0.5	–	+ 0.5	dB
G_{RR}	Gain Relative to the Gain at 1300 Hz (0 dB programmed)				
	< 150 Hz	–	–	– 60	dB
	150 Hz to 450 Hz	–	–	– 50	dB
	1300 Hz	– 0.5	–	0.5	dB
	2100 Hz	1.1	1.8	2.3	dB
	2300 Hz	–	–	2.7	dB
	5500 Hz to 10000 Hz	–	–	– 50	dB
	> 10000 Hz	–	–	– 60	dB

RECEIVE FILTER TRANSFER FUNCTION (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
G_{AR}	Absolute Gain at 420 Hz (back channel - narrow band) (0 dB programmed)	0.5	–	+ 0.5	dB
G_{RR}	Gain Relative to Gain at 420 Hz (0 dB programmed) < 150 Hz	–	–	– 50	dB
	380 Hz	–	–	+ 0.5	dB
	400 Hz to 440 Hz	– 0.5	–	+ 0.5	dB
	460 Hz	–	–	+ 0.5	dB
	1100 Hz to 10000 Hz	–	–	– 50	dB
	> 10000 Hz	–	–	– 60	dB
G_{AR}	Absolute Gain at 425 Hz (tone detection or back channel wide band) (0 dB programmed)	– 0.5	–	+ 0.5	dB
G_{RR}	Gain Relative to Gain at 425 Hz (0 dB programmed) < 112 Hz	–	–	– 50	dB
	275 Hz	–	–	+ 0.5	dB
	300 Hz to 525 Hz	– 0.5	–	+ 0.5	dB
	575 Hz	–	–	+ 0.5	dB
	1375 to 10 000 Hz	–	–	– 50	dB
	> 10 000 Hz	–	–	– 60	dB
	Psophometric Noise	–	–	300	µV

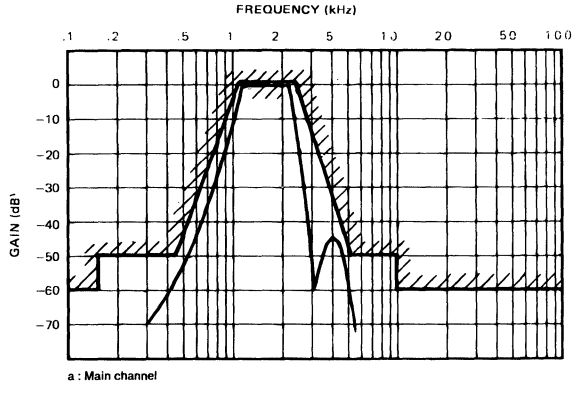
RECEIVE TRANSFER - GENERAL CHARACTERISTICS

	Absolute Filter Gain for : 0 dB programmed 6 dB programmed 12 dB programmed	– 0.5 + 5.5 + 11.5	– – –	+ 0.5 + 6.5 12.5	dB dB dB
R_{DS}	Signal Detection Level Relative to Programmed Value	– 0.5	–	+ 0.5	dB
R_{HY}	Hysteresis Value	– 2	–	–	dB
	Signal Level (loop 3) at Reception Input	– 40	– 35	– 33	dBm

LINE MONITORING - GENERAL CHARACTERISTICS (load conditions : R_L = 10 kΩ, C_L = 50 pF)

A_{TT}	Absolute Gain for 0 dB Programmed	–	0	–	dB
R_{AT}	Attenuation Relative to Programmed Value	– 1	–	+ 1	dB
	Attenuation for Programmed Value	70	–		dB
FS	Buzzer Signalling Frequency	–	2982	–	Hz
	Signalling Frequency Amplitude at : 0.42 V_{PP} Programmed	0.38	0.42	0.46	V_{PP}

Figure 4 : Receive Filter Transfer Characteristics.



a : Main channel

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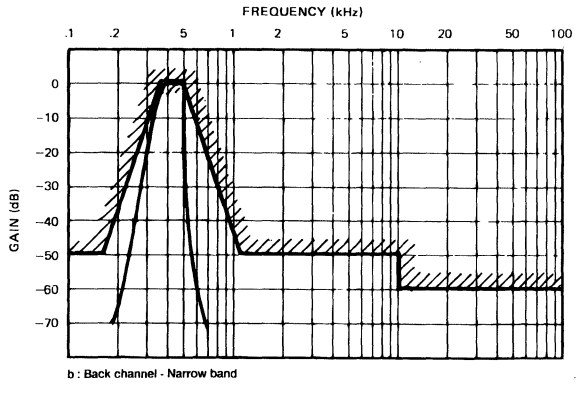
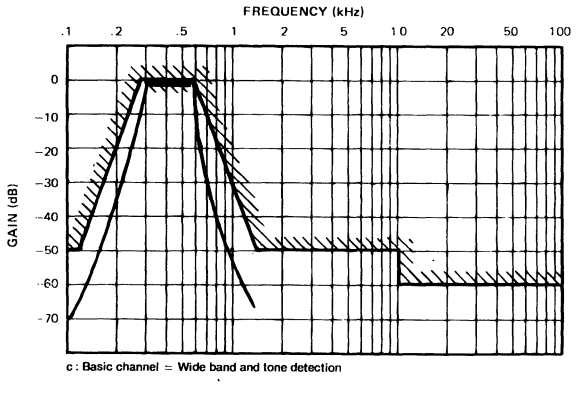


b : Back channel - Narrow band

M88TS7514-10

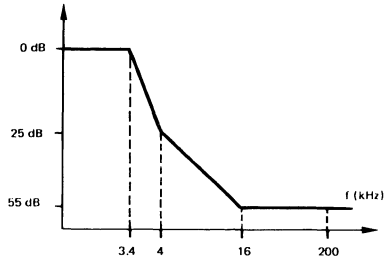


c : Basic channel = Wide band and tone detection

M88TS7514-11

Transmission spectum

At the ATO output, the out-of-band signal power conforms to the following specifications :



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Receiver

Measurement conditions

Local transmit level : -10 dBm on lower channel at 75 bps.

Receive level : -25 dBm, with 511 bit pseudo-random test pattern.

Test equipment : TRT sematest.

Isochronous distortion

The following table shows typical isochronous distortion obtained with the TS 7514 circuit :

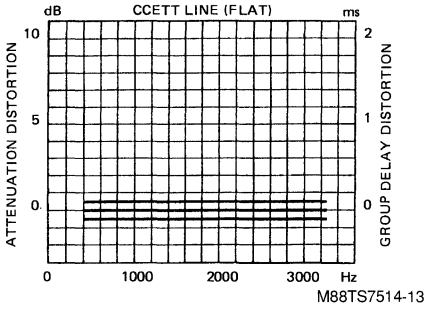
Line	**Reception** (1200)	**Reception** (75)
Line 1 (fiat)	10 %	4 %
Line 2	12 %	4 %
Line 3	18 %	6 %
Line 4	14 %	6 %

Bit error rate

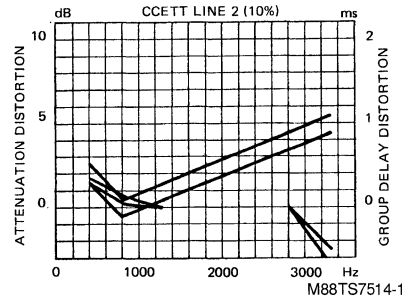
Typical bit error rates versus white noise are as follows (noise and signal levels are measured without weighting on the 300/ 3400 Hz band) :

	Reception (1200 bds)		**Reception** (75 bds)	
	S/N	BER	S/N	BER
Line 1	6 dB	2.10^{-3}	– 3 dB	2.10^{-3}
Line 2	7 dB	2.10^{-3}	– 3 dB	2.10^{-3}
Line 3	8 dB	2.10^{-3}	– 3 dB	2.10^{-3}
Line 4	7 dB	2.10^{-3}	– 3 dB	2.10^{-3}

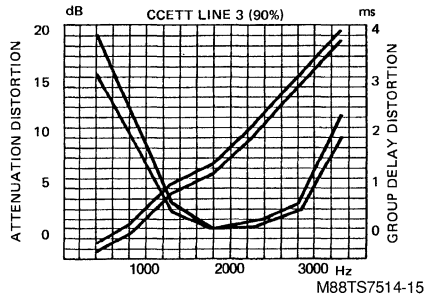
CHARACTERISTICS OF TEST LINES



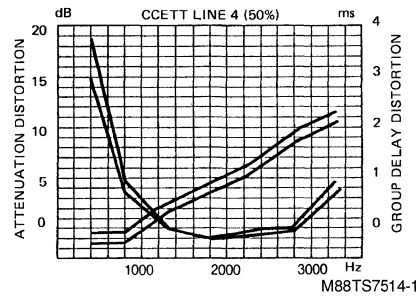
M88TS7514-13



M88TS7514-14



M88TS7514-15



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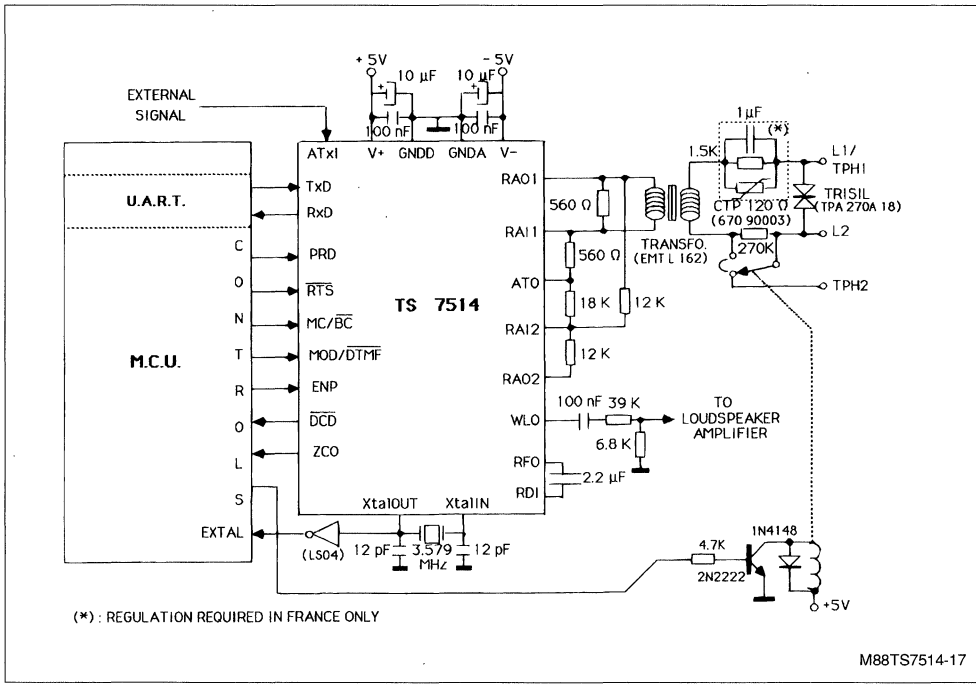
TYPICAL APPLICATION INFORMATIONS



POWER SUPPLIES DECOUPLING AND LAYOUT CONSIDERATIONS

Power supplies to digital systems may contain high amplitude spikes and other noise. To optimize performances of the TS7514 operating in close proximity to digital systems, supply and ground noise should be minimized. This involves attention to power supply design and circuit board layout.

The power supplies should be bypassed with tantalum or electrolytic capacitors to obtain noise free operation. These capacitors should be located close to the TS7514. The electrolytic type capacitors should be bypassed with ceramic capacitors for improved high frequency performance.

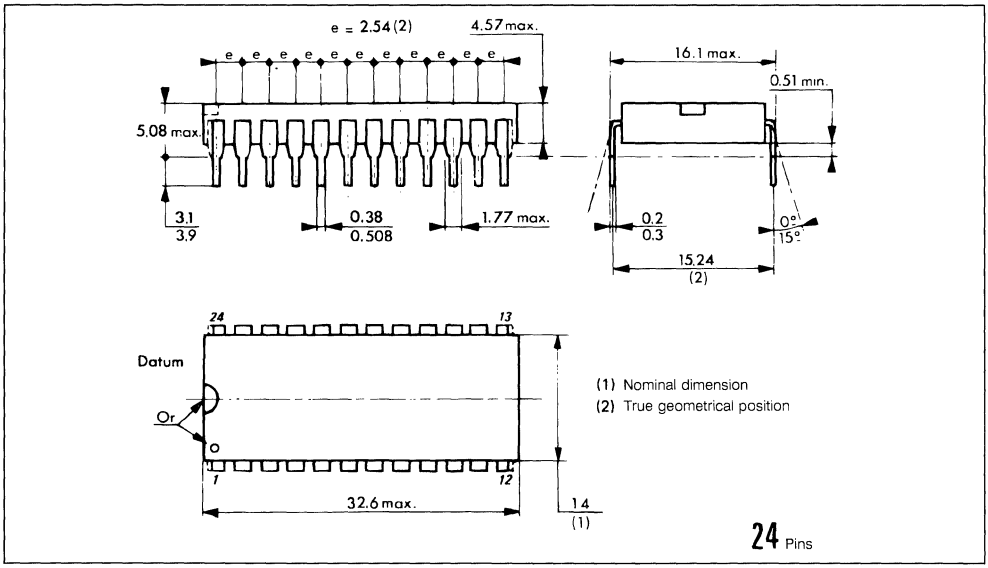
Power supplies connections should be short and direct. Ground loops should be avoided.

ORDER CODES

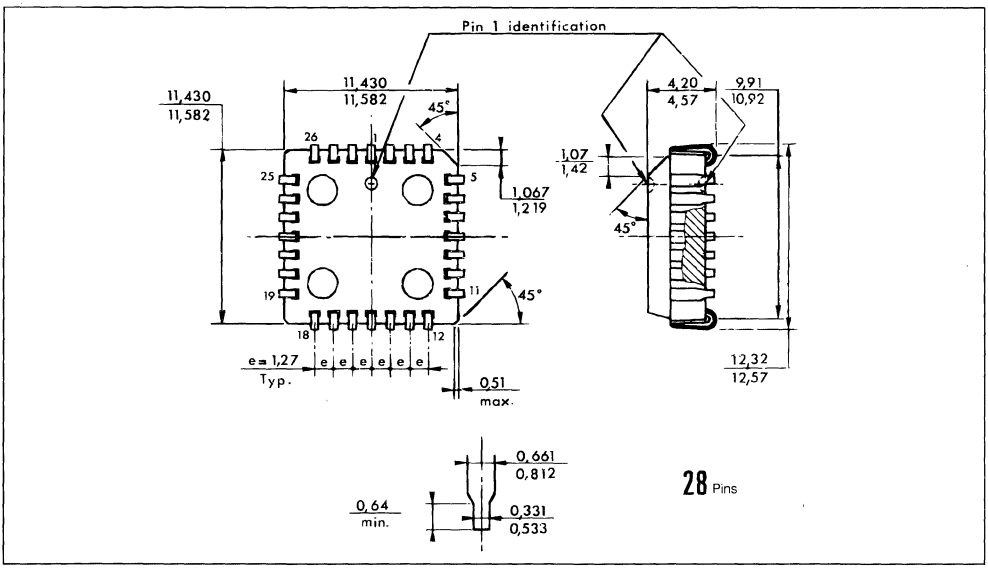
Part Number	Temperature Range	Package
TS7514CP	0 to + 70 °C	DIP 24
TS7514CFN	0 to + 70 °C	PLCC 28

PACKAGE MECHANICAL DATA

24 PINS – PLASTIC DIP



28 PINS – PLASTIC LEADLESS CHIP CARRIER



SINGLE CHIP DPSK AND FSK MODEM

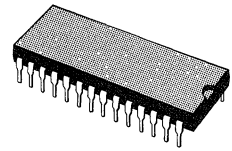
- MONOLITHIC DEVICE (includes both transmit and receive filters)
- MIXING ANALOG AND DIGITAL TECHNICS
- STANDARD LOW COST CRYSTAL (4.9152 MHz)
- AVAILABLE CLOCK FOR MICROPROCESSOR AT 4.9152 MHZ
- LOW POWER DISSIPATION (CMOS technology)
- SHARP ADJACENT CHANNEL REJECTION
- FIXED COMPROMIZE EQUALIZATION IN TRANSMITTER AND RECEIVER
- TEST LOOPS. (local analog, local digital and remote digital loopbacks)
- CARRIER DETECTION OUTPUT
- CCITT AND BELL SIGNALING TONE
- 1200 BPS AND 600 BPS BIT SYNCHRONOUS FORMAT IN DPSK
- 1200 BPS AND 600 BPS + 1 %, - 2.5 % OR + 2.3 %, - 2.5 % CHARACTER ASYNCHRONOUS FORMAT (8, 9, 10 or 11 bits) IN DPSK
- 0 TO 300 BPS IN FSK
- AUTOMATIC DIAL LINE MONITORING CAPABILITY
- BREAK SIGNAL SUPERVISION
- EXTERNAL VOICE BAND TONE FILTERING AVAILABLE (i.e. 550 Hz or DTMF)
- CMOS AND TTL COMPATIBLE
- DIRECT INTERFACE TO STANDARD MICROPROCESSOR FAMILIES

DESCRIPTION

The TS7515 is a single chip DPSK and FSK voice–band modem, compatible with the BELL 103, 212A and CCITT V.22 A/B recommended standards.

MAIN OPERATING MODES

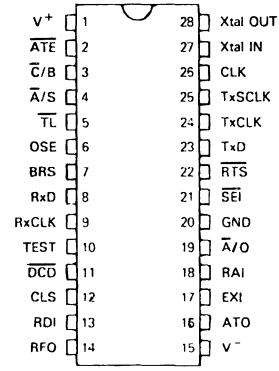
- STANDARD SELECTION (BELL 212A/BELL 103/V22)
- ANSWER TONE SELECTION (2100 or 2225 Hz)
- LOW SPEED MODE SELECTION
- CHANNEL SELECTION (answer/originate)
- SYNCHRONOUS/ASYNCHRONOUS MODE SELECTION
- 8 BITS TO 11 BITS WORD LENGTH SELECTION IN CHARACTER ASYNCHRONOUS FORMAT MODE
- OVERSPEED SELECTION IN CHARACTER ASYNCHRONOUS FORMAT MODE
- SCRAMBLER SELECTION
- 1800 Hz GUARD TONE SELECTION IN V.22
- TEST LOOP SELECTION (DIGITAL/ANALOG)



P
DIP28
(Plastic Package)

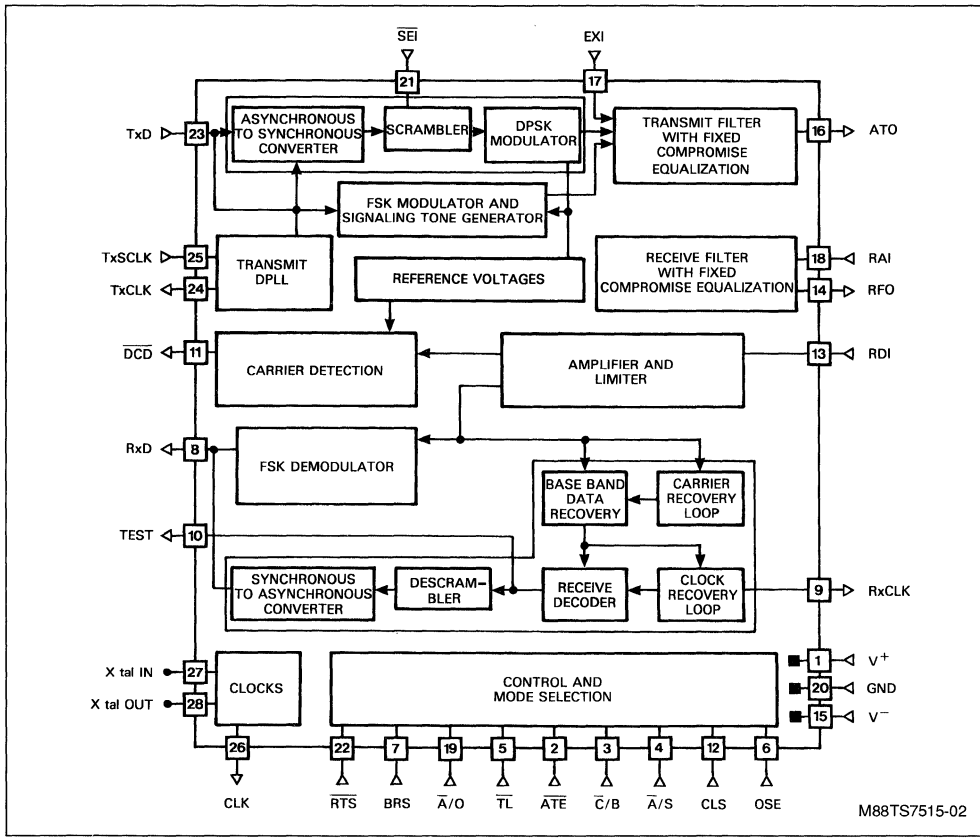
(Ordering Information at the end of the Datasheet)

PIN CONNECTION



M88TS7515-01

BLOCK DIAGRAM



PIN DESCRIPTION

COMMON SECTION (supply, clock, handshaking and mode selection)

Name	Pin Type	N°	Function	Description
V^+	I	1	Positive Power Supply	+ 5 V
V^-	I	15	Negative Power Supply	– 5 V
GND	I	20	Ground	0 V
XIN	I	27	Oscillator Input	This pin corresponds to the input of the oscillator. It is normally connected to an external crystal but may also be connected to a pulse generator. The nominal frequency of the oscillator is 4.9152 MHz.
XOUT	O	28	Oscillator Output	This pin corresponds to the output of an inverter with sufficient loop gain to start and maintain the crystal oscillating.
CLK	O	26	Clock	This pin delivers a clock signal, the frequency of which is the crystal frequency. It may be used as a buffered clock a microcontroller.
$\overline{C}$/B	I	3	CCITT/BELL Selection	This three-state input selects the features corresponding to CCITT or BELL recommandation.
$\overline{A}$/S	I	4	Synchronous/ Asynchronous Selection	This three-state input selects the synchronous bit format or the asynchronous character format mode in DPSK transmission. This input allows also character length selection (refer to table 8).
CLS	I	12	Character Length	This input selects the character length in conjunction with $\overline{A}$/S input (refer to table 8).
OSE	I	6	Over-speed Selection	This input selects the over-speed in asynchronous character format mode required by CCITT recommandation (refer to table 8).
BRS	I	7	Binary Rate Selection	A Logic "0" on this input turns chip on1200 bps rate. A logic "1" turns the chip on 600 bps or 0-300 bps according to $\overline{C}$/B selection.
$\overline{A}$/O	I	19	Answ./Orig. Selection	A logic "0" on this input turns the chip on answer mode. A logic "1" turns the chip on originate mode.
$\overline{TL}$	I	5	Test Loop Selection	This three-state input, selects the test loops mode (refer to table 6).

PIN DESCRIPTION (continued)

TRANSMIT SECTION

Name	Pin Type	N°	Function	Description
TxD	I	23	Transmit Data	Data bits to be transmitted are serially presented on this input. A mark corresponds to a logic "1" and a space to a logic "0". This data determines which phase or frequency appears at any instant at the ATO pin in DPSK or FSK modes.
ATO	O	16	Analog Transmit Output	The analog output is the modulated carrier or the answer tone to be conditionned and sent over the phone line mixed with the filtered signal from EXI.
EXI	I	17	External Tone Input	This analog input allows external tone to be filtered by an internal low-pass filter. Filtered signal appears at ATO whatever $\overline{RTS}$.
$\overline{ATE}$	I	2	Answer Tone Enable	A logic "0" on this input instructs the chip to enter answer signaling tone mode according C/B selection. A logic "1" turns the chip on transmit data mode (refer to table 9).
$\overline{SEI}$	I	21	Scrambler Enable Input	A logic "0" on this input enables the internal scrambler. A logic "1" instructs the chip to bypass the scrambler.
TxCLK	O	24	Transmit Clock from Modem	This output delivers a transmit bit clock generated by chip in synchronous mode. When TxSCLK is used, TxCLK is locked on TxSCLK. This output generates a logic "1" in asynchronous mode.
TxSCLK	I	25	Transmit Clock from Terminal	This input receives a bit clock supplied by the DTE. This clock synchronizes the internal transmit clock of the chip. In line monitoring mode this input receives the filters clock.
$\overline{RTS}$	I	22	Request to Send Terminal	When a logic "0" is present on this input, the chip delivers on ATO a modulated signal or a signaling tone and the filtered signal from EXI. When a logic "1" is present on this input, ATO delivers only the filtered signal from EXI. When a logic "– 1" is present on this input, the receive section may be used for line monitoring and ATO delivers only the filtered signal from EXI.

PIN DESCRIPTION (continued)

RECEIVE SECTION

Name	Pin Type	N°	Function	Description
RAI	I	18	Receive Analog Input	This input receives the analog signal from the hybrid. It corresponds to the input of the receive filters.
RFO	O	14	Receive Filter Output	This analog output is the signal received on RAI once filtered. The receive filter also equalizes the signal for adaptation to most existing lines. This output must be connected to RDI through a capacitor to meet the level detection conditions.
RDI	I	13	Receive Demodulator Input	This pin is the input of the carrier detection logic and of the demodulator
$\overline{DCD}$	O	11	Data Carrier Detect	A logic "0" on this output indicates that a valid carrier signal is present on RAI. A logic "1" means that no valid signal is being received. The hysteresis meet standards recommendation.
RxD	O	8	Receive Data	Data bits demodulated are available serially at this output.
RxCLK	O	9	Receive Clock	This output delivers a receive bit clock generated by the chip. In asynchronous mode this clock is 16 times the modulation rate. In synchronous mode the clock is equal to the bit rate.
TEST	O	10	Test	This output is an intermediate demodulator output intented for handshake and test purposes.

The TS7515 is a general purpose monolithic DPSK and FSK modem implemented with double poly CMOS process. It is capable of generating and receiving phase modulated signals at data rates of 1200 bps or 600 bps as well as frequency modulated signals at data rates up to 300 bps on voice-grade telephone lines. It is offered in a 28 or 44 in plastic package and is able to operate in full-duplex mode according to three pin selectable standards :

- CCITT V22 A-B.
- Bell 212A with its low speed mode ;
- Bell 103.

All filtering functions required for frequency generation, out-of-band noise rejection and demodulation are performed by on-chip switched capacitor filters. In phase modulation the modem provides all data buffering and scrambling functions necessary for bit synchronous format and asynchronous character format modes of operation. Internal frequencies are generated from a 4.9152 MHz crystal reference.

DEVICE OPERATION

TRANSMITTER

The transmitter consists of two analog signal generators followed by switched capacitor and continuous filters. In phase modulation operation mode the DPSK signal generator is preceded by a selectable scrambler and an asynchronous to synchronous converter is included in character asynchronous format mode.

Tone allocation : the modem on the end of the line which initiates the call is called the originate modem. In normal transmission operation it transmits in low channel and receives in high channel. The other modem is the answer modem which transmits in high channel and receives in low channel.

MODULATORS

DPSK modulator : the phase modulation type is differential quadrature four phase shift keying (see table 1). The 1200 bps data stream to be transmitted is converted into two 300 dibits per second streams which modulate alternatively two independant carriers. Consequently the base band shaping is included is a 5 bit address ROM which generates samples for a 8 bit switched capacitor DAC at a frequency equals to 8 times the carrier frequency.

Table 1 : DPSK Modulation.

BRS	TxD		Phase Shift
	n – 1	n	
0	0	0	+ 90 °
		1	0 °
	1	1	+ 270 °
		0	+ 180 °
1	X(*)	0	+ 90 °
		1	+ 270 °

(*) x : don't care.

FKS modulator and tone generator : a frequency synthesizer provides accurate clocks to a switched capacitor sine wave generator (see table 2). Phase continuity is maintained when a frequency shift occurs.

Table 2 : FSK Modulation (BELL 103).

$\overline{A}$/0	TxD	Standard frequency
0	0	2025 Hz
	1	2225 Hz
1	0	1070 Hz
	1	1270 Hz

TRANSMIT FILTERS

To avoid unwanted frequency components to be echoed by the hybrid in the reception path, to maintain the level of spurious out-of-band signals transmitted to the telephone line below the limits specified by administrations (see figure 1) and to complete statistical amplitude and phase equalization, the analog signals are processed by ten poles sharp pass-band switched capacitor filters. The response of these filters depends on the selected channel (Answer/Originate) and the selected standard (BELL 212 - V.22 BELL 103). A continuous filter eliminates parasitic sampling effects. An additional low-pass filter input is provided. This allows to mix and filter such tones as DTMF signals or special guard tones (550 Hz) to the transmitted signal.

SCRAMBLER

The scrambler used during phase modulation ensures the transmission of a continuously changing pattern. This avoids the receiving modem to drop out of lock on certain continuous repetitious data patterns.

This scrambler may be disabled during handshaking procedures. In V.22 a special unlocking sequence is performed on 64 spaces pattern at scrambler output.

ASYNCHRONOUS TO SYNCHRONOUS CONVERTER

The DPSK signal is synchronous in nature but the modem has both an asynchronous as well as a synchronous mode of operation in DPSK. So a data buffer is necessary to convert variable rate asynchronous character data to an equivalent bit oriented synchronous data stream. This is done by inserting or deleting stop bits. If serial input data contains a break signal through one character (including start and stop bits). One break will be extended to at least 2 * M + 3 bits long (where N is the number of transmitted bit/character).

Figure 1 : Transmitted Signal Template.

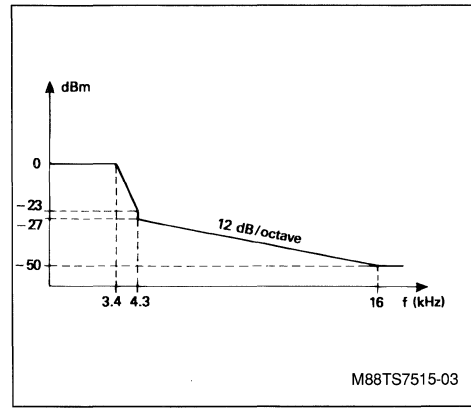


Table 3 : Output Frequency Deviation.

Standard Frequency	Frequency using 4.91 MHz	% Deviation from Standard	Mode
1070 Hz	1066.7 Hz	– 0.3 %	BELL 103 Originate
1200 Hz	1200 Hz		BELL 212A or V22, Originate
1270 Hz	1269.4 Hz	– 0.05 %	BELL 103 Originate
1800 Hz	1807.1 Hz	+ 0.4 %	Guard Tone V22
2025 Hz	2021 Hz	– 0.2 %	BELL 103 Answer
2100 Hz	2104. 1 Hz	+ 0.2 %	Answer Tone CCITT
2225 Hz	2226. 1 Hz	+ 0.05 %	BELL 103 Answer or Answer Tone BELL
2400 Hz	2400 Hz		BELL 212A or V22, Answer

RECEIVER

The receiver includes two band-pass filters followed by an amplifier and a hard limiter. Depending on selected standard, the detector output is passed through a DPSK demodulator or a FSK demodulator. The DPSK demodulator is followed by a descrambler and a selectable synchronous to asynchronous converter. In addition a carrier detector monitors the level of the received signal.

Tone allocation : in normal transmission operation the originate modem receives in high channel and transmits in low channel. The answer modem receives in low channel and transmits in high channel.

RECEIVE FILTERS

The signal delivered by the hybrid to the receive analog input is a mixture of transmitted signal, received signal and noise with a level in the range from - 48 dBm to - 0 dBm. Depending on the operating mode and the selected standard the 20 poles receive switched capacitor band-pass filter selects the frequency band of the low channel or the high channel. A ratio of 14/15 is applied on the sampling clock frequency between FSK and DPSK in the same operating mode (Answer/Originate). These filter reject out-of-band transmission noise components and undesirable adjacent channel echo signals which can be fed from the transmit section into the receive section. Fixed equalization is included in order to assure low error rate.

AMPLIFIER AND HARD LIMITER

Once filtered the received signal is amplified and fed to the carrier detector. In order to limit analog parts in the design all the demodulator techniques used in the TS7515 are based on zero crossing detection. So the received signal is just limited before entering demodulator.

DEMODULATORS

DPSK demodulator : a DPLL is used to recover the carrier signal. This DPLL has a lock range of ± 2 Hz but as the incoming carrier may present an offset of ± 7 Hz a second loop allows the first DPLL to lock on the exact frequency of the carrier with an accuracy of ± 1 Hz and to follow its slow variations in 1200 bands mode only. Then the limited received signal is mixed through exclusive-Or with the recovered carrier and with the 90 degrees phase shifted recovered carrier. The results are processed through four poles Bessel filters wich provide a good amplitude propagation time compromise. The received sampling clock recovered from these base and data with a simple DPLL. The received data are sampled by this clock and then converted into a serial synchronous bit stream.

FSK demodulator : the zero crossing detector output is passed through a shift register whose length depends on the operating mode (Answer/Originate). The output of the shift register and the detector are mixed into an exlusive Or. Then they are processed through a four poles Bessel filter and a slicer.

TEST OUTPUT

Once demodulated DPSK data are generally processed (cf next paragraph) but during call set-up procedures or data set testing it is of importante to monitor the demodulator output. So in DPSK mode demodulated data are available on TEST pin.

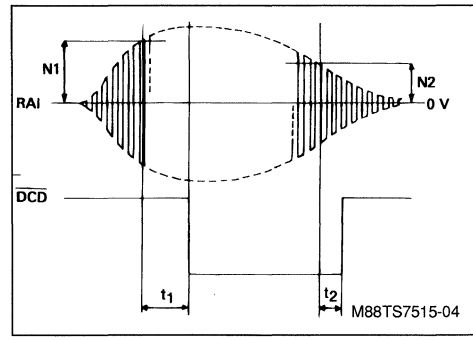
DESCRAMBLER AND SYNCHRONOUS TO ASYNCHRONOUS CONVERTER

Data coming from the DPSK demodulator are unscrambled. In V.22 the unlocking sequence is detected at descrambler input and the original data are

decoded before descrambling. In asynchronous character format mode of operation a data buffer is able to detect missing stop bits and reinsert them. The converter is able to recognize the break signal and transmits it without modification.

CARRIER DETECTOR

Whenever valid signals are being received at the input of the demodulator and are acceptable for demodulation, carrier detect output is pulled down. A delay is timed out before the carrier received or carrier lost signal changes carrier detect output to provide immunity against noise bursts. The modem also provides at least 2 dB of hysteresis between the carrier ON and the carrier OFF thresholds (see diagram below).



In DPSK mode 105 ms ≤ t1 ≤ 205 ms 10 ms ≤ t2 ≤ 24 ms
In FSK mode 105 ms ≤ t1 ≤ 205 ms 25 ms ≤ t2 ≤ 75 ms

LOOP TEST

LOOP 3

This loop is called the analog loop. When it is selected the receive filters and the modulators are configured to process the same channel as the transmit section. The transmit carrier has to be looped back externally to the receive analog input. This loop allows the user or the DTE to check the satisfactory working of the local DCE.

LOOP 2

This loop is called the digital loop. When it is selected received data, receive clock and data carrier detect signals are respectively and internally looped back on transmit data, transmit clock from terminal and request to send . This loop allows the user or the DTE to check the satisfactory working of the line and the remote DCE.

CLOCKS

In synchronous mode of operation TxCLK, TxSCLK and RxCLK are respectively working as the V.24 circuits C114, C13 and C15. In asynchronous mode of operation RxCLK can be used as baud rate clock to synchronize the transmit and the receive sections of a UART (see table 4).

OSCILLATOR OUTPUT

The buffered master clock (4.9152 MHz) is made available at output CLK. It can be used as a clock for a microcontroller.

VOLTAGE REFERENCE

A temperature compensated voltage reference build with a zener is included in the chip. This voltage is used to calibrate transmit levels and to generate the carrier detection thresholds.

Table 4 : Clock Operation.

$\overline{A}$/S	$\overline{C}$/B	BRS	TxCLK	RxCLK	Mode
– 1 ou 0	– 1 ou 0	0	1	19.2 kHz	V.22 Asynchronous
		1	1	9.6 kHz	
	1	0	1	19.2 kHz	BELL 212A Asynchronous and BELL 103
		1	1	4.8 kHz	
1	– 1 ou 0	0	1200 Hz	1200 Hz	V.22 Synchronous
		1	600 Hz	600 Hz	
	1	0	1200 Hz	1200 Hz	BELL 212A Synchronous and BELL 103
		1	1	4.8 kHz	

LINE MONITORING

A special mode has been included in the TS7515 to monitor the line during an automatic call. When this mode is selected (A/S = 0, RTS = - 1) receive filters clock is directly derived from TxSCLK which allows the user to precisely observe broad frequency bands. Furthermore the DCD performs a fast carrier detection equivalent to an envelope detection. As the center frequency of the receive filters is proportional to TxSCLK frequency in this mode it is possible to tune the passband according to the frequency to be detected (see table 5).
TxSCLK : must be created from the TS7515 master clock (4.9152 MHz).

Table 5.

TxSCLK	Originate ($\overline{A}$/O = 1)		Answer ($\overline{A}$/O = 0)		Application
	Center Frequency	Passband at 3 dB	Center Frequency	Passband at 3 dB	
210 kHz	2400 Hz	± 400 Hz	1200 Hz	± 400 Hz	Voice Detection
45 kHz	510 Hz	± 85 Hz			440 Hz Detection
			260 Hz	± 85 Hz	330 Hz Detection
76.8 kHz			440 Hz	± 150 Hz	Dial Tone and Busy Tone Detection

APPLICATION INFORMATION

In a typical application a microcontroller provides control and interface to the Data Terminal Equipment (DTE), and a Direct Access Arrangement provides connection to the telephone line. Then the TS7515 can communicate with the most popular modems (BELL 103 and BELL 212A) in countries under BELL standards and popular modems (V.22) in countries under CCITT recommendations.

POWER SUPPLIES DECOUPLING AND LAYOUT CONSIDERATIONS

Power supplies to digital systems may contain high amplitude spikes and other noise. To optimize performances of the TS7515 operating in close proximity to digital systems, supply and ground noise should be minimized. This involves attention to power supply design and circuit board layout.

The power supplies should be bypassed with tantalum or electrolytic capacitors to obtain noise free operation. These capacitors should be located close to the TS7515. The electrolytic type capacitors should be bypassed with ceramic capacitors for improved high frequency performance.

Power supplies connections should be short and direct. Ground loops should be avoided.

Coupling between analog inputs and digital lines should be minimized by careful layout. The RDI input (pin 13) is extremely sensitive to noise.

The connection between this point and RFO (pin 14) through a ceramic type capacitor should be as short as possible and coupling between this connection and digital signals should be minimized by careful layout.

CARRIER RECOVERY LOOP

The carrier recovery loop utilizes a digital phase lock loop. Performances of the TS7515 depend directly on this DPLL which needs to be resetted before receiving a DPSK carrier.

Three ways of resetting the DPLL exist on the TS7515 :

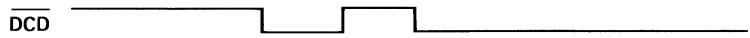
- A trailing edge on $\overline{DCD}$.
- Changing FSK mode to DPSK mode or reversely.
- Changing receive channel .

These three ways of resetting the DPLL should be used in the software included in the microcontroller to perform the various set-up procedures and handshakes.

EXAMPLES

• V.22-V.25 received signals in Originate mode.

Line ——— ( ) ( ) ( ) ——— [2100 Hz] ——— [unscrambled marks 2400 Hz] [data...



The DPLL is automatically resetted

© Bell 212A received signals in Originate mode.

Line ——— ( ) ( ) ( ) ———[2225 Hz] [scrambled marks 2400 Hz] [data...

This transition to "1" is needed to reset the DPLL

TYPICAL PERFORMANCES

The typical performances listed below are achieved with the environment described in the previous paragraph.

• Dynamic range : 0 dBm to - 45 dBm.

• BER performances :

Conditions : Xmit level = - 10 dBm,
Rec level = - 25 dBm,
Message 511 bits
on CCETT lines 1, 2, 3, 4
and CNET lines QN and 3 VHF
and US lines C4, C2, and C0.
1200 bps operation

BER 10^{-3} for a 7 dB SNR

BER 10^{-6} for a 11 dB SNR

300 bps operation

BER 10^{-3} for a 3 dB SNR

BER 10^{-6} for a 8 dB SNR

• Specific DPSK performances

Phase hits sensitivity : 25 degree
Phase Jitter : 35 degree
} BER < 10^{-6}

Amplitude hits sensitivity : ± 10 dB

Offset carrier sensitivity : SNR increase < + 1 dB

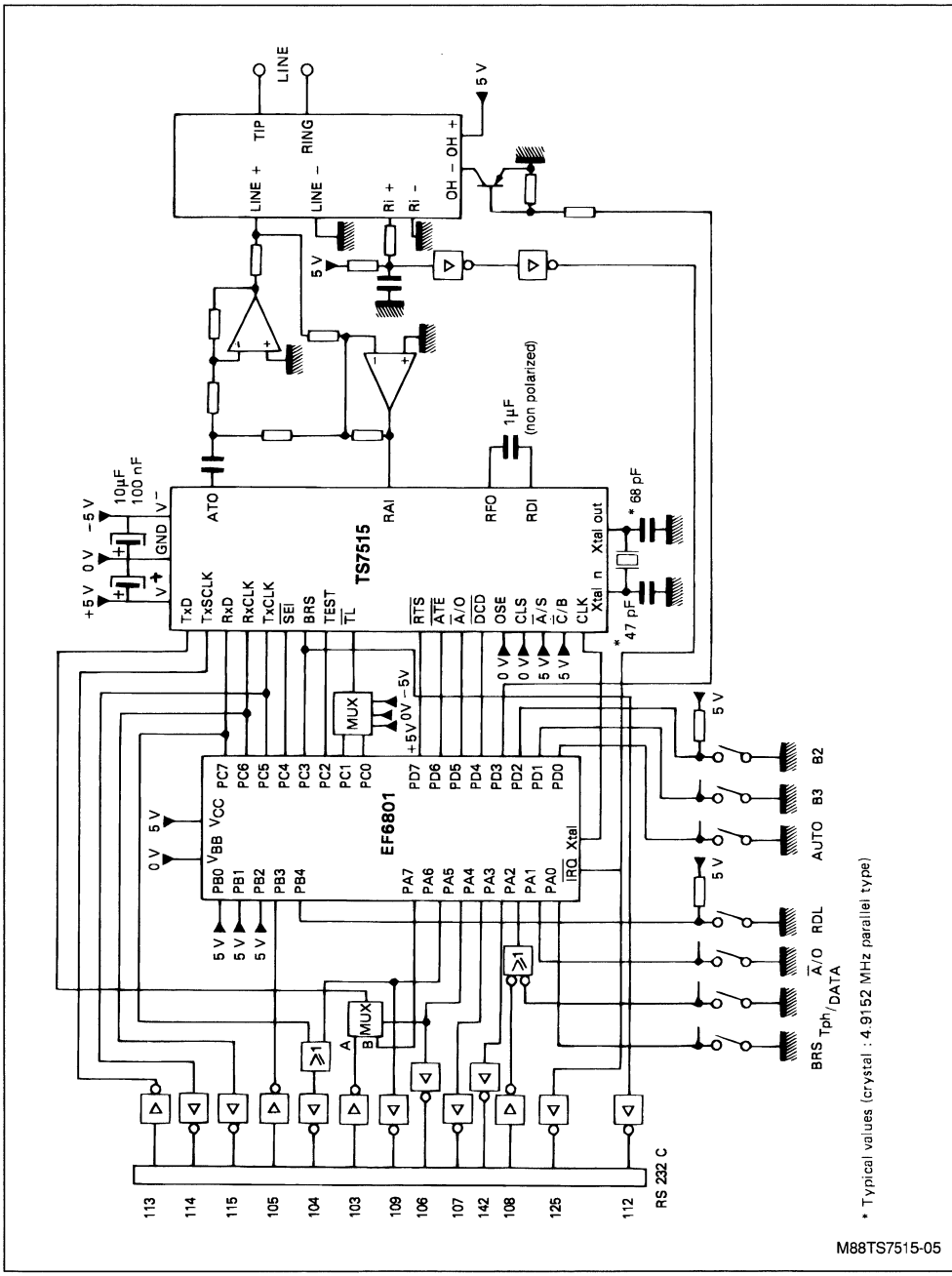
1800 Hz guard tone sensitivity : SNR increase < + 2 dB

• Specific FSK performances

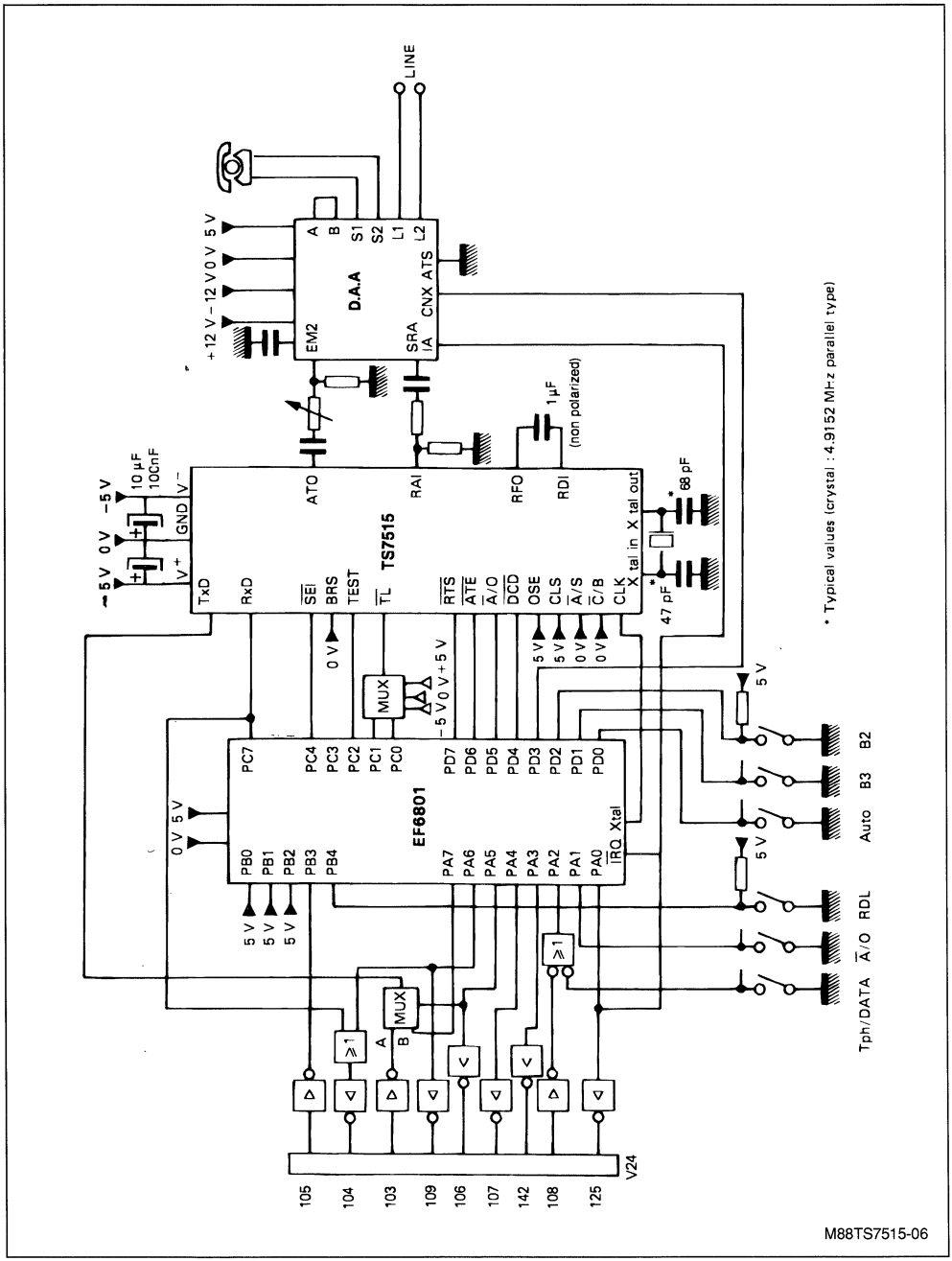
Bias Distortion : less than 5 %

Jitter : less than 12 %

BELL 212A APPLICATION : (synchronous)



V.22 (asynchronous, 10 bits, 1200 bps)



SELECTION MODE TABLES

SYNTHESIS OF DIFFERENT MODES FOR RECEIVE SECTION

Table 6.

$\overline{C}$/B	BRS	$\overline{TL}$	$\overline{A}$/0	Receive	Mode
– 1 ou 0	X	– 1	0	DPSK Originate Loop 3	V. 22
			1	DPSK Answer Loop 3	
		0	0	DPSK Answer Loop 2	
			1	DPSK Originate Loop 2	
		1	0	DPSK Answer	
			1	DPSK Originate	
1	0	– 1	0	DPSK Originate Loop 3	BELL 212 A Including BELL 103
			1	DPSK Answer Loop 3	
		0	0	DPSK Answer Loop 2	
			1	DPSK Originate Loop 2	
		1	0	DPSK Answer	
			1	DPSK Originate	
	1	– 1	0	FSK Originate Loop 3	
			1	FSK Answer Loop 3	
		0	0	FSK Answer Loop 2	
			1	FSK Originate Loop 2	
		1	0	FSK Answer	
			1	FSK Originate	

Answer : Receive in low channel
Originate : Receive in high channel
Loop 3 : Analog loop
Loop 2 : Digital loop

SELECTION MODE TABLES (continued)

SYNTHESIS OF DIFFERENT MODES FOR TRANSMIT SECTION

Table 7.

$\overline{ATE}$	C/B	BRS	A/0	Transmit	Mode
0	– 1 ou 0	X	X	2100 Hz	Answer Tone
	1			2225 Hz	
1	– 1	0	0	DPSK 1200 bps Answer	V.22 without Guard Tone
			1	DPSK 1200 bps Originate	
		1	0	DPSK 600 bps Answer	
			1	DPSK 600 bps Originate	
	0	0	0	DPSK 1200 bps Answer	V.22 with 1800 Hz Guard Tone
			1	DPSK 1200 bps Originate	
		1	0	DPSK 600 bps Answer	
			1	DPSK 600 bps Originate	
	1	0	0	DPSK 1200 bps Answer	BELL 212A
			1	DPSK 1200 bps Originate	
		1	0	FSK 0-300 bps Answer	
			1	FSK 0-300 bps Originate	

Answer : Transmit in high channel
Originate : Transmit in low channel

MODE SELECTION IN PHASE MODULATION TRANSMISSION

Table 8.

A/S	CLS	OSE	Transmission Mode	Length	Over-speed
– 1	0	0	Asynchronous	8	+ 1 %, – 2.5 %
		1			+ 2.3 %, – 2.5 %
	1	0		11	+ 1 %, – 2.5 %
		1			+ 2.3 %, – 2.5 %
0	0	0		9	+ 1 %, – 2.5 %
		1			+ 2.3 %, – 2.5 %
	1	0		10	+ 1 %, – 2.5 %
		1			+ 2.3 %, – 2.5 %
1	0	0	Synchronous		

SELECTION MODE TABLES (continued)

TEST PIN

Table 9.

$\overline{ATE}$	$\overline{C}$/B	BRS	Transmit	Receive	Test
0	– 1 ou 0	0	2100 Hz	V.22 DPSK 600 bps	DDO
		1		V.22 DPSK 1200 bps	DDO
	1	0	2225 Hz	BELL 212A DPSK 1200 bps	DDO
		1		BELL 103 FSK 0-300 bps	HLO
1	– 1	0	V.22 without Guard Tone DPSK 1200 bps		DDO
		1	V.22 without Guard Tone DPSK 600 bps		DDO
	0	0	V.22 with Guard Tone DPSK 1200 bps		DDO
		1	V.22 with Guard Tone DPSK 600 bps		DDO
	1	0	BELL 212A DPSK 1200 bps		DDO
		1	BELL 103 FSK 0-300 bps		HLO

DDO : DPSK demodulator output
HLO : Hard limiter output

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V^+	Supply Voltage	+ 7	V
V^-	Supply Voltage	– 7	V
V_{in}	Analog Input Range	$V^- < V_{in} < V^+$	V
V_i	Digital Input Range (except three-state inputs)	$GND < V_i < V^+$	V
V_{i3}	Three-state Input Range	$V^- < V_{i3} < V^+$	V
T_A	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	– 55 to 125	°C
T_S	Pin Temperature (soldering, 10 s)	260	°C

Stresses above those listed under "Absolute maximum ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions for extended periods may affect device reliability. Standard CMOS handling procedures should be employed to avoid possible damage to device.

ELECTRICAL OPERATING CHARACTERISTICS

Symbol	Parameter	Min.	Nom	Max.	Unit
V^+	Positive Supply Voltage	4.75	5	5.25	V
V^-	Negative Supply Voltage	– 5.25	– 5	– 4.75	V
I^+	V^+ Operating Current	–	10	30	mA
I^-	V^- Operating Current	– 20	– 7	–	mA

D.C. AND OPERATING CHARACTERISTICS

TA = 0°C to + 70°C, V^+ = + 5 V ± 5 %, V^- = – 5 V ± 5 %, GND = 0 V

DIGITAL INTERFACE

Symbol	Parameter	Min.	Typ. *	Max.	Unit
I_L	Input Current (V_{IL} min < V_I < V_{IH} max)	– 50	–	50	µA
I_{OL}	Output Low Level Current (V_{OL} = 0.4 V)	800	–	–	µA
I_{OH}	Output High Level Current (V_{OH} = 2.4 V)	–	–	– 40	µA
V_{IL}	Input Low Voltage	GND	–	0.8	V
V_{IH}	Input High Voltage	2	–	V^+	V
V_{in}	Input Negative Voltage	V^-	–	– 4	V

ANALOG INTERFACE, FILTERS INPUTS AND OUTPUTS (RAI–RFO, EXI–ATO)

Symbol	Parameter	Min.	Typ. *	Max.	Unit
I_L	Input leakage Current (– 3 V < V_{IN} < + 3 V)	– 10	–	10	µA
R_I	Input Resistance		3	–	MΩ
V_{IN}	Input Voltage Swing	– 3	–	+ 3	V
V_{OF}	Output Offset Voltage	– 500	–	+ 500	mV
V_{OS}	Output Voltage Swing (R_L > 10 kΩ)	– 2	–	+ 2	V
O_L	Load Capacitance	–	–	20	pF
R_L	Load Resistance	10	–		kΩ
D	Signal Distortion		– 40		dB

ANALOG INTERFACE, TRANSMIT OUTPUT (ATO) EXI Connected to GND

Symbol	Parameter	Min.	Typ. *	max.	Unit
V_{OF}	Output Offset Voltage	– 500	–	+ 500	mV
V_O	Output Voltage Swing (R_L/10 kΩ, C_L = 20 pF) Carriers	–	2.2	–	V_{pp}
V_O	Guard Tone 1800 Hz/Data Signal	– 7	– 6	– 5	dB
A_T	$\overline{RTS}$ Attenuation	55	–	–	dB

ANALOG INTERFACE, RECEIVE DEMODULATOR INPUT (RDI)

Symbol	Parameter	Min.	Typ. *	Max.	Unit
Clink **	Serial Capacitor from RFO	+ 1	1		µF
NI	Maximum Detection Level to Valid $\overline{DCD}$ Output	–	–	5.5	mVrms
N2	minimum Detection Level to Valid $\overline{DCD}$ Output	3.1	–	–	mVrms
N1/N2	Hysteresis Effect	2	–	5	dB

* Typical values are for TA = 25 °C and nominal power supply values.
* * This capacitor must be unpolarized type capacitor

DYNAMIC CHARACTERISTICS

RECEIVE FILTER TRANSFER CHARACTERISTICS IN DPSK

Low Channel

Symbol	Parameter		Min.	Typ. *	Max.	Unit
GA	Absolute Passband Gain at	1200 Hz	–	+ 9.5	–	dB
GR	Relative Gain to GA at	600 Hz	–	– 45	–	dB
		900 Hz	–	– 0.5	–	dB
		1500 Hz	–	+ 0.8	–	dB
		1800 Hz	–	– 50	–	dB
		2400 Hz	–	– 65	–	dB

High Channel

Symbol	Parameter		Min.	Typ. *	Max.	Unit
GA	Absolute Passband Gain at	2400 Hz	–	+ 9.5	–	dB
GR	Relative Gain to GA at	2100 Hz		– 0.2		dB
		2700 Hz	–	+ 0.7	–	dB
		1800 Hz	–	– 25	–	dB
		1200 Hz	–	– 68	–	dB

RECEIVE FILTER TRANSFER CHARACTERISTICS IN FSK

In FSK the receive filter is the same as in DPSK but the sampling frequency is multiplied by a 14/15 ratio (i.e. 2400 Hz in DPSK becomes 2240 Hz in FSK).

Low Channel

Symbol	Parameter		Min.	Typ. *	Max.	Unit
GA	Absolute Passband Gain at	1120 Hz	–	9.5	–	dB

High Channel

Symbol	Parameter		Min.	Typ. *	Max.	Unit
GA	Absolute Passband Gain at	2240 Hz	–	9.5	–	dB

* Typical values are for TA = 25°C and nominal power supply values.

SUMMARY OF THE DIFFERENCES BETWEEN BELL 212A AND V.22 A-B

Table 10.

Feature	BELL 212A	V.22
Low Speed Mode	0-300 bps FSK	600 bps DPSK
Guard Tone	No	1800 Hz Optional *
Answer Tone	2225 Hz	2100 Hz
Character Length is Asynchronous Mode in DPSK	9, 10 bits	8, 9, 10, 11 bits **
Over Speed Mode in Asynchronous Mode in DPSK	No	Yes **
64 Spaces Detection	No	Yes

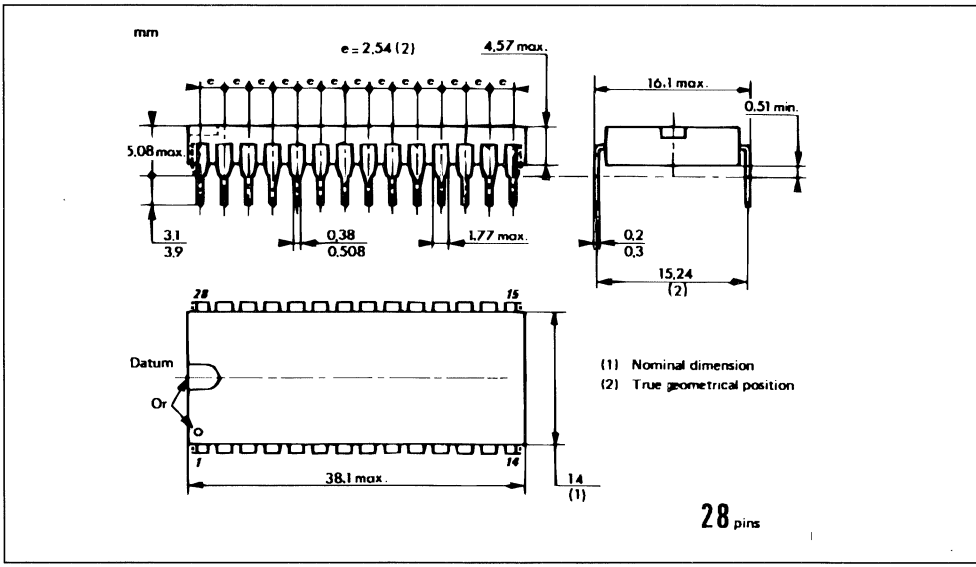
* 550 Hz may be externally generated and added to the transmit signal through EXI.
** Features of V.22 are available in BELL 212A on the chip.
All these differences are taken into consideration inside the TS7515.

ORDERING INFORMATION

Part Number	Temperature Range	Package
TS7515CP	0 to + 70 °C	PLASTIC 28 DIL
TS7515IP	– 25 to + 85 °C	PLASTIC 28 DIL

PACKAGE MECHANICAL DATA

28 PINS – PLASTIC DIP



SGS-THOMSON MICROELECTRONICS

TS7524

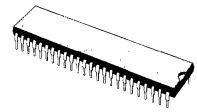
V.22 BIS, V.22, BELL 212, V.21 V.23, BELL 103 MODEM CHIP SET

ADVANCE DATA

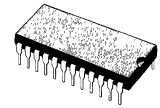
- CCITT V.22 BIS COMPATIBLE MODEM CHIP SET
- CCITT V.21, V.22 AND V.23 COMPATIBLE MODEM CHIP SET
- BELL 103 AND 212 COMPATIBLE MODEM CHIP SET
- DIGITAL SIGNAL PROCESSING (TS75240) AND ANALOG FRONT-END (TS68950/51/52) IMPLEMENTATION
- QAM, DPSK AND FSK MODULATION AND DEMODULATION
- DATA TRANSMISSION SPEED :
  - 2400 bps in QAM
  - 1200 or 600 bps in DPSK
  - 1200 or 300 or 75 bps in FSK
- ADAPTIVE EQUALIZATION
- TRANSMIT AND RECEIVE FILTERING
- SHARP ADJACENT CHANNEL REJECTION
- PROGRAMMABLE TRANSMIT OUTPUT LEVELS
- ON-CHIP 4/2-WIRE HYBRID CAPABILITY
- ANSWER TONE DETECTION AND GENERATION FOR CCITT (2100 Hz), BELL (2225 Hz), AND TRANSPAC (1650 Hz) RECOMMENDATIONS
- 550 Hz AND 1800 Hz GUARD TONE GENERATION
- DTMF TONE GENERATION
- CALL PROGRESS TONE DETECTION
- SELECTABLE SCRAMBLER AND DESCRAMBLER
- DYNAMIC RECEIVE RANGE 0 TO – 48 dBm
- TYPICAL 10^{-4} B.E.R. ACHIEVED WITH A 13 dB S/N RATIO (V.22 BIS)
- ± 10 Hz FREQUENCY OFFSET CAPABILITY
- SUPPLY VOLTAGE : ± 5 V

DESCRIPTION

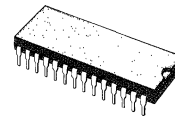
The SGS-THOMSON Microelectronics multi-standard V.22 bis chip set is a high performance modem engine, which can operate up to 2400 bps in full duplex over public switched telephone network or leased lines. The TS7524 also allows implementation of modems complying with CCITT V.21, V.22, V.23, and BELL 103, 212 recommendations. The modem hardware consists of a DSP chip and a 3-chip analog front end (MAFE). The modem signal processing functions are implemented on a TS68930 programmable digital signal processor, namely TS75240. The three analog front end chips (TS68950/51/52) are respectively the transmit interface, the receive interface and the clock generator.



P
DIP48
(Plastic Package)
TS75240



P
DIP24
(Plastic Package)
TS68950



P
DIP28
(Plastic Package)
TS68951/2

TS68950/51/52 available in PLCC Packages

(Ordering Information at the end of the datasheet)

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1. PIN DESCRIPTION

1.1. SYSTEM INTERFACE

TS75240 (DSP)

Name	N°	Type	Description
AD0.AD7	27.34	I/O	System Data Bus : these lines are used for transfer between the TS7524 mailbox and the control processor.
$\overline{CS}$	21	I	Chip Select : this input is asserted when the TS7524 is to be accessed by the control processor.
$\overline{RS}$	22	I	Register Select : this signal is used to control the data transfers between the control processor and the TS7524 mailbox.
$\overline{SDS}$	20	I	System Data Strobe : synchronizes the transfer between the TS7524 mailbox and the control processor.
SR/$\overline{W}$	19	I	System Read/Write : Control Signal for the TS7524 Mailbox Operation
$\overline{IRQ}$	24	O	Interrupt Request : signal sent to the control processsor to access the TS7524 mailbox.
$\overline{RESET}$	23	I	Reset of the TS7524. Must be maintened for a minimum of five clocks cycles.

1.2. ANALOG INTERFACE

TS68950 (analog front end transmitter)

Name	N°	Type	Description
ATO	15	O	Analog Transmit Output

TS68951 (analog front end receiver)

Name	N°	Type	Description
RAI	16	I	Receive Analog Input
LEI	17	I	Local Echo Input. This signal is subtracted from signal RAI.

1.3. CLOCK INTERFACE

TS68952 (clock generator)

Name	N°	Type	Description
TxCLK	23	O	Transmit Bit Clock
TxRCLK	16	O	Transmit Baud Clock
TxCCLK	24	O	Transmit Conversion Clock
TxMCLK	18	O	Additional Transmit Clock
RxCLK	22	O	Receive Bit Clock
RxRCLK	20	O	Receive Baud Clock
RxCCLK	21	O	Receive Conversion Clock
RxMCLK	19	O	Additional Receive Clock
TxSCLK	11	I	Transmit Synchro Clock : can be used to synchronize the transmitter on an external bit clock provided by the RS232C (or V 24) junction.

2. FUNCTIONAL DESCRIPTION

2.1. SYSTEM ARCHITECTURE

The SGS-THOMSON V.22 bis chip set is a highly integrated modem engine which provides the functionality and performance requirements for full-duplex 2400 bps modem solutions at a low cost with excellent performance due to digital signal processing technology. On top of the V.22 bis, the TS7524 chip set also implements the CCITT V.21, V.22, V.23 and BELL 103, 212 requirements.

The TS75240 is a programmable digital signal processor which implements the complete signal processing functions required to send and receive data according to the standard requirement and utilities such as call progress tone detection, auto-answer tone detection and tone generation.

The TS68950/51/52 MAFE (modem analog front end) is designed to meet the requirements of the whole range of voiceband modems.

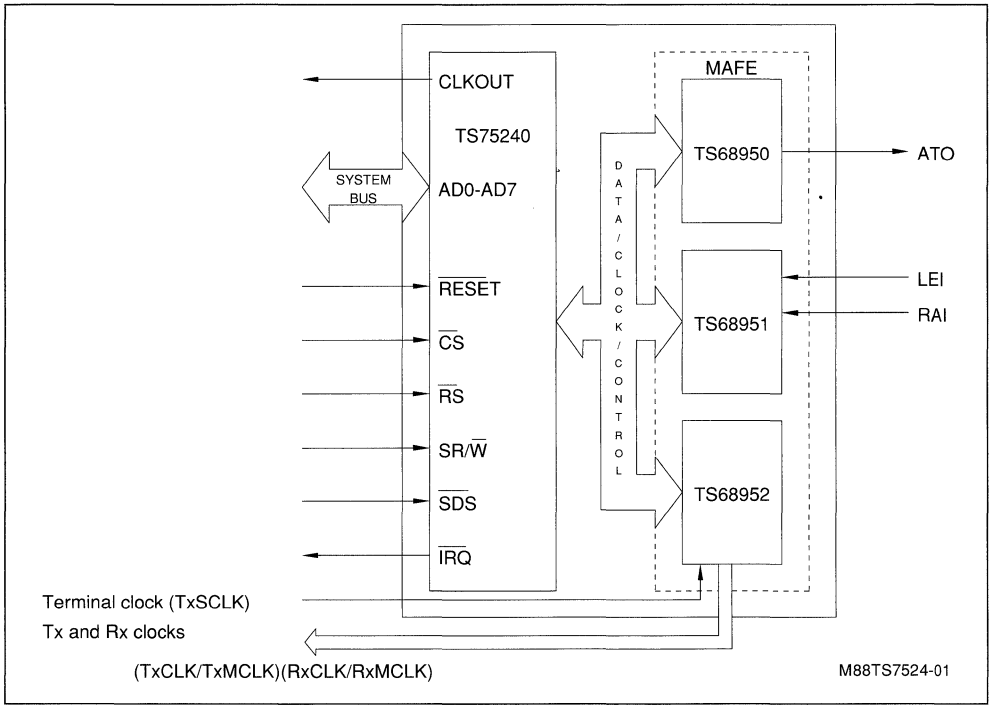
The MAFE incorporates all the required programmable gain control and clock circuitry, and signal filtering (band-limiting, anti-aliasing and smoothing filters).

Interfacing the TS7524 chip set to a control processor is very straightforward and requires no external interface circuitry.

The TS7524 chip set along with a data access arrangement (DAA), a control processor and a V.24/RS232 interface and/or an UART, is particularly well-suited for high-performance modem.

The modem supervision is insured by a control processor which implements the handshake monitoring, the auto/manual answer and dialing modes, the test modes and fall back capability and the async/sync and sync/async conversion.

Figure 1 : TS7524 Block Diagram.

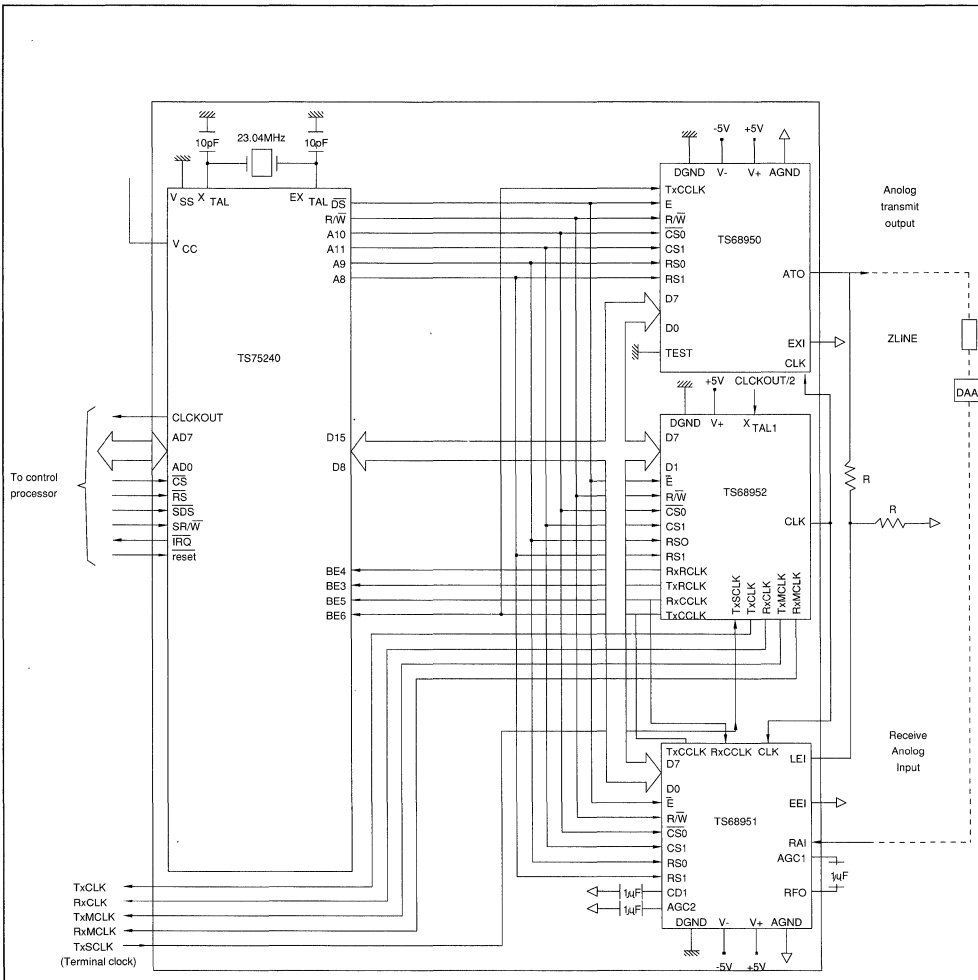


2.2. PROCESSOR AND MAFE CHIPS ARRANGEMENT

The TS75240 is connected to the analog front end chips through its local bus where D8 through D15 are the 8-bit data bus and A8 through A11 are four address lines used to address directly the three analog front end chips.

Data-Strobe ($\overline{DS}$) is used to synchronize the transfer of data. Read/Write (R/$\overline{W}$) indicates the direction of data. Four Branch-on-External-Condition signals (BE3 to BE6) are connected to the different clock signals issued from the clock generator interface (TS68952). They are used by the TS75240 to perform its real-time task scheduling.

Figure 2 : Interconnections between the Analog Front End Chips and the Digital Signal Processor TS75240.



Notes : D0 non connected on the TS68952
D8 (TS75240) connected to D0 (MAFE)
D15 (TS75240) connected to D7 (MAFE).

M88TS7524-02

2.3. OPERATION

2.3.1. ANALOG FRONT END DESCRIPTION. The MAFE (TS68950/1/2) is a modem analog front end designed in three chips which performs the following functions controlled by the TS75240 digital signal processor according to the selected modem standard.

Transmit Analog Interface (TS68950) :

- 12-bit D/A converter synchronized with the sampling transmit clock.
- Low-pass and smoothing continuous-time filters
- 0 to 22 dB (or infinite) programmable attenuation.

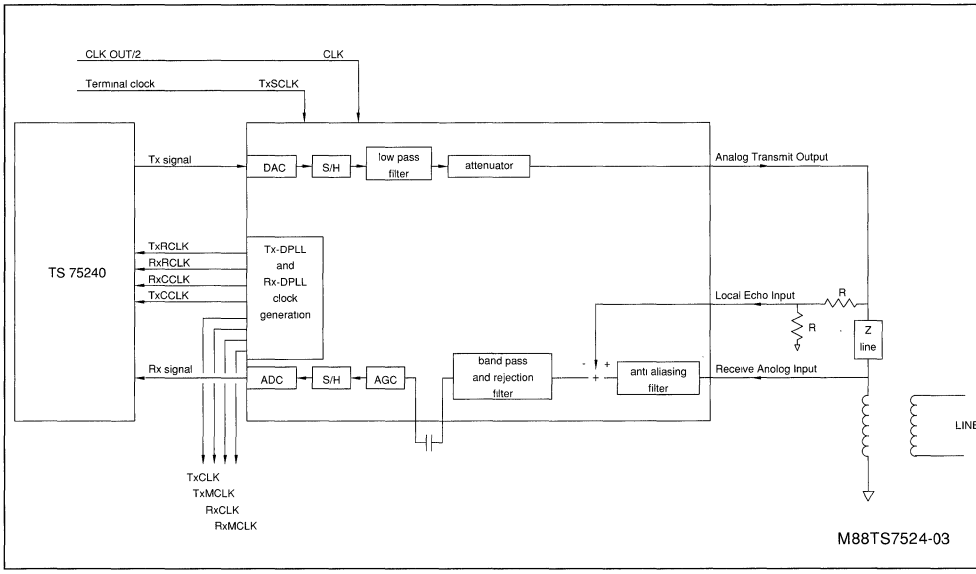
Receive analog Interface (TS68951) :

- 12-bit A/D converter synchronized with the sampling receive clock.
- Band-pass programmable filter.
- Back channel rejection filter.
- Smoothing filter.
- 0 to 46.5 dB gain amplifier.

Clock Generation Interface (TS68952) :

- Transmit time base with programmable synchronization on data terminal equipment clock or extracted receive clock.
- Programmable receive time base DPLL.
- Four programmable plesiochronous transmit and receive clocks (rate, sampling, bit and additional clocks).

Figure 3 : MAFE Block Diagram.



2.3.2. OPERATING MODES. The modem implementation is fully compatible with different CCITT and BELL recommendations as listed in table 1. It may operate at different bit rates, from 75 bps to 2400 bps.
In case of switching from any mode to another, a reset must be applied to the TS75240 reset pin, except during the V.22 bis handshaking (the V.22 bis and V.22/BELL 212 software modules implemented in the TS75240 are compatible).

A DTMF tone generator is provided to output one of 16 standard dual tones coded by a combination of two frequencies. For specific applications where single tone is required, the DTMF generator provides the possibility to select either the high frequency or the low frequency of the standard dual tones.

A tone detector and a carrier detector respectively recognize the different answer tones (CCITT 2100 Hz, BELL 2225 Hz and Transpac 1650 Hz) and call progress tones (300 Hz to 700 Hz), as well as the presence or the absence of the on-line carrier signal (both for PSTN and leased lines).

Table 1 : TS7524 Operating Modes.

Recommendation	Bauds	BPS	Duplex	Answer	Orig	Modulation
V. 22 BIS	600	2400	Full	Yes	Yes	QAM (quadribit)
V. 22	600	1200	Full	Yes	Yes	DPSK (dibit)
BELL 212	600	1200	Full	Yes	Yes	DPSK (dibit)
V. 22	600	600	Full	Yes	Yes	DPSK (bit)
V. 21	300	300	Full	Yes	Yes	FSK
BELL 103	300	300	Full	Yes	Yes	FSK
V. 23	1200/75	75/1200	Full	Yes	Yes	FSK

2.3.3. TRANSMIT (fig. 4) :

- *V.22 bis, V.22 and BELL 212.* QAM or DPSK modulation is used to send four (V.22 bis) or two (V.22 and BELL 212) or one (V.22) bit (s) of information at 600 bauds modulation rate.

The scrambler can be bypassed, as user's option usually during the handshake procedure. After coding, a raised cosine filter (roll-off factor 0.75) performs pulse shaping and provides a 45 dB rejection between the channels so as to comply with V.22 bis, V.22 and BELL 212 standard requirements. When required, a 1800 Hz or 550 Hz guard tone can be added to the transmitted signal.

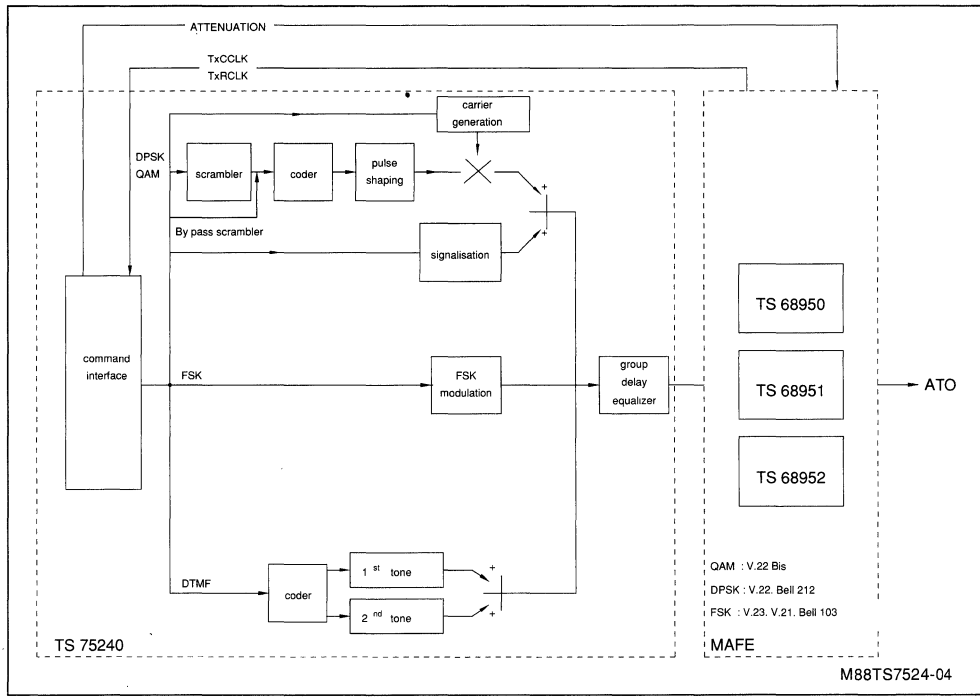
- *V.23, V.21 and BELL 103*

The FSK modulation is used to send one bit of information at 1200 or 75 baud (V.23) or 300 bauds (V.21 and Bell 103).

- *DTMF*

The DTMF generator outputs one of 16 standard dual tones synthetized by the TS75240 and selected by a 4-bit binary value as described later. Each tone is coded by a combination of two frequencies. The DTMF generator may be programmed to generate one tone at a time.
The transmit attenuation level is programmable over a 23 dB dynamic range by 1 dB steps.

Figure 4 : TS7524 Transmit Block Diagram.



2.3.4. RECEIVE (fig. 5) :

- V.22 bis, V.22 and BELL 212.

QAM or DPSK demodulation is used to receive four (V.22 bis) or two (V.22 and BELL 212) or one (V.22) bit (s) of information at 600 bauds.

- V.23, V.21 and BELL 103

The FSK demodulation is used to receive one bit of information at 1200 or 75 bauds (V.23) or 300 bauds (V.21 and BELL 103).

- Tone Detection

The TS7524 recognizes the following tones :

- 2100 Hz and 2225 Hz answer tone detection
- 1650 Hz V.21 Transpac answer tone detection
- 300 to 700 Hz call progress tone detection

Adaptive equalization, DPLL and AGC compensate for line impairments, frequency offset, group delay and amplitude distorsions.

Efficient rythm recovery algorithms provides accurate sampling on the receive signal with a variation up to $\pm 2.10^{-4}$.

Decoded data are provided in scrambled or descrambled format.

2.4. TS7524 INTERFACE (fig. 6)

2.4.1. TS7524 ANALOG INTERFACE. The transmit signal at the line interface (output ATO) is programmable over a 23 dB dynamic range by 1 dB steps through the TS75240 mailbox.

The receive signal at the line interface (input RAI) can have a dynamic range from 0 to – 48 dBm.

With a simple circuit using a minimum of external components, the TS7524 can transmit with a level of – 12 dBm on line and provide the adequate rejection of the transmit signal on the receive channel.

2.4.2. TS7524 DIGITAL INTERFACE. The interface between the TS7524 chip set and the control processor is managed by the TS75240 via its system bus and internal mailbox. The mailbox allows the control processor to read/write three consecutive data-bytes through AD0-AD7 bus. The mailbox exchanges follows the protocol described in fig. 2.4.3.

The TS75240 digital interface signals, and their definition are listed in table 2.

Figure 5 : TS7524 : Receive Block Diagram.

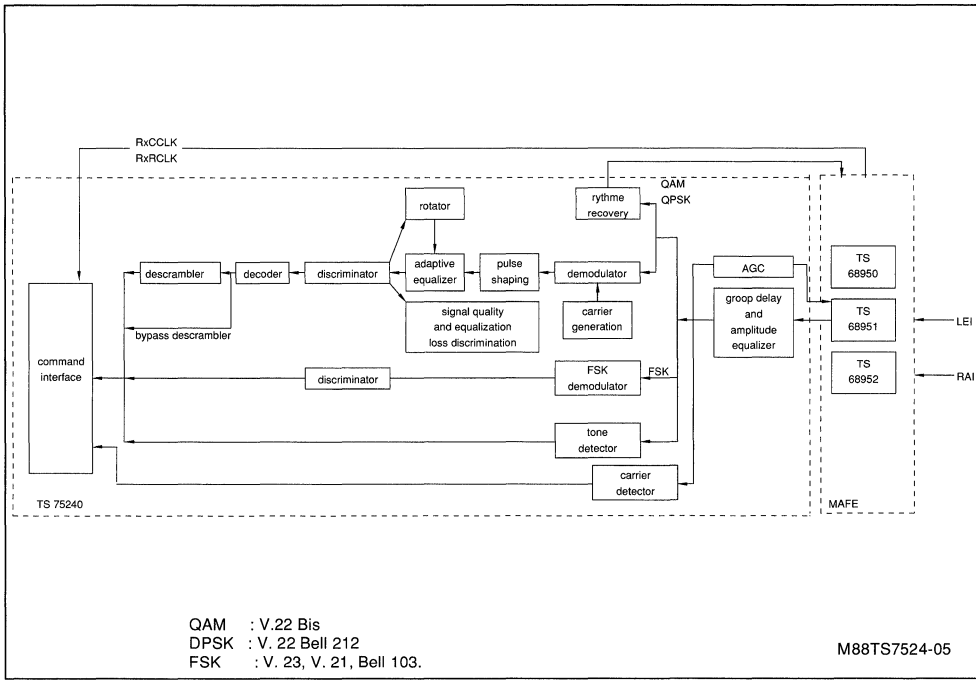
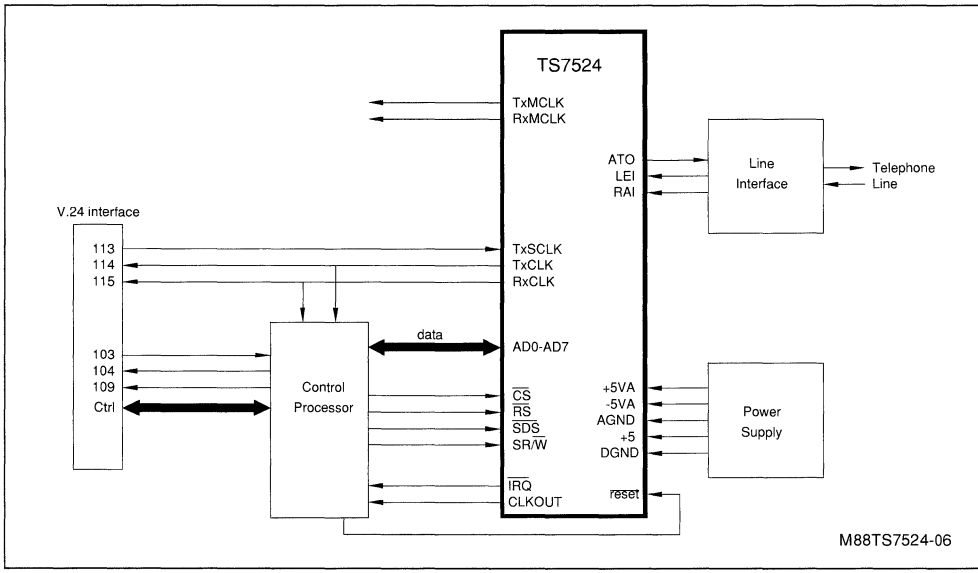


Table 2 : Digital Interface Signals.

Interface Signals	Input/output I/O	Signal Definition
AD0	I/O	Data-Bus (LSB)
AD1	I/O	Data-Bus
AD2	I/O	Data-Bus
AD3	I/O	Data-Bus
AD4	I/O	Data-Bus
AD5	I/O	Data-Bus
AD6	I/O	Data-Bus
AD7	I/O	Data-Bus (MSB)
SR/$\overline{W}$	I	Read/write Signal
$\overline{SDS}$	I	Data Strobe
$\overline{IRQ}$	O	Mailbox Handshake
$\overline{CS}$	I	TS75240 Chip Select
$\overline{RS}$	I	Register Select
$\overline{Reset}$	I	TS75240 Reset
TxMCLK *	O	Additional Transmit (2400 Hz) Clock
RxMCLK *	O	Additional Receive (2400 Hz) Clock
TxCLK	O	Transmit Bit Rate Clock
RxCLK	O	Receive Bit Rate Clock
TxSCLK	I	Transmit Terminal Clock

* These additional clocks may be used for specific applications.

Figure 6 : Functional Interconnect Diagram.



2.4.3. MAILBOX DESCRIPTION. The TS75240 requires the attention of the control processor at regular intervals in order to perform properly. The control processor must interact with the modem chip set in a timely manner to avoid improper operation.

To initialize communication exchanges between the TS7524 and the control processor, the TS7524 RESET pin must be maintained in its active (low) state during at least 870 ns (5 clock cycles) by the microprocessor. At the end of reset, the 75240 gives the mailbox control to the processor.

It is also recommended to maintain the RESET in its active state until the exchanges can start.

Following a reset the status word read from the mailbox is not significant, and the content of the command word is ignored. So, the first mailbox exchange is a dummy exchange.

The mailbox located internally to the TS75240 DSP contains 3-bytes input and 3-bytes output shift registers. The TS75240 has an internal flag which indicates whether the TS75240 or the control processor has access to the mailbox. The TS75240 can relinquish its accessability to the mailbox by setting this internal flag, but it can no longer regain access to the mailbox as the flag is reset only after the control processor relinquishes its accessability to the mailbox.

The access protocol and system bus transfers are controlled by an internal I/O sequencer within the TS75240 which operates as follows :

1/ The mailbox is made available to the control processor by the TS75240 which drives the IRQ mailbox handshake signal to the active (low) state.

2/ The control processor detects IRQ active and dummy reads the mailbox by forcing the TS75240 chip select (CS) and register select (RS) low along with the write signal (SR/W) high. The activated data strobe signal (SDS = 0) validates the above signals.

3/ The TS75240 detects the dummy read of its mailbox via the control signals mentioned in step 2 and negates IRQ mailbox handshake signal after 1 µS (at least 5 clock cycles).

4/ The control processor detects the negation of IRQ indicating that the TS75240 mailbox is available for data transfers. The control processor reads three bytes (one status word) and then writes three bytes (one command word) in the mailbox. If the status word is a transmit status word, then a transmit command word must be written into the mailbox. Else, a receive command word must be written into the mailbox.

5/ The control processor ends the exchange protocol performing a dummy read of the mailbox as in step 2 but with RS in the high state.

The TS75240 then owns the mailbox and can make it available again to the control processor as in step 1.

3. USER INTERFACE

3.1. COMMAND AND STATUS WORDS

The TS7524 chip set functionalities and status reporting are managed by the control processor through the TS75240 mailbox, according to the protocol outlined earlier.

The command words are issued by the control processor and received by the TS75240.

The command words provide the necessary functional control of the TS7524 chip set.

The status words are issued by the TS75240 and delivered to the control processor.

The status words provide the status reporting.

Each command and status word of both the transmit and receive part comprises three bytes as described in the following sections.

The control processor must be able to handle :

- one mailbox transfer per transmit baud period and,
- one mailbox transfer per receive baud period.
- these transfers are plesiochronous. (Tx and Rx clocks have the same nominal frequency but can shift of $\pm 1.10^{-4}$, so the phase relation between Tx and Rx is time varying).

3.2. TRANSMIT AND RECEIVE COMMAND WORDS

Both the transmit and receive command words are built on the same programming model, but have to be programmed completely independently.

3.2.1. TRANSMIT COMMAND WORD. The table 3 shows the transmit command word (three bytes) programmation and transmit functionalities.

The first byte of the transmit command word permits the choice of the DTMF mode or the selection of the requested CCITT (with or without guard tone) or BELL standards.

The second byte contains the transmit parameters information register.

The third byte is the transmit data register of DTMF tone selection register. In this byte is also included the transmit enable bit which instructs the TS7524 to transmit (or not) data to the line.

To manage the TS7524 in an efficient way, it is recommended to work with a table stored in the control processor memory space. This table will reflect the three bytes of the transmit command word and will be sent from the control processor to the TS7524 at

Table 3 : Transmit Command Word Format.

<table>
<tr><th>BIT</th><th>First Byte</th><th>Second Byte</th><th colspan="6">Third Byte</th></tr>
<tr><td>0</td><td rowspan="4">Transmit Mode Selection

0000 : Modem Disabled
0001 : V.22 Bis
0010 : V.22 0011 : B212
0100 : V.23 0101 : V.21
0110 : Bell 103
0111 : D.T.M.F.</td><td rowspan="4">Transmit
Attenuation</td><td colspan="6">Transmit (0)</td></tr>
<tr><td>1</td><td>D0</td><td rowspan="4">DPSK</td><td rowspan="4">QAM</td><td rowspan="5">FSK</td><td rowspan="4">DTMF</td></tr>
<tr><td>2</td><td>D1</td></tr>
<tr><td>3</td><td>D2</td><td>0</td></tr>
<tr><td>4</td><td rowspan="2">Transmit Signalling
00 : Signalling Disabled
01 : 550 Hz
11 : 1800 Hz</td><td>D3</td><td>0</td></tr>
<tr><td>5</td><td>Scrambler (ON/$\overline{\text{OFF}}$)</td><td>D4</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>6</td><td>Reserved</td><td>Reserved</td><td>D5</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>7</td><td>$\overline{\text{ANSW}}$/ORIG or DTMF</td><td>V.22 Binary Rate Select
or DTMF</td><td colspan="6">$\overline{\text{Transmit Enable}}$</td></tr>
</table>

Note : All the "RESERVED" bits must be cleared to "0" by the user.

each transmit baud. In this table, the different fields could be programmed according to the CCITT or BELL standard needed taking into account the transmit parameters. Once the contents of the first and second byte have been determined for the whole transmission, only the transmit data field in the third byte has to be updated in the table. So, at each transmit baud, the TS75240 will receive the complete three bytes, will check them and send the data.

FIRST BYTE :

Bit 3, 2, 1 and 0 : Transmit mode selection

These bits select the standard to use or the DTMF mode

0000	: Modem disabled
0001 to 0110	: Transmit mode selection
0111	: DTMF.In this mode, the number which may be dialed is given by the proper binary combination of bits 4, 3, 2 and 1 in the third byte. Refer to paragraph "DTMFmode" for detailed information.

Other bit codes are reserved.

Bit 5 and 4 : Transmit Signalling

These bits represent the tone to send regarding the requested functionalities.

00	: Signalling disabled
01 or 11	: Guard tone 550 Hz or 1800 Hz which can be added to the modulated signal.
10	: Reserved

Bit 6 : Reserved

Bit 7 : $\overline{\text{ANSWER}}$ / ORIGINATE or DTMF

This bit has two main functions. Its first function is to select the answer or originate mode. The second function is used in DTMF mode as explained in details in paragraph "DTMF mode".

In $\overline{\text{ANSWER}}$/ORIGINATE mode, the bit 7 cleared to zero selects the answer mode (transmit in high channel). The bit 7 set to one selects the originate mode (transmit in low channel).

SECOND BYTE :

Bit 4, 3, 2, 1, and 0 : Transmit attenuation

The transmit levels without attenuation at the transmit interface output (ATO) on 600 ohms are as follows :

- in FSK modes (V.23, V.21 and BELL 103)
  - 0 dBm
- in QAM (V.22 bis) and DPSK (V.22 and BELL 212) modes
  - 5 dBm when transmission on low channel
  - 4 dBm when transmission on high channel with guard tone composed by :
    - 5 dBm (signal)
    - 12 dBm (guard tone)
  - 5 dBm when transmission on high channel without guard tone
- 4 dBm in DTMF mode composed by
  - 5 dBm (high frequency)
  - 7 dBm (low frequency)

These are maximum levels which can be decreased by programming the transmit attenuation, with attenuation levels falling within 0 dB (00000) and 23 dB (10111) range, selectable in 1 dB steps.

Selection within 11000 to 11111 correspond to an infinite attenuation.

At power-on, or after a reset applied on the reset pin of the TS75240, an infinite attenuation is automatically programmed.

Bit 5 : Scrambler

The TS7524 incorporates an auto-synchronized scrambler/descrambler in accordance with CCITT V.22 bis and V.22 and BELL 212 recommendation.

The scrambler is enabled (1) or disabled (0) by programming the bit 5.

When the scrambler is enabled, the input data is scrambled by dividing the data by a generating polynomial as defined in the V.22 bis and V.22 recommendations.

When the scrambler is disabled, the input data is routed around the scrambler in the transmit path.

Bit 6 : Reserved

Bit 7 : V.22 binary rate selection or DTMF

This bit has two main functions. Its first function allows the possibility to select the lowest binary rate (V.22 at 600 bps) when set to one, or the highest binary rate (V.22 at 1200 bps) when cleared to zero.

The second function is used in DTMF mode as explained in details in paragraph "DTMF mode".

THIRD BYTE :

Bit 0 : Transmit

This bit indicates the nature of the command word. It must be cleared to zero by the control processor to indicate to the TS7524 that the command word is a transmit command word, and that the 3-bytes written in the mailbox contain transmit information.

Bit 6 Thru 1 : Transmitted data or DTMF tone selection. These bits have two main functions. The first function is to represent the data which will be sent according to the appropriate mode. The second function, used in DTMF mode, is to select by programming the bits 4, 3, 2, and 1 the generated tone which will be used to dial the proper number as shown in paragraph "DTMF mode" in table 5.

In QAM (V.22 bis) or DPSK (V.22 or BELL 212) modes, the bits 4, 3, 2, and 1 represent the data sent by the TS7524. According to the selected mode, up to 4 bits will be used :

- In V.22 bis, each symbol (baud) is coded by 4 bits (quadribit)
- In V.22 at 1200 bps and BELL 212 modes, each symbol is coded by 2 bits (dibit)
- In V.22 at 600 bps, each symbol is coded by only one bit.

In these modes, the mailbox exchanges are executed at the rate of 600 exchanges per second.

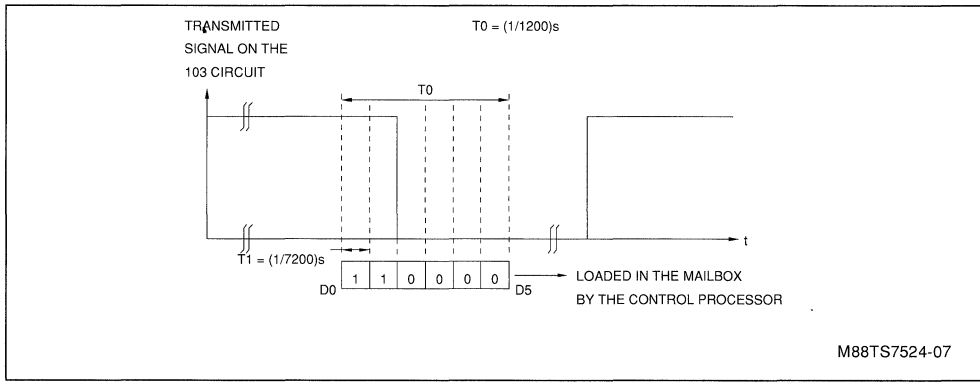
In FSK modes (V.21, V.23, and BELL 103) all the 6 bits (bit 6 thru 1) are used to represent the binary value of six samples of the transmitted signal. In these modes, the mailbox exchanges are executed at the rate of 1200 exchanges per second. Consequently, to perform a serial to parallel conversion the control processor has to sample the 103 circuit of the V.24/RS232 junction at 7.2 kHz which is the sampling clock frequency (TxCCLK).

The bit 1 (which correspond to D0) is the first sample of the signal transmitted over the line as shown in figure 7.

Bit 7 : transmit enable

This bit low instructs the TS7524 to send data.

Figure 7 : FSK Mode.



DTMF MODE

The DTMF generator outputs one of 16 standard dual-tones. For specific applications where single tone is required, the DTMF generator provides the possibility to select either the high frequency or the low frequency of the standard dual tones.

All the bytes used to program the DTMF mode and mentioned in this section are those of the transmit command word.

The DTMF mode is selected by programming bits 3 to 0 in the first byte.

Choosing the dual-tone mode, which is the normal operating mode, is done with bit 7 in the second byte cleared to zero. The DTMF generator then outputs one of the sixteen standard dual tones selected through bits 4 to 1 in the third byte as shown in table 5.

The single-tone mode is selected by setting to 1 the bit 7 in the second byte. This mode is used in specific cases where one frequency is to be generated. After one frequency pair is selected through bits 4 to 1 in the third byte as shown in table 5, the choice of the higher or lower frequency is made through bit 7 of the first byte. When bit 7 is set to 1 (respectively 0), the lower (respectively higher) frequency is generated.

In DTMF mode, the mailbox exchanges are executed at the rate of 1200 exchanges per second.

The programming of DTMF mode is summarized in table 4.

Table 4 : DTMF (dual or single tone) Programmation.

DTMF	First Byte Bits 3, 2, 1, 0		2nd Byte Bit 7	Third Byte Bits 4, 3, 2, 1
Dual-tone	0111		0	4-bit Binary Value Coding one of 16 Dual Tone
Single-tone	First Byte Bit 7	Bits 3, 2, 1, 0	2nd Byte Bit 7	Third Byte Bits 4, 3, 2, 1
High Frequency Selected	0	0111	1	4-bit Binary Value Coding one of 16 Dual Tone (high)
Low Frequency Selected	1	0111	1	4-bit Binary Value Coding one of 16 Dual Tone (low)

In DTMF mode the transmit levels at the analog transmit interface output (ATO) are respectively – 5 dBm for the high group frequencies, and – 7 dBm for the low group frequencies. These are maximum levels and can be decreased by programming the transmit attenuation in the second byte.

Table 5 : Tone Encoding.

Number to Dial	DTMF Code in Third Byte Generated Tones (Hz)						
	Bit4	Bit3	Bit2	Bit1	Low		High
0	0	0	0	0	941	&	1336
1	0	0	0	1	697	&	1209
2	0	0	1	0	697	&	1336
3	0	0	1	1	697	&	1477
4	0	1	0	0	770	&	1209
5	0	1	0	1	770	&	1336
6	0	1	1	0	770	&	1477
7	0	1	1	1	852	&	1209
8	1	0	0	0	852	&	1336
9	1	0	0	1	852	&	1477
A	1	0	1	0	697	&	1633
B	1	0	1	1	770	&	1633
C	1	1	0	0	852	&	1633
D	1	1	0	1	941	&	1633
*	1	1	1	0	941	&	1209
#	1	1	1	1	941	&	1477

The accuracy of the frequencies is $\pm 10^{-4}$.
The harmonic rejection level is at – 65 dB.

ANSWER TONE GENERATION

The TS7524 chip set may generate four different standard frequencies which represent the usual auto answer tones.

- 1300 Hz : V.23 Automatic connection tone
- 1650 Hz : V.21 Transpac specific answer tone
- 2100 Hz : CCITT V.22 bis, V.22, V.23 and V.21 answer tone
- 2225 Hz : BELL 212 and BELL 103 answer tone

For answer tone generation, mailbox exchanges are executed at the rate of 1200 exchanges/second.

Table 6 : Answer Tone Generation.

Tone	FSK Mode to Use	First Byte Bit 7	First Byte Bits 3, 2, 1, 0	Third Byte Bits 6, 5, 4, 3, 2, 1
1300 Hz	V. 23 Answer	0	0100	111 111
1650 Hz	V. 21 Answer	0	0101	111 111
2100 Hz	V. 23 Answer	0	0100	000 000
2225 Hz	B103 Answer	0	0110	111 111

3.2.2. RECEIVE COMMAND WORD. In the receive command word, the first byte permits the choice of the call progress and answer tone detection modes or the selection of the requested CCITT or BELL standards.

The second byte defines additional receive parameters.

The third byte informs the TS7524 that the command word is a receive command word.

To manage the TS7524 in an efficient way, it is recommended to work with a table stored in the control processor memory space. This table will reflect the three bytes of the receive command word and will be sent from the memory by the control processor to the TS7524 at each receive baud. In this table, the different fields could be programmed according to the CCITT or BELL standard needed taking into account the receive parameters. At each receive baud, the TS75240 will receive and processes the complete three bytes.

Table 7 : Receive Command Word Format.

BIT	First Byte	Second Byte	Third Byte
0	Receive Mode Selection	**Reserved**	Receive (1)
1	0000 : Modem Disabled 0001 : V.22 Bis 0010 : V.22 0011 : B212 0100 : V.23 0101 : V.21 0110 : Bell 103 0111 : Call Prog. / Answer Tone		**Reserved**
2			
3			
4	Answer Tone Selection		
5	Tx Synchronization	Descrambler (ON/$\overline{\text{OFF}}$)	
6	Carrier Detect Level	**Reserved**	
7	$\overline{\text{Answer}}$/originate	V.22 Binary Rate Select	

Note : All the "RESERVED" bits must be cleared to "0" by the user.

FIRST BYTE :

Bit 3, 2, 1, and 0 : Receive mode selection

These bits select the standard to use or the call progress and answer tone detection mode.

0000 : Modem disabled
0001 to 0110 : Receive mode selection
0111 : Call progress and answer tone detection mode. In this mode the TS7524 recognizes different tones as explained in paragraph "call progress and answer tone detection"

Other bit codes are reserved.

Bit 4 : Answer tone selection

This bit defines the answer tone to be detected. It selects either 1650 Hz (Transpac) or 2100/2225 Hz answer tone. When high, the detect answer tone is 1650 Hz. When low, the detect answer tone is 2100/2225 Hz.

Bit 5 : Tx synchronization signal programming

This bit allows synchronization of all transmit clocks on a selected source. When bit 5 is set to 1, all the TS7524 transmit clocks (TxCLK, TxCCLK, TxRCLK, TxMCLK) are synchronized on TxSCLK input (typically a terminal clock signal coming from

the V.24/RS232 interface). This avoids overspeed and maintains a complete synchronization during the transmission. If there is no signal on TxSCLK coming from the terminal clock, the transmit clocks are free-running at their nominal frequencies.

When the bit 5 is set to 0, the TS7524 transmit clocks are synchronized on the receive clocks. This possibility may be used for remote digital loopback.

Bit 6 : Carrier detection level

The TS7524 can be used both on the public switched telephone network (PSTN) and with leased lines.

When the bit 6 is set to 0, the carrier detection threshold are :

– 43 and – 48 dBm (PSTN).

When the bit 6 is set to 1, the carrier detection threshold are :

– 33 and – 38 dBm (leased lines).

Bit 7 : $\overline{\text{Answer}}$ / originate

The bit 7 cleared to zero selects the answer mode (receive in low channel). The bit 7 set to one selects the originate mode (receive in high channel).

SECOND BYTE :

Bit 4, 3, 2, 1, and 0 : Reserved (must be cleared to 0)

Bit 5 : Descrambler

The TS7524 incorporates an auto-synchronized scrambler/descrambler in accordance with CCITT V.22 bis and V.22 and BELL 212 recommendation.

The descrambler is enabled when bit 5 is set to 1, or disabled when bit 5 is set to 0.

When the descrambler is enabled, the data stream is multiplied by the same polynomial that divided the data at the scrambler in the transmission path.

When the descrambler is disabled, the data stream is routed around the descrambler in the receive path.

Bit 6 : Reserved (must be cleared to 0)

Bit 7 : V.22 binary rate select

This bit allows the possibility to select the lowest binary rate (V.22 at 600 bps) when set to one, or the highest binary rate (V.22 at 1200 bps) when set to zero.

THIRD BYTE :

Bit 0 : Receive

This bit indicates the nature of the command word. It must be set to one to indicate to the TS7524 that the command word is a receive command word. This involves that the 3-bytes written in the mailbox by the control processor to the TS7524 contain receive command information.

Bit 7 Thru 1 : Reserved (must be cleared to 0)

3.3. TRANSMIT AND RECEIVE STATUS WORD

The status words are issued by the TS75240 and provide the status reporting to the control processor.

3.3.1. TRANSMIT STATUS WORD

Table 8 : Transmit Status Word Format.

BIT	First Byte	Second Byte	Third Byte
0	Transmit (0)	**Reserved**	**Reserved**
1	**Reserved**		
2			
3			
4			
5			
6			
7			

FIRST BYTE :

Bit 0 : Transmit

This bit when low informs the control processor that the status word issued by the TS7524 is a transmit status word.

Bit 7 Thru 1 : Reserved

SECOND BYTE :

Bit 7 Thru 0 : Reserved

THIRD BYTE :

Bit 7 Thru 0 : Reserved

3.3.2. RECEIVE STATUS WORD

Table 9 : Receive Status Word Format.

BIT	First Byte		Second Byte	Third Byte			
0	Receive (1)		Reserved	Reserved			
1	D0	Data Before Descrambling (Q.A.M. , D.P.S.K.)		D0	Data After Descr. (Q.A.M., D.P.S.K.)	D0	Data (F.S.K.)
2	D1			D1		D1	
3	D2			D2		D2	
4	D3		Equalization Status	D3		D3	
5	Reserved		Signal Quality	1		D4	
6	S1 Sequence		Carrier Detect	1		D5	
7	S1 Sequence or Call Progress Tone Detection		Reserved	Answer Tone Detection			

Note : In QAM and DPSK modes, both for the data after and before descrambling, the unused bits are set to "1" by the TS7524.

FIRST BYTE :

Bit 0 : Receive

This bit set to one by the TS7524 indicates to the control processor that the current status word is a receive status word.

Bit 4, 3, 2, and 1 : Data before descrambling

Used only in QAM and DPSK modes, these four bits represent the data received before descrambling, i.e., after the demodulator and before the descrambler. Data is coded on four bits (D3, D2, D1, D0) in V.22 bis, on two bits (D1, D0) in V.22 at 1200 bps and BELL 212, on only one bit (D0) in V.22 at 600 bps. The unused bits are set to 1 by the TS7524.

The mailbox exchange rate between the TS75240 and the control processor is done at 600 exchanges per second. Both for QAM and DPSK modes, D0 (which correspond to the bit 1) is the first bit received.

Bit 5 : Reserved

Bit 7 and 6 : S1 handshake sequence (V.22 bis) mode

During the V.22 bis handshake sequence, these two bits indicate the presence or the absence of the "S1" sequence detected by the TS7524. If the TS7524 gives an alternance (at each baud period in reception) of values "10" and "01" on bit 7 and 6, the "S1" sequence is present in reception. Else, this means its absence.

Bit 7 : Call progress tone detection (call progress/answer tone mode).

This bit low indicates detection of energy in the band 300 – 700 Hz with a detection threshold of – 43 dBm. This bit high means there is no energy detected. (see paragraph call progress and answer tone detection).

SECOND BYTE

Bit 3, 2, 1, and 0 : Reserved

Bit 4 : Equalization status

This bit will go high (1) in case of equalization loss (retrain sequence initialization or fallback mode).

Bit 5 : Signal quality

This bit will go high (1) when the quality of the received signal is too low for a good transmission.

Bit 6 : Carrier detect

This bit indicates the presence or the absence of the on-line signal as follows :

- This bit will go low (0) if the signal level is higher than – 43 dBm on PSTN or – 33 dBm on

leased lines
- This bit will go high (1) if the signal level is lower than – 48 dBm on PSTN or – 38 dBm on leased lines

The minimum hysteresis level is 2 dB.

The information on the on-line signal may be used by the control processor to manage the 109 signal of the V.24 junction.

Bit 7 : Reserved

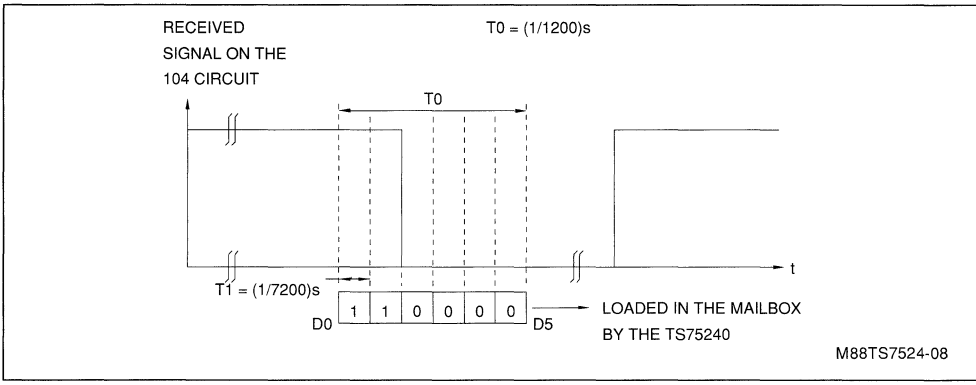
THIRD BYTE :

Bit 0 : Reserved

Bit 6 Thru 1 : Data received or data after descrambling.

These six bits contain the received data and have to be processed by the control processor according to the selected standards :
- In QAM and DPSK modes, bit 4 thru 1 represent the data received after descrambling, if the descrambler is enabled. Otherwise, they represent the data received without descrambling.
The data is encoded on four bits (D3, D2, D1, D0) in V.22Bis, on two bits (D1, D0), in V.22 at 1200 bps and Bell 212, on only one bit (D0) in V.22 at 600 bps. The unused bits are set to one by the TS7524.
The mailbox exchange rate between the TS75240 and the control processor is done at 600 exchanges per second. For both QAM and DPSK modes, D0 (which correspond to bit 1) is the first bit received.
- In FSK modes (V.21, V.23, and BELL 103) all the six bits are used to represent the digital value of six samples of the received signal. In these modes, the mailbox exchange must be executed at the rate of 1200 exchanges per second. Consequently to perform a parallel to serial conversion the control processor has to resend these bits on the 104 circuit of the V.24/RS232 junction at 7.2 kHz.
Bit 1 (which correspond to D0) is the first sample of the incoming signal received over the line as shown in figure 8.

Figure 8 : FSK Receive Mode.



Bit 7 : Answer tone detection

Used in answer tone detection mode, this bit when low (0), indicates the presence of the answer tone (CCITT 2100 Hz, BELL 2225 Hz or Transpac 1650 Hz) sent by the far-end modem. When high (1), it means no detection of answer tone. Refer to paragraph "call progress and answer tone detection" for further details.

CALL PROGRESS AND ANSWER TONE DETECTION

The TS7524 call progress detection part is activated by detection of energy in the 300 to 700 Hz call progress tone bandwidth. The call progress mode must be selected in the first byte (bit 3 thru 0) of the receive command word.

Then the bit 7 of the first byte of the receive status word indicates to the control processor that the call progress tone is detected (bit 7 = 0) or not (Bit 7 = 1).

In answer tone mode, the TS7524 may recognize three different standard frequencies which represent the usual answer tones sent by the far-end modem as described hereunder :

- 2100 Hz : CCITT modes answer tone V.21 and V.23
- 2225 Hz : BELL answer tones
- 1650 Hz : Transpac V.21 answer tone

The answer tone mode must be selected in the first byte (bit 3 thru 0) of the receive command word and the answer tone selection (1650 Hz or 2100/2225 Hz) with the bit 4.

Then bit 7 in the third byte of the receive status word indicates to the control processor that the answer tone is detected (bit 7 = 0) or not (bit 7 = 1).

The table 10 shows the programmation of the receive command word, and the status reporting contained in the receive status word.

DTMF mode and transmit enable = 1 must be selected in the transmit command word.

Table 10 : Call Progress and Answer Tone Detection Programming Model.

	Receive Command Word		Receive Status Word	
	First Byte Bit 3, 2, 1, 0,	Bit 4	First Byte Bit 7	Third Byte Bit 7
Call Progress Mode and 2100/2225 Answer Tone	0111	0	1 No Call Progress Tone Detected 0 Presence of Call Progress Tone	0 2100/2225 Hz Detected 1 No Detection
Call Progress Mode and 1650 Hz Answer Tone	0111	1	1 No Call Progress Tone Detected 0 Presence of Call Progress Tone	0 1650 HZ Detected 1 No Detection

4. ELECTRICAL SPECIFICATIONS

4.1. MAXIMUM RATINGS

TS75240

Symbol	Parameter	Value	Unit
V_{CC} *	Supply Voltage	– 0.3 to 7.0	V
V_{in} *	Input Voltage	– 0.3 to 7.0	V
T_A	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

* With respect to V_{SS}.

Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

TS68950/1/2

Symbol	Parameter	Value	Unit
	Supply Voltage between V^+ and AGND or DGND	– 0.3 to + 7	V
	Supply Voltage between V^+ and AGND or DGND	– 7 to + 0.3	V
	Voltage between AGND and DGND	– 0.3 to + 0.3	V
	Digital Input Voltage	DGND – 0.3 to V_{CC}^+ + 0.3	V
	Digital Output Voltage	DGND – 0.3 to V_{CC}^+ + 0.3	V
	Digital Output Current	– 20 to + 20	mA
	Analog Input Voltage	V_{CC}^- – 0.3 to V_{CC}^+ + 0.3	V
	Analog Output Voltage	V_{CC}^- – 0.3 to V_{CC}^+ + 0.3	V
	Analog Output Current	– 10 to + 10	mA
	Power Dissipation	500	mW
T_{oper}	Operating Temperature Range	0 to + 70	°C
T_{stg}	Storage Temperature	– 65 to + 150	°C

4.2. DC ELECTRICAL CHARACTERISTICS DGND = AGND = 0 V

Digital Supply

V_{CC} = 5.0V ± 5% , V_{SS} = 0, T_A = 0 to + 70°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IL}	Input Low Voltage	– 0.3		0.8	V
V_{IH}	Input High Voltage. All inputs except $\overline{RESET}$	24		V_{CC}	V
V_{IH}	$\overline{RESET}$ Input High Voltage	2.8		V_{CC}	V
I_i	Input Extal Current	– 50		+ 50	µA
I_{in}	Input Leakage Current BS0, BS1, BS2, BE3, BE4, RS, SDS, CS, SRW, $\overline{RESET}$	– 10		+ 10	µA
V_{OH}	Output High Voltage (I_{load} = – 300µA). All Outputs Except $\overline{DTACK}$	2.7			V
V_{OL}	Output Low voltage (I_{load} = 3.2mA). All Outputs			0.5	V
C_{in}	Input Capacitance		10		pF
I_{TSI}	Three State (off state) Input Current @ 2.4V/0.4V $\overline{DTACK}$, $\overline{BA}$, D0-D15, AD0-AD7	– 20		+ 20	µA
T_A	Operating Free-air Temperature (notes 1 and 2)	0		70	°C
I_{CC}	Supply Current TS75240 T_A = 25°C			480	mA
I_{CC}	T_C = 100°C			420	mA

Notes : 1. Case temperature Tc must be maintained below 100°C.
2. $R_{\theta JA}$ 39°C/watts Side-brazed ceramic DIL-48.
28°C/watts PDIL-48 heath spreader.

Analog Supply

Symbol	Parameter	Min.	Typ.	Max.	Unit
V^+	Positive Power Supply	4.75		5.25	V
V^-	Negative Power Supply	– 5.25		– 4.75	V
I^+	Positive Supply Current			35	mA
I^-	Negative Supply Current	– 35			mA

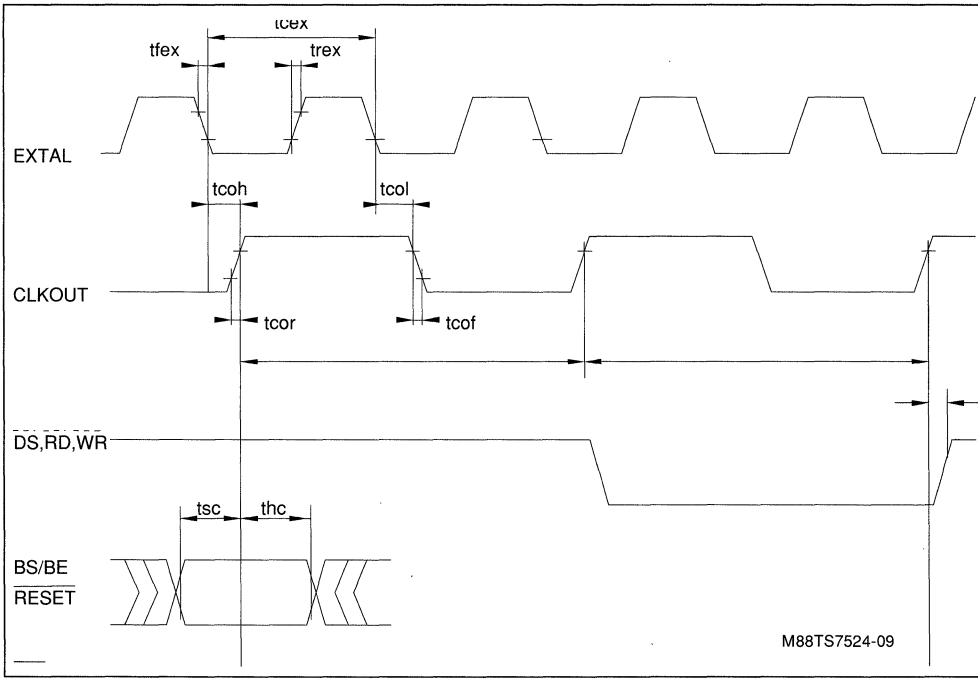
4.3. AC ELECTRICAL SPECIFICATIONS

4.3.1. CLOCK AND CONTROL PINS TIMING (V_{CC} = 5.0 V ± 5 %, T_A = 0 °C to + 70 °C, see figure 9)
OUTPUT LOAD = 50 pF + DC characteristics I load

Reference Levels : V_{IL} : 0 V V_{IH} : 2.4 V
V_{OL} : 1.5 V V_{OH} : 1.5 V tr, tf ≤ 5 ns for Input Signals

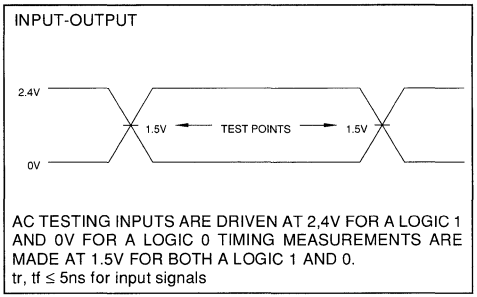
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{cex}	External Clock Cycle Time	43.4			ns
t_{fex}	External Clock Fall Time			5	ns
t_{rex}	External Clock Rise Time			5	ns
t_{coh}	EXTAL to CLKOUT High Delay		25		ns
t_{col}	EXTAL to CLKOUT Low Delay		25		ns
t_{cor}	CLKOUT Rise Time			10	ns
t_{cof}	CLKOUT Fall Time			10	ns
t_{dlc}	CLKOUT to Control Output Low ($\overline{IRQ}$, BA)			50	ns
t_{dhc}	CLKOUT to Control Output High ($\overline{IRQ}$, BA)			50	ns
t_{dsl}	CLKOUT to $\overline{DS}$, $\overline{RD}$, $\overline{WR}$ Low		5		ns
t_{dsh}	CLKOUT to $\overline{DS}$, $\overline{RP}$, $\overline{WR}$ High		5		ns
t_{sc}	Control Inputs Set-up Time (BS0 ... BE6, $\overline{RESET}$)	20			ns
t_{hc}	Control Inputs Hold Time (BS0 ... BE6, $\overline{RESET}$)	10			ns

Figure 9 : Clock and Control Pins Timing.

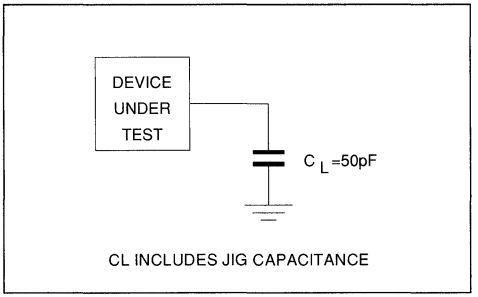


Notes : 1. tc = Instruction cycle time = 4 x tcex.
2. BE3.....BE6 min low level duration = tc.

A.C. TESTING INPUT, OUTPUT WAVEFORM



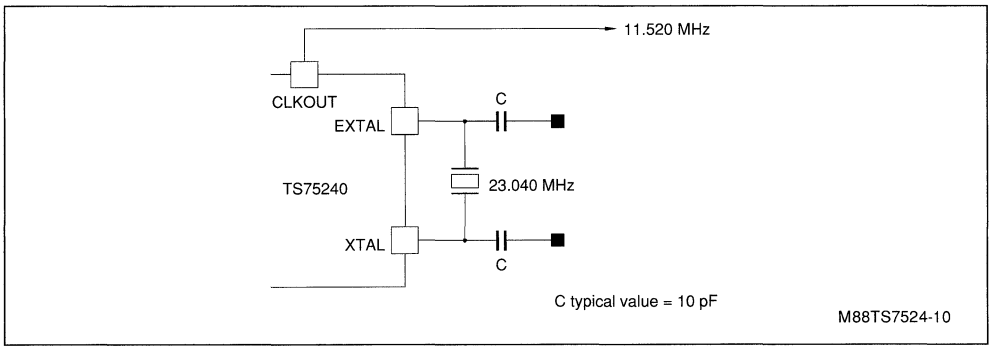
A.C. TESTING LOAD CIRCUIT



INTERNAL CLOCK OPTION

A crystal oscillator can be connected across XTAL and EXTAL. The frequency of CLKOUT is half the crystal fundamental frequency, and can be used by the control processor.

Then the 5.76 MHz required by the Analog Front End can be easily obtained.



Crystal nominal parameters :

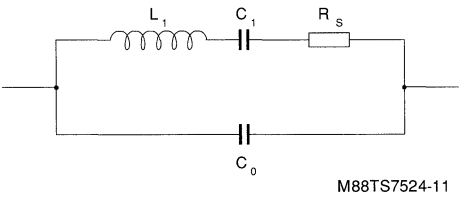
Parallel resonance fundamental mode - AT CUT

$R_S = 10\ \Omega$

$C_1 = 0.018$ pF

$C_0 = 3.5$ pF

$Q > 30$ K



4.3.2. TS68952 : CLOCK GENERATOR

Crystal Oscillator Interface

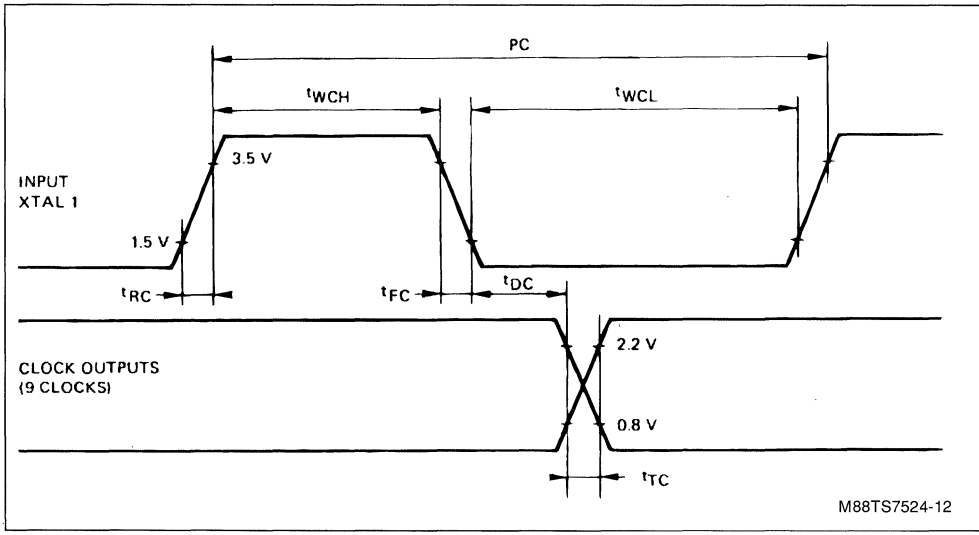
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level Voltage				1.5	V
V_{IH}	Input High Voltage		3.5			V
I_{IL}	Input Low Level Current	$DGND \leq V_I \leq V_{IL\,max}$	– 15			µA
I_{IH}	Input High Level Current	$V_{IH\,min} \leq V_I \leq V^+$			15	µA

CLOCK WAVE FORMS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PC	Main Clock Period	XTAL1 Input		173.6		ns
t_{WCL}	Main Clock Low Level Width	XTAL1 Input	50			ns
t_{WCH}	Main Clock High Level Width	XTAL1 Input	50			ns
t_{RC}	Main Clock Rise Time	XTAL1 Input			50	ns
t_{FC}	Main Clock Fall Time	XTAL1 Input			50	ns
t_{DC}	Clock Output Delay Time	All Clock Outputs CL = 50 pF			500	ns
t_{TC}	Clock Output Transition Time	All Clock Outputs CL = 50 pF			100	ns

Unless otherwise noted, electrical characteristics are specified over the operating range. Typical values are given for V^+ = 5.0 V and T_{amb} = 25 °C.

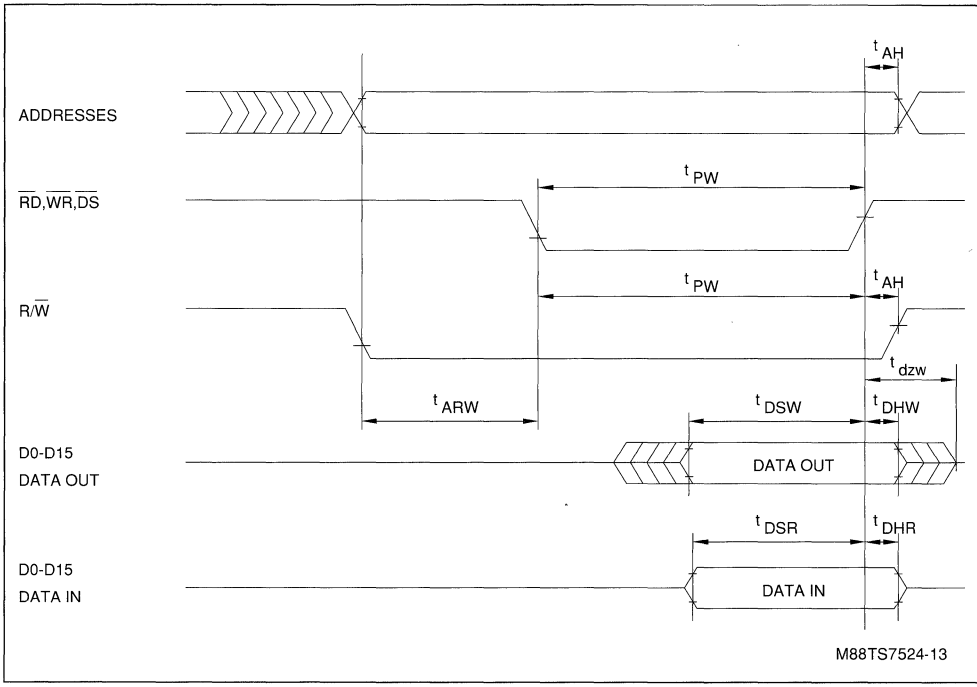
Figure 10 : Clock Generator.



4.3.3. LOCAL BUS TIMING (TS75240 and TS68950/51/52)
(V_{CC} = 5.0 V ± 5 %, T_A = 0° to + 70 °C, see figure 11)

Symbol	Parameter	Min.	Max.	Unit
t_{PW}	$\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Pulse Width	1/2 tc – 15	1/2 tc	ns
t_{AH}	Address Hold Time	10		ns
t_{DSW}	Data Set-up Time, Write Cycle	25		ns
t_{DHW}	Data Hold Time, Write Cycle	10		ns
t_{DSR}	Data Set-up Time, Read Cycle	20		ns
t_{DHR}	Data Hold Time, Read Cycle	5		ns
t_{ARW}	Address Valid to $\overline{WR}$, $\overline{DS}$, $\overline{RD}$ Low	1/2 tc – 40		ns
t_{DZW}	$\overline{DS}$ High to Data High Impedance, Write Cycle		40	ns

Figure 11 : Local Bus Timing Diagram.

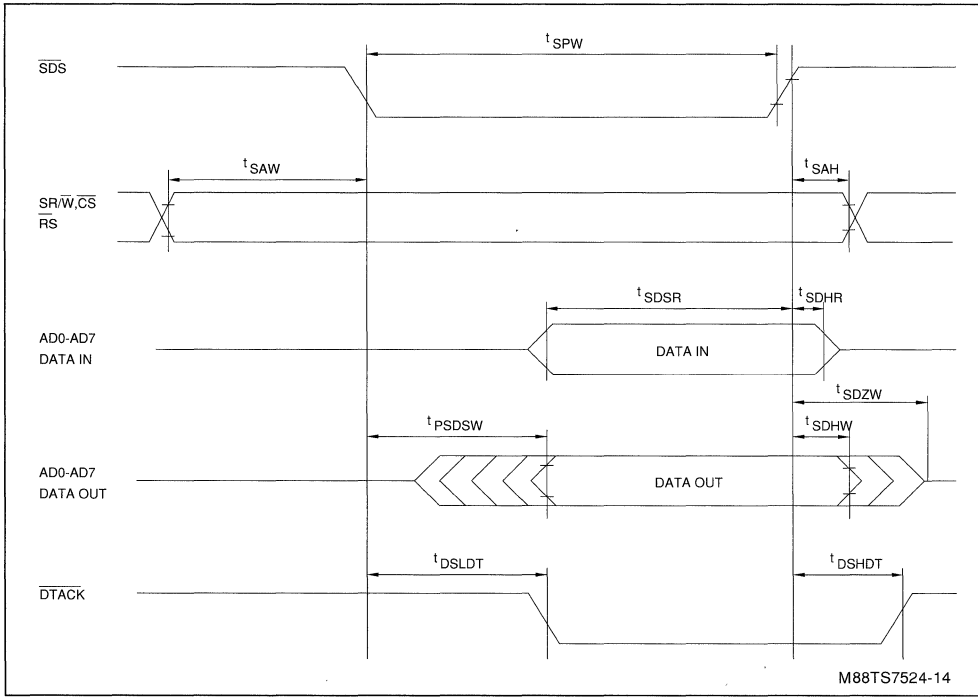


4.3.4. SYSTEM BUS TIMING (TS75240 and control processor)
V_{CC} = 5.0 V ± 5 %, T_A = 0° to + 70 °C

Symbol	Parameter	Min.	Max.	Unit
t_{SPW}	$\overline{SDS}$ Pulse Width	60		ns
t_{SAW}	SR/$\overline{W}$, $\overline{CS}$, $\overline{RS}$ Set-up Time	20		ns
t_{SAH}	SR/$\overline{W}$, $\overline{CS}$, $\overline{RS}$ Hold after $\overline{SDS}$ High	5		ns
t_{SDSR}	Data Set-up Time, Read Cycle	20		ns
t_{SDHR}	Data Hold Time, Read Cycle	5		ns
t_{PSDSW}	Data Propagation Delay, Write Cycle		35	ns
t_{SDHW}	Data Hold Time, Write Cycle	10		ns
t_{SDZW}	$\overline{SDS}$ High to Data High Impedance, Write Cycle		40	ns
t_{DSLDT}	$\overline{SDS}$ Low to $\overline{DTACK}$ Low		50	ns
t_{DSHDT}	$\overline{SDS}$ High to $\overline{DTACK}$ High*		50	ns

* DTACK is an open drain output test load include R_L = 820 Ω at V_{CC}.

Figure 12 : System Bus Timing Diagram.



4.3.5. DAA INTERFACE (DAA and TS68950 and TS68951)

Analog Transmit Output (ATO)
$V^+ = 5\ V \pm 5\ \%$, $0\ °C \leq T_{amb} \leq +70\ °C$ $V^- = -5\ V \pm 5\ \%$, $0\ °C \leq T_{amb} \leq +70\ °C$
(unless otherwise specified)

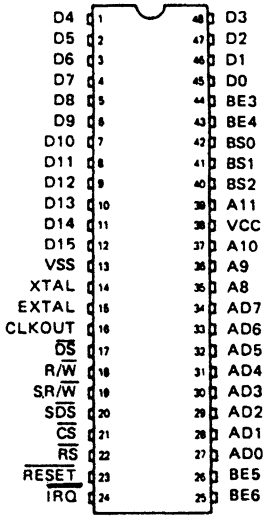
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OS}	Output DC Offset	− 250		+ 250	mV
C_L	Load Capacitance			50	pF
R_L	Load Resistance	1.2			kΩ
V_{out}	Output Voltage Swing (R_L > 1.2 kΩ C_L < 50 pF)	− 2.5		+ 2.5	V
R_{out}	Output Resistance (read cycle)			5	Ω

Receive Analog Input (RAI).

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{in}	Input Voltage	− 2.5		+ 2.5	V
I_{in}	Input Current (write cycle)	− 1		+ 1	µA

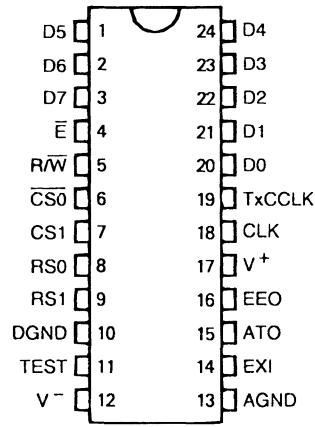
5. PIN CONNECTIONS

TS75240



M88TS7524-15

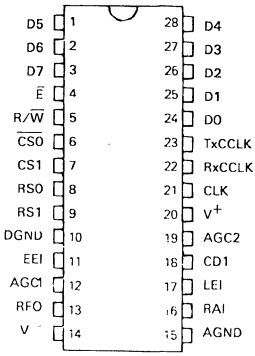
TS68950



M88TS7524-16

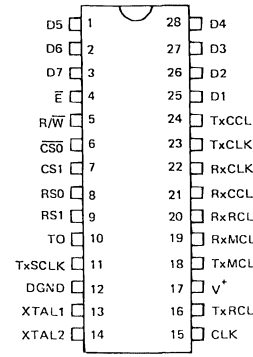
PIN CONNECTIONS (continued)

TS68951



M88TS7524-17

TS68952



M88TS7524-18

TS75240

MAFE Interface

Name	Pin	Function	Description
D0 thru D15	I/O	Local Data Bus	Only D8 thru D15 lines are used for data transfer between the TS75240 and MAFE Kit. D0 thru D7 are not used and are left unconnected.
A8 thru A11	O	Local Address Bus	Address Lines to the MAFE Kit.
$\overline{DS}$	O	$\overline{\text{Data Strobe}}$	This signal synchronizes the transfer between the TS75240 and the MAFE Kit.
R/$\overline{W}$	O	Read/$\overline{\text{Write}}$	Indicates the current bus cycle state.
CLKOUT	O	Clock Output	This signal generated by the TS75240 is at half the frequency of the crystal. It can be divided by 2 to provide the 5.76 MHz clock for the MAFE Kit.
BE3 thru BE6	I	Receive and Transmit Clocks	These four inputs are connected to the receive and transmit clocks generated by the clock generator circuit (TS68952) of the MAFE Kit.

TS75240

System Interface.

Name	Pin	Function	Description
AD0 thru AD7	I/O	System Data Bus	These bi-directional lines are used for data transfer between the TS75240 mailbox and a system processor.
$\overline{CS}$	I	$\overline{\text{Chip Select}}$	This active low input is asserted when the TS75240 is to be accessed by the system processor.
$\overline{RS}$	I	$\overline{\text{Register Select}}$	This signal is used with $\overline{CS}$ to control the data transfer between the system processor and the TS75240 mailbox.
$\overline{SDS}$	I	$\overline{\text{System Data Strobe}}$	Synchronizes the transfer on the system bus.
SR/$\overline{W}$	I	System Read/$\overline{\text{Write}}$	Indicates the current system bus cycle state.
$\overline{IRQ}$	O	$\overline{\text{Interrupt Request}}$	Handshake signal sent to the master to gain access to the mailbox.

Others Pins.

Name	Pin	Function	Description
BS0 thru BS2	I	Branch on State	These three inputs are not used and must be grounded.
EXTAL	I	Clock	Crystal Input for Internal Oscillator or Input Pin for External Oscillator.
XTAL	I	Clock	Together with EXTAL this pin is used for the external 23.040 MHz crystal.
V_{CC}	Supply	Power Supply	
V_{SS}	Supply	Ground	
$\overline{RESET}$	I	Reset	

TS68950

Name	N°	Description
D5-D7	1-3	8 bit data bus inputs giving access to Tx estimated echo, control and address registers. (same for pins 20-24).
$\overline{E}$	4	Enable Input. Data are strobed on the positive transitions of this input.
R/$\overline{W}$	5	Read/Write Selection. Internal registers can be written when R/$\overline{W}$ = 0. Read mode is not used.
$\overline{CS0}$-CS1	6-7	Chip Select Inputs. The chip set is selected when $\overline{CSO}$ = 0 and CS1 = 1.
RS0-RS1	8-9	Register Select Inputs. Used to select D/A input registers or control/address registers in the write mode.
DGND	10	Digital Ground = 0 V. All digital signals are referenced to this pin.
TEST	11	Test Input. Used for test purposes. This pin must be grounded in all applications
V^-	12	Negative Supply Voltage = – 5 V ± 5 %
AGND	13	Analog Ground = 0 V.
EXI	14	Programmable analog input tied to filter or attenuator input according to the RC4 register content.
ATO	15	Analog Transmit Output.
EEO	16	Analog Echo Cancelling Output.
V^+	17	Positive Power Supply Voltage = + 5 V ±5 %
CLK	18	Master Clock Input. Nominal Frequency 1.44 MHz
TxCCLK	19	Transmit Conversion Clock Input.
D0-D4	20-24	See description of D5-D7 (pins1-3) given above.

TS68951

Name	N°	Description
D5-D7	1-3	Data Bus.
$\overline{E}$	4	Enable Input. Enables Selection Inputs. Active on a low level for read operation. Active on a positive level for write operation.
R/$\overline{W}$	5	Read/Write Selection Input. Read operation is selected on a high level. Write operation is selected on a low level.
$\overline{CS0}$-CS1	6-7	Chip Select Inputs. The chip set is selected when $\overline{CS0}$ = 0 and CS1 = 1.
RS0-RS1	8-9	Register Select Inputs. Select the register involved in a read or write operation.
DGND	10	Digital Ground. All digital signals are referenced to this pin.
EEI	11	Estimated Echo Input. When operating in echo cancelling mode, this signal is added to the reception band-pass filter output.
AGC1	12	Analog Input of the Automatic Gain Control Amplifier and of the Carrier Level Dectector.
RFO	13	Reception Filter Analog Output. Designed to be connected to AGC1 input through a 1 µF non polarized capacitor.
V^-	14	Negative Supply Voltage = – 5 V ± 5 %
AGND	15	Analog Ground. All analog signals are referenced to this pin.
RAI	16	Receive Analog Input. Analog input tied to the transmission line.
LEI	17	Local Echo Input. Analog input subtracted from the receive anti-aliasing filter output.
CD1	18	This pin must be connected to the analog ground trough a 1 µF non polarized capacitor, in order to cancel the offset voltage of the carrier level detector amplifier.
AGC2	19	This pin must be connected to the analog ground trough a 1 µF non polarized capacitor, in order to cancel the offset voltage of the offset AGC amplifier.
V^+	20	Positive Supply Voltage = + 5 V ± 5 %
CLK	21	Master Clock Input. Nominal Frequency 1.44 MHz.
RxCCLK	22	Receive Conversion Clock.
TxCCLK	23	Transmit Conversion Clock.
D0-D4	24-28	Data Bus.

TS68952

Name	N°	Description
D5-D7	1-3	Data Bus Inputs to Internal Registers
$\overline{E}$	4	Enable Input. Data are strobed on the positive transitions of this input.
R/$\overline{W}$	5	Read/Write Selection Input. Internal registers can be written when R/$\overline{W}$ = 0. Read mode is only used for Rx front-end-chip.
$\overline{CS0}$-CS1	6-7	Chip Select Inputs. The chip set is selected when $\overline{CS0}$ = 0 and CS1 = 1.
RS0-RS1	8-9	Register Select Inputs. Used to select address or control registers
TO	10	Test Output. Must be left open in all applications.
TxSCLK	11	Transmit Synchronizing Clock Input. Normally tied to an external clock terminal. When this pin is tied to a permanent logical level, transmit DPLL free-runs or can be synchronized to the receive clock system.
DGND	12	Digital Ground = 0 V. All digital signals are referenced to this pin.
XTAL1	13	Crystal Oscillator or Pulse Generator Input.
XTAL2	14	Crystal Oscillator Output.
CLK	15	1.44 MHz Clock Output. Useful for TS68950/51.
TxRCLK	16	Transmit Baud Rate Clock Output
V^+	17	Positive Supply Voltage = + 5 V ± 5 %
TxMCLK	18	Transmit Multiplexing Clock Output
RxMCLK	19	Receive Multiplexing Clock Output
RxRCLK	20	Receive Baud Rate Clock Output
RxCCLK	21	Receive Conversion Clock Output
RxCLK	22	Receive Bit Rate Clock Output
TxCLK	23	Transmit Bit Rate Clock Output
TxCCLK	24	Transmit Conversion Clock Output
D1-D4	25-28	Data Bus Inputs to Internal Registers (D0 is not used)

6. ORDERING INFORMATION

The TS7524 corresponds to four different components which must be ordered separately.

Furthermore, a stand-alone evaluation board is available for a fast characterization improvement of the TS7524 in a real application.

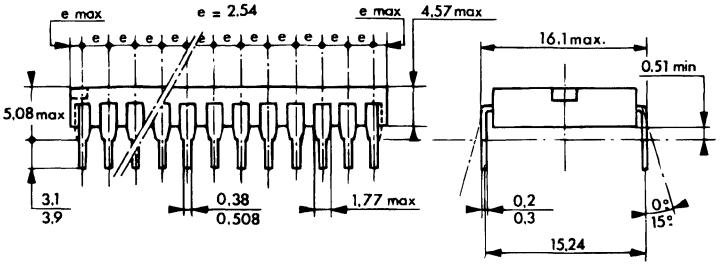
Part Number	Temp Range	Package	Device
TS75240CP/XX	0 °C to 70 °C	DIP-48	V. 22Bis Masked DSP
TS68950CP	0 °C to 70 °C	DIP-24	Transmit Analog Interface
TS68951CP	0 °C to 70 °C	DIP-28	Receive Analog Interface
TS68952CP	0 °C to 70 °C	DIP-28	Clock Generator Interface
TS7524EVA *	N. A		Stand Alone Evaluation Board

* Contact your SGS-THOMSON representative.

7. PACKAGE MECHANICAL DATA

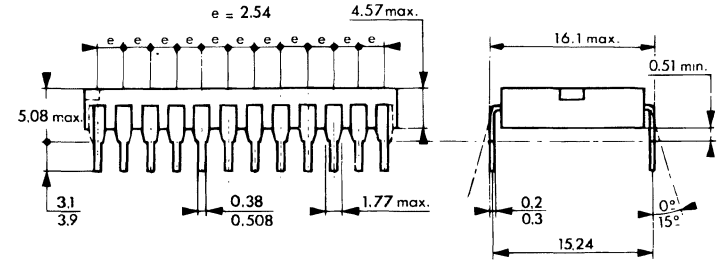
TS75240

48 Pins – Plastic Dip.



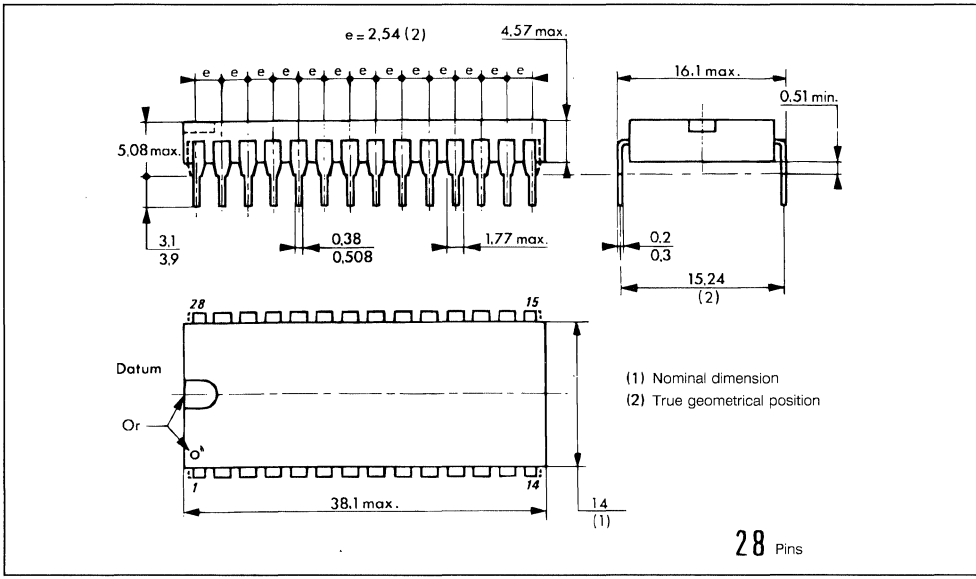
TS68950

24 Pins – Plastic Dip.



TS68951/TS68952

28 Pins – Plastic Dip.



ELECTRICAL CONSIDERATIONS

To avoid possible high frequency problems, the following precautions should be considered for PC board layout design :

- A ground plane on the component side connected to analog ground of the TS68950/51
- Analog and Digital ground tracks corresponding to different signals, e.g. clocks, input signals, references, ... should be adequately separated and terminated at a single point.
- Optimal distribution of power supplies and ground links using star-connection.
- Adequate decoupling capacitor mounted as close as possible to each device, and connected to analog ground.
- DSP and MAFE power supplies should be separated.

APPENDIX A

TRANSMIT/RECEIVE COMMAND WORDS

Transmit Command Word.

BIT	First Byte	Second Byte	Third Byte				
0	Transmit Mode Selection	Transmit Attenuation	Transmit (0)				
1	0000 : Modem Disabled 0001 : V.22 Bis		D0	DPSK	QAM		DTMF
2	0010 : V.22 0011 : B212 0100 : V.23 0101 : V.21		D1				
3	0110 : Bell 103 0111 : D.T.M.F.		D2	0			
4	Transmit Signalling 00 : Signalling Disabled		D3	0			
5	01 : 550 Hz 11 : 1800 Hz	Scrambler (ON/$\overline{OFF}$)	D4	0	0		0
6	**Reserved**	**Reserved**	D5	0	0		0
7	$\overline{ANSW}$/ORIG or DTMF	V.22 Binary Rate Select or DTMF	$\overline{Transmit\ Enable}$				

Note : All the "RESERVED" bits must be cleared to "0" by the user.

Receive Command Word.

BIT	First Byte	Second Byte	Third Byte
0	Receive. Mode Selection	**Reserved**	Receive (1)
1	0000 : Modem Disabled 0001 : V.22 Bis		**Reserved**
2	0010 : V.22 0011 : B212 0100 : V.23 0101 : V.21		
3	0110 : Bell 103 0111 : Call Prog / Answer Tone		
4	Answer Tone Selection		
5	Tx Synchronization	Descrambler (ON/$\overline{OFF}$)	
6	Carrier Detect Level	**Reserved**	
7	$\overline{Answer}$/originate	V.22 Binary Rate Select	

Note : All the "RESERVED" bits must be cleared to "0" by the user.

APPENDIX B

TRANSMIT/RECEIVE STATUS WORDS

Transmit Status Word.

BIT	First Byte	Second Byte	Third Byte
0	Transmit (0)	Reserved	Reserved
1	Reserved		
2			
3			
4			
5			
6			
7			

Receive Status Word.

BIT	First Byte		Second Byte	Third Byte			
0	Receive (1)		Reserved	Reserved			
1	D0	Data Before Descrambling (Q.A.M. , D.P.S.K.)		D0	Data After Descr. (Q.A.M., D.P.S.K.)	D0	Data (F. S. K.)
2	D1			D1		D1	
3	D2			D2		D2	
4	D3		Equalization Status	D3		D3	
5	Reserved		$\overline{\text{Signal Quality}}$	1		D4	
6	S1 Sequence		$\overline{\text{Carrier Detection}}$	1		D5	
7	$\overline{\text{S1 Sequence or Call Progress Tone Detection}}$		Reserved	$\overline{\text{Answer Tone Detection}}$			

Note : In QAM and DPSK modes, both for the data after and before descrambling, the unused bits are set to "1" by the TS7524.

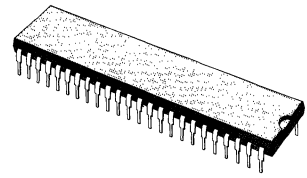
SGS-THOMSON MICROELECTRONICS

TS7532

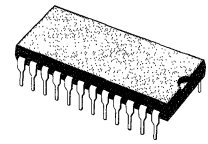
V. 32 MODEM CHIP SET

ADVANCE DATA

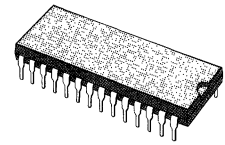
- CCITT V.32 COMPATIBLE MODEM CHIP SET [see ref 1 of Appendix D]
- INTEGRATED IMPLEMENTATION ON THREE DSP AND THREE MAFE CHIPS
- FULL DUPLEX OPERATION AT 9600 AND 4800 BPS
- FULL IMPLEMENTATION OF THE V.32 HAND-SHAKE
- DYNAMIC RANGE : 43 dB
- TWO SATELLITE HOPS AND FREQUENCY OFFSET CAPABILITIES (10 Hz) FOR THE FAR END ECHO CANCELLER
- TRELLIS ENCODING AND VITERBI DECODING
- 12.5 % ROLL-OFF RAISED COSINE TRANSMITTER PULSE SHAPING
- HIGH PERFORMANCE PASSBAND FRACTIONALLY SPACED ADAPTIVE EQUALIZER
- SIGNAL QUALITY MONITORING
- PARALLEL INTERFACE TO STANDARD MICROPROCESSORS
- BIT RATE DATA CLOCKS PROVIDED FOR SYNCHRONOUS DATA TRANSFER
- FULL DIAGNOSTIC CAPABILITY
- DTMF GENERATION
- CALL PROGRESS TONE DETECTION
- FUTURE UPGRADE TO INCLUDE V.22 BIS, V.22, B212A AND FSK (TOTALLY PIN-COMPATIBLE)
- SOFTWARE LICENSE AND DEVELOPMENT TOOLS AVAILABLE FOR EASY CUSTOMIZATION



P
DIP48
(Plastic Package)
TS75320/1/2



P
DIP24
(Plastic Package)
TS68950



P
DIP28
(Plastic Package)
TS68951/2

(Ordering information at the end of the datasheet)

DESCRIPTION

The SGS-THOMSON Microelectronics V.32 chip set is a highly integrated modem engine, which can operate in full duplex at 9600 and 4800 bps. The modem hardware consists of three analog front end (MAFE) chips, three DSP processor chips and additional memory chips.

The three SGS-THOMSON analog front end chips (TS68950/1/2) are the transmit interface, the receive interface and the clock generator respectively.

The modem signal processing functions are implemented on three TS68930 programmable digital signal processors. TS75320 supports the echo canceller, TS75321 the transmitter, handshake and user's interface and TS75322 the receiver.

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1. PIN DESCRIPTION

1.1. SYSTEM INTERFACE

TS75321 (DSP#1 Transmitter and Handshake)

Pin Name	Pin N°	Type	Signal Name	Description
AD0.AD7	27.34	I/O	D0H.D7H	System Data Bus : these lines are used for data transfer between the TS7532 mailbox and the host processor.
$\overline{CS}$	21	I	CSL	Chip Select : this input is asserted when the TS7532 is to be accessed by the host processor.
$\overline{RS}$	22	I	RSL	Register Select : this signal is used to control the data transfers between the host processor and the TS7532 mailbox.
$\overline{SDS}$	20	I	DSL	System Data Strobe : synchronizes the transfer between the TS7532 mailbox and the host processor.
SR/$\overline{W}$	19	I	RWL	System Read/Write : control signal for the TS7532 mailbox operation.
$\overline{IRQ}$	24	O	INTL	Interrupt Request : signal sent to the host processor to access the TS7532 mailbox.
$\overline{RESET}$	23	I	RSTL1	Master Reset of DSP#1

1.2. ANALOG INTERFACE

TS68950 (Analog Front End Transmitter)

Pin Name	Pin N°	Type	Signal Name	Description
AT0	15	AT0	AT0	Analog Transmit Output

TS68951 (Analog Front End Receiver)

Pin Name	Pin N°	Type	Signal Name	Description
RAI	16	I	RAI	Receive Analog Input
LEI	17	I	LEI	Local Echo Input. This signal is subtracted from signal RAI.

1.3. CLOCK INTERFACE

TS68952 (Clock Generator)

Pin Name	Pin N°	Type	Signal Name	Description
TxCLK	23	O	TxCLK	Transmit Bit Clock
TxRCLK	16	O	TxRCLK	Transmit Baud Clock
TxCCLK	24	O	TxCCLK	Transmit Conversion Clock
TxMCLK	18	O	TxMCLK	Transmit Multiplex Clock
RxCLK	22	O	RxCLK	Receive Bit Clock
RxRCLK	20	O	RxRCLK	Receive Baud Clock
RxCCLK	21	O	RxCCLK	Receive Conversion Clock
RxMCLK	19	O	RxMCLK	Receive Multiplex Clock
TxSCLK	11	I	TxSCLK	Transmit Synchro Clock : can be used to synchronize the transmitter on an external bit clock provided by the RS232C (or V.24) junction.

2. FUNCTIONAL DESCRIPTION

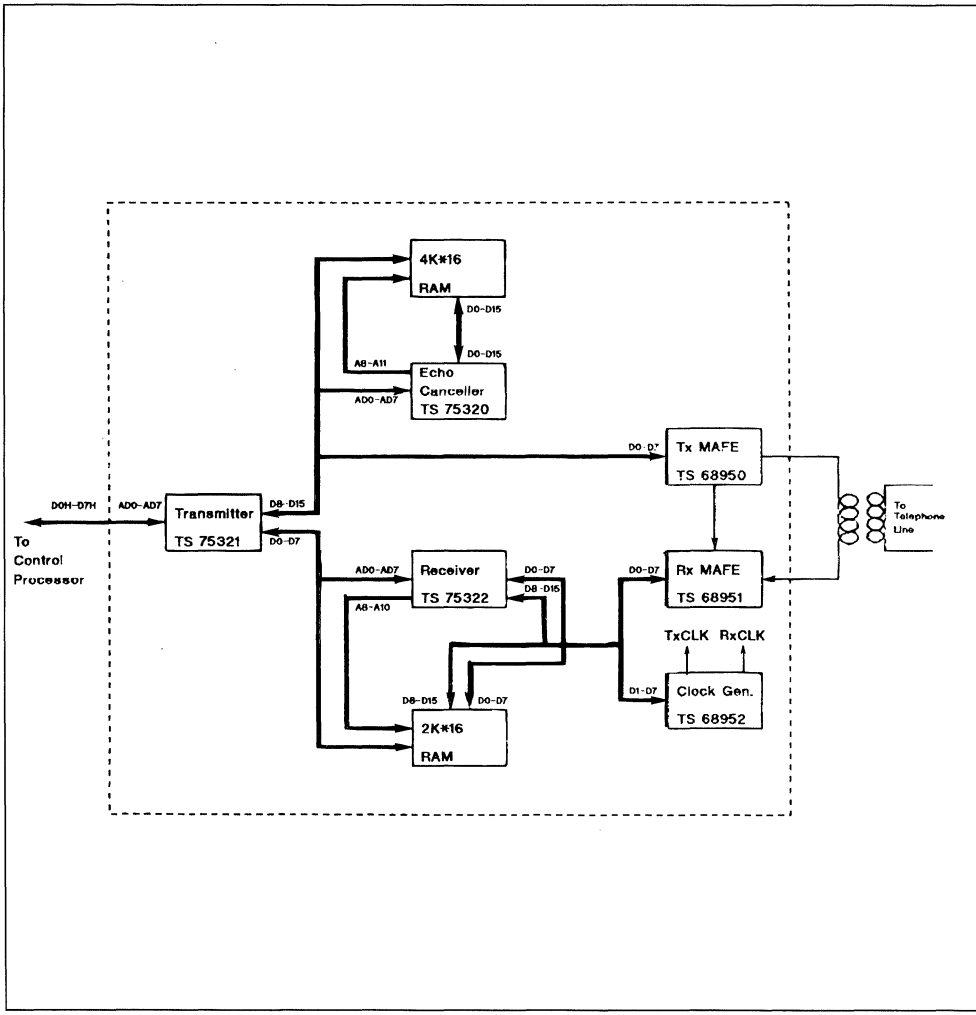
2.1. SYSTEM ARCHITECTURE

The SGS-THOMSON V.32 chip set is a highly integrated modem engine which provides the functionality and performance requirements for full-duplex 9600 bps modem solutions at a low cost and with a small circuit area. At the heart of the modem engine are three SGS-THOMSON DSPs which implement the complete signal processing and control functions. The analog front end of the modem engine consists of the SGS-THOMSON MAFE three-chip set which is designed to meet the requirements of high-speed modem applications and particularly V.32 modems. The only other components in the modem engine are the external RAM chips used for the far-end echo canceller delay line and the Viterbi decoder.

2.2 PROCESSOR AND MAFE CHIPS ARRANGEMENT

Figure 1 shows the interconnections between the MAFE and signal processors.

Figure 1 : Hardware Architecture.



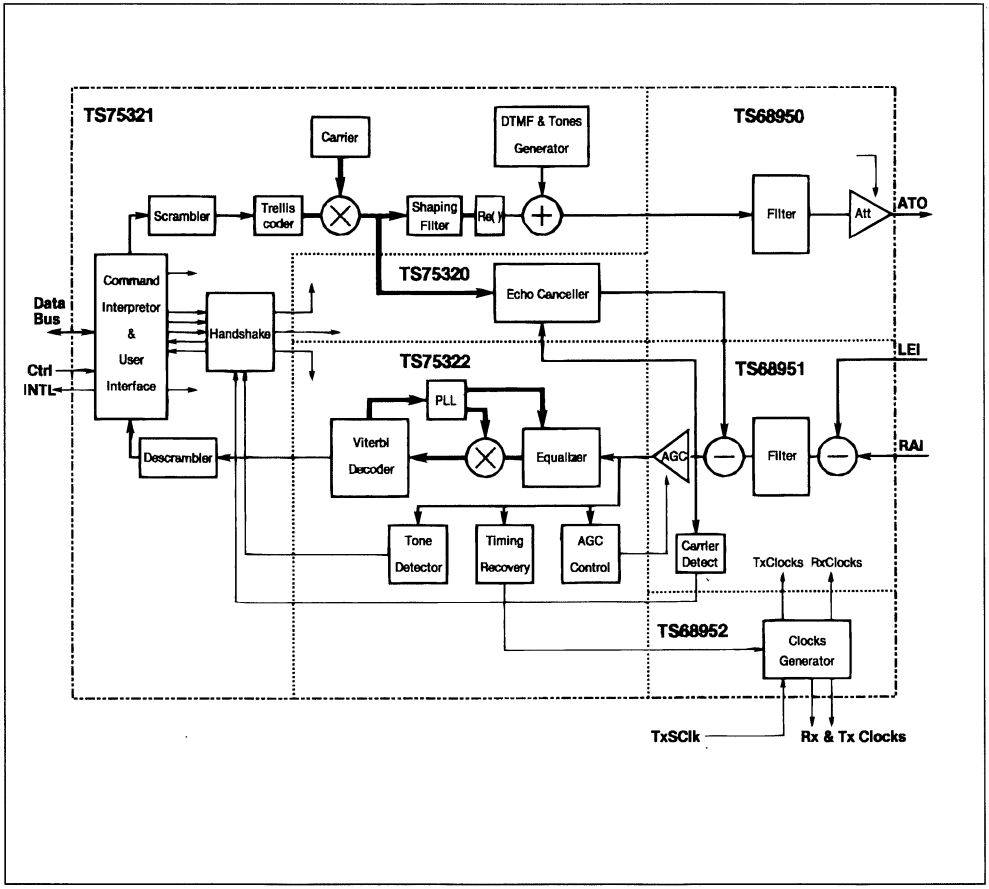
DSP 1 communicates with the control processor through its system bus, AD0-AD7. It is also connected to the two other DSPs through its D0-D7 and D8-D15 data buses to transfer data, to pass a control command to the DSPs and to get the modem operation status and then pass it to the control processor. The transmitter, V.32 handshake and part of the receiver algorithms are implemented in this processor. DSP 0 implements the echo cancellation function. 4Kx16 of RAM are connected to this processor to implement the data delay line for the far end echo cancellation. DSP 2 implements most of the receiver functions. 2Kx16 of RAM are attached to it due to the requirements of the Viterbi decoder.

The transmitter interface chip, TS68950 [see ref 5 of Appendix D], is connected to the 8 MSB's of the DSP 1 data bus. The echo replica is sent from DSP 1 to TS68950 then to the receiver interface chip, TS68951 [see ref 6 of Appendix D], after conversion to analog format. This chip and the clock generator chip, TS68952 [see ref 7 of Appendix D], are connected to the 8 MSB's of the DSP 2 data bus. The clock generator chip generates the A/D and D/A sampling clocks and the data bit and baud rate clocks.

2.3. OPERATION

2.3.1. MODES. The modem implementation is fully compatible with the CCITT recommendation V.32. It operates at two different bit rates, 9600 and 4800 bps. In the 9600 bps mode, the trellis encoder and the Viterbi decoder can be switched in or out. Both the bit rate and trellis options are determined during the initial modem handshake sequence.

Figure 2 : Functional Block Diagram.



2.3.2. SIGNAL SPECTRUM SHAPING. A square root of 12.5 percent roll-off raised cosine filter is implemented in the transmitter to properly shape the transmit signal pulse. This filter is chosen based on a compromise of two considerations. First, the signal should have a narrow spectrum to avoid severe distortion on the telephone line. Second, the signal spectrum should be made as wide as possible to facilitate timing recovery in receiver.

2.3.3. ECHO CANCELLATION. The echo canceller is implemented on a single DSP [see ref 8 of Appendix D] with its associated external RAM. It cancels both near-end and far-end echoes even in the presence of frequency offset in the far-end echo path. The near-end echo cancellation is better than 55 dB and the residual near-end echo is smaller than - 65 dBm with a near-end echo level of - 10 dBm at the receiver input and a far-end signal level of - 43 dBm.

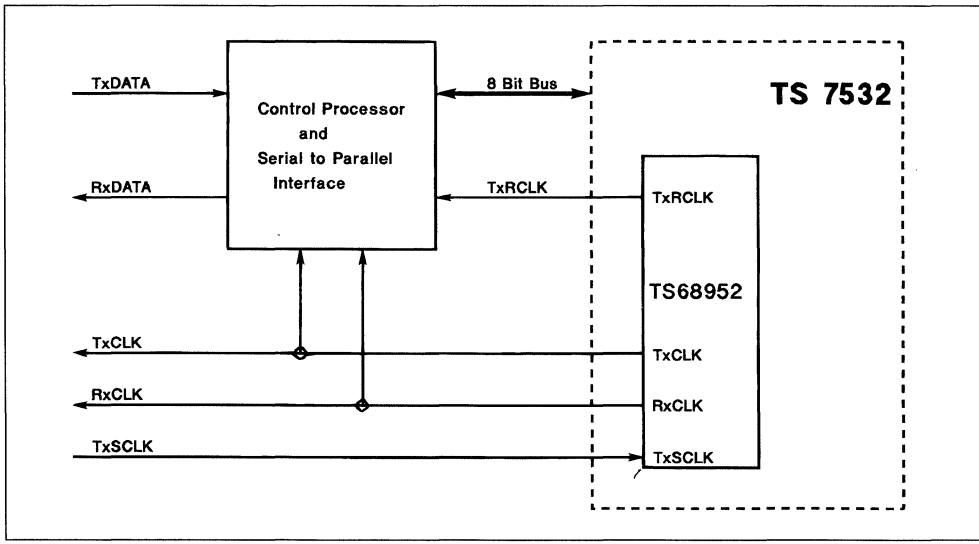
The combined near-end and far-end echo cancellers maintain the residual echo level 24 dB below the received signal even if the far-end echo signal path introduces up to 10 Hz of frequency offset. This level of cancellation is achieved when the far-end echo is 8 dB below the received far-end signal.

2.3.4. RECEIVER DESCRIPTION. The incoming signal is sent to the receiver interface chip to have the echo removed before being sent to DSP 2. The timing recovery algorithm takes the signal after the echo cancellation to derive the timing error to control the sampling phase of the A/D. It is able to cope with distant modem frequency drifts up to $\pm 2.10^{-4}$ as per CCITT rec. The A/D output samples are sent to the adaptive equalizer and the signal energy estimator for the gain control. The adaptive equalizer outputs a complex number every baud interval, which is then phase corrected by the carrier recovery loop. The Viterbi decoder makes hard decisions on the phase corrected samples for the adaptation of the equalizer and carrier recovery. It also makes soft decisions with an optimum decoding depth.

2.3.5. EQUALIZATION. The modem receiver has a passband T/3 fractionally spaced automatic adaptive equalizer which can compensate for the signal degradation caused by low quality line conditions.

2.3.6. SYNCHRONOUS AND ASYNCHRONOUS DATA TRANSFER. The V. 32 modem engine provides the control processor and the DTE with both the transmit and the receive bit clocks (Figure 3). These clocks are generated by the TS68952 and are independent of each other. The receive clock (RxCLK) is derived from the received data signal. The transmit clock (TxCLK) is free-running at the nominal bit rate (9600 or 4800 bps) except during Digital Loopback Mode when it is synchronous to the RxCLK. If the transmit clock is free-running and an external bit clock signal from the terminal is connected to point TxSCLK then the transmit bit clock will be synchronized to that signal. The baud clocks (TxRCLK and RxRCLK) are also available to the control processor. If the TxSCLK pin is not used, it should be tied to a fixed logic level.

Figure 3 : Clock Signals for Synchronous Transmission.



The control processor interface is synchronous with the transmit baud clock. Eight bits of data are transferred from the control processor to DSP 1 for each information exchange. At 9600 bps, the data is transmitted every 2 bauds and the data is transmitted every 4 bauds for 4800 bps. The received bits are also nominally transferred from DSP 1 to the control processor once every two transmit baud intervals. When the transmitter is not synchronized with the receiver, however, the receive baud interval may be slightly shorter or longer than the transmit baud interval. If it is shorter, it is necessary to periodically pass 16 received bits from DSP 1 to the control processor. If it is longer, then periodically, there will be no data transmitted from DSP 1 to the control processor. Since the received bits are being passed to the DTE at a fixed rate equal to the RxCLK, some buffering is necessary in the control processor.

For asynchronous transmission, the clocks are not required by the DTE. But since the control processor to DSP 1 interface is still synchronous with respect to the transmit baud clock, the control processor must implement the asynchronous to synchronous conversion (as specified in the V. 22 bis recommendation, for example). This will consist of inserting or deleting stop bits as required, to ensure that the transmitted bit rate is within 0.01 % of the nominal rate (9600 or 4800 bps).

2.3.7. TONE GENERATOR. The V.32 Engine has thirteen tone commands to quickly program the tone generators to generate the 2100 Hz Answer Tone (ANSWR) and the tone pairs for DTMF digits (DTMF0, ..., DTMF9, DTMF*, DTMF#). Silence, i.e. termination of tone generation, is accomplished by the use of a fourteenth command, SLNTS. These commands provide the tones and control required for normal operation of the modem.

Some circumstances might arise where additional tones are desired. For such cases, the V.32 Engine provides the user with the ability to generate such additional tones. This special feature is achieved through use of the tone control commands.

The V.32 Engine maintains a pair of locations which are reserved for tone generation parameters. These locations are denoted as TONE1 and TONE2. These locations may be programmed by the use of the define tone commands, DEFT1 and DEFT2. These commands provide the two tone generators with the phase increment of the tone to be generated with respect to the 7200 Hz sample rate.

The normal tone commands automatically program the tone generators. The DEFT1 and DEFT2 commands do not change the enabled or disabled state of the tone generators. If a tone is being generated when the DEFT command is received, the new tone will be generated without further action on the part of the user. If tone generation was not in progress it is not started.

Enabling the tone generators is accomplished by the tone control commands TGEN0, TGEN1, TGEN2, and TGEN12. Each of these commands affects both tone generators. TGEN0 disables both tone generators and TGEN12 enables both tone generators. To enable tone generator 1 and disable tone generator 2 the TGEN1 command is used. For the reverse condition, with generator 1 disabled and generator 2 enabled, the TGEN2 command is employed. if both tone generators are enabled, one of the tone levels can be scaled as specified by the control processor.

Refer to the command in appendix A for more detailed information.

Generation of special user tones is not part of the normal data communications operations of the modem. Use of this feature may interfere with data transfer operations. It is the responsability of the user to insure that the tone generators are used at a time when such interference will not occur and to disable both tone generators when the tone generation operations have been completed.

2.3.8. TEST MODES.The modem can be configured in two test modes, namely analog loop back and digital loop back modes. These loop back modes conform to the test loops 3 and 2 respectively defined in CCITT recommendation V.54.

In the local analog loop back mode, the transmitter signal is directly fed back into the local receiver input with the echo canceller enabled. The user is responsible for supplying a switch, which is controllable by the control processor, to enable or disable the analog loop back mode. The receiver descrambler is set as the inverse of the transmitter scrambler so that the receiver detects correct bits.

If the modem is configured in the digital loop back mode, the transmitter clock is locked to the receiver clock and the received bits are used as the transmitter input.

2.3.9. POWER ON INITIALIZATION. When the power is turned on, the transmitter interface sets the output signal attenuation to infinite. This avoids undesirable signal transmission on the telephone line [see ref 5 of Appendix D]. The gain of the AGC in the receive interface is set at the lowest level to avoid signal clipping during the initial handshake. The clock generator is programmed to generate all the necessary clocks for the 9600 bps mode. The clocks include the 7200 Hz sampling clock, the 2400 Hz baud rate clocks and the 9600 bps bit rate clocks. The

transmit clocks are free running when the TxSClk pin is tied to a fixed logic level. Otherwise, the transmit bit clock is synchronized to the frequency present at the TxSClk pin. DSP 1 is configured properly to receive commands from the control processor.

2.4. MODEM INTERFACE [Figure 4]

2.4.1. ANALOG INTERFACE. The transmit signal at the tip and ring is programmable over a 22 dB dynamic range by 2 dB steps in TS68950. The signal level can be further scaled to any value by setting a scaling factor in the DSP. The nominal Transmit level, at the ATO pin is – 5.7 dBm.

2.4.2. DIGITAL INTERFACE. The DSP and control processor interface complies with the system bus interface of the TS68930. The interface to the control processor is managed by DSP 1 as shown in Figure 1. The DSP signals which are presented to the interface, and a brief definition of the signals are tabulated in table 1.

Table 1 : Digital Interface Signals.

Interface Signals	Signal Definition
D0H	Data Bus (LSB)
D1H	Data Bus
D2H	Data Bus
D3H	Data Bus
D4H	Data Bus
D5H	Data Bus
D6H	Data Bus
D7H	Data Bus (MSB)
RWL	Write Signal
DSL	Data Strobe
INTL	Mailbox Handshake
CSL	DSP Select
RSL	Register Select
TxRCLK	Transmit baud rate clock
RxRCLK	Receive baud rate clock
TxCLK	Transmit bit rate clock
RxCLK	Receive bit rate clock
TxMCLK	Transmit multiplex clock
RxMCLK	Receive multiplex clock
TxSCLK	Transmit terminal clock

All information exchanges across this interface conform to the three byte mailbox structure [see ref 4 of Appendix D] and protocol of the DSP. As may be seen in the table, the DSP generates a control signal, INTL, which defines the mailbox handshake operation.

2.4.3. CONTROL PROCESSOR/DSP INTERFACE. As seen by the software in the user provided control processor, DSP 1 is a synchronous machine. It requires the attention of the control processor at regular intervals in order to perform properly. Any failure of the control processor to interact with the modem engine in a timely manner will result in reduced performance or improper operation.

Each interaction begins when the control processor sends a three byte command to the mailbox. Once the command has been written to the mailbox, the ownership of the mailbox is relinquished by the control processor. Upon acquisition of the mailbox, DSP 1 reads the command bytes and then sends a three byte response to the mailbox. Then, DSP 1 relinquishes the ownership of the mailbox back to the control processor. The received command is then decoded and the embedded data and/or operational parameters are extracted and acted upon as appropriate. The modem status information will be collected for the next mailbox exchange. The control processor handles the returned information as soon as it regains the ownership of the mailbox.

Because the control processor owns the mailbox initially, it may store a command at any time before it is required by DSP 1. After this, the mailbox becomes available to DSP1 and can be read by it when required.

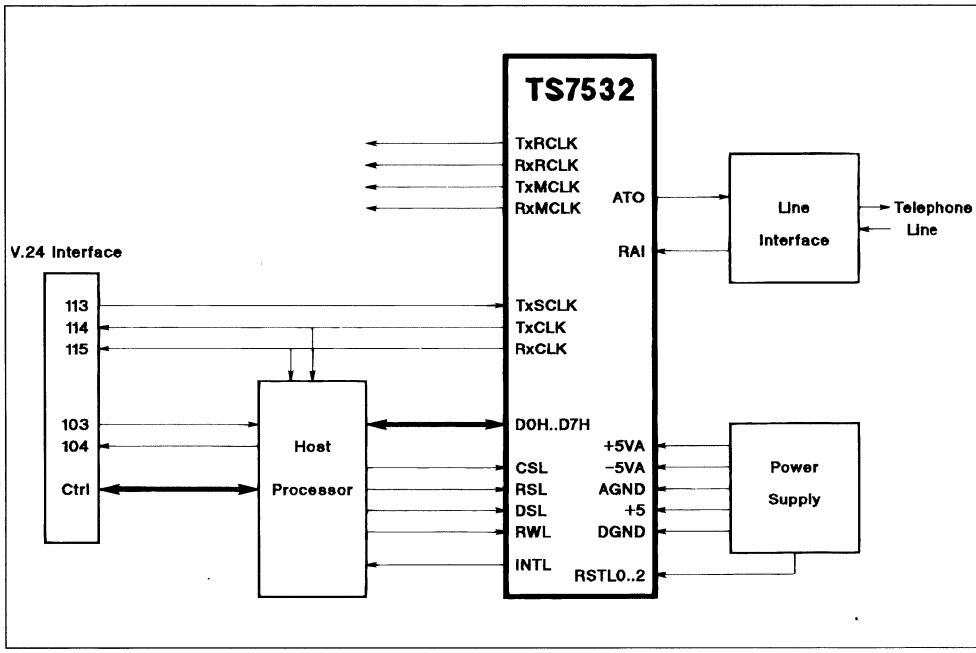
2.4.4. MAILBOX DESCRIPTION.The mailbox located internally to the DSP contains 3-byte input (RIN) and 3-byte output (ROUT) shift registers. The DSP has an internal flag RDYOIN which indicates whether the DSP (RDYOIN = 0) or control processor (RDYOIN = 1) has access to the mailbox. The DSP can relinquish its accessability to the mailbox by setting RDYOIN but it can no longer regain access to the mailbox as RDYOIN is reset only after the control processor relinquishes its accessability to the mailbox. The access protocol and system bus transfers are controlled by an internal I/O sequencer within the DSP described as follows :

1. The mailbox is made available to the control processor by the DSP program which sets RDYOIN flag to 1. This action will cause INTL mailbox handshake signal to switch to the active (low) state.
2. The control processor detects INTL active and dummy reads the mailbox by forcing DSP Select (CSL) and Register Select (RSL) low along with write signal (RWL) high. The activated Data Strobe signal (DSL = 0) validates the above signals.
3. The DSP detects the dummy read of its mailbox via the control signals mentioned in 2 and negates INTL mailbox handshake signal within 800 ns.
4. The control processor detects the negation of INTL indicating that the DSP mailbox is available for data transfers. The control processor writes

three 8-bit bytes and/or reads three 8-bit bytes in the mailbox shift registers RIN, ROUT respectively.

5. The exchange protocol described above is terminated by the control processor performing a dummy read of the mailbox as in 2 but with RSL in the high state.
6. The RDYOIN flag within the DSP is cleared to 0 by the dummy read of the mailbox in step 5 and the DSP now has access to RIN and ROUT registers within the mailbox.

Figure 4 : Functional Interconnect Diagram.



3. USER INTERFACE - COMMAND SET

The command set has the following attractive features :

- user friendly with easy to remember mnemonics
- allows straightforward expansion with new commands to suit specific customization requirements
- fully compatible with other SGS-THOMSON DSP-based modem products.

The command set has been designed to provide the necessary functional control of the V.32 Engine. Each command falls into one of several groups, based on function and the presence or absence of parameters. The length of the OP code varies with instruction type, but in all cases, a command consists of three bytes.

The commands which pass parameters or data to DSP 1 have a short OP code format. Byte 0 forms the OP code portion of the command. Bytes 1 and 2 are data and/or parameters associated with each OP code. The meaning of the last two bytes is dependent on the specific instruction.

Other instructions command the V.32 Engine to perform certain specific tasks. These do not pass parameters or data to the V.32 Engine. These commands have an OP code which is a full 24 bits in length.

The command set of the V.32 Engine is summarized below. The descriptions are of the form :

MNEMONIC (OPCODE) : DESCRIPTION.

For detailed information and data format specifics of each command, please refer to appendix A.

3.1. COMMAND SUMMARY

3.1.1. OPERATIONAL CONTROL COMMANDS.

FREZ (14) : Freeze adaptive processes. Freeze the adaptive processes as specified by the data in bits 0 and 1 of byte 1. Bit 0 of byte 1 controls the adaptive equalizer. Freeze the equalizer if bit 0 of byte 1 is 1. A 0 in this bit will unfreeze the equalizer. Echo canceller adaptation is controlled by bit 1 of byte 1. if bit 1 is 1, the echo canceller adaptation is frozen. The echo canceller adaptation is unfrozen by a 0 in bit 1.

HSHK (040000) : Handshake. Begin the handshake sequence. The V.32 modem engine carries out all the steps defined in the CCITT recommendation. The status reported to the control processor will indicate the success or failure of the process and its progress.

INIT (0600C0) : Initialize. Initialize the V.32 modem engine. Set all parameters to default values and wait for commands for the control processor.

JMP (06) : Force code execution at address. Force the selected processor of the V.32 Engine to begin execution at the address specified.

NOP (000000) : No Operation. No new operation is commanded. The state of the V.32 engine remains unaltered and a previously invoked multi-baud command (such as HSHK) continues.

RTRA (050000) : Retrain. Start sending the retrain sequence as defined in the CCITT recommendation.

SETGN (02) : Set Gain. This command sets a global gain factor, which will be multiplied by all transmit samples before being sent to the TS68950. Bytes 1 and 2 store the gain factor.

3.1.2. DATA COMMUNICATIONS COMMANDS.

XMIT (03) : Transmit data. Transmit data to far end modem. The data is provided in byte 1 of the command, where the least significant bit is the first bit to be transmitted. The third byte of the command must be provided, but is not used. Hence, any value may be supplied.

XMITI (01) : Transmit data and Initiate additional cycle. Transmit data and inform the DSP to accept another command at the next transmit baud. If the next command requires an answer from DSP 1, the control processor has to keep issuing this command followed by a command which does not requires an answer until the answer has been received.

3.1.3. MEMORY. MANIPULATION COMMANDS.

SPAC (13) : Store Parameter And Count. Store parameter in addressed memory and increment the pointer. This command passes data in bytes 1 and 2, least significant byte in byte 1. It is used to write an arbitrary 16-bit value into the writable memory location currently specified by the Memory Address Register. The contents of the Memory Address Register are incremented by 1 at the completion of this command.

SPAM (12) : Store parameter in Addressed Memory. This command passes data in bytes 1 and 2, least significant byte in byte 1. It is used to write an arbitrary 16-bit value into the writable momory location currently specified by the Memory Address Register.

WARP (10) : Write Address and Return Parameter. This command allows the controller to read any of the XRAM, YRAM, ERAM or CROM of any of the three modem DSPs without interrupting the processors. The address to the V.32 modem engine is provided in bytes 1 and 2 of the command (least significant byte first). DSP 1 stores the address in the Memory Address Register and returns the contents of the addressed location.

WARPX (11) : Write Address and Return Parameter Complex. The address to the V.32 modem engine is provided in bytes 1 and 2 of the command (least significant byte first). DSP 1 stores the address in the Memory Address Register. The most significant bytes of the real and imaginary parts of a complex number are returned. The 8 most significant bits of the data addressed by the Memory Address Register are returned to the control processor through byte 1. Byte 2 stores the 8 most significant bits of the data at the location immediately higher. The Memory Address Register retains the address provided. (i.e. it is not incremented.)

3.1.4. CONFIGURATION CONTROL COMMANDS

CV32 (20) : Configure modem for V.32. Configure the modem as Originate / Answer, 9600/4800, Viterbi / No-Viterbi, Analog Loopback, Digital Loopback.

CV29 (21) / CV27T (22) / CV26T (23) / CV23 (24) / CV22B (25) / CV21 (26) / CB212 (27) / CB103 (28) / CGRP2 (29) : Configure the modem to the basic operating mode specified, as well as Originate/Answer, 9600/4800, Analog Loopback, Digital Loopback. These commands are not supported by the V.32 Engine. They are listed here only for reference (i.e. for future upgrade or other product).

3.1.5. MAFE MANIPULATION COMMANDS.

CMAFE (07) : Configure MAFE. The following two bytes of this command are written directly to the MAFE chip set (TS68950/1/2). This allows the control processor to configure parameters, such as the transmit level, the receiver analog front end, and the transmit and receive clocks.

RRR1 (080000) : Read Register 1. Causes the V.32

Engine to read and immediately return the 12 bit contents of the MAFE register RR1.

RRR2 (090000) : Read Register 2. Causes the V.32 Engine to read and immediately return the 12 bit contents of the MAFE register RR2.

WTR1 (0A) : Write Register 1. Causes the V.32 Engine to write the supplied data to the MAFE register TR1.

WTR2 (0B) : Write Register 2. Causes the V.32 Engine to write the supplied data to the MAFE register TR2.

3.1.6. TONE SELECT COMMANDS.

TONE (0C) : Select Tone. Program the tone generator(s) for the desired tone(s). Examples include :

- **ANSWR** (0C1000) : Program the tone generator for the 2100 Hz answer tone.
- **DTMF** (see appendix) : Program the tone generators for the tone pair which forms the specified DTMF digit.

This command selects the tones to be transmitted, but does not enable the tone generators. To transmit the tones, the tone control commands must be issued.

3.1.7. TONE CONTROL COMMANDS

DEFT1 (0E) : Define Tone 1. Define tone 1 as specified by the parameter provided. The two data bytes following the opcode are used to program, but not enable, tone generator 1. The data for the tone is represented as a phase offset per sample. Byte 1 stores the least significant byte of the phase increment.

DEFT2 (0F) : Define Tone 2. Define tone 2 as specified by the parameter provided. The two data bytes following the opcode are used to program, but not enable, tone generator 2. The data for the tone is represented as a phase offset per sample. Byte 1 stores the least significant byte of the phase increment.

SLNT (0D0000) : Silence the tone generators. Discontinue tone transmissions by disabling the tone generators.

TGEN (0D) : Tone Generator control. Enable or disable tone generator 1 and tone generator 2 according to parameter provided. If both tone generators are enabled, the level of tone 2 is 2 dB higher than that of tone 1. However, the user can change the relative levels by modifying the amplitude level of both tone generators.

3.2. STATUS REPORTING

Whenever DSP 1 owns the mailbox, it transmits the modem status to the control processor. The status consists of three bytes of information which are stored by DSP 1 in its ROUT register for access by the control processor. These three bytes may consist of received bits and modem status or they may contain the answers to the previous command, such as WARP and RRR1/2.

Data bits have higher priority than the answer to the previous command. If both data byte and command answer are ready to be sent, the data will be sent.

Byte 0 contains status flags. Refer to appendix B for the detailed format of the status response. The four most significant bits, F00, F01, F10 and F11, indicate various conditions during the call establishment, handshaking and the data modes. They have different meanings in different modes. The flag DAV1 and DAV2 are used to indicate the type of information contained in bytes 1 and 2. Bit H is used to indicate the condition of the handshake and bit 107 informs the control processor whether the 107 flag has to be set.

DAV1 and DAV2. If both DAV1 and DAV2 are set to 1, bytes 1 and 2 contain the data in response to the previous command. Refer to the relevant commands in appendix A to get the detailed information on the interpretation of the data in bytes 1 and 2. Otherwise, they contain either the received data bits or the handshake detection status or both.

If both bits are set to 0, both byte 1 and byte 2 contain the data bits, where the bits in byte 1 are received earlier in time. The least significant bit is the first bit received. The data bits are stored in byte 1 and the modem status is stored in byte 2 when DAV2 is 1 and DAV1 is 0. When DAV1 is 1 and DAV2 is 0, the control processor should ignore the data in byte 1 and get the detection status from byte 2.

During handshake operations the V.32 Engine reports the detection status regularly. When the rate sequence is received, it will be transferred in byte 1 of the response. Each bit in byte 2 indicates the detection of a specific event in the training sequence. It has different meanings for call and answer modems. For detailed information, refer to appendix B. During the data mode, byte 2 is always provided, but is used only when there are two bytes of data to transmit. This occurs occasionally when the receiver clock is running faster than the transmitter clock.

F00-F11 bits. During the call establishment operation, the V.32 Engine reports call progress tones through the F01 and F00 flags. F00 is set to 1 when the signal energy in frequency band 1 is above the threshold level. F01 is set to 1 when the signal energy in band 2 is above the threshold level. Detection of the 2100 Hz answer tone is indicated by setting the F10 flag to a 1.

During handshake operations, all four bits are used to indicate the line condition and some detection results. F00 is set to 0 if the line quality is good and 1 if it is bad. F01 is set to 1 if any segment in the training sequence is not detected within a time out. This bit can be used to indicate a non V.32 detection if either AA is not detected in the answer modem or the AC is not detected in the call modem. Both F00 and F01 are set to 1 when an illegal mode or a GSTN cleardown is received in the rate sequence.

The detection of the rate sequence is reported in the flags F11 and F10. When the modem is operating at 9600 bps without trellis coding, these bits are both set to 0. With trellis coding at 9600 bps, F11 is set to 1 and F10 is cleared to 0. For 4800 bps, 0 and 1 will be placed in F11 and F10, respectively. When both F11 and F10 are set to 1, the modem has negotiated with the far end modem and determined that the maximum negotiated operating speed is 2400 bps.

During data mode, the perceived line quality is reported in the flags F01 and F00. The line conditions are reported as either good (code 00), poor (code 01), or terrible (code 10). The code 10 should be interpreted as a local modem retrain request. Upon receipt of this code, the controller can issue the RTRA command to begin the retrain procedure. The code 11 is used when the remote modem begins a retrain sequence. The control processor is then responsible for manipulating the appropriate data communications interface signals.

H and 107 bits. When the V.32 Engine is commanded to perform the CCITT handshake sequence, the H bit will be set to 1 for the duration of the handshake operation. At the successful completion of the handshake operation the H flag will go to 0 and the control processor is then responsible for manipulating the appropriate data communications interface signals. e.g. 106 and 109. The 107 flag is set to a 1 to indicate that the controller should assert signal 107 on the data communications interface.

3.3. COMMAND LIST

OPERATIONAL CONTROL COMMANDS

Command Mnemonic	OP Code (HEX)	Description
uFzec	170000	Unfreeze Echo Canceller
Frezq	1B0000	Freeze the Equalizer Adaptation
Frezc	160000	Freeze the Echo Canceller Adaptation
uFzeq	1C0000	Unfreeze Equalizer
hshk	040000	Handshake with Other Modem
init†	0600C0	Initialize Modem
jmp†	06	Force Code Execution
nop	000000	No Operation
rtra	050000	Retrain
setgn†	02	Set the Scaling Factor for the Transmitter

DATA COMMUNICATIONS COMMANDS

Command Mnemonic	OP Code (HEX)	Description
xmit	03	Transmit Data
xmiti†	01	Transmit Data and Initiate Additional Transfer

† Future enhancement or other product reference.

MAFE MANIPULATION COMMANDS

Command Mnemonic	OP Code (HEX)	Description
cmafe†	07	Configure MAFE Chipset
rrr1†	080000	Read MAFE Reg RR1
rrr2†	090000	Read MAFE Reg RR2
wtr1†	0A	Write MAFE Reg TR1
wtr2†	0B	Write MAFE Reg TR2

TONE SELECT COMMANDS

Command Mnemonic	OP Code (HEX)	Description
answ	0C1000	Select 2100 Hz Answer Tone
dtmf 0	0C0000	Select DTMF Digit 0
dtmf 1	0C0100	Select DTMF Digit 1
dtmf 2	0C0200	Select DTMF Digit 2
dtmf 3	0C0300	Select DTMF Digit 3
dtmf 4	0C0400	Select DTMF Digit 4
dtmf 5	0C0500	Select DTMF Digit 5
dtmf 6	0C0600	Select DTMF Digit 6
dtmf 7	0C0700	Select DTMF Digit 7
dtmf 8	0C0800	Select DTMF Digit 8
dtmf 9	0C0900	Select DTMF Digit 9
dtmf *	0C0E00	Select DTMF Digit *
dtmf #	0C0F00	Select DTMF Digit #
tone	0C	Select Tone (s)

CONFIGURATION CONTROL COMMANDS

Command Mnemonic	OP Code (HEX)	Description
cv32	20	Configure Modem for V.32
cv29†	21	† Configure Modem for V.29
cv27t†	22	† Configure Modem for V.27t
cv26t†	23	† Configure Modem for V.26t
cv23†	24	† Configure Modem for V.23
cv22B†	25	† Configure Modem for V.22 / V.22 bis
cv21†	26	† Configure Modem for V.21
cb212†	27	† Configure Modem for Bell 212
cb103†	28	† Configure Modem for Bell 103
cgrp2†	29	† Configure Modem for Group 2 Fax

MEMORY MANIPULATION COMMANDS

Command Mnemonic	OP Code (HEX)	Description
spac†	13	Write MEM and Increment MEM Pointer
spam†	12	Write MEM
warp†	10	Write MEM Pointer & Read MEM
warpx†	11	Write MEM Pointer & Read MEM & MEM + 1

† Future enhancement or other product reference.

TONE CONTROL COMMANDS

Command Mnemonic	OP Code (HEX)	Description
deft1†	0E	Define Tone 1
deft2†	0F	Define Tone 2
slnt	0D0000	Transmit no Tone
tgen 0	0D0000	Tone Generators Disabled
tgen 1†	0D0100	Tone Generator 1 Enabled
tgen 2†	0D0200	Tone Generator 2 Enabled
tgen 3	0D0300	Tone Generators 1 & 2 Enabled

4. ELECTRICAL SPECIFICATIONS

4.1. MAXIMUM RATINGS :

TS75320/1/2

Symbol	Parameter	Value	Unit
V_{CC}*	Supply Voltage	– 0.3 to 7.0	V
V_{in}*	Input Voltage	– 0.3 to 7.0	V
T_A	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

* With respect to V_{SS}.

Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

TS68950/1/2

Symbol	Parameter	Value	Unit
	Supply Voltage between V + and AGND or DGND	– 0.3 to + 7	V
	Supply Voltage between V - and AGND or DGND	– 7 to + 0.3	V
	Voltage between AGND and DGND	– 0.3 to + 0.3	V
	Digital Input Voltage	DGND – 0.3 to V_{CC}^+ + 0.3	V
	Digital Output Voltage	DGND – 0.3 to V_{CC}^+ + 0.3	V
	Digital Output Current	– 20 to + 20	mA
	Analog Input Voltage	V_{CC}^- – 0.3 to V_{CC}^+ + 0.3	V
	Analog Output Voltage	V_{CC}^- – 0.3 to V_{CC}^+ + 0.3	V
	Analog Output Current	– 10 to + 10	mA
	Power Dissipation	500	mW
T_{oper}	Operating Temperature	0 to + 70	°C
T_{stg}	Storage Temperature	– 65 to + 150	°C

4.2. DC ELECTRICAL CHARACTERISTICS DGND = AGND = 0 V

Digital Supply

V_{CC} = 5.0 V ± 5 %, V_{SS} = 0, T_A = 0 to + 70°C (Unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IL}	Input Low Voltage	– 0.3		0.8	V
V_{IH}	Input High Voltage	2.4		V_{CC}	V
I_i	Input Extal Current	– 50		+ 50	µA
I_{in}	Input Leakage Current	– 10		10	µA
V_{OH}	Output High Voltage (I_{load} = – 300 µA) except $\overline{DTACK}$	2.7			V
V_{OL}	Output Low Voltage (I_{load} = 3.2 mA)			0.5	V
P_D	Total Power Dissipation		4.5	6.6	W
C_{in}	Input Capacitance		10		pF
I_{TSI}	Three State (off state) Input Current (0.4 V - 2.4 V)	– 20		– 20	µA
T_{amb}	Operating Temperature (note 1)	0		70	°C
R_{BJA}	Thermal Resistance Junction-ambient		28		°C/W

Note 1 : Case temperature T_C must be maintained below 100 °C.

Analog Supply

Symbol	Parameter	Min.	Typ.	Max.	Unit
V^+	Positive Power Supply	4.75		5.25	V
V^-	Negative Power Supply	– 5.25		– 4.75	V
I^+	Positive Supply Current			35	mA
I^-	Negative Supply Current	– 35			

4.3. AC ELECTRICAL SPECIFICATIONS

4.3.1. CLOCK AND CONTROL PINS TIMING

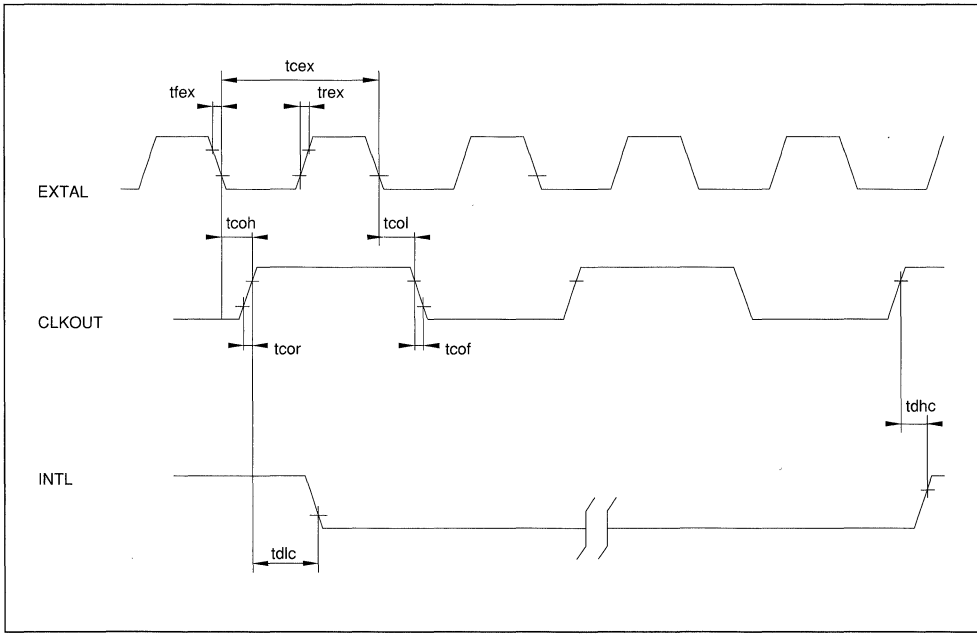
(V_{CC} = 5.0 V ± 5 %, T_A = 0° to + 70°C, see figure 5)
OUTPUT LOAD = 50 pF + DC characteristics I load

REFERENCE LEVELS : AC TESTING INPUTS ARE DRIVEN AT 2.4 V FOR A LOGIC "1" AND 0.4 V FOR A LOGIC "0".TIMING MEASUREMENTS ARE MADE AT 1.5 V FOR BOTH A LOGIC "1" AND "0".

tr, tf ≤ 5 ns for i nput signal

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{cex}	External Clock Cycle Time		40		ns
t_{fex}	External Clock Fall Time			5	ns
t_{rex}	External Clock Rise Time			5	ns
t_{coh}	EXTAL to CLKOUT High Delay		25		ns
t_{col}	EXTAL to CLKOUT Low Delay		25		ns
t_{cor}	CLKOUT Rise Time			10	ns
t_{cof}	CLKOUT Fall Time			10	ns
t_{dlc}	CLKOUT to Control Output Low (INTL)			50	ns
t_{dhc}	CLKOUT to Control High (INTL)			50	ns

Figure 5 : Clock and Control Pins Timing.



4.3.2. TS68952 : Clock Generator

CLRYSTAL OSCILLATOR INTERFACE

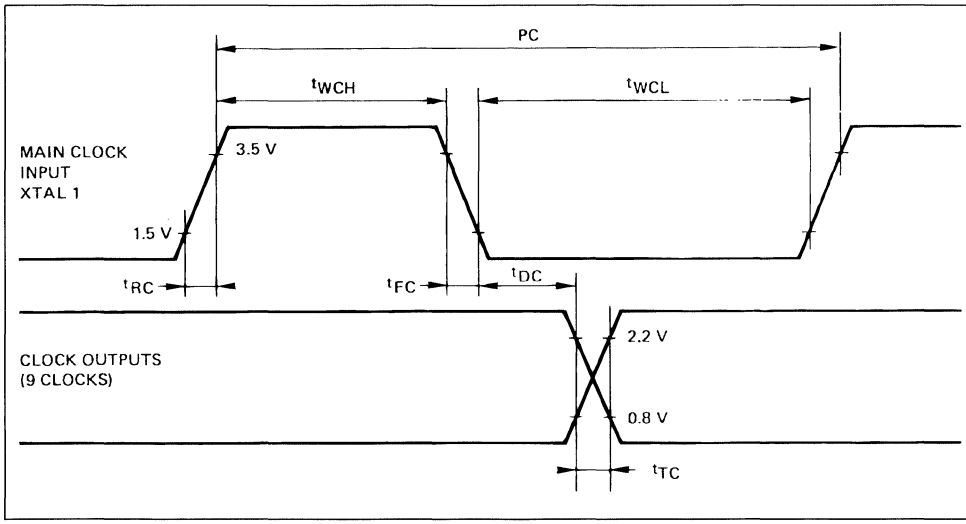
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level Voltage				1.5	V
V_{IH}	Input High Level Voltage		3.5			V
I_{IL}	Input Low Level Current	$DGND \leq V_I \leq V_{IL\ max}$	–15			µA
I_{IH}	Input High Level Current	$V_{IH\ min} \leq V_I \leq V^+$			15	µA

CLOCK WAVE FORMS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
PC	Main Clock Period	XTAL1 Input	150	173.6		ns
t_{WCL}	Main Clock Low Level Width	XTAL1 Input	50			ns
t_{WCH}	Main Clock High Level Width	XTAL1 Input	50			ns
t_{RC}	Main Clock Rise Time	XTAL1 Input			50	ns
t_{FC}	Main Clock Fall Time	XTAL1 Input			50	ns
t_{DC}	Clock Output Delay Time	All Clock Outputs CL=50 pF			500	ns
t_{TC}	Clock Output Transition Time	All Clock Outputs CL=50 pF			100	ns

Unless otherwise noted, electrical characteristics are specified over the operating range. Typical values are given for $V^+ = 5.0$ V and $t_{amb} = 25$ °C.

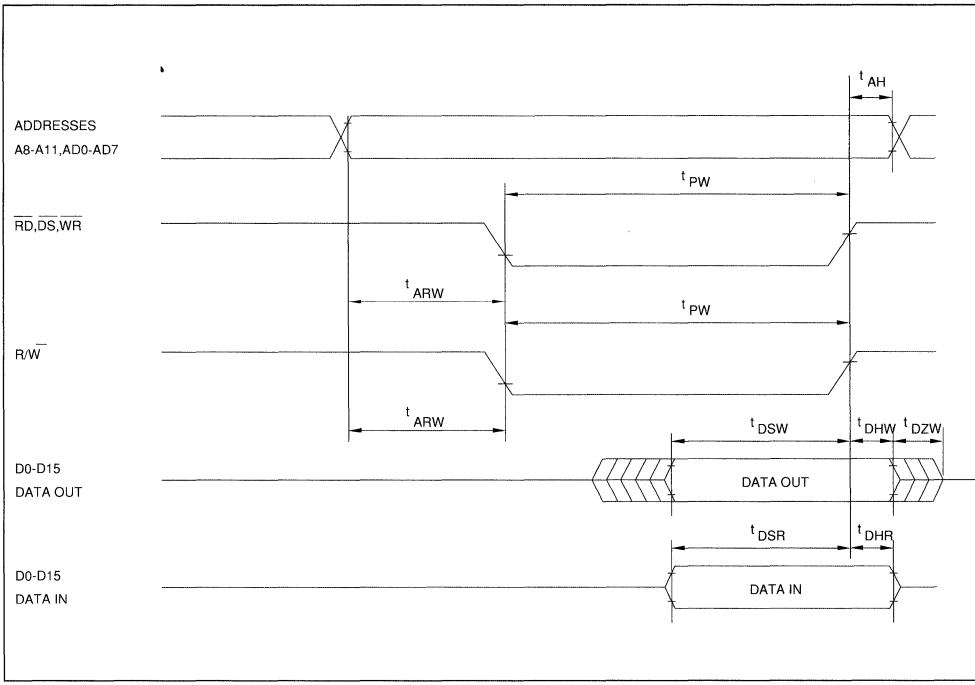
Figure 6 : Clock Generator.



4.3.3.LOCAL BUS TIMING
(V_{CC} = 5.0 V ± 5 %, T_A = 0° to + 70°C, see figure 7)

Symbol	Parameter	Min.	Max.	Unit
t_{PW}	$\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Pulse Width	1/2 tc – 15	1/2 tc	ns
t_{AH}	Address Hold Time	10		ns
t_{DSW}	Data Set-up Time, Write Cycle	25		ns
t_{DHW}	Data Hold Time, Write Cycle	10		ns
t_{DZW}	$\overline{DS}$ High to Data High Impedance, Write Cycle		40	ns
t_{DSR}	Data Set-up Time, Read Cycle	20		ns
t_{DHR}	Data Hold Time, Read Cycle	5		ns
t_{ARW}	Address Valid to $\overline{WR}$, $\overline{DS}$, $\overline{RD}$ Low	1/2 tc – 40		ns

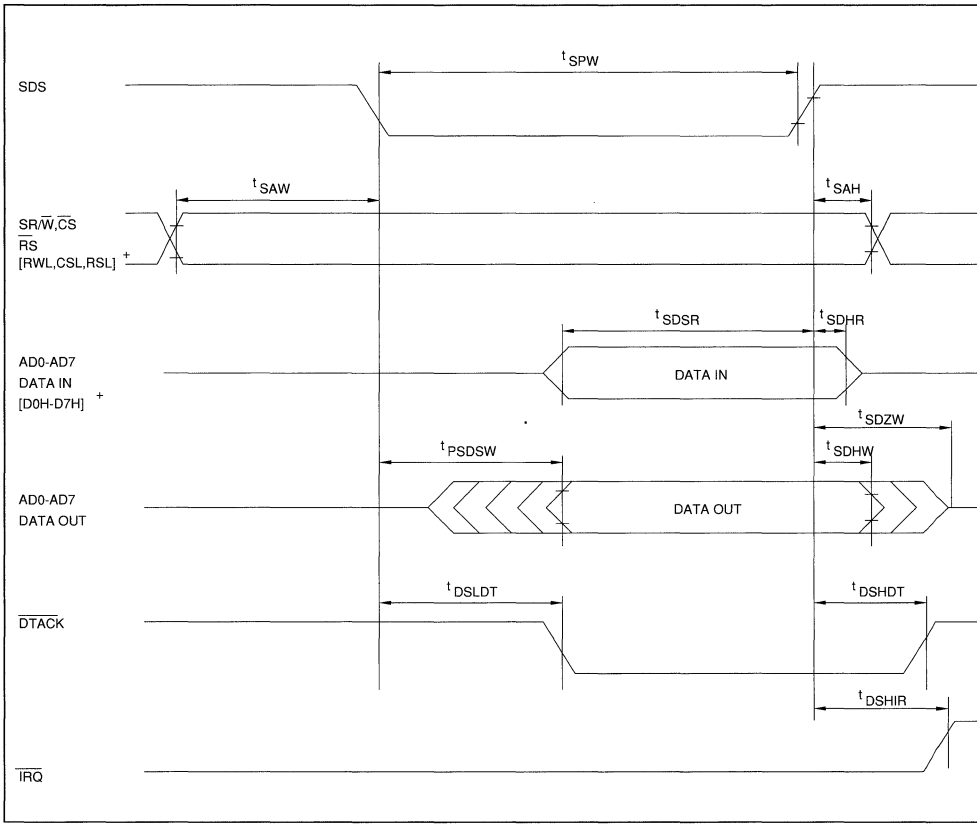
Figure 7 : Local Bus Timing Diagram.



4.3.4. SYSTEM BUS TIMING
(V_{CC} = 5.0 V ± 5 %, T_A = 0° to + 70°C, see figure 8)

Symbol	Parameter	Min.	Max.	Unit
t_{SPW}	$\overline{SDS}$ Pulse Width	60		ns
t_{SAW}	SR / $\overline{W}$, $\overline{CS}$, $\overline{RS}$ Set-up Time	20		ns
t_{SAH}	SR / $\overline{W}$, $\overline{CS}$, $\overline{RS}$ Hold After $\overline{SDS}$ High	5		ns
t_{SDSR}	Data Set-up Time, Read Cycle	20		ns
t_{SDHR}	Data Hold Time, Read Cycle	5		ns
t_{SDSW}	Data Set-up Time, Write Cycle		35	ns
t_{SDHW}	Data Hold Time, Write Cycle	10	50	ns
t_{DSHIR}	$\overline{SDS}$ High to $\overline{IRQ}$ High		800	ns
t_{SDZW}	$\overline{SDS}$ High to Data High Impedance, Write Cycle		40	ns

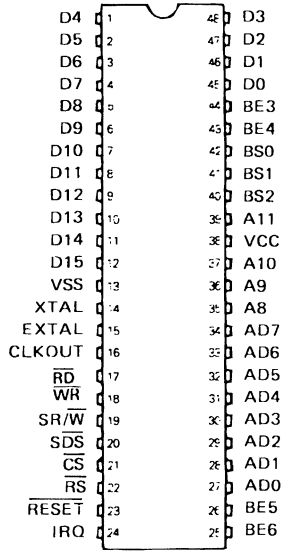
Figure 8 : System Bus Timing Diagram.



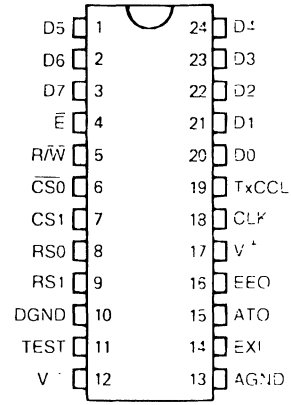
+ Note : Signal names on Host Processor Interface.

5. PIN CONNECTIONS

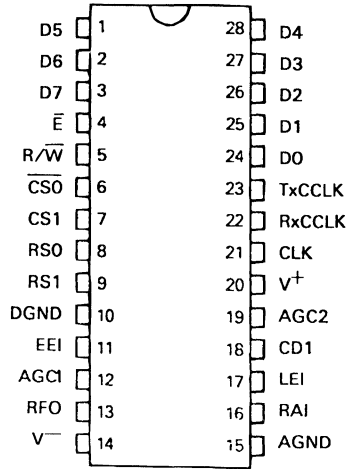
TS75320 - TS75321 - TS75322



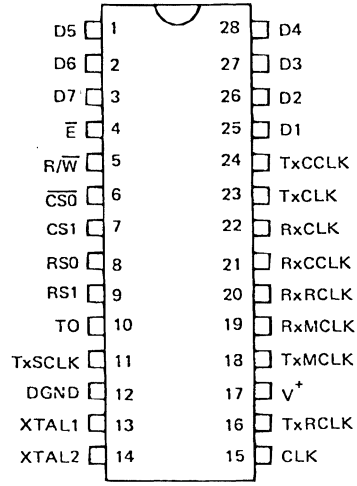
TS68950



TS68951



TS68952



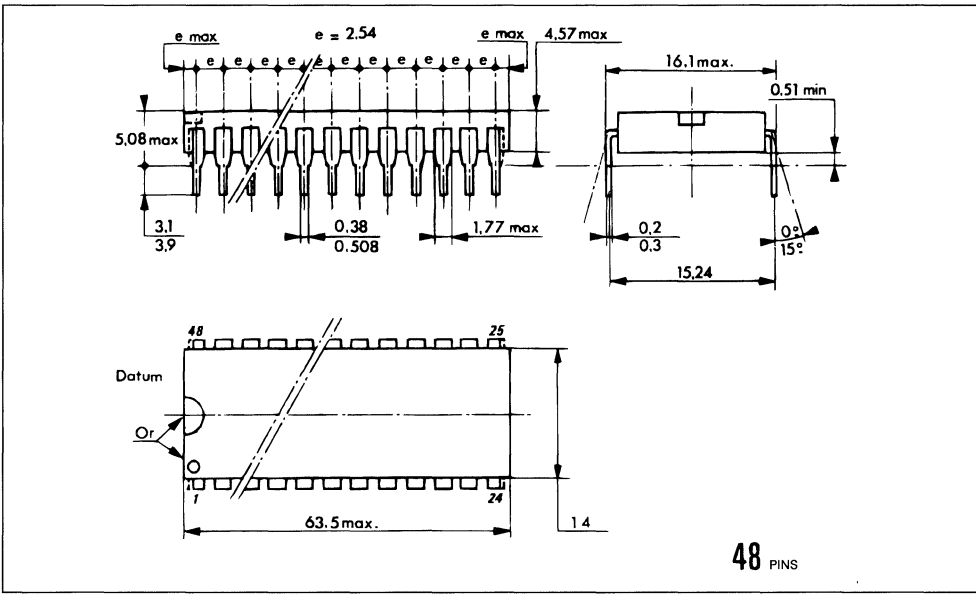
6. ORDERING INFORMATION

Part Number	Temperature Range	Package
TS75320CP	0 °C to + 70 °C	DIP48
TS75321CP	0 °C to + 70 °C	DIP48
TS75322CP	0 °C to + 70 °C	DIP48
TS68950CP	0 °C to + 70 °C	DIP24
TS68951CP	0 °C to + 70 °C	DIP28
TS68952CP	0 °C to + 70 °C	DIP28

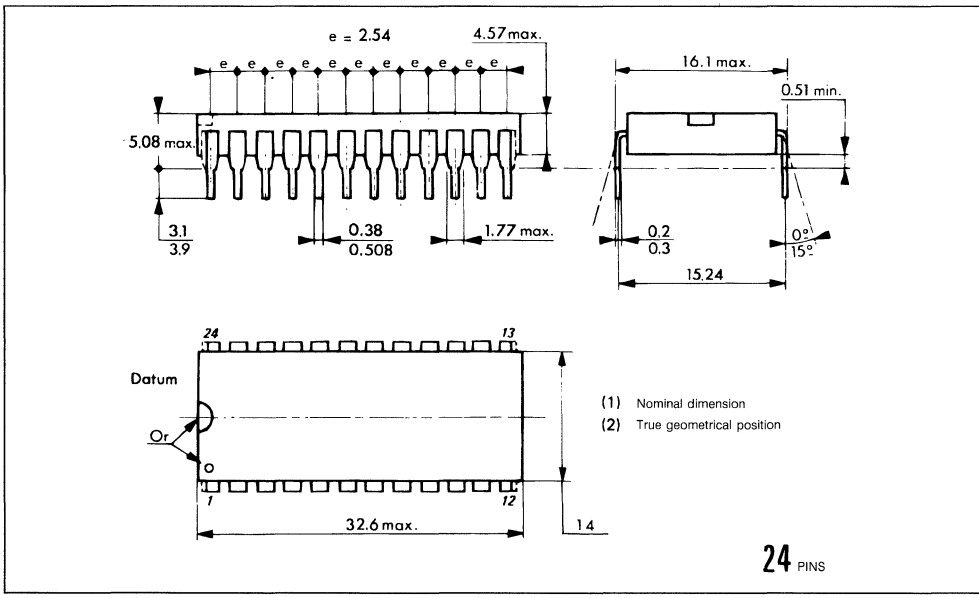
7.PACKAGE MECHANICAL DATA

TS75320/TS75321/TS75322

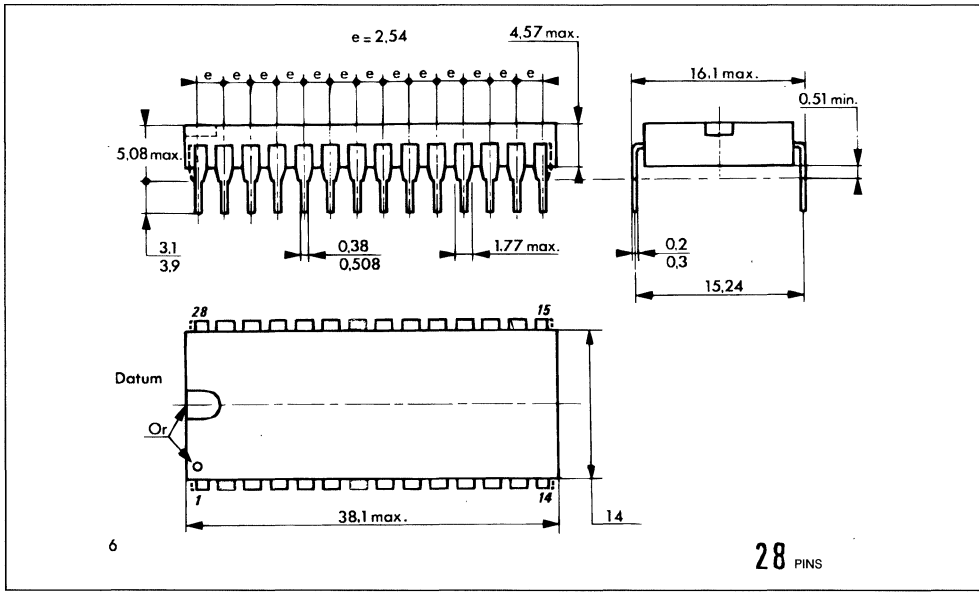
48 Pins - Plastic Dip.



TS68950
24 Pins - Plastic Dip.



TS68951/TS68952
28 Pins - Plastic Dip.



APPENDIX A
COMMAND SET DESCRIPTION

cmafe† - configure the TS68950/1/2 components of the V.32 Engine

INSTRUCTION TYPE
MAFE manipulation command

OPCODE
07

SYNOPSIS
cmafe address register code data

DESCRIPTION
cmafe is used to directly manipulate the operating parameters of the TS68950/1/2 components of the V.32 Engine. This is a low level command which allows the controller to alter such things as the transmit level, transmit timing, receive timing, and receiver parameters, etc. The command consists of a single byte OPcode followed by a byte containing the address code for the desired register and a data byte for the addressed register. The data bytes will be transferred in the order received and interpreted by the addressed device. Refer to the data sheets of the TS68950, TS68951, and TS68952 for programming specifics.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	1	1	1

BYTE 1 DEFINITION

R	R	R	0	0	0	0	0

REG CODE (Refer to TS68950 Data Sheet).

BYTE 2 DEFINITION

*	*	*	*	*	*	*	*

DATA BYTE (Refer to TS68950 Data Sheet).

APPENDIX A

cv32 - configure the V.32 Engine

INSTRUCTION TYPE

configuration control command

OPCODE

20

SYNOPSIS

cv32 speed ec orig atn al dl fc

DESCRIPTION

cv32 is used to alter the operating parameters of the V.32 Engine. The passed parameters provide a two bit speed code which selects the desired baud rate. Another parameter explicitly turns on or off the echo canceller. If the V.32 Engine is to operate in the originate mode, the orig parameter must be set. When this parameter is not set, the V.32 Engine is configured as an answer mode device. The al and dl parameters allow the user to select between the analog and digital loopback test conditions, respectively. The transmit attenuation level is selected by the atn parameter. etc.

BYTE 0 DEFINITION (OP CODE)

0	0	1	0	0	0	0	0

BYTE 1 DEFINITION

RSV	RSV	FC	EC	AL	SP1	SP0	ORIG

SPEED CODE
SP1-0
00 : 9600 bps
01 : 4800 bps
11 : 2400 bps

FLAG	BIT	DEFINITION
FC	0/1	Do not/Do force cleardown
EC†	0/1	Echo Canceller off/on
ORIG	0/1	Answer mode / Originate mode
AL†	0/1	Analog Loopback test disabled / enabled
RSV	-	Reserved

BYTE 2 DEFINITION

ATN3	ATN2	ATN1	ATN0	DL	RSV	RSV	RSV

FLAG	BIT	DEFINITION
DL†	0/1	Digital Loopback test disabled/ enabled
ATN3-0†		Transmit attenuation 0 dB to 22 dB : codes 0000 to 1011 in 2 dB steps Infinite : codes 1100 to 1111
RSV	-	Reserved

APPENDIX A

deft1† - define tone 1

INSTRUCTION TYPE
tone control command

OPCODE
0E

SYNOPSIS
deft tone descriptor

DESCRIPTION
deft1 is a command which used to program tone generator 1. The 16 bit value provided is used as the phase offset per sample for the generator. The deft1 command does not enable the tone generator. See also tgen.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	1	1	0

BYTE 1 DEFINITION

P7	P6	P5	P4	P3	P2	P1	P0

LOW BYTE OF DESCRIPTOR.

BYTE 2 DEFINITION

P15	P14	P13	P12	P11	P10	P9	P8

HI BYTE OF DESCRIPTOR.

deft2† - define tone 2

INSTRUCTION TYPE
tone control command

OPCODE
0F

SYNOPSIS
deft tone descriptor

DESCRIPTION
deft2 is a command which used to program tone generator 2. The 16 bit value provided is used as the phase offset per sample for the generator. The deft2 command does not enable the tone generator. See also tgen.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	1	1	1

BYTE 1 DEFINITION

P7	P6	P5	P4	P3	P2	P1	P0

LOW BYTE OF DESCRIPTOR.

BYTE 2 DEFINITION

P15	P14	P13	P12	P11	P10	P9	P8

HI BYTE OF DESCRIPTOR.

APPENDIX A

frzc - Freeze the echo canceller adaptation

INSTRUCTION TYPE
operational control command

OPCODE
160000

SYNOPSIS
frzec

DESCRIPTION
frzec causes the V.32 Engine to enable or disable the adaptation of the echo canceller, to the current parameter.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	0	1	1	0

BYTE 1 DEFINITION

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION

0	0	0	0	0	0	0	0

frezq - Freeze the equalizer adaptation

INSTRUCTION TYPE
operational control command

OPCODE
1B0000

SYNOPSIS
frzezq

DESCRIPTION
frzezq causes the V.32 Engine to disable the adaptation of the equalizer.

BYTE 0 (OP CODE)

0	0	0	1	0	1	1	0

BYTE 1 DEFINITION

0	0	0	0	0	0	C	0

BYTE 2 DEFINITION

0	0	0	0	0	0	0	0

APPENDIX A

hshk - begin handshake sequence

INSTRUCTION TYPE
operational control command

OPCODE
040000

SYNOPSIS
hshk

DESCRIPTION
hshk is used to command the V.32 Engine to begin the handshake sequence processing. The progress of the handshake is reported to the control processor along with the data bits. For detailed information, refer to appendix B.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	1	0	0

BYTE 1 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

APPENDIX A

init† - Initialize the V.32 Engine

INSTRUCTION TYPE
operational control command

OPCODE
0600C0

SYNOPSIS
init

DESCRIPTION
init forces the V.32 Engine to reset all parameters to their default conditions and restart operations.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	1	1	0

BYTE 1 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION (OP CODE)

1	1	0	0	0	0	0	0

jmp† - force code execution at address

INSTRUCTION TYPE
operational control command

OPCODE
06

SYNOPSIS
jmp processor code address

DESCRIPTION
jmp forces the selected processor of the V.32 Engine to begin execution at the address specified.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	1	1	0

BYTE 1 DEFINITION

A7	A6	A5	A4	A3	A2	A1	A0

ADDRESS LOW.

BYTE 2 DEFINITION (OP CODE)

P1	P0	0	0	0	A10	A9	A8

PROC CODE P1-0
00 : Master
01 : Receiver
10 : Echo Cancel
11 : All

ADDRESS HI A10-A8

APPENDIX A

nop - no operation is specified

INSTRUCTION TYPE
operational control command

OPCODE
000000

SYNOPSIS
nop

DESCRIPTION
nop is used when communications with the V.32 Engine are required but no action is desired.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 1 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

rrr1† - Read MAFE register RR1

INSTRUCTION TYPE
MAFE manipulation command
OPCODE
080000
SYNOPSIS
rrr1
DESCRIPTION
rrr1 causes the V.32 Engine to read the 12 bit contents of the MAFE chipset register RR1. The data is returned in a standard three byte format. The least significant data byte is returned in byte 1, followed by the most significant data byte. Byte 0 is the standard response format (refer to appendix B) with DAV1 and DAV2 bits set to 1. Consult the data sheet of the TS68951 for the specifics of the returned data.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	0	0	0

BYTE 1 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

APPENDIX A

rrr2† - Read MAFE register RR2

INSTRUCTION TYPE
MAFE manipulation command

OPCODE
090000

SYNOPSIS
rrr2

DESCRIPTION
rrr2 causes the V.32 Engine to read the 12 bit contents of the MAFE chipset register RR2. The data is returned in a standard three byte format. The least significant data byte is returned in byte 1, followed by the most significant data byte. Byte 0 is the standard response format (refer to appendix B) with DAV1 and DAV2 bits set to 1. Consult the data sheet of the TS68951 for the specifics of the returned data.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	0	0	1

BYTE 1 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

rtra - force a retrain of the V.32 Engine

INSTRUCTION TYPE
operational control command

OPCODE
050000

SYNOPSIS
rtra

DESCRIPTION
rtra is used to force the V.32 Engine to initiate a retrain sequence on the channel.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	1	0	1

BYTE 1 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

APPENDIX A

setgn† - set global gain factor

INSTRUCTION TYPE
operational control command

OPCODE
02

SYNOPSIS
stegn gain value

DESCRIPTION
setgn is a command which used to scale the transmit samples. The 16 bit value provided is used as the multiplicative constant to be multiplied with each transmit sample.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	0	1	0

BYTE 1 DEFINITION

G7	G6	G5	G4	G3	G2	G1	G0

LOW BYTE OF GAIN VALUE.

BYTE 2 DEFINITION

G15	G14	G13	G12	G11	G10	G9	G8

HI BYTE OF GAIN VALUE.

slnt - Disable tone generators

INSTRUCTION TYPE
tone command

OPCODE
0D0000

SYNOPSIS
slnt

DESCRIPTION
slnt causes the V.32 Engine to disable the tone generators, thus stopping the tone output (i.e. send silence).

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	1	0	1

BYTE 1 DEFINITION

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

APPENDIX A

spac† - Store Parameter And Count

INSTRUCTION TYPE
memory manipulation command

OPCODE
13

SYNOPSIS
spac lo-byte hi-byte

DESCRIPTION
spac is a command which used to write an arbitrary 16 bit value into the writable memory location currently specified by the Memory Address Register. The content of the Memory Address Register is incremented by 1 at the completion of command execution. See also WARP.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	0	0	1	1

BYTE 1 DEFINITION

D7	D6	D5	D4	D3	D2	D1	D0

LOW BYTE OF DATA.

BYTE 2 DEFINITION

D15	D14	D13	D12	D11	D10	D9	D8

HI BYTE OF DATA.

spam† - Store Parameter in Addressed Memory

INSTRUCTION TYPE
memory manipulation command

OPCODE
12

SYNOPSIS
spam lo-byte hi-byte

DESCRIPTION
spam is a command which used to write an arbitrary 16 bit value into the writable memory location currently specified by the Memory Address Register. See also WARP.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	0	0	1	0

BYTE 1 DEFINITION

D7	D6	D5	D4	D3	D2	D1	D0

LOW BYTE OF DATA.

BYTE 2 DEFINITION

D15	D14	D13	D12	D11	D10	D9	D8

HI BYTE OF DATA.

APPENDIX A

tgen - Enable and disable tone generators

INSTRUCTION TYPE
tone control command

OPCODE
0D

SYNOPSIS
tgen tg code

DESCRIPTION
tgen causes the V.32 Engine to enable or disable tone generator 1 and tone generator 2, according to the parameter provided. Either tone generator 1 or tone generator 2 can be scaled by the parameter provided in byte 2. If neither is scaled and both tone generators are enabled, tone 2 has a level 2 dB higher than tone 1. The user cannot scale both tone generators. If both generators are selected to be scaled, tone generator 1 has higher priority.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	1	0	1

BYTE 1 DEFINITION (TONE CODE)

0	0	0	0	TGN2	TGN1	0	0

TG CODE TGC2-1	TONE GEN 1	TONE GEN 2
00	disabled	disabled
01†	enabled	disabled
10†	disabled	enabled
11	enabled	enabled

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

tone - Select and transmit tone (s)

INSTRUCTION TYPE
tone select and command

OPCODE
0C

SYNOPSIS
tone tone code

DESCRIPTION
tone causes the V.32 Engine to program the tone generators for the specified tone or tones. The tones are defined by the tone code parameter passed in the second byte of the command. See also tonetab for the predefined single and double tones, and the commands deft and tgen for user definable tones and tone generator control.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	1	0	0

BYTE 1 DEFINITION (TONE CODE)

T7	T6	T5	T4	T3	T2	T1	T0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

Tone Code	Tone Parameters
0	DTMF 0 (941 & 1336 Hz)
1	DTMF 1 (697 & 1209 Hz)
2	DTMF 2 (697 & 1336 Hz)
3	DTMF 3 (697 & 1477 Hz)
4	DTMF 4 (770 & 1209 Hz)
5	DTMF 5 (770 & 1336 Hz)
6	DTMF 6 (770 & 1477 Hz)
7	DTMF 7 (852 & 1209 Hz)
8	DTMF 8 (852 & 1336 Hz)
9	DTMF 9 (852 & 1477 Hz)
A	(697 & 1633 Hz)
B	(770 & 1633 Hz)
C	(852 & 1633 Hz)
D	(941 & 1633 Hz)
E	DTMF * (941 & 1209 Hz)
F	DTMF # (941 & 1477 Hz)
10	Answer tone (2100 Hz)

APPENDIX A

ufzec - Unfreeze the echo canceller adaptation

INSTRUCTION TYPE
operational control command

OPCODE
170000

SYPNOSIS
ufzec

DESCRIPTION
Ufzec causes the V.32 Engine to enable the adaptation of the echo canceller.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	0	1	1	1

BYTE 1 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

ufzeq - Unfreeze the equalizer adaptation

INSTRUCTION TYPE
operational control command

OPCODE
1C0000

SYPNOSIS
ufzeq

DESCRIPTION
Ufzeq causes the V.32 Engine to enable the adaptation of the equalizer.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	1	1	0	0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 3 DEFINITION

0	0	0	0	0	0	0	0

APPENDIX A

warp† - Write Address & Return Parameter

INSTRUCTION TYPE
memory manipulation command

OPCODE
10

SYNOPSIS
warp address

DESCRIPTION
warp is a command which is used to write the Memory Address Register of the V.32 Engine. The V.32 Engine responds with the contents of the addressed location. The data is returned in a standard three byte transfer. The least significant data byte is returned in the byte 1, followed by the most significant data byte. Byte 0 is the standard response format (refer to appendix B) with DAV1 and DAV2 bits set to 1.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	0	0	0	0

BYTE 1 DEFINITION

A7	A6	A5	A4	A3	A2	A1	A0

LOW BYTE OF DATA.

BYTE 2 DEFINITION

P1	P0	M1	M0	A11	A10	A9	A8

PROC CODE P1-0	MEM CODE M1-0	ADDRESS HI A11-A8
00 : Master	00 : XRAM	
10 : Receiver	01 : YRAM	
01 : Echo Canceller	10 : EMEM	
	11 : CROM	

warpx† - Write Address & Return Parameter Complex

INSTRUCTION TYPE
memory manipulation command

OPCODE
11

SYNOPSIS
warpx address

DESCRIPTION
warpx is a command which is used to write the Memory Address Register of the V.32 Engine. The V.32 Engine responds with the contents of the most significant bytes of the addressed location and the addressed location + 1. The data is returned in a standard three byte transfer. Byte 0 is the standard response format (refer to appendix B) with DAV1 and DAV2 bits set to 1. Byte 1 is used to return the 8 most significant bits contained in the addressed location. The 8 most significant bits of the addressed location + 1 are returned in byte 2.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	0	0	0	1

BYTE 1 DEFINITION

A7	A6	A5	A4	A3	A2	A1	A0

LOW BYTE OF DATA.

BYTE 2 DEFINITION

P1	P0	M1	M0	A11	A10	A9	A8

APPENDIX A

wtr1† - Write MAFE register TR1

INSTRUCTION TYPE
MAFE manipulation command

OPCODE
0A

SYNOPSIS
wtr1

DESCRIPTION
wtr1 causes the V.32 Engine to take the two supplied data bytes and write them in sequence to the MAFE chipset register TR1.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	0	1	0

BYTE 1 DEFINITION (DATA)

D3	D2	D1	D0	0	0	0	0

BYTE 2 DEFINITION (DATA)

D11	D10	D9	D8	D7	D6	D5	D4

wtr2† - Write MAFE register TR2

INSTRUCTION TYPE
MAFE manipulation command

OPCODE
0B

SYNOPSIS
wtr2

DESCRIPTION
wtr2 causes the V.32 Engine to take the two supplied data bytes and write them in sequence to the MAFE chipset register TR2.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	0	1	1

BYTE 1 DEFINITION (DATA)

D3	D2	D1	D0	0	0	0	0

BYTE 2 DEFINITION (DATA)

D11	D10	D9	D8	D7	D6	D5	D4

APPENDIX A

xmit - transmit data to other modem

INSTRUCTION TYPE
data communications command

OPCODE
01

SYNOPSIS
xmit data

DESCRIPTION
xmit is used to command the V.32 Engine to send data. The OP code for the xmit command is a single byte. The data bits to be transmitted are stored in the second byte, where D0 is the first bit to be transmitted.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	0	0	1

BYTE 1 DEFINITION

D7	D6	D5	D4	D3	D2	D1	D0

D0-D7 DATA BITS

BYTE 2 DEFINITION

0	0	0	0	0	0	0	0

xmiti† - transmit data to other modem and initiate additional cycle

INSTRUCTION TYPE
data communications command

OPCODE
03

SYNOPSIS
xmit data

DESCRIPTION
xmit is used to command the V.32 Engine to send data. The OP code for the xmit command is a single byte. The data bits to be transmitted are stored in the second byte, where D0 is the first bit to be transmitted.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	0	1	1

BYTE 1 DEFINITION

D7	D6	D5	D4	D3	D2	D1	D0

D0-D7 DATA BITS

BYTE 2 DEFINITION

0	0	0	0	0	0	0	0

APPENDIX B
STATUS REPORTING DESCRIPTION

BYTE 0 DEFINITION

F11	F10	F01	F00	DAV2	DAV1	H	107

FLAG CODE F01-00	CALL ESTAB	HANDSHAKE OPERATIONS	DATA XFER OPERATIONS
00	no tones	line quality is good	line quality is good
01	Band 1 detected	line terrible (local retrain req.)	line quality is poor
10	Band 2 detected	time out	line terrible (local retrain req.)
11	Both bands detected	line cleardown	remote retrain sequence detected
F11-10			
00	reserved	9600 bps no trellis	reserved
01	Answer tone	4800 bps	reserved
10	AC detected	9600 bps trellis	reserved
11	reserved	2400 bps	reserved

DAV1	DAV2	DEFINITION
0	0	Data is in byte 1 and 2.
0	1	Data is in byte 1 and status word in byte 2.
1	0	No data bits and status word is in byte 2.
1	1	Answer to the last command is in bytes 1 and 2.

FLAG	BIT	DEFINITION
H	0/1	Handshake is not/is in progress
107	0/1	Set circuit 107 off/on

BYTE 1 DEFINITION

RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

BYTE 1 DEFINITION†

ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0

Bit	Call Modem	Answer Modem
ST7	AC detected	AA detected
ST6	AC-CA detected	AA-CC detected
ST5	CA-AC detected	Silence detected
ST4	S detected	S detected
ST3	S-S/detected	S-S / detected
ST2	R1 detected	R2 detected
ST1	R3 detected	N/A
ST0	E detected	E detected

APPENDIX C

This appendix describes the interconnection between the different chips.

SYSTEM INTERFACE

Signal Name	Chip/Pin	Description
DOH..D7H	TS75321/27..34	System Data Bus : connect to host processor.
CSL	TS75321/21	Chip Select : connect to host processor.
RSL	TS75321/22	Register Select : connect to host processor.
DSL	TS75321/20	Data Strobe : connect to host.
RWL	TS75321/19	Read/Write : connect to host.
INTL	TS75321/24	Interrupt Request : connect to host processor
RSTL1 RSTL2 RSTL0	TS75321/23 TS75322/23 TS75320/23	Reset : connect to host processor. Reset Reset

CLOCK SIGNAL

Signal Name	Chip/Pin	Description
TxRCLK	TS68952/16 TS75321/26	Transmit baud clock.
TxCCLK	TS68952/24 TS75321/44 TS68950/19 TS68951/23	Transmit conversion clock.
RxRCLK	TS68952/20 TS75321/43 TS75322/44	Receive baud clock.
RxCCLK	TS68952/21 TS75321/25 TS75322/43 TS68951/22	Receive conversion clock.
TxSCLK	TS68952/11	If not used must be grounded.
XTL1	TS68952/13	External crystal input : must be connected via a 5.76 MHz crystal to XTL2.
XTL2	TS68952/14	External Crystal Input
CLK	TS68952/15 TS68950/18 TS68951/21	Main analog clock : this output, in accordance with the XTL1/2 crystal, must be 1.4 MHz (+ - 7Hz).
25 MHz	TS75320/15 TS75321/15 TS75322/15	Main digital clock : connect to a 25 MHz oscillator.
TxCCLK RxCCLK	TS68952/23 TS68952/22	Transmit bit clock. Receive bit clock.

APPENDIX C

ANALOG SIGNALS

Signal Name	Chip/pin	Description
ATO	TS68950/15	Analog Transmit Output : connect to DAA.
EEO^T	TS68950/16 TS68951/11	Analog echo cancelling estimation.
LEI	TS68951/17	Local Echo Input : connect to DAA.
RAI	TS68951/16	Receive Analog Input : connect to DAA.
RFO	TS68951/13	This pin must be connected throught a 1 µF nonpolarised capacitor to AGC1 input.
AGC1	TS68951/12	
AGC2	TS68951/19	Connect to the analog loop back signal (see schematic).
CD1	TS68951/18	Connect to the analog ground through a 1 µF nonpolarised capacitor

Caution : T The connection between EEO (TS68950/16) and EEI (TS68951/11) must be as close as possible to avoid parasitics on echo estimate signal.

INTER DSP AND EXTERNAL MEMORY CONNECTION

Signal Name	Chip/Pin	Description
0D0..0D15	TS75320/45..48,1..12 RAM0/IO0..IO15	Data Bus
1D8..1D15	TS75321/5..12 TS75320/27..34 RAM0/AD0..AD7 TS68950/20..24, 1..3	Data and Address Buses
1D0..1D7	TS75321/45..48, 1..4 TS75322/27..34 RAM2/AD0..AD7	Data and Address Buses
2D9..2D15	TS75322/6..12 TS68951/25..28, 1..3 TS68952/25..28, 1..3 RAM2/IO9..IO15	Data Bus
2D8	TS75322/5 TS68951/24 RAM2/IO8	Data Pin
2D0..2D7	TS75322/45..48, 1..4 RAM2/IO0..IO7	Data Bus
1A11	TS75321/39 TS75320/21 TS75322/21 TS68950/7	Address Line
1A10	TS75321/37 TS68950/6	Adress Line
1A9	TS75321/36 TS68950/9 TS75320/22	Address Line

Note : RAM0 Refer to DSP0 4Kx16 External memory.
RAM2 Refer to DSP2 2Kx16 External memory.

Where : IO is bidirectional data bus
AD is address line
WEL is Write Enable (active low)
CEL is Chip Select (active low)

APPENDIX C

INTER DSP AND EXTERNAL MEMORY CONNECTION (continued)

Signal Name	Chip/Pin	Description
1A8	TS75321/35 TS68950/8 TS75322/22	Address Line
1RWL	TS75321/18 TS75320/19 TS75322/19 TS68950/5	Control Line
1DSL	TS75321/17 TS75320/20 TS75322/20 TS68950/4	Control Line
0A8..0A11	TS75320/35..37,39 RAM0/AD8..AD11	Address Line
0DSL	TS75320/17 RAM0/CEL	Control Line
0RWL	TS75320/18 RAM0/WEL	Control Line
2A8..2A11	TS75322/35..37,39 TS68951/8,9,6,7 TS68952/8,9,6,7 RAM2/A8..A10,CEL	Address Line
2DSL	TS75322/17 TS68951/4 TS68952/4 RAM2/OEL	Control Line
2RWL	TS75322/18 TS68951/5 TS68952/5 RAM2/WEL	Control Line
0IRQL	TS75320/24 TS75321/42	Synchro Line
2IRQL	TS75322/24 TS75321/41	Synchro Line

Note : RAM0 Refer to DSP0 4Kx16 External memory.
RAM2 Refer to DSP2 2Kx16 External memory.

Where : IO is bidirectional data bus
AD is address line
WEL is Write Enable (active low)
CEL is Chip Select (active low)
OEL is Output Enable (active low)

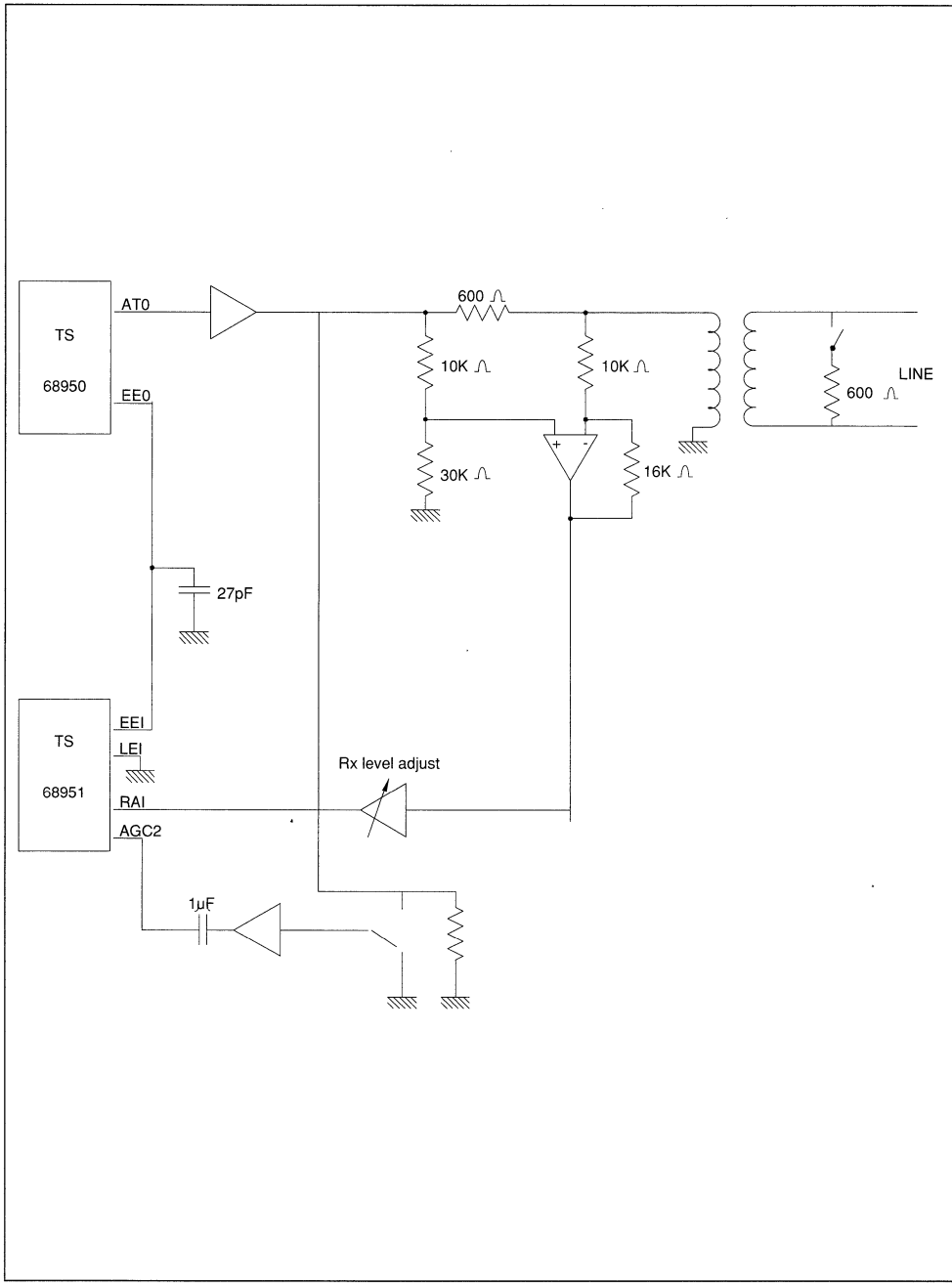
APPENDIX C

POWER SUPPLY AND MISCELLANEOUS

Signal Name	Chip/Pin	Description
+ 5VA	TS68951/20 TS68950/17	Positive Analog Power Supply
- 5VA	TS68951/14 TS68950/12	Negative Analog Power Supply
AGND	TS68950/13 TS68951/15	Analog Ground
VCC	TS75320/38 TS75321/38 TS75322/38 TS68952/17	Main Digital Power Supply
DGND	TS75320/13 TS75321/13 TS75322/13 TS68950/10 TS68951/10 TS68952/12	Digital Ground Power Supply
xtal	TS75320/14 TS75321/14 TS75322/14	Not Connected (must be left open)
Clkout	TS75320/16 TS75321/16 TS75322/16	Not Connected (25 MHz/4)
TO	TS68952/10	Not Connected (must be left open)
AGND	TS68950/14	Auxiliary Input
DGND	TS75321/40 TS75320/40..44 TS75320/25..26 TS75322/40..42 TS75322/25..26 TS68950/11	Not Used

APPENDIX C

Figure 9 : Analog Path.



APPENDIX D
REFERENCES

[1] CCITT recommendation V.32.
[2] CCITT recommendation V.54.
[3] Data sheet of the TS75320 , V.32 modem echo canceller, SGS - THOMSON Microelectronics.
[4] Data sheet of the TS68930, TS68931 programmable signal processor, SGS - THOMSON Microelectronics.
[5] Data sheet of the TS68950 transmitter interface chip, SGS - THOMSON Microelectronics.
[6] Data sheet of the TS68951 receiver interface chip, SGS - THOMSON Microelectronics.
[7] Data sheet of the TS68952 clock generation chip, SGS - THOMSON Microelectronics.
[8] Application guide : Using the TS75320 Echo canceller in V.32 modems, SGS - THOMSON Microelectronics.

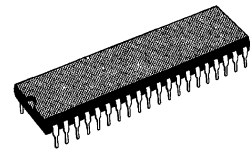
SGS-THOMSON MICROELECTRONICS

TS7542

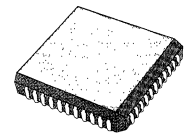
MULTI MODE MODEM ANALOG FRONT-END

ADVANCE DATA

- 12 BIT A/D AND D/A CONVERTERS WITH PROGRAMMABLE SAMPLING FREQUENCY : 7.2, 8.0, OR 9.6 kHz
- 6 TH ORDER SWITCHED CAPACITOR TRANSMIT FILTER
- TRANSMIT ATTENUATOR PROGRAMMABLE FROM 0 dB TO 22 dB WITH 2 dB STEP
- DUPLEXER OUTPUT AVAILABLE WITH PROGRAMMABLE ATTENUATION
- 15 TH ORDER SWITCHED CAPACITOR Rx FILTER (PROGRAMMABLE)
- TWO PROGRAMMABLE GAIN Rx AMPLIFIERS : FROM 0 dB TO 9 dB WITH 3 dB STEP BEFORE Rx FILTER AND FROM 0 dB TO 46.5 dB WITH 1.5 dB STEP AFTER Rx FILTER
- PROGRAMMABLE CARRIER LEVEL DETECTOR
- ON CHIP ANTI-ALIASING CELLS (TRANSMIT AND RECEIVE)
- TWO INDEPENDANT TRANSMIT AND RECEIVE DIGITAL PHASE LOCKED LOOPS (DPLLS)
- TERMINAL CLOCK INPUT FOR TRANSMIT SYNCHRONIZATION
- THREE AVAILABLE OUTPUT CLOCKS : BIT, BAUD AND CONVERSION CLOCKS
- DSP INTERFACE THROUGH 8 BIT STANDARD BUS FOR BOTH SIGNAL SAMPLES AND CONTROL REGISTER ACCESS
- AUTOMATIC RESET ON POWER-ON
- ± 5 V POWER SUPPLY
- 250 mW TYPICAL POWER CONSUMPTION



P
DIP40
(Plastic Package)



FN
PLCC44
(Plastic Package)

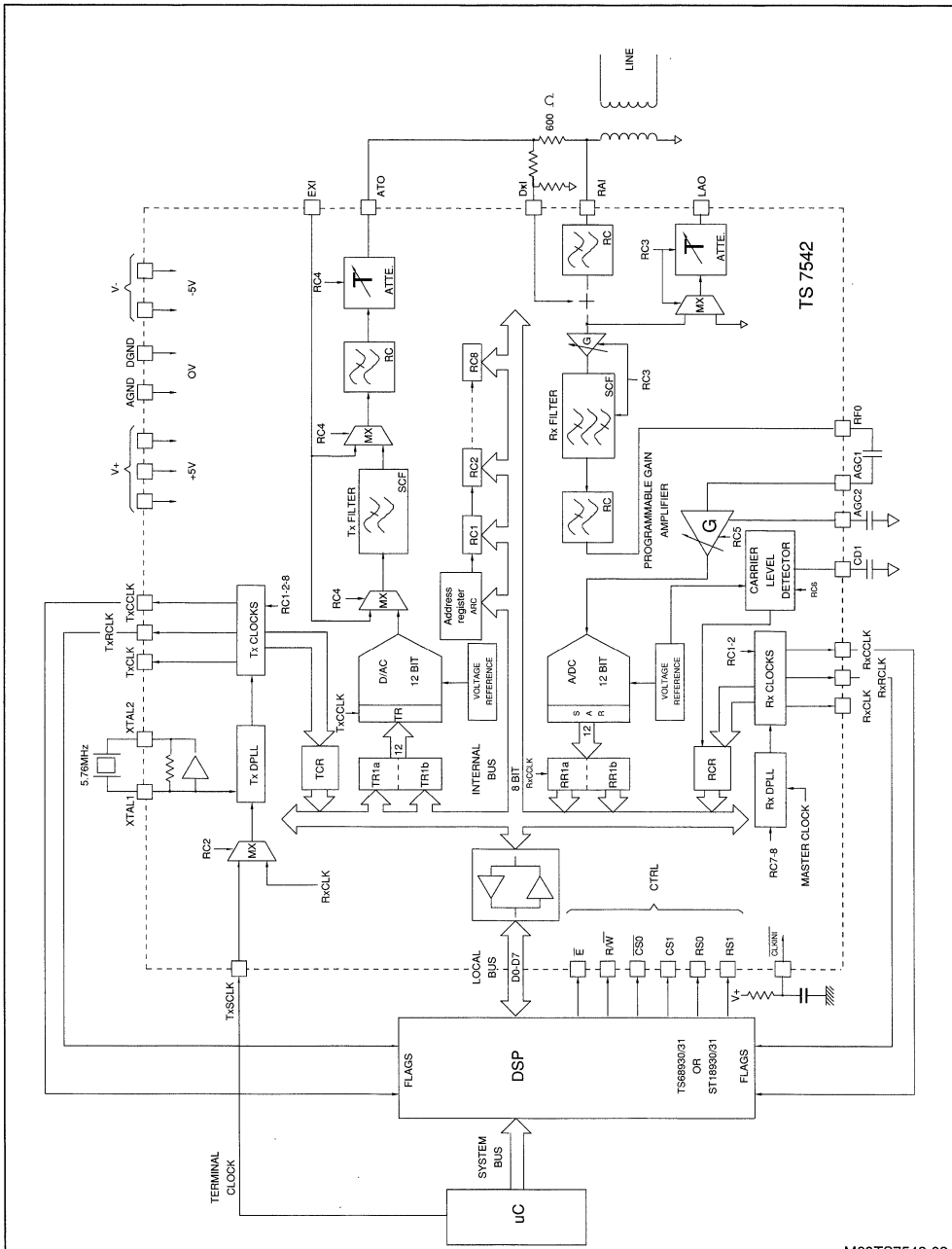
DESCRIPTION

The TS7542 is a single-chip analog front-end designed to implement high-performance voice-grade MODEMS. Associated with a Digital Signal Processor such as TS68930/31 or ST18930/31, it provides a cost-effective and powerful solution for implementation of multi-mode modems including CCITT V.21, V.22, V.22bis, V.23, V.26, V.27, V.29, V.33 and BELL 103, 202 and 212 A standards.

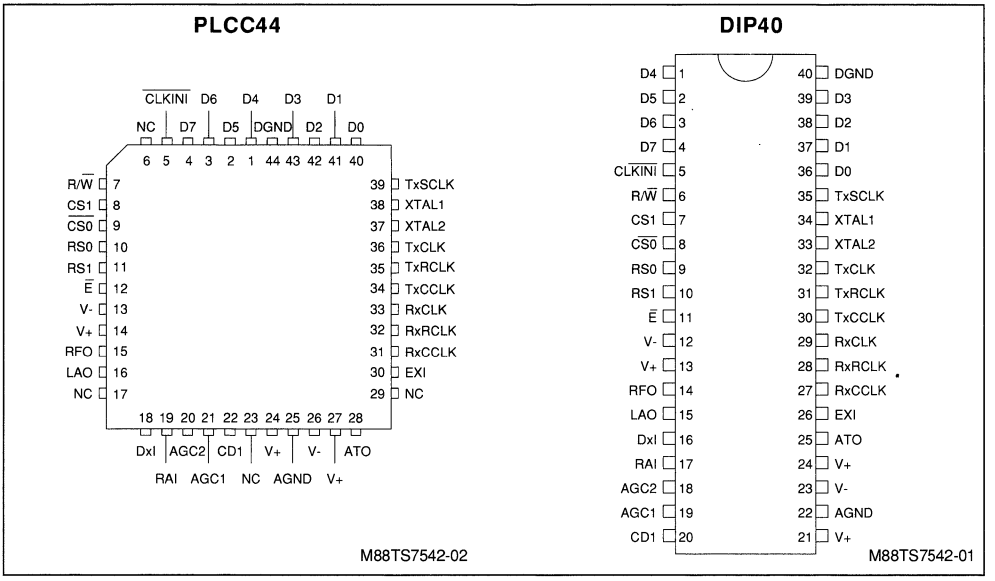
ORDERING INFORMATION

Part Number	Temperature Range	Package
TS7542CP	0 to 70 °C	DIP 40
TS7542CFN	0 to 70 °C	PLCC 44

BLOCK DIAGRAM



PIN CONNECTIONS



PIN DESCRIPTION

N°	Name	Description
1-4	D4-D7	Bidirectional Data Bus
5	$\overline{\text{CLKINI}}$	Clock Initialization Input. Must be tied to V^+ during normal operation.
6	R/$\overline{\text{W}}$	Read/Write Selection Input. This input indicates whether the current bus cycle is a read (high) or write (low) cycle.
7-8	CS1-$\overline{\text{CS0}}$	Chip Select Inputs. The chip is selected when $\overline{\text{CS0}}$ = 0 and CS1 = 1.
9-10	RS0-RS1	Register Select Inputs. Select the register involved in a read or write operation.
11	$\overline{\text{E}}$	Enable Input. Enables selection inputs. Active on a low level for read operation. Active on a positive-going edge for write operation.
12	V^-	Negative Supply Voltage. $V^- = -5\ V \pm 5\ \%$
13	V^+	Positive Supply Voltage. $V^+ = +5\ V \pm 5\ \%$
14	RFO	Receive Filter Analog Output. Designed to be connected to AGC1 input through a 1µF non polarized capacitor.
15	LAO	Line Attenuator Output. Duplexer analog output useful for line monitoring during call progress.
16	DxI	Duplexer Input. Signal on that analog input will be subtracted from the receive anti-aliasing filter output to implement duplexer function.
17	RAI	Receive Analog Input. Analog input tied to the transmission line.
18	AGC2	This pin must be connected to the analog ground through a 1µF non polarized capacitor, in order to cancel the offset voltage of the AGC amplifier.
19	AGC1	Analog input of the AGC amplifier and of the carrier level detector.

PIN DESCRIPTION (continued)

20	CD1	This pin must be connected to the analog ground through a 1µF non polarized capacitor, in order to remove the offset voltage of the carrier level detector amplifier.
21	V^+	Positive Power Supply Voltage
22	AGND	Analog Ground. All analog signals are referenced to this pin.
23	V^-	Negative Supply Voltage
24	V^+	Positive Supply Voltage
25	ATO	Analog Transmit Output. Capable of driving 1200 Ω load with 5 V peak to peak amplitude.
26	EXI	External Transmit Input. Can be programmed to be connected to the transmit filter or to the transmit attenuator input.
27	RxCCLK	Receive Conversion Clock Output
28	RxRCLK	Receive Baud Rate Clock Output
29	RxCLK	Receive Bit Rate Clock Output
30	TxCCLK	Transmit Conversion Clock Output
31	TxRCLK	Transmit Baud Rate Clock Output
32	TxCLK	Transmit Bit Rate Clock Output
33	XTAL2	Crystal Oscillator Output. Nominal Frequency = 5.76 MHz.
34	XTAL1	Crystal Oscillator or External Master Clock Input
35	TxSCLK	Transmit Synchronization Clock Input. Can be connected to an external terminal clock to phase lock the internal transmit clocks. When this pin is tied to a permanent logical level the transmit DPLL free-runs or can be phase locked on the receive clock system.
36-39	D0-D3	Bidirectional Data Bus
40	DGND	Digital Ground. All digital signals are referenced to this pin.

FUNCTIONAL DESCRIPTION

The TS7542 is generally used in conjunction with a DSP to realize the "data-pump" function of a high-speed modem. The circuit communicates with the DSP via an 8-bit bidirectional bus and mainly includes the following functions :

- the transmit analog channel with the D/A Converter, the transmit filter and the transmit attenuator.
- the receive analog channel with the local echo subtractor, the receive filter, the AGC amplifier, the A/D converter and the carrier level detector.
- the two independent transmit and receive clock generators using Digital Phase Locked Loops (DPLL).
- the 15 registers used to store the 12-bit transmit and receive digital samples, digital information for the DSP like the clock and the carrier level detector status, and the data needed to control the programmable functions or to synchronize the DPLLS.

TRANSMIT CHANNEL

The transmit channel converts the digital transmit signal coming from the DSP into the analog signal to be transmitted on the phone line. It includes a 12 bit digital to analog converter (DAC) operating at 7200, 8000 or 9600 samples per second according to the supported standard and the signal processing compromises made in the DSP. The maximum analog output signal amplitude is 5 V peak to peak , defined by the internal ± 2.5 V voltage reference. The DAC is monotonic and provides a guaranteed integral linearity better than 9 bit.

The transmit filter is a 6 th order low-pass switched capacitor filter (SCF) sampled at 288 kHz, whose cut-off frequency is 3.2 kHz. As the Sin x/x correction depends on the DAC sampling frequency, it has not been included in the tansmit filter and must be performed by the DSP. The transmit filter is followed by a second order, continuous time low-pass filter

that removes the residual high frequency parasitic signals.

The transmit attenuator allows the transmit signal gain to be programmed from 0 dB to – 22 dB with 2 dB steps. Infinite attenuation is also programmable. The output amplifier can directly drive a 1200 Ω load. For special applications, the EXI input can be programmed to give access to the input of the transmit filter or to the input of the attenuator.

RECEIVE CHANNEL

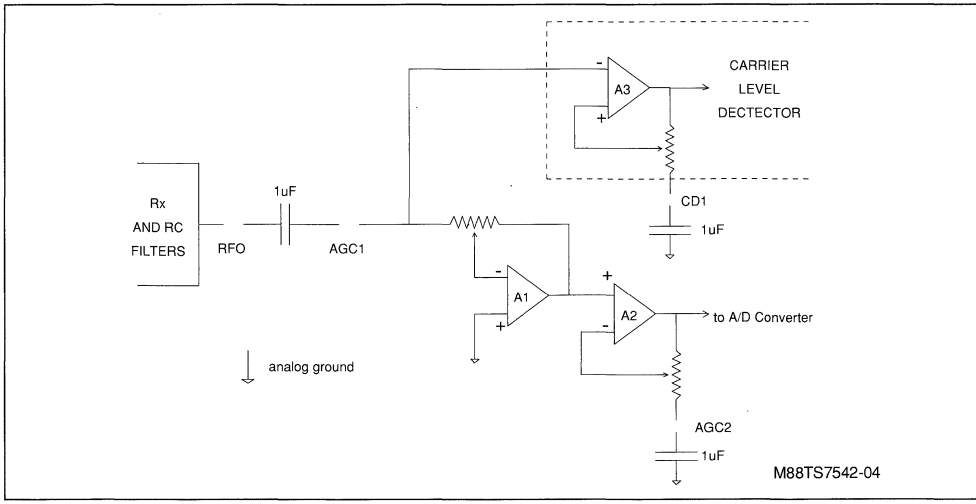
The receive channel begins with a second order continuous time anti- aliasing filter followed by a subtractor used to implement the two-wire to four-wire conversion with few external components. The receive signal is then directed to the receive filter input and also, after programmable attenuation, to the LAO output for line monitoring purpose during call progress. Attenuation can be 0 dB, 6 dB, 12 dB or infinite.The receive switched capacitor bandpass filter is composed of three programmable sections : A 5 th order low-pass section, a 4 th order optional 1800 Hz notch section and a 6 th order high-pass section. It also includes an input pre-filtering gain programmable from 0 dB to 9 dB with 3 dB steps. This feature is useful to optimize the dynamic range of the signal by setting the maximum receive level value close to 5 V peak to peak.The transfer function of the receive low-pass and high-pass filter sections can be translated by changing their sampling clock frequencies to support different communication standards. Ten modes are programmable to comply with CCITT V.21, V.22, V.22 bis, V.23, V.26, V.27, V.29 or V.33 as well as BELL 103, 202 or 212A. The typical curves obtained are given in the TRANSMISSION CHARACTERISTICS section of the data sheet. The receive filter output is smoothed in a continuous time low-pass filter and then directed to the automatic gain control (AGC) amplifier programmable from 0 dB to 46.5 dB with 1.5 dB steps. The same signal is also connected to the carrier level detector input. Three external capacitors are needed to eliminate the offset voltage as indicated in Fig.1. The residual DC level at the analog to digital converter (ADC) input is kept low and independent of the selected gain.

The carrier level detector performs the comparison between the full wave rectified receive signal and programmable threshold voltage nominally equivalent to - 45.5 dBm, - 34.4 dBm or –28.6dBm with a 2.5 dB hysteresis. The binary result of the comparison can be read by the DSP. The nominal response time of the carrier level detector to a signal settlement or removal is 1.78 ms. The receive signal delivered by the AGC amplifier is sampled and converted from analog to digital by a 12-bit monotonic A/D converter whose integral linearity is guaranteed better than 9 bit. The sampling frequency is the same as that programmed for the transmit DAC i.e. 7200, 8000,or 9600 samples per second.

CLOCK GENERATION

The 5.76 MHz master clock is obtained from either a crystal tied between XTAL1 and XTAL2 pins or an external generator connected to the XTAL1 pin. In the latter case the XTAL2 pin should be left open.

Figure 1 : AGC and Carrier Level Detector Amplifier Structure.



To meet the CCITT recommandation, the frequency tolerance requirement of the master clock must be better than ± 100 ppm. The different transmit (Tx) and receive (Rx) clocks are derived from the master clock via two independent digital phase locked loops (DPLL).

TRANSMIT CLOCKS

As shown in Fig.2 the transmit DPLL operates by adding or subtracting pulses to a 2.88 MHz internal clock at a rate of 600 Hz. Consequently the frequency capture range equals ± 600 Hz/2.88 MHz, i.e. ± 208 ppm, a value consistent with the worst case synchronization of two independent signals having ± 100 ppm of frequency accuracy. When V.27 clocks are selected, the DPLL up-dating rate is increased to 800 Hz which is a submultiple of the 1600 baud rate of that particular mode. In this case the frequency capture range is ± 278 ppm.

The transmit DPLL can be synchronized on an external terminal clock connected to the TxSCLK input or on the receive bit clock R x CLK internally generated from the receive DPLL. It can also free-run without any phase shift.

The TS7542 delivers three synchronous transmit clocks :

- a bit clockT x CLK whose frequency equals the bit rate of the MODEM
- a baud clock T x RCLK whose frequency equals the baud rate of the MODEM
- a conversion clock T x CCLK that gives the samplinfrequency of the transmit D/A converter

The frequencies of these three clocks are programmable to support the different MODEM modes. Their duty cycle is exactly 1 : 2. These clocks are available on three dedicated pins. Their status can also be read by the DSP from an internal register, TCR. Resetting of all the transmit clock generator counters on the next negative transition of T x SCLK or R x CLK can be controlled from the data bus.

RECEIVE CLOCKS

The receive DPLL phase shifts are performed in two ways :

- a coarse phase lag is obtained by suppressing several 5.76 MHz master clock pulses from the input of the receive clock generator under the control of the DSP. The number of suppressed pulses is programmable from 20 to 4800 with a step value of 20 or 300. That feature will be used to quickly synchronize the receive DPLL on the recovered receive rate.
- a fine phase lead or lag is obtained by adding or suppressing two master clock pulses from the receive clock generator input, like for the transmit DPLL. But in that case the shifts are controlled by the DSP that also implements the phase comparator of the phase locked loop.

The TS7542 delivers three receive clocks with the same nominal frequency values as their transmit counterparts :

- a bit clock R x CCLK
- a baud clock R x RCLK
- a conversion clock R x CCLK

The status of these clocks can also be read from an internal register, RCR.

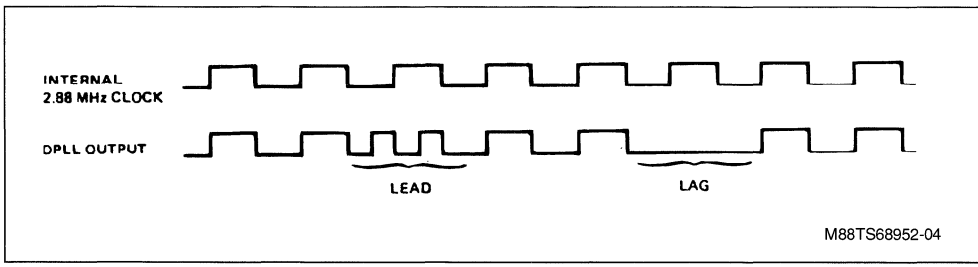
The receive and transmit clocks are plesiochronous.

INTERNAL REGISTERS

The 8-bit bidirectional data bus allows to access 15 internal registers as detailed in Fig.3. The data transfers are controlled by the six following signals :

- two chip select inputs $\overline{CS0}$ and CS1 that must be put respectively to 0 and 1 to allow a data transfer.
- The read/write input R/$\overline{W}$ that defines the transfer direction
- Two register select input that address one out of four registers for a read or a write operation. Actually indirect addressing is used to extend to eight the number of the control registers.

Figure 2 : DPLL Lead and Lag.



- The enable input $\overline{E}$ that strobes on its positive going transition the data to be written, or that enables on its low level state the output buffers when a data is to be read from a register.

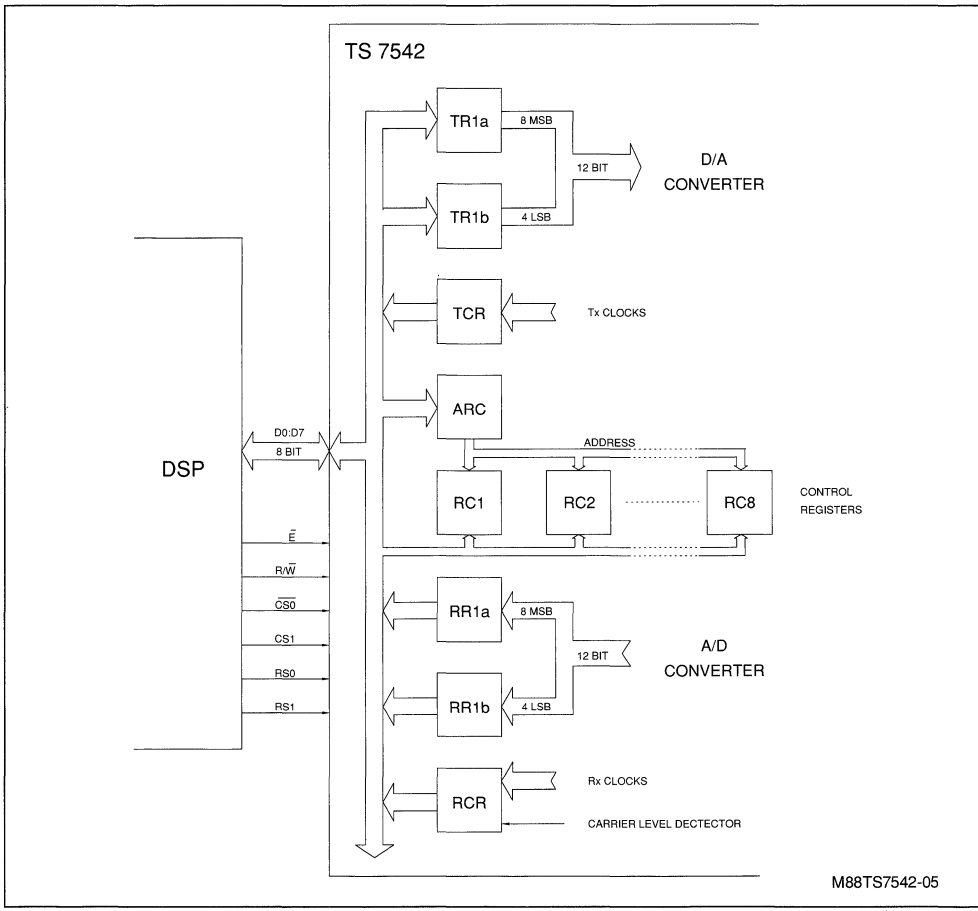
The timing diagram of the data transfers is given in the TIMING SPECIFICATIONS section of the data sheet.
The four registers only accessible in a write operation are :

- TR1a that stores the 8 most significant bit (MSB) of the 12-bit transmit signal digital samples.
- TR1b that stores the 4 least significant bit (LSB) of the transmit signal digital samples.
- ARC that stores the 3-bit address of one out of eight control registers.
- The control register whose address is stored in the ARC register. The content of ARC is automatically incremented after each access to a control register. This allows cyclical access to these registers.

The four registers only accessible in a read operation are :

- RR1a that stores the 8 MSB of the 12-bit receive signal digital samples
- RR1b that stores the 4 LSB of the 12-bit receive signal digital samples
- RCR that stores the receive clock and the carrier level detector status
- TCR that stores the transmit clock status

Figure 3 : Internal Registers Configuration.



The addresses of the internal registers are given in table 1. Table 2 shows the formats used for the digital signal samples stored in the TR1a/b registers, the RR1a/b registers and for the status data stored in the TCR and RCR registers. Table 3 summarizes the address and data format of the 8 control registers whose function is detailed in the PROGRAMMABLE FUNCTIONS section.

Table 1.

R/$\overline{W}$	RS0	RS1	AccessedRegister	Comment
0	0	0	TR1b	Write Only Registers
0	0	1	TR1a	
0	1	0	ARC	
0	1	1	The Control Register Addressed by ARC	
1	0	0	RR1b	Read Only Registers
1	0	1	RR1a	
1	1	0	RCR	
1	1	1	TCR	

Table 2.

Register Name	Register Content(note 1)								Comment
	D7	D6	D5	D4	D3	D2	D1	D0	
TR1a	Tx11	Tx10	Tx9	Tx8	Tx7	Tx6	Tx5	Tx4	
TR1b	Tx3	Tx2	Tx1	Tx0	X	X	X	X	
RR1a	Rx11	Rx10	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	
RR1b	Rx3	Rx2	Rx1	Rx0	0	0	0	0	
TCR	X	TxRCLK	TxCCLK	TxCLK	X	X	X	X	
RCR	CDL	RxRCLK	RxCCLK	RxCLK	X	X	X	X	CDL = 1 if Rx signal is greater than the programmed level.

X = Don't care.
Note 1 :D0 to D7 refer to the data bus pins and gives the bit position in the read or written data.

Table 3.

Control Register Name	ARC Content (address) (note 1)			Register Content (note 2)								Programmed Function
	D7	D6	D5	D7	D6	D5	D4	D3	D2	D1	D0	
RC1	0	0	0	HB3	HB2	HB1	HR2	HR1	X	X	X	Bit/Baud Rate for Tx and Rx Clocks
RC2	0	0	1	X	X	X	HS2	HS1	HTHR	FCLK	X	Conversion Frequency. Tx Synchronization Selection
RC3	0	1	0	RF3	RF2	RF1	REJ	RFG2	RFG1	LAT2	LAT1	Rx Filter and 1800Hz Notch. LAO Attenuation
RC4	0	1	1	ATT4	ATT3	ATT2	ATT1	X	EM2	EM1	X	Tx Attenuation. EXI Input.
RC5	1	0	0	RG5	RG4	RG3	RG2	RG1	X	X	X	AGC Amplifier Gain
RC6	1	0	1	CDG2	CDG1	CDH	X	X	X	X	X	Carrier Level Detector Gain and Hysteresis
RC7	1	1	0	SP5	SP4	SP3	SP2	SP1	X	X	X	RxDPLL Coarse Phase Shift
RC8	1	1	1	MPE	SPR	AVRE	VAL	X	X	X	X	TxDPLL Reset. Rx DPLL Fine Phase Shifts.

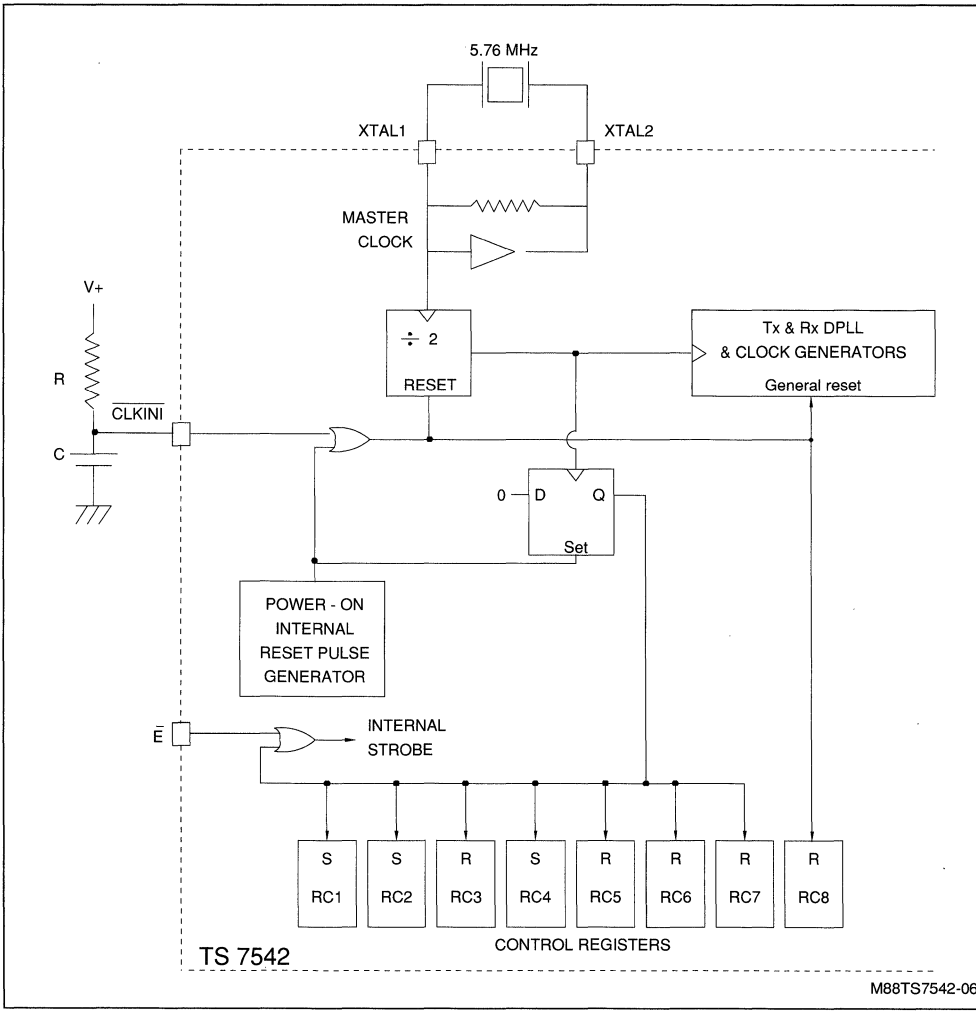
X = Don't care value.
Note 2 : D0 to D7 refers to the data bus pins and gives the bit position in the loaded address or data.

POWER-ON INITIALIZATION

Internal power-on circuitry (Fig.4) automatically resets the DPLL and the clock generators counters, and initializes the RC1 to RC8 control registers. The initial status of these registers are given in the PROGRAMMABLE FUNCTIONS section. The transmit attenuator is initialized to an infinite attenuation in order to avoid the transmission of indesirable signals on the phone line.

Access to the control registers is desabled during power-on reset until the clock oscillator starting. The reset time duration can be increased by connecting the CLKINI input to an external RC timer as indicated in Fig.4. That feature will prevent, in particular applications, possible problems due to incontrolled signals coming from the DSP during power-on. In normal operation the CLKINI input can be used to reset the DPLL and clock generator counters and the RC8 control register. When that pin as not used, it must be tied to V^+

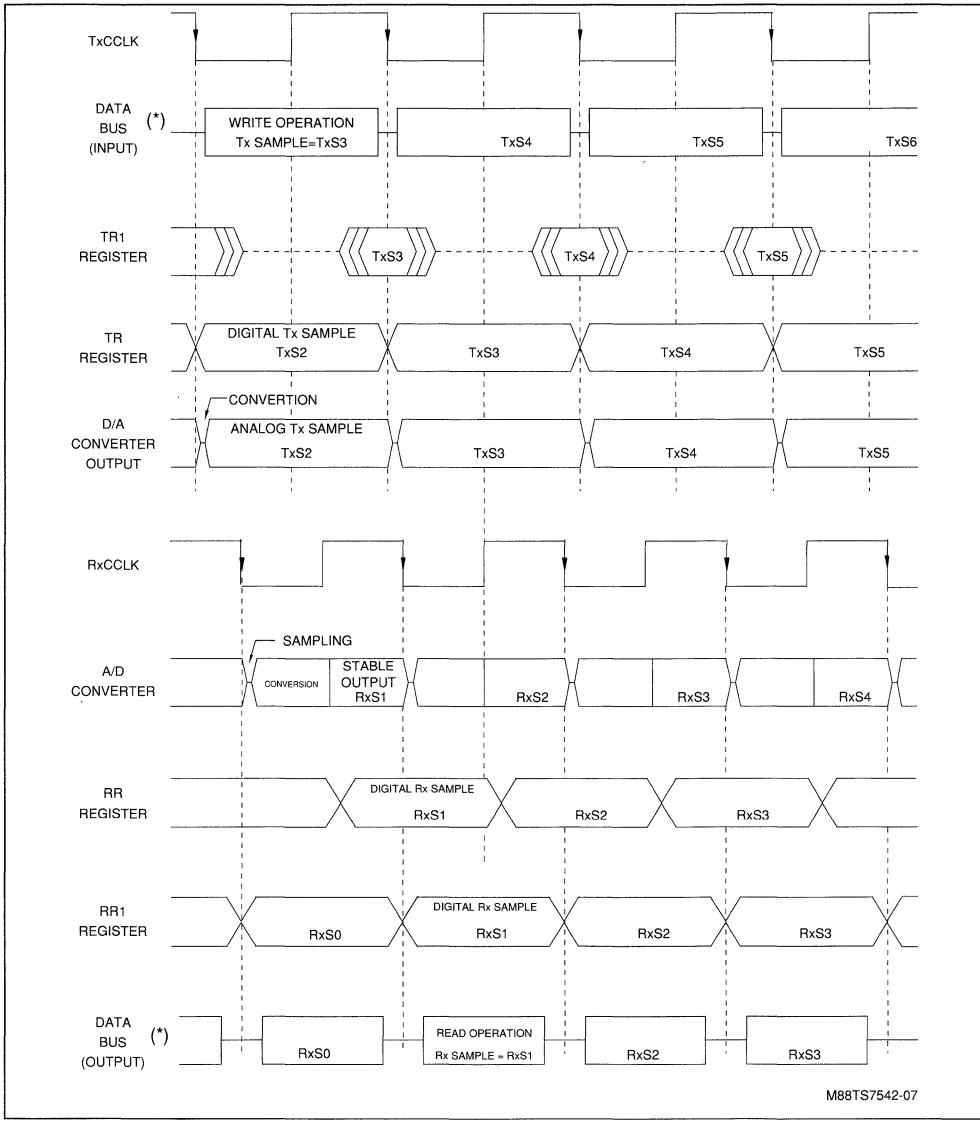
Figure 4 : Power-on Initialization Circuitry.



PROGRESSION OF SIGNAL SAMPLES

Fig.5 shows the progression in the TS7542 of the digital and analog signal samples. It appears that the transfers of the data representing the transmit and the receive signals have to be synchronized on the TxCCLK or the RxCCLK conversion clock, respectively. This is the reason why the DSP needs to receive these clock signals or to read their status from the dedicated registers.

Figure 5 : Digital and Analog Samples Progress.



Notes : Txi = ith analog or digital sample of the Tx signal.
Rxi = ith analog or digital sample of the Rx signal.
(*) Data can be written (read) six master clock periods after the T x CCLK (R x CCLK) negative–going transition respectively

PROGRAMMABLE FUNCTIONS

Table 4 : Bit Clock Frequency Programming (Tx and Rx).

	RC1 Register								TxCLK or RxCLK Bit Clock Nominal Frequency (Hz)	Communication Standard
	D7	D6	D5	D4	D3	D2	D1	D0		
	HB3	HB2	HB1	HR2	HR1	–	–	–		
	0	0	0						9600	V.29
	0	0	1						4800	V.27
	0	1	0						2400	V.22 bis, V.26
	0	1	1						1200	V.22, BELL 212A
	1	0	0						600	V.22 Fall-back
	1	0	1						600	"
	1	1	0						2400	V.22 bis, V.26
P/O	1	1	1						1200	V.22, BELL 212A

P/O : Power on status.

Table 5 : Baud Rate Clock Frequency Programming (Tx and Rx).

	RC1 Register								TxRCLK or RxBCLK Baud Rate Clock Nominal Frequency(Hz)	Communication Standard (note 3)
	D7	D6	D5	D4	D3	D2	D1	D0		
	HB3	HB2	HB1	HR2	HR1	–	–	–		
				0	0				2400	V.29, V.33
				0	1				1600*	V.27*
				1	0				1200	V.26
P/O				1	1				600	V.22, V.22 Bis, BELL 212A

Note 3 : The phase shift frequency of the transmit DPLL is 600 Hz, excepted for (*) 800 Hz.

Table 6 : Conversion Clock Frequency Programming (Tx and Rx).

	RC2 Register								TxCCLK or RxCCLK Conversion (sampling) Clock Nominal Frequency(Hz)	Communication Standard
	D7	D6	D5	D4	D3	D2	D1	D0		
	–	–	–	HS2	HS1	HTHR	FCLK	–		
				0	0				9600	
				0	1				8000	V.27
				1	0				7200	
P/O				1	1				7200	

Table 7 : Tx Synchronization Signal Programming.

	RC2 Register								Selected Synchronisation Signal
	D7	D6	D5	D4	D3	D2	D1	D0	
	–	–	–	HS2	HS1	HTHR	FCLK	–	
						0	0		RxCLK
						1	0		TxSCLK (note 4)
P/O						X	1		Transmit DPLL free-runs

Note 4 : The Tx DPLL free runs if there is no transistion on this pin in that case.
X = Don't care value.

Table 8 : Tx Clock General Reset.

RC8 Register (note 5)								ResettingTransition
D7	D6	D5	D4	D3	D2	D1	D0	
MPE	SPR	AVRE	VAL	–	–	–	–	
1	0	0	0					Next Negative-going Transition of Synchronizing Signal

Note 5 : RC8 register is cleared after the programmed control operation is completed and on power-on.

Table 9 : Rx Clock Phase Shift Programming.

RC8 Register (note 5)							Actionon RxDPLL
D7	D6	D5	D4	D3	D2	D1	
MPE	SPR	AVRE	VAL	–	–	–	
0	1	0	0				Phase Lag of Programmed Amplitude
0	0	0	1				Phase Lag of Two 5.76 MHz Master Clock Periods
0	0	1	1				Phase Lead of Two 5.76 MHz Master Clock Periods

Note 5 : RC8 register is cleared after the programmed control operation is completed and on power-on.

Table 10 : Rx Clock Phase Shift Amplitude Programming.

	RC7 Register							Phase Shift in Degrees		Number of Master Clock Pulses Suppressed
	D7	D6	D5	D4	D3	D2	D1			
	SP5	SP4	SP3	SP2	SP1	–	–	1200 Bauds*	1600 Bauds	
	0	0	0	0	0			1.5	2	20
	0	0	0	0	1			3	4	40
	0	0	0	1	0			4.5	6	60
	0	0	0	1	1			6	8	80
	0	0	1	0	0			7.5	10	100
	0	0	1	0	1			9	12	120
	0	0	1	1	0			10.5	14	140
	0	0	1	1	1			12	16	160
	0	1	0	0	0			13.5	18	180
	0	1	0	0	1			15	20	200
	0	1	0	1	0			16.5	22	220
	0	1	0	1	1			18	24	240
	0	1	1	0	0			19.5	26	260
	0	1	1	0	1			21	28	280
	0	1	1	1	0			22.5	30	300
	0	1	1	1	1			24	32	320
	1	0	0	0	0			22.5	30	300
	1	0	0	0	1			45	60	600
	1	0	0	1	0			67.5	90	900
	1	0	0	1	1			90	120	1200
	1	0	1	0	0			112.5	150	1500
	1	0	1	0	1			135	180	1800
	1	0	1	1	0			157.5	210	2100
	1	0	1	1	1			180	240	2400
	1	1	0	0	0			202.5	270	2700
	1	1	0	0	1			225	300	3000
	1	1	0	1	0			247.5	330	3300
	1	1	0	1	1			270	360	3600
	1	1	1	0	0			292.5		3900
	1	1	1	0	1			315		4200
	1	1	1	1	0			337.5		4500
P/O	1	1	1	1	1			360		4800

(*) 2400 bauds : multiply by two. 600 bauds : divide by two.

Table 11 : Tx Attenuator Programming.

	RC4 Register								Attenuation (dB)
	D7	D6	D5	D4	D3	D2	D1	D0	
	ATT4	ATT3	ATT2	ATT1	–	EM2	EM1	–	
	0	0	0	0					0
	0	0	0	1					2
	0	0	1	0					4
	0	0	1	1					6
	0	1	0	0					8
	0	1	0	1					10
	0	1	1	0					12
	0	1	1	1					14
	1	0	0	0					16
	1	0	0	1					18
	1	0	1	0					20
	1	0	1	1					22
P/O	1	1	X	X					Infinite

X = Don't care value.

Table 12 : EXI and AGC1 Inputs Programming.

	RC4 Register								EXI Input Status	AGC1 Input Status
	D7	D6	D5	D4	D3	D2	D1	D0		
	ATT4	ATT3	ATT2	ATT1	–	EM2	EM1	–		
						0	0		Disabled	Tied to AGC Amplifier Input
						0	1		Tied to Tx Filter Input	"
						1	0		Tied to Tx Attenuator Input	"
P/O						1	1		Disabled	Tied to A/DC Input

Table 13 : Rx Filter Programming.

	RC3 Register				Sampling (Fs) and Cut-off (Fc) Frequencies (note 6)				Communication Standard	See Figure N°
	D7	D6	D5	D4	Low Pass Section		High Pass Section			
	RF3	RF2	RF1	RF0	Fs(kHz)	Fc(Hz)	Fs(kHz)	Fc(Hz)		
P/O	0	0	0	X	288	3200	144	1820	V.22, V.22 bis, BELL 212A and BELL 103 High Channels	7
	0	0	1	X	192	2133	115.2	1456	V.21 High Channel	8
	0	1	0	X	288	3200	82.3	1040	V.27 ter 2400 bps	9
	0	1	1	X	288	3200	72	910	V.27 ter 4800 bps, V.23, V.26 and BELL 202	10
	1	0	0	0	144	1600	64	809	V.22, V.22 bis, ,BELL 212A and BELL 103 Low Channels	11
	1	0	0	1	144	1600	64	809	V.22, V.22 bis Low Channels with 1800 Hz Tone Rejection (*)	12
	1	0	1	X	115.2	1280	64	809	V.21 Low Channel	13
	1	1	0	X	288	3200	36	455	V.29, V.33	14
	1	1	1	X	288	3200	18	228	Full Channel Bandwidth	15
	1	1	1	X	48	533	27.4	347	75 bps Back Channel	16

(*) In this mode the 1800 Hz notch filter section is enabled.
X = Don't care values. The notch section is disabled in all these cases.
Note 6 : The sampling clocks used by the Rx switched capacitor filters are straightly derived from the crystal oscillator. The Tx switched capacitor filter is driven from the Tx DPLL.

Table 14.

	RC3 Register								Rx Filter Gain (dB)
	D7	D6	D5	D4	D3	D2	D1	D0	
	RF3	RF2	FR1	RF0	RFG2	RFG1	LAT2	LAT1	
P/O					0	0			0
					0	1			3
					1	0			6
					1	1			9

Table 15 : Line Output Attenuator Programming.

	RC3 Register								LAO Output Attenuation (dB)
	D7	D6	D5	D4	D3	D2	D1	D0	
	RF3	RF2	RF1	RF0	RFG2	RFG1	LAT2	LAT1	
P/O							0	0	Infinite
							0	1	0
							1	0	6
							1	1	12

Table 16 : Carrier Level Detector Programming.

	RC6 Register								Carrier Level Detector Threshold(dBm) (note 7)
	D7	D6	D5	D4	D3	D2	D1	D0	
	CDG2	CDG1	CDH	–	–	–	–	–	
P/O	0	0	0						– 29.85
	0	0	1						– 27.35
	0	1	0						– 36.65
	0	1	1						– 34.15
	1	0	0						– 46.75
	1	0	1						– 44.25
	1	1	0						– 46.75
	1	1	1						– 44.25

Note 7 : These values applies when the total Rx gain from the phone line to the Rx filter output is 0 dB.

Table 17 : AGC Amplifier Gain Programming.

	RC5 Register					AGC AmplifierGain (dB)	
	D7	D6	D5	D4	D3		
	RG5	RG4	RG3	RG2	RG1	AGC1 Input	AGC2 Input
P/O	0	0	0	0	0	0	− ∞
	0	0	0	0	1		1.5
	− ∞	0	0	0	1	0	3
	− ∞	0	0	0	1	1	4.5
	− ∞	0	0	1	0	0	6
	− ∞	0	0	1	0	1	7.5
	− ∞	0	0	1	1	0	9
	− ∞	0	0	1	1	1	10.5
	− ∞	0	1	0	0	0	12
	− ∞	0	1	0	0	1	13.5
	− ∞	0	1	0	1	0	15
	− ∞	0	1	0	1	1	16.5
	− ∞	0	1	1	0	0	18
	− ∞	0	1	1	0	1	19.5
	− ∞	0	1	1	1	0	21
	− ∞	0	1	1	1	1	22.5
	− ∞	1	0	0	0	0	24
	− 14.5	1	0	0	0	1	25.5
	− 7.7	1	0	0	1	0	27
	− 3.4	1	0	0	1	1	28.5
	0	1	0	1	0	0	30
	2.7	1	0	1	0	1	31.5
	5.2	1	0	1	1	0	33
	7.4	1	0	1	1	1	34.5
	9.5	1	1	0	0	0	36
	11.4	1	1	0	0	1	37.5
	13.3	1	1	0	1	0	39
	15.1	1	1	0	1	1	40.5
	16.8	1	1	1	0	0	42
	18.5	1	1	1	0	1	43.5
	20.2	1	1	1	1	0	45
	21.8	1	1	1	1	1	46.5

ELECTRICAL SPECIFICATIONS

Unless otherwise noted, electrical characteristics are specified over the operating range. Typical values are given for $V^+ = +5$ V, $V^- = -5$ V and $t_{amb} = 25$ °C.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
	DGND Digital Ground to AGND Analog Ground	− 0.3 to + 0.3	V
	V^+ Supply Voltage to DGND or AGND Ground	− 0.3 to + 7	V
	V^- Supply Voltage to DGND or AGND Ground	− 7 to + 0.3	V
V_I	Voltage at any Digital Input or Output	DGND − 0.3 to V^+ + 0.3	V
I_I	Digital Output Current	− 20 to + 20	mA
V_{in}	Voltage at any Input or Output	V^- − 0.3 to V^+ + 0.3	V
I_{out}	Analog Output Current	− 10 to + 10	mA
P_{tot}	Power Dissipation	500	mW
t_{amb}	Operating Temperature Range	0 to + 70	°C
t_{stot}	Storage Temperature Range	− 65 to + 150	°C
t_{sold}	Pin Temperature (soldering 10 s.)	+ 260	°C

POWER SUPPLIES
DGND = AGND = 0 V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V^+	Positive Power Supply	4.75		5.25	V
V^-	Negative Power Supply	− 5.25		− 4.75	V
I^+	Positive Supply Current (receive signal level 0 dBm)			35	mA
I^-	Negative Supply Current (receive signal level 0 dBm)	− 35			mA

DIGITAL INTERFACE
Control Inputs, Data Bus and Clock Outputs. Voltages referenced to DGND = 0 V

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2.2			V
I_{IL}	Low Level Input Current	DGND < V_I < 0.8 V	− 10		10	µA
I_{IH}	High Level Input Current	2.2 V < V_I < V^+	− 10		10	µA
V_{OL}	Low Level Output Voltage (I_{OL} = 2.5 mA)				0.4	V
V_{OH}	High Level Output Voltage (I_{OH} = − 2.5 mA)		2.4			V
I_{OZ}	High Impedance Output Current (when $\overline{E}$ is high and DGND < V_O < V^+)		− 50		50	µA
Crystal Oscillator Interface (XTAL1 input)						
V_{IL}	Low Level Input Voltage				1.5	V
V_{IH}	High Level Input Voltage		3.5			V
I_{IL}	Low Level Input current	DGND ≤ V_I ≤ V_{ILmax}	− 15			µA
I_{IH}	High Level Input Current	V_{IHmin} ≤ V_I ≤ V^+			15	µA

ELECTRICAL SPECIFICATIONS (continued)

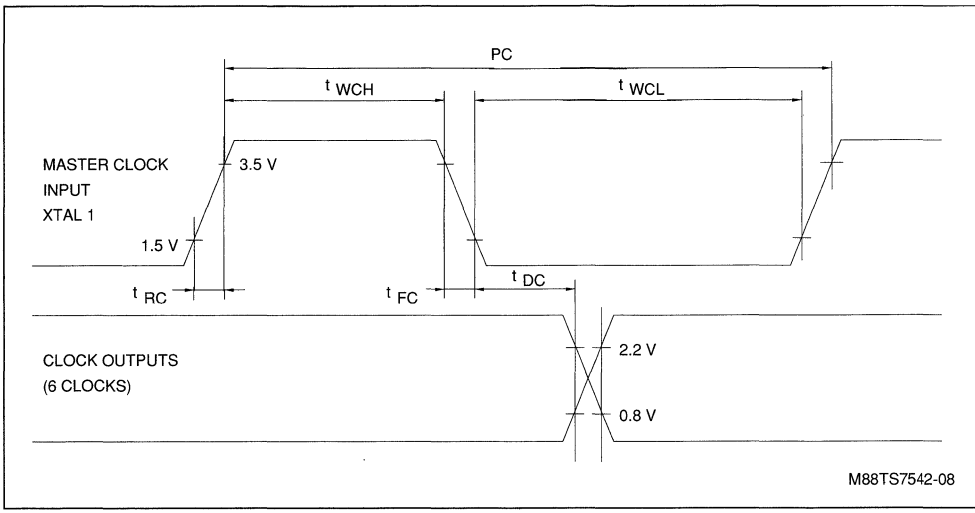
ANALOG INTERFACE All voltages referenced to AGND = 0 V

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{in}	Input Voltage EXI, DxI, RAI		– 2.5		2.5	V
I_{in}	Input Current EXI, DxI, RAI (– 2.5 V < V_{in} < 2.5 V)		– 1		1	µA
R_{in}	Input Resistance AGC1, AGC2		1.5			kΩ
R_{in}	Input Resistance CD1		0.7			kΩ
V_{out}	Output Voltage ATO, LAO, RFO	RL = 1 kΩ, CL = 50 pF	– 2.5		2.5	V
R_{out}	Output Resistance	ATO LAO RFO			4 50 15	Ω
R_L	Load Resistance ATO, RFO		1			kΩ
C_L	Load Capacitance ATO, RFO				50	pF
R_L	Load Resistance LAO		10			kΩ
C_L	Load Capacitance LAO				20	pF

TIMING SPECIFICATIONS

TIMING SPECIFICATIONS Clock Timing Characteristics (XTAL1 input)

Symbol	Parameter		Min.	Typ.	Max.	Unit
PC	Master Clock Period			173.6		ns
t_{WCL}	Master Clock Width Low Level		50			ns
t_{WCH}	Master Clock Width High Level		50			ns
t_{RC}	Master Clock Rise Time				50	ns
t_{FC}	Master Clock Fall Time				50	ns
t_{DC}	Clock Output Delay Time	C_L = 50 pF			500	ns
t_{TC}	Clock Output Transition Time	C_L = 50 pF			100	ns

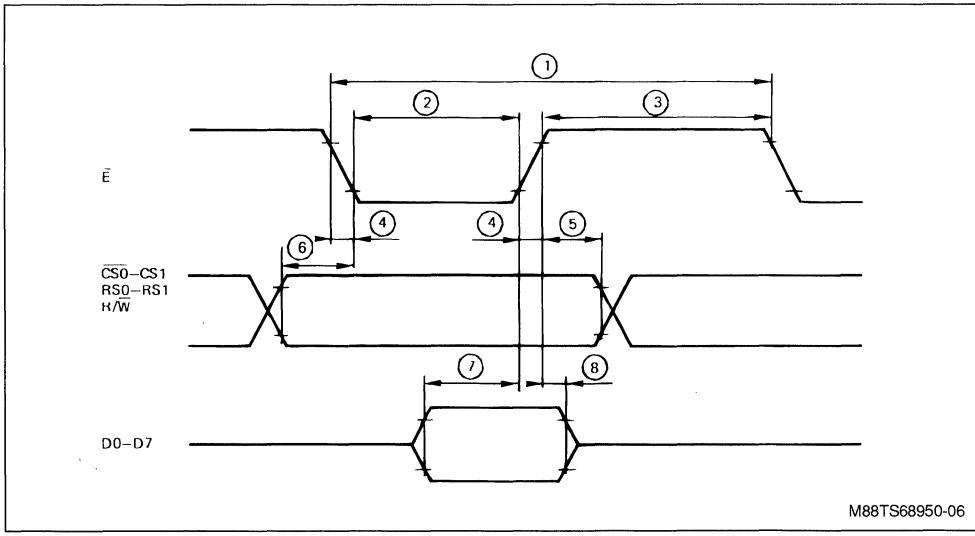


ELECTRICAL SPECIFICATIONS (continued)

BUS TIMING CHARACTERISTICS (see foot notes 1 and 2 on timing diagrams)

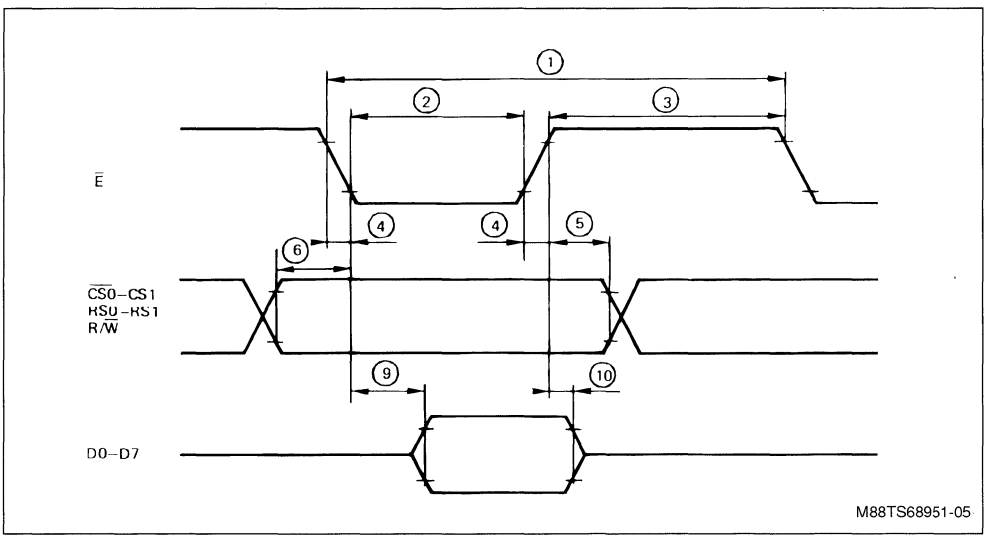
Symbol	Parameter		Min.	Typ.	Max.	Unit
t_{CYC}	Cycle Time	(1)	320			ns
t_{WEL}	Pulse Width $\overline{E}$ Low Level	(2)	180			ns
t_{WEH}	Pulse Width $\overline{E}$ High Level	(3)	100			ns
t_r, t_g	Clock Rise and Fall Time	(4)			20	ns
t_{HCE}	Control Signal Hold Time	(5)	10			ns
t_{SCE}	Control Signal Set-up Time	(6)	40			ns
t_{SDI}	Input Data Set-up Time	(7)	120			ns
t_{HDI}	Input Data Hold Time	(8)	10			ns
t_{SDO}	Output Data Set-up Time (1 TTL load and CL = 50 pF)	(9)			150	ns
t_{dz}	Output High Impedance Delay Time (1 TTL load and CL = 50 pF)	(10)			80	ns

WRITE OPERATION



Note 1 : Voltage levels shown are VIL < 0.4 V, VIH > 2.4 V, unless otherwise specified.
Note 2 : Measurement points shown are 0.8 V and 2.2 V, unless otherwise specified.

READ OPERATION



Note 1 : Voltage levels shown are VIL < 0.4 V, VIH > 2.4 V, unless otherwise specified.
Note 2 : Measurement points shown are 0.8 V and 2.2 V, unless otherwise specified.

TRANSMISSION CHARACTERISTICS

PERFORMANCES OF THE WHOLE TRANSMISSION CHAIN (Input TR1, Output ATO)

Symbol	Parameter	Min.	Typ.	Max.	Unit
G_{abs}	ATO Absolute Gain at 1 kHz	– 0.5	0	0.5	dB
N	ATO Psophometric Noise			100	µV
$PSRR^+$	ATO Positive Power Supply Rejection Ratio V_{ac} = 200 mV_{pp} f = 1 kHz		40		dB
$PSRR^-$	ATO Negative Power Supply Rejection Ratio V_{ac} = 200 mV_{pp} f = 1 kHz		40		dB
THD	Total Harmonic Distortion			– 54	dB

DAC TRANSFER CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Converter Resolution		12		Bit
V_{out}(max)	Nominal Output Peak to Peak Amplitude		5.0		V
LSB	Least Significant Bit Amplitude		1.2		mV
E_{il}	Integral Linearity Error Relative to Best Fit Line		± 4	± 8	LSB
E_{dl}	Differential Linearity Error			± 0.7	LSB

TRANSMISSION CHARACTERISTICS

TRANSMIT FILTER TRANSFER CHARACTERISTICS (input EXI, output ATO)
(see figure 6)

Symbol	Parameter	Min.	Typ.	Max.	Unit
G_{abs}	Absolute Gain at 1 kHz	– 0.3	0	0.3	dB
G_{rel}	Gain Relative to G_{abs} without Sin x/x Correction of DAC Sampling				
	Below 3100 Hz	– 0.4		0.3	dB
	3200 Hz	– 3			dB
	4000 Hz			– 36	dB
	5000 Hz to 12000 Hz			– 46	dB
	12000 Hz and Above			– 50	dB
T_{gp}	Group Propagation Delay Time (f = 1800 Hz)		250		µs
T_{gpd}	Group Propagation Delay Time Distortion (600 Hz < f < 3000 Hz)		430		

Tx ATTENUATOR TRANSFER CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
AT_{abs}	Absolute Attenuation at 0 dB Nominal Value	– 0.3	0	0.3	dB
AT_{rel}	Attenuation Relative to Nominal Value	– 0.5		0.5	dB
AT_{max}	Maximum Attenuation	50			dB

RECEPTION CHARACTERISTICS

PERFORMANCE OF THE WHOLE RECEPTION CHAIN (input RAI or DxI, output RR1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
G_{abs}	Absolute Gain (AGC gain = 0 dB, RxCCLK = 9600 Hz, V_{in} = 775 mVrms, f = 2000 Hz)	– 0.5	0	1.5	dB
HD_T	Total Harmonic Distortion (AGC gain = 0 dB, RxCCLK = 9600 Hz, V_{in} = 775 mVrms, f = 2000 Hz, programmed band = 475 Hz – 3200 Hz)			– 54	dB
N	Equivalent RMS Noise (see note) (AGC gain = 0 dB, RAI, DxI tied to AGND, frequency band = 228 Hz – 3200 Hz)			800	µVrms

Note : Noise depends on AGC gain value.

RECEPTION CHARACTERISTICS (continued)

RECEIVE BAND-PASS FILTER AND REJECTION FILTER (input RAI or DxI, output RFO)

The characteristics and specifications (templates) of the ten programmable transfer functions are given on figures 7 to 16.

RECEIVE FILTER INPUT GAIN CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
G_{rel}	Relative Gain to Programmed Gain	– 0.5		0.5	dB

LINE MONITORING ATTENUATOR CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
AT_{abs}	Absolute Attenuation at 0 dB Nominal Value	– 0.3	0	0.3	dB
AT_{rel}	Attenuation Relative to Nominal Value (2 dB ≤ AT ≤ 22 dB)	– 0.5		0.5	dB
AT_{max}	Maximum Attenuation (AT = ∞)	50			dB

AGC AMPLIFIER AND A/D CONVERTER (input AGC1, output RR1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
G_{rel}	Relative Gain to Programmed Gain				
	0 dB ≤ AGC ≤ 24 dB	– 0.5		0.5	dB
	25.5 ≤ AGC ≤ 46.5 dB	– 1		1	dB
V_{os}	Offset Voltage	– 70		70	LSB

CARRIER LEVEL DETECTOR (input AGC1, output CDR)

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{rel}	Relative Threshold to Programmed Value T				
	– 36.65 < T ≤ – 27.35 dBm	0.5		0.5	dB
	– 46.75 ≤ T ≤ – 36.65 dBm	1		1	dB
H_{yst}	Hysteresis	2		3	dB
V_{os}	Input Offset Voltage				
	1st Threshold Pair (see table 16 and fig. 2)	– 1		1	mV
	2nd Threshold Pair	– 2		2	mV
	3rd Threshold Pair	– 3		3	mV
T_{dd}	Detection Delay Time 0 mVrms to 775 mVrms Transition or 775 mVrms to 0 mVrms Transition	1		3	ms

PERFORMANCE OF THE A/D CONVERTER (input AGC1, output RR1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{in(max)}$	Input Voltage (peak to peak)			5	V
R_{esh}	A/D Converter Resolution			12	Bit
LSB	Analog Increment		1.2		mV
E_{il}	Integral Linearity Error Relative to Best Fit Line		± 4	± 8	LSB
E_{dl}	Differential Linearity Error			± 0.7	LSB
V_{os}	Offset Voltage	– 100		100	LSB

Figure 6 : Tx Filter Frequency Response.

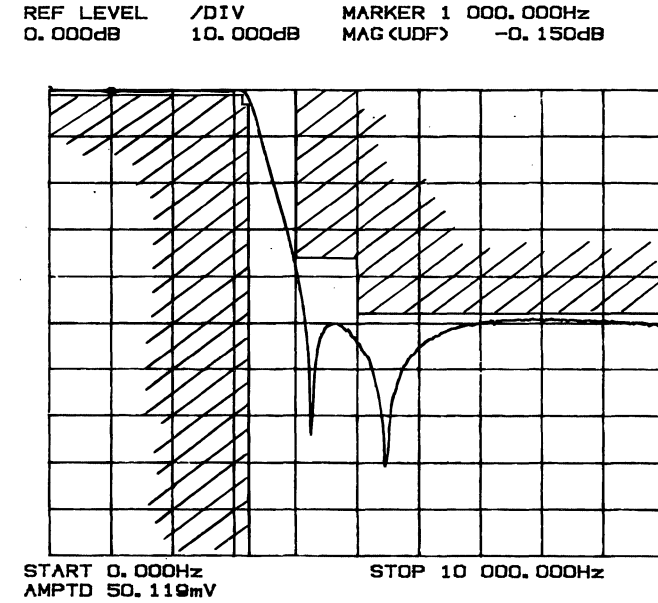


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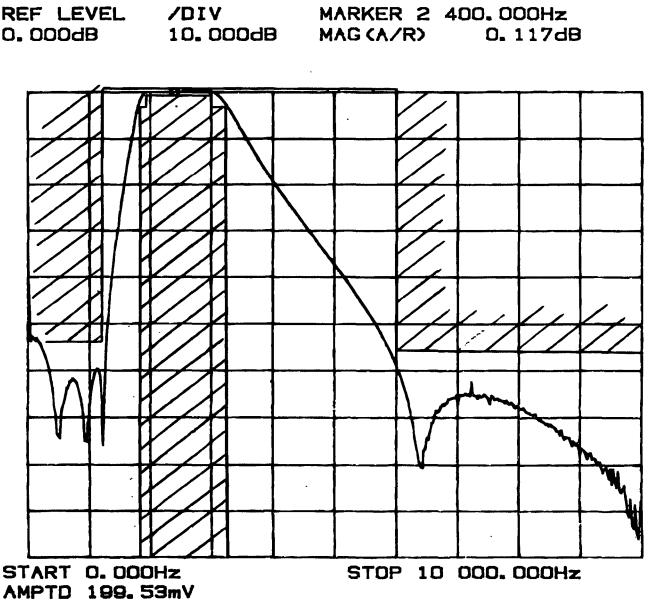
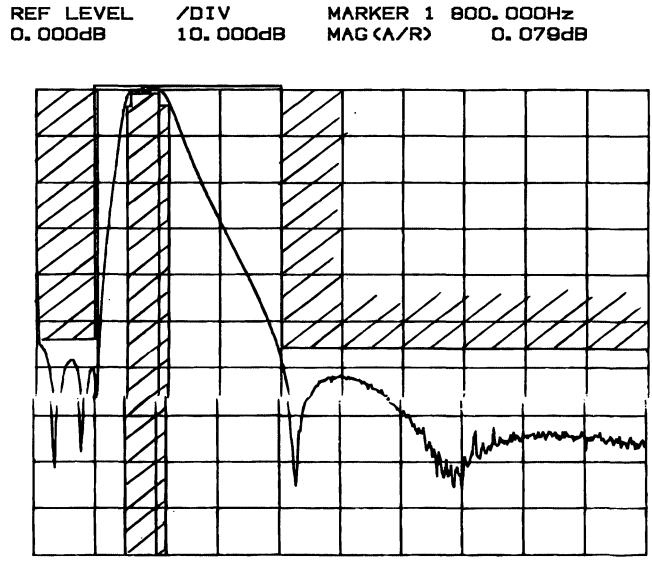
Figure 7 : Rx Filter Frequency Response for V.22, V.22bis, BELL212A and BELL103 High Channels (see table 13).



M88TS7542-10

Figure 8 : Rx Filter Frequency Response for V.21 High Channel (see table 13).



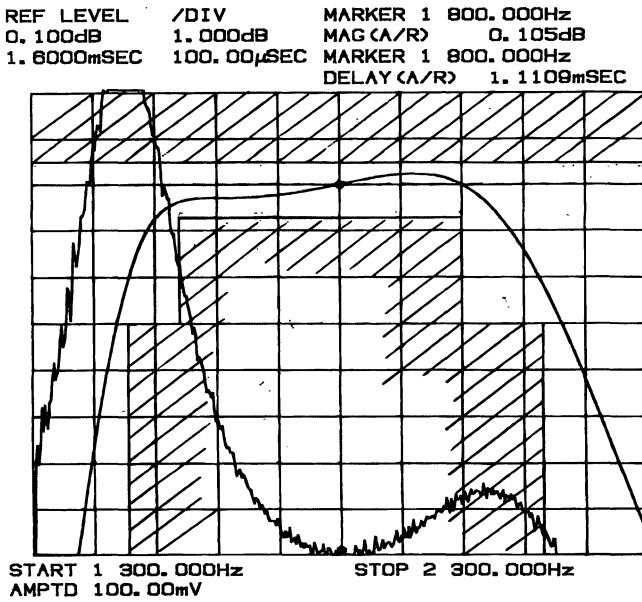


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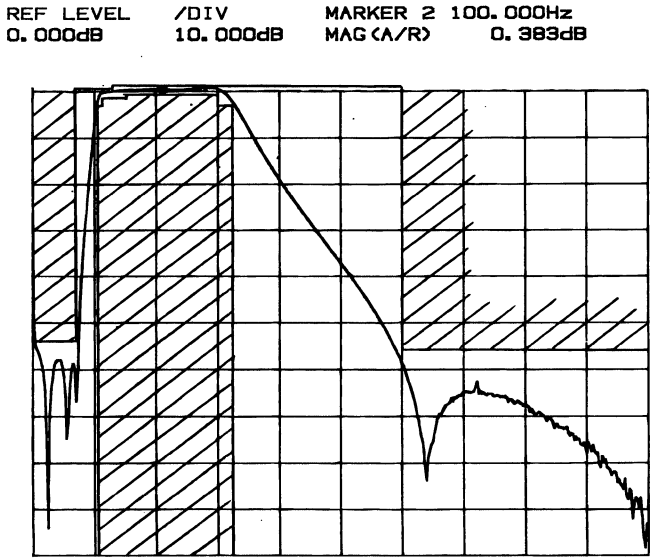
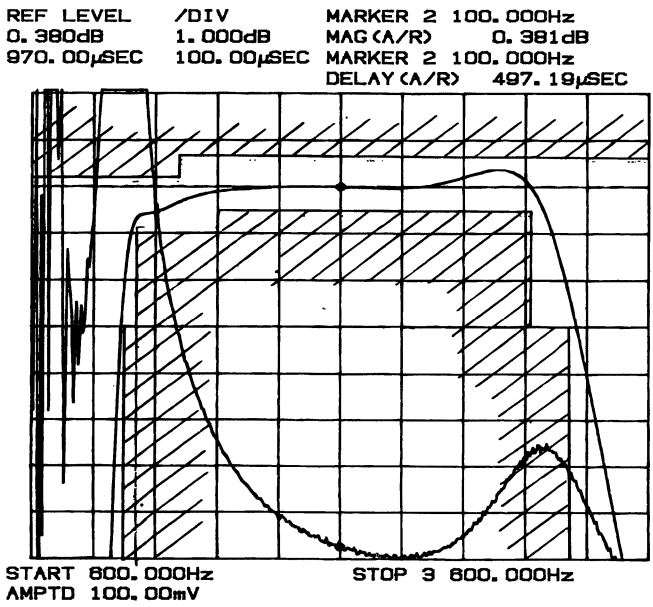
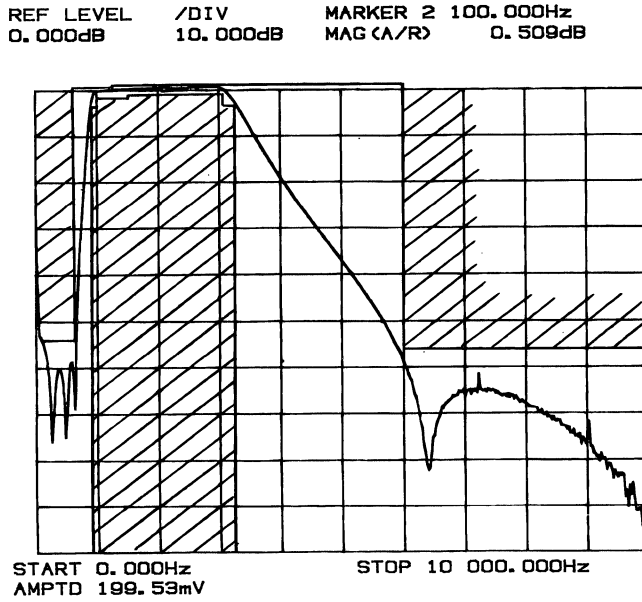
Figure 9 : Rx Filter Frequency Response for V.27ter 2400bps (see table 13).





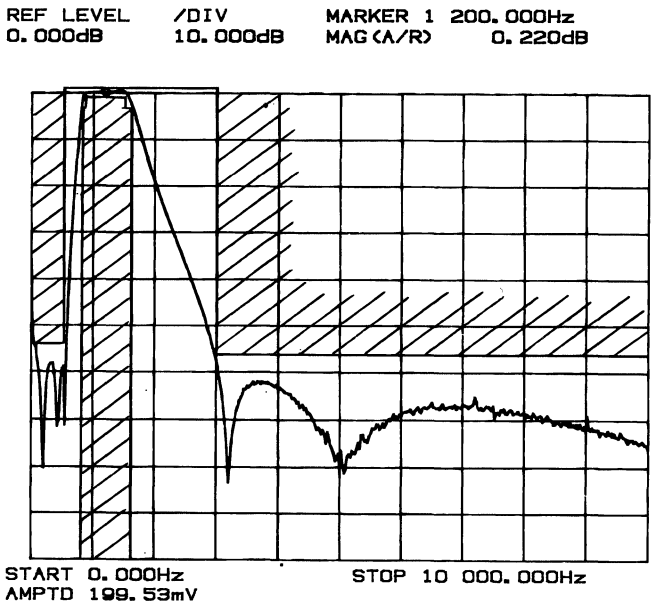
M88TS7542-12

Figure 10 : Rx Filter Frequency Response for V.27ter 4800bps, V.23, V.26 and BELL202 (see table 13).



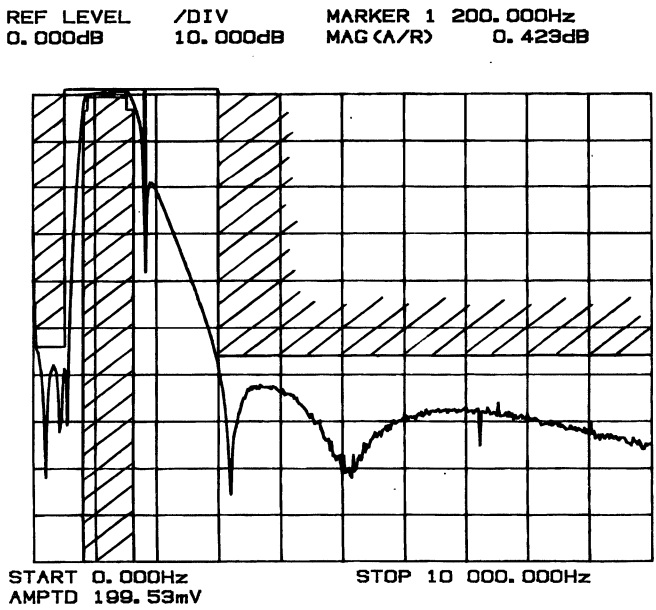
M88TS7542-13

Figure 11 : Rx Filter Frequency Response for V.22, V.22bis, BELL212A and BELL103 Low Channel (see table 13).



M88TS7542-14

Figure 12 : Rx Filter Frequency Response for V.22 and V.22bis Low Channels with 1800Hz Tone Rejection (see table 13).



M88TS7542-15

Figure 12 (continued) : Rx Filter Frequency Response for V.22 and V.22bis Low Channels with 1800Hz Tone Rejection (see table 13).

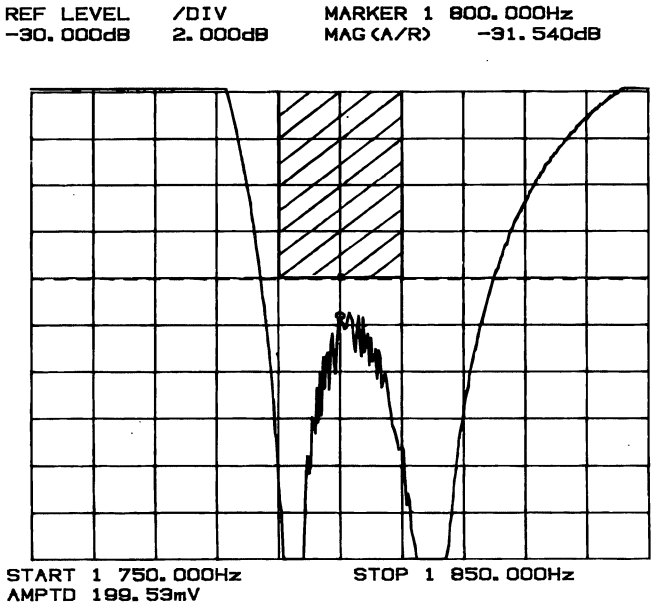
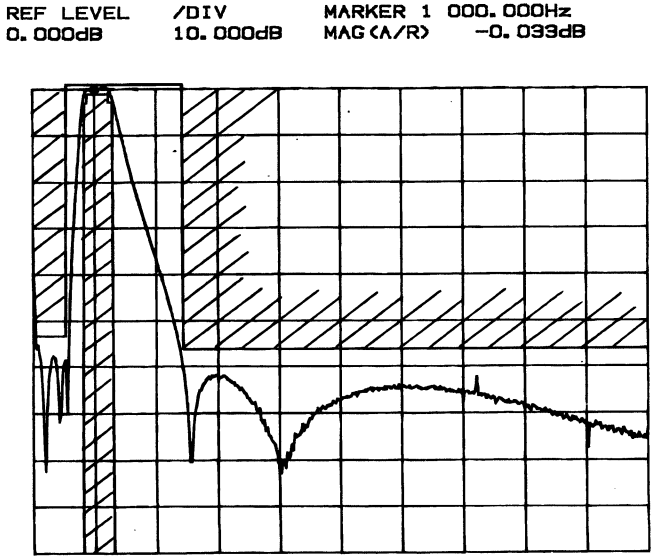


Figure 13 : Rx Filter Frequency Response for V.21 Low Channel (see table 13).



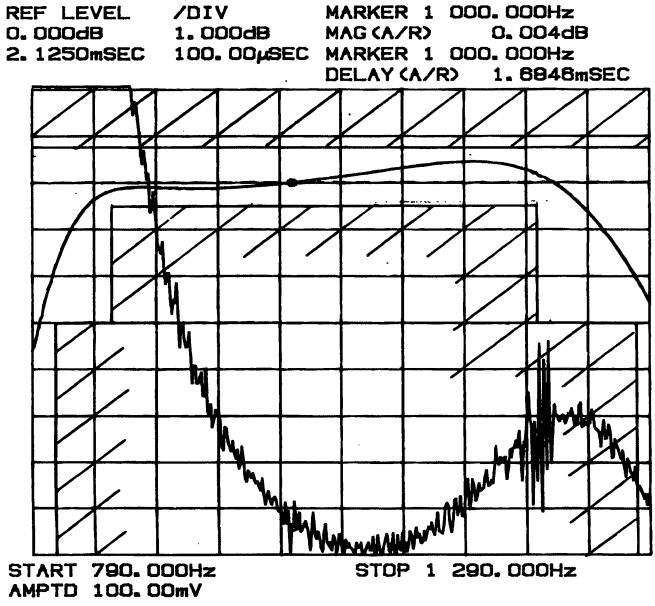


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Figure 14 : Rx Filter Frequency Response for V.29 and V.33 (see table 13).

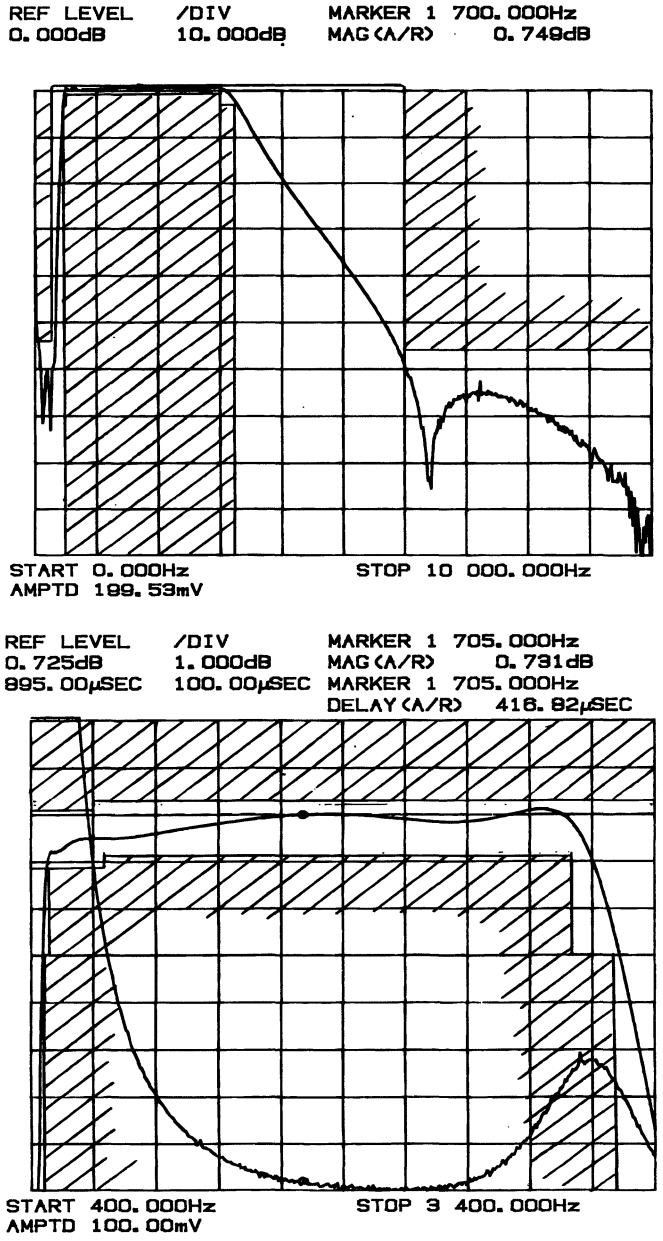

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Figure 15 : Rx Filter Frequency Response with Full Channel Bandwidth (see table 13).

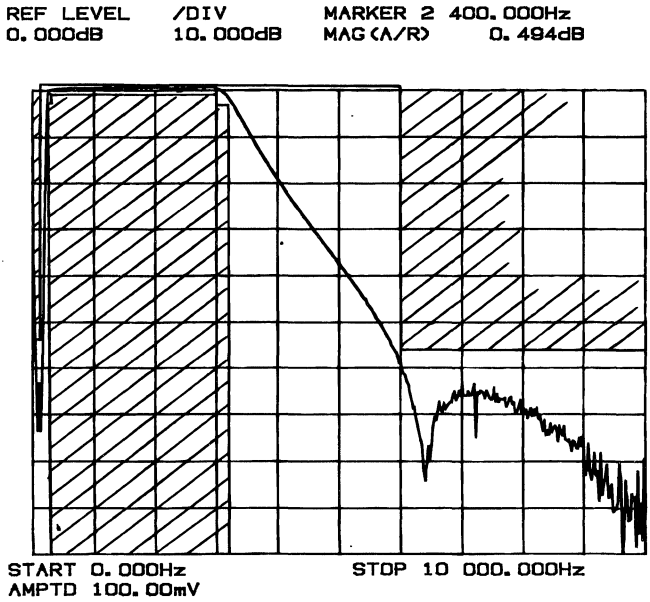

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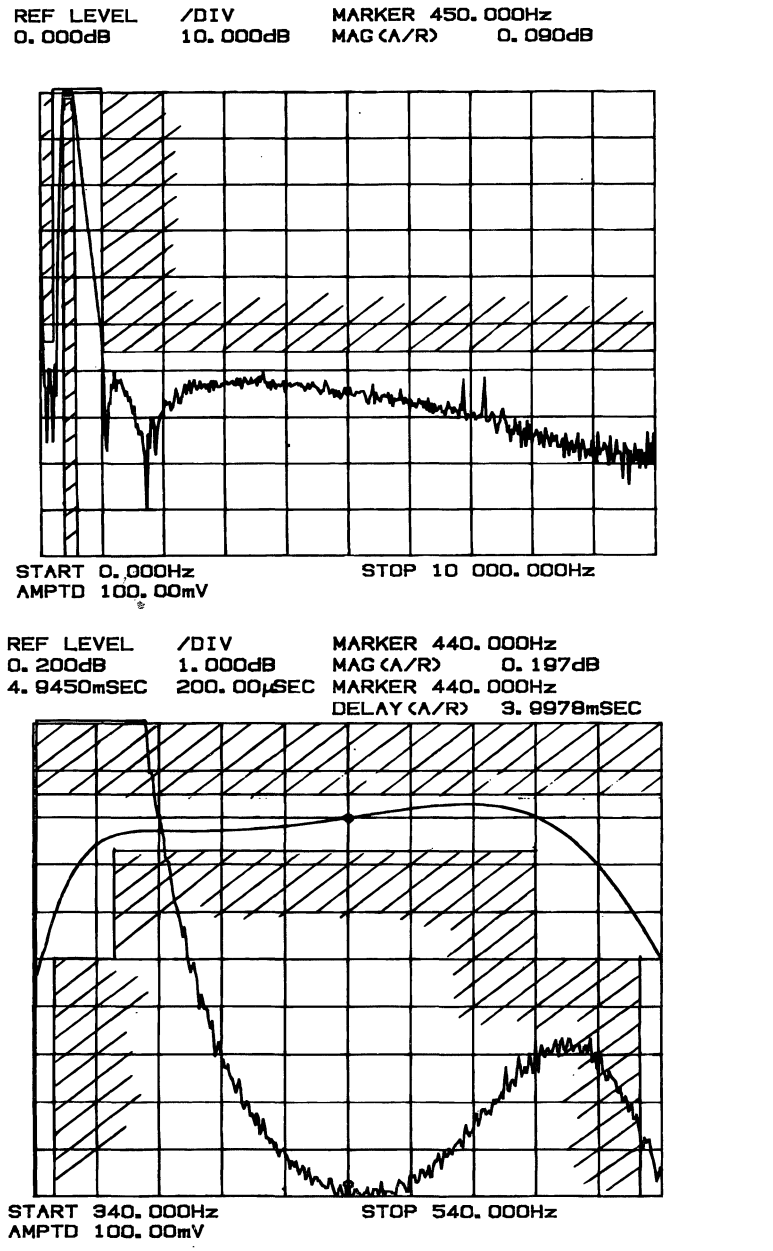
Figure 16 : Rx Filter Frequency Response for 75bps Back Channel (see table 13).



M88TS7542-19

SGS-THOMSON MICROELECTRONICS

TS75C25

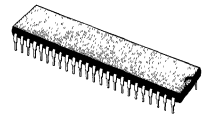
V.22 BIS, V.22, BELL 212, V.21 V.23, BELL 103 MODEM CHIP SET

ADVANCE DATA

- CCITT V.22 BIS COMPATIBLE MODEM CHIP SET
- CCITT V.21, V.22 AND V.23 COMPATIBLE MODEM CHIP SET
- BELL 103 AND 212 COMPATIBLE MODEM CHIP SET
- DIGITAL SIGNAL PROCESSING (TS75C250) AND ANALOG FRONT-END (TS7542) IMPLEMENTATION
- QAM, DPSK AND FSK MODULATION AND DEMODULATION
- DATA TRANSMISSION SPEED :
  - 2400BPS IN QAM
  - 1200 OR 600BPS IN DPSK
  - 1200 OR 300 OR 75BPS IN FSK
- ADAPTIVE EQUALIZATION
- TRANSMIT AND RECEIVE FILTERING
- SHARP ADJACENT CHANNEL REJECTION
- PROGRAMMABLE TRANSMIT OUTPUT LEVELS
- ON-CHIP 4/2-WIRE HYBRID CAPABILITY
- ANSWER TONE DETECTION AND GENERATION FOR CCITT (2100Hz), BELL (2225Hz), AND TRANSPAC (1650Hz) RECOMMENDATIONS
- 550Hz AND 1800Hz GUARD TONE GENERATION
- DTMF TONE GENERATION
- CALL PROGRESS TONE DETECTION
- SELECTABLE SCRAMBLER AND DESCRAMBLER
- DYNAMIC RECEIVE RANGE 0 TO - 48dBm
- TYPICAL 10^{-4} B.E.R. ACHIEVED WITH A 13dB S/N RATIO (V.22 BIS)
- ± 10Hz FREQUENCY OFFSET CAPABILITY
- SUPPLY VOLTAGE : ± 5V
- POWER CONSUMPTION 0.7W
- CMOS TECHNOLOGY
- SOFTWARE LICENSE AND DEVELOPMENT TOOLS AVAILABLE FOR EASY CUSTOMIZATION

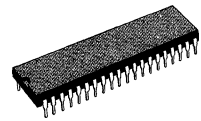
DESCRIPTION

The SGS THOMSON Microelectronics multi-standard V.22 bis chip set is a high performance modem engine, which can operate up to 2400bps in full duplex over public switched telephone network or leased lines. The TS75C25 also allows implementation of modems complying with CCITT V.21, V.22, V.23, and BELL 103, 212 recommendations. The modem hardware consists of a DSP chip and an analog front end (TS7542). The modem signal processing functions are implemented on a ST18930 CMOS programmable digital signal processor, namely TS75C250. In the DSP, internal program memory is available allowing easy customization.

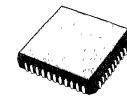


P
DIP48
(Plastic Package)
TS75C250

FN
PLCC52
(Plastic Lead Chip **TS75C250** Carrier)



P
DIP40
(Plastic Package)
TS7542



FN
PLCC44
(Plastic Package)
TS7542

(Ordering Information at the end of the datasheet)

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1. PIN DESCRIPTION

1.1. SYSTEM INTERFACE

TS75C250 (DSP)

Name	Type	Description
AD0.AD7	I/0	System Data Bus : these lines are used for transfer between the TS75C25 mailbox and the control processor.
$\overline{CS}$	I	Chip Select : this input is asserted when the TS75C25 is to be accessed by the control processor.
$\overline{RS}$	I	Register Select : this signal is used to control the data transfers between the control processor and the TS75C25 mailbox.
$\overline{SDS}$	I	System Data Strobe : synchronizes the transfer between the TS75C25 mailbox and the control processor.
SR/$\overline{W}$	I	System Read/Write : Control Signal for the TS75C25 Mailbox Operation
$\overline{IRQ}$	O	Interrupt Request : signal sent to the control processsor to access the TS75C25 mailbox.
$\overline{RESET}$	I	Reset of the TS75C25. Must be maintened for a minimum of five clocks cycles.

1.2. ANALOG INTERFACE

TS7542 (analog transmit and Receive parts)

Name	Type	Description
ATO	O	Analog Transmit Output
LAO	O	Line Monitoring Output for Loud Speaker
RAI	I	Receive Analog Input
DXI	I	Duplexer Input. This signal is subtracted from signal RAI.

1.3. CLOCK INTERFACE

TS7542 (clock part)

Name	Type	Description
TxCLK	O	Transmit Bit Clock
TxRCLK	O	Additional Transmit Clock
TxCCLK	O	Transmit Conversion Clock
RxCLK	O	Receive Bit Clock
RxRCLK	O	Additional Receive Clock
RxRCCLK	O	Receive Conversion Clock
TxSCLK	I	Transmit Synchro Clock : can be used to synchronize the transmitter on an external bit clock provided by the RS232C (or V 24) junction.

2. FUNCTIONAL DESCRIPTION

2.1. SYSTEM ARCHITECTURE

The SGS-THOMSON V.22 bis chip set is a highly integrated modem engine which provides the functionality and performance requirements for full-duplex 2400bps modem solutions at a low cost with excellent performance due to digital signal processing technology. On top of the V.22 bis, the TS75C25 chip set also implements the CCITT V.21, V.22, V.23 and BELL 103, 212 requirements.

The TS75C250 is a programmable digital signal processor which implements the complete signal processing functions required to send and receive data according to the standard requirement and utilities such as call progress tone detection, auto-answer tone detection and tone generation.

The TS7542 (modem analog front end) is designed to meet the requirements of the whole range of voiceband modems.

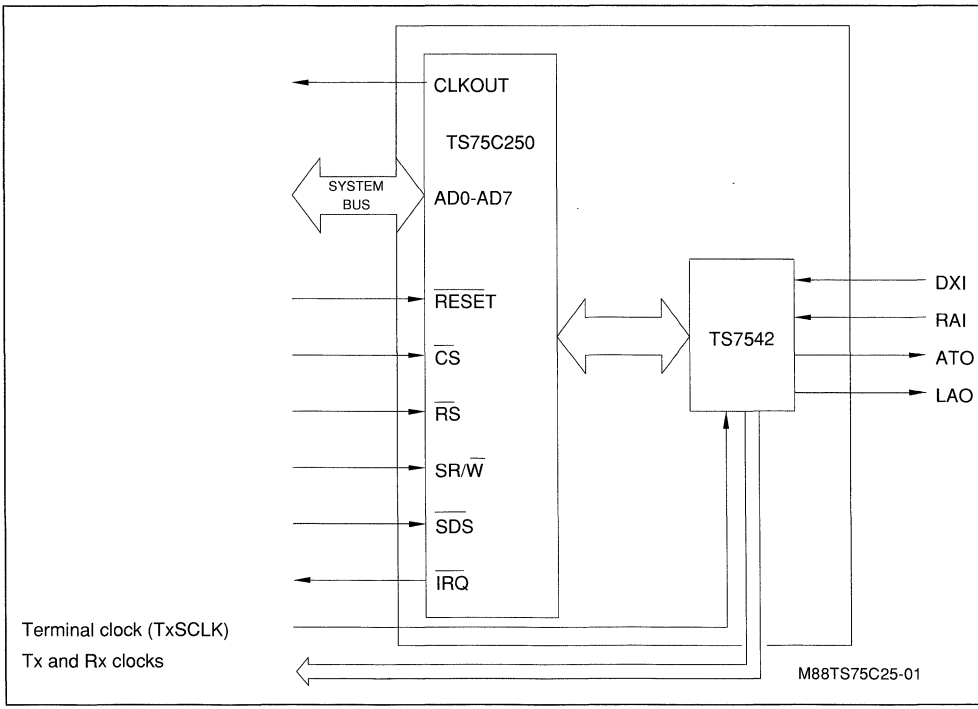
The TS7542 incorporates all the required programmable gain control and clock circuitry, and signal filtering (band-limiting, anti-aliasing and smoothing filters).

Interfacing the TS75C25 chip set to a control processor is very straightforward and requires no external interface circuitry.

The TS75C25 chip set along with a data access arrangement (DAA), a control processor and a V.24/RS232 interface and/or an UART, is particularly well-suited for high-performance modem.

The modem supervision is insured by a control processor which implements the handshake monitoring, the auto/manual answer and dialing modes, the test modes and fall back capability and the async/sync and sync/async conversion.

Figure 1 : TS75C25 Block Diagram.

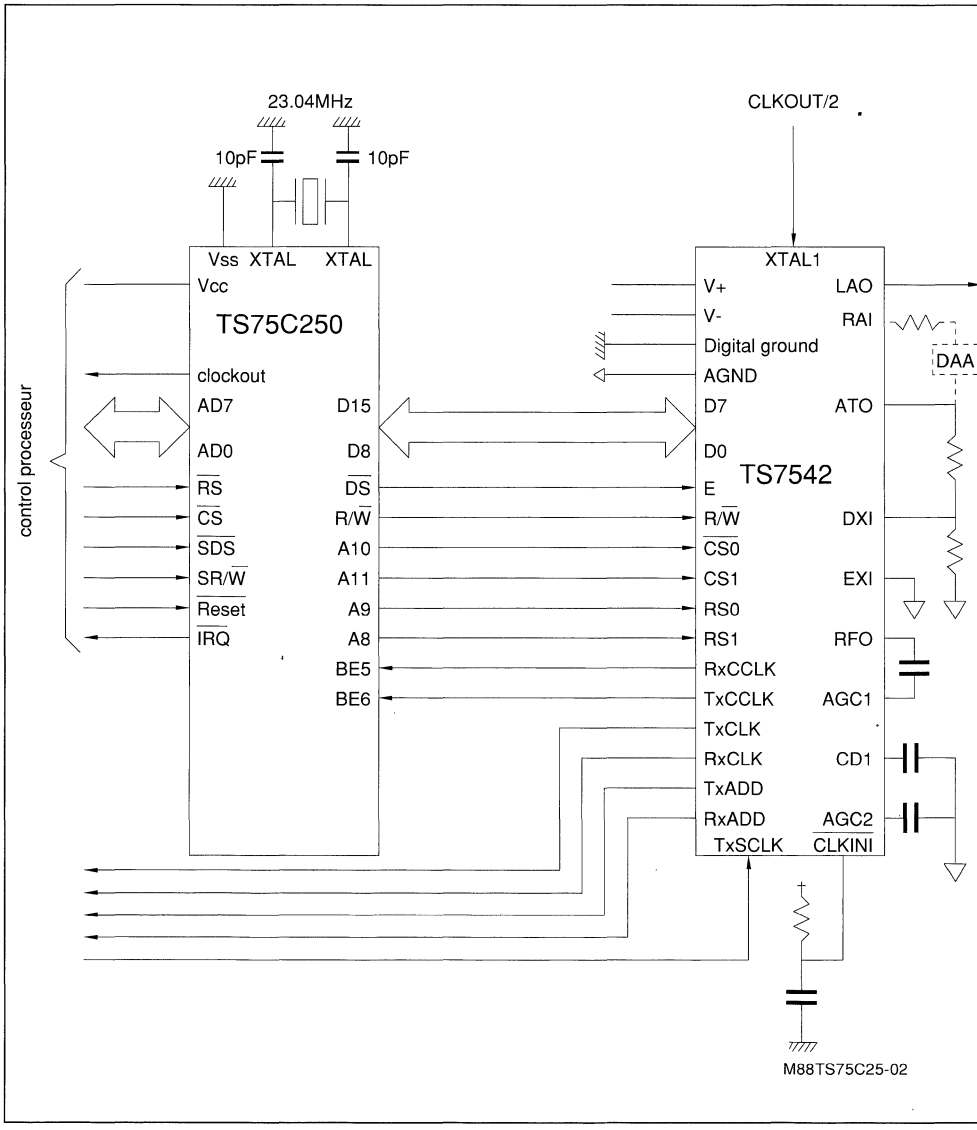


2.2. PROCESSOR AND MAFE CHIPS ARRANGEMENT

The TS75C25 is connected to the analog front end chip through its local bus where D8 through D15 are the 8-bit data bus and A8 through A11 are four address lines used to address directly the analog front end chip.

Data-Strobe ($\overline{DS}$) is used to synchronize the transfer of data. Read/write (R/$\overline{W}$) indicates the direction of data. Two Branch-on-External-Condition signals (BE5 to BE6) are connected to the different clock signals issued from the TS7542 clock generator part. They are used by the TS75C250 to perform its real-time task scheduling.

Figure 2 : Interconnections between the Analog Front End Chip and the Digital Signal Processor TS75C250.



2.3. OPERATION

2.3.1. ANALOG FRONT END DESCRIPTION. The TS7542 is a modem analog front end which performs the following functions controlled by the TS75C250 digital signal processor according to the selected modem standard.

Transmit Analog Part :

- 12-bit D/A converter synchronized with the sampling transmit clock
- Low-pass and smoothing continuous-time filters
- 0 to 22dB (or infinite) programmable attenuation

Receive analog Part :

- 12-bit A/D converter synchronized with the sampling receive clock.
- Band-pass programmable filter
- Back channel rejection filter
- Smoothing filter
- 0 to 46.5dB gain amplifier

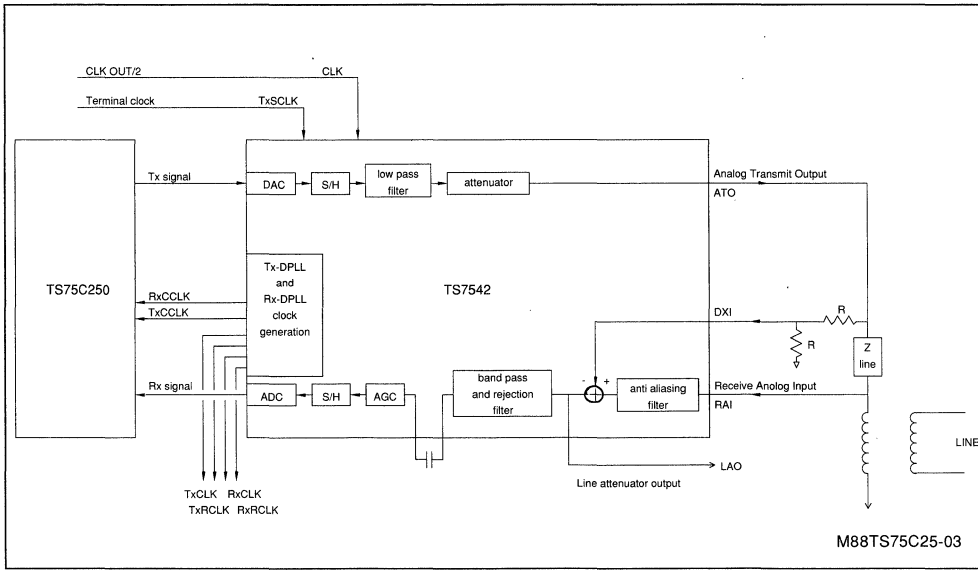
Clock Generation Part :

- Transmit time base with programmable synchronization on data terminal equipment clock or extracted receive clock.
- Programmable receive time base DPLL
- Programmable plesiochronous transmit and receive clocks (sampling, bit and additional clocks).

Loudspeaker Part :

- Loudspeaker with programmable level line output

Figure 3 : TS7542 Block Diagram.



2.3.2. OPERATING MODES. The modem implementation is fully compatible with different CCITT and BELL recommendations as listed in table 1. It may operate at different bit rates, from 75bps to 2400bps.

In case of switching from any mode to another, a reset must be applied to the TS75C250 reset pin, except during the V.22 bis handshaking (the V.22 bis and V.22/BELL 212 software modules implemented in the TS75C250 are compatible).

A DTMF tone generator is provided to output one of 16 standard dual tones coded by a combination of two frequencies. For specific applications where single tone is required, the DTMF generator provides the possibility to select either the high frequency or the low frequency of the standard dual tones.

A tone detector and a carrier detector respectively recognize the different answer tones (CCITT 2100Hz, BELL 2225Hz and Transpac 1650Hz) and call progress tones (300Hz to 700Hz), as well as the presence or the absence of the on-line carrier signal (both for PSTN and leased lines).

Table 1 : TS75C25 Operating Modes.

Recommendation	Bauds	BPS	Duplex	Answer	Orig	Modulation
V. 22 BIS	600	2400	Full	Yes	Yes	QAM (quadribit)
V. 22	600	1200	Full	Yes	Yes	DPSK (dibit)
BELL 212	600	1200	Full	Yes	Yes	DPSK (dibit)
V. 22	600	600	Full	Yes	Yes	DPSK (bit)
V. 21	300	300	Full	Yes	Yes	FSK
BELL 103	300	300	Full	Yes	Yes	FSK
V. 23	1200/75	75/1200	Full	Yes	Yes	FSK

2.3.3. TRANSMIT (fig. 4) : *V.22 bis, V.22 and BELL 212.* QAM or DPSK modulation is used to send four (V.22 bis) or two (V.22 and BELL 212) or one (V.22) bit(s) of information at 600 bauds modulation rate.

The scrambler can be bypassed, as user's option usually during the handshake procedure. After coding, a raised cosine filter (roll-off factor 0.75) performs pulse shaping and provides a 45dB rejection between the channels so as to comply with V.22 bis, V.22 and BELL 212 standard requirements. When required, a 1800Hz or 550Hz guard tone can be added to the transmitted signal.

- *V.23, V.21 and BELL 103*

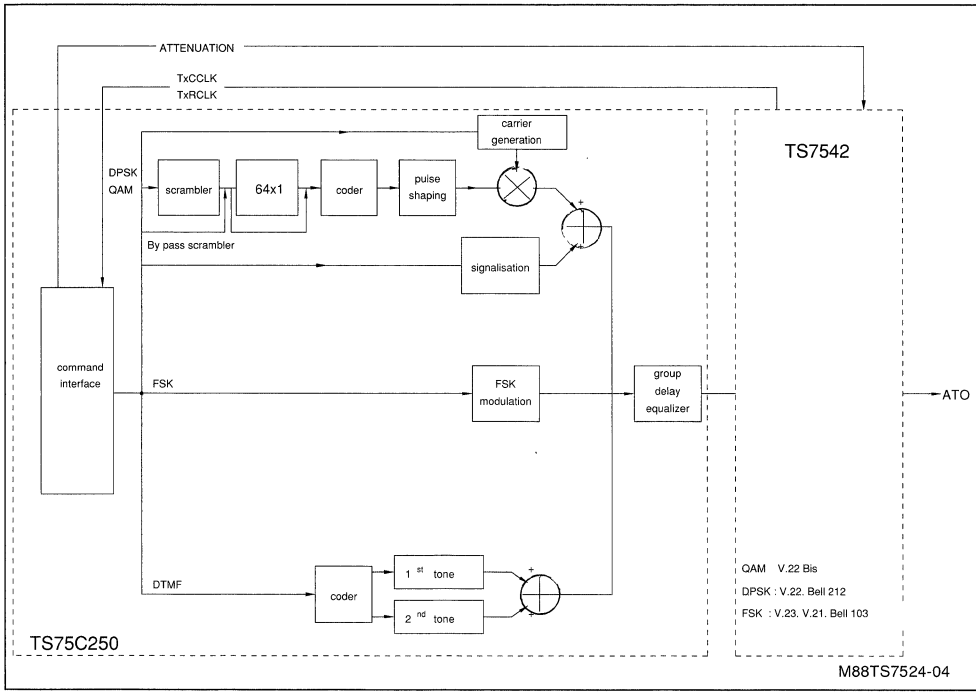
The FSK modulation is used to send one bit of information at 1200 or 75 baud (V.23) or 300 bauds (V.21 and Bell 103).

- *DTMF*

The DTMF generator outputs one of 16 standard dual tones synthetized by the TS75C250 and selected by a 4-bit binary value as described later. Each tone is coded by a combination of two frequencies. The DTMF generator may be programmed to generate one tone at a time.

The transmit attenuation level is programmable over a 23dB dynamic range by 1dB steps.

Figure 4 : TS75C25 Transmit Block Diagram.



2.3.4. RECEIVE (fig. 5) :

- *V.22 bis, V.22 and BELL 212.*

QAM or DPSK demodulation is used to receive four (V.22 bis) or two (V.22 and BELL 212) or one (V.22) bit(s) of information at 600 bauds.

- *V.23, V.21 and BELL 103*

The FSK demodulation is used to receive one bit of information at 1200 or 75 bauds (V.23) or 300 bauds (V.21 and BELL 103).

- *Tone Detection*

The TS75C25 recognizes the following tones :

- 2100Hz and 2225Hz answer tone detection
- 1650Hz V.21 Transpac answer tone detection
- 300 to 700Hz call progress tone detection

Adaptive equalization, DPLL and AGC compensate for line impaiments, frequency offset, group delay and amplitude distorsions.

Efficient rythm recovery algorithms provides accurate sampling on the receive signal with a variation up to $\pm 2.10^{-4}$.

Decoded data are provided in scrambled or descrambled format.

2.4. TS75C25 INTERFACE (fig. 6)

2.4.1. TS75C25 ANALOG INTERFACE. The transmit signal at the line interface (output ATO) is programmable over a 23dB dynamic range by 1dB steps through the TS75C250 mailbox.

The receive signal at the line interface (input RAI) can have a dynamic range from 0 to - 48dBm.

With a simple circuit using a minimum of external components, the TS75C25 can transmit with a level of - 12dBm on line and provide the adequate rejection of the transmit signal on the receive channel.

2.4.2. TS75C25 DIGITAL INTERFACE. The interface between the TS75C25 chip set and the control processor is managed by the TS75C250 via its system bus and internal mailbox. The mailbox allows the control processor to read/write three consecutive data-bytes through AD0-AD7 bus. The mailbox exchanges follows the protocol described in fig. 2.4.3.

The TS75C250 digital interface signals, and their definition are listed in table 2.

Figure 5 : TS75C25 : Receive Block Diagram.

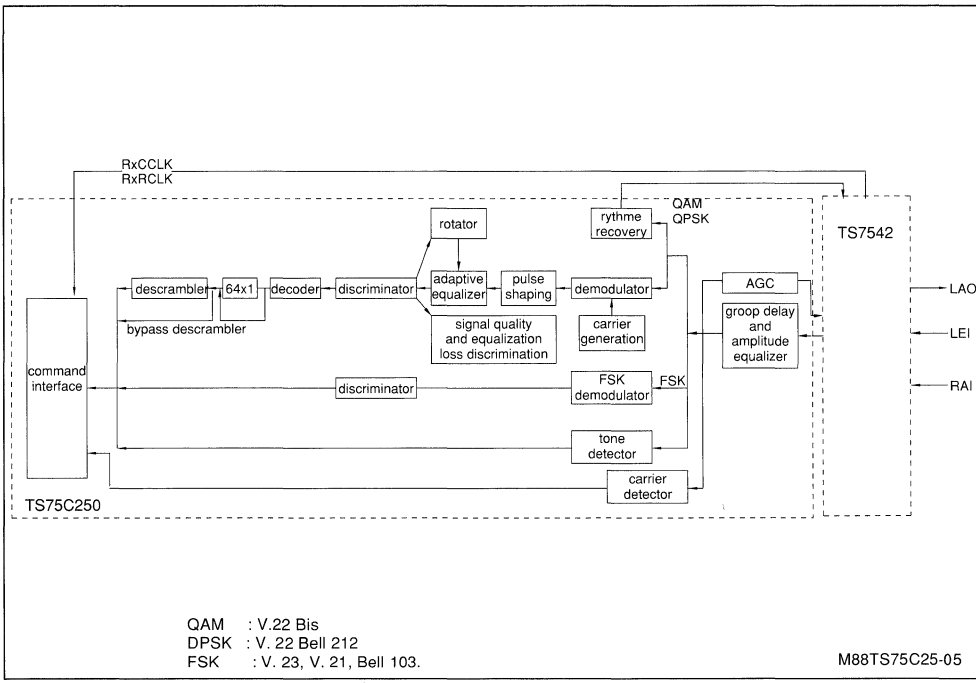
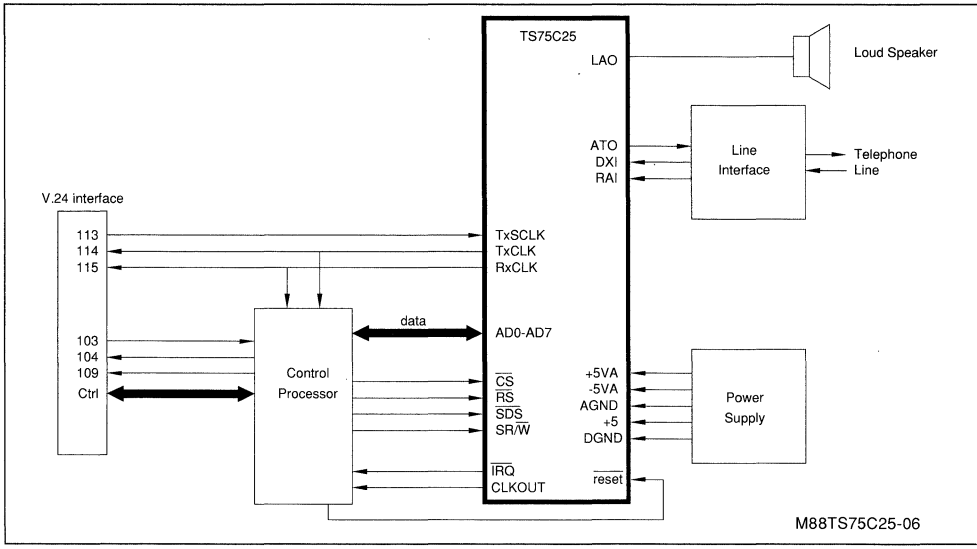


Table 2 : Digital Interface Signals.

Interface Signals	Input/output I/O	Signal Definition
AD0	I/O	Data-Bus (LSB)
AD1	I/O	Data-Bus
AD2	I/O	Data-Bus
AD3	I/O	Data-Bus
AD4	I/O	Data-Bus
AD5	I/O	Data-Bus
AD6	I/O	Data-Bus
AD7	I/O	Data-Bus (MSB)
$\overline{SR/W}$	I	Read/write Signal
$\overline{SDS}$	I	Data Strobe
$\overline{IRQ}$	O	Mailbox Handshake
$\overline{CS}$	I	TS75C250 Chip Select
$\overline{RS}$	I	Register Select
$\overline{Reset}$	I	TS75C250 Reset
TxCLK	O	Additional Transmit Clock
RxCLK	O	Additional Receive Clock
TxSCLK	I	Transmit Terminal Clock

* These additional clocks may be used for specific applications.

Figure 6 : Functional Interconnect Diagram.



2.4.3. MAILBOX DESCRIPTION. The TS75C250 requires the attention of the control processor at regular intervals in order to perform properly. The control processor must interact with the modem chip set in a timely manner to avoid improper operation.

To initialize communication exchanges between the TS75C25 and the control processor, the TS75C25 RESET pin must be maintained in its active (low) state during at least 870ns (5 clock cycles) by the microprocessor. At the end of reset, the TS75C250 gives the mailbox control to the processor.

It is also recommended to maintain the RESET in its active state until the exchanges can start.

Following a reset the status word read from the mailbox is not significant, and the content of the command word is ignored. So, the first mailbox exchange is a dummy exchange.

The mailbox located internally to the TS75C250 DSP contains 3-bytes input and 3-bytes output shift registers. The TS75C250 has an internal flag which indicates whether the TS75C250 or the control processor has access to the mailbox. The TS75C250 can relinquish its accessability to the mailbox by setting this internal flag, but it can no longer regain access to the mailbox as the flag is reset only after the control processor relinquishes its accessability to the mailbox.

The access protocol and system bus transfers are controlled by an internal I/O sequencer within the TS75C250 which operates as follows :

1/ The mailbox is made available to the control processor by the TS75C250 which drives the IRQ mailbox handshake signal to the active (low) state.

2/ The control processor detects IRQ active and dummy reads the mailbox by forcing the TS75C250 chip select (CS) and register select (RS) low along with the write signal (SR/W) high. The activated data strobe signal (SDS = 0) validates the above signals.

3/ The TS75C250 detects the dummy read of its mailbox via the control signals mentioned in step 2 and negates IRQ mailbox handshake signal after 1µS (at least 5 clock cycles).

4/ The control processor detects the negation of IRQ indicating that the TS75C250 mailbox is available for data transfers. The control processor reads three bytes (one status word) and then writes three bytes (one command word) in the mailbox. If the status word is a transmit status word is a transmit status word, then a transmit command word must be written into the mailbox. Else, a receive command word must be written into the mailbox.

5/ The control processor ends the exchange protocol performing a dummy read of the mailbox as in step 2 but with RS in the high state.

The TS75C250 then owns the mailbox and can make it available again to the control processor as in step 1.

3. USER INTERFACE

3.1. COMMAND AND STATUS WORDS

The TS75C25 chip set functionalities and status reporting are managed by the control processor through the TS75C250 mailbox, according to the protocol outlined earlier.

The command words are issued by the control processor and received by the TS75C250.

The status words are issued by the TS75C250 and delivered to the control processor.

The status words provide the status reporting.

Each command and status word of both the transmit and receive part comprises three bytes as described in the following sections.

The control processor must be able to handle :

- one mailbox transfer per transmit baud period and,
- one mailbox transfer per receive baud period
- these transfers are plesiochronous. (Tx and Rx clocks have the same nominal frequency but can shift of $\pm 1.10^{-4}$, so the phase relation between Tx and Rx is time varying).

3.2. TRANSMIT AND RECEIVE COMMAND WORDS

Both the transmit and receive command words are built on the same programming model, but have to be programmed completely independently.

3.2.1. TRANSMIT COMMAND WORD. The table 3 shows the transmit command word (three bytes) programmation and transmit functionalities.

The first byte of the transmit command word permits the choice of the DTMF mode or the selection of the requested CCITT (with or without guard tone) or BELL standards.

The second byte contains the transmit parameters information register.

The third byte is the transmit data register of DTMF tone selection register. In this byte is also included the transmit enable bit which instructs the TS75C25 to transmit (or not) data to the line.

To manage the TS75C25 in an efficient way, it is recommended to work with a table stored in the control processor memory space. This table will reflect the

Table 3 : Transmit Command Word Format.

<table>
<tr><th>BIT</th><th>First Byte</th><th>Second Byte</th><th colspan="5">Third Byte</th></tr>
<tr><td>0</td><td rowspan="4">Transmit Mode Selection
0000 : Modem Disabled
0001 : V.22 Bis
0010 : V.22 0011 : B212
0100 : V.23 0101 : V.21
0110 : Bell 103
0111 : D.T.M.F.</td><td rowspan="4">Transmit
Attenuation</td><td colspan="5">Transmit (0)</td></tr>
<tr><td>1</td><td>D0</td><td rowspan="2">DPSK</td><td rowspan="3">QAM</td><td rowspan="4">FSK</td><td rowspan="3">DTMF</td></tr>
<tr><td>2</td><td>D1</td></tr>
<tr><td>3</td><td>D2</td><td>0</td></tr>
<tr><td>4</td><td rowspan="2">Transmit Signalling
00 : Signalling Disabled
01 : 550Hz
11 : 1800Hz</td><td rowspan="2">D3</td><td rowspan="2">0</td></tr>
<tr><td>5</td><td>Scrambler (ON/$\overline{\text{OFF}}$)</td><td>D4</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>6</td><td>Reserved</td><td>64 x 1 (ON/$\overline{\text{OFF}}$)</td><td>D5</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>7</td><td>$\overline{\text{ANSW}}$/ORIG or DTMF[1]</td><td>V.22 Binary Rate Select
or DTMF[2]</td><td colspan="5">$\overline{\text{Transmit Enable}}$</td></tr>
</table>

Notes : All the "RESERVED" bits must be cleared to "0" by the user.
1. DTMF : Higher/lower tone selection.
2. DTMF : DUAL/single tone.

three bytes of the transmit command word and will be sent from the control processor to the TS75C25 at each transmit baud. In this table, the different fields could be programmed according to the CCITT or BELL standard needed taking into account the transmit parameters. Once the contents of the first and second byte have been determined for the whole transmission, only the transmit data field in the third byte has to be updated in the table. So, at each transmit baud, the TS75C250 will receive the complete three bytes, will check them and send the data.

FIRST BYTE :

Bit 3, 2, 1 and 0 : Transmit mode selection

These bits select the standard to use or the DTMF mode

0000	: Modem disabled
0001 to 0110	: Transmit mode selection
0111	: DTMF. In this mode, the number which may be dialed is given by the proper binary combination of bits 4, 3, 2 and 1 in the third byte. Refer to paragraph "DTMF mode" for detailed information.

Other bit codes are reserved.

Bit 5 and 4 : Transmit Signalling

These bits represent the tone to send regarding the requested functionalities.

00	: Signalling disabled
01 or 11	: Guard tone 550Hz or 1800Hz added to the modulated signal.
10	: Reserved

Bit 6 : Reserved

Bit 7 : $\overline{\text{ANSWER}}$/ORIGINATE or DTMF

This bit has two main functions. Its first function is to select the answer or originate mode. The second function is used in DTMF mode as explained in details in paragraph "DTMF mode".

In $\overline{\text{ANSWER}}$/ORIGINATE mode, the bit 7 cleared to zero selects the answer mode (transmit in high channel). The bit 7 set to one selects the originate mode (transmit in low channel).

SECOND BYTE :

Bit 4, 3, 2, 1, and 0 : Transmit attenuation

The transmit levels without attenuation at the transmit interface output (ATO) on 600Ω are as follows :

- in FSK modes (V.23, V.21 and BELL 103)
  - 0dBm
- in QAM (V.22 bis) and DPSK (V.22 and BELL 212) modes
  - 5dBm when transmission on low channel
  - 4dBm when transmission on high channel with guard tone composed by :
    - 5dBm (signal)
    - 12dBm (guard tone)
  - 5dBm when transmission on high channel without guard tone
- 4dBm in DTMF mode composed by
  - 5dBm (high frequency)
  - 7dBm (low frequency)

These are maximum levels which can be decreased by programming the transmit attenuation, with attenuation levels falling within 0dB (00000) and 23dB (10111) range, selectable in 1dB steps.

Selection within 11000 to 11111 correspond to an infinite attenuation.

At power-on, or after a reset applied on the reset pin of the TS75C250, an infinite attenuation is automatically programmed.

Bit 5 : Scrambler

The TS75C25 incorporates an auto-synchronized scrambler/descrambler in accordance with CCITT V.22 bis and V.22 and BELL 212 recommendation.

The scrambler is enabled (1) or disabled (0) by programming the bit 5.

When the scrambler is enabled, the input data is scrambled by dividing the data by a generating polynomial as defined in the V.22 bis and V.22 recommendations.

When the scrambler is disabled, the input data is routed around the scrambler in the transmit path.

Bit 6 : 64 x 1 Counter : The 64 x 1 counter is enabled (1) or disabled (0) by programming the bit 6.

When the 64 x 1 counter is enabled, if 64 consecutive bits "1" are outputed by the scrambler, the next scrambler input bit is one's complemented. When the 64 x 1 counter is disabled, the input data is routed around the 64 x 1 counter in the transmit path.

Bit 7 : V.22 binary rate selection or DTMF

This bit has two main functions. Its first function allows the possibility to select the lowest binary rate (V.22 at 600bps) when set to one, or the highest binary rate (V.22 at 1200bps) when cleared to zero.

The second function is used in DTMF mode as explained in details in paragraph "DTMF mode".

THIRD BYTE :

Bit 0 : Transmit

This bit indicates the nature of the command word. It must be cleared to zero by the control processor to indicate to the TS75C25 that the command word

is a transmit command word, and that the 3-bytes written in the mailbox contain transmit information.

Bit 6 Thru 1 : Transmitted data or DTMF tone selection. These bits have two main functions. The first function is to represent the data which will be sent according to the appropriate mode. The second function, used in DTMF mode, is to select by programming the bits 4, 3, 2, and 1 the generated tone which will be used to dial the proper number as shown in paragraph "DTMF mode" in table 5.

In QAM (V.22 bis) or DPSK (V.22 or BELL 212) modes, the bits 4, 3, 2, and 1 represent the data sent by the TS75C25. According to the selected mode, up to 4 bits will be used :

- In V.22 bis, each symbol (baud) is coded by 4 bits (quadribit)
- In V.22 at 1200bps and BELL 212 modes, each symbol is coded by 2 bits (dibit)
- In V.22 at 600bps, each symbol is coded by only one bit.

In these modes, the mailbox exchanges are executed at the rate of 600 exchanges per second.

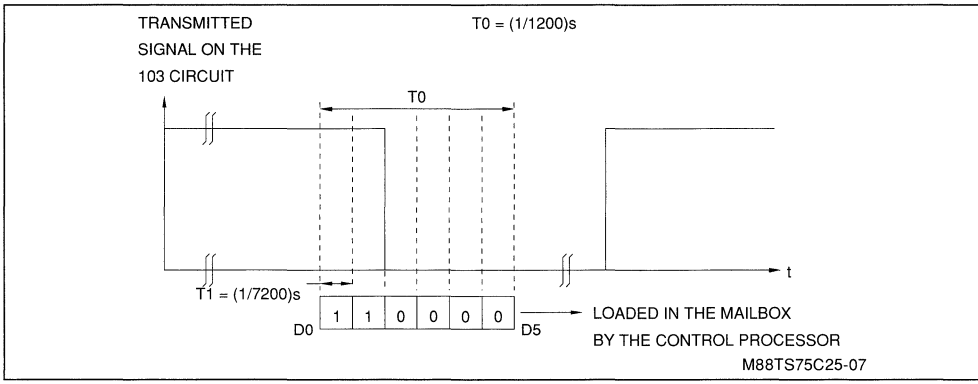
In FSK modes (V.21, V.23, and BELL 103) all the 6 bits (bit 6 thru 1) are used to represent the binary value of six samples of the transmitted signal. In these modes, the mailbox exchanges are executed at the rate of 1200 exchanges per second. Consequently, to perform a serial to parallel conversion the control processor has to sample the 103 circuit of the V.24/RS232 junction at 7.2kHz which is the sampling clock frequency (TxCCLK).

The bit 1 (which correspond to D0) is the first sample of the signal transmitted over the line as shown in figure 7.

Bit 7 : transmit enable

This bit low instructs the TS75C25 to send data.

Figure 7 : FSK Mode.



DTMF MODE

The DTMF generator outputs one of 16 standard dual-tones. For specific applications where single tone is required, the DTMF generator provides the possibility to select either the high frequency or the low frequency of the standard dual tones.

All the bytes used to program the DTMF mode and mentioned in this section are those of the transmit command word.

The DTMF mode is selected by programming bits 3 to 0 in the first byte.

Choosing the dual-tone mode, which is the normal operating mode, is done with bit 7 in the second byte cleared to zero. The DTMF generator then outputs one of the sixteen standard dual tones selected through bits 4 to 1 in the third byte as shown in table 5.

The single-tone mode is selected by setting to 1 the bit 7 in the second byte. This mode is used in specific cases where one frequency is to be generated. After one frequency pair is selected through bits 4 to 1 in the third byte as shown in table 5, the choice of the higher or lower frequency is made through bit 7 of the first byte. When bit 7 is set to 1 (respectively 0), the lower (respectively higher) frequency is generated.

In DTMF mode, the mailbox exchanges are executed at the rate of 1200 exchanges per second.

The programming of DTMF mode is summarized in table 4.

Table 4 : DTMF (dual or single tone) Programmation.

DTMF	First Byte Bits 3, 2, 1, 0		2nd Byte Bit 7	Third Byte Bits 4, 3, 2, 1
Dual-tone	0111		0	4-bit Binary Value Coding one of 16 Dual Tone
Single-tone	First Byte Bit 7	Bits 3, 2, 1, 0	2nd Byte Bit 7	Third Byte Bits 4, 3, 2, 1
High Frequency Selected	0	0111	1	4-bit Binary Value Coding one of 16 Dual Tone (high)
Low Frequency Selected	1	0111	1	4-bit Binary Value Coding one of 16 Dual Tone (low)

In DTMF mode the transmit levels at the analog transmit interface output (ATO) are respectively - 5dBm for the high group frequencies, and - 7dBm for the low group frequencies. These are maximum levels and can be decreased by programming the transmit attenuation in the second byte.

Table 5 : Tone Encoding.

Number to Dial	DTMF Code in Third Byte Generated Tones (Hz)						
	Bit4	Bit3	Bit2	Bit1	Low		High
0	0	0	0	0	941	&	1336
1	0	0	0	1	697	&	1209
2	0	0	1	0	697	&	1336
3	0	0	1	1	697	&	1477
4	0	1	0	0	770	&	1209
5	0	1	0	1	770	&	1336
6	0	1	1	0	770	&	1477
7	0	1	1	1	852	&	1209
8	1	0	0	0	852	&	1336
9	1	0	0	1	852	&	1477
A	1	0	1	0	697	&	1633
B	1	0	1	1	770	&	1633
C	1	1	0	0	852	&	1633
D	1	1	0	1	941	&	1633
*	1	1	1	0	941	&	1209
#	1	1	1	1	941	&	1477

The accuracy of the frequencies is $\pm 10^{-4}$.
The harmonic rejection level is at – 65dB.

ANSWER TONE GENERATION

The TS75C25 chip set may generate four different standard frequencies which represent the usual auto answer tones.

- 1300Hz : V.23 Automatic connection tone
- 1650Hz : V.21 Transpac specific answer tone
- 2100Hz : CCITT V.22 bis, V.22, V.23 and V.21 answer tone
- 2225Hz : BELL 212 and BELL 103 answer tone

For answer tone generation, mailbox exchanges are executed at the rate of 1200 exchanges/second.

Table 6 : Answer Tone Generation.

Tone	FSK Mode to Use	First Byte Bit 7	First Byte Bits 3, 2, 1, 0	Third Byte Bits 6, 5, 4, 3, 2, 1
1300Hz	V. 23 Answer	0	0100	111 111
1650Hz	V. 21 Answer	0	0101	111 111
2100Hz	V. 23 Answer	0	0100	000 000
2225Hz	B103 Answer	0	0110	111 111

3.2.2. RECEIVE COMMAND WORD. In the receive command word, the first byte permits the choice of the call progress and answer tone detection modes or the selection of the requested CCITT or BELL standards.

The second byte defines additional receive parameters.

The third byte informs the TS75C25 that the command word is a receive command word.

To manage the TS75C25 in an efficient way, it is recommended to work with a table stored in the control processor memory space. This table will reflect the three bytes of the receive command word and will be sent from the memory by the control processor to the TS75C25 at each receive baud. In this table, the different fields could be programmed according to the CCITT or BELL standard needed taking into account the receive parameters. At each receive baud, the TS75C250 will receive and processes the complete three bytes.

Table 7 : Receive Command Word Format.

BIT	First Byte	Second Byte	Third Byte
0	Receive Mode Selection	Line Output Level	Receive (1)
1	0000 : Modem Disabled 0001 : V.22 Bis		**Reserved**
2	0010 : V.22 0011 : B212 0100 : V.23 0101 : V.21	**Reserved**	
3	0110 : Bell 103 0111 : Call Progress Tone	Additional Clocks	
4	Answer Tone Selection		
5	Tx Synchronization	Descrambler (ON/$\overline{\text{OFF}}$)	
6	Carrier Detect Level	64 x 1 (ON/$\overline{\text{OFF}}$)	
7	$\overline{\text{Answer}}$/originate	V.22 Binary Rate Select	

Note : All the "RESERVED" bits must be cleared to "0" by the user.

FIRST BYTE :

Bit 3, 2, 1, and 0 : Receive mode selection

These bits select the standard to use or the call progress and answer tone detection mode.

0000 : Modem disabled

0001 to 0110 : Receive mode selection

0111 : Call progress and answer tone detection mode. In this mode the TS75C25 recognizes different tones as explained in paragraph "call progress and answer tone detection"

Other bit codes are reserved.

Bit 4 : Answer tone selection

This bit defines the answer tone to be detected. It selects either 1650Hz (Transpac) or 2100/2225Hz answer tone. When high, the detect answer tone is 1650Hz. When low, the detect answer tone is 2100/2225Hz.

Bit 5 : Tx synchronization signal programming

This bit allows synchronization of all transmit clocks on a selected source. When bit 5 is set to 1, all the TS75C25 transmit clocks (TxCLK, TxCCLK, TxRCLK) are synchronized on TxSCLK input (typically a terminal clock signal coming from the V.24/RS232 interface). This avoids overspeed and maintains a complete synchronization during the transmission. If there is no signal on TxSCLK coming from the terminal clock, the transmit clocks are free-running at their nominal frequencies.

When the bit 5 is set to 0, the TS75C25 transmit clocks are synchronized on the receive clocks. This possibility may be used for remote digital loopback.

Bit 6 : Carrier detection level

The TS75C25 can be used both on the public switched telephone network (PSTN) and with leased lines.

When the bit 6 is set to 0, the carrier detection threshold are :

– 43 and – 48dBm (PSTN)

When the bit 6 is set to 1, the carrier detection threshold are :

– 33 and – 38dBm (leased lines).

Bit 7 : $\overline{\text{Answer}}$ / originate

The bit 7 cleared to zero selects the answer mode (receive in low channel). The bit 7 set to one selects the originate mode (receive in high channel).

SECOND BYTE :

The signal level applied to the loud speaker will be as follow :

Bit 1 and 0 : Line Output Programmable Level.

B1 B0	Attenuation Level	Unit
00	∞	dB
01	0	dB
10	6	dB
11	12	dB

Bit 2 : Reserved.

Bit 4 and 3 : Additional Clocks

B4 B3	Clock Frequency	Unit
00	2400	Hz
01	1600	Hz
10	1200	Hz
11	600	Hz

Both Tx and Rx clocks are programmed with the same frequency according to B4 and B3. These clocks are not obligatory for the functionning of the TS75C25, but may be useful for specific application.

Bit 5 : Descrambler

The TS75C25 incorporates an auto-synchronized scrambler/descrambler in accordance with CCITT V.22 bis and V.22 and BELL 212 recommendation.

The descrambler is enabled when bit 5 is set to 1, or disabled when bit 5 is set to 0.

When the descrambler is enabled, the data stream is multiplied by the same polynomial that divided the data at the scrambler in the transmission path.

When the descrambler is disabled, the data stream is routed around the descrambler in the receive path.

Bit 6 : *64 x 1 Counter.* When the 64 x 1 counter is enabled, if 64 consecutive bits "1" are decoded, the next descrambler input bit is one's complemented. When the 64 x 1 counter is disabled, the output data is routed around the 64 x 1 counter in the receive part. The 64 x 1 counter is enabled when bit 6 is set to 1, or disabled when bit 6 is set to 0.

Bit 7 : V.22 binary rate select

This bit allows the possibility to select the lowest binary rate (V.22 at 600bps) when set to one, or the highest binary rate (V.22 at 1200bps) when set to zero.

THIRD BYTE :

Bit 0 : Receive

This bit indicates the nature of the command word. It must be set to one to indicate to the TS75C25 that the command word is a receive command word. This involves that the 3-bytes written in the mailbox by the control processor to the TS75C25 contain receive command information.

Bit 7 Thru 1 : Reserved (must be cleared to 0)

3.3. TRANSMIT AND RECEIVE STATUS WORD

The status words are issued by the TS75C250 and provide the status reporting to the control processor.

3.3.1. TRANSMIT STATUS WORD

Table 8 : Transmit Status Word Format.

BIT	First Byte	Second Byte	Third Byte
0	Transmit (0)	Reserved	Reserved
1	Reserved		
2			
3			
4			
5			
6			
7			

FIRST BYTE :

Bit 0 : Transmit

This bit when low informs the control processor that the status word issued by the TS75C25 is a transmit status word.

Bit 7 Thru 1 : Reserved

SECOND BYTE :

Bit 7 Thru 0 : Reserved

THIRD BYTE :

Bit 7 Thru 0 : Reserved

3.3.2. RECEIVE STATUS WORD

Table 9 : Receive Status Word Format.

BIT	First Byte	Second Byte	Third Byte
0	Receive (1)	**Reserved**	**Reserved**
1	D0 Data Before		D0 Data After Descr. (Q.A.M., D.P.S.K.) D0
2	D1 Descrambling		D1 D1
3	D2 (Q.A.M. , D.P.S.K.)		D2 D2 Data (F.S.K.)
4	D3	Equalization Status	D3 D3
5	**Reserved**	$\overline{\text{Signal Quality}}$	1 D4
6	S1 Sequence	$\overline{\text{Carrier Detect}}$	1 D5
7	S1 Sequence or Call Progress Tone Detection	**Reserved**	$\overline{\text{Answer Tone Detection}}$

Note : In QAM and DPSK modes, both for the data after and before descrambling, the unused bits are set to "1" by the TS75C25.

FIRST BYTE :

Bit 0 : Receive

This bit set to one by the TS75C25 indicates to the control processor that the current status word is a receive status word.

Bit 4, 3, 2, and 1 : Data before descrambling

Used only in QAM and DPSK modes, these four bits represent the data received before descrambling, i.e., after the demodulator and before the descrambler. Data is coded on four bits (D3, D2, D1, D0) in V.22 bis, on two bits (D1, D0) in V.22 at 1200bps and BELL 212, on only one bit (D0) in V.22 at 600bps. The unused bits are set to 1 by the TS75C25.

The mailbox exchange rate between the TS75C250 and the control processor is done at 600 exchanges per second. Both for QAM and DPSK modes, D0 (which correspond to the bit 1) is the first bit received.

Bit 5 : Reserved

Bit 7 and 6 : S1 handshake sequence (V.22 bis) mode

During the V.22 bis handshake sequence, these two bits indicate the presence or the absence of the "S1" sequence detected by the TS75C25. If the TS75C25 gives an alternance (at each baud period in reception) of values "10" and "01" on bit 7 and 6, the "S1" sequence is present in reception. Else, this means its absence.

Bit 7 : Call progress tone detection (call progress/answer tone mode).

This bit low indicates detection of energy in the band 300 - 700Hz with a detection threshold of - 43dBm. This bit high means there is no energy detected. (see paragraph call progress and answer tone detection).

SECOND BYTE :

Bits 3, 2, 1, and 0 : Reserved

Bit 4 : Equalization status

This bit will go high (1) in case of equalization loss (retrain sequence initialization or fallback mode).

Bit 5 : Signal quality

This bit will go high (1) when the quality of the received signal is too low for a good transmission.

Bit 6 : Carrier detect

This bit indicates the presence or the absence of the on-line signal as follows :

- This bit will go low (0) if the signal level is higher than –43dBm on PSTN or - 33dBm on leased lines
- This bit will go high (1) if the signal level is lower than –48dBm on PSTN or - 38dBm on leased lines.

The minimum hysteresis level is 2dB.

The information on the on-line signal may be used by the control processor to manage the 109 signal of the V.24 junction.

Bit 7 : Reserved

THIRD BYTE :

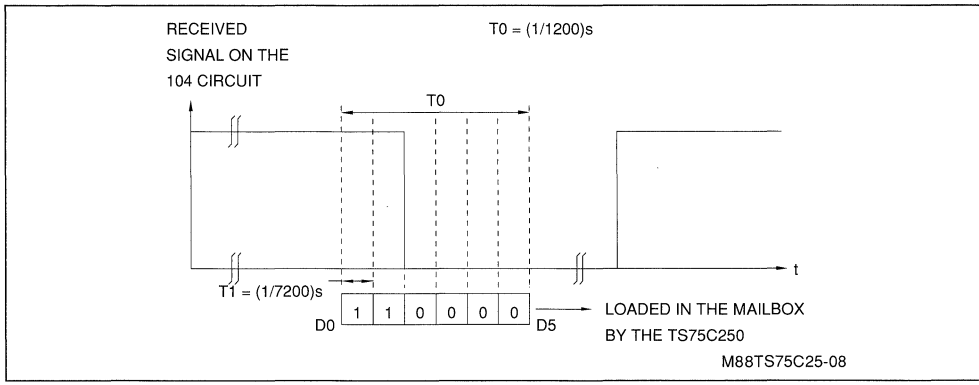
Bit 0 : Reserved

Bit 6 Thru 1 : Data received or data after descrambling.

These six bits contain the received data and have to be processed by the control processor according to the selected standards :

- In QAM and DPSK modes, bit 4 thru 1 represent the data received after descrambling, if the descrambler is enabled. Otherwise, they represent the data received without descrambling.
  The data is encoded on four bits (D3, D2, D1, D0) in V.22 bis, on two bits (D1, D0), in V.22 at 1200bps and Bell 212, on only one bit (D0) in V.22 at 600bps. The unused bits are set to one by the TS75C25.
  The mailbox exchange rate between the TS75C250 and the control processor is done at 600 exchanges per second. For both QAM and DPSK modes, D0 (which correspond to bit 1) is the first bit received.
- In FSK modes (V.21, V.23, and BELL 103) all the six bits are used to represent the digital value of six samples of the received signal. In these modes, the mailbox exchange must be executed at the rate of 1200 exchanges per second. Consequently to perform a parallel to serial conversion the control processor has to resend these bits on the 104 circuit of the V.24/RS232 junction at 7.2kHz.
  Bit 1 (which correspond to D0) is the first sample of the incoming signal received over the line as shown in figure 8.

Figure 8 : FSK Receive Mode.



Bit 7 : Answer tone detection

Used in answer tone detection mode, this bit when low (0), indicates the presence of the answer tone (CCITT 2100Hz, BELL 2225Hz or Transpac 1650Hz) sent by the far-end modem. When high (1), it means no detection of answer tone. Refer to paragraph "call progress and answer tone detection" for further details.

CALL PROGRESS AND ANSWER TONE DETECTION

The TS75C25 call progress detection part is activated by detection of energy in the 300 to 700Hz call progress tone bandwidth. The call progress mode must be selected in the first byte (bit 3 thru 0) of the receive command word.

Then the bit 7 of the first byte of the receive status word indicates to the control processor that the call progress tone is detected (bit 7 = 0) or not (Bit 7 = 1).

In answer tone mode, the TS75C25 may recognize three different standard frequencies which represent the usual answer tones sent by the far-end modem as described hereunder :

- 2100Hz : CCITT modes answer tone V.21 and V.23
- 2225Hz : BELL answer tones
- 1650Hz : Transpac V.21 answer tone

The answer tone mode must be selected in the first byte (bit 3 thru 0) of the receive command word and the answer tone selection (1650Hz or 2100/2225Hz) with the bit 4.

Then bit 7 in the third byte of the receive status word indicates to the control processor that the answer tone is detected (bit 7 = 0) or not (bit 7 = 1).

The table 10 shows the programmation of the receive command word, and the status reporting contained in the receive status word.

DTMF mode and transmit enable = 1 must be selected in the transmit command word.

Table 10 : Call Progress and Answer Tone Detection Programming Model.

	Receive Command Word		Receive Status Word	
	First Byte Bit 3, 2, 1, 0,	Bit 4	First Byte Bit 7	Third Byte Bit 7
Call Progress Mode and 2100/2225 Answer Tone	0111	0	1 No Call Progress Tone Detected 0 Presence of Call Progress Tone	0 2100/2225Hz Detected 1 No Detection
Call Progress Mode and 1650Hz Answer Tone	0111	1	1 No Call Progress Tone Detected 0 Presence of Call Progress Tone	0 1650HZ Detected 1 No Detection

4. ELECTRICAL SPECIFICATIONS

4.1. MAXIMUM RATINGS

TS75240

Symbol	Parameter	Value	Unit
V_{CC} *	Supply Voltage	– 0.3 to 7.0	V
V_{in} *	Input Voltage	– 0.3 to 7.0	V
T_A	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

* With respect to V_{SS}.

Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

TS7542

Symbol	Parameter	Value	Unit
	Supply Voltage between V^+ and AGND or DGND	– 0.3 to + 7	V
	Supply Voltage between V^- and AGND or DGND	– 7 to + 0.3	V
	Voltage between AGND and DGND	– 0.3 to + 0.3	V
	Digital Input Voltage	DGND – 0.3 to V_{CC}^+ + 0.3	V
	Digital Output Voltage	DGND – 0.3 to V_{CC}^+ + 0.3	V
	Digital Output Current	– 20 to + 20	mA
	Analog Input Voltage	V_{CC}^- – 0.3 to V_{CC}^+ + 0.3	V
	Analog Output Voltage	V_{CC}^- – 0.3 to V_{CC}^+ + 0.3	V
	Analog Output Current	– 10 to + 10	mA
	Power Dissipation	500	mW
T_{oper}	Operating Temperature Range	0 to + 70	°C
T_{stg}	Storage Temperature	– 65 to + 150	°C

4.2. DC ELECTRICAL CHARACTERISTICS DGND = AGND = 0 V

Digital Supply

V_{CC} = 5.0 V ± 10 %, V_{SS} = 0, T_A = 0 to + 70 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IL}	Input Low Voltage	– 0.3		0.8	V
V_{IH}	Input High Voltage	2.4		V_{CC}	V
I_{in}	Input Leakage Current	– 10		+ 10	µA
V_{OH}	Output High Voltage (I_{load} = – 300µA)	2.7			V
V_{OL}	Output Low Voltage (I_{load} = 2mA)			0.5	V
P_D	Total Power Dissipation		0.5		W
C_{in}	Input Capacitance		10		pF
I_{TSI}	Three State (off state) Input Current	– 20		+ 20	µA

Analog Supply

Symbol	Parameter	Min.	Typ.	Max.	Unit
V^+	Positive Power Supply	4.75		5.25	V
V^-	Negative Power Supply	– 5.25		– 4.75	V
I^+	Positive Supply Current (receive signal level 0dbm)			30	mA
I^-	Negative Supply Current (receive signal level 0dBm)	– 25			mA

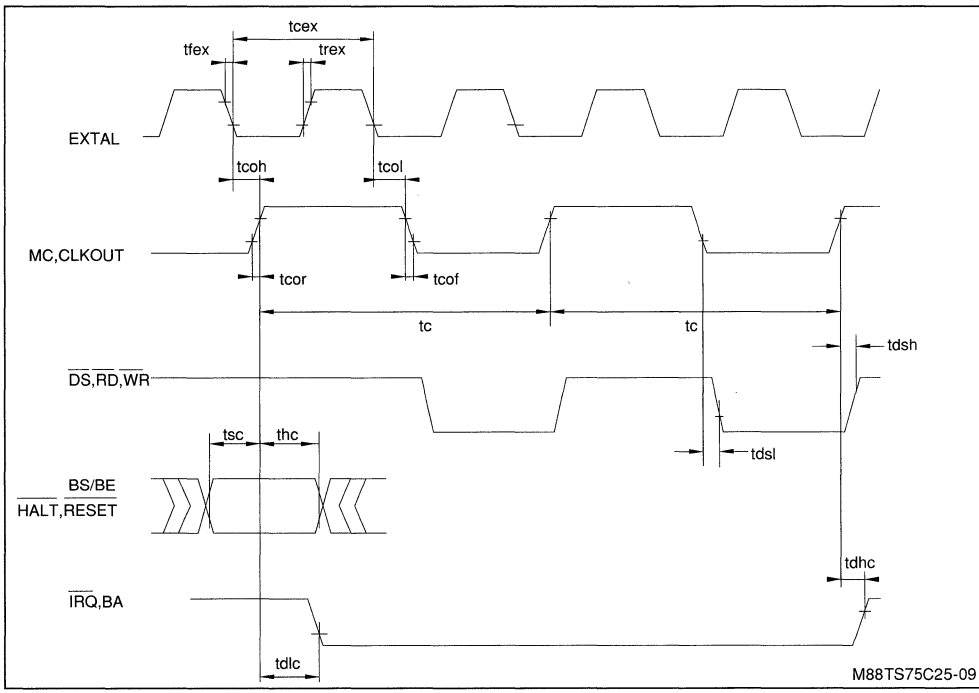
AC ELECTRICAL SPECIFICATIONS - CLOCK AND CONTROL PINS TIMING

$5V_{CC} = 5.0V \pm 10\%$, $T_A = 0$ to 70°C, see figure 9.1.)
OUTPUT LOAD = 50 pF . DC characteristics I load

REFERENCE LEVELS $V_{IL} = 0.8V$ $V_{IH} = 2.4V$
$V_{OL} = 0.8V$ $V_{OH} = 2.4V$ tr, tf ≤ 5ns for Input Signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
tcex	External Clock Cycle Time (tc = 2 x tcex)	50		200	ns
tcex	External Clock Cycle Time (tc = 4 x tcex)	25		100	ns
tfex	External Clock Fall Time			5	ns
trex	External Clock Rise Time			5	ns
tcoh	EXTAL to CLKOUT High Delay		25		ns
tcol	EXTAL to CLKOUT Low Delay		25		ns
tcor	CLKOUT Rise Time			10	ns
tcof	CLKOUT Fall Time			10	ns
tdsl	CLKOUT to $\overline{DS}$, $\overline{RD}$, $\overline{WR}$ Low		5		ns
tdsh	CLKOUT to $\overline{DS}$, $\overline{RD}$, $\overline{WR}$ High		5		ns
tsc	Control Input Set-up Time (BS/IT, BE, $\overline{Reset}$)	20			ns
thc	Control Input Hold Time (BS0, BS2, BE3, BE6, $\overline{Reset}$)	10			ns
tdlc	CLKOUT to Control Output Low ($\overline{RQ}$, BA)			30	ns
tdhc	CLKOUT to Control Output High (BA, $\overline{IRQ}$)			30	ns

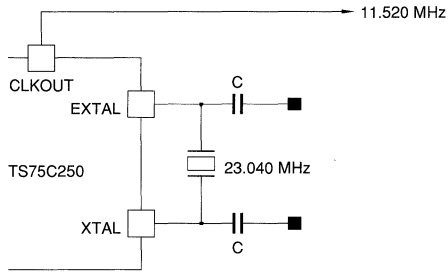
Figure 9 : Clock and Control Pins Timing.



INTERNAL CLOCK OPTION

A crystal oscillator can be connected across XTAL and EXTAL. The frequency of CLKOUT is half the crystal fundamental frequency, and can be used by the control processor.

Then the 5.76MHz required by the Analog Front End can be easily obtained.



M88TS75C25-10

Crystal nominal parameters :

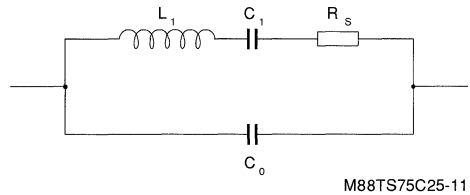
Parallel resonance fundamental mode - AT CUT

RS = 10Ω

C1 = 0.018pF

Co = 3.5pF

Q > 30K



M88TS75C25-11

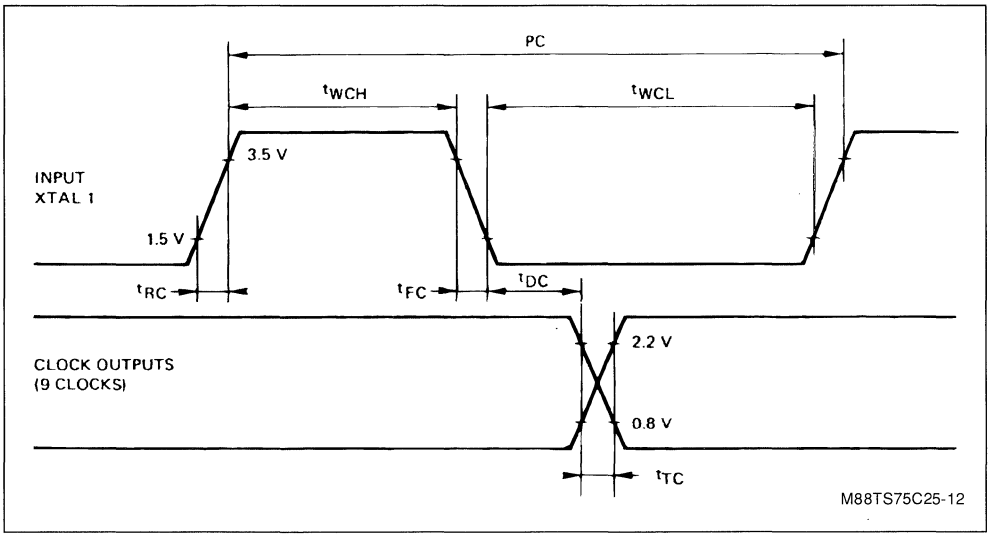
4.3.2. TS7542 : CLOCK GENERATOR

CLOCK WAVE FORMS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PC	Main Clock Period	XTAL1 Input	150	173.6		ns
t_{WCL}	Main Clock Low Level Width	XTAL1 Input	50			ns
t_{WCH}	Main Clock High Level Width	XTAL1 Input	50			ns
t_{RC}	Main Clock Rise Time	XTAL1 Input			50	ns
t_{FC}	Main Clock Fall Time	XTAL1 Input			50	ns
t_{DC}	Clock Output Delay Time	All Clock Outputs CL = 50pF			500	ns
t_{TC}	Clock Output Transition Time	All Clock Outputs CL = 50pF			100	ns

Unless otherwise noted, electrical characteristics are specified over the operating range. Typical values are given for V^+ = 5.0V and T_{amb} = 25°C.

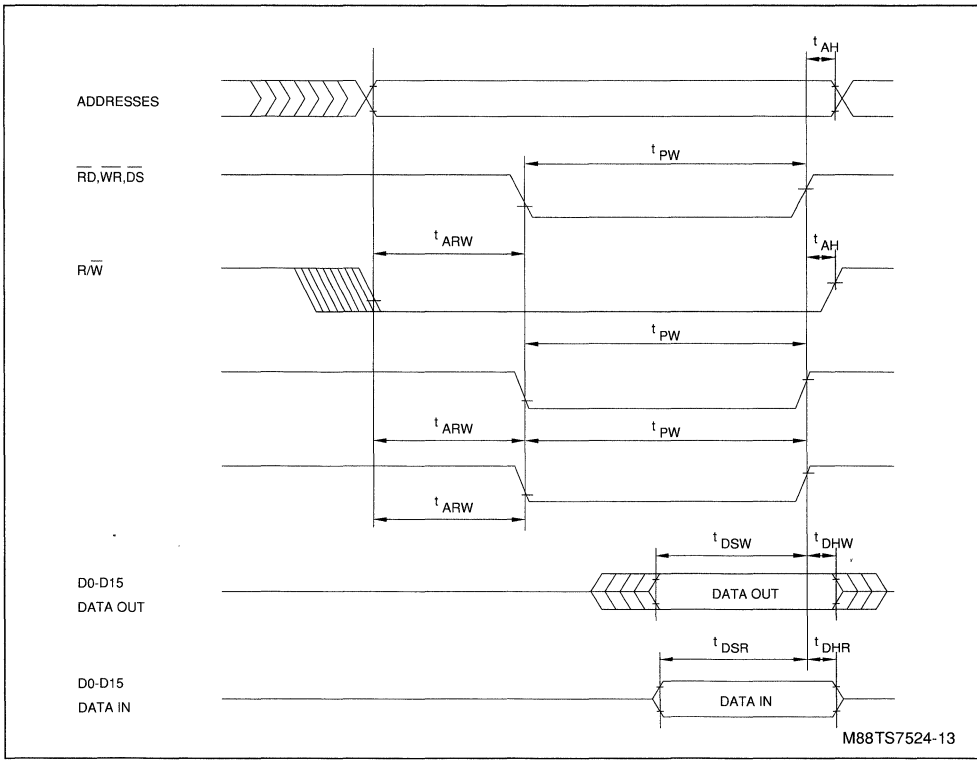
Figure 10 : Clock Generator.



4.3.3. LOCAL BUS TIMING (TS75C250 and TS7542)
(V_{CC} = 5.0V ± 10%, T_A = 0° to + 70°C, see figure 11)

Symbol	Parameter	Min.	Max.	Unit
t_{PW}	$\overline{RD}$, $\overline{WR}$, $\overline{AS}$ Pulse Width	1/2 tc – 10	1/2 tc	ns
t_{ARW}	Address Valid to $\overline{WR}$, $\overline{AS}$, $\overline{RD}$ Low	1/2 tc – 25		ns
t_{AH}	Address Hold Time	5		ns
t_{DSW}	Data Set-up Time, Write Cycle	1/2 tc – 25		ns
t_{DHW}	Data Hold Time, Write Cycle	5		ns
t_{DSR}	Data Set-up Time, Read Cycle	15		ns
t_{DHR}	Data Hold Time, Read Cycle	5		ns

Figure 11 : Local Bus Timing Diagram.



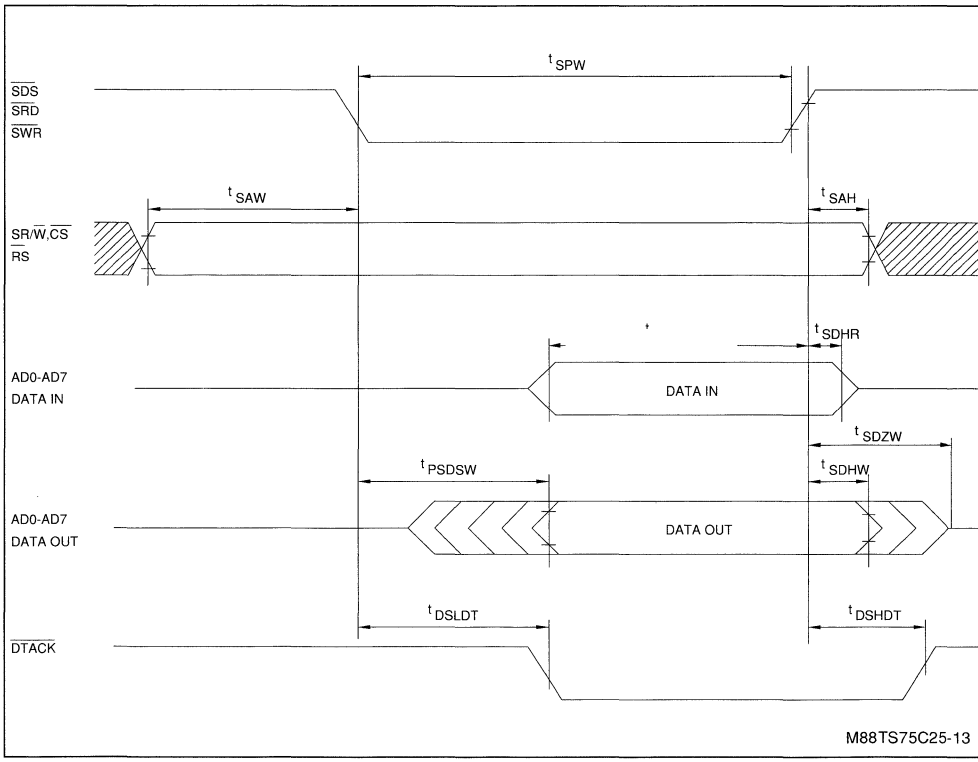
Note : In multicycle exchanges, tpw, tdsw, duration is extended by 1, 2 or 3 machine cycle lenghts (tc).

4.3.4. SYSTEM BUS TIMING (TS75C250 and control processor)
(V_{CC} = 5.0V ± 10%, T_A = 0° to + 70°C)

Symbol	Parameter	Min.	Max.	Unit
t_{SPW}	$\overline{SDS}$ Pulse Width	50		ns
t_{SAW}	SR/$\overline{W}$, $\overline{CS}$, $\overline{RS}$ Set-up Time	20		ns
t_{SAH}	SR/$\overline{W}$, $\overline{CS}$, $\overline{RS}$ Hold after $\overline{SDS}$ High	5		ns
t_{SDSR}	Data Set-up Time, Read Cycle	20		ns
t_{SDHR}	Data Hold Time, Read Cycle	5		ns
t_{SDSW}	Data Set-up Time, Write Cycle		30	ns
t_{SDHW}	Data Hold Time, Write Cycle	5	30	ns
t_{DSLDT}	$\overline{SDS}$ Low to $\overline{DTACK}$ Low		30	ns
t_{DSHDT}	$\overline{SDS}$ High to $\overline{DTACK}$ High*		40	ns

* DTACK is an open drain output test load include R_L = 820 Ω at V_{CC}.

Figure 12 : System Bus Timing Diagram.



4.3.5. DAA INTERFACE (DAA and TS7542)

Analog Transmit Output (ATO)
$V^+ = 5V \pm 5\%$, $0°C \leq T_{amb} \leq +70°C$ $V^- = -5V \pm 5\%$, $0°C \leq T_{amb} \leq +70°C$
(unless otherwise specified)

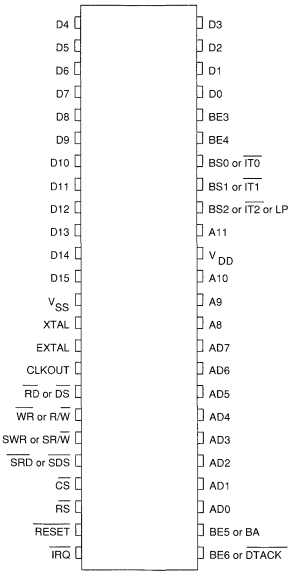
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OS}	Output DC Offset	– 250		+ 250	mV
C_L	Load Capacitance			50	pF
R_L	Load Resistance	1.2			kΩ
V_{out}	Output Voltage Swing ($R_L > 1.2k\Omega$ $C_L < 50pF$)	– 2.5		+ 2.5	V
R_{out}	Output Resistance (read cycle)			5	Ω

Receive Analog Input (RAI).

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{in}	Input Voltage	– 2.5		+ 2.5	V
I_{in}	Input Current (write cycle)	– 1		+ 1	µA

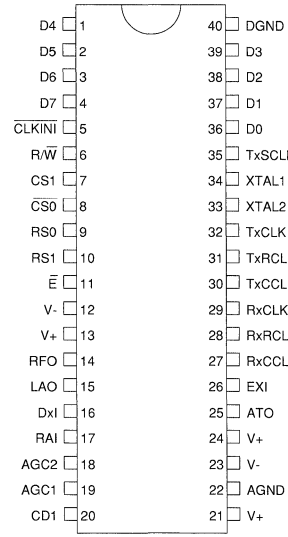
5. PIN CONNECTIONS

TS75C250



M88TS75C25 -15

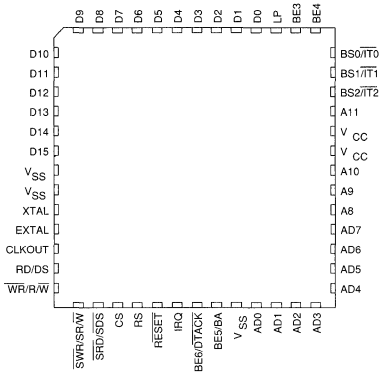
TS7542



M88TS75C25-16

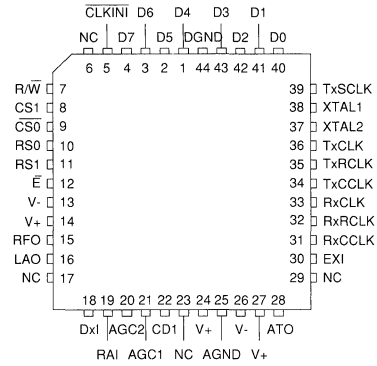
PIN CONNECTIONS (continued)

TS75C250



M88TS75C25-17

TS7542



M88TS75C25-18

TS75C250

TS7542 Interface

Name	Pin	Function	Description
D0 thru D15	I/O	Local Data Bus	Only D8 thru D15 lines are used for data transfer between the TS75C250 and TS7542. D0 thru D7 are not used and are left unconnected.
A8 thru A11	O	Local Address Bus	Address Lines to the TS7542
$\overline{DS}$	O	$\overline{Data\ Strobe}$	This signal synchronizes the transfer between the TS75C250 and the TS7542.
R/$\overline{W}$	O	Read/$\overline{Write}$	Indicates the current bus cycle state.
CLKOUT	O	Clock Output	This signal generated by the TS75240 is at half the frequency of the crystal. It can be divided by 2 to provide the 5.76MHz clock for the TS7542.
BE3 thru BE6	I	Receive and Transmit Clocks	These two inputs are connected to the receive and transmit clocks generated by the TS7542.

TS75C250

System Interface.

Name	Pin	Function	Description
AD0 thru AD7	I/O	System Data Bus	These bi-directional lines are used for data transfer between the TS75C250 mailbox and a control processor.
$\overline{CS}$	I	Chip Select	This active low input is asserted when the TS75C250 is to be accessed by the control processor.
$\overline{RS}$	I	Register Select	This signal is used with $\overline{CS}$ to control the data transfer between the control processor and the TS75C250 mailbox.
$\overline{SDS}$	I	System Data Strobe	Synchronizes the transfer on the system bus.
SR/$\overline{W}$	I	System Read/Write	Indicates the current system bus cycle state.
$\overline{IRQ}$	O	Interrupt Request	Handshake signal sent to the master to gain access to the mailbox.

Others Pins.

Name	Pin	Function	Description
BS0 thru BS2	I	Branch on State	These three inputs are not used and must be grounded.
EXTAL	I	Clock	Crystal Input for Internal Oscillator or Input Pin for External Oscillator.
XTAL	I	Clock	Together with EXTAL this pin is used for the external 23.040MHz crystal.
V_{CC}	Supply	Power Supply	
V_{SS}	Supply	Ground	
$\overline{RESET}$	I	Reset	
BE3 thru BE4	I	Branch on Edge	These two inputs are not used and must be grounded.

PIN DESCRIPTION TS7542

N°	Name	Description
1-4	D4-D7	Bidirectional Data Bus.
5	$\overline{\text{CLKINI}}$	Clock Initialization Input. Must be tied to V^+ during normal operation.
6	R/W	Read/Write Selection Input. This input indicates whether the current bus cycle is a read (high) or write (low) cycle.
7-8	CS1-$\overline{\text{CS0}}$	Chip Select Input. The chip is selected when $\overline{\text{CS0}}$ = 0 and CS1= 1.
9-10	RS0-RS1	Register Select Input. Select the register involved in a read or write operation.
11	$\overline{\text{E}}$	Enable Input. Enables Selection Inputs Active on a low level for read operation. Active on a positive-going edge for write operation.
12	V^-	Negative Supply Voltage. $V^- = -5V \pm 5\%$
13	V^+	Positive Supply Voltage. $V^+ = +5V \pm 5\%$
14	RFO	Receive Filter Analog Output. Designed to be connected to AGC1 input through a 1 µF non polarized capacitor.
15	LAO	Line Attenuator Output. Duplexer analog output usefull for line monitoring during call progress.
16	DxI	Duplexer Input. Analog input subtracted from the receive anti-aliasing filter output to implement duplexer function.
17	RAI	Receive Analog Input. Analog input tied to the transmission line.
18	AGC2	This pin must be connected to the analog ground through a 1 µF non polarized capacitor, in order to cancel the offset voltage of the AGC amplifier.
19	AGC1	Analog input of the AGC amplifier and of the carrier level detector.
20	CD1	This pin must be connected to the analog ground through a 1µF non polarized capacitor, in order to remove the offset voltage of the carrier level detector amplifier.
21	V^+	Positive Power Supply Voltage
22	AGND	Analog Ground. All analog signals are referenced to this pin.
23	V^-	Negative Supply Voltage
24	V^+	Positive Supply Voltage
25	ATO	Analog Transmit Output. Capable of driving 1200Ω load with 5V peak to peak amplitude.
26	EXI	External Transmit Input. Can be programmmed to be connected to the transmit filter or to the transmit attenuator input.
27	RxCCLK	Receive Conversion Clock Output
28	RxRCLK	Receive Baud Rate Clock Output
29	RxCLK	Receive Bit Rate Clock Output
30	TxCCLK	Transmit Conversion Clock Output
31	TxRCLK	Transmit Baud Rate Clock Output
32	TxCLK	Transmit Bit Rate Clock Output
33	XTAL2	Crystal Oscillator Output. Nominal Frequency = 5.76MHz
34	XTAL1	Crystal Oscillator or External Master Clock Input
35	TxSCLK	Transmit Synchronization Clock Input. Can be connected to an external terminal clock to phase lock the internal transmit clocks. When this pin is tied to a permanent logical level the transmit DPLL free-rises or can be phase locked on the receive clock system.
36-39	D0-D23	Bidirectional Data Bus.
40	DGND	Digital Ground. All digital signals are referenced to this wire.

ORDERING INFORMATION

The TS75C25 corresponds to two different components which must be ordered separately.

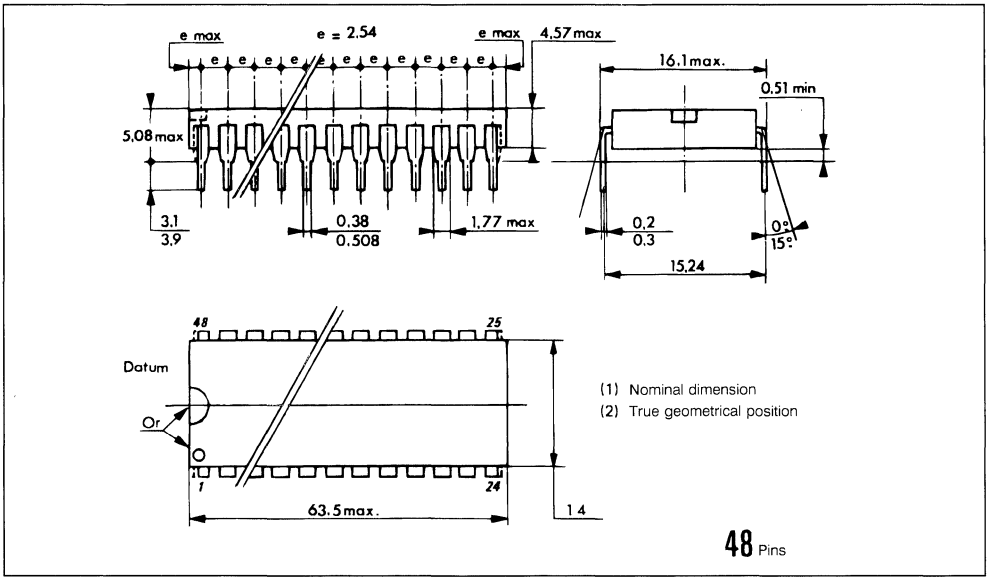
Furthermore, a stand-alone evaluation board is available for a fast characterization improvement of the TS75C25 in a real application.

Part Number	Temp Range	Package	Device
TS75C250CP	0 °C to 70 °C	DIP-48	V. 22Bis Masked DSP
TS7542CP	0 °C to 70 °C	DIP-40	Analog Front End
TS75C250CFN	0 °C to 70 °C	PLCC-52	V. 22Bis Masked DSP
TS7542CFN	0 °C to 70 °C	PLCC-44	Analog Frond End

7. PACKAGE MECHANICAL DATA

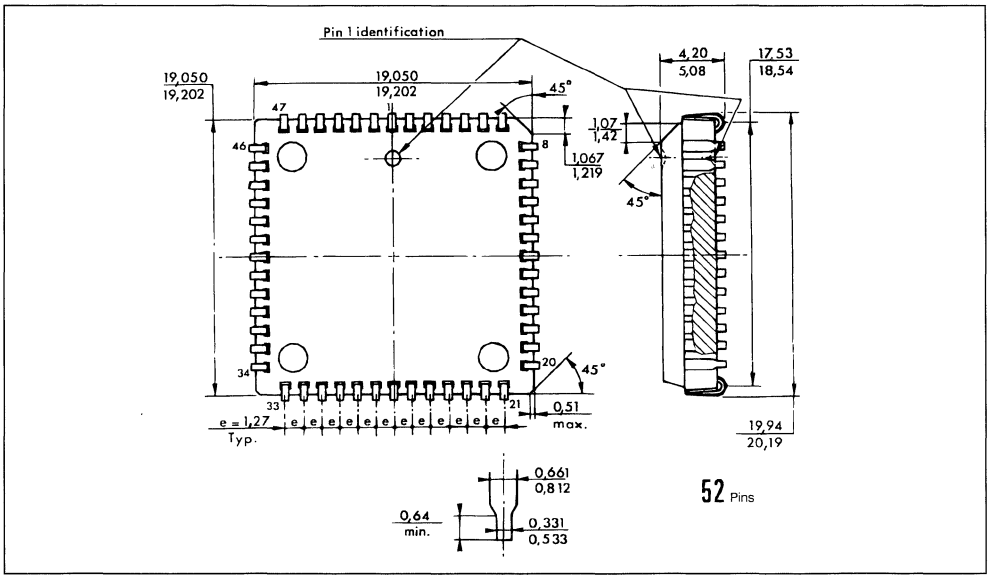
TS75C250

48 Pins – Plastic Dip.



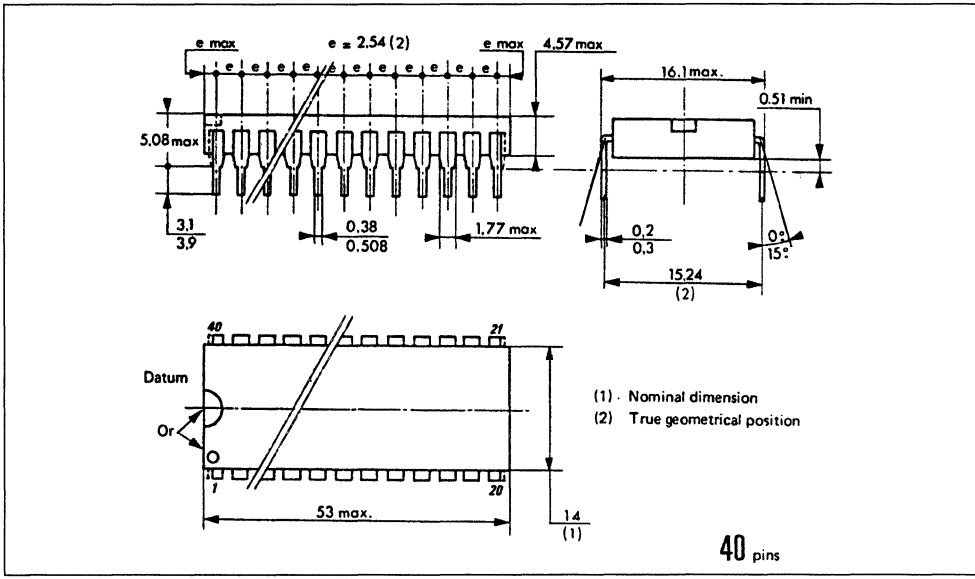
TS75C250

52 Pins – Plastic Leaded Chip Carrier.



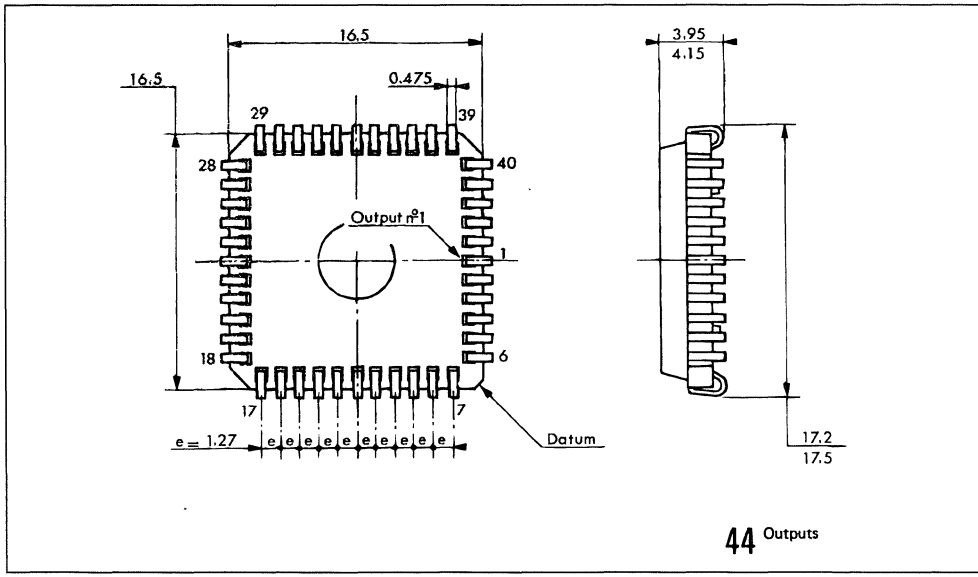
TS7542

40 Pins – Plastic Dip.



TS7542

44 Pins – Plastic Leadless Chip Carrier



ELECTRICAL CONSIDERATIONS

To avoid possible high frequency problems, the following precautions should be considered for PC board layout design :

- A ground plane on the component side connected to analog ground of the TS7542
- Analog and Digital ground tracks corresponding to different signals, e.g. clocks, input signals, references,... should be adequately separated and terminated at a single point.
- Optimal distribution of power supplies and ground links using star-connection
- Adequate decoupling capacitor mounted as close as possible to each device, and connected to analog ground
- DSP and MAFE power supplies should be separated

APPENDIX A

TRANSMIT/RECEIVE COMMAND WORDS

Transmit Command Word

BIT	First Byte	Second Byte	Third Byte				
0	Transmit Mode Selection	Transmit Attenuation	Transmit (0)				
1	0000 : Modem Disabled 0001 : V.22 Bis		D0	DPSK	QAM	FSK	DTMF
2	0010 : V.22 0011 : B212 0100 : V.23 0101 : V.21		D1				
3	0110 : Bell 103 0111 : D.T.M.F.		D2	0			
4	Transmit Signalling 00 : Signalling Disabled		D3	0			
5	01 : 550Hz 11 : 1800Hz	Scrambler (ON/$\overline{OFF}$)	D4	0	0		0
6	**Reserved**	64 x 1(ON/$\overline{OFF}$)	D5	0	0		0
7	$\overline{ANSW}$/ORIG or DTMF[1]	V.22 Binary Rate Select or DTMF[2]	$\overline{Transmit\ Enable}$				

Notes : All the "RESERVED" bits must be cleared to "0" by the user.
1 : DTMF : Higher/lower tone selection.
2 : DTMF : DUAL/single tone.

Receive Command Word

BIT	First Byte	Second Byte	Third Byte
0	Receive Mode Selection	Line output Level	Receive (1)
1	0000 : Modem Disabled 0001 : V.22 Bis		**Reserved**
2	0010 : V.22 0011 : B212 0100 : V.23 0101 : V.21	**Reserved**	
3	0110 : Bell 103 0111 : Call Progress Tone	Additional Clocks	
4	Answer Tone Selection		
5	Tx Synchronization	Descrambler (ON/$\overline{OFF}$)	
6	Carrier Detect Level	64 x 1 (ON/$\overline{OFF}$)	
7	$\overline{Answer}$/originate	V.22 Binary Rate Select	

Note : All the "RESERVED" bits must be cleared to "0" by the user.

APPENDIX B

TRANSMIT/RECEIVE STATUS WORDS

TRANSMIT STATUS WORD FORMAT

BIT	First Byte	Second Byte	Third Byte
0	Transmit (0)	**Reserved**	**Reserved**
1	**Reserved**		
2			
3			
4			
5			
6			
7			

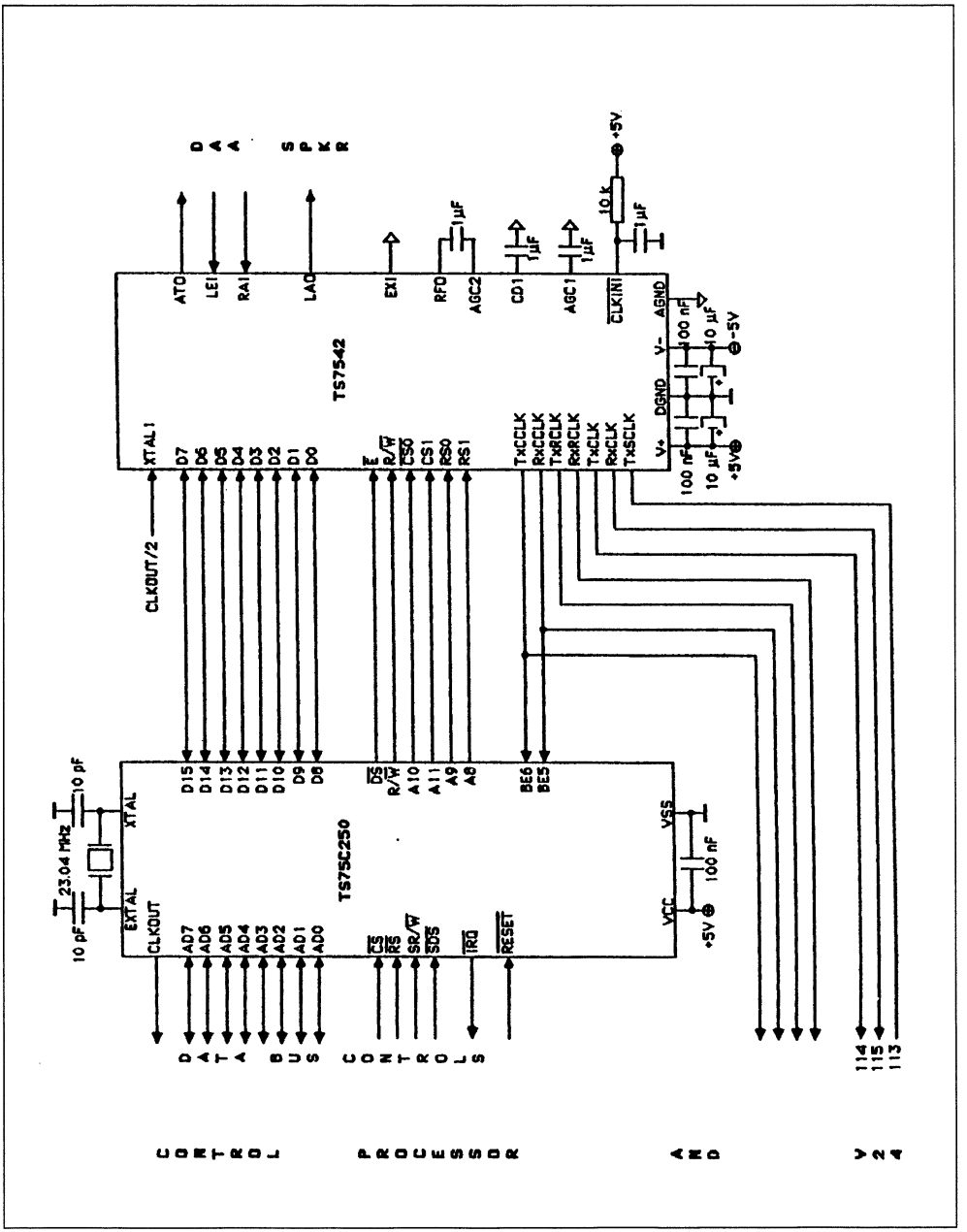
RECEIVE STATUS WORD FORMAT

BIT	First Byte		Second Byte	Third Byte			
0	Receive (1)		**Reserved**	**Reserved**			
1	D0	Data Before Descrambling (Q.A.M. , D.P.S.K.)		D0	Data After Descr. (Q.A.M., D.P.S.K.)	D0	Data (F.S.K.)
2	D1			D1		D1	
3	D2			D2		D2	
4	D3		Equalization Status	D3		D3	
5	**Reserved**		$\overline{\text{Signal Quality}}$	1		D4	
6	S1 Sequence		$\overline{\text{Carrier Detect}}$	1		D5	
7	$\overline{\text{S1 Sequence or Call Progress Tone Detection}}$		**Reserved**	$\overline{\text{Answer Tone Detection}}$			

Note : In QAM and DPSK modes, both for the data after and before descrambling, the unused bits are set to "1" by the TS75C25.

APPENDIX C

TS75C25 CHIP SET



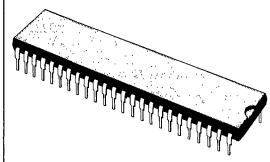
SGS-THOMSON MICROELECTRONICS

TS75C32

V.32, V.22BIS, V.22, V.23, V.21, BELL212A, BELL103 MODEM CHIP SET

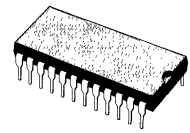
ADVANCE DATA

- CCITT V.32, V22bis, V.22, V.21,V.23, Bell 212A, Bell 103 COMPATIBLE MODEM CHIP SET
- INTEGRATED IMPLEMENTATION ON THREE DSP AND THREE MAFE CHIPS
- FULL DUPLEX OPERATION FROM 9600 TO 300 BPS
- FULL IMPLEMENTATION OF THE V.32 AND V.22BIS HANDSHAKE
- DYNAMIC RANGE : 43 dB
- TWO SATELLITE HOPS AND FREQUENCY OFFSET CAPABILITIES (10 Hz) FOR THE FAR END ECHO CANCELLER IN V.32 MODE
- TRELLIS ENCODING AND VITERBI DECODING
- 12.5 % ROLL-OFF RAISED COSINE TRANSMITTER PULSE SHAPING
- HIGH PERFORMANCE PASSBAND FRACTIONALLY SPACED ADAPTIVE EQUALIZER
- SIGNAL QUALITY MONITORING
- PARALLEL INTERFACE TO STANDARD MICROPROCESSORS
- BIT RATE DATA CLOCKS PROVIDED FOR SYNCHRONOUS DATA TRANSFER
- FULL DIAGNOSTIC CAPABILITY
- DTMF GENERATION
- CALL PROGRESS TONE DETECTION
- SOFTWARE LICENSE AND DEVELOPMENT TOOLS AVAILABLE FOR EASY CUSTOMIZATION
- TOTAL POWER CONSUMPTION BELOW 2W

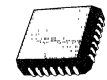


P
DIP48
(Plastic Package)
TS75C320/1/2

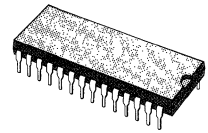
FN
PLCC52
(Plastic Leaded Chip Carrier)
TS75C320/1/2



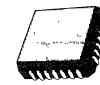
P
DIP24
(Plastic Package)
TS68950



FN
PLCC28
(Plastic Leaded Chip Carrier)
TS68950



P
DIP28
(Plastic Package)
TS68951/52



FN
PLCC28
(Plastic Leaded Chip Carrier)
TS68951/52

(Ordering Information at the end of the datasheet)

DESCRIPTION

The SGS-THOMSON Microelectronics TS75C32 chip set is a highly integrated modem engine, which can operate in full duplex from 9600 to 300 bps. The modem hardware consists of three analog front end (MAFE) chips, three DSP processor chips and additional memory chips.

The three SGS-THOMSON analog front end chips (TS68950/1/2) are the transmit interface, the receive interface and the clock generator respectively.

The modem signal processing functions are implemented on three ST18930 programmable digital signal processors.

TABLE OF CONTENTS

TABLE OF APPENDICES

1. PIN DESCRIPTION

1.1. SYSTEM INTERFACE

TS75C321 (DSP#1 Transmitter and Handshake)

Pin Name	Type	Signal Name	Description
AD0.AD7	I/O	D0H.D7H	System Data Bus : these lines are used for data transfer between the TS75C32 mailbox and the host processor.
$\overline{CS}$	I	CSL	Chip Select : this input is asserted when the TS75C32 is to be accessed by the host processor.
$\overline{RS}$	I	RSL	Register Select : this signal is used to control the data transfers between the host processor and the TS75C32 mailbox.
$\overline{SDS}$	I	DSL	System Data Strobe : synchronizes the transfer between the TS75C32 mailbox and the host processor.
SR/$\overline{W}$	I	RWL	System Read/Write : control signal for the TS75C32 mailbox operation.
$\overline{IRQ}$	O	INTL	Interrupt Request : signal sent to the host processor to access the TS75C32 mailbox.
$\overline{RESET}$	I	RSTL1	Master Reset of DSP#1

1.2. ANALOG INTERFACE

TS68950 (Analog Front End Transmitter)

Pin Name	Type	Signal Name	Description
ATO	O	ATO	Analog Transmit Output

TS68951 (Analog Front End Receiver)

Pin Name	Type	Signal Name	Description
RAI	I	RAI	Receive Analog Input
LEI	I	LEI	Local Echo Input. Must be grounded.

1.3. CLOCK INTERFACE

TS68952 (Clock Generator)

Pin Name	Type	Signal Name	Description
TxCLK	O	TxCLK	Transmit Bit Clock
TxRCLK	O	TxRCLK	Transmit Baud Clock
TxCCLK	O	TxCCLK	Transmit Conversion Clock
TxMCLK	O	TxMCLK	Transmit Multiplex Clock
RxCLK	O	RxCLK	Receive Bit Clock
RxRCLK	O	RxRCLK	Receive Baud Clock
RxCCLK	O	RxCCLK	Receive Conversion Clock
RxMCLK	O	RxMCLK	Receive Multiplex Clock
TxSCLK	I	TxSCLK	Transmit Synchro Clock : can be used to synchronize the transmitter on an external bit clock provided by the RS232C (or V.24) junction.

2. FUNCTIONAL DESCRIPTION

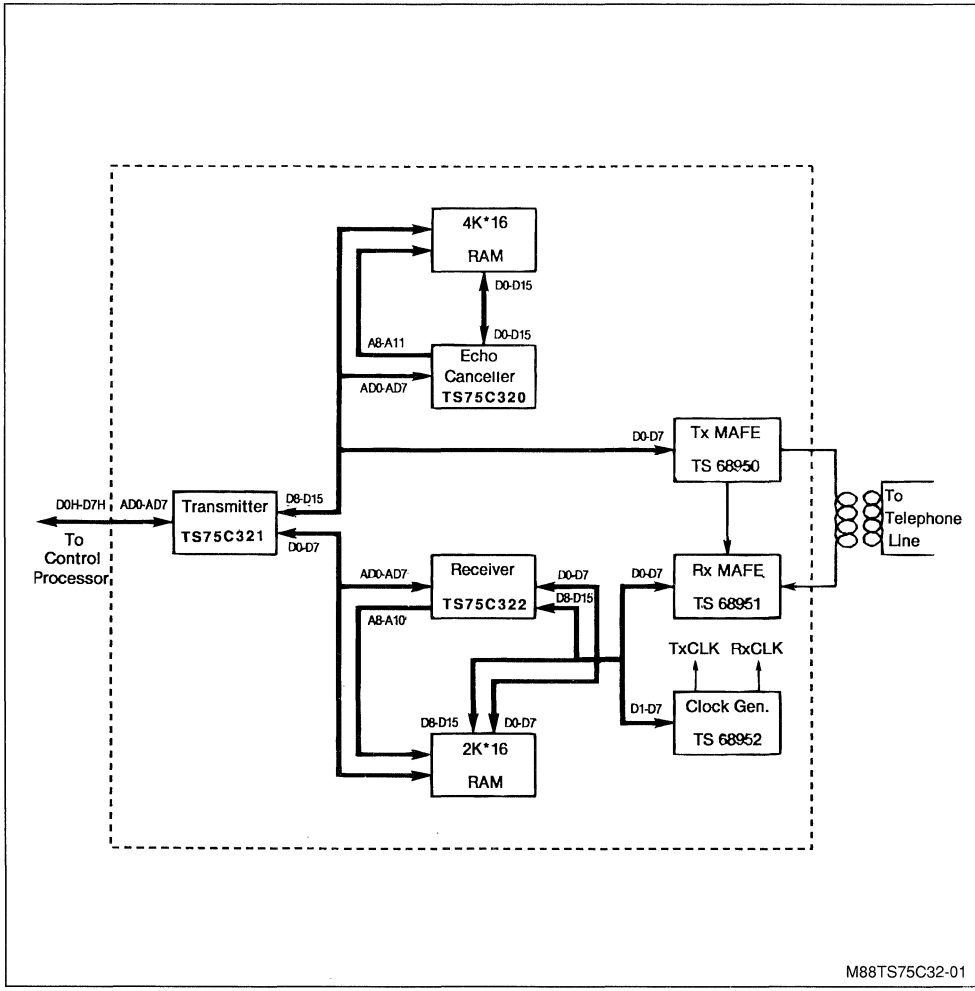
2.1. SYSTEM ARCHITECTURE

The SGS-THOMSON TS75C32 chip set is a highly integrated modem engine which provides the functionality and performance requirements for full-duplex 9600 bps modem solutions at a low cost and with a small circuit area. At the heart of the modem engine are three SGS-THOMSON DSPs which implement the complete signal processing and control functions. The analog front end of the modem engine consists of the SGS-THOMSON MAFE three-chip set which is designed to meet the requirements of high-speed modem applications and particularly V.32 modems. The only other components in the modem engine are the external RAM chips used for the far-end echo canceller delay line and the Viterbi decoder.

2.2 PROCESSOR AND MAFE CHIPS ARRANGEMENT

Figure 1 shows the interconnections between the MAFE and signal processors.

Figure 1 : Hardware Architecture.



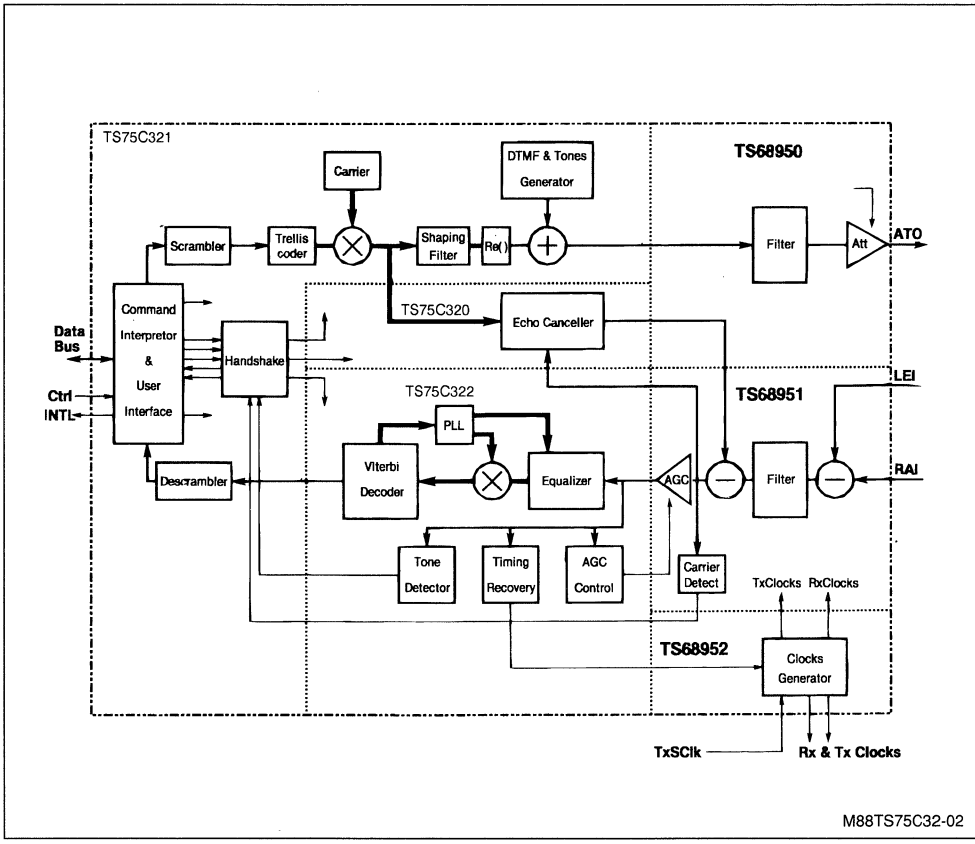
DSP 1 communicates with the control processor through its system bus, AD0-AD7. It is also connected to the two other DSPs through its D0-D7 and D8-D15 data buses to transfer data, to pass a control command to the DSPs and to get the modem operation status and then pass it to the control processor. The transmitter, V.32 handshake and part of the receiver algorithms are implemented in this processor. DSP 0 implements the echo cancellation function. 4Kx16 of RAM are connected to this processor to implement the data delay line for the far end echo cancellation. DSP 2 implements most of the receiver functions. 2Kx16 of RAM are attached to it due to the requirements of the Viterbi decoder.

The transmitter interface chip, TS68950 [see ref 5 of Appendix D], is connected to the 8 MSB's of the DSP 1 data bus. The echo replica is sent from DSP 1 to TS68950 then to the receiver interface chip, TS68951 [see ref 6 of Appendix D], after conversion to analog format. This chip and the clock generator chip, TS68952 [see ref 7 of Appendix D], are connected to the 8 MSB's of the DSP 2 data bus. The clock generator chip generates the A/D and D/A sampling clocks and the data bit and baud rate clocks.

2.3. OPERATION

2.3.1. MODES. The modem implementation is fully compatible with many CCITT and Bell recommendation. It operates at different bit rates from 9600 to 300 bps. In the 9600 bps mode, the trellis encoder and the Viterbi decoder can be switched in or out. Both the bit rate and trellis options are determined during the initial modem handshake sequence.
During FSK Modes (Bell 103, V.21 and V.23) a byte of information is exchanged with the Data Pump. This byte is a sampling image (7.2 KHz) of the Transmit circuit (TxD) of the junction.

Figure 2 : Functional Block Diagram (V.32 operation).



2.3.2. SIGNAL SPECTRUM SHAPING. A square root of 12.5 percent roll-off raised cosine filter is implemented in the transmitter to properly shape the transmit signal pulse. This filter is chosen based on a compromise of two considerations. First, the signal should have a narrow spectrum to avoid severe distortion on the telephone line. Second, the signal spectrum should be made as wide as possible to facilitate timing recovery in receiver.

2.3.3. ECHO CANCELLATION. The echo canceller is implemented on a single DSP [see ref 8 of Appendix D] with its associated external RAM. It cancels both near-end and far-end echoes even in the presence of frequency offset in the far-end echo path. The near-end echo cancellation is better than 55 dB and the residual near-end echo is smaller than - 65 dBm with a near-end echo level of - 10 dBm at the receiver input and a far-end signal level of - 43 dBm.

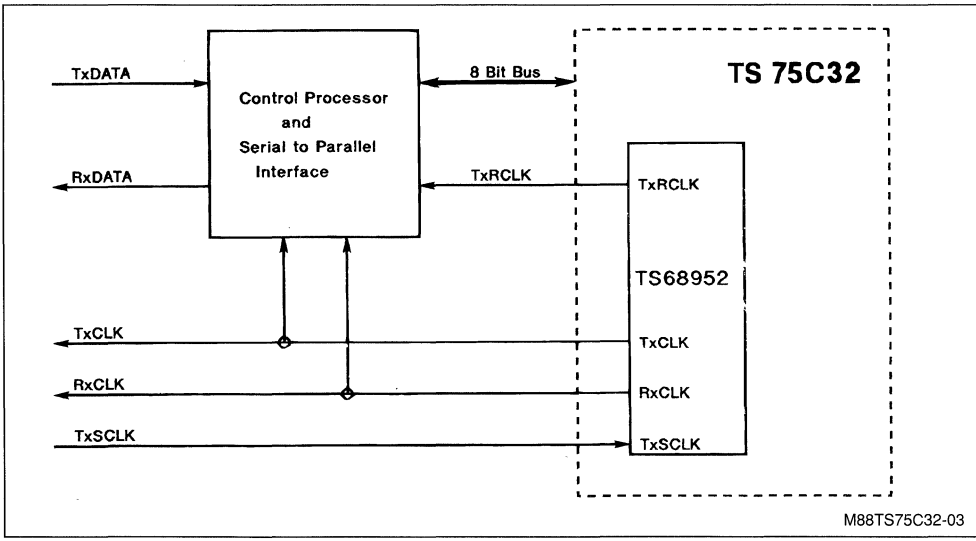
The combined near-end and far-end echo cancellers maintain the residual echo level 24 dB below the received signal even if the far-end echo signal path introduces up to 10 Hz of frequency offset. This level of cancellation is achieved when the far-end echo is 8 dB below the received far-end signal.

2.3.4. RECEIVER DESCRIPTION. The incoming signal is sent to the receiver interface chip to have the echo removed before being sent to DSP 2. The timing recovery algorithm takes the signal after the echo cancellation to derive the timing error to control the sampling phase of the A/D. It is able to cope with distant modem frequency drifts up to $\pm 2.10^{-4}$ as per CCITT rec. The A/D output samples are sent to the adaptive equalizer and the signal energy estimator for the gain control. The adaptive equalizer outputs a complex number every baud interval, which is then phase corrected by the carrier recovery loop. The Viterbi decoder makes hard decisions on the phase corrected samples for the adaptation of the equalizer and carrier recovery. It also makes soft decisions with an optimum decoding depth.

2.3.5. EQUALIZATION. The modem receiver has a passband T/3 fractionally spaced automatic adaptive equalizer which can compensate for the signal degradation caused by low quality line conditions.

2.3.6. SYNCHRONOUS AND ASYNCHRONOUS DATA TRANSFER. The TS75C32 modem engine provides the control processor and the DTE with both the transmit and the receive bit clocks (Figure 3). These clocks are generated by the TS68952 and are independent of each other. The receive clock (RxCLK) is derived from the received data signal. The transmit clock (TxCLK) is free-running at the nominal bit rate except during Digital Loopback Mode when it is synchronous to the RxCLK. If the transmit clock is free-running and an external bit clock signal from the terminal is connected to point TxSCLK then the transmit bit clock will be synchronized to that signal. The baud clocks (TxRCLK and RxRCLK) are also available to the control processor. If the TxSCLK pin is not used, it should be tied to a fixed logic level.

Figure 3 : Clock Signals for Synchronous Transmission.



The control processor interface is synchronous with the transmit baud clock. Eight bits of data are transferred from the control processor to DSP 1 for each information exchange. At 9600 bps, the data is transmitted every 2 bauds and the data is transmitted every 4 bauds for 4800 bps. The received bits are also nominally transferred from DSP 1 to the control processor once every two transmit baud intervals. When the transmitter is not synchronized with the receiver, however, the receive baud interval may be slightly shorter or longer than the transmit baud interval. If it is shorter, it is necessary to periodically pass 16 received bits from DSP 1 to the control processor. If it is longer, then periodically, there will be no data transmitted from DSP 1 to the control processor. Since the received bits are being passed to the DTE at a fixed rate equal to the RxCLK, some buffering is necessary in the control processor.

For asynchronous transmission, the clocks are not required by the DTE. But since the control processor to DSP 1 interface is still synchronous with respect to the transmit baud clock, the control processor must implement the asynchronous to synchronous conversion (as specified in the V. 22 bis recommendation, for example). This will consist of inserting or deleting stop bits as required, to ensure that the transmitted bit rate is within 0.01 % of the nominal rate (9600 or 4800 bps).

2.3.7. CLOCK AND DATA SYNCHRONIZATION. Both transmit and receive clocks have the same nominal frequency value. However, except in FSK Modes, these clocks are plesiochronous. The nominal frequencies are :

Mode	TxCLK	TxRCLK	Byte/Irq	Rate
V.32TCM	9.6K	2.4K	1/2	9600bps Trellis
V.32QAM	9.6K	2.4K	1/2	9600bps QAM
V.32QAM	4.8K	2.4K	1/4	4800bps
V.22Bis	2.4K	600	1/8	2400bps
V.22	1.2K	600	1/16	1200bps
V.22	600	600	1/32	600bps
Bell212A	1.2 K	600	1/16	1200bps
V.23	7.2K	1.2K	1/3	1200/75bps
Bell103	7.2K	1.2K	1/3	300bps
V.21	7.2K	1.2K	1/3	300bps

The TxCCLK is always 7.2 KHz. The TxMCLK is always set to 2.4 KHz after a configuration command (**cv32, cv22b**...), but can be changed by a **cmafe** command.

During the Hansdshake (V.32 and V.22bis) the bit clock (TxCLK and RxCLK) is set to the maximum value (respectively 9600 Hz and 2400 Hz). At the end of the handshake, depending of the negociation, this frequency is automatically set to the proper value.

The Irq Rate is always 2400 interruptions by second. The Byte/Irq is the nominal ratio of number of Byte of information (data) for each Irq generated by the data pump. The 1/2 ratio means that we have to send (**xmiti** command) 1 byte of data each two Irq, the additional Irq can be used to send an extra CCI command or must be a **nop** command.

2.3.8. TONE GENERATOR. The TS75C32 Engine has thirteen tone commands to quickly program the tone generators to generate the 2100 Hz Answer Tone (ANSWR) and the tone pairs for DTMF digits (DTMF0, ..., DTMF9, DTMF*, DTMF#). Silence, i.e. termination of tone generation, is accomplished by the use of a fourteenth command, SLNTS. These commands provide the tones and control required for normal operation of the modem.

Some circumstances might arise where additional tones are desired. For such cases, the V.32 Engine provides the user with the ability to generate such additional tones. This special feature is achieved through use of the tone control commands.

The TS75C32 Engine maintains a pair of locations which are reserved for tone generation parameters. These locations are denoted as TONE1 and TONE2. These locations may be programmed by the use of the define tone commands, DEFT1 and DEFT2. These commands provide the two tone generators with the phase increment of the tone to be generated with respect to the 7200 Hz sample rate.

The normal tone commands automatically program the tone generators. The DEFT1 and DEFT2 commands do not change the enabled or disabled state of the tone generators. If a tone is being generated when the DEFT command is received, the new tone will be generated without further action on the part of the user. If tone generation was not in progress it is not started.

Enabling the tone generators is accomplished by the tone control commands TGEN0, TGEN1, TGEN2, and TGEN12. Each of these commands affects both tone generators. TGEN0 disables both tone generators and TGEN12 enables both tone generators. To enable tone generator 1 and disable tone generator 2 the TGEN1 command is used. For the reverse condition, with generator 1 disabled and generator 2 enabled, the TGEN2 command is employed.

Refer to the command in appendix A for more detailed information.

Generation of special user tones is not part of the normal data communications operations of the modem. Use of this feature may interfere with data transfer operations. It is the responsability of the user to insure that the tone generators are used at a time when such interference will not occur and to disable both tone generators when the tone generation operations have been completed.

2.3.9. TEST MODES.The modem can be configured in two test modes, namely analog loop back and digital loop back modes. These loop back modes conform to the test loops 3 and 2 respectively defined in CCITT recommendation V.54.

In the local analog loop back mode, the transmitter signal is directly fed back into the local receiver input with the echo canceller enabled. The user is responsible for supplying a switch, which is controllable by the control processor, to enable or disable the analog loop back mode. The receiver descrambler is set as the inverse of the transmitter scrambler so that the receiver detects correct bits.

If the modem is configured in the digital loop back mode, the transmitter clock is locked to the receiver clock and the received bits are used as the transmitter input.

2.3.10. POWER ON INITIALIZATION. When the power is turned on, the transmitter interface sets the output signal attenuation to infinite. This avoids undesirable signal transmission on the telephone line [see ref 5 of Appendix D]. The gain of the AGC in the receive interface is set at the lowest level to avoid signal clipping during the initial handshake. The clock generator is programmed to generate all the necessary clocks for the 9600 bps mode. The clocks include the 7200 Hz sampling clock, the 2400 Hz baud rate clocks and the 9600 bps bit rate clocks. The transmit clocks are free running when the TxSClk pin is tied to a fixed logic level. Otherwise, the transmit bit clock is synchronized to the frequency present at the TxSClk pin. DSP 1 is configured properly to receive commands from the control processor.

2.4. MODEM INTERFACE [Figure 4]

2.4.1. ANALOG INTERFACE. The transmit signal at the tip and ring is programmable over a 22 dB dynamic range by 2 dB steps in TS68950. The signal level can be further scaled to any value by setting a scaling factor in the DSP. The nominal Transmit level, at the ATO pin is – 5.7 dBm.

2.4.2. DIGITAL INTERFACE. The DSP and control processor interface complies with the system bus interface of the ST18930. The interface to the control processor is managed by DSP 1 as shown in Figure 1. The DSP signals which are presented to the interface, and a brief definition of the signals are tabulated in table 1.

Table 1 : Digital Interface Signals.

Interface Signals	Signal Definition
D0H	Data Bus (LSB)
D1H	Data Bus
D2H	Data Bus
D3H	Data Bus
D4H	Data Bus
D5H	Data Bus
D6H	Data Bus
D7H	Data Bus (MSB)
RWL	Write Signal
DSL	Data Strobe
INTL	Mailbox Handshake
CSL	DSP Select
RSL	Register Select
TxRCLK	Transmit Baud Rate Clock
TxRCLK	Receive Baud Rate Clock
TxCLK	Transmit Bit Rate Clock
RxCLK	Receive Bit Rate Clock
TxMCLK	Transmit Multiplex Clock
RxMCLK	Receive Multiplex Clock
TxSCLK	Transmit Terminal Clock

All information exchanges across this interface conform to the three byte mailbox structure [see ref 4 of Appendix D] and protocol of the DSP. As may be seen in the table, the DSP generates a control signal, INTL, which defines the mailbox handshake operation.

2.4.3. CONTROL PROCESSOR/DSP INTERFACE. As seen by the software in the user provided control processor, DSP 1 is a synchronous machine. It requires the attention of the control processor at regular intervals in order to perform properly. Any failure of the control processor to interact with the modem engine in a timely manner will result in reduced performance or improper operation.

Each interaction begins when the control processor sends a three byte command to the mailbox. Once the command has been written to the mailbox, the ownership of the mailbox is relinquished by the control processor. Upon acquisition of the mailbox, DSP 1 reads the command bytes and then sends a three byte response to the mailbox. Then, DSP 1 re-

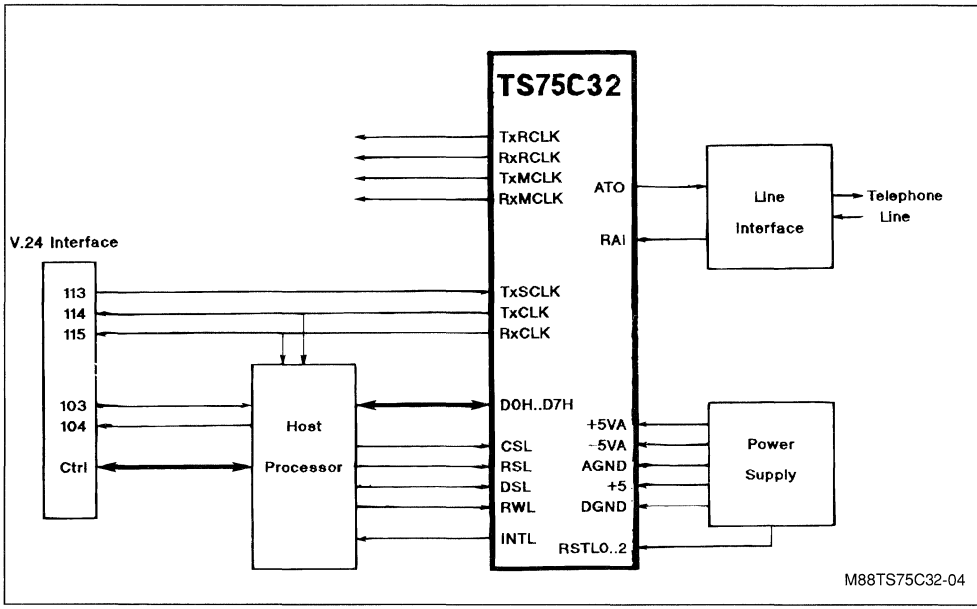
linquishes the ownership of the mailbox back to the control processor. The received command is then decoded and the embedded data and/or operational parameters are extracted and acted upon as appropriate. The modem status information will be collected for the next mailbox exchange. The control processor handles the returned information as soon as it regains the ownership of the mailbox.

Because the control processor owns the mailbox initially, it may store a command at any time before it is required by DSP 1. After this, the mailbox becomes available to DSP1 and can be read by it when required.

2.4.4. MAILBOX DESCRIPTION.The mailbox located internally to the DSP contains 3-byte input (RIN) and 3-byte output (ROUT) shift registers. The DSP has an internal flag RDYOIN which indicates whether the DSP (RDYOIN = 0) or control processor (RDYOIN = 1) has access to the mailbox. The DSP can relinquish its accessability to the mailbox by setting RDYOIN but it can no longer regain access to the mailbox as RDYOIN is reset only after the control processor relinquishes its accessability to the mailbox. The access protocol and system bus transfers are controlled by an internal I/O sequencer within the DSP described as follows :

1. The mailbox is made available to the control processor by the DSP program which sets RDYOIN flag to 1. This action will cause INTL mailbox handshake signal to switch to the active (low) state.
2. The control processor detects INTL active and dummy reads the mailbox by forcing DSP Select (CSL) and Register Select (RSL) low along with write signal (RWL) high. The activated Data Strobe signal (DSL = 0) validates the above signals.
3. The DSP detects the dummy read of its mailbox via the control signals mentioned in 2 and negates INTL mailbox handshake signal within 800 ns.
4. The control processor detects the negation of INTL indicating that the DSP mailbox is available for data transfers. The control processor writes three 8-bit bytes and/or reads three 8-bit bytes in the mailbox shift registers RIN, ROUT respectively.
5. The exchange protocol described above is terminated by the control processor performing a dummy read of the mailbox as in 2 but with RSL in the high state.
6. The RDYOIN flag within the DSP is cleared to 0 by the dummy read of the mailbox in step 5 and the DSP now has access to RIN and ROUT registers within the mailbox.

Figure 4 : Functional Interconnect Diagram.



3. USER INTERFACE - COMMAND SET

The command set has the following attractive features :

- user friendly with easy to remember mnemonics
- allows straightforward expansion with new commands to suit specific customization requirements
- fully compatible with other SGS-THOMSON DSP-based modem products.

The command set has been designed to provide the necessary functional control of the TS75C32. Each command falls into one of several groups, based on function and the presence or absence of parameters. The length of the OP code varies with instruction type, but in all cases, a command consists of three bytes.

The commands which pass parameters or data to DSP 1 have a short OP code format. Byte 0 forms the OP code portion of the command. Bytes 1 and 2 are data and/or parameters associated with each OP code. The meaning of the last two bytes is dependent on the specific instruction.

Other instructions command the TS75C32 to perform certain specific tasks. These do not pass parameters or data to the TS75C32. These commands have an OP code which is a full 24 bits in length.

The command set of the TS75C32 is summarized below. The descriptions are of the form :

MNEMONIC (OPCODE) : DESCRIPTION.

For detailed information and data format specifics of each command, please refer to appendix A.

3.1. COMMAND SUMMARY

3.1.1. OPERATIONAL CONTROL COMMANDS.

FREZ (14) : Freeze adaptive processes. Freeze the adaptive processes as specified by the data in bits 0 and 1 of byte 1. Bit 0 of byte 1 controls the adaptive equalizer. Freeze the equalizer if bit 0 of byte 1 is 1. A 0 in this bit will unfreeze the equalizer. Echo canceller adaptation is controlled by bit 1 of byte 1. if bit 1 is 1, the echo canceller adaptation is frozen. The echo canceller adaptation is unfrozen by a 0 in bit 1.

HSHK (040000) : Handshake. Begin the handshake sequence. The V.32 modem engine carries out all the steps defined in the CCITT recommendation. The status reported to the control processor will indicate the success or failure of the process and its progress.

INIT (0600C0) : Initialize. Initialize the V.32 modem engine. Set all parameters to default values and wait for commands for the control processor.

NOP (000000) : No Operation. No new operation is commanded. The state of the V.32 engine remains unaltered and a previously invoked multi-baud command (such as HSHK) continues.

RTRA (050000) : Retrain. Start sending the retrain sequence as defined in the CCITT recommendation.

SETGN (02) : Set Gain. This command sets a global gain factor, which will be multiplied by all transmit samples before being sent to the TS68950. Bytes 1 and 2 store the gain factor.

3.1.2. DATA COMMUNICATIONS COMMANDS.

XMIT (03) : Transmit data. Transmit data to far end modem. The data is provided in byte 1 of the command, where the least significant bit is the first bit to be transmitted. The third byte of the command must be provided, but is not used. Hence, any value may be supplied.

XMITI (01) : Transmit data and Initiate additional cycle. Transmit data and inform the DSP to accept another command at the next transmit baud. If the next command requires an answer from DSP 1, the control processor has to keep issuing this command followed by a command which does not requires an answer until the answer has been received.

3.1.3. MEMORY. MANIPULATION COMMANDS.

SPAC (13) : Store Parameter And Count. Store parameter in addressed memory and increment the pointer. This command passes data in bytes 1 and 2, least significant byte in byte 1. It is used to write an arbitrary 16-bit value into the writable memory location currently specified by the Memory Address Register. The contents of the Memory Address Register are incremented by 1 at the completion of this command.

SPAM (12) : Store parameter in Addressed Memory. This command passes data in bytes 1 and 2, least significant byte in byte 1. It is used to write an arbitrary 16-bit value into the writable momory location currently specified by the Memory Address Register.

WARP (10) : Write Address and Return Parameter. This command allows the controller to read any of the XRAM, YRAM, ERAM or CROM (DSP internal memory areas) of any of the three modem DSPs without interrupting the processors. The address to the V.32 modem engine is provided in bytes 1 and 2 of the command (least significant byte first). DSP 1 stores the address in the Memory Address Register and returns the contents of the addressed location.

WARPX (11) : Write Address and Return Parameter Complex. The address to the V.32 modem engine is provided in bytes 1 and 2 of the command (least significant byte first). DSP 1 stores the address in the Memory Address Register. The most significant bytes of the real and imaginary parts of a complex number are returned. The 8 most significant bits of the data addressed by the Memory Address Register are returned to the control processor through byte 1. Byte 2 stores the 8 most significant bits of the data at the location immediately higher. The Memory Address Register retains the address provided. (i.e. it is not incremented.)

3.1.4. CONFIGURATION CONTROL COMMANDS
CV32 (20) : Configure modem for V.32. Configure the modem as Originate / Answer, 9600/4800, Viterbi / No-Viterbi, Analog Loopback, Digital Loopback.

CFSK (1D) : Configure modem for FSK modes of operation (V.23/V.21/Bell103).

CV22B (1E) : Configure modem for V.22Bis/V.22/Bell212A modes.

3.1.5. MAFE MANIPULATION COMMANDS.
CMAFE (07) : Configure MAFE. The following two bytes of this command are written directly to the MAFE chip set (TS68950/1/2). This allows the control processor to configure parameters, such as the transmit level, the receiver analog front end, and the transmit and receive clocks.

RRR1 (080000) : Read Register 1. Causes the TS75C32 Engine to read and immediately return the 12 bit contents of the MAFE register RR1.

RRR2 (090000) : Read Register 2. Causes the TS75C32 to read and immediately return the 12 bit contents of the MAFE register RR2.

WTR1 (0A) : Write Register 1. Causes the TS75C32 to write the supplied data to the MAFE register TR1.

WTR2 (0B) : Write Register 2. Causes the TS75C32 to write the supplied data to the MAFE register TR2.

3.1.6. TONE SELECT COMMANDS.
TONE (0C) : Select Tone. Program the tone generator(s) for the desired tone(s). Examples include :

- **ANSWR** (0C1000) : Program the tone generator for the 2100 Hz answer tone.
- **DTMF** (see appendix) : Program the tone generators for the tone pair which forms the specified DTMF digit.

This command selects the tones to be transmitted, but does not enable the tone generators. To transmit the tones, the tone control commands must be issued.

3.1.7. TONE CONTROL COMMANDS
DEFT1 (0E) : Define Tone 1. Define tone 1 as specified by the parameter provided. The two data bytes following the opcode are used to program, but not enable, tone generator 1. The data for the tone is represented as a phase offset per sample. Byte 1 stores the least significant byte of the phase increment.

DEFT2 (0F) : Define Tone 2. Define tone 2 as specified by the parameter provided. The two data bytes following the opcode are used to program, but not enable, tone generator 2. The data for the tone is represented as a phase offset per sample. Byte 1 stores the least significant byte of the phase increment.

SLNT (0D0000) : Silence the tone generators. Discontinue tone transmissions by disabling the tone generators.

TGEN (0D) : Tone Generator control. Enable or disable tone generator 1 and tone generator 2 according to parameter provided. If both tone generators are enabled, the level of tone 2 is 2 dB higher than that of tone 1.

3.2. STATUS REPORTING

Whenever DSP 1 owns the mailbox, it transmits the modem status to the control processor. The status consists of three bytes of information which are stored by DSP 1 in its ROUT register for access by the control processor. These three bytes may consist of received bits and modem status or they may contain the answers to the previous command, such as WARP and RRR1/2.

Data bits have higher priority than the answer to the previous command. If both data byte and command answer are ready to be sent, the data will be sent.

Byte 0 contains status flags. Refer to appendix B for the detailed format of the status response. The four most significant bits, F00, F01, F10 and F11, indicate various conditions during the call establishment, handshaking and the data modes. They have different meanings in different modes. The flag DAV1 and DAV2 are used to indicate the type of information contained in bytes 1 and 2. Bit H is used to indicate the condition of the handshake and bit 107 informs the control processor whether the 107 flag has to be set.

DAV1 and DAV2. If both DAV1 and DAV2 are set to 1, bytes 1 and 2 contain the data in response to the previous command. Refer to the relevant commands in appendix A to get the detailed information on the interpretation of the data in bytes 1 and 2. Otherwise, they contain either the received data bits or the handshake detection status or both.

If both bits are set to 0, both byte 1 and byte 2 contain the data bits, where the bits in byte 1 are received earlier in time. The least significant bit is the first bit received. The data bits are stored in byte 1 and the modem status is stored in byte 2 when DAV2 is 1 and DAV1 is 0. When DAV1 is 1 and DAV2 is 0, the control processor should ignore the data in byte 1 and get the detection status from byte 2.

During handshake operations the TS75C32 reports the detection status regularly. When the rate sequence is received, it will be transferred in byte 1 of the response. Each bit in byte 2 indicates the detection of a specific event in the training sequence. It has different meanings for call and answer modems. For detailed information, refer to appendix B. During the data mode, byte 2 is always provided, but is used only when there are two bytes of data to transmit. This occurs occasionally when the receiver clock is running faster than the transmitter clock.

F00-F11 bits. During the call establishment operation, the V.32 Engine reports call progress tones through the F01 and F00 flags. F00 is set to 1 when the signal energy in frequency band 1 is above the threshold level. F01 is set to 1 when the signal energy in band 2 is above the threshold level. Detection of the 2100 Hz answer tone is indicated by setting the F10 flag to a 1.

During handshake operations, all four bits are used to indicate the line condition and some detection results. F00 is set to 0 if the line quality is good and 1 if it is bad. F01 is set to 1 if any segment in the training sequence is not detected within a time out. This bit can be used to indicate a non V.32 detection if either AA is not detected in the answer modem or the AC is not detected in the call modem. Both F00 and F01 are set to 1 when an illegal mode or a GSTN cleardown is received in the rate sequence.

The detection of the rate sequence is reported in the flags F11 and F10. When the modem is operating at 9600 bps without trellis coding, these bits are both set to 0. With trellis coding at 9600 bps, F11 is set to 1 and F10 is cleared to 0. For 4800 bps, 0 and 1 will be placed in F11 and F10, respectively. When both F11 and F10 are set to 1, the modem has negotiated with the far end modem and determined that the maximum negotiated operating speed is 2400 bps.

During data mode, the perceived line quality is reported in the flags F01 and F00. The line conditions are reported as either good (code 00), poor (code 01), or terrible (code 10). The code 10 should be interpreted as a local modem retrain request. Upon receipt of this code, the controller can issue the RTRA command to begin the retrain procedure. The code 11 is used when the remote modem begins a retrain sequence. The control processor is then responsible for manipulating the appropriate data communications interface signals.

H and 107 bits. When the TS75C32 is commanded to perform the CCITT handshake sequence, the H bit will be set to 1 for the duration of the handshake operation. At the successful completion of the handshake operation the H flag will go to 0 and the control processor is then responsible for manipulating the appropriate data communications interface signals. e.g. 106 and 109. The 107 flag is set to a 1 to indicate that the controller should assert signal 107 on the data communications interface.

3.3. COMMAND LIST

OPERATIONAL CONTROL COMMANDS

Command Mnemonic	OP Code (HEX)	Description
uFzec	170000	Unfreeze Echo Canceller
Frezq	1B0000	Freeze the Equalizer Adaptation
Frezc	160000	Freeze the Echo Canceller Adaptation
uFzeq	1C0000	Unfreeze Equalizer
hshk	040000	Handshake with Other Modem
init	0600C0	Initialize Modem
nop	000000	No Operation
rtra	050000	Retrain
setgn	02	Set the Scaling Factor for the Transmitter

DATA COMMUNICATIONS COMMANDS

Command Mnemonic	OP Code (HEX)	Description
xmit	03	Transmit Data
xmiti	01	Transmit Data and Initiate Additional Transfer

MAFE MANIPULATION COMMANDS

Command Mnemonic	OP Code (HEX)	Description
cmafe	07	Configure MAFE Chipset
rrr1	080000	Read MAFE Reg RR1
rrr2	090000	Read MAFE Reg RR2
wtr1	0A	Write MAFE Reg TR1
wtr2	0B	Write MAFE Reg TR2

TONE SELECT COMMANDS

Command Mnemonic	OP Code (HEX)	Description
answ	0C1000	Select 2100 Hz Answer Tone
dtmf 0	0C0000	Select DTMF Digit 0
dtmf 1	0C0100	Select DTMF Digit 1
dtmf 2	0C0200	Select DTMF Digit 2
dtmf 3	0C0300	Select DTMF Digit 3
dtmf 4	0C0400	Select DTMF Digit 4
dtmf 5	0C0500	Select DTMF Digit 5
dtmf 6	0C0600	Select DTMF Digit 6
dtmf 7	0C0700	Select DTMF Digit 7
dtmf 8	0C0800	Select DTMF Digit 8
dtmf 9	0C0900	Select DTMF Digit 9
dtmf *	0C0E00	Select DTMF Digit *
dtmf #	0C0F00	Select DTMF Digit #
tone	0C	Select Tone (s)

CONFIGURATION CONTROL COMMANDS

Command Mnemonic	OP Code (HEX)	Description
cv32	20	Configure Modem for V.32
CFSK	1D	Configure Modem for FSK (V.23 / V.21 / Bell 103)
cv22B	1E	Configure Modem for V.22 / V.22 bis / Bell 212A
cb21	26	Configure Modem for V.21
cb212	27	Configure Modem for Bell 212
cb103	28	Configure Modem for Bell 103

MEMORY MANIPULATION COMMANDS

Command Mnemonic	OP Code (HEX)	Description
spac	13	Write MEM and Increment MEM Pointer
spam	12	Write MEM
warp	10	Write MEM Pointer & Read MEM
warpx	11	Write MEM Pointer & Read MEM & MEM + 1

TONE CONTROL COMMANDS

Command Mnemonic	OP Code (HEX)	Description
deft1	0E	Define Tone 1
deft2	0F	Define Tone 2
slnt	0D0000	Transmit no Tone
tgen 0	0D0000	Tone Generators Disabled
tgen 1	0D0100	Tone Generator 1 Enabled
tgen 2	0D0200	Tone Generator 2 Enabled
tgen 12	0D0300	Tone Generators 1 & 2 Enabled

4. ELECTRICAL SPECIFICATIONS

4.1. MAXIMUM RATINGS :

TS75C320/1/2

Symbol	Parameter	Value	Unit
V_{CC}*	Supply Voltage	– 0.3 to 7.0	V
V_{in}*	Input Voltage	– 0.3 to 7.0	V
T_A	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

* With respect to V_{SS}.

Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

TS68950/1/2

Symbol	Parameter	Value	Unit
	Supply Voltage between V + and AGND or DGND	– 0.3 to + 7	V
	Supply Voltage between V - and AGND or DGND	– 7 to + 0.3	V
	Voltage between AGND and DGND	– 0.3 to + 0.3	V
	Digital Input Voltage	DGND – 0.3 to V_{CC}^+ + 0.3	V
	Digital Output Voltage	DGND – 0.3 to V_{CC}^+ + 0.3	V
	Digital Output Current	– 20 to + 20	mA
	Analog Input Voltage	V_{CC}^- – 0.3 to V_{CC}^+ + 0.3	V
	Analog Output Voltage	V_{CC}^- – 0.3 to V_{CC}^+ + 0.3	V
	Analog Output Current	– 10 to + 10	mA
	Power Dissipation	500	mW
T_{oper}	Operating Temperature	0 to + 70	°C
T_{stg}	Storage Temperature	– 65 to + 150	°C

4.2. DC ELECTRICAL CHARACTERISTICS DGND = AGND = 0 V

Digital Supply

V_{CC} = 5.0 V ± 10 %, V_{SS} = 0, T_A = 0 to + 70°C (Unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IL}	Input Low Voltage	– 0.3		0.8	V
V_{IH}	Input High Voltage	2.4		V_{CC}	V
I_i	Input Extal Current	– 50		+ 50	µA
I_{in}	Input Leakage Current	– 10		10	µA
V_{OH}	Output High Voltage (I_{load} = – 300 µA)	2.7			V
V_{OL}	Output Low Voltage (I_{load} = 3.2 mA)			0.5	V
P_D	Total Power Dissipation		1.5		W
C_{in}	Input Capacitance		10		pF
I_{TSI}	Three State (off state) Input Current	– 20		– 20	

Note 1 : Case temperature T_C must be maintained below 100 °C.

Analog Supply

Symbol	Parameter	Min.	Typ.	Max.	Unit
V^+	Positive Power Supply	4.75		5.25	V
V^-	Negative Power Supply	– 5.25		– 4.75	V
I^+	Positive Supply Current			35	mA
I^-	Negative Supply Current	– 35			

4.3. AC ELECTRICAL SPECIFICATIONS

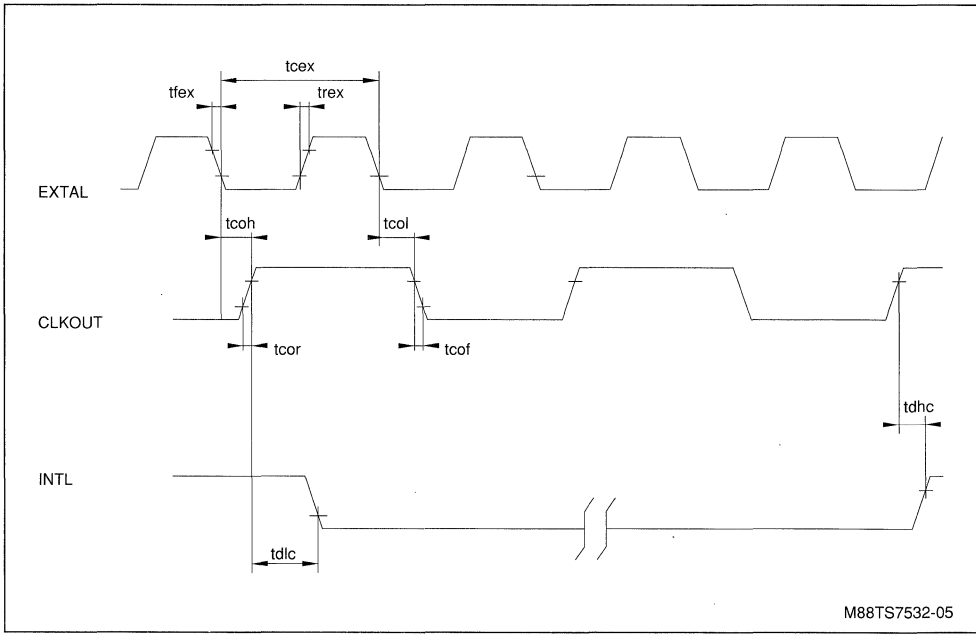
4.3.1. CLOCK AND CONTROL PINS TIMING

(V_{CC} = 5.0 V ± 10 %, T_A = 0° to + 70°C, see figure 5)
OUTPUT LOAD = 50 pF + DC characteristics I load

REFERENCE LEVELS : V_{IL} : 0.8 V V_{IH} : 2.4 V
V_{OL} : 1.4 V V_{OH} : 2.4 V tr, tf ≤ 5 ns for input signal

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{cex}	External Clock Cycle Time $T_C = 4 \times t_{cex}$ $T_C = 2 \times t_{cex}$ $T_C = t_{cex}$	40 50 40		100 200 100	ns ns ns
t_{fex}	External Clock Fall Time			5	ns
t_{rex}	External Clock Rise Time			5	ns
t_{coh}	EXTAL to CLKOUT High Delay		25		ns
t_{col}	EXTAL to CLKOUT Low Delay		25		ns
t_{cor}	CLKOUT Rise Time			10	ns
t_{cof}	CLKOUT Fall Time			10	ns
t_{dlc}	CLKOUT to Control Output Low (INTL)			30	ns
t_{dhc}	CLKOUT to Control High (INTL)			30	ns

Figure 5 : Clock and Control Pins Timing.



4.3.2. TS68952 : Clock Generator

CRYSTAL OSCILLATOR INTERFACE

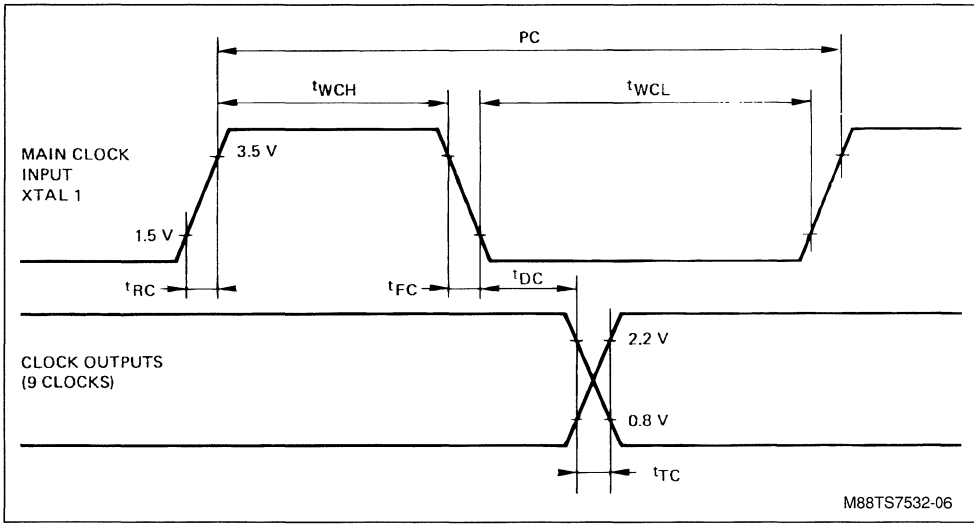
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level Voltage				1.5	V
V_{IH}	Input High Level Voltage		3.5			V
I_{IL}	Input Low Level Current	$DGND \leq V_I \leq V_{IL\ max}$	−15			µA
I_{IH}	Input High Level Current	$V_{IH\ min} \leq V_I \leq V^+$			15	µA

CLOCK WAVE FORMS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
PC	Main Clock Period	XTAL1 Input	150	173.6		ns
t_{WCL}	Main Clock Low Level Width	XTAL1 Input	50			ns
t_{WCH}	Main Clock High Level Width	XTAL1 Input	50			ns
t_{RC}	Main Clock Rise Time	XTAL1 Input			50	ns
t_{FC}	Main Clock Fall Time	XTAL1 Input			50	ns
t_{DC}	Clock Output Delay Time	All Clock Outputs CL=50 pF			500	ns
t_{TC}	Clock Output Transition Time	All Clock Outputs CL=50 pF			100	ns

Unless otherwise noted, electrical characteristics are specified over the operating range. Typical values are given for $V^+ = 5.0$ V and $t_{amb} = 25$ °C.

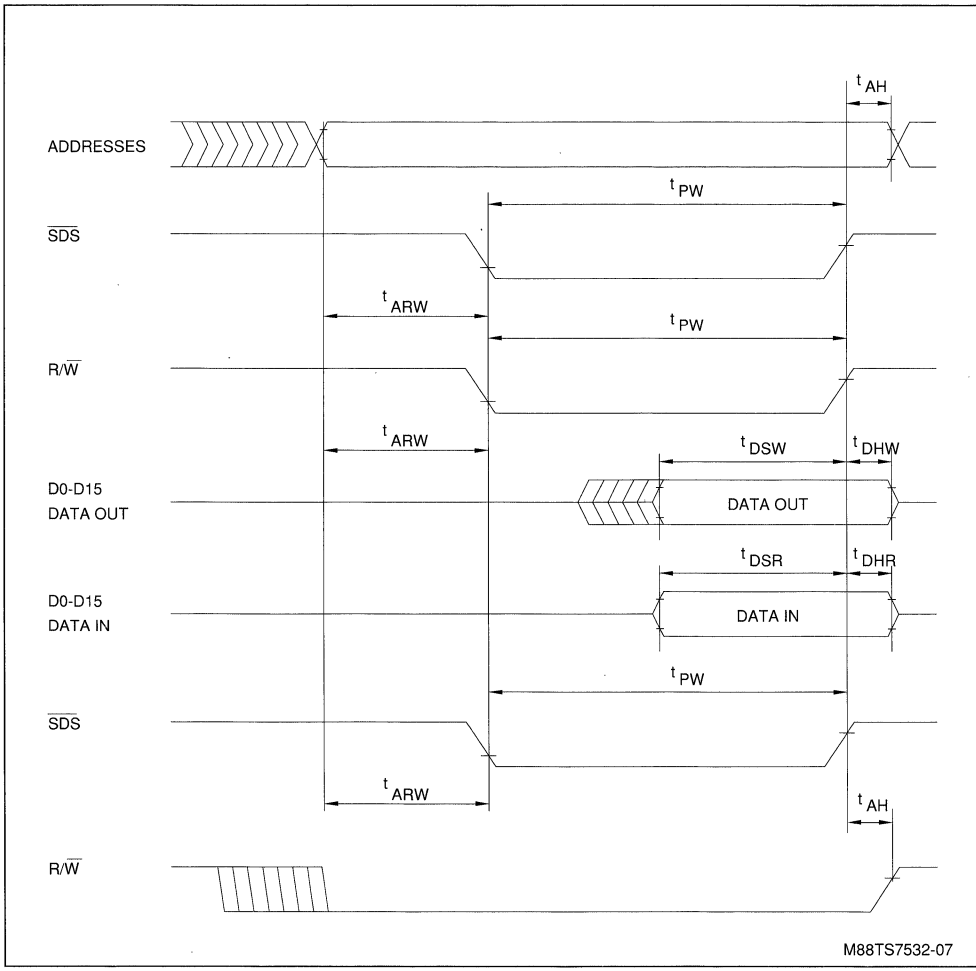
Figure 6 : Clock Generator.



4.3.3.LOCAL BUS TIMING
(V_{CC} = 5.0 V ± 10 %, T_A = 0° to + 70°C, see figure 7)

Symbol	Parameter	Min.	Max.	Unit
t_{PW}	$\overline{RD}$, $\overline{WR}$, $\overline{SDS}$ Pulse Width	1/2 tc – 10	1/2 tc	ns
t_{AH}	Address Hold Time	10		ns
t_{DSW}	Data Set-up Time, Write Cycle	25		ns
t_{DHW}	Data Hold Time, Write Cycle	10		ns
t_{DZW}	$\overline{DS}$ High to Data High Impedance, Write Cycle		40	ns
t_{DSR}	Data Set-up Time, Read Cycle	20		ns
t_{DHR}	Data Hold Time, Read Cycle	5		ns
t_{ARW}	Address Valid to $\overline{WR}$, $\overline{SDS}$, $\overline{RD}$ Low	1/2 tc – 25		ns

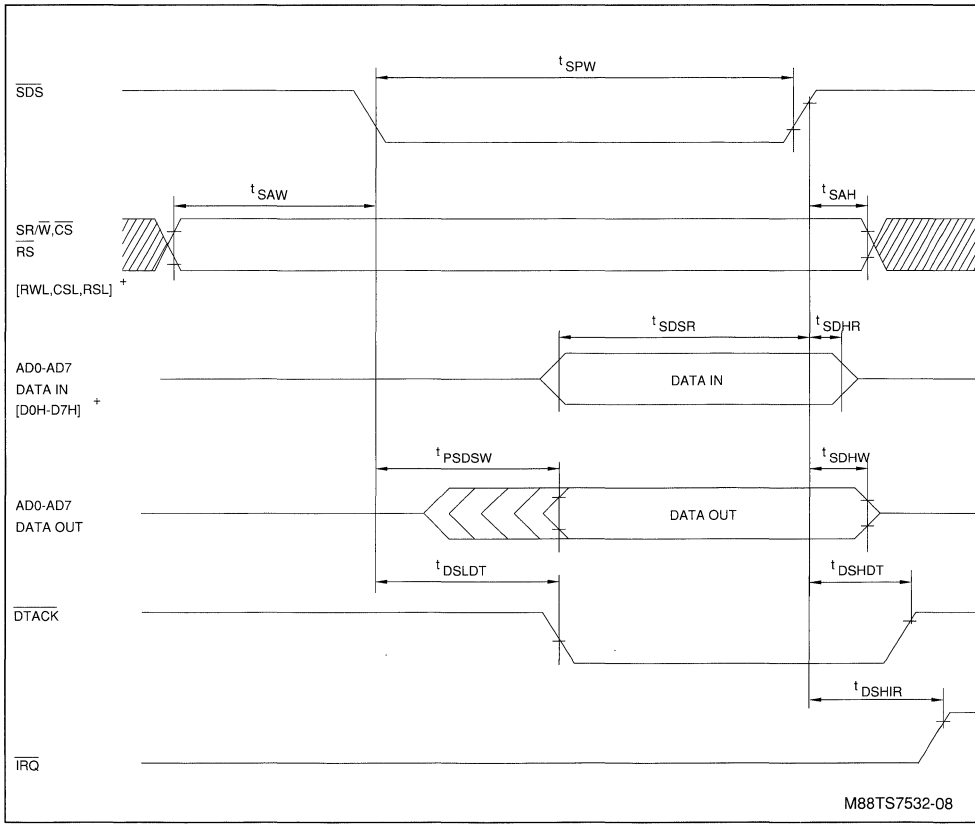
Figure 7 : Local Bus Timing Diagram.



4.3.4. SYSTEM BUS TIMING
(V_{CC} = 5.0 V ± 10 %, T_A = 0° to + 70°C, see figure 8)

Symbol	Parameter	Min.	Max.	Unit
t_{SPW}	$\overline{SDS}$ Pulse Width	50		ns
t_{SAW}	SR / $\overline{W}$, $\overline{CS}$, $\overline{RS}$ Set-up Time	15		ns
t_{SAH}	SR / $\overline{W}$, $\overline{CS}$, $\overline{RS}$ Hold After $\overline{SDS}$ High	5		ns
t_{SDSR}	Data Set-up Time, Read Cycle	15		ns
t_{SDHR}	Data Hold Time, Read Cycle	5		ns
t_{SDSW}	Data Set-up Time, Write Cycle		30	ns
t_{SDHW}	Data Hold Time, Write Cycle	10	50	ns
t_{DSHIR}	$\overline{SDS}$ High to $\overline{IRQ}$ High		800	ns

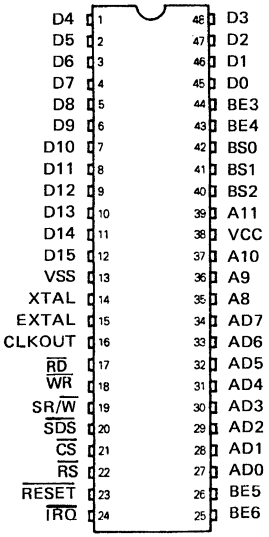
Figure 8 : System Bus Timing Diagram.



+ Note : Signal names on Host Processor Interface.

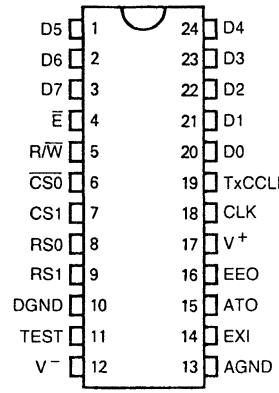
5. PIN CONNECTIONS

TS75C320 - TS75C321 - TS75C322



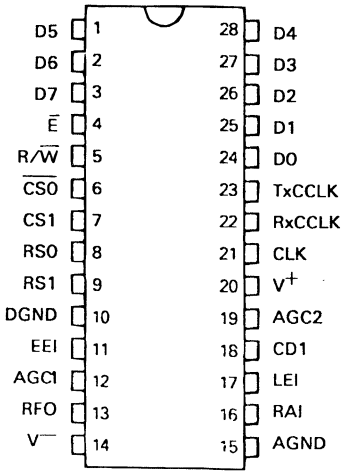
M88TS7532-09

TS68950



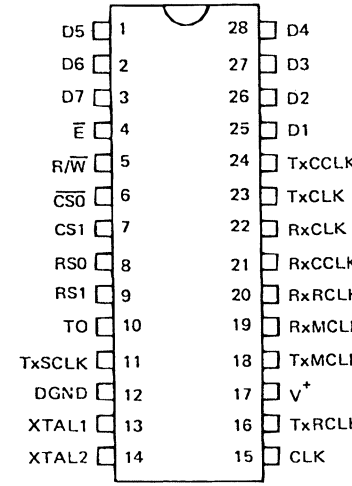
M88TS68950-01

TS68951



M88TS68951-01

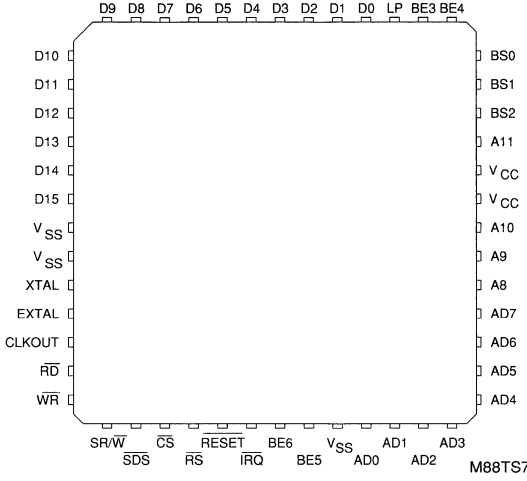
TS68952



M88TS68952-01

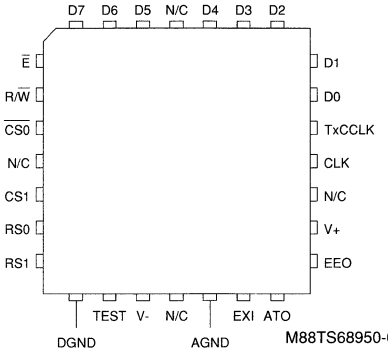
5. PIN CONNECTIONS (continued)

TS75C320 - TS75C321 - TS75C322



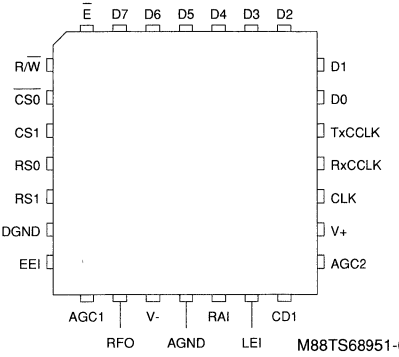
M88TS75C32-05

TS68950



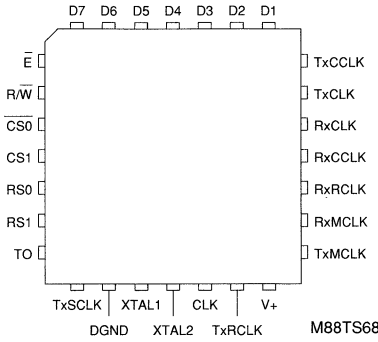
M88TS68950-02

TS68951



M88TS68951-02

TS68952



M88TS68952-02

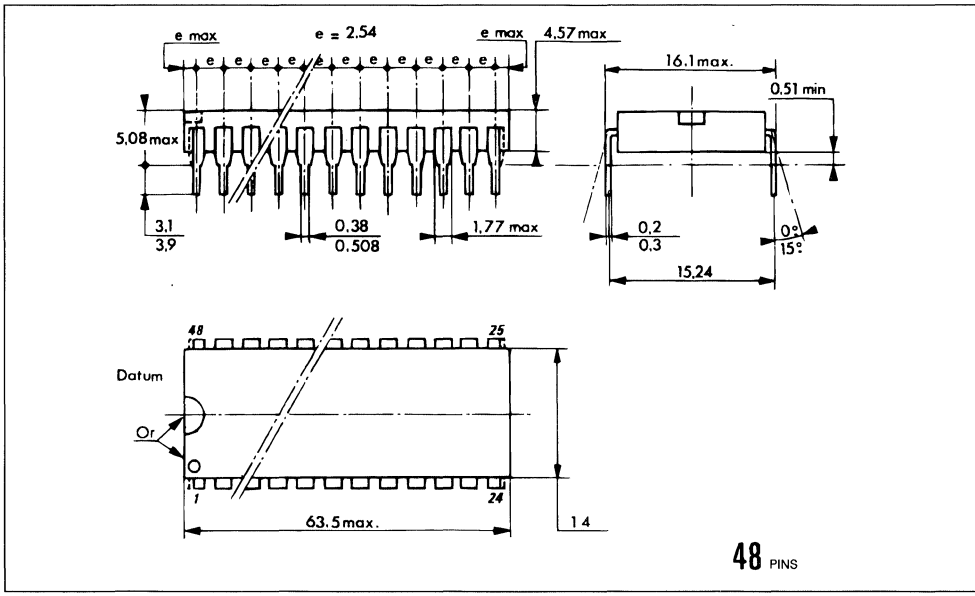
ORDERING INFORMATION

Part Number	Temperature Range	Package
TS75C320CP	0 °C to + 70 °C	DIP48
TS75C321CP	0 °C to + 70 °C	DIP48
TS75C322CP	0 °C to + 70 °C	DIP48
TS68950CP	0 °C to + 70 °C	DIP24
TS68951CP	0 °C to + 70 °C	DIP28
TS68952CP	0 °C to + 70 °C	DIP28
TS75C320CFN	0 °C to + 70 °C	PLCC52
TS75C321CFN	0 °C to + 70 °C	PLCC52
TS75C322CFN	0 °C to + 70 °C	PLCC52
TS68950CFN	0 °C to + 70 °C	PLCC28
TS68951CFN	0 °C to + 70 °C	PLCC28
TS68952CFN	0 °C to + 70 °C	PLCC28

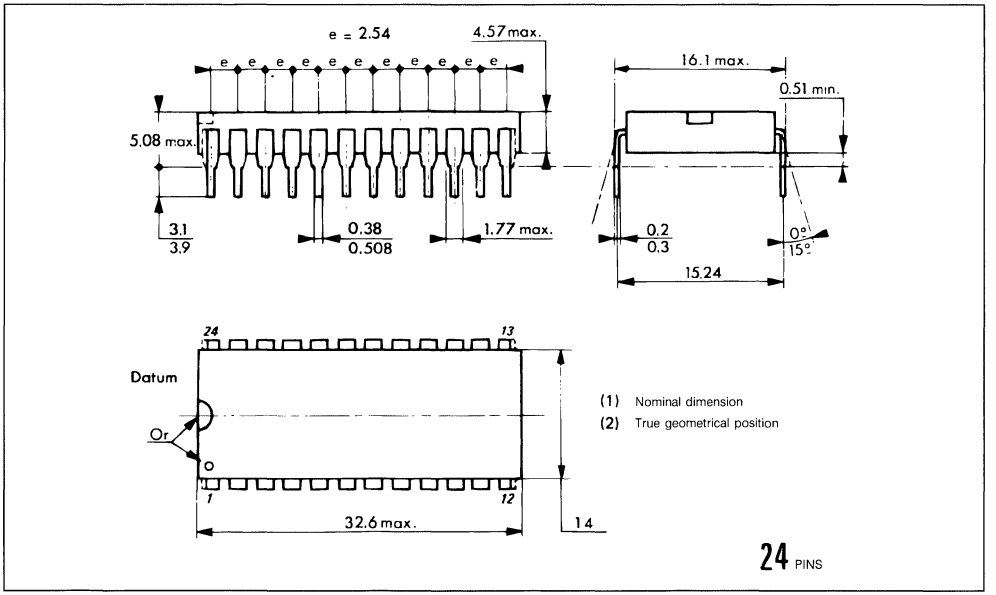
7. PACKAGE MECHANICAL DATA

TS75C320/TS75C321/TS75C322

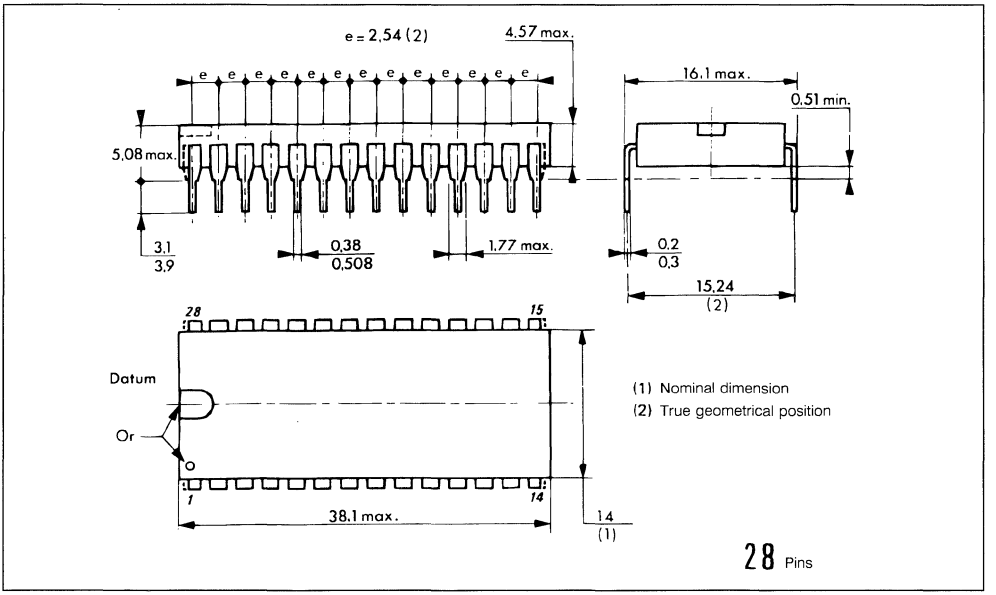
48 Pins - Plastic Dip.



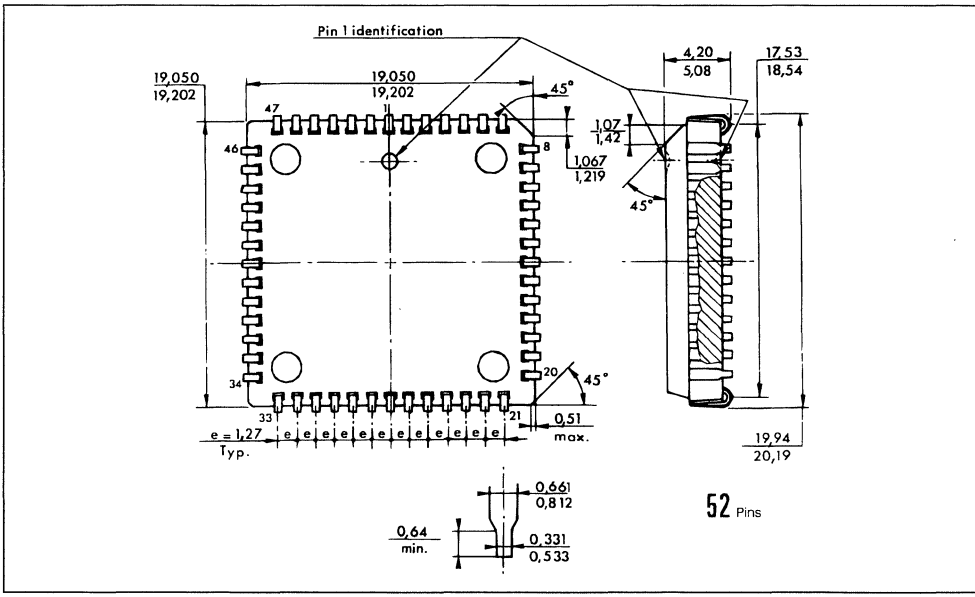
TS68950
24 Pins - Plastic Dip.



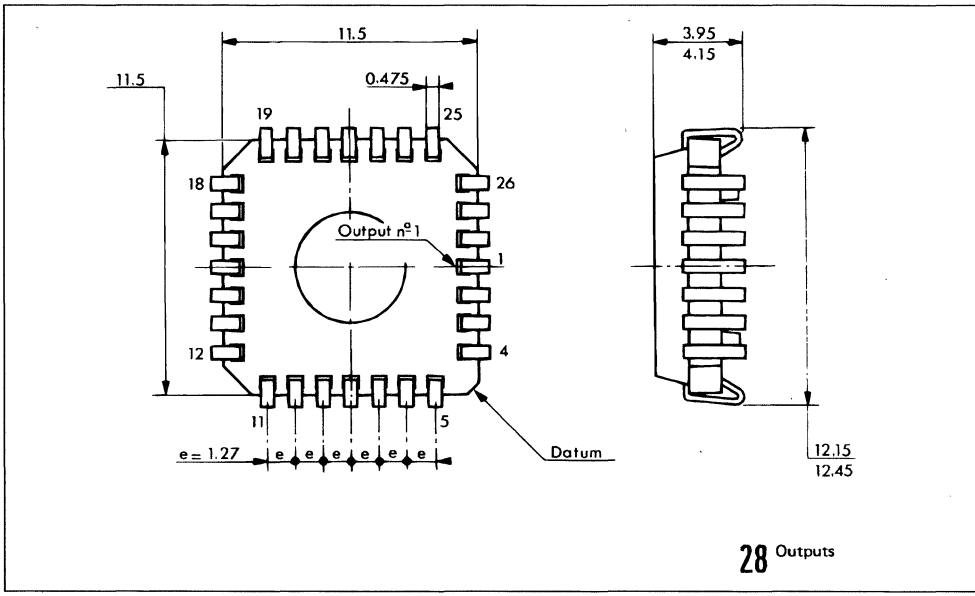
TS68951/TS68952
28 Pins - Plastic Dip.



TS75C320/21/22
52 Pins - Plastic Leaded Chip Carrier.



TS68950/51/52
28 Pins - Plastic Leaded Chip Carrier.



APPENDIX A
COMMAND SET DESCRIPTION

cmafe - configure the TS68950/1/2 components of the V.32 Engine

INSTRUCTION TYPE
MAFE manipulation command

OPCODE
07

SYNOPSIS
cmafe address register code data

DESCRIPTION
cmafe is used to directly manipulate the operating parameters of the TS68950/1/2 components of the V.32 Engine. This is a low level command which allows the controller to alter such things as the transmit level, transmit timing, receive timing, and receiver parameters, etc. The command consists of a single byte OPcode followed by a byte containing the address code for the desired register and a data byte for the addressed register. The data bytes will be transferred in the order received and interpreted by the addressed device. Refer to the data sheets of the TS68950, TS68951, and TS68952 for programming specifics.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	1	1	1

BYTE 1 DEFINITION

R	R	R	0	0	0	0	0

REG CODE (Refer to TS68950 Data Sheet).

BYTE 2 DEFINITION

*	*	*	*	*	*	*	*

DATA BYTE (Refer to TS68950 Data Sheet).

APPENDIX A

CFSK - configure for FSK Modes

INSTRUCTION TYPE
configuration control command

OPCODE
1D

SYNOPSIS
CFSK al orig atn mode ll

DESCRIPTION
CFSK is used to select the FSK mode of operation.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	1	1	0	1

BYTE 1 DEFINITION

0	0	0	0	AL	MOD1	MOD0	ORIG

BIT		DEFINITION
AL		Analog Loopback Enable
ORIG		Answer mode/Originate mode
MOD1	MOD0	
0	0	V.23
0	1	V.21
1	0	Bell103

BYTE 2 DEFINITION

ATN3	ATN2	ATN1	ATN0	0	0	LL	0

BIT	DEFINITION
ATN3-0	Transmit attenuation
LL	Leased line carrier detect
	0 –43dBm/–48dBm
	1 –33dBm/–38dBm

cv22B - configure for CCITT V.22Bis Mode, CCITT V.22 and Bell 212A

INSTRUCTION TYPE
configuration control command

OPCODE
1E

SYNOPSIS
cv22B al mode orig atn LL guard fallback

DESCRIPTION
cv22B is used to select the CCITT V.22Bis mode of operation. Select also, depending of Mode bits, the V.22, V.22 600bps and the Bell 212A.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	1	1	1	0

BYTE 1 DEFINITION

G1	G0	0	0	AL	MOD1	MOD0	ORIG

BIT		DEFINITION
AL		Analog Loopback Enable
MOD1	MOD0	Selected Mode
0	0	V.22Bis 2400bps
0	1	V.22 1200bps
1	0	Bell 212A 1200bps
1	1	V.22 600bps
ORIG		Answer mode/Originate mode
G1	G0	Guard tone selection
0	0	No tone
0	1	1800Hz
1	0	550Hz

BYTE 2 DEFINITION

ATN3	ATN2	ATN1	ATN0	0	0	LL	FB

BIT	DEFINITION
ATN3-0	Transmit attenuation
FB	Fallback mode for V.22bis
	0 disabled
	1 enabled
LL	Leased line carrier detect
	0 –43dBm/–48dBm
	1 –33dBm/–38dBm

APPENDIX A

cv32 - configure for V.32 Mode

INSTRUCTION TYPE
configuration control command

OPCODE
20

SYNOPSIS
cv32 speed ec orig atn al fc

DESCRIPTION
cv32 is used to alter the operating parameters of the V.32 Engine. The passed parameters provide a two bit speed code which selects the desired baud rate. Another parameter explicitly turns on or off the echo canceller. If the V.32 Engine is to operate in the originate mode, the orig parameter must be set. When this parameter is not set, the V.32 Engine is configured as an answer mode device. The al parameter allows the user to select the analog loopback test conditions. The transmit attenuation level is selected by the atn parameter. etc.

BYTE 0 DEFINITION (OP CODE)

0	0	1	0	0	0	0	0

BYTE 1 DEFINITION

RSV	RSV	FC	EC	AL	SP1	SP0	ORIG

SPEED CODE
SP1-0
00 : 9600 bps
10 : 9600 bps Treillis
01 : 4800 bps
11 : 2400 bps

FLAG	BIT	DEFINITION
FC	0/1	Do not/Do force cleardown
EC	0/1	Echo Canceller off/on
ORIG	0/1	Answer mode / Originate mode
AL	0/1	Analog Loopback test disabled / enabled
RSV	-	Reserved

BYTE 2 DEFINITION

ATN3	ATN2	ATN1	ATN0	RSV	RSV	RSV	RSV

FLAG		DEFINITION
ATN3-0		Transmit attenuation 0 dB to 22 dB : codes 0000 to 1011 in 2 dB steps Infinite : codes 1100 to 1111
RSV	-	Reserved

APPENDIX A

deft1 - define tone 1

INSTRUCTION TYPE
tone control command

OPCODE
0E

SYNOPSIS
deft tone descriptor

DESCRIPTION
deft1 is a command which used to program tone generator 1. The 16 bit value provided is used as the phase offset per baud for the generator. The deft1 command does not enable the tone generator. See also tgen.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	1	1	0

BYTE 1 DEFINITION

P7	P6	P5	P4	P3	P2	P1	P0

LOW BYTE OF DESCRIPTOR.

BYTE 2 DEFINITION

P15	P14	P13	P12	P11	P10	P9	P8

HI BYTE OF DESCRIPTOR.

deft2 - define tone 2

INSTRUCTION TYPE
tone control command

OPCODE
0F

SYNOPSIS
deft tone descriptor

DESCRIPTION
deft2 is a command which used to program tone generator 2. The 16 bit value provided is used as the phase offset per baud for the generator. The deft2 command does not enable the tone generator. See also tgen.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	1	1	1

BYTE 1 DEFINITION

P7	P6	P5	P4	P3	P2	P1	P0

LOW BYTE OF DESCRIPTOR.

BYTE 2 DEFINITION

P15	P14	P13	P12	P11	P10	P9	P8

HI BYTE OF DESCRIPTOR.

APPENDIX A

frez - Freeze the equalizer or echo canceller adaptation

INSTRUCTION TYPE
operational control command

OPCODES
16/17/1B/1C

SYNOPSIS
frez freeze code

DESCRIPTION
frez causes the V.32 Engine to enable or disable the adaptation of the equalizer and / or the echo canceller, to the parameter provided.

Frez includes four different opcodes, each one with a specific option :

Frezc (16) : Freeze the echo canceller adaptation

uFzec (17) : Unfreeze the echo canceller

Frezq (1B) : Freeze the equalizer adaptation

uFzeq (1C) : Unfreeze the equalizer

hshk - begin handshake sequence

INSTRUCTION TYPE
operational control command

OPCODE
040000

SYNOPSIS
hshk EA

DESCRIPTION
hshk is used to command the V.32 Engine to begin the handshake sequence processing. The progress of the handshake is reported to the control processor along with the data bits. For detailed information, refer to appendix B.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	1	0	0

BYTE 1 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	EA

EA : V.25Bis

0 enable V.25Bis generation/recognition

1 disable V.25Bis

APPENDIX A

init - Initialize the V.32 Engine

INSTRUCTION TYPE
operational control command

OPCODE
0600C0

SYNOPSIS
init

DESCRIPTION
init forces the V.32 Engine to reset all parameters to their default conditions and restart operations.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	1	1	0

BYTE 1 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION (OP CODE)

1	1	0	0	0	0	0	0

APPENDIX A

nop - no operation is specified

INSTRUCTION TYPE
operational control command

OPCODE
000000

SYNOPSIS
nop

DESCRIPTION
nop is used when communications with the V.32 Engine are required but no action is desired.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 1 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

rrr1 - Read MAFE register RR1

INSTRUCTION TYPE
MAFE manipulation command

OPCODE
080000

SYNOPSIS
rrr1

DESCRIPTION
rrr1 causes the V.32 Engine to read the 12 bit contents of the MAFE chipset register RR1. The data is returned in a standard three byte format. The least significant data byte is returned in byte 1, followed by the most significant data byte. Byte 0 is the standard response format (refer to appendix B) with DAV1 and DAV2 bits set to 1. Consult the data sheet of the TS68951 for the specifics of the returned data.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	0	0	0

BYTE 1 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

APPENDIX A

rrr2 - Read MAFE register RR2

INSTRUCTION TYPE
MAFE manipulation command

OPCODE
090000

SYNOPSIS
rrr2

DESCRIPTION
rrr2 causes the V.32 Engine to read the 12 bit contents of the MAFE chipset register RR2. The data is returned in a standard three byte format. The least significant data byte is returned in byte 1, followed by the most significant data byte. Byte 0 is the standard response format (refer to appendix B) with DAV1 and DAV2 bits set to 1. Consult the data sheet of the TS68951 for the specifics of the returned data.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	0	0	1

BYTE 1 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

rtra - force a retrain of the V.32 Engine

INSTRUCTION TYPE
operational control command

OPCODE
050000

SYNOPSIS
rtra fall

DESCRIPTION
rtra is used to force the V.32 Engine to initiate a retrain sequence on the channel.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	1	0	1

BYTE 1 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	FALL

Fallback (V.22Bis only)
1 Fallback to 1200Bps
0 goes up to 2400Bps

APPENDIX A

setgn - set global gain factor

INSTRUCTION TYPE
operational control command

OPCODE
02

SYNOPSIS
stegn gain value

DESCRIPTION
setgn is a command which used to scale the transmit samples. The 16 bit value provided is used as the multiplicative constant to be multiplied with each transmit sample.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	0	1	0

BYTE 1 DEFINITION

G7	G6	G5	G4	G3	G2	G1	G0

LOW BYTE OF GAIN VALUE.

BYTE 2 DEFINITION

G15	G14	G13	G12	G11	G10	G9	G8

HI BYTE OF GAIN VALUE.

slnt - Disable tone generators

INSTRUCTION TYPE
tone command

OPCODE
0D0000

SYNOPSIS
slnt

DESCRIPTION
slnt causes the V.32 Engine to disable the tone generators, thus stopping the tone output (i.e. send silence).

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	1	0	1

BYTE 1 DEFINITION

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

APPENDIX A

spac - Store Parameter And Count

INSTRUCTION TYPE
memory manipulation command

OPCODE
13

SYNOPSIS
spac lo-byte hi-byte

DESCRIPTION
spac is a command which used to write an arbitrary 16 bit value into the writable memory location currently specified by the Memory Address Register. The content of the Memory Address Register is incremented by 1 at the completion of command execution. See also WARP.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	0	0	1	1

BYTE 1 DEFINITION

D7	D6	D5	D4	D3	D2	D1	D0

LOW BYTE OF DATA.

BYTE 2 DEFINITION

D15	D14	D13	D12	D11	D10	D9	D8

HI BYTE OF DATA.

spam - Store Parameter in Addressed Memory

INSTRUCTION TYPE
memory manipulation command

OPCODE
12

SYNOPSIS
spam lo-byte hi-byte

DESCRIPTION
spam is a command which used to write an arbitrary 16 bit value into the writable memory location currently specified by the Memory Address Register. See also WARP.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	0	0	1	0

BYTE 1 DEFINITION

D7	D6	D5	D4	D3	D2	D1	D0

LOW BYTE OF DATA.

BYTE 2 DEFINITION

D15	D14	D13	D12	D11	D10	D9	D8

HI BYTE OF DATA.

APPENDIX A

tgen - Enable and disable tone generators

INSTRUCTION TYPE
tone control command

OPCODE
0D

SYNOPSIS
tgen tg code

DESCRIPTION
tgen causes the V.32 Engine to enable or disable tone generator 1 and tone generator 2, according to the parameter provided.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	1	0	1

BYTE 1 DEFINITION (TONE CODE)

0	0	0	0	0	0	TGC2	TGC1

TG CODE TGC2-1	TONE GEN 1	TONE GEN 2
00	disabled	disabled
01	enabled	disabled
10	disabled	enabled
11	enabled	enabled

tone - Select and transmit tone (s)

INSTRUCTION TYPE
tone select and command

OPCODE
0C

SYNOPSIS
tone tone code

DESCRIPTION
tone causes the V.32 Engine to program the tone generators for the specified tone or tones. The tones are defined by the tone code parameter passed in the second byte of the command. See also tonetab for the predefined single and double tones, and the commands deft and tgen for user definable tones and tone generator control.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	1	0	0

BYTE 1 DEFINITION (TONE CODE)

T7	T6	T5	T4	T3	T2	T1	T0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

Tone Code	Tone Parameters
0	DTMF 0 (941 & 1336 Hz)
1	DTMF 1 (697 & 1209 Hz)
2	DTMF 2 (697 & 1336 Hz)
3	DTMF 3 (697 & 1477 Hz)
4	DTMF 4 (770 & 1209 Hz)
5	DTMF 5 (770 & 1336 Hz)
6	DTMF 6 (770 & 1477 Hz)
7	DTMF 7 (852 & 1209 Hz)
8	DTMF 8 (852 & 1336 Hz)
9	DTMF 9 (852 & 1477 Hz)
A	(697 & 1633 Hz)
B	(770 & 1633 Hz)
C	(852 & 1633 Hz)
D	(941 & 1633 Hz)
E	DTMF * (941 & 1209 Hz)
F	DTMF # (941 & 1477 Hz)
10	Answer tone (2100 Hz)

APPENDIX A

warp - Write Address & Return Parameter

INSTRUCTION TYPE
memory manipulation command

OPCODE
10

SYNOPSIS
warp address

DESCRIPTION
warp is a command which is used to write the Memory Address Register of the V.32 Engine. The V.32 Engine responds with the contents of the addressed location. The data is returned in a standard three byte transfer. The least significant data byte is returned in the byte 1, followed by the most significant data byte. Byte 0 is the standard response format (refer to appendix B) with DAV1 and DAV2 bits set to 1.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	0	0	0	0

BYTE 1 DEFINITION

A7	A6	A5	A4	A3	A2	A1	A0

LOW BYTE OF DATA.

BYTE 2 DEFINITION

P1	P0	M1	M0	A11	A10	A9	A8

PROC CODE P1-0	MEM CODE M1-0	ADDRESS HI A11-A8
00 : Master	00 : XRAM	
10 : Receiver	01 : YRAM	
01 : Echo Canceller	10 : EMEM	
	11 : CROM	

warpx - Write Address & Return Parameter Complex

INSTRUCTION TYPE
memory manipulation command

OPCODE
11

SYNOPSIS
warpx address

DESCRIPTION
warpx is a command which is used to write the Memory Address Register of the V.32 Engine. The V.32 Engine responds with the contents of the most significant bytes of the addressed location and the addressed location + 1. The data is returned in a standard three byte transfer. Byte 0 is the standard response format (refer to appendix B) with DAV1 and DAV2 bits set to 1. Byte 1 is used to return the 8 most significant bits contained in the addressed location. The 8 most significant bits of the addressed location + 1 are returned in byte 2.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	0	0	0	1

BYTE 1 DEFINITION

A7	A6	A5	A4	A3	A2	A1	A0

LOW BYTE OF DATA.

BYTE 2 DEFINITION

P1	P0	M1	M0	A11	A10	A9	A8

PROC CODE P1-0	MEM CODE M1-0	ADDRESS HI A11-A8
00 : Master	00 : XRAM	
10 : Receiver	01 : YRAM	
01 : Echo Canceller	10 : EMEM	
	11 : CROM	

APPENDIX A

wtr1 - Write MAFE register TR1

INSTRUCTION TYPE
MAFE manipulation command

OPCODE
0A

SYNOPSIS
wtr1

DESCRIPTION
wtr1 causes the V.32 Engine to take the two supplied data bytes and write them in sequence to the MAFE chipset register TR1.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	0	1	0

BYTE 1 DEFINITION (DATA)

D3	D2	D1	D0	0	0	0	0

BYTE 2 DEFINITION (DATA)

D11	D10	D9	D8	D7	D6	D5	D4

wtr2 - Write MAFE register TR2

INSTRUCTION TYPE
MAFE manipulation command

OPCODE
0B

SYNOPSIS
wtr2

DESCRIPTION
wtr2 causes the V.32 Engine to take the two supplied data bytes and write them in sequence to the MAFE chipset register TR2.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	0	1	1

BYTE 1 DEFINITION (DATA)

D3	D2	D1	D0	0	0	0	0

BYTE 2 DEFINITION (DATA)

D11	D10	D9	D8	D7	D6	D5	D4

APPENDIX A

xmit - transmit data to other modem

INSTRUCTION TYPE
data communications command

OPCODE
03

SYNOPSIS
xmit data

DESCRIPTION
xmit is used to command the V.32 Engine to send data. The OP code for the xmit command is a single byte. The data bits to be transmitted are stored in the second byte, where D0 is the first bit to be transmitted.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	0	0	1

BYTE 1 DEFINITION

D7	D6	D5	D4	D3	D2	D1	D0

D0-D7 DATA BITS

BYTE 2 DEFINITION

0	0	0	0	0	0	0	0

xmiti - transmit data to other modem and initiate additional cycle

INSTRUCTION TYPE
data communications command

OPCODE
01

SYNOPSIS
xmit data

DESCRIPTION
xmit is used to command the V.32 Engine to send data. The OP code for the xmit command is a single byte. The data bits to be transmitted are stored in the second byte, where D0 is the first bit to be transmitted.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	0	1	1

BYTE 1 DEFINITION

D7	D6	D5	D4	D3	D2	D1	D0

D0-D7 DATA BITS

BYTE 2 DEFINITION

0	0	0	0	0	0	0	0

APPENDIX B
STATUS REPORTING DESCRIPTION

BYTE 0 DEFINITION

F11	F10	F01	F00	DAV2	DAV1	H	CD

FLAG CODE F01-00	CALL ESTABLISH	HANDSHAKE OPERATIONS	DATA XFER OPERATIONS
00	no tones	line quality is good	line quality is good
01	Band 1 detected	line terrible (local retrain req.)	line quality is poor
10	Band 2 detected	time out	line terrible (local retrain req.)
11	Both bands detected	line cleardown (V.32 only)	remote retrain sequence detected
F11-10			
00	reserved	9600 bps no trellis or 2400bps	reserved
01	Answer tone detected	4800 bps or 1200bps	reserved
10	V.32 : AC detected	9600 bps trellis	reserved
11	reserved	2400 bps	reserved

DAV1	DAV2	DEFINITION
0	0	Data is in byte 1 and 2.
0	1	Data is in byte 1 and status word in byte 2.
1	0	No data bits and status word is in byte 2.
1	1	Answer to the last command is in bytes 1 and 2.

FLAG	BIT	DEFINITION
H	0/1	Handshake is not/is in progress
CD	0/1	Set circuit 107 off/on (V.32) Set circuit 109 on/off (V.22Bis)

BYTE 1 DEFINITION

RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

BYTE 2 DEFINITION

ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0

FLAG CODE F01-00	HANDSHAKE OPERATIONS				DATA XFER OPERATIONS
	V.32		V.22Bis		When DAV1, DAV2 bits are 0 an additional byte of receive data is available.
	ANSWER	ORIGINATE	ANSWER	ORIGINATE	
ST7	AA	AC	–	Unscr. 1	
ST6	AA - CC	AC - CA	S1	S1	
ST5	silence	CA - AC	"1", 1.2K	"1", 1.2 K	
ST4	$\overline{S}$	$\overline{S}$	"1", 2.4K	"1", 2.4 K	
ST3	$\overline{S/S}$	$\overline{S/S}$	–	–	
ST2	R2	R1	–	–	
ST1	R3	–	–	–	
ST0	E	E	–	–	

APPENDIX C

This appendix describes the interconnection between the different chips (in DIP package).

SYSTEM INTERFACE

Signal Name	Chip/Pin	Description
DOH..D7H	TS75C321/27..34	System Data Bus : connect to host processor.
CSL	TS75C321/21	Chip Select : connect to host processor.
RSL	TS75C321/22	Register Select : connect to host processor.
DSL	TS75C321/20	Data Strobe : connect to host.
RWL	TS75C321/19	Read/Write : connect to host.
INTL	TS75C321/24	Interrupt Request : connect to host processor
RSTL1 RSTL2 RSTL0	TS75C321/23 TS75C322/23 TS75C320/23	Reset : connect to host processor. Reset Reset

CLOCK SIGNAL

Signal Name	Chip/Pin	Description
TxRCLK	TS68952/16 TS75C321/26	Transmit baud clock.
TxCCLK	TS68952/24 TS75C321/44 TS68950/19 TS68951/23	Transmit conversion clock.
RxRCLK	TS68952/20 TS75C321/43 TS75C322/44	Receive baud clock.
RxCCLK	TS68952/21 TS75C321/25 TS75C322/43 TS68951/22	Receive conversion clock.
TxSCLK	TS68952/11	If not used must be grounded.
XTL1	TS68952/13	External crystal input : must be connected via a 5.76 MHz crystal to XTL2.
XTL2	TS68952/14	External Crystal Input
CLK	TS68952/15 TS68950/18 TS68951/21	Main analog clock : this output, in accordance with the XTL1/2 crystal, must be 1.4 MHz (+ - 7Hz).
25 MHz	TS75C320/15 TS75C321/15 TS75C322/15	Main digital clock : connect to a 25 MHz oscillator.
TxCCLK RxCCLK	TS68952/23 TS68952/22	Transmit bit clock. Receive bit clock.

APPENDIX C

ANALOG SIGNALS

Signal Name	Chip/pin	Description
ATO	TS68950/15	Analog Transmit Output : connect to DAA.
EEO^T	TS68950/16 TS68951/11	Analog echo cancelling estimation.
LEI	TS68951/17	Local Echo Input : must be grounded.
RAI	TS68951/16	Receive Analog Input : connect to DAA.
RFO	TS68951/13	This pin must be connected throught a 1 µF nonpolarised capacitor to AGC1 input.
AGC1	TS68951/12	
AGC2	TS68951/19	Connect to the analog ground through a 1 µF nonpolarised capacitor.
CD1	TS68951/18	Connect to the analog ground through a 1 µF nonpolarised capacitor.

Caution : T The connection between EEO (TS68950/16) and EEI (TS68951/11) must be as close as possible to avoid parasitics on echo estimate signal.

INTER DSP AND EXTERNAL MEMORY CONNECTION

Signal Name	Chip/Pin	Description
0D0..0D15	TS75C320/45..48,1..12 RAM0/IO0..IO15	Data Bus
1D8..1D15	TS75C321/5..12 TS75C320/27..34 RAM0/AD0..AD7 TS68950/20..24, 1..3	Data and Address Buses
1D0..1D7	TS75C321/45..48, 1..4 TS75C322/27..34 RAM2/AD0..AD7	Data and Address Buses
2D9..2D15	TS75C322/6..12 TS68951/25..28, 1..3 TS68952/25..28, 1..3 RAM2/IO9..IO15	Data Bus
2D8	TS75C322/5 TS68951/24 RAM2/IO8	Data Pin
2D0..2D7	TS75C322/45..48, 1..4 RAM2/IO0..IO7	Data Bus
1A11	TS75C321/39 TS75C320/21 TS75C322/21 TS68950/7	Address Line
1A10	TS75C321/37 TS68950/6	Adress Line
1A9	TS75C321/36 TS68950/9 TS75C320/22	Address Line

Note : RAM0 Refer to DSP0 4Kx16 External memory.
RAM2 Refer to DSP2 2Kx16 External memory.

Where : IO is bidirectional data bus
AD is address line
WEL is Write Enable (active low)
OEL is Chip Select (active low)

APPENDIX C

INTER DSP AND EXTERNAL MEMORY CONNECTION (continued)

Signal Name	Chip/Pin	Description
1A8	TS75C321/35 TS68950/8 TS75C322/22	Address Line
1RWL	TS75C321/18 TS75C320/19 TS75C322/19 TS68950/5	Control Line
1DSL	TS75C321/17 TS75C320/20 TS75C322/20 TS68950/4	Control Line
0A8..0A11	TS75C320/35..37,39 RAM0/AD8..AD11	Address Line
0DSL	TS75C320/17 RAM0/CEL	Control Line
0RWL	TS75C320/18 RAM0/WEL	Control Line
2A8..2A11	TS75C322/35..37,39 TS68951/8,9,6,7 TS68952/8,9,6,7 RAM2/A8..A10,CEL	Address Line
2DSL	TS75C322/17 TS68951/4 TS68952/4 RAM2/OEL	Control Line
2RWL	TS75C322/18 TS68951/5 TS68952/5 RAM2/WEL	Control Line
0IRQL	TS75C320/24 TS75C321/42	Synchro Line
2IRQL	TS75C322/24 TS75C321/41	Synchro Line

Note : RAM0 Refer to DSP0 4Kx16 External memory.
RAM2 Refer to DSP2 2Kx16 External memory.

Where : IO is bidirectional data bus
AD is address line
WEL is Write Enable (active low)
CEL is Chip Select (active low)
OEL is Output Enable (active low)

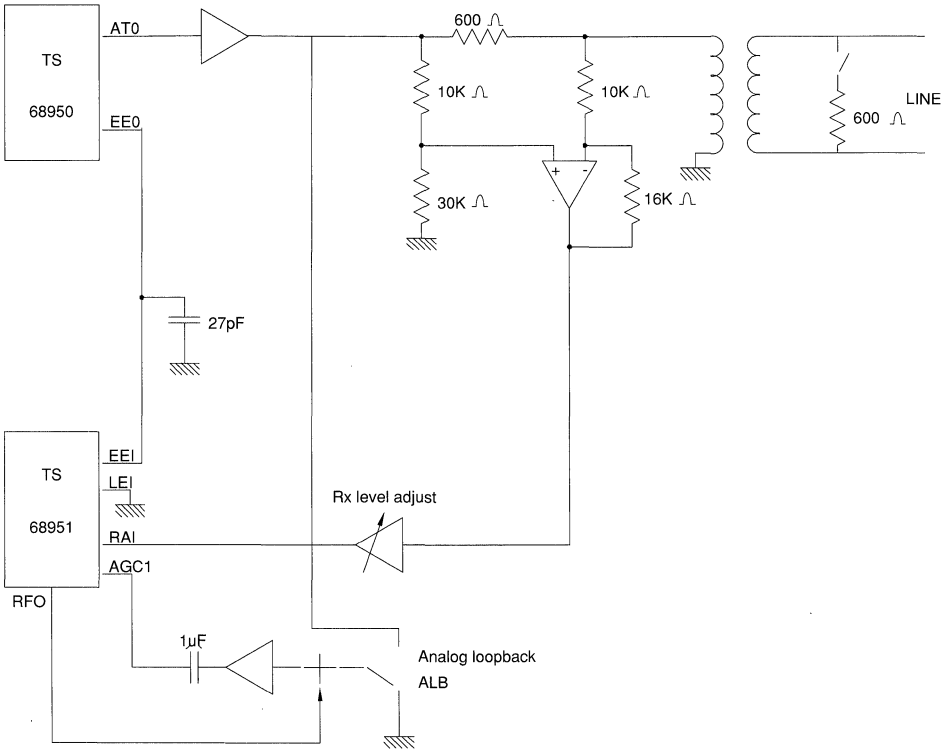
APPENDIX C

POWER SUPPLY AND MISCELLANEOUS

Signal Name	Chip/Pin	Description
+ 5VA	TS68951/20 TS68950/17	Positive Analog Power Supply
- 5VA	TS68951/14 TS68950/12	Negative Analog Power Supply
AGND	TS68950/13 TS68951/15	Analog Ground
VCC	TS75C320/38 TS75C321/38 TS75C322/38 TS68952/17	Main Digital Power Supply
DGND	TS75C320/13 TS75C321/13 TS75C322/13 TS68950/10 TS68951/10 TS68952/12	Digital Ground Power Supply
xtal	TS75C320/14 TS75C321/14 TS75C322/14	Not Connected (must be left open)
Clkout	TS75C320/16 TS75C321/16 TS75C322/16	Not Connected (25 MHz/4)
TO	TS68952/10	Not Connected (must be left open)
AGND	TS68950/14	Auxiliary Input
DGND	TS75C321/40 TS75C320/40..44 TS75C320/25..26 TS75C322/40..42 TS75C322/25..26 TS68950/11	Not Used

APPENDIX C

Figure 9 : Analog Path.



APPENDIX D
REFERENCES

[1] CCITT recommendation V.32.
[2] CCITT recommendation V.54.
[3] Data sheet of the TS75320 , V.32 modem echo canceller, SGS - THOMSON Microelectronics.
[4] Data sheet of the ST18930/31 programmable signal processor, SGS - THOMSON Microelectronics.
[5] Data sheet of the TS68950 transmitter interface chip, SGS - THOMSON Microelectronics.
[6] Data sheet of the TS68951 receiver interface chip, SGS - THOMSON Microelectronics.
[7] Data sheet of the TS68952 clock generation chip, SGS - THOMSON Microelectronics.
[8] Application guide : Using the TS75320 Echo canceller in V.32 modems, SGS - THOMSON Microelectronics.

MODEM TRANSMIT ANALOG INTERFACE

- TWO CHANNEL DIGITAL TO ANALOG CONVERTER FOR TRANSMISSION OF DIGITAL DATA TO THE TELEPHONE LINE AND ECHO CANCELLATION
- 6TH ORDER SWITCHED CAPACITOR LOW PASS FILTER FOR ADAPTATION TO THE TELEPHONE BANDWIDTH
- OUTPUT CONTINUOUS TIME SMOOTHING FILTER
- PROGRAMMABLE TRANSMIT OUTPUT ATTENUATION OVER A 22dB RANGE WITH 2dB STEPS.
- DIRECT INTERFACE WITH DSP STANDARD MPU 8-BIT BUS
- LOW POWER CMOS TECHNOLOGY
- AVAILABLE IN DIL OR SURFACE MOUNT PACKAGE

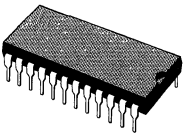
DESCRIPTION

The TS68950 is a Transmit (Tx) Analog Front-End circuit designed to implement the filtering and digital to analog conversion required by high speed voice-band modems, telephony or speech coding applications using digital signal processing technology.

The TS68950 copes with all the CCITT recommendations from V.21 to V.33 including full-duplex recommendations with echo-cancellation (V.32) thanks to its second transmit channel.

Used in conjunction with the TS68951 Receive (Rx) Analog Front-End circuit and the TS68952 clock generator*, it provides a very economic and efficient interface to digital signal processing functions in high speed modems or telephony applications.

* The interconnection between the 3 MAFE chips is detailed p11/18.



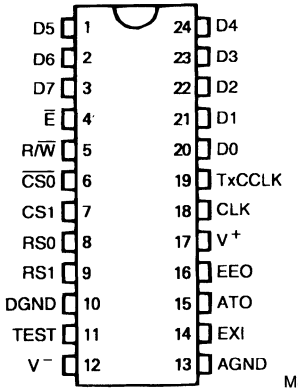
P
DIP24
(Plastic Package)

FN
PLCC28
(Plastic Package)

(Ordering Information at the end of the datasheet)

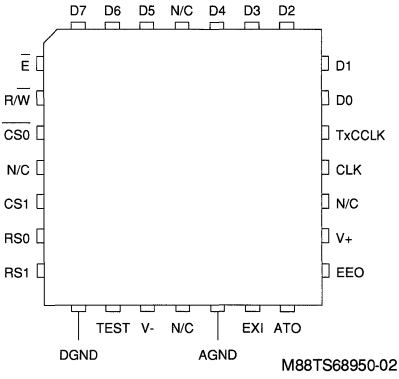
PIN CONNECTIONS

DIP24



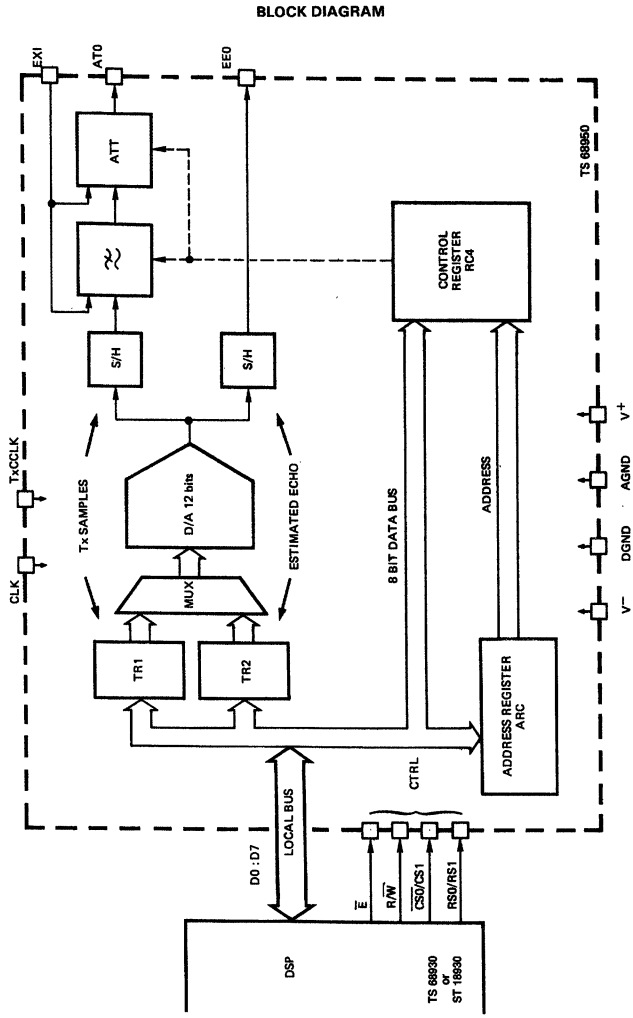
M88TS68950-01

PLCC28



M88TS68950-02

BLOCK DIAGRAM



M88TS68950-03

PIN DESCRIPTION

Name	Function
D5-D7	8 bit data bus inputs giving access to Tx, estimated echo, control and address registers.
$\overline{E}$	Enable Input. Datas are strobed on the positive transitions of this input.
R/$\overline{W}$	Read/$\overline{\text{Write}}$ Selection Input. Internal registers can be written when R/$\overline{W}$ = 0. Read mode is not used.
$\overline{CS0}$-CS1	Chip Select Inputs. The chip set is selected when $\overline{CS0}$ = 0 and CS1 = 1
RS0-RS1	Register Select Inputs. Used to select D/A input registers or control/address registers in the write mode.
DGND	Digital Ground = 0 V. All digital signals are referenced to this pin.
TEST	Test Input. Used to reduce testing time. This Pin must be connected to DGND in all applications.
V^-	Negative Power Supply Voltage = – 5 V ± 5 %
AGND	Analog Ground = 0 V. Reference point for analog signals.
EXI	Programmable analog input tied to filter or attenuator input according to the RC4 register content.
ATO	Analog Transmit Output
EEO	Analog Echo Cancelling Output (estimated echo)
V^+	Positive Power Supply Voltage : + 5 V ± 5 %
CLK	1.44 MHz Clock Input. Used for internal sequencing.
TxCCLK	Transmit Conversion Clock Input. Must be derived from CLK.
D0-D4	See pins D5-D7.

DEVICE OPERATION

The TS68950 is a transmit analog interface circuit dedicated to voice-grade MODEMs, telephony and speech applications. The TS68950, the TS68951 (receive analog front-end circuit) and the TS68952 (clock generator) constitute an analog front-end chip set useful for implementation of synchronous modems operating on two or four wires according to the CCITT V.26, V.26bis, V.27, V.27bis, V.27ter and V.29 recommandations or BELL 208 and 209 standards, or on two wires full-duplex according to CCITT V.22, V.22 bis or BELL 212A (split band) and CCITT V.26 ter and V.32 (echo cancelling). The chipset can also be used for asynchronous recommendations such as V.21, V.23, Bell 103.

By receiving digital samples from a DSP like the ST 8930/31, the TS68950 delivers two analog signals : the transmitted (Tx) signal that will be sent on the line and the estimated echo signal that will be subtracted from the received (Rx) signal on the TS68951 Rx chip.

The digital Tx and estimated echo samples are converted to analog during the low state and the high state of the TxCCLK clock, respectively.

MAIN FUNCTIONS (see block diagram)

- 12 bit digital to analog converter multiplexed on two channels.
- Tx signal sample and hold running with Tx sampling frequency TxCCLK.
- Tx low-pass filter with continuous-time smoothing.
- Programmable attenuator from 0 to –22 dB with 2 dB steps.
- Estimated echo sample and hold running with Tx sampling frequency TxCCLK.

DSP INTERFACE SIGNALS

The TS68950 interfaces to the signal processor via an 8 bit data bus (only used in writing mode), two chip select lines, two register select lines, a read/write line and an enable line.

Data bus (D0-D7) - The write only data lines allow the transfer of data from the DSP to the TS68950. Input buffers are high-impedance devices.

Enable ($\overline{E}$) - The enable pulse ($\overline{E}$) is the basic timing signal that is supplied to the TS68950. All the other

signals are referenced to the leading and trailing edges of the E pulse.

Read/Write (R/W) - This signal is generated by the DSP to control the direction of data transfers on the data bus. A low level state on the TS68950 read/write line enables the input buffers and data is transferred from the DSP to the TS68950 on the E signal if the circuit has been selected. The device is unselected when a high level signal is applied to the R/W pin.

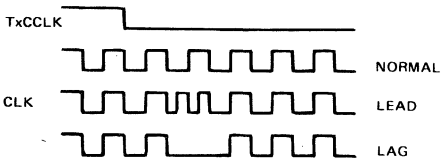
Chip Select (CS0, CS1) - These two input signals are used to select the chip. CS0 must be low and CS1 must be high for selection of the device. Data transfers are then performed under the control of the enable and R/W signals. The chip select lines must be stable for the duration of the E pulse.

Register Select (RS0, RS1) - The two register select lines are used to access the different registers inside the chip. For instance these two lines are used in conjunction with the internal control register ARC to select a particular register RC4. The register select lines must be stable when the E signal is low.

CLOCK INTERFACE BETWEEN TS68950 AND TS68952

The TS68950 receives two clock lines from the clock generator TS68952.

MASTER CLOCK SEQUENCING (CLK) : The typical frequency is 1.44 MHz but the recurrence frequency must be an exact multiple of the terminal clock frequency. The TxDPLL included in the clock generator circuit (TS68952) operates by adding or subtracting pulses to a 2.88 MHz internal clock. This corresponds to phase leads or phase lags of about 350 ns duration. To ensure correct device operation, clock synchronization must be done immediately after the negative-going transition of TxCCLK clock.



M88TS68950-04

TRANSMIT CONVERSION CLOCK (TxCCLK) : The conversion clock TxCCLK must be derived from the master clock CLK. Three nominal values are possible : 9.6 kHz, 8 kHz and 7.2 kHz. 9.6 kHz is the highest allowable frequency.

To run properly the TxCCLK clock must be a submultiple of CLK/5:

TxCCLK x 5 x N = CLK (with N integer) : This is ensured when using the TS68952 clock generator.

The sampling clock of the switched capacitor filter section is obtained by dividing the CLK frequency by five and performing internal synchronization on the leading edges of TxCCLK.

The Tx samples are converted from digital to analog during the low state of TxCCLK. The estimated echo samples are converted during the high state of TxCCLK.

INTERNAL CONTROLS

POWER-ON : The chip contains internal power-on reset logic to initialize the RC4 control register in order to avoid undesirable signal transmission on the telephone line with infinite attenuation.

INTERNAL ADDRESSING

RS0	RS1	Access	Write Cycle Number
0	0	TR1 Transmitted Sample Register	2
0	1	TR2 Estimated Echo Sample Register	2
1	0	ARC Address Register	1
1	1	RC4 Control Register (if addressed by ARC)	1

SAMPLE REGISTERS (TR1 AND TR2) : TR1 is the transmitted sample register and TR2 the estimated echo sample register. TR1 and TR2 store two's complement 12 bit data (DAC0 to DAC11). As indicated below, writing each sample requires two cycles.

First Cycle

D7	D6	D5	D4	D3	D2	D1	D0
DAC 3	DAC 2	DAC 1	DAC 0	X	X	X	X

Second Cycle

DAC 11	DAC 10	DAC 9	DAC 8	DAC 7	DAC 6	DAC 5	DAC 4

An internal flip-flop is used to select the first or the second byte. It advances one count on the positive-going edge of the E pulse when the sample registers are selected (CS0 = 0, CS1 = 1 and RS0 = 0). When the sample registers are disabled, the latch is reset on any E positive-going edge.

Both TR1 and TR2 registers are sampled by the DAC on the falling edge of TxCCLK. Therefore their contents must remain stable during this edge.

CONTROL REGISTER (RC4) : The RC4 control register has two different functions. Its four most significant bits give the transmit attenuator gain following the table below.

RC4 REGISTER

D7	D6	D5	D4	D3	D2	D1	D0	Attenuation (dB)
ATT 4	ATT 3	ATT 2	ATT 1		EM 2	EM 1		
0	0	0	0					0
0	0	0	1					2
0	0	1	0					4
0	0	1	1					6
0	1	0	0					8
0	1	0	1					10
0	1	1	0					12
0	1	1	1					14
1	0	0	0					16
1	0	0	1					18
1	0	1	0					20
1	0	1	1					22
1	1	0	0					Infinite
1	1	0	1					Infinite
1	1	1	0					Infinite
1	1	1	1					Infinite

Depending on the EM1 and EM2 states in the RC4 register, the programmable analog input (EXI) can be connected to the filter input or to the transmit attenuator input.

RC4 REGISTER

D7	D6	D5	D4	D3	D2	D1	D0	EXI INPUT
ATT 4	ATT 3	ATT 2	ATT 1	–	EM 2	EM 1	–	
					0	0		Disabled
					0	1		Transmit Filter Input
					1	0		Transmit Attenuator Input
					1	1		Disabled

Following power-up, all RC4 bits are preset at one : EXI input is disabled and the transmit signal is cancelled.

D0 and D3 bits are not used in the RC4 register.

ADDRESS REGISTER (ARC) : The address register stores 3 bits (D5, D6 and D7). Among the 8 possible addresses, only one is used inside the TS68950 (RC4 address).

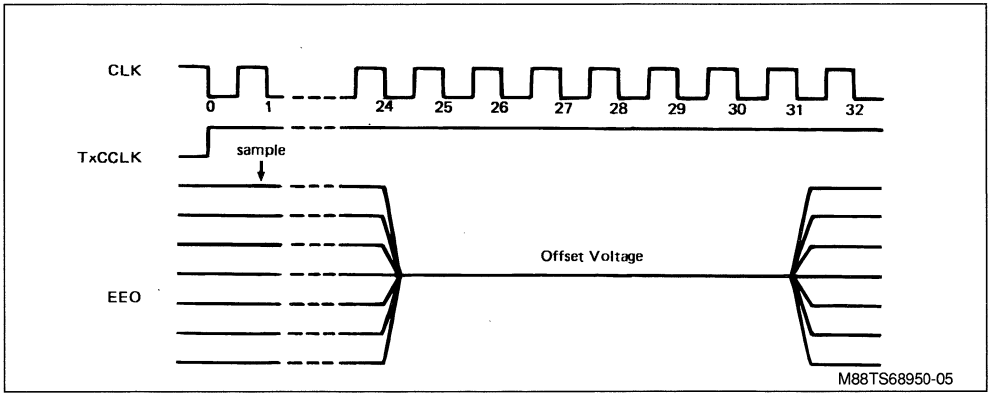
RC 4

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	X	X	X	X	X

X : don't care

The address of the ARC register is automatically increased by one each time the control register is accessed. This allows indirect or cyclical addressing to RC4.

EEO OUTPUT WAVEFORM



The EEO output is not valid during S/H sampling. The output presents at this time the S/H offset voltage.

This offset voltage appears at the 24th CLK period after rise transition of TxCCLK and disappears at the 31th.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
	DGND Digital Ground to AGND Analog Ground	– 0.3 to + 0.3	V
	V^+ Supply Voltage to DGND or AGND Ground	– 0.3 to + 7	V
	V^- Supply Voltage to DGND or AGND Ground	– 7 to + 0.3	V
V_I	Voltage at any Digital Input or Output	DGND – 0.3 to V^+ + 0.3	V
V_{in}	Voltage at any Analog Input or Output	V^- – 0.3 to V^+ + 0.3	V
I_{out}	Analog Output Current	– 10 to + 10	mA
P_{tot}	Power Dissipation	500	mW
t_{amb}	Operating Temperature Range	0 to + 70	°C
t_{stot}	Storage Temperature Range	– 65 to + 150	°C
t_{sold}	Pin Temperature (soldering 10 s.)	+ 260	°C

Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard CMOS handling procedures should be employed to avoid possible damage to device.

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V^+	Positive Supply Voltage	4.75	5	5.25	V
V^-	Negative Supply Voltage	– 5.25	– 5.0	– 4.75	V
I^+	V^+ Operating Current			15	mA
I^-	V^- Operating Current	– 15			mA

D.C. AND OPERATING CHARACTERISTICS

Unless otherwise noted, electrical characteristics are specified over the operating range. Typical values are given for $V^+ = +5V$, $V^- = -5V$ and $T_{amb} = 25\ ^\circ C$.

DIGITAL INTERFACE

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level Voltage			0.8	V
V_{IH}	Input High Level Voltage	2.2			V
I_{IL}	Input Low Level Current $DGND < V_I < V_{IL\ max}$	– 10		10	µA
I_{IH}	Input High Level Current $V_{IH\ min} < V_I < V^+$	– 10		10	µA

ANALOG INTERFACE, EXI PROGRAMMABLE INPUT

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{in}	Input Voltage Swing	– 2.5		+ 2.5	V
I_{in}	Input Current (input Tx filter selected)	– 10		+ 10	µA
C_{in}	Input Capacitance (input ATT selected) f < 50 kHz f > 50 kHz			 50 20	 pF pF
R_{in}	Input Resistance (input ATT selected)	20			kΩ

ANALOG INTERFACE, ATO TRANSMIT OUTPUT

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{os}	Output DC Offset	– 250		+ 250	mV
C_L	Load Capacitance			50	pF
R_L	Load Resistance	1200			Ω
V_{out}	Output Voltage Swing R_L > 1200 Ω and C_L < 50 pF	– 2.5		+ 2.5	V
R_{out}	Output Resistance			5	Ω

ANALOG INTERFACE, EEO ESTIMATED ECHO OUTPUT

Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{os}	Output DC Offset	– 100		+ 100	mV
C_L	Load Capacitance			50	pF
R_L	Load Resistance	10			kΩ
V_{out}	Output Voltage Swing R_L > 10 kΩ and C_L < 50 pF	– 2.5		+ 2.5	V
R_{out}	Output Resistance	350	500	650	Ω

DAC TRANSFER CHARACTERISTICS

Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
	Converter Resolution		12		Bit
V_{out}(max)	Nominal Output Peak to Peak Amplitude		5.0		V
LSB	Least Significant Bit Amplitude		1.2		mV
	Integral Linearity Error	– 1		+ 1	LSB
	Differential Linearity Error	– 0.7		+ 0.7	LSB

TRANSMIT FILTER TRANSFER CHARACTERISTICS (see appendix 1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
G_{AR}	Absolute Passband Gain at 1 kHz		0		dB
G_{RR}	Gain Relative to Gain at 1 kHz without Sin x/x Correction of DAC Sampling				
	Below 3100 Hz	− 0.5		0.2	dB
	3200 Hz	− 3			dB
	4000 Hz			− 36	dB
	5000 Hz to 12000 Hz			− 46	dB
D_{AR}	Absolute Group Delay 600 Hz to 3000 Hz	160		680	µs

ATTENUATOR TRANSFER CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
A_{TT}	Absolute Gain at 0 dB Nominal Value		0		dB
R_{AT}	Attenuation Relative to Nominal Value	− 0.5		+ 0.5	dB
B_{AT}	Maximum Attenuation	40			dB

GENERAL TRANSFER CHARACTERISTICS (from DATA BUS to ATO)

Symbol	Parameter	Min.	Typ.	Max.	Unit
G_{EX}	ATO Absolute Gain at 1 kHz	− 0.5	0	+ 0.5	dB
	ATO Psophometric Noise			200	µV
	ATO Positive Power Supply Rejection Ratio V_{ac} = 200 mVpp f = 1 kHz		40		dB
	ATO Negative Power Supply Rejection Ratio V_{ac} = 200 mVpp f = 1 kHz		40		dB
	Signal to Harmonic Distorsion Ratio (psophometric band)	60			dB

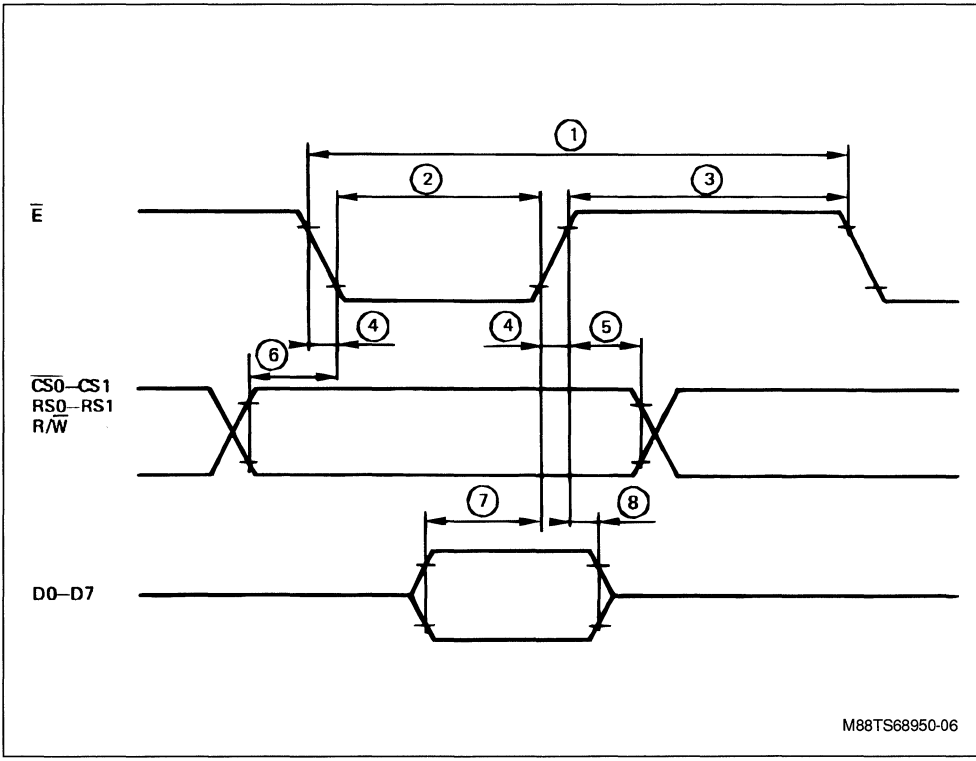
GENERAL TRANSFER CHARACTERISTICS (from DATA BUS to EEO)

Symbol	Parameter	Min.	Typ.	Max.	Unit
G_{AX}	EEO Absolute Gain at 1 kHz	− 0.5	0	+ 0.5	dB
	EEO Psophometric Noise			200	µV
	EEO Positive Power Supply Rejection Ratio V_{ac} = 200 mVpp f = 1 kHz		40		dB
	EEO Negative Power Supply Rejection Ratio V_{ac} = 200 mVpp f = 1 kHz		40		dB

BUS TIMING CHARACTERISTICS (see notes 1 and 2)

Symbol	Parameter	Min.	Max.	Unit
t_{cyc} (1)	Cycle Time	320		ns
t_{WEL} (2)	Pulse Width, $\overline{E}$ Low Level	180		ns
t_{WEH} (3)	Pulse Width, $\overline{E}$ High Level	100		ns
t_r, t_f (4)	Clock Rise and Fall Time		20	ns
t_{HCE} (5)	Control Signal Hold Time	10		ns
t_{SCE} (6)	Control Signal Set-up Time	40		ns
t_{SDI} (7)	Input Data Set-up Time	120		ns
t_{HDI} (8)	Input Data Hold Time	10		ns

Figure 1 : Bus Timing.

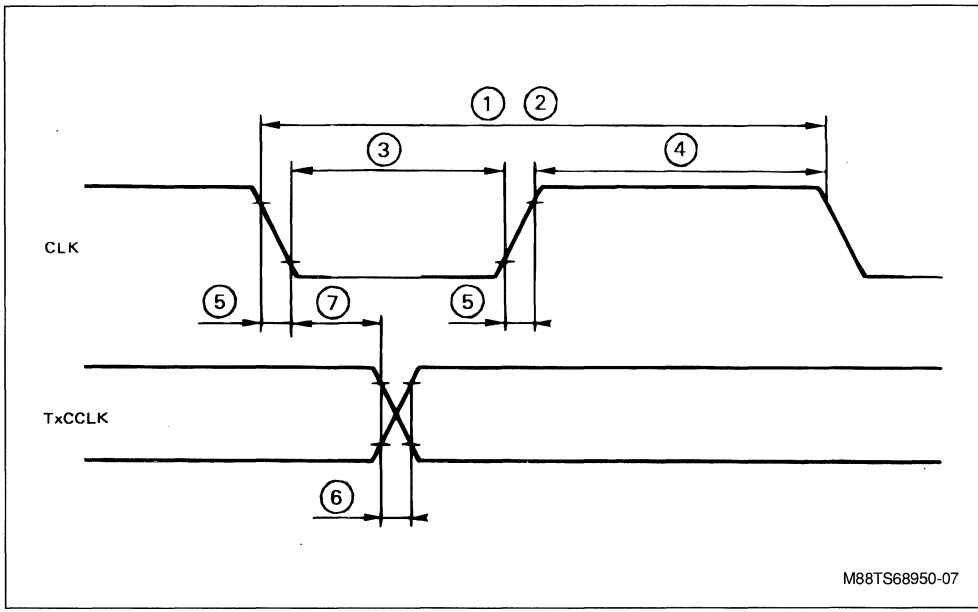


Notes : 1. Voltage levels shown are $V_L < 0.4$ V, $V_H > 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.2 V, unless otherwise specified.

CLOCK TIMING CHARACTERISTICS

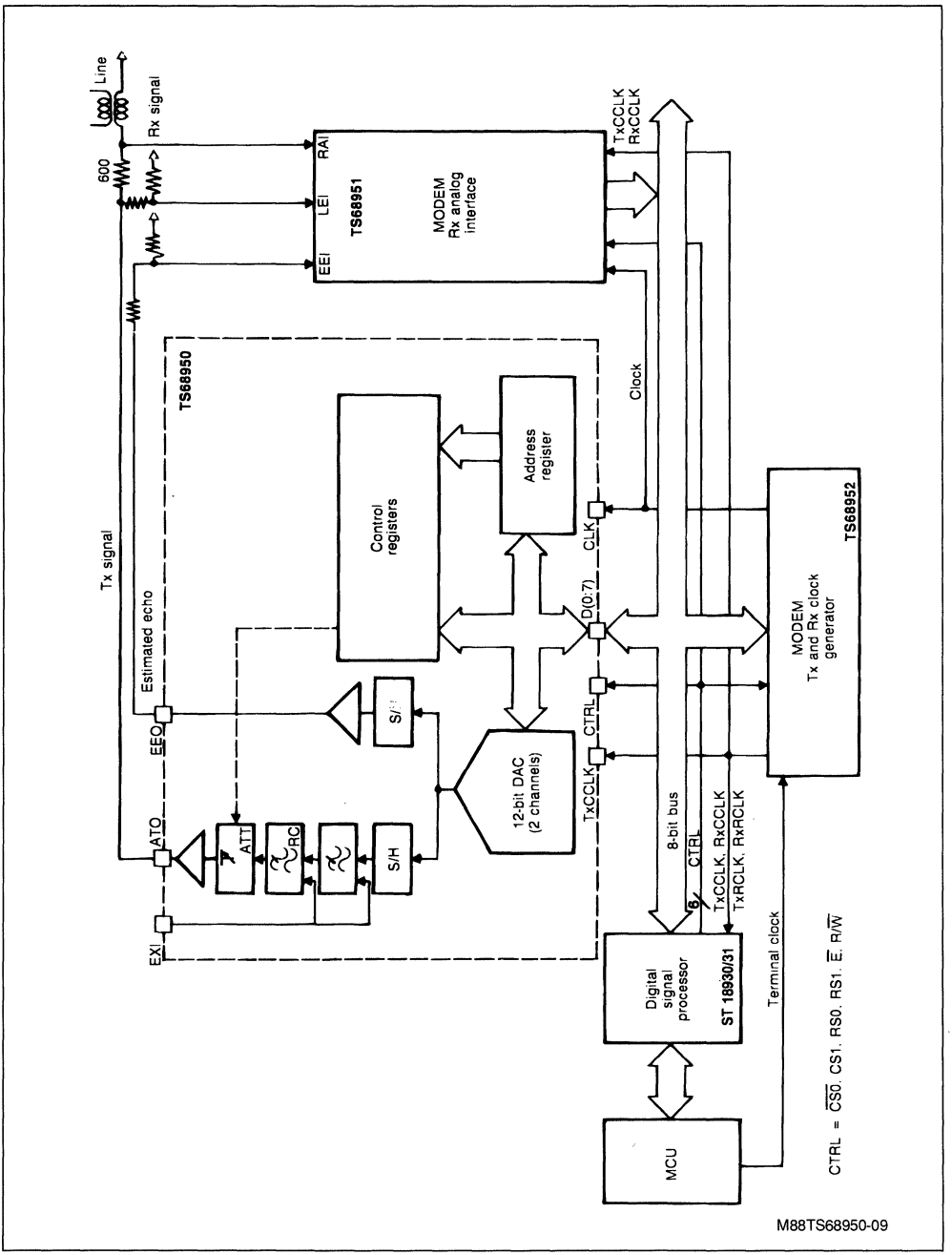
Symbol	Parameter	Min.	Typ.	Max.	Unit
P_C (1)	CLK Clock Period		695		ns
P_{CL} (2)	CLK During Phase Lead on DPLL		348		ns
t_{WCL} (3)	CLK Low Level Width	150			ns
t_{WCH} (4)	CLK High Level Width	150			ns
t_{RC}, t_{FC} (5)	CLK Rise and Fall Time			100	ns
t_{RT}, t_{FT} (6)	TxCCLK Rise and Fall Time			100	ns
t_{DC} (7)	TxCCLK Delay Time	20		130	ns

Figure 2 : Clock Timing.



Notes : 1. Voltage levels are $V_L < 0.4$ V, $V_H > 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.2 V, unless otherwise specified.

APPLICATIONS INFORMATION

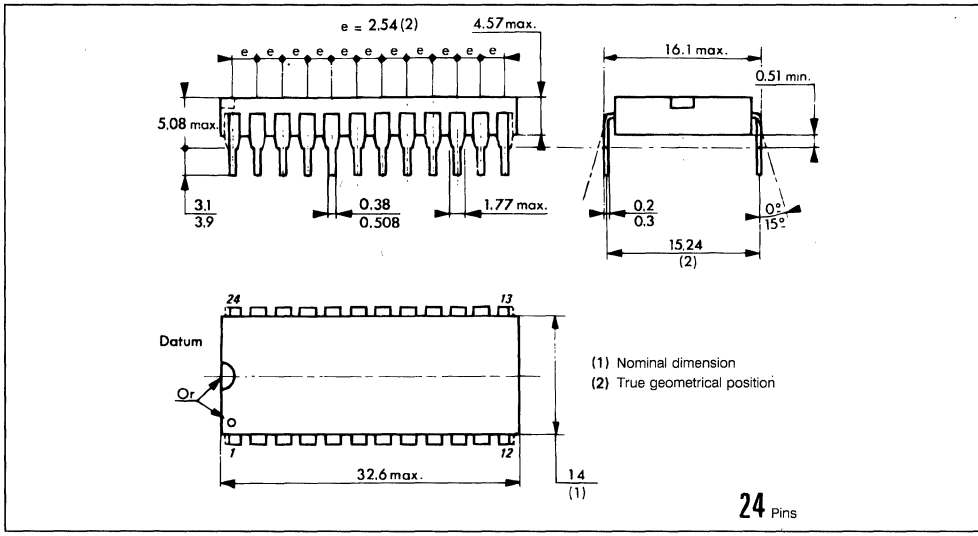


ORDERING INFORMATION

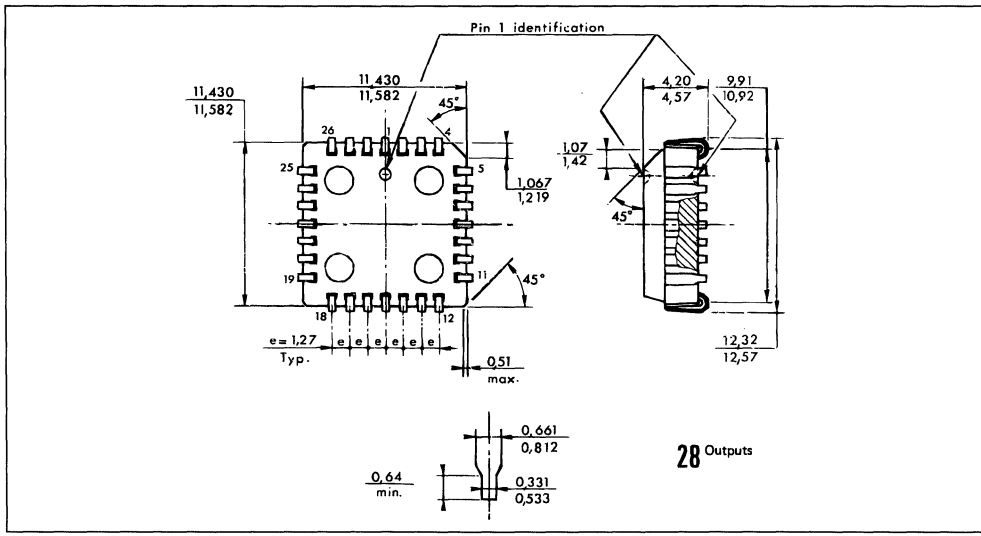
Part Number	Temperature Range	Package
TS68950CP	0 to + 70 °C	DIP 24
TS68950CFN	0 to + 70 °C	PLCC 28

PACKAGE MECHANICAL DATA

24 PINS – PLASTIC DIP

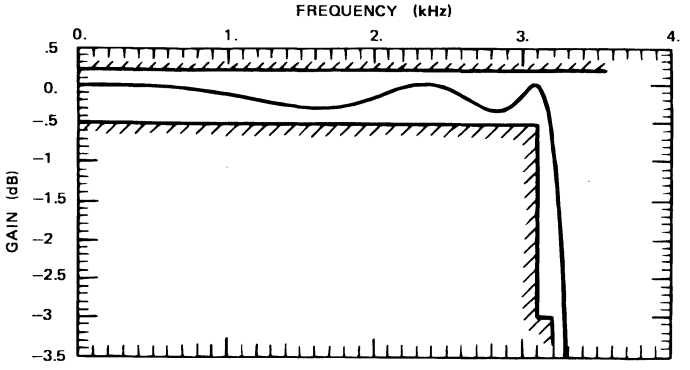


28 PINS – PLASTIC LEADLESS CHIP CARRIER



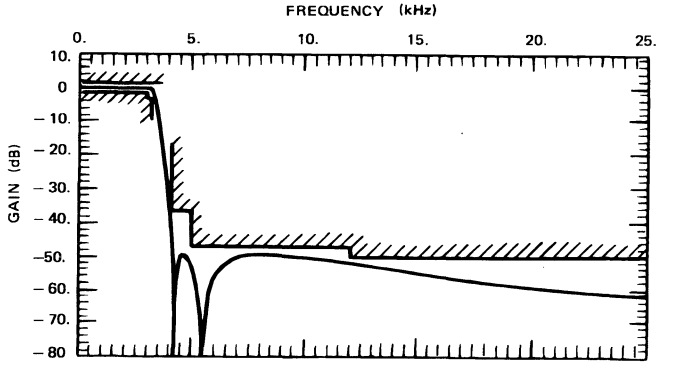
APPENDIX 1

TRANSMIT LOW–PASS FILTER TYPICAL RESPONSE AND LIMITS CHART



M88TS68950-10

TRANSMIT LOW–PASS FILTER TYPICAL RESPONSE AND LIMITS CHART



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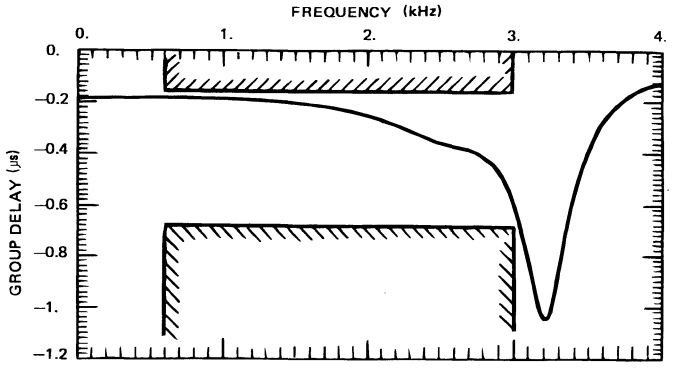
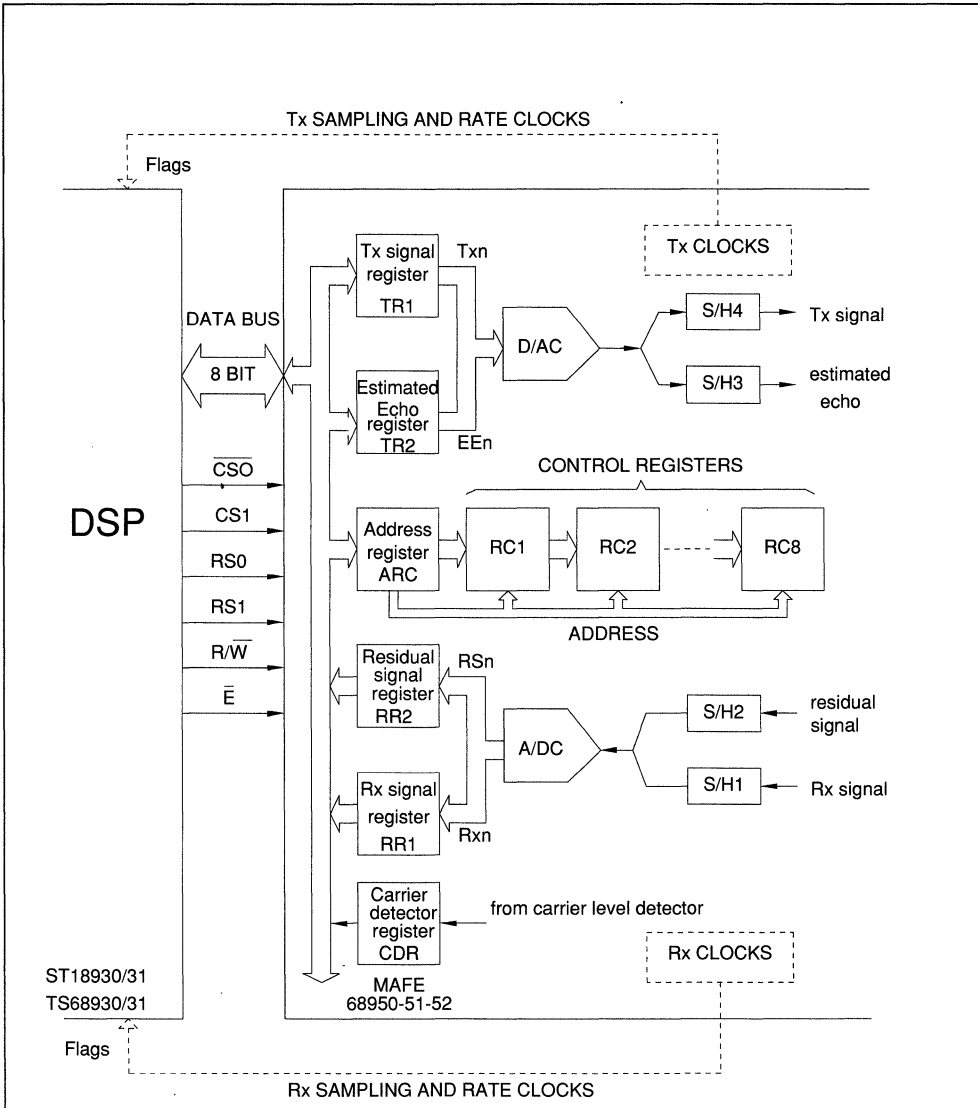
TRANSMIT LOW–PASS FILTER TYPICAL GROUP DELAY AND LIMITS CHART



M88TS68950-12

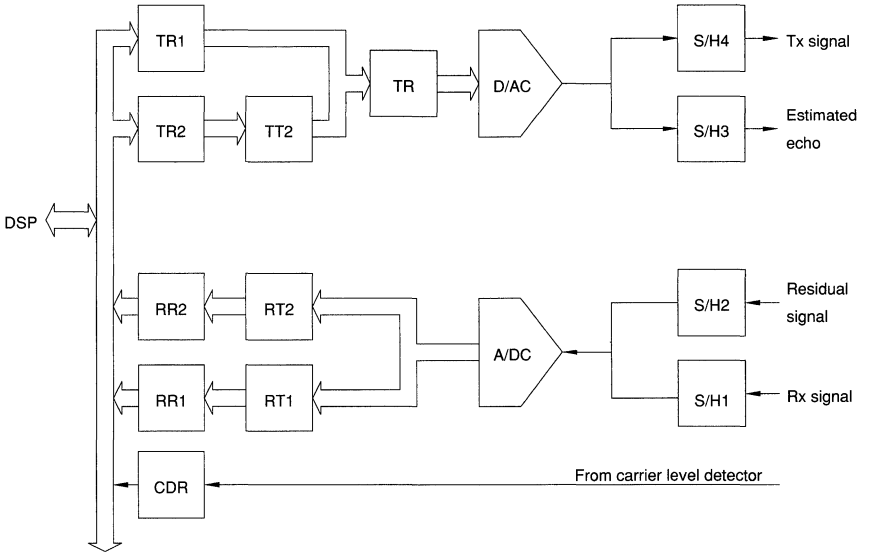
APPENDIX 2

INTERFACE BETWEEN DSP AND MODEM ANALOG FRONT-END (TS68950/51/52)



APPENDIX 3

DETAILED INPUT/ OUTPUT REGISTERS DIAGRAM



M88TS68950-14

R/$\overline{W}$	RS0	RS1	Register Accessed
Writing 0	0	0	TR1
Writing 0	0	1	TR2
Writing 0	1	0	ARC
Writing 0	1	1	Control Register Addressed by ARC
Reading 1	0	0	RR1
Reading 1	0	1	RR2
Reading 1	1	0	CDR
Reading 1	1	1	Not Used

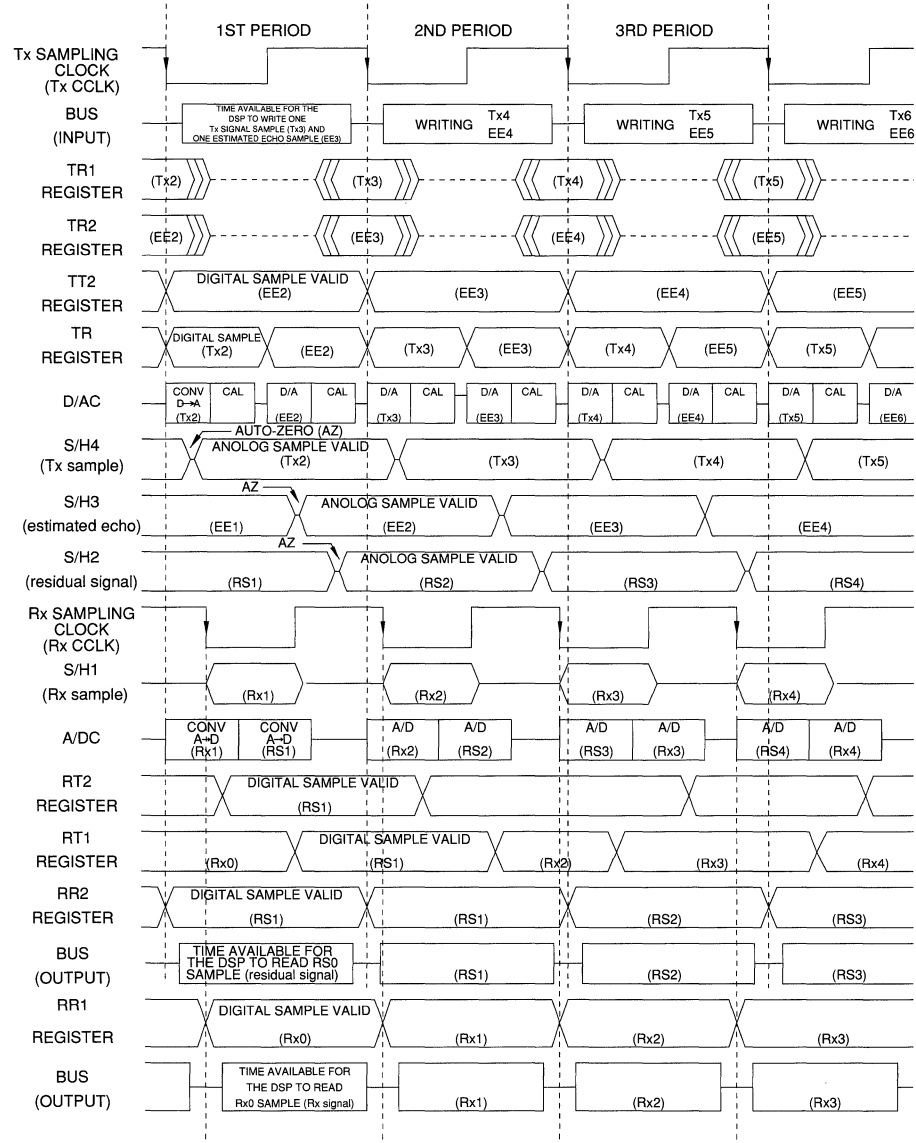
APPENDIX 4

CONTROL REGISTERS PROGRAMMING

Register Name	Circuit Including this Register	Register Content								ARC Content (register address)		
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5
RC1	68952	HB4	HB3	HB2	HB1	HR3	HR2	HR1		0	0	0
RC2	68952	HM3	HM2	HM1	HS2	HS1	HTHR			0	0	1
RC3	68951	HP2	HP1	LP2	LP1	REJ	S/A	REC		0	1	0
RC4	68950	ATE4	ATE3	ATE2	ATE1		EM2	EM1		0	1	1
RC5	68951	GR5	GR4	GR3	GR2	GR1				1	0	0
RC6	68951	GDS2	GDS1	HDS						1	0	1
RC7	68952	SP5	SP4	SP3	SP2	SP1				1	1	0
RC8	68952	MPE	SPR	AVRE	VAL	INIT				1	1	1

APPENDIX 5

PROGRESSION OF THE DIGITAL AND ANALOG SAMPLES IN THE MAFE



M88TS68950-15

APPENDIX 6

FURTHER REFERENCES

1/MAFE CHARACTERIZATION REPORT

This report gives the results of the measurements performed on the TS68950/51/52 Modem Analog Front-End (MAFE) chip set.

Chapter 1 describes the configuration and the method used for these measurements.

Chapter 2 comments the results obtained on the two signal paths of the transmit (Tx) analog front-end TS68950, i.e. the echo path and the Tx signal path Similarly chapter 3 gives the results obtained on the echo path and the receive (Rx) signal path of the Rx analog front-end TS68951

Performances obtained on the TS68951 when using plesiochronous clocks are given in chapter 4. In this case, the TS68952 clock generator delivers the main clock and the two sampling clocks to the Rx analog interface

2/MAFE EVALUATION BOARD

The MAFE evaluation board is a complete unit for evaluation of the TS68950/51/52 MAFE chip set.

The MAFE evaluation board is equipped with the TS68950/51/52 chip set and phone line interface facilities.

It can be directly connectable to an external Digital Signal Processor through a 50-pin connector or can be linked to the SGS-THOMSOM family of digital signal processors emulation-evaluation tools. In this case, along with the software tools (MACROASSEMBLER, SIMULATOR and LINKER), it provides a ready-to-use Digital Signal Processor System Interface well adapted to the analog word and high speed modems development.

3/APPLICATION NOTE

This Application Note describes the development of Real-Time Algorithms using the SGS-THOMSON Digital Signal Processor TS68930 and the MAFE chip set.

MODEM RECEIVE ANALOG INTERFACE

- TWO CHANNEL 12-BIT ANALOG TO DIGITAL CONVERTER FOR RECEPTION OF DIGITAL DATA FROM THE TELEPHONE LINE AND ECHO CANCELLATION (with asynchronous multiplexing of 2 plesiochronous channels)
- PROGRAMMABLE SWITCHED CAPACITOR BAND-PASS FILTER
- PROGRAMMABLE GAIN AMPLIFIER FROM 0 TO 46.5 dB WITH 1.5 dB STEPS
- PROGRAMMABLE BACK CHANNEL REJECTION AND RECONSTRUCTION FILTER
- CARRIER LEVEL DETECTOR WITH PROGRAMMABLE THRESHOLD
- DIRECT INTERFACE WITH STANDARD MPU 8-BIT BUS
- LOW POWER CMOS TECHNOLOGY
- AVAILABLE IN DIL OR SURFACE MOUNT PACKAGE

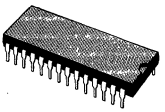
DESCRIPTION

The TS68951 is a Receive (Rx) Analog Front-End circuit designed to implement the analog to digital conversion and filtering required by high-speed voice-band modems or speech coding applications using digital signal processing technology.

The TS68951 meets all the CCITT recommendations from V.22 to V.33 including full-duplex recommendations with echo-cancellation (V.32) thanks to its multiplexed 2nd channel.

Used in conjunction with the TS68950 Transmit (Tx) Analog Front-End circuit and the TS68952 clock generator*, it provides a very cheap and efficient interface to digital signal processing functions in high speed modems or telephony applications.

*The interconnection between the 3 chips of the Modem Analog Front End (MAFE) is decribed p16/30.



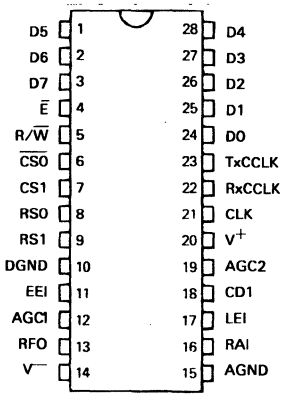
P
DIP28
(Plastic package)

FN
PLCC28
(Plastic package)

(Ordering Information at the end of the datasheet)

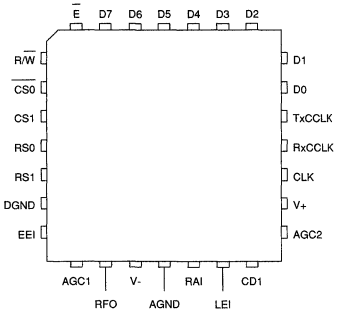
PIN CONNECTIONS

DIP28



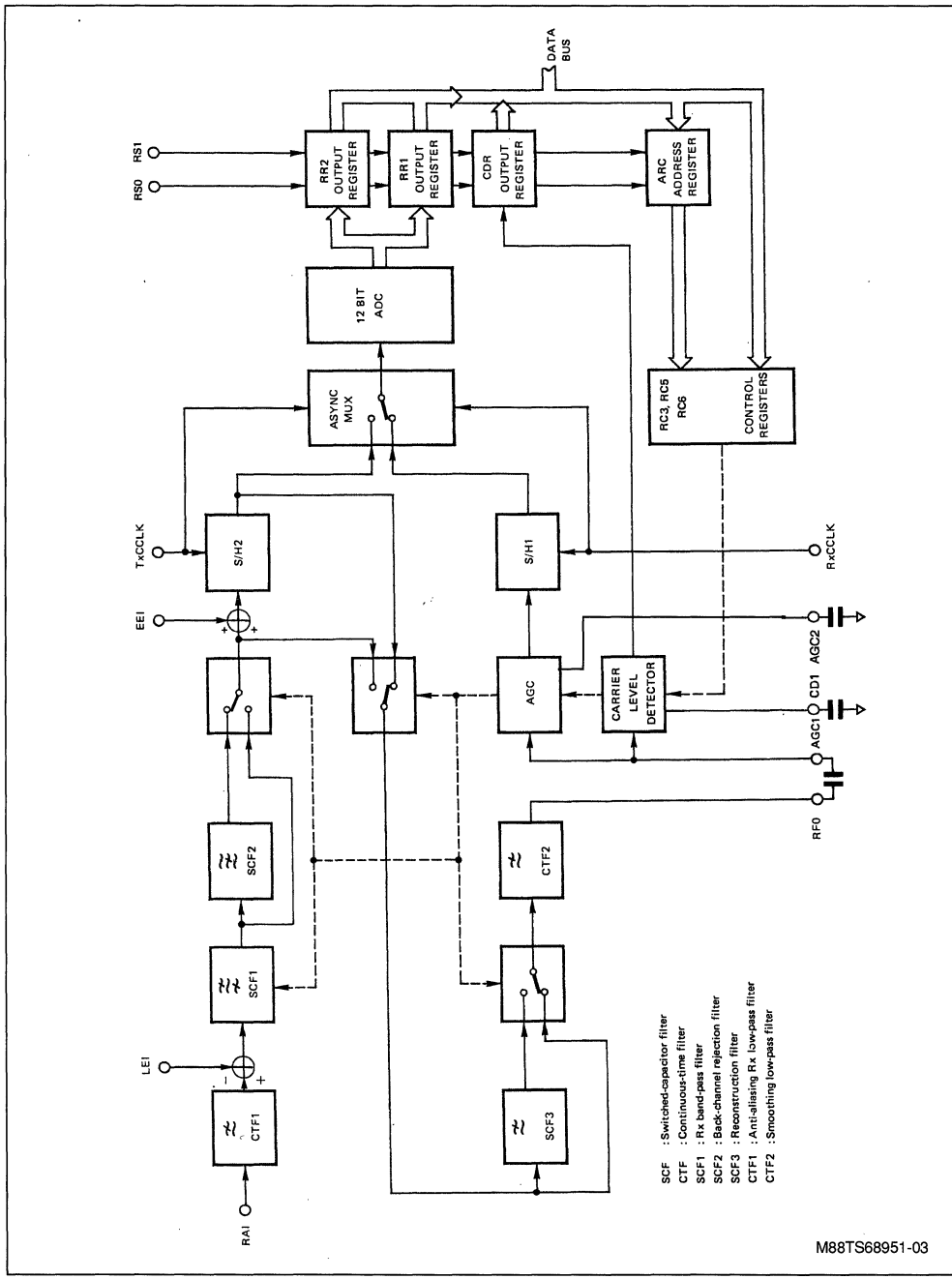
M88TS68951-01

PLCC28



M88TS68951-02

BLOCK DIAGRAM



PIN DESCRIPTION

Name	Description
D5-D7	Data Bus
$\overline{E}$	Enable Input. Enables Selection Inputs. Active On a Low Level for Read Operation. Active On a Positive Edge for Write Operation.
R/$\overline{W}$	Read/write Selection Input. Read operation is selected on a high level. Write operation is selected on a low level.
$\overline{CSO}$-CS1	Chip Select Inputs. The chip set is selected when $\overline{CSO}$ = 0 and CS1 = 1.
RSO-RS1	Register Select Inputs. Select the register involved in a read or write operation.
DGND	Digital Ground. All digital signals are referenced to this pin.
EEI	Estimated Echo Input. When operating in echo cancelling mode, this signal is added to the reception bandpass filter output.
AGC1	Analog input of the automatic gain control amplifier and of the carrier level detector.
RFO	Reception Filter Analog Output. Designed to be connected to AGC1 input through a 1 µF non polarised capacitor.
V^-	Negative Power Supply. $V^- = -5\ V \pm 5\ \%$.
AGND	Analog Ground. All analog signals are referenced to this pin.
RAI	Receive Analog Input. Analog input tied to the transmission line.
LEI	Local Echo Input. Analog input substracted from the receive anti-aliasing filter output.
CD1	This pin must be connected to the analog ground through a 1 µF non polarised capacitor, in order to cancel the offset voltage of the carrier level detector amplifier.
AGC2	This pin must be connected to the analog ground through a 1 µF non polarised capacitor, in order to cancel the offset voltage of the AGC amplifier.
V^+	Positive Power Supply $V^+ = +5\ V \pm 5\ \%$.
CLK	Master Clock Input. Nominal Frequency 1.44 MHz.
RxCCLK	Receive Conversion Clock.
TxCCLK	Transmit Conversion Clock.
D0-D4	Data Bus.

FUNCTIONAL DESCRIPTION

The TS68951 is a received analog interface for voice-band MODEM. It is able to perform the receive interface function for three types of synchronous MODEM :

- Four-wire or two-wire half duplex MODEM
- Two-wire full duplex band-split MODEM
- Two-wire full duplex echo cancelling MODEM

FOUR/TWO WIRE HALF DUPLEX MODEM
TWO WIRE BAND SPLIT MODEM

In these modes of operation, EEI input must be tied to the analog ground. The analog signal treatment of receive input is shown in figure 3 p17/30.

Programming requirements :

- Band-pass filter cut-off frequencies
- Back channel rejection filter (presence or absence according to the application)
- SCF1 or SCF2 output as input of CTF2
- AGC gain
- Carrier level detector threshold

The receive samples are coded at RxCCLK rate and can be read from receive register (RR1)

TWO WIRE ECHO CANCELLING MODEM

This mode of operation uses the full capabilities of the TS68951. The analog treatment of receive input is shown in figure 4 p18/30. The echo cancelling operation is achieved by means of subtraction of the LEI signal from the output of CTF1 duplexer and addition of the EEI signal to the output of SC1.

After the local echo reduction by the duplexer the resultant signal consists of the receive signal plus the echo signal generated by the transmission line mismatch : this undesirable signal is then cancelled at the output of the Rx band-pass filter.

Programming requirements :

- Band-pass filter cut-off frequencies
- SCF1 output as input of S/H2
- Output of S/H2 as input of SCF3 and output of SCF3 as input of CTF2.
- AGC gain
- Carrier level detector threshold

Residual signal samples from S/H2 output are coded at TxCCLK rate and can be read from receive register 2 (RR2), hence the signal processor may correlate them with the transmit samples to update the coefficients of the filter that generates the estimated echo.

The receive signal samples are coded at RxCCLK rate and can be read from receive register 1 (RR1).

FUNCTIONAL SPECIFICATIONS

BUS AND REGISTERS CONTROL

For any operation involving bus and registers, the chip select bits $\overline{CS0}$ and CS1 must be active ($\overline{CS0}$ = 0 and CS1 = 1)

The seven internal registers are divided into four write only registers and three read-only registers

WRITE OPERATION

There are three control registers (RC3, RC5, RC6) and one address register (ARC) which can be written ; but only ARC can be directly addressed.

The control registers are indirectly addressed by the word contained in ARC according to table 1.

Table 1.

Addressed Control Register	Word Contained in ARC							
	D7	D6	D5	D4	D3	D2	D1	D0
RC3	0	1	0	X	X	X	X	X
RC5	1	0	0	X	X	X	X	X
RC6	1	0	1	X	X	X	X	X

X : don't care.

When a write operation is selected (refer to table 3) the data present on the bus are strobed on a positive edge of $\overline{E}$ and the content of ARC is incremented

Note : Addresses of RC3 and RC5 are separated by two increments

READ OPERATION

There are two 12-bit receive registers (RR1, RR2) and a 1-bit carrier detector register (CDR)

RR2 contains the coded samples of the residual signal and RR1 the coded samples of the receive signal

The active bit of CDR is D7:D0 to D6 are forced to 0

When the RMS value of CTF2 output is greater than the programmed threshold, bit 7 of CDR is set. The nominal response time of the carrier detector to a signal settlement or removal is 1.78 ms.

When a read operation is selected (refer to table 3) the data are sent to the bus on a low level of $\overline{E}$; a high level on $\overline{E}$ sets the output bus drivers in a high impedance state

As the data bus has only 8 bits, the contents of RR1 or RR2 must be read in two cycles. The four less significant bits are transferred in the first cycle and the eight most significant bits are transferred in the second cycle according to the format, table 2.

Table 2.

	D7	D6	D5	D4	D3	D2	D1	D0
First Cycle	RRx3	RRx2	RRx1	RRx0	0	0	0	0
Second Cycle	RRx11	RRx10	RRx9	RRx8	RRx7	RRx6	RRx5	RRx4

An internal latch selects the first or the second byte and is automatically incremented on a positive edge of $\overline{E}$ when one of the receive registers is addressed. This latch is not reset at power-on, so it needs to be reset before the first read operation : reset occurs on any positive edge of $\overline{E}$ for any operation, provided none of the receive registers is addressed ; the first byte is selected when reset.

RR1 AND RR2 OUTPUT CODE :

The output code is a 2's complement delivering values from – 2048 up to + 2047. Since the converter codes voltage between – V_{ref} and + V_{ref}, the theoretical decision voltage corresponding to code C can be computed as follows :

$$V_C = \frac{2C + 1}{4095} V_{ref}$$

where V_{ref} is the reference voltage of the A/D converter, V_{ref} nominal value is 2.5 V and C is the algebraic value of code C.

Example :
Assume the output code is the hexadecimal value $8B1 ; the algebraic value of this code C = – 1871 therefore V_C = – 2.283 V.

Table 3.

R/$\overline{W}$	RSO	RS1	Operation
0	1	1	Write Control Register Addressed by ARC
0	1	0	Write Address Register (ARC)
1	0	1	Read Receive Register 2 (RR2) (residual signal sample)
1	0	0	Read Receive Register 1 (RR1) (receive signal sample)
1	1	0	Read Carrier Detector Register (CDR)

CONTROL REGISTERS DESCRIPTION

POWER-ON

The control registers are not initialised at power-on ; they must be initialised before reading any word from the output registers.

REGISTER RC3

The contents of RC3 sets the – 3 dB cut-off frequencies of SCF1 receive band-pass filter, determines the presence or the absence of SCF2 back channel rejection filter and of SCF3 reconstruction filter, and selects receive signal path to the second filtering section ; without echo-cancelling the output of SCF1 or SCF2 is selected ; with echo-cancelling the output of S/H2 is selected.

The band-pass filter consists of a 5th-order elliptic low-pass filter and of a 2nd order high-pass filter whose cut-off frequencies can be programmed by (LP1, LP2) and (HP1, HP2) respectively, (refer table 4).

The rejection filter is present when REJ bit is high.

The reconstruction filter is present when REC bit is high.

S/H2 output is selected when S/A bit is high.

Table 4.

D7 HP2	D6 HP1	D5 LP2	D4 LP1	D3 REJ	D2 S/A	D1 REC	D0	RC3 Register	
								Low-pass Filter	
								Sampling Frequency Fs (kHz)	**– 3 dB Cut-off Frequency** (Hz)
		0	0				x	72	800
		0	1				x	144	1600
		1	0				x	288	3200
		1	1				x	288	3200
								High-pass Filter	
								Sampling Frequency Fs (kHz)	**– 3 dB Cut-off Frequency** (Hz)
0	x			0			x	36	250
1	0			0			x	72	500
1	1			0			x	144	1600
								High-pass and Rejection Filter	
								Sampling Frequency (kHz)	**– 3 dB Cut-off Frequency** (Hz) / **Rejected Band** (Hz)
1	0			1			x	72	800 / 370-470
1	1			1			x	144	2200 / 800-1600
								S/H2 Selection	
					0		x	Deselected	
					1		x	Selected	
								Reconstruction Filter Selection	
						0	x	Deselected	
						1	x	Selected (sampling frequency Fs = 288 kHz)	

X : don't care.

REGISTER RC5

The content of RC5 sets the gain of the AGC amplifier between 0 dB and 46.5 dB with 1.5 dB steps.

Note : The AGC loop control is performed by the signal processor.

Table 5.

D7	D6	D5	D4	D3	D2	D1	D0	RC5
								AGC Gain (dB)
0	0	0	0	0	x	x	x	0
0	0	0	0	1	x	x	x	1.5
0	0	0	1	0	x	x	x	3
0	0	0	1	1	x	x	x	4.5
0	0	1	0	0	x	x	x	6
0	0	1	0	1	x	x	x	7.5
0	0	1	1	0	x	x	x	9
0	0	1	1	1	x	x	x	10.5
0	1	0	0	0	x	x	x	12
0	1	0	0	1	x	x	x	13.5
0	1	0	1	0	x	x	x	15
0	1	0	1	1	x	x	x	16.5
0	1	1	0	0	x	x	x	18
0	1	1	0	1	x	x	x	19.5
0	1	1	1	0	x	x	x	21
0	1	1	1	1	x	x	x	22.5
1	0	0	0	0	x	x	x	24
1	0	0	0	1	x	x	x	25.5
1	0	0	1	0	x	x	x	27
1	0	0	1	1	x	x	x	28.5
1	0	1	0	0	x	x	x	30
1	0	1	0	1	x	x	x	31.5
1	0	1	1	0	x	x	x	33
1	0	1	1	1	x	x	x	34.5
1	1	0	0	0	x	x	x	36
1	1	0	0	1	x	x	x	37.5
1	1	0	1	0	x	x	x	39
1	1	0	1	1	x	x	x	40.5
1	1	1	0	0	x	x	x	42
1	1	1	0	1	x	x	x	43.5
1	1	1	1	0	x	x	x	45
1	1	1	1	1	x	x	x	46.5

X : don't care.

REGISTER RC6

The content of RC6 sets the carrier level detector threshold. (Refer to table 6).

The threshold values are grouped by pair ; values belonging to each pair have 2.5 dB separation which allows the signal processor to perform software hysteresis.

Table 6.

D7	D6	D5	D4	D3	D2	D1	D0	RC6
								Threshold (dBm)
0	0	0	x	x	x	x	x	– 29.85
0	0	1	x	x	x	x	x	– 27.35
0	1	0	x	x	x	x	x	– 36.65
0	1	1	x	x	x	x	x	– 34.15
1	0	0	x	x	x	x	x	– 46.75
1	0	1	x	x	x	x	x	– 44.25
1	1	0	x	x	x	x	x	– 46.75
1	1	1	x	x	x	x	x	– 44.25

X : don't care.

CLOCK

The master clock CLK, the receive conversion clock (RxCCLK) and the transmit conversion clock (TxCCLK) are generated in the TS68952 clock generator. There are three possible frequencies for the conversion clocks : 7.2 kHz, 8 kHz and 9.6 kHz.

The nominal values of the RxCCLK and TxCCLK clocks must be identicals (these clocks are plesiochronous and real values within ± 100 ppm according to CCITT recommandations).

The frequency of RxCCLK and TxCCLK is controlled by two independant Digital Phase Locked Loops (DPLL). TxCCLK can be synchronised on an external Terminal Clock (TxSCLK) or on the Rx bit rate clock ; in these cases 350 ns discrete phase shifts occurs on CLK and TxCCLK synchronously with TxCCLK negative edge with a repetition rate of 600 Hz, 800 Hz or 1 000 Hz according to the programmation of RC1 control register in the TS68952.

A/D CONVERSION

The A/D converter is a 12 bit resolution, 8 bit minimum integral linearity, monotonic converter. The input voltage ranges from – 2.5 V to + 2.5 V ; and the conversion time is better than 50 µs.

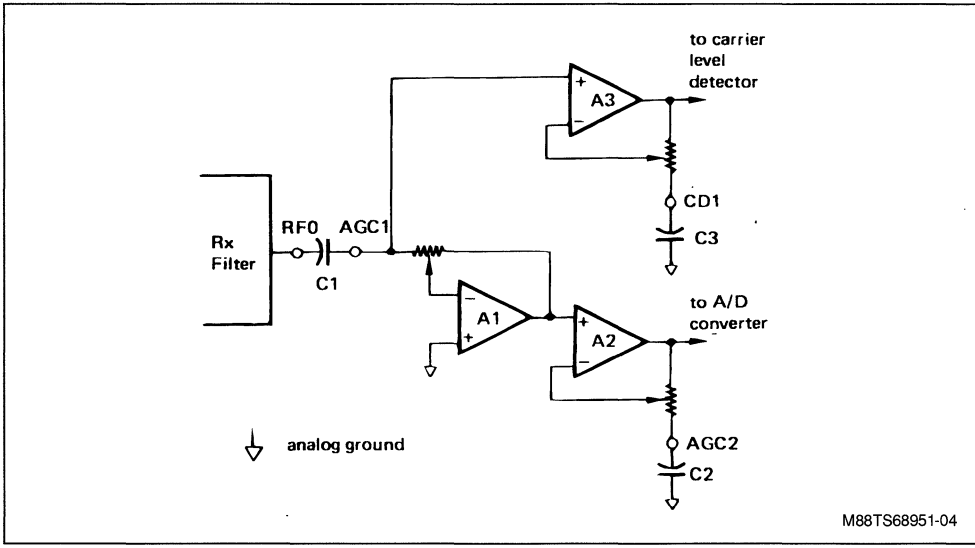
ASYNCHRONOUS MULTIPLEXING

Samples on the output of S/H1 and S/H2 are converted respectively at RxCCLK frequency and TxCCLK frequency. Since RxCCLK and TxCCLK are plesiochronous, the order of conversion is determined by an asynchronous logic. The output register RR1 and RR2 are respectively loaded on the negative edge of RxCCLK and TxCCLK.

AGC AND CLD AMPLIFIERS

The AGC consists of two cascaded amplifiers A1 and A2 (see fig.1) AC coupling is obtained from C1 and C2 external capacitors. C2 can be used as an auxiliary input for performing an analog loop located after echo cancellation. The carrier level detector (CLD) amplifier A3 also needs an external capacitor C3.

Figure 1 : Rx Amplifiers Schematic.



ELECTRICAL SPECIFICATIONS

The electrical specifications are given for operating temperature range (0 °C, 70 °C).

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
	Supply Voltage between V^+ and AGND or DGND	– 0.3 to + 7	V
	Supply Voltage between V^- and AGND or DGND	– 7 to + 0.3	V
	Voltage between AGND and DGND	– 0.3 to + 0.3	V
	Digital Input Voltage	DGND – 0.3 to V^+ + 0.3	V
	Digital Output Voltage	DGND – 0.3 to V^+ + 0.3	V
	Digital Output Current	– 20 to + 20	mA
	Analog Input Voltage	V^- – 0.3 to V^+ + 0.3	V
	Analog Output Voltage	V^- – 0.3 to V^+ + 0.3	V
	Analog Output Current	– 10 to + 10	mA
	Power Dissipation	500	mW
T_{oper}	Operating Temperature	0 to + 70	°C
T_{stg}	Storage Temperature	– 65 to + 150	°C

POWER SUPPLIES
DGND = AGND = 0 V

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V^+	Positive Power Supply	4.75		5.25	V
V^-	Negative Power Supply	– 5.25		– 4.75	V
I^+	Positive Supply Current (receive signal level 0 dBm)			20	mA
I^-	Negative Supply Current (receive signal level 0 dBm)	– 20			mA

DIGITAL INTERFACE
Control Inputs.
Voltages Referenced to DGND = 0 V

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{IL}	Low Level Input Voltage			0.8	V
V_{IH}	High Level Input Voltage	2.2			V
V_{IL}	Low Level Input Current DGND < V_I < 0.8 V	– 10		10	µA
V_{IH}	High Level Input Current 2.2 V < V_I < V^+	– 10		10	µA

DATA BUS
Voltages Referenced to DGND = 0 V

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{IL}	Low Level Input Voltage			0.8	V
V_{IH}	High Level Input Voltage	2.2			V
V_{OL}	Low Level Output Voltage (I_{OL} = 2.5 mA)			0.4	V
V_{OH}	High Level Output Voltage (I_{OL} = 2.5 mA)	2.4			V
I_{OZ}	High Impedance Output Current (when $\overline{E}$ is high and DGND < V_I < V^+)	– 50		50	µA

ANALOG INTERFACE
All Voltages Referenced to AGND = 0 V

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{in}	Input Voltage EEI, LEI, RAI	– 2.5		2.5	V
I_{in}	Input Current EEI, LEI, RAI (– 2.5 V < V_{in} < 2.5 V)	– 1		1	µA
R_{in}	Input Resistance AGC1, AGC2	1.5			kΩ
R_{in}	Input Resistance CD1	0.7			kΩ
V_{out}	Output Voltage RFO CL = 50 pF, RL = 1 kΩ	– 2.5		2.5	V
R_{out}	Output Resistance RFO			2	Ω
R_L	Load Resistance RFO	1			kΩ
C_L	Load Capacitance RFO			50	pF

BUS TIMING CHARACTERISTICS
(see foot notes 1 and 2 on timing diagrams)

Symbol	Parameter		Value			Unit
			Min.	Typ.	Max.	
t_{CYC}	Cycle Time	(1)	320			ns
t_{WEL}	Pulse Width $\overline{E}$ Low Level	(2)	180			ns
t_{WEH}	Pulse Width $\overline{E}$ High Level	(3)	100			ns
t_r, t_f	Clock Rise and Fall Time	(4)			20	ns
t_{HCE}	Control Signal Hold Time	(5)	10			ns
t_{SCE}	Control Signal Set-up Time	(6)	40			ns
t_{SDI}	Input Data Set-up Time	(7)	120			ns
t_{HDI}	Input Data Hold Time	(8)	1			ns
t_{SDO}	Output Data Set-up Time (1 TTL load and CL = 50 pF)	(9)			150	ns
t_{DZ}	Output High Impedance Delay Time (1 TTL load and CL = 50 pF)	(10)			80	ns

RECEPTION CHARACTERISTICS

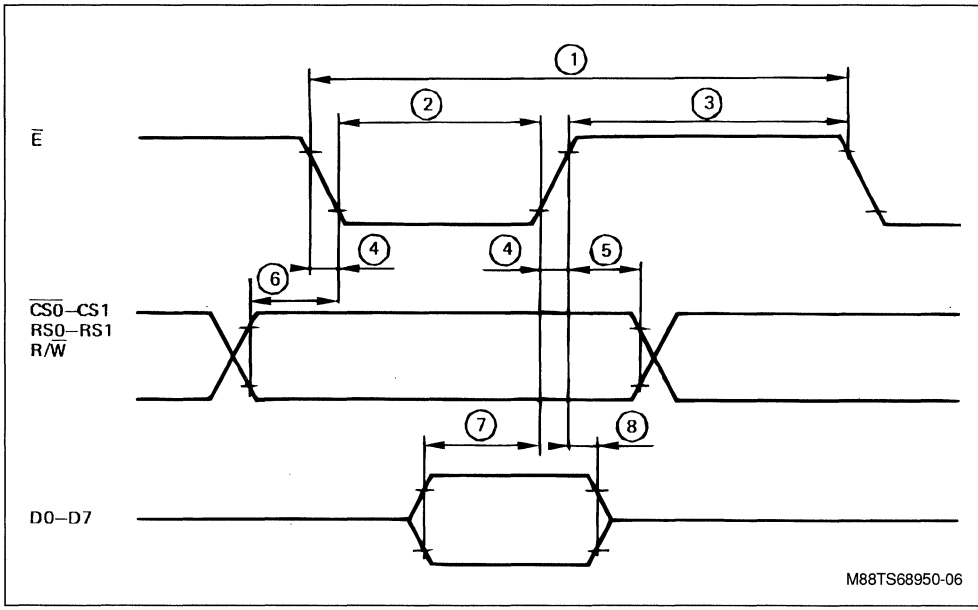
PERFORMANCE OF THE WHOLE RECEPTION CHAIN (input RAI or LEI, output RR1)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
G	Gain (AGC gain = 0 dB, RxCCLK = 9600 Hz, V_{in} = 775 mV_{eff}, f = 2000 Hz)	– 0.5		– 0.5	dB
TD	Total Non Harmonic Distortion (AGC gain = 0 dB, RxCCLK = 9600 Hz, V_{in} = 775 mV_{eff}, f = 2000 Hz)			– 58	dB

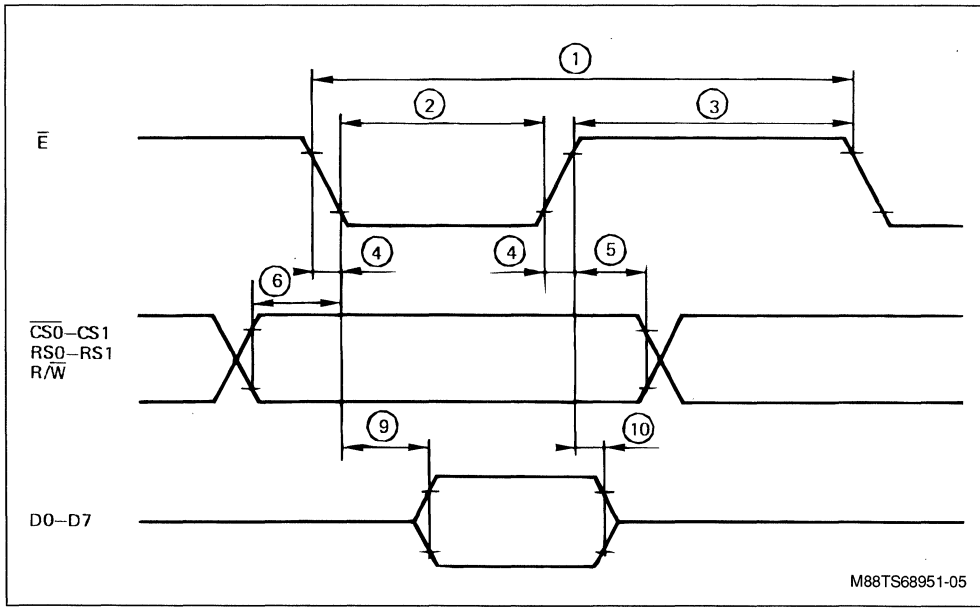
PERFORMANCE OF THE RECEPTION SUB-CHAIN (from RAI input to S/H2 input)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
TD	Total Distortion (RxCCLK = 9600 Hz, V_{in} = 1.6 V_{eff}, f = 2000 Hz)			– 72	dB

WRITE OPERATION



READ OPERATION



Notes : 1. Voltage levels shown are $V_{IL} < 0.4$ V, $V_{IH} > 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.2 V, unless otherwise specified.

RECEIVE BAND-PASS FILTER AND REJECTION FILTER (input RAI, output RFO)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
Low-pass Filter (Fs = 288 kHz)					
G_{ref}	Reference Gain (V_{in} = 775 mV_{eff}, f = 1800 Hz)	– 0.5		0.5	dB
G_{rel}	Relative Gain to G_{ref} 0 Hz < f < 3000 Hz f = 3200 Hz f > 6250 Hz	 – 0.4 – 3		 0.3 0.3 – 60	 dB dB dB
T_{gp}	Group Propagation Delay Time (f = 1800 Hz)			300	µs
T_{gpd}	Group Propagation Delay Time Distortion (600 Hz < f < 3000 Hz)			360	µs
High-pass Filter (Fs = 72 kHz)					
G_{ref}	Reference Gain (V_{in} = 775 mV_{eff}, f = 1800 Hz)	– 0.5		0.5	dB
G_{rel}	Relative Gain to G_{ref} 500 Hz < f ≤ 3000 Hz f = 500 Hz f < 100 Hz	 – 0.4 – 3		 0.3 0.5 – 25	 dB dB dB
T_{gp}	Group Propagation Delay Time (f = 1800 Hz)			50	µs
T_{gpd}	Group Propagation Delay Time Distortion (600 Hz < f < 3000 Hz)			450	µs
High-pass Filter and Rejection Filter (Fs = 72 kHz)					
G_{ref}	Reference Gain (V_{in} = 775 mV_{eff}, f = 1800 Hz)	– 1		0	dB
G_{rel}	Relative Gain to G_{ref} f = 100 Hz f = 370 Hz 390 Hz < f < 450 Hz f = 470 Hz f = 900 Hz			 – 25 – 27 – 30 – 27 0	 dB dB dB dB dB
T_{gp}	Group Propagation Delay Time (f = 1800 Hz)			75	µs
T_{gpd}	Group Propagation Delay Time Distortion (600 Hz < f < 3000 Hz)			1400	µs

Note : The measurement frequencies are integer sub-multiples of filters sampling frequencies.

RECONSTRUCTION FILTER

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
Reconstruction Filter (Fs = 288 kHz)					
G_{ref}	Reference Gain (V_{in} = 775 mV_{eff}, f = 2000 Hz)	– 0.3		0.3	dB
G_{rel}	Relative Gain to G_{ref} 0 Hz < f < 2900 Hz f = 3100 Hz f > 6000 Hz	 – 0.4 – 3		 0.3 0.3 – 60	 dB dB dB
T_{gp}	Group Propagation Delay Time (f = 1800 Hz)			300	µs
T_{gpd}	Group Propagation Delay Time Distortion (600 Hz < f < 3000 Hz)			440	µs
Whole Reception Filtering Chain (input RAI or LEI, output RFO)					
G_{ref}	Reference Gain (V_{in} = 775 mV_{eff}, f = 2000 Hz, RC3 = $AO)	– 0.5		0.5	dB
N_{rfo}	Noise on RFO (RAI, LEI, EEI tied to AGND 250 Hz < f < 3200 Hz)			350	μV_{eff}

PERFORMANCE OF RESIDUAL SIGNAL CHANNEL AND A/D CONVERTER
(input EEI, output RR2)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{in}	Input Voltage (peak to peak)			5	V
R_{esh}	A/D Converter Resolution			12	Bit
LSB	Analog Increment		1.2		mV
E_{il}	Integral Linearity Error	– 16		16	LSB
E_{dl}	Differential Linearity Error	– 0.7		0.7	LSB
V_{os}	Offset Voltage	– 100		100	LSB

AGC AMPLIFIER AND A/D CONVERTER (input AGC1, output RR1)

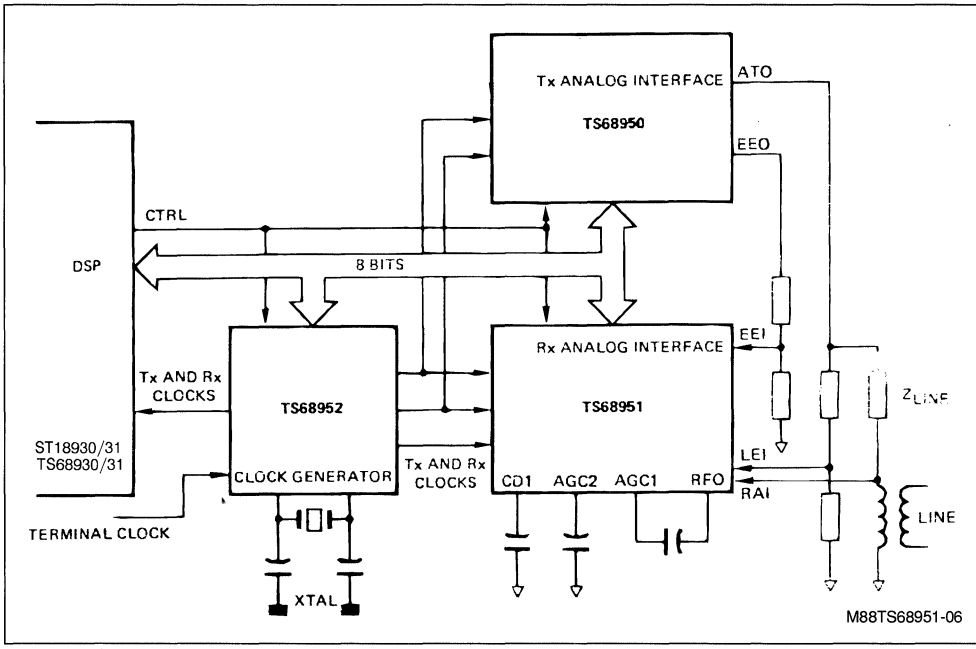
Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
G_{rel}	Relative Gain to Programmed Gain 0 dB ≤ AGC ≤ 24 dB 25.5 dB ≤ AGC ≤ 46.5 dB	 – 0.5 – 1		 0.5 1	 dB dB
V_{os}	Offset Voltage	– 70		70	LSB
N	Equivalent RMS Noise (AGC gain = 0 dB, RAI, LEI, EEI tied to AGND)			1.2	mV_{eff}

CARRIER LEVEL DETECTOR (input AGC1, output CDR)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
T_{rel}	Relative Threshold to Programmed Threshold	–1		1	dB
H_{yst}	Hysteresis	2		3	dB
V_{os}	Input Offset Voltage 1st Threshold Pair 2nd Threshold pair 3rd Threshold Pair	 – 1 – 2 – 3		 1 2 3	 mV mV mV
T_{dd}	Detection Delay Time 0 mV_{eff} to 775 mV_{eff} Transition or 775 mV_{eff} to 0 V_{eff} Transition	1		3	ms

APPLICATIONS INFORMATIONS

Figure 2 : Modem Analog Front-end Chip Set.



Notes : 1. Digital ground.
Analog ground.

2. In some cases, external-user circuitry may induces power-up sequency latch-up problems that can be efficiently avoided by using BAT43 schottky small signal diodes as follow :

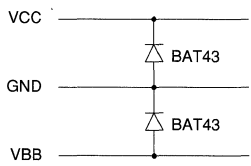


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Figure 3 : Four-wire or Two-wire Half Duplex and Two-wire Band-split Analog Signal Treatment.

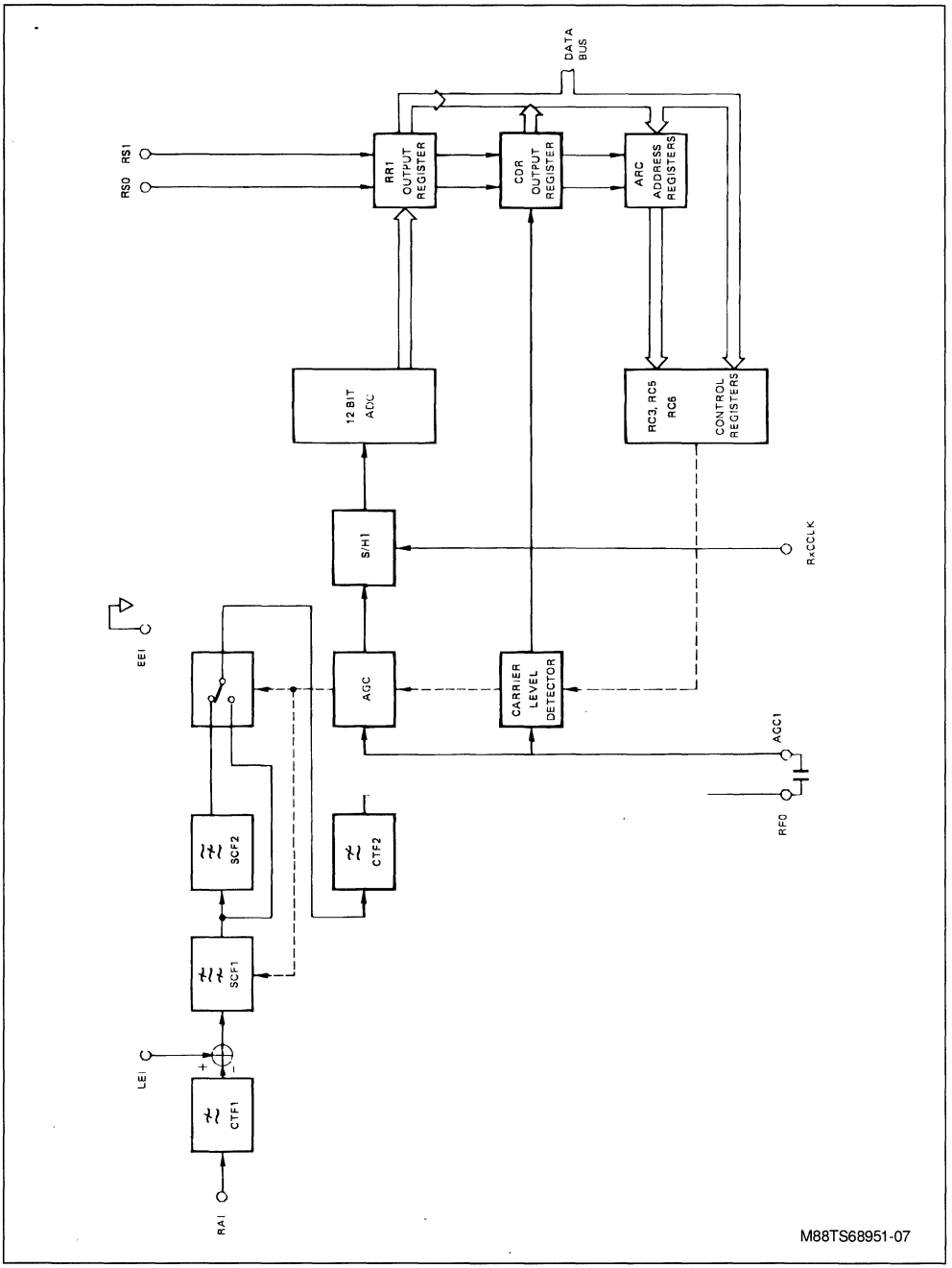
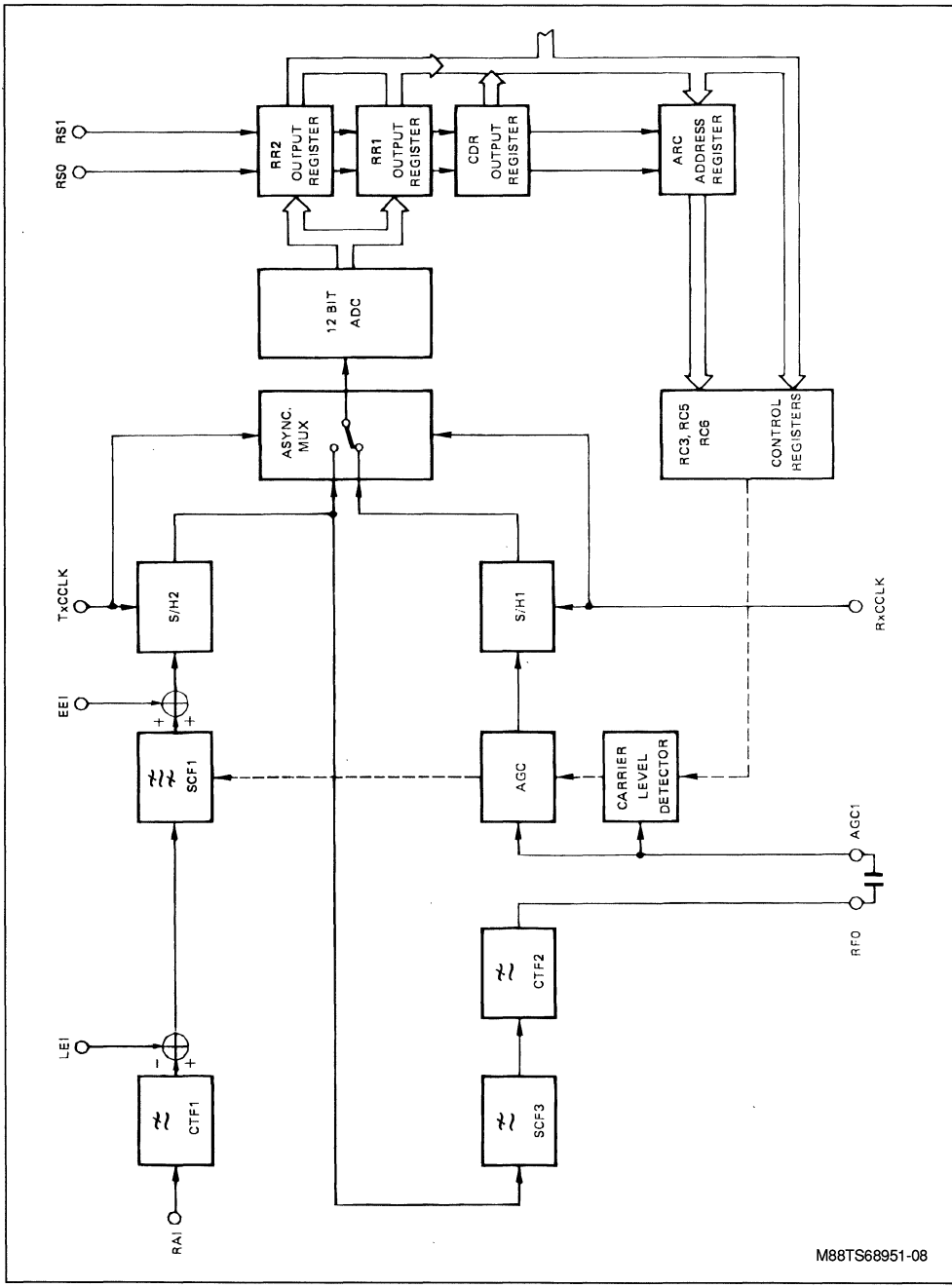


Figure 4 : Two-wire Echo Cancelling Analog Signal Treatment.

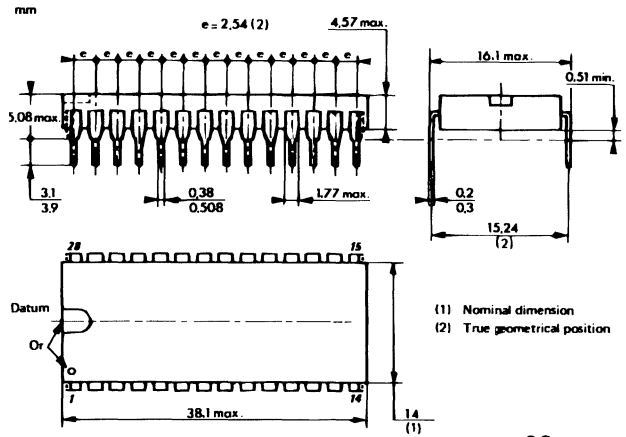


ORDERING INFORMATION

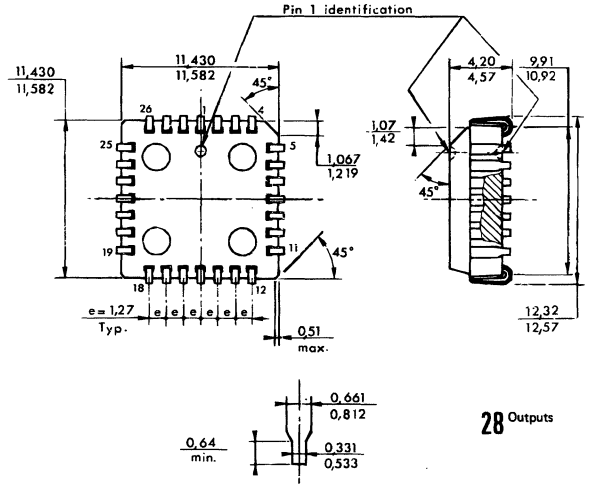
Part Number	Temperature Range	Package
TS68951CP	0 to + 70 °C	DIP 28
TS68951CFN	0 to + 70 °C	PLCC 28

PACKAGE MECHANICAL DATA

CB-132 – 28 PINS – PLASTIC DIP

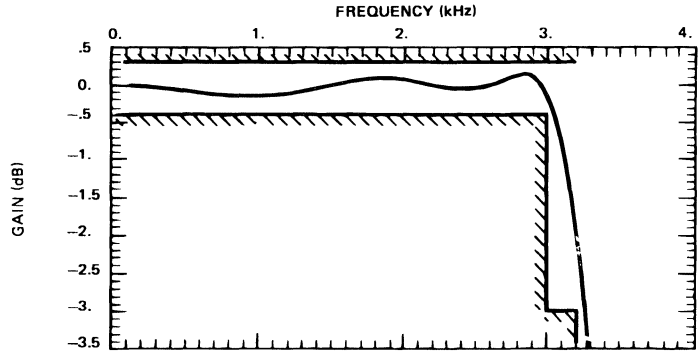


CB-520 – 28 PINS – PLASTIC LEADLESS CHIP CARRIER



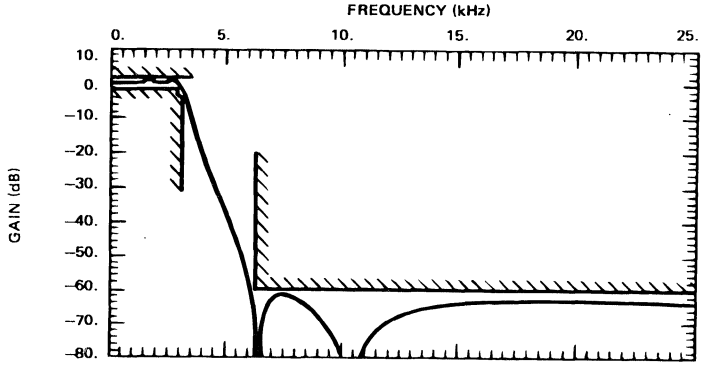
APPENDIX 1

Rx LOW-PASS FILTER TYPICAL RESPONSE AND LIMITS CHART (fs = 288 kHz).



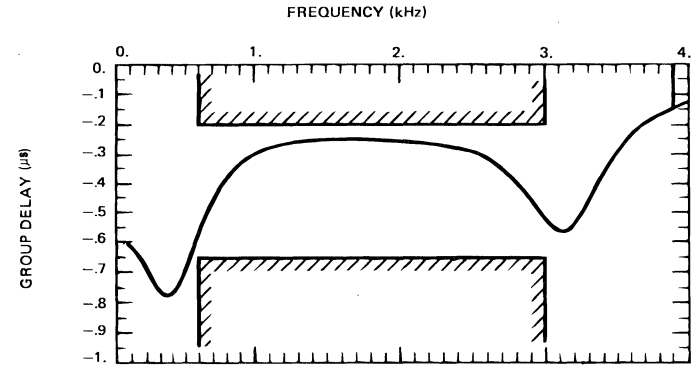
M88TS68951-09

Rx LOW-PASS FILTER TYPICAL RESPONSE AND LIMITS CHART (fs = 288 kHz).



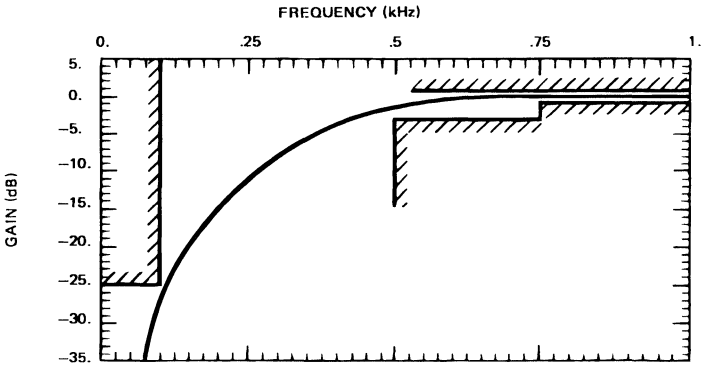
M88TS68951-10

Rx LOW-PASS FILTER TYPICAL GROUP DELAY TIME AND LIMITS CHART (fs = 288 kHz).



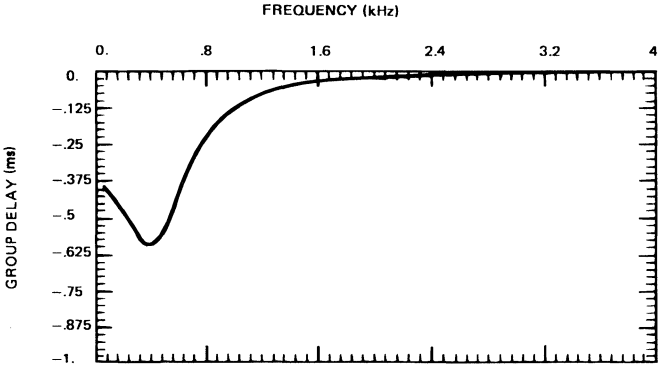
M88TS68951-11

Rx HIGH-PASS FILTER TYPICAL RESPONSE AND LIMITS CHART (Fs = 72 kHz).



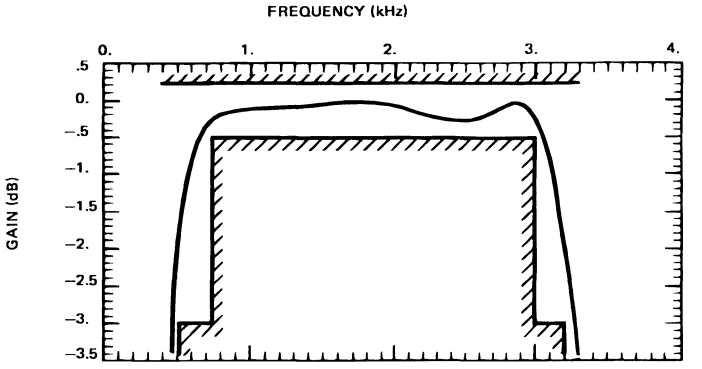
M88TS68951-12

Rx HIGH-PASS FILTER TYPICAL GROUP DELAY TIME AND LIMITS CHART (Fs = 72 kHz).



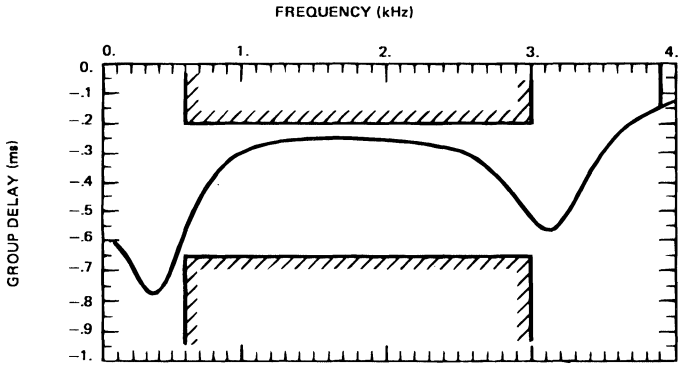
M88TS68951-13

Rx BAND-PASS FILTER TYPICAL RESPONSE AND LIMITS CHART (HP : Fs = 72 kHz, LP : Fs = 288 kHz).



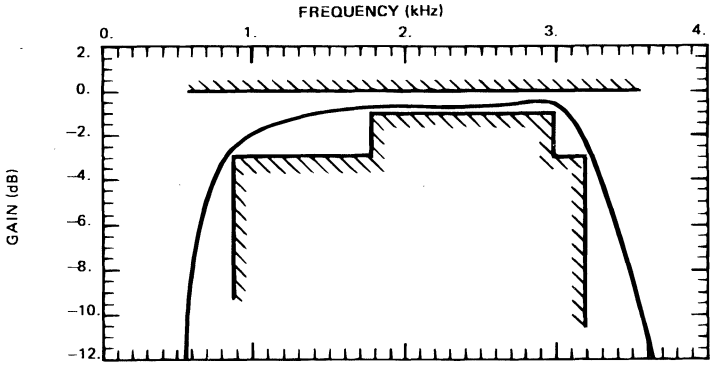
M88TS68951-14

Rx BAND-PASS FILTER TYPICAL GROUP DELAY TIME AND LIMITS CHART
(HP : Fs = 72 kHz, LP : Fs = 288 kHz).



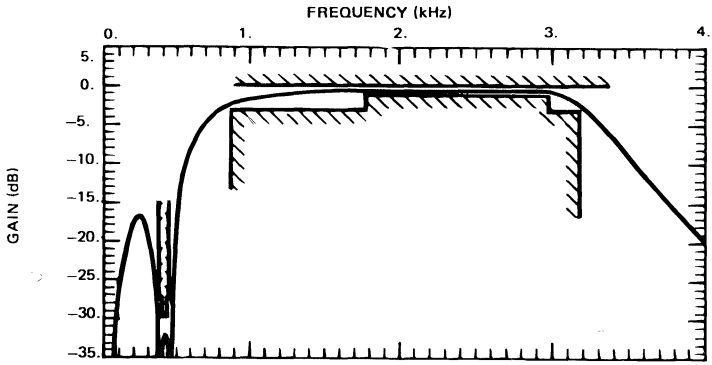
M88TS68951-15

Rx BAND-PASS AND REJECTION FILTER TYPICAL RESPONSE AND LIMITS CHART
(HP and REJ. : Fs = 72 kHz, LP : Fs = 288 kHz).



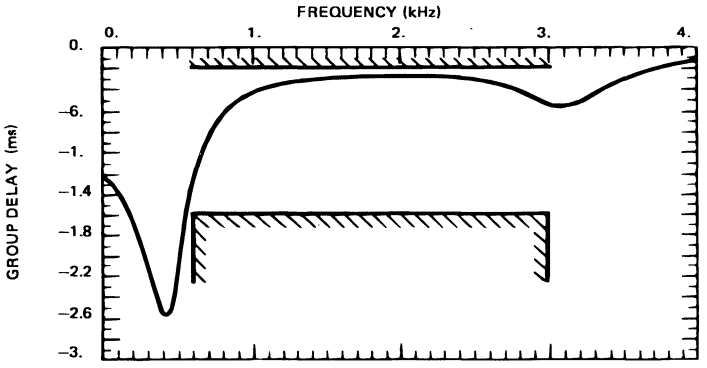
M88TS68951-16

Rx BAND-PASS AND REJECTION FILTER TYPICAL RESPONSE AND LIMITS CHART
(HP and REJ. : Fs = 72 kHz, LP : Fs = 288 kHz).



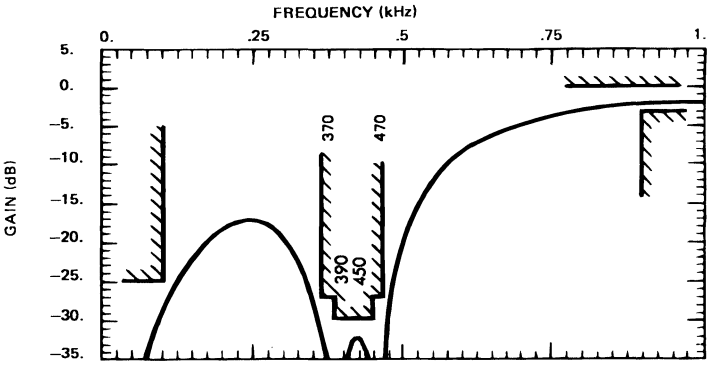
M88TS68951-17

Rx BAND-PASS AND REJECTION FILTER TYPICAL GROUP DELAY TIME AND LIMITS CHART (HP and REJ. : Fs = 72 kHz, LP : Fs = 288 kHz).



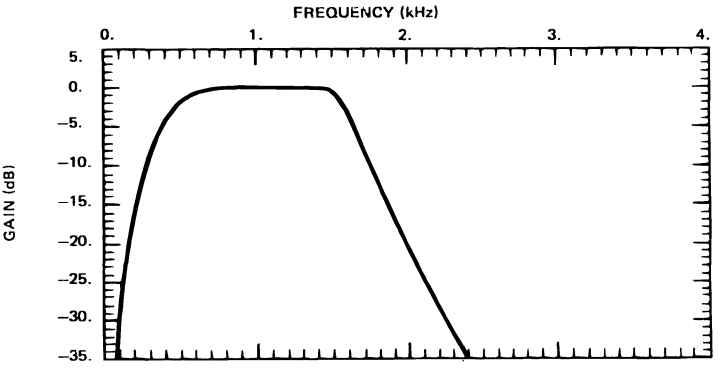
M88TS68951-18

Rx HIGH-PASS AND REJECTION FILTER TYPICAL RESPONSE AND LIMITS CHART (Fs = 72 kHz).



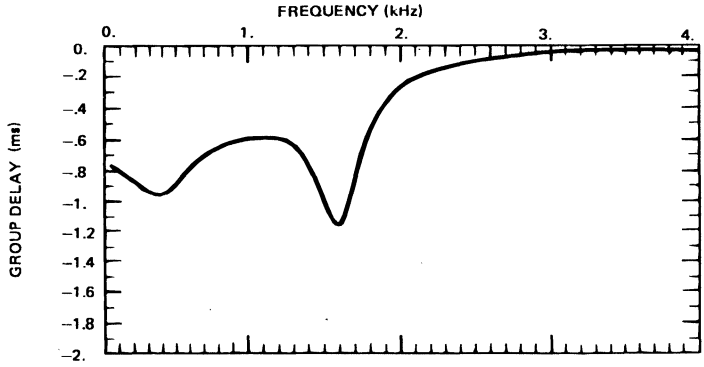
M88TS68951-19

Rx BAND-PASS FILTER TYPICAL RESPONSE FOR V22 MODE (Low Channel)
(HP : Fs = 72 kHz, LP : Fs = 144 kHz).



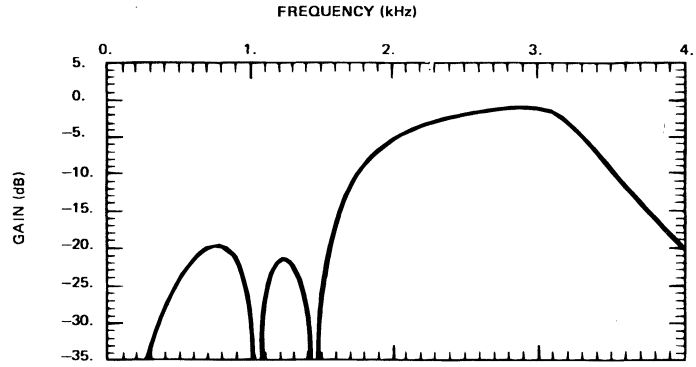
M88TS68951-20

Rx BAND-PASS FILTER TYPICAL GROUP DELAY TIME FOR V.22 MODE (Low Channel)
(HP : Fs = 72 kHz, LP : Fs = 144 kHz).



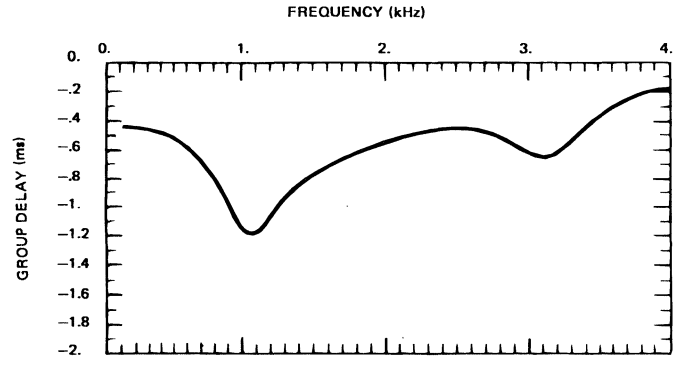
M88TS68951-21

Rx BAND-PASS FILTER TYPICAL RESPONSE FOR V.22 MODE (High Channel)
(HP and REJ. : fs = 144 kHz, LP : fs = 288 kHz).



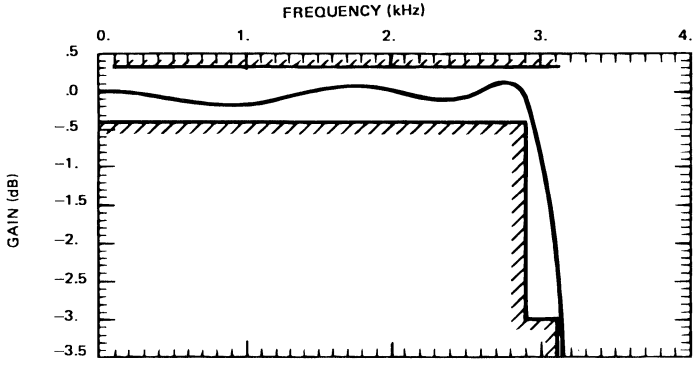
M88TS68951-22

Rx BAND-PASS FILTER TYPICAL GROUP DELAY TIME FOR V.22 MODE (High Channel)
(HP and REJ. : Fs = 144 kHz, LP : Fs = 288 kHz).



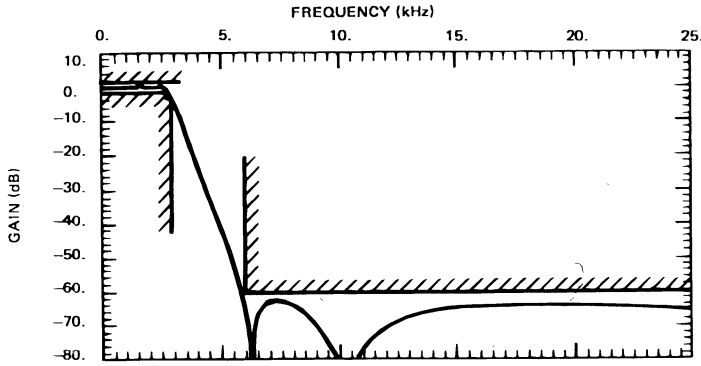
M88TS68951-23

RECONSTRUCTION FILTER TYPICAL RESPONSE AND LIMITS CHART.



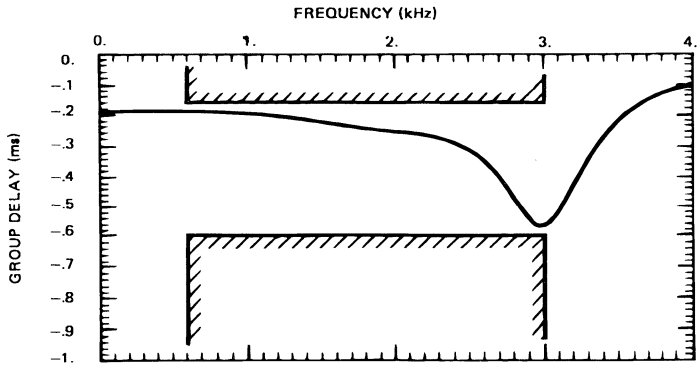
M88TS68951-24

RECONSTRUCTION FILTER TYPICAL RESPONSE AND LIMITS CHART.



M88TS68951-25

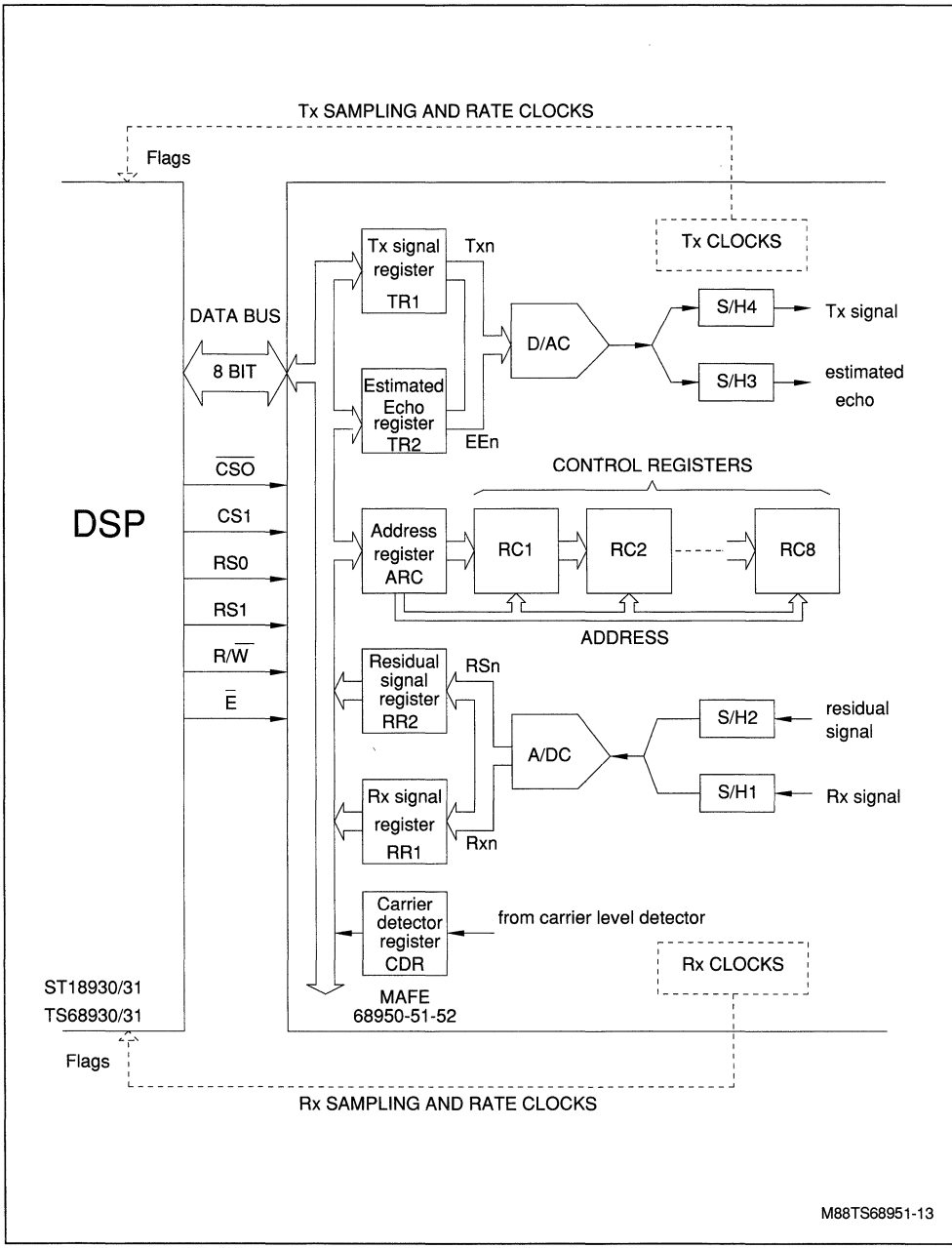
RECONSTRUCTION FILTER TYPICAL GROUP DELAY TIME AND LIMITS CHART.



M88TS68951-26

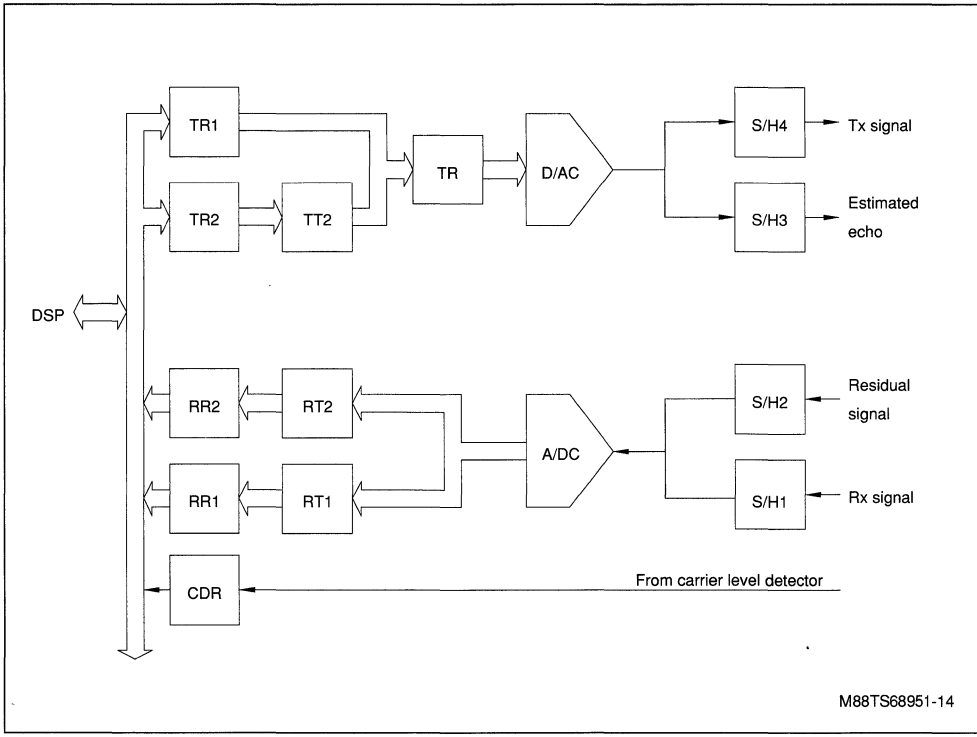
APPENDIX 2

INTERFACE BETWEEN DSP AND MODEM ANALOG FRONT-END (TS68950/1/2)



APPENDIX 3

DETAILED INPUT/OUTPUT REGISTERS DIAGRAM



	R/$\overline{W}$	RS0	RS1	Register Accessed
Writing	0	0	0	TR1
	0	0	1	TR2
	0	1	0	ARC
	0	1	1	Control Register Addressed by ARC
Reading	1	0	0	RR1
	1	0	1	RR2
	1	1	0	CDR
	1	1	1	Not Used

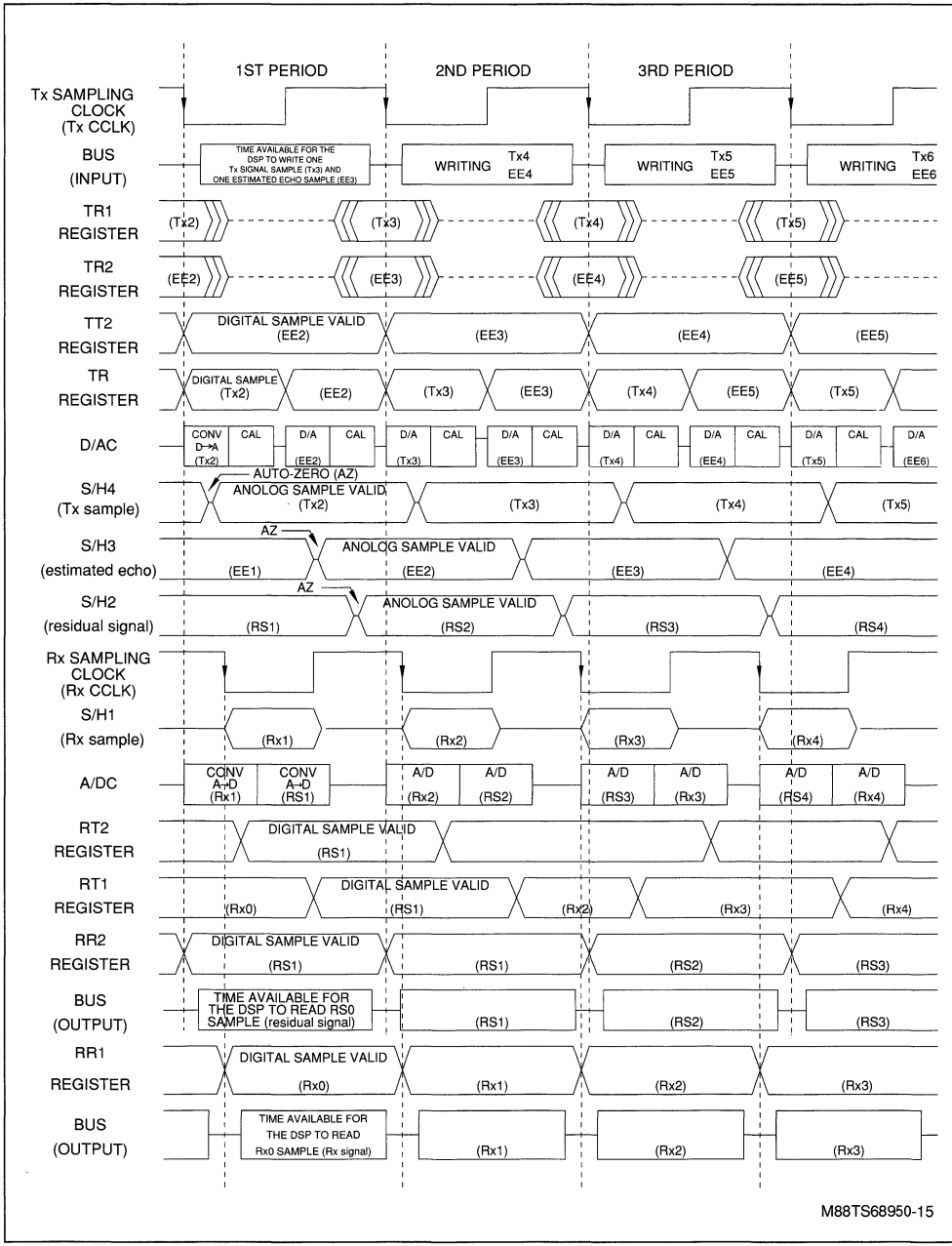
APPENDIX 4

CONTROL REGISTERS PROGRAMMING

Register Name	Circuit Including this Register	Register Content								Arc Content (register address)		
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5
RC1	68952	HB4	HB3	HB2	HB1	HR3	HR2	HR1		0	0	0
RC2	68952	HM3	HM2	HM1	HS2	HS1	HTHR			0	0	1
RC3	68051	HP2	HP1	LP2	LP1	REJ	S/A	REC		0	1	0
RC4	68950	ATE4	ATE3	ATE2	ATE1		EM2	EM1		0	1	1
RC5	68951	GR5	GR4	GR3	GR2	GR1				1	0	0
RC6	68951	GDS2	GDS1	HDS						1	0	1
RC7	68952	SP5	SP4	SP3	SP2	SP1				1	1	0
RC8	68952	MPE	SPR	AVRE	VAL	INIT				1	1	1

APPENDIX 5

PROGRESSION OF THE DIGITAL AND ANALOG SAMPLES IN THE MAFE



M88TS68950-15

APPENDIX 6

FURTHER REFERENCES

1/MAFE CHARACTERIZATION REPORT

This report gives the results of the measurements performed on the TS68950-51-52 Modem Analog Front-End (MAFE) chip set.

Chapter 1 describes the configuration and the method used for these measurements.

Chapter 2 comments the results obtained on the two signal paths of the transmit (Tx) analog front-end TS68950. i.e the echo path and the Tx signal path. Similarly chapter 3 gives the results obtained on the echo path and the receive (Rx) signal path of the Rx analog front-end TS68951.

Performances obtained on the TS68951 when using plesiochronous clocks are given in chapter 4. In this case, the TS68952 clock generator delivers the main clock and the two sampling clocks to the Rx analog interface.

2/MAFE EVALUATION BOARD

The MAFE evaluation board is a complete unit for evaluation of the TS68950/51/52 MAFE chip set.

The MAFE evaluation board is equipped with the TS68950/51/52 chip set and a phone line interface facilities.

It can be directly connectable to an external Digital Signal Processor through a 50-pins connector or can be linked to the SGS-THOMSON family of digital signal processors emulation-evaluation tools. In this case, along with the software tools (MACROASSEMBLER, SIMULATOR and LINKER), it provides a ready-to-use Digital Signal Processor System Interface well adapted to the analog word and high speed modems development.

3/APPLICATION NOTE

This application note describes the development of Real-Time Algorithms using the SGS-THOMSON Digital Signal Processor TS68930 and the MAFE chip set.

MODEM TRANSMIT/RECEIVE CLOCK GENERATOR

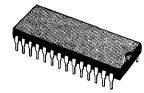
- INDEPENDANT TRANSMIT AND RECEIVE CLOCK GENERATORS WITH DIGITAL PHASE LOCKED LOOPS
- TRANSMIT DPLL SYNCHRONIZATION ON EXTERNAL TERMINAL CLOCK OR INTERNAL RECEIVE CLOCK
- RECEIVE DPLL SYNCHRONIZATION CONTROLLED FROM THE BUS
- FOUR EXTERNAL CLOCKS AVAILABLE, PLESIOCHRONOUS ON TRANSMIT AND RECEIVE CHANNELS :
  - BIT RATE CLOCK
  - BAUD RATE CLOCK
  - SAMPLING CLOCK
  - MULTIPLEXING CLOCK
- DIRECT INTERFACE WITH STANDARD MPU 8-BIT BUS
- LOW POWER CMOS TECHNOLOGY
- AVAILABLE IN DIL OR SURFACE MOUNT PACKAGE

DESCRIPTION

The TS68952 is a Clock Generator circuit designed to generate all the necessary clocks frequencies needed by high-speed modems applications.

The TS68952 copes with all the CCITT recommendations from V.22 to V.33 including full-duplex recommendations. Used in conjunction with the TS68950 Transmit (Tx) Analog Front-End circuit and the TS68951 Receive Analog Front-End*, it provides a very cheap and efficient interface to digital signal processing functions in high speed modems.

* The interconnection between the 3 chips of the Modem Analog Front-end (MAFE) and a DSP is decribed page 11/17.



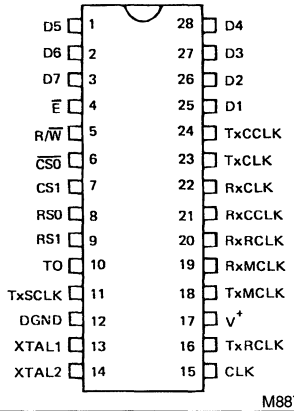
P
DIP 28
(Plastic Package)

FN
PLCC 28
(Plastic Package)

(Ordering information at the end of the data sheet.)

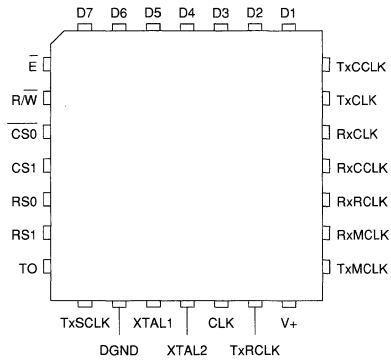
PIN CONNECTIONS

DIP 28



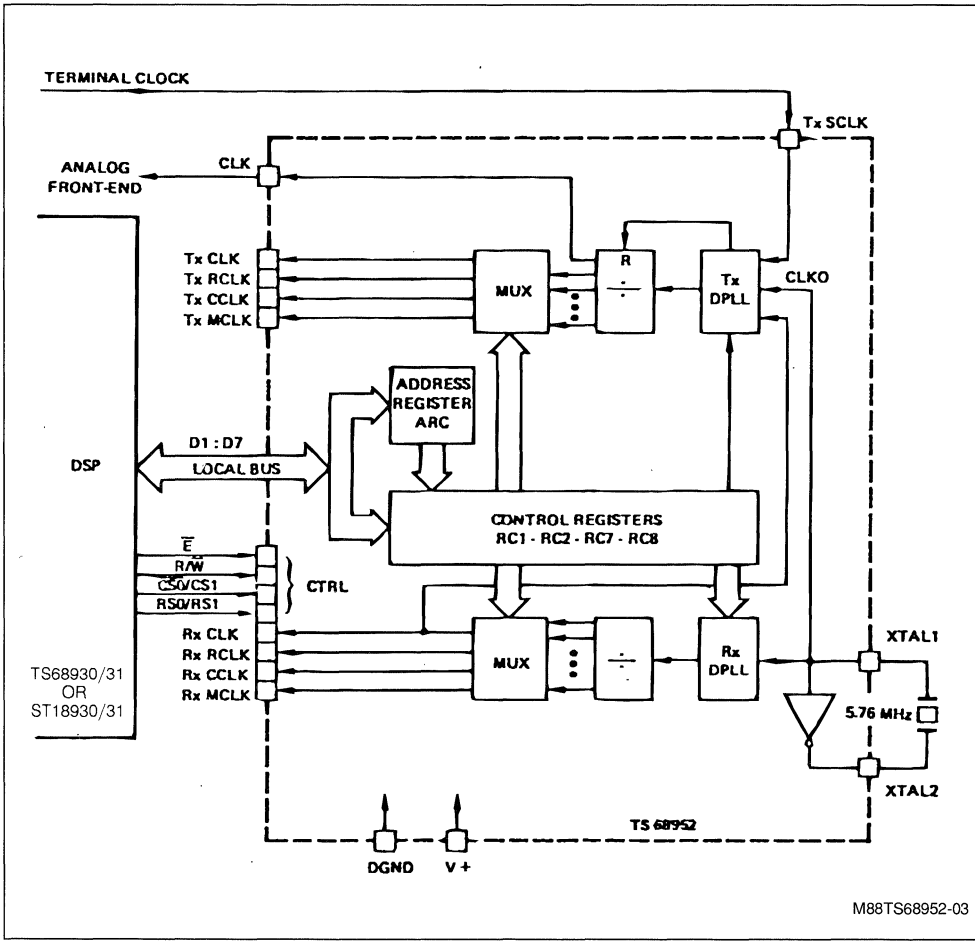
M88TS68952-01

PLCC 28



M88TS68952-02

BLOCK DIAGRAM



PIN FUNCTIONS

Name	Function
D1-D7	Data Bus Inputs to Internal Registers. (DO is not used)
$\overline{E}$	Enable Input. Data are strobed on the positive transitions of this input.
R/$\overline{W}$	Read/Write Selection Input. Internal registers can be written when R/W = 0. Reading mode is only used for Rx analog front-end chip.
$\overline{CS0}$-CS1	Chip Select Inputs. The chip set is selected when $\overline{CS0}$ = 0 and CS1 = 1
RS0-RS1	Register Select Inputs. Used to select address or control registers.
TO	Test Output. Must be left open.
TxSCLK	Transmit Synchronizing Clock Input. Normally tied to an external terminal clock. When this pin is tied to a permanent logical level, transmit DPLL free-runs or can be synchronized to the receive clock system.
DGND	Digital Ground = 0 V All digital signals are referenced to this pin.
XTAL1	Crystal Oscillator or Pulse Generator Input
XTAL2	Crystal Oscillator Output
CLK	1.44 MHz Clock output useful for Tx and Rx analog front-end chips.
TxRCLK	Transmit Baud Rate Clock Output
V^+	Positive Power Supply Voltage = + 5 V ± 5 %
TxMCLK	Transmit Multiplexing Clock Output
RxMCLK	Receive Multiplexing Clock Output
RxRCLK	Receive Baud Rade Clock Output
RxCCLK	Receive Conversion Clock Output
RxCLK	Receive Bit Rate Clock Output
TxCLK	Transmit Bit Rate Clock Output
TxCCLK	Transmit Conversion Clock Output

FUNCTIONAL DESCRIPTION

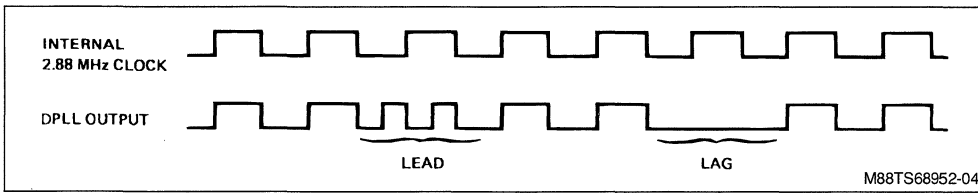
The TS68952 is a digital circuit that synthesises all the frequencies required to implement synchronous voice-grade MODEMs from 1200 bps to 19200 bps. It consists of two clock generators using Digital Phase Locked Loops (DPLLs). Frequency programming and DPLL updating can be obtained through four control registers accessed by indirect or cyclical addressing (see p 8117).

This circuit is a part of a three chip Modem Analog Front-End that also includes the TS68950 transmit analog interface and the TS68951 receive analog interface.

POWER-UP INITIAL CONDITIONS

Following power-up, the eight transmit and receive clock outputs are undefined and may deliver any frequencies. Control registers RC1 and RC2 must be properly programmed to obtain the requested operation.

Figure 1 : DPLL Lead and Lag.



CLOCK GENERATION

Master clock is obtained from either a crystal tied between XTAL1 and XTAL2 pins or an external signal connected to the XTAL1 pin ; in this case, the XTAL2 pin should be left open. Clock frequency nominal value is 5.76 MHz, but 5.12 MHz and 5.40 MHz frequencies are also specified for particular applications.

The different transmit (Tx) and receive (Rx) clocks are obtained by frequency division in several counters and output selection through digital multiplexers. They can be synchronized on external signal via two independent digital phase locked loops (DPLL).

TRANSMIT DPLL

As shown figure 1, the TxDPLL operates by adding or subtracting pulses to a 2.88 MHz internal clock, with a reference frequency that is a submultiple of the programmed "rate clock" frequency. This corresponds to phase leads or phase lags of about 350 ns duration, more precisely, two master clock periods.

The TxDPLL can be synchronized on an external terminal clock tied to TxSCLK pin or on the receive bit clock RxCLK internally generated from the RxDPLL. It can also free-run without any phase shift, when the TxSCLK input is tied to a fixed logical level.

TRANSMIT CLOCKS

The TS68952 delivers four synchronous Tx clocks :

- a bit clock, TxCLK, whose frequency equals the bit rate ot the modem,
- a baud clock, TxRCLK, whose frequency equals the baud rate of the modem,
- a conversion clock, TxCCLK, that gives the sampling frequency of the Tx converter (also used by the Rx converter in echo cancelling applications)
- a multiplexing clock, TxMCLK, usable when several terminals are multiplexed on a single physical link.

The frequencies of these four clocks are programmable through RC1 and RC2 control registers. Their cyclical ratio is exactly 1 : 2, except for the 16.8 kHz frequency whose cyclical ratio is slightly modulated around 1 : 2, and their relative phase locking is ensured without user intervention, by periodic reset of the counters.

Immediate phasing of these clocks on the synchronizing external TxSCLK or internal RxCLK clock can be obtained through bit 7 or RC8 register. The content of this register is automatically cleared after phasing completion.

The TS68952 also delivers, on pin CLK, a 1.44 MHz clock that is synchronous with the Tx clock system and will be used as the main clock to the TS68950/51 analog interface circuits.

RECEIVE DPLL

RxDPLL phase shifts are performed by addition and subtraction of pulses from an internal 1.44 MHz clock under the control of RC8 register. Two modes of operation are provided :

- a coarse phase lag whose amplitude has been loaded into RC7 register, can be controlled by one bit of RC8 register. This mode is useful for a fast synchronization of the RxDPLL. The phase lag is obtained by suppressing a variable number of pulses at the input of the counters,
- a fine phase shift with lead or lag amplitude equal to two master clock periods, can be controlled by two bits of RC8. This mode corresponds to normal operation. The phase shifts are obtained by addition or suppression of pulses as indicated in figure 1.

RC8 register is automatically cleared when the programmed phase shift is completed. Simultaneous programming of Tx and Rx control bits of this register has to be avoided.

RECEIVE CLOCKS

The TS68952 delivers four Rx clocks with the same nominal frequency values as their Tx counterparts :

- a bit clock RxCLK,
- a baud clock RxRCLK,
- a conversion clock RxCCLK,
- a multiplexing clock RxMCLK.

The Rx and Tx output clocks are plesiochronous.

BIT CLOCK FREQUENCY PROGRAMMING (Tx and Rx)

RC1 Register							Output Frequency (kHZ)		
D7	D6	D5	D4	D3	D2	D1			
HB4	HB3	HB2	HB1	HR3	HR2	HR1	F_Q = 5.76 MHz	F_Q = 5.40 MHz	F_Q = 5.12 MHz
0	0	0	0				19.2		
0	0	0	1				16.8		
0	0	1	0				14.4		
0	0	1	1				12.0		
0	1	0	0				9.6		
0	1	0	1				7.2		6.4
0	1	1	0				6.4		
0	1	1	1				6.0		
1	0	0	0				4.8		
1	0	0	1				3.2	3.0	
1	0	1	0				2.4		
1	0	1	1				1.2		
1	1	0	0				0.6		
1	1	0	1				0.6		
1	1	1	0				0.6		
1	1	1	1				0.6		

F_Q = crystal oscillator frequency.

RATE CLOCK FREQUENCY PROGRAMMING (Tx and Rx)

RC1 Register							Output Frequency (kHZ)		
D7	D6	D5	D4	D3	D2	D1			
HB4	HB3	HB2	HB1	HR3	HR2	HR1	F_Q = 5.76 MHz	F_Q = 5.40 MHz	F_Q = 5.12 MHz
				0	0	0	2.4		2.133
				0	0	1	2.0*		
				0	1	0	1.6**	1.5	
				0	1	1	1.2		
				1	0	0	0.6		
				1	0	1	0.6		
				1	1	0	0.6		
				1	1	1	0.6		

Note : Phase shift frequency of TxDPLL is 600 Hz excepted for (*) 1000 Hz and for (**) 800 Hz.

CONVERSION CLOCK FREQUENCY PROGRAMMING (Tx and Rx)

RC2 Register							Output Frequency (kHZ)		
D7	D6	D5	D4	D3	D2	D1			
HM3	HM2	HM1	HS2	HS1	HTHR	—	F_Q = 5.76 MHz	F_Q = 5.40 MHz	F_Q = 5.12 MHz
			0	0			9.6	9.0	8.533
			0	1			8.0	7.5	
			1	0			7.2		
			1	1			7.2		

MULTIPLEXING CLOCK FREQUENCY PROGRAMMING (Tx and Rx)

RC2 Register							Output Frequency (kHz)
D7	D6	D5	D4	D3	D2	D1	
HM3	HM2	HM1	HS2	HS1	HTHR	–	F_Q = 5.76 MHz
0	0	0					1440
0	0	1					288
0	1	0					12
0	1	1					9.6
1	0	0					7.2
1	0	1					4.8
1	1	0					2.4
1	1	1					1.2

Tx SYNCHRONIZATION SIGNAL PROGRAMMING

RC2 Register							Synchronization Signal
D7	D6	D5	D4	D3	D2	D1	
HM3	HM2	HM1	HS2	HS1	HTHR	–	
					0		RxCLK
					1		TxSCLK (note 1)

Note : 1. TxDPLL free-runs if there is no transition on this input.

TxCLOCK GENERAL RESET

RC8 Register (notes 2, 3)							The Tx counters are resetted on the first negative-going transition of the synchronization signal following MPE programming to 1.
D7	D6	D5	D4	D3	D2	D1	
MPE	SPR	AVRE	VAL	INIT	–	–	
1	0	0	0	0			Next Negative-Going Transition on Synchronization Signal.

Notes : 2. RC8 register is cleared after the programmed control operation is completed.
3. INIT bit is only used for test purpose.

RxCLOCK PHASE SHIFT PROGRAMMING

RC8 Register (note 2)							Action on RxDPLL
D7	D6	D5	D4	D3	D2	D1	
MPE	SPR	AVRE	VAL	INIT	-	-	
0	1	0	0	0			Phase Lag of Programmed Amplitude
0	0	0	1	0			Phase Lag of Two 5.76 MHz Master Clock Periods
0	0	1	1	0			Phase Lead of Two 5.76 MHz Master Clock Periods

RxCLOCK PHASE SHIFT AMPLITUDE PROGRAMMING

RC7 Register							Phase Shift in Degrees		Number of Master Clock Pulses Suppressed
D7	D6	D5	D4	D3	D2	D1			
SP5	SP4	SP3	SP2	SP1	-	-	1200 Bauds*	1600 Bauds	
0	0	0	0	0			1.5	2	20
0	0	0	0	1			3	4	40
0	0	0	1	0			4.5	6	60
0	0	0	1	1			6	8	80
0	0	1	0	0			7.5	10	100
0	0	1	0	1			9	12	120
0	0	1	1	0			10.5	14	140
0	0	1	1	1			12	16	160
0	1	0	0	0			13.5	18	180
0	1	0	0	1			15	20	200
0	1	0	1	0			16.5	22	220
0	1	0	1	1			18	24	240
0	1	1	0	0			19.5	26	260
0	1	1	0	1			21	28	280
0	1	1	1	0			22.5	30	300
0	1	1	1	1			24	32	320
1	0	0	0	0			22.5	30	300
1	0	0	0	1			45	60	600
1	0	0	1	0			67.5	90	900
1	0	0	1	1			90	120	1200
1	0	1	0	0			112.5	150	1500
1	0	1	0	1			135	180	1800
1	0	1	1	0			157.5	210	2100
1	0	1	1	1			180	240	2400
1	1	0	0	0			202.5	270	2700
1	1	0	0	1			225	300	3000
1	1	0	1	0			247.5	330	3300
1	1	0	1	1			270	360	3600
1	1	1	0	0			292.5		3900
1	1	1	0	1			315		4200
1	1	1	1	0			337.5		4500
1	1	1	1	1			360		4800

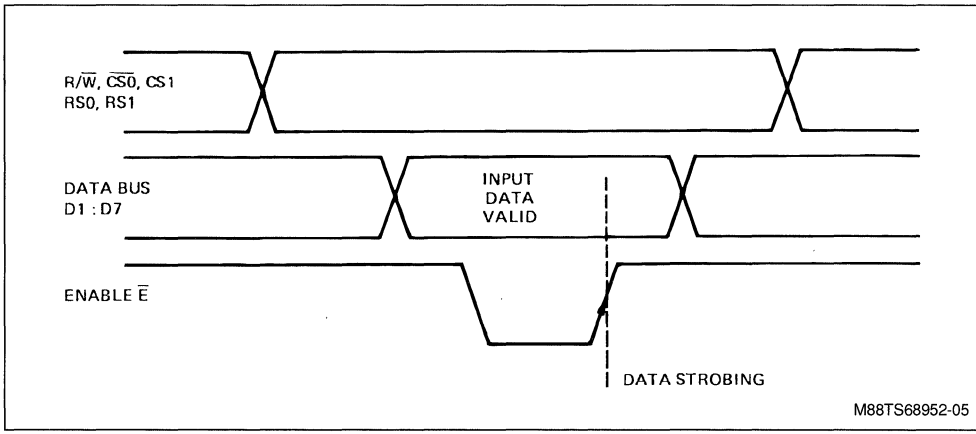
(*) 2400 bauds : multiply by two. 600 bauds : divide by two.

DATA BUS CONTROL

Six signals control the access from the bus to the internal registers according to the table and the timing diagram given below. Control registers are written using an indirect addressing mode where the internal address is stored in the 3 bit ARC register. After each write operation to a control register, the ARC register value is automatically increased by one. This allows cyclical addressing of the eight registers of the MODEM chip set.

R/$\overline{W}$	$\overline{CS0}$	CS1	RS0	RS1	$\overline{E}$	Accessed Register
0	0	1	1	0	↓	Address Register ARC
0	0	1	1	1	↓	Control Register whose Address is in ARC

BUS TIMING DIAGRAM



DATA FORMAT

Data Loaded in ARC			Addressed Register
D7	D6	D5	
ARC3	ARC2	ARC1	
0	0	0	RC1
0	0	1	RC2
1	1	0	RC7
1	1	1	RC8

ABSOLUTE MAXIMUM RATINGS

Parameter	Min.	Max.	Unit
V^+ Supply Voltage to DGND Ground	– 0.3	7	V
Voltage at any Input or Output	DGND – 0.3	V^+ + 0.3	V
Current at any Output	– 20	20	mA
Power Dissipation		500	mW
Operating Temperature Range	0	70	°C
Storage Temperature Range	– 65	+ 150	°C

OPERATING RANGE

Ambient Temperature	V^+	DGND
0 °C ≤ t_{amb} ≤ 70 °C	+ 5.0 V ± 5 %	0 V

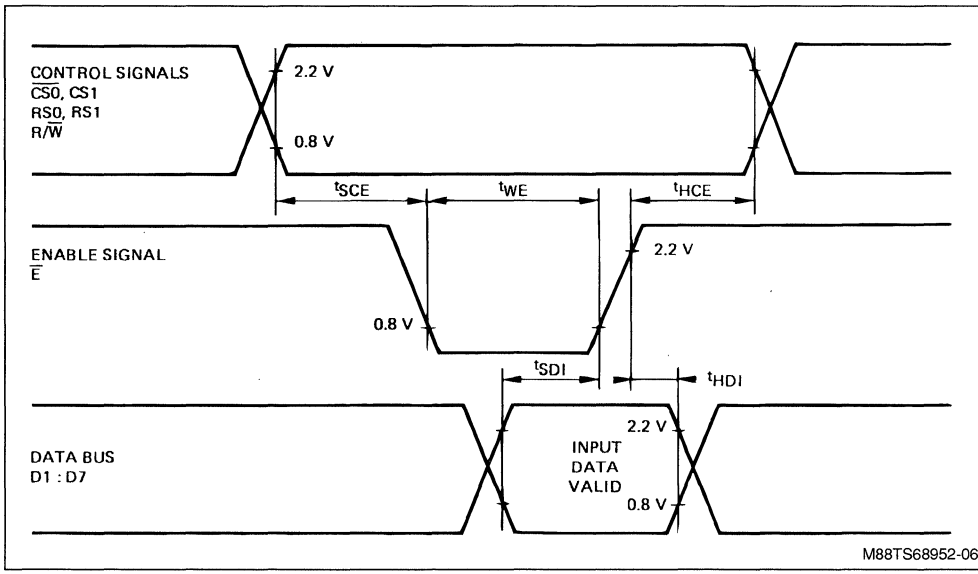
ELECTRICAL OPERATING CHARACTERISTICS

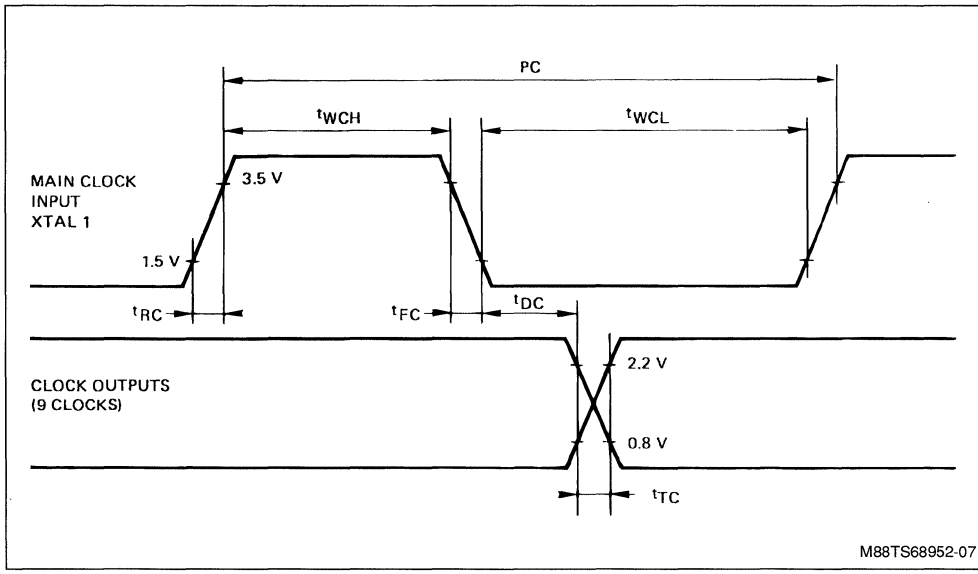
Unless otherwise noted, electrical characteristics are specified over the operating range. Typical values are given for V^+ = 5.0 V and T_{amb} = 25 °C

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Power Dissipation						
I^+	Positive Supply Current				5.0	mA
Digital Interface						
V_{IL}	Input Low Level Voltage				0.8	V
V_{IH}	Input High Level Voltage		2.2			V
I_{IL}	Input Low Level Current	DGND ≤ V_I ≤ $V_{IL\ max}$	– 10		10	µA
I_{IH}	Input High Level Current	$V_{IH\ min}$ ≤ V_I ≤ V^+	– 10		10	µA
V_{OL}	Output Low Level Current	I_O = 2.5 mA			0.4	V
V_{OH}	Output High Level Current	I_O = – 2.5 mA	2.4			V
Crystal Oscillator Interface						
V_{IL}	Input Low Level Voltage				1.5	V
V_{IH}	Input High Level Voltage		3.5			V
I_{IL}	Input Low Level Curent	DGND ≤ V_I ≤ $V_{IL\ max}$	- 15			µA
I_{IH}	Input High Level Current	$V_{IH\ min}$ ≤ V_I ≤ V^+			15	µA

TIMING CHARACTERISTICS

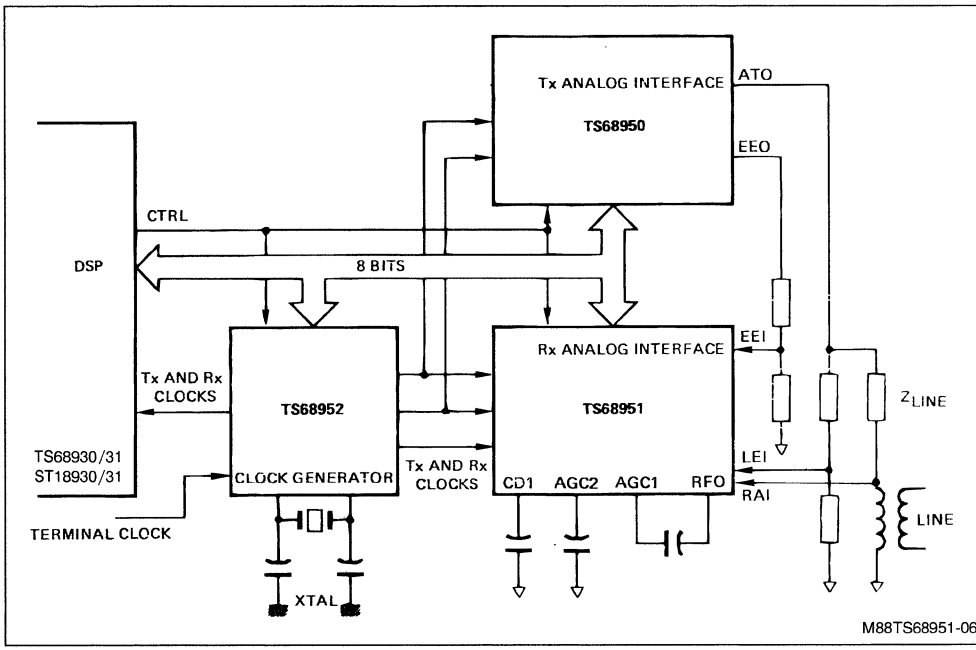
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Data Bus Access						
t_{SCE}	Control Signals Set-up Time	$\overline{CS0}$, CS1, RS0, RS1, R/$\overline{W}$ to $\overline{E}$	40			ns
t_{HCE}	Control Signals Hold Time	$\overline{CS0}$, CS1, RS0, RS1, R/$\overline{W}$ to $\overline{E}$	10			ns
t_{SDI}	Data-in Set-up Time	D1 : D7 to $\overline{E}$	120			ns
t_{HDI}	Data-in Hold Time	D1 : D7 to $\overline{E}$	10			ns
t_{WE}	Enable Signal Low Level Width	$\overline{E}$		180		ns
Clock Wave forms						
PC	Main Clock Period	XTAL1 Input	150	173.6		ns
t_{WCL}	Main Clock Low Level Width	XTAL1 Input	50			ns
t_{WCH}	Main Clock High Level Width	XTAL1 Input	50			ns
t_{RC}	Main Clock Rise Time	XTAL1 Input			50	ns
t_{FC}	Main Clock Fall Time	XTAL1 Input			50	ns
t_{DC}	Clock Output Delay Time	All Clock Outputs CL = 50 pF			500	ns
t_{TC}	Clock Output Transition Time	All Clock Outputs CL = 50 pF			100	ns


CONTROL SIGNALS
CS0, CS1
RS0, RS1
R/W
2.2 V
0.8 V
tSCE
tWE
tHCE
ENABLE SIGNAL
E
2.2 V
0.8 V
tSDI
tHDI
DATA BUS
D1 : D7
2.2 V
INPUT
DATA
VALID
0.8 V
M88TS68952-06


PC
tWCH
tWCL
MAIN CLOCK
INPUT
XTAL 1
3.5 V
1.5 V
tRC
tFC
tDC
CLOCK OUTPUTS
(9 CLOCKS)
2.2 V
0.8 V
tTC
M88TS68952-07

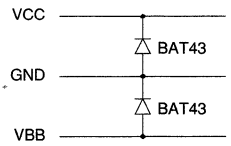
APPLICATIONS INFORMATIONS

MODEM ANALOG FRONT-END CHIP SET (TS38950/51/52).



Notes : 1. ⏚ Digital ground.
⏚ Analog ground.

2. In some cases, external-user circuitry may induce power-up sequency latch-up problems that can be efficiently avoided using ST BAT43 schottky small signal diodes as follow :



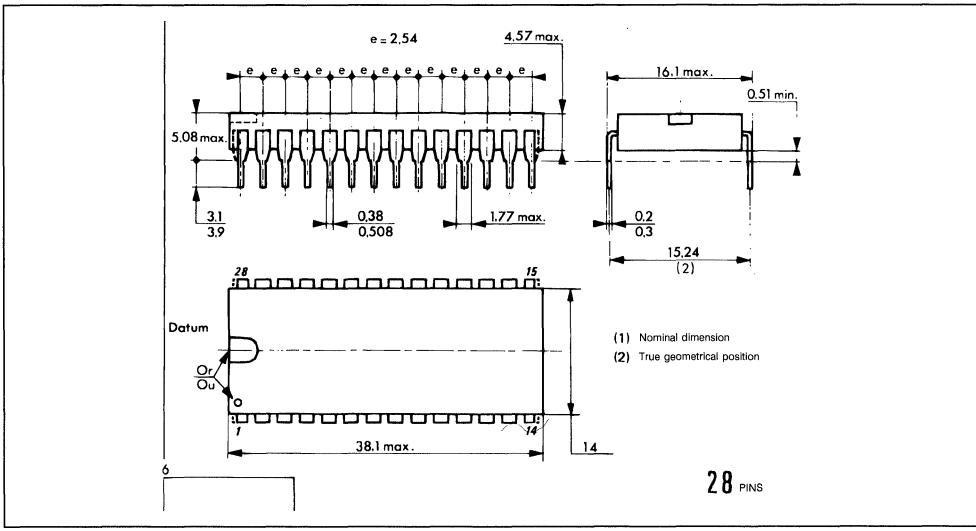
M88TS68951-09

ORDERING INFORMATION

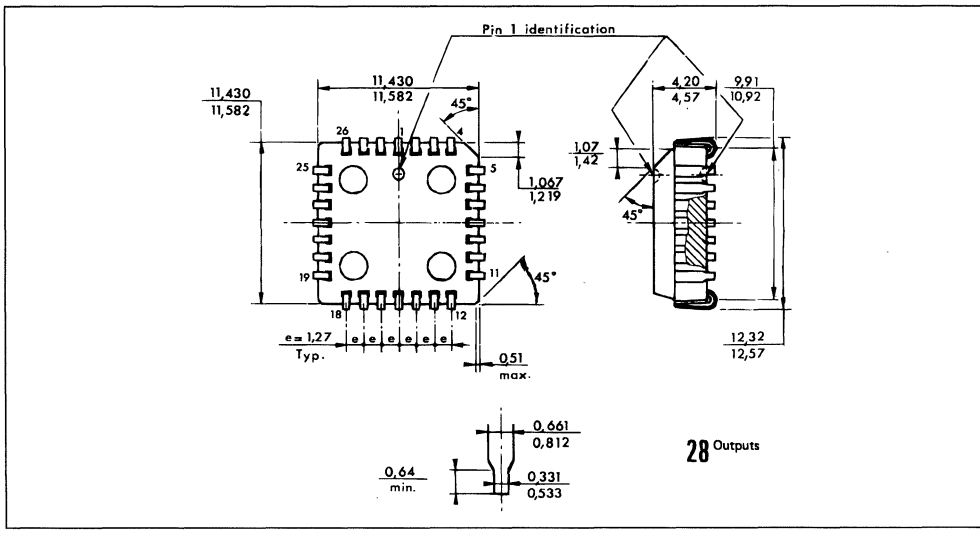
Part Number	Temperature Range	Package
TS68952CP	0 to + 70 °C	DIP28
TS68952CFN	0 to + 70 °C	PLCC28

PACKAGE MECHANICAL DATA

CB-132 – 28 PIN – PLASTIC DIP

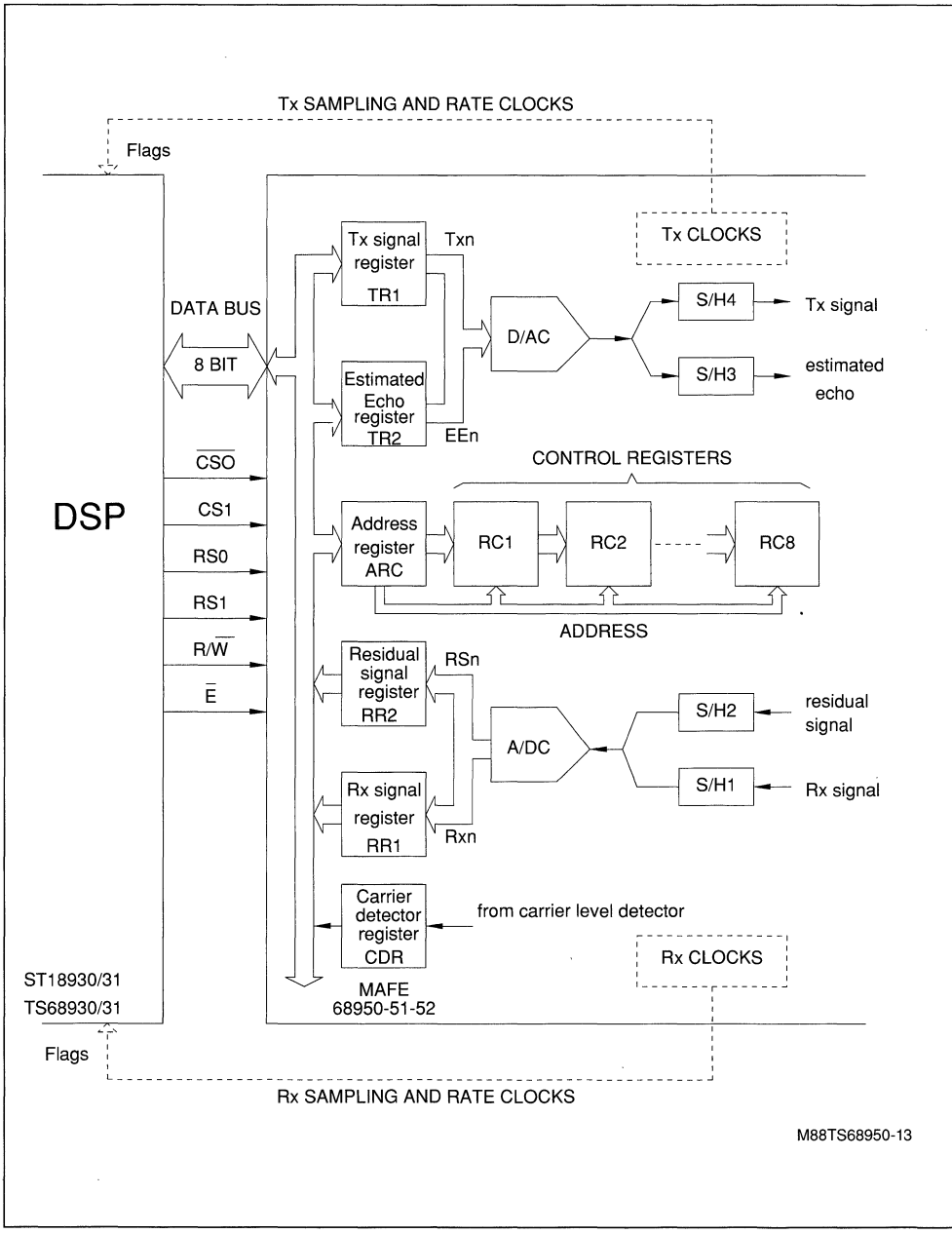


CB-520 – 28 PIN – PLASTIC LEADLESS CHIP CARRIER



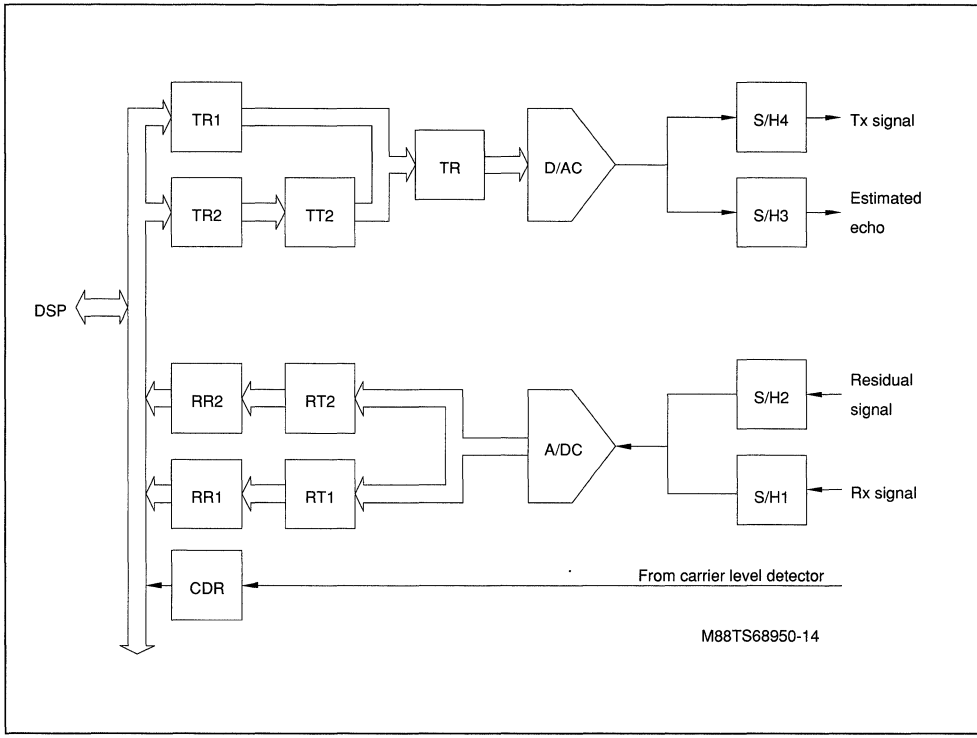
APPENDIX 1

INTERFACE BETWEEN DSP AND MODEM ANALOG FRONT-END (TS68950/51/52)



APPENDIX 2

DETAILED INPUT/OUTPUT REGISTERS DIAGRAM



	R/$\overline{W}$	RS0	RS1	Register Accessed
Writing	0	0	0	TR1
	0	0	1	TR2
	0	1	0	ARC
	0	1	1	Control Register Addressed by ARC
Reading	1	0	0	RR1
	1	0	1	RR2
	1	1	0	CDR
	1	1	1	Not Used

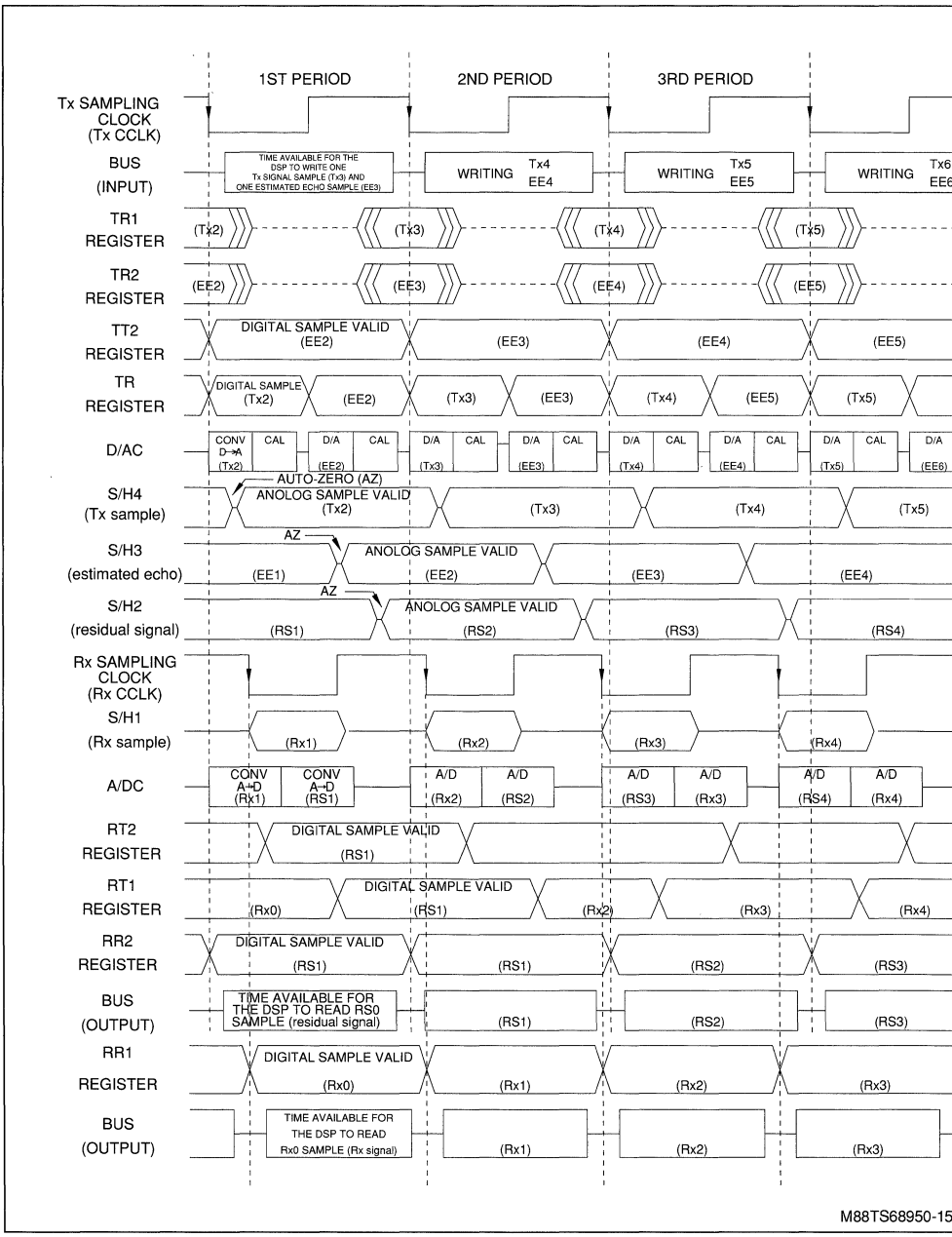
APPENDIX 3

CONTROL REGISTERS PROGRAMMING

Register Name	Circuit Including this Register	Register Content								ARC Content (register address)		
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5
RC1	68952	HB4	HB3	HB2	HB1	HR3	HR2	HR1	-	0	0	0
RC2	68952	HM3	HM2	HM1	HS2	HS1	HTHR	-	-	0	0	1
RC3	68951	HP2	HP1	LP2	LP1	REJ	S/A	REC	-	0	1	0
RC4	68950	ATE4	ATE3	ATE2	ATE1	-	EM2	EM1	-	0	1	1
RC5	68951	GR5	GR4	GR3	GR2	GR1	-	-	-	1	0	0
RC6	68951	GDS2	GDS1	HDS	-	-	-	-	-	1	0	1
RC7	68952	SP5	SP4	SP3	SP2	SP1	-	-	-	1	1	0
RC8	68952	MPE	SPR	AVRE	VAL	INIT	-	-	-	1	1	1

APPENDIX 4

PROGRESSION OF THE DIGITAL AND ANALOG SAMPLES IN THE MAFE



APPENDIX 5

FURTHER REFERENCES

1/MAFE CHARACTERIZATION REPORT

This report gives the results of the measurements performed on the TS68950-51-52 Modem Analog Front-End (MAFE) chip set.

Chapter 1 describes the configuration and the method used for these measurements.

Chapter 2 comments the results obtained on the two signal paths of the transmit (Tx) analog front-end TS68950. i.e the echo path and the Tx signal path. Similarly chapter 3 gives the results obtained on the echo path and the receive (Rx) signal path of the Rx analog front-end TS68951.

Performances obtained on the TS68951 when using plesiochronous clocks are given in chapter 4. In this case, the TS68952 clock generator delivers the main clock and the two sampling clocks to the Rx analog interface.

2/MAFE EVALUATION BOARD (EFRMAFE)

The MAFE evaluation board is a complete unit for evaluation of the TS68950/51/52 MAFE chip set.

The MAFE evaluation board is equipped with the TS68950/51/52 chip set and phone line interface facilities.

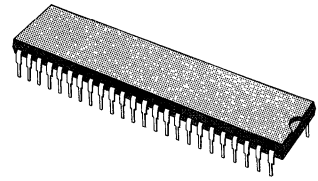
It can be directly connectable to an external Digital Signal Processor through a 50-pins connector or can be linked to the SGS-THOMSON family of digital signal processors emulation-evaluation tools. In this case, along with the software tools (MACROASSEMBLER, SIMULATOR and LINKER), it provides a ready-to-use Digital Signal Processor System Interface well adapted to the analog word and high speed modems development.

3/APPLICATION NOTE

This application note describes the development of Real-Time Algorithms using the SGS-THOMSON Digital Signal Processor TS68930 and the MAFE chip set.

DIGITAL ECHO CANCELLER

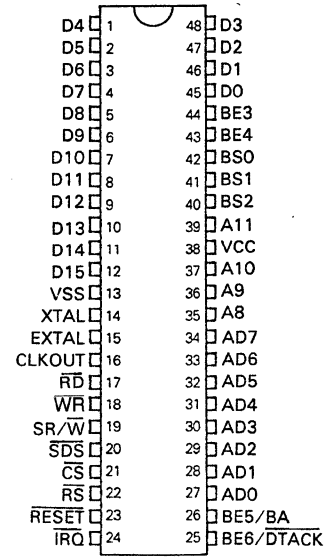
- SIMPLIFIED INTERFACE CIRCUITRY FOR FLEXIBLE ADAPTION TO A WIDE RANGE OF V.32 CONFIGURATIONS
- DOVETAILED HARDWARE AND FIRMWARE CONNECTION WITH TS68950/1/2 MODEM ANALOG FRONT-END CHIP SET
- KEY COMPONENT IN THE ADVANCED TS7532 V.32 MODEM
- 16 msec OF ECHO PATH IMPULSE RESPONSE IN THE NEAR END AND IN THE FAR-END CANCELLERS
- 1.14 SEC OF CHANNEL DELAY (two satellite hops) IN FAR-END ECHO CANCELLER.
- 10Hz OF FREQUENCY OFFSET IN FAR-END ECHO PATH
- MEETS OR EXCEEDS THE REQUIREMENTS OF CCITT RECOMMENDATION V.32



P
DIP-48
(Plastic Package)

(Ordering Information at the end of the datasheet)

PIN CONNECTIONS



M88TS75320-01

DESCRIPTION

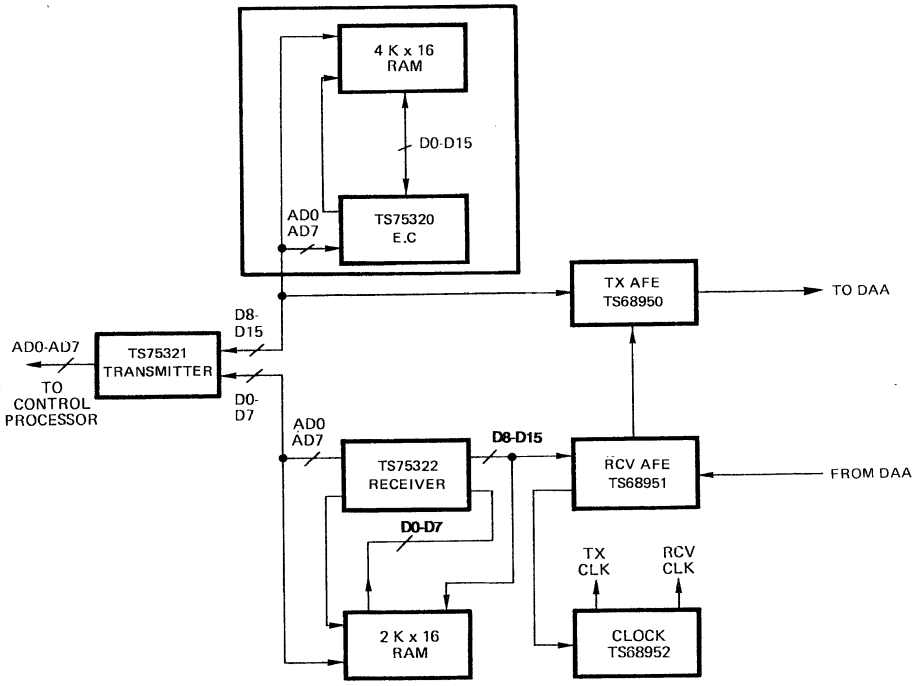
The TS75320 is a high performance voiceband data modem echo canceller implemented on a single chip using advanced digital signal processing technology. Using sophisticated adaptive algorithms, the TS75320 realizes the high precision cancellation of near-end and far-end echoes, even in the presence of frequency offset in the far end echo.

The residual cancellation levels and convergence rates of the TS75320 meet or exceed the demanding requirements of high performance V.32 modems.

The TS75320 is ideally suited for high performance low-cost integrated V.32 solutions.

BLOCK DIAGRAM

Figure 1 : Shows a Configuration for a V.32 Modem utilizing the TS75320 with the TS68950/51/52 MAFE Chip Set.



M88TS75320-02

PIN DESCRIPTION

LOCAL INTERFACE

Pin Name	Pin N°	Type	Function	Description
D (0:15)	45-48 1-11	I/O	Data Bus	D(0:15) Data Bus
A (8:11)	35.37.39	O	Address Bus	High Order Addresses for Local Interface
$\overline{RD}$	17	O	Read	Transfer Data Read
$\overline{WR}$	18	O	Write	Transfer Data Write
CLKOUT	16	O	Clock Output	The frequency of CLKOUT is one half the frequency of the input clock or crystal.

SYSTEM INTERFACE

Pin Name	Pin N°	Type	Function	Description
AD (0:7)	27-34	I/O	System Data Bus or Local Address Bus	The data exchanges between the processor and a master via a mailbox is the function of this bus. It is also used to generate the addresses of an external RAM.
$\overline{CS}$	21	I	Chip Select	Used by a Master to Gain Access to the Mailbox and System Bus
$\overline{RS}$	22	I	Register Select	Used by a Master to Gain Access to the Mailbox and System Bus
$\overline{SDS}$	20	I	System Data Strobe	Synchronizes the Transfer on the System Bus
SR/$\overline{W}$	19	I	System Read/Write	Indicates the Current System Bus Cycle State
$\overline{DTACK}$	25	O	Data Transfer Acknowledge	Indicates that the processor has recognized it is being accessed.
BA	26	O	Bus Available	Indicates Availability of System Bus to Master
$\overline{IRQ}$	24	O	Interrupt Request	Handshake signal sent to the master gain access to the mailbox.

OTHER PINS

Pin Name	Pin N°	Type	Function	Description
EXTAL	15	I	Clock	Crystal Input Pin for Internal Oscillator or Input Pin for External Oscillator
XTAL	14	I	Clock	Together with EXTAL it is used for the external 25 MHz crystal.
VCC	38	I	Power Supply	
VSS	13	I	Ground	
$\overline{RESET}$	23	I	Reset	

FUNCTIONAL DESCRIPTION

PERFORMANCE SUMMARY

The TS75320 performance figures below are obtained with analog front-end D/A converters with integral linearity of 12 bits or better, such as the TS68950.

- Near-end echo cancellation : > 55 dB

  With a near-end echo level of - 10 dBm at the receiver input, in the absence of a far-end signal and of a far-end echo, the residual echo level is below - 65 dBm.
- Combined near–end and far–end echo cancellers :

  For a typical receive level of –20 dBm and far-end echo smaller than –28 dBm the received signal to residual echo ratio is better than 24 dB even in the presence of up to 10 Hz of frequency offset in the far-end echo.
- The signal to residual echo ratio is better than 21 dB even for receive levels as small as –40 dBm, provided that the far-end echo is 8 dB below the received far-end signal.
- The far-end echo channel delay can be as large as 1.14 s.
- Convergence Time : meets or exceeds CCITT V.32 handshake requirements.

ECHO CANCELLER OPERATION

The principal task of the echo canceller is the determination by means of adaptive algorithms, of the coefficients of digital filters and phasing processors that will generate a modem receiver input free of near-end or far-end echoes. The signals processed by the echo canceller are the cancellation error at the receiver input and the V.32 date sequence being transmitted. These signals will normally be available in the appropriate format in a digitally realized modem.

The echo canceller hardware and firmware have been designed for ease of interface with a general purpose DSP or microprocessor and require minimal interaction with the modem. In this section we describe the hardware and software interfaces to the TS75320.

HARDWARE INTERFACE

The TS75320 echo canceller is configured as an essentially self-contained digital peripheral interfaced to a host microcontroller or to a host digital signal processor through an 8-bit system bus. The bus interface dovetails with the control bus of the TS68930 digital signal processor. Straightforward interconnection to other processors or to peripheral circuits is realized by wirtue of an asynchronous mailbox that is readily controlled by means of a flexible handshake protocol.

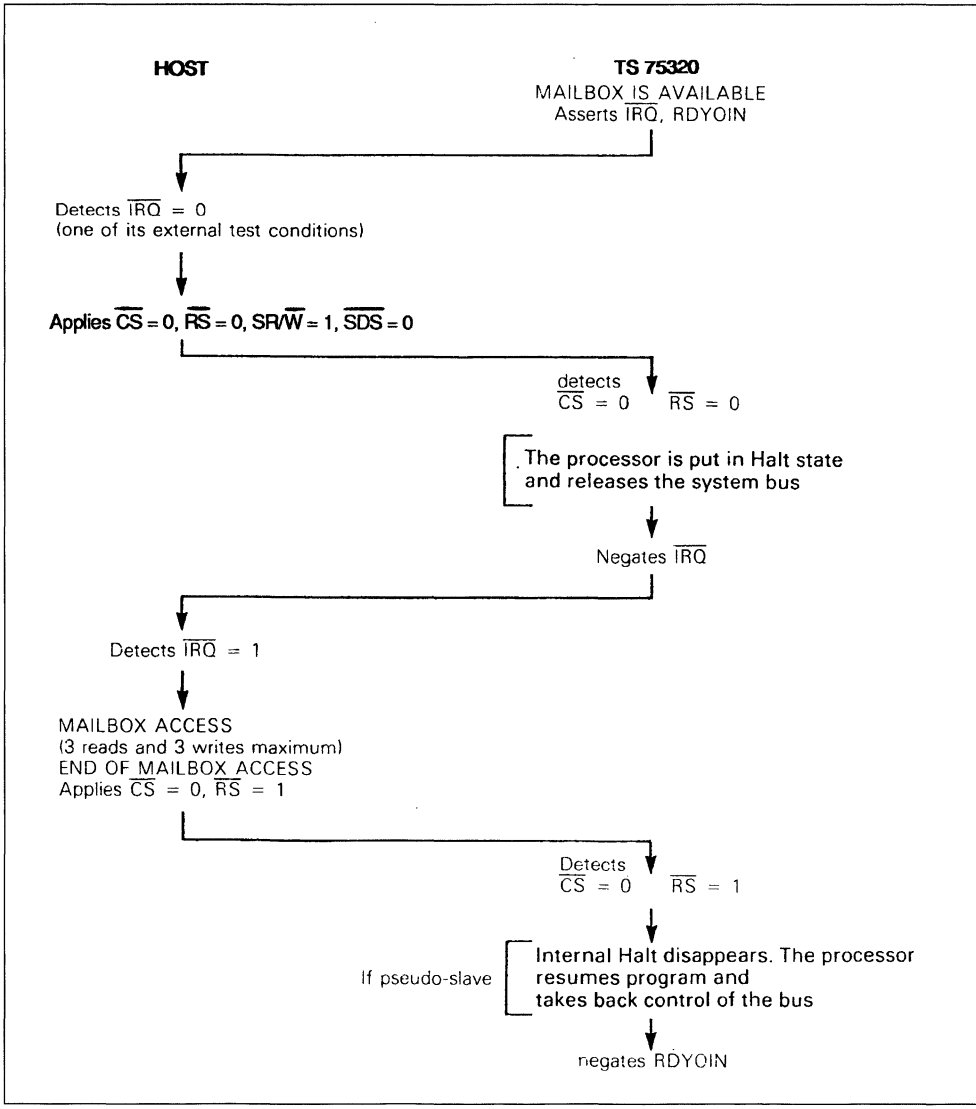
The system bus is also used for addressing the echo canceller external RAM, during which time it is not available to the host controller. Data transfer to the echo canceller's RAM is effected through the 16-bit data bus.

The timing of all communications with the host is determined by the echo canceller.

Data for transmission to the host is loaded into the TS75320 three-byte wide ROUT shift register. The communication process is effected by means of the mailbox transfer protocol. Data for transmission from the host is stored in the TS75320 RIN register, which is also three bytes wide.

The operation of the mailbox transfer protocol is described schematically in the flow chart in Figure 2.

Figure 2 : Mailbox Handshake Protocol.



While the mailbox protocol is in progress only, the host may deselect the TS75320 ($\overline{CS} = 1$) to use the system bus to communicate with other peripherals.

At all other times, the system bus is under the control of the TS75320 and it is therefore essential that the connection of the bus to the host be tri-state at those times.

FIRMWARE INTERFACE

The echo canceller firmware is designed in the first instance for V.32 modem applications, and therefore operates at a Baud rate of 2400 symbols per second. The sampling rate is 7200 per second, i.e. three samples per Baud interval.

In the period of one Baud interval, the echo canceller generates three echo estimates, one for each of the three receiver samples, and it requires the input of the three corresponding echo cancellation errors. The echo estimates and the cancellation errors are both 16 bit quantities. The echo canceller requires also the input of the complex-valued V.32 format current symbol from the transmitter, this is the reference signal for the computation of the echo estimates. By virtue of the V.32 constellation requirements, three bits are sufficient for the representation of the real and imaginary parts, respectively. Hence, the transfer of this signal is effected with a single byte (the four MSBs for the real part, the four LSBs for the imaginary part).

Three mailbox exchanges are required per Baud interval to transfer the data. Once an echo estimate has been computed, it is stored in the TS75320 ROUT register (3-byte wide). The LSB and MSB are stored in the first and second bytes, respectively.

The TS75320 then initiates a mailbox transfer during which the host reads the echo estimate (LSBs followed by MSBs) and stores the two bytes for the transmitted symbol. The mailbox transfer operation is identical for the second and third echo estimates and for the cancellation errors except that there is no need for the transmitted symbol to be transferred more than once per baud interval.

Particular care must be taken, however, to ensure that the modem does not hold the echo canceller during the mailbox transfer for more than the time required for the data transfer. Otherwise problems relating to cycle duration may arise.

INITIALIZATION

The echo canceller is initialized by first asserting the reset signal (RESET = 0) for at least 640 ns. The TS75320 will then automatically clear its internal status and filter coefficients. It will then wait for a mailbox transfer consisting of the following three hexadecimal bytes : AA AA 00. This will indicate the beginning of echo canceller configuration.

The first mailbox transfer after the configuration bytes must contain the far-end echo round trip delay expressed in number of Baud periods. This number must be smaller than 3000 (1.25 seconds). The echo canceller will interpret the first two bytes in its RIN register as the round trip delay, LSBs followed by MSBs, right justified. If the third byte is 0, the far-end echo canceller is disabled. If it is 1, the far-end canceller is enabled.

The near-end echo canceller convergence is enabled by the following 3 bytes in the RIN register of the TS75320 : AA AA 01. If the far-end echo canceller is enabled it will start adapting automatically once the near-end echo canceller has converged.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}*	Supply Voltage	– 0.3 to 7.0	V
V_{in}*	Input Voltage	– 0.3 to 7.0	V
T_A	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

* With respect to V_{SS}.

Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

DC ELECTRICAL OPERATING - CHARACTERISTICS

V_{CC} = 5.0 V ± 5 %, V_{SS} = 0, T_{amb} = 0 to + 70 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IL}	Input Low Voltage	– 0.3	–	0.8	V
V_{IH}	Input High Voltage	2.4	–	V_{CC}	V
I_{in}	Input Leakage Current Except EXTAL	– 10	–	10	µA
I_i	Input EXTAL Current	– 50	–	50	µA
V_{OH}	Output High Voltage (I_{load} = – 300 µA)	2.7	–	–	V
V_{OL}	Output Low Voltage (I_{load} = 3.2 mA)	–	–	0.5	V
P_D	Power Dissipation	–	1.5	–	W
C_{in}	Input Capacitance	–	10	–	pF
I_{TSI}	Three State (off state) Input Current	– 20	–	20	µA

AC ELECTRICAL SPECIFICATIONS - CLOCK AND CONTROL PINS TIMING

(VCC = 5.0V ± 5%, Tamb = 0° to +70°C ; see figure 3)

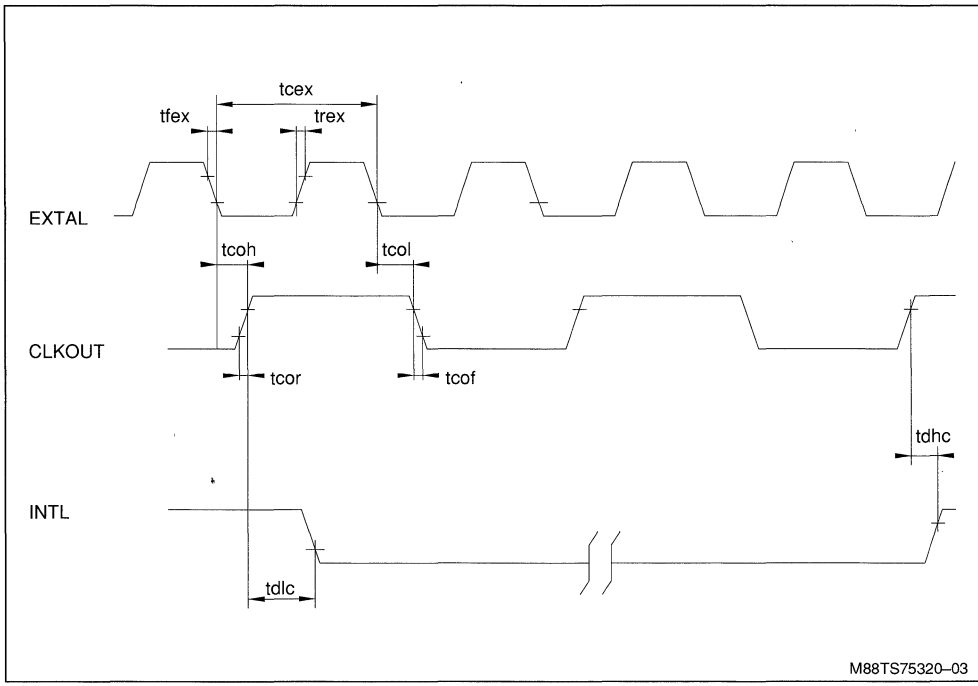
Output load = 50 pF + DC characteristics load

Reference levels : V_{IL} : 0.45 V V_{IH} : 2.4 V

V_{OL} : 0.45 V V_{OH} : 2.4 V tr, tf ≤ 5 ns for input signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{cex}	External Clock Cycle Time	40		160	ns
t_{fex}	External Clock Fall Time			5	ns
t_{rex}	External Clock Rise Time			5	ns
t_{coh}	EXTAL to CLKOUT High Delay		25		ns
t_{col}	EXTAL to CLKOUT Low Delay		25		ns
t_{rco}	CLKOUT Rise Time			10	ns
t_{fco}	CLKOUT Fall Time			10	ns
t_{dsl}	CLKOUT to $\overline{DS}$, $\overline{RD}$, $\overline{WR}$ Low		5		ns
t_{dsh}	CLKOUT to $\overline{DS}$, $\overline{RD}$, $\overline{WR}$ High		5		ns
t_{sc}	Control Inputs Set-up Time (BS0... BS2, BE3... BE6, $\overline{Reset}$, $\overline{Halt}$)	20			ns
t_{hc}	Control Inputs Hold Time (BS0... BS2, BE3... BE6, $\overline{Reset}$, $\overline{Halt}$)	10			ns
t_{dlc}	CLKOUT to Control Output Low ($\overline{IRQ}$, BA)			50	ns
t_{dhc}	CLKOUT to Control Output High (BA, $\overline{IRQ}$)			50	ns

Figure 3 : Clock and Control Pins Timing.

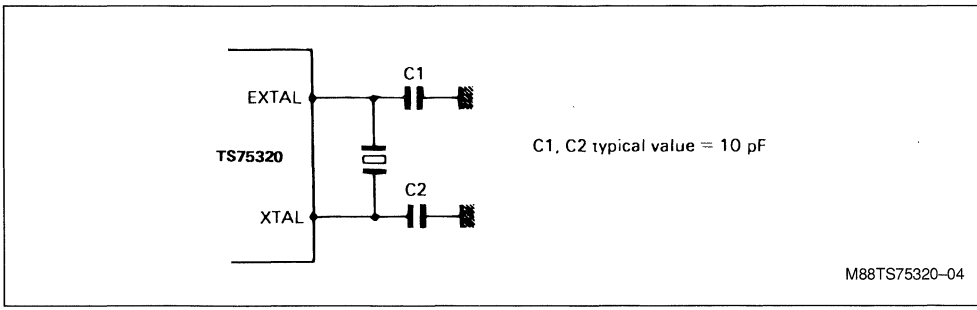


Note 1 : t_c = Instruction cycle time = 4 t_{cex}.

INTERNAL CLOCK OPTION

A crystal oscillator can be connected across XTAL and EXTAL. The frequency of CLKOUT : tc/2 is half the crystal fundamental frequency.

Figure 4.

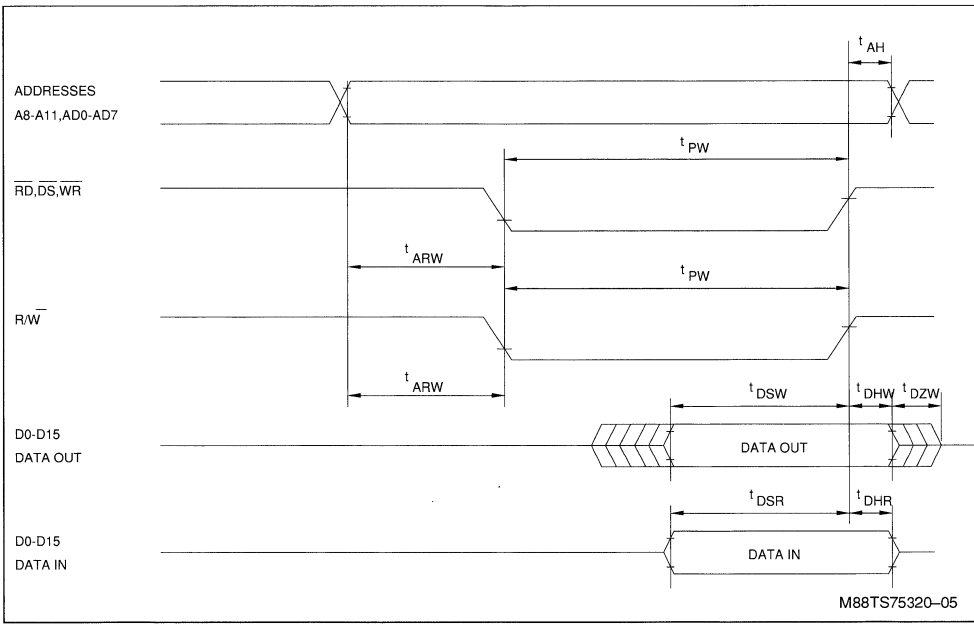


ELECTRICAL CHARACTERISTICS - LOCAL BUS TIMING

(V_{CC} = 5.0 V ± 5 %, T_{amb} = 0 °C to + 70 °C ; see figure 5)

Symbol	Parameter	Min.	Max.	Unit
t_{PW}	$\overline{RD}$, $\overline{WR}$, $\overline{SDS}$, Pulse Width	1/5 tc – 15	1/2 tc	ns
t_{AH}	Address Hold Time	10	–	ns
t_{DSW}	Data Set-up Time, Write Cycle	25	–	ns
t_{DHW}	Data Hold Time, Write Cycle	10	–	ns
t_{DZW}	$\overline{SDS}$ High to Data High Impedance, Write Cycle	–	40	ns
t_{DSR}	Data Set-up Time, Read Cycle	20	–	ns
t_{DHR}	Data Hold Time, Read Cycle	5	–	ns
t_{ARW}	Address Valid to $\overline{WR}$, $\overline{SDS}$, $\overline{RD}$ Low	1/2 tc – 40	–	ns

Figure 5 : Local Bus Timing Diagram.



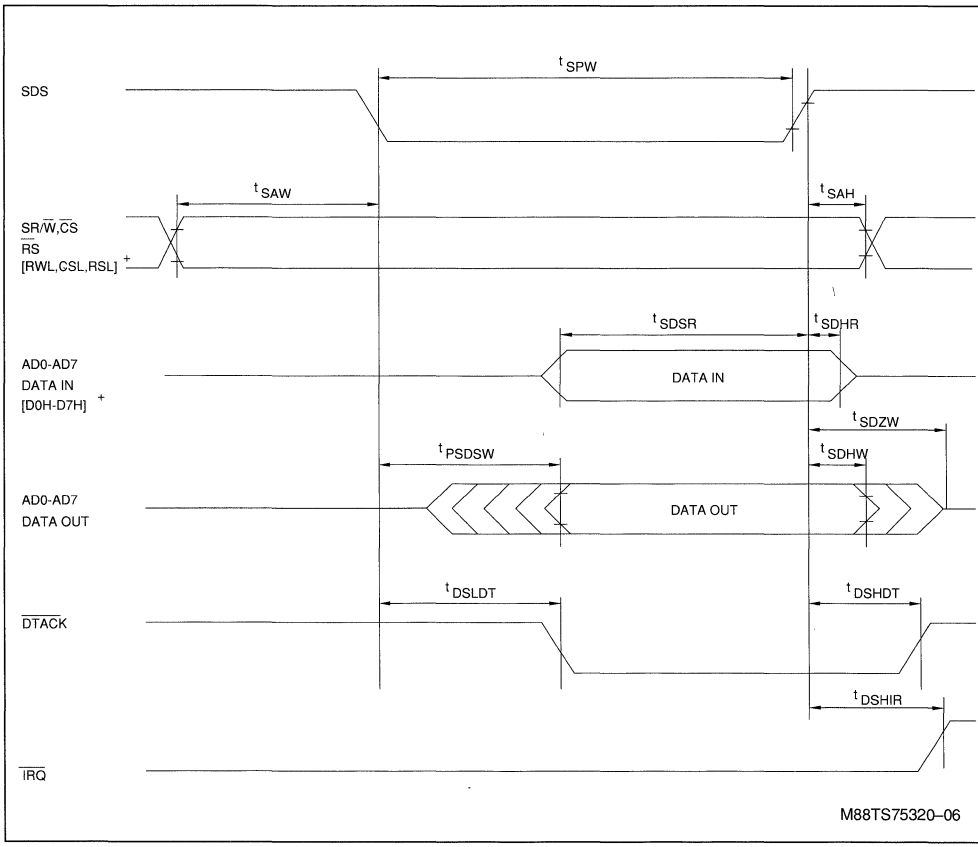
AC ELECTRICAL SPECIFICATIONS. SYSTEM BUS TIMING

(V_{CC} = 5.0 V ± 5 %, T_{amb} = 0 °C to + 70 °C ; see figure 6)

Symbol	Parameter	Min.	Max.	Unit
t_{SPW}	$\overline{SDS}$ Pulse Width	60	–	ns
t_{SAW}	SR/$\overline{W}$, $\overline{CS}$, $\overline{RS}$ Set-up Time	20	–	ns
t_{SAH}	SR/$\overline{W}$, $\overline{CS}$, $\overline{RS}$ Hold after $\overline{SDS}$ High	5	–	ns
t_{SDSR}	Data Set-up Time, Read Cycle	20	–	ns
t_{SDHR}	Data Hold Time, Read Cycle	5	–	ns
t_{SDSW}	Data Set-up Time, Write Cycle	–	35	ns
t_{SDHW}	Data Hold Time, Write Cycle	10	50	ns
t_{DSLDT}	$\overline{SDS}$ Low to $\overline{DTACK}$ Low	–	50	ns
t_{DSHDT}	$\overline{SDS}$ High to $\overline{DTACK}$ High *	–	50	ns
t_{DSHIR}	$\overline{SDS}$ High to $\overline{IRQ}$ High	–	50	ns
t_{SDZW}	$\overline{SDS}$ High to Data High Impedance, Write Cycle	–	40	ns

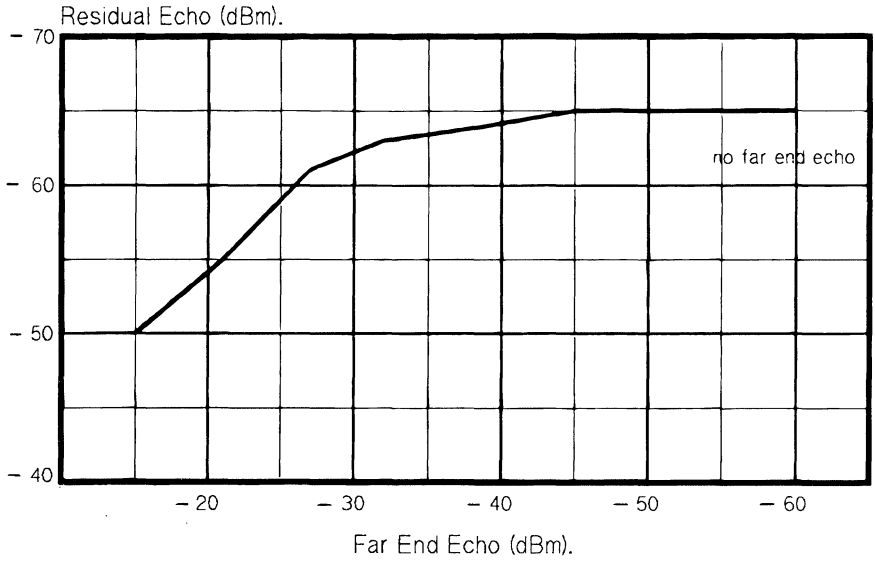
* $\overline{DTACK}$ is an open drain output test load include R_L = 890Ω at V_{CC}.

Figure 6 : System Bus Timing Diagram.



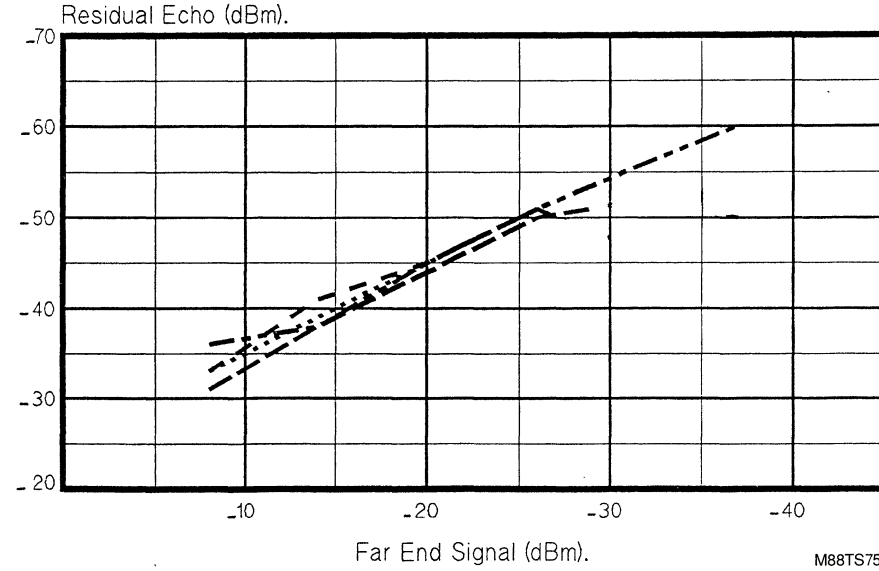
TYPICAL PERFORMANCE

TS75320 : Residual Echo without Far-end Signal.



M88TS75320-07

TS75320 : Residual Echo versus Far End Signal (with far-end echo level 8dB below far-end signal).



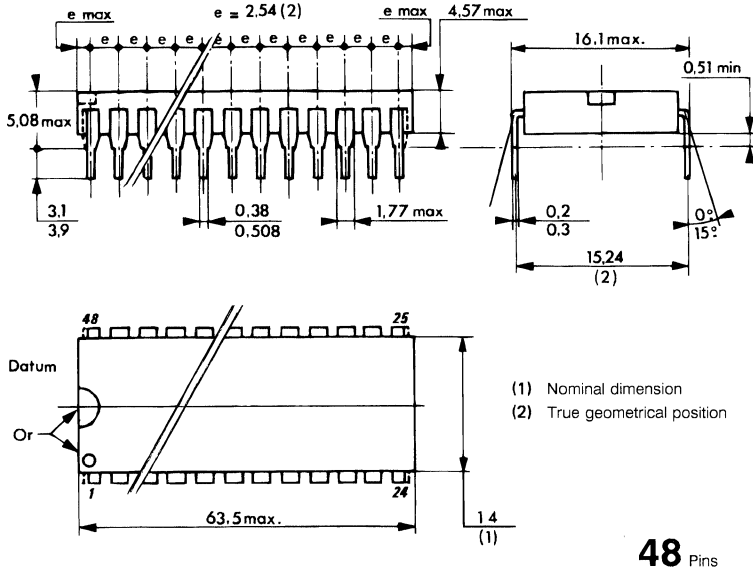
M88TS75320-08

ORDERING INFORMATION

Part Number	Temperature RAnge	Package
TS75320CP	0 °C to + 70 °C	48 Pin Plastic Dil

PACKAGE MECHANICAL DATA

48 PINS – PLASTIC DIP



MODEM APPLICATION SUPPORT

SGS-THOMSON MICROELECTRONICS

EFRMAFE

TS68950/51/52 MODEM ANALOG FRONT END EVALUATION BOARD

- EVALUATION BOARD FOR TS68950/51/52 MAFE.
  - 34 TEST POINTS AVAILABLE
- EASY TO USE FOR HIGH SPEED MODEM DEVELOPMENT UP TO 19200 BPS
  - THREE USER MODES AVAILABLE
  - DIRECTLY CONNECTABLE TO THE SGS THOMSON MICROELECTRONICS DSP HARDWARE TOOLS WITH A 84-PGA EMULATION PROBE
  - DIRECTLY CONNECTABLE TO AN EXTERNAL PROCESSOR THROUGH A 50-PIN CONNECTOR
- MASTER CLOCK (5.76MHz) PROVIDED BY AN ON-BOARD CRYSTAL WHICH CAN BE REPLACED BY AN EXTERNAL CLOCK.
- MODEM LINE INTERFACE OR GENERAL PURPOSE WIRE WRAPPING AREA AVAILABLE

DESCRIPTION

The EFRMAFE is a modem analog front end board equipped with the TS68950/51/52 MAFE chip set (ADC, DAC, filters, AGC amplifier, clock generator) and the phone line interface circuitry.

It offers a very simple and straightforward means of interfacing the SGS THOMSON DSP to analog signals. It is especially well suited for development and debugging of modem applications designed to meet CCITT V.22, V.26, V.27, V.29, V.32, and V.33 recommendations as well as the Bell 212A, 208 and 209 standards. The EFRMAFE can be linked to the SGS THOMSON DSP tools. Along with the software library, it provides a ready to use digital signal processing system interface well adapted to the analog world.

FUNCTIONAL DESCRIPTION

In normal mode the EFRMAFE is a real modem analog front end.

The simple analog loop mode loops the transmitted signal output on the received signal input after an attenuation of the transmitted signal. It permits auto test of the local reception.

The double analog loop mode loops the transmitted signal output on both the received signal input and the analog gain amplifier 2 input. It allows the test of the reception while the modem receive analog interface eliminates the transmitted signal by filtering (split band modem) or echo cancelling (modem with echo canceller).

MASTER CLOCK

The on-board Q1 (5.76MHz) is needed by the TS68952 to generate the different clocks by frequency division. It can be replaced by an external clock.

POWER REQUIREMENTS

+ 5V ± 5% (0.5A). Additional ± 12V is required only if the operational amplifier (IC6) is included in the transmission chain between the TS68950 and the TS68951 devices.

ORDER CODES

EFRMAFE

Note : The EFRMAFE board is delivered with the following documentation :

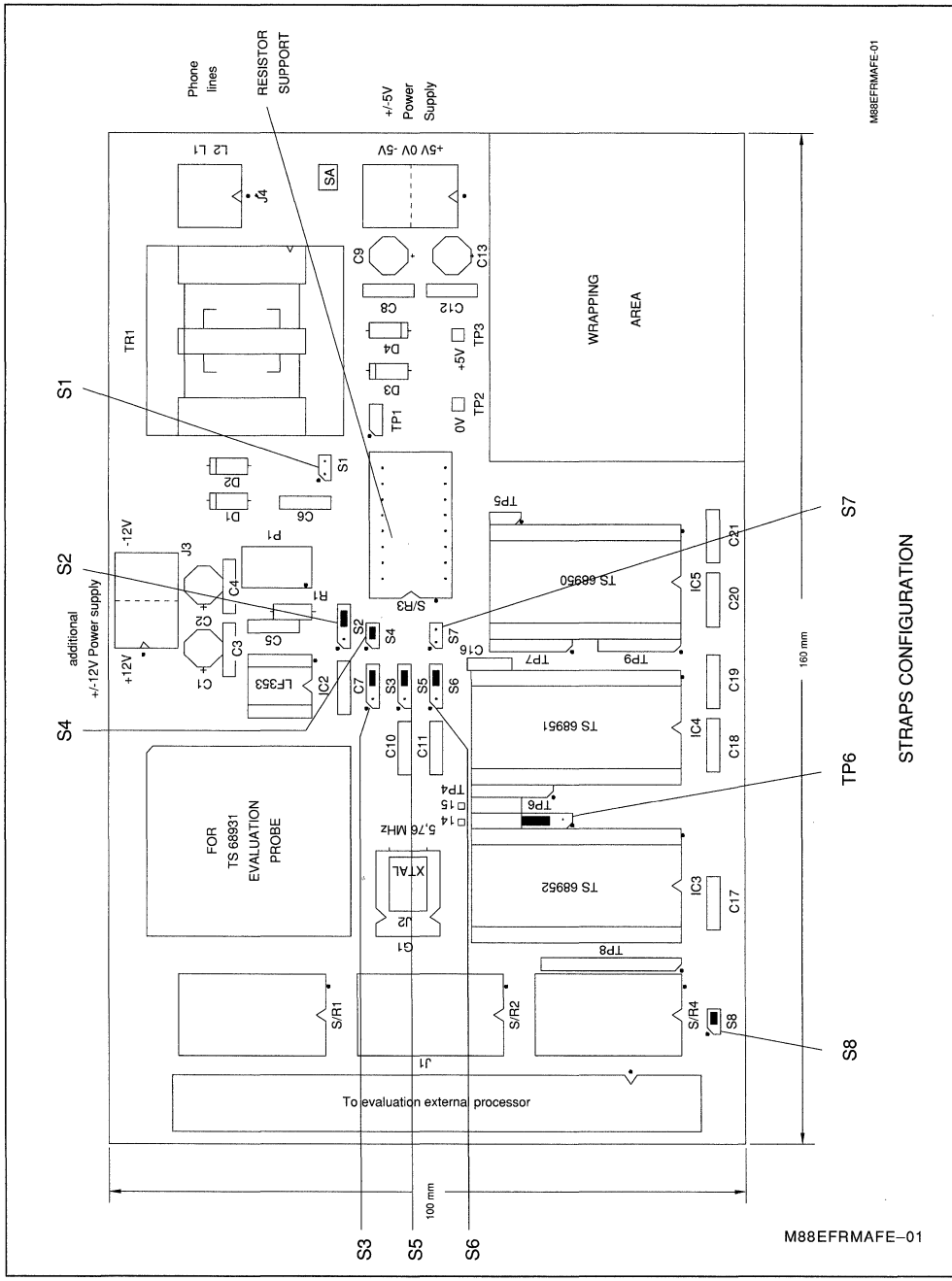
– TS68950/51/52 Data Sheet

– EFRMAFE user's manual

– Application note AN076 (development of Real Time Algorithm using the TS68930/31 DSP and the MAFE)

– Characterization report (MAFE)

LAYOUT AND STRAPS ACCESS



TEST POINTS

34 test–points are available on the board. According to the layout, they have been divided in 9 groups :

DESIGNATION	TESTED POINTS	COMMENTS
TP1	2 Test-points : 1 : V– . TS68951 2 : EEI	
TP2	1 Test-point : 1 : V+ TS68952	
TP3	1 Test-point : 1 : DGND TS68951	
TP4	6 Test-point : 1 : V+ 2 : AGC2 3 : CD1 TS68951 4 : LEI 5 : RAI 6 : AGND	Analog Part of the TS68951
TP5	2 Test-points : 1 : DGND TS68950 2 : V–	
TP6	3 Test-points : 1 : TO 2 : TxSCLK TS68952 3 : DGND	
TP7	5 Test-points : 1 : V+ 2 : EEO 3 : ATO TS68950 4 : EXI 5 : AGND	Analog Part of the TS68950
TP8	9 Test-points : 1 : D5 2 : D6 Data 3 : $\overline{D7}$ 4 : $\overline{E}$ _ 5 : $\overline{R/W}$ 6 : $\overline{CSO}$ Control 7 : CS1 8 : $\overline{RSO}$ 9 : RS1	
TP9	5 Test-points : 1 : D4 2 : D3 3 : D2 Data 4 : D1 5 : D0	

N.B. These test–points have been chosen to observe the supply voltages at the terminals of each MAFE circuit, control and data buses, and analog inputs/outputs.

POWER SUPPLIES

The board requires the following power supplies :

+ 5V 0V – 5V	J5 connector	+ 12V 0V – 12V	J3 connector

N.B. The ± 12V supplies are required only if the IC6 operational amplifier is included in the transmission chain between the TS68950 and the TS68951 circuits. The grounds of the + 5V and + 12V are separated. If using IC6, connect them together.

SGS-THOMSON MICROELECTRONICS

TS7514EVA

TS7514 EVALUATION BOARD

- V.23 STANDARD OPERATION
- SELECTABLE 75/1200 OR 1200/75 bps (half duplex on 2 wire)
- DTMF DIALLING CAPABILITY
- ANALOG TEST LOOP CAPABILITY
- TONE RING GENERATION AND DETECTION
- TWO PROGRAMMING WAYS :
  MANUAL (switches)
  AUTOMATIC (V.24/RS232 junction)
- ALL PROGRAMMABLE FUNCTIONS :
  - TRANSMIT/RECEIVE LEVELS
  - RECEIVE FILTER GAIN
  - HYSTERESIS AND DETECTION LEVELS
  - LINE MONITORING LEVEL
  - SIGNALLING FREQUENCY (2982Hz)

DESCRIPTION

The TS7514EVA is an evaluation board which allows a very convenient evaluation of the single chip modem TS7514 (V.23 operation).

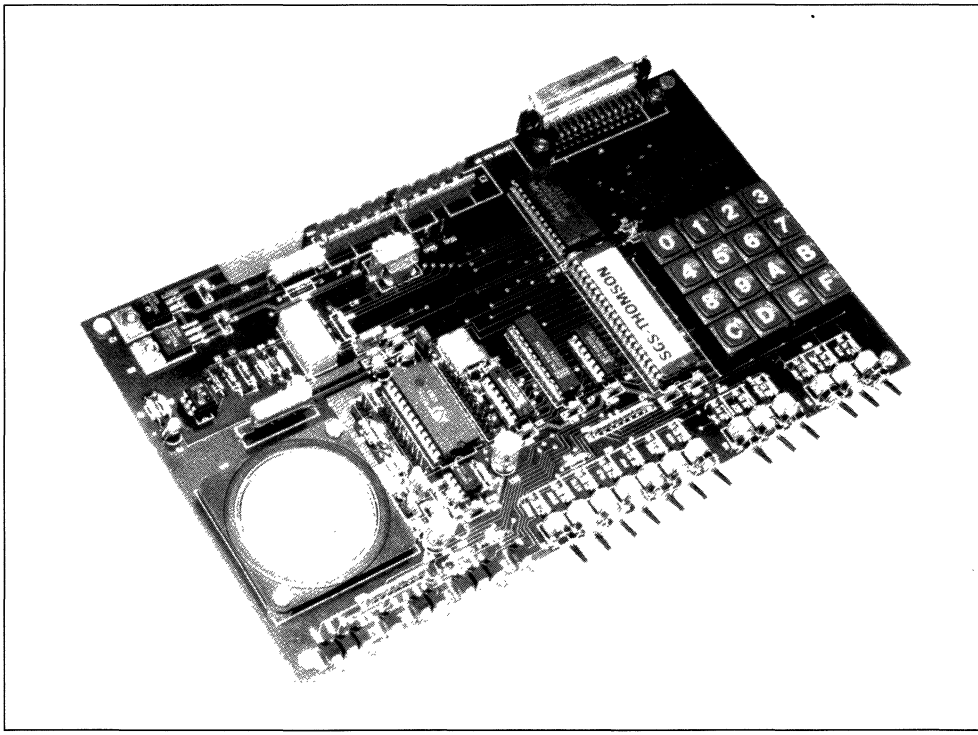
The TS7514EVA performs 2-wire 1200/75 bps half duplex modem operation in accordance with V.23 CCITT requirements.

The board is controlled by a microcontroller.

A loudspeaker is provided to monitor the line during the call/handshake procedure.

It provides a direct interface to a V.24 junction through a 25-pin female connector and a direct interface to the telephone line.

TS7514EVA EVALUATION BOARD



SGS-THOMSON MICROELECTRONICS

TS7515EVA

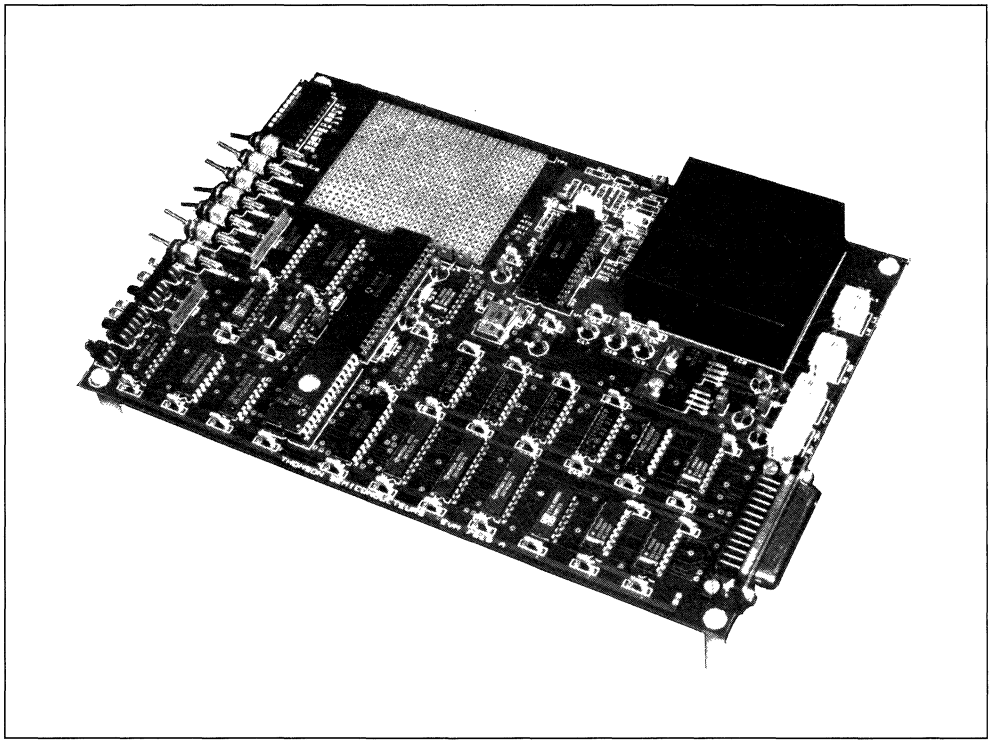
TS7515 EVALUATION BOARD

- V.22A/B AND BELL 212/BELL 103 STANDARDS OPERATION
- SYNCHRONOUS/ASYNCHRONOUS MODE SELECTION
- CHARACTER LENGTH SELECTION IN ASYNCHRONOUS MODE
- GUARD TONE SELECTION/ENABLE
- SCRAMBLER SELECTION/ENABLE
- ANSWER TONE SELECTION/ENABLE
- ANSWER/ORIGINATE MODE SELECTION
- TRANSMIT/RECEIVE ADJUSTABLE LEVELS
- BINARY RATE SELECTION
- LOOP 2/ LOOP 3/ REMOTE DIGITAL LOOP SELECTION
- COMPLETE V.24/RS232C AND TELEPHONE LINE INTERFACE

DESCRIPTION

The TS7515EVA is an evaluation board which allows a very convenient evaluation of the single chip modem TS7515 (V.22, Bell212 and Bell103 operations).

The TS7515EVA performs 2-wire 1200 bps full duplex modem operation in accordance with V.22 A/B CCITT requirements.



V.22 BIS EVALUATION BOARD

- CCITT V.22BIS EVALUATION MODEM
- CCITT V.21, V.22, V.23 EVALUATION MODEM
- BELL 103 AND 212 EVALUATION MODEM
- FAST EVALUATION OF TS7524 CHIP SET
- CALL MODE INCLUDING AUTOMATIC DIALING THROUGH PSTN (DTMF AND PULSE MODES)
- AUTOMATIC ANSWER MODE
- DIGITAL AND ANALOG LOOPBACK MODES
- DATA TRANSFER MODE FROM 2400BPS TO 75BPS
- CALL PROGRESS TONE AND ANSWER TONE MONITORING
- ASYNCHRONOUS OR SYNCHRONOUS SERIAL LINE FOR TERMINAL OR HOST COMPUTER
- PHONE LINE INTERFACE FOR IMMEDIATE CONNECTION ON PSTN OR PBX
- HAYES COMMANDS COMPATIBLE

DESCRIPTION

The TS7524EVA is a V.22BIS evaluation board which directly supports the TS7524 chip set. It can operate up to 2400bps in full duplex over Public Switched Telephone Network. It also allows evaluation of V.21, V.22, V.23 and Bell 103, 212 recommendations.

The TS7524EVA furnishes many of the capabilities of a multi-mode stand-alone modem to provide a fast evaluation and performance demonstration of the TS7524 chip set such as calling another modem, answering, performing necessary handshaking operations, as well as passing data.

A terminal or host computer must be connected to the board allowing the user to see the messages printed on the screen or to enter and receive data from a far end modem. The TS7524EVA operates under Hayes 'AT' commands.

The TS7524EVA can also be connected to a modem test station for performance measurements.

A loudspeaker and associated circuitry enables the possibility to monitor the call progress tone, the answer tone and the handshaking during a connection with a far-end modem.

ORDER CODE

TS7524EVA

SGS-THOMSON MICROELECTRONICS

TS7532DEMO

V.32 DEMO BOARD

- FAST EVALUATION OF TS7532 CHIP SET
- COMPLEMENTARY TOOL FOR TS7532 DPUMP
- PROVIDES MANY FEATURES OF A CCITT V.32 STAND-ALONE MODEM
- HANDSHAKE AND RETRAIN SEQUENCE
- CALL MODE INCLUDING AUTOMATIC DIALING THROUGH PSTN
- ANSWER MODE
- DATA TRANSFER MODE AT 9600BPS WITH OR WITHOUT TREILLIS CODING MODULATION, OR 4800BPS
- CONSTELLATION VIEWING
- CALL PROGRESS TONE AND ANSWER TONE MONITORING
- SYNCHRONOUS SERIAL LINE FOR OPTIONAL TERMINAL OR HOST COMPUTER
- PHONE LINE INTERFACE FOR IMMEDIATE CONNECTION ON PSTN OR PBX

DESCRIPTION

The TS7532DEMO is a V.32 demonstration board which directly supports the TS7532DPUMP (V.32 data pump). It is the ideal complementary tool for the V.32 data pump. The TS7532DEMO furnishes many of the capabilities of a V.32 stand-alone modem to provide a fast evaluation and performance demonstration of the TS7532 chip set such as calling another modem, answering, performing necessary handshaking and retraining operations, as well as passing data. An optional terminal or personnal computer may be connected to the board through a synchronous serial line, allowing the user to see the messages printed on the screen or to enter and receive data from a far end modem.

The TS7532DEMO can also be connected to a modem test station for performance measurements.

The TS7532DEMO also includes the ability to watch the constellation on an X-Y oscilloscope screen.

The TS7532DEMO has switches to select the right number to dial through the Public Switched Telephone Network, and establish a connection in the call mode.

A loudspeaker and associated circuitry provides the possibility to monitor the call progress tone, the answer tone and the handshaking during a connection with a far-end modem.

ORDER CODE

TS7532DEMO

SGS-THOMSON MICROELECTRONICS

TS7532DPUMP

V.32 DATA PUMP

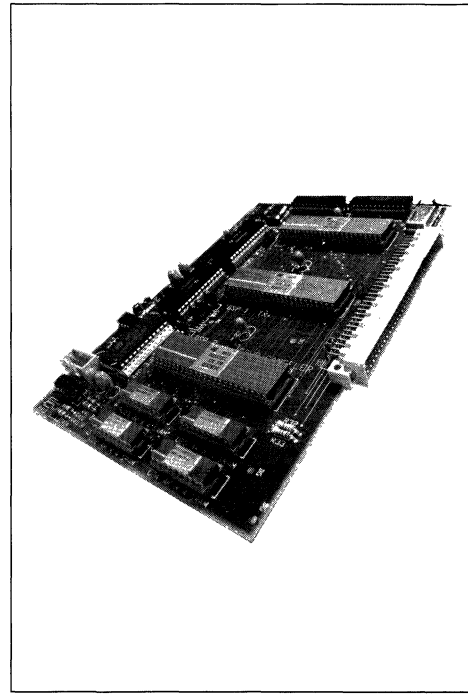
- CCITT V.32 COMPATIBLE MODEM DATA PUMP BOARD
- FULL DUPLEX OPERATION AT 9600BPS AND 4800BPS
- FULL IMPLEMENTATION OF CCITT V.32 HANDSHAKE
- SIMPLIFY V.32 PRODUCT DEVELOPMENT
- CANCELLATION OF BOTH NEAR AND FAR-END ECHOES WITH UP TO 10HZ OF FREQUENCY OFFSET FOR FAR-END ECHO
- TWO SATELLITE HOPS
- TREILLIS ENCODING AND VITERBI DECODING
- 12.5% ROLL-OFF RAISED COSINE TRANSMIT PULSE SHAPPING
- HIGH PERFORMANCE PASSBAND FRACTIONALLY SPACED ADAPTIVE EQUALIZER
- SIGNAL QUALITY MONITORING
- DTMF GENERATION
- CALL PROGRESS TONE DETECTION
- PARALLEL INTERFACE TO STANDARD MICROPROCESSORS
- SINGLE BOARD WITH TWO INTERFACE CONNECTORS FOR ANALOG AND DIGITAL SIGNALS TO DAA AND HOST MICROCONTROLLER
- IMPLEMENTATION WITH THREE DSPS, THREE MAFE CHIPS AND STATIC MEMORY

DESCRIPTION

The TS7532DPUMP is a V.32 modem data pump board. It comes with preprogrammed Digital Signal Processors for immediate evaluation or performance demonstration of the TS7532 chip set. The TS7532DPUMP contains three DSPs (TS75320, TS75321 and TS75322), three Modem Analog Front End chips (TS68950, TS68951 and TS68952), four 4k x 4 of static RAM for far-end echo canceller and two 2k x 8 of static RAM for the Viterbi decoder.

The TS7532DPUMP has two I/O connectors. The first one is used for all digital and control lines. The second connector is used for the analog signals to and from the Data Access Arrangement of the telephone interface.

Figure 1 : TS7532DPUMP.



The TS7532DPUMP could be directly connected to a user controller board through an 8-bit parallel interface or can be used with the TS7532DEMO which contains DAA, microcontroller, dial switches, and D/A converters for constellation monitoring.

The TS7532DPUMP greatly reduces and simplifies V.32 product development.

Moreover, by buying a V.32 software license, modification or extension of the V.32 modem product can be done with the TS7532DPUMP using the company's DSP development tools.

ORDER CODE

TS7532DPUMP

TS7542 MODEM ANALOG FRONT END EVALUATION BOARD

- EVALUATION BOARD FOR TS7542 AND TS68950/51/52 MAFE
- PERFORM THE EVALUATION OF MODEM USING THE FOLLOWING STANDARDS (both with TS7542 or TS68950/51/52) :
  - CCITT V.21, V.22, V.22bis, V.23, V.26, V.27, V.29
  - BELL 103, 208, 209, AND 212A
  - CCITT V.32 WITH TS68950/51/52
- 48- PIN DIL SOCKET COMPATIBLE WITH SGS-THOMSON MICROELECTRONICS DSP TOOLS (emulator and/or hardware development system) OR WITH SGS-THOMSON DSP EPROM MODULES (TS68930EPR - ST18930EPR)
- MASTER CLOCK (5.76MHz) PROVIDED BY AN ON-BOARD CRYSTAL OR BY THE DSP CLOCK OUTPUT
- EXTERNAL 2k x 16 BIT DSP MEMORY
- 2 WIRE-WRAPPING AREAS :
  - ONE FOR USER'S LINE INTERFACE
  - ONE FOR CONNECTION OF A MICRO-COMPUTER
- +/- 5V ± 5% POWER SUPPLY

DESCRIPTION

The TS7542EVA is a Modem Analog Front End Evaluation Board equipped with the monochip MAFE TS 7542 or with the chipset MAFE TS68950/51/52.

It offers a very simple and straightforward means of interfacing DSP to analog signals.

It is especially well suited for development and debugging of modem applications designed to meet CCITT and Bell recommendations.

The TS7542EVA can be managed under the control of the TS68930 or ST18930 DSP.

It can be linked to the SGS-THOMSON DSP tools and provide a ready-to-use digital processing system well adapted to the analog world.

The TS7542EVA can be used in stand-alone Modem Evaluation Board when under control of a SGS-THOMSON DSP Eprom module, or under control of a SGS-THOMSON Programmed DSP (V.22bis applications).

ORDER CODE

TS7542EVA

USING THE TS75320 ECHO CANCELLER IN V.32 MODEMS

By F.B. Druilhe, W.D. Glass, R. Radzyner

INTRODUCTION

The SGS-THOMSON Microelectronics TS75320 is a high performance voiceband echo canceller implemented with one SGS-THOMSON TS68930 single-chip VLSI digital signal processor. The TS75320 is intended in the first instance for applications with CCITT V.32 modems for bi-directional full duplex data transmission at rates up to 9.6 kb/s on switched telephone network two-wire circuits.

With the echo cancellation approach the whole bandwidth of the line is available for transmission in both directions simultaneously ; i.e. it is not necessary to split the band (e.g. as is done for V.22bis modems) or to time-share between terminals using burst transmissions. With echo cancellation the effective channel capacity is doubled in comparison with conventional alternatives.

The task of the echo canceller is to ensure the signal presented to the modem receiver is free of components emanating from its own transmitter.

The TS75320 is implemented as a passband echo canceller, i.e. for operation directly with the modulated (line) signal. With this method the echo canceller uses the cancellation error as it appears at the receiver input. Hence, the only interaction needed with the host modem is the transfer of the V.32 format rotated data symbols and initialization data during the call set-up procedure.

By virtue of its highly flexible asynchronous parallel input/output port with its associated mailbox protocol, interfacing the TS75320 to a host processor is very straightforward. Virtually no external interface circuitry is required where the modem is implemented with SGS-THOMSON TS68930 digital signal processors. The TS75320 requires 4 K x 16-bit of external RAM, used mostly as a delay line (see Section 2.2).

Moreover, the use of the SGS-THOMSON TS68950/951/952 digitally programmable modem analog front end (MAFE) chip set is particularly well suited to this approach (Fig. 2.7). The SGS-THOMSON MAFE provides all the necessary analog interface circuitry for voiceband modem applications, including dedicated circuitry for the subtraction of the estimated echo. The MAFE is especially convenient as it incorporates all the required programmable gain control and clock circuitry, and interface filters (bandlimiting, anti-aliasing and smoothing filters, realized with switched-capacitor technology and tunable according to sampling rate requirements).

The TS75320 meets or exceeds all the requirements of CCITT Recommendation V.32. It is designed for operation in circuits with up to two satellite hops of far-end echo delay (1.14 seconds), and up to 10 Hz of frequency offset in the far-end echo path.

The TS75320 is a key component in the advanced SGS-THOMSON TS7532 V.32 modem.

This application guide introduces the TS75320 digital echo canceller in the context of V.32 modem applications (Sections 1.2 - 1.3), and provides the details of the operation of the interface circuitry and of the procedures for the input and output of data (Section 2). Results of performance measurements are given in Section 3.

CONTENTS

LIST OF FIGURES

1. GENERAL CONSIDERATION

1.1. ECHO CANCELLATION IN VOICEBAND MODEMS

The basic components making up a typical dialled modem connection are shown in Fig. 1.1. The functional blocks labelled "H" represent the "hybrid" transformer (Fig. 1.2) normally found at the junction of conventional two-wire and four-wire telephone circuits. The hybrid transformer realizes a rudimentary echo cancellation function that provides a minimal degree of separation between the two directions of transmission. The separation ratio is normally not better than 20 dB, and, though adequate generally for analog voice purposes, this is well short of the performance needed for data transmission.

The essentials of the data modem echo cancellation system are shown in Fig. 1.3. The task of the echo canceller "EC" is to provide an emulation of the characteristics of the echo path, including level changes (gain/attenuation), delays, frequency shifts, distortion processes, such that a high degree of echo suppression results when the estimated echo ê is subtracted from the incoming echo. The overall echo cancellation system consists of a channel emulator and of an adaptive procedure (algorithm) for the determination of optimum emulator parameters (coefficients). The echo canceller may be considered as an adaptive filter whose transfer function models that of the echo path.

For the purposes of echo cancellation in telephone networks it is necessary to distinguish between

- *the near-end echo, due to feedthrough in the local hybrid transformer,*

and,

- *the far-end echo, due to feedthrough and reflections at the remote terminal.*

This is shown in Fig. 1.1.

The far-end echo is generated in the hybrid at the junction of the far end two-wire local loop with the four-wire circuit, and will appear at the receiver input after some delay, corresponding to the round trip to and from the remote hybrid. Since this path may include satellite links, the delay may be large in comparison to the duration of the impulse response of the system. Provision has been made for a far-end echo delay of up to 1.14 second, corresponding to the delay incurred with two satellite links. CCITT recommendation V.32 includes a provision for measuring this delay during the modem handshake procedure.

Owing to the large delays possible between the near-end and far-end echo contributions it is necessary to use a separate echo estimation process for each, as shown in Fig. 1.4. The requirements of the near-end and far-end cancellers differ significantly. As discussed in Section 1.3, below, the echo suppression performance requirement for the near-end canceller is considerably greater than for far-end canceller. However, the far-end canceller must be capable of functioning in the presence of nontrivial frequency offset.

Both near-end and far-end echo cancellers in the TS75320 accomodate up to 16 ms of echo path impulse response.

1.2. ECHO CANCELLATION PERFORMANCE REQUIREMENTS

For a V.32 receiver operating in additive white gaussian noise, the minimum signal-to-noise ratio for a bit error rate of 10^{-5} is 18 dB, on a mean power basis [Ref. 2, Fig. 5.58, p. 186]. Supposing channel noise and residual echo contributions of similar magnitudes, the minimum signal-to-residual-echo ratio requirement is 21 dB. Again, with approximately equal near-end and far-end residual echo contributions the minimum signal-to-residual-echo ratio is 24 dB for each of these contributions.

The near-end echo level is typically 10 to 20 dB below that of the transmitted signal. The level of the received signal may occasionally fall as low as 30 to 40 dB below that of the transmitted signal. Hence, under certain line conditions, the near-end echo level could be 30 dB above that of the received signal. To obtain a signal-to-residual-echo ratio better than 24 dB at the receiver input, near-end echo suppression better than around 54 to 55 dB is necessary. This is a stringent performance requirement met by the TS75320.

The far-end echo is subject to attenuation twice in the local loop and in the network, and is also attenuated in the far-end hybrid. Hence, its level is normally several decibels below that of the received signal, about 10 dB typically ; the worst-case figure for system design purposes is 8 dB. To obtain a minimum signal to residual echo ratio of 24 dB for the far-end echo contribution it follows the suppression ratio for the far-end echo canceller must be around 14 dB under typical operating conditions and not below 16 dB under adverse conditions.

While this is considerably less than the requirement for the near-end echo canceller, it is important to note that the far-end echo canceller must be capable of maintaining this level of performance in the presence of nontrivial frequency offsets. The current version of the TS75320 meets this requirement in the presence of frequency offsets of 10 Hz* in the far-end echo.

Convergence requirements are 1.5 second for the near-end echo algorithm, and 6.9 seconds for the near-end and far-end echo algorithms combined.

The results of TS75320 performance measurements are documented in Section 3.

2. INTERFACING THE TS75320 TO A MODEM

2.1. INTRODUCTION

The purpose of this section is to provide in detail the essential information required for the trouble-free operation of the TS75320. This includes pin by pin and bit by bit descriptions of hardware connections, signal format and timing requirements, and data exchange protocols.

The TS75320 echo canceller is implemented with the SGS-THOMSON TS68930 monolithic digital signal processor (Ref. 4). In this application guide no previous experience with the TS68930 is assumed. All the essential details for the embedding of the TS75320 in a CCITT V.32 modem environment will be found herein ; reference to TS68930 documentation should not be required under normal circumstances.

The description is divided into three parts :

(a) Interface circuitry

the detailed description of the data, address and control buses available for the connection of the echo canceller to a host or to other processors (Sections 2.2 - 2.4).

(b) Data exchange protocols

the mechanics of the operation and sequencing of the control signals for the management of data transfers to and from the TS75320 (Section 2.5).

(c) Organization and formatting of data

the definition of the input and output data signals, and of the initialization timing and formatting requirements (Sections 2.6 - 2.7).

2.2. INTERFACE CIRCUITRY OVERVIEW

Two buses are used for the exchange of data with the TS75320 :

- The **local bus** (16 data lines D0-D15), which is a transparent extension of the internal bus structure
- The **system bus** (8 data lines AD0-AD7) which provides an asynchronous data transfer mechanism by means of a mailbox protocol.

These buses are not independent : the eight lines AD0-AD7 which constitute the data lines of the system bus also serve as address lines on the local bus.

The TS75320 uses the local bus to access the 4 K x 16-bit of external RAM needed for the symbol bulk delay and other data workspace requirements. The system bus is used for communication with the host processor.

A schematic representation of the interface circuitry is shown in Fig. 2.1.

2.3. DATA EXCHANGE INTERFACE WITH HOST PROCESSOR (System Bus)

Data exchanges between the TS75320 and the host system take place by means of a "mailbox" within the TS75320, accessible externally through the system bus. These data transfers are asynchronous, i.e. their timing in independent of the TS75320 clock.

The mailbox consists of two shift registers, the "R-IN" register for data input, and the "R-OUT" register for data output ; each of these is 3-byte wide. The system bus has eight data lines AD0-AD7. Hence, to effect a complete 24-bit data exchange via the system bus, three sequential 8-bit transfers are required.

The system bus consists of three basic sections :

- **the data bus :**
  AD0-AD7 (bidirectional, 8-bit wide)
  (these lines are also used as address lines on the local bus)
- **the address bus :**
  $\overline{CS}$ chip select (input)
  RS register select (input)
- **the control bus :**
  SR/$\overline{W}$ system read/write (input)
  $\overline{SDS}$ system data strobe (input)
  $\overline{IRQ}$ interrupt request (output)
  $\overline{DTACK}$ data transfer acknowledge (output)
  BA bus available (output)

The operation of these buses (data transfer protocol) is described in detail in Section 2.5.

An important aspect of system bus operation is that processing within the TS75320 halts when control of the bus is released to the host. (This occurs because the local bus is disabled owing to the unavailability of lines AD0-AD7, needed to address the external RAM). Hence careful attention must be paid to the management of the system bus by the host processor. The total occupation time of the system bus by the host must be less than 10 µs during any mailbox access as described in Fig. 2.12.

Prior to the release of the system bus to the host and the initiation of the echo canceller HALT state, the current program instruction will be completed. In the HALT state

- the program counter is not incremented

- no address is generated on the system bus
- on the local bus, D0-D15 and A8-A11 are switched to the high impedance state.

The description of the organization, sequencing and formatting of the data exchanges is given in Sections 2.6 and 2.7.

2.4. DATA EXCHANGE INTERFACE WITH EXTERNAL RAM (Local Bus)

Data exchanges between the TS75320 and its external RAM take place via the *local bus* (Figs. 2.1, 2.2). This bus operates as a direct extension of the internal 16-bit bus structure. As such, it is under the total (synchronous) control of the TS75320.

The local bus consists of three basic sections :

- **the data bus :**
  16 lines : D0-D15
- **the address bus :**
  12 lines :
  four dedicated : A8-A11
  eight shared with system bus : AD0-AD7
- **the control bus :**
  2 lines : (Motorola protocol)
  $\overline{R/W}$: write strobe signal
  $\overline{DS}$: read strobe signal

The eight address lines AD0-AD7 also serve as the data lines of the system bus. These may be isolated from the host side of the system bus by means of a bus transceiver (such as a 74F245) using the system bus control line $\overline{BA}$ (bus available) or its complement to provide the switching signal, as shown in Figs. 2.1 and 2.2 (refer to Section 2.5). As noted in the previous section, program execution within the TS75320 halts when control of the system bus is relinquished, i.e. when the lines AD0-AD7 are not available for local bus operation.

The timing diagrams and requirements for READ and WRITE operations on the local bus are displayed in Fig. 2.3. For normal full speed operation (25 MHz master clock), the maximum access time is 45 ns for data transfer from memory (READ cycle). The maximum access time for data transfer to memory is 35 ns (WRITE cycle).

The CLKOUT line provides access to a clock signal at half the crystal frequency, i.e. 80 ns cycle period. This is a useful timing reference when monitoring the operation of the interface circuitry. The period of a TS75320 unit operation is twice the period of the CLCKOUT signal, i.e. 160 ns.

2.5. MAILBOX AND SYSTEM BUS PROTOCOL

To best understand the mailbox data exchange mechanism it is important to recall the following considerations :

(a) External access to the mailbox (system bus) provides eight data lines, i.e. transfers must be effected in units of one byte.

(b) The mailbox consists of one input and one output shift register (R-IN and R-OUT, respectively), each able to store a string of three 8-bit words.

(c) The eight data lines on the system bus (AD0-AD7) are shared with the local bus.

(d) TS75320 processing ceases while lines (AD0-AD7) are not available for local bus operation (processor HALT state).

(e) Data transfers between the mailbox and the TS75320 internal buses cannot take place while the mailbox and the system bus are under external control.

On the basis of the foregoing, two key points emerge :

(a) One full transfer into the mailbox (R-IN register) and one full transfer out of the mailbox (R-OUT register) are possible per external mailbox access, i.e. three byte-wide WRITE operations, and three byte-wide READ operations.

(b) New data exchanges with the host cannot be effected until the host relinquishes control of the mailbox and of the system bus to allow reading and reloading within the TS75320.

Thus, it is evident that effective management of data transfers to and from the host will hinge on the timely hand-over of mailbox and system bus control between TS75320 and host. It is important to note that this control mechanism operates on the "possession" principle ; i.e. the processor in possession of the bus and mailbox retains control of data transfer until such time as it initiates its release*.

It follows the data input/output procedure may be described in terms of two distinct phases :

(a) Bus control transfer protocol :

A dialogue for the management of the successive transfers of control of the mailbox and bus between TS75320 and host.

(b) Data transfer protocol :

A dialogue for the management of the successive transfers of data bytes between mailbox and host in each control phase.

The system bus timing diagrams and associated tolerance specifications are given in Fig. 6, p. 10 in the TS75320 data sheet and in fig. 2.4.

System bus control transfer protocol

The description below refers to figures 2.1, 2.4 and 2.5.

To signal readiness for data exchanges with the host, the TS75320 transmits an interrupt request, IRQ\ = 0. To signal acceptance of the request the host responds (when ready) by sending CS\ = 0, RS\ = 0 ("address" signals), SR/W\ = 1, i.e. READ signal : it is important that a WRITE signal is **not sent** at this stage, as local bus operations using lines AD0-AD7 may still be in progress.

Following validation (SDS\ = 0 data strobe pulse), the TS75320 detects the host response (after 3-5 operation cycles) and completes the mailbox and system bus handover protocol by setting the bus available signal BA = 1, and resetting IRQ\ = 1.

The system bus and mailbox are now available to the host, and processing within the TS75320 has been halted.

*** REMARK :** The TS75320 is said to be *pseudo-slave.* It is not totally slave, in the sense that it remains independent of the host while it retains control of the system bus. When control of the system bus is handed over to the host, the TS75320 becomes a slave (in particular, processing halts). It should be noted that the converse is not true, i.e. when control of the system bus is with the TS75320, the host remains independent (albeit not master over the TS75320).

The TS75320 will have sent a data transfer acknowledge pulse, DTACK\ = 0 within 50 ns of receiving the data strobe SDS\ = 0.

The host may now proceed with one sequence of up to three byte-wide mailbox READ operations (R-OUT register) and/or one sequence of up to three byte-wide mailbox WRITE operations (R-IN register). The data read/write procedure is described in the next subsection "Data transfer protocol".

At the end of the data transfer operations, the host initiates the release of the mailbox and system bus with CS\ = 0, RS\ = 1, SR/W\ = 1.

These signals become effective with the transmission of the strobe pulse, SDS\ = 0, whereupon the TS75320 will initiate internal procedure for the resumption of processing. It will respond externally with a DTACK\ = 0 pulse within 50 ns of the leading edge of the SDS\ LOW pulse, and with the resetting of the bus available line (BA = 0) within 100 ns of the reset of the strobe pulse (SDS\ = 1). The TS75320 internal HALT state ceases one processing cycle (nominally 160 ns) after the resetting of the BA signal. The lines AD0-AD7 are not accessed for local bus operations until after that time.

As indicated in Section 2.4, the BA signal is useful to switch local bus isolation circuitry for the data lines AD0-AD7. The use of the DTACK\ signals is optional, subject to the requirements of the host processor.

Data transfer protocol

As in the foregoing subsection, the description below refers to Figures 2.1, 2.4 and 2.5.

The host is able to proceed with mailbox data transfer operations as soon as the handover of the system bus control is completed. This corresponds to the detection by the host of the reset of the interrupt request line, IRQ\ = 1.

A mailbox READ operation is carried out as follows :

When ready, the host sets CS\ = 0, RS\ = 0, SR/W\ = 1, and transmits the data strobe after a minimum set-up time of 5 ns (t_{SAW}). Data becomes available to the bus within 35 ns (t_{SDRS}) after the end of the data strobe (SDS\) leading edge, and remains held for t_{SDRS} ns after the completion of SDS\ reset ($10 < t_{SDRS} < 50$).

After the completion of each READ operation, the next byte is shifted into the interface buffer. As indicated earlier, up to three READ operations may be executed usefully in any exchange period. After that, new data will not be available in the buffer until the TS75320 has been given the opportunity to reload the R-OUT shift register.

The mailbox WRITE procedure follows the same pattern, with the main difference that the read/write signal SR/W\ is LOW :

The data must be valid for a minimum period t_{SDSW} = 20 ns before the completion of SDS\ reset, and held not less than t_{SDHW} = 5 ns after that reference time. After the completion of each write operation, the input byte is shifted to the next location in the TS75320 R-IN register to vacate the input for the next byte. As before, up to three WRITE operations may be effected usefully per exchange. Before further useful WRITE operations are effected, control of the mailbox must be released to the TS75320 so it can proceed with the retrieval of the new data in the R-IN register.

2.6. OPERATING PROCEDURE : OVERVIEW

The TS75320 is designed to provide an echo cancellation function for V.32 modems in the first instance. As such, a V.32 format rotated symbol is expected at the rate of 2400 Baud, and the incoming line signal is processed at the rate of 7200 samples per second, i.e. three samples per Baud interval.

The output of the echo canceller is an *estimated echo.* To cancel the unwanted echo, the echo estimate is subtracted from the incoming V.32 line signal.

This subtraction is external to the TS75320 and may be realized digitally (e.g. in one of the other processors of the modem), or in the analog domain as discussed below (see Fig. 2.6).

It is important to note that the polarity of the TS75320 estimated echo output value is such that the "subtraction" operation must be realized as a physical **addition**.

Implementation of the subtraction in the analog domain may be carried out with the SGS-THOMSON TS68950/951/952 modem analog front-end (MAFE) chip set (see Fig. 2.7). This approach is attractive since the SGS-THOMSON MAFE circuitry is designed with features aimed specifically for this class of applications, and incorporates a dedicated signal path for the estimated echo, with an in-built analogue adder for the "subtraction" operation.

The echo estimate samples are output via the mailbox R-OUT register at the rate of three per Baud interval, i.e. 7200 per second.

The TS75320 expects the input of an error signal (residual echo) and of a reference signal, i.e. the line output of the local transmitter.

The error signal is the difference between the V.32 incoming line signal and the estimated echo. As shown in Figs. 1.3, 1.4 and 2.6, this signal is the echo-free V.32 signal required at the modem receiver input. Under normal operating conditions both the far-end signal and the residual echo will be present. However, as part of the normal procedure for setting up a call between two modems it is necessary to provide an initialization period for the echo cancellers at each terminal. So, to allow rapid convergence of the adaptive algorithm, the far-end signal is not transmitted during this period, i.e. the modem receives only the echo of its own transmission while the initialization of the algorithm is in progress. It should be noted that the far-end signal is seen as noise by the echo canceller algorithm.

Error signal samples are required at the rate of 7200 per second. The rotated reference symbols are required at the Baud rate only (i.e. 2400 per second), since they remain unchanged over one Baud interval.

The convergence of the adaptive algorithm proceeds in two phases : first the near-end cancellation algorithm is brought into operation on its own. Convergence of this process is normally completed within around 500 ms ; a period of 3500 Baud intervals (i.e. 1.46 seconds) is provided for the completion of this phase.

After this time has elapsed, operation of the far-end cancellation algorithm is commenced (including frequency offset correction). The total time provided for the convergence of both near-end and far-end algorithms is 16656 Baud intervals, i.e. 6.9 seconds.

The TS75320 has been developped for compatibility with CCITT V.32 handshake protocol using a particular sequence for echo canceller adaptation before segment 1 consisting of 8192 bauds of scrambled 1's. The TS75320 then uses the segment 1 to estimate the frequency offset of the far-end echo. The sequence TRN consisting of scrambled 1's at 4800 bits/sec during 8192 bauds to terminate the far-end and near-end echo canceller convergence.

After the completion of the initialization processes at each end, full duplex data transmission may proceed. The algorithm continues to track and to adaptively adjust coefficient values beyond the initialization period, for the duration of the transmission. At the beginning of the initialization process, the TS75320 requires the input of the two-way far-end echo bulk delay.

A walkthrough description of the operation of the echo canceller is given in the next section. This includes the initialization processes and the details for formatting and for the selection of the appropriate order for the input and output of the data samples.

2.7. OPERATING PROCEDURE : INITIALIZATION AND DATA FORMATTING

The description below refers to flowcharts and sequence diagrams in Figures 2.8 to 2.12.

The initialization of the TS75320 is invoked by asserting the RESET signal (RESET\LOW, minimum duration 640 ns). This is the "booting" process during which the echo canceller workspace memory is cleared (coefficients, delay lines, operating variables) and the necessary parameters for the operation of all internal and interface processes are configured. The initialization sequence conforms to the requirements of CCITT Recommendation V.32 and is operated for starting up from cold, and also in case of retrains.

The **first mailbox exchange** after a RESET does not conform to the standard protocol described in Section 2.5. This is because the RESET generates an IRQ\LOW level well before the mailbox becomes available. Hence, for the first data transfer, and IRQ\triggered protocol cannot be used. Instead, the host must wait a minimum of 2 ms after the activation of the RESET\ signal, and then may proceed with the transfer of the three bytes **AA, AA, 00** (hexadecimal) into the mailbox R-IN register, using the mailbox data WRITE procedure as described in Section 2.5. This initiates the operation of the echo

canceller algorithm. The IRQ\ line is then restored to the RESET state (IRQ\ HIGH), and will thereafter be available for use in accordance with the normal protocol.

A mailbox exchange request will follow (**second mailbox exchange**), this time conforming to the normal (IRQ\ triggered) procedure as described in Section 2.5. In response the host is required to transfer the far-end round trip delay as a hexadecimal number using units of Baud periods. This number must be smaller than 3000 (decimal), i.e. 1.25 seconds. CCITT Recommendation V.32 includes a provision for measuring this delay during the modem handshake procedure.

The TS75320 will interpret the first two bytes in the R-IN register as the round trip delay, LSBs followed by MSBs, right justified. This delay must be greater than 0. The third byte must be 01 for normal operation, i.e. with far-end echo canceller enabled. If the third byte is 00, the far-end echo canceller is inhibited.

Example :

To enter a delay of (decimal) 2751 Baud periods, i.e. hexadecimal **0ABF**, the following three bytes must be transferred : first **BF**, then **0A**, then **01**. The third byte **01** is to enable the far-end echo canceller.

In response to a **third mailbox exchange** request the host enters a confirmation signal : **AA, AA, 01** ; this triggers the onset of the near-end cancellation algorithm. This confirmation must be sent at the start of the particular CCITT echo canceller adaptable sequence as an internal baud counter within the TS75320 will begin to increment at each baud interval. Two additional mailbox exchanges requests will occur which must be handled as dummy exchanges by the host. The host must perform at least 2 real operations per exchange-one to initiate the protocol and one to terminate the protocol as described in Section 2.5. Mailbox exchanges after this will be for the input of the rotated data symbols and of the cancellation error and for the output of the estimated echo.

During the first transfer the host transfers the cancellation error (first two bytes), followed by the rotated transmitted data symbol (third byte : a new rotated data symbol is input every third mailbox exchange). In the second mailbox exchange the estimated echo is transferred to the host using the same data format as for the cancellation error (details below). It should be noted that the first cancellation error and the first estimated echo will not represent meaningful data, but will serve as starting values. Also, the EC is frozen is the cancelling error is zero.

Thereafter, input and output data transfers will continue to alternate following the pattern detailed above, with the difference that, in the second and third input exchanges of the Baud interval, a new transmitted symbol is not transferred ; on those occasions the transfer of a CCI command as described in Fig. 2.9. must nevertheless be carried out.

The timing of these data transfers is determined by the modem transmitter sampling clock. Sample timing relationships are shown in Fig. 2.10. Fig. 2.10(a) illustrates the timing sequence for an implementation with a TS68950/51/52 analog front end. Fig. 2.10(b) shows the delay relationship between echo estimate and echo error.

The cancellation error and estimated echo are represented as 16-bit two's complement sample values. The least significant byte must be transferred first. The level of these signals will be determined by the level of the incoming line signal.

A question that arises at this point is whether there should be any scaling of the cancellation error before it is loaded in the echo canceller, in particular in the case of very low levels. The answer is that this signal **must not** be scaled. All that is required is that the incoming **line signal** at the point of substraction of the estimated echo should be at a level appropriate for the requirements of the analogue-digital interface circuitry, i.e. it should not be so high as to produce excessively frequent converter overflows, nor so low as to result in the waste of converter dynamic range. Within the TS75320, processing takes places in 32-bit arithmetic (corresponding to a range of 192 dB from quantization noise floor to saturation ceiling). This provides an adequate margin against erosion of numerical accuracy.

The data symbol is a complex-valued rotated trellis-coded V.32 encoder output (x, y), such that

- x and y are 4-bit two's complement integers in the range -4 to +4 (Fig. 2.11)
- the symbol must be rotated due to the effect of the modulation. The end result is to multiply the symbol by $(-j)^n$ where n = baud number being sent. This is seen as a -90 ° phase shift per baud interval.

Example : Consider the trellis-coded symbol **10010** in the V.32 signal constellation (see Fig. 2.11). The corresponding co-ordinates are x = – 2, y = – 3. If n = 9, $(-j)^n = -j$, and the rotated coordinates become x = – 3, y = –2.

- the real part x is located in the four most significant bits, the imaginary part y in the four least significant bits

For the example above the real part is hexadecimal D, and the imaginary part is 2 in two's complement representation. Hence, the data byte to be transferred for this symbol is D2.

A new rotated data symbol is transferred only once per Baud interval, i.e. every third input sample transfer.

Fig. 2.12 displays the overall sequence of interface exchanges in relation to echo canceller internal processes. As indicated in the previous section, only the near-end algorithm operates in the first phase of adaptation. After S-S transition, the near-end algorithm will have converged, and the far-end algorithm is set into operation automatically (subject to the value of the third byte in the bulk delay data transfer, see above). In this phase both the near-end and far-end algorithms operate together.

After 16656 Baud intervals, transmission is interrupted to allow the other terminal set up its echo canceller. Full duplex data transmission may begin once both echo canceller algorithms have converged, and the modem handshakes completed.

3. PERFORMANCE VALIDATION

3.1. GENERAL

The minimum signal-to-residual-echo ratio and cancellation algorithm convergence rate requirements for V.32 modems are given in Section 1.3. Measurements procedures to obtain benchmark indicators of the performance of the TS75320 are described below. The test procedures and benchmark results are intended to provide reference conditions for application development and trouble shooting. The results obtained using these test procedures meet or exceed the requirements of CCITT Recommendation V.32.

The tests consist of the measurement of convergence times and residual echo levels under various conditions of operation as follows :

(a) near-end echo algorithm operating alone, with far-end signal absent

(b) near-end echo and far-end echo algorithms both in operation, with far-end signal absent, with and without frequency offset

(c) near-end and far-end echo algorithms both in operation, over a range of far-end signal levels, with and without frequency offset.

The tests are carried out using the normal initialization procedures (as described in Section 2.6), i.e. tests in category (b) require prior convergence of the near-end echo algorithm under condition (a), and, similarly, tests in category (c) require prior convergence of the combined near-end echo and far-end echo algorithms under conditions (a) and (b), respectively. For this reason, convergence times are relevant only for tests in categories (a) and (b).

3.2. TEST SYSTEM

A block schematic diagram of the test system is shown in Fig. 3.1.

TS68931 digital signal processors and a TS68950/951/952 modem analog front-end (MAFE) chip set are used to generate the near-end and far-end signals, and to emulate the transmission conditions for the far-end echo, including frequency offset and bulk delay. The integral linearity of the TS68950 Modem Transmit Analog Interface D/A converters is 11 bits, as needed to realize the required cancellation performance.

The line characteristics for the near-end echo are generated using a Wilcom line simulator model T240 (Wilcom Products Inc., Laconia, N.H., U.S.A.). The following artificial line module types are included :

(a) compromise network with 600/900 Ohm switch

(b) 6000ft/22gauge, 83nF/mile

(c) 88mH module with 3-position switch for normal, no-load or half-load operation

The impulse response of the far-end echo path is given in Fig. 3.2 (excluding the bulk delay).

3.3. NEAR-END ECHO ALGORITHM WITH NO FAR-END SIGNAL

The conditions for these tests correspond to the first phase of the initialization procedure, i.e. the far-end modem is not transmitting, and the far-end echo algorithm is not enabled.

The Wilcom line simulator is set up with six modules in circuit, as follows :

(i)	6000ft/22g
(ii)	88mH/half load
(iii)	6000ft/22g
(iv)	88mH/no load
(v)	compromise network/600Ohm
(vi)	6000ft/22g

The V.32 transmitter output is - 2.2 dBm. The near-end echo level at the canceller input is - 9.2 dBm, i.e. 7 dB below the transmitted V.32 signal. It should be noted this represents a highly pessimistic condition (see Section 1.3).

A typical oscilloscope trace of the residual echo versus time is shown in Fig. 3.3. The convergence time for this test is 360 ms (cf. 1.5 second maximum allowed). Similar convergence characteristics are ob-

tained for this test over a wide range of line conditions.

3.4. NEAR-END ECHO AND FAR-END ECHO ALGORITHMS WITH NO FAR-END SIGNAL

In these tests the convergence of both the near-end echo and the far-end echo algorithms are measured. The test conditions for the results documented are as follows :

- Wilcom line simulator as in Section 3.3
- bulk delay 570 ms
- frequency offset 0.5 Hz
- far-end echo level - 16 dBm

A typical oscilloscope trace of the residual echo versus time is shown in Fig. 3.3. The overall convergence time for the two algorithms is less than 6.9 seconds.

Similar convergence characteristics are obtained for this test without frequency offset, and over a wide range of line conditions.

The steady-state residual echo level versus far-end echo level is displayed in graphical form in Fig. 3.4.

3.5. NEAR-END ECHO AND FAR-END ALGORITHMS WITH FAR-END SIGNAL

In this test the steady-state residual echo level is measured as a function of the far-end signal level, for various levels of far-end echo. The test conditions are the same as in Section 3.4.

The results are displayed in Fig. 3.5. Similar performance is obtained in the absence of frequency offset.

3.6. PERFORMANCE SUMMARY

The TS75320 achieves the suppression ratios and convergence speeds required for high performance V.32 modems. With an appropriate choice of analog front-end (such as the SGS-THOMSON TS68950/951/952 MAFE chip set) the near-end echo canceller yields a suppression ratio better than 55 dB. In the absence of far-end signal and far-end echo, the residual echo level is below - 65 dBm for a near-end echo level of - 10 dBm at the receiver input.

For operation with combined near-end and far-end cancellers, the signal-to-residual-echo ratio achieved at the receiver input is better than 24 dB for typical receive levels around - 20 dBm. This performance is maintained in the presence of 10 Hz of frequency offset in the far-end echo. The signal-to-residual-echo ratio remains better than 21 dB for receive levels as low as - 40 dBm, provided the far-end echo is at least 8 dB below the level of the received far-end signal.

The convergence time for the near-end echo canceller is typically around 0.5 second, and not greater than 1.5 seconds. The overall convergence time for near-end and far-end cancellers combined is not greater than 6.9 seconds (16656 Baud intervals), without or with frequency offset, conforming to the handshake requirements in CCITT Recommendation V.32.

REFERENCES

1. D.G. Messerschmitt, *Echo Cancellation in Speech and Data transmission;* Chapter 4 in K. FEHER, *Advanced Digital Communications: Systems and Signal Processing Techniques,* Prentice-Hall 1987.
2. M. Stein, *Les Modems pour Transmission de Données,* Masson 1987, see Section 6.5 (pp. 227-239).
3. SGS-THOMSON Data Sheet: *TS75320 Digital Echo Canceller.*
4. SGS-THOMSON Data Sheet: *TS68930/931 Programmable Signal Processor.*
5. SGS-THOMSON Data Sheet: *TS68950 Modem Transmit Analog Interface.*
6. SGS-THOMSON Data Sheet: *TS68951 Modem Receive Analog Interface.*
7. SGS-THOMSON Data Sheet: *TS68952 Modem Transmit/Receive Clock Generator.*
8. SGS-THOMSON: *Development of Real-time Algorithms Using the Thomson Digital Signal Processor TS68930 and the Thomson Analog Front-end TS68950/1/2;* Thomson Semiconducteurs, Application Note AN-076.

Figure 1.1 : Near-end and Far-end Echo Paths in Conventional Telephone Network Connections (blocks labelled "H" are hybrid transformers, shown in figure 1.2).

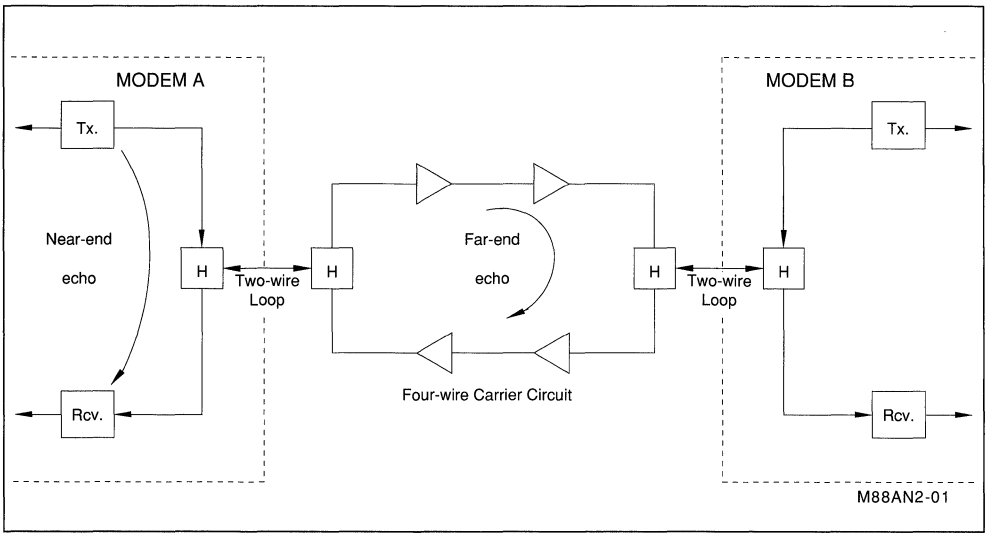


Figure 1.2 : Simplified Model of Echo Suppression in Hybrid Transformers.

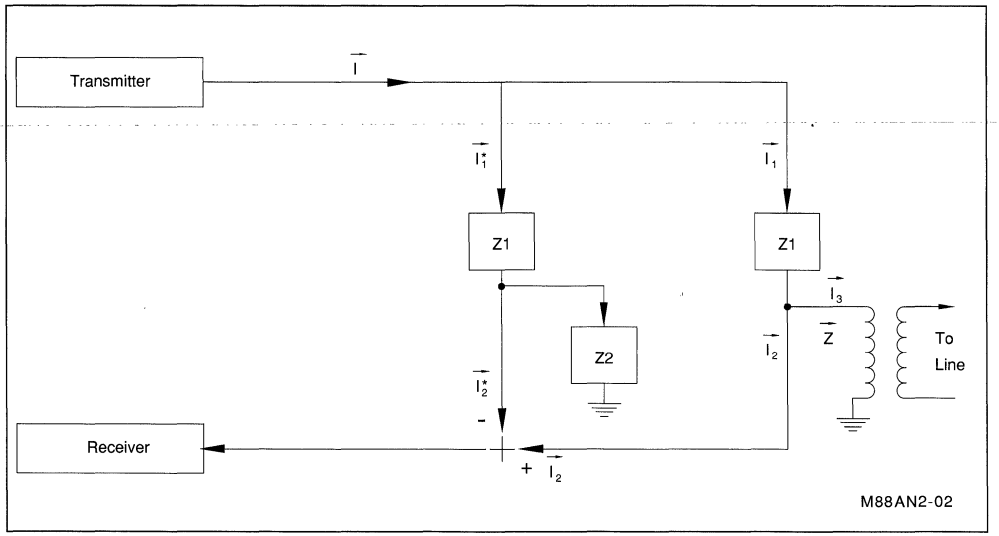


Figure 1.3 : Block Diagram Showing Modem and Echo Canceller Connection to the Telephone Network.

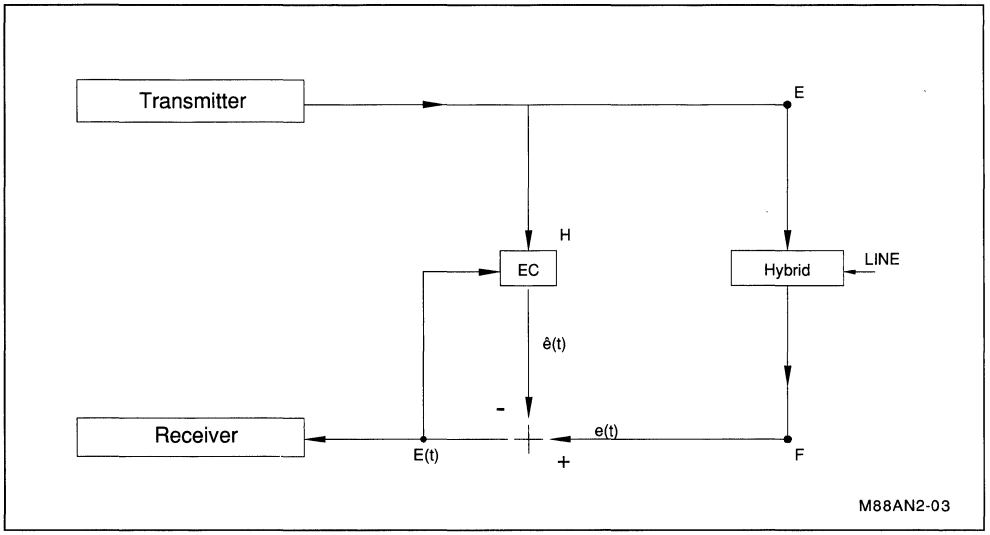


Figure 1.4 : Block Diagram Showing the Connection of the Near-end and Far-end Echo Cancellers to the Modem and Telephone Network.

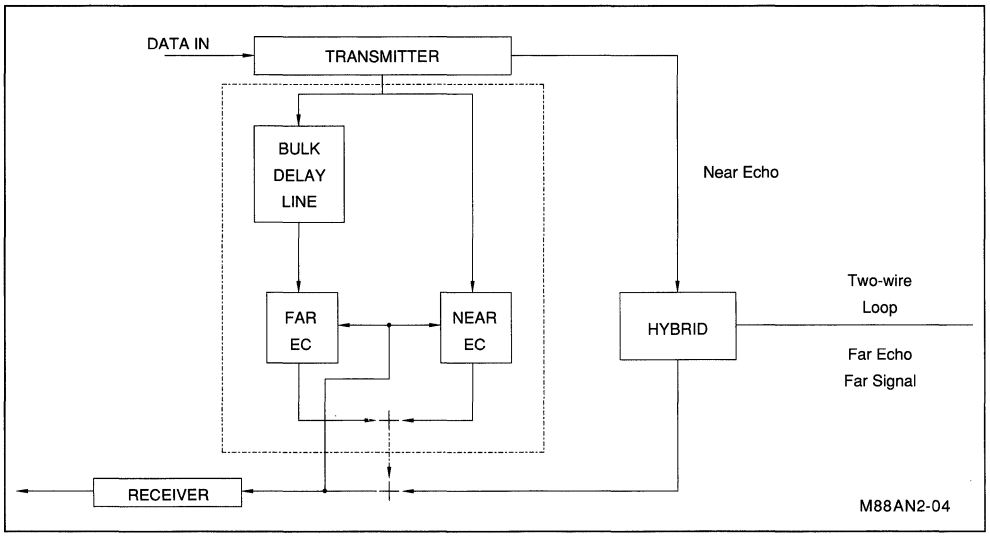


Figure 2.1 : Blocks Schematic Diagram of TS75320 Hardware Interface Showing Connection to Host Via the System Bus and RAM Access Via the Local Bus.

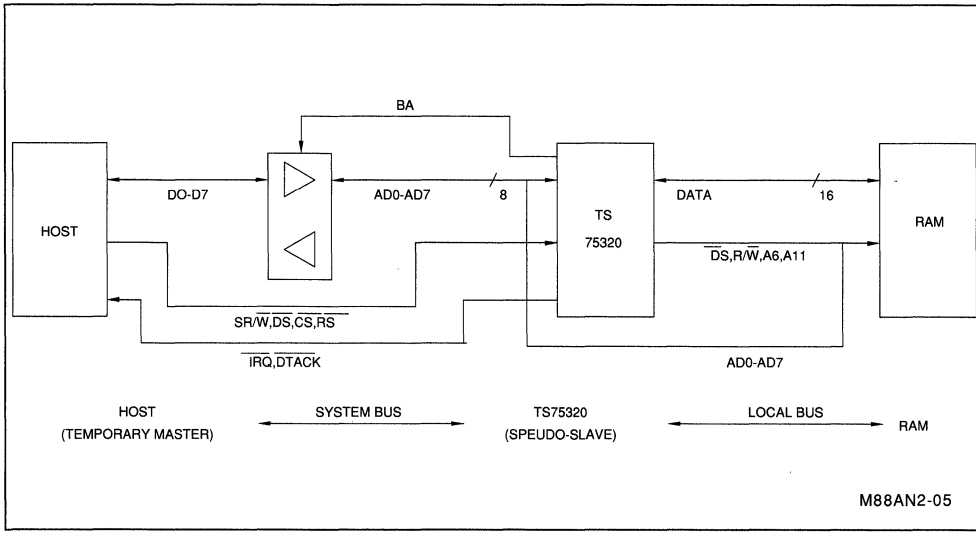
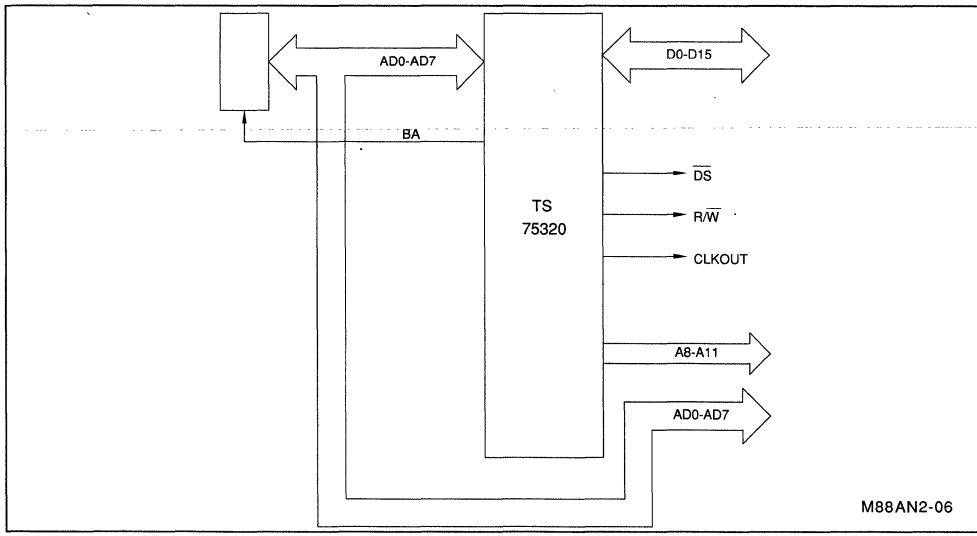


Figure 2.2 : Local Bus Hardware Interface.

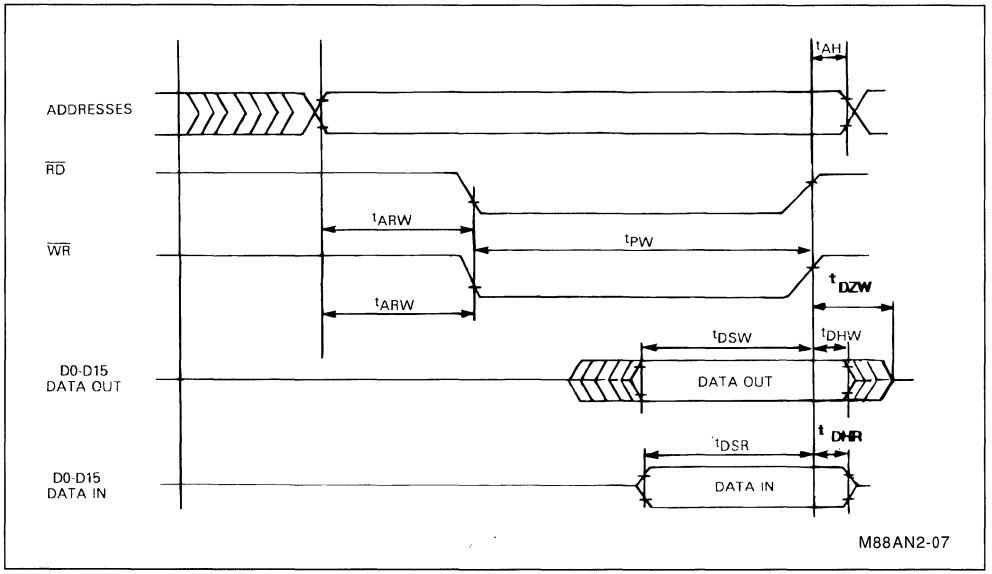


ELECTRICAL CHARACTERISTICS - LOCAL BUS TIMING

Symbol	Parameter	Min.	Max.	Unit
t_{PW}	$\overline{RD}$, $\overline{WR}$ Pulse Width	1/5 tc – 15	1/2 tc	ns
t_{AH}	Address Hold Time	10		ns
t_{DSW}	Data Set-up Time, Write Cycle	25		ns
t_{DHW}	Data Hold Time, Write Cycle	10		ns
t_{DSR}	Data Set-up Time, Read Cycle	20		ns
t_{DHR}	Data Hold Time, Read Cycle	5		ns
t_{ARW}	Address Valid to $\overline{WR}$, $\overline{RD}$ Low	1/2 tc – 40		ns

* Assuming 25 MHz clock (CLKOUT CYCLE = 80 ns).

Figure 2.3 A : Local Bus Timing.



AC ELECTRICAL SPECIFICATIONS. SYSTEM BUS TIMING

(Vcc = 5.0V ± 5%, T_{amb} = 0°C to + 70°C ; see figure 6)

Symbol	Parameter	Min.	Max.	Unit
t_{SPW}	$\overline{SDS}$, Pulse Width	60		ns
t_{SAW}	SR/$\overline{W}$, $\overline{CS}$, $\overline{RS}$ Set-up Time	10		ns
t_{SAH}	SR/$\overline{W}$, $\overline{CS}$, $\overline{RS}$ Hold after $\overline{SDS}$ High	5		ns
t_{SDSR}	Data Set-up Time, Read Cycle	20		ns
t_{SDHR}	Data Hold Time, Read Cycle	5		ns
t_{SDSW}	Data Set-up Time, Write Cycle		35	ns
t_{SDHW}	Data Hold Time, Write Cycle	10	50	ns
t_{DSLDT}	$\overline{SDS}$ Low To $\overline{DTACK}$ Low		50	ns
t_{DSHDT}	$\overline{SDS}$ High to $\overline{DTACK}$ High*		50	ns
t_{DSHIR}	$\overline{SDS}$ High to $\overline{IRQ}$ High		50	ns
t_{SDZW}	$\overline{SDS}$ High to Data High Impedance, Write Cycle		40	ns

* DTACK is an open drain output first load include R_L = 890 Ω at V_{CC}.

Figure 2.3 B : System Bus Timing Diagram.

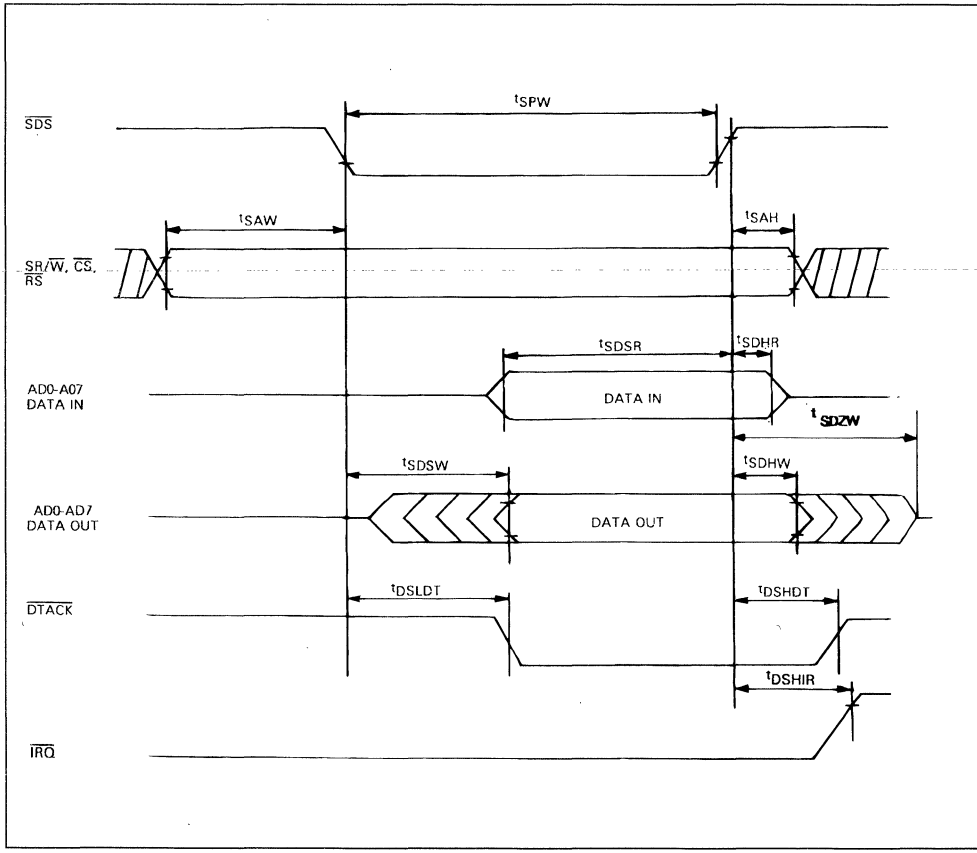


Figure 2.4 : Functional Timing Diagram for System Bus Data Transfers.

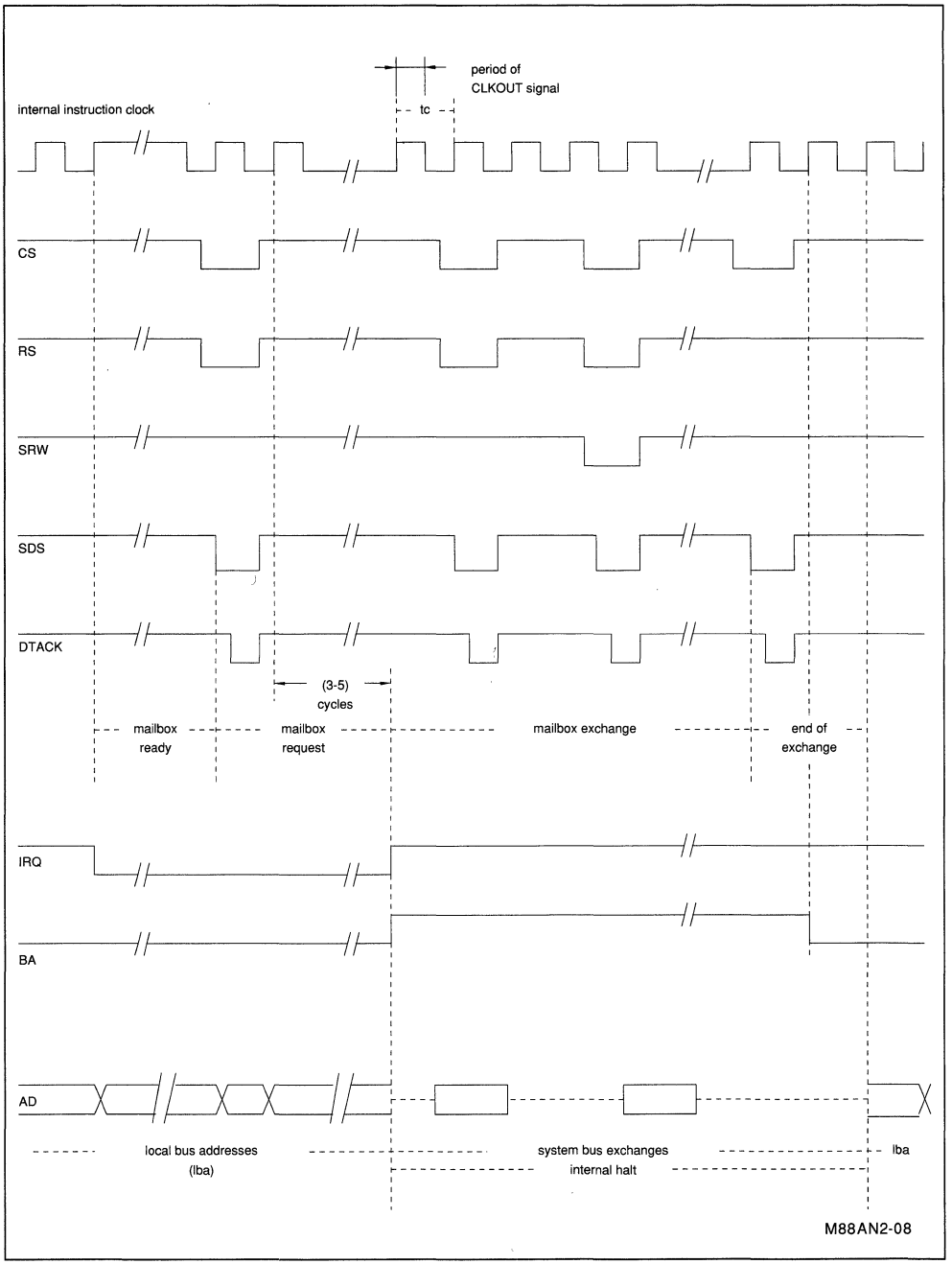


Figure 2.5 : (a) Flowchart of Mailbox Handshake Protocol.

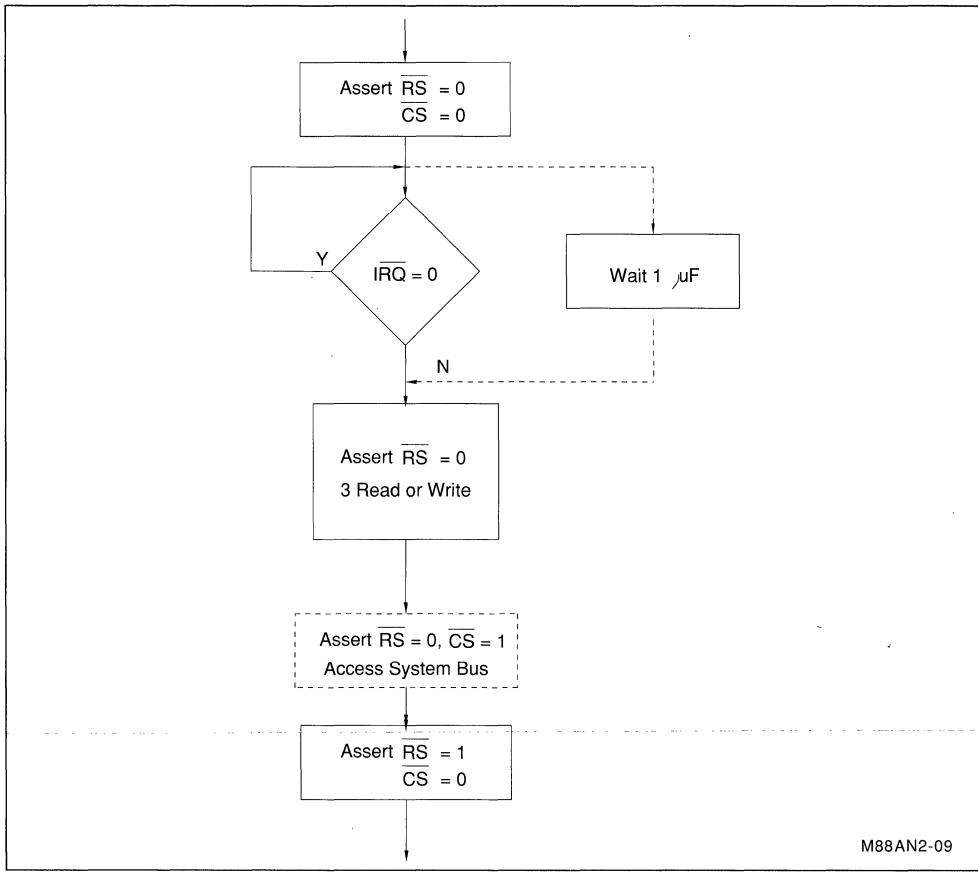
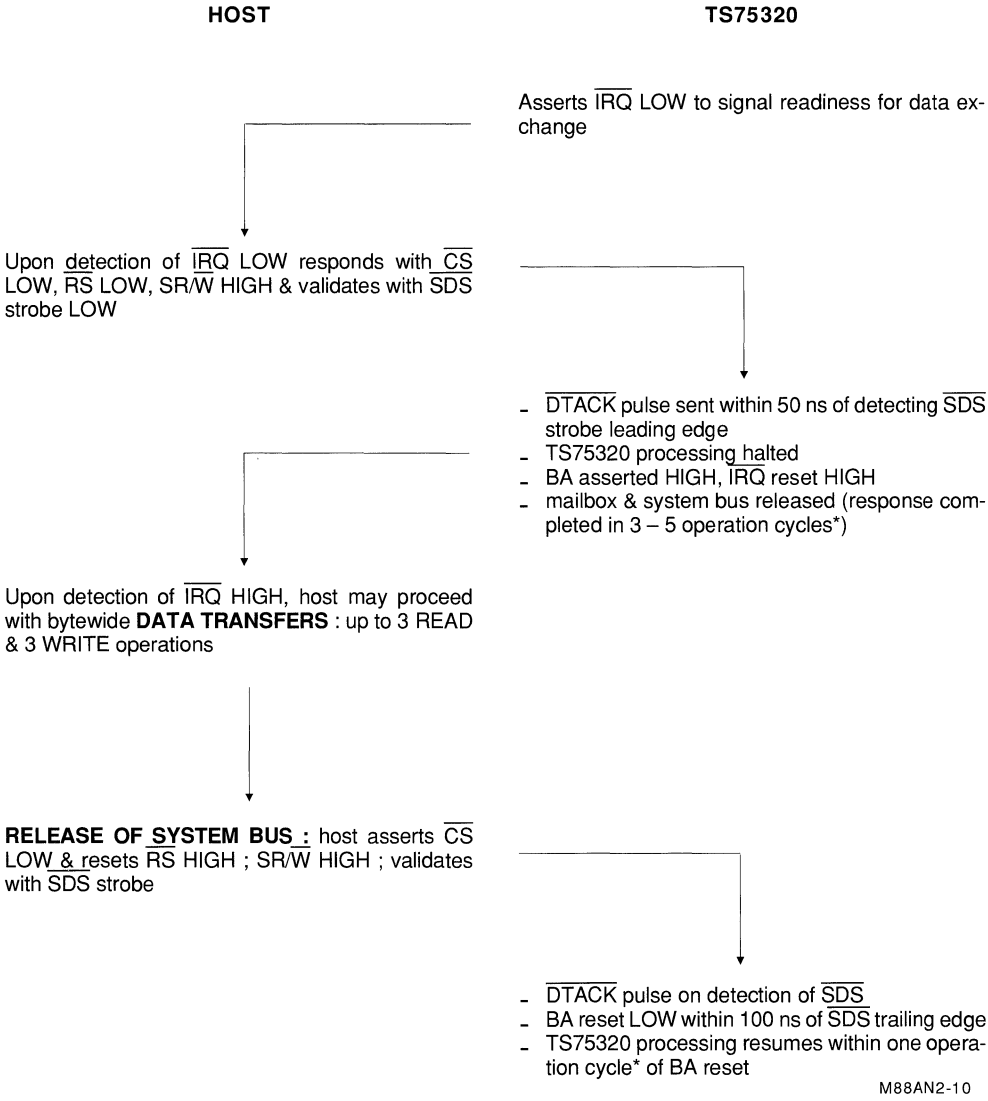
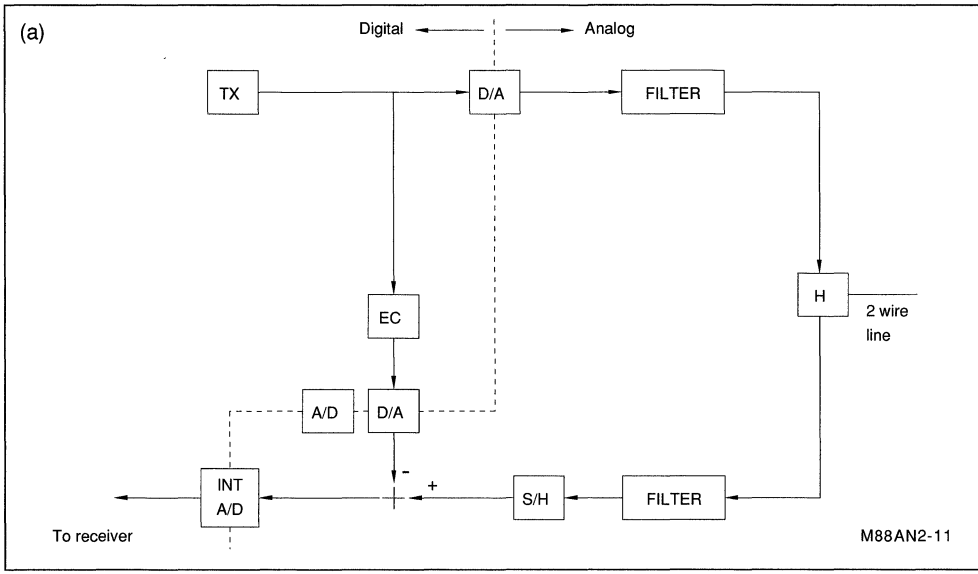


Figure 2.5 : (b) Schematic Description of Mailbox Handshake Protocol.



* The CLKOUT pin allows access to the TS75320 internal clock. There are two CLKOUT cycles per operation cycle.

Figure 2.6 : Block Diagram Showing Implementations of a Digital Passband Echo Canceller Using.
(a) Analog Substraction
and,
(b) Digital Substraction



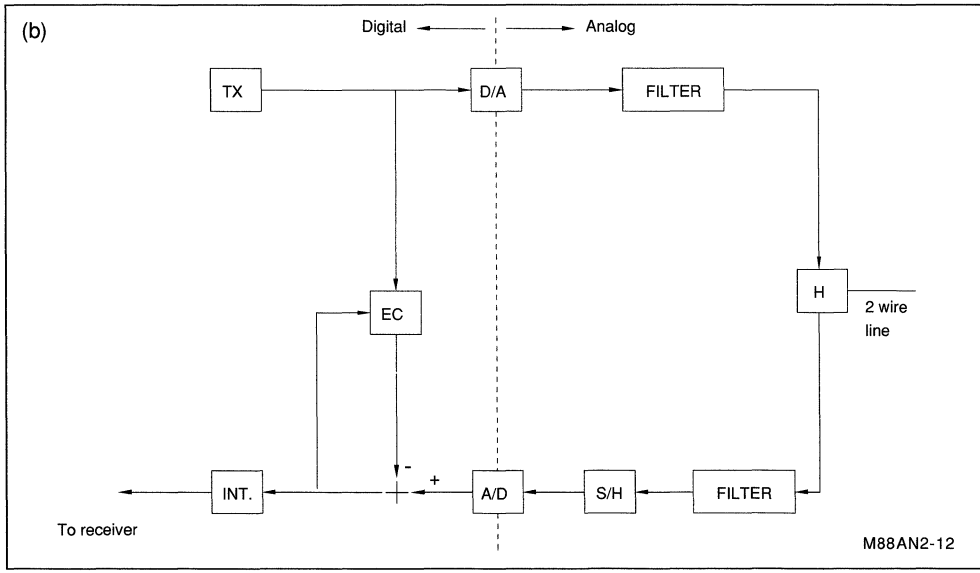


Figure 2.7 : (a) Block Schematic Representation of the TS68950/951/952 Showing Functional Components and the Connection to a Host System.

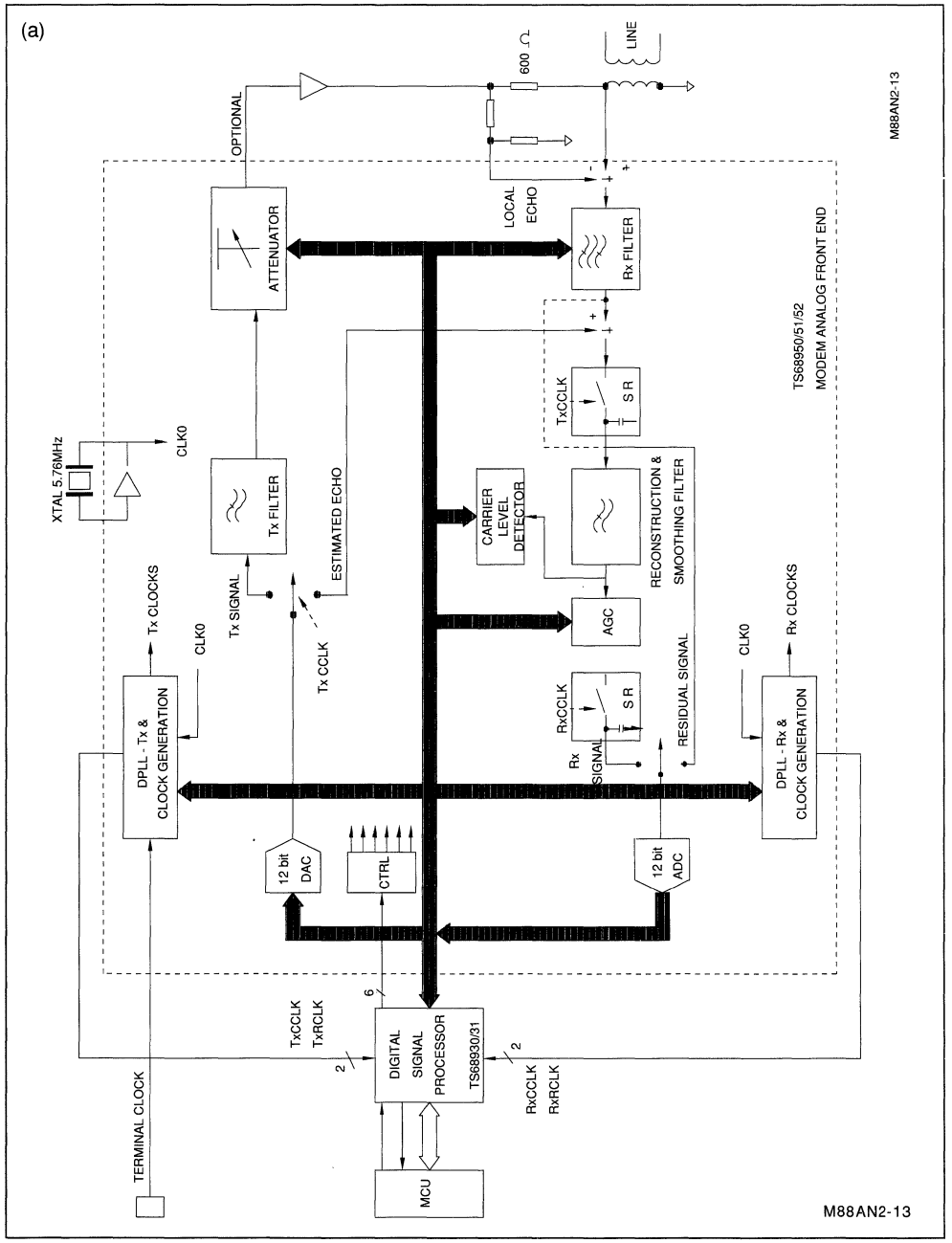
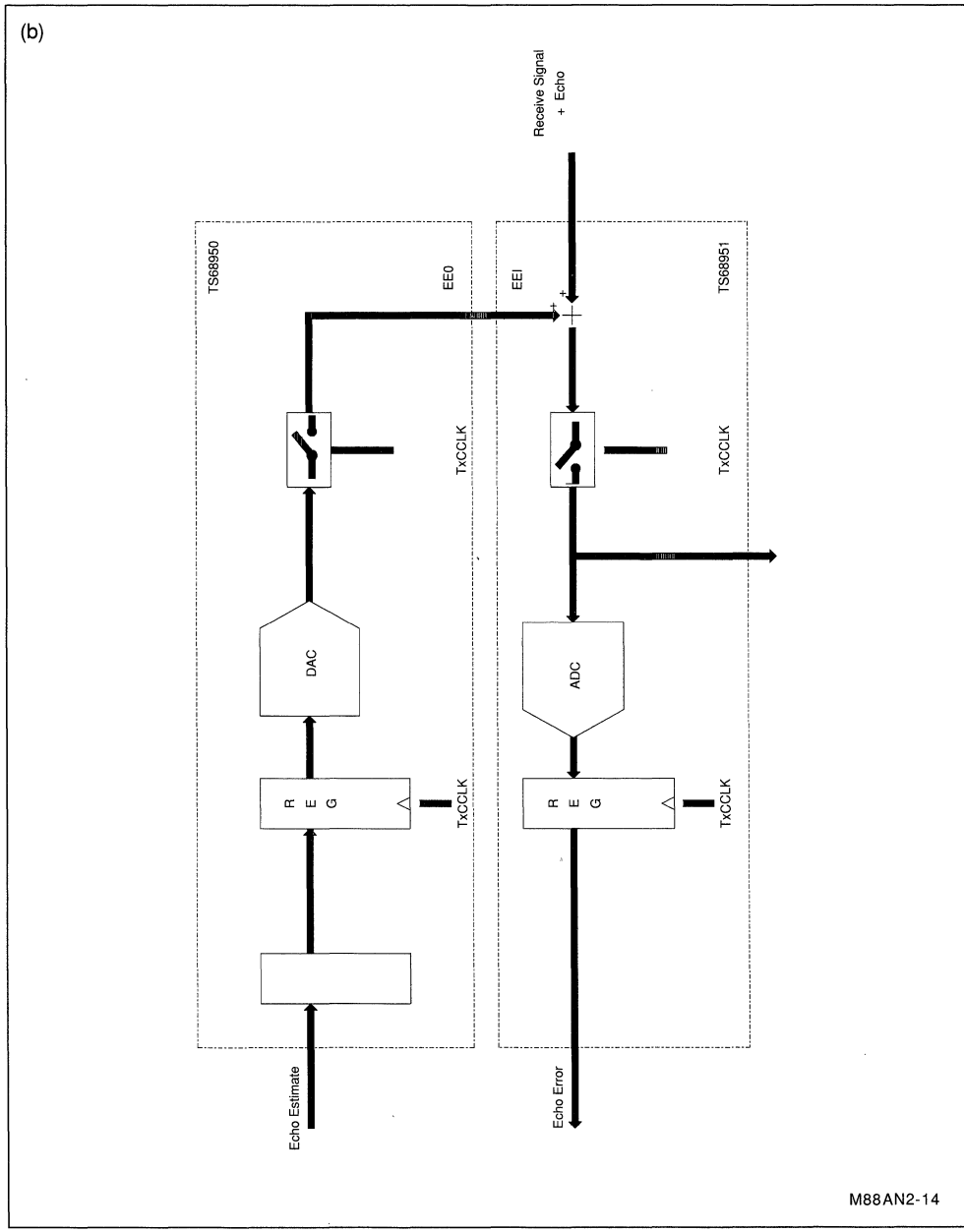


Figure 2.7 : (b) V.32 Echo Canceller Analog Loop Using SGS-THOMSON TS68930/931/932 Modem Analog Front End.



N.B : Within the TS75320 the polarity of the estimated echo output sample is inverted ; hence, the substraction operation is realized as a physical **addition**.

Figure 2.8 : Flow Chart of TS75320 Echo Canceller Start-up Sequence.

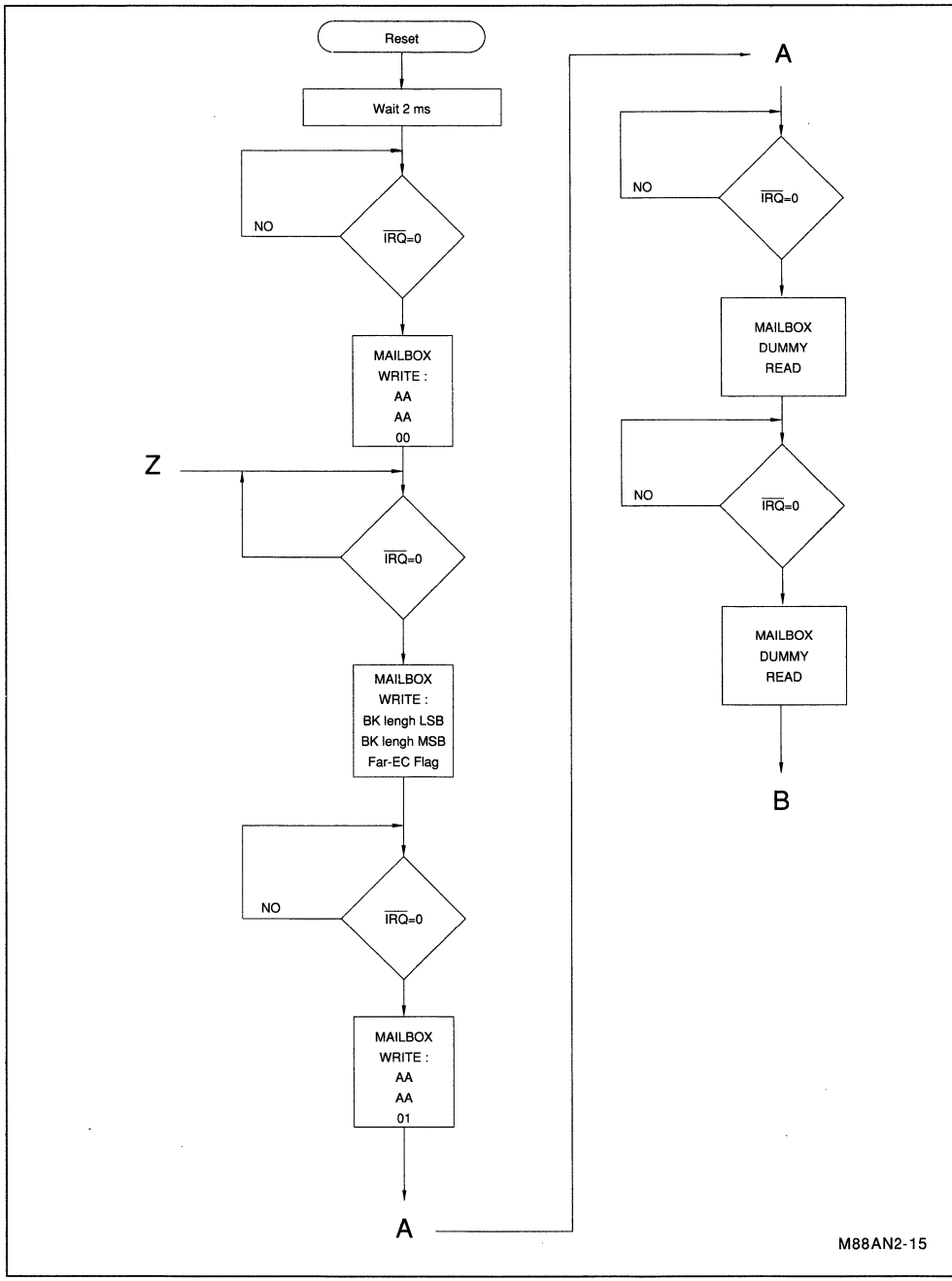
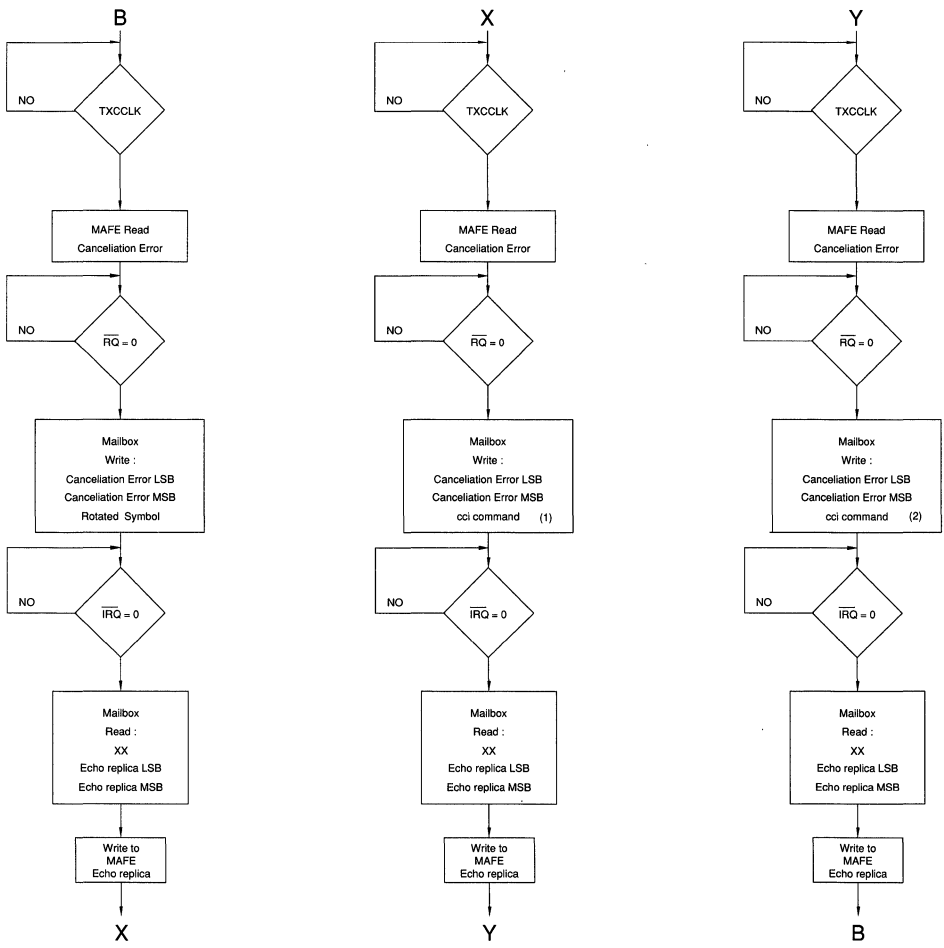
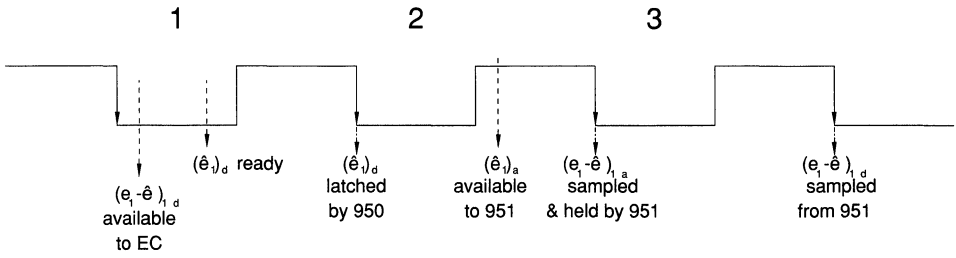


Figure 2.9 : Flow Chart of TS75320 Echo Canceller Master Synchronization Procedure.



Notes : 1. If CCI command sent is $6, then branch to RESET (must be used for retrain).
2. If CCI command sent is $15, then branch to Z .

Figure 2.10 : (a) Transmit Sample Timing Example (implementation with a TS68930/931/932 Analog Front End).
(b) Simplified Block Diagram Representation Showing Delay Relationship between Echo Estimate and Echo Error.



e_1 : echo of phase 1
$(\hat{e}_1)_d$: echo replica of phase 1 in digital form
$(\hat{e}_1)_a$: echo replica of phase 1 in analog form

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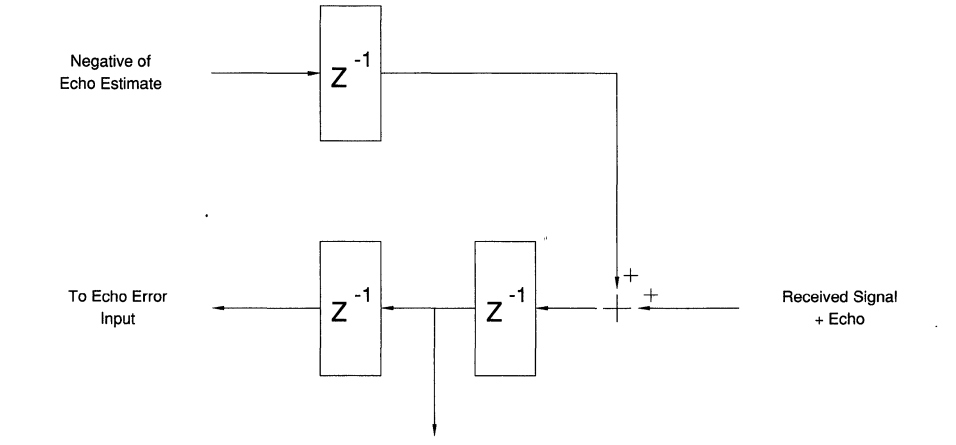

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Figure 2.11 : V.32 Signal Space Constellation After Trellis Coding.

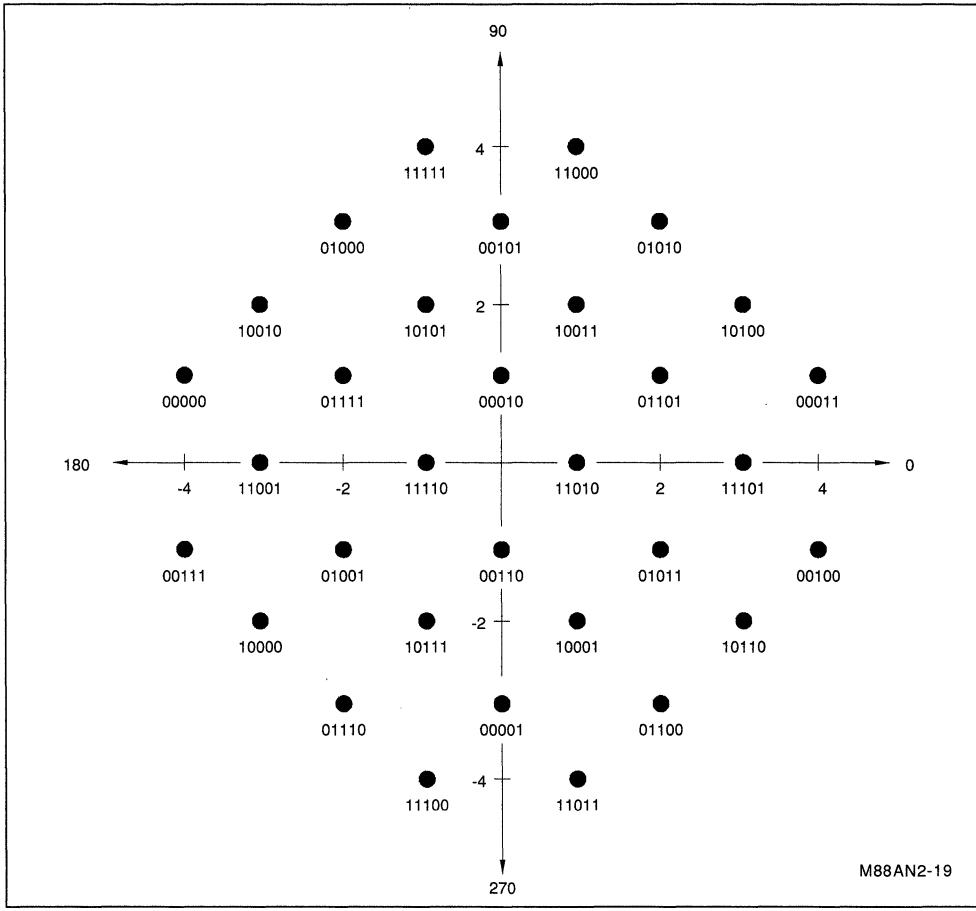
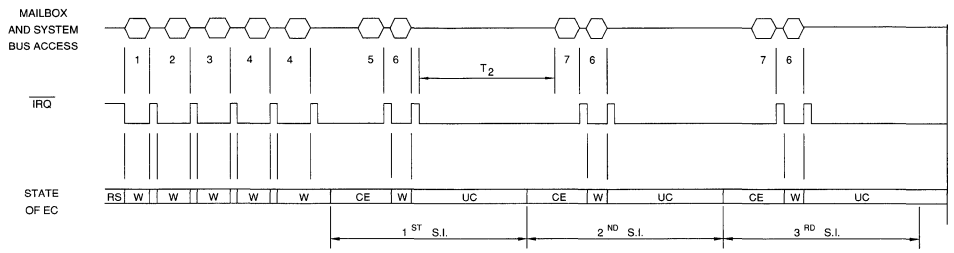


Figure 2.12 : Sequence of Interface Exchanges in Relation to Echo Canceller Internal Processes.



$t_2 - t_1 < 10\ \mu s$

Notations :

MWR	–	Mailbox Write & Read
W	–	Wait Mailbox Access
H	–	Hait and Releases System Bus
CE	–	Compute Echo Estimate
UC	–	Update Coefficients

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Figure 3.1 : Block Diagram of Modem and Line Emulation Unit.

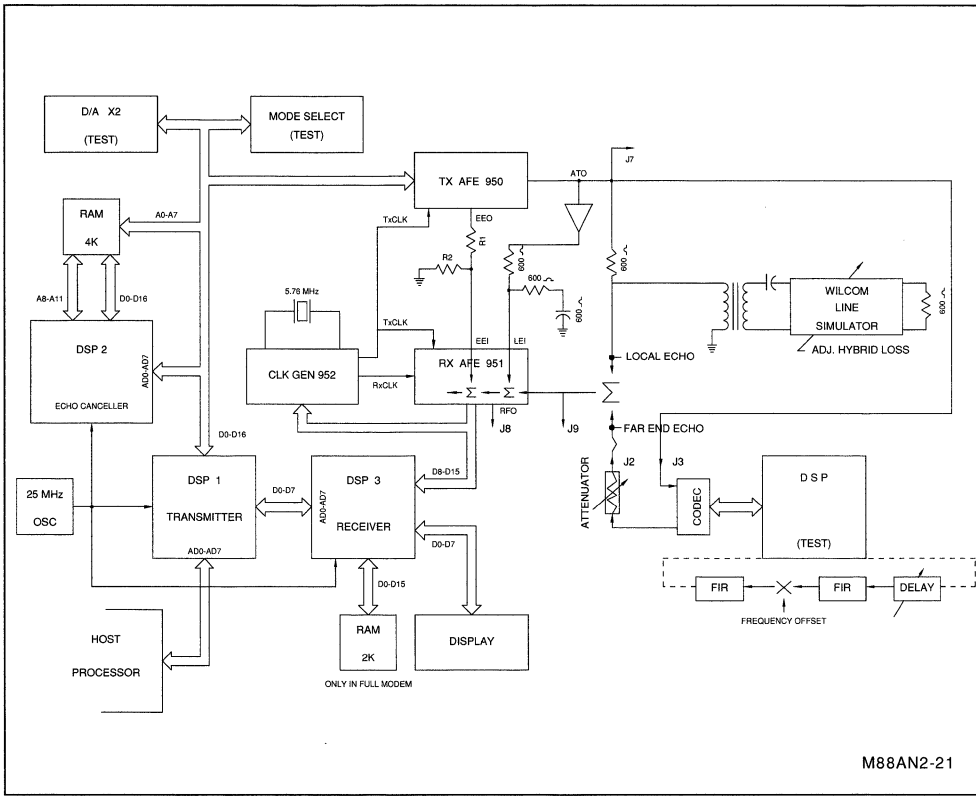

Figure 3.2 : Impulse Response of Far-end Echo Path Emulation (Excluding Bulk Delay).

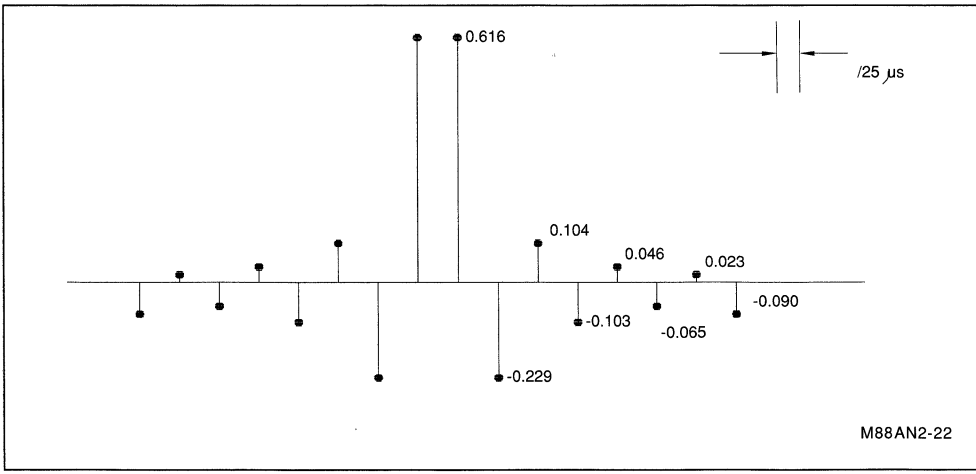

Figure 3.3 : Convergence of Near-end Echo Cancellation Algorithm.

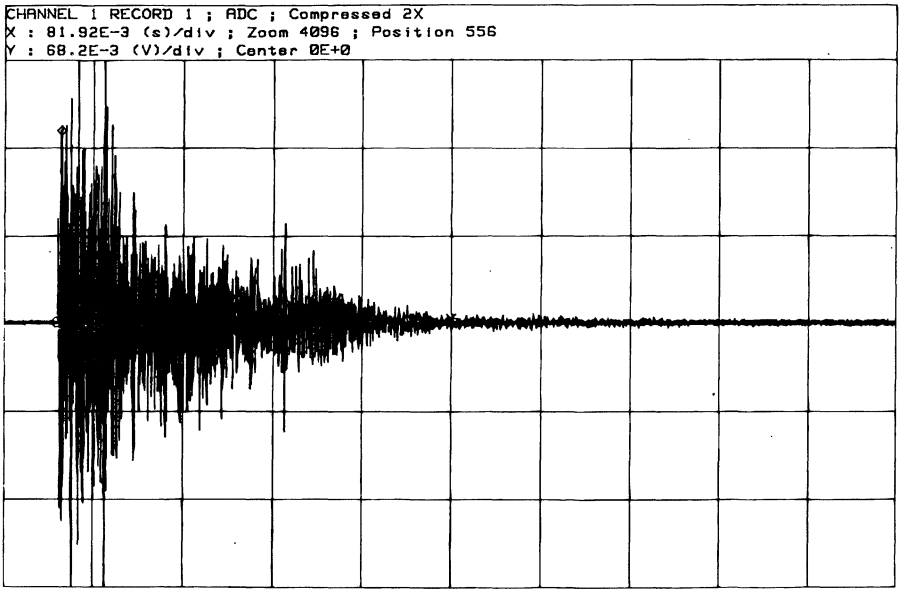

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Figure 3.4 : Residual Echo Versus Far-end Echo Level without Far-end Signal.

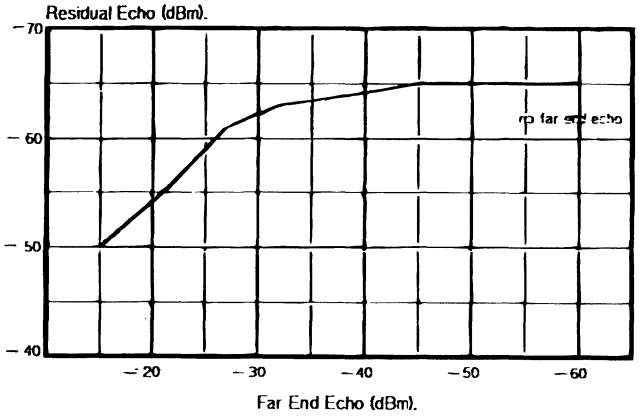

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Figure 3.5 : Residual Echo Versus Far-end Signal Level for Various Far-end Echo Levels.

TEST CONDITIONS

1. Far-end Echo Delay of 570 ms
2. Wilcom Line Simulator 6000 Ft. ; 1/2 Load, 88 mH ; 6000 88 mH, no Load ; Compromise Network = 600 Ω ; 6000 F.

Far-end Echo	Far-end Signal				
	– 8dBm .0, .5HZ	**– 14 .0, .5HZ**	**– 20 .0, .5 HZ**	**– 26 .0, .5HZ**	**– 32 .0, .5HZ**
– 15dBm	– 22, – 24	X	X	X	X
– 21	– 25, – 25	– 24, – 24	X	X	X
– 27	– 26, – 25	– 27, – 27	– 24, – 25	X	X
– 32	– 25, – 25	– 25, – 25	– 25, – 25	– 24, – 25	X
– 39	– 25, – 25	– 24, – 24	– 25, – 25	– 25, – 25	– 22, – 23

INTERFACING THE TS7524 MODEM CHIP-SET TO A COMMUNICATION CONTROL PROCESSOR

By O. LEEHNARDT (applications laboratory)

The S.G.S.-THOMSON Microelectronics **TS7524** is a high performance voiceband multi-standard modem chip set covering all C.C.I.T.T. and BELL standards from 300 to 2400 bps full-duplex over public switched telephone network or leased lines. The chip set consists of the **TS75240** Digital Signal Processor and the **TS68950/51/52** Modem Analog Front End.

This application note details the basic interface principle between the TS7524 and the communication control processor. Also included are architecture examples as well as programming examples.

1. HARDWARE INTERFACE

The basic interface signals between the TS7524 and the control processor are summarized in figure 1. Data exchange between the TS75240 and the control processor take place by means of a "mailbox" within the TS75240, accessible externally through the 8-bit bidirectional system data bus of the TS75240.

1.1 THE SYSTEM BUS

Its consists of three basic sections :

- **Data bus** : AD0/AD7 (8 bidirectional lines)
- **Address bus** : $\overline{CS}$ Chip Select
  $\overline{RS}$ Register Select
- **Control bus** : SR/$\overline{W}$ System Read/Write
  $\overline{SDS}$ System Data Strobe
  $\overline{IRQ}$ Interrupt Request

Note : The RESET pin, not included in the control bus, must be used when interfacing the TS7524 and the control processor (see 1.3.).

1.2. THE MAILBOX

The mailbox, located internally to the TS75240, consists of two shift registers, each of these is 24 bit wide :

- the "R-IN" register, or **command register**, for the data written by the control processor into the TS75240 (data input),
- the "R-OUT" register, or **status register**, for the data written by the TS75240 into the control processor (data output).

These two registers are each splitted in a 3-byte word, each word being of two types : **transmit** and **receive**.

Note : The general description of these different status and command words (transmit and receive) is given in appendix E. For any additional information, please refer to the TS7524 data sheet.

1.3. INTERFACE SIGNALS

From a hardware point of view, the different resources of the control processor required to perform the functional interface with the TS7524 are the following :

- 1 output port line to reset the TS75240,
- 1 external active low interrupt input ($\overline{IRQ1}$),
- 4 output lines for address and control (output port or bus control signals),
- 8 bidirectional data lines AD0/AD7 (I/O port or bus). AD0 is the least significant bit of the data bus.

1.4. RESET OF TS 75240

After power-up, the first mailbox transfer will occur only after reset of TS75240.

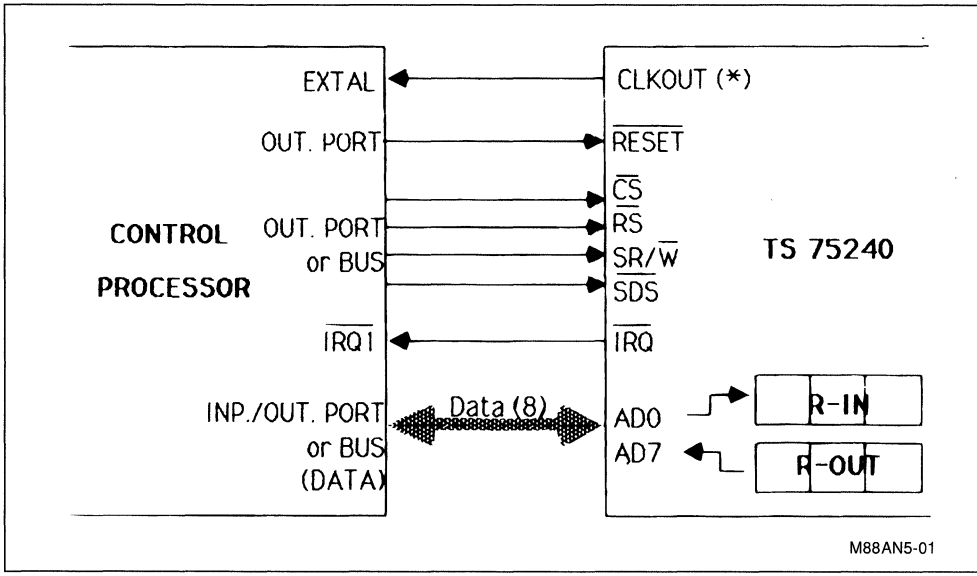
The minimum duration of the reset is 870 nsec. (5 cycles of 174 nsec. with a 23.04 MHz crystal).

It is also absolutely **required to reset the TS75240 before changing the operational mode of the modem** (except during the V.22 bis handshake where changing the two command words are sufficient when switching from V.22 to V.22 bis).

After all reset of TS75240, the only thing to do for the control processor is to wait for activation of $\overline{IRQ}$ signal by the TS75240. This activation is the first action which occurs, from the TS75240, immediately after setting the reset signal issued by the control processor.

During the first mailbox transfer following each reset of TS75240, all the bits of the status word (three bytes) are not significant. The TS75240 waits for the first command word (three bytes) before sending significant bits in the status word during the next following mailbox transfer.

Figure 1.



(*) The TS75240 provides on its CLKOUT pin a clock signal at 11.52 MHz (23.04 MHz/2) which can be used by the control processor.

2. SOFTWARE INTERFACE

2.1. TRANSFER MECHANISM

Information exchange between the control processor and the TS75240 is made by enslaving the mailbox exchange to the differend Baud period (* *) (transmit and receive) of the TS75240. The control processor will have to be able to manage :

- one mailbox transfer at each transmit Baud period allowing exchange of :
  - one status word from the TS75240 to the control processor,
  - one command word from the control processor to the TS75240 (the transmit data belong to these bytes).
- one mailbox transfer at each receive Baud period allowing exchange of :
  - one status word from the TS75240 to the control processor (the receive data belong to these bytes),
  - one command word from the control processor to the TS75240.

(* *) : Baud period corresponds to 600 Hz in Q.A.M. (V.22 bis) and D.P.S.K. (V.22 and BELL 212) and 1200 Hz in F.S.K. (V.21, V.23 and BELL 103).

Note : Either "RESERVED" or without change (see appendix E), two words must be transferred at each mailbox transfer : one status word (transmit or receive) and one command word (transmit or receive).

2.2. MAILBOX TRANSFER PROTOCOL

This section describes the functional mailbox transfer protocol. System bus timing characteristics are given in appendix D.

Each mailbox transfer is **driven by the control processor but controlled through a sequencer included in the TS75240** by means of an internal flag (RDYOIN) and an external interrupt request signal (IRQ).

The internal flag RDYOIN indicates whether the TS75240 (RDYOIN = 0) or the control processor (RDYOIN = 1) has access to the mailbox.

The external IRQ interrupt request signal is used by the control processor to gain access to the mailbox :

This sequencer is shown figure 2.

- The mailbox is made available to the control

processor by the TS75240 program which sets RDYOIN flag to 1.

- $\overline{IRQ}$ is asserted (*) ($\overline{IRQ}$ = 0) by the TS75240 to indicate the availability of the mailbox (at the same time as RDYOIN = 1),

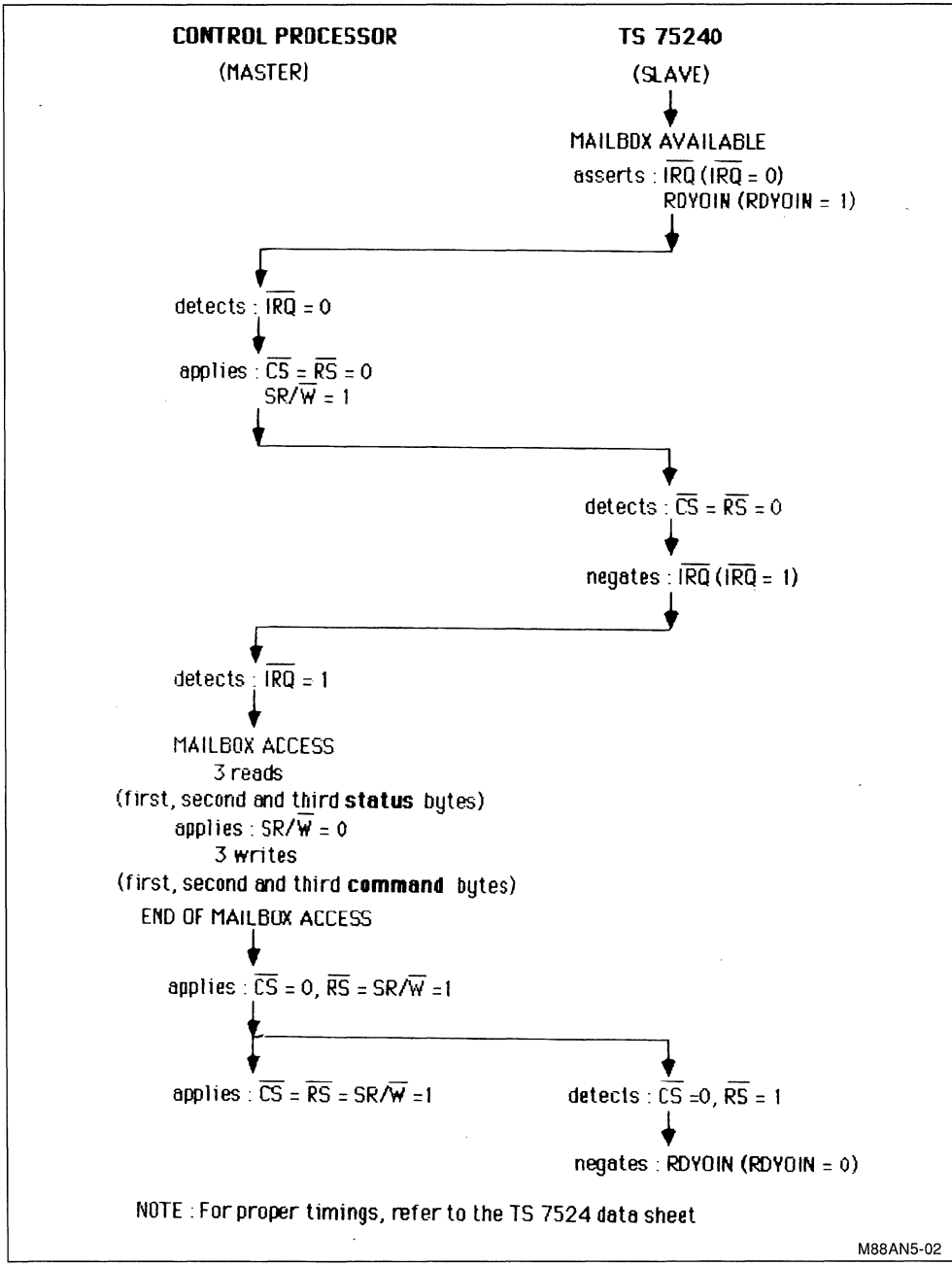
(*) : $\overline{IRQ}$ is asserted by the TS75240 immediately after each reset of TS75240.

- After detecting $\overline{IRQ}$ assertion, the control processor knows that it can access the mailbox but does not know if it has access to the bus. It requests the bus by generating the address $\overline{CS}$ = $\overline{RS}$ = 0 and the control signal SR/$\overline{W}$ = 1. A dummy read is performed by the TS75240.
- After detecting the dummy read of its mailbox, the TS75240 internal I/O sequencer answers back by negating $\overline{IRQ}$ ($\overline{IRQ}$ = 1). The control processor detects the negation of $\overline{IRQ}$ indicating that the mailbox is available for data transfers.
  It has now full control of the bus and the mailbox. The data exchange can be performed.
  The control processor reads one status word (SR/$\overline{W}$ = 1) and writes one command word (SR/$\overline{W}$ = 0) in the mailbox shift registers R-OUT and R-IN respectively.
  After each read or write, the data is automatically shifted to allow read or write of the following byte.
- The exchange protocol described above is terminated by the control processor performing a dummy read of the mailbox ($\overline{CS}$ = 0, SR/$\overline{W}$ = 1) but with $\overline{RS}$ in the high state.
- The RDYOIN flag within the TS75240 is cleared to 0 by this dummy read of the mailbox and the TS75240 now has access to R-IN and R-OUT registers within the mailbox.
- The control processor gives the bus back to the TS75240 by negating $\overline{CS}$ ($\overline{CS}$ = 1).
  The same type of exchanges must be implemented for each transmit and receive Baud period.

Notes : 1. Processings of the two different words exchanged during each mailbox transfer must be performed after a complete mailbox transfer is implemented (i.e. the mailbox transfer must be performed as fast as possible so as to respect the real-time task scheduling of the TS75240).

2. The internal RDYOIN flag indicates the property of the mailbox :
   - 0 for the TS75240,
   - 1 for the control processor.
   As this flag can be set only by the TS75240 and reset only by the control processor, this means that one of these two devices gives the control of the mailbox back to the other when it finishes to use it. **The control processor and the TS75240 can not request the mailbox at the same time,** but can only wait for the other to give it back.

Figure 2.


CONTROL PROCESSOR
(MASTER)
TS 75240
(SLAVE)
MAILBOX AVAILABLE
asserts : IRQ (IRQ = 0)
RDYOIN (RDYOIN = 1)
detects : IRQ = 0
applies : CS = RS = 0
SR/W = 1
detects : CS = RS = 0
negates : IRQ (IRQ = 1)
detects : IRQ = 1
MAILBOX ACCESS
3 reads
(first, second and third status bytes)
applies : SR/W = 0
3 writes
(first, second and third command bytes)
END OF MAILBOX ACCESS
applies : CS = 0, RS = SR/W =1
applies : CS = RS = SR/W =1
detects : CS =0, RS = 1
negates : RDYOIN (RDYOIN = 0)
NOTE : For proper timings, refer to the TS 7524 data sheet
M88AN5-02

3. ARCHITECTURE EXAMPLES

The TS75240 asynchronous parallel port with its associated mailbox transfer allows the TS7524 chipset to be interfaced to a control processor straightforwardly and with a minimum of interface circuitry.

3.1. WITH THE ADDRESS/DATA BUS

Examples of this type of architecture are given figure 3 (with the **ST9030** microcontroller) and figure 4 (with the **INTEL 8032** microcontroller).

Figure 3.

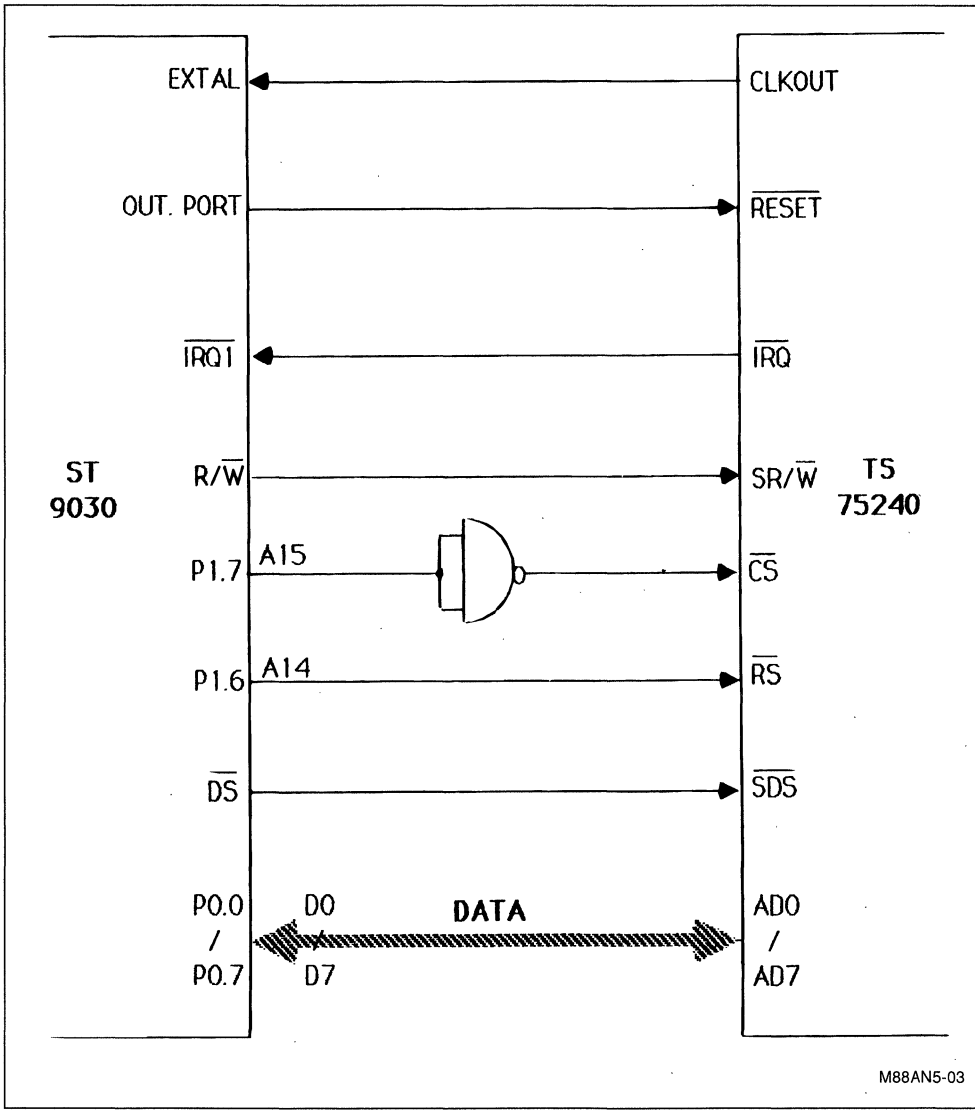
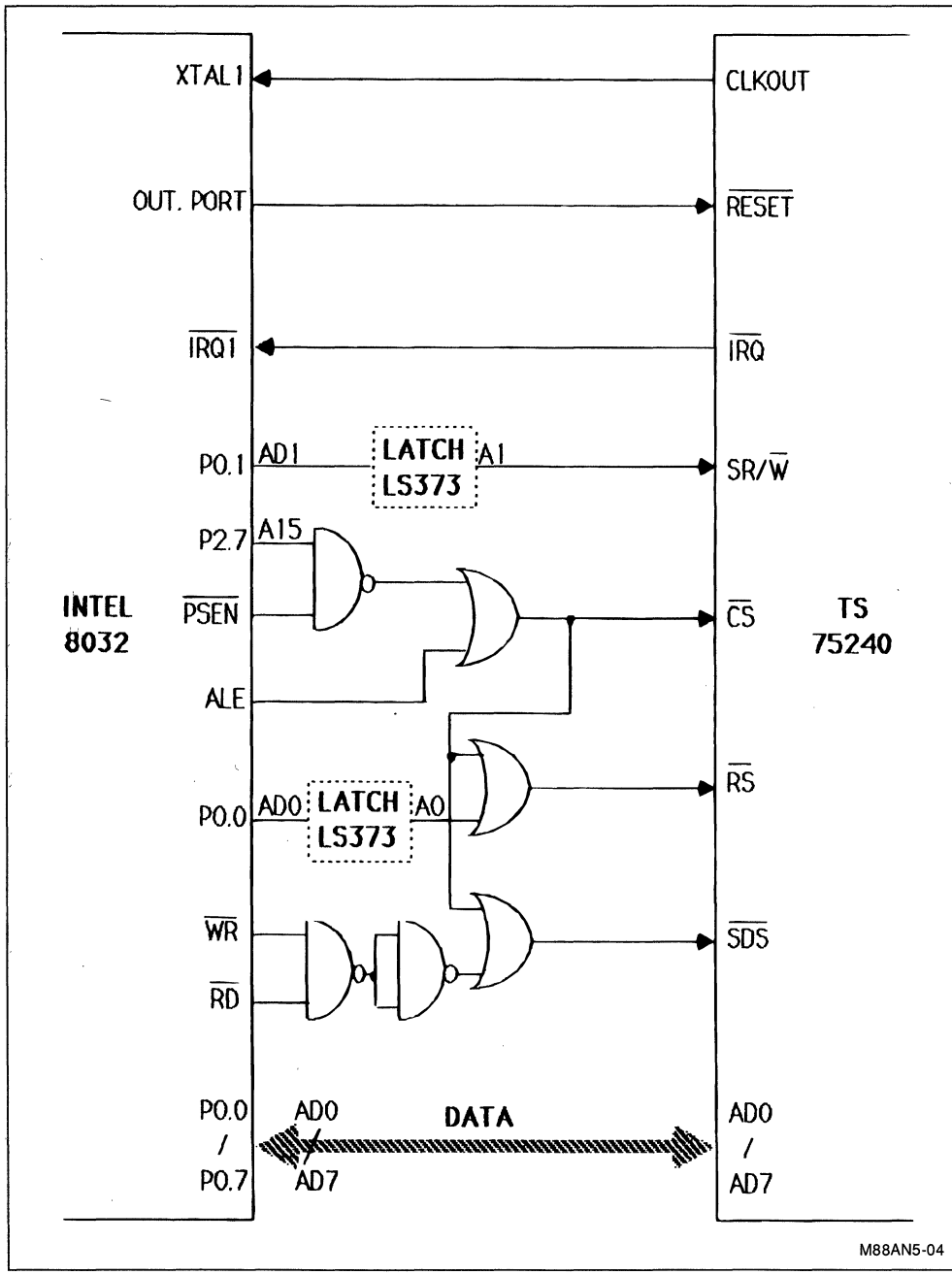


Figure 4.



Note : An assembly program example is given in appendix C.

3.2. WITH A GENERAL PURPOSE I/O PORT

Example of this type of architecture is given figure 5 with the **HITACHI 63701** microcontroller.

4. PROGRAMMING EXAMPLES

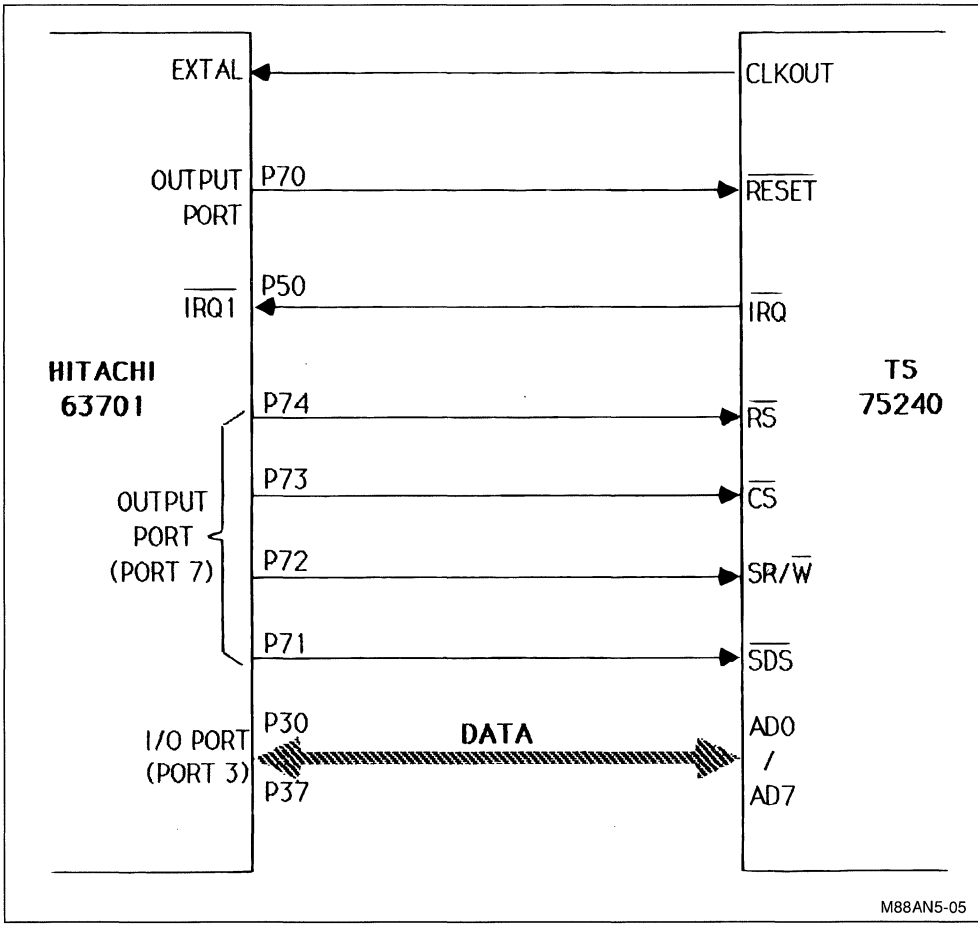
4.1. TRANSMIT THE 1800 Hz GUARD TONE IN V.22 WITH 0 dB ATTENUATION

- 1st transmit command byte : $32 (1800 Hz, V.22)
- 2nd transmit command byte : $00 (0 dB attenuation, answer)
- 3rd transmit command byte : $00 (transmit enabled).

4.2. TRANSMIT THE 550 Hz GUARD TONE IN V.22 BIS WITH 10 dB ATTENUATION

- 1st transmit command byte : $11 (550 Hz, V.22 bis)
- 2nd transmit command byte : $0A (10 dB attenuation, answer)
- 3rd transmit command byte : $00 (transmit enabled).

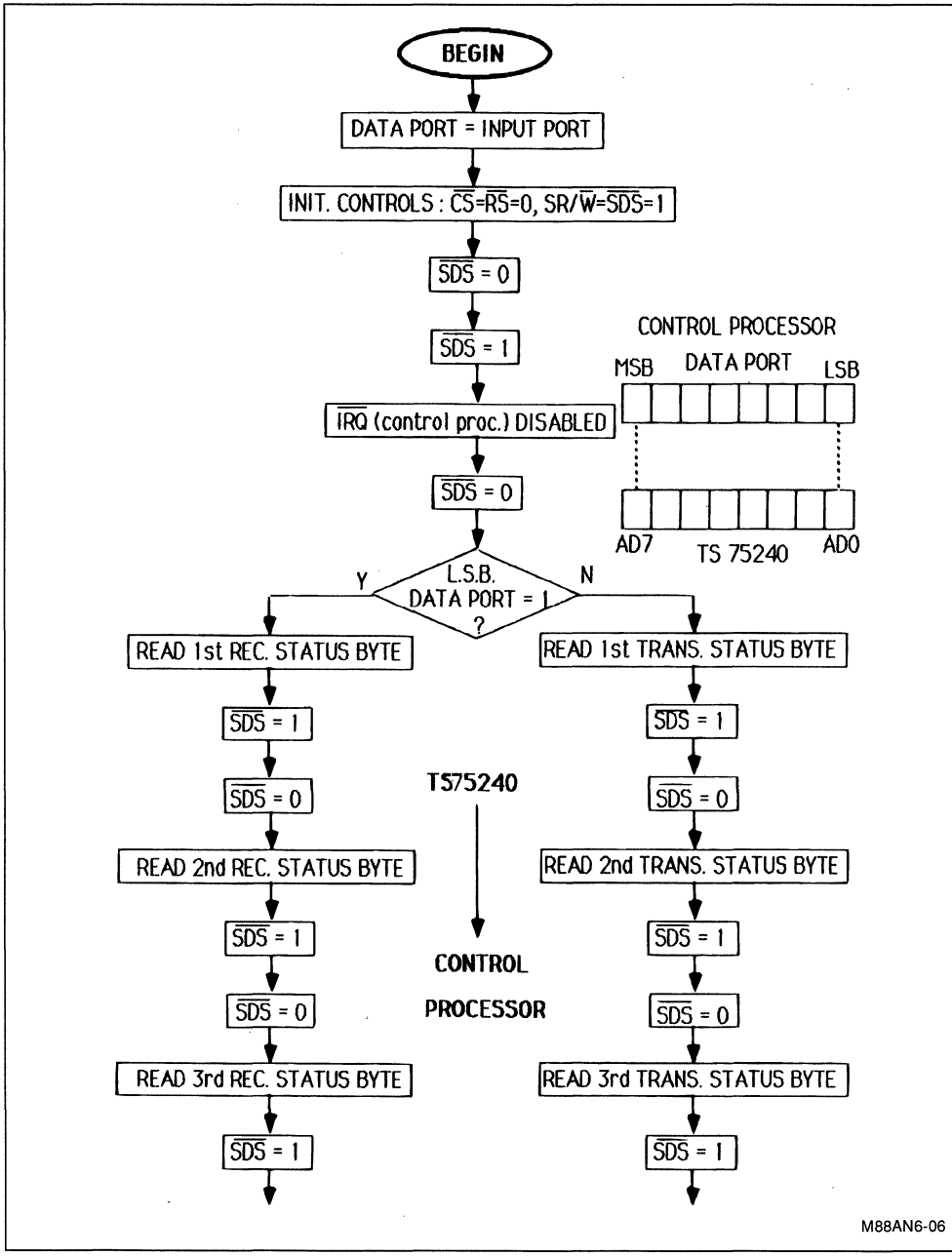
Figure 5.



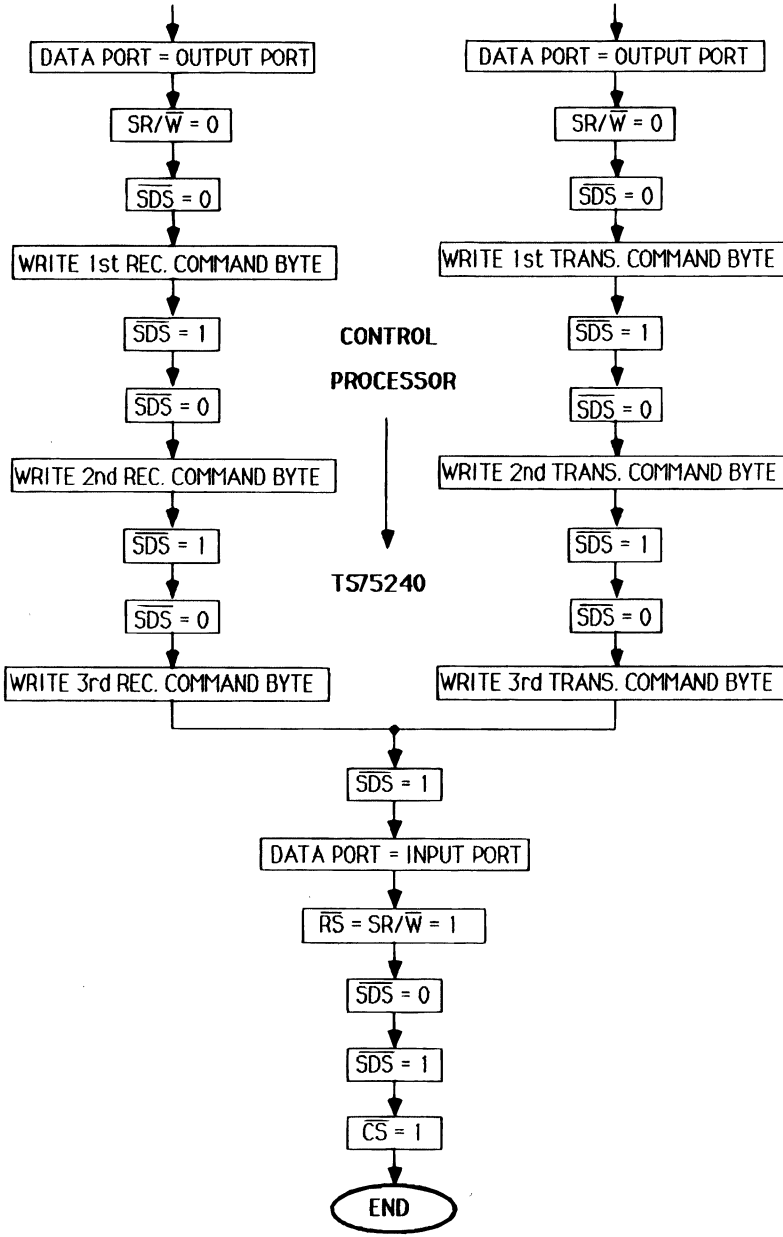
Note : A flowchart and an assembly program example are given in appendix A and B.

APPENDIX A

MAILBOX EXCHANGE INTERRUPT ROUTINE FLOWCHART (with I/O port architecture)



MAILBOX EXCHANGE INTERRUPT ROUTINE FLOWCHART (continued)



M88AN5-06

APPENDIX B

This programming example in 63701 Assembler language is related to the circuit shown in figure 5 and gives an example of mailbox exchange interrupt subroutine.

```
IRQ1    LDD     #$E7E5
        STAA    PORT7     (CS = RS = 0, SDS = SR/W = 1)
        STAB    PORT7     (SDS = 0)   (dummy
        STAA    PORT7     (SDS = 1)    read)
        STAB    PORT7     (SDS = 0)
        LDAA    PORT3
        LSRA

        IR RESULT IS C    ("0" if transmit, "1" if receive)
                LDAA    PORT3     (read 1st receive
                STAA    STARE1     status byte)
                LDAA    #$E7
                STAA    PORT7     (SDS = 1)
                STAB    PORT7     (SDS = 0)
                LDAA    PORT3     (read 2nd receive
                STAA    STARE2     status byte)
                LDAA    #$E7
                STAA    PORT7     (SDS = 1)
                STAB    PORT7     (SDS = 0)
                LDAA    PORT3     (read 3rd receive
                STAA    STARE3     status Byte)
                LDAA    #$E7
                STAA    PORT7     (SDS = 1)

                LDAB    #$E3
                STAB    PORT7     (SR/W = 0)
                LDAA    #$FF
                STAA    P3DDR     (PORT3 = OUTPUT)
                LDAB    #$E1
                STAB    PORT7     (SDS = 0)

                LDAA    COMRE1    (write 1st receive
                STAA    PORT3      command byte)
                LDAA    #$E3
                STAA    PORT7     (SDS = 1)
                STAB    PORT7     (SDS = 0)
                LDAA    COMRE2    (write 2nd receive
                STAA    PORT3      command byte)
                LDAA    #$E3
                STAA    PORT7     (SDS = 1)
                STAB    PORT7     (SDS = 0)
                LDAA    COMRE3    (write 3rd receive
                STAA    PORT3      command byte)
        ELSE
                LDAA    PORT3     (read 1st transmit
                STAA    STATR1     status byte)
                LDAA    #$E7
                STAA    PORT7     (SDS = 1)
                STAB    PORT7     (SDS = 0)
                LDAA    PORT3     (read 2nd transmit
                STAA    STATR2     status byte)
```

APPENDIX B(continued)

```
        LDAA    #$E7
        STAA    PORT7    (SDS = 1)
        STAB    PORT7    (SDS = 0)
        LDAA    PORT3    (read 3rd transmit
        STAA    STATR3    status byte
        LDAA    #$E7
        STAA    PORT7    (SDS = 1)

        LDAB    #$E3
        STAB    PORT7    (SR/W = 0)
        LDAA    #$FF
        STAA    P3DDR    (PORT3 = OUTPUT)
        LDAB    #$E1
        STAB    PORT7    (SDS = 0)

        LDAA    COMTR1   (write 1st transmit
        STAA    PORT3     command byte)
        LDAA    #$E3
        STAA    PORT7    (SDS = 1)
        STAB    PORT7    (SDS = 0)
        LDAA    COMTR2   (write 2nd transmit
        STAA    PORT3     command byte)
        LDAA    #$E3
        STAA    PORT7    (SDS = 1)
        STAB    PORT7    (SDS = 0)
        LDAA    COMTR3   (write 3rd transmit
        STAA    PORT3     command byte)

ENDS

LDD     #$E300
STAA    PORT7            (SDS = SR/W = 1)
STAB    P3DDR            (PORT3 = INPUT)
LDD     #$F7F5
STAA    PORT7            (RS = 1)
STAB    PORT7            (SDS = 0)
STAA    PORT7            (SDS = 1)
LDAA    #$FF
STAA    PORT7            (CS = 1)
RTI
```

Note : See note appendix C.

APPENDIX C

This programming example in 8032 Assembler language is related to the circuit shown in figure 4 and gives an example of mailbox exchange interrupt subroutine.

The TS75240 is accessed at three address locations :

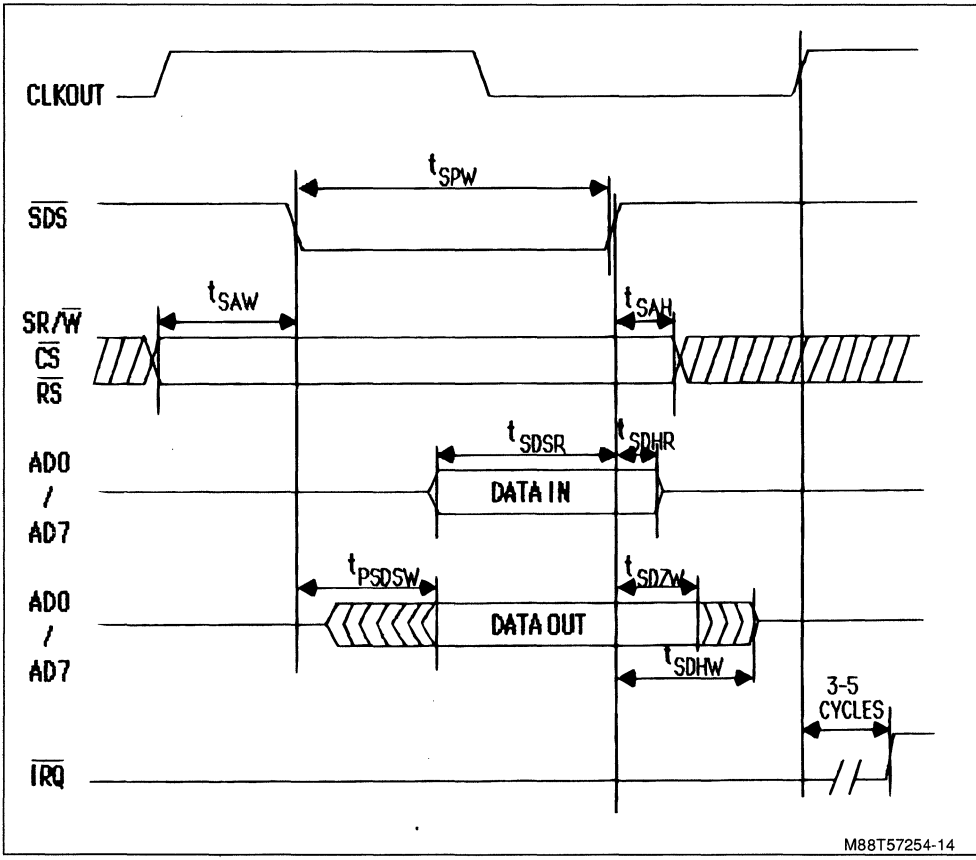
```
        DSPREA  EQU   8002W   Read address with RS = 0
        DSPWRI  EQU   8000H   Write address (RS = 0)
        DSPEND  EQU   8003H   Read address with RS = 1

IRQ1    MOV     DPTR, #DSPREA          (read of TS75240)
        CLR     EA                     (interrupt disabled)
        MOVX    A, @DPTR               (dummy read)
        MOVX    A, @DPTR               (read the first status byte)
        RRC     A
        JNC     IRQ11                  (jump if "0" (transmit))
        RLC     A
        MOV     STARE1, A              (read 1st rec. status byte)
        MOVX    A, @DPTR
        MOV     STARE2, A              (read 2nd rec. status byte)
        MOVX    A, @DPTR
        MOV     STARE3, A              (read 3rd rec. status byte)
        MOV     DPTR, #DSPWRI          (write of TS75240)
        MOV     A, COMRE1              (write 1st rec. command byte)
        MOVX    @DPTR, A
        MOV     A, COMRE2              (write 2nd rec. command byte)
        MOVX    @DPTR, A
        MOV     A, COMRE3              (write 3rd rec. command byte)
        MOVX    @DPTR, A
        JMP     IRQ12
IRQ11   RLC     A
        MOV     STATR1, A              (read 1st tra. status byte)
        MOVX    A, @DPTR
        MOV     STATR2, A              (read 2nd tra. status byte)
        MOVX    A, @DPTR)
        MOV     STATR3, A              (read 3rd tra. status byte)
        MOV     DPTR, #DSPWRI          (write of TS75240)
        MOV     A, COMTR1              (write 1st tra. command byte)
        MOVX    @DPTR, A
        MOV     A, COMTR2              (write 2nd tra. command byte)
        MOVX    @DPTR, A
        MOV     A, COMTR3              (write 3rd tra. command byte)
        MOVX    @DPTR, A
IRQ12   MOV     DPTR, #DSPEND          (RS = 1)
        MOVX    A, @DPTR               (dummy read)
        SETB    EA                     (interrupt enabled)
        RETI
```

Note : STARE1, STARE2 and STARE3 (resp. STATR1, STATR2, STATR3) are microcontroller RAM locations used to save the receive (resp. transmit) status bytes read from the TS75240.
COMRE1, COMRE2 and COMRE3 (resp. COMTR1, COMTR2, COMTR3) are microcontroller RAM locations which contains the receive (resp. transmit) command bytes to be written into the TS75240.

APPENDIX D

SYSTEM BUS TIMING CHARACTERISTICS



Symbol	Parameter	Min.	Max.	Unit
t_{SPW}	$\overline{SDS}$ Pulse Width	60		ns
t_{SAW}	SR/$\overline{W}$, $\overline{CS}$, $\overline{RS}$ Set-up Time	20		ns
t_{SAH}	SR/$\overline{W}$, $\overline{CS}$, $\overline{RS}$ Hold After $\overline{SDS}$ High	5		ns
t_{SDSR}	Data Set-up Time, Read Cycle	20		ns
t_{SDHR}	Data Hold Time, Read Cycle	5		ns
t_{PSDSW}	Data Propagation Delay, Write Cycle		35	ns
t_{SDHW}	Data Hold Time, Write Cycle	10		ns
t_{SDZW}	$\overline{SDS}$ High to Data High Impedance, Write Cycle		40	ns

V_{CC} = + 5 V ± 5 %, 0 °C < Tamb < + 70 °C unless otherwise specified.

APPENDIX E

TRANSMIT/RECEIVE STATUS WORDS

TRANSMIT STATUS WORD

BIT	STATR1	STATR2	STATR3
0	Transmit (0)	Reserved	Reserved
1	Reserved		
2			
3			
4			
5			
6			
7			

RECEIVE STATUS WORD

BIT	STARE1		STARE2	STARE3			
0	Receive (1)		Reserved	Reserved			
1	D0	Data Before Descrambling (Q.A.M. , D.P.S.K.)		D0	Data After Descr. (Q.A.M., D.P.S.K.)	D0	Data (F .S.K.)
2	D1			D1		D1	
3	D2			D2		D2	
4	D3		Equalization Status	D3		D3	
5	Reserved		$\overline{\text{Signal Quality}}$	1		D4	
6	S1 Sequence		$\overline{\text{Carrier Detect}}$	1		D5	
7	$\overline{\text{S1 Sequence or Call Progress Tone Det}}$		Reserved	$\overline{\text{Answer Tone Detect}}$			

Note : In QAM and DPSK modes, both for the data after and before descrambling, the unused bits are set to "1" by the TS7524.

APPENDIX E (continued)

TRANSMIT COMMAND WORD

BIT	COMTR1	COMTR2	COMTR3				
0	Trans. Mode Selection	Transmit Attenuation	Transmit (0)				
1	0000 : Modem Disabled 0001 : V.22 Bis 0010 : V.22 0011 : B212 0100 : V.23 0101 : V.21 0110 : Bell 103 0111 : D.T.M.F.		D0	DPSK	QAM	FSK	DTMF
2			D1				
3			D2	0			
4	Transmit Signalling 00 : Signalling Dis. 01 : 550 Hz 11 : 1800 Hz		D3	0			
5		Scrambler (ON/$\overline{\text{OFF}}$)	D4	0	0		0
6	**Reserved**	**Reserved**	D5	0	0		0
7	$\overline{\text{answ}}$/ori or DTMF	V.22 Binary Rate Select or DTMF	$\overline{\text{Transmit Enable}}$				

Note : All the "RESERVED" bits must be cleared to "0" by the user.

RECEIVE COMMAND WORD

BIT	COMRE1	COMRE2	COMRE3
0	REC. Mode Selection	**Reserved**	Receive (1)
1	0000 : Modem Disable 0001 : V.22 Bis 0010 : V.22 0011 : B212 0100 : V.23 0101 : V.21 0110 : Bell 103 0111 : CALL/PROG. Tone		**Reserved**
2			
3			
4	Answer Tone Selection		
5	Tx Synchronization	Descrambler (ON/$\overline{\text{OFF}}$)	
6	Carrier Detect Level	**Reserved**	
7	$\overline{\text{Answer}}$/originate	V.22 Binary Rate Select	

Note : All the "RESERVED" bits must be cleared to "0" by the user.

USING A TS7515 SINGLE CHIP V.22/BELL 212A MODEM AROUND 80C51 MICROCONTROLLER

1. INTRODUCTION

This application note must be used in addition with the TS7515 data sheet to show the way to use this single chip V.22/Bell 212A modem around the 80C51 microcontroller. The goal of this note is not to explain the block diagram of a complete modem board but rather to give some indications about using and interfacing the TS7515 and the 80C51 in the best way.

2. DESCRIPTION

In these typical applications, the TS7515 is used in conjonction with a 80C51 microcontroller and an EF6850 U.A.R.T.

The D.T.M.F. dialing is performed through the TS7515 external pin (EXI) via the EFG7189 D.T.M.F. dialer.

The CMOS 4024 circuit is used to generate the different clocks required for the "call progress" mode. In this mode, by programming the $\overline{RTS}$ pin to 5 V and the A/S pin to 0 V, the TS7515 behaves like a clock programmable receive filter whose center frequency can be calculated through the following formula :

$$Fc = \frac{Fm \times TxSCLK}{210}$$

Where : Fc is the filter center frequency (in Hz)
Fm is the carrier frequency (in Hz) in modem mode (i.e 1200 or 2400 Hz according to A/O pin : Answer or Originate)

TxSCLK is the filter sampling clock (in Hz).

In this mode, the $\overline{DCD}$ pin behaves like a fast carrier detect and the filter bandwith so programmed is the initial bandwith of receive filter (400 Hs in answer or originate mode) multiplied by the clock ratio.

Example : To detect the 440 Hz dialing invite tone, the TS7515 will have to be programmed in answer mode (A/O = 0) and the sampling clock to be applied to it will be :

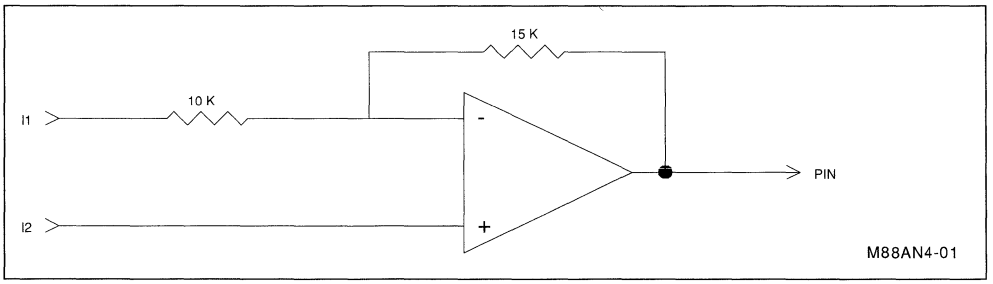
$$TxSCLK = \frac{210 \times 440}{1200} = 76.8 \text{ kHz}$$

Which is the crystal frequency (4,9152 MHz) divided by 64 (2^6).

In this case the filter bandwith will be : 145 Hz

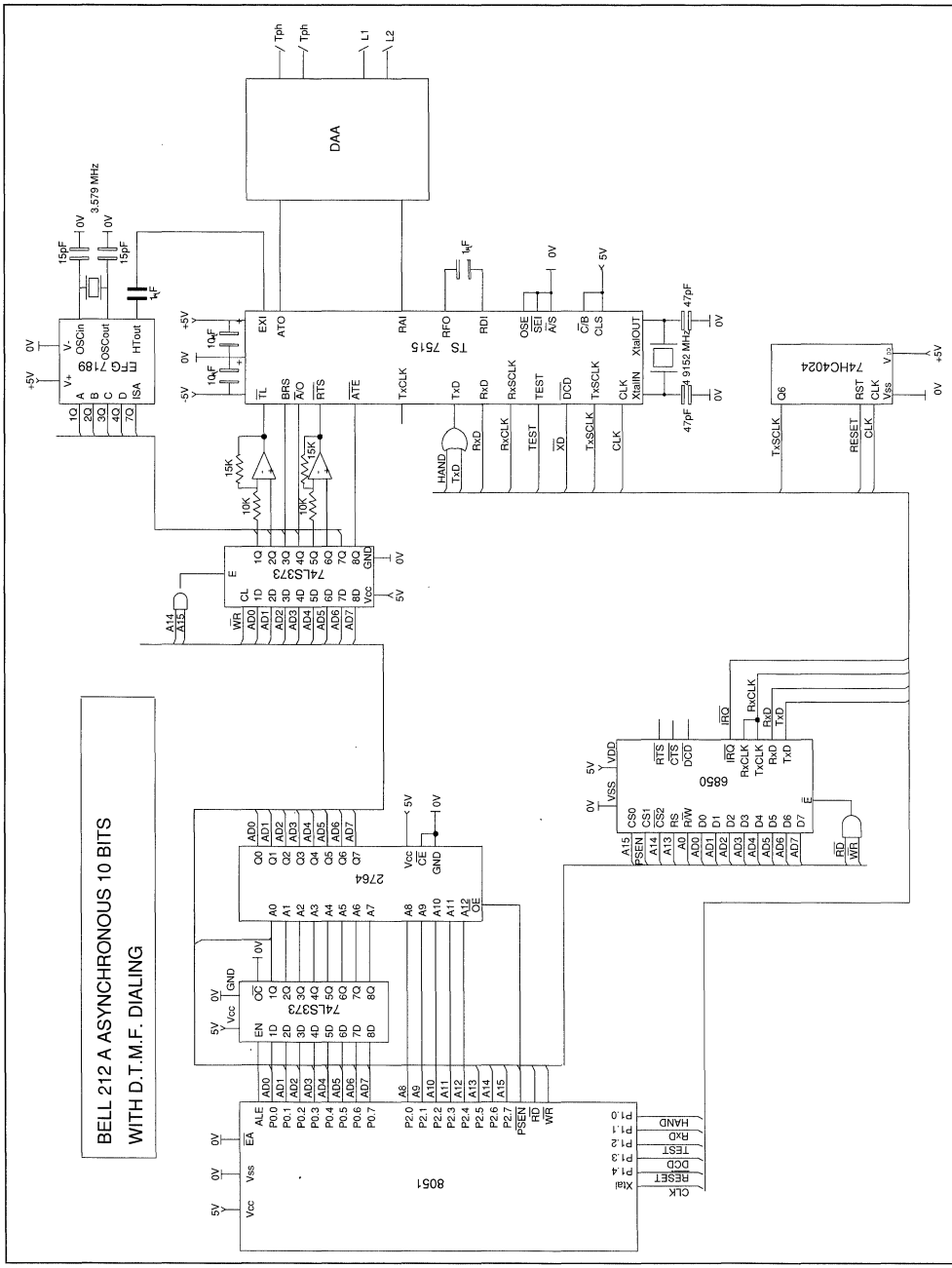
$$(400 \times \frac{440}{1200})$$

The three states of the TS7515 $\overline{RTS}$ and $\overline{TL}$ pins are performed through a dual general purpose operational amplifier according to following way :



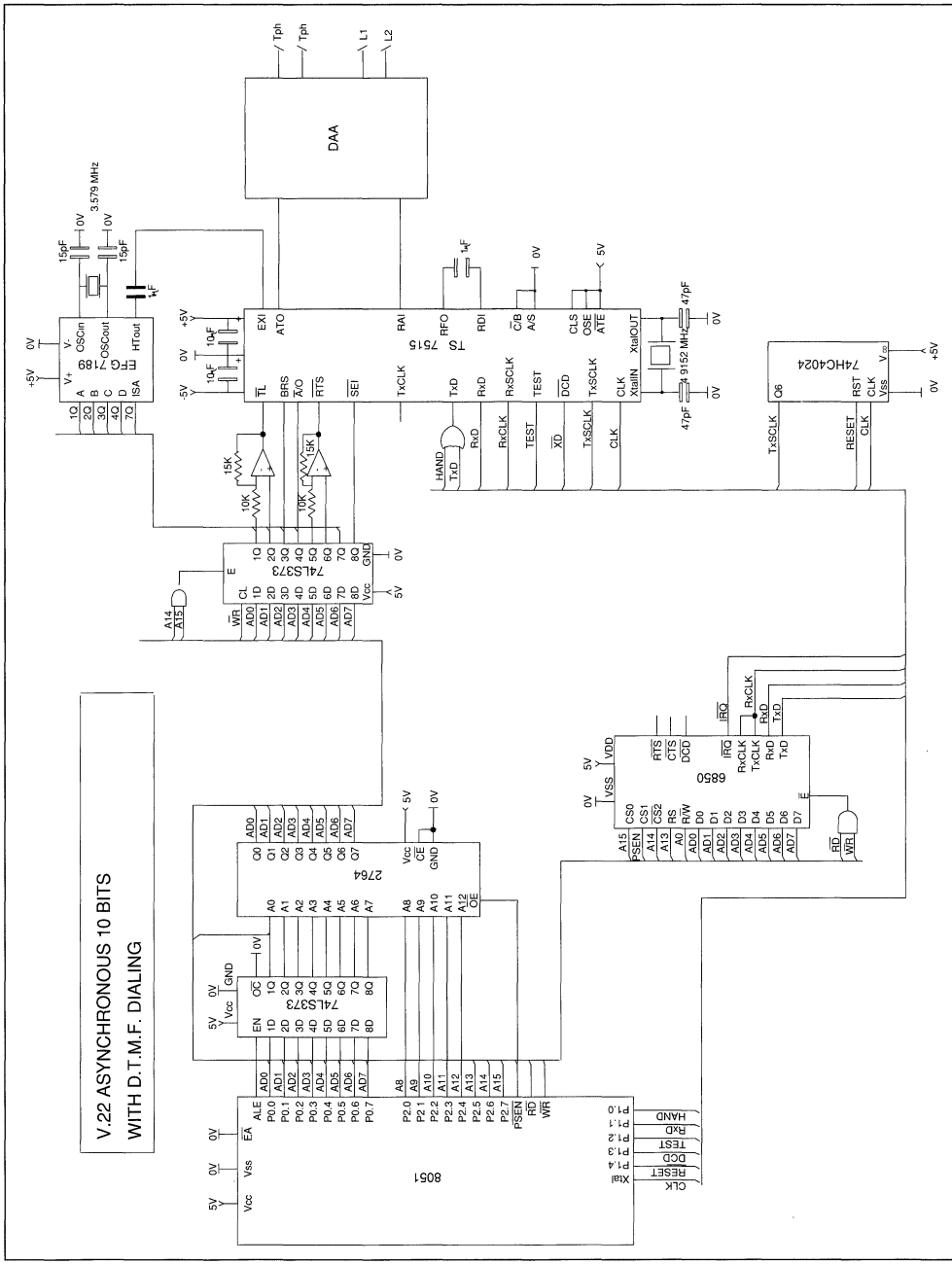
I1	I2	Pin
0 V	0 V	0 V
0 V	+ 5 V	+ 5 V
+ 5 V	0 V	– 5 V
+ 5 V	+ 5 V	Undefined

BELL 212A ASYNCHRONOUS 10 BITS WITH D.T.M.F. DIALING



(*) All circuits assuming to be uncoupled by 100µF capacitor.

V.22 ASYNCHRONOUS 10 BITS WITH D.T.M.F. DIALING



(*) All circuits assuming to be uncoupled by 100µF capacitor.

HOW TO ESTABLISH A CONNECTION WITH AN UNKNOWN MODEM USING CCITT V.22 PROTOCOL

INTRODUCTION

To establish a connection to a data base per the CCITT V.22 specification implies respecting the originate and answer (manual and automatic) handshake sequences described by the flowcharts in figures 1 and 2.

ORIGINATE MODE (figure 1)

In the originate mode ($\overline{A}/O = 1$), the modem transmits on the low frequency channel and receives on the higher frequency channel. Once the modem has established a connection to the line (initialization), it applies an ON condition to circuit 107 in accordance with V.25 recommendation. The modem then remains silent until unscrambled binary 1 * (TEST = 1) is detected for 155 50ms. After waiting for 456 10ms, the modem transmits scrambled binary 1 ($\overline{RTS} = 0$, $\overline{SEI} = 0$, $\overline{TxD} = 1$). In parallel, upon detecting scrambled binary ($RxD = 1$) within 270 ±40ms, the modem turns circuit 109 ON, then waits a further 765 ± 10ms. Circuit 106 then responds to the condition of circuit 105 (supposedly set to the ON condition during initialization).

ANSWER MODE (figure 2)

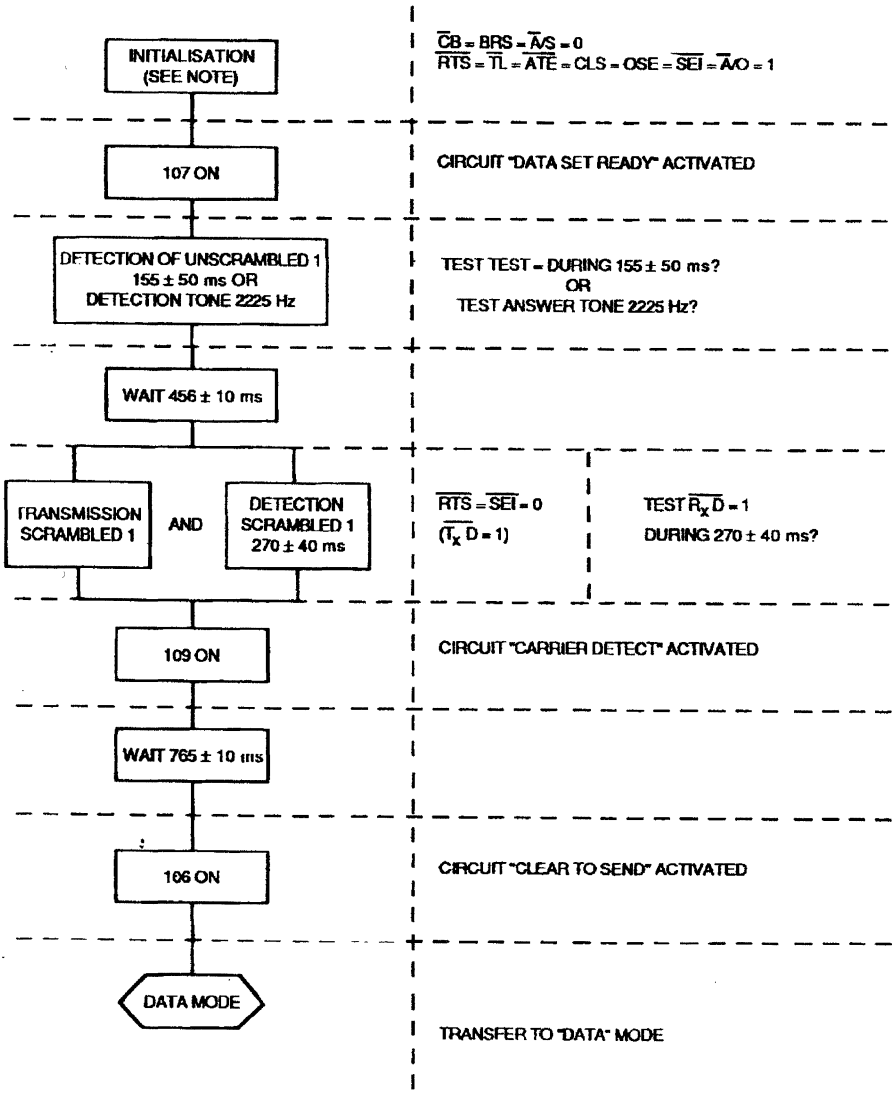
In the answer mode ($\overline{A}O = 0$), the modem transmits on the high frequency channel and receives on the low frequency channel. Two cases may occur : either answer is manual or automatic. In the automatic answer mode, the modem connects to the line (initialization) and, after a silence of 2150 ±300ms, transmits ($\overline{RTS} = 0$) the 2100Hz answer tone ($\overline{ATE} = 0$) during 3300 ±700ms. After a period of silence ($\overline{RTS} = \overline{ATE} = 1$) of 75 ± 20ms, the modem applies an ON condition to circuit 107 following the V.25 recommendation. The action corresponds to connecting the modem to the line in the manual mode. The manual mode differs from the automatic mode during the three sequences : silence, answer tone, silence. The modem transmits ($\overline{RTS} = 0$) unscrambled ($\overline{SEI} = 1$) binary 1 * ($\overline{TxD} = 1$). In parallel, upon detecting scrambled binary 1 ($RxD = 1$) during 270 ± 40ms, the modem transmits scrambled ($\overline{SEI} = 0$) binary 1 ($\overline{TxD} = 1$) and, after waiting for 765 ± 10ms, turn ON circuit 109. Circuit 106 then responds to the condition of circuit 105 (supposedly set to ON condition during initialization).

CONCLUSION

The two handshake sequences described above are theoretical. Many modems do not follow this convention completely. We must match these sequences to the unknown modem we want to connect to. The difficulties of establishing a connection is not a problem of hardware circuits but a handshake problem between the two circuits.

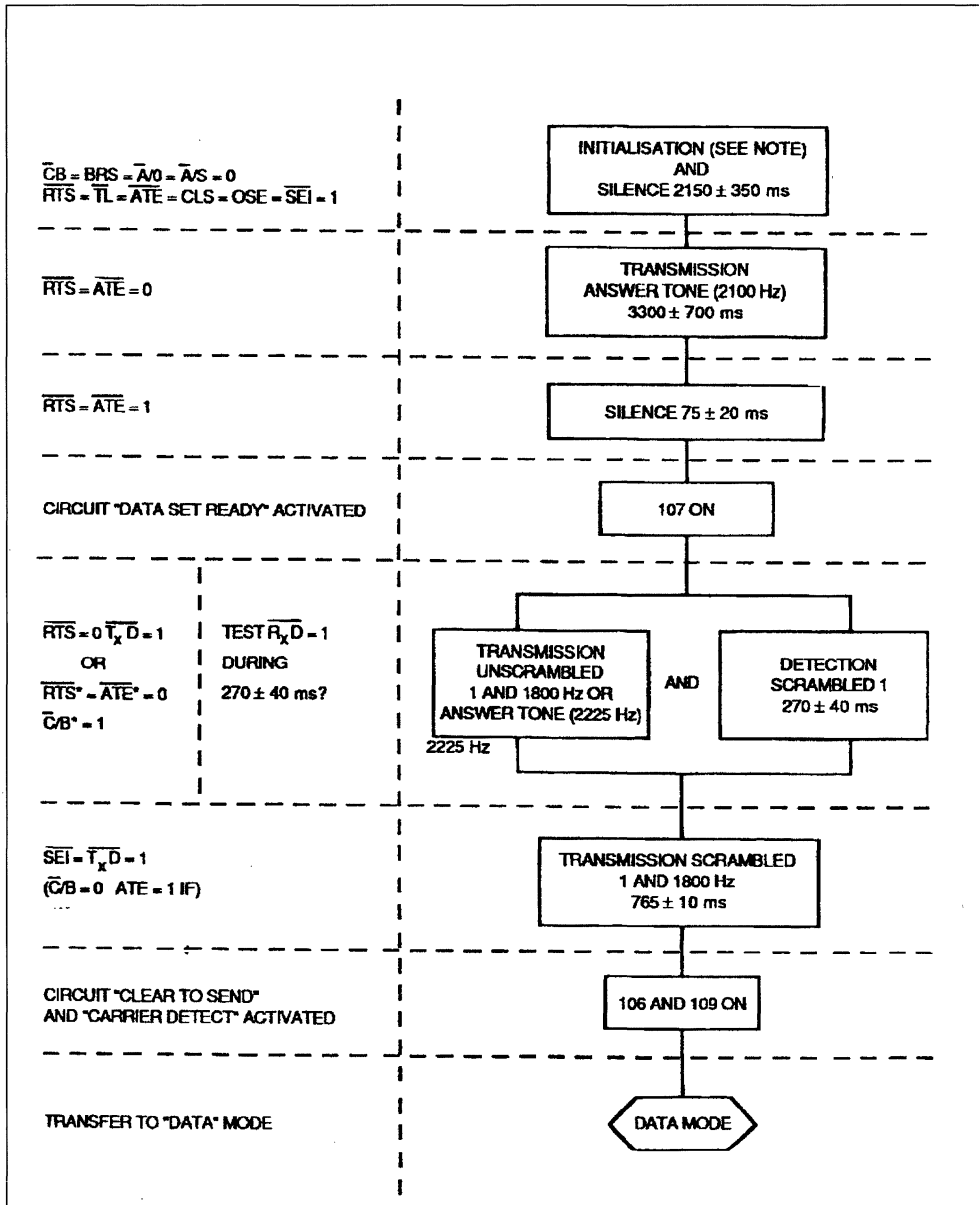
* In certain countries, unscrambled binary 1 (TEST = 1) replaced by an answer tone of 2225Hz.

Figure 1 : Handshake Sequence in V.22 (Originate Mode).



Note : Assumed to be in 1200bps, asynchronous, 10 bits, with maximum overspeed authorized and not in test loop mode.

Figure 2 : Handshake Sequence in V.22 (Automatic Answer Mode).



Note : Assumed to be in 1200bps, asynchronous, 10 bits, with maximum overspeed authorized and not in test loop mode.

APPLICATION GUIDE TO THE USE OF THE TS7515 SINGLE CHIP MULTI-STANDARD DPSK AND FSK MODEM

INTRODUCTION

This application note is a complete guide to the realization of a multi-standard modem by using the TS7515 FSK and DPSK monochip from SGS-THOMSON Microelectronics.

The note successively describes the main characteristics of the TS7515 and its functional operation. Then a detailed background of V.22, Bell 212A and Bell 103 standards is given before pating in application the advanced features of the device. The microprocessor software modules necessary to a complete application are also provided with general precautions hints.

TABLE OF CONTENTS

1 - MAIN CHARACTERISTICS OF TS7515

1.1 - General Features

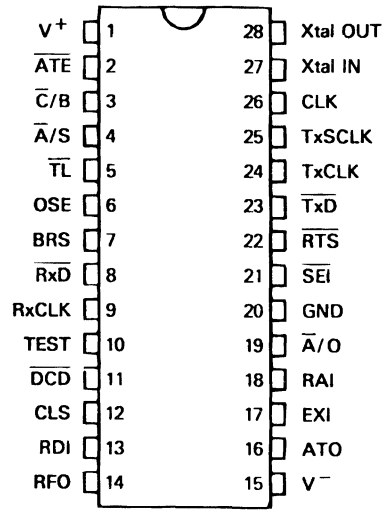
The TS7515 is a single chip voice-band modem compatible with BELL 212A, CCITT V.22 A and B standard requirements.

- Includes both Receive and Transmit Filters.
- Designed using analog and digital techniques.
- Requires standard 4.9152 MHz crystal oscillator.
- Buffered clock output for microprocessor-based applications.
- Low power consumption - CMOS technology.
- High adjacent channel signal rejection.
- Fixed equalization in transmission and reception.
- Maintenance loop : type 2 and 3.
- Carrier detect output.
- CCITT and BELL answer tones.
- 1200 and 600 bps synchronous operation in DPSK mode.
- 1200 and 600 bps + 1 %, – 2.5 % or + 2.3 %, – 2.5 % asynchronous operation in DPSK mode.
- 8-, 9-, 10-, 11-bit character format in asynchronous mode of operation.
- 0 to 300 bps data rate in FSK operation.
- Break signal supervision.
- Special line monitoring facilities.

Main Operating Modes

- BELL 212A/BELL 103/V.22 Standard Selection.
- Answer tone selection.
- Fallback Mode selection.
- Originate/Answer Channel Selection.
- Synchronous/Asynchronous Mode Selection.
- Character length selection in asynchronous mode.
- Overspeed Selection.
- Scrambler Selection.
- Guard tone selection in V.22 mode.
- Analog/Digital test loop Selection.

1.2 - Pin Configuration



M88TS7515-01

1.3 - Description of Pins

Pin 1 : V^+

Positive power supply : 5 V ± 5 %

Pin 2 : $\overline{\text{ATE}}$ ($\overline{\text{Answer Tone Enable}}$)

This pin allows to configure the device in either modem mode or as a transmitter of pure frequency (answer tone).

- A logic low (0) signal applied to this pin causes the device to output through ATO (Analog Transmit Output) pin a pure sinewave whose frequency depends on the programming of $\overline{\text{C}}$/B ($\overline{\text{CCITT}}$/BELL) pin.
- Inversely, a logic high (1) on $\overline{\text{ATE}}$ pin will configure the device in modem mode.

Pin 3 : $\overline{\text{C}}$/B ($\overline{\text{CCITT}}$/BELL)

This three-state input selects one of CCITT V.22 and BELL 212A standards.

Pin 4 : $\overline{\text{A}}$/S ($\overline{\text{Asynchronous}}$/Synchronous)

In DPSK mode, this three-state input selects Asynchronous or Synchronous mode of operation. In asynchronous operation, it also provides the character length selection.

Pin 5 : $\overline{\text{TL}}$ ($\overline{\text{Test Loop}}$)

Three-state input pin for the selection of Test loop 2 or Test loop 3.

Pin 6 : OSE (Over Speed Enable)

In asynchronous mode, this input selects one of two possible over speed configurations available in CCITT standard recommendations.

Pin 7 : BRS (Binary Rate Selection)

This pin is used for the selection of binary rate as follows :

- a logic low (0) signal on this input configures the device to receive and transmit data at 1200 bps,
- a logic high (1) signal applied to this input enables the circuit to receive and transmit data at 600 bps in CCITT mode or 300 bps in BELL 212A mode.

Pin 8 : $\overline{\text{RxD}}$ ($\overline{\text{Receive Data}}$)

This output provides binary data provided by the demodulator.

Pin 9 : RxCLK (Receive Clock)

This output corresponds to Modem's receive bit clock.

- In synchronous mode, the clock is synchronized with data output through $\overline{\text{RxD}}$ pin.
- In asynchronous mode, this pin delivers a clock rate 16 times faster than modem's modulation rate.

Pin 10 : TEST

The output signal is available on this pin before passing through the descrambler. This pin is intended for "handshake" and "remote loop request" purposes.

Pin 11 : $\overline{\text{DCD}}$ ($\overline{\text{Data Carrier Detect}}$)

This pin will go low when device receives a signal level higher than – 43 dBm on RDI (Receive Demodulator Input) pin and goes high if the signal level is lower than – 48 dBm. The – 43 dBm to – 48 dBm range provides a 5 dB hysteresis for the initiation of $\overline{\text{DCD}}$ function.

Pin 12 : CLS (Character Length Selection)

In conjunction with $\overline{\text{A}}$/S pin, this input selects the character length.

Pin 13 : RDI (Receive Demodulator Input)

This input receives analog signals and directs them to comparators associated with demodulator and signal detector. The signal is also applied to various demodulation circuitry.

Pin 14 : RFO (Receive Filter Output)

The analog signal first goes through various bandpass and equalization filters and is then available at this output pin.

Access to this pin simplifies in particular the device test procedures.

While designing an application, and as far as possible, the P.C. Board layout must be so arranged that RFO output could be coupled to RDI input terminal through a single capacitor as close as possible to the device.

Pin 15 : V^-

Negative power supply : – 5 V ± 5 %

Pin 16 : ATO (Analog Transmit Output)

In conjunction with analog applied to $\overline{\text{ATE}}$ ($\overline{\text{Answer Tone Enable}}$) terminal, this output delivers either a modulated carrier or an answer tone.

Pin 17 : EXI (External Tone Input)

With $\overline{\text{RTS}}$ ($\overline{\text{Request To Send}}$) terminal at logic "1", this analog input accepts an external tone which will be first filtered and then routed to ATO (Analog Transmit Output) terminal.

Pin 18 : RAI (Receive Analog Input)

This is input terminal to the receive filter. Signals received via line are applied to this pin.

Pin 19 : $\overline{A}$/O ($\overline{\text{Answer/Originate}}$)

Signal level applied to this pin selects modem's operating mode (Answer or Originate) as follows :

A "0" applied to this pin selects Answer mode.

A "1" applied to this pin selects Originate mode.

Note : In answer modem, upper channel (2400 Hz) and guard tone (1800 Hz) may be transmitted simultaneously, provided that the guard tone power level is 6 dB less than that of modulated 2400 Hz signal. Transmission of this guard tone is enabled through C/B terminal.

Pin 20 : GND

This is the ground terminal common to all digital and analog sections of TS 7515.

Pin 21 : $\overline{\text{SEI}}$ ($\overline{\text{Scrambler Enable Input}}$)

This input enables the scrambler operation.

A "0" applied to this input enables the scrambler.

A "1" applied to this input disables the scrambler.

Pin 22 : $\overline{\text{RTS}}$ ($\overline{\text{Request To Send}}$)

With a logic level "1" applied to this pin, the device outputs through ATO pin the signal delivered by EXI terminal.

With a logic level "0" on this pin, the circuit delivers through ATO terminal a signal whose characteristics are determined by the state of $\overline{\text{ATE}}$ terminal.

With this pin at logic level "-1", the TS 7515 is configured as a programmable filter. That is, TxSCLK input becomes a clock input running at a frequency equal to twice the sampling frequency of the receive filter, that may be assigned to upper or lower channel, in accordance with signal level applied to A/O terminal. In this configuration of RTS, the signal originated through DCD terminal is the exact representation of the tone envelope detected via line.

Pin 23 : $\overline{\text{TxD}}$ ($\overline{\text{Transmit Data}}$)

This input receives the data transmitted by terminal.

In DPSK and FSK operating modes, these data bits (1 and 0) determine the phase (for DPSK) or the frequency (for FSK) of the signal output through ATO pin.

Pin 24 : TxCLK (Transmit Clock [Generated by Modem])

In the absence of TxSCLK, this output delivers the bit clock transmitted by the modem for the synchronization of data output through TxD terminal.

BRS selects the frequency as follows :

BRS = 0 → TxCLK = 1200 Hz

BRS = 1 → TxCLK = 600 Hz

Pin 25 : TxSCLK (Transmit Clock [Generated by Terminal])

This input corresponds to bit clock generated by the terminal whose frequency is 1200 Hz if BRS = 0 and 600 Hz if BRS = 1. This clock allows to lock the modem's internal clock on the clock generated by terminal, thus providing synchronization between these two clocks.

Pin 26 : CLK (Clock)

This is buffered output of the clock running at 4.9152 MHz.

Pin 27 : Xtal in (Oscillator Input)

This pin corresponds to the oscillator's input inverter. It is normally connected to an external crystal but may also be fed by a pulse generator. The crystal frequency must correspond to standard frequency of 4.9152 MHz.

Pin 28 : Xtal out (Oscillator Output)

This pin corresponds to the output of an inverter with sufficient loop gain to trigger and maintain the crystal oscillation.

1.4 - General Description & Block Diagram

TS 7515 is an integrated circuit manufactured in silicon gate CMOS technology. Device includes major modem functions required for simultaneous bidirectional transmission of asynchronous or synchronous data in accordance with the following standard requirements :

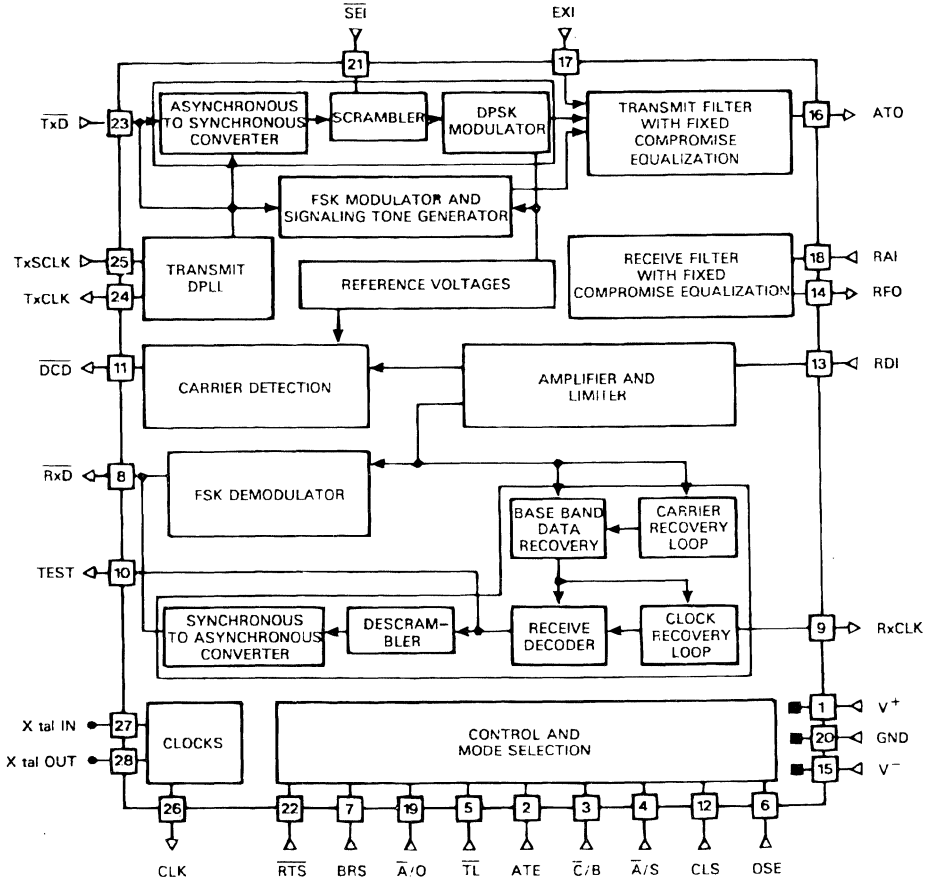
- CCITT V.22 variants A & B.
- BELL 212A DPSK operation.
- BELL 103 FSK.

This modem operates using channel multiplexing techniques by frequency allocation of 600 bauds for modulations rate and 1200 bits/s (600 bits/s in fallback mode) for transmission rate.

Transmission mode for each channel is Differential Phase Shift Keying (DPSK) modulation combined with on-line synchronous transmission. This feature is entirely reversible, i.e. operation is possible in either of Originate or Answer modes.

When used in combination with appropriate line and controller circuits, this device can operate on both 2-wire switched telephone network and all point-to-point leased lines.

Figure 1 : TS7515 Block Diagram.



M88TS7515-03

1.5 - Functional Description

The device is organized in 3 distinct sections :
- Transmit section.
- Receive section.
- Common units.

1.5.1 - TRANSMIT SECTION

This section comprises :
- An asynchronous to synchronous converter whose duty is to accept chain of asynchronous characters and to convert it to a form suitable for 1200 bits/s or 600 bits/s + 0.01 % synchronous transmission.
  This converter meets in all respects CCITT standard requirements defined in Chapter "4.2.1" of V.22 recommendations.
  In synchronous mode of operation, the converter is disabled.
- A variable ratio divider used for the generation of eight different frequencies :
  1200 Hz ± 0.5 Hz DPSK lower channel (Originate Mode)
  1800 Hz ± 20 Hz Guard tone transmitted optionally with upper channel
  2100 Hz ± 16 Hz Answer tone (CCITT Standards)
  2400 Hz ± 1 Hz DPSK upper channel (Answer Mode)
  2225 Hz ± 16 Hz Answer tone (BELL Standards)
  or FSK upper channel
  2025 Hz ± 10 Hz FSK upper channel
  1270 Hz ± 5 Hz FSK lower channel
  1070 Hz ± 5 Hz FSK lower channel
- A transmit clock generator using a phase-locked loop circuit in order to lock the transmission clock onto either the clock generated by data terminal or the receive clock.
- A data scrambler in accordance with CCITT standard requirements as defined in "Chapter 5.1" of V.22 recommendations.
- A buffer circuit that stores the last phase of the carrier and generates appropriate phase shift thus providing the new phase shift to be applied to the carrier.
- A carrier generator that uses two sub-carriers over modulated in amplitude, to synthesize the DPSK signal.
- A transmit filter whose frequency response is determined by selected mode of operation (Originate or Answer).
- A non switched smoothing filter that removes clock transients and rejects out-of-band frequencies.

1.5.2 - RECEIVE SECTION

This section includes :
- An anti-aliasing filter
- A band-pass receive filter whose frequency response depends on the selected mode of operation.
- A compromise equalizer filter that provides appropriate functional performance on a variety of lines.
- A phase-locked loop for the recovery of carrier signal frequency so as to perform a coherent differential phase demodulation on received signal.
- A demodulator.
- Two low-pass digital filters for the extraction of Eges Pattern.
- A decision making module that converts the eyes pattern into logic signals, stores them, detects the phase shift and performs identification of the received data.
- A synchronization unit that recovers the modulation time base and delivers RxCLK (Receive signal Clock) to the data terminal.
- A delayed hysteresis level detector that meets CCITT standard requirements of connector pin 109 as defined in "Chapter 3.3" of V.22 recommendations.
- A data descrambler in accordance with CCITT V.22 recommendations.
- A synchronous to asynchronous converter whose duty is as follows :
  - Accept chain of characters originated from a V.22-type asynchronous modem operating in transmit mode, demodulated by a V.22-type synchronous demodulator.
  - Recover the initial character chain applied to the asynchronous to synchronous converter of the transmitting modem.
  This synchronous to asynchronous converter meets in all respects the CCITT standard requirements as defined in"Chapter 4.2.2" of V.22 recommendations.
  The converter is disabled in synchronous mode of operation.

1.5.3 - COMMON UNITS

This section includes :
- A time base generator that uses a standard 4.9152 MHz crystal oscillator to derive all internal clock frequencies required for modulator and demodulator operation.
- A reference voltage generator delivering an internal reference voltage for :
  - Amplitude clamping of the transmitted signal.
  - Definition of demodulator's two threshold detection levels.

1.6 - Functional Characteristics

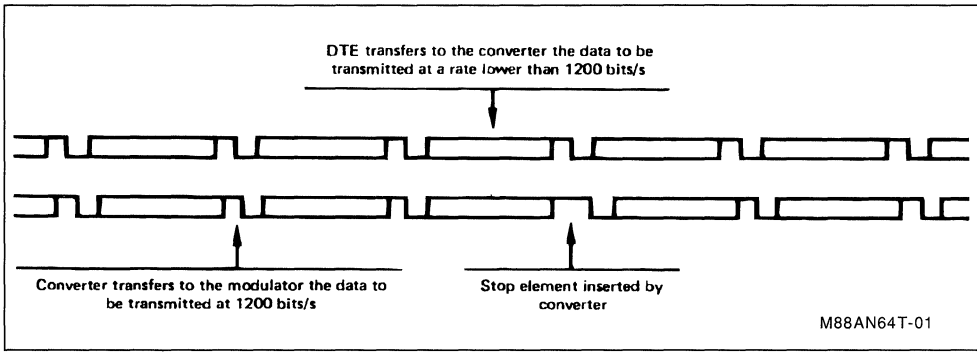
Asynchronous/Synchronous & Synchronous/Asynchronous Converters

Operating principles of these converters are covered in Sections 4.2.1 and 4.2.2 of CCITT V.22 recommendations.

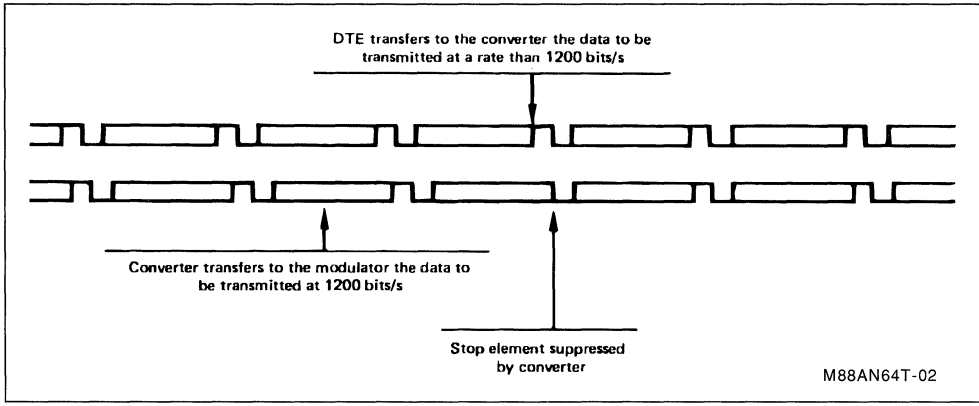
These converters are employed only in the case of variant B configuration.

1.6.1 - ASYNCHRONOUS/SYNCHRONOUS CONVERTER

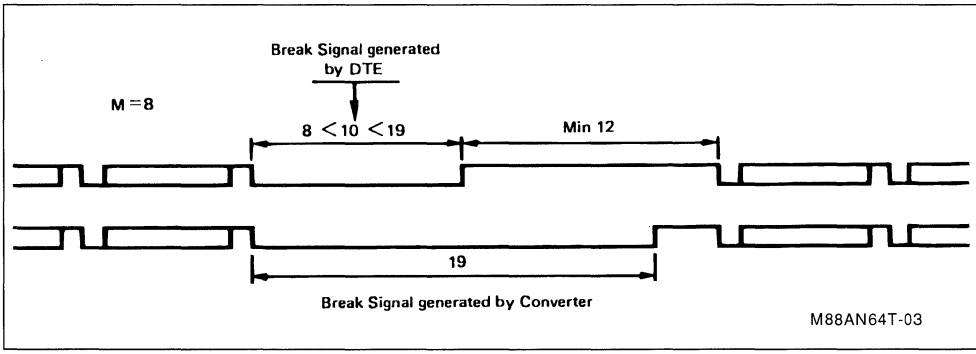
a) If data to be transmitted is generated at a rate lower than 1200 bits/s (but within the over speed selection limits imposed by OSE), the converter will insert the necessary stop elements as illustrated by timing diagram below.



b) If data to be transmitted is generated at a rate higher than 1200 bits/s (but within over speed selection limits imposed by OSE), the converter will suppress the stop elements as shown in timing diagram below.



c) Break Signal
Break signal contains M to 2 M + 3 bits, all of which maintain their initial state. M represents number of bits per character corresponding to selected format. Upon detection of such signal, the converter automatically generates 2 M + 3 bits all having their initial polarity. Timing diagram below illustrates this procedure.

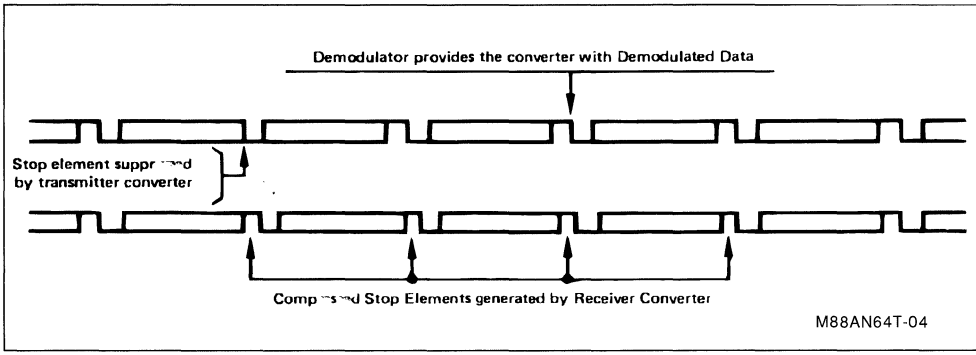


1.6.2 - SYNCHRONOUS TO ASYNCHRONOUS CONVERTER

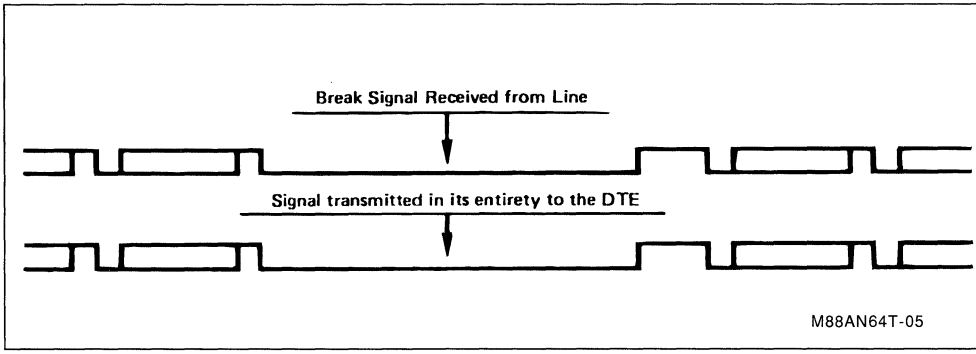
In receive mode, this converter must be capable of recovering the data transmitted by distant DTE while respecting the break signal generated by asynchronous to synchronous converter of the distant modem.

a) If the converter detects a missing stop element within the demodulated signal :
- It will regenerate this missing element, and
- In order to resynchronize the demodulated signal, it will reduce the duration of stop elements by as much as necessary but within over speed selection limits of OSE.

This procedure is illustrated in timing diagram given below.



b) The converter detects the missing stop elements at the end of break signal character, and transfers this signal in its entirety to the DTE as shown in timing diagram below.



1.6.3 - SCRAMBLER & DESCRAMBLER

Operating principles of the scrambler and the descrambler are discussed in "Chapter 5.1 and 5.2" of CCITT V.22 recommendations.

The scrambler allows to recover, at receiver, the clock rate associated with the received data so as to perform a coherent demodulation and also to provide the DTE with a clock whose phase is synchronized with the received data.

Figure 2 illustrates the "scrambling fundamentals".

As shown, the scrambler includes a pseudo-random sequence generator composed of :

- A single-input, single-output shift-register.
- In general, a single interconnection point.
- An Exclusive OR gate.

If the interconnection point is appropriately located and if N represents the number of shift-register stages, then the generated bit sequence representing a pseudo-random character will have a period of $2^N - 1$.
Note that the number of identical bits of this sequence will not exceed N.

The shift-register is driven by the transmit clock. The pseudo-random sequence so generated is applied to one of the inputs of the "Exclusive OR" whose other input is loaded with the data to be scrambled. Thus, data bits are inverted whenever they coincide with a high level (1) of the sequence.

Inverse procedure is performed in receive mode and requires the pseudo-random generator to operate in synchronization with the pseudo-random sequence generator used at transmission end. In order to avoid this constraint, it is generally preferable to emply a self-synchronizing scrambler similar to the one depicted in Figure 3.

Operation is identical to that given in Figure 2. However, in this case the scrambled data is applied to the transmit register and similarly, after transmission, the scrambled data is applied to the input of the receive register. It is clear that at the end of first N-bit transmission, the receive register will be in the same state as the transmit register - taking into consideration the propagation delay time inherent to the transmission line.

In both types of the scrambler, data recovery procedure is accomplished thanks to reversible property of the Exclusive Or gate.

If $a \oplus b = c$ [where $\oplus$ represents modulo-2 sum] then $a = b \oplus c$

The self-synchronizing scrambler has the disadvantage of multiplying the number of errors by a factor of 3. In fact, when an isolated error appears at the input of the receive register, it causes a first error in the recovered bit sequence - then a second error occurs as it reaches the level of interconnection point - and finally a third error is generated at the last stage of the register.

Figure 2 : Scrambler Block Diagram.

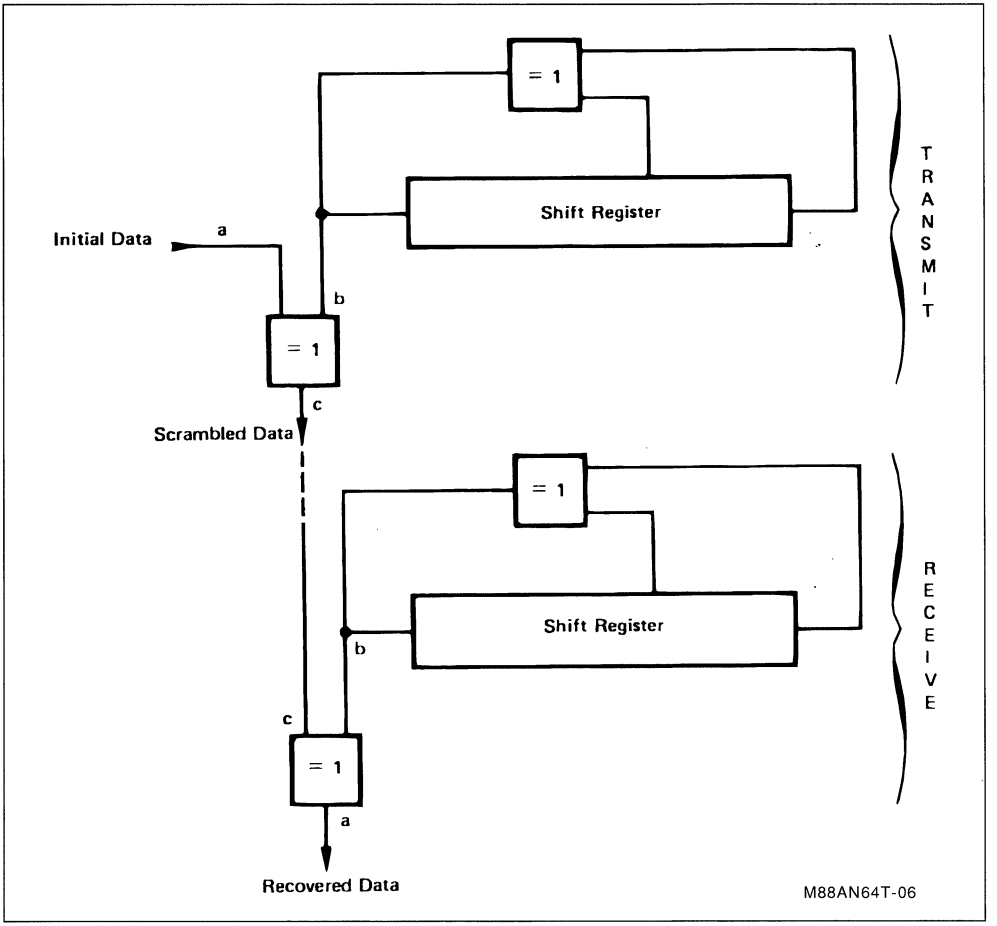
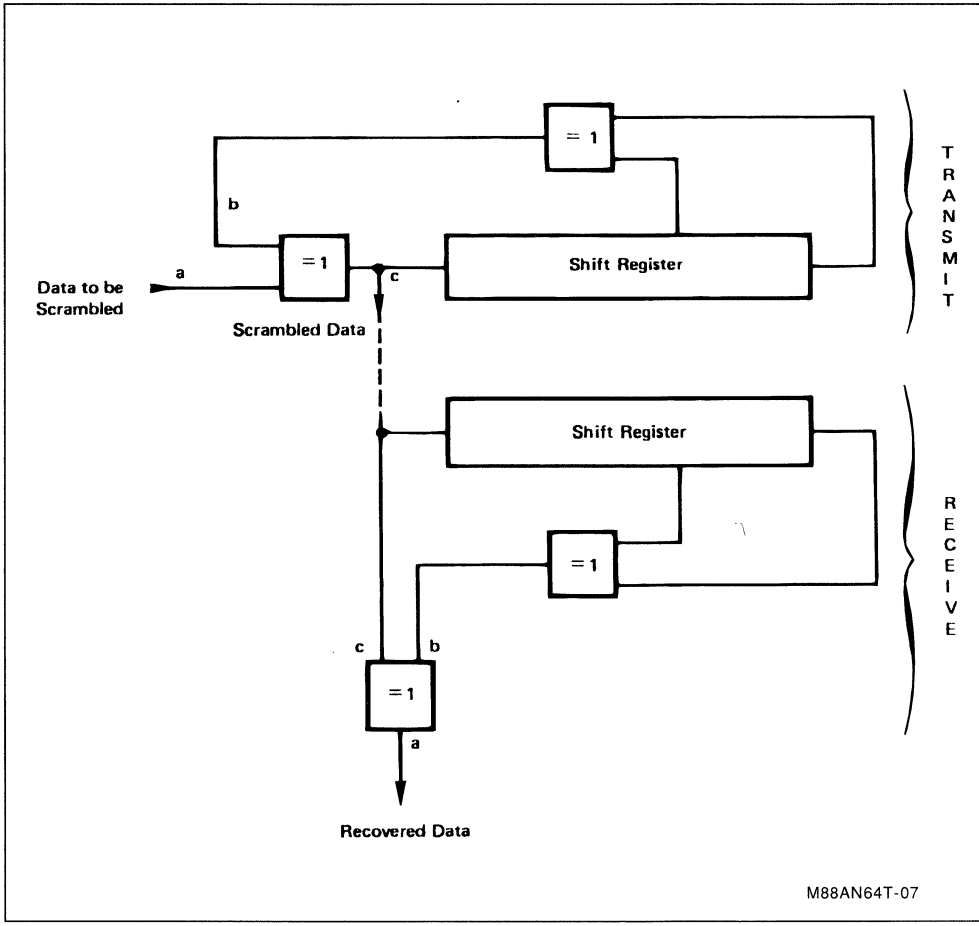


Figure 3 : Self-synchronizing Scrambler.

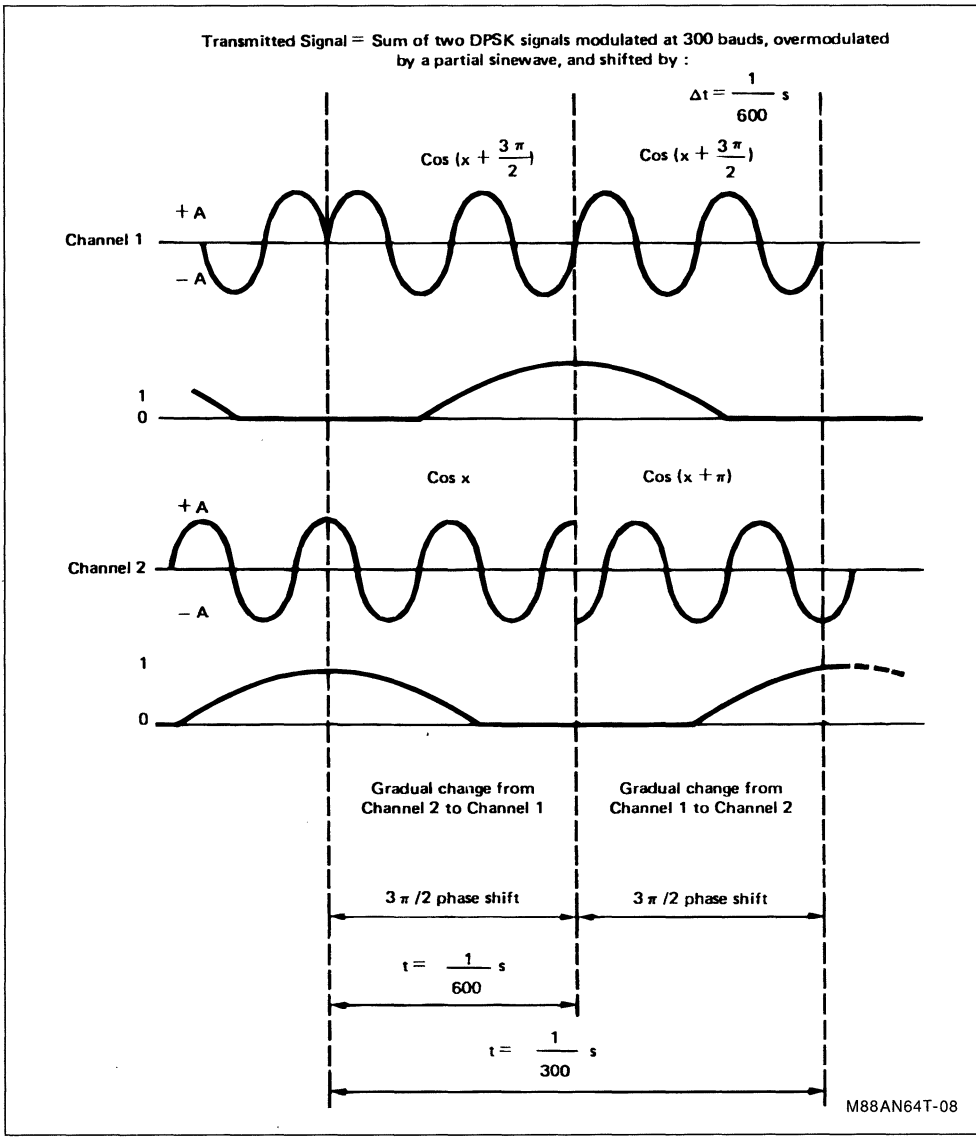


1.6.4 - CARRIER & TONE GENERATORS

The DPSK signal generation is achieved using a ROM containing 32 x 8-bit states and an 8-bit C-2C converter circuit.

1.6.5 - TRANSMITTED SPECTRUM

In order to respect the limits of ampitude and distortion due to propagation delay time recommended by CCITT, the modulated signal comprises sum of two carriers alternately modulated at a master rate of 600 bauds and overmodulated by a partial sinewave, as shown in timing diagram below.



1.6.6 - FILTERS

1.6.6.1 - Transmit Filter

In combination with the modulation effects, the transmit filter allows to meet performance characteristics recommended by CCITT. A compromise equalizer compensates partially for line irregularities.

This is a 12th order switched-capacitor filter.

1.6.6.2 - Receive Filter

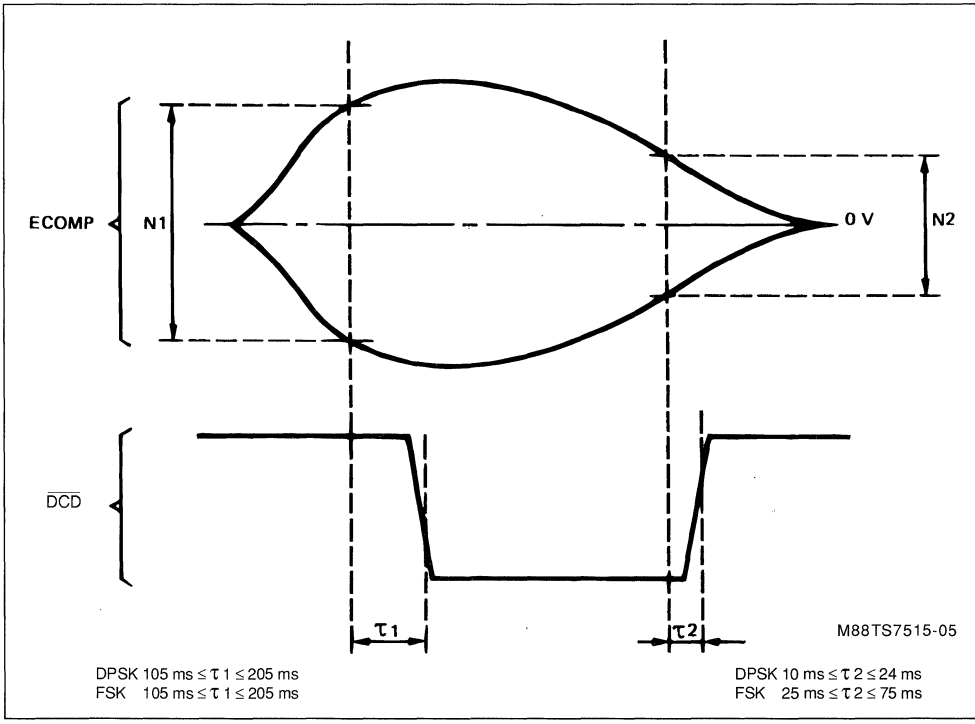
The receive filter allows to recover a maximum amount of energy in receive channel while it offers an efficient rejection of the transmission channel and the guard tones. A fixed compromise equalizer compensates partially for irregularities due to line characteristics.

a) Lower Channel
This is 20th order filter implemented by cascading a 14th order amplitude clamping module and a 6th order all-pass module providing propagation delay time correction.

b) Upper Channel
This is 14th order filter implemented by cascading a 10th order amplitude clamping unit and a 4th order all-pass unit providing propagation delay time correction.

1.6.7 - LEVEL DETECTOR

RDI input connected to a signal detection circuit that discriminates between two positive levels N1 and N2. Output of the detector is delayed so as to provide hysteresis effects between N1 and N2. See timing diagram given next.



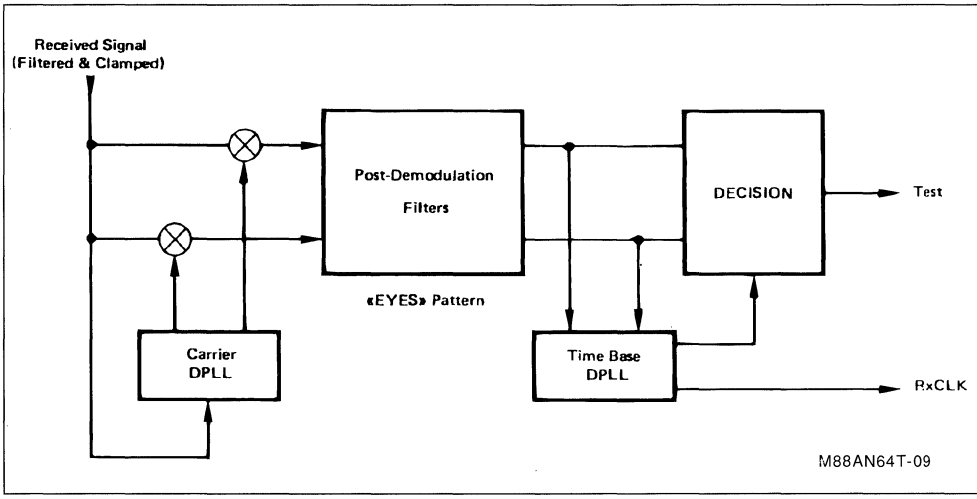
DPSK 105 ms ≤ τ 1 ≤ 205 ms
FSK 105 ms ≤ τ 1 ≤ 205 ms

DPSK 10 ms ≤ τ 2 ≤ 24 ms
FSK 25 ms ≤ τ 2 ≤ 75 ms

1.6.8 - SYNCHRONOUS DEMODULATOR

The signal received on line is first filtered and clamped at appropriate level and then applied to this synchronous modulator which will deliver demodulated data synchronized on receive clock.

1.6.8.1 - Demodulator Block Diagram



1.6.9 - SUMMARY TABLES OF OPERATING MODES

1.6.9.1 - Synthesis of different Modes for Receive Section

$\overline{C}$/B	BRS	$\overline{TL}$	$\overline{A}$/O	Receive	Mode
– 1 or 0	X	– 1	0	DPSK Originate Loop 3	V.22
			1	DPSK Answer Loop 3	
		0	0	DPSK Answer Loop 2	
			1	DPSK Originate Loop 2	
		1	0	DPSK Answer	
			1	DPSK Originate	
1	0	– 1	0	DPSK Originate Loop 3	BELL 212A Including BELL 103
			1	DPSK Answer Loop 3	
		0	0	DPSK Answer Loop 2	
			1	DPSK Originate Loop 2	
		1	0	DPSK Answer	
			1	DPSK Originate	
	1	– 1	0	FSK Originate Loop 3	
			1	FSK Answer Loop 3	
		0	0	FSK Answer Loop 2	
			1	FSK Originate Loop 2	
		1	0	FSK Answer	
			1	FSK Originate	

Answer : Receive in Lower Channel
Originate : Receive in Upper Channel

Loop 3 : Analog Loop
Loop 2 : Digital Loop

1.6.9.2 - Synthesis of different Modes for Transmit Section

$\overline{ATE}$	$\overline{C}$/B	BRS	$\overline{A}$/O	Transmit	Mode
0	– 1 or 0			2100 Hz	Answer Tone
	1			2225 Hz	
1	– 1	0	0	DPSK 1200 bps Answer	V.22 without Guard Tone
			1	DPSK 1200 bps Originate	
		1	0	DPSK 600 bps Answer	
			1	DPSK 600 bps Originate	
	0	0	0	DPSK 1200 bps Answer	V.22 with 1800 Hz Guard Tone
			1	DPSK 1200 bps Originate	
		1	0	DPSK 600 bps Answer	
			1	DPSK 600 bps Originate	
	1	0	0	DPSK 1200 bps Answer	BELL 212A
			1	DPSK 1200 bps Originate	
		1	0	FSK 0 – 300 bps Answer	
			1	FSK 0 – 300 bps Originate	

Answer : Transmit in Upper Channel
Originate : Transmit in Lower Channel

1.6.9.3 - Mode Selection in Phase Modulation Transmission

$\overline{A}$/S	CLS	OSE	Transmission Mode	Character Length	Overspeed
– 1	0	0	Asynchronous	8	+ 1 %, – 2.5 %
		1			+ 2.3 %, – 2.5 %
	1	0		11	+ 1 %, – 2.5 %
		1			+ 2.3 %, – 2.5 %
0	0	0		9	+ 1 %, – 2.5 %
		1			+ 2.3 %, – 2.5 %
	1	0		10	+ 1 %, – 2.5 %
		1			+ 2.3 %, – 2.5 %
1	0	0	Synchronous		

1.6.9.4 - Test pin

$\overline{ATE}$	$\overline{C}$/B	BRS	Transmit	Receive	Test
0	– 1 or 0	0	2100 Hz	V.22 DPSK 600 bps	DDO
		1		V.22 DPSK 1200 bps	DDO
	1	0	2225 Hz	BELL 212A DPSK 1200 bps	DDO
		1		BELL 103 FSK 0 – 300 bps	HLO
1	– 1	0	V.22 without Guard Tone DPSK 1200 bps		DDO
		1	V.22 without Guard Tone DPSK 600 bps		DDO
	0	0	V.22 with Guard Tone DPSK 1200 bps		DDO
		1	V.22 with Guard Tone DPSK 600 bps		DDO
	1	0	BELL 212A DPSK 1200 bps		DDO
		1	BELL 103 FSK 0 – 300 bps		HLO

DDO : DPSK Demodulator Output
HLO : Hard Limiter Output

2 - DETAILED DESCRIPTION OF V.22 & BELL 212A STANDARDS

2.1 - Foreword

Due to the fact that the present application note is primarily intended for technicians not possessing an in-depth knowledge of this "advanced" field of telecommunications, it seemed appropriate to include an overview of the most recent publications covering specifications of the V.22 and BELL 212A standard requirements.

We shall also discuss line interface characteristics and requirements which together with modulator, demodulator, carrier detection, user interface (V.24, RS-232C) must be appropriately employed -or else, equipment of different manufacture will be unable to communicate with each other.

On the other hand, if standard requirements and rules are properly observed, then a system implemented in Japan and another in France, will be able to communicate without any difficulty.

2.2 - V.22 Standard

Modem operating at 1200 bits/s in full duplex.

Normalized for operation on general switched telephone lines and leased networks.

2.2.1 - GENERAL DESCRIPTION

This Modem is intended for operation on switched telephone networks and point-to-point leased lines.

Main characteristics are as follows :

- Duplex operation on switched 2-wire telephone and point-to-point leased lines.
- Frequency division channel assignment.
- Differential Phase Modulation for each channel with on-line synchronous transmission at 600 bauds.
- Scrambler availability.
- Measurement facilities.

Since the application coverage is wide, V.22 recommendations provide for 3 possible configuration variants. As far as we are concerned, we shall limit our discussion to two of these variants.

Characteristics of these variants are as follows :

2.2.1.1 - Variant A

1200 bits/s synchronous
600 bits/s synchronous

2.2.1.2 - Variant B

1200 bits/s synchronous
600 bits/s synchronous
} Variant A
+
1200 bits/s Asynchronous
600 bits/s Asynchronous

2.2.2 - ON-LINE SIGNALS

2.2.2.1 - Carrier frequency and Guard Tone.

Frequencies of the operation are respectively 1200 Hz ± 0.5 Hz for lower channel and 2400 Hz ± 1 Hz for upper channel. A 1800 Hz ± 20 Hz Guard Tone is transmitted continuously whenever modem transmits in upper channel. This guard tone must be disabled when modem transmits in lower channel.

An additional 550 Hz guard tone may be transmitted for national applications.

2.2.2.2 - Levels of transmitted Data Signals & Guard Tone

The 1800 Hz guard tone must be 6 ± 1 dB below power level of data signals transmitted in upper channel.

Total power of signal transmitted on-line must meet specifications defined by V.2 recommendations :

Total power drawn from line by subscriber equipment must not exceed 1 mW, whatever the operating frequency.

Note that this power must be identical in both directions (go & return).

Due to the presence of the guard tone, power level of upper channel signals is approximately 1 dB below that of the lower channel signals.

2.2.3 - FIXED DELAY COMPROMISE EQUALIZER

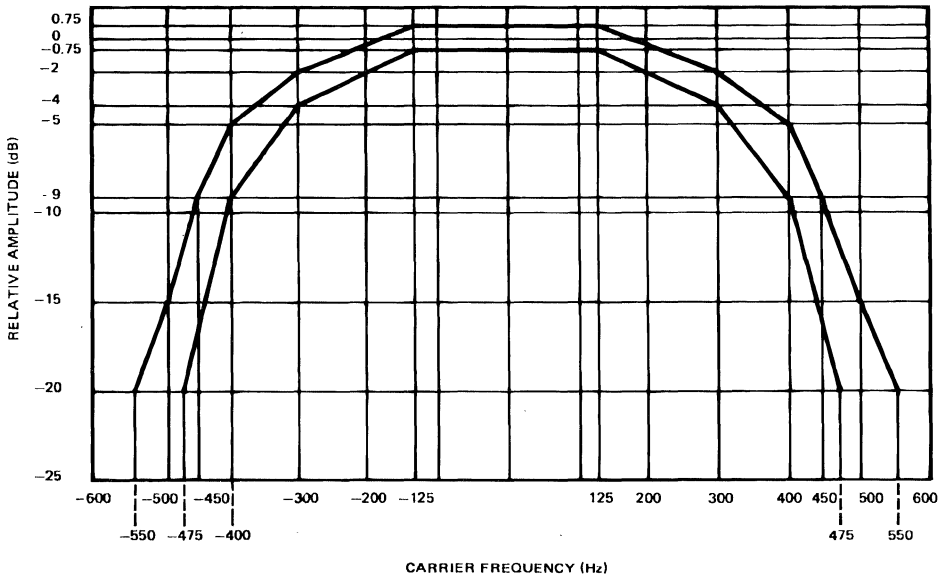
This on-chip compromise equalizer is commonly shared by both transmit and receive sections.

Note : This equalizer is mainly intended to compensate for transmission line irregularities caused by signal amplitude attenuation and group propagation delay time $d\varphi/d\omega$.

2.2.4 - SPECTRUM & GROUP PROPAGATION TIMES

Signal transmitted on the line must conform to characteristics depicted in the following Figure.

Figure 7 : Amplitude Limits of Signal Transmitted On-line (without equalization).



The group propagation time of transmitter output signals must fall within ± 100 µs limits in frequency range of 800 Hz to 1600 Hz (lower channel) and 2000 Hz to 2800 Hz (upper channel).

2.2.5 - MODULATION

2.2.5.1 - Bit Rate

As mentioned earlier, we shall only discuss variants A and B of V.22.

The on-line transmission bit rate must be either 1200 bits/s or 600 bits/s ± 0.01 % with a modulation rate of 600 bauds ± 0.01 %.

2.2.5.2 - Data bits coding

Data stream to be transmitted is split into groups of consecutive 2 bits called dibits. Each dibit is encoded by considering the relative phase change with respect to previous phase element of the signal (see table below).

Dibit Value (at 1200 bits/s)	**Bit Value** (at 600 bits/s)	**Phase Change**
00	0	+ 90°
01		0°
11	1	+ 270°
10		+ 180°

Note : The phase change is the actual phase shift on-line within signal transition area situated between the middle of a signal element and the mid point of the following element.
Upon receipt, dibits are decoded and recovered bits arranged in correct order. The left number of the dibit appears first within the data streams as they enter modem's demodulator section located following the scambler.

The foregoing applies to bit rate of 1200 bits/s. In the case of 600 bits/s, each bit is coded by a phase change with respect to the preceding phase of the signal element.

2.2.6 - FREQUENCY TOLERANCE OF THE RECEIVED SIGNAL

The transmitter carrier frequency tolerance is at maximum ± 1 Hz and allowing a drift of ± 6 Hz due to transmission line characteristics, the receiver must therefore be capable of accepting errors at ± 7 Hz tolerance on received frequencies.

2.2.7 - CONNECTOR PINS

The following table gives a list of indispensable and optional connector pins used for DTE/DCE Interface.

2.2.7.1 - Summary of Connector Pins

Pin Number	Function	Note
102	Signal Ground or Common Return Line	
102 a	DTE Common Return Line	
102 b	DCE Common Return Line	
103	Transmitted Data	
104	Received Data	
105	Request to Send	
106	Clear to Send	
107	Data Set Ready	
108/1	Connect Data Set to Line	
108/2	Data Terminal Ready	
109	Received Line Signal (carrier detector)	
111	Bit Rate Selection (DTE originated)	1
113	Transmit Signal Element Timing (DTE source)	2
114	Transmit Signal Element Timing (DCE source)	3
115	Receive Signal Element Timing (DCE source)	3
125	Ring/Calling Indicator	4
140	Test/Diagnostic Loop	
141	Local Loop	
142	Test Indicator	

Notes : 1. This pin is optional.
2. Signals on this pin are ignored when modem not operating in synchronous mode.
3. This pin is locked on OFF state when modem does not operate in synchronous mode.
4. Used only when modem is connected to public switched telephone lines.

2.2.7.2 - Thresholds of Pin 109

Thresholds of pin 109 are specified at modem input terminals, ignoring effects produced by compromise equalizer.

This pin must not react to 1800 Hz Guard Tone and 2100 Hz Answer Tone transmitted during call establishment sequence.

Upper Channel threshold

Higher than – 43 dBm → Pin 109 ON

Lower than – 48 dBm → Pin 109 OFF

Lower Channel threshold

Higher than – 43 dBm → Pin 109 ON

Lower than – 48 dBm → Pin 109 OFF

The intermediate state of pin 109 between ON and OFF levels is not specified. However, the signal level detector must exibit a hysteresis higher than 2 dB.

2.2.7.3 - Pin 111 & Bit Rate Control

The bit rate is selected by :
- Appropriate strap or switch settings on Modem Board.
- Using connector pin 111.
- Or, combination of both.

If used, pin 111 will in ON state enable 1200 bits/s operation, and 600 bits/s in Off condition.

2.2.7.4 - Electrical Characteristics of Connector Pins

It is advised to respect electrical characteristics specified in V.28 recomendations. Applicable connector and pin spacing requirements are defined in ISO 2110 publication.

2.2.7.5 - Error Condtions of Connector Pins

Some applications require detection of failure conditions on connector pins, a summary of which is given next.

1) Lack of connection between DTE and DCE
2) Open-circuited interconnecting cable
3) Short-circuited interconnecting cable

Type 1 error : Data pins are all at logic level "1". Control and timing pins are in OFF state.

The DTE must consider an error on pin 107 as being in OFF state.

Similarly, failure conditions on pins 105 and 108, are considered as OFF states by DCE.

2.2.8 - DTE/DCE INTERFACE MODES OF OPERATION

2.2.8.1 - Variant A

The Modem may be configured for the following modes of operation :

- 1200 bits/s ± 0.01 % synchronous
- 600 bits/s ± 0.01 % synchronous

In these modes, the modem monitors pin 113 or pin 114 and accepts through pin 103 the synchronous data originated from DTE. These data are then scrambled and forwarded to the modulator for coding.

In addition to normal transmit timing element, the modem must provide the possibility of deriving the transmit signal element timing from receive signal element timing.

2.2.8.2 - Variant B

- 1200 bits/s ± 0.01 % synchronous
- 1200 bits/s asynchronous, 8-, 9-, 10-, 11-bit characters
- 600 bits/s ± 0.01 % synchronous
- 600 bits/s asynchrnous, 8-, 9-, 10-, 11-bit characters

Synchronous modes are identical to those outlined for variant A.

2.2.9 - TRANSMITTER

In asynchronous modes, modem accepts asynchronous data stream issued by DTE at a nominal rate of 1200 or 600 bps.

Asynchronous data are converted into suitable format for synchronous transmission at 1200 or 600 bps ± 0.01 %, then scrambled and sent to the modulator for encoding.

The converter must be configured to accept the following character formats :

a) One start bit, followed by seven data bits and one stop bit (9-bit character).

b) One start bit, followed by eight data bits and one stop bit (10-bit character).

c) One start bit, followed by nine data bits and one stop bit (11-bit character).

d) One start bit, followed by six data bits and one stop bit (8-bit character).

2.2.10 - FUNDAMENTAL BIT RATE

The intercharacter binary bit rate (including start and information bits) generated by DTE or provided through pin 103, must be 1200 or 600 bits/s with tolerance falling within + 1 % to - 25 % limits.

When the character bit rate falls within the limits of theoretical values (1200 or 600 bits/s) and the maximum value (+ 1 %), the asynchronous to synchronous converter implemented in the transmitter section must suppress, whenever necessary, the stop bits of the input characters.

Within 8 consecutive characters, at most one stop element may be eliminated.

On the other hand, if the character bit rate falls within the limits of theoretical values (1200 or 600 bits/s) and the minimum value (- 2.5 %), then the asynchronous to synchronous converter will provide more bits per second than DTE is generating. As a consequence, the converter will insert additional stop elements within the transmitted characters.

Some Data Terminal Equipment and Multiplexors exceed the + 1 % bit rate tolerance. The modem must therefore be capable of accepting data provided by DTE at 1200 or 600 bits/s, tolerance between + 2.3 % and – 2.5 % and consequently suppress at most one stop element per 4 consecutive characters.

2.2.11 - BREAK SIGNAL

If the converter detects M to 2 M + 3 bits all of which have the polarity of start bit, where M is the number of bits per character in selected format, it will transmit 2 M + 3 bits all with start polarity. However, if more than 2 M + 3 bits of start polarity are detected, the converter will transmit them all with start polarity.

2.2.12 - RECEIVER

Intercharacter bit rate delivered to DTE through pin 104 must have a value between 1200 and 1221 bits/s.

For all characters, start and data elements should be of identical nominal length. The width of the stop

element should not be reduced by more than 12.5 % for fundamental bit rates so as to allow detection of any excessive bit rate caused by transmission terminal equipment.

Received 2 M + 3 bits (or more) with start polarity sent by originating modem are supplied to pin 104. The modem detects the transition from stop polarity to start polarity in order to regenerate character synchronization.

2.2.13 - SCRAMBLER & DESCRAMBLER

2.2.13.1 - Scrambler

The modem includes a self-synchronizing scrambler that implements $1 + x^{-14} + x^{-17}$ polynomial generator. This scrambler is integrated inside the transmitter section of the modem.

The data message sequence applied to the scrambler are divided by the polynomial generator. The resultant quotient coefficients, arranged in decreasing order, represent the data sequence to appear at scrambler output.

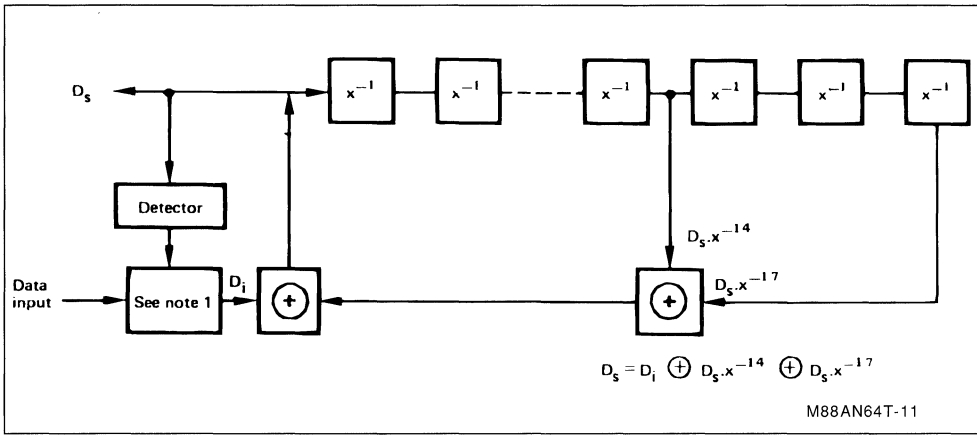
The scrambler output data sequence is given by the following expression.

$$D_S = D_i \oplus DS \,.\, x^{-14} \oplus DS \,.\, x^{-17}$$

Where :

D_S : Data sequence at Scrambler Output
D_i : Data sequence applied to Scrambler Input
$\oplus$: Modulo-2 Sum
"·" : Binary multiplication

The following Figure illustrates Scrambler functional configuration.



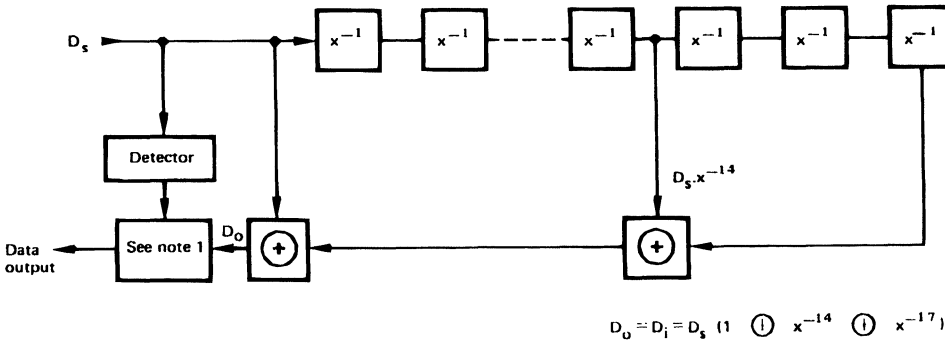
Note 1 : In order to avoid scrambler blocking to cause occasional and unpredicted occurrence of type-2 loopback, 64 consecutive binary "1"s must be first detected on scrambler output (D_S) and only then, the next signal applied to scrambler input (D_i) will be inverted. This function must be disabled during both call establishment and type-2 loopback sequences.

2.2.13.2 - Descrambler

Modem's receiver integrates a self-synchronizing descrambler implementing the $1 + x^{-14} + x^{-17}$ polynomial. The data sequence obtained after demodulation must be multiplied by $1 + x^{-14} + x^{-17}$ polynomial generator so as to obtain the descrambled message. Coefficients of the regenerated message, arranged in decreasing order, represent the data sequence on D_O output. This sequence is defined by the following expression :

$$D_O = D_S\,(1 \oplus x^{-14} \oplus x^{-17})$$

Figure below gives Descrambler functional diagram.



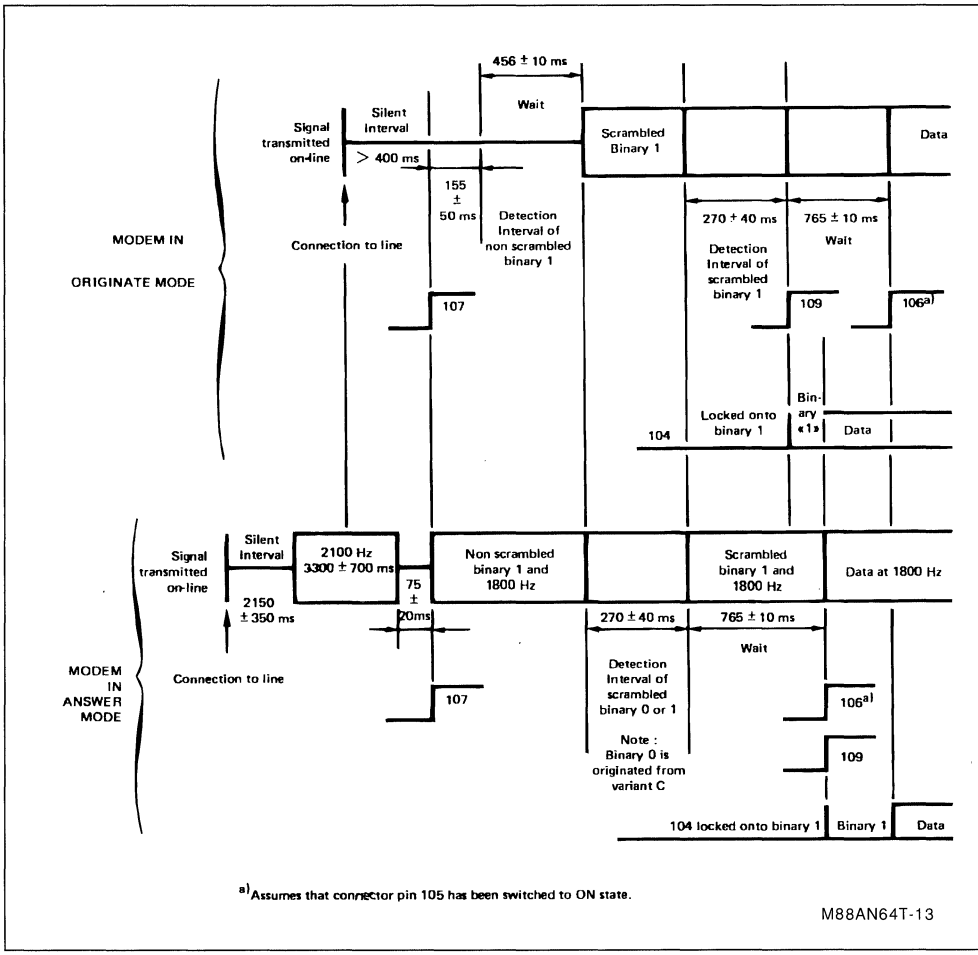
2.2.14 - SEQUENCE OF OPERATION (Permanent Carrier)

2.2.14.1 - Channel & Operating mode Selection

In public switched telephone lines, the called modem receives data in lower channel and transmits in upper channel.

2.2.14.2 - Operation on switched telephone lines

Timing diagram below illustrates how initial synchronization is established between originating and answering modem communicating through international switched telephone networks.



a) Assumes that connector pin 105 has been switched to ON state.

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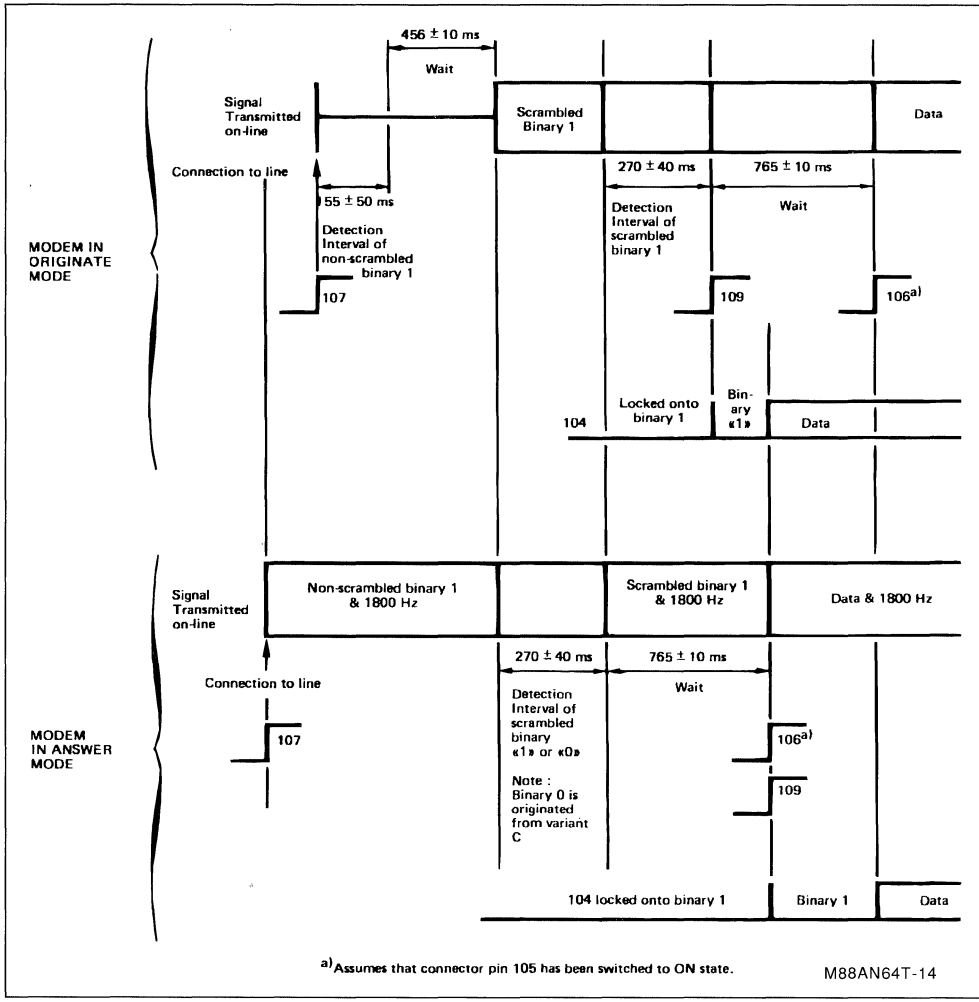
The following timing diagram depicts the call establishment sequence without auto-answer capability, as defined in V.25 recommendations.



a) Assumes that connector pin 105 has been switched to ON state.

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2.2.14.3 - Modem in Originate Mode

Once the originating Modem is connected to line, it must be conditioned to receive signals in upper channel by switching the connector pin 107 to ON state as required by V.25 recommendations. Then, the modem remains silent until it detects a sequence of non scrambled "1"s during an interval of 155 ± 50 ms, waits another 456 ± 10 ms and then begins sending a sequence of scrambled "1"s in the lower channel. When it detects a sequence of scrambled binary "1"s for a period of 270 ± 40 ms in the upper channel, the modem switches connector pin 109 (Received Line Signal) to ON state and then goes silent for 765 ± 10 ms. Then pin 106 (Clear To Send) will react in response to the state of pin 105 (Request To Send).

When pin 106 (Clear To Send) goes to OFF state, pin 103 (Transmitted Data) will be locked on binary "1".

2.2.14.4 - Modem in Answer Mode

Once the answering modem is connected to line, and immediately after answer sequence defined by V.25 recommendations is terminated, the modem will be conditioned to receive signals in the lower channel. Connector pin 107 (Data Set Ready) is switched to ON state and the modem begins transmitting a sequence of non scrambled binary "1"s. When it detects scrambled binary "1"s for an interval of 270 ± 40 ms in lower channel, the modem begins sending scrambled binary "1"s in the upper channel, waits 765 ± 10 ms and then switches pin 109 (Data Carrier Detect) to ON state and as a consequence pin 106 will react in response to pin 105. In the case where pin 106 is OFF, connector pin 103 (Transmitted Data) will be locked on binary state "1".

The foregoing sequence must be applied whenever two modems are connected to the line manually and irrespective of which modem is connected first. Once the contact has been established, any unpredicted loss and the reappearance of the signal on line, must not cause the generation of another call establishment sequence.

2.2.15 - Measurement Facilities (Maintenance)

The system must provide for both type-2 (local & remote) test loops and also type-3 loops, in accordance with V.54 recommendations.

2.2.15.1 - Type-2 Loopback Establishment

Important : Signals used to establish type-2 loopback may be transmitted only after the conclusion of synchronization handshake procedure.

As defined in V.54 recommendations, from now on, the modems will be called Modem A & Modem B.

When Modem A receives "through a switch mounted on front panel" an instruction to establish type-2 loopback, it begins the transmission of the initiation signal composed of non scrambled binary "1" elements.

Modem B detects this signal for an interval of 154 to 231 ms returns to Modem A a sequence of scrambled alternate "1"s and "0"s at 1200 bits/s (or 600 bits/s).

Modem A detects alternate scrambled "1"s and "0"s during an interval of 231 to 308 ms, ends the initiation signal and transmits scrambed "1"s at 1200 bits/s (or 600 bits/s).

Modem B detects the loss of the initiation signal and consequently establishes a type-2 loopback locally.

After the reception of scrambled binary "1"s during 231 to 308 ms, Modem A informs the DTE that transmission of test messages may begin.

2.2.15.2 - Suppression of Type-2 Loopback

When Modem A receives instruction to remove the type-2 loopback, the one-line signal transmission must be halted for 77 ± 10 ms interval, then re-initiated.

Modem B detects, signal loss within 17 ± 7 ms, signal reappearance within 155 ± 50 ms, and then resumes its normal mode of operation.

2.3 - BELL 212A Standard Description

Previous discussion covered in detail V.22 standard requirements that approach closely those of BELL 212A standards. In order to avoid unnecessary repetition of common topics, we shall limit our discussion to differences between V.22 and BELL 212A standard requirements.

BELL 212A covers entirely the A and B variants of V.22 with minor differences indicated below :

- Variant B has no fallback mode at 600 bits/s.
- Character lengths in asynchronous mode are limited to 9 and 10 bits.
- Only one overspeed (+ 1 %, – 2.5 %) is available.

BELL 212A standard includes a fallback mode called BELL 103.

BELL 103 Characteristics

Modulation Speed : 300 bits/s

Modulation Type : Frequency Shift Keying (FSK)

Data Transfer : Asynchronous, through both the RS-232C interface connector and the telephone line.

Frequency Spectrum : Band Division

Communication : Full duplex

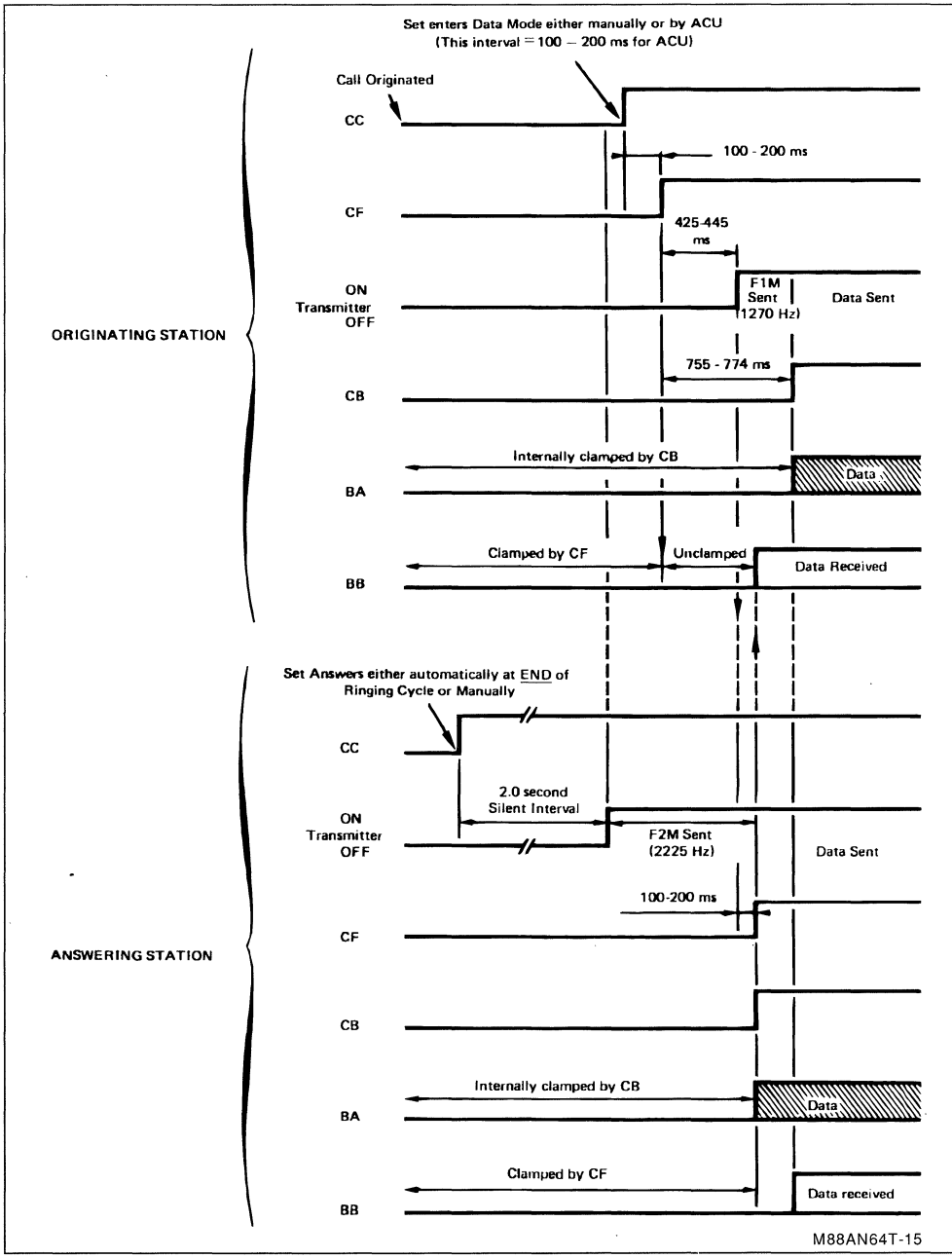
It differs from its CCITT equivalent in that logic "1" is represented by the high frequency and logic "0" by the low frequency of the frequency pair used for the modulation.

Differences between BELL 212 A & V.22

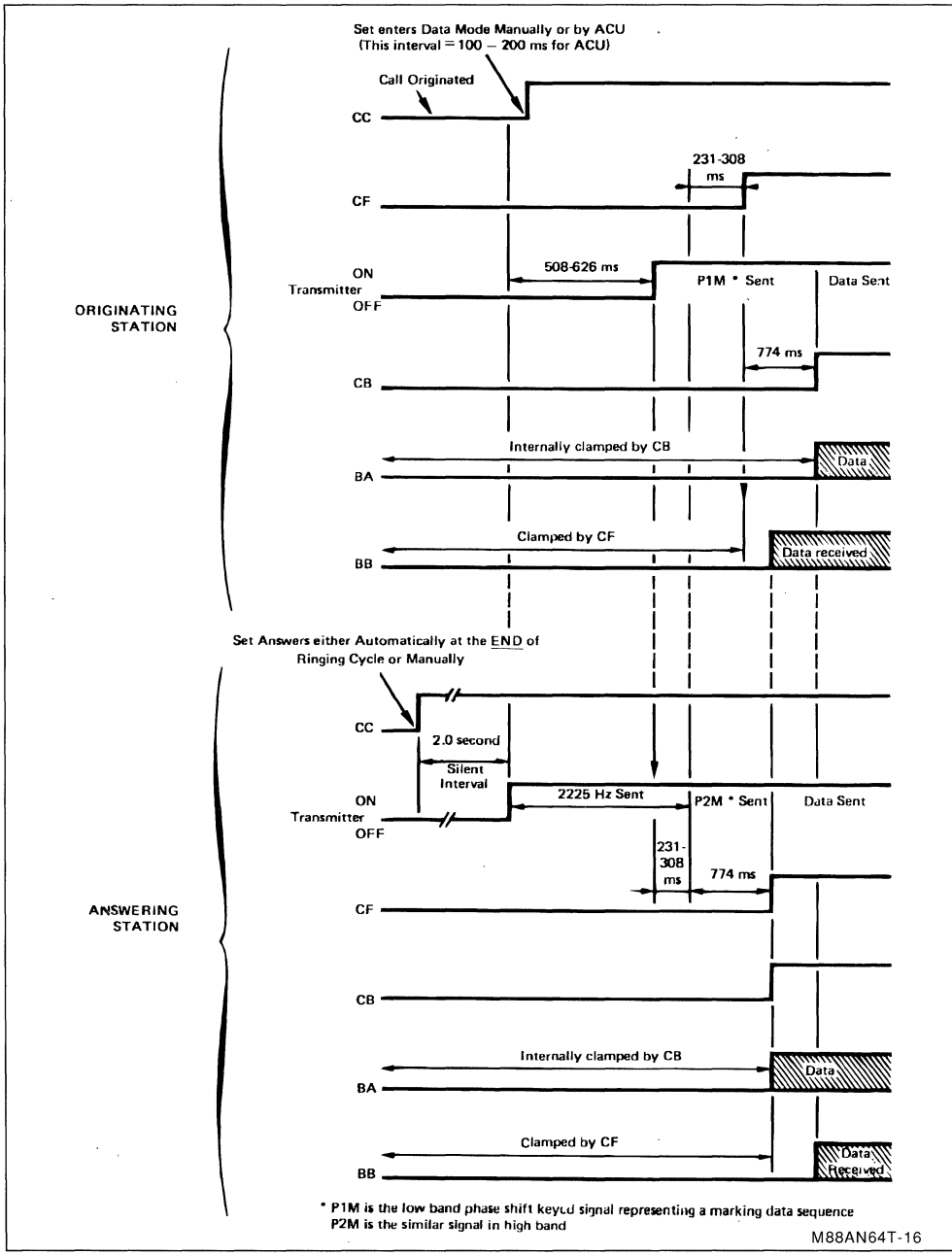
- In answer mode, detection of originating modem's speed.
- During call initiation sequence, the answering modem first sends the answer tone and then transmits a sequence of scrambled "1"s without interruption of carrier signal.
- Modem disconnection upon the reception of a sequence called Long Space.
- Transmission of Long Space to disconnect the distant modem.
- Absence of 64 consecutive binary "1" detection.

The following timing diagrams show different BELL 212A sequences.

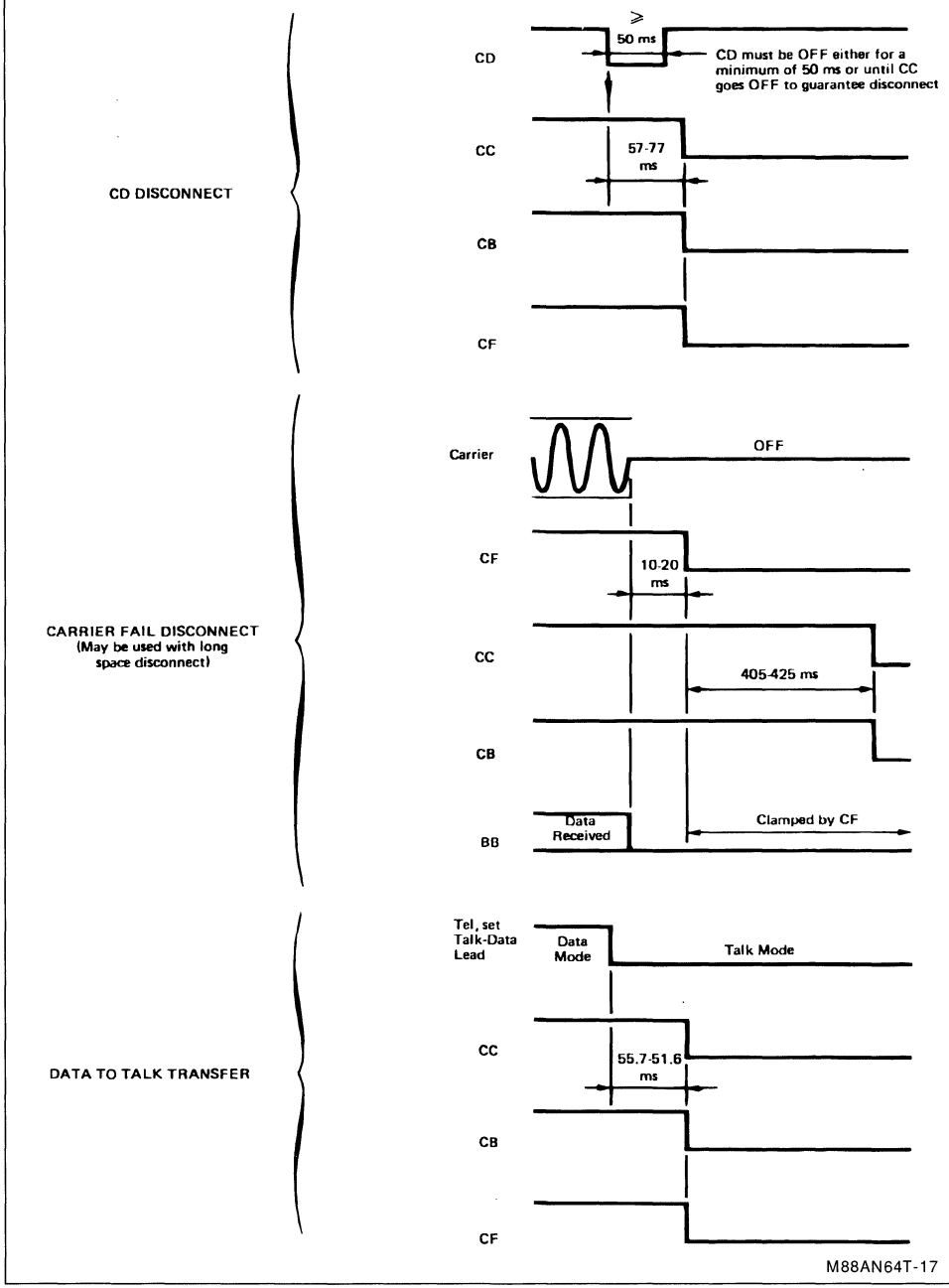
BELL 212A LOW SPEED CONNECT SEQUENCE CD ON : EITHER AUTOMATIC OR MANUAL OPERATION



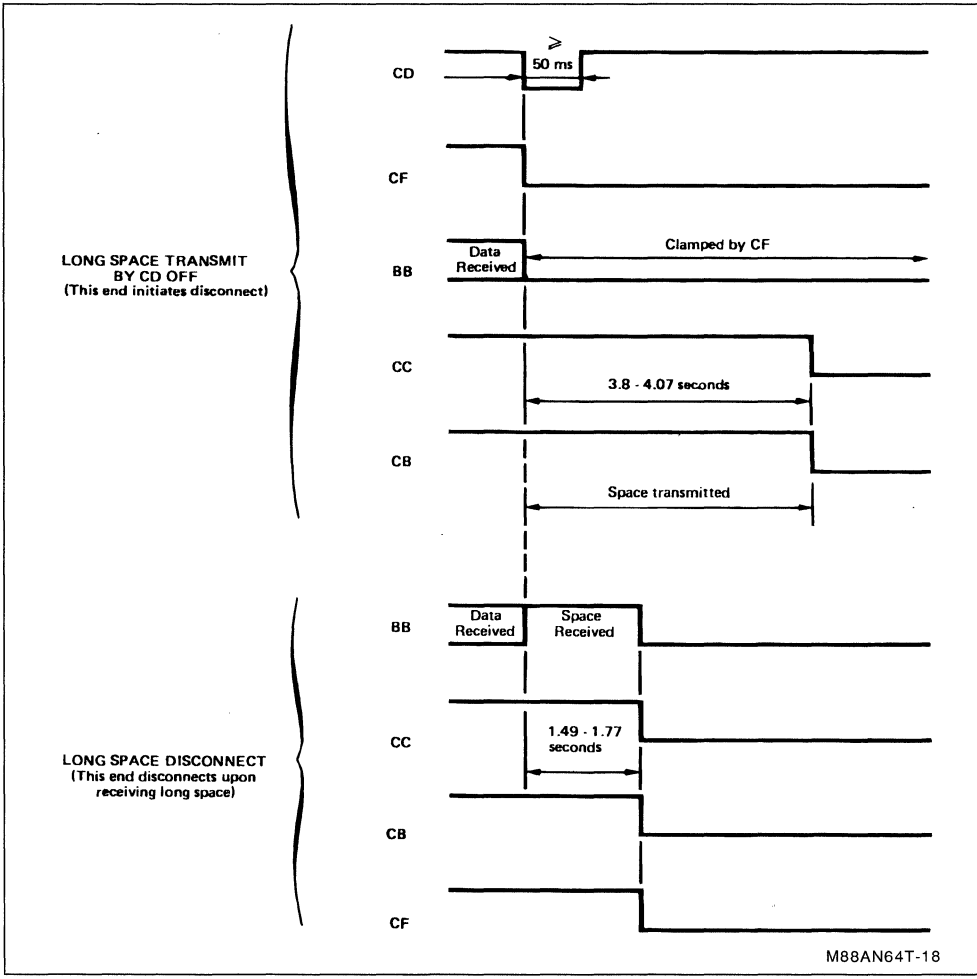
BELL 212A HIGH SPEED CONNECT SEQUENCE CD ON : EITHER AUTOMATIC OR MANUAL OPERATION



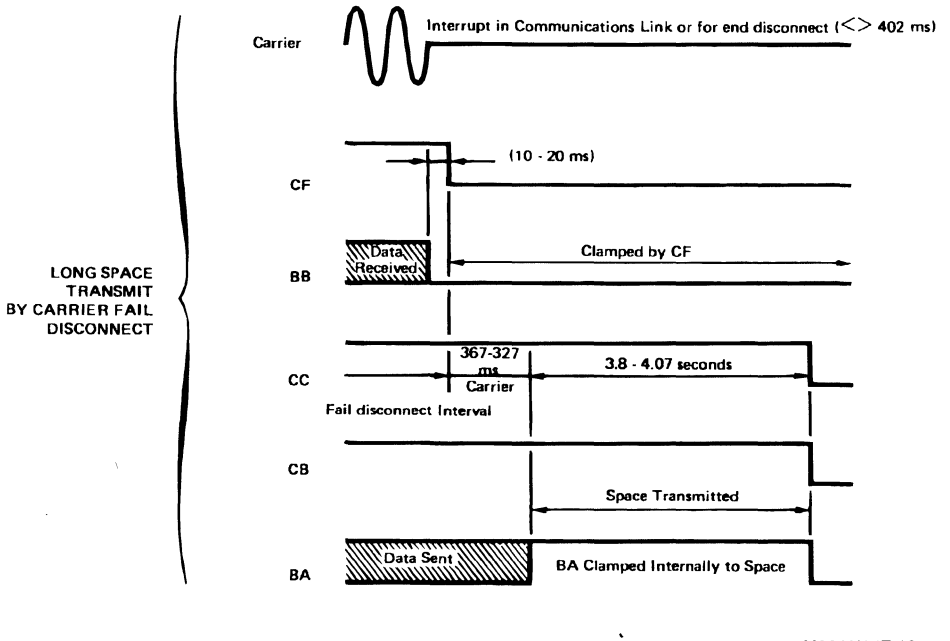
BELL 212A DISCONNECT SEQUENCES (high or low speed)



BELL 212A DISCONNECT SEQUENCES (continued)



BELL 212A DISCONNECT SEQUENCES (continued)



EIA CONNECTOR PIN CONNECTIONS

N°	Name	Direction	Function
1	–	–	No Connection (NC)*
2	BA	to Data Set	Transmitted Data
3	BB	from Data Set	Received Data
4	–	–	NC
5	CB	from Data Set	Clear to Send
6	CC	from Data Set	Data Set Ready
7	AB	–	Signal Ground
8	CF	from Data Set	Received Line Signal Detector
9	+ P	from Data Set	Testing Voltage
10	– P	from Data Set	Testing Voltage
11	–	–	NC
12	CI**	from Data Set	Speed Mode Indication
13	–	–	NC
14	–	–	NC
15	DB**	from Data Set	Transmit Signal Element Timing (data communication equipment source)
16	–	–	NC
17	DD**	from Data Set	Received Signal Element Timing (data communication equipment source)
18	CN**	to Data Set	Make Busy/Analog Loop
19	–	–	NC
20	CD	to Data Set	Data Terminal Ready
21	RL**	to Data Set	Remote Digital Loop
22	CE	from Data Set	Ring Indicator
23	CH**	to Data Set	Speed Select – Originate
24	DA	to Data Set	Transmit Signal Element Timing-data (terminal equipment source)
25	CN**	to Data Set	Make Busy/Analog Loop
	or		
	TM**	from Data Set	Test Mode

* Protective Ground is provided on a screw terminal.
** May be disconnected from interface via options.

3 - TS7515 APPLICATIONS

3.1 - Introduction

This chapter describes a TS7515 based application implemented in SGS-THOMSON Microelectronics application laboratories.

This is stand-alone application for both V.22 and BELL 212A standard requirements.

Following modes of operation are available :
- Manual call mode.
- Manual answer mode.
- Automatic answer mode.

In order to develop a pratical configuration in conjuction with the sub-section called line interface (will be explained in detail later), the interface used was deliberately selected among those currently approuved by telecommunications authorities.

3.2 - Application Diagram

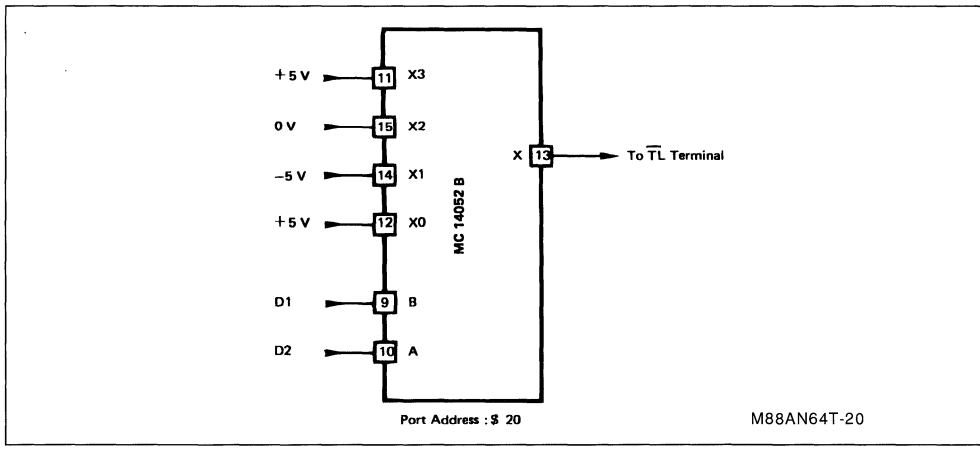
The complete application diagram is given at the end of this chapter.
- Modulation - Demodulation, Transmission-Reception Filtering. Asynchronous-Synchronous Conversion, Scrambling-Descrambling, Carrier Detection functions are accomplished by TS 7515.
  - A 6805 CT single-chip microcomputer, configured in type 2 open mode, executes the modem management functions.
- The program memory is a 2732-type PROM containing the object code.

Since the selected mode of 6805 CT operation uses the available C and D ports for Data and Address Bus, it was a consequence necessary to add 5 bi-directional ports within the area reserved for this function. This explains the presence of 74LS244 and 74LS377 devices.
- Interface to the telephone lines is implemented by "IRC 2000" of LTT whose characteristics will be detailed later.

Additional details concerning the application diagram

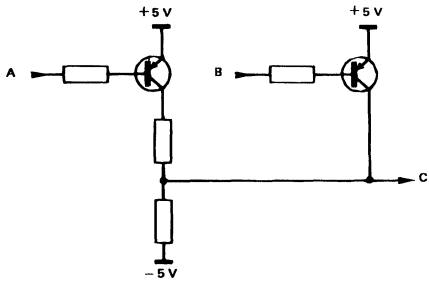
- **MUX 1 multiplexor :** allows transmission of messages issued by the microcomputer during connection establishment or loopback answer sequences.
  (description of software, chapter 4, explains the occurrence of these events).
- **OR Gate connected to Pin 104** : Some particular sequences defined by V.22 and BELL 212A recommendations require the connector pin 104 to go to logic "1" in response to the state of V.24 connector pin 109.
- **MUX 2, MUX 3, MUX 4 Multiplexors :** Some of TS7515 terminals have been designed to accept three-state input signals to perform 3 different functions.
  Suitable translation of these three-state signals is obtained by applying the two logic outputs to an analog multiplexor. Various solutions, two of which are outlined next, are possible.

1 - Using a "4000" series CMOS multiplexor (e.g. MC 14052 B) as shown below (example of type 2 and type 3 loops).



This solution has the disadvantage of requiring one MC 14052 B circuit or equivalent for each 3-state input.

2 - Using a transistor array as shown below.



A	B	C
+ 5 V	+ 5 V	– 5 V
0 V	+ 5 V	0 V
+ 5 V	0 V	+ 5 V
0 V	0 V	+ 5 V

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This alternative offers the advantage of using currently available resistor and transistor arrays thereby achieving component count reduction.

- **Purpose of adjustable resistors for on-line signal transmission/reception**
  Telecommunications authorities have established maximum admissible on-line power level transmitted by any device. In order to comply with these strict limits, a combination of fixed and adjustable resistors is used to achieve signal level adjustment.
  Resistor bridge on receive channel allows adjustment of complete loop gain so as to enable the carrier detection circuit (internal to TS7515) to meet the requirements of V.22 and BELL 212A standards :
  High level : – 43 dBm on-line
  Low level : – 48 dBm on-line

3.3 - Modem Configuration Switches

16 programming switches are available - some of them are used for the selection of modem's operational status (data format, channel selection,...) and the others for monitoring purposes such as maintenance loop, remote loop request, ...

A summary description of these switches is given next.

SWO : BRS (Binary Rate Selection)

Selects Data Transfer Rate as follows :

SW0 Setting	Binary Rate
1	1200 bits/s
0	600 bits/s (CCITT) 300 bits/s – FSK BELL

SW1 : $\overline{L2}$ (Loop 2)

Configures the modem for type-2 maintenance loop operation.

Type-2 loop is intended to enable the station or the network to monitor the error-free operation of both the line (or a section of the line) and the distant modem.

SW1 Setting	Loop 3
1	Deselected
0	Selected

SW3 : $\overline{L3}$ (Loop 3)

Configures the modem for type-3 maintenance loop operation.

This is a local analog loop used to test modem's correct operation. It should be as close to the line as possible.

In the case of our application, this loop is implemented by disconnecting the modem from line which will cause an imbalance of 4-wire/2-wire converter. (further details are given later in this chapter).

SW1 Setting	Loop 3
1	Deselected
0	Selected

SW3 : $\overline{C}$/B

Configures the modem for operation in accordance with CCITT V.22 or BELL 212A standards.

SW4 : $\overline{GT}$ ($\overline{Guard\ Tone}$)

In CCITT V.22 mode of operation, enables or disables the transmission of 1800 Hz guard tone.

When SW3 is switched to "1" level, a 1800 ± 20 Hz guard tone is continuously transmitted while modem is sending in upper channel.

This guard tone is disabled when modem transmits in lower channel.

SW3 Setting	Transmit Channel	
	Lower	Upper
1	Without 1800 Hz	With 1800 Hz
0	Without 1800 Hz	Without 1800 Hz

SW5 : $\overline{SEI}$

Scrambler $\overline{Enable}$/Disable. Employed for debug mode only.

SW6 : $\overline{A}$/O ($\overline{Answer}$/Originate)

Selection of Answer or Originate mode. This switch affects directly the selection of the transmission channel (lower/upper), other channel being automatically assigned to reception.

SW7 : $\overline{ATE}$ ($\overline{Answer\ Tone\ Enable}$)

This switch enables the transmission of the answer tone.
Employed for debug mode only.

SW8 : $\overline{T}$/D ($\overline{Telephone}$/Data)

Allows to switch between telephone line (TPH) and Modem (DATA) connections.

SW9 : RDL (Remote Digital Loop)

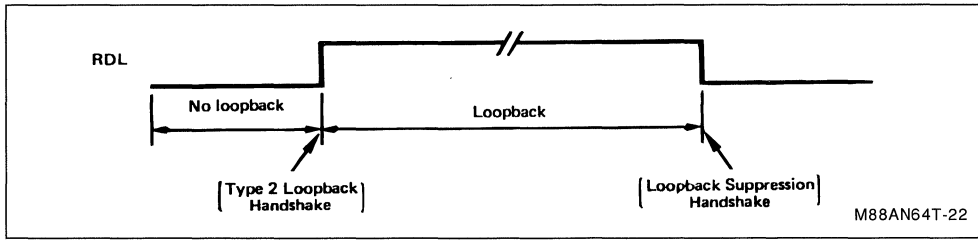
Used to send loop 2 request to remote modem. This request initiates the loopback handshake sequence.

Signals used for type-2 loopback establishment may be transmitted only after the conclusion of contact initiation procedure of synchronization.

When a type-2 loopback sequence is terminated and when RDL switch returns to "0", the modem sends a loopback suppression instruction.

SW10 : AA (Auto Answer)

Enables or disables modem configuration for auto answer capability to incoming calls.



SW11 : $\overline{S1}$/A **SW12 : $\overline{S2}$/A**	Synchronous/Asynchronous Mode Selection
SW13 : CLS **SW14 : OSE**	In asynchronous mode, selects the character length and configures the modem for overspeed function.

Table next page gives all possible configurations.

$\overline{S1}$/A	$\overline{S2}$/A	CLS	OSE	Mode of Operation
0	X	0	0	Synchronous
1	1	0	0	Asyn 9 bits (+ 1 %, – 2.5 %)
1	1	0	1	Asyn 9 bits (+ 2.3 %, – 2.5 %)
1	1	1	0	Asyn 10 bits (+ 1 %, – 2.5 %)
1	1	1	1	Asyn 10 bits (+ 2.3 %, – 2.5 %)
1	0	0	0	Asyn 8 bits (+ 1 %, – 2.5 %)
1	0	0	1	Asyn 8 bits (+ 2.3 %, – 2.5 %)
1	0	1	0	Asyn 11 bits (+ 1 %, – 2.5 %)
1	0	1	1	Asyn 11 bits (+ 2.3 %, – 2.5 %)

x : Don't care.

Remarks concerning the above table

1 - When the application boards is configured for synchronous operation, it is **strictly forbidden** to set CLS and OSE switches to any state other than "0". Any other setting will configure the TS7515 for factory test configurations.
In chapter 4 (Description of Software) the inclusion of this illegal configurations is illustrated.

2 - Note that the following configurations are not available in either asynchronous or BELL 212A modes of operation :
- CLS = 8 bits & CLS = 11 bits
- OSE = + 2.3 %, - 2.5 %

The integrated firmware will alert the user of any illegal configuration.

SW15 : $\overline{RTS}$

Disables the data transmission. Employed for debug mode only.

3.4 - Terminal Interface

Terminal to Application board interconnection is implemented via a 25-pin connector (ISO 2110 standards) mounted on the Printed Circuit Board.

This interface meets both CCITT V.24/V.28 and EIA RS-232C specifications.

CCITT : Comité Consultatif International Télégraphique et Téléphonique.
EIA : Electronic Industries Association.

The following table gives a list of interface connector pins.

Pin Number	CCITT Circuit Number	French Designation	American Designation	Signal Direction Terminal Modem
2	103	ED	BA	–>
3	104	RD	BB	<–
4	105	DPE	–	–>
5	106	PAE	CB	<–
6	107	PDP	CC	<–
7	102	TS	AB	0 Volt
8	109	DS	CF	<–
12	112	–	CI	<–
15	114	HEM	DB	<–
17	115	HRM	DD	<–
20	108	CPD	CD	–>
22	125	IA	CE	<–
24	113	HET	DA	–>
25	142	IE	TM	<–

3.5 - Line Interface

This is a hybrid device inserted between TS7515 and the telephone line.
In general, it performs the following functions :

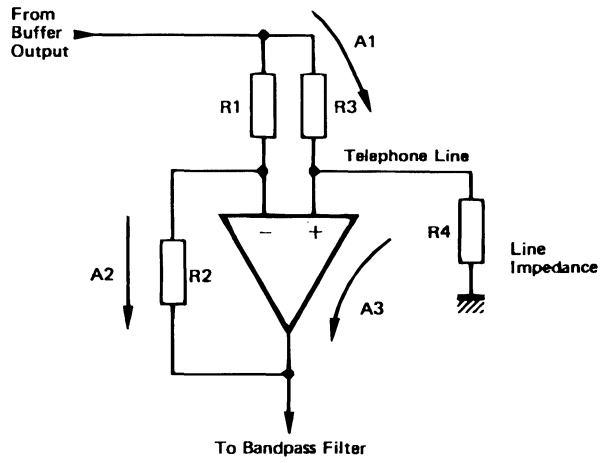
- 4-wire/2-wire conversion.
- Line current regulation.
- Overvoltage protection.
- Ring detection.
- Pulse dialing.
- Telephone/Data switching.
- Galvanic Isolation.

3.5.1 - 4-WIRE/2-WIRE CONVERSION

This configuration employs an operational amplifier - whose duty is to route signals issued by the modulator towards the telephone line - while preventing, by as much as possible, the signal reinjection into the demodulator.

Inversely, it routes the signal received via line towards the demodulator with minimal attenuation.

Figure below illustrates the arrangement of a popular 4-wire/2-wire converter.



The gain between the on-line signal and modulator's output is :

$$A1 = \frac{R4}{R3 + R4}$$

Where R4 is the Line Impedance **theoretically** considered as 600 Ω resistive.

If the line is properly matched, R3 must be equal to R4 :

i.e. R3 = R4 = 600 Ω

therefore : A1 = 0.5

The gain between the modulator and the demodulator (bandpass filter) is given by the following expression :

$$A2 = -\frac{R2}{R1} + \left(1 + \frac{R2}{R1}\right)\left(\frac{R4}{R3 + R4}\right)$$

To obtain a null signal reinjection : A2 = 0

$$\text{i.e. } 0 = -\frac{R2}{R1} + 1\left(+\frac{R2}{R1}\right)\frac{1}{2}$$

after simplification : **R2 = R1**

The gain between the demodulator and the line :

$$A3 = 1 + \frac{R2}{R1}$$

therefore : **A3 = 2**

It is obviously clear that these calculations are purely theoretical. In practice, the line impedance has a complex component whose value varies as a function of the frequency. However, the 4-wire/2-wire converter is considered as acceptable if the Gain "A2" is approximately - 10 dB.

Further discussion on this topic is beyond the scope of the present application note. The interested reader is advised to refer to specialized text books for a full coverage of this subject.

3.5.2 - GALVANIC ISOLATION

This isolation is achieved by a transformer whose rating should be higher than 4500 volts.

3.5.3 - LINE CURRENT REGULATION

The on-chip regulation circuitry maintain the line current within two limits, which vary from country to country according to specifications in force.

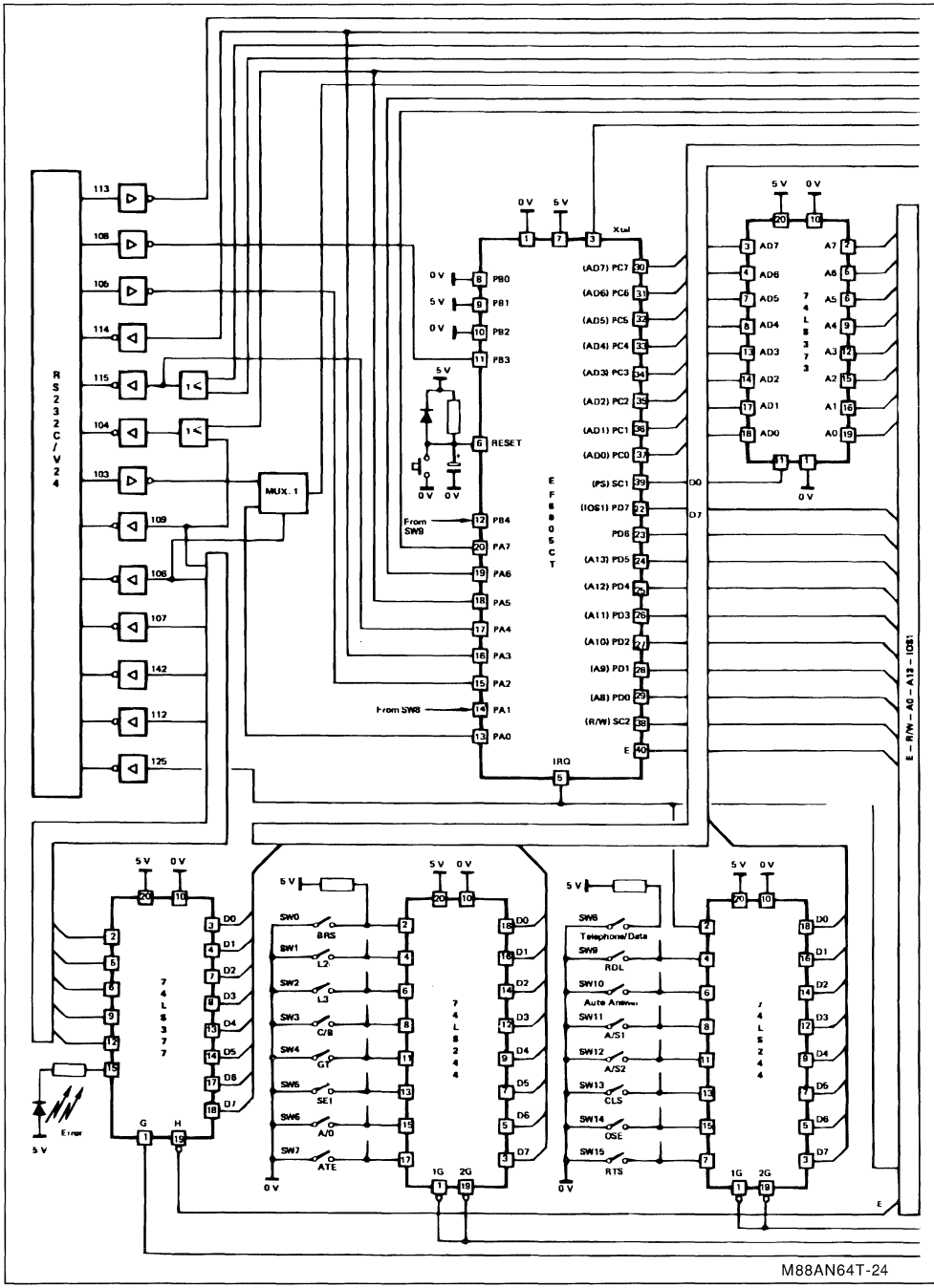
Line Interface Device	Max. Current (mA)	Min. Current (mA)
IRC 2000	50	20

3.5.4 - RING DETECTION

In general, this output delivers a logic signal corresponding to ring signal envelope.

3.5.5 - PULSE DIALING

In the case of IRC 2000, this pin delivers loop disconnect pulses for dialing and modem connection. In addition, it offers the possiblity of telephone connection/disconnection.


RS232C/V24
MUX. 1
EF6805CT
74LS373
74LS244
74LS377
From SW9
From SW8
Xtal
RESET
IRQ
E – R/W – A0 – A13 – IOS1
Error
BRS
L2
L3
C/B
GT
SE1
A/0
ATE
Telephone/Data
RDL
Aute Answ.
A/S1
A/S2
CLS
OSE
RTS

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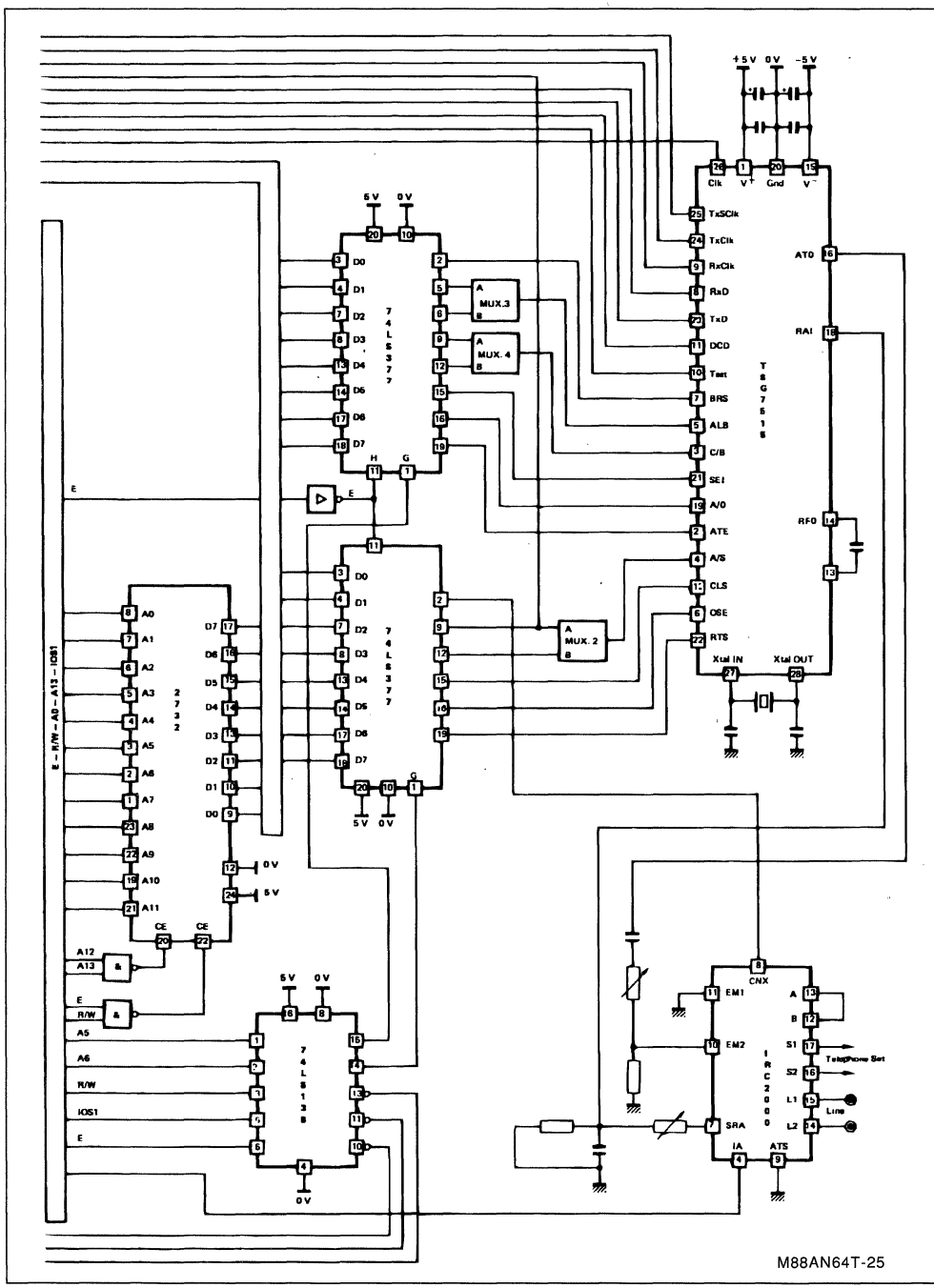

+5V
0V
-5V
Clk
V+
Gnd
V-
TxSClk
TxClk
RxClk
RxD
TxD
DCD
Test
BRS
ALB
C/B
SEI
A/D
ATE
A/S
CLS
OSE
RTS
Xtal IN
Xtal OUT
ATO
RAI
RFO
TEG7515
MUX.3
MUX.4
MUX.2
74LS377
74LS138
2732
E - R/W - A0 - A13 - IOS1
CNX
EM1
EM2
SRA
IA
ATS
S1
S2
L1
L2
Telephone Set
Line
IRC2000
M88AN64T-25

4 - DESCRIPTION OF SOFTWARE

4.1 - Definition of software modules

Each individual module given in this chapter is intended for a particular function. They cover the occurence of events sequentially from the time of modem's initial power on until the completion of online information transfer.

4.1.1 - IDLE STATE MANAGEMENT MODULE

- Microcomputer configuration.
- V.24 connector initialization.
- Interface disconnection from line.
- Read the settings of programming switches, monitor absence of error and configure the TS7515 according to switch settings.
- Loop 3 management.
- Wait for an event causing connection to line.

4.1.2 - CCITT HANDSHAKE MODULE.

- V.25 sequence.
- Answer handshake.
- Originate handshake.

4.1.3 - BELL HANDSHAKE MODULE

- 1200 Originate handshake.
- 300 Originate handshake.
- Answer handshake.

4.1.4 - CCITT TRANSMISSION MODULE

- Telephone line monitoring (appearance of special sequences).
- V.24 connector management.
- Monitoring several switch settings.
- Monitoring DCD terminal of TS7515.

4.1.5 - BELL TRANSMISSION MODULE

Identical to preceding CCITT module. In addition, it provides for the identification of "Long Space" for line disconnection.

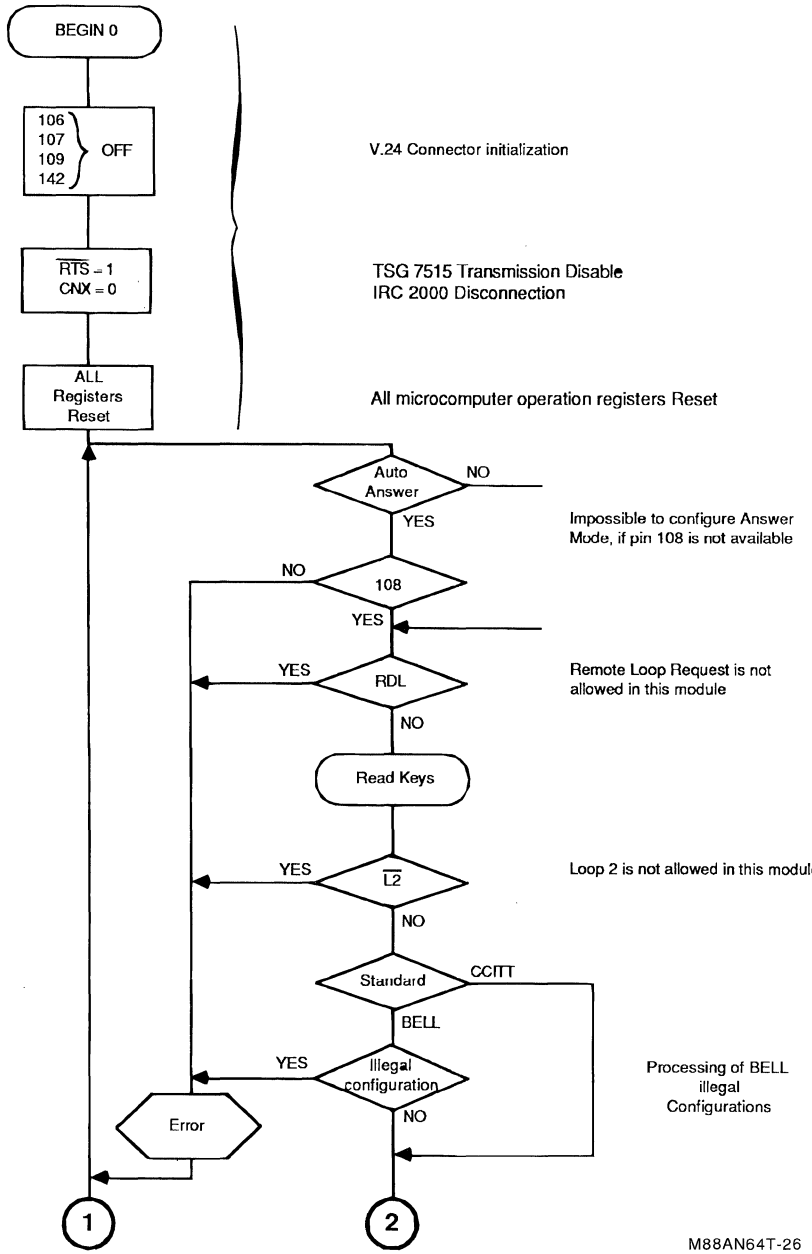
4.1.6 - RDL HANDSHAKE MODULE

Protocol used for the initiation of remote loop sequence.

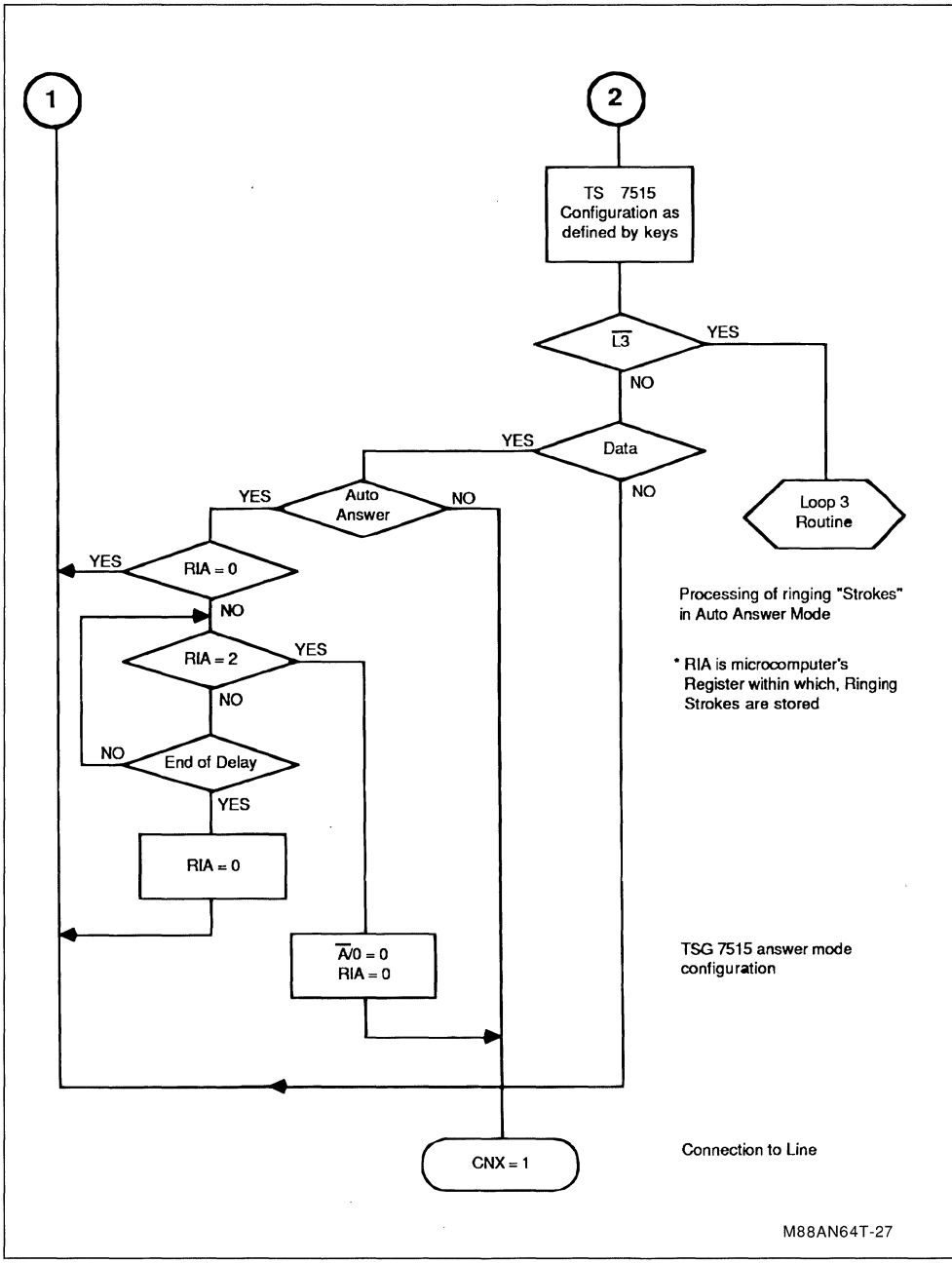
4.1.7 - LOOP 2 RECEIVE HANDSHAKE MODULE

Protocol for the reception of type-2 loopback request initiated by distant modem.

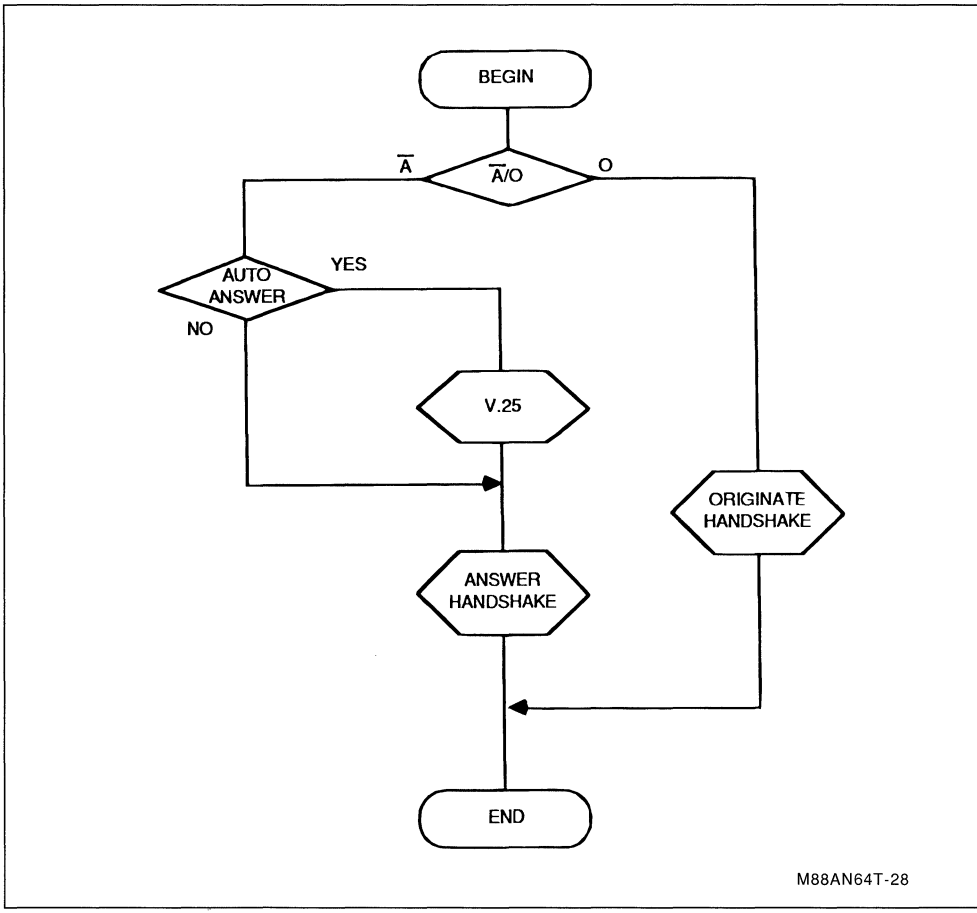
IDLE STATE MANAGEMENT MODULE



IDLE STATE MANAGEMENT MODULE (continued)

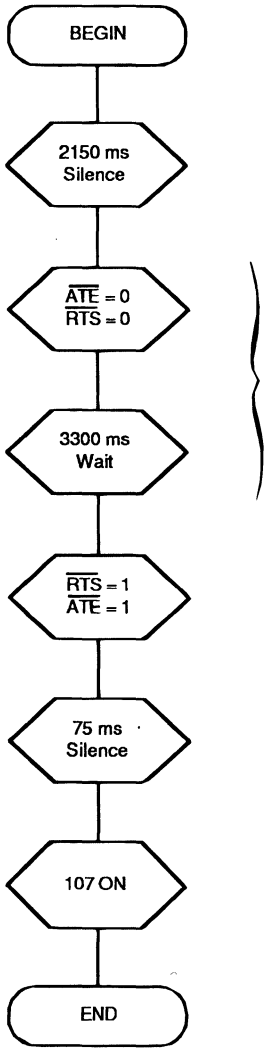


CCITT HANDSHAKE MODULE



This flowchart illustrates clearly the sequence of events. In the case of manual answer, the software will ignore the V.25 module.

V.25 SEQUENCE



2150 ms Silent Interval

Answer Tone transmission for 3300 ms

Stop answer tone Transmission

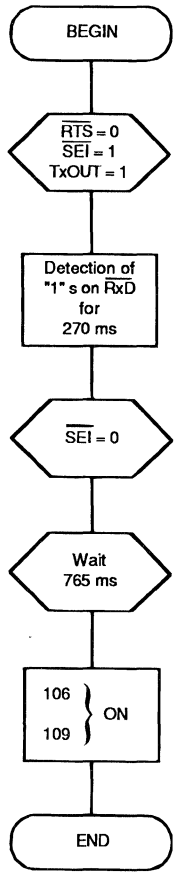
Absence of carrier transmission for 75 ms

Connector Signal "Data Set Ready" at active level

M88AN64T-29

Comment : Writing this sequence meets no difficulty.
Only, CCITT recommendations must be carefully observed.

ANSWER HANDSHAKE SEQUENCE



Transmission of non scrambled "1" s

Detection of scrambled is issued by the distant Modem for a period of at least 270 ms

Scramber Enabled

Delay

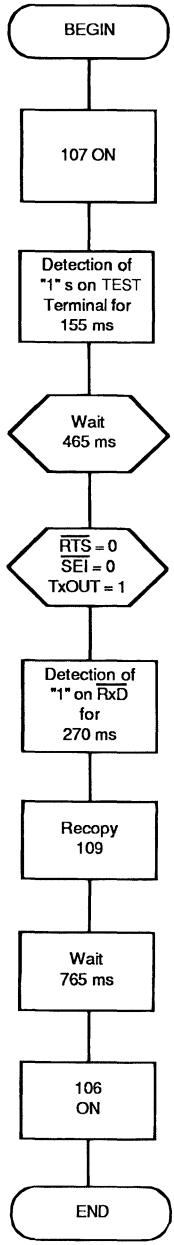
Connector pins conditioned

M88AN64T-30

Comments : Detection of scrambled "1" on RxD terminal for an interval of 270 ms is performed as follows :

The sequence begins within a loop searching to detect a logic "1" on RxD terminal while simultaneously, a 15-second "time out" is initiated. If within the loop a logic "0" is detected on RxD pin, 270 ms count is reset but the "time out" continues. The sofware sequence will return to the starting point (i.e. idle state management), if at the end of 15-second interval a sequence of continuous "1"s for a 270 ms duration has not been found.

ORIGINATE HANDSHAKE



This interval corresponds to the period during which the distant Modem transmits non scrambled "1" s

Delay

Transmission of scrambled "1" s

Detection of scrambled "1" s issued by distant Modem

Detection of scrambled "1" s issued by distant Modem

Delay

Connector pin 106 conditioned

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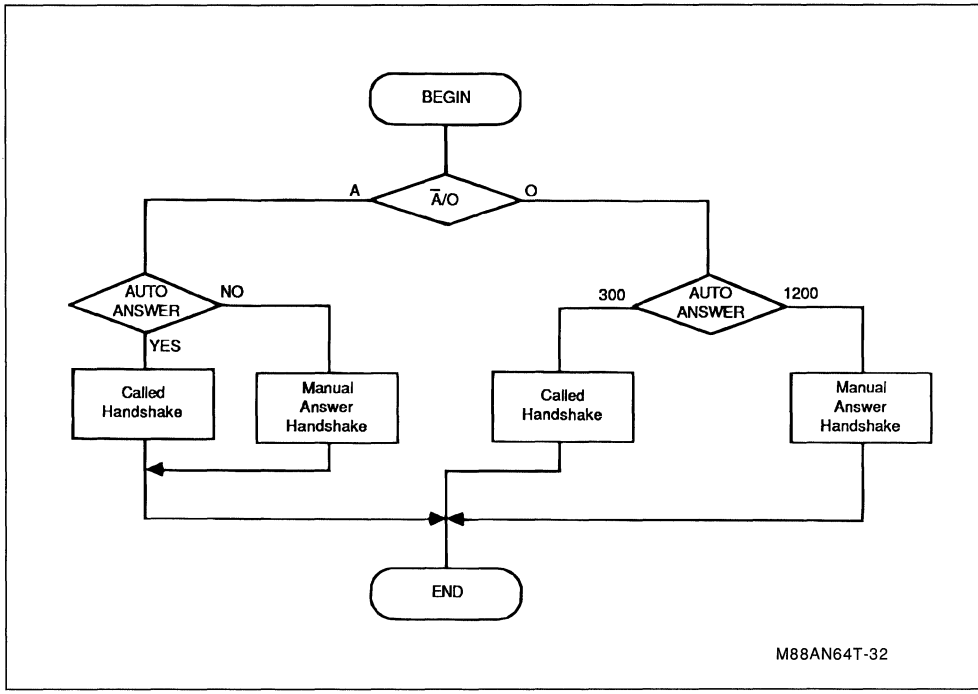
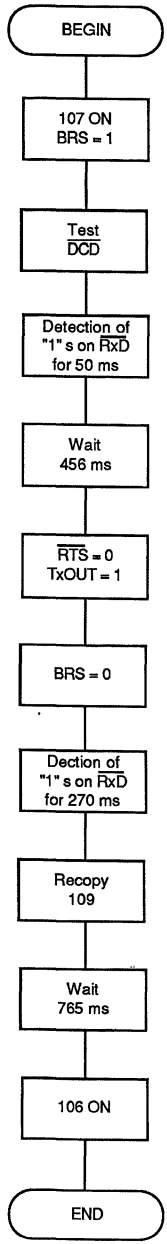
BELL HANDSHAKE MODULE



1200 ORIGINATE HANDSHAKE



Change to FSK mode

Test to detect presence of 2225 Hz

Delay

Transmission of scrambled "1" s

Change to DPSK mode

Detection of scrambled "1" s sequence originated by distant modem

Connector configuration

Delay

Connector configuration

M88AN64T-33

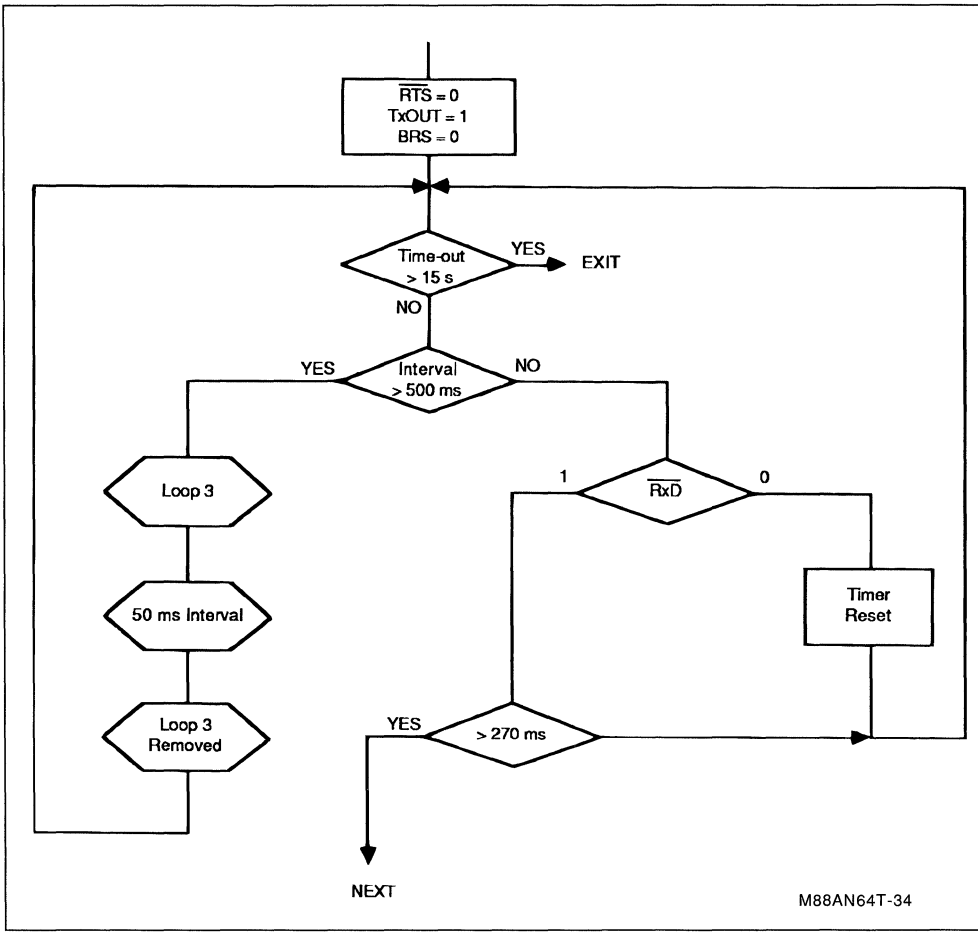
Important : Sequence of events in BELL Answer Mode differs slightly from equivalent CCITT sequence as follows :

There is no transistion between the transmission of **Answer Tone** and **Scrambled "1"s Sequence**.

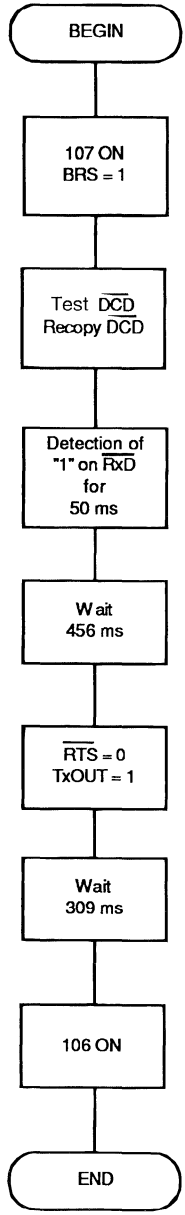
In the case of TS7515 and upon the appearance of scrambled "1"s sequence, this may result in "Carrier DPLL" locking on an incorrect frequency.

An efficient solution to overcome this problem would be to program the TS7515, for a short interval, in loop 3 configuration.

The following flowchart illustrates this recommended solution.

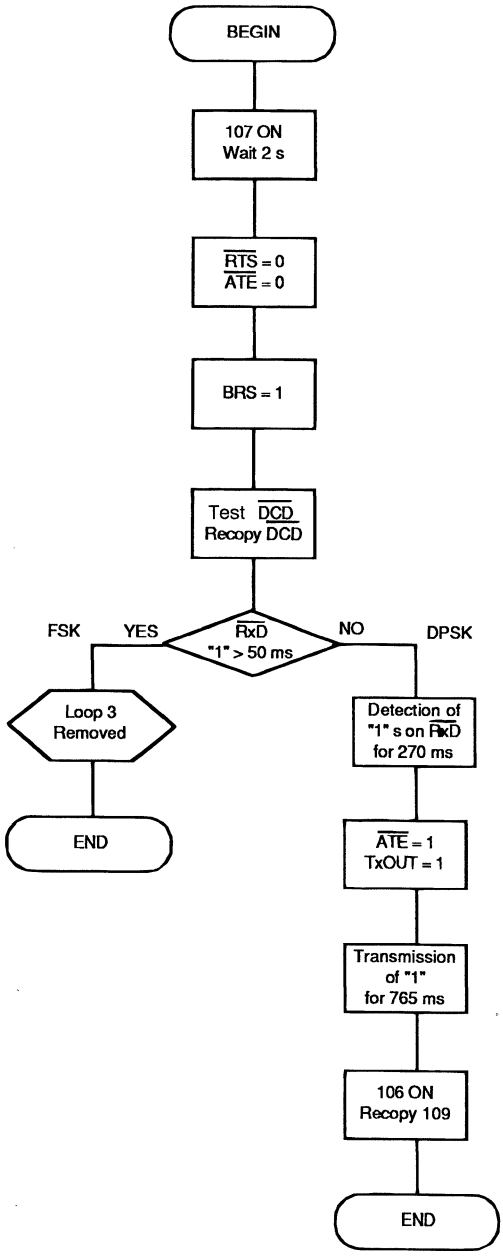


300 ORIGINATE HANDSHAKE



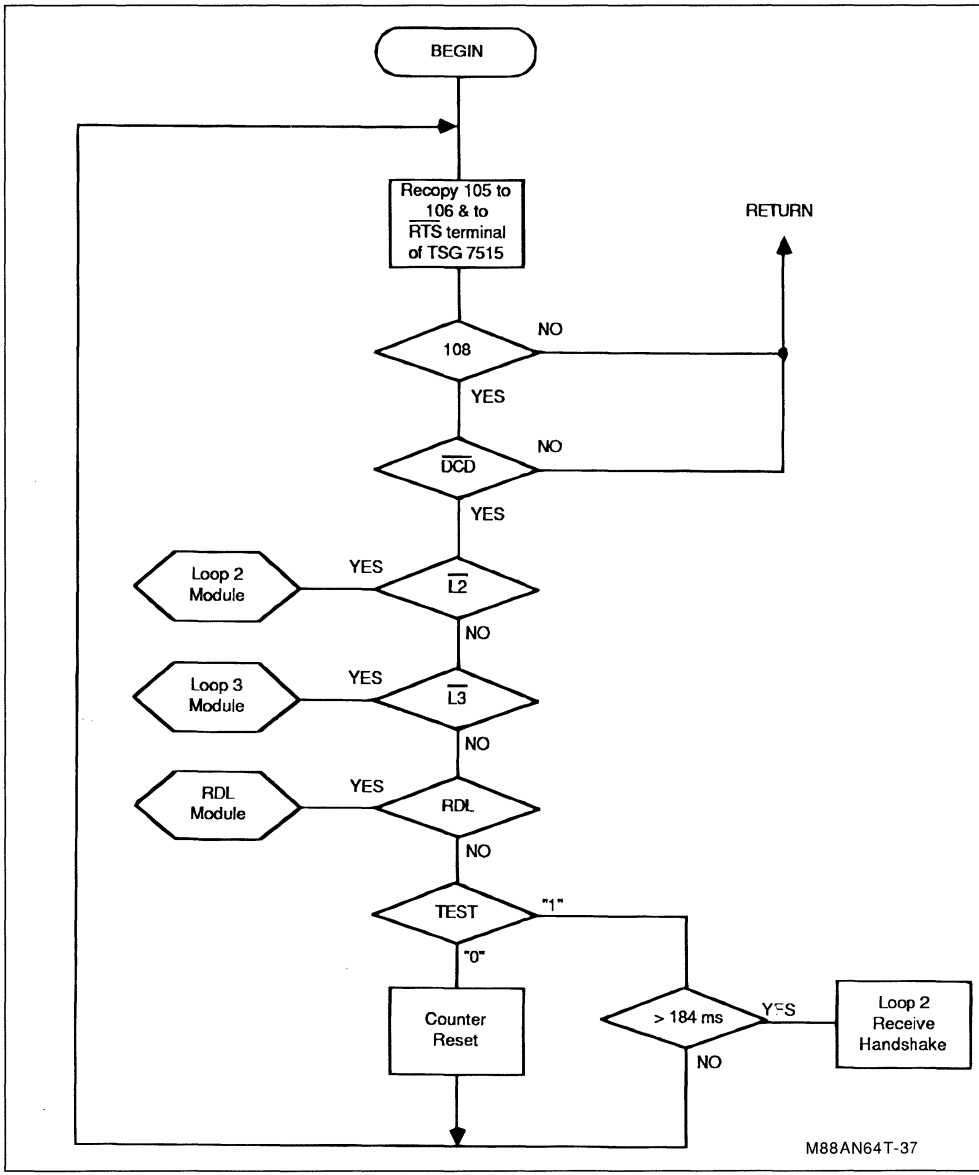
M88AN64T-35

ANSWER HANDSHAKE



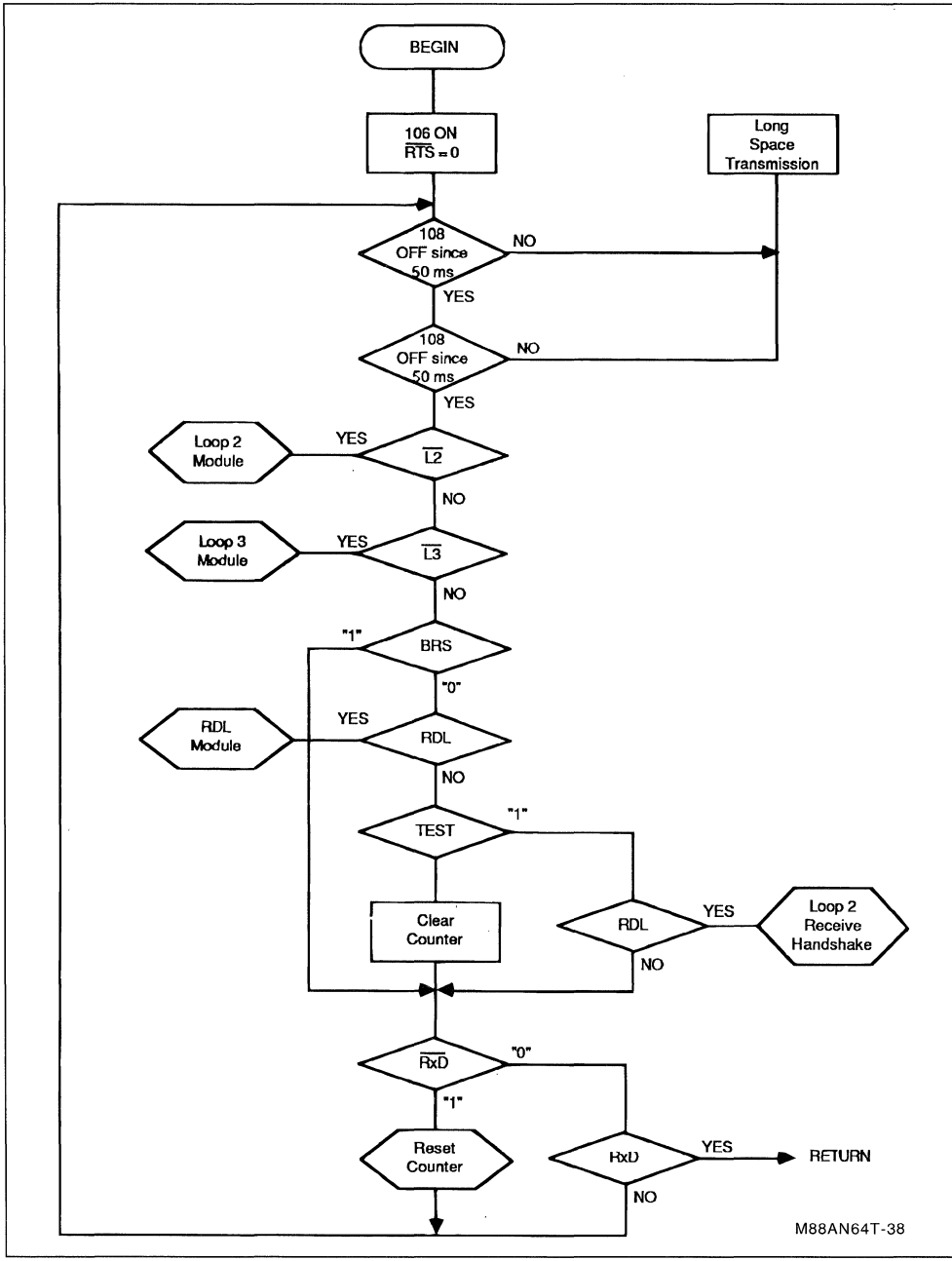
M88AN64T-36

CCITT TRANSMISSION MODULE

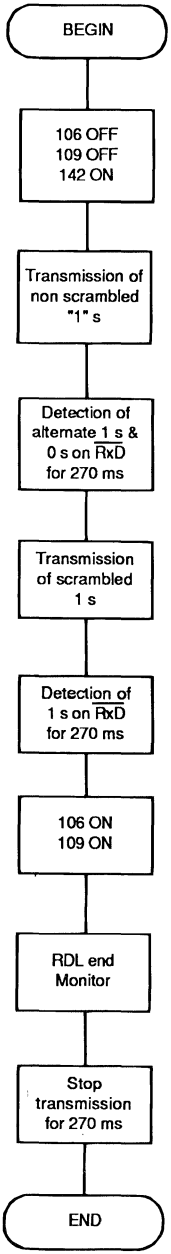


The duty of this module is to monitor either the user connector to detect a line disconnect sequence, or to monitor the telephone line since programming switch settings may cause occurence of special on-line sequences.

BELL TRANSMISSION MODULE



RDL HANDSHAKE MODULE



Configuration of the user connector

Transmission of RDL Request Sequence

Detection of answer to this Request

End of RDL Request Signal
and transmission of scrambled "1" s

Detection of signal "echoed" by distant Modem on $\overline{RxD}$ terminal

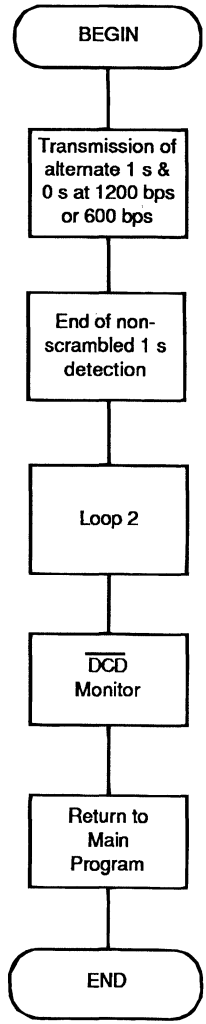
Configuration of the user connector

Monitopring of RDL key

Transmission of loopback suppression sequence

M88AN64T-39

LOOP 2 RECEIVE HANDSHAKE MODULE



Answer to Loopback Request

Dectection of trigger signal loss

Loop 2 programming of TS 7515

A waiting Loop 2 end

M88AN64T-40

APPENDIX A - TS7515 HANDLING PRECAUTIONS

A.1 - Power supplies decoupling and layout considerations

Power supplies to digital systems may contain high amplitude spikes and other noise. To optimize performances of the TS7515, operating in close proximity to digital systems, supply and ground noise should be minimized. This involves attention to power supply design and circuit board layout.

The power supplies should be bypassed with tantalum or electrolytic type capacitors to obtain noise-free operation. These capacitors should be located close to the TS7515. The electrolytic type capacitors should be bypassed with ceramic capacitors for improved high frequency performance.

Power supply connections should be short and direct. Ground loops should be avoided.

Coupling between analog inputs and digital lines should be minimized by careful layout. The RDI input (pin 13) is extremely sensitive to noise. The connection between this point and RFO (pin 4) throu a ceramic type capacitor should be as short as possible and coupling between this connection and digital signals should be minimized by careful layout.

A.2 - Carrier Recovery Loop

This carrier recovery loop utilizes a digital phase-locked loop. Performances of the TS7515 depend directly on this DPLL which needs to be reset prior to the reception of a DPSK carrier.

TS7515 offers three possibilities of resetting this DPLL :

- A trailing edge on $\overline{DCD}$ terminal.
- Switching from FSK mode to DPSK mode.
- Changing the receive channel.

These three possibilities of resetting the DPLL should be integrated within the microcontroller so as to provide for various set-up and handshake procedures.

Timing diagrams given in chapter 2 illustrate examples of V.22/V.25 and BELL 212A received signals in originate mode.

A.3 - Frequency Precision of Crystal Oscillator

In order to meet the frequency precision of the transmission baud rate required by V.22 and BELL 212A specifications, it is recommended to use a crystal oscillator whose series resonance frequency precision is better than 0.01 % with respect to the theoretical frequency of 4.9152 MHz.

Such precision would be feasible by optimizing the capacitance values spread around the quartz oscillator.

APPENDIX B - GLOSSARY OF TERMS

Acoustic Coupler : A device that permits the use of a telephone handset as a connection to dial-up telephone lines (rather than a direct connection using DAA interface) for data transmission by means of sound transducers. Usually implemented for call origination, and is frequently used with portable terminals.

Analog Loopback : A diagnostic mode whereby the transmitted analog output is internally connected to the analog received signal input in a single band (determined by A/0 pin) so that the device's entire signal path is under test.

Answer Tone : A tone returned by the answering modem to the originating modem and the network.

ASCII : American Standard Code for Information Interchange. This is a seven-bit-plus-parity code established by the American National Standards Institute (Formerly American Standards Association) to achieve compatibility between data services. Also called USASCII.

Attenuation : The difference between transmitted and received power due to transmission loss through equipment, lines or other communications devices.

Asynchronous Transmission : A data transmission scheme that handles data on a character-by-character basis (without synchronization by a clocking signal). Time intervals between transmitted characters may be of unequal length. The character code includes a "start" bit to identify the beginning of a data character, a "stop" bit (or bits) to identify the end of the data character and a "parity" bit to check for errors in transmission. Also called "Start-Stop" transmission.

Auto-Answer : A circuit in a modem system that can automatically make a connection on the switched telephone system when its number is dialed.

Automatic Dialer : A device which will automatically dial telephone numbers on the switched telephone network. An automatic dialer can be easily incorporated into a TS7515 - based modem system.

Bandpass Filter : A filter circuit that passes a single band of frequencies and filters out, or excludes, all others.

Bandwidth : The range of frequencies assigned to a channel or system ; the difference expressed in Hertz (Hz) between the highest and lowest frequencies of a band.

Baud : A unit of signalling speed equal to the number of modulations or signal events per second. In FSK synchronous transmission, the unit of signalling speed corresponding to one unit interval per second ; that is, if the duration of the unit interval is 20 milliseconds, the signalling speed is 50 baud. Baud is the same as "bits per second" only if each signal event represents exactly one bit, as in the frequency-shift keyed TS7515 modem.

As used in the TS7515 four-phase PSK transmission, every two bits of digital data are encoded into dibits (1 dibit = two bits) for translation or modulation into phase shift information. In PSK the baud rate is one-half the bit rate.

Bit Error Rate (BER) : A measurement of the average number of bits transmitted before an error occurs. Usually expressed as the reciprocal of the average.

Bit Rate : For modems using voicegrade telephone lines, the bit rate equals the data rate. The baud rate is the actual number of times per second that the transmited carrier is modulated or changes state. Each modulation may represent multiple bits.

Carrier : An analog signal fixed in amplitude and frequency that can be combined in a modulation process with a second information-bearing signal to produce a signal for transmission.

CCITT (Comité Consultatif International de Télégraphie et Téléphonie) : An international committee established by the United Nations to recommend international telecommunications standards of transmission within the International Telecommunications Union (ITU).

Channel : A communications path providing signal transfer in a single direction at a time.

Circuit Grade : The grades of circuits are broadband, voice, sub-voice and telegraph. Circuits are graded on the basic line speed expressed in characters per second, bits per second, or words per second.

Coherent Detection : A method of phase-shift detection, used in the TS7515 PSK modem, in which the received modulated signal is compared with a purified and locallygenerated reference frequency, instead of using the instantaneous value of the received carrier frequency (which is often distorted).

Common Carrier : A company which dedicates its facilities to a public offering universal communications services and which is subject to public utility regulations.

DAA (Data Access Arrangement) : Originally this term was used to define a device, provided by the telephone company, which was used to connect privately owned or customer provided equipment (data sets) to the switched telephone network.

dB (Decibel) : The decibel is defined by the ratio of output signal power to input signal power as dB = 10 Log 10 (Output Power).

Note that if the output power is less than the input power, the logarithmic result is negative. In this case the line is said to have a loss of that many dB.

dBm : Input and output signal powers may be related to a specific level called a dBm for reference purposes. Zero dBm (log 1 = 0) equals 1 mW dissipated in 600 Ω impedance. The reference frequency used in most circuits in 1000 Hz. Measurements relative to reference frequency are expressed in decibels relative to 1 mW as follows :

dBm = 10 log 10 (Signal Power in mW/1 mW)

Thus, zero dBm means 1 mW and absolute power levels may be expressed as so many dBm.

dBSPL : In acoustics, the unit commonly utilized to measure sound pressure level or dBSPL. The zero reference for this measurement is 0.0002 dynes per square centimeter.

dBv : Microphone sensitivities are commonly related to a specific level called a dBv for reference purposes. Zero dBv (log 1 = 0) represents one mW dissipated in 1000 Ω impedance. The unit dBv is expressed in terms of the peak voltage of a signal reference to one volt.

dBv = 20 log 10 (Peak Voltage of Signal/1 volt)

DCE (Data Communications Equipment) : Consists of the modem and any other equipment related to the transmission or reception of analog signals over the telephone lines, such as the FCC-approved Registered Protective Circuit.

Data Set :
- A modem.
- A collection of similar and related data records.

DTE (Data Terminal Equipment) : The digital equipment to which a data communications path begins or ends.

Demodulator : A component of a modem which recovers data from received analog signals and converts them to a form suitable for the DTE.

Descrambler : A device or circuit that transposes or decodes a demodulated signal to restore the original data prior to transmission by the remote transmitter and scrambler.

Digital Loopback : A means of routing data from the transmit path back to the received data path by switches, as a means of testing a modem.

Equalization : Compensation for the increase of attenuation with frequency. Its purpose is to produce a flat frequency response.

FSK (Frequency Shift Keying) : A method of frequency modulation which varies the carrier frequency at significant instants by smooth as well as abrupt transitions.

Full Duplex : Simultaneous two-way independent transmission in both directions on a communications channel. Also called Duplex.

Cross Distortion : Distortion is an undisred change in a signal or data transmission. The primary sources of distortion in modem communication are in speed differences between the Data Terminal Equipment (DTE) and the modem, and circuit variations and noise. The maximum gross (total) distortion in modem communication is 45 %, as defined by EIA standards RS-404.

Half Duplex : A circuit designed for transmission in either direction, but not in both directions simultaneously. A modem in half-duplex mode will be either transmitting or receiving, but not both at the same time.

Handshaking : An exchange of predetermined signals when a connection is established between two modems.

Host Computer : A computer attached to a network providing primary services such as computation, data base access, special programs, or programming languages.

Information Bit : A bit generated by the data source which is not used fo error control.

Impulse Noise or Surge : A type of high-amplitude short-duration interference on communications lines caused by events such as lightning, electrical sparking action, make/break action of switching devices, or electrostatic discharge. A registered protective network is required to protect the modem from such voltages which occur on communications lines.

Mark : A logic one, or the presence of current or carrier on a digital communications channel in the idle condition. Compare with space.

Parity Check : Addition of non-information bits to data, making the number of ones in each group either always even (for even parity) or odd (for odd parity).
This permits single error detection in each group.

Phase Locked Loop : An electronic servo system controlling an oscillator so that it maintains a constant phase angle relative to a reference signal source.

PSK (Phase-Shift Keying) : A type of phase modulation in which the modulation function shifts the instantaneous phase of the modulated wave between predetermined discrete values.

Protocol : A procedure used to control the orderly communications between stations on a data link. Examples of protocols are HDLC, SDLC, and Synchronous Bit-Oriented protocols.

QAM (Quadrature Amplitude Modulation) : One form of-4-level differential Phase-Shift Keying.

Reference Clock : A clock of high stability and accuracy used to govern the frequency of a network of mutually synchronized clocks of lesser stability.

RDL (Remote Digital Loopback) : A type of test in which a signal is transmitted from a local modem to a remote modem, or other device or switch, to loop the remote received data back to the sending modem to measure or test the modem, communications line, remote modem or device, or the entire circuit.

Scrambler : A device or circuit that encodes a data signal at the transmitting modem, to make it unitelligible for data security purposes (at a receiver not equipped with an appropriate descrambler), and to maintain carrier detect lock during idle or slow data rate input.

Serial Transmission : A method of transmission in which each bit of information is sent sequentially on a single channel, rather than simultaneously on several channels, as in parallel transmission.

SNR (Signal-to-Noise Ratio) : The ratio of the signal power to the noise power on a communications line, expressed in dB.

Space : A logic zero, or the absence of current or carrier on a digital communications channel. Compare with Mark.

Start Element : In character synchronous (start-stop) transmission, the first element in each character, which serves to prepare the receiving equipment for the reception and registration of the character.

Start-Stop Transmission : Asynchronous transmission in which a group of code elements are preceded by a start element (or bit) and ended with a stop element (or bit).

Statistical Equalizer : A modem compensation circuit which provides equalization of a communications line based on the average switched telephone line circuit distortion.

Stop Element : In character asynchronous (start-stop) transmission, the last element in each character, to which is assigned a minimum duration, during which the receiving equipment is returned to its rest (idle) condition in preparation for receiving the next character.

Switched Line : A communications link for which the physical path may vary each time it is used, as in the dial-up (switched) public telephone network.

Synchronous Transmission : A data transmission scheme in which the data characters and bits are transmitted at a fixed rate with the transmitter and receiver synchronized. This eliminates the need for start-stop elements, thus providing greater efficiency.

APPENDIX C - BIBLIOGRAPHY

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  August 1969

TS7513 V.23 MODEM PRINCIPLE AND APPLICATIONS

ABSTRACT

The present Application Note outlines the basic application principles of TS7513 circuit. A typical application and its performances are also discussed.

INTRODUCTION

TS7513 circuit of SGS-THOMSON Microelectronics offers a low cost solution with a minimum of external components to achieve MODEM applications compatible with the applicable CCITT recommended standard for V.23 type modems. In fact, this circuit provides all modulation, demodulation, and filtering functions required for FSK modulated data transmission via either public switched telephone networks or leased data links. Control signal are compatible with CCITT recommended standard for V.24 junction.

FUNDAMENTAL PRINCIPLES

One of the most important applications is to connect a terminal via telephone network to a central computer for data acquisition or information retrieval purposes.

Public switched telephone network is generally designed for voice transmission and as a consequence, have a frequency band of 300 Hz to 3400 Hz.

Consequently, the data transmission must be performed via a modem circuit which will convert the binary data into analog signals falling within the voice-frequency band.

Using public switched telephone network is an economic solution since the required installation already exists on customer location. Nevertheless, telephone lines impose an important restriction which is data transmission rate. This is directly due to the channel bandwidth of the transmission lines. As a result, a bidirectional simultaneous transmission is only possible if the two transmission channels are adequately separated and fall within the frequency band authorized by the channel.

For a system employing the V.23 CCITT standard, the TS7513 allows for a simultaneous data exchange, as indicated below :

- On main channel, with a 1200-baud modulation rate. The two frequencies used are $f_0 = 2100$ Hz and $f_1 = 1300$ Hz.
- On back channel, with a 75-baud modulation rate. The two frequencies used are $f_0 = 450$ Hz and $f_1 = 390$ Hz.

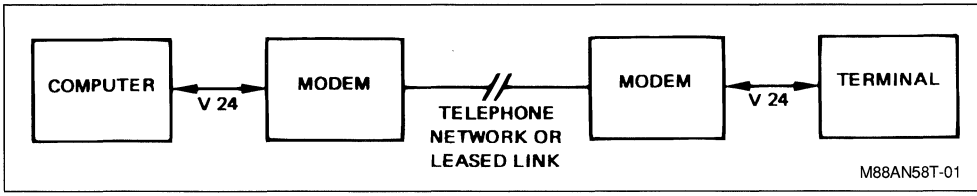
For the situation where TS7513 is used to link a remote terminal to a host computer, the data transfer from the host computer to the terminal is done on the main channel and takes place at a much higher rate than in the opposite direction. The back channel is used by the remote terminal to communicate with the host computer. In general, these communications are short and consist of, for example, typed messages entered via a keyboard.

The function of a MODEM is to allow via public switched telephone network or leased data links, a bidirectional data transfer between two distant computer-based systems.

Figure 1 illustrates an example where a computer and a terminal are linked via two modems.

Operating principles are quite simple. The modem receives the data to be transmitted in digital form, converts it to analog signal (MODULATION) suitable for transmission over telephone lines. Inversely, it receives analog signals transmitted from distant station, converts them back to digital form (DEMODULATION) suitable for the computer.

Figure 1 : Computer to Terminal Link Via Modems.



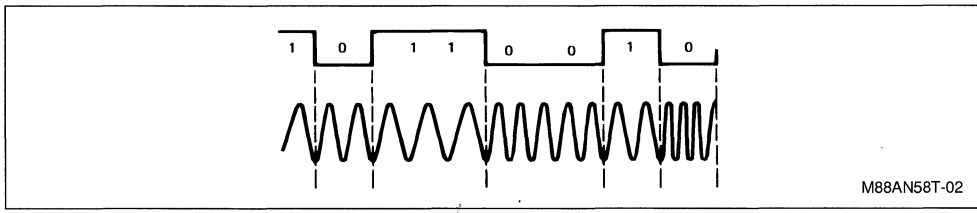
One of the most commonly employed techniques in digital signal transmission is FSK (Frequency Shift Keying) modulation. In this system, 2 frequencies f_0 and f_1 are used to represent digital levels "0" and "1" respectively.

In transmit mode, the modem receives binary data supplied for example by a microcomputer or by an UART (Universal Asynchronous Receiver Transmitter). When a logic "0" is detected the modem outputs a sinewave signal of frequency f_0. Likewise, for a logic "1" the modulator outputs a sinewave signal of frequency f_1.

Binary digital data are so converted by the modem to analog signal containing 2 different frequencies of f_0 and f_1 with of course, a continuity in phase (see figure 2). The analog signal so obtained, must be correctly filtered in order to eliminate the transmission of frequencies other than f_0 and f_1.

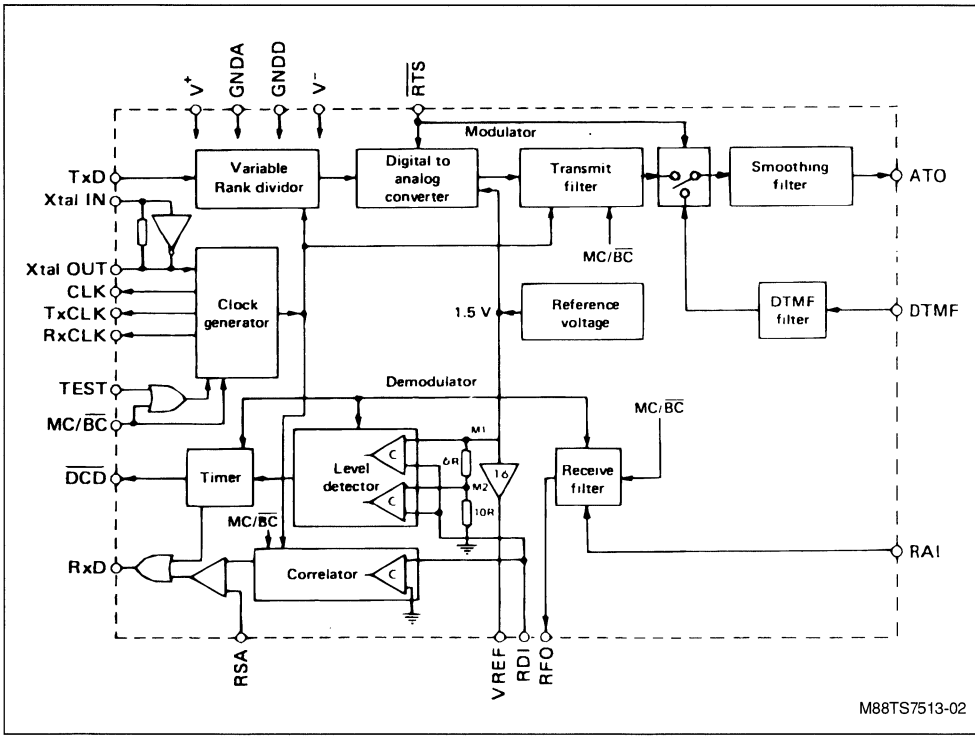
Inversely, the demodulator receives via telephone line, a FSK modulated analog signal. This signal is first applied to a band-pass filter which removes all frequencies outside the modem reception band. The signal is then converted to digital form and applied to the computer system.

Figure 2 : FSK Modulation.



With a minimum of external components, the TS7513 performs all of the functions just described. In addition to modulation and demodulation of signals, this circuit contains all necessary filtering for reception and transmission, while signals compatible with CCITT V.24 recommendation are also provided.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

CLOCK GENERATOR

TS7513 master clock can be generated either from a quartz oscillator with a standard 3.579545 MHz frequency connected across pins XtalIN and XtalOUT, or from an external CMOS clock connected to pin XtalIN. The clock generator generates :

- The internal clocks required to operate the modulator, demodulator and the various filters.
- The external clocks (CLK, TxCLK, RxCLK) required to operate the following related circuits :
  - CLK : oscillating at the same frequency as the crystal 3.579545 MHz, the clock is used to control the DTMF frequency generator : the EFG7189 circuit (see application).
  - TxCLK/RxCLK : used to control the UART (Universal Asynchronous Receiver Transmitter), these two variable frequency clocks are equal to 16 times the transmission (TxCLK) and reception (RxCLK) modulation rate.

Pin	Modulation	Demodulation	Frequency
CLK	X	X	3.579545 MHz
T x CLK	75 Bauds	X	1200 Hz
	1200 Bauds	X	19200 Hz
R x CLK	X	75 Bauds	1200 Hz
	X	1200 Bauds	19200 Hz

REFERENCE VOLTAGE REGULATOR

The reference voltage generator generates an internal reference voltage with a 1.5 V nominal value used to calibrate the amplitude of the signal transmitted and to define the two demodulator detection thresholds. After amplification, the reference voltage output goes out to VREF pin (VREF = – 2.4 V). With an external potentiometer a fraction of this voltage is applied to RSA input pin in order to adjust the bias distortion (see application).

3.4 kHz LOW PASS FILTER

This filter with the input connected to DTMF input pin is used to modify the DTMF transmission spectrum.

The filter output is connected to a multiplexer controlled by $\overline{RTS}$ logic signal. The DTMF frequency couple is sent to a smoothing filter and transmitted to ATO pin.

MODULATOR

The modulator receives binary data from a source such as an UART or a V.24 junction and converts them into an analog signal using frequency modulation (FSK).

This signal is transmitted over the telephone network via an appropriate interface.

The modulator comprises the following :

- A variable rank divider generating the four transmission frequencies, i.e. 390 Hz, 450 Hz, 1300 Hz, 2100 Hz.
- A digital/analog converter used to synthesize the sinewave signals.
- A transmission filter with the response depending of the modulation rate. A smoothing filter is added to this transmission filter in order to eliminate the noise generated by the transmission filter switching capacitors.

The modulator is controlled by three digital inputs ($\overline{RTS}$, MC/$\overline{BC}$, TxD) and transmits a signal to ATO pin.

When $\overline{RTS}$ pin is low, ATO pin sends a signal from the modulator. When $\overline{RTS}$ pin is high, ATO pin sends a signal from DTMF input. With no DTMF frequency generator connected, DTMF pin on TS7513 should be set to 0 V.

$\overline{RTS}$	ATO
" L "	FSK Modulated Signal
" H "	DTMF Signal

The signal applied to MC/$\overline{BC}$ (Main Channel/Back Channel) pin selects the frequency couple to be transmitted. Each couple consists of a high frequency (f_0) and a low frequency (f_1). With respect to the couple selected on MC/$\overline{BC}$ pin and with $\overline{RTS}$ pin low, the modulator outputs a high frequency (f_0) if TxD (Transmit Data) input is low ("0"), and a low frequency (f_1) if TxD input is high ("1").

MC/$\overline{BC}$	Modulation Rate	T x D	R .35 and V .23 Recommandations (Hz)
GNDD	75 Bauds	" H " " L "	390 ± 2 450 ± 2
V+	1200 Bauds	" H " " L "	1300 ± 10 2100 ± 10

For transmission spectrum optimization, frequency switching is established with phase continuity.

DEMODULATOR

The demodulator receives on RAI pin via a line interface a frequency modulated analog signal from the telephone network and converts this signal into binary data. The binary data is transmitted via RxD pin over a V.24 junction to a computer or a terminal.

The demodulator consists of the following :

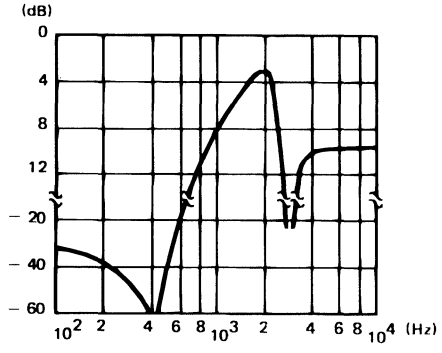
- A receive filter with 2 parts :
  - a 12 kHz rejector to eliminate taxation frequency at 1200 bauds or 75 bauds,
  - a band-pass filter with a response related to the frequency couple received.
- A frequency-voltage converter or frequency discriminator with self correlation capable of demodulating at 75 bauds or 1200 bauds.
- A time-delayed hysteresis level detector where the time delay is related to the frequency couple received.

The band-pass filter attenuates down to the maximum the frequency bands outside the demodulator receiver band. Figure 3 shows receive filter typical frequency response. In addition figure 3 shows that while the modem is receiving at a rate of 1200 bauds the 1300 Hz and 2100 Hz frequencies and is transmitting simultaneously on the back channel with the 390 Hz and 450 Hz frequencies, then, the frequencies of 390 Hz and 450 Hz are rejected in order to improve the performance of the demodulator.

Another important characteristic associated with the receive filter is the gain difference of 3 dB between 1300 Hz and 2100 Hz signal frequencies.

In fact, during the transmission of analog signals via telephone network, high frequency signals are more attenuated than the low frequency signals. The receive filter provides a fixed compromise equalizer in order to correct this attenuation difference.

Figure 3 : Received Filter Typical Frequency Response.



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Receive filter outputs a signal to RFO pin. An external shaping stage is required for the following :

- Eliminate the noise generated by the receive filter clocks.
- Eliminate the continuous component of the signal due to the receive filter.
- Amplify this signal with a fixed gain up to 1.4 V peak to peak and clip it symmetrically above 1.4 V.

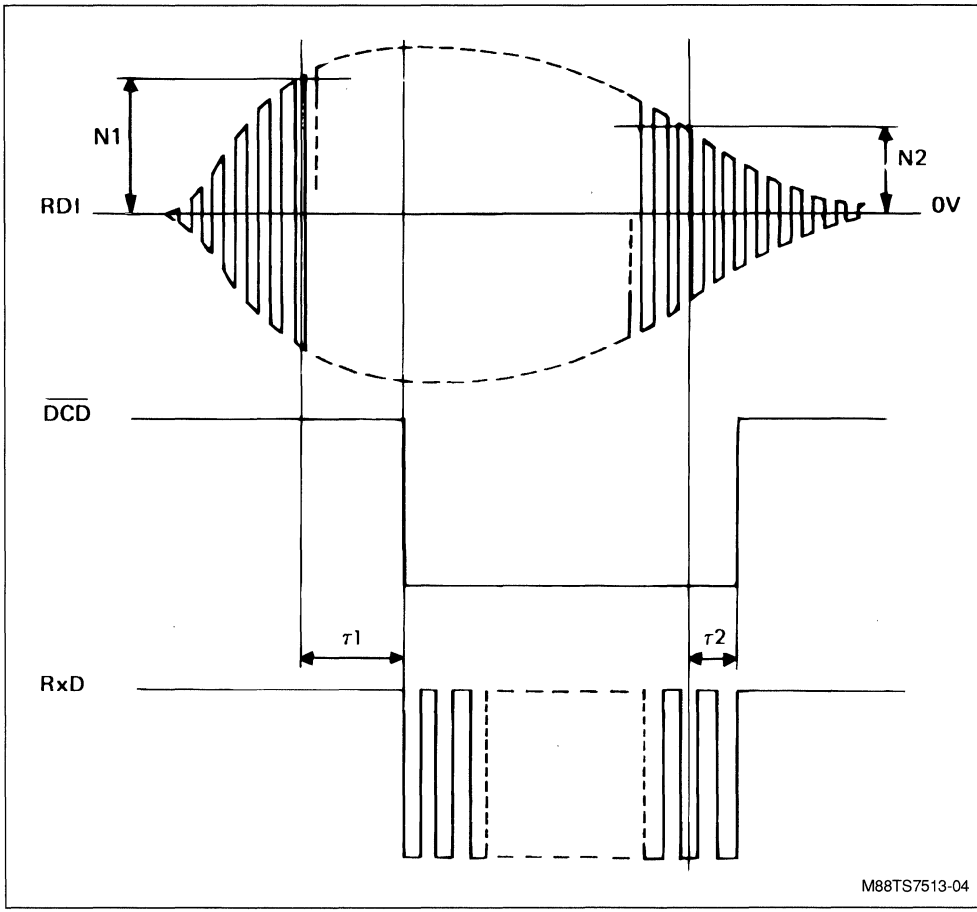
The application gives an example at an external shaping stage.

The shaping stage drives (via RDI input pin) a signal detector capable of discriminating two levels (N1 = 1.4 V, N2 = 1 V).

The detector output is time delayed and used in order to present an hysteresis effect between levels N1 and N2 levels. The typical hysteresis value is 2.9 dB. When detection conditions are met, the DCD detection signal switches to logic "0" : binary data is output to RxD pin.

RDI input drives a signal detector the $\overline{\text{DCD}}$ output of which is at logic "0" if the level of RDI signal is higher than N1. The output of this detector is at logic "1" if the level of RDI signal is lower than N2. This detector has an hysteresis effect : N1/N2.

Timing detection conditions. The timing performance of the level detector ($\overline{\text{DCD}}$) conforms to CCITT V.23 recommendation.



Under normal working conditions, DCD output is :

- low if RDI signal conforms to level detection condition,
- high if RDI signal does not conform to the level detection conditions.

$\overline{DCD}$ output goes from high to low when RDI signal conforms to the level detection conditions for 10 ms or more (respectively 10 ms for 75 bauds).

$\overline{DCD}$ output does not go from high to low when RDI signal conforms to the level detection conditions for 10 ms or less (respectively 10 for 75 bauds).

$\overline{DCD}$ output goes from low to high when RDI signal does not conform to the level detection conditions for 10 ms or more (respectively 20 ms for 75 bauds).

$\overline{DCD}$ output does not go from low to high when RDI signal does not conform to the level detection conditions for 10 ms or less (respectively 20 ms for 75 bauds).

Modulation Rate	$\overline{DCD}$ Transition	Min.	Typ. (1)	Max.	Unit
1200 bds	τ1	10	12	15	ms
	τ2	10	12	15	ms
75 bds	τ1	10	15	20	ms
	τ2	20	30	40	ms

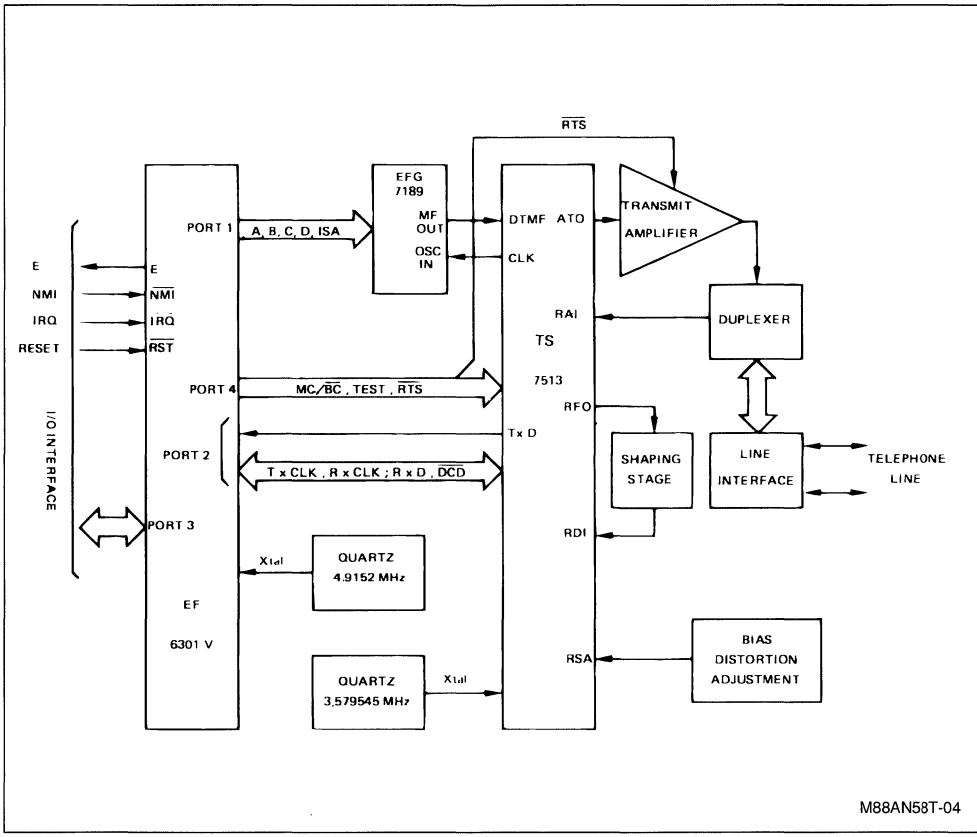
APPLICATION

In the example of TS7513 application presented below, TS7513 circuit is in a system configuration. The figure below shows an application block diagram with its differents sections :

- Transmit amplifier with the duplexer and line interface.
- TS7513 circuit with its shaping stage.
- EFG7189 circuit generator of DTMF frequencies.
- EF6801 microcomputer used as an interface between the terminal and TS7513 circuit.
- The bias distortion adjustment.

An example of TS7513 circuit application is shown on the following page with an EF6850 UART.

APPLICATION BLOCK DIAGRAM



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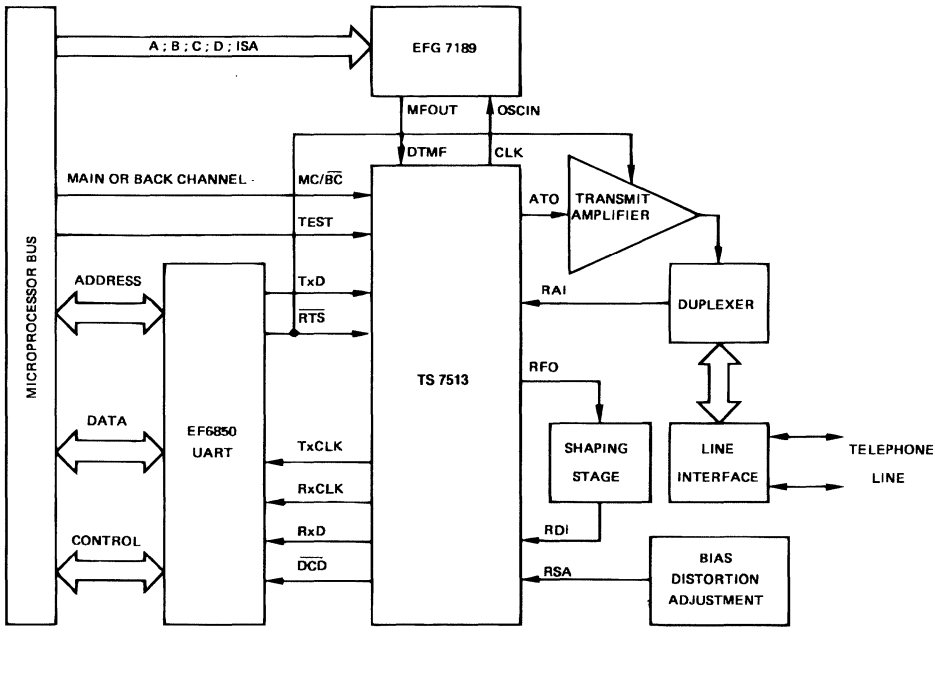
APPLICATION BLOCK DIAGRAM



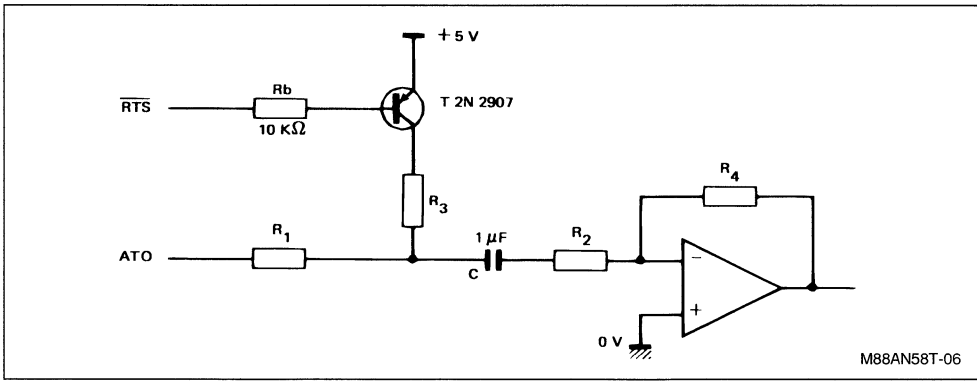
TRANSMIT AMPLIFIER AND DUPLEXER WITH LINE INTERFACE

TRANSMIT AMPLIFIER.

The TS7513 ATO pin can transmit two types of analog signals according to the status of $\overline{RTS}$ logic input.

- If $\overline{RTS}$ is low, ATO pin sends a frequency modulated signal. The frequencies transmitted are the following :
  - f_0 = 2100 Hz f_1 = 1300 Hz (modulation rate = 1200 bauds).
  - f_0 = 450 Hz f1 = 390 Hz (modulation rate = 75 bauds).
- If $\overline{RTS}$ is high, ATO pin sends a pair of DTMF frequencies.
- The input of the transmit amplifier is connected to ATO pin. The amplifier must present two possible gains depending on whether ATO pin transmits a frequency modulated signal or a pair of DTMF frequencies.

The following diagram shows an example of an amplifier with variable gain controlled by $\overline{RTS}$ signal.



When $\overline{RTS}$ is high, the transistor is OFF, R3 resistor does not control gain calculation. The gain value depends on R1, R2, R4.

When $\overline{RTS}$ is low, the transistor is ON, the gain value depends on R1, R2, R3, R4.

DEMODULATOR

$\overline{RTS}$	ATO	Gain
0	FSK Modulated Signal	$-\frac{R3 .R4}{R1 .R2 + R2 .R3 + R3 .R1}$
1	DTMF Signal	$-\frac{R4}{R1 + R2}$

TRANSMIT GAIN

TS7513 reception performance is directly related to duplexer quality. The duplexer is intended to provide an interface between the TS7513 and the telephone system. Since data flow is bidirectional on the telephone line, the duplexer must allow :

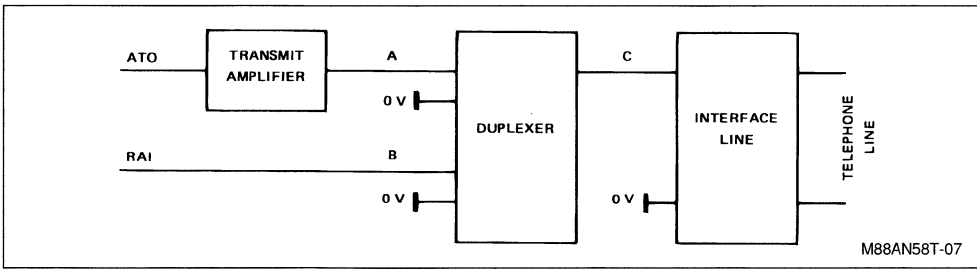
- the received signal to pass on the RAI input,
- properly couple the transmitted signal into the line,
- minimize the local transmitted level towards the receiver,
- properly terminate the transmission line.

The duplexer consists of the following :

- an A input (transmission),
- a B output (reception),
- a C input/output (transmission/reception).

Transmission and reception signals are grouped on a single wire on Input/output C.

TRANSMITTER-RECEIVER BLOCK DIAGRAM

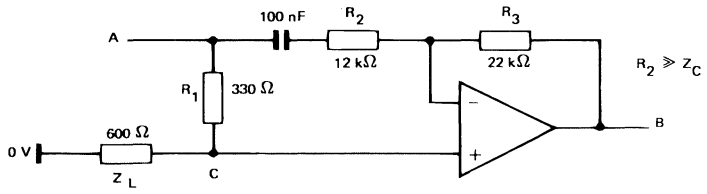


There are three different gains on the duplexer :

- Gain from point A to point C : G_T. This gain must be constant for the frequencies transmitted (from 390 Hz to 2100 Hz).
- Gain from point A to point B : G_D. This gain must be lower than - 10 dBm in order to reject most of the signal transmitted over point A.
- Gain from point C to point B : G_R. This gain must be constant for the frequencies received (from 390 Hz to 2100 Hz).

Solution proposed :

DUPLEXER BLOCK DIAGRAM



Z_L stands for the line interface impedance loaded by the telephone line (600 Ω).

- The gain from point A to point C is :

$$G_T = \frac{Z_L}{Z_L + R1}$$

With R1 = 330 Ω and if telephone line impedance is 600 Ω gain G_T = - 3.8 dB (a ratio of 0.65).

- The gain desired from point A to point B is $G_D = 0$

$$G_D = -\frac{R3}{R2} + \left(1 + \frac{R3}{R2}\right)\left(\frac{Z_L}{R1 + Z_L}\right)$$

If R2 = 12 kΩ and R3 = 22 kΩ, gain $G_D \approx 0$ (rejection is almost perfect).

Since all impedances (except the line impedance Z_L) can be accurately controlled, the duplexer rejection performance depends directly on Z_L. In practice, due to the variations of the line impedance which is not in reality a pure resistive load, an attenuation of around - 10 dB is assumed to be provided by the duplexer.

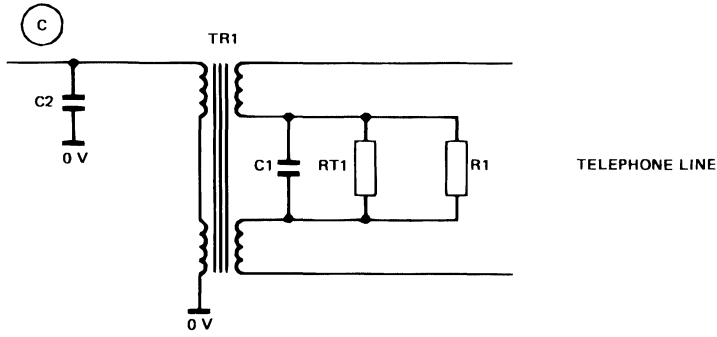
- The gain from point C to point B is :

$$G_R = 1 + \frac{R3}{R2}$$

With R2 = 12 kΩ and R3 = 22 kΩ, gain G_R = + 9 dB (a ratio of 2.8).

LINE INTERFACE.

Duplexer connection to the telephone line via a line interface is given below.



TR1	Line transformer LTT220963L	R1	Resistor 680 Ω 3 W.
RT1	Thermistor with positive temperature coefficient for current regulation of telephone line CTP67090003.	C1	Capacitor 2.2 µF 250 V.
		C2	Capacitor 10 nF 50 V.

M88AN58T-09

The diagram above shows the following specific features :

- For transmission, the gain from duplexer point C to telephone line is - 1.5 dB.
- For reception, the gain from telephone line to duplexer point C is - 4.5 dB (different from transmission).

The gain introduced by duplexer is + 9 dB. Therefore the gain introduced by the duplexer line interface unit is + 4.5 dB.

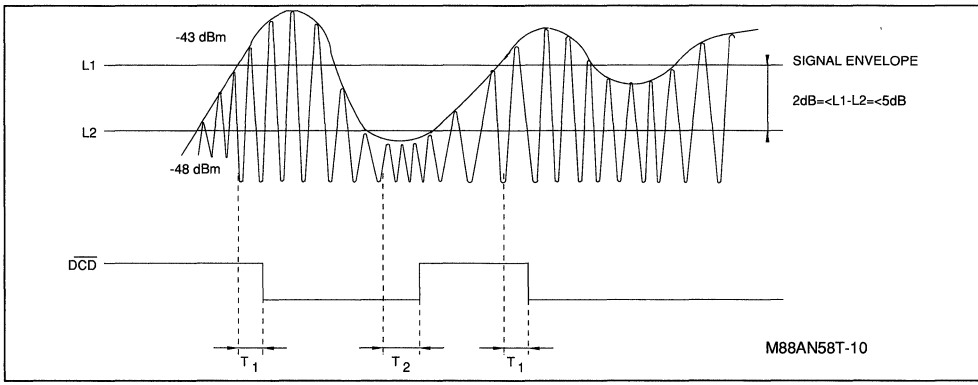
Note : The duplexer line interface unit presented above is designed to operate on the French telephone network (line impedance = Z_L = 600 Ω). If TS 7513 circuit was used on a different telephone network the duplexer line interface unit would have to be changed.

Shaping stage. TS7513 reception performance is directly related to duplexer quality and shaping stage. The shaping stage is positioned across RFO pin, the receive filter output, and RDI pin, the demodulator input.

The shaping stage must perform the following functions :

- Eliminate the noise generated by the receive filter clock.
- Eliminate the continuous component of the signal from the receive filter.
- Amplify this signal with a fixed gain up to 1.4 V peak to peak and clip it symmetrically above 1.4 V.

DEMODULATION CONDITION



Levels L1 and L2 have a value ranging from – 43 dBm to – 48 dBm, with the following restriction difference L1 – L2 should range from 2 dB to 5 dB.

In TS7513 circuit the hysteresis effect (N1 – N2) is 2.9 dB (example L1 = – 44.6 dBm, L2 = – 47.5 dBm).

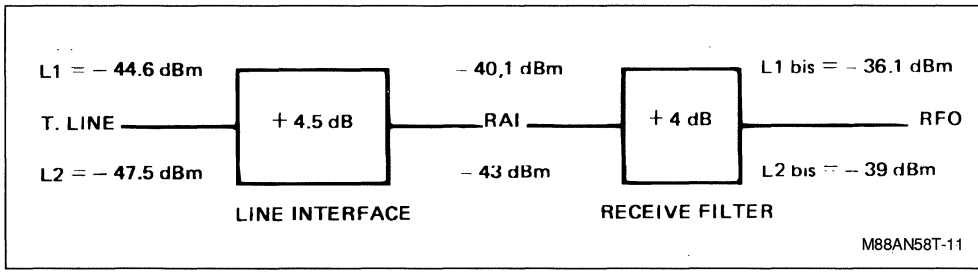
This duplexer line interface unit presents a RAI telephone line gain of + 4.5 dB.

The gain introduced by the receive filter is + 4 dB.

The signal on RFO pin is therefore amplified by + 8.5 dB.

The following diagram shows the signal amplification via the line interface and TS7513 receive filter.

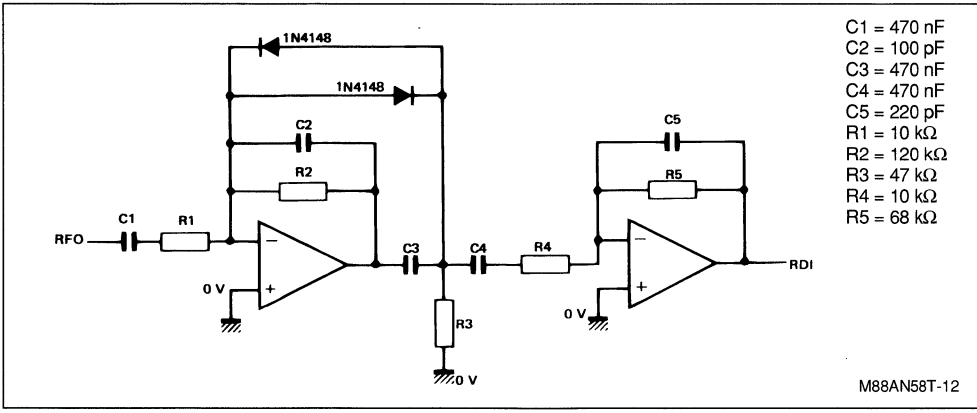
RECEIVE SECTION



The values of the levels on RDI pin are : N1 = 1.4 V peak to peak.
= 2.1 dBm.
N2 = 1 V peak to peak.
= 0.8 dBm.

The figure below shows signal amplification via the shaping stage. The shaping stage should amplify the signal by 38.2 dB (a ratio of 81.6) in order to provide N1 and N2 levels on RDI input.

Solution proposed



- In the 1st stage, the gain is 21.6 dB (ratio of 12).
- In the 2nd stage, the gain is 16.6 dB (ratio of 6.8). Therefore, the shaping stage presents a gain of 38.2 dB (ratio of 81.6).
- C1 eliminates any possible offset generated by TS7513 receive filter.
- C2 eliminates switching peaks generated by receive filter clock.
- The diodes clip the signal at – 0.7 V or + 0.7 V. In order to obtain a symmetrical clipping of the stage in relation to 0 V, the unit R3C3 performs a high pass filter (fc = 7.2 Hz) to eliminate the offset generated by the operational amplifier.

CIRCUIT EFG7189 : GENERATOR OF DTMF FREQUENCIES

The TS7513 has a DTMF input pin capable of receiving a signal from the DTMF frequency generator EFG7189. When RTS is high, the signal is then filtered in a low-pass filter (fc = 3.4 kHz) and sent to ATO pin.

The EFG7189 is a CMOS circuit. It operates with a single voltage (+ 5 V) and uses a standard 3.579545 MHz crystal. It can generate eight different frequencies :

Four "low" frequencies : f1 = 697 Hz
f2 = 770 Hz
f3 = 852 Hz
f4 = 941 Hz
Four "high" frequencies : f5 = 1209 Hz
f6 = 1336 Hz
f7 = 1477 Hz
f8 = 1633 Hz

The signal transmitted is sent on MFOUT pin. It consists of a "low" frequency and a "high" frequency. It is therefore possible to obtain 2^4 i.e. 16 pairs of different DTMF frequencies. The frequency pair is selected by four bits.

The acquisition of these 4 bits is parallel via A, B, C, D pins, when H logic input is high.

The acquisition of these 4 bits is serial via A pin when H logic input is low.

The ISA pin inhibits MFOUT analog output.

When ISA is high, MFOUT output is inactive and connected to 0 V.

When ISA is low, MFOUT output is active and sends a DTMF signal.

Validation of the hexadecimal code consisting of 4 bits occurs on a falling edge of ISA signal.

EFG7189 - TS7513 CONNECTION

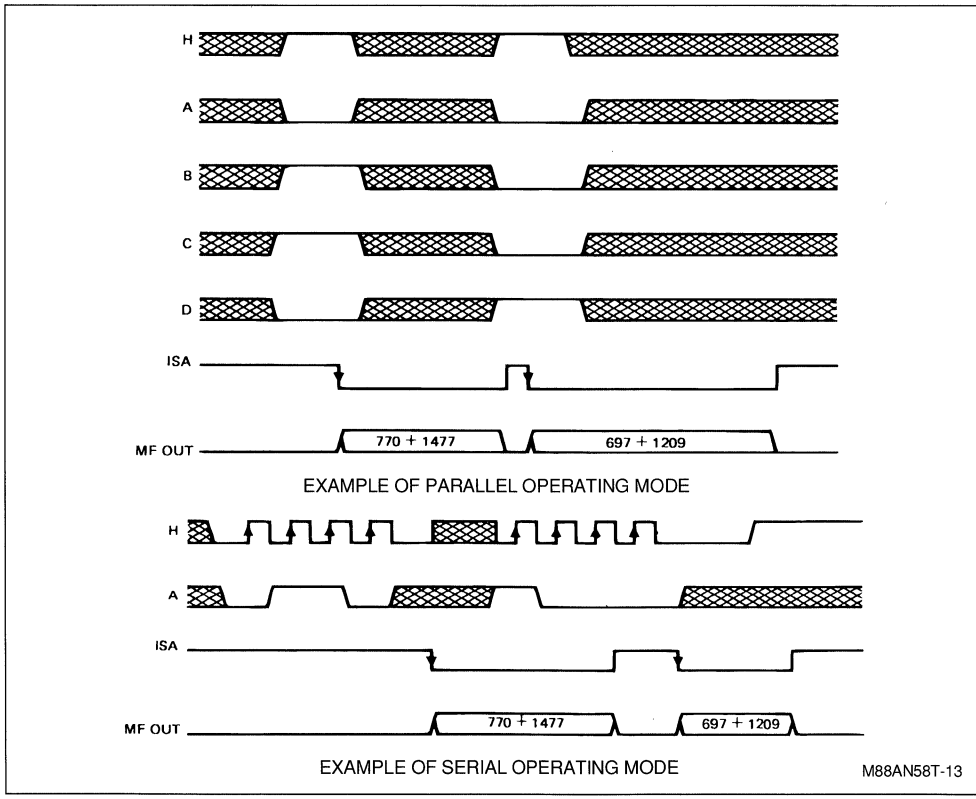
The DTMF frequency generator EFG7189 uses a crystal similar to that used by TS7513. To avoid using two crystals, CLK pin on TS7513 delivers a clock signal at a frequency of 3.579545 MHz which is connected to the OSCIN pin on the EFG7189.

MFOUT pin on EFG7189 is directly connected to DTMF pin on TS7513.

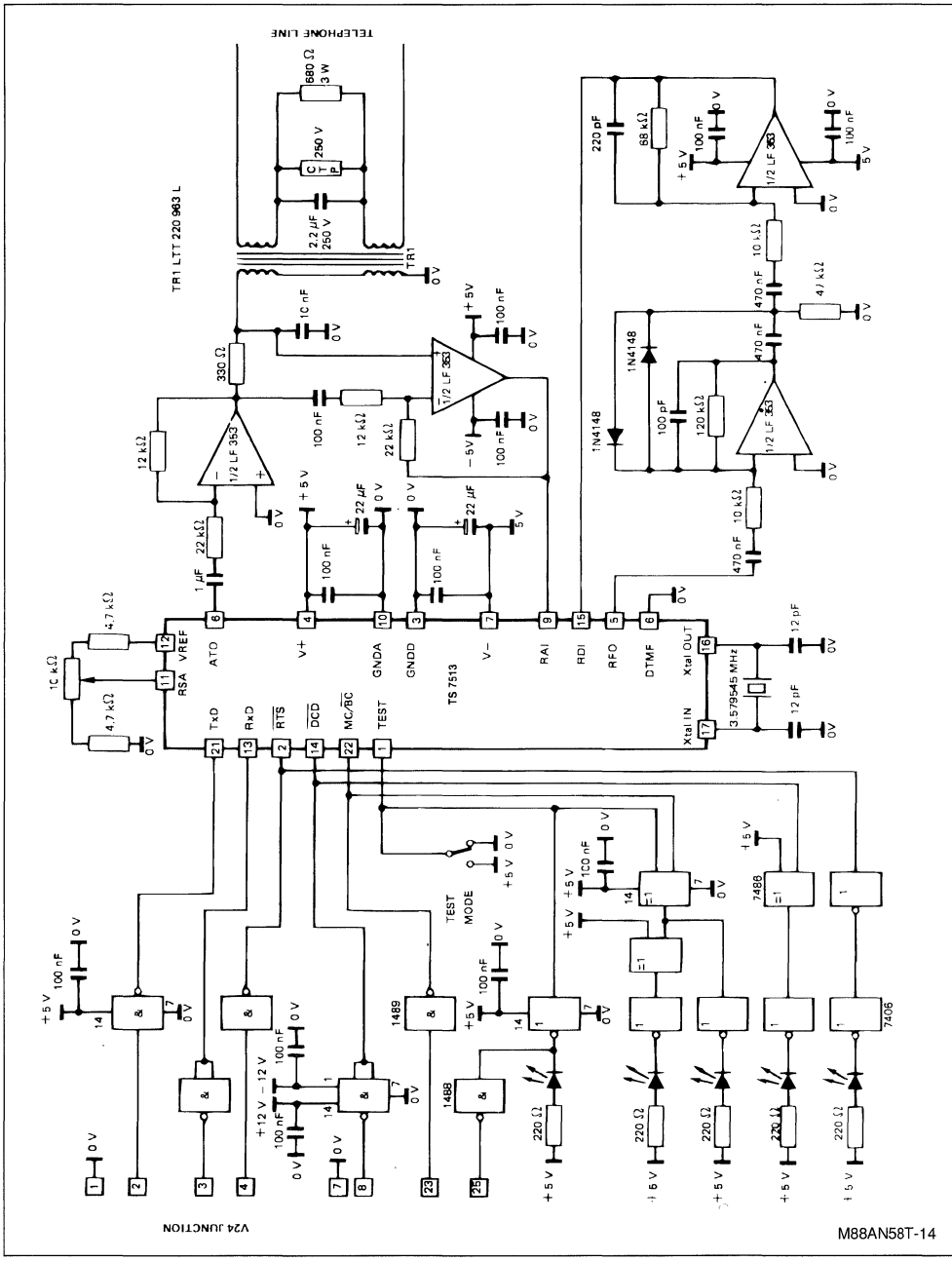
CIRCUIT EFG 7189

Keyboard Code	Hexadecimal Code				ISA	Generated Frequencies	
	A	B	C	D		f(Hz)	f(Hz)
X	X	X	X	X	1		
1	0	0	0	1	↓	697	1209
2	0	0	1	0	↓	697	1336
3	0	0	1	1	↓	697	1477
4	0	1	0	0	↓	770	1209
5	0	1	0	1	↓	770	1336
6	0	1	1	0	↓	770	1477
7	0	1	1	1	↓	852	1209
8	1	0	0	0	↓	852	1336
9	1	0	0	1	↓	852	1477
0	1	0	1	0	↓	941	1331
.	1	0	1	1	↓	941	1209
*	1	1	0	0	↓	941	1477
A	1	1	0	1	↓	697	1633
B	1	1	1	0	↓	770	1633
C	1	1	1	1	↓	852	1633
D	0	0	0	0	↓	941	1633

FREQUENCIES TRANSMITTED WITH RESPECT TO HEXADECIMAL CODE



TYPICAL APPLICATION OF TS7513 : MODEM STAND ALONE WITHOUT DTMF GENERATOR



TELEGRAPHIC PERFORMANCE MEASUREMENT

GENERAL SPECIFICATIONS

Transmission line simulator 300 to 3400 Hz controlled characteristics :

- Output level (signal).
- Output level (noise).
- Group delay/HF - MF - BF.
- Amplitude filter HF - BF.

Gadem - logic system specially manufactured by SGS-THOMSON Microelectronics.

- Maximum transmission rate 19200 bits/sec.
- Generate normalized patterns.
  - Pseudo random 511 bits.
  - 1.0... with synchro.
  - Specific sequence.
- Clock recovery by DPLL.
- Bias distortion.
- Data transition statistics (distribution).
- Error counting.
- Error rates.
- Delay measurements between command and status register.

MEASUREMENT PROGRAMS (EXTENDED BASIC HP)

Menu

It's an interactive program to create a specific sequence of measurements.

Modem's measurements

It's the main program to control the execution of the measurements (only one, for all modem's measurements).

Trace

Result treatment, graphic output.

Filter

It's used to measure the amplitude and group delay/versus frequency of :

- Filter.
- Modem output.
- Line simulator.

MEASUREMENTS

Bias distortion

- Sequence 1.0...
- Gap between the mean of the time of the "1" and the mean of the time of the "0".
- Expressed in percentage of clock period.

Telegraphic distortion

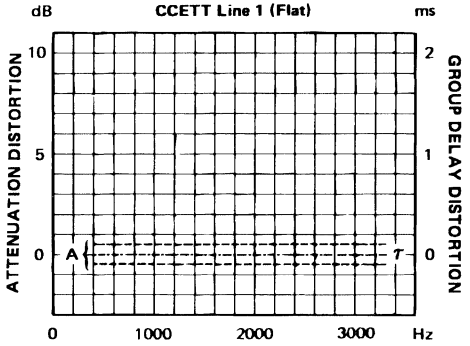
- Sequence pseudo random 511 bits.
- Gap between the theoretical transitions of the received signal (defined by the clock recovery by DPLL) and the real position.
- Expressed in percentage of the clock period.
- More than 50 % of telegraphic distortion made errors.
- Measurement may be :
  - Peak to peak.
  - Standard deviation.
  - Weighted (ex. value at 10 %).

Bit error rate

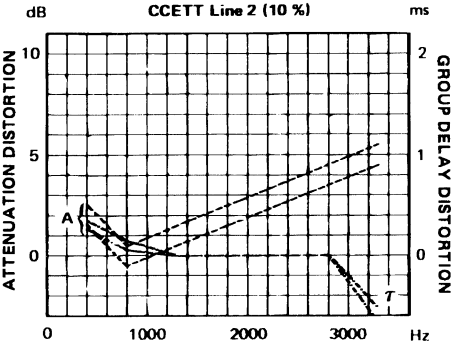
- Sequence pseudo random 511 bits.
- Line...
- White noise in the band 300 - 3400 Hz.
- Ration of the number of false received bits to the number of emitted bits, as a function of signal to noise ratio.

APPENDIX

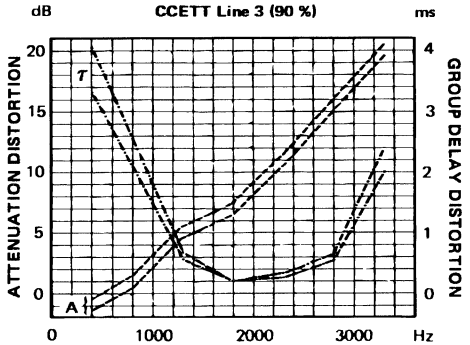
CHARACTERISTICS OF CCETT LINES



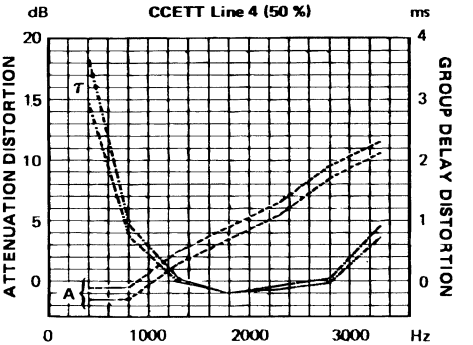
M88TS7513-09



M88TS7513-10



M88TS7513-11



M88TS7513-12

A VERY LOW COST AND POWERFUL SOLUTION FOR V.23 APPLICATION : TS7514

by O. Leenhardt – R. Girard

1. INTRODUCTION

The TS7514 is a single chip F.S.K. voiceband modem offering a real low cost powerful solution for all C.C.I.T.T. V.23 recommended standard applications.

The TS7514 main features are :

PROGRAMMABLE MODES :

- MODEM 75/1200 or 1200/75 bps (full duplex on 2 wire line),
- MODEM 75/75 or 1200/1200 bps (full duplex on 4 wire line),
- D.T.M.F. DIALING,
- ANALOG TEST LOOP,
- TONE DETECTION (ring, dialing,...),

PROGRAMMABLE FUNCTIONS :

- TRANSMIT/RECEIVE LEVELS,
- RECEIVE FILTER GAIN,
- HYSTERESIS AND DETECTION LEVELS,
- LINE MONITORING LEVEL,
- SIGNALLING FREQUENCY (2982 Hz) LEVEL,

Indeed, TS7514 integrates many possibilities and functionalities by requiring only very few external components. Its block diagram is shown figure 1.

ADDITIONAL FEATURES :

- INTEGRATED DUPLEXER,
- AUXILIARY ANALOG SIGNAL TRANSMISSION (voiceband),
- AUTOMATIC BIAS DISTORTION ADJUSTMENT,
- TAX REJECTION FILTER (12 and 16 kHz),
- FIXED COMPROMISE EQUALIZATION,
- STANDARD LOW COST CRYSTAL (3.579 MHz),
- C.M.O.S. TECHNOLOGY,
- LESS THAN 100 mW POWER DISSIPATION,
- ± 5 VOLTS SUPPLIES,
- 24 PIN PACKAGE.

Figure 1.

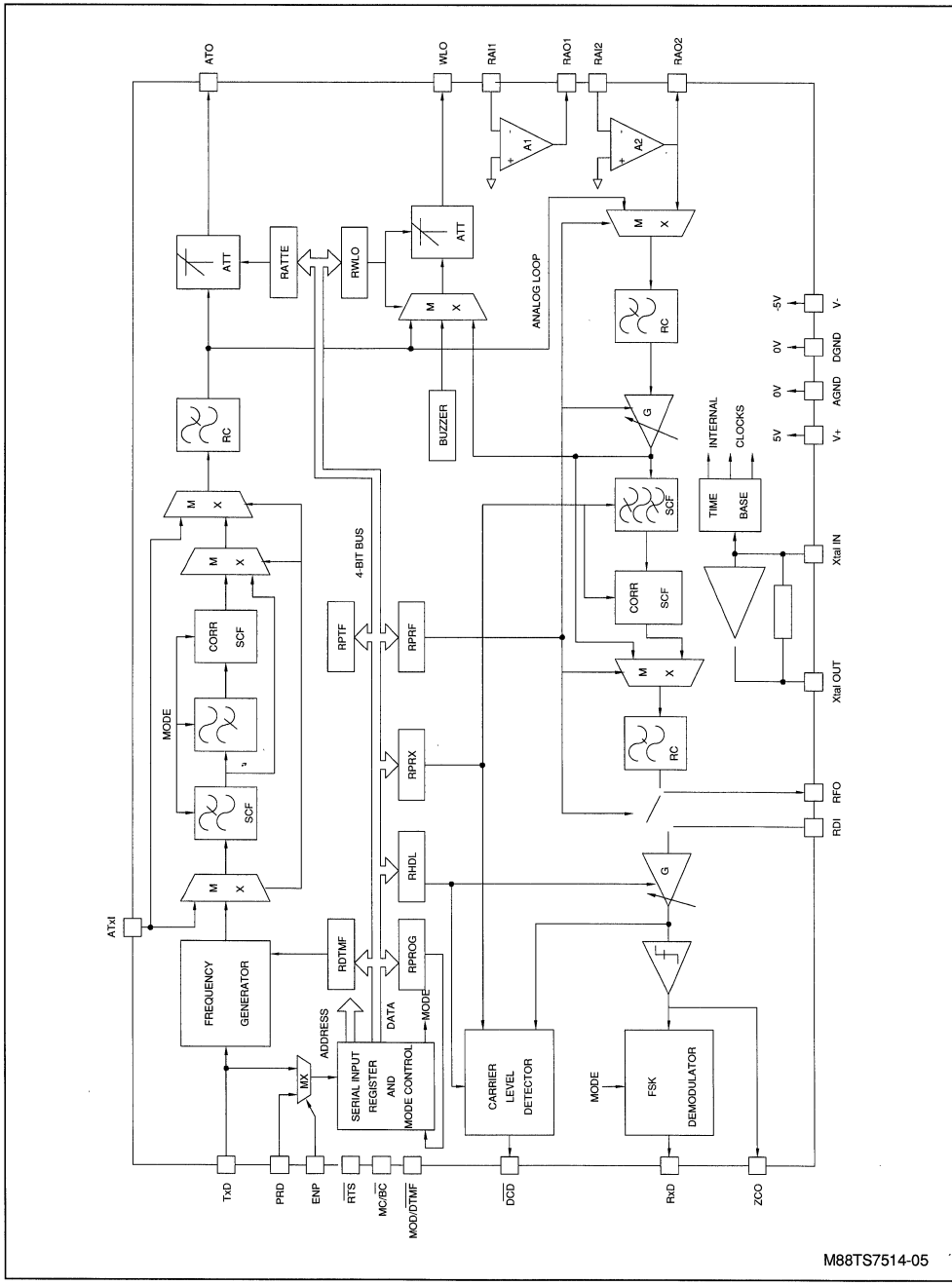
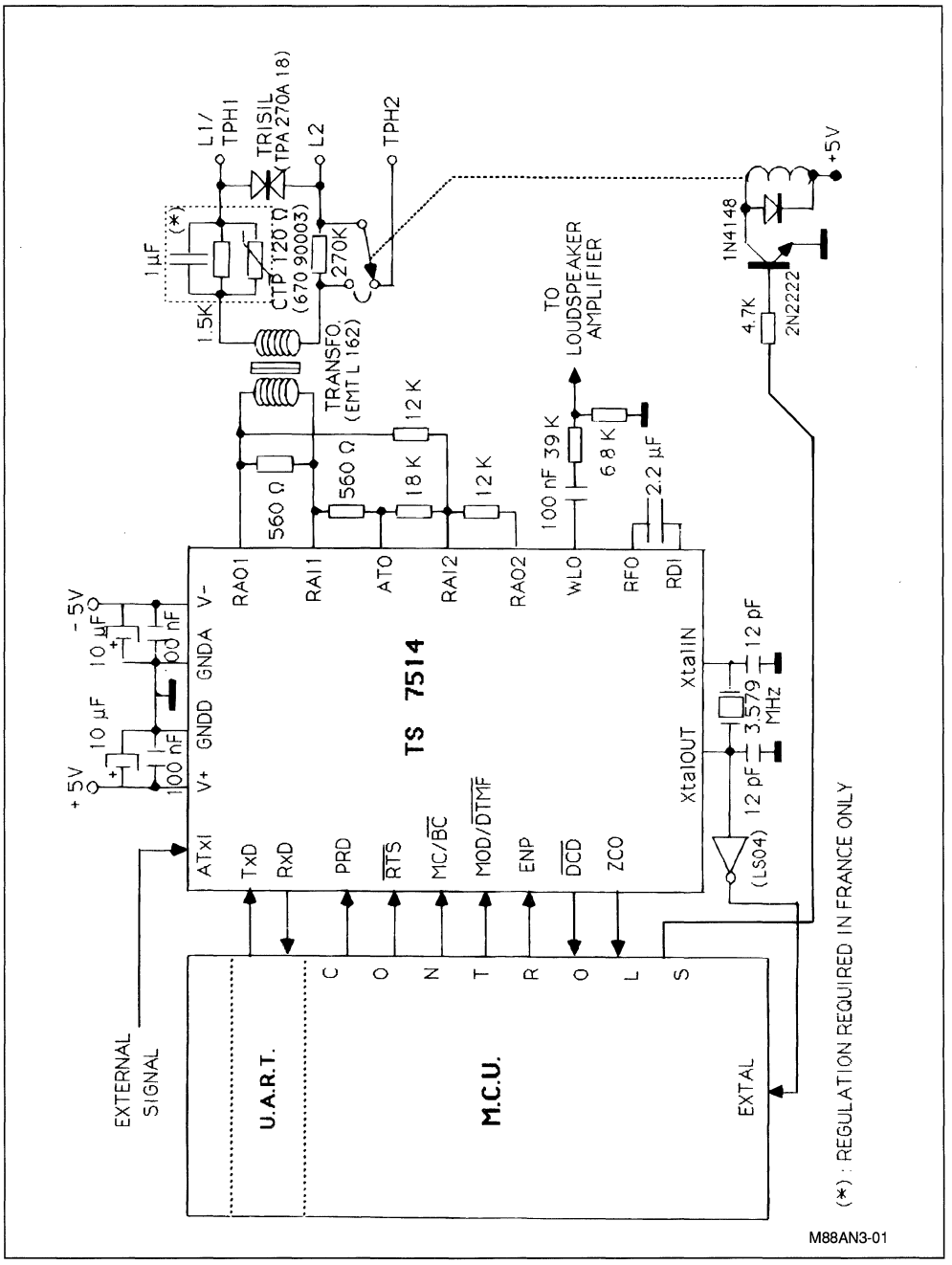

ATO
WLO
RAI1
RAO1
RAI2
RAO2
A1
A2
ATT
RATTE
RWLO
ANALOG LOOP
M
X
RC
G
BUZZER
INTERNAL
CLOCKS
TIME
BASE
SCF
CORR
4-BIT BUS
RPTF
RPRF
RPRX
RHDL
RDTMF
RPROG
MODE
ATxI
FREQUENCY
GENERATOR
MX
ADDRESS
DATA
SERIAL INPUT
REGISTER
AND
MODE CONTROL
CARRIER
LEVEL
DETECTOR
FSK
DEMODULATOR
HF
-5V
0V
5V
V-
DGND
AGND
V+
Xtal IN
Xtal OUT
RFO
RDI
TxD
PRD
ENP
RTS
MC/BC
MOD/DTMF
DCD
RxD
ZCO
M88TS7514-05

Figure 2.


L1/
TPH1
TRISIL
(TPA 270A 18)
L2
TPH2
+5V
1µF
(*)
CTP 1120 Ω
(670 90003)
270K
1N4148
1.5K
TRANSFO.
(EMT L 162)
TO
LOUDSPEAKER
AMPLIFIER
4.7K
2N2222
560 Ω
560 Ω
18 K
12 K
12 K
100 nF 39 K
6.8 K
2.2 µF
- 5V
10 µF
100 nF
+ 5V
10 µF
100 nF
TS 7514
V-
GNDA
V+
GNDD
ATxI
TxD
RxD
PRD
RTS
MC/BC
MOD/DTMF
ENP
DCD
ZCO
RA01
RAI1
ATO
RAI2
RAO2
WLO
RFO
RDI
XtalIN
XtalOUT
3.579 MHz
12 pF
12 pF
(LS04)
EXTERNAL
SIGNAL
U.A.R.T.
M.C.U.
EXTAL
(*) : REGULATION REQUIRED IN FRANCE ONLY
M88AN3-01

This application note describes some of the TS7514 most important features detailed before from a typical and simplified application scheme shown figure 2 (more informations are given in the following sheets).

2. PROGRAMMABLE MODE

2.1. WITH WHAT TO PROGRAM ?

The TS7514 contains 8 control registers.

The programming used is serial where data input is TxD or PRD and clock input $\overline{RTS}$.

From now, it is important to point out that during programming, the $\overline{RTS}$ (Request To Send) signal and the TxD (Transmit Data) signal to be transmitted from the local terminal over the telephone line are internally safeguarded in order to not modify the transmission.

- By using TxD either to program or transmit data, only one signal has to be managed. In this case, you must take in care to program the TS7514 out of the transitions between two successive data bits and during a maximum duration equal to a "bit time" (833.3 µsec. in 1200 bps) to avoid transmission errors.
- By using PRD to program the TS7514 allows to use TxD only for data to be transmitted and avoids the preceeding cautions but requires the management of these two signals.

The choice will depend on the application (microcontroller used, number of I/0 ports, ...).

TxD is selected by ENP = "0" ; PRD by ENP = "1".

2.2. HOW TO PROGRAM ?

The programming is indirect via an 8 bit shift register, called input register, least significant bits first.

The 4 M.S.B.'s of the input register are the address of the control register to program ; the 4 L.S.B.'s the data.

The input register is selected by MOD/$\overline{DTMF}$ = MC/$\overline{BC}$ = "0".

Then, $\overline{RTS}$ (Request To Send) and TxD (Transmit Data) signals are internally safeguarded and the corresponding pins must be used as clock ($\overline{RTS}$) and data to be programmed (TxD).

The $\overline{RTS}$ clock, active on the falling edge, shifts the programming data available on TxD or PRD.

The transfer of programming data to the control register previously addressed is made by rising MOD/$\overline{DTMF}$ or MC/$\overline{BC}$.

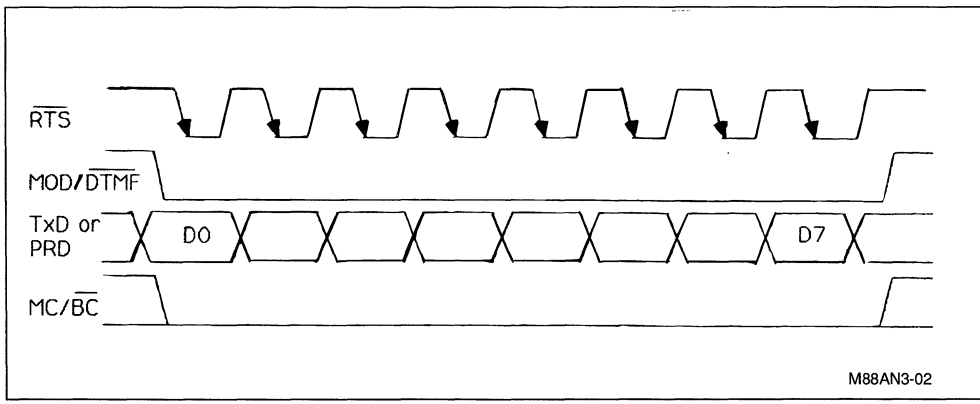
From now, the $\overline{RTS}$ signal comes back to its previous functioning mode : Request To Send.

There are 2 cases of end of programming :

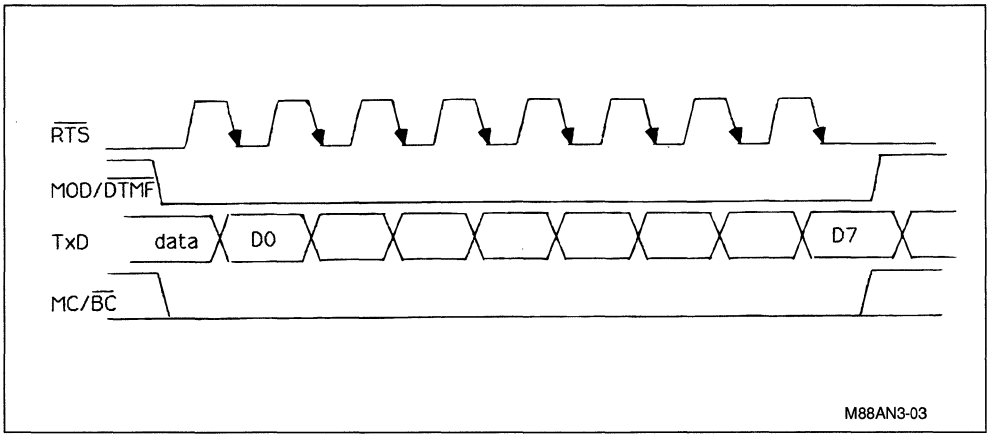
- At the end of programming of all the control registers, excepted RDTMF, MOD/$\overline{DTMF}$ rises to "1" while MC/$\overline{BC}$ indicates the channels used for transmission before programming ("0" for low channel transmission, "1" for high channel transmission).
- At the end of programming of RDTMF register only, MC/$\overline{BC}$ rises to "1" while MOD/$\overline{DTMF}$ and $\overline{RTS}$ are "0" during all the time of D.T.M.F. signal programmed transmission.

2.3. TIMING DIAGRAMS

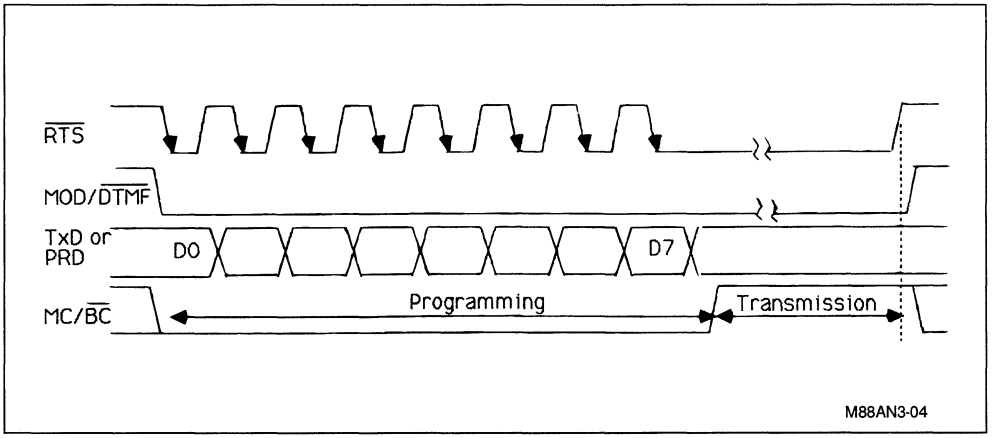
Programming without Transmission.



Programming during Transmission.



DTMF Programming and Transmission.



3. THE TS7514 REGISTERS

We are going to describe now the most important points to know about these eight control registers.

Notes : In the following, all the bits described are the data bits of the control registers (X = don't care).

For additional informations on these registers, refer to the TS7514 corresponding data sheet.

3.1. MODE REGISTER : RPROG

This control register allows to choose the functioning mode of the TS7514 : either two different or the same channels for transmit and receive.

The most used mode (power-up initialization) is the receive channel programmed in the opposite way to the transmit channel controlled by MC/$\overline{BC}$ pin. In this case, bits 2 and 3 must be programmed to "0".

If bit 3 is programmed to "0" while bit 2 is programmed to "1", then transmit and receive channels are the same (high channel if MC/$\overline{BC}$ is "1", low channel if MC/$\overline{BC}$ is "0").

This last mode can be used for the full duplex on 4 wire line modem functioning or for the test with an external analog loop between transmit and receive sections (this last mode is not a loop 3 (see RPRF register)).

3.2. D.T.M.F. REGISTER : RDTMF

This control register allows the D.T.M.F. dialing from the TS7514.

Bits 0 and 1 program the 4 low frequencies of the D.T.M.F. signal, bits 2 and 3 the 4 high frequencies.

This register is not initialized at the power-up.

The following table give the correspondance between the digit to be dialed and the data to be programmed.

DIGIT	D3	D2	D1	D0	Low Fre. (Hz)	High Fre. (Hz)
0	0	1	1	1	941	1336
1	0	0	0	0	697	1209
2	0	1	0	0	697	1336
3	1	0	0	0	697	1477
4	0	0	0	1	770	1209
5	0	1	0	1	770	1336
6	1	0	0	1	770	1477
7	0	0	1	0	852	1209
8	0	1	1	0	852	1336
9	1	0	1	0	852	1477
A	1	1	0	0	697	1633
B	1	1	0	1	770	1633
C	1	1	1	0	852	1633
D	1	1	1	1	941	1633
*	0	0	1	1	941	1209
#	1	0	1	1	941	1477

3.3. TRANSMIT ATTENUATION REGISTER : RATTE

This control register allows to program a transmit attenuation from 0 (0000) to 13 dB (1101), with 1 dB step.

With such values, the analog transmit output level on ATO pin varies from + 4 (0000) to – 9 dBm (1101).

Two programming values (1110 and 1111) allows an infinite attenuation.

Such attenuation is automatically programmed at the power-up initialization. So, a different attenuation will have to be programmed to transmit data (typically 0 dBm (0100) on ATO pin).

3.4. LINE MONITORING REGISTER : RWLO

This control register allows :

- to monitor the transmit signal from – 10 (0000) to – 40 dB (0011) with 10 dB step,
- to monitor the receive signal from 0 (0100) to – 30 dB (0111) with 10 dB step,
- to send a square wave signalling frequency (2982 Hz) with a level comprised between – 4 (1000) and –34 dBm (1011).

This register is initialized to 11XX (neither monitoring nor signalling transmission) at the power-up.

If a receive signal monitoring is programmed, it is possible to monitor also simultaneously the transmit signal on account of the non infinite rejection ratio of the hybrid (typically 20 dB) and thanks to the TS7514 internal architecture (see figure 1), the receive signal monitoring being implemented before the receive filter.

3.5. TRANSMIT FILTER register : RPTF

This control register allows to transmit on ATO pin one of the following signals :

- normal (power-up initialization) modem or D.T.M.F. signals (0000),
- external voiceband analog signal through :
  - smoothing filter and attenuator (0001),
  - low-pass filter and attenuator (0010),
  - band-pass filter and attenuator (0011),
- low frequency only (0100) in D.T.M.F. mode,
- high frequency only (1000) in D.T.M.F. mode.

3.6. RECEIVE FILTER register : RPRF

This control register allows to program different configurations for the receive filter :

- receive filter gain of 0 (XX00), 6 (XX01) or 12 dB (XX10),
- receive channel looped back on the transmit channel with a – 35 dBm level and a 0 dB gain (XX11) for analog test loop (loop 3),
- receive filter bypassed (X1XX) or not (X0XX),
- external connection (1XXX) via a 2.2 µF non-polarized capacitor between RFO and RDI pins.

The external connection (bit 3 programmed to "1") with the capacitor is the most used mode to connect the receive filter output to the demodulator input.

Nevertheless, if an internal connection is used, bit 3 has to be programmed to "0" and external capacitor and connection between RFO and RDI pins have to be suppressed.

This register is initialized to X001 (receive filter enabled with 6 dB gain) at the power-up.

3.7. DETECTION LEVEL AND HYSTERESIS REGISTER : RHCD

This register allows to control :

- the loss carrier detection level between – 41 (X000) and – 27 dBm (X111) with 2 dB step,
- the hysteresis between carrier detect on and off : 2.5 (0XXX) or 3.25 (1XXX) dB.

Be careful that the loss carrier detection level value (N2) is given related to the demodulator input (RDI). The on-line loss carrier detection level (NL) is obtained by substracting from N2 the receive filter and the hybrid gain values.

In consequence, the on-line detection level is obtained by adding to NL the hysteresis value.

This register is initialized to 0000 (– 41 dBm for loss carrier detection level with a 2.5 dB hysteresis) at the power-up.

3.8. RECEIVE CHANNEL REGISTER : RPRX

This control register allows to program different configurations for the receive channel :

- to use a wide (for data and tone detection) (XX0X) or a narrow (for data only) (XX1X) band filter for the receive low channel,
- to suppress (XXX1) or not (XXX0) the carrier detection delays for a "fast" carrier detection ($\overline{DCD}$ digital signal following the receive carrier signal level variations).

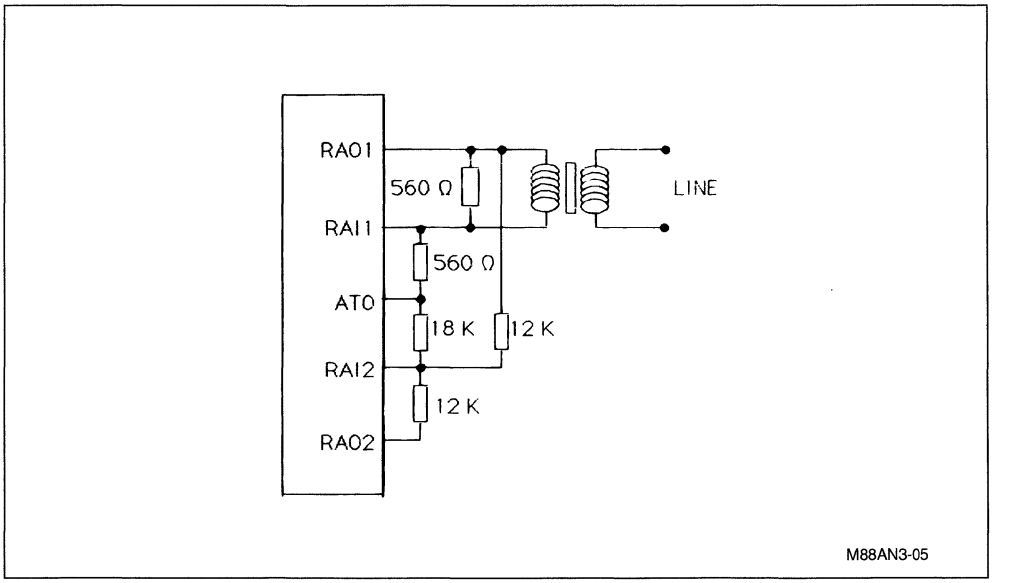
This register is initialized to XX00 (wide band filter and carrier detection delays) at the power-up.

4. THE 4/2 WIRE CONVERSION : THE HYBRID

The TS7514 integrates two operational amplifiers. So, the hybrid implementation consists of selecting only 5 resistors in order to obtain the best adaptation and rejection possible.

With 5 % resistors and a transformer 600Ω/600Ω respecting the local agreement conditions, the hybrid so designed offers an ATO/RA02 rejection ratio upper than 20 dB.

Figure 3.



5. THE D.T.M.F. DIALING

To dial a digit (0,..., 9, A, B, C, D,*,#) in D.T.M.F. consists of programming the RDTMF control register like an other register but leaving, at the end of programming, the MOD/$\overline{DTMF}$ and $\overline{RTS}$ signals to "0" during all the time desired (in practise, the time of pressing key on a dialer).

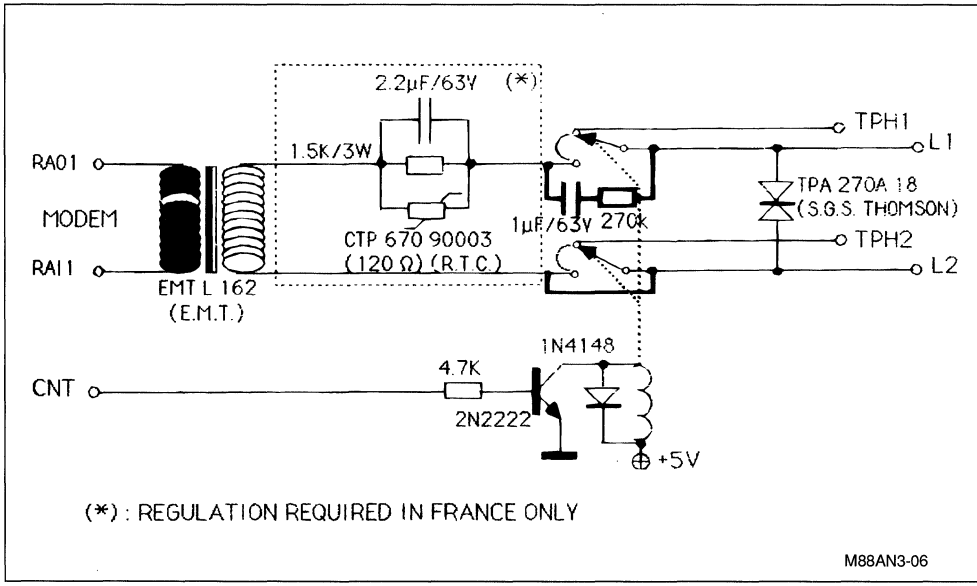
No external component is required for this dialing.

6. RING DETECTION

Thanks to ZCO output, it is possible to obtain in a digital way the analog zero crossing signal available on the RA02 pin of the TS7514. Then, by not totally insulating the modem from the telephone line (L1, L2) and bypassing the receive filter, ZCO can deliver the digital form of the ringing signal that may be then processed by the microcontroller.

With the scheme given figure 4, we avoid to use opto-coupler and other external associated components to detect ring, the only external components required being a resistor and a capacitor.

Figure 4.



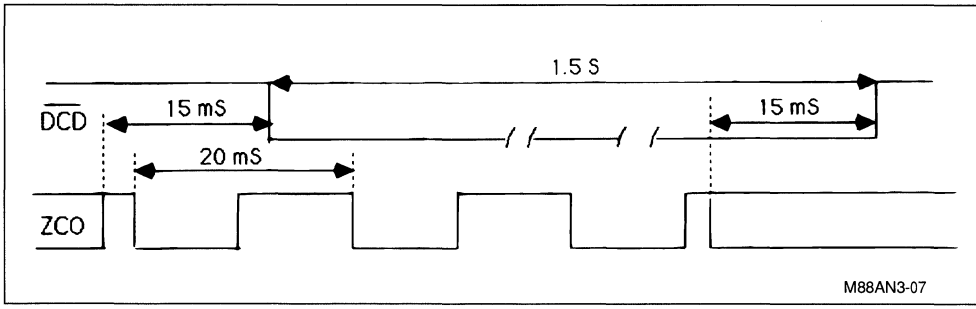
When the modem is connected to the telephone line (L1, L2), the components are bypassed (see relay) and the telephone set (TPH1, TPH2) disconnected.

The ringing signal (50 Hz alternative voltage superimposed to the 50 V telephone line voltage), is so attenuated by the resistor but the level is sufficient to be detected by the TS7514.

Do not forget during the detection to bypass the receive filter in the RPRF register (bit 2 programmed to "1").

So programmed, the TS7514 output on ZCO pin a 50 Hz digital signal and on $\overline{DCD}$ pin the ring "enveloppe" (figure 5).

Figure 5.

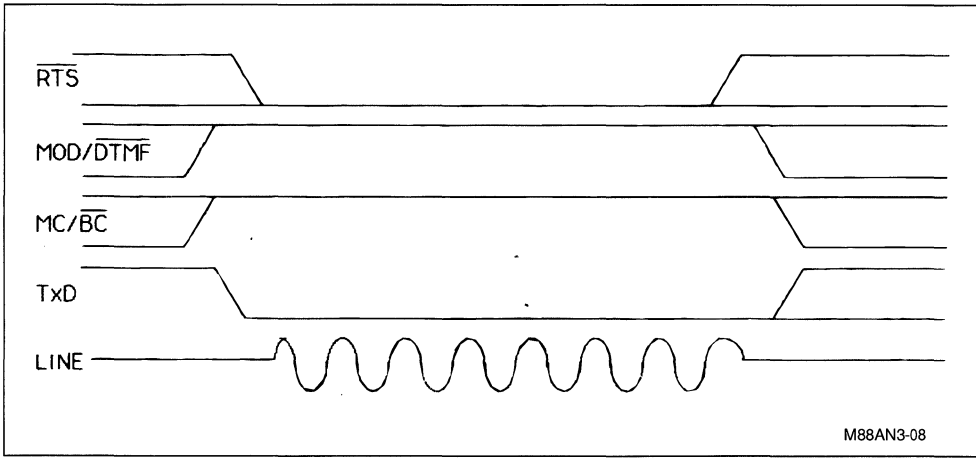


7. TONE TRANSMISISON AND DETECTION

7.1. 2100Hz TRANSMISSION

To send the 2100 Hz answer tone over the telephone line, the TS7514 must be programmed as follows :

- MOD/$\overline{\text{DTMF}}$ = "1" (modem),
- MC/$\overline{\text{BC}}$ = "1" (main channel),
- $\overline{\text{TxD}}$ = "0" (2100 Hz),
- $\overline{\text{RTS}}$ = "0" (transmission).

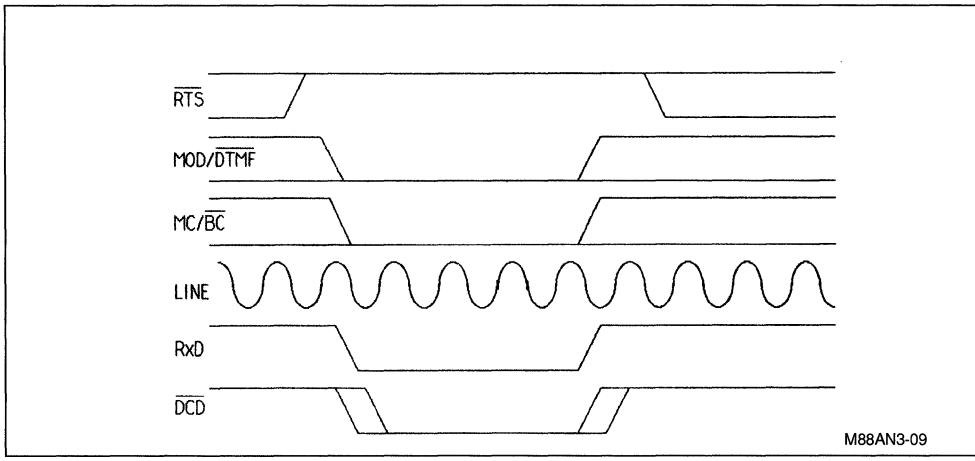


7.2. 2100 Hz DETECTION

To detect the 2100 Hz answer tone sended by the far-end modem, the TS7514 must be programmed as follows :

- $\overline{\text{RTS}}$ = "1" (no transmission),
- MOD/$\overline{\text{DTMF}}$ = "0" (tone detection),
- MC/$\overline{\text{BC}}$ = "0" (back channel).

So programmed, the TS7514 detects the 2100 Hz answer tone on line if $\overline{\text{DCD}}$ = "0" (carrier detection) and RxD = "0" (2100 Hz).

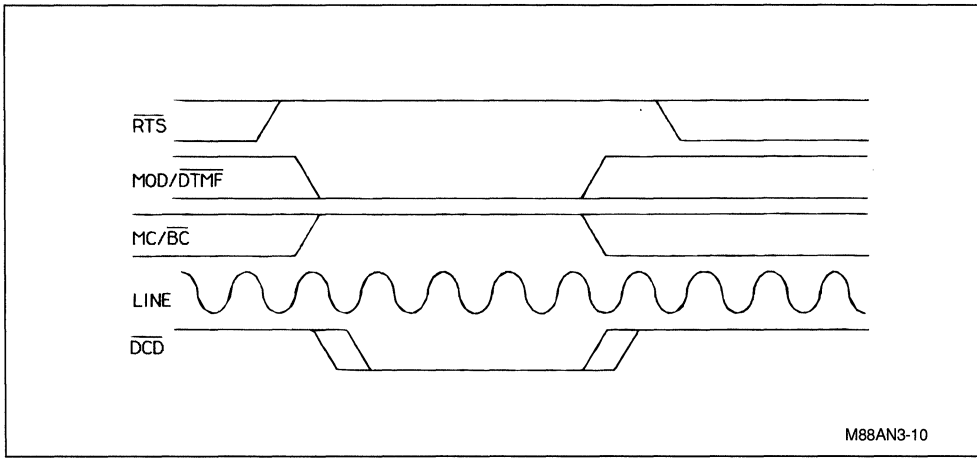


7.3. LOW FREQUENCY TONE DETECTION

To detect low frequency tones (typically the 440 Hz dialing tone in France) ; the TS7514 must be programmed as follows :

- RTS = "1" (no transmission),
- MOD/DTMF = "0" (tone detection),
- MC/BC = "1" (main channel),

Then, such tones are present on line if DCD = "0" (carrier detection).



Note : In this mode, the RPRX register is automatically programmed to wide band filter for the receive low channel.

8. LINE MONITORING

To monitor the different signals present on the telephone line, figures 6 and 7 give two typical loudspeaker amplifier application schemes.

Thanks to RWLO monitoring level programming register, no external potentiometer is required to adjust the volume.

Figure 6.

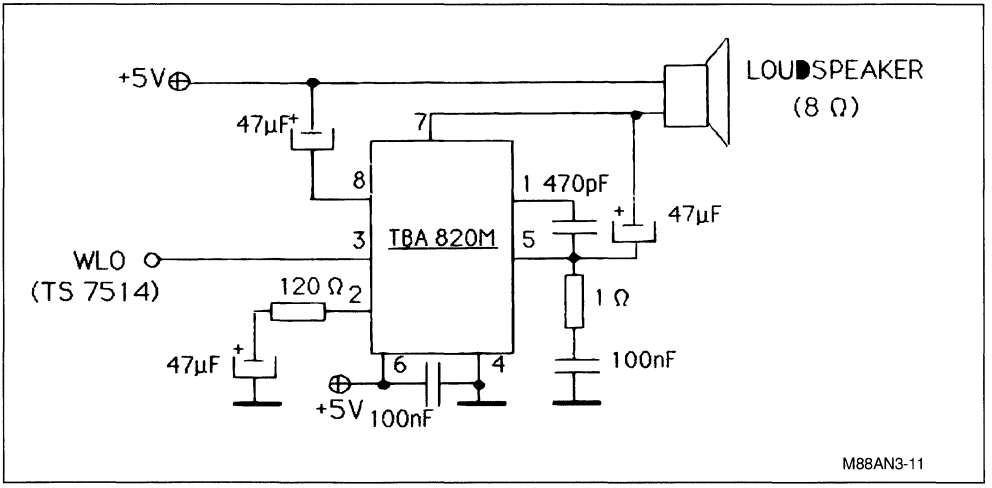
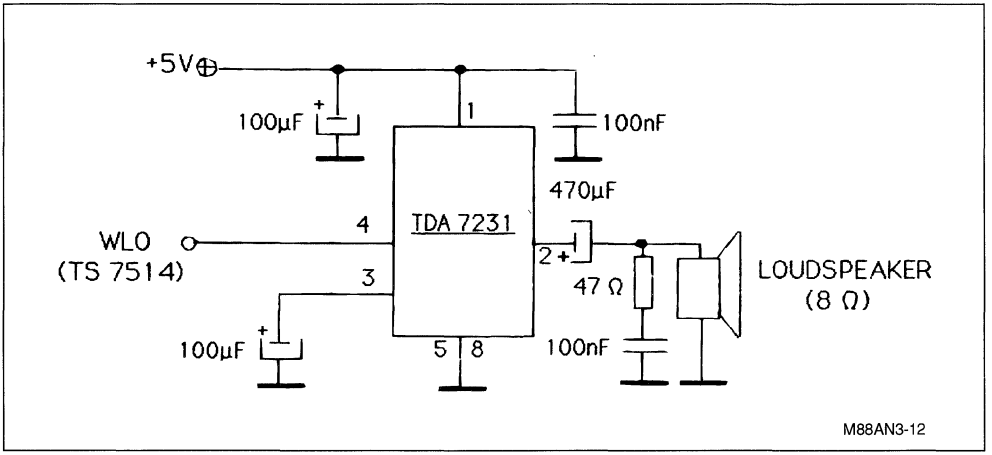


Figure 7.



9. OTHER FEATURES

- by ATxI, it is possible to send a voiceband signal over the telephone line,
- the XtalOUT may be used to implement via a buffer, the external clock of the microcontroller,
- the lay-out implementation must be as clean as possible in order to obtain the best electrical performances :

■ separation between analog and digital parts and tracks of the board,
■ analog and digital grounds separated and connected in a single point,
■ a ground plane for the component side,
■ a star distributed power supplies (idem for ground) to avoid any possible loop,
■ a maximum capacitive uncoupling as close as possible to the device,
■ a connection as short as possible between RFO and RDI via the external capacitor.

10. CONCLUSION

We just saw, with this application note, the different functions and internal possibilities included in the TS7514 among which D.T.M.F. dialing, integrated duplexer, tone and ring detection and transmit and receive channel programmings are the most interesting.

For these features and all the others, only about 20 external passive components (resistors, capacitors, ...) are required (out of microcontroller interface) to implement a complete V.23 modem.

The TS7514 is a real low cost and powerful solution for all C.C.I.T.T. V.23 recommended standard applications.

POWER SUPPLY MODULE

SGS-THOMSON MICROELECTRONICS

GS-M51212

13W TRIPLE OUTPUT DC-DC CONVERTER MODULE

- MTBF IN EXCESS OF 200.000 HOURS
- 2A OUTPUT CURRENT @ 5V
- ± 12V/0.125A OUTPUTS
- WIDE INPUT VOLTAGE RANGE
- 75% EFFICIENCY
- PROTECTED AGAINS SHORT CIRCUITS
- VERY LOW RIPPLE AND NOISE

DESCRIPTION

The GS-M51212 is a versatile triple output module specifically designed for modem boards supply. The unit can be supplied either with a center tapped transformer secondary winding or a DC voltage.

Two unregulated outputs (± 12V @ 125mA) useful for LED lamps or relay supply are also available.

These outputs are not short circuit protected and an input fuse on the input return is recommended.

The unit is characterized by a .65 inches maximum height to allow a 1 inch board spacing.

MAIN CHARACTERISTICS

Output Voltage (V)	Output Current (A)	Input Voltage (V)	Output Ripple (mVpp)	Eff. (%)
V1 + 5.1 ± 4%	2.000		50	
V2 + 12.0 ± 5%	0.125	±12Vdc ± 25%	20	
V3 − 12.0 ± 5%	0.125	or	20	75
V4 + 12.0 unr.	0.125	9 + 9Vac ± 25%	1600	
V5 − 12.0 unr.	0.125		1600	

ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C and V_{in} = 9 + $9V_{ac}$ ± $12V_{dc}$ unless otherwise specified)

Symbol	Parameter	Value	Unit
	Input Data		
	Maximum DC Input Voltage	± 15	V
	Maximum AC Input Voltage	11,25 + 11,25	V
	Output Data		
	Minimum Load Current (5V output)	200	mA
	Current Limitation Intervention	< 3	A
	Environmental Data		
	Operating Temperature Range	0 to + 70	°C
	Storage Temperature Range	− 40 to + 85	°C

USER NOTES

INPUT VOLTAGE

The recommended operating maximum DC input voltage is ± 15V inclusive of the ripple voltage.

The recommended operating maximum AC input voltage is 11,25 + 11,25V derived by a transformer center tapped secondary.

MODULE PROTECTIONS

The module is protected against occasional and permanent short circuits of the regulated output pins to ground, as well as output current overload. The two unregulated outputs are not protected versus short circuit.

THERMAL MANAGEMENT

The module is rated for correct operation up to an ambient temperature of 70°C assuming a sufficient air volume in the surrounding is provided to allow normal correction.

Figure 1 : GS-M51212 Block Diagram.

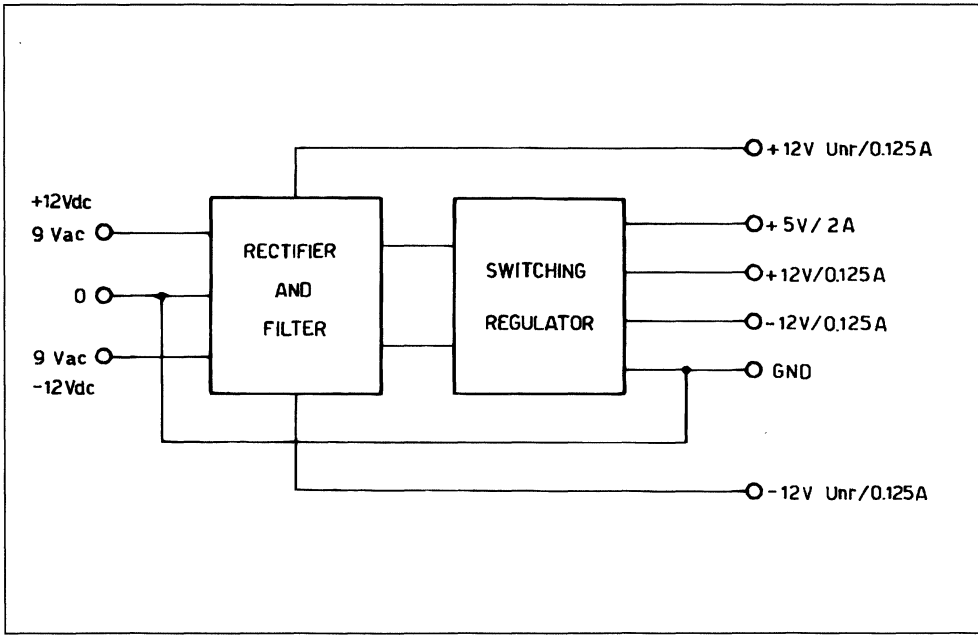
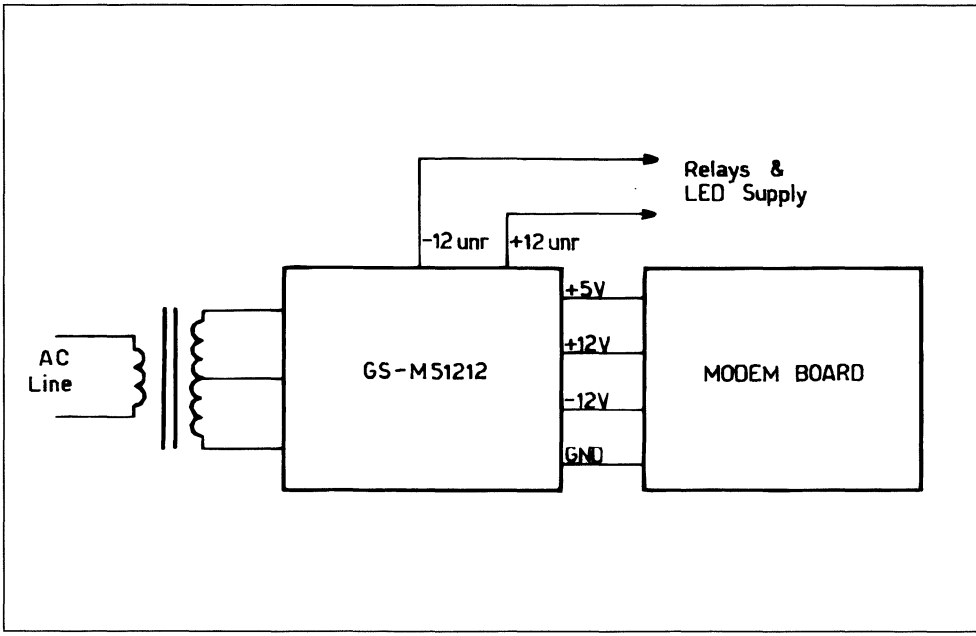


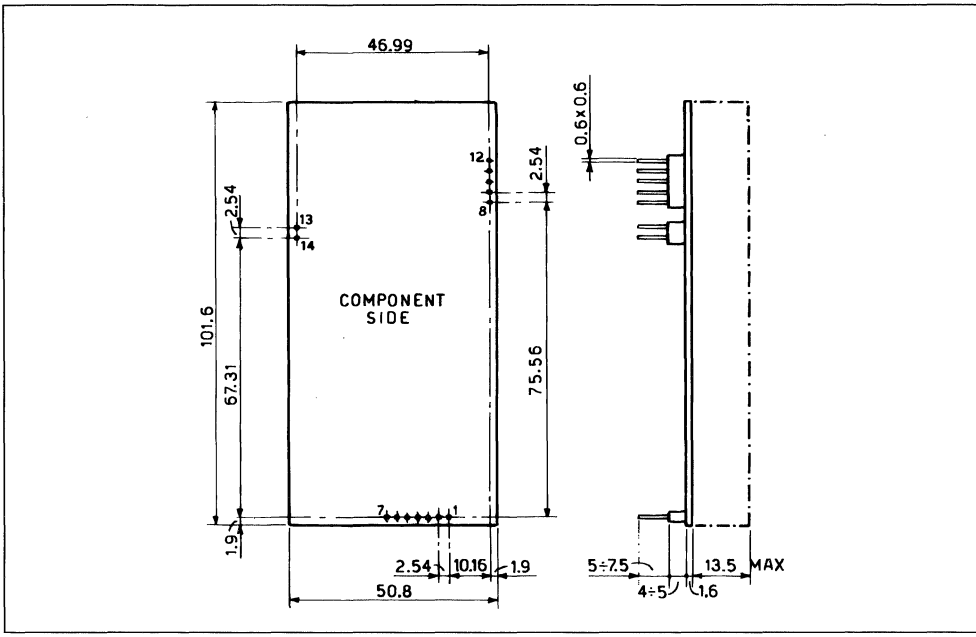
Figure 2 : GS-M51212 Typical Application.



PIN CONNECTION

Pin	Function	Description
1	Vac/V_{DC} IN	AC Input Voltage. Recommended voltage is 9 V_{DC} or 12 V_{DC}.
2, 3, 4	Ground in	Return for Input AC/DC voltage. The transformer center tap must be connected to this pin. This pin is also the return path.
5	Vac/V_{DC} IN	Input Voltage. Recommended voltage is 9V or 12V_{DC}.
6	– 12Vunr	Unregulated – 12V output
7	+ 12Vunr	Unregulated + 12V output
8, 9	+ 5V	Regulated 5V output
10	Ground out	Return path for regulated outputs. Connected to pin 2/3/4.
11	– 12V	Regulated – 12V output
12	+ 12V	Regulated + 12V output
13	Enable	Hardware Enable Pin. This pin must be tied to pin 11 to operate the unit.
14	En. return	Return path for the Enable.

MECHANICAL DRAWING



DSP DATASHEETS

DIGITAL SIGNAL PROCESSOR

- 80 ns INSTRUCTION CYCLE TIME * (1.2 µ CMOS technology)
- PARALLEL HARVARD ARCHITECTURE
- SEPARATED PROGRAM AND DATA BUSES
- THREE DATA BUSES STRUCTURE
- DUAL EXTERNAL BUSES
- ONE CYCLE 16-BIT R/W OPERATION ON EXTERNAL DATA MEMORY
- THREE DATA TYPES : 16-BIT REAL, 32-BIT REAL, 16 + 16-BIT COMPLEX
- HARDWARE MASKABLE INTERRUPT
- COMPLEX MULTIPLIER
- 320 x 16-BIT INTERNAL RAMs, 512 x 16-BIT INTERNAL COEFFICIENT ROM
- 3 K x 32-BIT WORDS OF INTERNAL PROGRAM ROM
- LOW POWER MODE
- REALTIME EMULATION OF ST18930 ROM VERSION WITH ST18931 ROMLESS VERSION

DESCRIPTION

The ST18930/31 HCMOS digital signal processors are members of SGS-THOMSON family of general purpose DSP's fully software and hardware compatible with previous members of the family.

By virtue of their highly parallel architecture, these digital signal processors are well suited to a wide range of applications including those requiring operations on complex numbers.

Typical examples are found in telecommunications, modems, image and speech processing, high speed control, digital filtering, sonar and radar applications.

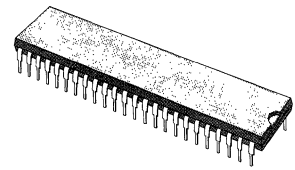
They are able to execute simultaneously within 100 ns an ALU function, a Multiplication, two Read and one Write operations with associated address calculation.

The on-chip large memory resources and multiprocessor direct interface allows the development at the lowest cost/complexity of high performance applications. The ST18931 is the ROMless version of the ST18930. In addition of the ST18930 features, it provides the capability of addressing up to 64Kx32-bit external instruction memory and allows a total realtime emulation of the ST18930. It is also particularly well adapted for applications where large program memory is required or for low quantities.

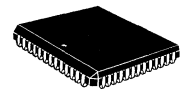
DEVELOPMENT SYSTEMS

The ST18930 is supported by a complete set of hardware and software tools for applications development. Software packages include assembler, linker and simulator on VAX and PC as well as a high level "C" compiler and optimizer.

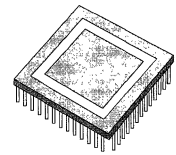
Hardware tools include a stand-alone emulator, eprom emulation module and a powerful multiprocessor development station.



ST18930
P
DIP 48
(Plastic Package)



ST18930
FN
PLCC52
(Plastic Leaded Chip Carrier)



ST18931
R
PGA121
(Pin Grid Array Ceramic)

For pin connections and order codes, please see inside

* Also available 100 and 160 ns cycle time versions.

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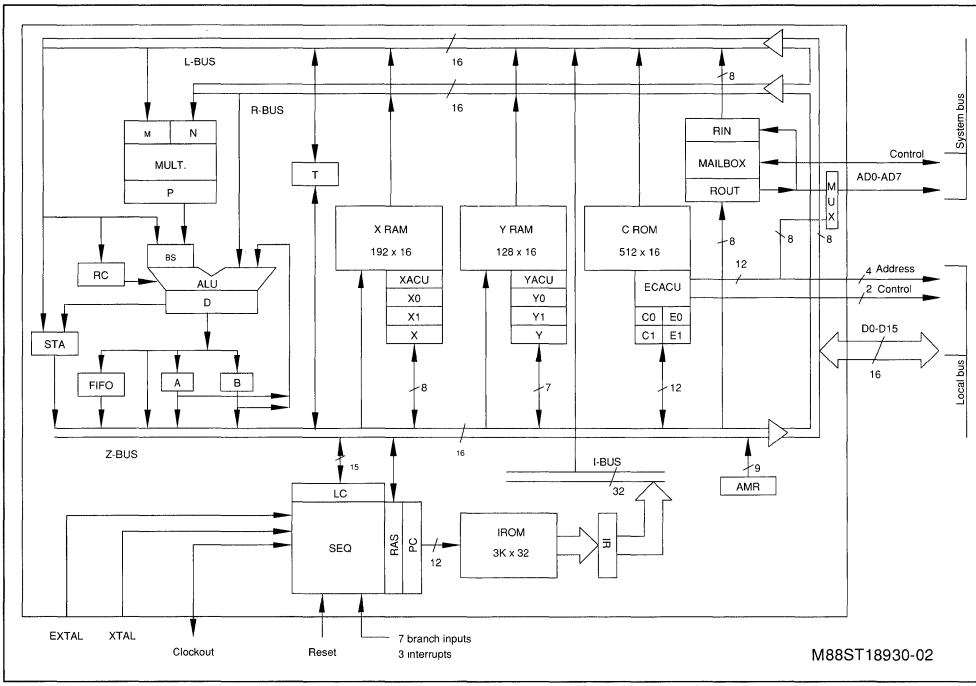
1. BLOCK DIAGRAM (ST18930)

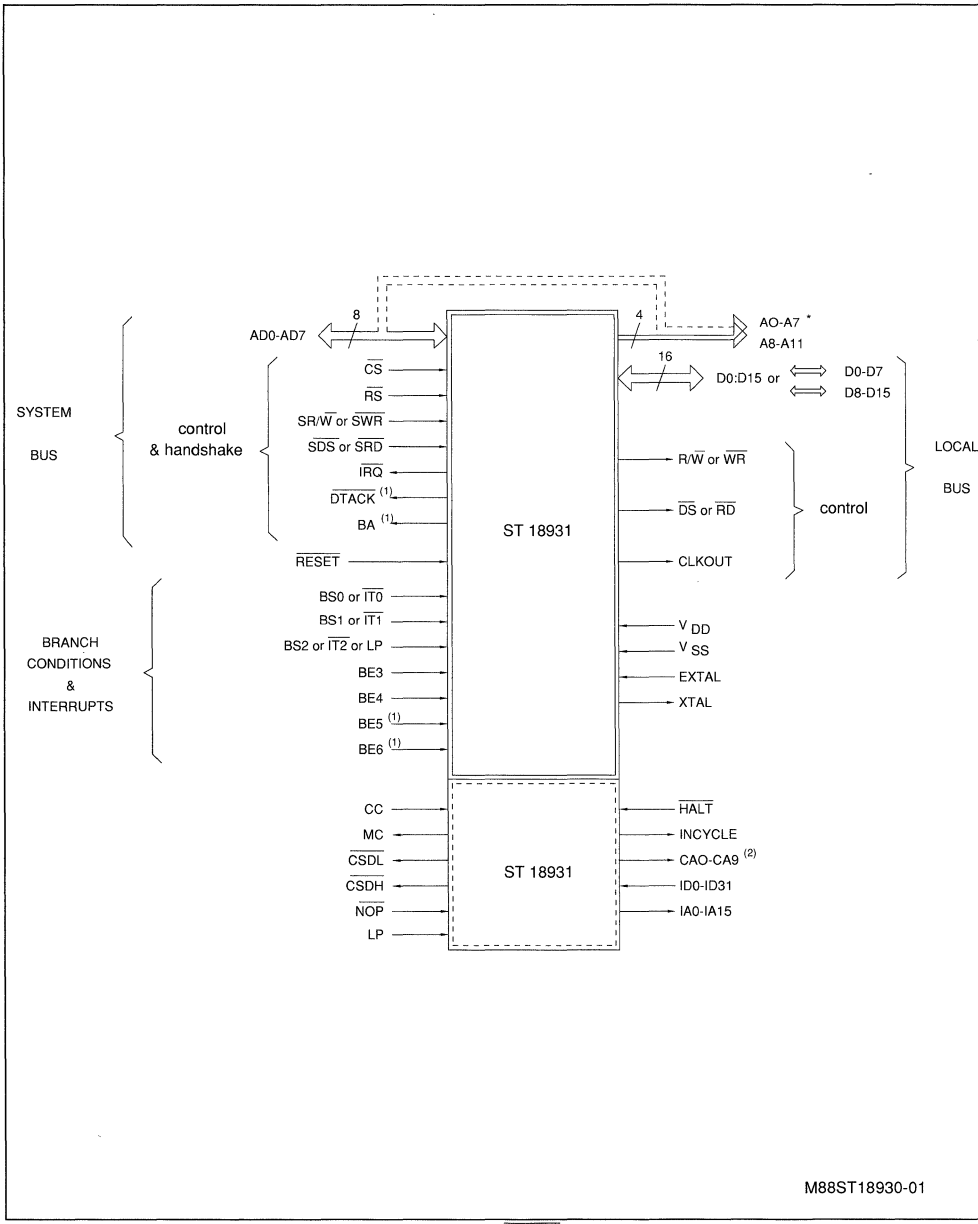


DEFINITION OF ACRONYMS

L-bus	: Left data bus	CROM	: Coefficient ROM
R-bus	: Right data bus	X0, X1, X	: Addressing registers XRAM
M	: Multiplier input register	Y0, Y1, Y	: Addressing registers YRAM
N	: Multiplier input register	C0, C1	: Addressing registers CROM
P	: Multiplier output register	E0, E1	: Addressing registers ERAM
BS	: Barrel Shifter	XACU	: Address calculation unit XRAM
ALU	: Arithmetic and Logic Unit	YACU	: Address calculation unit YRAM
D	: ALU output register	ECACU	: Address calculation unit CROM & ERAM
RC	: Replace Code register	RIN	: Input register of mailbox
STA	: Status register	ROUT	: Output register of mailbox
FIFO	: ALU output FIFO	AMR	: Access mode register
A	: ALU accumulator	IR	: Instruction register
B	: ALU accumulator	PC	: Program counter
Z- bus	: Result data bus	RAS	: Return address stack
T	: Transfer register	SEQ	: Sequencer
XRAM	: X Data RAM	LC	: Loop Counter
YRAM	: Y Data RAM	IROM	: Instruction ROM

2. PIN DESCRIPTION

Figure 1 : Input/Output Pins.



Notes : 1. these pins are shared and software programmable : BE5/DTACK, BE6/BA
2. A0-A7 and AD0-AD7 may be multiplexed.

LOCAL INTERFACE

Name	Pin Type	Function	Description
D0-D15	I/O	Data Bus	Can be concatenated or separate D (0 : 7), D (8 : 15).
A8-A11	O	Address Bus	High order addresses for local interface (RAM).
$\overline{DS}$ or $\overline{RD}$	O	Data Strobe/Read	Synchronizes the transfer on local bus/read cycle.
R/$\overline{W}$ or $\overline{WR}$	O	Read/write/Write	Indicates the current bus cycle state/write cycle.
CLKOUT	O	Clock Output	Frequency programmable from EXTAL ÷ 2 to EXTAL ÷ 16.
A0-A7	I/O	Address Bus	Low order addresses for local interface (RAM).

SYSTEM INTERFACE

Name	Pin Type	Function	Description
AD0-AD7	I/O	System Data Bus	System data bus for exchanges between the processor and a host via the mailbox.
$\overline{CS}$	I	Chip Select	Used by a host to gain access to the mailbox and system bus.
$\overline{RS}$	I	Register Select	Used by a host to gain access to the mailbox and system bus.
$\overline{SDS}$ or $\overline{SRD}$	I	Data Strobe/read	Synchronizes the transfer on the system bus/read cycle.
SR/$\overline{W}$ or $\overline{SWR}$	I	Read/write/Write	Indicates the current system bus cycle state/write cycle.
$\overline{DTACK}$	O	Data Transfer Acknowledge	Indicates that the processor has recognized the access data transfer.
BA	O	Bus Available	Indicates the availability of the sytem bus to the host.
$\overline{IRQ}$	O	Interrupt Request	Handshake signal sent to the host to gain access to the mailbox.

EXTERNAL BRANCH CONDITIONS AND INTERRUPT

Name	Pin Type	Function	Description
BS0-$\overline{BS2}$ or IT0-$\overline{IT2}$	I I	Branch on State Interrupt	External Branch Conditions. (low power mode through BS2 see 3, 6, 4) Interrup Input Pins
BE3-BE6*	I	Branch on Edge	External conditions. Falling edge is memorised and reset when tested.

* BE5 shares pin with $\overline{BA}$
BE6 shares pin with DTACK

OTHER PINS

Name	Pin Type	Function	Description
EXTAL	I	Clock	Are used for crystal oscillator ; if crystal oscillator is not used, pin XTAL is not connected.
XTAL	O	Clock	
V_{DD}	I	Power Supply	
VSS	I	Ground	
$\overline{RESET}$	I	Reset	
LP	I	Low Power	Active at high state. Freezes the circuit operation.

INSTRUCTION INTERFACE AND SYSTEM CONTROL INTERFACE (ST18931 only)

Name	Pin Type	Function	Description
ID0-ID31 IA0-IA15 CA0-CA9	I O O	Instruction Data Instruction Address Coef. ROM Address or External RAM Address	Instruction Data Bus Instruction Address Bus External coefficient ROM address 10 bit or External RAM address (9-bit address – output enable signal) (8-bit address)
$\overline{HALT}$	I	Halt Signal	Halts the processor. This signal freezes the program and loop counters
INCYCLE	O	Instruction Cycle Clock	A transition from low to high indicates that a new instruction is processed
$\overline{NOP}$	I	Hardware NOP	Force NOP instruction for development system.
$\overline{CSDL}$ $\overline{CSDH}$	O	Bus Low Z Control	D0 – D7 (CSDL) and D8 – D15 (CSDH) are data valid control pins for external buffers
CC	I	Clock Cycle Control	Machine cycle = 2 T_c (EXTAL) or 4 T_c (EXTAL)
MC	O	Master clock	EXTAL ÷ 2 Output

3. FUNCTIONAL DESCRIPTION

3.1. GENERAL ARCHITECTURE

The ST18930/31 architecture is based upon the innovative architectural concepts already proven in the previous members of SGS-THOMSON digital signal processors family.

Therefore, the compatibility is kept at object code level with the TS68930/31.

The ST18930/31 confirm the efficiency of a highly parallel and pipelined operation using a true Harvard memory space and bus structure. This efficiency is there improved by the advanced 1.2 µ HCMOS technology providing 80 ns instruction cycle.

The block diagram shows four main blocks :

. The sequencer block

. The operating unit (ALU, Multiplier and Barrel Shifter)

. The data memories

. The inputs/outputs

These four blocks can be considered as four independent units working in parallel and communicating through a network of 16/32 - bit buses.

By taking advantage of the 32 - bit wide instruction bus, the ST18930/31 are able to execute simultaneously the following operations during each 80 ns machine cycle :

. Read two operands from internal or external memory

. Execute a multiplication

. Perform an ALU operation

. Write a result into internal or external memory

. Post modify three pointers independently

. Store data into the transfer register

In addition, data exchanges through mailbox occur concurrently and independently of internal operations.

All instructions are executed in a single cycle time except branch instructions.

Some additional features give the ST18930/31 extremely powerful performances. They provide three operating modes (real, complex and double precision) dynamically set by software and user transparent.

In complex mode, the hardware multiplier provides (16 + 16 - bit) results from 2 x (16 + 16 - bit) inputs each machine cycle.

(25 - million multiplications per second).

The ALU, reinforced by a barrel shifter, provides 30 basic arithmetic and logic functions.

Three dedicated calculation units control the four data memory spaces.

A large 3Kx32 (96Kbits) program ROM (for the ST18930) enlarge the usual digital signal processor applications possibilities, using the efficiency of the

code and architecture. The following sections will detail all the hardware blocks of the ST18930/31 and demonstrate its software performances provided by the high level of parallelism in the operations.

3.2. OPERATING UNIT

One of the most useful features of the ST18930/31 is to provide the user three operating modes which can be dynamically set by software.

These three modes are :

. REAL 16 - bit

. COMPLEX 16 - bit real + 16 - bit imaginary

. DOUBLE PRECISION 32 - bit

Thus, the DSP is seen by the user as a standard 16 - bit real or complex machine or a 32 - bit real machine. All operating units and working registers are automatically adjusted by the processor to the right length. In real mode, all instructions are executed in a single machine cycle. In complex and double precision mode, the instruction time is doubled.

In all modes, the number representation used is signed 2's complement.

3.2.1. 16/32 - Bit ALU/Accumulator (fig. 2). The ALU can be seen either as a 16 or 32 - bit ALU. The ALU is loaded on the right side by the R - bus or by the A or B accumulators.

On the left side, the operands always access the ALU through the barrel shifter, coming either for the L (left) - bus or the hardware multiplier output register P.

The result of an ALU operation is automatically written in the D register and, if required into the Accumulator or FIFO. The ALU provides a range of 30 codes for operations which execute in a single machine cycle. They include arithmetic and logic operations, shift and rotate operations.

The high degree of parallelism of the ST18930/31 processor allows more combinations than previous generation DSP devices which require a more complex instruction set.

The complete list of ALU codes and description is given in 3.8.2.

3.2.2. Barrel Shifter. The 16 - bit barrel shifter located on the left side of the ALU performs all logic/arithmetic shifts and rotations. It is used for normalization and formatting of data in floating point operations and bit or byte manipulations. Two types of operations are allowed in the barrel shifter.

- Operations defined by ALU codes (shifts of 1 or 8 bits) see 3.8.2
- Operations defined by specific dedicated instructions :

ASR ($0 \rightarrow 15$) arithmetic shift right by N ($0 < N \leq 15$)

LSR ($0 \rightarrow 15$) logical shift right by N ($0 < N \leq 15$)

LSL ($0 \rightarrow 15$) logical shift left by N ($0 \leq N \leq 15$)

ROR ($0 \rightarrow 15$) rotation right by N ($0 < N \leq 15$)

In complex mode, the barrel shifter performs the same operations on complex and imaginary part.

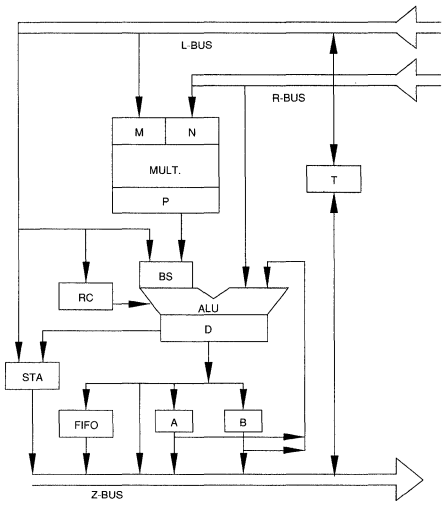
3.2.3. Multiplier. The multiplier executes a 16 x 16-bit multiplication with a 32-bit result at each machine cycle. The operands are loaded into the M and N registers and the result of a previous multiplication is written in the P register during the same cycle.

The pipeline structure makes the multiplication result available with a delay of two instruction cycles.

The multiplier provides a multiplier overflow flag OVFM which is memorized in the status register in complex mode only (see 3.2.4).

The efficiency of the parallel pipeline operation of the multiplier is shown in fig. 3.

Figure 2 : Alu Block Diagram.



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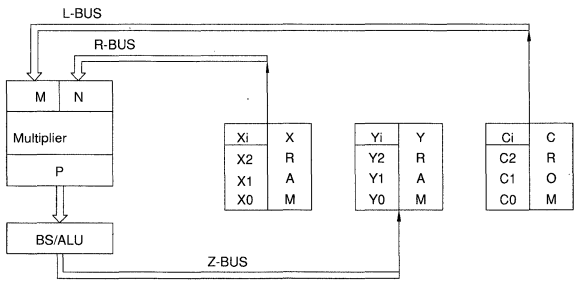
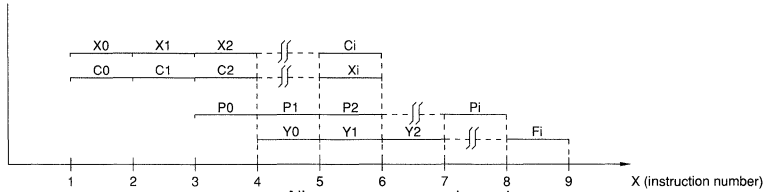
- 4 Inputs
  giving access to 10 possible sources :
  XRAM, YRAM,CROM, ERAM,
  P, T, RIN, A, B, FIFO
- 5 Destinations : A, B, D, FIFO, Z BUS
- R side by Accumulators
  L side by T registers
- 30 operations : including Arithmetic,
  Logic, Shifts,
  With 3 modes of execution :
  Real
  Complex
  Double precision
- Saturation mode to prevent overflow
- The status register gives information
  on the results of operations.
- The Replace Code Register allows dynamically changing the ALU operation code with a data.

The ALU formats are : 16-bit in Real mode
16 + 16-bit in Complex mode
32-bit in Double Precision mode

Figure 3 : Multiplier Efficiency.



$Yi = Xi.Ci$



All components are always busy

M88ST18930-04

3.2.4. Associated registers.

Registers A, B.

A and B store the results from the ALU. They are sized according to the mode of operation. They also provide capability to feedback the ALU for a new operation with the ALU result of a previous operation.

Register FIFO.

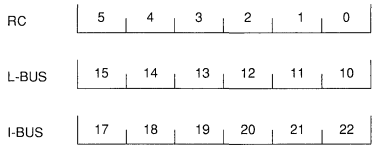
The 4 x 16-bit FIFO is used for intermediate storages. Initialization of the FIFO (empty FIFO) can be made by an INI instruction.

A result loaded in FIFO at instruction N is available at least at instruction N+2 in real mode and N+1 in complex and double precision modes.

Register RC (Replace Code register).

This register can dynamically load an ALU code to be executed by the processor from the data memories.

This register is 6-bit wide and is loaded by the 6 MSB of L-bus :



Bit 1 to 5 contain the executable ALU code corresponding to the bits I21-I17. Bit 0 allows the choice of ALU output destination (A or B register).

Its contents is defined by three ALU codes : (see 5.2.)

ALU Code	Function
RCR	Load ALU control code in register RC
RCE	Execute ALU code contained in register RC
RCER	Execute ALU code contained in RC and load new ALU code in RC

Status register (STA).

This register provides a status of the ALU, operating and addressing modes, and multiplier. It is divided into two sub-registers :

CCR (Condition Code Register)
STR (State Register)

A detailed description of this register is given in δ 5.4.

Transfer register T.

The transfer register provides a direct transfer capability between L-bus and Z-bus.

It can either be source or destination for the two buses.

Its various uses include :

* Loop back to the multiplier in one cycle
* Temporary register between memory and ALU
* Temporary register between memory and multiplier
* Operation between two accumulators in the same instruction
* Memory to memory transfer
* Saving program counter (in a branch instruction)

The status register content can be saved using instruction SVR.

The condition code register CCR can be read in OPIN instruction and it can be loaded via L-bus (ALU code LCCR).

The state register STR can be programmed by an INI instruction or an SVR instruction (except EF bit).

Register D.

This is an intermediate register which is loaded with ALU result at each machine cycle.

3.3. DATA MEMORY BLOCKS.

3.3.1. Available spaces. The ST18930/31 provides four separated memory spaces (see fig. 4)

. two internal RAMs of respectively 192 x 16-bit (XRAM) and 128 x 16-bit (YRAM)

. one internal data ROM (independent from the program ROM) of 512 x 16-bit (CROM) (ST18930 only)

. one optional external memory (ERAM) of 4 K x 16-bit accessible in 1 single instruction cycle in exactly the same way as internal memories.

This external memory is controlled by an Intel or Motorola type control interface and offers full speed, fully transparent, Read and Write operations.

However slower external memories or peripherals can be accessed by using slow exchanges mode.

The powerful instruction set and the Harvard architecture allows many combinations of simultaneous memory accesses. The only forbidden situations are :

- read and write access is the same RAM within the same instruction
- simultaneous access to CROM and ERAM

3.3.2. Address Calculation Units. Three different Addresses Calculation Units are available.

XACU is associated with XRAM

YACU is associated with YRAM

ECACU is associated with the ERAM and the CROM

3.3.3. Addressing modes. The ST18930/31 provides four addressing modes :

- Direct addressing
- Immediate operand
- Indirect addressing with or without post modification of the pointers
- Circular addressing (also called virtual shift mode) for XACU and YACU.

The circular addressing mode is of particular interest in digital signal processing typical operations like convolution algorithms used in FIR filters. It has the same function as a shift register but does not move the data stored.

For this feature, three pointers are used in the memory space chosen (X or Y). The current address is given by a specific X pointer shifting repetitively between two limits X0 and X1 (respectively Y, Y0 and Y1).

The circular mode is declared in the status register STA (see 3.2.4) by an INI instruction.

3.3.4. Pointers. The ST18930/31 offers a large number of address pointers for each memory space :

- X0, X1 and X for XRAM
- Y0, Y1 and Y for YRAM
- C0, C1 for CROM
- E0, E1 for ERAM

The pointers Xi, Yi, Ci and Ei can be independently incremented, decremented or maintained. The two pointers X and Y are specific to the circular addressing mode. The pointers can be loaded with new addresses (constant or computed values) through Z-bus. In this case, the value of unused Z-bus MSBs are irrelevant. The unused bits are set to 1.

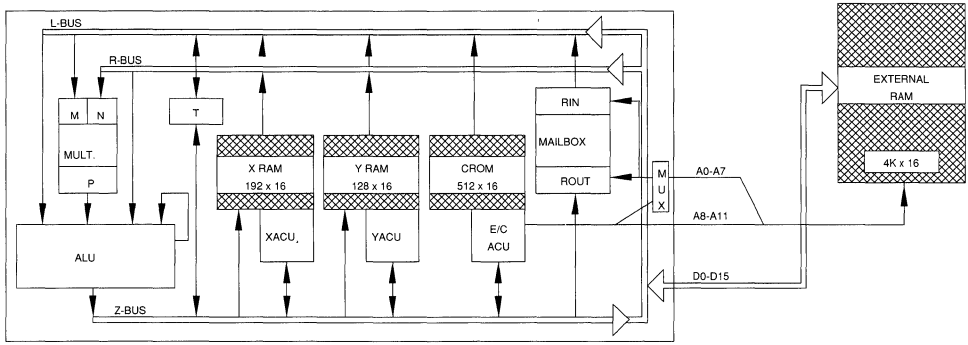
3.3.5 Odd/Even addresses. In complex and double precision modes, the processor automatically generates the two addresses necessary to store

one data word (even first, then odd addresses).

The user can reverse this order by setting to 1 the ADOF bit with the INI instruction (refer to OPCODE). This feature is available independently for XRAM and YRAM.

	COMPLEX WORD	DOUBLE PR. WORD
Even Address	Real Part	Lower Part
Odd Address	Imaginary Part	Upper Part

Figure 4 : Data Memory Blocks.



3.4. SEQUENCER BLOCKS

3.4.1. Sequencer. The purpose of the sequencer is to generate the next instruction address.

The sequencer takes into account the current operating mode of the ST18930/31 to execute this task. The instruction is executed in one cycle time in real mode and two cycles time in complex or double precision mode.

The linear address program generation may be interrupted by several means hereunder described.

A. Execution of a branch instruction
- unconditional branch always.
- seven ALU conditions flagged from the status register :

SR	Sign real
SI	Sign Imaginary
CR	Carry Real
CI	Carry Imaginary
Z	Zero
OVF	Overflow
MOVF	Memorized overflow MOVF is reset when tested by branch instruction.

- three external conditions on state of pins BS0, BS1, BS2 (the pins BS0, BS1, BS2 can also be used as interrupt pins if enable interrupt is programmed).
- four edge sensitive external conditions on pins BE3, BE4, BE5, BE6. The falling edges of BE3-BE6 are memorized internally and reset when tested by the branch instruction. The external test conditions are used to synchronize different processes.
- The mailbox flag RDYOIN indicating mailbox availability.

All the branch conditions can be tested on true or false conditions.

B. Subroutine call

C. Loop execution

One of the most powerful features of the ST18930/31 is its ability to repeat the execution of several instructions with very straightforward commands. The loop execution is set with the instructions : REPEAT, BEGIN, END which respectively define the number of loops, the beginning of loop and its end. The DSP will then manage all the necessary pointers to execute the loop with no overhead time (see 3.4.4.).

D. Execution of an interrupt routine

When the Enable Interrupt bit (EI) of the status register (STA) is set, a low level on any of IT0, IT1 and IT2 inputs forces the PC content at $ 0001. Mailbox interrupts can be enabled separately from IT inputs interrupt ; it occurs when a mailbox exchange has been completed (see & 3.5.6). During interrupt routines execution, the program counter is saved in the Return Address Stack (RAS).

3.4.2. Instruction ROM. The ST18930 instruction ROM has a capacity of 3072 words of 32-bit available for the user. The ROM code is defined following the user's information (see appendix C for masking information). The ST18931 does not provide an on-chip ROM memory, but can address an external 64 K program memory space in a single cycle.

3.4.3. Program Counter. The program counter is a 16-bit wide Register ; 12 bits are used in the ST18930 (ROM version).

3.4.4. Loop Counter. The loop counter does considerably increase the efficiency of the processor in repeated calculations, very commonly used in digital signal processing.

Three counters define a hardware loop :

- LCI Instruction Loop Counter (4-bit). Counts the number of instructions to be executed in the loop.
- LCR Repeat Loop Counter (8-bit). Gives the number of times the loop will be repeated (can be loaded by a calculated value).
- LCD Delay Loop Counter (3-bit). Gives the delay between the declaration and the start of a loop.

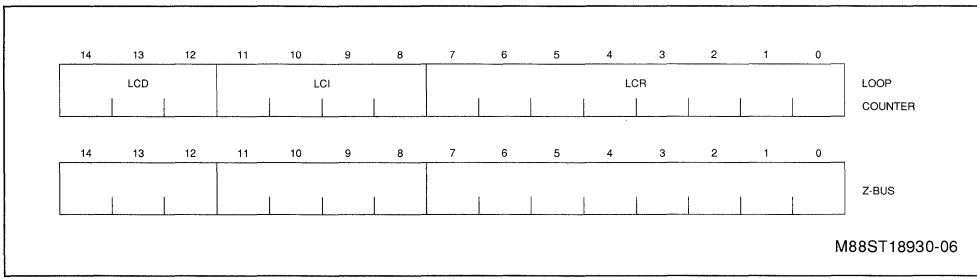
The loop counter content can be saved (SVR instruction) with the format shown in table below :

The loop counter is set by the three pseudo-instructions Begin, Repeat and End in the Macroassembler.

The loop counter is frozen during an interrupt routine.

On the ST18931, a HALT freezes the state of the loop counter. A RESET signal resets the loop counter.

3.4.5. Return Address Stack. The JSR instruction allows one level of subroutine nesting with automatic saving of the PC on to the Return Address Stack. Multiple Level of subroutine nesting can be implemented in RAM using either of the two pointers as stack pointer.



3.5. INPUTS/OUTPUTS

A very important feature of a signal processor is its ability to be inserted in a complete system including memories, other processes, analog interface circuits.

Basically, the external world seen by a ST18930/31 can be divided in two main sections : communications with its own local resources (peripheral, memories, converters) and communications with control processor, either microcontroller or master DSP in a multiprocessor application.

To communicate with its local resources, the ST18930/31 uses its local bus.

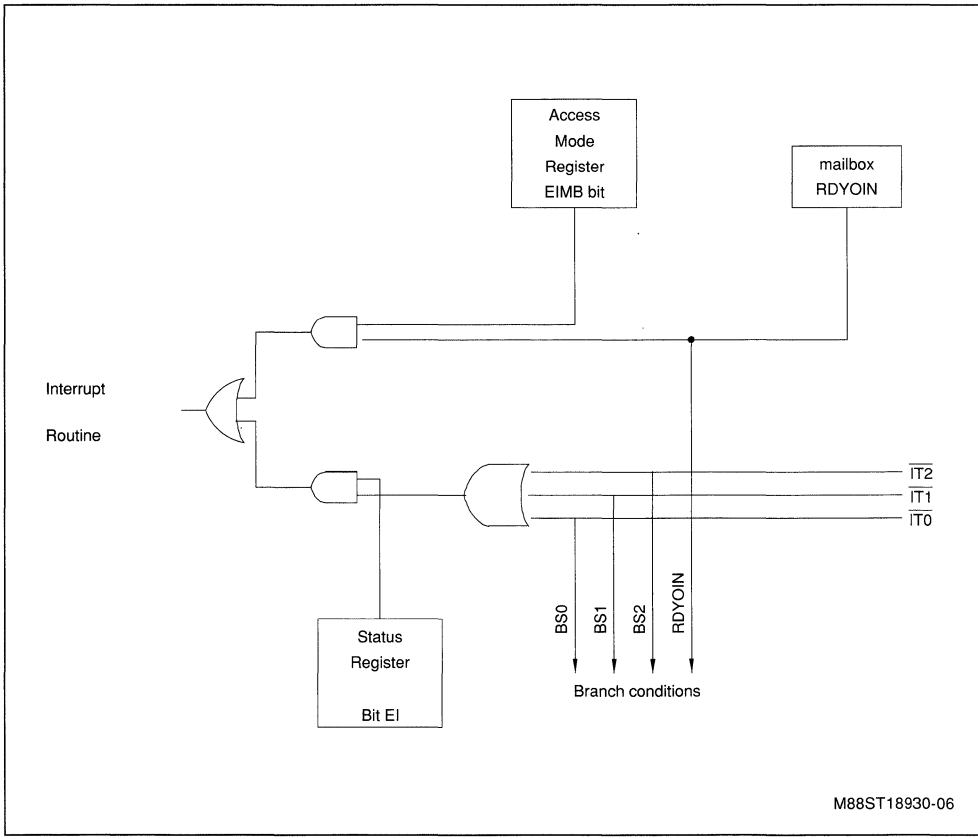
To interface with a host, the ST18930/31 uses its system bus and interrupt/branch capabilities.

However, the local and system bus configuration is flexible and allows many combinations for the architecture of a system based around a ST18930/31.

3.5.1. Interrupt branches. Several sources of interrupt and branch conditions are accepted by the ST18930/31. Depending on the initialization (INI) the ST18930/31 can accept interrupts from pins, IT0, IT1, IT2. It can also and independently accept software interrupts transmitted through the mailbox.

The various sources/conditions of interrupts are summarized in fig. 5 :

Figure 5 : Interrupt Inputs and Conditions.



3.5.2. Dual bus interface. In order to provide the maximum flexibility, the ST18930/31 provides two buses. One is called the system bus and is found on pins AD0-AD7, the other one called local bus is situated on pins D0-D15. The system bus provides a very straightforward interface to a host controller, while the local bus allows the ST18930/31 to make an efficient use of external resources such as memories, analog interface circuits etc... This dual bus structure allows many combinations of circuits where the ST18930/31 can act in different ways :

Fig. 6A as a microprocessor peripheral

Fig. 6B as a processor with its associated memory

Fig. 6C as an intelligent peripheral having its own external memory and connected to a microprocessor.

It must be emphasized that, in most configurations, the connections are absolutely direct and do not use any external additional logic.

Furthermore, thanks to the dual bus structure, several ST18930/31 can be very simply combined together in multiprocessor applications, thereby directly increasing the processing power.

Figure 6 A : HOST/ST18930.

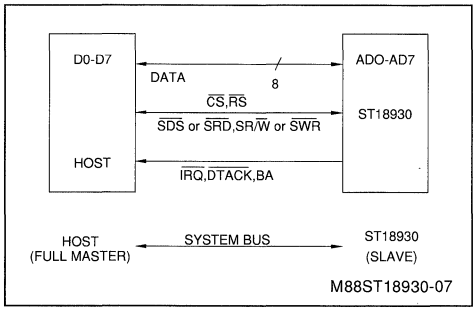


Figure 6 B : ST18930/RAM.

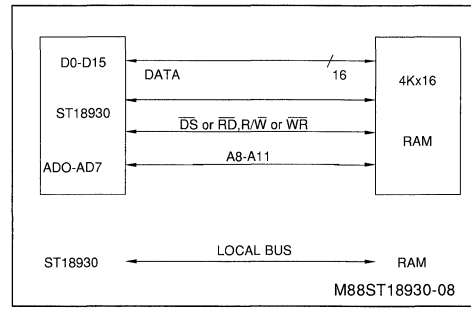
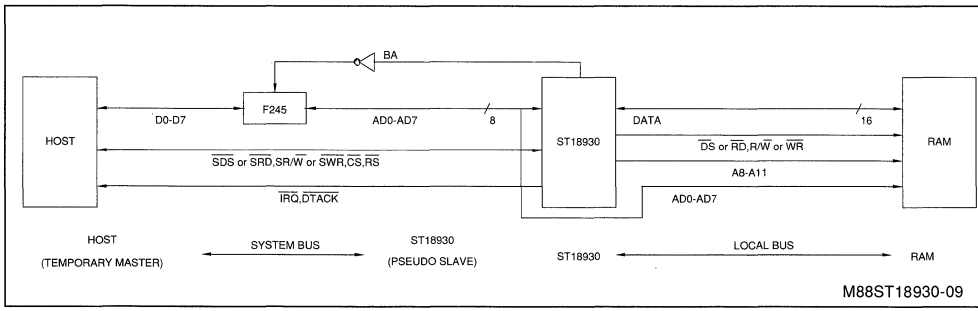


Figure 6 C : HOST/ST18930/RAM.



3.5.3. Host/slave configuration. The processor acts as a host on its local bus and as a slave on its system bus.

In configurations in which the ST18930 accesses external RAMS on its local bus, pins AD0-AD7 can be used to provide 8 LSB addresses, while A8-A11 provides 4 MSB addresses to the RAM.

In this case, the ST18930/31 prevents the host from using the system bus and is then called a pseudo-slave.

Since the host can only temporarily access the system bus it is defined as a temporary master. That mode of operation is software controlled through the Access Mode Register (AMR) (see 3.5.7.).

On the ST18931 the pins CA0-CA7, which present the least significant bits of external ERAM/CROM addresses can be connected to that RAM in place of system bus pins AD0-AD7.

3.5.4. Local bus. The local bus uses two software programmable signals to control the data on D0-D15.

$\overline{DS}$: Data Strobe. Synchronizes the transfer on local bus.

R/$\overline{W}$: Read/Write. Indicates the direction of the data.

These signals are used for Motorola-like bus compatibility.

$\overline{RD}$: Read. Read clock pulse.

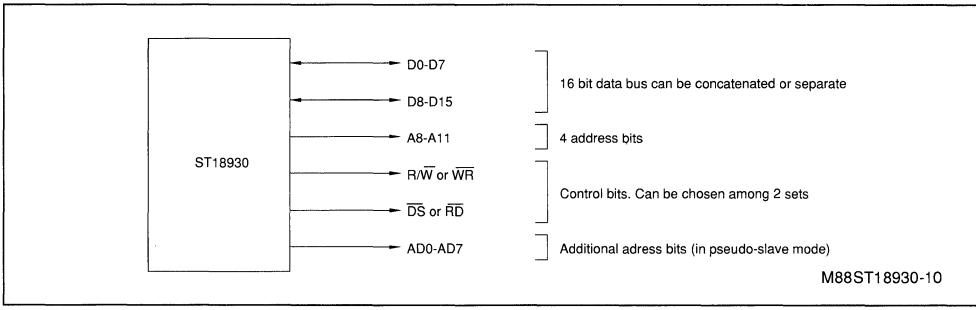
$\overline{WR}$: Write. Write clock pulse.

These signals are used for Intel-like bus compatibility.

A8-A11 : Address bits (4)

AD0-AD7 : Optional additional address bits (8)

Figure 7 : Local Bus Pin Description.



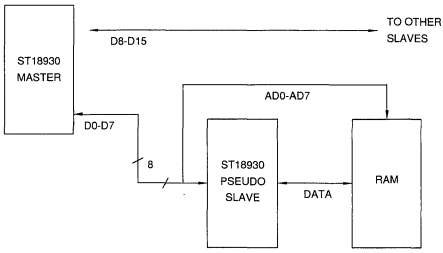
The four address bits of the local bus are usually sufficient to address peripherals. When an access to external RAM is necessary with the ST18930/31, the address bus can then be extended by using the AD0-AD7 pins of the system bus as address lines.

If an external peripheral or external memories are too slow to answer in one machine cycle, the ST18930/31 can be programmed to execute an external access in several cycles (2, 3 or 4) using the bits ES0 and ES1 of Access Mode Register (see 3.5.7.).

This mode is particularly useful for peripherals such as data converters, or dedicated interface like the MAFE chip set (Modem Analog Front End) from SGS-THOMSON.

The local data bus can also be splitted into two independent 8-bit buses. This is used in a multiprocessor architecture when a pseudo-slave uses the system bus to transfer its own RAM addresses on D0-D7 (fig. 8). By dividing its local bus, the temporary master can remain a full-master on bus D8-D15 and does not require a bus transceiver on D0-D7. The selection between the two buses is then made by the addresses A10-A11 as indicated in Fig. 8.

Figure 8 : Separate Local Buses.



A_{11}	A_{10}	$D_0 - D_7$	$D_8 - D_{15}$
0	0	Selection	High Impedance
0	1	High Impedance	Selection
1	0	High Impedance	Selection
1	1	High Impedance	Selection

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3.5.5. System Bus : The system bus uses two software programmable signals to control the data on AD0-AD7.

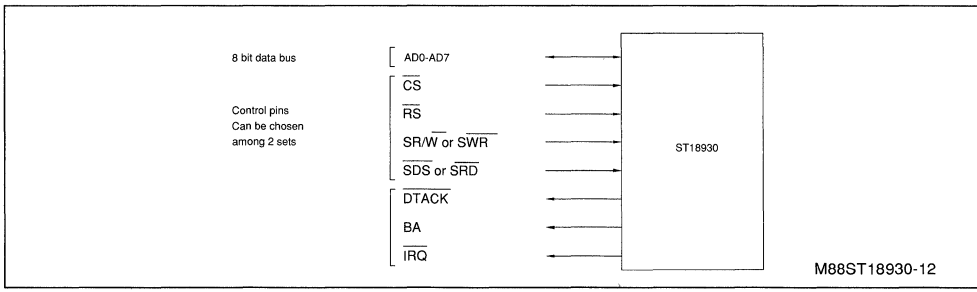
The system bus mode of operation (Intel or Motorola) is set by asserting the SIM Flag using an INI instruction).

SR/$\overline{W}$ and $\overline{SDS}$ signals are used for Motorola-like bus compatibility.

$\overline{SWR}$ and $\overline{SRD}$ signals are used for Intel-like compatibility.

$\overline{CS}$/$\overline{RS}$	Mailbox control signal. Also used by a host to gain access to the bus.
SR/$\overline{W}$ or $\overline{SWR}$ $\overline{SDS}$ or $\overline{SRD}$	System Read/Write System Data Strobe } Generated by an external processor (host)
$\overline{IRQ}$	Handshake Signal (see 3.5.6)
$\overline{DTACK}$	Data Transfer Acknowledge. Compatibility with 68000 family. Is programmed by Access Mode Register.
BA	Bus Available. The ST18930/31 is not currently using the system data bus to generate addresses. BA is also programmable by the Access Mode Register.

Figure 9 : System Bus Description.



3.5.6. Mailbox. The mailbox is a set of registers which interface with the system data bus. The mailbox is divided in two parts :

- RIN (3 x 8 bit register) : This register is read internally by the ST18930/31 on the upper byte of L-bus (L8-L15) and written externally from the system bus. After each write or read operation the data is shifted by one byte.
- ROUT (3 x 8 bit register) : This register is written internally with the upper byte of the Z-bus (Z8-Z15) and read externally on the system bus. After each operation (read or write), the data is shifted by one byte.

protocol signal description.

RDYOIN.
Internal flag indicating the status of the mailbox
0 = DSP has access to the mailbox
1 = host has access to the mailbox

a. RDYOIN is set by the DSP and reset by the host. That means that the DSP gives the mailbox to the host when it finishes using it and vice-versa. In no case can the host or the DSP take possession of the mailbox, it can only wait for the other to give it back.

b. The ST18930/31 sees RDYOIN as a flag :
   - tested by a branch instruction
   - set to 1 by an initialization instruction in order to give the availability of the mailbox to the host.

$\overline{IRQ}$.
Handshake signal enabling the host to gain access to the mailbox.

a. $\overline{IRQ}$ is asserted low by the DSP to indicate the availability of the mailbox (at the same time as RDYOIN).

b. The host after testing $\overline{IRQ}$, knows that it can access the mailbox. The access to the bus (which can be currently used by the DSP as a local address bus) must be requested by reading the address CS = 0, RS = 0.

c. The DSP then answers back by asserting $\overline{IRQ}$ high. (In pseudo-slave mode, the DSP is halted). The host now has full control of the bus and mailbox.

   When the host has completed the exchange it generates the address CS = 0, RS = 1 and the DSP resets RDYOIN.

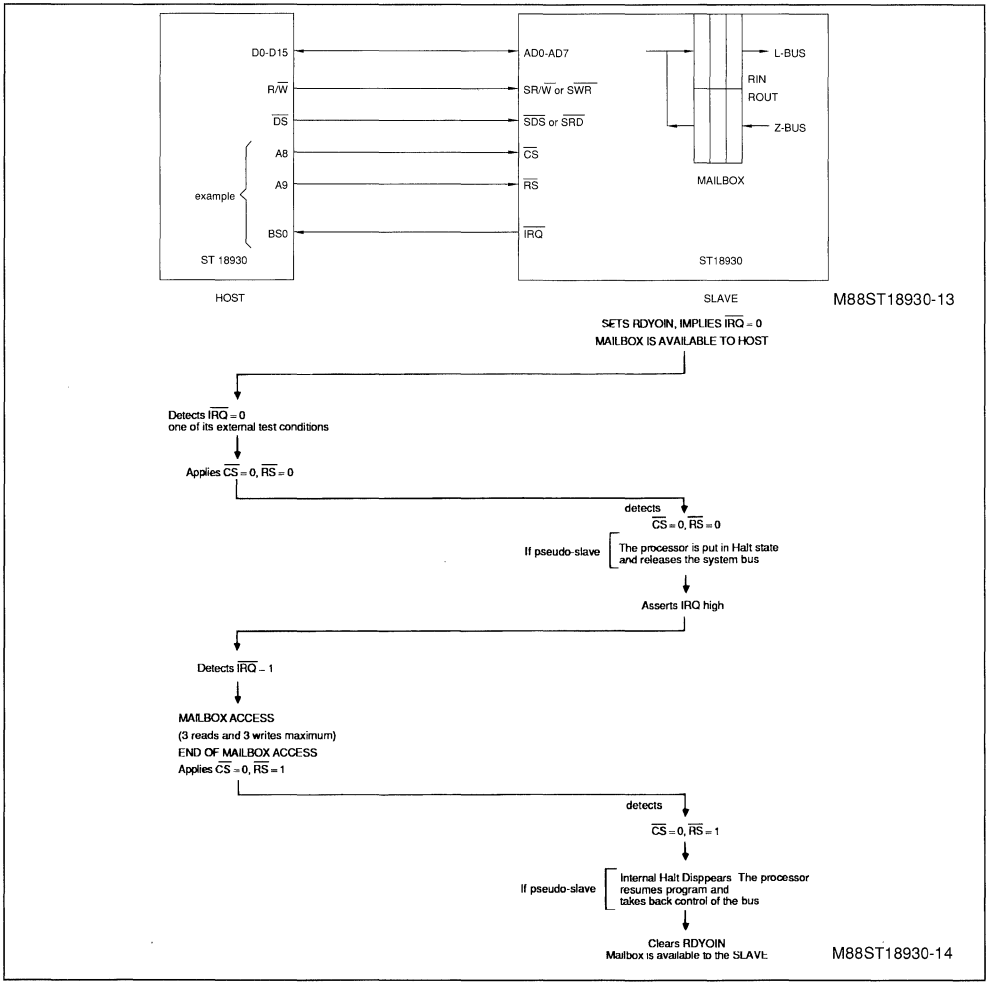
HALT (internal).
The internal halt has the following effect on the circuit :

- the program is stopped at the end of the current instruction, the program and loop counter are frozen
- a NOP is executed
- no more addresses are generated on the system bus

MAILBOX INTERRUPT.
Enabled by initializing the bit EIMB of Access Mode Register (AMR). When RDYOIN is reset, the PC is forced to address $ 0001.

Refer to figures 11.A and 11.B for timing detail of mailbox protocol.

Figure 10 : Mailbox Connection and Protocol.



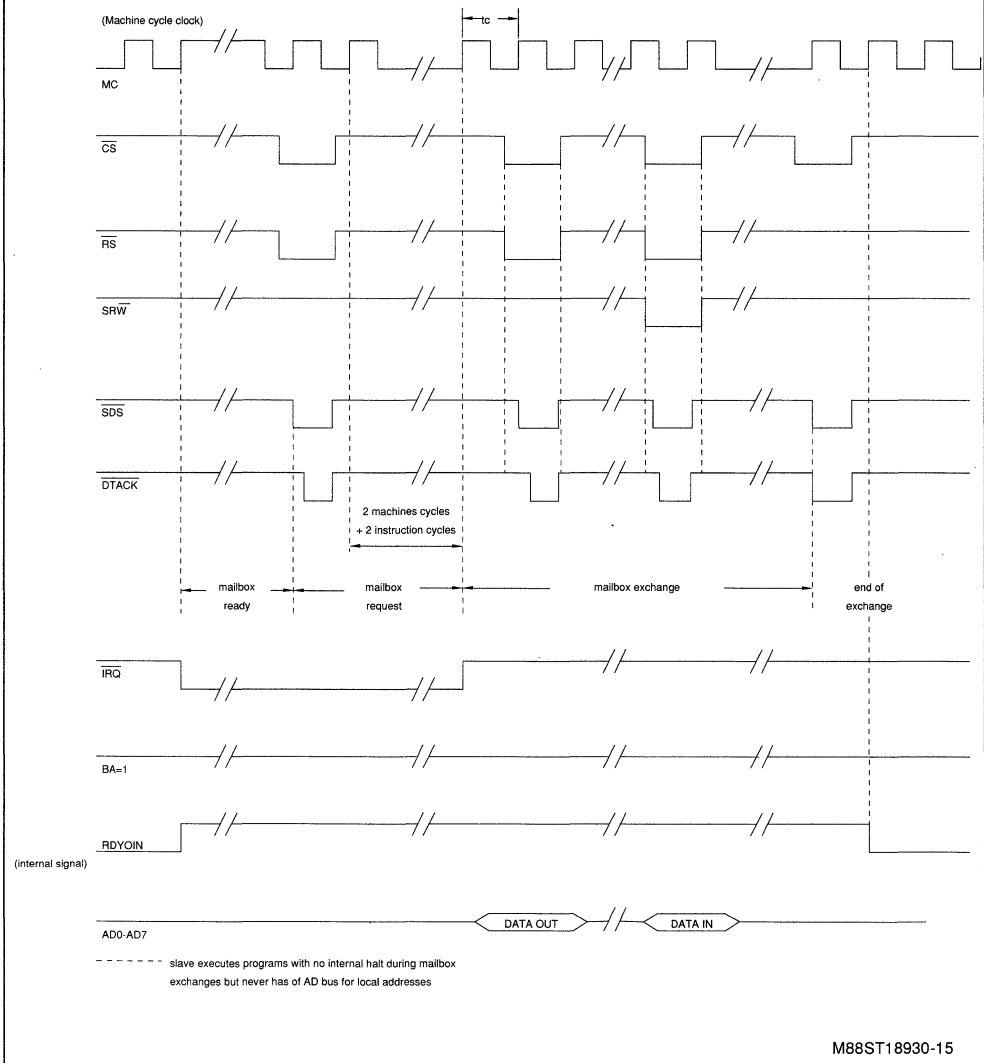
This protocol is hardwired on the slave side and programmed on the host side. The mailbox is included in the slave. The two slave address pins (CS, RS) are directly connected to two host address lines.

Therefore, the slave is seen as two external memory locations by the host which will address it by generating an external address directly or indirectly (pointer E0or E1).

By addressing the location 00 the host echoes the IRQ to the slave and accesses the mailbox.

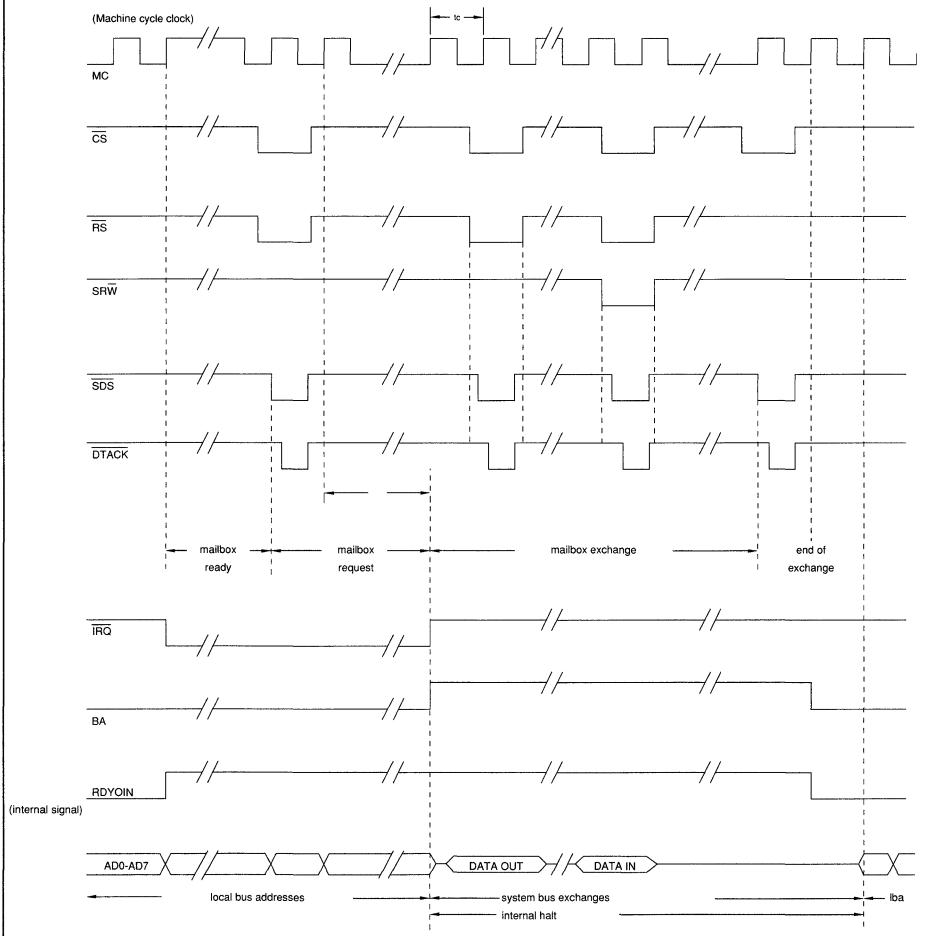
By addressing the location 01 the host releases the bus.

Figure 11.A : ST18930/31 Mailbox Exchange, Slave Mode.



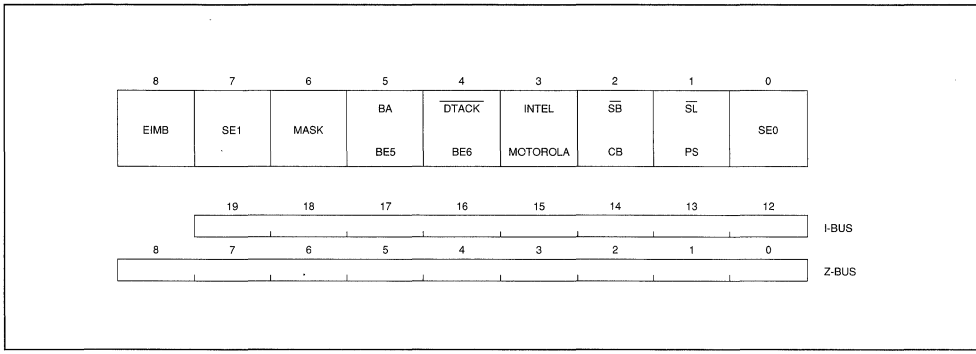
* Up to three consecutive read/write operations may take place.

Figure 11.B : ST18930/31 Mailbox Exchange, Pseudo Slave Mode.



3.5.7. Access Mode Register (AMR). The AMR is a 9-bit register which defines the processor external access modes.

It is loaded by an INI or SVR instruction and saved by an SVR instruction. Its fields are defined as follows :



Bits 0 and 7 - SE0, SE1.

These two bits define the number of cycles fixed by the user to access external resources. If the user defines a multicycle exchange (i.e. for access to slow memories), internal wait states are automatically inserted allowing the processor to wait for the completion of the external exchanges. The instruction executes once with the number of cycles chosen by the programmer.

Multicycles exchanges can be programmed in any operating mode (real, complex or double precision).

SE1	SE0	Number of machine cycles for external access
0	0	1
0	1	2
1	0	3
1	1	4

Bit 1 : $\overline{SL}$/PS.

0 = Slave.
1 = Pseudo-slave.

This bit defines the behaviour of the ST18930/31 regarding the system bus (AD0-AD7). In slave mode, the processor will never use the system bus as local bus address.

In pseudo-slave, the processor uses address bus (AD0-AD7) for local resources. These bits are concatenated with A8-A11 to form a 12-bit address bus.

Bit 2 : $\overline{SB}$/CB.

0 = Separated bus.
1 = Concatenated bus.
This bit indicates whether the local bus is used as a 16-bit concatenated bus or as 2 independent 8-bit buses.
(see 3.5.4. - local bus description).

Bit 3 : I ntel/Motorola type local bus

0 = Control pulses Read ($\overline{RD}$) and Write ($\overline{WR}$) are generated. This is the case with an Intel type peripheral or a standard byte-wide RAM.
1 = Control pulses data strobe ($\overline{DS}$) and Read/Write (R/$\overline{W}$) are generated.

This is the case for exchanges with a slave processor, a Motorola type peripheral, a data converter such as the TS7542 or the M.A.F.E. chip set (TS68950/51/52).

Bit 4 : $\overline{DTACK}$/BE6.

0 = DTACK function. The ST18930/31 does acknowledge correct access by generation of a DTACK output.
1 = BE6. An external test condition is available on pin BE6.

Bit 5 : BA/BE5.

0 = Configurates the pin (BA)5 as bus available output indicating the availability of the system bus.
1 = Pin BE5 is used for external test conditions.

Bit 6 : MASK (ST18931 only).

0 = An external Halt applied to the processor will not change the values in the AMR register.

1 = During external Halt applied to the processor the AMR register is forced to following configuration : one cycle exchange, pseudo-slave, concatenated bus, $\overline{RD}$ and $\overline{WR}$ control pulses.

This bit can be modified by the programmer even while the $\overline{HALT}$ is asserted.

Bit 8 : EIMB.

Enables interrupt mailbox. When set to 1, this bit validates the start of an interrupt when RDYOIN internal flag goes low.

This bit is programmed with an INI instruction.

3.5.8. Instruction interface and system control (ST18931 only). On the ST18931, the coefficient ROM and the instruction ROM (CROM & IROM) are external. The device provides the necessary buses to access these data. Instructions are read on ID0 : ID31 using IA0-IA15 for addressing. Coefficients are read on local address bus D0-D15 using CA0-CA8 for addressing. CA9 is at low level for address validation. CA0-CA7 also contains external RAM addresses (if necessary) associated with a high level for CA9.

So, for the ST18931, there is no need of a pseudo slave mode as AD0-AD7 remain available for data transfer on the system bus. Clock signals are also provided for interfacing purposes (3.6.1.). Controls signals on CSDL and CSDH indicates data transfers on D0-D7 and D8-D15 respectively when at a low level. A NOP control input is also provided on ST18931 to allow hardware simplification of development systems. This input forces a NOP instruction when low and forces all addresses in high impedance state.

3.5.9. Halt (ST18931 only). The external $\overline{\text{HALT}}$ signal will freeze the program counter, the loop counter and the multiplier. The instruction register can then be loaded from an external source. This signal is used for system development.

3.6. OTHER RESOURCES

3.6.1. Clock generators. Three different clock outputs are available on the ST18931 and one on the ST18930.

CLKOUT : available on ST18930 and ST18931.

INCYCLE and MC (master clock) : available on ST18931 only.

The internal processor cycle is equal to the frequency of the EXTAL input divided by 2 or 4. The choice of the dividing factor is done by option at the masking level for the ST18930 and by control of CC input on the ST18931. If CC = 1 then the dividing factor is 2, if CC = 0 it becomes 4 for TS68930/31 compatibility.

The CLKOUT output period is function of the EXTAL period and the value of CRR register programmed by INI instruction.

CRR (3; 0)	**CLKOUT/EXTAL RATIO**
1	2
2	3
....	....
15	16

The INCYCLE output is equal to instruction cycle. The MC output period is equal to half of EXTAL period.

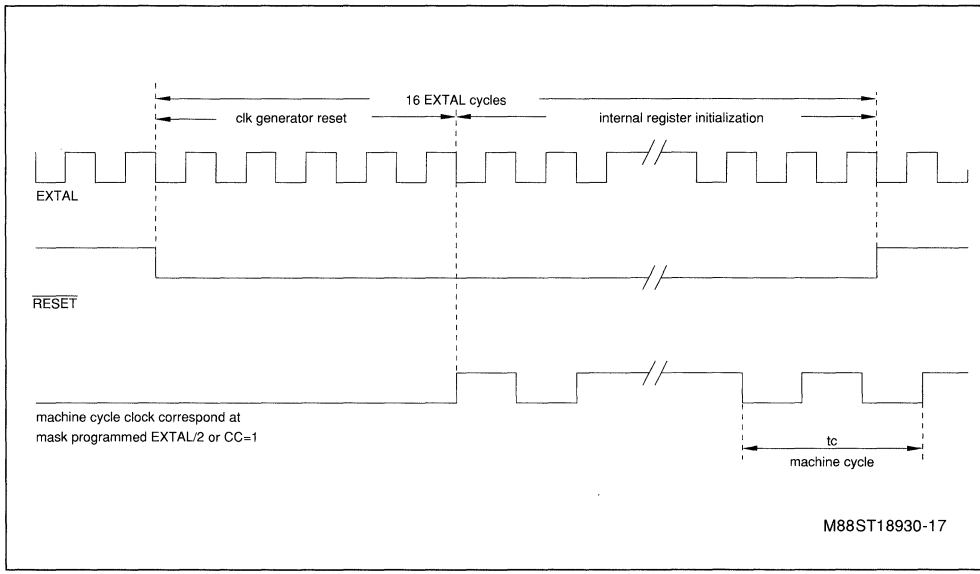
3.6.2. Reset. The reset signal acts on several processors blocks as follows :

- Sequencer : the program counter (PC) and the loop counter (LC) are cleared to zero. The instruction register is loaded with NOP instruction.
- Status register : set in real mode, no saturation, empty FIFO (EF = 1), overflows (MOVF = AOVF = OVFM = 0), interrupt disabled (EI = 0), and XRAM and YRAM in non circular addressing mode.
- Access Mode Register (AMR) : set for one cycle external exchange, slave mode, concatenated bus, $\overline{\text{RD}}$ and $\overline{\text{WR}}$, BE5 and BE6.
- Motorola mode is set on system bus.
- Mailbox control is disabled.

The reset signal must be maintained for a minimum of 16 cycles of EXTAL signal (see fig. 12 for timing). If machine cycle = EXTAL ÷ 2.

3.6.3. Watchdog capability (ST18930 only). The watchdog prevents the processor from staying locked in an undesired state or internal loop caused by adverse conditions. The circuitry does include a 2-bit counter which is incremented by each falling edge on BE3 input and reset by software testing of the BE3 condition. If three falling edges of BE3 input occurs without a test of the condition, the ST18930 is reset by the watchdog circuit. This capability is a mask option of the ST18930.

Figure 12 : Reset Timing.



3.6.4. Low power mode. The low power mode freezes the circuit operation and divide by 16 the internal clock generator frequency (see masking options).

In this mode, the DSP will use typically less than 5 mA.

The access to this mode can be done by software or hardware.

- Hardware mode :

On the ST18931 and the ST18930 in PLCC 52 package the LP pin forces the low power mode.

For the ST18930 in 48 pin package, the BS2 pin can be configurated by a mask option as a low power mode input pin. In this case, if the bit EI of the status register is set to 1, BS2 pin will work as low power control pin, and

If EI = 0, BS2 will work as a branch condition pin.

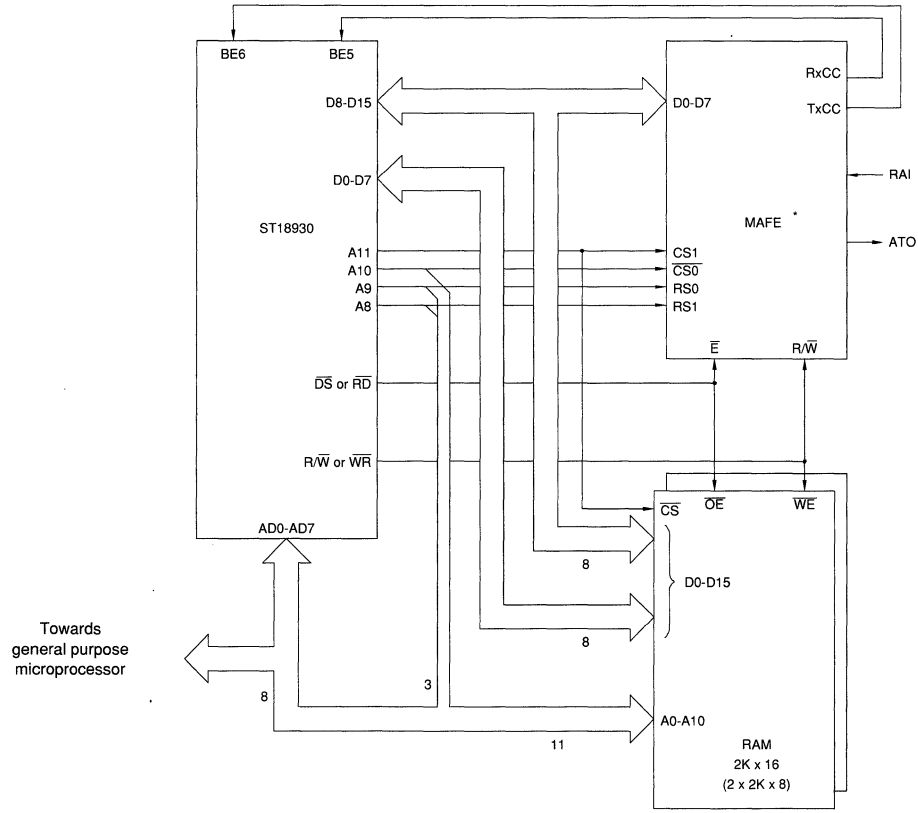
- Software mode :

The low power mode is activated by an INI instruction.

The return from low power mode is obtained with a reset or an interrupt.

4. TYPICAL APPLICATION CONFIGURATIONS

Figure 13 : Configuration Example with ST18930 + RAM + MAFE*.

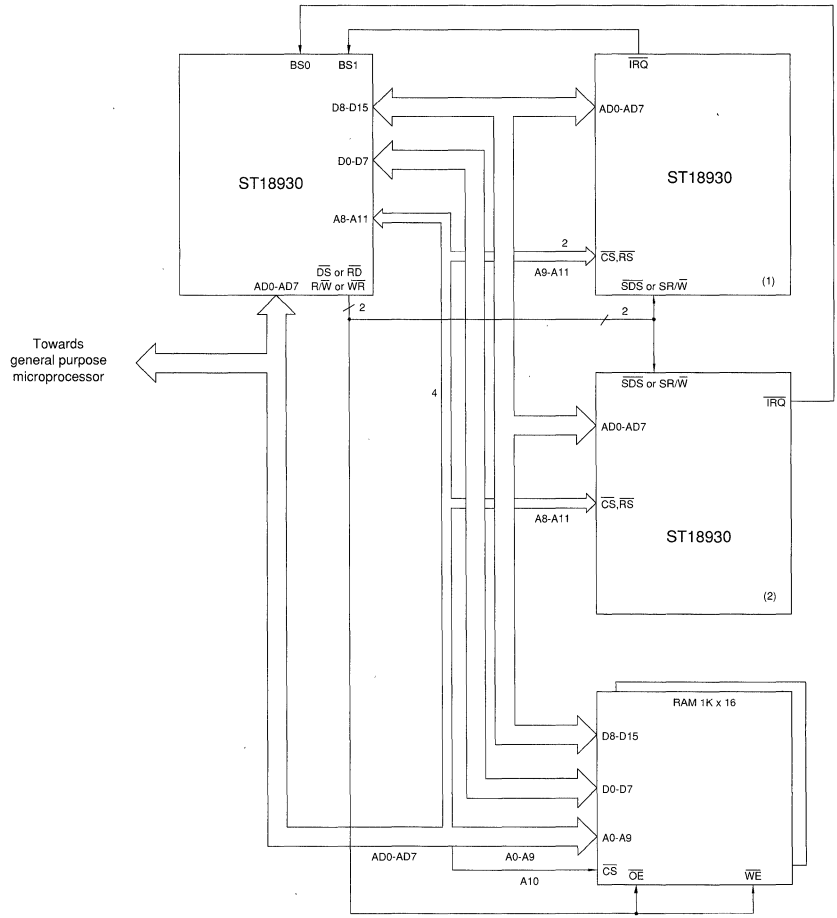


A_{11}	A_{10}	A_9	A_8	
1	0	X	X	**MAFE**
0	X	X	X	**RAM**

* MAFE is the TS68950/51/52 Modem Analog Front – End Chip Set.

M88ST18930-18

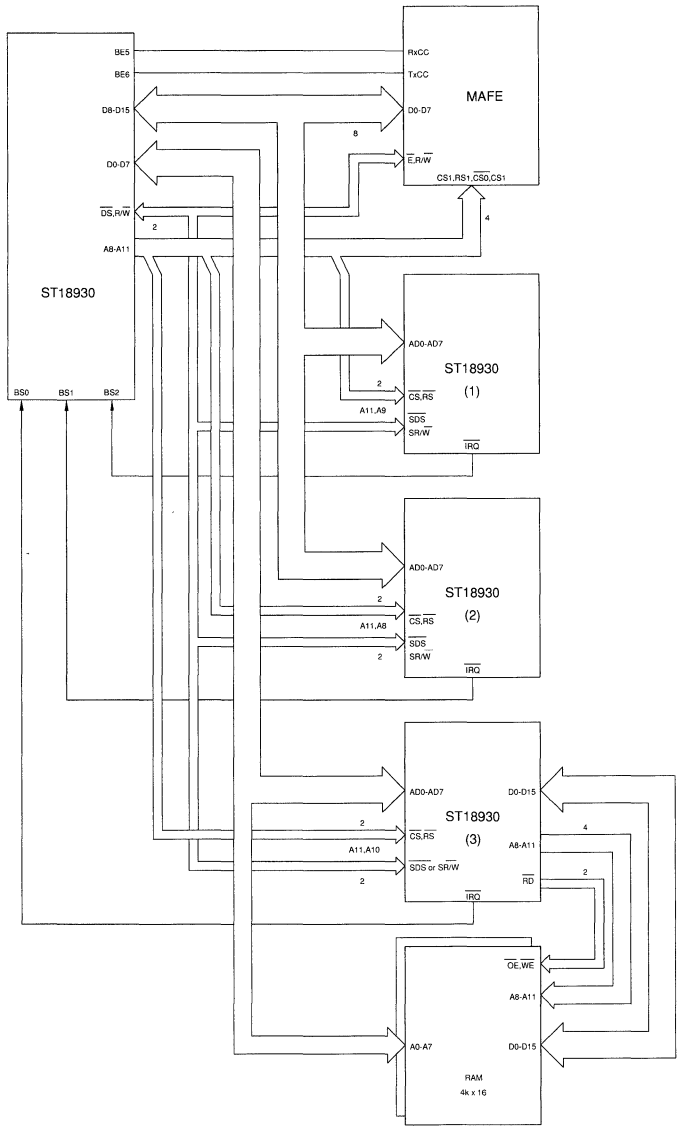
Figure 14 : Configuration Example : 3 ST18930 + RAM.



A_{11}	A_{10}	A_9	A_8	
0	1	0/1	1	**ST18930** (1)
0	1	1	0/1	**ST18930** (2)
1	0	X	X	**RAM**

M88ST18930-19

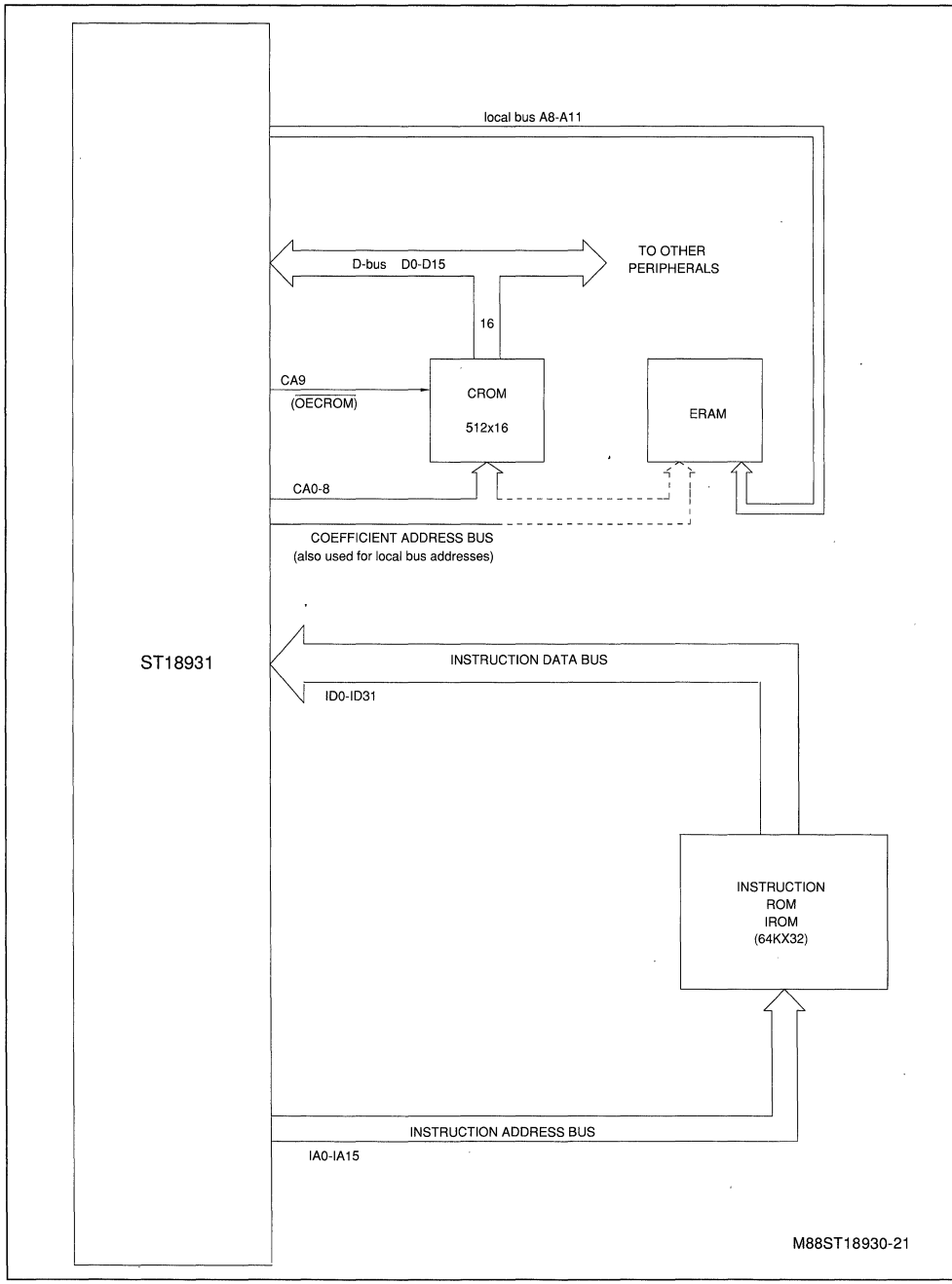
Figure 15 : Configuration Example 4 ST18930 + MAFE + RAM.



A_{11}	A_{10}	A_9	A_8	
1	0	X	X	**MAFE**
0	1	0/1	1	**ST18930** (1)
0	1	1	0/1	**ST18930** (2)
0	0/1	1	1	**ST18930** (3)

M88ST18930-20

Figure 16 : Interfacing CROM, IROM to ST18931.



5. INSTRUCTION SET

Symbol	Type	Operation	Number of Cycles	
			REAL	CPLX DBPR
OPIN	Calculation Instruction with Indirect Addressing	This instruction refers to operands indirectly addressed.	1	2
OPDI	Calculation Instruction with Direct Addressing	The operand sourcing the L-BUS is directly addressed.	1	2
OPIM	Calculation Instruction with Immediate Operand	An immediate operand is read on R-BUS.	1	2
ASR ASL LSR ROR	General Shift Instruction	The operand sourcing the L-BUS can be shifted/rotated by 0 $\rightarrow$ 15 bits.	1	2
BRI	Immediat Branch Instruction	Conditional/unconditionnal branch to direct address.	2	2
BRC	Computed Branch Instruction	Conditional/unconditional branch to computed address.	2	2
SVR TFR	Data Transfer Instruction	This instruction is used to save register contents in external or internal RAM.	1	2
INI	Initialization and Control Instruction	Pointers, acces mode register, loop counter, mode initialization, interrupts.	1	2

INSTRUCTION SET LANGUAGE DEFINITIONS

LDT	Load L-BUS source into Transfer Register T
R SRC	R-BUS Source
L SRC	L-BUS Source
SL	ALU Input Selection Left Side
SR	ALU Input Selection Right Side
ALU DST	ALU Output Destination
ALU CODE	ALU Codes
LDM	Load L-BUS Source into Multiplier Input M
LDN	Load R-BUS Source into Multiplier Input N
Z SRC	Z-BUS SOURCE
Z DST	Z-BUS DESTINATION
ZT	Load Z-BUS into Transfer Register T
ACE	Post Incrementation Pointers CROM or ERAM
AY	Post Incrementation Pointers YRAM
AX	Post Incrementation Pointers XRAM
BRA	Branch Address Source
FT	False/True Condition
SVPC	Save Program Counter
JDST	Destination Register for J Constant
KDST	Destination Register for K Constant
MODE	Operating Mode
SAT	Saturation Flag
ADOF	Even/odd Flag
J Constant	8-bit Constant used to initialize registers
K Constant	12-bit constant used to initialize registers

5.1 OPERATING CODE FORMATS

Fig. 17 : OPIN : Calculation Instruction with Indirect Addressing.

Bit	Field	Operations and Codes
31 30	OP CODE	00
29	LDT	0-NO LOAD, 1-LBUS → T
28 27	R SRC	00 01 10 11 [X0] [E0] [Y0] [Y1]
26 25 24	L SRC	000 001 010 011 100 101 110 111 [X0] [X1] [Y0] RIN T [E1] [C0] [C1]
23	SL	0-LBUS / 1-P
22	SR	0-RBUS / 1-A/B (refer to ALU DST)
21 20 19 18 17	ALU CODE	cf. Special Table
16 15	ALU DST	00 01 10 11 D F A B
14 13 12	Z SRC	000 001 010 011 100 101 110 111 D F A B T CCR – –
11	LDM	0-NO LOAD / 1-LBUS → M
10	LDN	0-NO LOAD / 1-RBUS → N
9 8	ACE	00 01 10 11 + 0 + 1 – – 1
7 6	AY	00 01 10 11 + 0 + 1 – – 1
5 4	AX	00 01 10 11 + 0 + 1 – – 1
3 2 1	Z DST	000 001 010 011 100 101 110 111 NONE ROUT [Y0] [Y1] [E0] [E1] [X0] [X1]
0	ZT	0-NO LOAD / 1 ZBUS → T

Fig. 18 : OPDI : Calculation Instruction with Direct Addressing.

Bit	Field	Operations and Codes
31 30 29	OP CODE	010
28 27	R SRC	00 01 10 11 [X0] [E0] [Y0] [Y1]
26 25 24	L SRC	000 001 010 011 100 101 110 111 X – Y RIN T E – C
23	Z SRC	0-D / 1-F
22	SR	0-RBUS / 1-A
21 20 19 18 17	ALU CODE	cf. Special Table
16	ALU DST	0-F / 1-A
15 14 13 12 11 10 9 8 7 6 5 4	LBUS DIRECT ADDRESS	MSB LSB
3 2 1 0	Z DST	0000 0010 0100 0110 1000 1010 1100 1110 NONE ROUT [Y0] [Y1] [E0] [E1] [X0] LCR 0001 0011 0101 0111 1001 1011 1101 1111 X0 X1 Y0 Y1 E0 E1 C0 C1

Fig. 19 : OPIM : Calculation Instruction with Immediate Operand.

Bit	Field	Operations and Codes
31 30 29 28 27	OP CODE	01110
26 25 24	L SRC	000 001 010 011 100 101 110 111 [X0] [X1] [Y0] RIN T [E1] [C0] [C1]
23	SL	0-LBUS / 1-P
22	SR	0-RBUS / 1-A
21 20 19 18 17	ALU CODE	cf. Special Table
16	ALU DST	0-F / 1-A
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	IMMEDIATE VALUE (R-BUS)	MSB LSB

Fig. 20 : ASR, LSL, LSR, ROR, Shift Instructions.

Bit	Field	Operations and Codes	
31 30 29 28 27	OP CODE	01111	
26 25 24	L SRC	000 001 010 011 100 101 110 111 X – Y RIN T E – C	
23	SL	0-LBUS / 1-P	
22 21	ALU CODE	00 01 10 11 ASR LSL LSR ROR	**NOTE** : When LSR, ASR, ROR shift value is complemented to 2.
20 19 18 17	SHIFT VALUE	0000 0001 ..... 1111 0 1 15	
16	ALU DST	0-F / 1-A	
15 14 13 12 11 10 9 8 7 6 5 4	LBUS DIRECT ADDRESS	MSB LSB	
3 2 1 0			

Fig. 21 : BRI : Branch Immediate Instruction.

Bit	Field	Operations and Codes
31 30 29	OP CODE	100
28	BRA	0-IR, 1-RAS
27	FT	0-FALSE, 1-TRUE
26 25 24 23	COND	CF Special Table
22	SVPC	0-NO SVPC, 1-PC → RAS*
21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6	BRANCH ADDRESS	MSB LSB
5 4	AX	00 01 10 11 + 0 + 1 − − 1
3 2 1	Z DST	000 001 010 011 100 101 110 111 NONE − [Y0] [Y1] − − [X0] [X1]
0	ZT	0 NO LOAD, 1-ZBUS → T

* The PC write operation in X or Y RAM (defined by Z DST) is realized if the branching is really executed.

Fig. 22 : BRC : Branch Computed Instruction.

Bit	Field	Operations and Codes
31 30 29 28	OP CODE	1010
27	FT	0-FALSE, 1-TRUE
26 25 24 23	COND	CF Special Table
22	SVPC	0-NO SVPC, 1-PC → RAS*
21 20		
19	RTI	0-NO RTI, 1-RAS → PC
18 17 16		
15 14 13 12	BRANCH SOURCE	000 001 010 011 100 101 110 111 NONE F A B T – – –
11 10 9 8 7 6		
5 4	AX	00 01 10 11 + 0 + 1 – – 1
3 2 1	Z DST	000 0001 010 011 100 101 110 111 NONE – [Y0] [Y1] – – [X0] [X1]
0	ZT	0-NO LOAD, 1-ZBUS → T

* See BRI.

Fig. 23 : SVR : Data Transfer Instruction.

Bit	Field	Operations and Codes
31 30 29 28 27 26	OP CODE	011000
25 24 23 22	Z SRC	0000 0001 0010 0011 0100 0101 0110 0111 X0 X1 Y0 Y1 E0 E1 C0 C1 1000 1001 1010 1011 1100 1101 1110 1111 AMR LC A F D STA B –
21 20 19 18 17 16		
15 14 13 12 11 10 9 8 7 6 5 4	ZBUS DIRECT ADDRESS	MSB LSB
3 2 1	Z DST	000 001 010 011 100 101 110 111 NONE ROUT Y AMR E STR X –
0	ZT	0-NO LOAD, 1-ZBUS → T

Fig. 24 : INI : Initialization and Control Instruction.

Bit	Field	Operations and Codes
31 30	OP CODE	11
29 28 27	J DST	000 001 010 011 100 101 110 111 AMR LCD Y0(3) Y1(3) CRR EN(1) EF NONE(2)
26 25 24	K DST	000 001 010 011 100 101 110 111 X0 X1 LCI-LCR NONE E0 E1 C0 C1
23 22	MODE	00 01 10 11 – REAL DBPR CPLX
21	SAT	0 NO SATURATION MODE 1 SATURATION MODE
20	AD0F	0 NO INVERSION 1 INVERSION LSB ADDRESS X/Y RAM
19 18 17 16 15 14 13 12	J7 J CONSTANT J0	If JDEST = EN see table below.
11 10 9 8 7 6 5 4 3 2 1 0	K11 K CONSTANT K0	If KDEST = X0 or KDEST = X1 and K7 = 0 then XRAM Normal Mode K7 = 1 then XRAM Circular Addressing Mode

* EN (Enable) code (101) is a multi–function condition permitting independant programming of RDYOIN and SIM flags, and STA register bit EI in J field of the INI instruction.

Notes :

1) If JDST = EN and :

J7	J6		J5	J4		J2	J1		J0	
0	X	EIMB = no change	0	X	: EI = no change	0	X	: SIM = no change		
1	0	EIMB = 0	1	0	: EI = 0	1	0	: SIM = 0 system bus Intel	0	: RDYON = no change
1	1	EIMB = 1	1	1	: EI = 1	1	1	: SIM = 1 system bus Motorol	1	: RDYON = 1

2) If JDST = NONE and J7 = 1 then low Power mode.

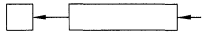
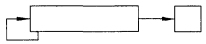
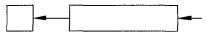
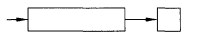
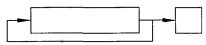
3) If JDST = Y0 or JDST = Y1 and

J7

0 : Y RAM normal mode

1 : Y RAM circular addressing mode.

5.2 ALU CODES

MNEMO	Function	SR	SI	CR	CI	Z	OV F	MO VF	AO VF	Code (I17-I21)
ADD	A + B	*	*	*	*	*	*	*	*	00010
ADDC	A + B + CARRY	*	*	*	*	*	*	*	*	00011
ADDS	B + A/16	*	*	*	*	*	*	*	*	00001
ADDX	B + A* (COMPLEX CONJUGATE)	*	*	*	*	*	*	*	*	01010
AND	A • B	*	*	0	0	*	0		*	01110
ASL	CARRY  0	*	*	*	*	*	*		*	01011
ASR	 CARRY	*	*	*	*	*	0		*	01111
CLR	CLEAR	0	0	0	0	1	0		0	10011
COM	COMPLEMENT A	*	*	0	0	*	0		*	10110
COM	COMPLEMENT B	*	*	0	0	*	0		*	11000
LCCR	LBUS –> CCR	*	*	*	*	*	*	*	*	01001
LSL	CARRY  0	*	*	*	*	*	0		*	11011
LSLB	LSL BYTE	*	*	*	*	*	0		*	11001
LSR	0  CARRY	*	*	*	*	*	0		*	00111
LSRB	LSR BYTE	*	*	*	*	*	0		*	11010
NOP										00000
OR	A ∧ B	*	*	0	0	*	0		*	01101
RCE	EXECUTE RC	*	*	*	*	*	*	*	*	10001
RCER	EXECUTE RC / LOAD NEW CODE	*	*	*	*	*	*	*	*	10000
RCR	LOAD RC									10010
ROR	 CARRY	*	*	*	*	*	0		*	10111
SBC	A + $\overline{B}$ + CARRY	*	*	*	*	*	*	*	*	00101
SBCR	$\overline{A}$ + B + CARRY	*	*	*	*	*	*	*	*	01000
SET		1	1	0	0	0	0		0	11100
SUB	A + $\overline{B}$ + 1	*	*	*	*	*	*	*	*	00100
SUBR	$\overline{A}$ + B + 1	*	*	*	*	*	*	*	*	00110
TRA	TRANSFER A	*	*	0	0	*	0		*	10100
TRA	TRANSFER B	*	*	0	0	*	0		*	10101
XOR	A ⊕ B	*	*	0	0	*	0		*	01100
SUBS	B + A/16 + 1	*	*	*	*	*	*	*	*	11101

Notes : 1. A B refer to ALU inputs (respectively LSIDE, RSIDE) not to accumulators A/B.
2. In ASL the OVF bit is equivalent to exclusive OR of bit 14 and 15.

5. 3. TEST CONDITIONS

True Condition	False Condition	Code
BE3	No BE3	0100
BE4	No BE4	0010
BE5	No BE5	0011
BE6	No BE6	0001
Branch Always	Branch Never	0000
BS0	No BS0	1100
BS1	No BS1	1101
BS2	No BS2	1110
CI	No CI	1010
CR	No CR	0110
MOVF	No MOVF	1011
OVF	No OVF	0111
RDYOIN	No RDYOIN	1111
SI	No SI	1001
SR	No SR	0101
Z	No Z	1000

5.4. AMR AND STA REGISTERS

AMR (Access Mode Register)

8	7	6	5	4	3	2	1	0
EIMB	SE1	MASK	BA BE5	$\overline{\text{DTACK}}$ BE6	T M	$\overline{\text{SB}}$ CB	$\overline{\text{SL}}$ PS	SE0

STA (Status Register)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SR	SI	CR	CI	Z	OVF	MOVF	AOVF	OVFM	EF	SAT	MODE		XC	YC	EI
CCR									STR						

CONDITION CODE REGISTER (CCR)

Name	Function	Description
SR	Sign Real	Set if the MSB of the ALU result is 1. Cleared otherwise.
SI	Sign Imaginary	Set if the MSB of the ALU imaginary result is 1 (in complex mode). Cleared otherwise.
CR	Carry Real	Set if a carry is generated out of the MSB of the result for arithmetic and shift operations. Cleared otherwise.
CI	Carry Imaginary	Set if a carry is generated out of the MSB of the imaginary part of the result for complex arithmetic and shift operations. Cleared otherwise.
Z	Zero	Set if the ALU result equals zero. In complex mode it is set if both real and imaginary parts are equal to zero.
OVF	Overflow	Set if there was an arithmetic overflow. This implies that the result cannot be represented in the operand size. In complex mode it is set for an overflow of either real or imaginary part. Cleared otherwise.
MOVF	Memorized Overflow	Set in the same conditions as overflow. Is cleared only when tested by a branch instruction.
AOVF	Advanced Overflow	Exclusive OR of bit 14 and 15 of the ALU. If there was an arithmetic overflow on half capacity (15 bits in real/complex mode, 31 bits in double precision mode). Is memorized and cleared by LCCR ALU instruction.
OVFM	Overflow Multiplier	Set if the multiplier has overflowed. Only meaningful for complex multiplication. Is memorized and cleared by LCCR ALU instruction.

STATE REGISTER (STR)

Name	Function	Description
EF	Empty FIFO	Set if FIFO is empty. Cleared otherwise.
SAT mode	Saturation Flag	Set if the ST18930 is programmed in saturation mode. In this configuration, the processor will behave as follows : Positive overflow : ALU result forced to 7FFF Negative overflow : ALU result forced to 8000 This feature does not apply to double precision mode. This bit is cleared otherwise.
MODE (2bits)	Operating Mode	Define a real (01), complex (11) or double precision (10) mode.
XC	XRAM Circular	Circular addressing mode flag for XRAM. (see 3.3.3)
YC	YRAM Circular	Circular addressing mode flag for YRAM. (see 3.3.3)
EI	Enable Interrupt	Enable interrupt flag (IT0, IT1, IT2).

6. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.3 to 7.0	V
V_{in}	Input Voltage	– 0.3 to 7.0	V
T_A	Operating Temperature Range	0 to 70*	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C
P_{Dmax}	Maximum Power Dissipation	0.8	W

Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability Standard MOS circuits handling procedure should be used to avoid possible damage to the device.
With respect to VSS.
* Other temperature ranges also available on request.

DC CHARACTERISTICS

V_{CC} = 5.0 V ± 10 %, V_{SS} = 0 V, T_A = 0 to + 70 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IL}	Input Low Voltage	– 0.3		0.8	V
V_{IH}	Input High Voltage (all inputs except EXTAL)	2.4		V_{CC}	V
V_{IHE}	Input High Voltage EXTAL	2.7		V_{CC}	V
I_{in}	Input Leakage Current (1) - (3)	– 10		+ 10	µA
I_{inEX}	Input Leakage Current on EXTAL (3)				
V_{OH}	Output High Voltage (I_{load} = – 300 µA, except $\overline{DTACK}$)	2.7			V
V_{OL}	Output Low Voltage (I_{load} = 2 mA)			0.5	V
P_D	Power Dissipation		0.35		W
P_{pd}	Power Dissipation Low Power Mode		10		mW
C_{in}	Input Capacitance		10		pF
I_{TSI}	Three State (off state) Input Current (2)	– 20		+ 20	µA

Notes : 1. ID0-ID31, $\overline{RESET}$, BE3, BE4, BE5 and $\overline{HALT}$, $\overline{NOP}$, CC (for ST18931).
2. D0-D15, AD0-AD7, BE5, BE6 and IA0-IA15, CAD-CAB (for ST18931).
3. Test conditions : V_{in} = 0.4 V and V_{in} = V_{DD}.

AC ELECTRICAL SPECIFICATIONS - CLOCK AND CONTROL PINS TIMING (ST18931 only)
(V_{CC} = 5.0 V ± 10 %, T_A = 0 to +70 °C, see figure 9.1.)
OUTPUT LOAD = 50 pF, DC Characteristics | load
REFERENCE LEVELS V_{IL} = 0.8 V V_{IH} = 2.4 V t_r, $t_f \leq 5$ ns for inputs signals
V_{OL} = 0.8 V V_{OH} = 2.4 V

N°	Symbol	Parameter	T_C = 80 ns		T_C = 100 ns		T_C = 160 ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	T_C	Machine Clock Cycle Time	80	320	100	400	160	640	ns
2	tcex2	External Clock Cycle Time (T_C = 2 x tcex)			50	200			ns
3	tcex4	External Clock Cycle Time (T_C = 4 x tcex)					40	160	ns
4	tcext	External Clock Fall and Rise Time		5		5		5	ns
5	tcexw	EXTAL High or Low	16	24	20	30	16	24	ns
6	trst	$\overline{RESET}$ to EXTAL Low Set-up and Hold Time	20		20		20		ns
7	trstd	$\overline{RESET}$ Width Low	8		8		8		T_C
8	tcod	EXTAL to CLKOUT Low and High Delay		25		25		25	ns
9	tcot	CLKOUT, MC, $\overline{DS}$, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$ Fall and Rise Time	2	5	2	5	2	5	ns
10	tdsl	CLKOUT, High to $\overline{DS}$, $\overline{RD}$, $\overline{WR}$ Low	– 3	3	– 3	3	– 5	5	ns
11	tdsh	CLKOUT, High to $\overline{DS}$, $\overline{RD}$, $\overline{WR}$ High	– 3	3	– 3	3	– 5	5	ns
12	tsc	Control Input Set-up Time (BS0-BS2, $\overline{IT0}$-$\overline{IT2}$, BE3-BE6)	20		20		20		ns
13	thc	Control Input Hold Time (BS0-BS2, BE3-BE6, $\overline{IT0}$-$\overline{IT2}$)	10		10		10		ns
14	tdlc	CLKOUT High to Control Output Low ($\overline{IRQ}$,BA)		25		25		25	ns
15	tdhc	CLKOUT High to Control Output High (BA)		25		25		25	ns
16		$\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Pulse Width	32		42		70		ns

Figure 25 : Clock and Control Pins Timing for Internal Machine Cycle Tc = 2 x External Clock Cycle Time (tcex) and frequency of CLKOUT equal EXTAL freq /2.

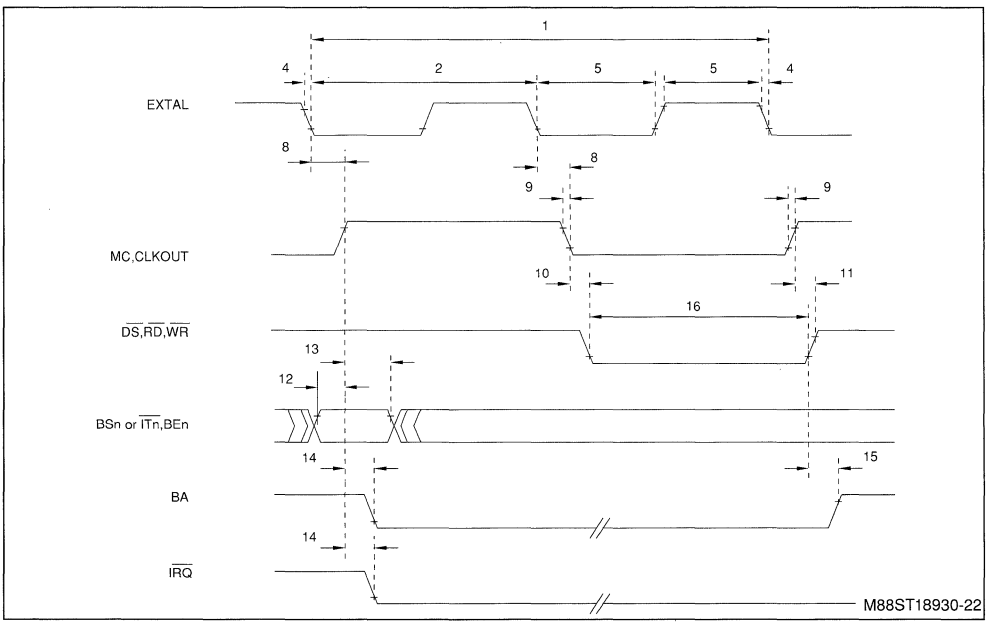


Figure 26 : Clock and Control Pins Timing for Internal Machine Cycle Tc = 4 · t_{cex4}.

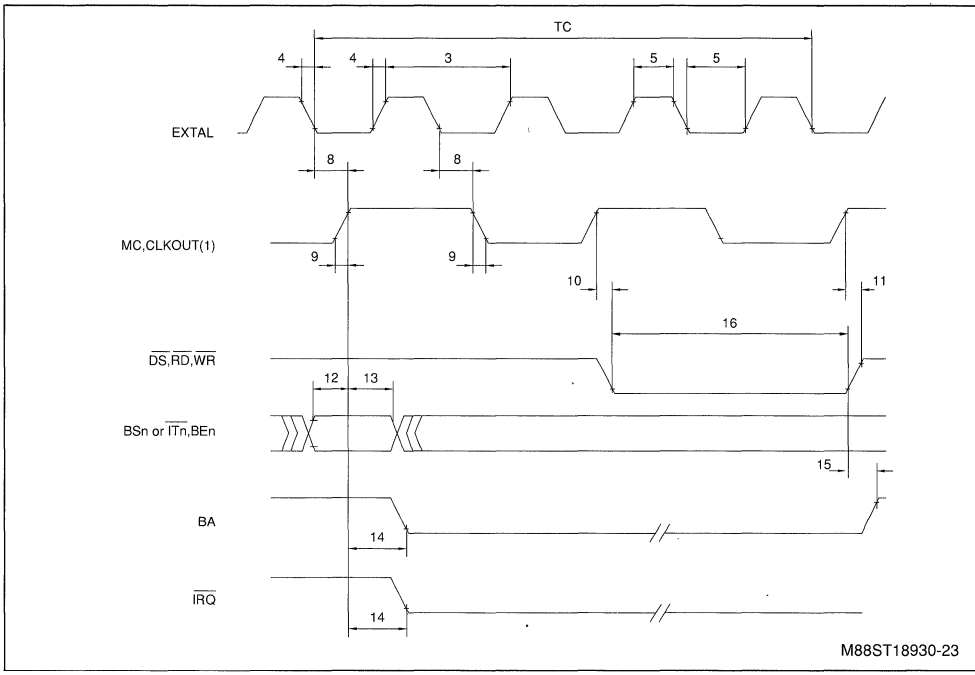
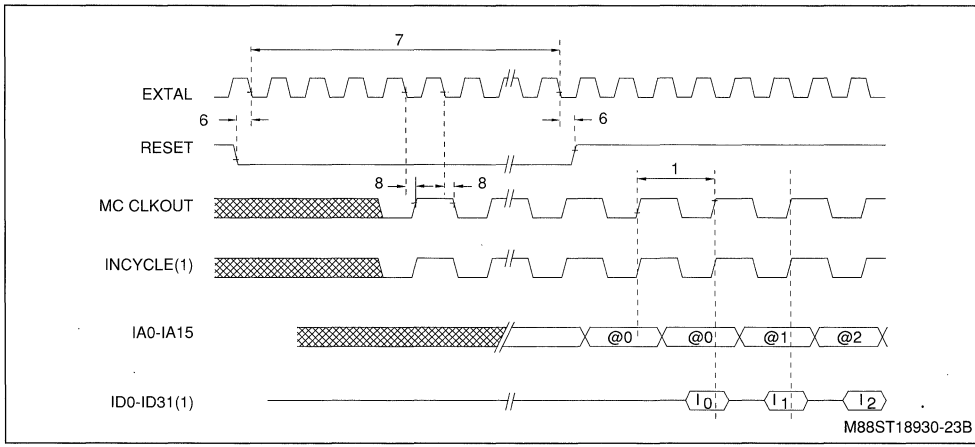


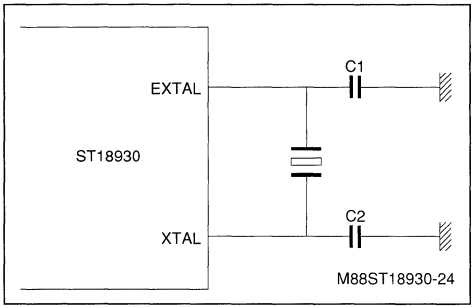
Figure 27 : Reset Timing for Internal Machine Cycle T_C = 2 · EXTAL.



Note : 1. INCYCLE and ID0-ID31 are ST18931 signals.

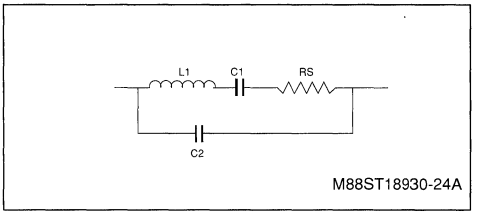
INTERNAL CLOCK OPTION

A crystal can be connected across XTAL and EXTAL functioning in the parallel resonant fundamental mode, AT–cut.



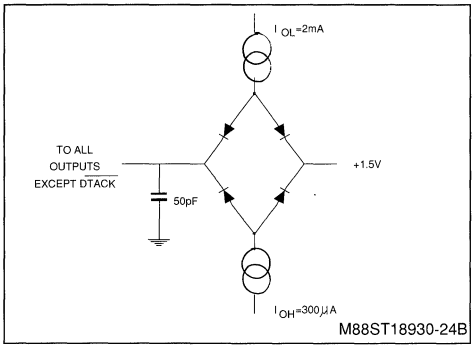
C1, C2 typical value = 10pF.

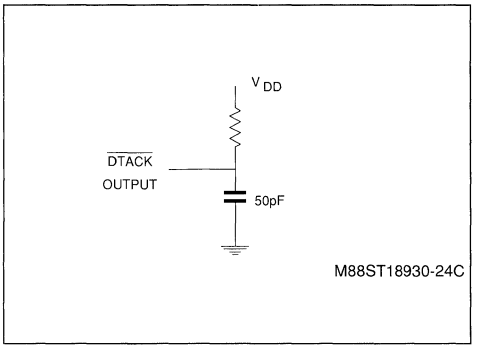
TYPICAL CRYSTAL EQUIVALENT CIRCUIT



Typical values : R_S = 10 Ω
C1 = 0.02 pF
C2 = 4 pF
Q> 30 K

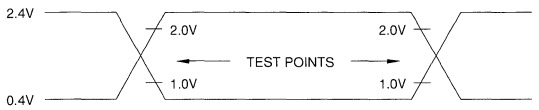
AC MEASUREMENT LOADS





AC TESTING INPUT, OUTPUT WAVEFORM

INPUT/OUTPUT



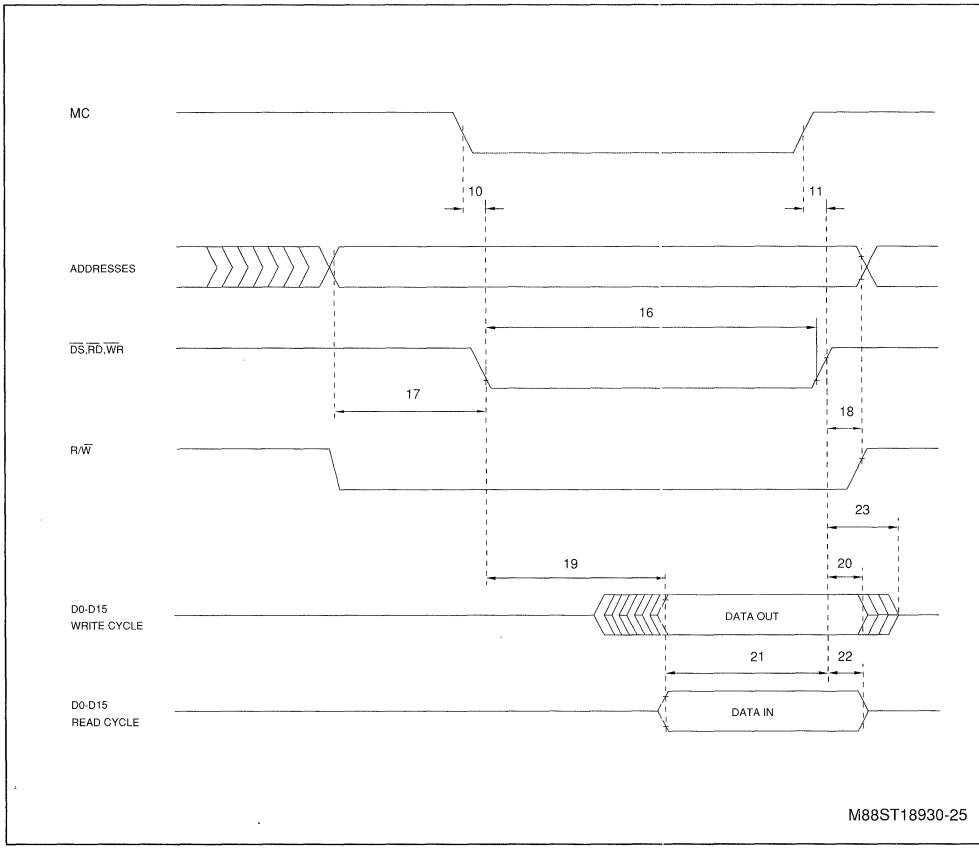
A.C. TESTING : Inputs are driven at 2.4V for a logic "1" and 0.4V for a logic "0" timing measurements are made at 2V for a logic "1" and at 1.0V for a logic "0".

AC ELECTRICAL SPECIFICATIONS - LOCAL BUS TIMING

(V_{CC} = 5.0 V ± 10 %, T_A = 0 to +70 °C)

N°	Symbol	Parameter	T_C = 80 ns		T_C = 100 ns		T_C = 160 ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
16	t_{PW}	$\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Pulse Width	32		42		70		ns
17	t_{ARW}	Address Valid to $\overline{WR}$, $\overline{DS}$, $\overline{RD}$ Low	20		30		55		ns
18	t_{AH}	Address and R/$\overline{W}$ Hold Time		5		5		5	ns
19	t_{DDW}	Data Delay Time, Write Cycle		25		25		30	ns
20	t_{DHW}	Data Hold Time, Write Cycle		5		5		5	ns
21	t_{DSR}	Data Set-up Time, Read Cycle	15		15		20		ns
22	t_{DHR}	Data Hold Time, Read Cycle				5		5	ns
23	t_{DDZ}	Data Valid to Z State		20		20		20	ns

Figure 28 : Local Bus Timing Diagram.



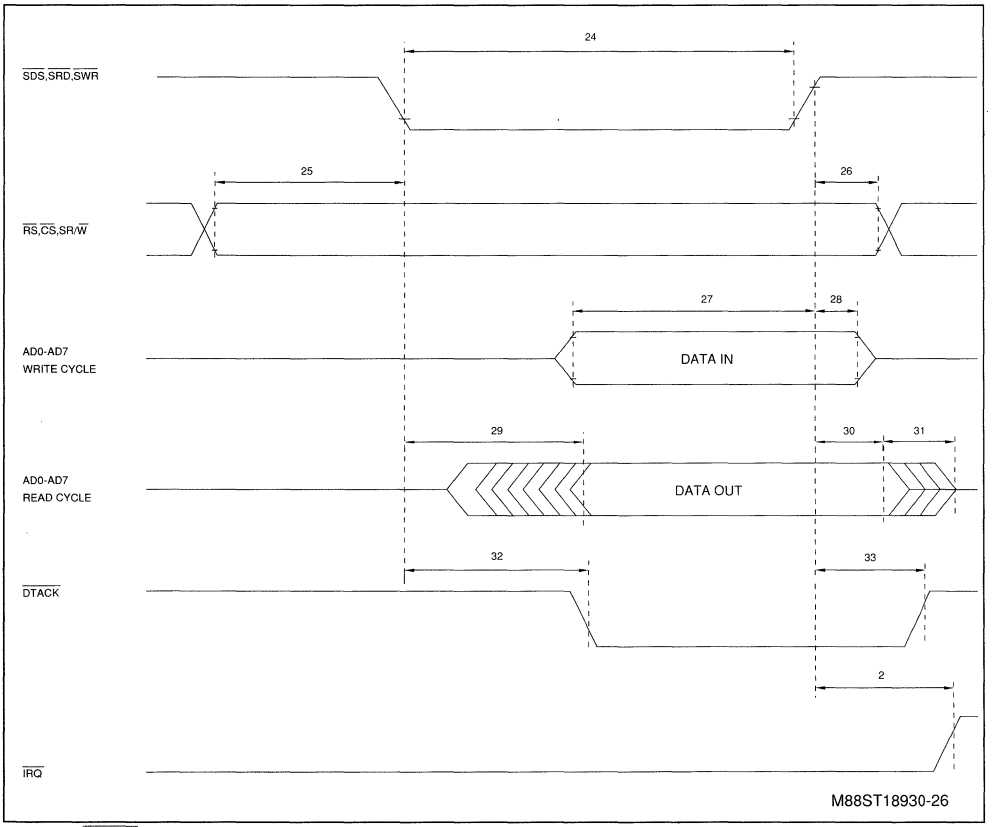
Note : In multicycle exchanges, t_{pw} duration is extended by 1, 2, or 3 machine cycle lengths.

AC ELECTRICAL SPECIFICATIONS - SYSTEM BUS TIMING

(V_{CC} = 5.0 V ± 10 %, T_A = 0 to +70 °C)

N°	Symbol	Parameter	T_C = 80 ns		T_C = 100 ns		T_C = 160 ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
24	t_{SPW}	$\overline{SDS}$, $\overline{SRD}$, $\overline{SWR}$ Pulse Width	30		40		60		ns
25	t_{SAW}	SR/$\overline{W}$, $\overline{CS}$, $\overline{RS}$ Set-up Time	15		15		15		ns
26	t_{SAH}	SR/$\overline{W}$, $\overline{CS}$, $\overline{RS}$ Hold after $\overline{SDS}$ High	5		5		5		ns
27	t_{SDSW}	Data Set-up Time, Write Cycle	15		15		15		ns
28	t_{SDHW}	Data Hold Time, Write Cycle		5		5		5	ns
29	t_{SDDR}	Data Delay Time, Read Cycle		25		30		30	ns
30	t_{SDHR}	Data Hold Time, Read Cycle	5		5		5		ns
31	t_{SDZR}	$\overline{SDS}$, $\overline{SRD}$ High to Z State		25		25		30	ns
32	t_{DSLDT}	$\overline{SDS}$ Low to $\overline{DTACK}$ Low		20		20		20	ns
33	t_{DSHDT}	$\overline{SDS}$ High to $\overline{DTACK}$ Desactivated (1)		20		20		20	ns

Figure 29 : System Bus Timing Diagram for Tranfer of 1 Byte.



Notes : 1. $\overline{DTACK}$ is an open drain output. Test load includes R_L = 820 Ω to V_{DD}.
2. This delay depends on programming mode. Its maximum value is 2 · T_C +2 instruction cycles (see user's manual).

AC ELECTRICAL SPECIFICATIONS - INSTRUCTION INTERFACE TIMING (ST18931 only)
(V_{CC} = 5.0 V ± 10 %, T_A = 0 to +70 °C)

N°	Symbol	Parameter	T_C = 80 ns		T_C = 100 ns		T_C = 160 ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
34	t_{INCH}	MC High to INCYCLE High Time	− 5	+ 5	− 5	+ 5	− 5	+ 5	ns
35	t_{INCL}	MC High or Low to INCYCLE Low Time	− 5	+ 5	− 5	+ 5	− 5	+ 5	ns
36	t_{IAD}	Instruction Address Delay Time		20		20		30	ns
37	t_{IAH}	Instruction Address Hold Time	5		5		5		ns
38	tIDS	Instruction Data Set-up Time	30		30		40		ns
39	t_{IDH}	Instruction Data Hold Time	5		5		5		ns
40	t_{CAD}	External CROM Address Delay Time		25		25		30	ns
41	t_{CAH}	External CROM Address Hold Time	5		5		5		ns
42	t_{CDS}	External CROM Data Set-up Time	15		15		20		ns
43	t_{CDH}	External CROM Data Hold Time	5		5		5		ns
44	t_{HS}	$\overline{\text{HALT}}$ Set-up Time	20		20		20		ns
45	t_{HH}	$\overline{\text{HALT}}$ Hold Time	10		10		10		ns
46	t_{CSD}	MC High to Data Bus		20		30		40	ns
47	t_{CSH}	MC High to Data Bus	5		5		5		ns

Figure 30 : ST18931 Timing Diagram for Internal Machine Cycle $T_C = 2 \cdot t_{cex2}$.

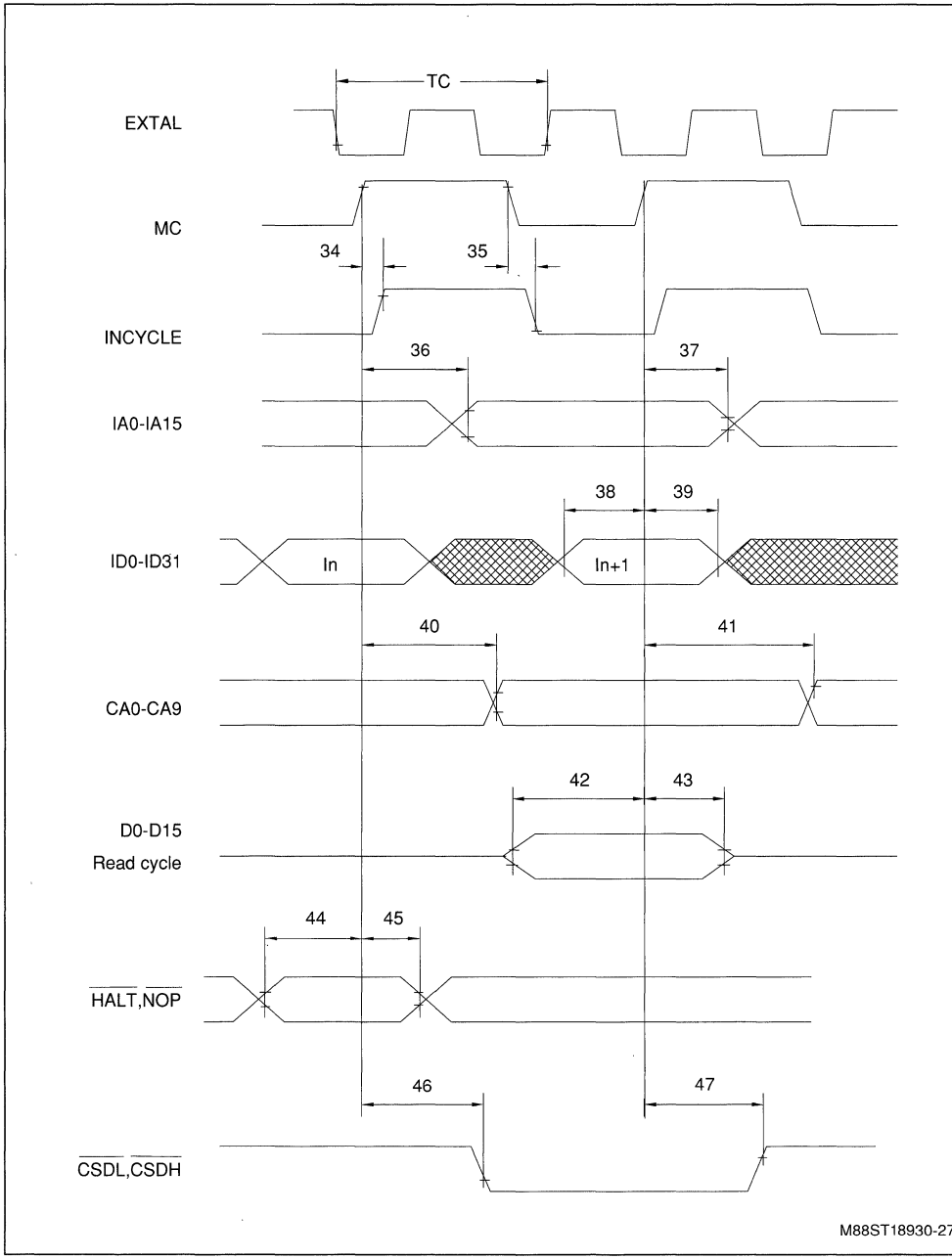


Figure 31 : ST18931 Timing Diagram for Internal Machine Cycle $T_C = 4 \cdot t_{cex4}$.

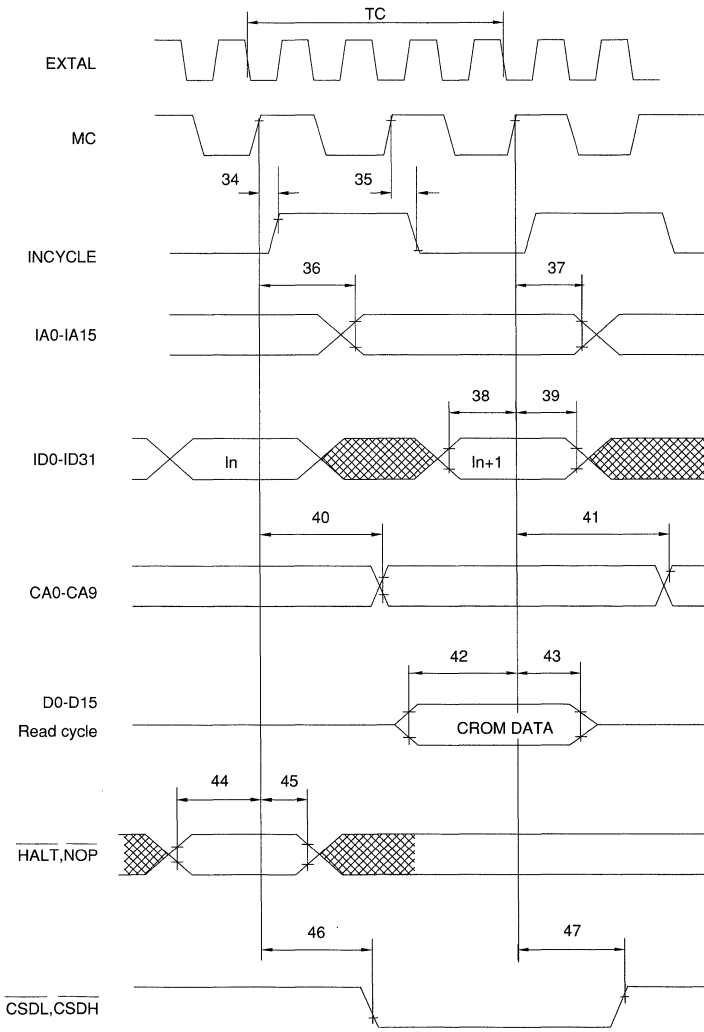


Figure 32 : CLKOUT Output Period Function of the CRR Register Value.

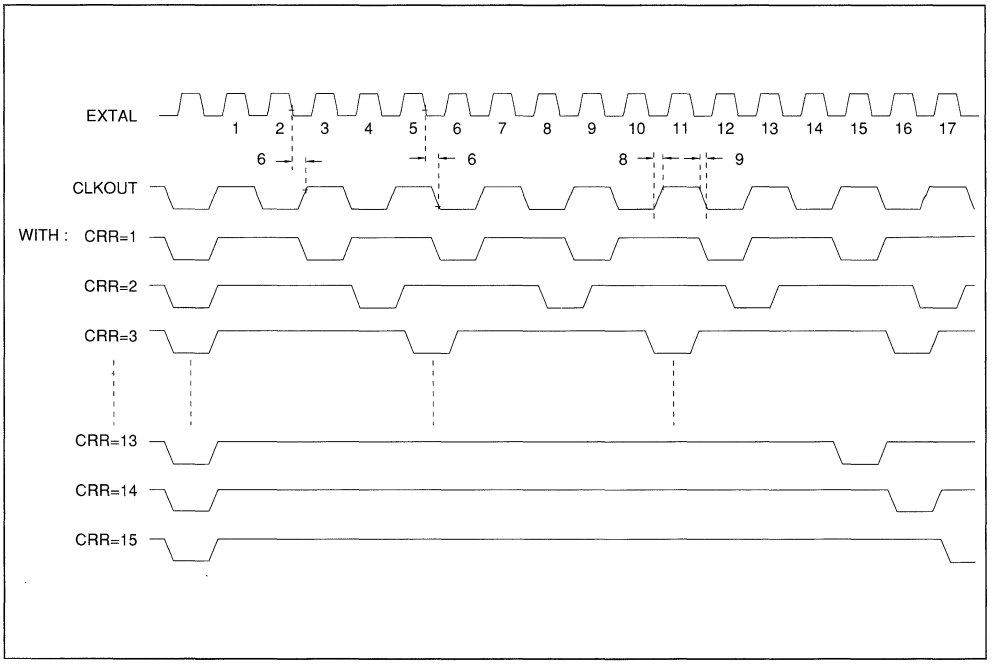


Figure 33 : Local Bus "Motorola" Write Cycle Timing Diagram.

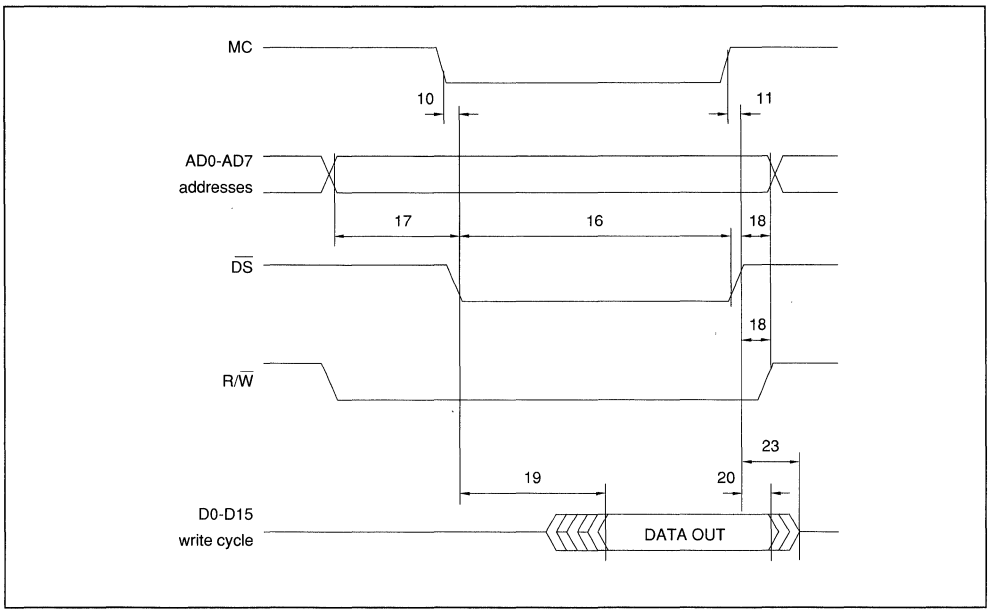


Figure 34 : Local Bus "Motorola" Read Cycle Timing Diagram.

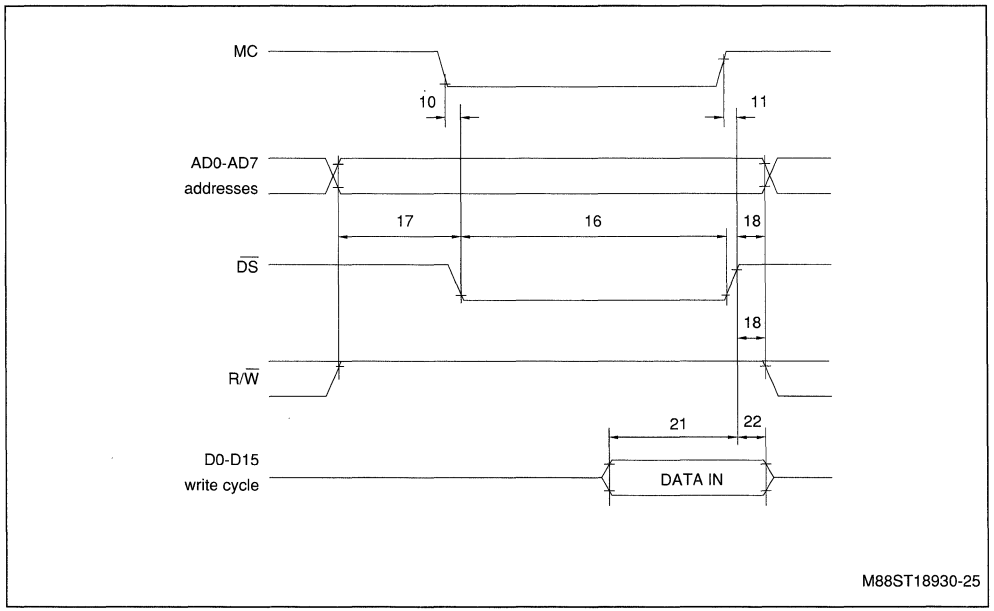


Figure 35 : Local Bus "Intel" Write Cycle Timing Diagram.

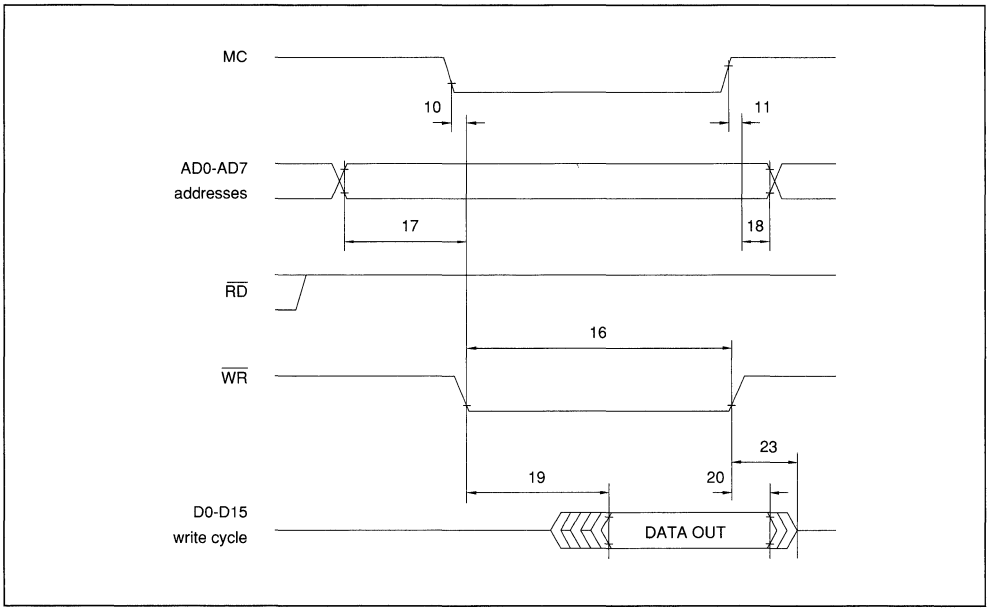


Figure 36 : Local Bus "Intel" Read Cycle Timing Diagram.

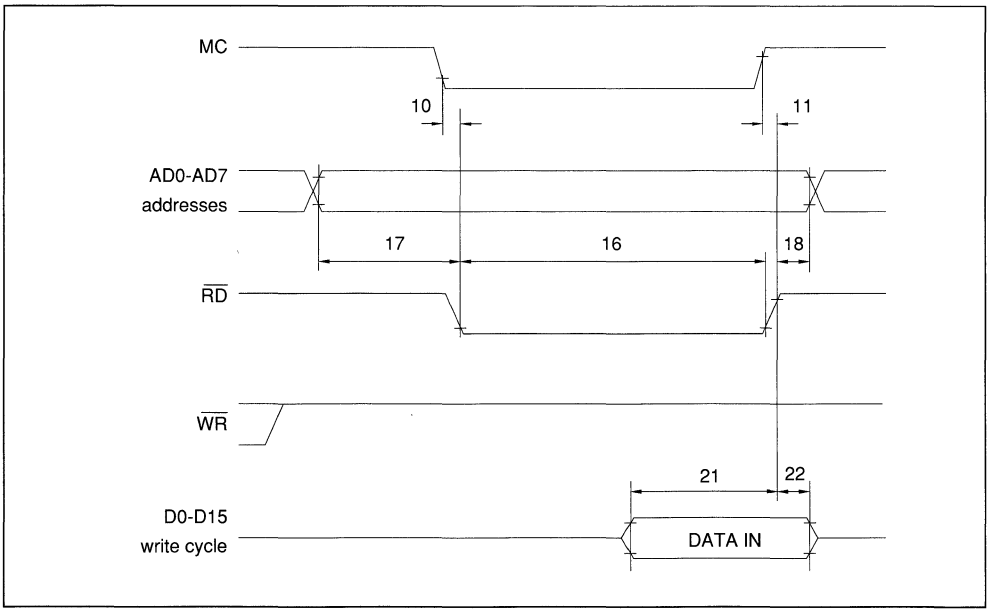


Figure 37 : Multicycles Exchange Exemple on Local Bus, "Motorola" Write Cycle (one wait state programmed).

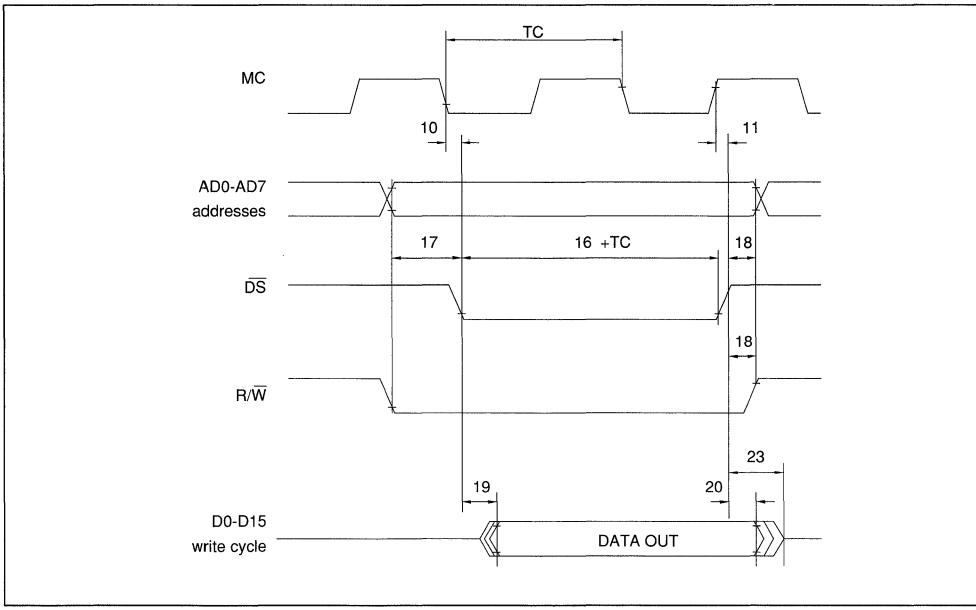


Figure 38 : Multicycle Exchange Exemple on Local Bus, "Motorola" Read Cycle (one wait state programmed.

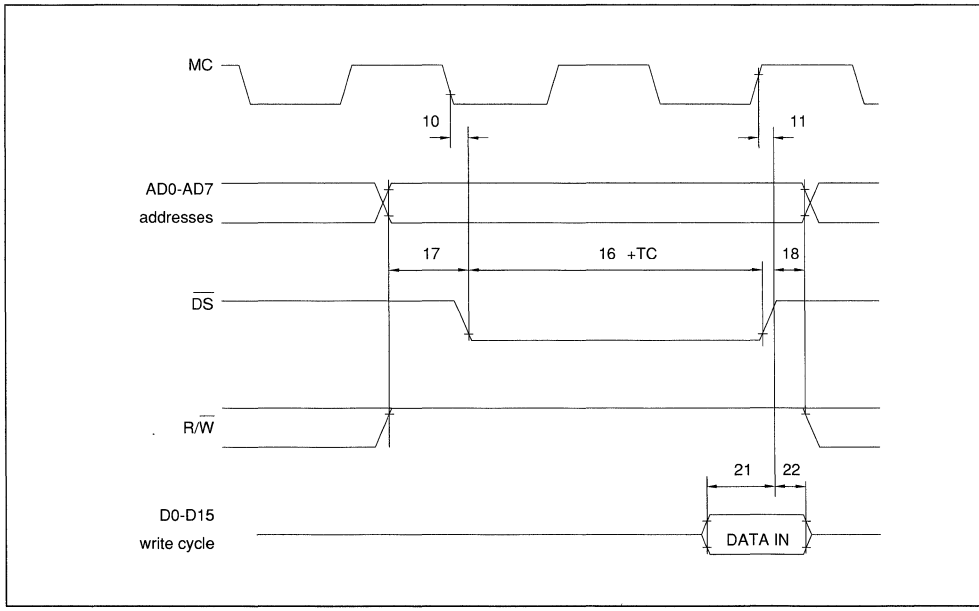


Figure 39 : System Bus : "Motorola" Write Cycle Timing Diagram.

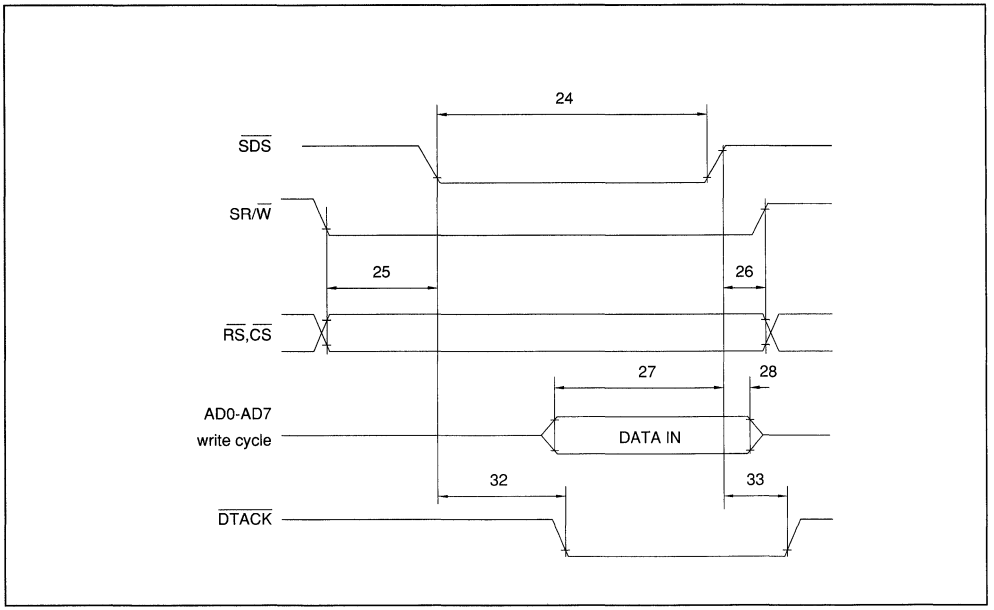


Figure 40 : System Bus : "Motorola" Read Cycle Timing Diagram.

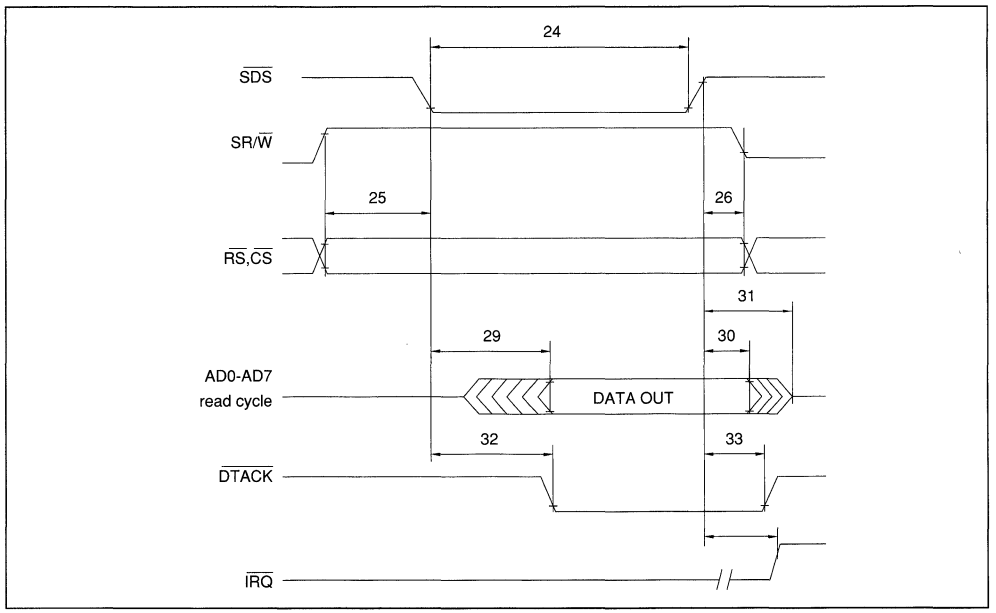


Figure 41 : System Bus : "Intel" Write Cycle Timing Diagram.

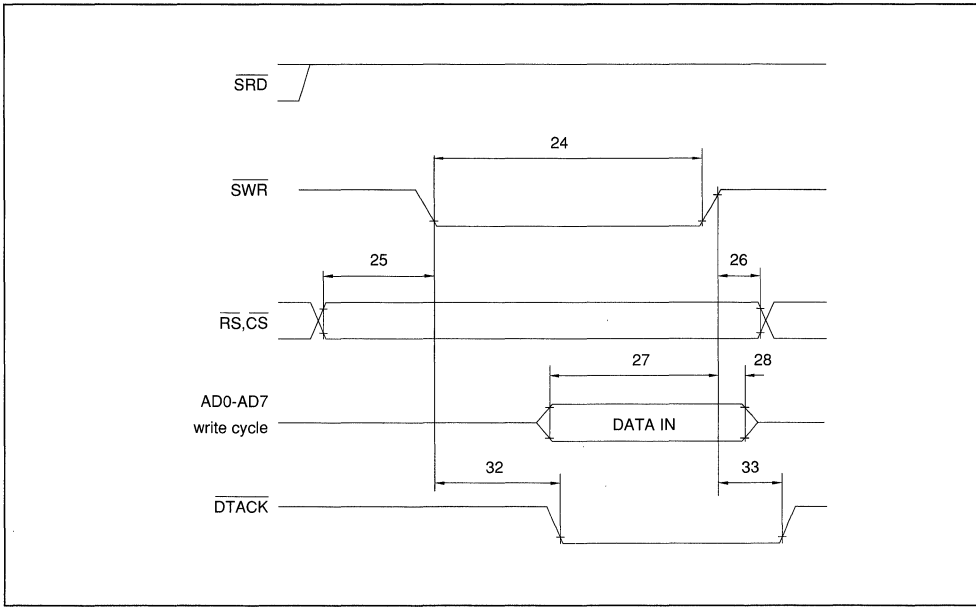
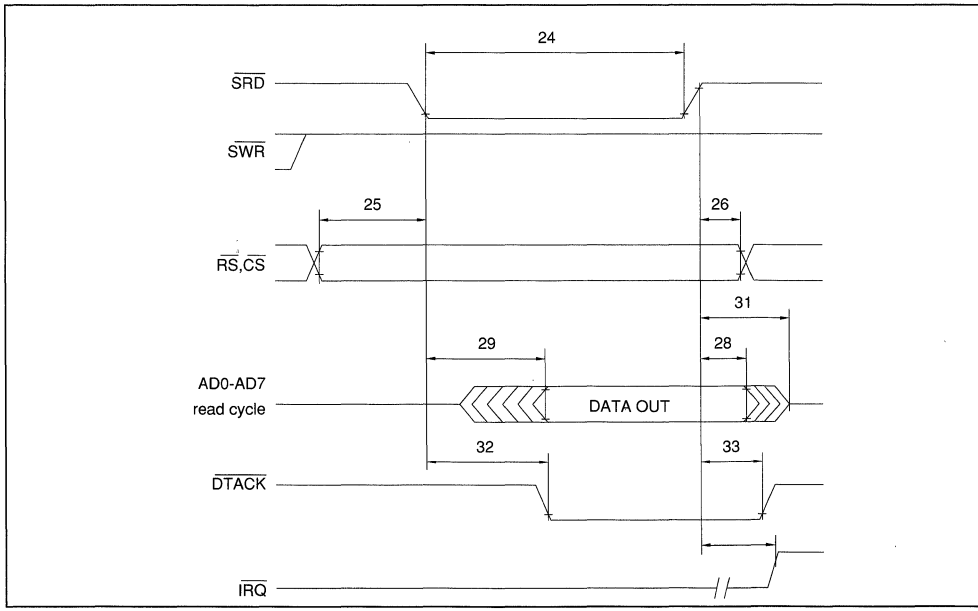
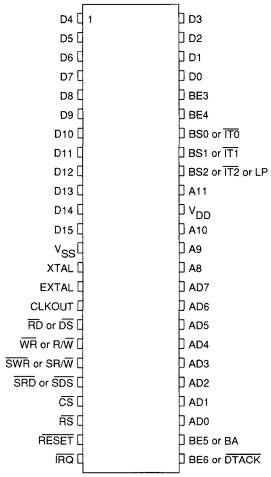


Figure 42 : System Bus : "Intel" Read Cycle Timing Diagram.



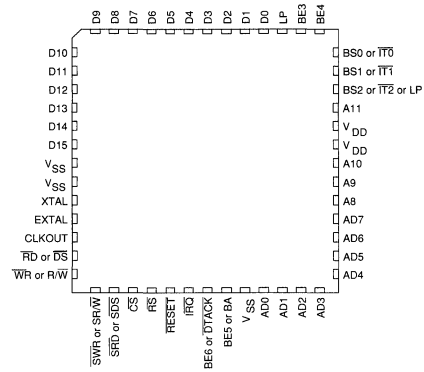
7. PIN CONNECTIONS

48 – Pin Dual – in – Line Package (top view)



M88ST18930-28

52 – Pin Plastic Leaded Chip Carrier (top view)



M88ST18930-29

1. ST18930 (top view)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	ID28	ID31	IA15	IA12	IA10	IA7	IA6	IA5	IA2	IA0	BE4	BS0	$\overline{HAIT}$
B	ID25	ID26	ID29	IA14	IA11	IA8	VSS	IA4	IA1	BE5/BA	BE3	BS1	CA0
C	ID22	ID23	ID27	ID30	IA13	IA9	VDD	IA3	BE6 / $\overline{DTACK}$	CA9	BS2	$\overline{NOP}$	CA1
D	ID19	ID21	ID24								$\overline{RESET}$	CA2	CA4
E	ID17	ID18	ID20								CA3	CA5	CA6
F	ID14	ID15	ID16								CA7	CA8	A8
G	ID13	VSS	VDD				ST 18931 PGA 121				VDD	VSS	A9
H	ID12	ID11	ID10								AD0	A11	A10
J	ID9	ID8	ID6								AD4	AD2	AD1
K	ID7	ID5	ID2	N/C							$\overline{RS}$	AD5	AD3
L	ID4	ID1	D0	D3	D7	D11	VSS	$\overline{CSDH}$	MC	EXTAL	$\overline{SDS}$	AD7	AD6
M	ID3	D1	D4	D6	D9	D12	VSS	$\overline{CSDL}$	R/$\overline{W}$	IN CYCLE	CC	SR/$\overline{W}$	$\overline{CS}$
N	ID0	D2	D5	D8	D10	D13	D14	D15	$\overline{DS}$	CLKOUT	LP	XTAL	$\overline{IRQ}$

M88ST18930-30

ORDERING INFORMATION

Part Number	Temperature Range*	Package
ST18930CP/PXXX**	0 to 70 °C	48 Pin Plastic DIL
ST18930CFN/PXXX**	0 to 70 °C	52 Pin Plastic LCC
ST18931CR	0 to 70 °C	121 Pin Grid Array

* For extended temp. range, please consult your sales office.
** XXX is the specific number associated to a customer code.
* The ST18930/31 is available in 80 ns, 100 ns cycle time versions. Please consult your sales office.

SOFTWARE TOOLS

ST18930 SP-PC	Software Package for PC Including Macroassembler Functionnal Stimulator Linker
ST18930 SP-VMS	Same Software Package for VAX Machines under VMS
ST18930 SPC-PC	Same Software with C-compiler for PC
ST18930 SPC-VMS	Same Software with C-compiler for VAX

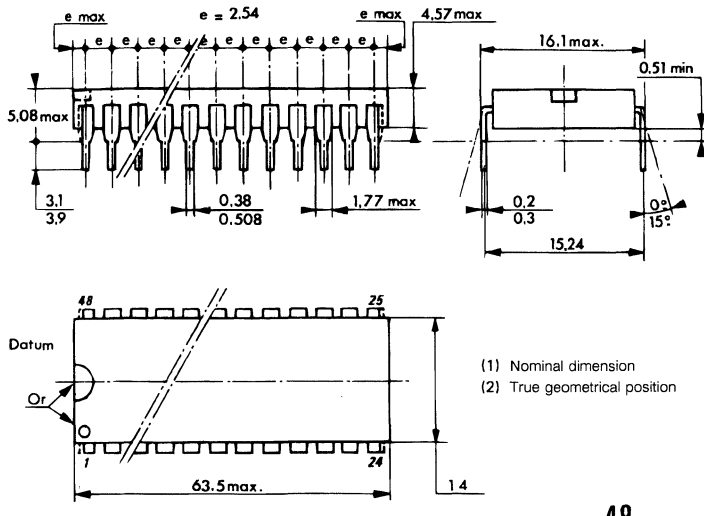
HARDWARE TOOLS

ST18930 EMU	Stand-alone Emulator
ST18930 HDS-1	Hardware Development System 110 V Power Supply
ST18930 HDS-0	Hardware Development System 220 V Power Supply
ST18930 EPR48	EPROM Simulation Module for ST18930 in 48 Pins DIP
ST18930 EPR52*	EPROM Simulation Module for ST18930 in PLCC52

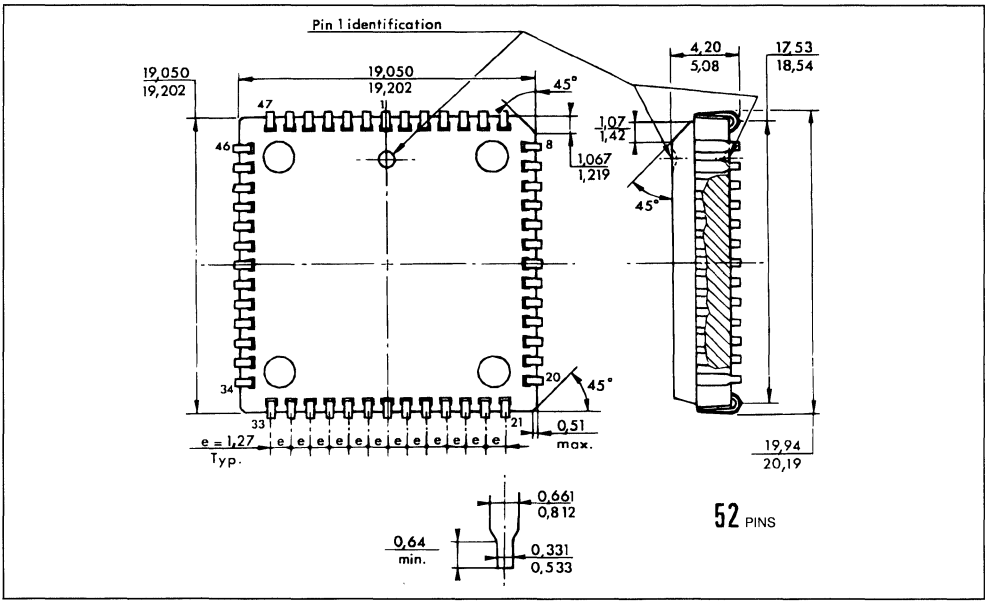
* Consult your sales office for availability.

9. PACKAGE MECHANICAL DATA

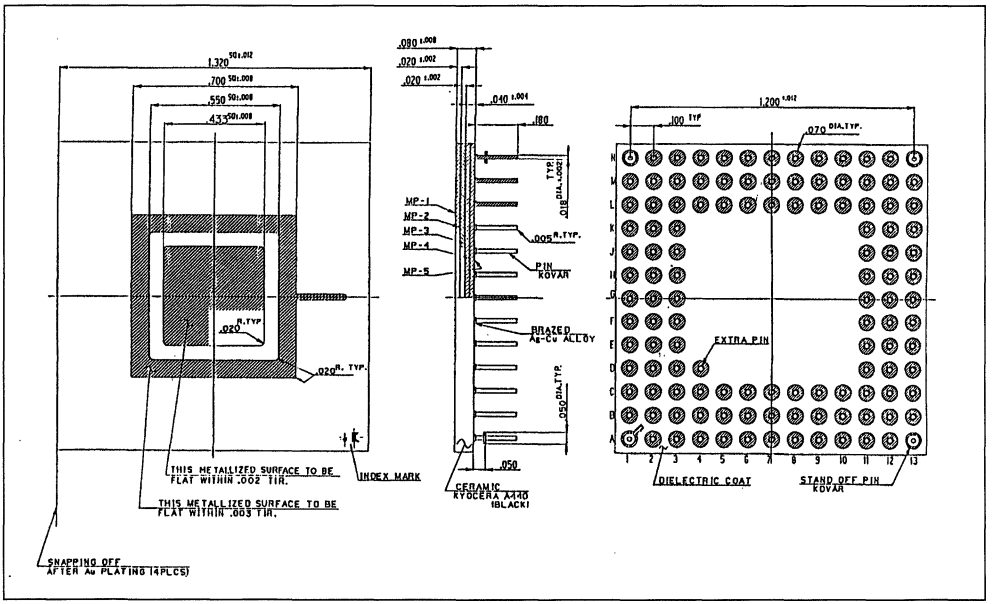
48 PINS – PLASTIC DIP



52 PINS – PLASTIC LEADED CHIP CARRIER



121 PINS – PIN GRID ARRAY CERAMIC



APPENDIX A

BENCHMARK

	Execution Time (nsec)	Memory Size (words) Prgm + coef	Number of Clock Cycles	Clock Freq. (MHz)	Word Size (bits)	Coefficient Size (bits)	Result Size (bits)
20 Tap FIR Filter	2400	6 + 20	24	10	32	16	16
64 Tap FIR Filter	6800	6 + 64	68	10	32	16	16
67 Tap FIR Filter	7100	6 + 67	71	10	32	16	16
8 Pole Cascaded Canonic Biquad IIR Filter (4X)	2800	13 + 20	23	10	32	16	16
8 Pole Cascaded Canonic Biquad IIR Filter (5X)	2400	13 + 20	23	10	32	16	16
8 Pole Cascaded Transpose Biquad IIR Filter	3300	15 + 20	33	10	32	16	16
Dot Product	600	6	6	10	32	16	16
Matrix Mult 2X2 Times 2X2	1400	14	14	10	30	16	16
Matrix Mult 3X3 Times 3X1	1500	15	15	10	32	16	16
M-to-M FFT 64 Point	121300	203 + 388	1213	10	32	16	16
256 Point	757300	349 + 764	7573	10	32	16	16

APPENDIX B

DEVELOPMENT TOOLS

DEVELOPMENT PROCESS

The development process of a digital signal processing application using the ST18930 or ST18931 is supported by a complete range of dedicated software and hardware tools which includes macroassembler, linker, simulator, C compiler and optimizer (respectively ST18930SP or ST18930SPC), standalone emulation card ST18930EMU, multiprocessor hardware development system ST18930HDS, EPROM emulation module, ST18930EPROM.

SOFTWARE TOOLS

All the development softwares run on the most common computers, such as IBM-PC® or AT®, under MS-DOS® or VAX®, VMS®, UNIX® or ULTRIX® operating systems.

The macroassembler supports conditional assembly, high level language facilities for loop definition and generates all the files for simulation, emulation and PROM programming.

The functional simulator provides step by step execution, break on address and data values, access to all internal registers and interface to I/O files (ADC, DAC, test inputs).

The linker provides modular programming facilities.

The library consists of macros, basic DSP routines etc... and provides additional help to user's for their applications.

The C language compiler offers high-level language facilities which meets the advanced requirements (parallelism, pipe-line, three computation modes, 32-bit instruction set) of the ST18930/31.

HARDWARE TOOLS

All the hardware tools are designed to provide ease of use and minimum learning time by utilizing menu driven and DSP specific emulation features.

ST18930 EMU and ST18930 HDS have in common :

- Full speed emulation of ST18930 and ST18931
- Use of internal, external or application clock
- 20 breakpoints (stops at defined addresses)
- 8 complex breakpoints (stop after N address X and M address Y)
- Realtime trace of internal resources
- Emulation probes (for ST18930 or ST18931)
- Menu driven operation (about 100 commands)
- Resident Assembler/Disassembler with full screen editor
- Symbolic debbuging
- Direct link with PROM programmers

Emulator specific features.

The ST18930EMU is a low cost, stand-alone emulator providing advanced emulation features such as real-time trace. It can be driven via a RS232C link by a terminal or an IBM-PC^R and offers :

- 8 K program memory (expandable to 64 K)
- 2 K x 16-bit data RAM
- A wire-wrapping area
- Full speed 100 ns cycle emulation
- 2 RS232C serial ports
- Complex conditions break-points

Hardware development station features :

The ST18930 HDS is a hardware development station, aimed at the development of multiprocessor applications. Up to four pairs of emulator boards, and logic analyser boards can be combined to match exactly the user needs :

- CMOS memory for backup of configuration
- 64 K x 32 program memory
- 4 K x 16 data RAM
- A logic analyser with :

* 2 K x 19 bit for trace of ST18930/31 bus and 15 external inputs

* Synchronous analyzer on program and local buses

* Asynchronous analyzer on system bus or external inputs

* Triggering conditions (Address bus with count, data bus external branch inputs, mailbox exchanges, external inputs).

EPROM module.

The ST18930EPROM is a small-sized module which uses the perfect compatibility between ST18930 and ST18931. The module uses a ST18931 and fast EPROM memories to emulate in real time a ROM masked SR18930 during prototyping or field tests to minimize hardware developments. The module is plug and function compatible with ST18930 pin out.

APPENDIX C

MASKING INFORMATION

The information required by SGS-THOMSON Microelectronics to realize a customer masked version of the ST18930 are provided below.

The files for masking must include program ROM content and coefficient ROM content. They can be transferred on EPROMS, 5" 1/4 floppy disks, magnetic tapes (VAX/VMS format) or by link to SGS-THOMSON Microelectronics. This must be done in conjunction with your local sales office or representative indications.

VERIFICATION MEDIA

All original pattern media are filed for contractual purpose and are not returned. A computer listing of the ROM content code will be generated and returned to the customer with a listing verification form. The listing should be carefully checked and the approval form completed, signed and returned to SGS-THOMSON. The returned verification form is the contractual agreement for generation of the customer masks and batch manufacturing.

VERIFICATION UNITS

Ten engineering samples containing the customer ROM patterns will be sent for program verification. These samples will be engineering samples and must be kept by user as reference parts.

DIGITAL SIGNAL PROCESSOR
CUSTOMER ORDERING SHEET

COMMERCIAL REFERENCE* : .....

CUSTOMER'S MARKING : .....

COMPANY : .....

ADDRESS : .....

PHONE : .....

PATTERN MEDIAS :

O EPROMS

O 5 1/4" FLOPPY

O MAGNETIC TYPE

O OTHER*

OPTION :

O WATCHDOG

O LOW POWER ON BS2 PIN

O DIVISION OF CLOCK IN LOW POWER MODE

O DIVISION OF EXTAL
- ÷ 2
- ÷ 4

YEARLY QUANTITY FORECASTED :

START OF PRODUCTION DATE :

FOR A SHIPMENT PERIOD OF :

Customer Contact Name **Date** **Signature**

* See your local sales office the different options.

APPENDIX D

SUMMARY OF RESOURCES PER FUNCTION

OPERATING MODES

Symbol	Function	Resource	Paragraph Nb
MODE	2-bit register defining the operating mode (real/complex/double precision)	Access Mode Register	3.2

OPERATING UNIT

Symbol	Function	Resource	Paragraph Nb
ALU	2 Port 16-bit Arithmetic Logic Unit. 5 Possible Sources. 4 Possible Destinations. 30 ALU Codes Works on 32-bit. Data in 2 Machines Cycles.	Arithmetic Logic Unit	3. 2. 1
D	ALU Output Register		
BS	Variable 0 – 15-bit right shift, left shift, right rotation barrel shifter.	Barrel Shifter	3. 2. 2
MULT	16 X 16 → 32 parallel pipeline multiplier + 16-bit adder/substractor , used in complex Multiplications.	Pipeline Multiplier	3. 2. 3
M, N	2 X 16-bit registers containing multiplier operands.		
P	2 X 16-bit register containing multiplier result.		
STA	16-bit register containing status of ALU, mode, status of address calculation units,enable interrupt flag.	Status	3. 2. 4
STR	7-bit register included in STA.	Status	3. 2. 4
CCR	9-bit register included in STA.	Status	3. 2. 4
A	2 x 16-bit accumulator.	Accumulators	3. 2. 4
B	2 x 16-bit accumulator.		
F	4 x 16-bit first in first out register.	Fifo	3. 2. 4
EF	Flag. Indicates that the Fifo is empty; can be set by software.	Empty Fifo	
RC	6-bit register allowing replacement of ALU operation code by a data coming from L-BUS.	Replace Code Register	3. 2. 4
T	2 x 16-bit register providing direct transfer between L-BUS and Z-BUS.	Transfer Register	3. 2. 4
SAT	Flag indicates saturation mode.	Saturation	3. 2. 4

DATA MEMORY BLOCK

Symbol	Function	Resource	Paragraph Nb
XRAM YRAM	192 x 16-bit (X) and 128 x 16-bit (Y) Random Access Memories	Data RAMs	3. 3. 1
CROM	512 x 16-bit read only memory containing coefficients or constants.	Data ROM	
XACU YACU	Arithmetic units providing address incrementation, decrementation and automatic loop. XACU is dedicated to XRAM. (8 bits) YACU is dedicated to YRAM. (7 bits)	Address Calculation Units	3. 3. 2
ECACU	12-bit arithmetic unit providing incrementation, decrementation of address. Shared by CROM and ERAM (external RAM).		
XC YC	Flag indicates the circular addressing mode for XRAM. Flag indicates the circular addressing mode for YRAM.	XRAM Circular Flag YRAM Circular Flag	3. 3. 3
X0, X1 X	2 x 8-bit registers used for indirect addressing of XRAM Supplementary register used for circular addressing.	Pointers	3. 3. 4
Y0, Y1 Y	2 x 7-bit registers used for indirect addressing for YRAM. Supplementary register used for circular addressing.		
C0, C1	2 x 9-bit register used for indirect addressing of CROM.		
E0, E1	2 x 12-bit registers used for indirect addressing of ERAM.		

CONTROL BLOCK

Symbol	Function	Resource	Paragraph Nb
IROM	3072 x 32-bit word read-only-memory containing program code and immediate data for ST18930 (ref section 6. 6 for ST18931)	Instruction ROM	3. 4. 2
IR	32-bit register containing instruction.	Instruction Register	
PC	Register containing address of program memory.	Program Counter	3. 4. 3
SEQ	The sequencer can test directly 16 conditions programmed on a high or low state and the sequencer controls next program address defined by BRANCH, subroutine call, next instructions or interrupt.	Sequencer	3. 4. 1
RAS	2 x 16-bit register for saving programm counter in case of subroutine call or interrupt.	Return Address Stack	3. 4. 1
LC	15-bit register containing a control word for automatic loop. It is divided into the following sub-registers.	Loop Counter	3. 4. 4
LCI	4-bit register containing the number of instructions to be executed in the loop.		
LCR	8-bit register containing the number of loops.		
LCD	3-bit register containing the number of instructions between declaration and start of the loop.		
	Prevents locked states for ST18930 only.	Watchdog Circuit	3. 6. 3
LP	Freezes the circuit operation.	Low Power Mode	3. 6. 4

INPUT/OUTPUT BLOCK

Symbol	Function	Ressource	Paragraph Nb
IT	Interrupt routine start.	Interrupts	3. 5. 1
AMR	8-bit register defining the access mode on the 2 external buses (local and system).	Access Mode Register	3. 5. 7
RIN ROUT	3 x 8-bit shift registers. Mailbox input. 3 x 8-bit shift registers. Mailbox output.	Input Registers Output Registers	3. 5. 6
RDYOIN	Flag used in the protocol to indicate witch processor has access to the mailbox.	Read Out Internal	3. 5. 5
CRR	4-bit register defining EXTAL to CLKOUT frequency ratio.	CLK Rate Register	3. 6. 1
$\overline{SIM}$	Flag used to define access mode on system bus.	System Intel Motorola	3. 5. 7

SGS-THOMSON MICROELECTRONICS

ST18940/41

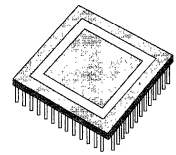
DIGITAL SIGNAL PROCESSOR

MAIN FEATURES

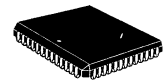
- 100ns MACHINE CYCLE TIME (1.2 CMOS Technology)
- PARALLEL HARVARD ARCHITECTURE
- TRIPLE DATA BUSES STRUCTURE
- 3 DATA MODES . SINGLE PRECISION
  . DOUBLE PRECISION
  . COMPLEX
- 32-BIT INSTRUCTION
- MULTIPLIER 16 x 16 —> 32, SIGNED AND UNSIGNED
- 32-BIT BARREL SHIFTER, 32-BIT ALU
- PROVISION FOR FLOATING POINT
- FOUR 32-BIT ACCUMULATORS, FOUR LEVEL 32-BIT FIFO
- IMMEDIATE AND COMPUTED BRANCH
- 8-LEVEL STACK
- 9 EXTERNAL AND 3 INTERNAL INTERRUPTS
- AUTOMATIC LOOP, UP TO 256 TIMES 32 INSTRUCTIONS
- 2 INDEPENDENT PARALLEL BUSES ; LOCAL AND SYSTEM
- FULL SPEED ACCESS TO EXTERNAL 64K x 16-BIT MEMORY ON THE LOCAL BUS
- HARDWARE AND/OR SOFTWARE WAIT STATES MODE TO ACCESS SLOWER EXTERNAL MEMORIES/PERIPHERALS, DMA CHANNEL
- 2 x 16 BYTES FIFO ON THE SYSTEM BUS
- SERIAL CHANNEL FOR DIRECT INTERFACE WITH CODEC, ISDN IC's...
- GENERAL PURPOSE PARALLEL PORT
- ON CHIP DATA RAM 2 x 256 x 16-bit
- FOUR INDEPENDENT ADDRESS CALCULATION UNITS
- ADDRESSING MODES : IMMEDIATE, DIRECT, INDIRECT WITH POST MODIFICATION, CIRCULAR, BIT REVERSED
- 2 VERSIONS : - ST18940 (PLCC/PGA 84) CLOSED VERSION WITH 3K x 32-BIT ON-CHIP PROGRAM ROM AND 512 x 16-BIT COEFFICIENT ROM
  - ST18941 (PGA 144) OPEN VERSION WITH 64K x 32-BIT OFF-CHIP PROGRAM ROM AND 128 x 16 BIT ON-CHIP COEFFICIENT RAM
- POWER DOWN MODE
- TYPICAL CONSUMPTION 0.5W

DEVELOPMENT SYSTEM

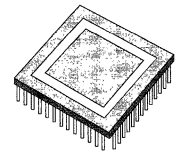
The ST18940-41 is supported by a complete set of hardware and software tools for system development. The software package includes an assembler/linker, a simulator, and a "C" compiler and optimizer which run under several VAX and PC operating systems. Hardware tools include a standalone emulator, an EPROM emulation module, a multiprocessor development station and an evaluation module (PC compatible).



ST18941 - PIN GRID ARRAY - 144-pin



ST18940 - PLASTIC LEADED CHIP CARRIER - 84-pin



ST18940 - PIN GRID ARRAY - 84-pin

DESCRIPTION

The ST18940/41 Digital Signal Processor is a member of SGS-THOMSON Microelectronics ST18 family.

The ST18 family comprises 3 products covering a wide spectrum of DSP applications. Complete development tools (hardware and software) are available as aids to efficient system designs.

The first processor in the ST18 family is the TS68930/31 (NMOS) with a 160ns machine cycle time. The second member of the family, the ST18930/31, is a CMOS version of the TS68930 with a faster instruction cycle time (80ns) and the inclusion of additional hardware and software features (The ST18930 is pin compatible with the TS68930).

The ST18940/41, which is described in this datasheet, is the third member in the family. It is upward compatible with the other members of the family, but provides enhanced arithmetic capabilities, addressing modes and additional I/O functions.

It is an advanced HCMOS single chip general purpose DSP designed for fast arithmetic intensive applications in the areas of telecommunications, modems, speech processing, graphic/image processing spectrum analysis, audio processing, digital filtering, high speed control, instrumentation, numeric processing...

The ST18940 structure is based on a triple 16-bit data bus, a 16 x 16 multiplier, a 32-bit ALU. The powerful parallel and serial Input/Output interfaces and the DMA channel contribute to the flexibility of the system interface with external environment.

Two versions are available :

- the ST18940 includes 3K x 32-bit program ROM and 512 x 16-bit coefficient ROM.
- the ST18941 microprocessor version can address up to 64K of program memory on a dedicated bus, thus providing true real-time emulation of the ST18940 ROM version. In addition to the two internal RAMs (X and Y), a 128 x 16-bit coefficient RAM is included for coefficient memory emulation.

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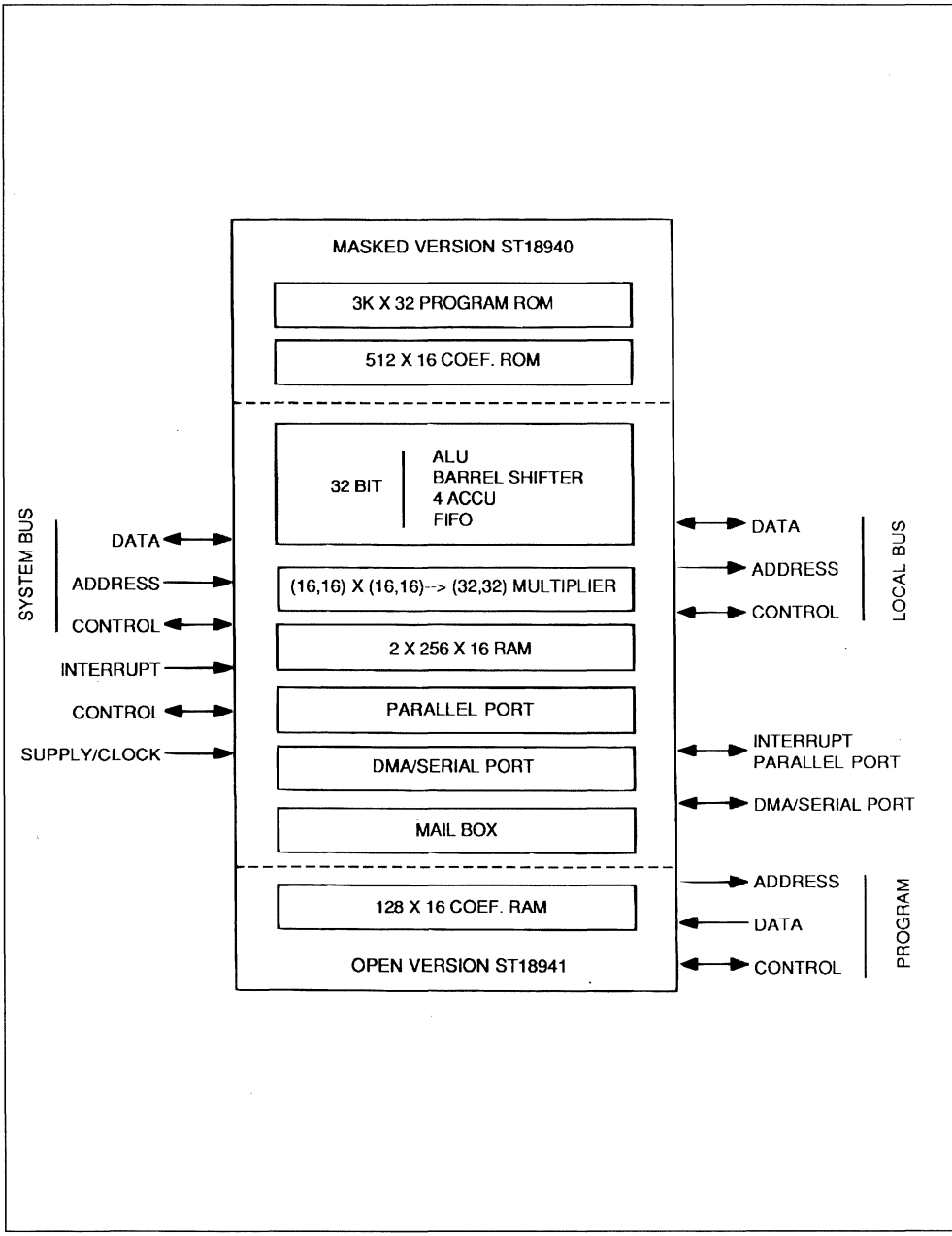
TABLE OF FIGURES

1. PIN DESCRIPTION

Figure 1 : Input/Output Pins.



1.1. LOCAL BUS

Name	Pins Type	Function	Description
D0-D15	I/O	Local Data Bus	16-Bit Data Bus. In high impedance when exchanges are not active or when RESET, HOLD, HALT or LP are active.
A0-A15	O	Local Address Bus	16-Bit Address Bus for Local Data. In high impedance when HOLD, HALT or LP are active.
$\overline{DS}/\overline{RD}$	O	Data Strobe/read	Synchronizes the transfer on local bus/read cycle.
R/$\overline{W}$ / $\overline{WR}$	O	Read/write/write	Indicates the current bus cycle state/write cycle.
$\overline{DTACK}$	I	Data Transfer Acknowledge	Indicates exchange acknowledgement.
$\overline{BR}$	O	Bus Request	Active at each exchange on the local bus. In combination with DTACK, can be used to address resources shared by several processors.
$\overline{HOLD}$	I	Hold Data	Used to free local bus in shared memory application. To HALT state if an access is attempted.
$\overline{HOLDACK}$	O	Hold Acknowledge	Indicates that the processor is in hold state.

1.2. SYSTEM BUS

Name	Pins Type	Function	Description
SD0-SD7	I/O	System Data Bus	8-Bit data bus used for exchanges between the processor and a host via the mailbox.
$\overline{CS}$	I	Chip Select	Selection of the system bus interface.
RS	I	Register Select	Address to select data FIFO or status register (MBS).
$\overline{SDS}/\overline{SRD}$	I	Data Strobe/read	Synchronizes the transfer on the system bus/read cycle.
SR/$\overline{W}$/$\overline{SWR}$	I	Read/write/write	Indicates the current system bus cycle/write cycle.
$\overline{SDTACK}$	O	System Data Transfer Acknowledge	Indicates data exchange is acknowledged. Open drain.
$\overline{IRQ}$	O	Interrupt Request	Signal sent to the host to signal readiness for mailbox data exchange.

1.3 DMA/SERIAL I/O INTERFACE : DUAL PURPOSE INTERFACE

Internally the DMA channel and serial I/O are implemented as fully independent separate blocks, although externally they are share 4 dual purpose I/O pins.

- DMA CHANNEL

Name	Pins Type	Function	Description
$\overline{DMARQ}$	I	DMA Request	Activated by the device requesting the DMA. Can be a pulse ("single" mode) or a level ("burst" mode) (DPI0).
$\overline{DMACK}$	O	DMA Acknowledge	Indicates that the request for DMA is acknowledged (DPI1).
$\overline{DMAEND}$	O	DMA End	Indicates the end of the DMA exchange. Active as long as the channel is not reinitialized (DPI2).
$\overline{DSDMA}$	O	Data Strobe DMA	Synchronizes the DMA exchange (DPI3).

- SERIAL INPUT/OUTPUT INTERFACE

Name	Pins Type	Function	Description
FSR	I/O	Frame Synchronization Receive	Synchronizes the receive. Can be generated or received by the processor (DPI0).
BCLKR	I/O	Bit Clock Receive	Receive bit clock. Can be generated or received by the processor (DPI1).
DA	I/O	Data A	Input or Output of Data A (DPI2).
DB	I/O	Data B	Input or Output of Data B (DPI3).
FSX	I/O	Frame Synchronization Transmit	Synchronizes the transmit. Can be generated or received by the processor (DPI4).
BCLKX	I/O	Bit Clock Transmit	Transmit bit clock. Can be generated or received by the processor (DPI5).

Note : $\overline{\text{DMARQ}}$/FSR, $\overline{\text{DMACK}}$/BCKLR, $\overline{\text{DMAEND}}$/DA, $\overline{\text{DSDMA}}$/DB are multiplexed.

1.4 PARRALLEL/INTERRUPT INTERFACE

This 8-bit port can be configured either as an interrupt controller or as a parallel input/output port.

- INTERRUPT CONTROLLER

Name	Pins Type	Function	Description
P0-P3	I	Maskable Interrupt Request	A negative transition on these input pins will initiate an interrupt sequence.
P4-P7	I	Maskable Interrupt Request	A low level on these input pins will initiate an interrupt sequence.

- PARALLEL INTERFACE

Name	Pins Type	Function	Description
P0-P7	I/O	Parallel Port	8-Bit parallel port with each bit programmable individually as input or output. Can be used as test conditions in branch instructions; four bits are edge sensitive, four are level sensitive.

1.5. POWER SUPPLY - CLOCK

Name	Pins Type	Function	Description
XTAL	O	Crystal Output	Internal oscillator output for crystal. Not connected if the internal oscillator is not used.
EXTAL/ CLKIN	I	Crystal Input	Internal oscillator input. External clock input, when the internal oscillator is not used. Oscillator frequency is twice the machine frequency.
CLKOUT	O	Clock Out	Internal clock output (oscillator frequency ÷ 2).
V_{CC}		5 Volts	Power Supply.
V_{SS}		Ground	Connected to Ground.

1.6. OTHER PINS

Name	Pins Type	Function	Description
$\overline{INT}$	I	Interrupt	Maskable interrupt request. Active Low
$\overline{RESET}$	I	Reset	Program counter is loaded with Hex. 0 and a NOP instruction is executed. Clock generator is resynchronized.
LP	I	Low Power	Stops the processor at the end of the current cycle, forces the NOP instruction and puts the processor in the powerdown mode. The internal processor state is conserved.
HT2	O	Clock	Reserved for test.

1.7. SPECIFIC PINS TO THE 18941 (open version)

Name	Pins Type	Function	Description
IA0-IA15	O	Instruction Address Bus	16-Bit address bus for external program memory. In high impedance if HALT is active or during a DMA exchange.
ID0-ID31	I	Instruction Data Bus	32-Bit data bus from external program memory.
$\overline{NMI}$	I	Non Maskable Interrupt	Interrupt input edge sensitive. Program counter is loaded with Hex. A.
$\overline{HALT}$	I	Halt	Stops the processor at the end of the current instruction. Local bus and instruction address buses are in high impedance.
$\overline{ECR}$	O	Enable CROM	Indicates that the A0-A8 addresses are used for the external emulation of the CROM.
INCYCLE	O	Instruction Clock	A falling edge indicates the start of a new instruction cycle.

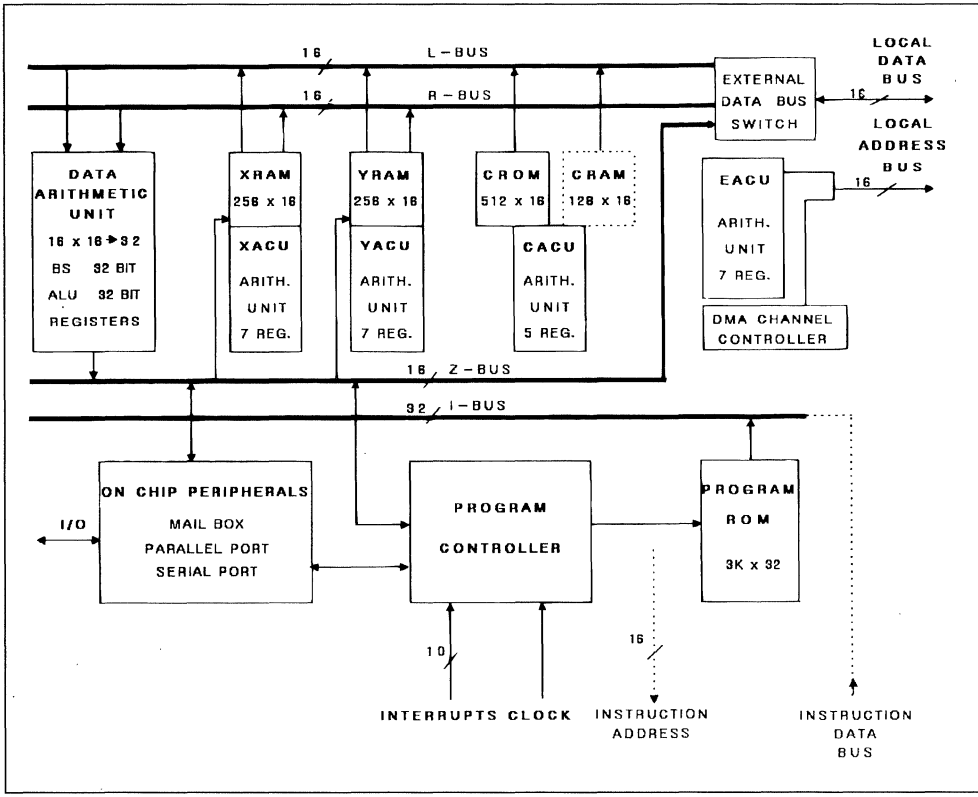
2. ARCHITECTURE

The architecture is HARVARD like with separate instruction bus and data buses. The block diagram shows four main blocks (see fig. 2) :
- the program controller
- the data arithmetic unit
  (ALU, multiplier and barrel shifter)
- the data storage unit
- the inputs/outputs

These four blocks can be considered as four independent processors working in parallel and communicating via three 16-bit data buses.
Within a single machine cycle the processor is able to execute all of the following operations :
- read two operands in internal or external memory
- execute a multiplication
- execute an ALU operation
- write a result to internal or external memory
- modify three address pointers
- in addition, I/O operations with on-chip peripherals may take place concurrently with internal operations.

3. BLOCK DIAGRAM

Figure 2 : ST18940/41 Block Diagram.



4. FUNCTIONAL DESCRIPTION

4.1. INTRODUCTION

One of the key features of the ST1840/41 is that all hardware resources have been designed to support the following three data types :

- simple precision : 16-bit data
- double precision : 32-bit data
- complex : 16-bit real and 16-bit imaginary

Any one of the above three arithmetic modes can be dynamically selected by means of a single program instruction. Once the mode has been selected, all resources (such as ALU, memories, registers, multiplier) are automatically configured for the appropriate operations. The same assembler instructions are used in all three modes. In double-precision and complex modes the data are stored in two contiguous memory locations, with an automatic adjustment of the address calculation unit. Two's complement representation is used throughout. In real mode, all instructions except branch are executed in one cycle time. In complex and double precision modes, all instructions are executed in two cycle times.

4.2. PROGRAM CONTROLLER

4.2.1. PROGRAM CONTROLLER (see figure 3). The purpose of the program controller is to generate the next instruction address to be executed, this instruction being in external memory for the ST18941 (64K word of 32-bit) or in the masked ROM for the ST18940 (3K word of 32-bit). The program controller takes into account the current mode to execute the instruction ; one cycle per instruction in

real mode, two cycles per instruction in double precision and complex mode. The HALT, HOLD, LP and the "WAIT STATES" suspend the sequencer cycle.

Exceptions in linear program address generation are the following :

- Execution of a branch instruction
- Call and return of a subroutine
- Execution of an interrupt routine : 2 types of hardware interrupt sources are possible : external interrupt [INT + P PORT + NMI (ST18941 only)], internal interrupt (Mailbox, serial port). The EI register enables or disables these interrupt sources.
- An 8-level stack is used to save and restore the PC in case of interrupts or subroutines.
- Loop execution : Automatic loop execution is possible by means of the loop register. This register defines the number of loops to be executed (max. 256), and the number of instructions in the loop (max. 32).

Programming model for loop execution

LOOP : Loop Register

It is used to automatically control the execution of a loop. This 16-bit register is divided in to 3 fields, LCI, LCR, LCD.

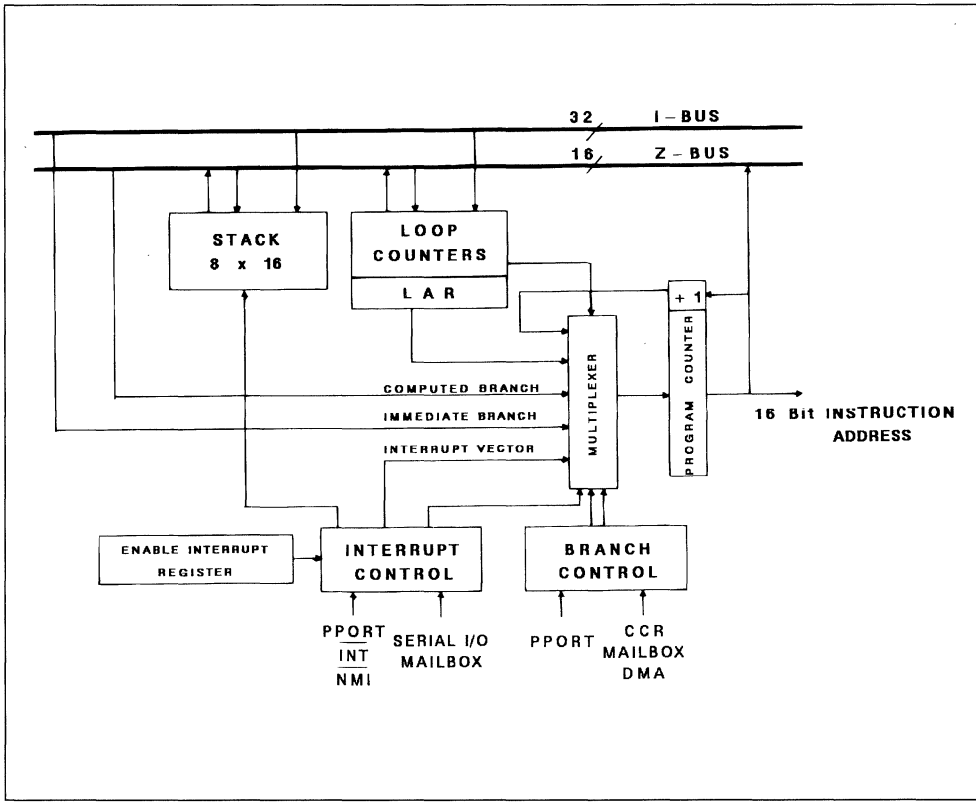
LCI (Loop Count Instruction) defines the number of instructions to be executed in a loop ; the maximum is 32 (5-bit).

LCR (Loop Count Register) defines the repeat count of the loop ; the maximum is 256 (8-bit).

LCD (Delay) defines, in terms of the number of instructions, the delay between the loop declaration and the beginning of the loop execution. The maximum is 7 (3-bit).

This "repeat of instruction blocks" feature provides code compaction and time efficient execution for vector and array processing frequently used in DSP algorithms. It is set at the macroassembler level by using a simple REPE-BEGIN-END construct.

Figure 3 : ST18940/41 Program Controller.



4.2.2. INTERRUPT CONTROL

* There are two types of hardware interrupt sources on the ST18940/41 : internal and external.

-The internal sources include chip peripheral devices : Mailbox (input/output)

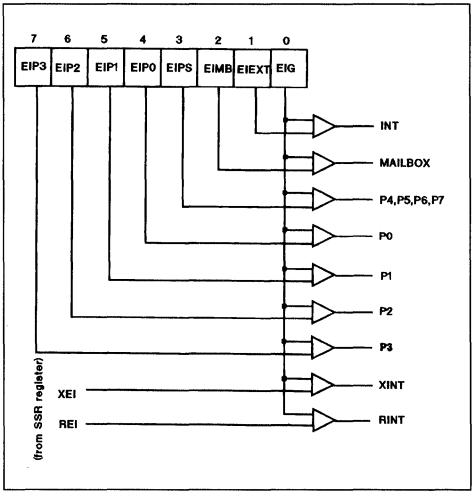
Serial port (1 for transmit, 1 for Receive)

-The external interrupts include $\overline{\text{RESET}}$, $\overline{\text{INT}}$, $\overline{\text{NMI}}$ (ST18941 only) and the P Port (8 pins)

$\overline{\text{RESET}}$, $\overline{\text{INT}}$, $\overline{\text{P4}}$, $\overline{\text{P5}}$, P6, P7 are low level sensitive interrupts and $\overline{\text{NMI}}$, P0, P1, P2, P3 are falling edge sensitive.

* The EI (enable interrupt) register is an 8-bit wide enable interrupt register. It controls the following interrupt sources : Mailbox, INT, P Port (see figure 4).

Figure 4 : ST18940/41 Enable Interrupt Register XEI, REI part of SSR Register (see page 21).



* Software interrupt can be implemented using P-Port.

* When an interrupt is acknowledged, the current program counter is pushed on the stack and the interrupt vector corresponding to the interrupt source (see table 1) is loaded into the program counter (PC). Upon completion of interrupt routine, a RTI (return from interrupt) instruction is processed. The content of the top location in the stack is popped into the PC.

Table 1 : Interrupt Vectors.

Address	Interrupt Sources
0	$\overline{\text{RESET}}$
1	$\overline{\text{INT}}$
2	R INT (serial I/O receive)
3	X INT (serial I/O Transmit)
4	B INT (mailbox)
5	P4, P5, P6, P7
6	P0
7	P1
8	P2
9	$\overline{\text{P3}}$
10	$\overline{\text{NMI}}$ (ST18941 only)

4.3. DATA ARITHMETIC UNIT (figure 5)

One of the most useful features of the ST18940-41 is to provide the user with three operating modes which can be dynamically set by software.

These three modes represent different data types :

-REAL 16-bit data

-Complex (CPLX) 16-bit real + 16-bit imaginary data

-Double-precision (DBPR) 32-bit data.

In double precision mode, data moves from and to memories are performed on 32 bits. This is especially useful in adaptive processing to keep track of L.S.B. updated coefficients.

Thus the DSP is seen by the user as a standard 16-bit real or complex machine or a 32-bit real machine. All operating units are automatically adjusted by the processor to the right length.

In all modes, the number representation used is signed 2's complement.

4.3.1. MULTIPLIER. In real and double-precision modes, the multiplier executes a 16x16-bit —> 32-bit signed or unsigned multiplication every instruction cycle.

-The operands are loaded into the M and N registers and the result of a previous multiplication is written in the P register during the same cycle.

-In complex mode the multiplier executes a complex multiplication every instruction cycle (2 x machine cycles) ie :

(a + jb) x (c + jd) = (ac - bd) + j(ad + bc).
In this case the registers M and N are 2 x 16-bit and the P register is 2 x 32-bit.

-The pipeline structure makes the multiplication result available 2 instruction cycles later in all 3 modes. The status bits relating to the multiplier are in STA (Status register) and the multiplier overflow (complex mode only) is updated in the Code Condition Register.

4.3.2. 32-Bit ALU/ACCUMULATOR. The 32-bit ALU is loaded on the right side by the R bus, by the RBD register or by the accumulators (A, B). On the left side, the operands always access the ALU through the barrel shifter, coming either from the L (left) bus or from the multiplier output register P.

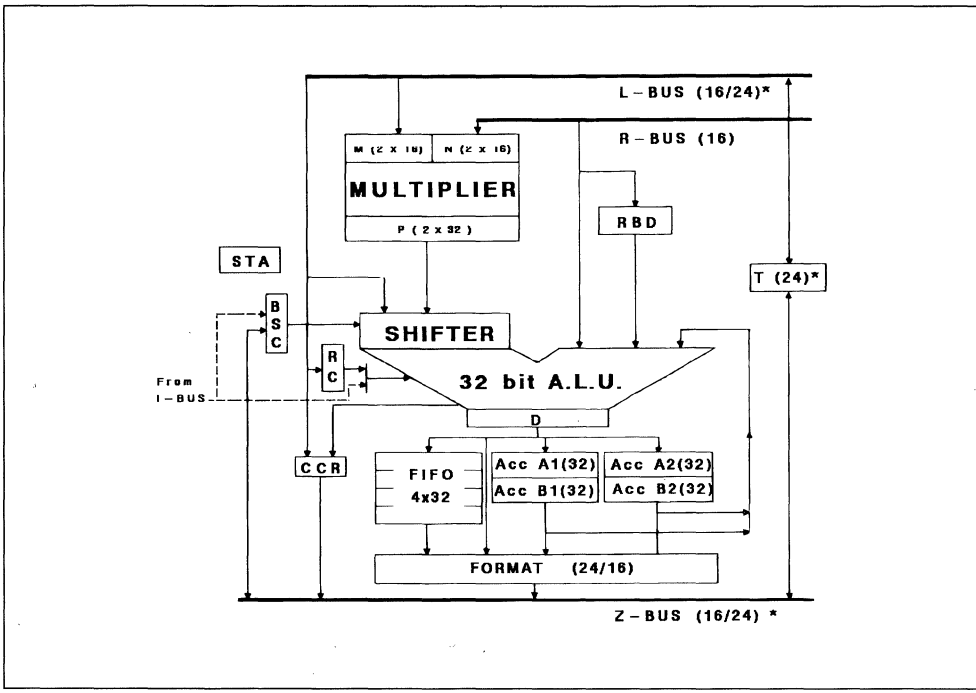
The result of an ALU operation is automatically written in the D register and, if required, into the accumulators or FIFO.

The ALU performs 32 different operations. These include the usual arithmetic, logical and shift operations e.g. ADD, SUB and AND. Additional special operations are also implemented. These include ADDS or SUBS (addition and subtraction with automatic prescaling of the left-side ALU input), and ABSolute value and EDGE operations (used for first significant bit detection and exponent adjustment).

The complete list of ALU codes and description is given in table 2 - p 27.

4.3.3. BARREL SHIFTER. The 32-bit barrel shifter located on the left side of the ALU performs all logic/arithmetic shifts and rotations. The shift value comes from the ALU code or from the BSC (Barrel Shift Control) register loaded by the Z bus. This feature combined with EDGE (Alu Code) allows easy, efficient and dynamic normalization used in floating point and dynamic scaling operations.

Figure 5 : Data Arithmetic Unit Block Diagram.



* See Note Page 15/58.

4.3.4. PROGRAMMING MODEL

Name	Function	Description
M	16 - Bit Register 2x16 - Bit (complex mode)	Left side operand of multiplier loaded via L bus.
N	16 - Bit Register 2x16 - Bit (complex mode)	Right side operand of multiplier loaded via R bus.
P	32 - Bit Register 2x32 - Bit Register (complex)	Multiplication Result
D	32 - Bit Register	ALU Result
A1, A2	2x32 - Bit Registers	Accumulators A1 and A2 are selected by ACS bit 2 of STA register in real and double precision modes.
B1, B2	2x32 - Bit Registers	Accumulators B1 and B2 are selected by ACS bit 2 of STA register in real and double precision modes.
FIFO	4x32 - Bit Registers	FIFO loaded by ALU.
T	2x24 - Bit Registers	Bidirectional register between L bus and Z bus.
RBD	2x16 - Bit Registers	Right bus delay, this register is used as a buffer on the ALU right side.
STA	16 - Bit Register	Status register defining the state of the data arithmetic unit.
CCR	16 - Bit Register	Condition code register containing the flags generated by the data arithmetic unit. Every bit can be tested as a branch condition.
RC	7 - Bit Register	This register, directly connected to the ALU control unit, can be dynamically loaded by the L bus.
BSC	5 - Bit Register	Barrel shift control register is loaded by the Z bus and contains the shift value for the barrel shifter.

CONDITION CODE REGISTER (CCR)

Name	Bit #	Function	Description
SR	15	Sign Real	Set if the MSB of the ALU result is 1. Cleared Otherwise.
SI	14	Sign Imaginary	Set if the MSB of the ALU imaginary result is 1 (in complex mode). Cleared Otherwise.
CR	13	Carry Real	Set if carry is generated out of the MSB of the result for arithmetic and shift operations. Cleared Otherwise.
CI	12	Carry Imaginary	Set if a carry is generated out of the MSB of the imaginary part of the result for complex arithmetic and shift operations. Cleared Otherwise.
Z	11	Zero	Set if the ALU result equals zero. In complex mode it is set if both real and imaginary parts are equal to zero.
OVF	10	Overflow	Set if an arithmetic overflow occurs. This implies that the result cannot be represented in the operand size. In complex mode it is set for an overflow of either the real or imaginary part. Cleared Otherwise.
MOVF	09	Memorized Overflow	Set under the same conditions as overflow. Cleared when tested by a branch instruction.
AOVF	08	Advanced Overflow	Exclusive OR of bits 30 and 31 of the ALU. Set and memorized if arithmetic overflow occurs on half capacity. Cleared when tested by a branch instruction.
OVFM	07	Overflow Multiplier	Set and memorized if the multiplier has overflowed in complex mode. Cleared by LCCR ALU instruction.
EF	06	Empty FIFO	Set if FIFO is empty. Cleared Otherwise.
	05→00		Reserved

STATUS REGISTER (STA)

Name	Bit #	Function	Description
EPI	15	Enable Imaginary Product	Imaginary product enable under interrupt.
EPR	14	Enable Real Product	Real product enable under interrupt.
SE	13	Smallest Exponent	Conditional Load of BSC
	12	Reserved	
	11	Reserved	
	10	Reserved	
MODE	09/08		Real /CPLX/DBPR
EMI	07	Enable Multiplier Input	Multiplier enable under interrupt.
TCM	06	Two's Complement M	M signed/unsigned.
TCN	05	Two's Complement N	N signed/unsigned.
CPR	04	Conjugate Product Result	M x N conjugate.
SAT	03	SATuration	ALU Saturation
ACS	02	ACcumultator Selection	A1 or A2 and B1 or B2
FORM	01	FORMat * see note 1.	24 MSB/16 LSB Selection
RBDS	00	Right Bus Delay Selection	RBD Register Selection

Note : The data buses and the T register are 24 bits wide enabling 24-bit wide ALU results to be fed back to the left ALU input.

4.4. DATA STORAGE UNIT (figure 6)

The ST18940/41 provides four different data memories within two categories : the data memories and the coefficient memory. The coefficient memory in the ST18940 is a 512 x 16-bit masked ROM (CROM). For emulation of the ST18940 CROM, a 128x16 internal CRAM is provided in addition to the external 512x16 CRAM. Internal CRAM is usefull when coefficients are to be used in conjunction with external data in the same instruction. For both versions the internal data memories consist of two 256x16 bit RAM's denoted XRAM and YRAM. The external addressing space is of size 64k x 16-bit (ERAM) and is accessible via the local bus using a single instruction as for the internal memories.

Each memory is controlled by a dedicated Address Calculation Unit called XACU for the XRAM, YACU for the YRAM, CACU for the CRAM or CROM and EACU for the ERAM.

4.4.1. ADDRESSING MODES. The addresses are generated by each ACU according to the four addressing modes :

- Immediate addressing :
the data is in the instruction
- Direct addressing :
the address is in the instruction
- Indirect addressing :
the address is in one of the ACU registers
- Circular addressing :
also called virtual shift mode
Bit reversed mode

4.4.2. ADDRESS CALCULATION UNITS (ACU). The dedicated ACU's are independent and contain 7 registers : two banks of dual pointers selected by a bit in the ASTA register, one current pointer used in the circular addressing mode, and, two post-incrementing/decrementing registers. The register structure of XACU is given below :

X0A, X1A : dual pointer bank A

X0B, X1B : dual pointer bank B

X2 : current pointer in circular addressing

K, L : two post-incrementing/decrementing registers

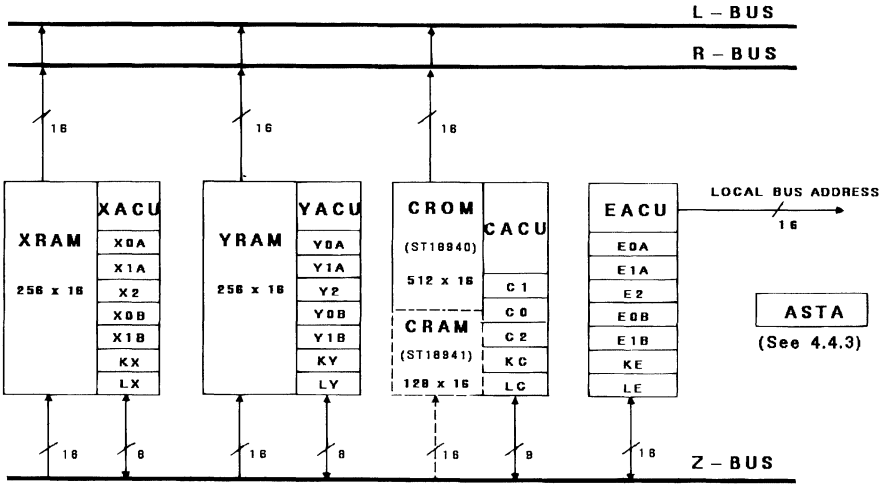
The CACU is the only ACU with a single pointer bank.

The circular addressing mode uses the A bank pointer for the minimum and maximum limits and the current pointer for the current address.

Each ACU (with the exception of CACU) supports bit reversed addressing as required for the FFT algorithms.

For the external data memory in direct addressing mode, the 16-bit address is obtained by concatenating the 13 bits contained in the instruction (LSB) to the 3 bits of the page register (MSB).

Figure 6 : ST18940/41 - Data Memories Block Diagram.



____ : ST18941 ONLY

4.4.3. ASTA REGISTER - ADDRESS STATUS REGISTER

Name	Bit #	Function	Description
RBX	15	Register Bank Selection RAMX	Select Bank A or B for X, Y or ERAM
RBY	14	Register Bank Selection RAMY	
RBE	13	Register Bank Selection ERAM	
	12		Reserved.
EC	11	External Coefficient	ST18941 only, Internal or External CRAM Selection
BRX	10	Bit reversed RAMX.	Set bit reversed mode.
BRY	09	Bit reversed RAMY.	
BRE	08	Bit reversed ERAM.	
X_C	07	Circular RAMX	Set circular addressing mode.
Y_C	06	Circular RAMY	
E_C	05	Circular ERAM	
C_C	04	Circular CROM	
ADOFX	03	ADOF RAMX	Force the 1st address in complex or double. Precision mode to be odd or even.
ADOFY	02	ADOF RAMY	
ADOFE	01	ADOF ERAM	
ADOFC	00	ADOF CROM	

4.5. INPUT/OUTPUT

The ST18940/41 provides four I/O interfaces :
-the system bus
-the local bus
-the parallel port
-the serial interface

4.5.1. THE SYSTEM BUS. For asynchronous exchanges between the ST18940/41 and a host (general purpose MCU and/or other ST18940/41 processors), the ST18940/41 is provided with a "mailbox mechanism" comprising a double 16-byte FIFO, one for input (RIN), one for output (ROUT).

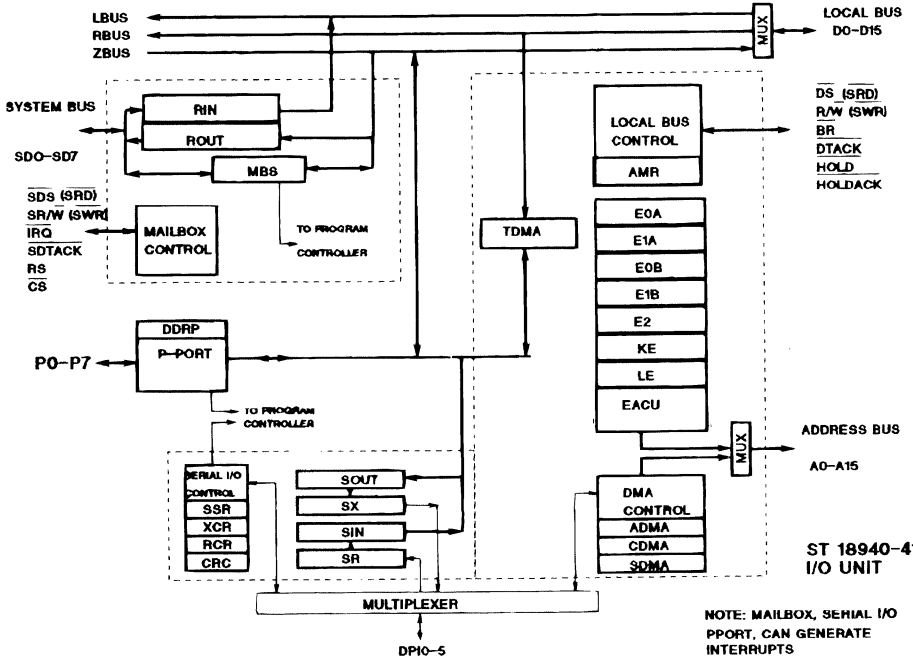
A 6-bit status register MBS is accessible to both the ST18940/41 and the host. Internally RIN is connected to the L bus and ROUT to the Z bus. Externally SD0-SD7 gives access to RIN and ROUT.

The $\overline{CS}$ input selects the mail box (RIN, ROUT, MBS) in the host system addressing space while the RS input selects RIN-ROUT or MBS. The (SR/W, $\overline{SWR}$) and ($\overline{SDS}$, $\overline{SRD}$) inputs synchronize and control the exchanges on the system bus. These signals are programmable (AMR bit 7) in order to be directly compatible with MOTOROLA or INTEL hosts.

MBS REGISTER : MAILBOX STATUS REGISTER (6-BIT - R/W)

Name	Bit #	Function	Description
RIE	5	Register Input Empty	Input FIFO Empty
RIF	4	Register Input Full	Input FIFO Full
RISH	3	Register Input DSP/host	Input to processor/host indicates to which input mailbox belongs to.
ROE	2	Register Output Empty	Output FIFO Empty
ROF	1	Register Output Full	Output FIFO Full
ROSH	0	Register Output DSP/host	Output to processor/host indicates to which mailbox belongs to.

Figure 7 : Input/output Functions.



4.5.2. LOCAL BUS. On this 16-bit bus (16-bit data, 16-bit address) the ST18940/41 can access external memories or peripherals. To access slow devices, the DSP can stretch its external memory cycle by the insertion of wait states. This can be achieved using either of the two following methods :

-Hardware mechanism : the external memory or peripherals generates a DTACK pulse to signal the end of the exchange

-Programmable multicycle exchanges : the exchange lasts for the number of cycles programmed by the ES0 and ES1 bits of the Access Mode Register. Easy implementation of multiprocessor application using the local bus is allowed by mean of the HOLD function. External devices can take control of the local bus by using the HOLD and HOLDA pins.

-AMR REGISTER : ACCESS MODE REGISTER (8 - BIT, R/W)

Name	Bit #	Functions	Description
I/M	7	Intel/MOTOROLA Format System Bus	Must be set according to the host control : ($\overline{RD}$, $\overline{WR}$) or (SDS, SW/R)
MASK	6		When this bit is set, an interrupt will reset the AMR bits : ES0, ES1, DTACKEN, CSS0, CSS1 (at the end of the interrupt routine, previous AMR state is automatically restored).
DPIF	5	Dual Purpose Interface	DPI Function Selection (serial I/O or DMA)
CSS1 CSS0	4 3	Control Signal Selection	Select one of the three possible sets of control signals on the local bus.
DTACKEN	2	DTACK Enable	DTACK Validation
ES1 ES0	1 0		Exchange speed (1 to 4 cycles)

4.5.3. PARALLEL INTERFACE. The P port is a general purpose 8-bit port, where each bit is programmable as input or as output by means of the DDR 8-bit register. In addition each bit can be used as an external test condition in a branch instruction or as an interrupt source. Four bits (P0-P3) are edge sensitive and four bits (P4-P7) are level sensitive.

4.5.4. DMA CHANNEL. The DMA channel controls transparent exchanges on the local bus between internal XRAM, YRAM or ERAM and an external device.

Single and burst modes are provided. In single mode, the exchange is processed word by word and synchronized by the DMARQ signal (edge sensitive). In burst mode, the exchange is carried out on a block basis with the number of words to be transferred stored in CDMA (13-bit register). In this case the DMARQ is level sensitive and the end of the exchange is indicated by the assertion of the DMAEND signal. The DMA channel is accessed through four pins of DPI port (Dual Purpose interface) and is programmed by the three following registers :

-SDMA REGISTER : STATUS DMA (6 - BIT-R/W)

Name	Bit #	Functions	Description
DMEND	5		End of DMA
O/I	4		DMA as Input or Output
E	3		DMA with ERAM
Y	2		DMA with YRAM
X	1		DMA with XRAM
B/S	0		Burst/single Mode

ADMA Register (13-bit-R/W) : contains the DMA address

TDMA Register (16-bit-R/W) : DMA data buffer

4.5.5. SERIAL I/O. This serial port provides 2 bidirectional lines DA and DB programmable as input or output to give access to the receive or to the transmit part of the port.

Four pins are dedicated to clock and synchronization :

-BCLKX and BCLKR : Transmit and Receive Clocks Frequency equals to single or double the data rate.

-FSX and FSR : Frame synchro pulse.

These four signals can be internally or externally generated.

-Transmitted and received words can be programmed to 8 or to 16 bits (XWL-RWL).

-In one frame several words can be transmitted or received. XS0-XS5 (resp. RS0-RS5) indicate the starting time slot for the transmit (resp. receive) part, XE0-XE5 (resp. RE0-RE5) indicate the ending time slot for the transmit (resp. receive) part.

-The serial port shares 4 pins with the DMA channel controller.

-Direct interfacing with serial devices (such as CODEC, ISDN...) is provided.

-SIN - Serial Input Register (8 - 16-bit - Read)

-SOUT - Serial output Register (8 - 16-bit - Write).

SSR - SERIAL STATUS REGISTER (16-bit - R/W)

Name	Bit #	Functions
XEI	15	Transmit - Interrupt Enable
XRE	14	Transmit - Interrupt (SOUT empty)
XER	13	Transmit - Underspeed Error
XEN	12	Transmit - Enable
XWL	11	Transmit - Word Length (8 or 16)
XF	10	Transmit - Frequency
XDL	09	Transmit - Delay Synchro
XCS	08	Transmit - Internal Clock
REI	07	Receive - Interrupt Enable
RRF	06	Receive - Interrupt (SIN full)
RER	05	Receive - Overspeed Error
REN	04	Receive - Enable
RWL	03	Receive - World Length (8 or 16)
RF	02	Receive - Frequency
RDL	01	Receive - Delay Synchro
RCS	00	Receive - External Clock

XCR - TRANSMIT CONTROL REGISTER (15-bit - R/W)

Name	Bit #	Functions
XZ	14	Level 1 High Impedance
XV	13	Output Buffer Enable
X A/B	12	Transmit on DA or DB
XEO-XE5	06-11	Time Slot # End of Transmit
XSO-XS5	00-05	Time Slot # Start of Transmit

RCR - RECEIVE CONTROL REGISTER (13-bit - R/W)

Name	Bit #	Functions
R A/B	12	Receive on DA or DB
REO-RE5	06-11	Time Slot # End of Receive
RSO-RS5	00-05	Time Slot # Start of Receive

CRC - CLOCK CONTROL REGISTER(16-bit - R/W)

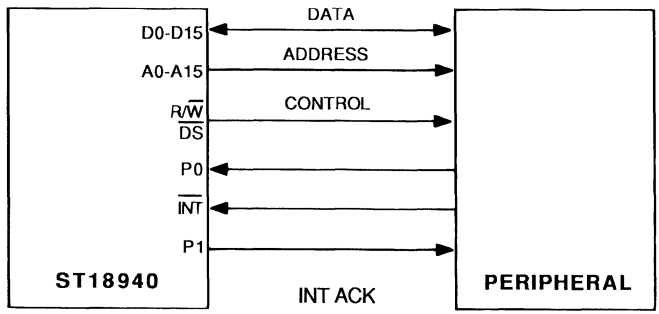
Name	Bit #	Functions
Reserved	15	Reserved
T0-T5	09-14	Frame Synchro Frequency
PSC	08	Prescaler 1/8
CDO-CD7	00-07	Internal Clock Division Range

5. SYSTEM CONFIGURATIONS

5.1. MINIMUM APPLICATION (ST18940 + peripherals)
The ST18940/41 input/output architecture has been designed to support a wide variety of peripherals types, speeds, and organizations without the use of additional circuit chips (glue chip). A minimum application consists of one processor connected to one peripheral.

The following examples show the method to interface several types of peripherals with the ST18940.

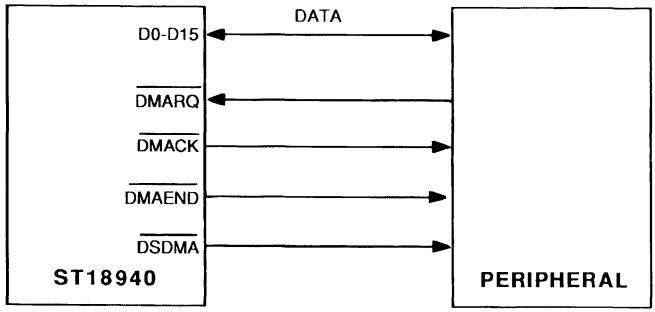
5.1.1. PERIPHERAL ON LOCAL BUS.



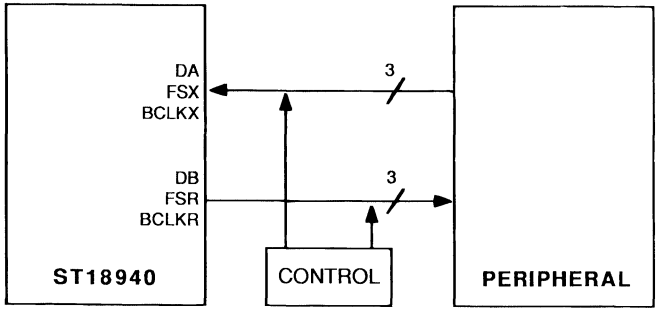
The peripheral can be A/D converter, parallel CODEC...
Exchange can be initialized by interrupt or polling (branch condition).

* (R/$\overline{W}$, $\overline{DS}$) can be changed to ($\overline{RD}$, $\overline{WR}$) signals.

5.1.2. PERIPHERAL ON DMA CHANNEL, DPI PORT.

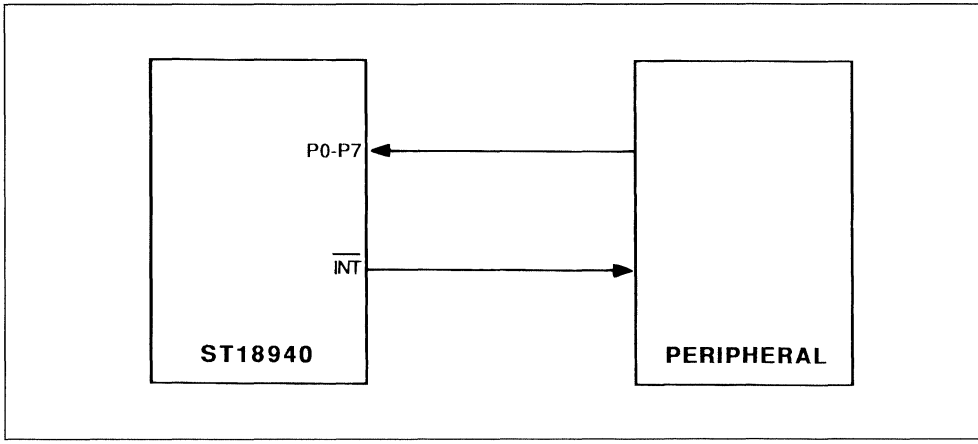


5.1.3. PERIPHERAL ON SERIAL PORT (TYPICAL APPLICATION - SERIAL CODEC)



Several peripherals can be connected, assuming they use different time - slots (up to 64)

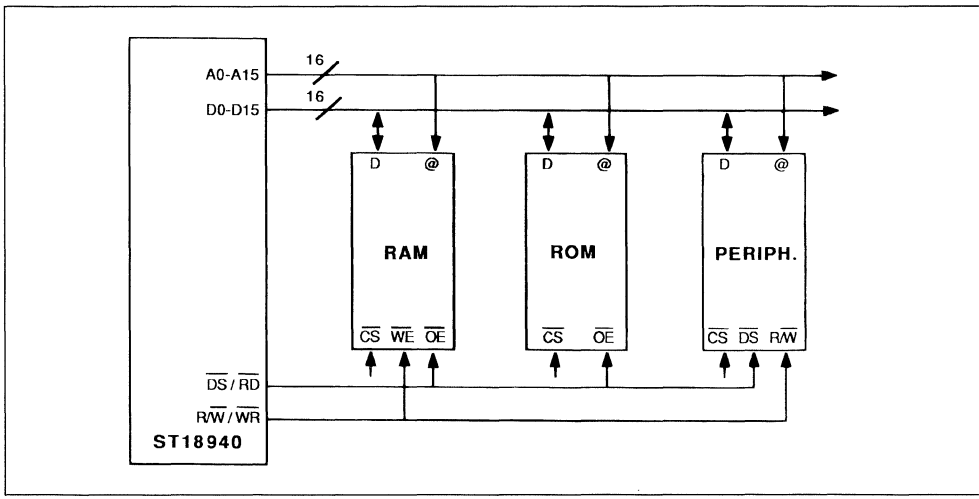
5.1.4. PERIPHERAL ON PARALLEL PORT.



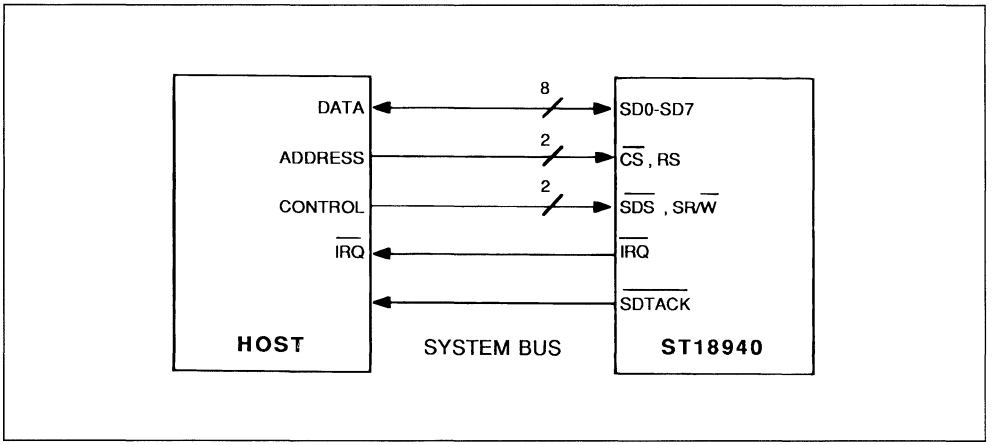
5.2. BUS EXTENSION

The external double-bus architecture is well suited for connections to memory extensions or to a host computer. The system bus/mailbox is intended for communication with other procesors while the local bus is designed for flexible straightforward memory extension interfacing.

5.2.1. EXTENSION ON LOCAL BUS.



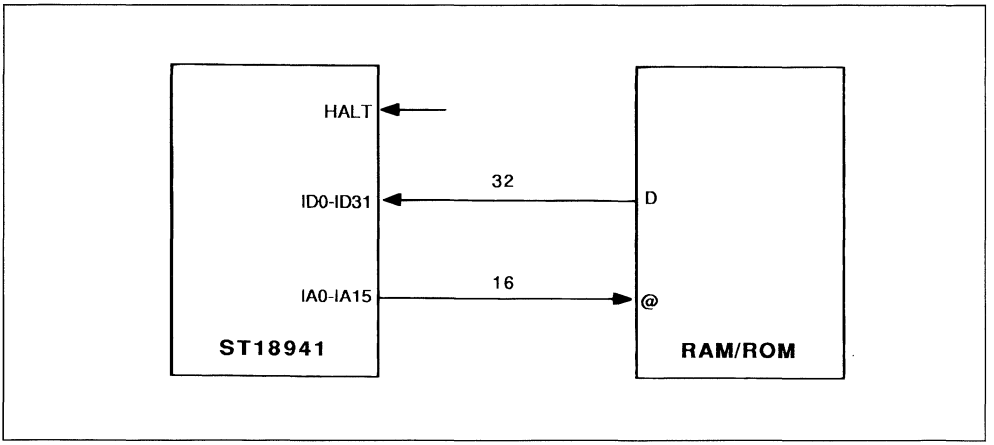
5.2.2. HOST PROCESSOR INTERFACE ON SYSTEM BUS.



* ($\overline{SDS}$, SR/$\overline{W}$) can be changed to ($\overline{SRS}$, $\overline{SWR}$) signals.

5.3. SPECIFIC APPLICATION WITH ST18941 (ROMLESS VERSION)

The ST18941 (open version) provides a dedicated PROGRAM MEMORY INTERFACE bus to access 64K x 32-bit of external program memory without any additional logical glue.



6. SOFTWARE

6.1. INSTRUCTION FORMAT

The instruction set is divided into 5 instruction types :

* calculation instruction	:	OPIM	with immediate addressing
		OPIN	with indirect addressing
		OPDI	with direct addressing
* shift instruction	:	SHIFT	with direct addressing
* transfer instruction	:	TFR	with direct addressing
* branch instruction	:	BRI	Immediate branch
		BRC	Computed branch
* Initialization instruction	:	PINI	Pointer initialization
		RINI	Register initialization

By virtue of the parallel architecture, each instruction controls a number of concurrent operations. The instruction format is divided into a number of fields, which can be used to specify source and destination and operation type for the 4 resources : Zbus, Lbus, Rbus and ALU.

Typical instruction format :

<instr. mnemonioc>, <Z bus field>, < bus field>, <bus field>, <ALU field>

Typical field :

<mnemonic>, and < sources>, and <destinations>

All instructions (except control instructions) are executed in 1 machine cycle (100ns) in REAL mode. All instructions are executed in 2 machine cycles (200ns) in complex and double-precision modes.

In all three modes, every instruction occupies 1 single word (32-bit) of program memory.

6.2. INSTRUCTION SET

6.2.1. ALU CODES. The ALU code is used with calculation instructions (section 6.3.2). Enhanced shift operations are available with the shift instruction (section 6.3.3).

Table 2 : List of Alu Codes.

Type	Mnemonic	Function
ADD	ADD	Addition
	ADDC	Addition with Carry
	ADDS	Addition with L side operand shifted by N bits.
	ADDX	Add the complex conjugate of L-side.
SUB	SBC	Substract with Carry
	SBCR	Reversed substract with carry (Rside - Lside).
	SUB	Substract Lside - Rside
	SUBR	Substract R side - L side
	SUBS	Substract with L side operand shifted by N bits.
LOGIC	AND	Logical AND
	COM L or R	Complement R side or L side
	XOR	Exclusive OR
	OR	Inclusive OR
SHIFT	ASL	Arithmetic Shift Left
	ASR	Arithmetic Shift Right
	LSL	Logical Shift Left
	LSLB	Logical Shift Left of 8 Positions
	LSR	Logical Shift Right
	LSRB	Logical Shift Right of 8 Positions
	ROR	Rotate
RC	RCE	Execute RC
	RCER	Execute and replace RC.
	RCR	Load RC
MISCELLANEOUS	ABS	Absolute Value
	CLR	Clear
	NOP	no Operation
	SET	Set to One
	LCCR	Load L Bus into CCR Register
	TRA L or R	Transfer operation from L side or R side.
	EDGE	Edge Transition for Binary Point Detection

6.2.2. CALCULATION INSTRUCTION. The three instruction types OPIM, OPDI, OPIN have the same structure but differ in terms of addressing mode. OPIM is for use with immediate addressing on R source operands. OPDI is for use with direct addressing on L source operands. OPIN is for use with indirect addressing on all operands. With the exception of some shift operations, the calculation instructions are the only instructions providing access to the ALU codes.

Instruction structures are given below for each class.

Detailed information is provided in the user's manual and in the programming reference card.

OPIN	Z Field		L Field		R Field		ALU Code Source Dest.
	Source	Dest.	Source	Dest.	Source	Dest.	
	(1)	Indirect	Indirect	(2)	Indirect	(2)	

Most of the typical DSP algorithms are implemented on the ST18940-41 system using OPIN class instructions.

OPDI	Z Field		L Field		R Field		ALU Code Source Dest.
	Source	Dest.	Source	Dest.	Source	Dest.	
	(1)	Indirect	Direct	(2)	Indirect	(2)	

OPIM	Z Field	L Field		R Field		ALU Code Source Dest.
	NOT AVAILABLE	Source	Dest.	Source	Dest.	
		Indirect	(2)	Value	(2)	

(1) Sources of the Z field are typically selected from the set of options : ALU output (D register), accumulators A1, B1, A2, B2 and FIFO.
(2) Destinations of the Lbus and Rbus are typically the multiplier input registers and the ALU inputs (which are not latched).

6.2.3. SHIFT INSTRUCTIONS. The shift instruction allows access to barrel shifter operations with programmable shift values.

SHIFT CODE	SHIFT VALUE	L Bus		Z Bus	
		Source	DEST.	Source	DEST.
		Direct	(2)	(1)	Indirect

6.2.4. TRANSFER INSTRUCTION. The transfer instruction TFR is used to move data through the Z bus. All internal registers can be accessed in read and write through the Z bus.

TFR	Z Bus		
	Source	DESTINATION 1	DESTINATION 2
	Register	Register	Direct

6.2.5. BRANCH INSTRUCTION. The branch address for conditional branch operations may be immediate or computed. In the latter case the new PC value may be loaded from accumulators A, B, FIFO or the T register. Twenty three conditions can be tested (Condition Code Register, mailbox and DMA flags, and PPORT).

BRANCH	Branch	Branch Address Immediate or Computed	PC Save Operations Z Bus	
			Source	DESTINATION
	Conditions		PC	Indirect

The "PC save" field allows stack extension in data memory (either internal or external) with a minimum execution time overhead.

6.2.6. INITIALIZATION INSTRUCTIONS. The PINI instruction is used for pointer initialization. In addition to mode setting, PINI instruction provides initialization of 2 address pointers in one cycle.

PINI	Mode	Field 1		Field 2	
		Immediate Value	Register or Resource	Immediate Value	Register or Resource

The RINI instruction is used to initialize index address registers, DMA registers, loop counters as well as the bits of the status (STA register).

RINI	Value	Register	Register
		Dest. 1	Dest. 2

Note : Two registers cannot be initialized in the same RINI instruction. Only one register of class 1 or 2 can be initialized within a single instruction.

6.3. PROGRAMMING EXAMPLE

OPIN ST B [E0] + K ; LDL [X0] + L M ; LDR [Y0] - K N ; ADDS P A, A\

OPIN	Instruction type
ST B [E0] + K	Z field : B is stored into ERAM location addressed by E0. The next E0 value will be E0 + KE
LDL [X0] + L M	L field : XRAM location addressed by X0 is transferred via the LBUS and stored in the MULTIPLIER input M. The next X0 value will be X0 + LX
LDR [Y0] - K N	R field : YRAM location addressed by Y0 is transferred via the RBUS and stored in the MULTIPLIER input N. The next Y0 value will be Y0 - KY
ADDS PA, A	ALU field : product scaled by BARREL SHIFTER (shift value given by BSC) is added to previous value of A, result is stored into A.

7. ELECTRICAL SPECIFICATIONS

7.1. DC ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}*	Supply Voltage	– 0.3 to 7.0	V
V_{in}*	Input Voltage	– 0.3 to 7.0	V
T_A	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C
P_{Dmax}	Maximum Power Dissipation	0.8	W

* With respect to V_{SS}.

Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

7.2. DC ELECTRICAL CHARACTERISTICS

Conditions : V_{CC} ± 10%, Ambient Temperatures = 0°C to 70°C

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply	4.5	5	5.5	V
V_{IL}	Input Low Level	– 0.3		0.8	V
V_{IH}	Input High Level	2.4		V_{CC}+0.3	V
I_{in}	Input Leakage Current	– 10		10	µA
V_{OH}	Output High Level (I_{OH} = 300µA)	2.7			V
V_{OL}	Output Low Level (I_{OL} = 2mA)			0.5	V
P_D	Power Dissipation		0.5		W

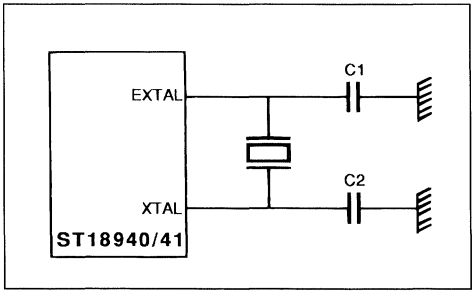
7.3. CLOCK CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_X	Frequency	5		20	Mhz
	C1, C2		10		pF

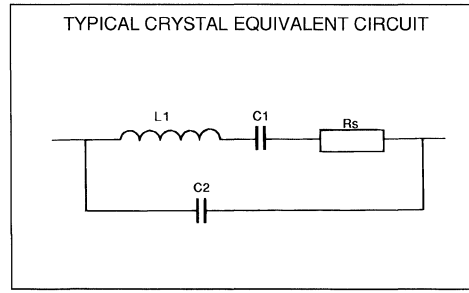
The CKLOUT frequency is half the crystal operating frequency.

INTERNAL CLOCK OPTION

A crystal can be connected across XTAL and EXTAL functioning in the parallel resonant fundamental mode, AT – cut.



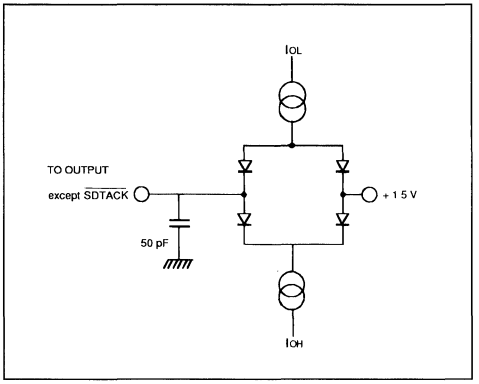
C1, C2 TYPICAL VALUE = 10 PF

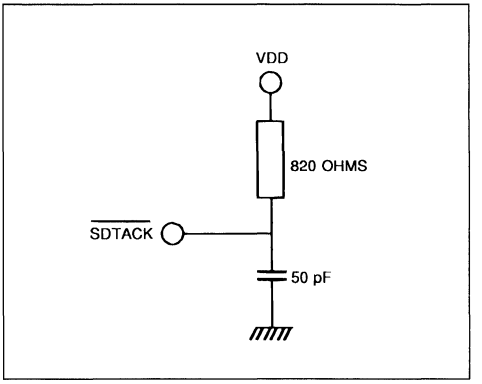


TYPICAL VALUES :
RS = 10 OHMS C2 = 4 PF
C1 = 0.02 PF Q > 30 K

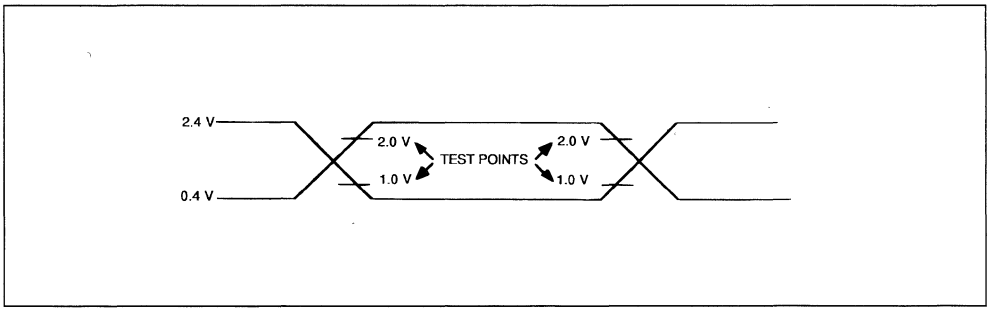
7.4. AC MEASUREMENT CONDITIONS

OUTPUT LOAD





AC TESTING INPUT, OUTPUT WAVEFORM

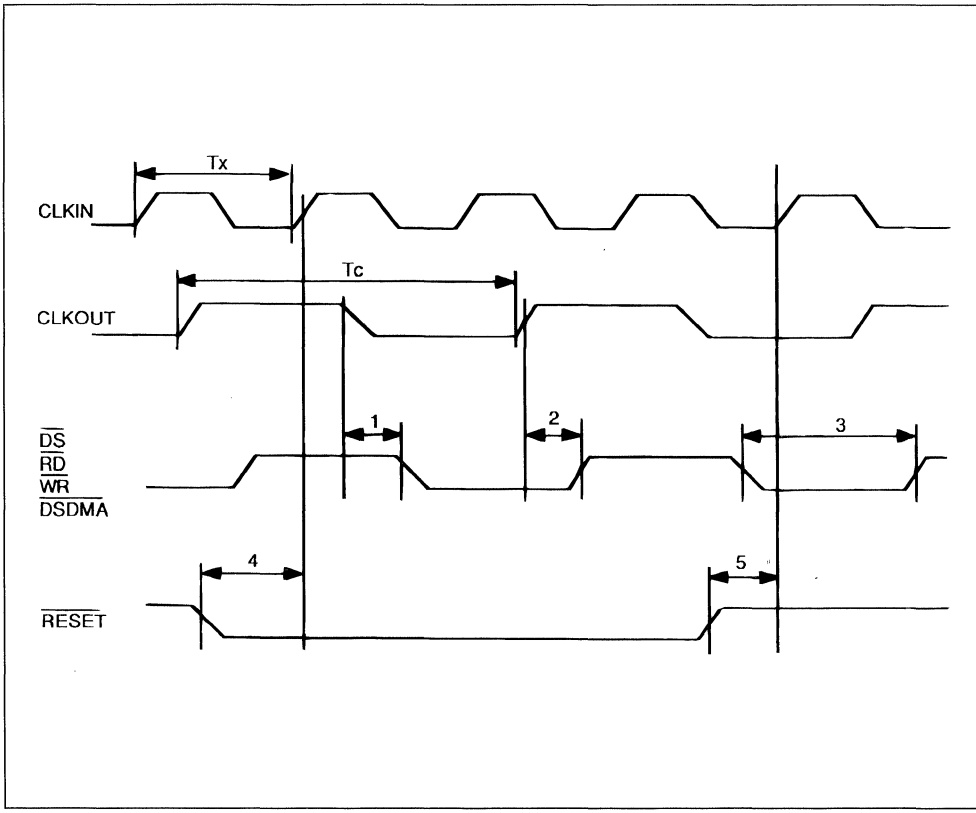


AC TESTING INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.4V FOR A LOGIC "0".
TIMING MEASUREMENTS ARE MADE AT 2V FOR A LOGIC "1" AND AT 1.0V FOR A LOGIC "0".

7.5. EXTERNAL CLOCK OPTION

Num.	Parameter	Min.	Typ.	Max.	Unit
TX	Period	50		200	ns
	Duty Cycle	40		60	%
	Rise Time			5	ns
	Fall Time			5	ns
T_C	CLKOUT Period		$2xT_X$		ns
1	$\overline{DS}$ Low to CLKOUT Delay	− 5		+ 5	ns
2	$\overline{DS}$ High to CLKOUT Delay	− 5		+ 5	ns
3	$\overline{DS}$, $\overline{RD}$, $\overline{WR}$, $\overline{DSDMA}$ Low Level		$T_C/2$		ns
4, 5	$\overline{RESET}$ Set up	15			ns

Conditions : V_{CC} = 5.0V ± − 10%, V_{SS} = 0V, T_A = 0 to 70°C.

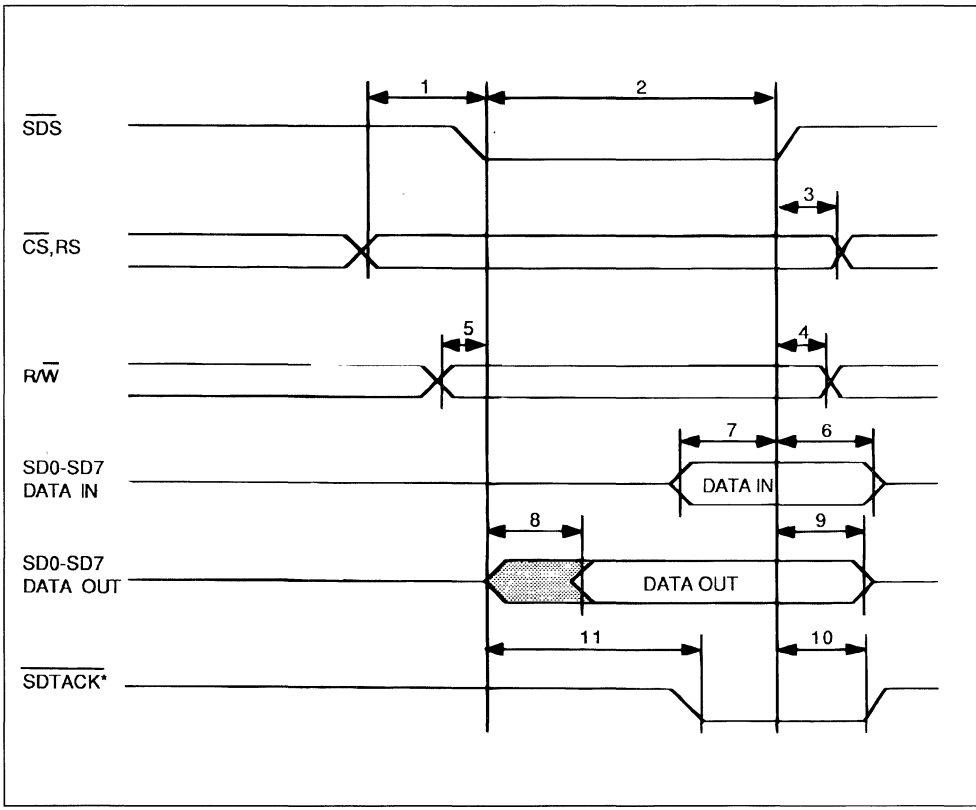


7.6. SYSTEM BUS TIMING

Num.	Parameter	Min.	Max.	Unit
2	$\overline{SDS}$, $\overline{SRD}$, $\overline{SWR}$ Pulse Width	40		ns
1	Address to $\overline{SDS}$ Setup	15		ns
3	Address to $\overline{SDS}$ Hold	5		ns
5	R/$\overline{W}$ to $\overline{SDS}$ Setup	15		ns
4	SR/$\overline{W}$ to $\overline{SDS}$ Hold	5		ns
7	Data in to $\overline{SWR}$, $\overline{SDS}$ Setup	15		ns
6	Data in to $\overline{SWR}$, $\overline{SDS}$ Hold	5		ns
8	Data out to $\overline{SRD}$, $\overline{SDS}$ Delay		25	ns
9	Data out to $\overline{SRD}$, $\overline{SDS}$ Hold	5	25	ns
11	$\overline{SDTACK}$ to $\overline{SRD}$, $\overline{SWR}$, $\overline{SDS}$ Delay		25	ns
10	$\overline{SDTACK}$ to $\overline{SRD}$, $\overline{SWR}$, $\overline{SDS}$ Hold	5	50	ns

Conditions : V_{CC} = 5.0V ± 10%, V_{SS} = 0V, T_A = 0 to 70°C.

SYSTEM BUS TIMINGS

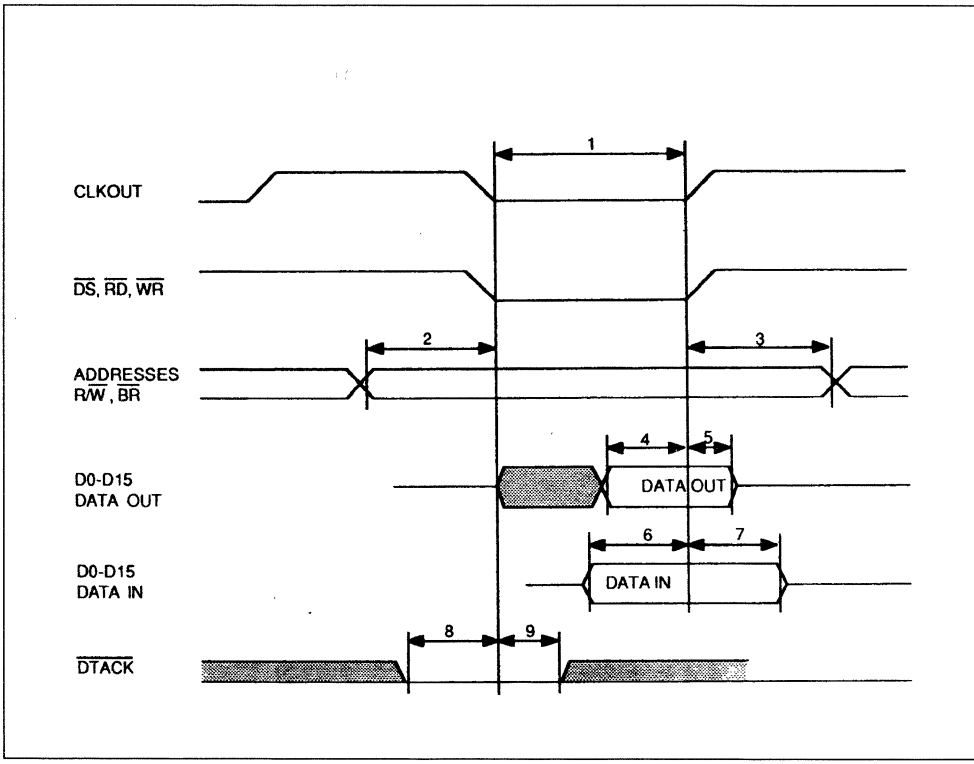


Note : $\overline{SDTACK}$ is an open drain output.

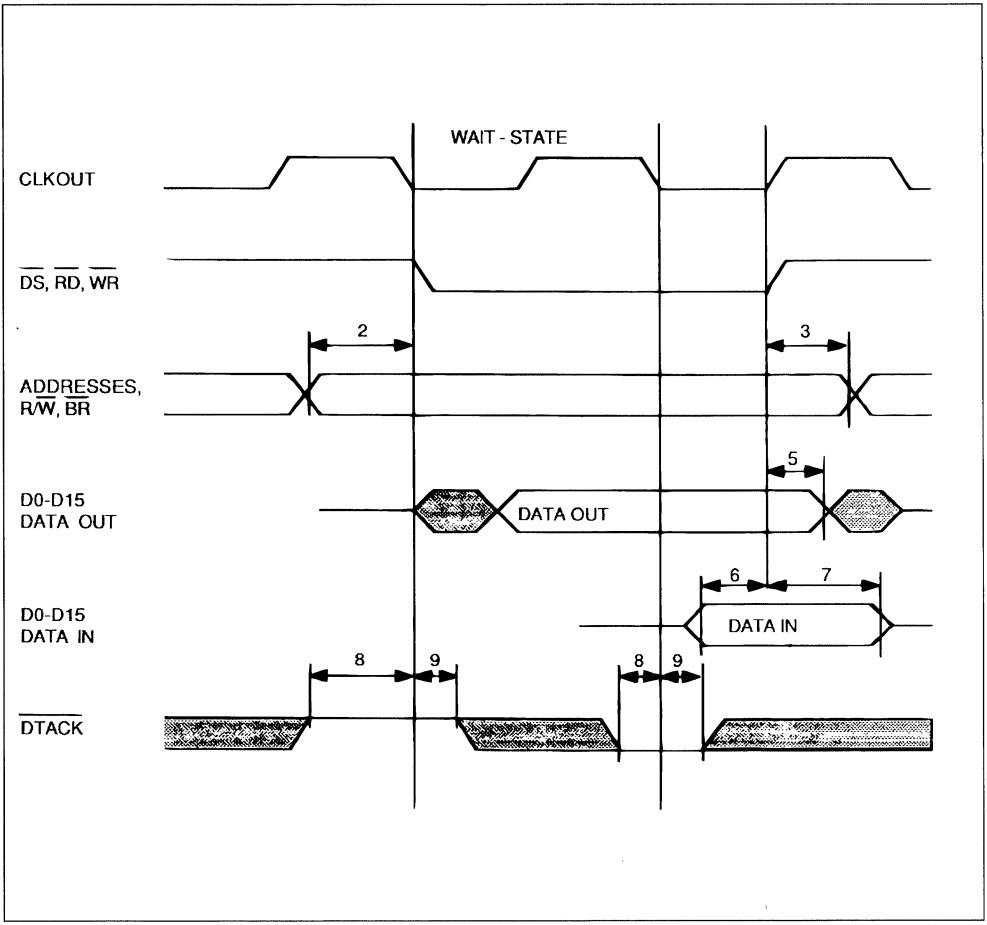
7.7. LOCAL BUS TIMING

Num.	Parameter	Min.	Max.	Unit
1	$\overline{DS}$, $\overline{RD}$, $\overline{WR}$ Pulse Width	$T_C/2$-10	$T_C/2$	ns
2	Address to $\overline{DS}$, $\overline{RD}$, $\overline{WR}$ Delay	$T_C/2$-25		ns
3	Address to $\overline{DS}$, $\overline{RD}$, $\overline{WR}$ Hold	5		ns
4	DATA to $\overline{DS}$, $\overline{WR}$ Delay Write	$T_C/2$-25		ns
5	DATA to $\overline{DS}$, $\overline{WR}$ Hold Write	5	25	ns
6	DATA to $\overline{DS}$, $\overline{RD}$ Setup Read	15		ns
7	DATA to $\overline{DS}$, $\overline{RD}$ Hold Read	5		ns
8	$\overline{DTACK}$ to CLKOUT Delay	15		ns
9	$\overline{DTACK}$ to CLKOUT Hold	15		ns

7.7.1. LOCAL BUS TIMING WITHOUT WAIT STATE



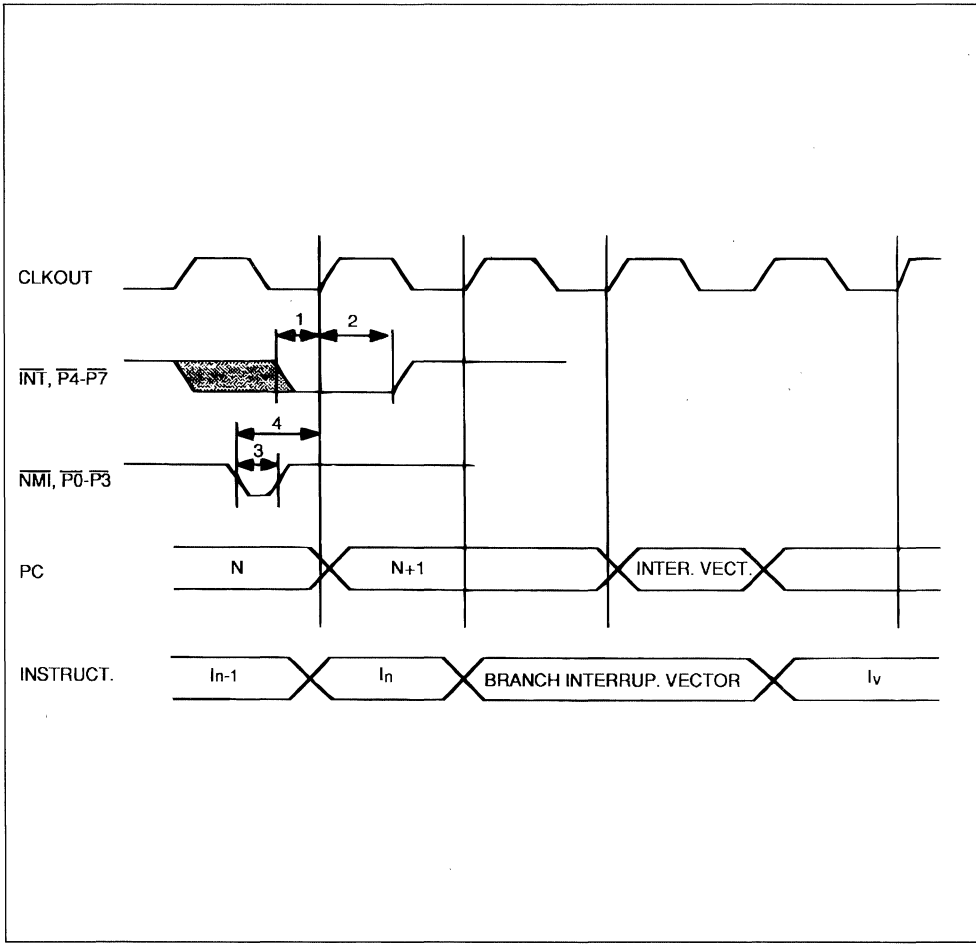
7.7.2. LOCAL BUS TIMING WITH WAIT - STATE



7.8. INTERRUPT TIMING

Num.	Parameter	Min.	Max.	Unit
1	$\overline{INT}$, $\overline{P4}$-$\overline{P7}$ to CLKOUT Setup	20		ns
2	$\overline{INT}$, $\overline{P4}$-$\overline{P7}$ to CLKOUT Hold	5		ns
4	$\overline{NMI}$, $\overline{P0}$-$\overline{P3}$ to CLKOUT Setup	15		ns
3	$\overline{NMI}$, $\overline{P0}$-$\overline{P3}$ to CLKOUT Hold	10		ns

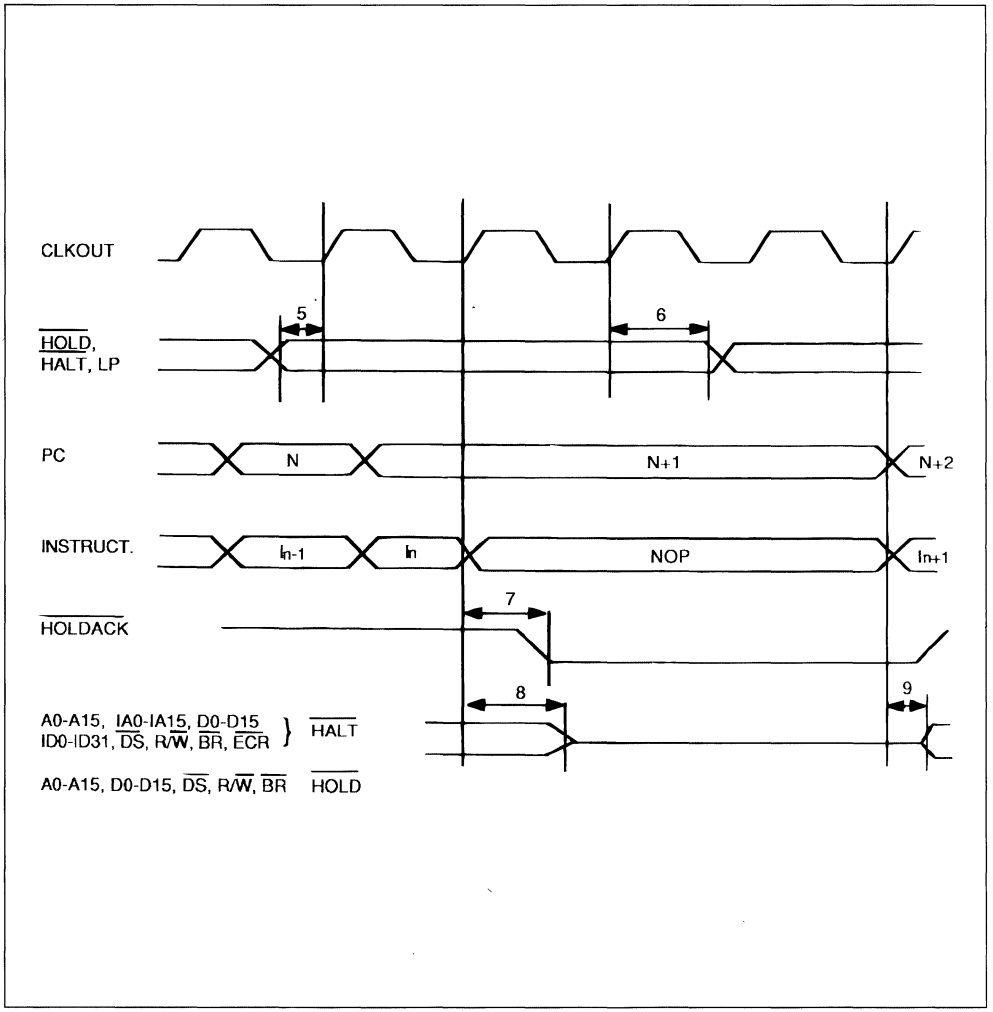
Conditions : V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.



7.9. $\overline{HOLD}$, LP, $\overline{HALT}$ TIMING

Num.	Parameter	Min.	Max.	Unit
5	$\overline{HOLD}$ to CLKOUT Setup	20		ns
6	$\overline{HOLD}$ to CLKOUT Hold	5		ns
7	CLKOUT High to $\overline{HOLDACK}$ Low		30	ns
8	CLKOUT High to HI-Z	5	30	ns
9	CLKOUT High to Valid	0	5	ns

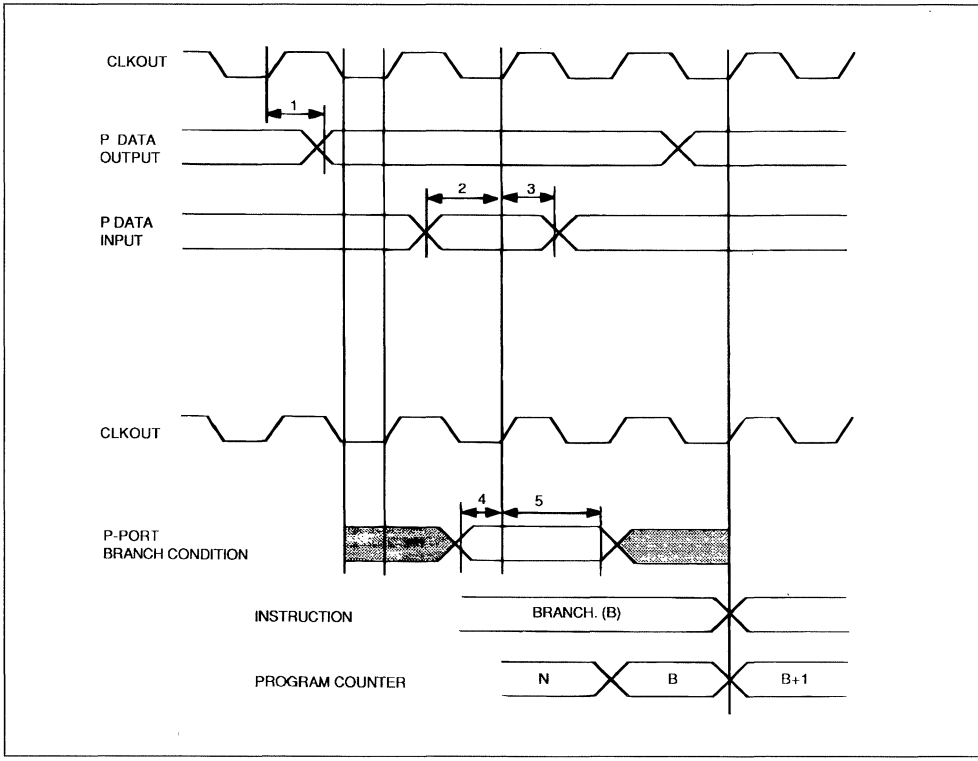
Conditions : V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.



7.10. P-PORT TIMING

Num.	Parameter	Min.	Max.	Unit
1	CLKOUT to High to P0:7 Valid		30	ns
2, 4	P0:P7 to CKLOUT Setup	20		ns
3, 5	P0:P7 to CKLOUT Hold	5		ns

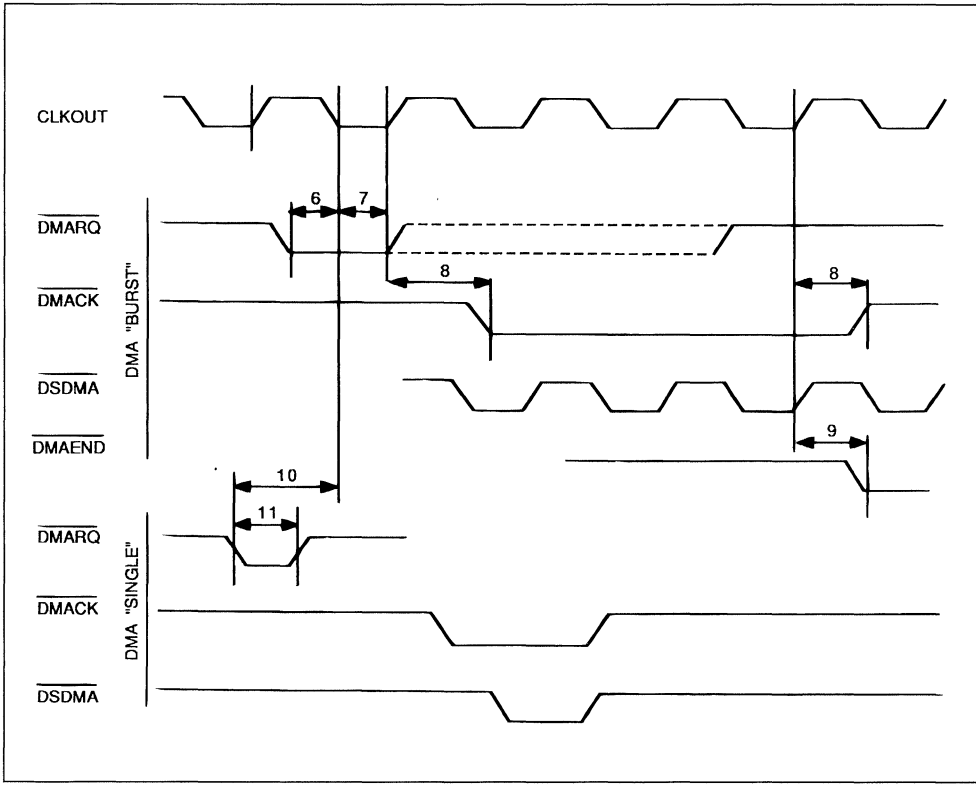
Conditions : V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.



7.11. DMA TIMING

Num.	Parameter	Min.	Max.	Unit
6	$\overline{\text{DMARQ}}$ to CLKOUT Setup	20		ns
7	$\overline{\text{DMARQ}}$ to CLKOUT Hold	5		ns
8	$\overline{\text{DMACK}}$ to CLKOUT Delay		30	ns
9	CLKOUT High to $\overline{\text{DMAEND}}$ Valid		30	ns
10	$\overline{\text{DMARQ}}$ to CLKOUT Setup	40		ns
11	$\overline{\text{DMARQ}}$ Pulse Width	10		ns

Conditions : V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.

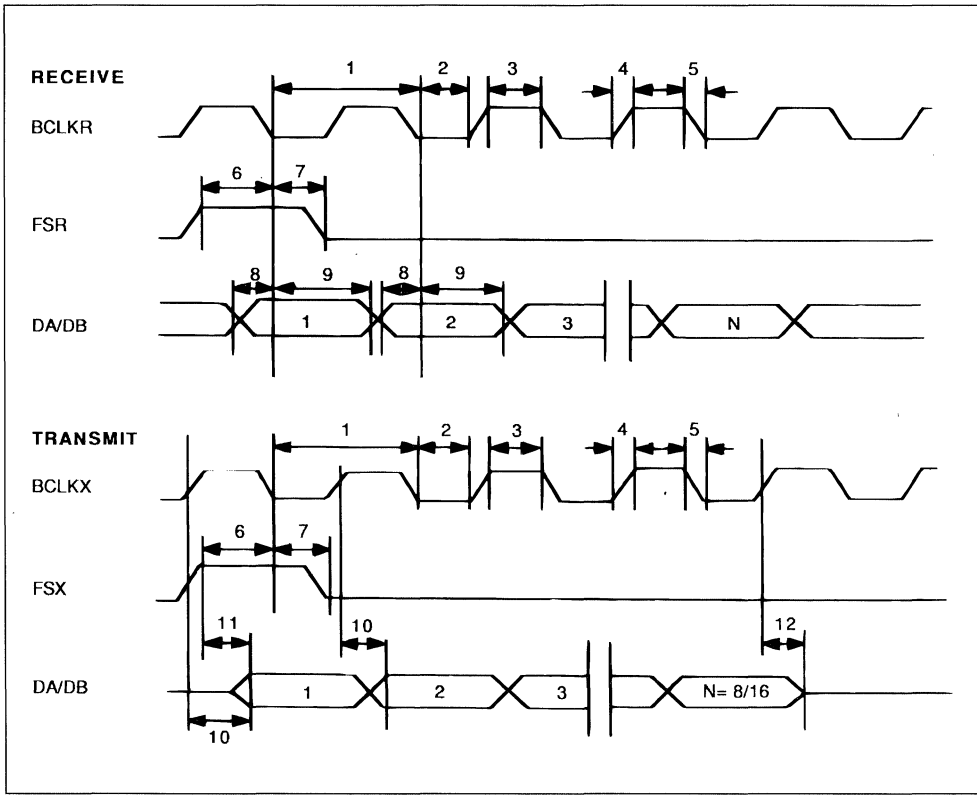


7.12. SERIAL CHANNEL TIMING

Num.	Parameter	Min.	Max.	Unit
1	BCLKR, BCLKX Period	200		ns
2	BCLKR, BCLKX Width Low	80		ns
3	BCLKR, BCLKX Width High	80		ns
4	BCLKR, BCLKX Rise Time		30	ns
5	BCLKR, BCLKX Fall Time		30	ns
6	FSR, FSX to BCLKX, BCLKR Setup	30		ns
7	FSR, FSX to BCLKX, BCLKR Hold	0		ns
8	DA, DB to BCLKR Setup	20		ns
9	DA, DB to BCLKR Hold	0		ns
10	BCLKX High to DA, DB Valid		30	ns
11	FSX High to DA, DB Valid		30	ns
12	BCLKX High to DA, DB-Z	0	30	ns

Serial Channel Timing : Non Delayed Data Mode.
Conditions : V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.

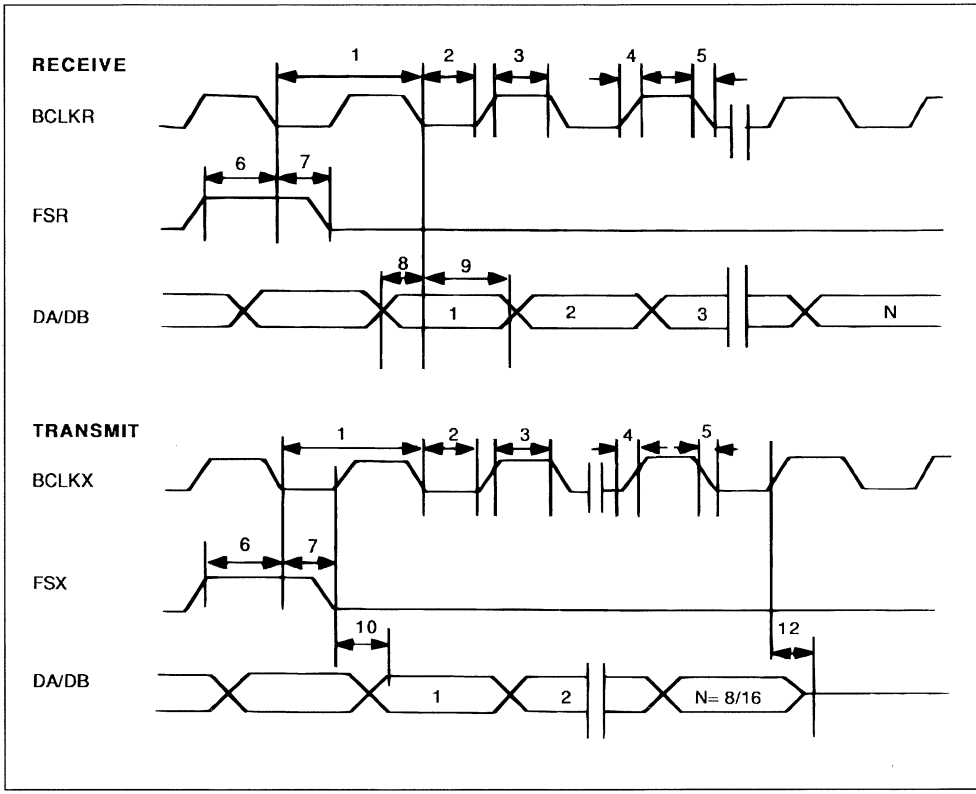
SERIAL CHANNEL TIMING : NON DELAYED DATA MODE



Num.	Parameter	Internal Clock		External Clock		Unit
		Min.	Max.	Min.	Max.	
1	BCLKR, BCLKX Period	200		125		ns
2	BCLKR, BCLKX Width Low	80		50		ns
3	BCLKR, BCLKX Width High	80		50		ns
4	BCLKR, BCLKX Rise Time		30		10	ns
5	BCLKR, BCLKX Fall Time		30		10	ns
6	FSR, FSX to BCLKR, BCLKX Setup	30		30		ns
7	FSR, FSX to BCLKR, BCLKX Hold	0		0		ns
8	DA, DB to BCLKR Setup	20		20		ns
9	DA, DB to BCLKR Hold	0			30	ns
10	BCLKX High to DA, DB Valid		30		30	ns
12	BCLKX High to DA, DB-Z		30		30	ns

Conditions : V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.

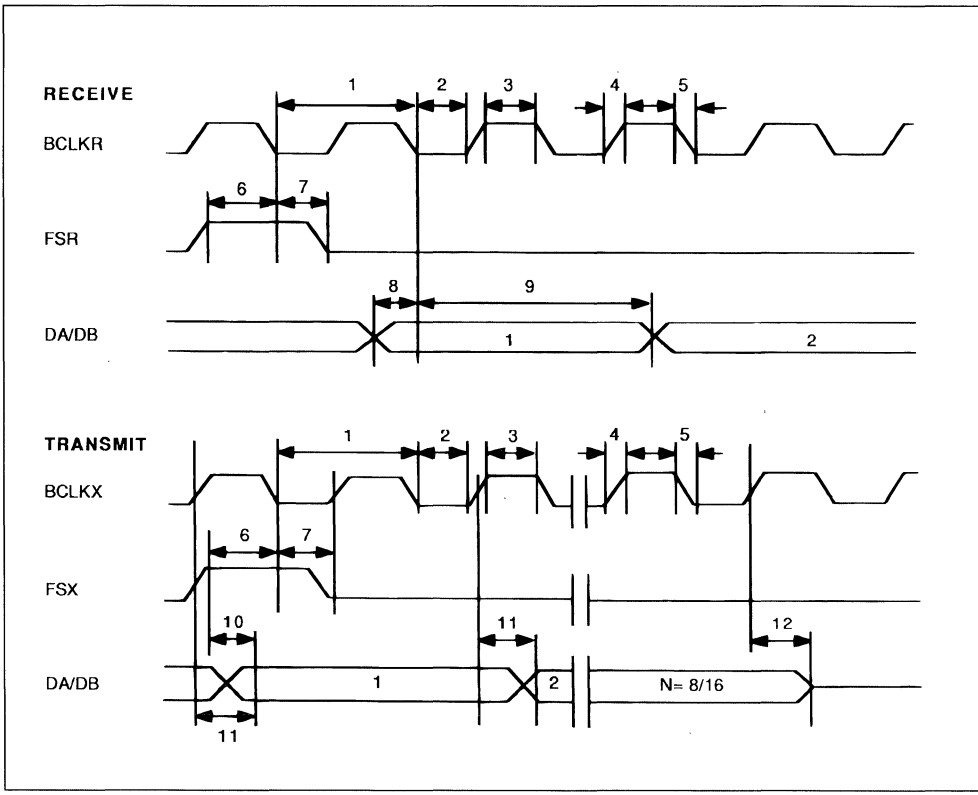
SERIAL CHANNEL TIMING : DELAYED DATA MODE



Num.	Parameter	Internal Clock		External Clock		Unit
		Min.	Max.	Min.	Max.	
1	BCLKR, BCLKX Period	200		125		ns
2	BCLKR, BCLKX Width Low	80		50		ns
3	BCLKR, BCLKX Width High	80		50		ns
4	BCLKR, BCLKX Rise Time		30		10	ns
5	BCLKR, BCLKX Fall Time		30		10	ns
6	FSR, FSX to BCLKR, BCLKX Setup	30		30		ns
7	FSR, FSX to BCLKR, BCLKX Hold	0		0		ns
8	DA, DB to BCLKR Setup	20		20		ns
9	DA, DB to BCLKR Hold	0			30	ns
10	BCLKX High to DA, DB Valid		30		30	ns
11	FSX High to DA, DB Valid		30		30	ns
12	BCLKX High to DA, DB-Z		30		30	ns

Conditions : V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.

SERIAL CHANNEL TIMING : ISDN GCI MODE

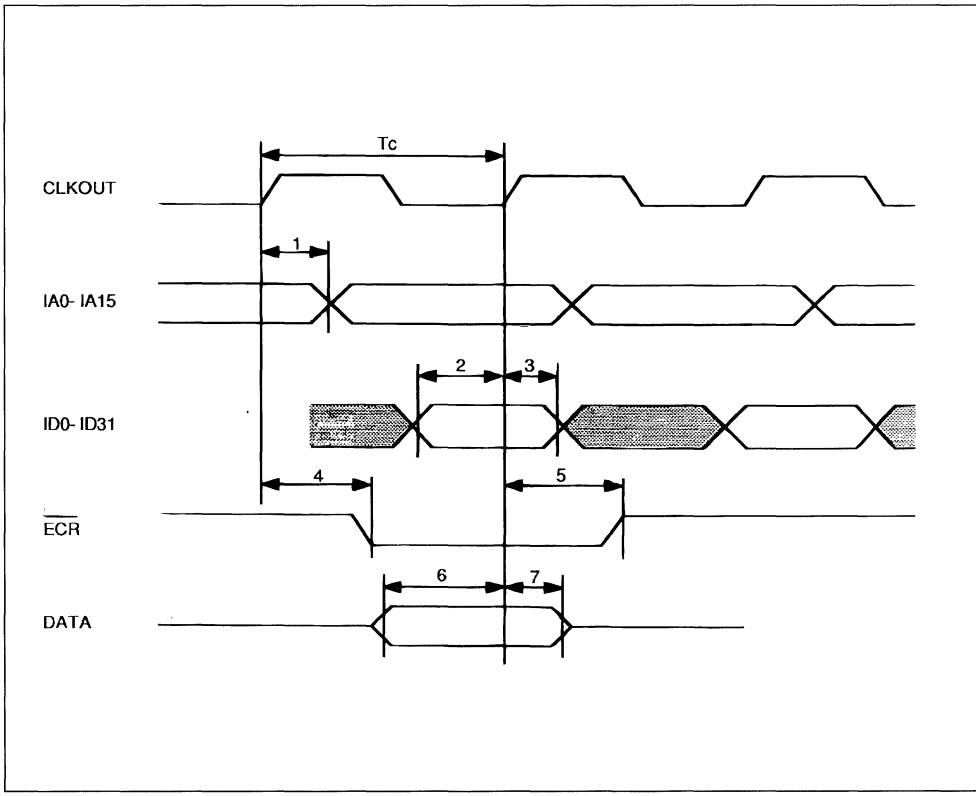


7.13. INSTRUCTION BUS TIMING ST 18941

Num.	Parameter	Min.	Max.	Unit
1	CLKOUT High to Address Valid		25	ns
2	Data to CLKOUT Setup	40		ns
3	Data to CLKOUT Hold	5		ns
4	CLKOUT High to ECR Valid		30	ns
5	$\overline{ECR}$ to CLKOUT Hold	5		ns
6	Data to CLKOUT Setup	15		ns
7	Data to CKLOUT Hold	5		ns
8	CLKOUT High to HI Low Delay	− 5	+ 5	ns
9	CLKOUT Low to HI High Delay	− 5	+ 5	ns

Conditions : V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.

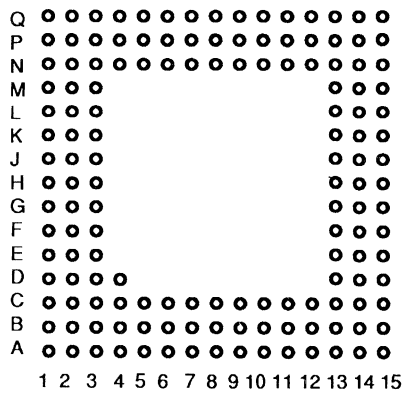
INSTRUCTION BUS TIMING



8. PIN CONNECTIONS

8.1 ST18941 : OPEN VERSION

144-pin Pin Grid Array Ceramic Package



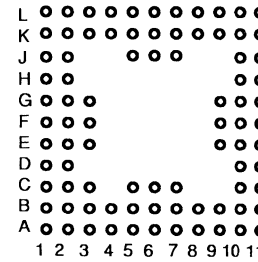
BOTTOM VIEW

ST18941 PIN GRID ARRAY 144-PIN

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A1	SD7	C7	VDD	H13	VSS	N10	ID11
A2	SD3	C8	VSS	H14	DPI1	N11	ID5
A3	CS	C9	D12	H15	DPI0	N12	ID2
A4	SRW / SWR	C10	D8	J1	IA8	N13	ID1
A5	SDS / SRD	C11	D4	J2	IA10	N14	HT2
A6	VDD	C12	VDD	J3	VDD	N15	HOLDA
A7	VDD	C13	A14	J13	DPI4	P1	INT
A8	VSS	C14	A11	J14	DPI5	P2	RESET
A9	D14	C15	A8	J15	DPI2	P3	ID31
A10	D13	D1	P1	K1	IA9	P4	ID29
A11	D10	D2	P5	K2	IA11	P5	ID26
A12	D7	D3	VSS	K3	VSS	P6	ID23
A13	D5	D13	A13	K13	CLKOUT	P7	ID21
A14	D2	D14	A9	K14	DTACK	P8	ID17
A15	D0	D15	A7	K15	DPI3	P9	ID13
B1	P6	E1	IA1	L1	VSS	P10	ID12
B2	SD6	E2	P2	L2	VSS	P11	ID9
B3	SD2	E3	P4	L3	IA15	P12	ID6
B4	SD0	E13	A10	L13	DS / RD	P13	ID4
B5	RS	E14	A6	L14	XTAL	P14	ID0
B6	IRQ	E15	A5	L15	BR	P15	ECR
B7	VDD	F1	IA4	M1	IA12	Q1	LP
B8	D15	F2	IA0	M2	IA14	Q2	ID30
B9	D11	F3	P0	M3	NMI	Q3	ID27
B10	D9	F13	A4	M13	VSS	Q4	ID25
B11	D6	F14	A3	M14	R/W / WR	Q5	ID22
B12	D3	F15	A1	M15	EXTAL	Q6	ID19
B13	D1	G1	IA5	N1	IA13	Q7	ID18
B14	A15	G2	IA2	N2	HALT	Q8	ID16
B15	A12	G3	IA3	N3	INCYCLE	Q9	ID15
C1	P3	G13	VDD	N4	VSS	Q10	ID14
C2	P7	G14	A2	N5	ID28	Q11	ID10
C3	SD5	G15	A0	N6	ID24	Q12	ID8
C4	SD4	H1	IA7	N7	ID20	Q13	ID7
C5	SD1	H2	IA6	N8	VDD	Q14	ID3
C6	SDTACK	H3	VSS	N9	VSS	Q15	HOLD

8.2. ST18940 : MASKED VERSION

84-pin Pin Grid Array Ceramic Package

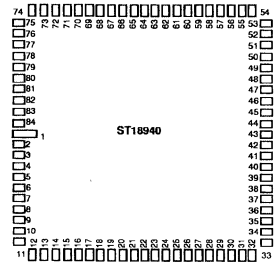


BOTTOM VIEW

ST18940 PLCC 84-PIN

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A1	A9	B11	LP	F9	VSS	L11	SD2
A2	A7	C1	A13	F10	VDD	K2	VSS
A3	A6	C2	A11	F11	P3	K3	D13
A4	A4	C5	A3	G1	D4	K4	IRQ
A5	A1	C6	VDD	G2	D5	K5	RS
A6	A0	C7	XTAL	G3	D6	K6	VSS
A7	CLKOUT	C10	HOLD	G9	P0	K7	DPI1
A8	BR	C11	RESET	G10	P1	K8	DPI4
A9	HOLDA	D1	A15	G11	P2	K9	SD1
A10	DS / RD	D2	A14	H1	D7	K10	VSS
A11	HT2	D10	INT	H2	D8	K11	SD4
B1	A12	D11	P7	H10	SD6	L1	D12
B2	A10	E1	D2	H11	SD7	L2	D14
B3	A8	E2	D1	J1	D9	L3	D15
B4	A5	E3	D0	J2	D11	L4	SDTACK
B5	A2	E9	P6	J5	SDS	L5	SR/W / SWR
B6	VSS	E10	P5	J6	VDD	L6	CS
B7	EXTAL	E11	P4	J7	DPI2	L7	DPI0
B8	DTACK	F1	D3	J10	SD3	L8	DPI3
B9	R/W / WR	F2	VDD	J11	SD5	L9	DPI5
B10	VDD	F3	VSS	K1	D10	L10	SD0

84-pin Plastic Leaded Chip Carrier



TOP VIEW

ST18940 PLCC 84-PIN

PAD	NAME	PAD	NAME	PAD	NAME	PAD	NAME
1	VDD	22	VSS	43	VDD	64	VSS
2	A0	23	D3	44	CS	65	P3
3	A1	24	D4	45	DPI0	66	P4
4	A2	25	D5	46	DPI1	67	P5
5	A3	26	D6	47	DPI2	68	P6
6	A4	27	D7	48	DPI3	69	P7
7	A5	28	D8	49	DPI4	70	INT
8	A6	29	D9	50	DPI5	71	RESET
9	A7	30	D10	51	SD0	72	LP
10	A8	31	D11	52	SD1	73	HOLD
11	A9	32	D12	53	SD2	74	HT2
12	A10	33	VSS	54	VSS	75	VDD
13	A11	34	D13	55	SD3	76	R/W / WR
14	A12	35	D14	56	SD4	77	DS / RD
15	A13	36	D15	57	SD5	78	HOLDA
16	A14	37	IRQ	58	SD6	79	DTACK
17	A15	38	SDTACK	59	SD7	80	BR
18	D0	39	SDS / SRD	60	P0	81	XTAL
19	D1	40	RS	61	P1	82	EXTAL
20	D2	41	SR/W / SWR	62	P2	83	CLKOUT
21	VDD	42	VSS	63	VDD	84	VSS

9. ORDERING INFORMATION

9.1. DEVICE TYPE

Part Number	Operating Temperature Range*	Package Type
ST 18940 CR/PXXX**	0 to + 70°C	84 - pin Ceramic Pin Grid Array
ST 18940 CFN/PXXX	0 to + 70°C	84 - pin Plastic Leaded Chip Carrier
ST 18941 CR	0 to + 70°C	144 - pin Ceramic Pin Grid Array

** XXX is the specific number associated to the customer code.
* for extended temperature range, please consult ST sales offices.

9.2. SOFTWARE TOOLS

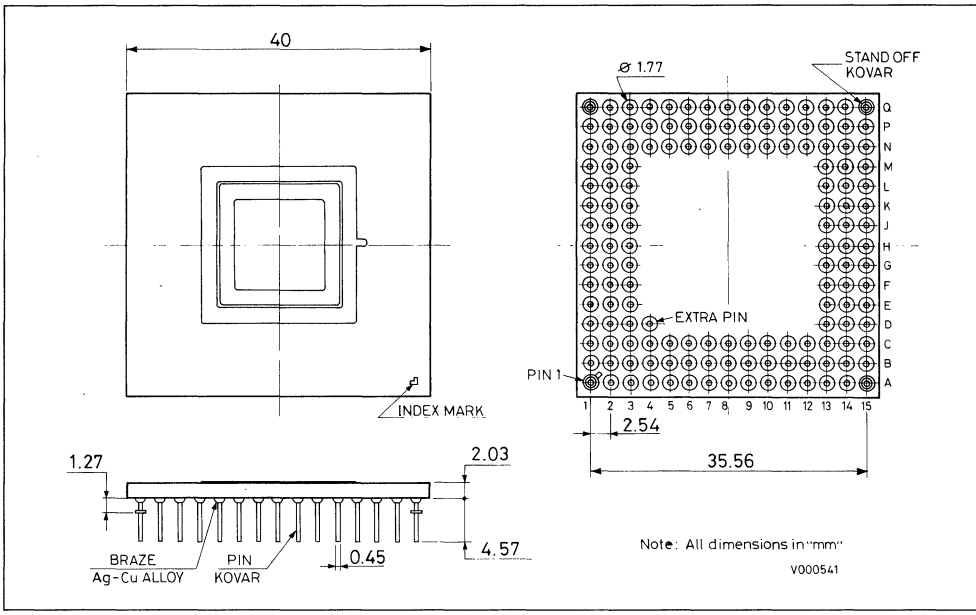
ST 18940 SP-PC	Software Package Including Macroassembler Functionnal Stimulator Linker for PC
ST 18940 SP-VM	Same Software Package for VAX Machines
ST 18940 SPC-PC	Same Software with C-compiler for PC
ST 18940 SPC-VM	Same Software Package with C - Compiler for VAX

9.3. HARDWARE TOOLS

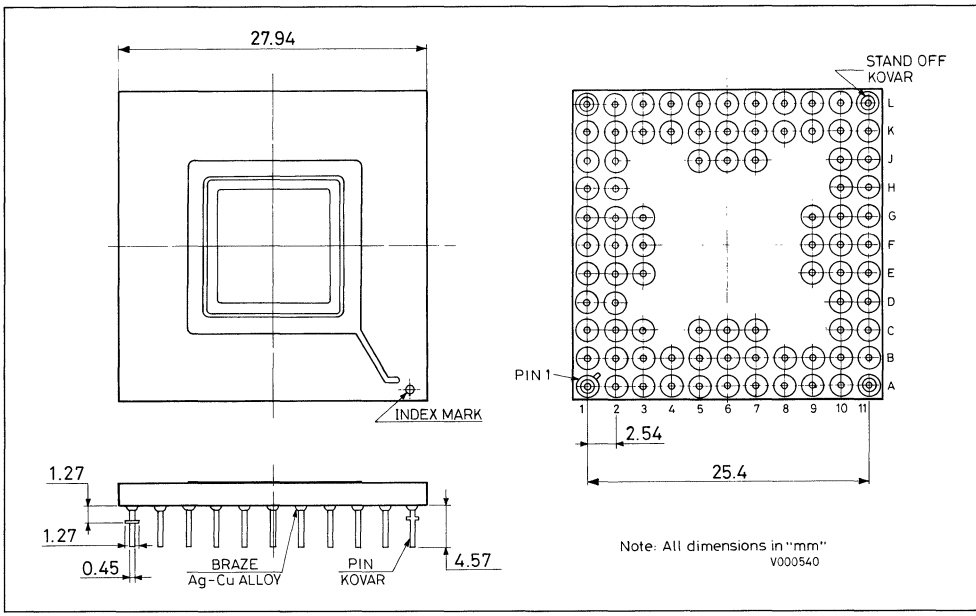
ST 18940 EMU	Stand - Alone Emulator
ST 18940 HDS-110	Hardware Development System 110V Power Supply
ST 18940 HDS-220	Hardware Development System 220V Power Supply
ST 18940 EPROM	EPROM Simulation Module for ST 18940
ST 18940-PC	PC Compatible Emulation Board

10. MECHANICAL DATA

Pin Grid Array 144-pin - ST18941



Pin Grid Array 84-pin - ST18940



11. DEVELOPMENT TOOLS

11.1. DESIGN PROCEDURE

The design of a digital signal processing application using the ST18940/41 is supported by a complete range of dedicated software and hardware tools including macroassembler, linker, high-level simulator and a C compiler and optimizer.

Additional hardware design tools include :

1 - stand alone emulation card ST18940-EMU
2 - multiprocessor hardware development system ST18940-HDS
3 - EPROM emulation module ST18940-EPROM
4 - PC compatible card ST18940-PC.

11.2. SOFTWARE TOOLS

All the development softwares run on the most common computers, such as IBM-PC XT, AT, under MS-DOS, VAXR under VMS, UNIXR or ULTRIX operating systems.

The macroassembler supports conditional assembly, high level language facilities for loop definition and generates all the files for simulation, emulation and PROM programming.

The functional simulator provides step by step execution, break on address and data values, access to all internal registers and interface to I/O files (ADC, DAC, test inputs).

The linker provides modular programming facilities.

The library consists of macros, basic DSP routines etc... and provides additional help to user's for their applications.

The C language compiler offers high-level language facilities which meets the advanced requirements (parallelism, pipe-line, three computation modes, 32-bit instruction set) to the ST18940.

11.3. HARDWARE TOOLS

All the hardware tools are designed to provide ease of use and minimum learning time by means of a menu driven interface and DSP specific emulation features.

ST18940 EMU and ST18940 HDS have in common :

- Full speed emulation of ST18940 and ST18941
- Use of internal or external clock
- 28 breakpoints (stops at defined addresses)
- 8 conditional breakpoints (stop after N address X and M address Y)
- Realtime trace of internal resources
- Emulation probes (for ST18940 - 41)
- Menu driven operation (about 100 commands)
- Resident Assembler/Disassembler with full screen editor
- Symbolic debugging
- Direct link with PROM programmers
- Direct link with host (KERMIT protocol)

Emulator specific features :

The ST18940 EMU is a low cost, stand-alone emulator providing advanced emulation features such as real-time trace. It can be driven via a RS232C link by a terminal or an IBM-PC^{R} and offers :

- 3K program memory
- 4K x 16-bit data RAM
- A wire-wrapping area
- Full speed 100 ns cycle emulation
- 2 RS232C serial ports
- Complex conditions break-points

Hardware development station features :

The ST18941 HDS is a hardware development station, aimed at the development of multiprocessor applications. Up to four pairs of emulator board/logic analyzer board can be combined to match exactly the user's needs :

- CMOS memory for backup of configuration
- 64K x 32 program memory
- 64K x 16 data RAM (mapping on a word basis)
- A logic analyser with :

*2K x 119 bits for trace of ST18940-41 bus and 15 external inputs

*Synchronous analyser on program and local buses

*Asynchronous analyser on system bus or external inputs

*Triggering conditions (Address bus with count, data bus external branch inputs, mailbox exchanges, external inputs).

EPROM module :

The ST18940 EPROM is a small-sized module which uses the perfect compatibility between ST18940 and ST18941. The module uses a ST18941 and fast EPROM memories to emulate in real time a ROM masked ST18940 during prototyping or field tests to minimize hardware developments. The module is plug - and function-compatible with ST18940.

APPENDIX A - BENCHMARKS

	Execution Time 100ns Instruction Cycle	**Memory Size** (words) **Prgm + coef.**
20 Tap FIR Filter	2.4µs	6 + 20
64 Tap FIR Filter	6.8µs	6 + 64
67 Tap FIR Filter	7.1µs	6 + 67
20 Tap Double Precision FIR Filter	7.6µs	26 + 40
3x3 Bidimentional FIR Filter	8.5µs	8 + 9
20 Tap Adaptive FIR Filter	4.6µs	12
8 Pôle Cascaded Canonic Biqual IIR Filter (4x)	2.4µs	13 + 20
8 Pôle Cascaded Canonic Biqual IIR Filter (5x)	2.8µs	13 + 20
8 Pôle Cascaded Transpose Biqual IIR Filter	3.3µs	15 + 20
Dot Product 2 x 2	0.6µs	6
Matrix Mult (2x2) Times (2x2)	1.4µs	14
Matrix Mult (3x3) Times (3x1)	1.5µs	15
FFT 64 pts	90.3µs	45 + 64
FFT 256 pts	500.1µs	177 + 256
FFT 1024 pts	3.15ms	234 + 512
8x8 Discrete Cosine Transform	4.75ms	650 + 12

APPENDIX B

MASKING INFORMATION

The information required by SGS-THOMSON Microelectronics to realize a customer masked version of the ST18940 must include program ROM content and coefficient ROM content. They can be transferred on EPROMS, 5" 1/4 floppy disks, magnetic tapes (VAX/VMS format) or by link to SGS-THOMSON Microelectronics. This must be done in conjunction with your local sales office or representative indications.

VERIFICATION MEDIA

All original pattern media are filled for contractual purpose and are not returned. A computer listing of the ROM content code will be generated and returned to the customer with a listing verification form. The listing should be carefully checked and the approval form completed, signed and returned to SGS-THOMSON. The returned verification form is the contractual agreement for generation of the customer masks and batch manufacturing.

VERIFICATION UNITS

Ten engineering samples containing the customer ROM patterns will be sent for program verification.

These samples will be engineering samples and must be kept by user as reference parts.

DIGITAL SIGNAL PROCESSOR

- 160ns INSTRUCTION CYCLE TIME
- PARALLEL HARVARD ARCHITECTURE
- SEPARATED PROGRAM AND DATA BUSES
- THREE DATA BUSES STRUCTURE
- DUAL EXTERNAL BUSES
- ONE CYCLE 16-BIT R/W OPERATION ON EXTERNAL DATA MEMORY
- THREE DATA TYPES : 16-BIT REAL, 32-BIT REAL, 16 + 16-BIT COMPLEX
- EXTERNAL MASKABLE INTERRUPT
- COMPLEX MULTIPLIER
- 256 x 16-BIT INTERNAL RAMs, 512 x 16-BIT INTERNAL COEFFICIENT ROM
- 1.28K x 32-BIT WORDS OF INTERNAL PROGRAM ROM
- NO FUNCTIONAL DIFFERENCES BETWEEN TS68930 ROM VERSION AND TS68931 ROMLESS VERSION

DESCRIPTION

The TS68930/31 HMOS digital signal processors are members of SGS-THOMSON family of general purpose DSP's fully software and hardware compatible with other members of the family.

By virtue of their highly parallel architecture, these digital signal processors are well suited to a wide range of applications including those requiring operations on complex numbers.

Typical examples are found in telecommunications, modems, image and speech processing, high speed control, digital filtering, sonar and radar applications.

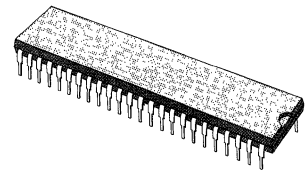
They are able to execute simultaneously within 160 ns an ALU function, a Multiplication, two Read and one Write operations with associated address calculation.

The on-chip large memory resources and multiprocessor direct interface allows the development at the lowest cost/complexity of high performance applications. The TS68931 is the ROMless version of the TS68930. In addition of the TS68930 features, it provides the capability of addressing up to 64K x 32 external instruction memory and allows a total realtime emulation of the TS68930. It is also particularly well adapted for applications where large program is required or for low quantities.

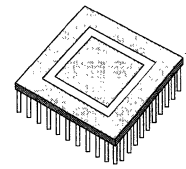
DEVELOPMENT SYSTEMS

The TS68930 is supported by a complete set of hardware and software tools for applications development. Software packages include assembler, linker and simulator on VAX and PC as well as a high level "C" compiler and optimizer.

Hardware tools include a stand-alone emulator, eprom emulation module and a powerful multiprocessor development station.



TS68930
P
DIP 48
(Plastic Package)



TS68931
R
PGA84
(Pin Grid Array Ceramic)

For pin connections and order codes, please see inside

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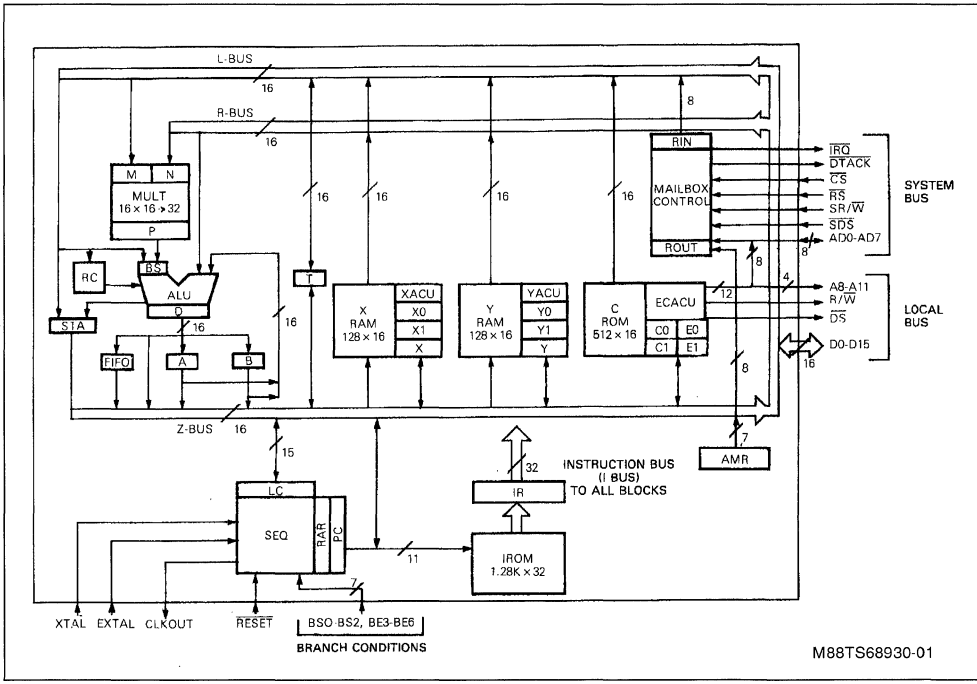
1. BLOCK DIAGRAM (TS68930)

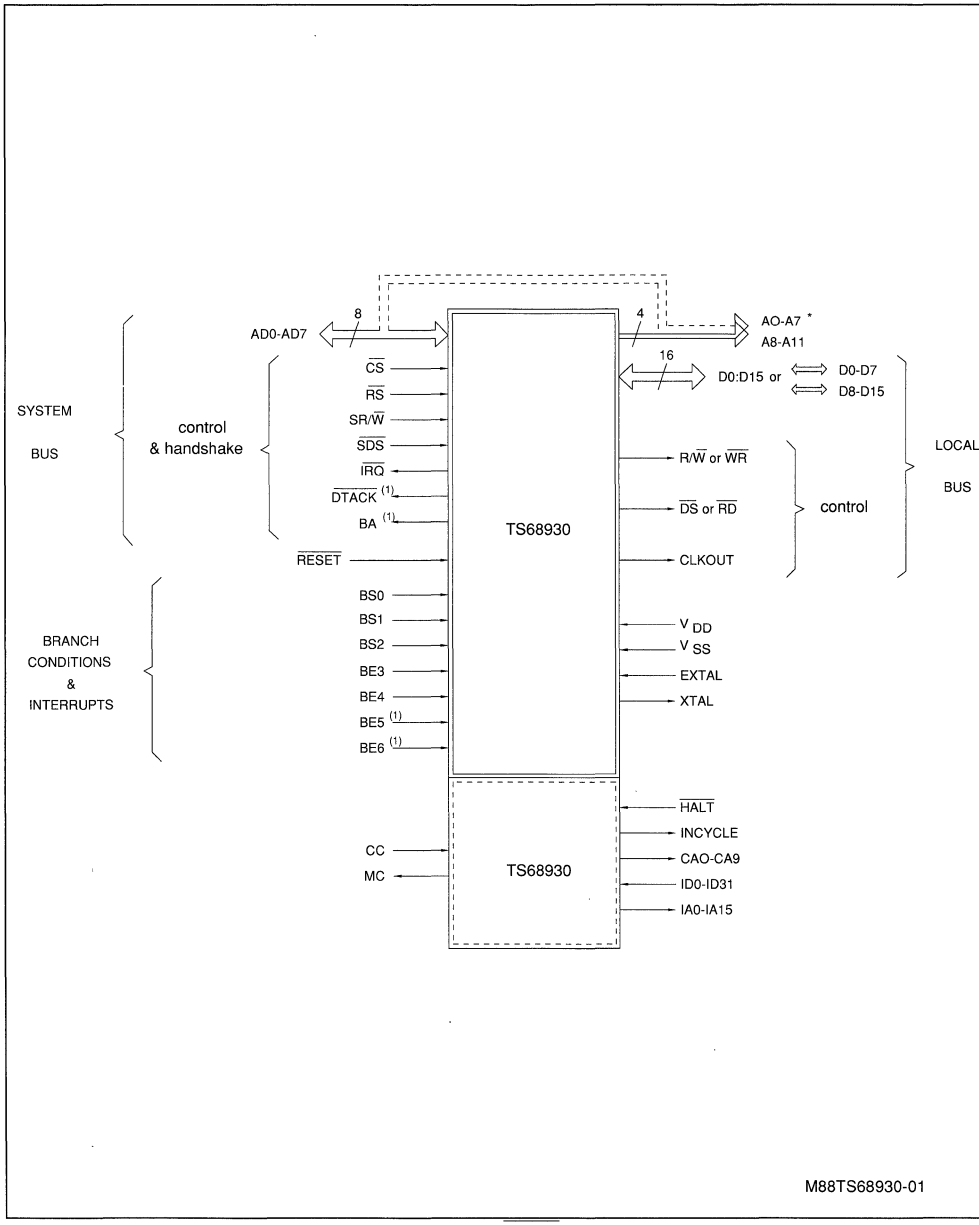


DEFINITION OF ACRONYMS

L-bus	: Left data bus	CROM	: Coefficient ROM
R-bus	: Right data bus	X0, X1, X	: Addressing registers XRAM
M	: Multiplier input register	Y0, Y1, Y	: Addressing registers YRAM
N	: Multiplier input register	C0, C1	: Addressing registers CROM
P	: Multiplier output register	E0, E1	: Addressing registers ERAM
BS	: Barrel Shifter	XACU	: Address calculation unit XRAM
ALU	: Arithmetic and Logic Unit	YACU	: Address calculation unit YRAM
D	: ALU output register	ECACU	: Address calculation unit CROM & ERAM
RC	: Replace Code register	RIN	: Input register of mailbox
STA	: Status register	ROUT	: Output register of mailbox
FIFO	: ALU output FIFO	AMR	: Access mode register
A	: ALU accumulator	IR	: Instruction register
B	: ALU accumulator	PC	: Program counter
Z- bus	: Result data bus	RAR	: Return address register
T	: Transfer register	SEQ	: Sequencer
XRAM	: X Data RAM	LC	: Loop Counter
YRAM	: Y Data RAM	IROM	: Instruction ROM

2. PIN DESCRIPTION

Figure 1 : Input/Output Pins.



Notes : 1. these pins are shared and software programmable : BE5/DTACK, BE6/BA
2. A0-A7 and AD0-AD7 may be multiplexed.

LOCAL INTERFACE

Name	Pin Type	Function	Description
D (0:15)	I/O	Data Bus	Can be concatenated or separate D (0:7), D (8:15).
A (8:11)	O	Address Bus	High order addresses for local interface.
$\overline{DS}/\overline{RD}$	O	$\overline{\text{Data Strobe}}$/read	Synchronizes the transfer on local bus/read cycle.
R/$\overline{W}$/$\overline{WR}$	O	Read/$\overline{\text{write}}$/write	Indicates the current bus cycle state/write cycle.
CLKOUT	O	Clock Output	CLKOUT Frequency is half input clock frequency.

SYSTEM INTERFACE

Name	Pin Type	Function	Description
AD (0:7)	I/O	System Data Bus or Local Address Bus	System data bus for exchanges between the processor and a host via an internal mailbox or local address bus for external RAM.
$\overline{CS}$	I	Chip Select	Used by a host to gain access to the mailbox and system bus.
$\overline{RS}$	I	Register Select	Used by a host to gain access to the mailbox and system bus.
$\overline{SDS}$	I	Data Strobe	Synchronizes the transfer on the system bus.
SR/$\overline{W}$	I	Read/write	Indicates the current system bus cycle state.
$\overline{DTACK}$	O	Data Transfer Acknowledge	Indicates that the processor has recognized it is being accessed.
BA	O	Bus Available	Indicates availability of the sytem bus to host.
$\overline{IRQ}$	O	Interrupt Request	Handshake signal sent to the master to gain access to the mailbox.

EXTERNAL BRANCH CONDITIONS

Name	Pin Type	Function	Description
BS (0:2)	I	Branch on State	External Conditions
BE (3:4)	I I	Branch on Edge	External Conditions. Falling edge is memorised and reset when tested.
BE5/$\overline{BA}$	I/O		BE5 shares pin with $\overline{BA}$.
BE6/$\overline{DTACK}$	I/O		BE6 shares pin with $\overline{DTACK}$.

OTHER PINS

Name	Pin Type	Function	Description
EXTAL	I	Clock	Crystal input pin for internal oscillator or input pin for external oscillator.
XTAL	I	Clock	Together with EXTAL it is used for crystal oscillator. If external oscillator is used, pin XTAL is not connected.
V_{DD}	I	Power Supply	
V_{SS}	I	Ground	
$\overline{RESET}$	I	Reset	

INSTRUCTION INTERFACE AND SYSTEM CONTROL INTERFACE (ST18931 only)

Name	Pin Type	Function	Description
ID (0:31) IA (0:15) CA (0:9)	I/O O O	Instruction Data Instruction Address Coef. ROM Address or External RAM Address	Instruction Bus. 32 Bit Data Instruction Address External Coefficient ROM Address 10 Bit OR External RAM Address (9-bit address – output enable signal) (8-bit address)
$\overline{\text{HALT}}$	I	Halt Signal	Halts the processor. This signal freezes the program and loop counters.
INCYCLE	O	Instruction Cycle Clock	A transition from low to high indicates that a new instruction is processed.

3. FUNCTIONAL DESCRIPTION

3.1. GENERAL ARCHITECTURE

The TS68930/31 architecture is based on an innovative architectural concep developped by SGS-THOMSON Microelectronics.

The TS68930 is compatible with the ST18930 and ST18940 other members of SGS-THOMSON digital signal processors family.

The TS68930 confirms the efficiency of a highly parallel and pipelined operation using a true Harvard memory space and bus structure.

The block diagram shows four main blocks :

. The sequencer block

. The operating unit (ALU, Multiplier and Barrel Shifter)

. The data memories

. The inputs/outputs

These four blocks can be considered as four independent units working in parallel and communicating through a network of 16/32 - bit buses.

By taking advantage of the 32 - bit wide instruction bus, the TS68930/31 are able to execute simultaneously the following operations during each machine cycle :

. Read two operands from internal or external memory

. Execute a multiplication

. Perform an ALU operation

. Write a result into internal or external memory

. Post modify three pointers independently

. Store data into the transfer register

In addition, data exchanges through mailbox occur concurrently and independently of internal operations.

All instructions are executed in a single cycle time except branch instructions.

Some additional features give the TS68930/31 extremely powerful performances. They provide three operating modes (real, complex and double precision) dynamically set by software and user transparent.

In complex mode, the hardware multiplier provides (16 + 16 - bit) results from 2 x (16 + 16 - bit) inputs each machine cycle.

(12.5 - million multiplications per second).

The ALU, reinforced by a barrel shifter, provides 27 basic arithmetic and logic functions.

Three dedicated calculation units control the four data memory spaces.

A 1.28K x 32 program ROM (for the TS68930) allows most of digital signal processor applications possibilities, using the efficiency of the code and architecture. The following sections will detail all the hardware blocks of the TS68930/31 and demonstrate its software performances provided by the high level of parallelism in the operations.

3.2. OPERATING UNIT

One of the most useful features of the TS68930 is to provide the user three operating modes which can be dynamically set by software.

These three modes are :

. REAL 16-bit

. COMPLEX 16-bit real + 16-bit imaginary

. DOUBLE PRECISION 32-bit

Thus, the DSP is seen by the user as a standard 16 - bit real or complex machine or a 32-bit real machine. All operating units and working registers are automatically adjusted by the processor to the right length. In real mode, all instructions are executed in

a single machine cycle. In complex and double precision mode, the instruction time is doubled.

In all modes, the number representation used is signed 2's complement.

3.2.1. 16/32 - Bit ALU/Accumulator (fig. 2). The ALU can be seen either as a 16 or 32 - bit ALU. The ALU is loaded on the right side by the R - bus or by the A or B accumulators.

On the left side, the operands always access the ALU through the barrel shifter, coming either for the L (left) - bus or the hardware multiplier output register P.

The result of an ALU operation is automatically written in the D register and, if required into the Accumulator or FIFO. The ALU provides a range of 27 codes for operations which execute in a single machine cycle. They include arithmetic and logic operations, shift and rotate operations.

The high degree of parallelism of the TS68930/31 processor allows more combinations than previous generation DSP devices which require a more complex instruction set.

The complete list of ALU codes and description is given in 3.8.2.

3.2.2. Barrel Shifter. The 16-bit barrel shifter located on the left side of the ALU performs all logic/arithmetic shifts and rotations. It is used for normalization and formatting of data in floating point operations and bit or byte manipulations. Two types of operations are allowed in the barrel shifter.

- Operations defined by ALU codes (shifts of 1 or 8 bits) see 3.8.2
- Operations defined by specific dedicated instructions :

ASR ($0 \rightarrow 15$) arithmetic shift right by N ($0 < N \leq 15$)

LSR ($0 \rightarrow 15$) logical shift right by N ($0 < N \leq 15$)

LSL ($0 \rightarrow 15$) logical shift left by N ($0 \leq N \leq 15$)

ROR ($0 \rightarrow 15$) rotation right by N ($0 < N \leq 15$)

These codes allow all types of shifts from 0 to 15 bits.

3.2.3. Multiplier. The multiplier executes a 16 x 16-bit multiplication with a 32-bit result at each machine cycle. The operands are loaded into the M and N registers and the result of a previous multiplication is written in the P register during the same cycle.

The pipeline structure makes the multiplication result available with a delay of two instruction cycles.

The multiplier provides a multiplier overflow flag OVFM which is memorized in the status register in complex mode only (see 3.2.4).

The efficiency of the parallel pipeline operation of the multiplier is shown in fig. 3.

3.2.4. Associated registers. Registers A and B store the results from the ALU. They are sized according to the mode of operation. They also provide capability to feedback the ALU for a new operation with the ALU result of a previous operation.

Register FIFO.

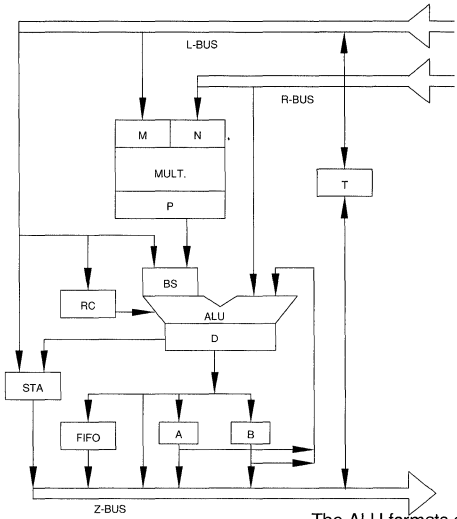
The 4 x 16-bit FIFO is used for intermediate storages. Initialization of the FIFO (empty FIFO) can be made by an INI instruction.

A result loaded in FIFO at instruction N is available at least at instruction N+2 in real mode and N+1 in complex and double precision modes.

Register RC (Replace Code register).

This register can dynamically load an ALU code to be executed by the processor from the data memories. It allows data control program sequencing without the use of a systematic test instruction. For instance, in FFT calculation, scanning may or may not be necessary during a pass.

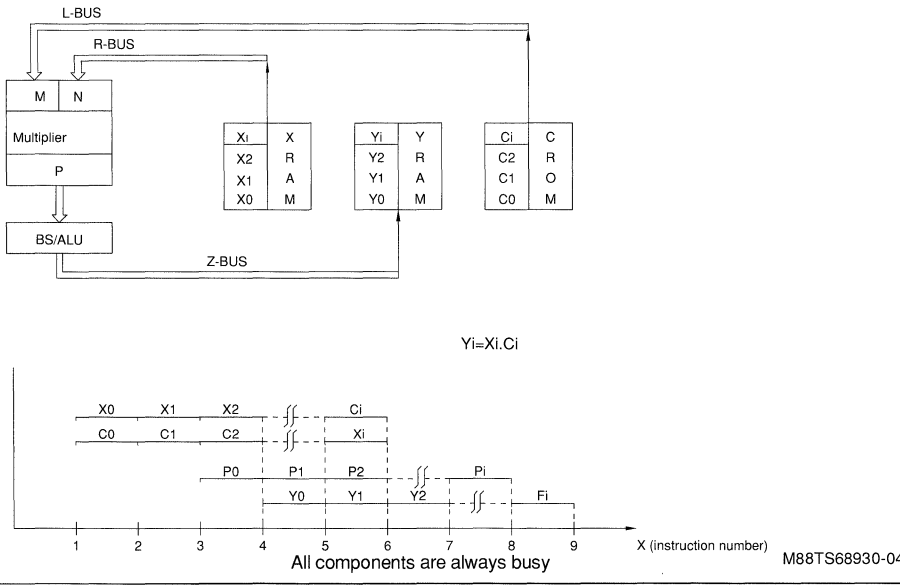
Figure 2 : Alu Block Diagram.



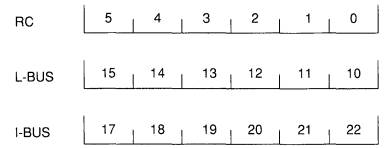
- 4 Inputs
  giving access to 10 possible sources :
  XRAM, YRAM,CROM, ERAM,
  P, T, RIN, A, B, FIFO
- 5 Destinations : A, B, D, FIFO, Z BUS
- R side by Accumulators
  L side by T registers
- 27 operations : including Arithmetic,
  Logic, Shifts,
  With 3 modes of execution :
  Real
  Complex
  Double precision
- Saturation mode to prevent overflow
- The status register gives information
  on the results of operations.
- The Replace Code Register allows dynamically changing the ALU operation code with a data.

The ALU formats are : 16-bit in Real mode
16 + 16-bit in Complex mode
32-bit in Double Precision mode

Figure 3 : Multiplier Efficiency.



This register is 6-bit wide and is loaded by the 6 MSB of L-bus :



Bit 1 to 5 contain the executable ALU code corresponding to the bits I21-I17. Bit 0 allows the choice of ALU output destination (A or B register).

Its contents is defined by three ALU codes : (see 5.2.)

ALU Code	Function
RCR	Load ALU control code in register RC.
RCE	Execute ALU code contained in register RC.
RCER	Execute ALU code contained in RC and load new ALU code in RC.

Status register (STA).

This register provides a status of the ALU, operating and addressing modes, and multiplier. It is divided into two sub-registers :

CCR (Condition Code Register)
STR (State Register)

A detailed description of this register is given in δ 5.4.

Transfer register T.

The transfer register provides a direct transfer capability between L-bus and Z-bus.

It can either be source or destination for the two buses.

Its various uses include :

* Loop back to the multiplier in one cycle
* Temporary register between memory and ALU
* Temporary register between memory and multiplier
* Operation between two accumulators in the same instruction
* Memory to memory transfer
* Saving program counter (in a branch instruction)

The status register content can be saved using instruction SVR.

The condition code register CCR can be read in OPIN instruction and it can be loaded via L-bus (ALU code LCCR).

The state register STR can be programmed by an INI instruction or an SVR instruction (except EF bit).

3.3. DATA MEMORY BLOCKS.

3.3.1. Available spaces. The TS68930 provides four separated memory spaces (see fig. 4)

. two internal RAMs of 128 x 16-bit (YRAM and XRAM)

. one internal data ROM (independent from the program ROM) of 512 x 16-bit (CROM) (ST18930 only)

. one optional external memory (ERAM) of 4K x 16-bit accessible in one single instruction cycle in exactly the same way as internal memories.

This external memory is controlled by an Intel or Motorola type control interface and offers full speed, fully transparent, Read and Write operations.

Slower external memories or peripherals can be accessed by using slow exchanges modes.

However slower external memories or peripherals can be accessed by using slow exchanges mode.

The powerful instruction set and the Harvard architecture allows many combinations of simultaneous memory accesses. The only forbidden situations are :

- read and write access is the same RAM within the same instruction
- simultaneous access to CROM and ERAM

3.3.2. Address Calculation Units. Three different Addresses Calculation Units are available.

XACU is associated with XRAM

YACU is associated with YRAM

ECACU is associated with the ERAM and the CROM

3.3.3. Addressing modes. The TS68930 provides four addressing modes :

- Direct addressing
- Immediate operand
- Indirect addressing with or without post modification of the pointers
- Circular addressing (also called virtual shift mode) for XACU and YACU.

The circular addressing mode is of particular interest in digital signal processing typical operations like convolution algorithms used in FIR filters. It has the same function as a shift register but does not move the data stored.

For this feature, three pointers are used in the memory space chosen (X or Y). The current address is given by a specific X pointer shifting repetitively between two limits X0 and X1 (respectively Y, Y0 and Y1).

The circular mode is declared in the status register STA (see 3.2.4) by an INI instruction.

3.3.4. Pointers. The TS68930 offers a large number of address pointers for each memory space :

- X0, X1 and X for XRAM
- Y0, Y1 and Y for YRAM
- C0, C1 for CROM
- E0, E1 for ERAM

The pointers Xi, Yi, Ci and Ei can be independently incremented, decremented or maintained. The two pointers X and Y are specific to the circular addressing mode. The pointers can be loaded with new addresses (constant or computed values) through Z-bus. In this case, the value of unused Z-bus MSBs are irrelevant. The unused bits are set to 1.

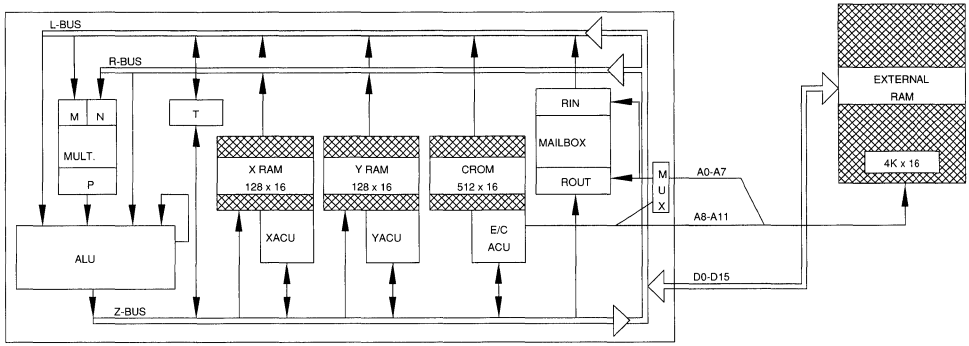
3.3.5 Odd/Even addresses. In complex and double precision modes, the processor automatically generates the two addresses necessary to store

one data word (even first, then odd addresses).

The user can reverse this order by setting to 1 the ADOF bit with the INI instruction (refer to OPCODE). This feature is available independently for XRAM and YRAM.

	COMPLEX WORD	DOUBLE PR. WORD
Even Address	Real Part	Lower Part
Odd Address	Imaginary Part	Upper Part

Figure 4 : Data Memory Blocks.



full speed, and fully transparent read and write operations

3.4. SEQUENCER BLOCKS

3.4.1. Sequencer. The purpose of the sequencer is to generate the next instruction address.

The sequencer takes into account the current operating mode of the TS68930/31 to execute this task. The instruction is executed in one cycle time in real mode and two cycles time in complex or double precision mode.

The linear address program generation may be interrupted by several means hereunder described.

A. Execution of a branch instruction
- unconditional branch always.
- seven ALU conditions flagged from the status register :

SR	Sign real
SI	Sign Imaginary
CR	Carry Real
CI	Carry Imaginary
Z	Zero
OVF	Overflow
MOVF	Memorized overflow MOVF is reset when tested by branch instruction.

- three external conditions on state of pins BS0, BS1, BS2 (the pins BS0, BS1, BS2 can also be used as interrupt pins if enable interrupt is programmed).
- four edge sensitive external conditions on pins BE3, BE4, BE5, BE6. The falling edges of BE3-BE6 are memorized internally and reset when tested by the branch instruction. The external test conditions are used to synchronize different processes.
- The mailbox flag RDYOIN indicating mailbox availability.

All the branch conditions can be tested on true or false conditions.

B. Subroutine call

C. Loop execution

One of the most powerful features of the TS68930/31 is its ability to repeat the execution of several instructions with very straightforward commands. The loop execution is set with the instructions : REPEAT, BEGIN, END which respectively define the number of loops, the beginning of loop and its end. The DSP will then manage all the necessary pointers to execute the loop with no overhead time (see 3.4.4.).

3.4.2. Instruction ROM. The TS68930 instruction ROM has a capacity of 1280 words of 32-bit available for the user. The ROM code is defined following the user's information (see appendix C for masking information). The TS68931 does not provide an on-chip ROM memory, but can address an external 64K program memory space in a single cycle.

3.4.3. Program Counter. The program counter is a 16-bit wide Register ; 12 bits are used in the TS68930 (ROM version).

3.4.4. Loop Counter. The loop counter does considerably increase the efficiency of the processor in repeated calculations, very commonly used in digital signal processing.

Three counters define a hardware loop :

- LCI Instruction Loop Counter (4-bit). Counts the number of instructions to be executed in the loop.
- LCR Repeat Loop Counter (8-bit). Gives the number of times the loop will be repeated (can be loaded by a calculated value).
- LCD Delay Loop Counter (3-bit). Gives the delay between the declaration and the start of a loop.

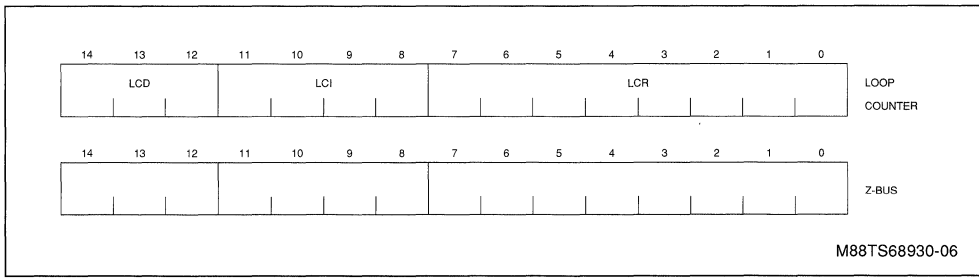
The loop counter content can be saved (SVR instruction) with the format shown in table below :

The loop counter is set by the three pseudo-instructions Begin, Repeat and End in the Macroassembler.

The loop counter is frozen during an interrupt routine.

On the TS68931, a HALT freezes the state of the loop counter. A RESET signal resets the loop counter.

3.4.5. Return Address Register. The JSR instruction allows one level of subroutine nesting with automatic saving of the PC on to the Return Address Register. Multiple Level of subroutine nesting can be implemented in RAM using either of the two pointers as stack pointer.



3.5. INPUTS/OUTPUTS

A very important feature of a signal processor is its ability to be inserted in a complete system including memories, other processes, analog interface circuits.

Basically, the external world seen by a TS68930/31 can be divided in two main sections : communications with its own local resources (peripheral, memories, converters) and communications with control processor, either microcontroller or master DSP in a multiprocessor application.

To communicate with its local resources, the TS68930/31 uses its local bus.

To interface with a host, the TS68930/31 uses its system bus and branch capabilities.

However, the local and system bus configuration is flexible and allows many combinations for the architecture of a system based around a TS68930/31.

3.5.2. Dual bus interface. In order to provide the maximum flexibility, the TS68930/31 provides two buses. One is called the system bus and is found on pins AD0-AD7, the other one called local bus is situated on pins D0-D15. The system bus provides a very straightforward interface to a host controller, while the local bus allows the TS68930/31 to make an efficient use of external resources such as memories, analog interface circuits etc... This dual bus structure allows many combinations of circuits where the TS68930/31 can act in different ways :

Fig. 6A as a microprocessor peripheral

Fig. 6B as a processor with its associated memory

Fig. 6C as an intelligent peripheral having its own external memory and connected to a microprocessor.

It must be emphasized that, in most configurations, the connections are absolutely direct and do not use any external additional logic.

Furthermore, thanks to the dual bus structure, several TS68930/31 can be very simply combined together in multiprocessor applications, thereby directly increasing the processing power.

Figure 6 A : HOST/TS68930.

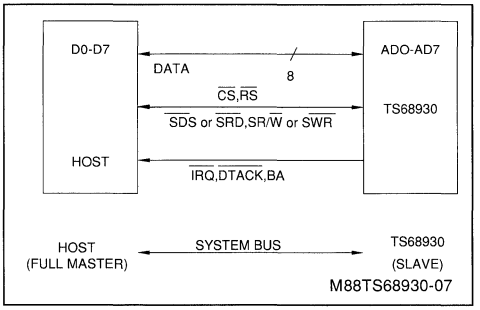


Figure 6 B : TS68930/RAM.

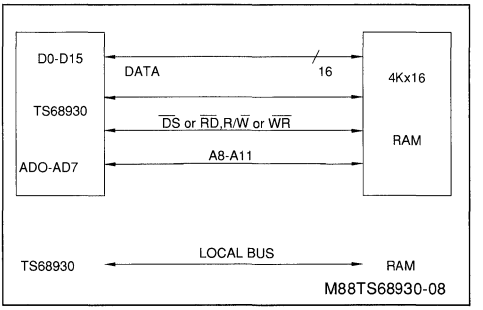
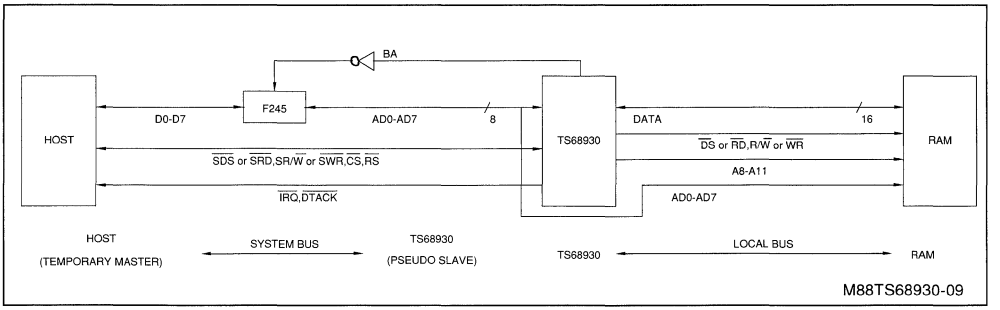


Figure 6 C : HOST/TS68930/RAM.



3.5.3. Host/slave configuration. The processor acts as a host on its local bus and as a slave on its system bus.

In configurations in which the TS68930 accesses external RAMS on its local bus, pins AD0-AD7 can be used to provide 8 LSB addresses, while A8-A11 provides 4 MSB addresses to the RAM.

In this case, the TS68930/31 prevents the host from using the system bus and is then called a pseudo-slave.

Since the host can only temporarily access the system bus it is defined as a temporary master. That mode of operation is software controlled through the Access Mode Register (AMR) (see 3.5.7.).

On the TS68931 the pins CA0-CA7, which present the least significant bits of external ERAM/CROM addresses can be connected to that RAM in place of system bus pins AD0-AD7.

3.5.4. Local bus. The local bus uses two software programmable signals to control the data on D0-D15.

$\overline{DS}$: Data Strobe. Synchronizes the transfer on local bus.

R/$\overline{W}$: Read/Write. Indicates the direction of the data.

These signals are used for Motorola-like bus compatibility.

$\overline{RD}$: Read. Read clock pulse.

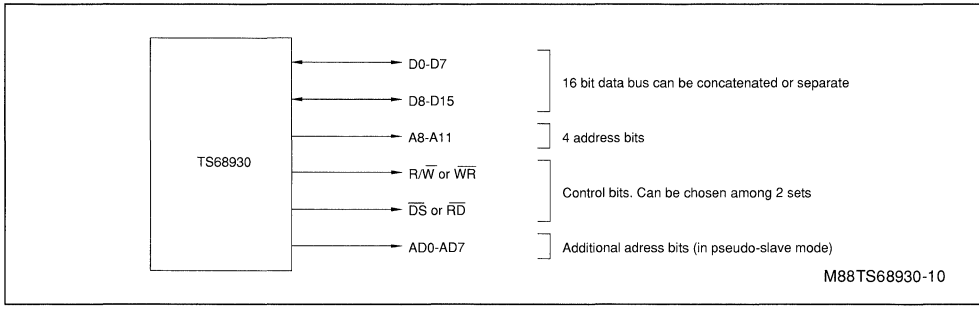
$\overline{WR}$: Write. Write clock pulse.

These signals are used for Intel-like bus compatibility.

A8-A11 : Address bits (4)

AD0-AD7 : Optional additional address bits (8)

Figure 7 : Local Bus Pin Description.



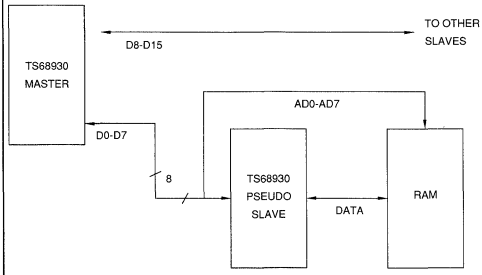
The four address bits of the local bus are usually sufficient to address peripherals. When an access to external RAM is necessary with the TS68930/31, the address bus can then be extended by using the AD0-AD7 pins of the system bus as address lines.

If an external peripheral or external memories are too slow to answer in one machine cycle, the TS68930/31 can be programmed to execute an external access in 2 cycles using the bits ES0 and ES1 of Access Mode Register (see 3.5.7.).

This mode is particularly useful for peripherals such as data converters, or dedicated interface like the MAFE chip set (Modem Analog Front End) from SGS-THOMSON.

The local data bus can also be splitted into two independent 8-bit buses. This is used in a multiprocessor architecture when a pseudo-slave uses the system bus to transfer its own RAM addresses on D0-D7 (fig. 8). By dividing its local bus, the temporary master can remain a full-master on bus D8-D15 and does not require a bus transceiver on D0-D7. The selection between the two buses is then made by the addresses A10-A11 as indicated in fig. 8.

Figure 8 : Separate Local Buses.



A_{11}	A_{10}	$D_0 - D_7$	$D_8 - D_{15}$
0	0	Selection	High Impedance
0	1	High Impedance	Selection
1	0	High Impedance	Selection
1	1	High Impedance	Selection

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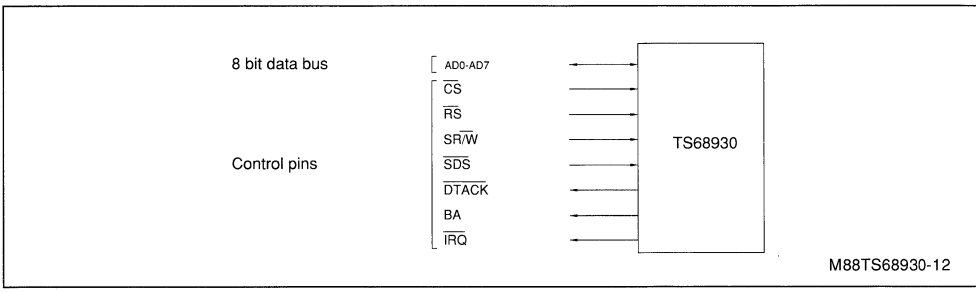
3.5.5. System Bus : The system bus uses two signals to control the data on AD0-AD7. The system bus mode of operation is Motorola like.

$\overline{CS}/\overline{RS}$	Mailbox Control Signal. Also used by a host to gain access to the bus.
$SR/\overline{W}$ $\overline{SDS}$	System Read/Write System Data Strobe } Generated by an external processor (host).
$\overline{IRQ}$	Handshake Signal (see 3.5.6)
$\overline{DTACK}$	Data Transfer Acknowledge. Compatibility with 68000 family. Is programmed by Access Mode Register.
BA	Bus Available. The TS68930/31 is not currently using the system data bus to generate addresses. BA is also programmable by the Access Mode Register.

Figure 9 : System Bus Description.



protocol signal description.

RDYOIN.
Internal flag indicating the status of the mailbox
0 = DSP has access to the mailbox
1 = host has access to the mailbox

a. RDYOIN is set by the DSP and reset by the host. That means that the DSP gives the mailbox to the host when it finishes using it and vice-versa. In no case can the host or the DSP take possession of the mailbox, it can only wait for the other to give it back.

b. The TS68930/31 sees RDYOIN as a flag :
   - tested by a branch instruction
   - set to 1 by an initialization instruction in order to give the availability of the mailbox to the host.

$\overline{IRQ}$.
Handshake signal enabling the host to gain access to the mailbox.

a. $\overline{IRQ}$ is asserted low by the DSP to indicate the availability of the mailbox (at the same time as RDYOIN).

b. The host after testing $\overline{IRQ}$, knows that it can access the mailbox. The access to the bus (which can be currently used by the DSP as a local address bus) must be requested by reading the address $\overline{CS}$ = 0, $\overline{RS}$ = 0.

c. The DSP then answers back by asserting $\overline{IRQ}$ high. (In pseudo-slave mode, the DSP is halted). The host now has full control of the bus and mailbox.

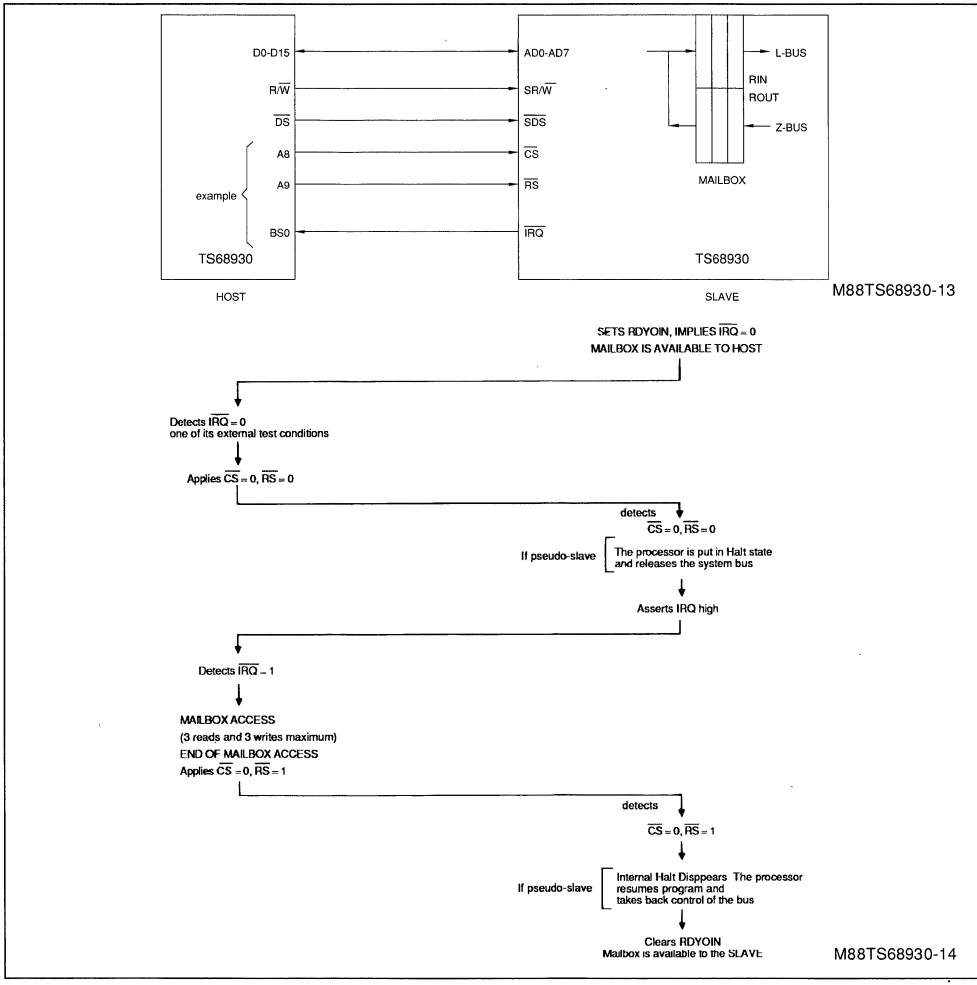
   When the host has completed the exchange it generates the address $\overline{CS}$ = 0, $\overline{RS}$ = 1 and the DSP resets RDYOIN.

HALT (internal).
The internal halt has the following effect on the circuit :
- the program is stopped at the end of the current instruction, the program and loop counter are frozen
- a NOP is executed
- no more addresses are generated on the system bus

3.5.6. Mailbox. The mailbox is a set of registers which interface with the system data bus. The mailbox is divided in two parts :

- RIN (3 x 8 bit register) : This register is read internally by the TS68930/31 on the upper byte of L-bus (L8-L15) and written externally from the system bus. After each write or read operation the data is shifted by one byte.
- ROUT (3 x 8 bit register) : This register is written internally with the upper byte of the Z-bus (Z8-Z15) and read externally on the system bus. After each operation (read or write), the data is shifted by one byte.

Figure 10 : Mailbox Connection and Protocol.



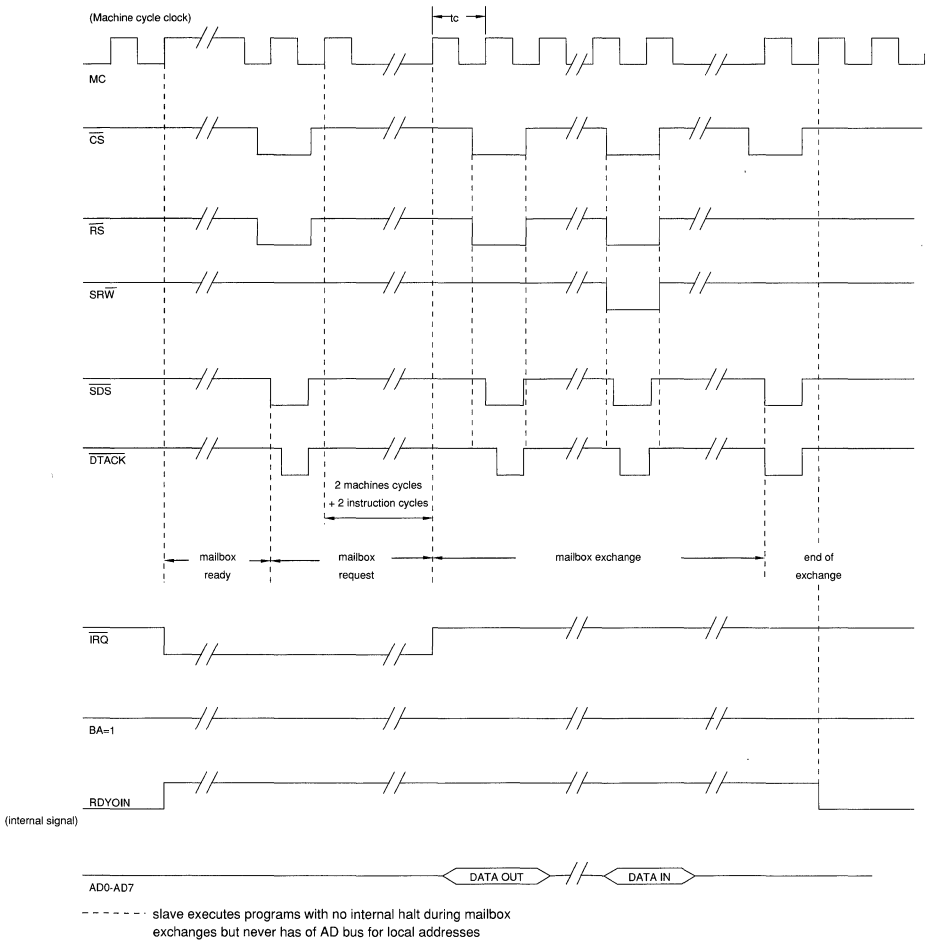
This protocol is hardwired on the slave side and programmed on the host side. The mailbox is included in the slave. The two slave address pins (CS, RS) are directly connected to two host address lines.

Therefore, the slave is seen as two external memory locations by the host which will address it by generating an external address directly or indirectly (pointer E0 or E1).

By addressing the location 00 the host echoes the IRQ to the slave and accesses the mailbox.

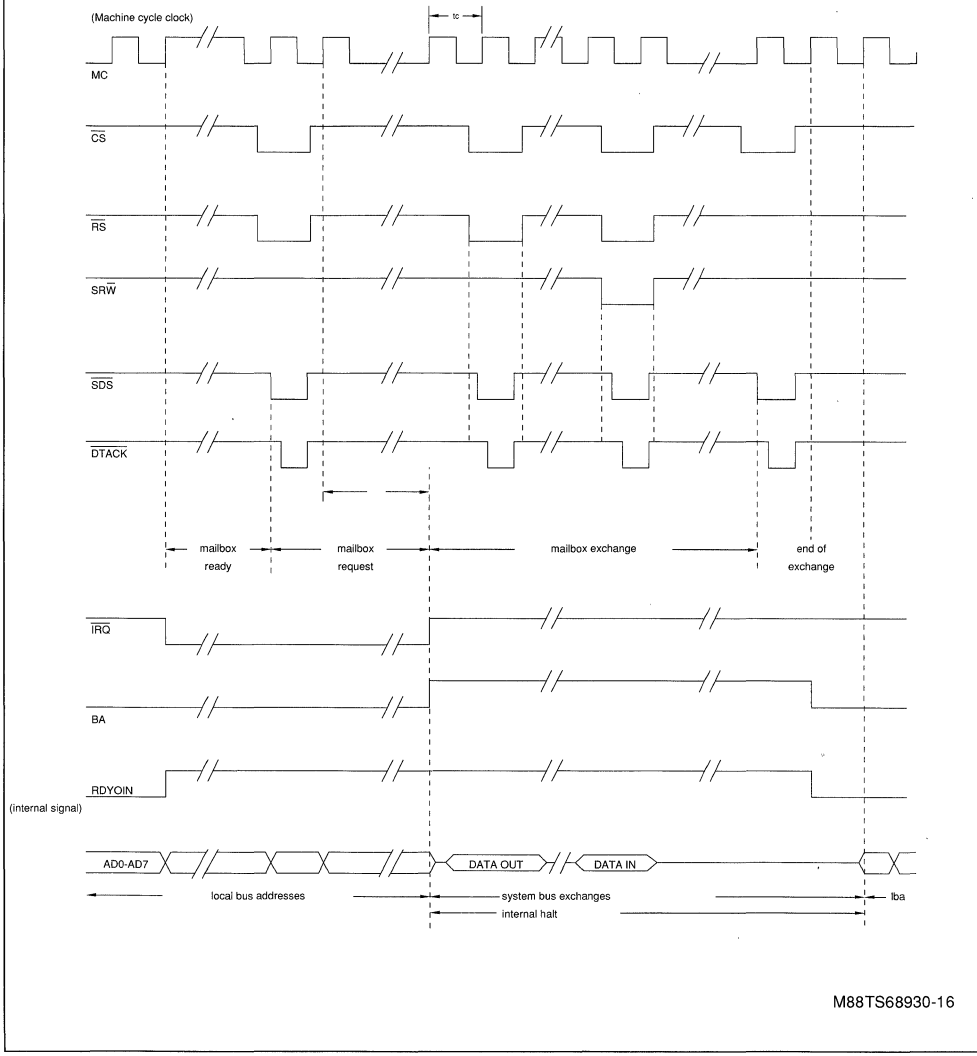
By addressing the location 01 the host releases the bus.

Figure 11.A : TS68930/31 Mailbox Exchange, Slave Mode.



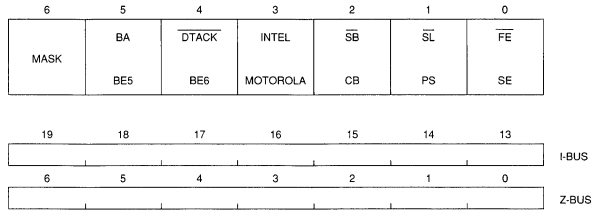
* Up to three consecutive read/write operations may take place.

Figure 11.B : TS68930/31 Mailbox Exchange, Pseudo Slave Mode.



3.5.7. Access Mode Register (AMR). The AMR is a 7-bit register which defines the processor external access modes.

It is loaded by an INI or SVR instruction and saved by an SVR instruction. Its fields are defined as follows :



Bit 0 : $\overline{FE}$/SE

This bit defines Fast Exchange in one cycle to access external resources when low. Or slow exchange in two cycles when high. The slow exchange mode can only be used in the real mode. The circuit automatically repeats the instruction which defines the external transfer. The control of the multiplier, ALU, ACU, loop counter is the responsibility of the programmer who must take into account the repetition of the instruction.

Bit 1 : $\overline{SL}$/PS.

0 = Slave.
1 = Pseudo-slave.

This bit defines the behaviour of the TS68930/31 regarding the system bus (AD0-AD7). In slave mode, the processor will never use the system bus as local bus address.

In pseudo-slave, the processor uses address bus (AD0-AD7) for local resources. These bits will be concatenated with A8-A11 bits of the local bus to form a 12-bit address bus for larger external memory spaces. The pseudo-slave will then address an external RAM with LSB's address on AD0-AD7 and MSB's on A8-A11. After an exchange the TS68930 in pseudo-slave mode must relinquish the master (see 3.5.3. - Master/slave configuration).

Bit 2 : $\overline{SB}$/CB.

0 = Separated bus.
1 = Concatenated bus.
This bit indicates whether the local bus is used as a 16-bit concatenated bus or as 2 independent 8-bit buses.
(see 3.5.4. - local bus description).

Bit 3 : I/M.

0 = Control pulses Read ($\overline{RD}$) and Write ($\overline{WR}$) are generated. This is the case with an Intel type peripheral or a standard byte-wide RAM.
1 = Control pulses data strobe ($\overline{DS}$) and Read/Write (R/$\overline{W}$) are generated.

This is the case for exchanges with a slave processor, a 68000 type peripheral, a data converter such as TS7542 or the M.A.F.E. chip set (TS68950/51/52).

Bit 4 : $\overline{DTACK}$/BE6.

The TS68930 does acknowledge correct access by generation of a DTACK output. In this case, the BE6 pin is not available for an external test condition.

Bit 5 : BA/BE5.

This bit low configurates the pin BA/BE5 as bus available output (BA) indicating to the master that the pseudo-slave is not using the system bus for generating addresses on the local bus. When high, it is used as an external test condition (BE5).

Bit 6 : MASK (TS68931 only).

When this bit is low, an external Halt applied to the processor will not change the values in the ARM register. When high, an external Halt applied to the processor will reset the ARM register with following configuration :

ONE CYCLE EXCHANGE, PSEUDO-SLAVE, CONCATENATED BUS, RD AND WR CONTROL PULSES.

This bit can be modified by the programmer even while the HALT is asserted.

3.5.8. Instruction interface and system control (TS68931 only). On the TS68931, the coefficient ROM and the instruction ROM (CROM & IROM) are external. The device provides the necessary buses to access these data. Instructions are read on ID0 : ID31 using IA0-IA15 for addressing. Coefficients are read on local address bus D0-D15 using CA0-CA8 for addressing. CA9 is at low level for address validation. CA0 : CA7 also contains external RAM addresses (if necessary) associated with a high level for CA9.

So, for the TS68931, there is no need of a pseudo slave mode as AD0:AD7 remain available for data transfer on the system bus. Clock signals are also provided for interfacing purposes (3.6.1.).

3.5.9. Halt (TS68931 only). The external $\overline{\text{HALT}}$ signal will freeze the program counter, the loop counter. The instruction register can then be loaded from an external source. This signal is used for system development. If the MASK bit = 1 then it will force the AMR into the following configuration :

ONE CYCLE EXCHANGE, PSEUDO SLAVE, SEPARATE BUS, RD AND WR CONTROL PULSES.

3.6. OTHER RESOURCES

3.6.1. Clock generators. Different clock outputs are available on the TS68931 and on the TS68930.

CLKOUT : available on TS68930 and TS68931.

INCYCLE : available on TS68931 only.

The CLKOUT output period is function of the EXTAL period and is half the frequency of the input clock.

The INCYCLE output is equal to machine cycle in real mode and half of machine cycle in complex and double precision mode.

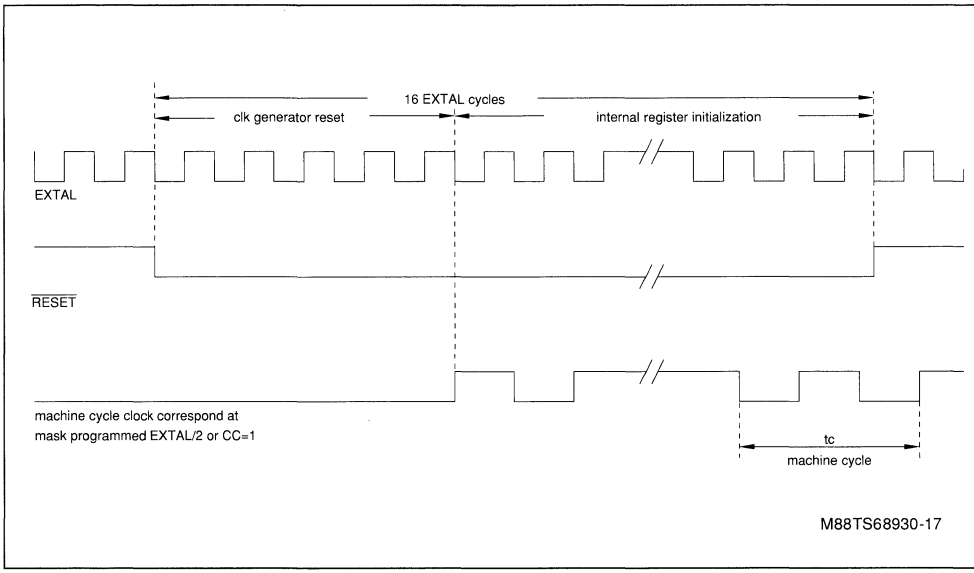
3.6.2. Reset. The reset signal acts on several processors blocks as follows :

- Sequencer : the program counter (PC) and the loop counter (LC) are cleared to zero. The instruction register is loaded with NOP instruction.
- Status register : set in real mode, no saturation, empty FIFO (EF = 1), memorized overflows (MOVF = 0), and XRAM and YRAM in non circular addressing mode.
- Access Mode Register (AMR) : set for one cycle external exchange, slave mode, concatenated bus, RD and WR, BE5 and BE6, SDS and SR/W.

The reset signal must be maintained for a minimum of 16 cycles of EXTAL signal .

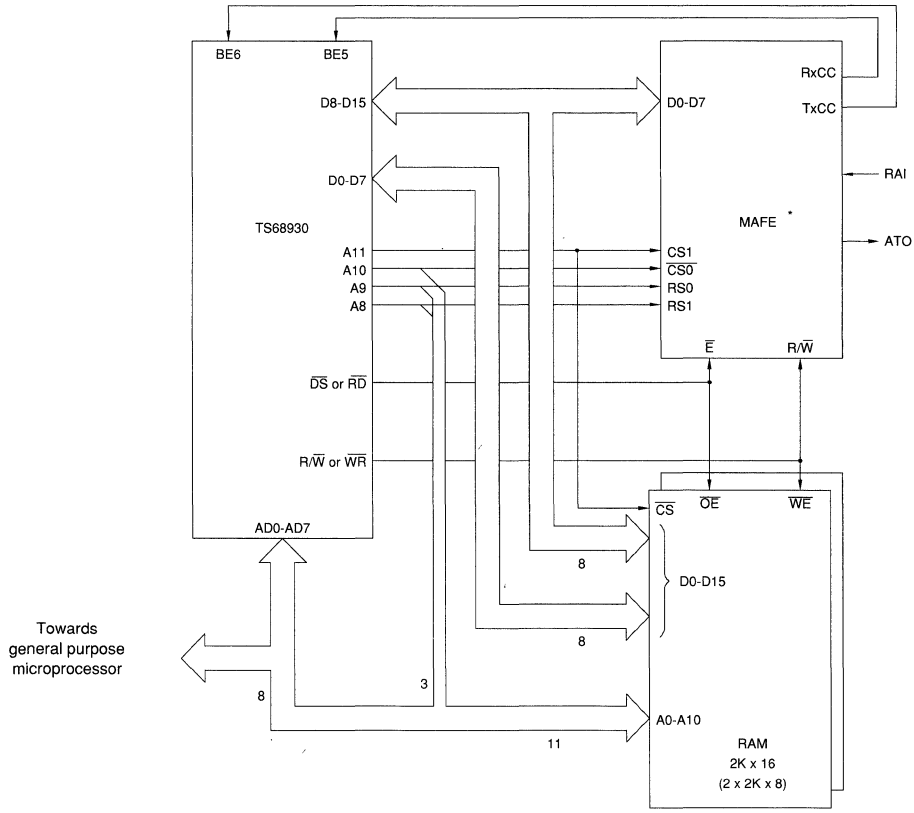
3.6.3. Watchdog capability. The watchdog prevents the processor from staying locked in an undesired state or internal loop caused by adverse conditions such as high-voltage transients. The circuitry includes a 2-bit counter which is incremented by each falling edge on BE3 input and reset by software testing of any of the BE3 conditions. If three falling edges of BE3 input occurs without a test of the condition, the TS68930 is reset by the watchdog circuit. This capability is a mask option of the TS68930 which is chosen (or not) by the user.

Figure 12 : Reset Timing.



4. TYPICAL APPLICATION CONFIGURATIONS

Figure 13 : Configuration Example with TS68930 + RAM + MAFE*.

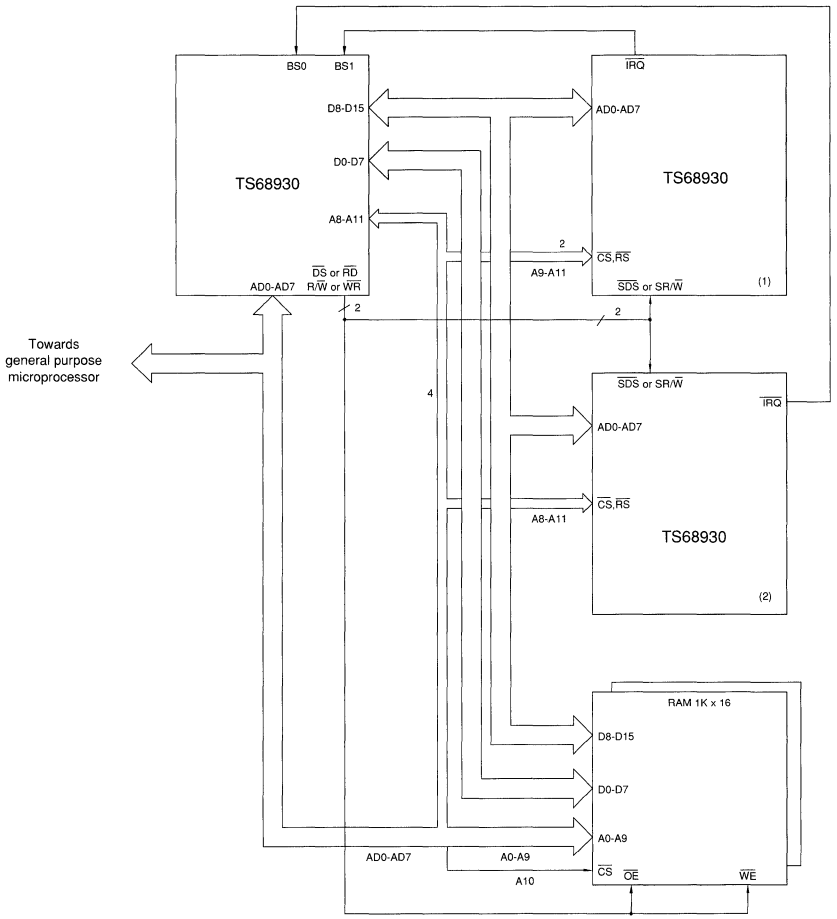


A_{11}	A_{10}	A_9	A_8	
1	0	X	X	**MAFE**
0	X	X	X	**RAM**

* MAFE is the TS68950/51/52 Modem Analog Front – End Chip Set.

M88TS68930-18

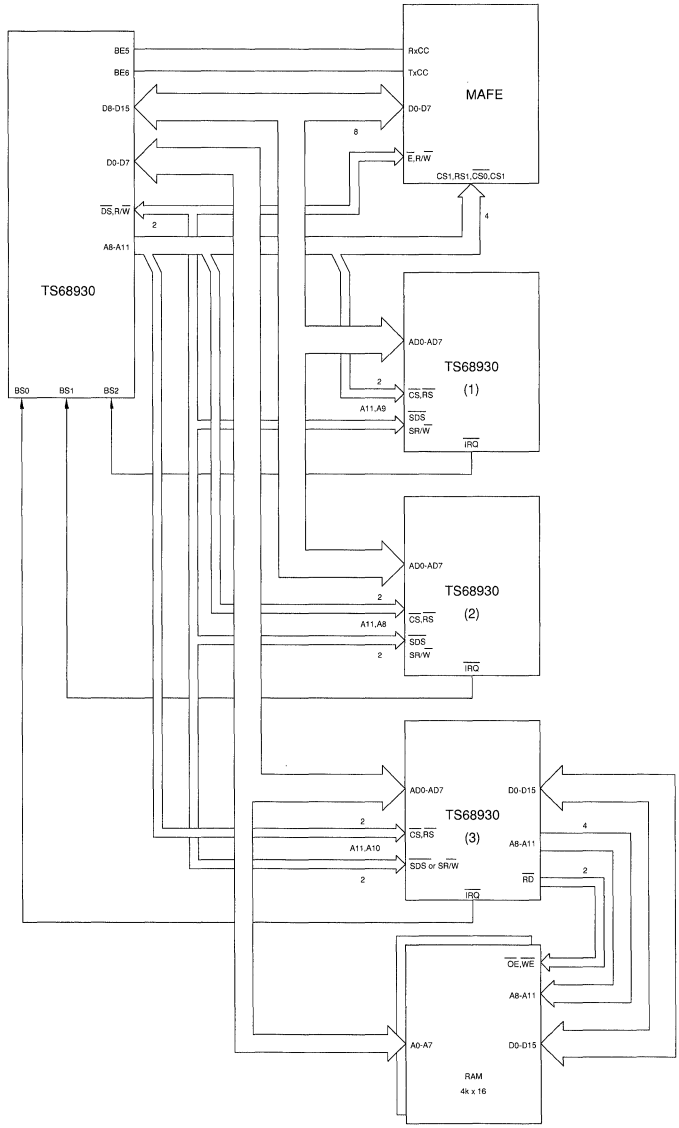
Figure 14 : Configuration Example : 3 TS68930 + RAM.



A_{11}	A_{10}	A_9	A_8	
0	1	0/1	1	**TS68930** (1)
0	1	1	0/1	**TS68930** (2)
1	0	X	X	**RAM**

M88TS68930-19

Figure 15 : Configuration Example 4 TS68930 + MAFE + RAM.



A_{11}	A_{10}	A_9	A_8	
1	0	X	X	**MAFE**
0	1	0/1	1	**TS68930** (1)
0	1	1	0/1	**TS68930** (2)
0	0/1	1	1	**TS68930** (3)

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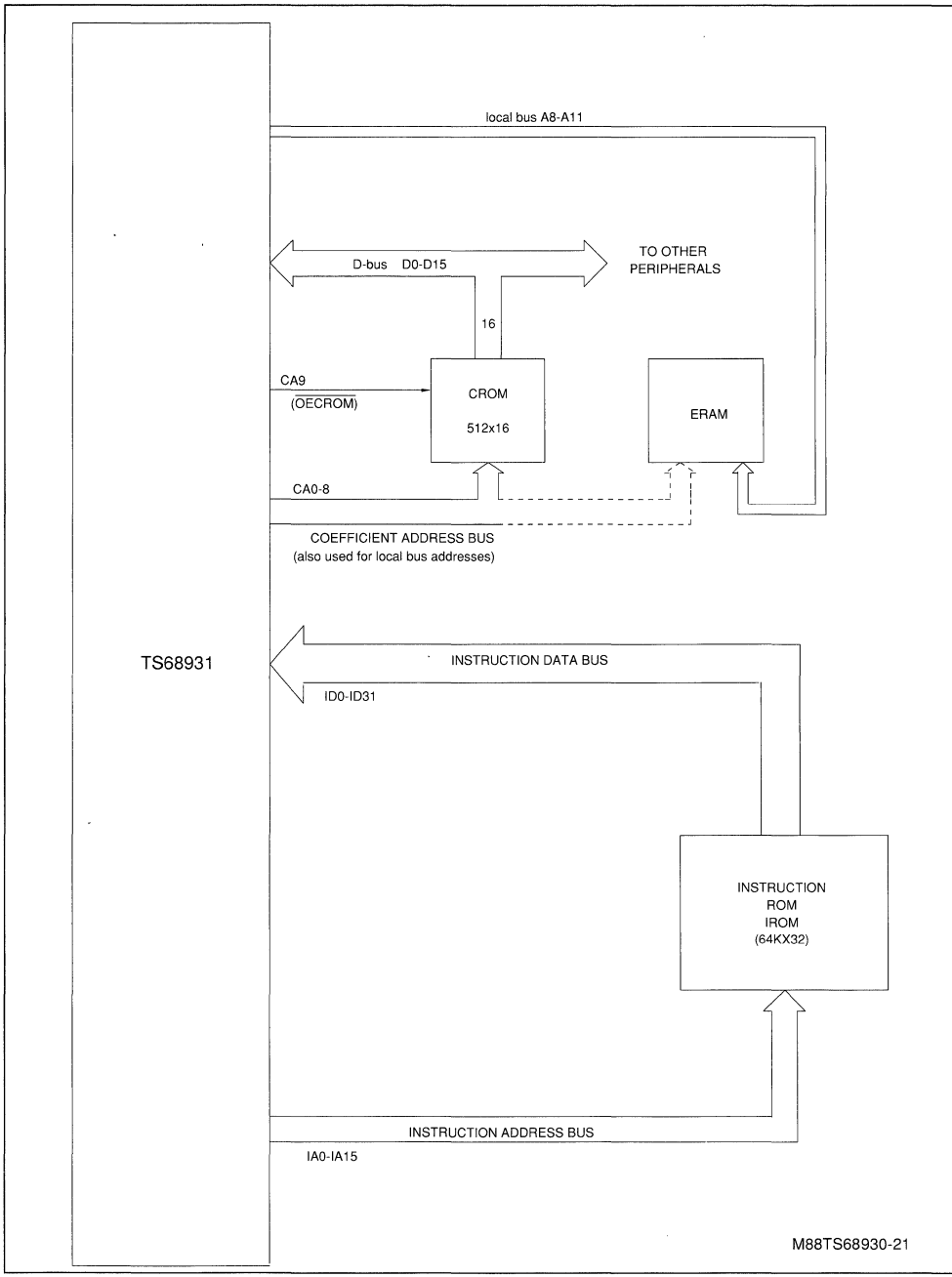
Figure 16 : Interfacing CROM, IROM to ST18931.



5. INSTRUCTION SET

Symbol	Type	Operation	Number of Cycles	
			REAL	CPLX DBPR
OPIN	Calculation Instruction with Indirect Addressing	This instruction refers to operands indirectly addressed.	1	2
OPDI	Calculation Instruction with Direct Addressing	The operand sourcing the L-BUS is directly addressed.	1	2
OPIM	Calculation Instruction with Immediate Operand	An immediate operand is read on R-BUS.	1	2
ASR ASL LSR ROR	General Shift Instruction	The operand sourcing the L-BUS can be shifted/rotated by 0 → 15 bits.	1	2
BRI	Immediate Branch Instruction	Conditional/unconditionnal branch to direct address.	2	2
BRC	Computed Branch Instruction	Conditional/unconditional branch to computed address.	2	2
SVR TFR	Data Transfer Instruction	This instruction is used to save register contents in external or internal RAM.	1	2
INI	Initialization and Control Instruction	Pointers, acces mode register, loop counter, mode initialization.	1	2

INSTRUCTION SET LANGUAGE DEFINITIONS

LDT	Load L-BUS source into Transfer Register T
R SRC	R-BUS Source
L SRC	L-BUS Source
SL	ALU Input Selection Left Side
SR	ALU Input Selection Right Side
ALU DST	ALU Output Destination
ALU CODE	ALU Codes
LDM	Load L-BUS Source into Multiplier Input M
LDN	Load R-BUS Source into Multiplier Input N
Z SRC	Z-BUS SOURCE
Z DST	Z-BUS DESTINATION
ZT	Load Z-BUS into Transfer Register T
ACE	Post Incrementation Pointers CROM or ERAM
AY	Post Incrementation Pointers YRAM
AX	Post Incrementation Pointers XRAM
BRA	Branch Address Source
FT	False/true Condition
SVPC	Save Program Counter
JDST	Destination Register for J Constant
KDST	Destination Register for K Constant
MODE	Operating Mode
SAT	Saturation Flag
ADOF	Ever add Flag
J Constant	8-bit Constant used to initialize registers
K Constant	12-bit constant used to initialize registers

5.1 OPERATING CODE FORMATS

Fig. 17 : OPIN : Calculation Instruction with Indirect Addressing.

Bit	Field	Operations and Codes
31 30	OP CODE	00
29	LDT	0-NO LOAD, 1-LBUS → T
28 27	R SRC	00 01 10 11 (X0) (E0) (Y0) (Y1)
26 25 24	L SRC	000 001 010 011 100 101 110 111 (X0) (X1) (Y0) RIN T (E1) (C0) (C1)
23	SL	0-LBUS / 1-P
22	SR	0-RBUS / 1-A/B (refer to ALU DST)
21 20 19 18 17	ALU CODE	cf. Special Table
16 15	ALU DST	00 01 10 11 D F A B
14 13 12	Z SRC	000 001 010 011 100 101 110 111 D F A B T CCR – –
11	LDM	0-NO LOAD / 1-LBUS → M
10	LDN	0-NO LOAD / 1-RBUS → N
9 8	ACE	00 01 10 11 + 0 + 1 – – 1
7 6	AY	00 01 10 11 + 0 + 1 – – 1
5 4	AX	00 01 10 11 + 0 + 1 – – 1
3 2 1	Z DST	000 001 010 011 100 101 110 111 NONE ROUT (Y0) (Y1) (E0) (E1) (X0) (X1)
0	ZT	0-NO LOAD / 1 ZBUS → T

Fig. 18 : OPDI : Calculation Instruction with Direct Addressing.

Bit	Field	Operations and Codes
31 30 29	OP CODE	010
28 27	R SRC	00 (X0) 01 (E0) 10 (Y0) 11 (Y1)
26 25 24	L SRC	000 X 001 – 010 Y 011 RIN 100 T 101 E 110 – 111 C
23	Z SRC	0-D / 1-F
22	SR	0-RBUS / 1-A
21 20 19 18 17	ALU CODE	cf. Special Table
16	ALU DST	0-F / 1-A
15 14 13 12 11 10 9 8 7 6 5 4	LBUS DIRECT ADDRESS	MSB LSB
3 2 1 0	Z DST	0000 NONE 0010 ROUT 0100 (Y0) 0110 (Y1) 1000 (E0) 1010 (E1) 1100 (X0) 1110 LCR 0001 X0 0011 X1 0101 Y0 0111 Y1 1001 E0 1011 E1 1101 C0 1111 C1

Fig. 19 : OPIM : Calculation Instruction with Immediate Operand.

Bit	Field	Operations and Codes
31 30 29 28 27	OP CODE	01110
26 25 24	L SRC	000 (X0) 001 (X1) 010 (Y0) 011 RIN 100 T 101 (E1) 110 (C0) 111 (C1)
23	SL	0-LBUS / 1-P
22	SR	0-RBUS / 1-A
21 20 19 18 17	ALU CODE	cf. Special Table
16	ALU DST	0-F / 1-A
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	IMMEDIATE VALUE	MSB LSB

Fig. 20 : ASR, LSL, LSR, ROR, Shift Instructions.

Bit	Field	Operations and Codes	
31 30 29 28 27	OP CODE	01111	
26 25 24	L SRC	000 001 010 011 100 101 110 111 X – Y RIN T E – C	
23	SL	0-LBUS / 1-P	
22 21	ALU CODE	00 01 10 11 ASR LSL LSR ROR	**NOTE** : When LSR, ASR, ROR shift value is complemented to 2.
20 19 18 17	SHIFT VALUE	0000 0001 ..... 1111 0 1 15	
16	ALU DST	0-F / 1-A	
15 14 13 12 11 10 9 8 7 6 5 4	LBUS DIRECT ADDRESS	MSB LSB	
3 2 1 0			

Fig. 21 : BRI : Branch Immediate Instruction.

Bit	Field	Operations and Codes
31 30 29	OP CODE	100
28	BRA	0-IR, 1-RAS
27	FT	0-FALSE, 1-TRUE
26 25 24 23	COND	CF Special Table
22	SVPC	0-NO SVPC, 1-PC → RAS*
21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6	BRANCH ADDRESS	MSB LSB
5 4	AX	00 01 10 11 + 0 + 1 − − 1
3 2 1	Z DST	000 001 010 011 100 101 110 111 NONE − [Y0] [Y1] − − [X0] [X1]
0	ZT	0 NO LOAD, 1-ZBUS → T

* The PC write operation in X or YRAM (defined by Z DST) is realized if the branching is really executed.

Fig. 22 : BRC : Branch Computed Instruction.

Bit	Field	Operations and Codes
31 30 29 28	OP CODE	1010
27	FT	0-FALSE, 1-TRUE
26 25 24 23	COND	CF Special Table
22	SVPC	0-NO SVPC, 1-PC → RAS*
21 20		
19	RTI	0-NO RTI, 1-RAS → PC
18 17 16		
15 14 13 12	BRANCH SOURCE	000 001 010 011 100 101 110 111 NONE F A B T – – –
11 10 9 8 7 6		
5 4	AX	00 01 10 11 + 0 + 1 – – 1
3 2 1	Z DST	000 0001 010 011 100 101 110 111 NONE – [Y0] [Y1] – – [X0] [X1]
0	ZT	0-NO LOAD, 1-ZBUS → T

* See BRI.

Fig. 23 : SVR : Data Transfer Instruction.

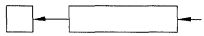
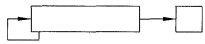
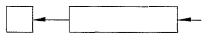
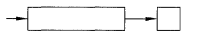
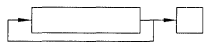
Bit	Field	Operations and Codes
31 30 29 28 27 26	OP CODE	011000
25 24 23 22	Z SRC	0000 0001 0010 0011 0100 0101 0110 0111 X0 X1 Y0 Y1 E0 E1 C0 C1 1000 1001 1010 1011 1100 1101 1110 1111 AMR LC A F D STA B –
21 20 19 18 17 16		
15 14 13 12 11 10 9 8 7 6 5 4	ZBUS DIRECT ADDRESS	MSB LSB
3 2 1	Z DST	000 001 010 011 100 101 110 111 NONE ROUT Y AMR E STR X –
0	ZT	0-NO LOAD, 1-ZBUS → T

Fig. 24 : INI : Initialization and Control Instruction.

Bit	Field	Operations and Codes			
31 30	OP CODE	11			
29 28 27	J DST	000 001 010 011 100 101 110 111 AMR LCD Y0 Y1 CRR EN* EF NONE			
26 25 24	K DST	000 001 010 011 100 101 110 111 X0 X1 LCI-LCR NONE E0 E1 C0 C1			
23 22	MODE	00 01 10 11 – REAL DBPR CPLX			
21	SAT	0 NO SATURATION MODE		1 SATURATION MODE	
20	AD0F	0 NO INVERSION		1 INVERSION LSB ADDRESS X/Y RAM	
19	J7	J7 0 YRAM NORMAL MODE		1 YRAM CIRCULAR ADDRESSING MODE	
18 17 16 15 14 13 12	J6 J5 J4 J CONSTANT J3 J2 J1 J0	(if EN) (if EN) (if EN)	0X EI = N/C 10 EI = 0 11 EI = 1	OX SIM = N/C 10 SIM = 0 (INTEL) 11 SM = 1 (MOTOROLA)	0 RDY O/N = N/C 1 RDY O/N = 1
11 10 9 8 7 6 5 4 3 2 1 0	K11 K CONSTANT K0	K7 0 XRAM Normal Mode		1 XRAM Circular Addressing Mode	

* EN (Enable) code (101) is a multi–function condition permitting independant programming of RDYOIN and SIM flags, and STA register bit EI in J field of the INI instruction.

5.2 ALU CODES

MNEMO	Function	SR	SI	CR	CI	Z	OV F	MO VF	AO VF	Code (I17-I21)
ADD	A + B	*	*	*	*	*	*	*	*	00010
ADDC	A + B + CARRY	*	*	*	*	*	*	*	*	00011
ADDS	B + A/16	*	*	*	*	*	*	*	*	00001
ADDX	B + A* (COMPLEX CONJUGATE)	*	*	*	*	*	*	*	*	01010
AND	A • B	*	*	0	0	*	0		*	01110
ASL	CARRY  0	*	*	*	*	*	*		*	01011
ASR	 CARRY	*	*	*	*	*	0		*	01111
CLR	CLEAR	0	0	0	0	1	0		0	10011
COM	COMPLEMENT A	*	*	0	0	*	0		*	10110
COM	COMPLEMENT B	*	*	0	0	*	0		*	11000
LCCR	LBUS –> CCR	*	*	*	*	*	*	*	*	01001
LSL	CARRY  0	*	*	*	*	*	0		*	11011
LSLB	LSL BYTE	*	*	*	*	*	0		*	11001
LSR	0  CARRY	*	*	*	*	*	0		*	00111
LSRB	LSR BYTE	*	*	*	*	*	0		*	11010
NOP										00000
OR	A ∧ B	*	*	0	0	*	0		*	01101
RCE	EXECUTE RC	*	*	*	*	*	*	*	*	10001
RCER	EXECUTE RC / LOAD NEW CODE	*	*	*	*	*	*	*	*	10000
RCR	LOAD RC									10010
ROR	 CARRY	*	*	*	*	*	0		*	10111
SBC	A + $\overline{B}$ + CARRY	*	*	*	*	*	*	*	*	00101
SBCR	$\overline{A}$ + B + CARRY	*	*	*	*	*	*	*	*	01000
SET		*	*	0	0	0	0		0	11100
SUB	A + $\overline{B}$ + 1	*	*	*	*	*	*	*	*	00100
SUBR	$\overline{A}$ + B + 1	*	*	*	*	*	*	*	*	00110
TRA	TRANSFER A	*	*	0	0	*	0		*	10100
TRA	TRANSFER B	*	*	0	0	*	0		*	10101
XOR	A ⊕ B	*	*	0	0	*	0		*	01100
SUBS	B + $\overline{A}$/16 + 1	*	*	*	*	*	*	*	*	11101

Notes : 1. A B refer to ALU inputs (respectively LSIDE, RSIDE) not to accumulators A/B.
2. In ASL the OVF bit is equivalent to exclusive OR of bit 14 and 15.

5.3. TEST CONDITIONS

True Condition	False Condition	Code
BE3	No BE3	0100
BE4	No BE4	0010
BE5	No BE5	0011
BE6	No BE6	0001
Branch Always	Branch Never	0000
BS0	No BS0	1100
BS1	No BS1	1101
BS2	No BS2	1110
CI	No CI	1010
CR	No CR	0110
MOVF	No MOVF	1011
OVF	No OVF	0111
RDYOIN	No RDYOIN	1111
SI	No SI	1001
SR	No SR	0101
Z	No Z	1000

5.4. AMR AND STA REGISTERS

AMR (Access Mode Register)

6	5	4	3	2	1	0
MASK	BA BE5	$\overline{\text{DTACK}}$ BE6	T M	$\overline{\text{SB}}$ CB	$\overline{\text{SL}}$ PS	SE0

STA (Status Register)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SR	SI	CR	CI	Z	OVF	MOVF	AOVF	OVFM	EF	SAT	MODE		XC	YC	
CCR									STR						

CONDITION CODE REGISTER (CCR)

Name	Function	Description
SR	Sign Real	Set if the MSB of the ALU result is 1. Cleared otherwise.
SI	Sign Imaginary	Set if the MSB of the ALU imaginary result is 1 (in complex mode). Cleared otherwise.
CR	Carry Real	Set if a carry is generated out of the MSB of the result for arithmetic and shift operations. Cleared otherwise.
CI	Carry Imaginary	Set if a carry is generated out of the MSB of the imaginary part of the result for complex arithmetic and shift operations. Cleared otherwise.
Z	Zero	Set if the ALU result equals zero. In complex mode it is set if both real and imaginary parts are equal to zero.
OVF	Overflow	Set if there was an arithmetic overflow. This implies that the result cannot be represented in the operand size. In complex mode it is set for an overflow of either real or imaginary part. Cleared otherwise.
MOVF	Memorized Overflow	Set in the same conditions as overflow. Is cleared only when tested by a branch instruction.
AOVF	Advanced Overflow	Exclusive OR of bit 14 and 15 of the ALU. If there was an arithmetic overflow on half capacity (15 bits in real/complex mode, 31 bits in double precision mode). Is memorized and cleared by LCCR ALU instruction.
OVFM	Overflow Multiplier	Set if the multiplier has overflowed. Only meaningful for complex multiplication. Is memorized and cleared by LCCR ALU instruction.

STATE REGISTER (STR)

Name	Function	Description
EF	Empty FIFO	Set if FIFO is empty. Cleared otherwise.
SAT	Saturation Flag	Set if the TS68930 is programmed in saturation mode. In this configuration, the processor will behave as follows : Positive overflow : ALU result forced to 7FFF. Negative overflow : ALU result forced to 8000. This feature does not apply to double precision mode. This bit is cleared otherwise.
MODE (2bits)	Operating Mode	Define a real (01), complex (11) or double precision (10) mode.
XC	XRAM Circular	Circular addressing mode flag for XRAM. (see 3.3.3)
YC	YRAM Circular	Circular addressing mode flag for YRAM. (see 3.3.3)

6. ELECTRICAL SPECIFICATIONS

6.1. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}*	Supply Voltage	– 0.3 to 7.0	V
V_{in}*	Input Voltage	– 0.3 to 7.0	V
T_A	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C
P_{Dmax}	Maximum Power Dissipation	3	W

With respect to V_{SS}

Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

6.2. DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0 V ± 5 %, V_{SS} = 0, T_A = 0 °C to + 70 °C (unless otherwise specified)

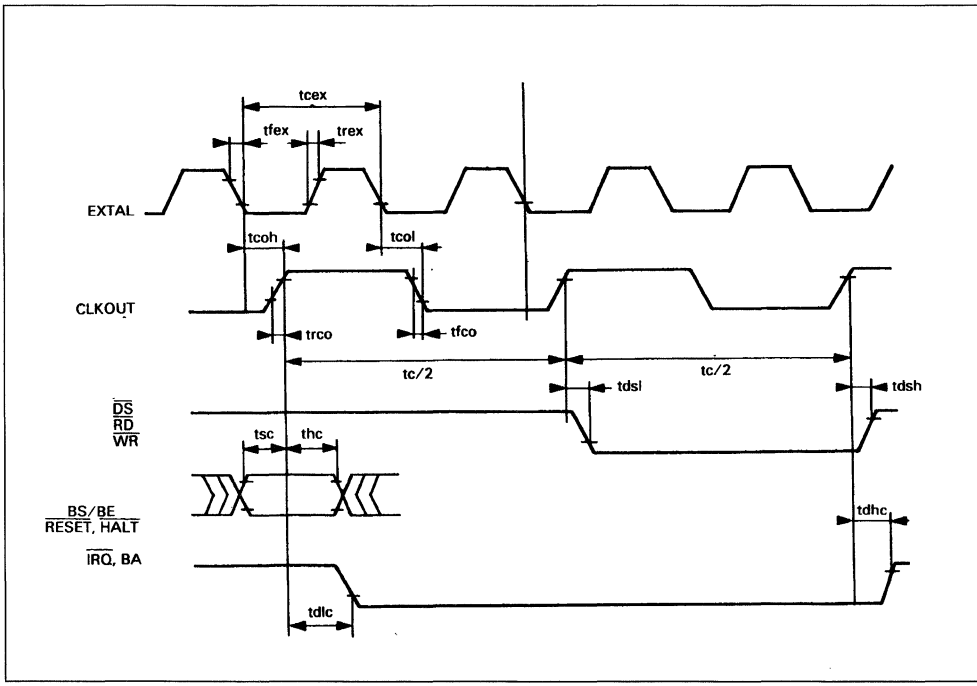
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IL}	Input Low Voltage	– 0.3		0.8	V
V_{IH}	Input High Voltage	2.4		V_{CC}	V
I_{in}	Input Leakage Current			10	µA
V_{OH}	Output High Voltage (I_{load} = – 300 µA)	2.7			V
V_{OL}	Output Low Voltage (I_{load} = 3.2 mA)			0.5	V
P_D	Power Dissipation		1.5		W
C_{in}	Input Capacitance		10		pF
I_{TSI}	Three State (off state) Input Current			10	µA

6.3. AC ELECTRICAL SPECIFICATIONS - CLOCK AND CONTROL PINS TIMING

(V_{CC} = 5.0 V ± 5 %, T_A = 0 °C to + 70 °C, see figure 6.1.)
OUTPUT LOAD = 50 pF + DC Characteristics I load
REFERENCE LEVELS : V_{IL} : 0.8 V V_{IH} : 2.4 V
V_{OL} : 0.8 V V_{OH} : 2.4 V tr, tf ≤ 5 ns for input signals

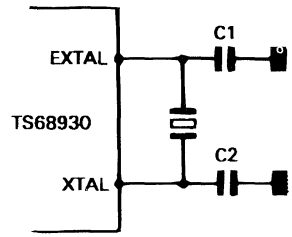
Symbol	Parameter	Min.	Typ.	Max.	Unit
tcex	External Clock Cycle Time	40		160	ns
tfex	External Clock Fall Time			5	ns
trex	External Clock Rise Time			5	ns
tcoh	EXTAL to CLKOUT High Delay		25		ns
tcol	EXTAL to CLKOUT Low Delay		25		ns
tcor	CLKOUT Rise Time			10	ns
tcof	CLKOUT Fall Time			10	ns
tdsl	CLKOUT to $\overline{DS}$, $\overline{RD}$, $\overline{WR}$ Low		5		ns
tdsh	CLKOUT to DS, RD, WR High		5		ns
tsc	Control Inputs Set-up Time (BS0...BS2, BE3...BE6, Reset, halt)	20			ns
thc	Control Inputs Hold Time (BS0...BS2, BE3...BE6, $\overline{Reset}$, $\overline{halt}$)	10			ns
tdlc	CLKOUT to Control Output Low ($\overline{IRQ}$, BA)			50	ns
tdhc	CLKOUT to Control Output High (BA)			50	ns

Figure 25 : Clock and Control Pins Timing.



INTERNAL CLOCK OPTION

A crystal oscillator can be connected across XTAL and EXTAL. The frequency of CLKOUT : tc/2 is half the crystal fundamental frequency.



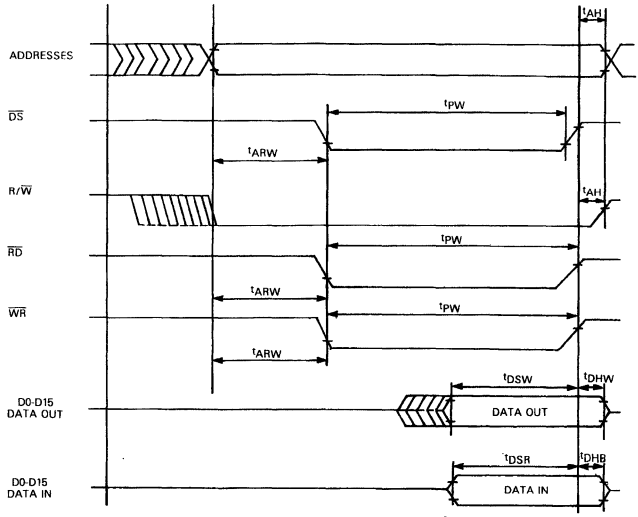
C1,C2 typical value = 10pF

6.4. AC ELECTRICAL SPECIFICATIONS - LOCAL BUS TIMING

(V_{CC} = 5.0 V ± 5 %, T_A = 0 °C to + 70 °C ; see figure 6. 2.)

Symbol	Parameter	Min.	Max.	Unit
t_{PW}	$\overline{RD}$, $\overline{WR}$, $\overline{AS}$ Pulse Width	1/2 tc – 15	1/2 tc	ns
t_{AH}	Address Hold Time	10		ns
t_{DSW}	Data Set-up Time, Write Cycle	25		ns
t_{DHW}	Data Hold Time, Write Cycle	10		ns
t_{DSR}	Data Set-up Time, Read Cycle	20		ns
t_{DHR}	Data Hold Time, Read Cycle	5		ns
t_{ARW}	Address Valid to $\overline{WR}$, $\overline{AS}$, $\overline{RD}$ Low	1/2 tc – 40		ns

Figure 26 : Local Bus Timing Diagram.



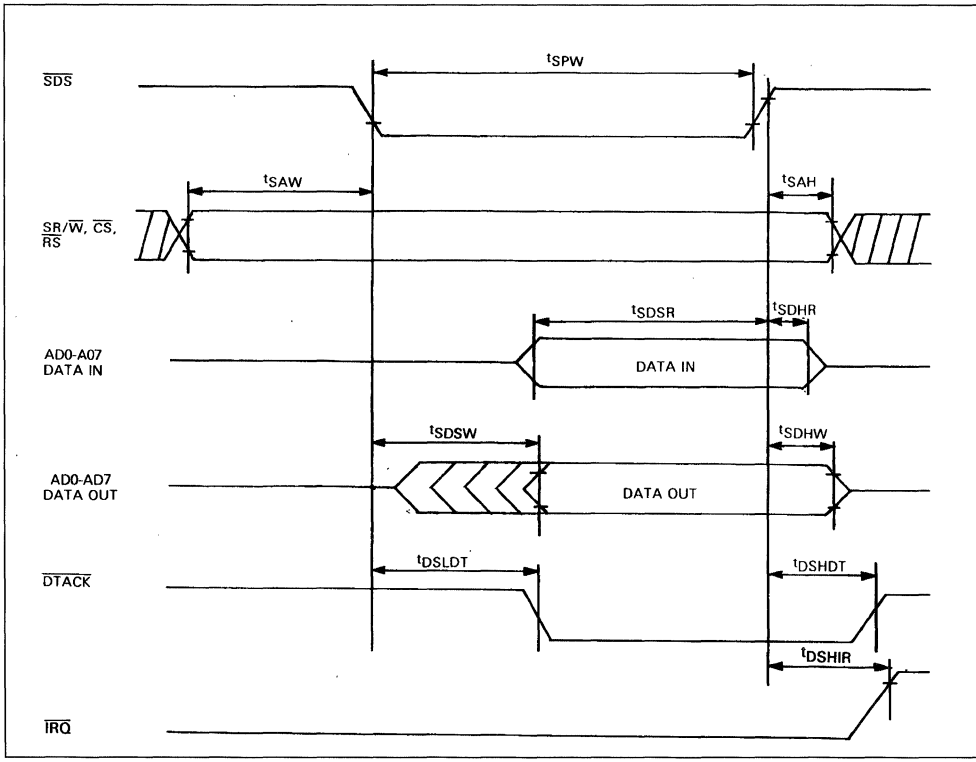
6.5. AC ELECTRICAL SPECIFICATIONS - SYSTEM BUS TIMING

(V_{CC} = 5.0 V ± 5 %, T_A = 0 °C to + 70 °C ; see figure 6. 3.)

Symbol	Parameter	Min.	Max.	Unit
t_{SPW}	$\overline{SDS}$ Pulse Width	60		ns
t_{SAW}	SR/$\overline{W}$, $\overline{CS}$, $\overline{RS}$ Set-up Time	20		ns
t_{SAH}	SR/$\overline{W}$, $\overline{CS}$, $\overline{RS}$ Hold after $\overline{SDS}$ High	5		ns
t_{SDSR}	Data Set-up Time, Read Cycle	20		ns
t_{SDHR}	Data Hold Time, Read Cycle	5		ns
t_{SDSW}	Data Set-up Time, Write Cycle		35	ns
t_{SDHW}	Data Hold Time, Write Cycle	10	50	ns
t_{DSLDT}	$\overline{SDS}$ Low to $\overline{DTACK}$ Low		50	ns
t_{DSHDT}	$\overline{SDS}$ High to $\overline{DTACK}$ High*		50	ns
t_{DSHIR}	$\overline{SDS}$ High to $\overline{IRQ}$ High		50	ns

* DTACK is an open drain output test load include RL = 820Ω at Vcc

Figure 27 : System Bus Timing Diagram.

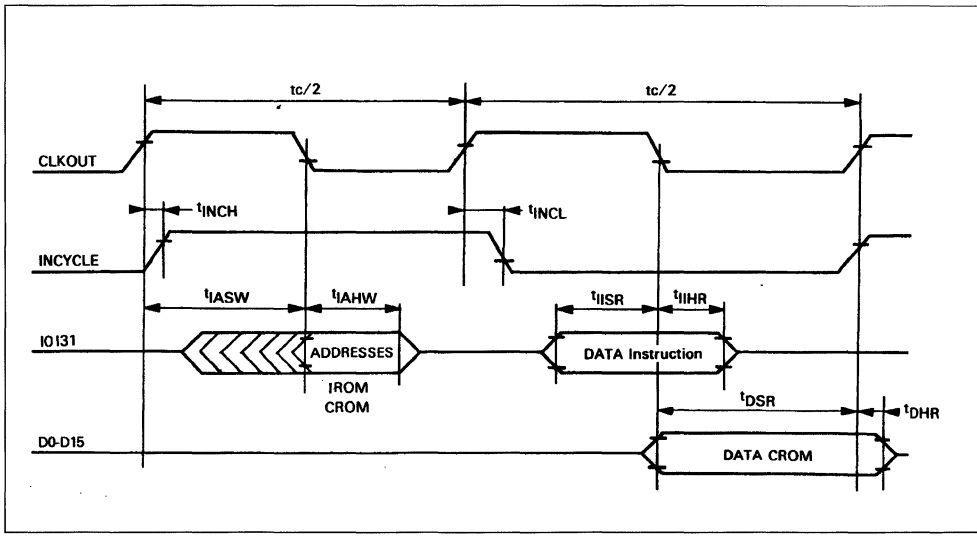


6.6. AC ELECTRICAL SPECIFICATIONS - INSTRUCTION BUS TIMING

(V_{CC} = 5.0 V ± 5 %, T_A = 0 °C to + 70 °C ; see figure 6. 4.)

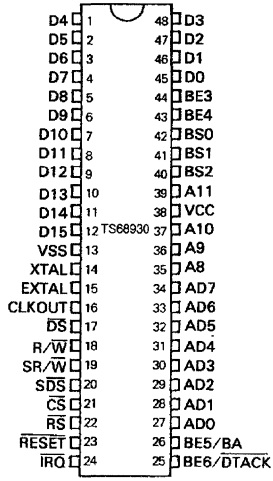
Symbol	Parameter	Min.	Max.	Unit
t_{INCH}	CLKOUT High to INCYCLE High	5	15	ns
t_{INCL}	CLKOUT Low to INCYCLE Low	5	15	ns
t_{IASW}	CLKOUT High to Address Valid		40	ns
t_{IAHW}	I-BUS Address Hold	20	40	ns
t_{IISR}	Instruction Valid	20		ns
t_{IIHR}	Instruction Hold	10		ns
t_{DSR}	CROM Data Set-up Time	tc/2 – 40		ns
t_{DHR}	CROM Data Hold Time	5		ns

Figure 28 : Bus Timing Diagram.



7. PIN CONNECTIONS

48 – Pin Dual – in – Line Package (top view)



M88TS68930-28

84 Pin Grid Array Ceramic(top view)

ID22	ID20	ID19	ID17	ID14	VDD	ID12	ID9	ID7	ID6	BE3
ID25	ID23	ID21	ID18	ID15	ID10	ID11	ID8	INCYCLE	$\overline{HALT}$	B50
ID26	ID24			ID16	VSS	ID13			BE4	BS1
ID28	ID27								BS2	A11
ID31	ID30	ID29						A10	A9	A8
ID5	ID0	ID1						$\frac{BE6}{DTACK}$	AD4	$\frac{BES}{BA}$
ID3	ID4	ID2						AD7	AD5	AD6
D0	D1								AD2	AD3
D2	D4			D12	VSS	VDD			$\overline{IRQ}$	AD1
D3	D6	D7	D10	D13	D15	EXTAL	R/$\overline{W}$	$\overline{CS}$	$\overline{RESET}$	AD0
D5	D8	D9	D11	D14	CLKOUT	XTAL	$\overline{DS}$	SR/$\overline{W}$	SDS	$\overline{RS}$

8. ORDERING INFORMATION

Part Number	Temperature Range*	Package
TS68930CP/PXXX**	0 to 70 °C	48 Pin Plastic DIL
TS68931CR	0 to 70 °C	84 Pin Grid Array

* For extended temp. range, please consult your sales office.
* * XXX is the specific number associated to a customer code.

SOFTWARE TOOLS

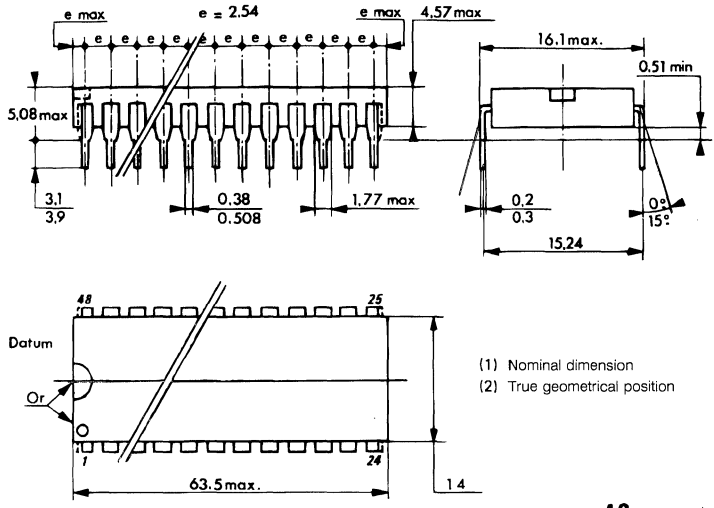
TS68930 SP-PC	Software Package Including Macroassembler Functionnal Stimulator Linker for PC
TS68930 SP-VMS	Same Software Package for VAX Machines
TS68930 SPC-PC	Same Software with C-compiler for PC
TS68930 SPC-VMS	Same Software Package with C-compiler for VAX

HARDWARE TOOLS

TS68930 EMU	Stand-alone Emulator
TS68930 HDS-1	Hardware Development System 110 V Power Supply
TS68930 HDS-0	Hardware Development System 220 V Power Supply
TS68930 EPR	EPROM Simulation Module for TS68930

9. PACKAGE MECHANICAL DATA

48 PINS – PLASTIC DIP



APPENDIX A

DEVELOPMENT TOOLS

DEVELOPMENT PROCESS

The development process of a digital signal processing application using the TS68930 or TS68931 is supported by a complete range of dedicated software and hardware tools which includes macroassembler, linker, simulator, C compiler and optimizer (respectively TS68930SP or TS68930SPC), standalone emulation card TS68930EMU, multiprocessor hardware development system TS68930HDS, EPROM emulation module, TS68930EPR.

SOFTWARE TOOLS

All the development softwares run on the most common computers, such as IBM-PC or AT® , under MS-DOS® or VAX® , VMS® , UNIX® or ULTRIX operating systems.

The macroassembler supports conditional assembly, high level language facilities for loop definition and generates all the files for simulation, emulation and PROM programming.

The functional simulator provides step by step execution, break on address and data values, access to all internal registers and interface to I/O files (ADX, DAC, test inputs).

The linker provides modular programming facilities.

The library consists of macros, basic DSP routines etc... and provides additional help to user's for their applications.

The C language compiler offers high-level language facilities which meets the advanced requirements (parallelism, pipe-line, three computation modes, 32-bit instruction set) of the TS68930/31.

HARDWARE TOOLS

All the hardware tools are designed to provide ease of use and minimum learning time by utilizing menu driven and DSP specific emulation features.

TS68930 EMU and TS68930 HDS have in common :

- Full speed emulation of TS68930 and TS68931
- Use of internal, external or application clock
- 20 breakpoints (stops at defined addresses)
- 8 complex breakpoints (stop after N address X and M address Y)
- Realtime trace of internal resources
- Emulation probes (for TS68930 or TS68931)
- Menu driven operation (about 100 commands)
- Resident Assembler/Disassembler with full screen editor
- Symbolic debbuging
- Direct link with PROM programmers

Emulator specific features.

The TS68930EMU is a low cost, stand-alone emulator providing advanced emulation features such as real-time trace. It can be driven via a RS232C link by a terminal or an IBM-PC^R and offers :

- 8K program memory (expandable to 64K)
- 2K x 16-bit data RAM
- A wire-wrapping area
- Full speed 100ns cycle emulation
- 2RS232C serial ports
- Complex conditions break-points

Hardware development station features :

The TS68930 HDS is a hardware development station, aimed at the development of multiprocessor applications. Up to four pairs of emulator boards, and logic analyser boards can be combined to match exactly the user needs :

- CMOS memory for backup of configuration
- 64K x 32 program memory
- 4K x 16 data RAM
- A logic analyser with :

* 2K x 19 bit for trace of TS68930/31 bus and 15 external inputs

* Synchronous analyzer on program and local buses

* Asynchronous analyzer on system bus or external inputs

* Triggering conditions (Address bus with count, data bus external branch inputs, mailbox exchanges, external inputs).

EPROM module.

The TS68930EPR is a small-sized module which uses the perfect compatibility between TS68930 and TS68931. The module uses a TS68931 and fast EPROM memories to emulate in real time a ROM masked TS68930 during prototyping or field tests to minimize hardware developments. The module is plug and function compatible with TS68930 pin out.

APPENDIX B

MASKING INFORMATION

The information required by SGS-THOMSON to realize a customer masked version of the TS68930 are provided below.

The files for masking must include program ROM content and coefficient ROM content. They can be transferred on EPROMS, 5" 1/4 floppy disks, magnetic tapes (VAX/VMS format) or by link to SGS-THOMSON Microelectronics. This must be done in conjunction with your local sales office or representative indications.

VERIFICATION MEDIA

All original pattern media are filed for contractual purpose and are not returned. A computer listing of the ROM content code will be generated and returned to the customer with a listing verification form. The listing should be carefully checked and the approval form completed, signed and returned to SGS-THOMSON Microelectronics. The returned verification form is the contractual agreement for generation of the customer masks and batch manufacturing.

VERIFICATION UNITS

Ten engineering samples containing the customer ROM patterns will be sent for program verification. These samples will be engineering samples and must be kept by user as reference parts.

DIGITAL SIGNAL PROCESSOR
CUSTOMER ORDERING SHEET

COMMERCIAL REFERENCE* : .TS68930CP/XXX...

CUSTOMER'S MARKING : .....

COMPANY : .....

ADDRESS : .....

PHONE : .....

PATTERN MEDIAS :

O EPROMS

O 5 1/4" FLOPPY

O MAGNETIC TYPE-

O OTHER*

OPTION :

O WATCHDOG

YEARLY QUANTITY FORECASTED :

START OF PRODUCTION DATE :

FOR A SHIPMENT PERIOD OF :

Customer Contact Name **Date** **Signature**

APPENDIX C

SUMMARY OF RESOURCES PER FUNCTION

OPERATING MODES

Symbol	Function	Resource	Paragraph Nb
MODE	2-bit register defining the operating mode (real/complex/double precision)	Access Mode Register	

OPERATING UNIT

Symbol	Function	Resource	Paragraph Nb
ALU	2 Port 16-bit Arithmetic Logic Unit 5 Possible Sources. 4 Possible Destinations. 30 ALU Codes Works on 32-bit. Data in 2 Machines Cycles.	Arithmetic Logic Unit	3. 2. 1
D	ALU Output Register		
BS	Variable 0 – 15-bit right shift, left shift, right rotation barrel shifter.	Barrel Shifter	3. 2. 2
MULT	16 x 16 → 32 parallel pipeline multiplier + 16-bit adder/substractor, used in complex Multiplications.	Pipeline Multiplier	3. 2. 3
M, N	2 x 16-bit registers containing multiplier operands.		
P	2 x 16-bit register containing multiplier result.		
STA	16-bit register containing status of ALU, mode, status of address calculation units,enable interrupt flag.	Status	3. 2. 4
A	2 x 16-bit accumulator.	Accumulators	3. 2. 4
B	2 x 16-bit accumulator.		
F	4 x 16-bit first in first out register.	Fifo	3. 2. 4
EF	Flag. Indicates that the Fifo is empty; can be set by software.	Empty Fifo	
RC	6-bit register allowing replacement of ALU operation code by a data coming from L-BUS.	Replace Code Register	3. 2. 4
T	2 x 16-bit register providing direct transfer between L-BUS and Z-BUS.	Transfer Register	3. 2. 4
SAT	Flag indicates saturation mode.	Saturation	3. 2. 4

DATA MEMORY BLOCK

Symbol	Function	Resource	Paragraph Nb
XRAM YRAM	128 x 16-bit Random Access Memories	Data RAMs	3. 3. 1
CROM	512 x 16-bit read only memory containing coefficients or constants.	Data ROM	
XACU YACU	Arithmetic units providing address incrementation, decrementation and automatic loop. XACU is dedicated to XRAM. (8 bits) YACU is dedicated to YRAM. (7 bits)	Address Calculation Units	3. 3. 2
ECACU	12-bit arithmetic unit providing incrementation, decrementation of address. Shared by CROM and ERAM (external RAM).		
XC YC	Flag indicates the circular addressing mode for XRAM. Flag indicates the circular addressing mode for YRAM.	XRAM Circular Flag YRAM Circular Flag	3. 3. 3
X0, X1 X	2 x 8-bit registers used for indirect addressing of XRAM Supplementary register used for circular addressing.	Pointers	3. 3. 4
Y0, Y1 Y	2 x 7-bit registers used for indirect addressing for YRAM. Supplementary register used for circular addressing.		
C0, C1	2 x 9-bit register used for indirect addressing of CROM.		
E0, E1	2 x 12-bit registers used for indirect addressing of ERAM.		

CONTROL BLOCK

Symbol	Function	Resource	Paragraph Nb
IROM IR	1280 x 32-bit word read-only-memory containing program code and immediate data for TS68930 (ref section 6. 6 for TS68931) 32-bit register containing instruction.	Instruction ROM Instruction Register	3. 4. 2
PC	Register containing address of program memory.	Program Counter	3. 4. 3
SEQ	The sequencer can test directly 16 conditions programmed on a high or low state and the sequencer controls next program address defined by BRANCH, subroutine call, next instructions.	Sequencer	3. 4. 1
RAS	2 x 16-bit register for saving programm counter in case of subroutine call or interrupt.	Return Address Stack	
LC	15-bit register containing a control word for automatic loop. It is divided into the following sub-registers.	Loop Counter	3. 4. 4
LCI LCR LCD	4-bit register containing the number of instructions to be executed in the loop. 8-bit register containing the number of loops. 3-bit register containing the number of instructions between declaration and start of the loop.		
	Prevents locked states for TS68930 only.	Watchdog Circuit	3. 6. 3

INPUT/OUTPUT BLOCK

Symbol	Function	Ressource	Paragraph Nb
AMR	8-bit register defining the access mode on the local bus.	Access Mode Register	3. 5. 7
RIN ROUT	3 x 8-bit shift register. Mailbox input. 3 x 8-bit shift register. Mailbox output.	Input Register Output Register	3. 5. 6
RDYOIN	Flag used in the protocol to indicate witch processor has access to the mailbox.	Read Out Internal	3. 5. 5

DSP APPLICATION SUPPORT

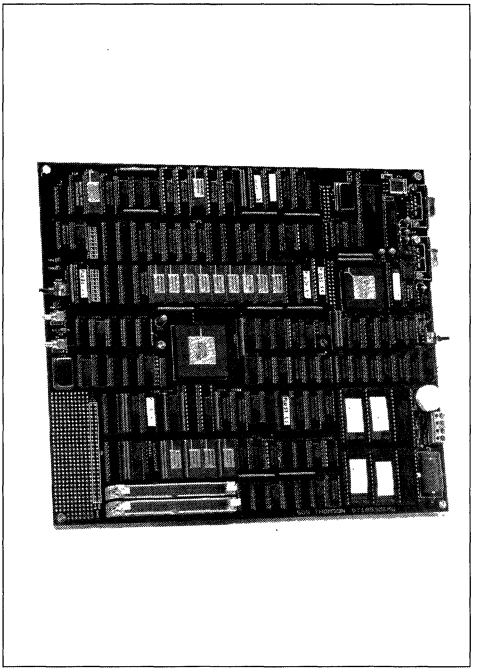
SGS-THOMSON MICROELECTRONICS

ST18930EMU

ST18930/31 DSP EMULATION BOARD

- FULL SPEED ST18930/31 EMULATION
- USER FRIENDLY MENU
- STEP BY STEP EXECUTION
- BREAKPOINTS ON PC OR DATA VALUES
- TS68000 BASED MONITOR
- FULL SCREEN SYMBOLIC ASSEMBLER AND DISASSEMBLER EDITOR
- CONTROLLED BY STANDARD TERMINAL OR IBM-PC HOSTED
- PROGRAM DOWN-LOADING FROM VAX, IBM PC-XT/AT (under kermit)
- PRINTER ECHO
- PROGRAM RAM OF 4K X 32-BIT
- COEFFICIENT RAM OF 512 X 16-BIT
- READ AND MODIFY ALL INTERNAL REGISTERS AND MEMORIES
- EXTERNAL DSP RAM OF 2K X 16-BIT
- TWO RS232 SERIAL LINKS FOR TERMINAL, HOST, PRINTER OR PROM PROGRAMMER
- CONFIGURATION SAVED ON POWER OFF
- MULTIPROCESSING REAL TIME EMULATION ALLOWED

Figure 1 : ST18930EMU.



DESCRIPTION

The ST18930EMU is a powerful stand-alone development tool intended for the emulation of the ST18930/31 DSP. The ST18930EMU board has been designed to be compatible with the "C" Compiler, Macro-Assembler, Functional Simulator and Hardware Development System (HDS) tools. The ST18930EMU allows full real-time application development.

The TS68000 based interactive monitor features a menu-driven display and also supports a full Screen Symbolic Assembler and Disassembler as well as Communication Software enabling Uplink/Downlink with VAX and IBM PC.

All software required for operation of the ST18930EMU is resident within four on-board EPROMs.

The ST18930EMU board offers three probes for connection to the target application :

- One 120-pin PGA probe for ST18931 emulation
- One 48-pin DIP probe for ST18930 emulation
- One 52-pin PLCC probe for ST18930 emulation

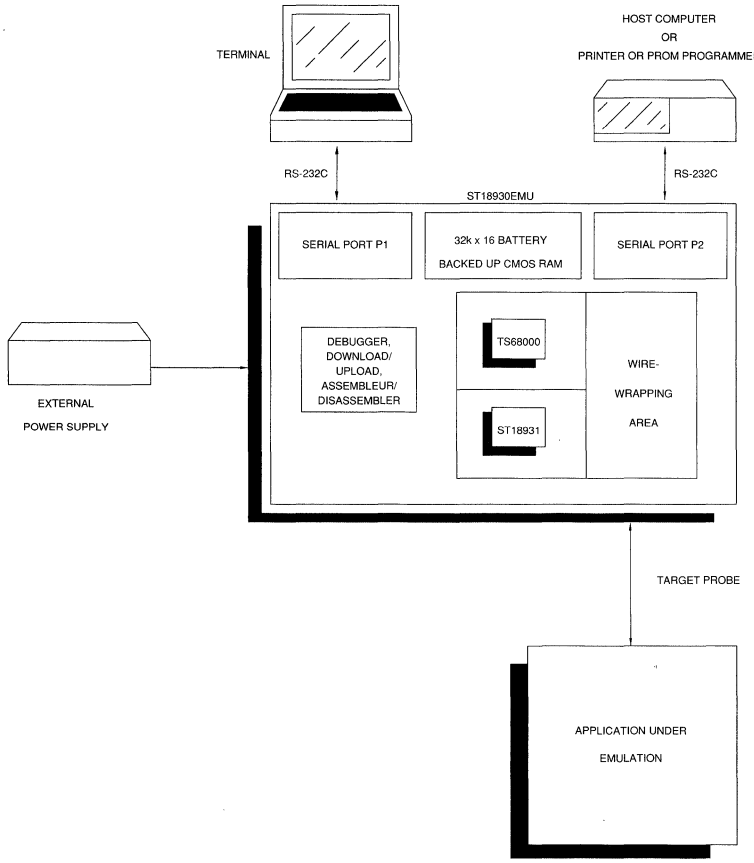
A 32K x 16 battery backed-up CMOS RAM allows an automatic saving of configuration (user program and data).

The ST18930EMU board is a powerful low-cost tool for software development, debugging, and real-time emulation of the ST18930/31.

ORDER CODES

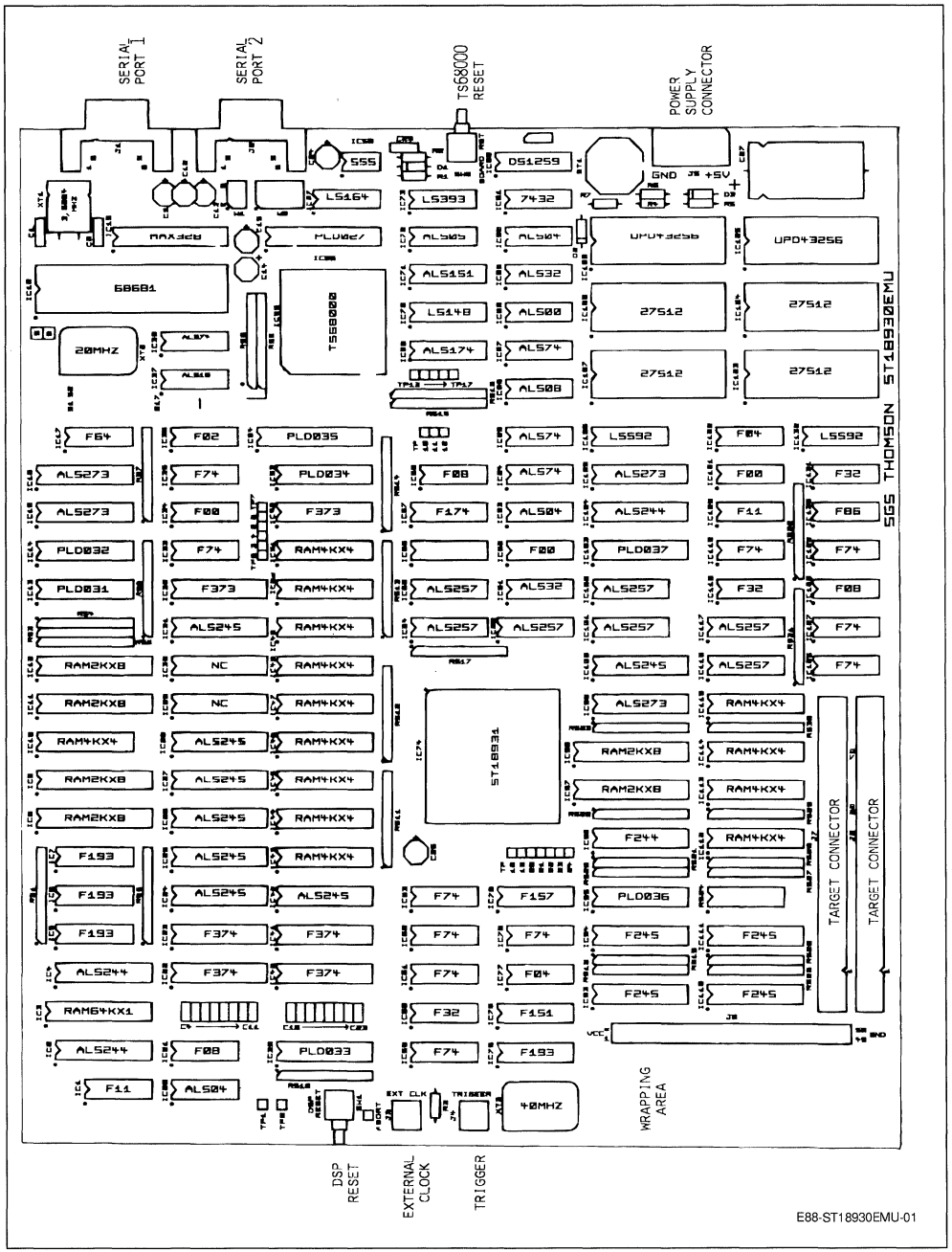
ST18930EMU

Figure 2 : ST18930EMU Complete configuration.



E88-TS68930-EMU-01

Figure 3 : ST18930EMU Board General Arrangement.



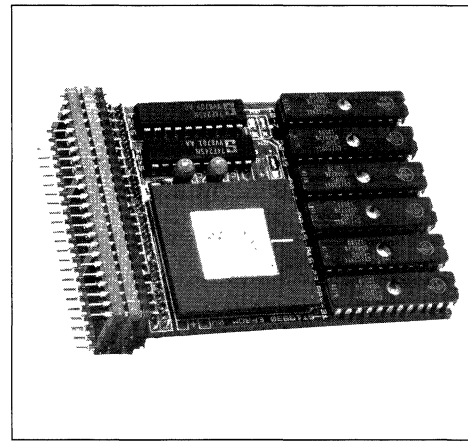
SGS-THOMSON MICROELECTRONICS

ST18930EPR

ST18930/31 DSP EPROM MODULE

- FULL SPEED ST18930 EMULATION
- PLUG AND FUNCTION COMPATIBLE WITH ST18930 DSP CHIP
- INCLUDES PROGRAM AND COEFFICIENT EPROMS
- VERTICAL AND HORIZONTAL PLUG-IN VERSIONS
- MULTIPROCESSOR CONFIGURATION ALLOWED
- USEFUL DURING PROTOTYPING AND FIELD APPLICATIONS
- LARGE PROGRAM CAPACITY ALLOWED (up to 8k x 32 bit)
- DELIVERED WITH SIX BLANK EPROMS (2k x 8 bit)
- COMPLEMENTARY TOOL FOR ST18930 DSP FAMILY

Figure 1 : ST18930EPR.



DESCRIPTION

The ST18930EPR module is a board which permits the replacement of the ST18930 (DSP in ROM version) by the ST18931 (DSP in ROMLESS version) with external coefficient and program Eprom memories. The ST18930EPR is the ideal and complementary tool for debugging an application at the prototype level or when the program length exceeds the 3k of the ST18930 ROM Program capacity. Another advantage provided by the ST18930EPR is to manufacture compact prototypes before ordering the final ST18930 masked version, or to develop low-quantity applications, eliminating masking cost. The ST18930EPR is designed to physically fit in the same board surface as the ST18930 device.

It allows a complete full speed emulation of the ST18930 even in multi-DSP configurations. Fast buffers are added on the data-bus and may be removed depending of the multiprocessing architecture.
The module is delivered with six blank EPROMs (2k x 8 bit). Suggested references are CYPRESS CY7C291-35WC or any compatible memories. The capacity of the program EPROM memory is 2k x 32 bit, or optionnally can be 8k x 32 bit as compared with 3k x 32 bit for the ST18930. The capacity of the coefficient EPROM memory is 512 x 16 bit. The ST18930EPR is compatible with the use of a crystal on the input pins EXTAL and XTAL, or with an external clock on the input pin EXTAL. The 5 volts power supply can be provided on the socket of the target application, or by an external power supply.

ORDER CODES

ST18930EPR-H horizontal version (surface requirement : 60 x 81mm, height : 15mm)

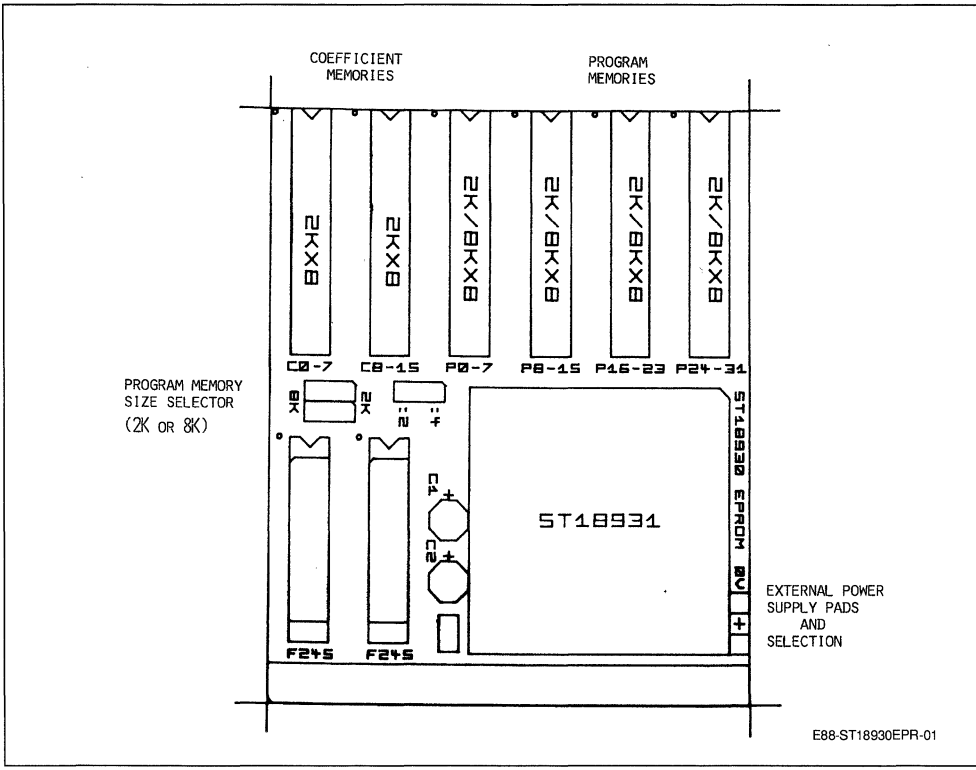
ST18930EPR-V vertical version (surface requirement : DIL 48 socket, height = 78mm)

NOTE : Several options are possible for the Eprom module (high quantity without memories or with Prom or OTP memories, or with 8k x 8 bit Eproms, or with 52-PLCC socket). Please contact your local SGS-THOMSON sales office and/or distributor.

PROGRAMMING

Using the ST18930 EMUlator or HDS monitor with "PROG" menu, the program and coefficients are down-loaded to the Prom-Programer in byte-wide sections. An EPROM is programmed with each byte-wide section. Six EPROMs are required ; 4 for the 32-bit wide Program memory and 2 for the 16-bit wide coefficient memory. The programmed EPROMs are then inserted in the EPROM-sockets according to the module layout.

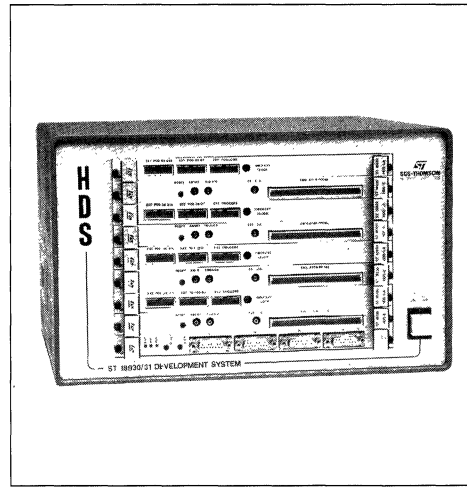
Figure 2 : ST18930EPR Module Layout.



ST18930/31 DSP HARDWARE DEVELOPMENT STATION

- EMULATION/LOGIC ANALYSIS FOR
  - ST18930 INTERNAL PROGRAM ROM
  - ST18931 EXTERNAL PROGRAM ROM
- MULTIPROCESSING
  - UP TO FOUR EMULATOR BOARDS AND FOUR OPTIONAL DEDICATED LOGICAL ANALYZER BOARDS
- MULTIUSER
  - UP TO FOUR INDEPENDANT EMULATION/LOGIC ANALYZER STATIONS
- USER-FRIENDLY INTERFACE
  - REDUCED LEARN-TIME
  - MENU DRIVEN
  - SYMBOLIC DEBUGGING
  - RESIDENT ASSEMBLER WITH FULL SCREEN EDITOR
  - CONTROLLED BY STANDARD TERMINALS OR IBM-PC HOSTED
  - DIRECT LINK TO PROM PROGRAMMER
  - CMOS BATTERY BACKUP OF CONFIGURATION (breakpoints, mode...)
  - UPLOAD-DOWNLOAD KERMIT PROTOCOL WITH HOST (VAX, IBM-PC)
- EMULATION FEATURES
  - FULL SPEED
  - 64K PROGRAM MEMORY (32 bit wide)
  - 4K EXTERNAL DATA MEMORY, MAPPING ON A WORD BASIS
  - BREAKPOINTS ON PC VALUE
  - COMPLEX BREAKPOINTS ON DATA VALUES
  - SYNCHRO SIGNAL GENERATION AT SELECTED ADRESSES OR RANGE
  - PSEUDO REAL TIME TRACE OF INTERNAL REGISTERS WITHOUT SLOWING DOWN EXECUTION
- LOGIC ANALYZER
  - REAL-TIME TRACE (2K depth, 95 bits)
  - SYNCHRONOUS ON DSP BUSES
  - ASYNCHRONOUS ON DSP SYSTEM BUS AND ON 15 EXTERNAL INPUTS
  - MIXED MODE SYNCHRONOUS-ASYNCHRONOUS
  - TRIGGERING CONDITIONS
    - ON PROGRAM ADDRESS IN CONJUNCTION WITH MANY DIVERSIFIED CONDITIONS (N times addr. 1 followed by M times addr. 2)
    - ON LOCAL DATA BUS VALUE
    - ON EXTERNAL BRANCH DSP INPUTS CONDITIONS
    - ON START OF MAILBOX EXCHANGE
  - BEFORE, AFTER AND WINDOW TRIGGERING
  - TIME MEASUREMENT FUNCTION
  - BREAKPOINT GENERATION ON LOCAL BUS VALUE

Figure 1 : ST18930HDS.



DESCRIPTION

The ST18930HDS is specifically designed for real-time multi-DSP applications. A menu-driven user interface allows a quick learning time to completely and easily use all of the system efficiently.

The designer can add the number of emulator and logic analyzer boards to meet exactly his requirements.

The ST18930HDS enhances the large range of development tools for the SGS-THOMSON DSP family.

The ST18930HDS greatly reduces the time required for development of application softwares.

1. GENERAL PRESENTATION OF THE ST18930HDS

The ST18930HDS (Hardware Development Station) is a real-time multi-processors (up to 4) emulation system which provides a simple but extremely powerful user interface due to its interactive menu-driven organization.

The ST18930HDS is a modular system consisting of :

- a rack with power supplies, fans and standard double-Eurocard 9 slots VMEBUS backplane
- a 68010 VME bus controller board
- up to four real-time emulator boards with 64k x 32 of program memory
- up to four logic analyzer boards with 2k x 95 bit trace memory associated with each emulator board. These analyzer boards are optional and can be used or not according to the application.

The ST18930HDS includes four programmable RS232C serial ports for connection either to a terminal, printer, PROM or EPROM programmer, or host computer such as Vax or IBM-PC.

This means also that four users can work independently with four terminals, each one associated with a particular ST18930HDS emulator board.

This multi-task capability is managed by the 68010 CPU board. In case of power failure or when switching off the system, a large 64k x 8 CMOS RAM with battery back-up permits automatic saving of system configuration and user programs and data.

The connector P2 on the VME bus is normally not used by the ST18930HDS boards. So it is possible on the emulation board and by wire-wrapping to send DSP signals on connector P2. This possibility enables the user to use these signals on a double-Eurocard format application. One possible example is a D/A and A/D conversion board.

All the software management of the ST18930HDS is written in "C" language modules.

2. ORDER CODES

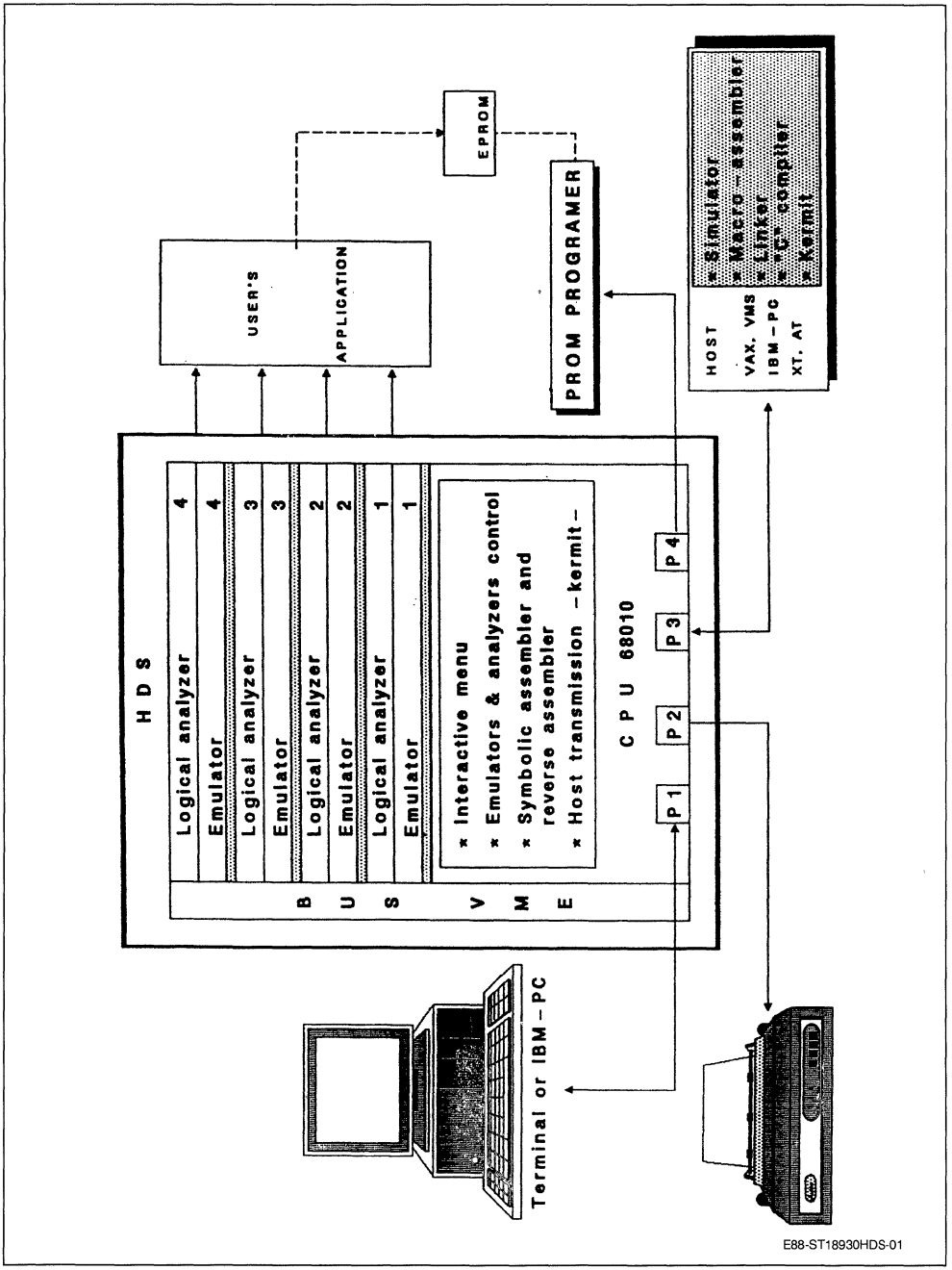
The basic configuration of the ST18930HDS includes one emulation board with its set of three probes (48-pin DIP and 52-pin PLCC for ST18930 and 120-pin for ST18931), and one logic analyzer board with its set of probes.

The ST18930HDS is available in two versions (220V or 110V). The emulation board and logic analyzer boards with their respective probes are also available as separate items to fully use the system's efficiency.*

Part number	Power supply
ST18930HDS-0	220V
ST18930HDS-1	110V

* Contact your SGS-THOMSON sales office and/or distributor

Figure 2 : ST18930HDS Complete configuration.



SGS-THOMSON MICROELECTRONICS

ST18930LIB

ST18930/31 DSP LIBRARY

- MULTIPLICATION/ACCUMULATION ROUTINES
- OPERATIONS ON COMPLEX NUMBERS
- DOUBLE PRECISION SHIFTS (32-bit Word)
- DSP FUNCTIONS :
  - Real, Complex and Adaptive Complex FIR
  - Biquadratic Filter Routine
  - Autocorrelation Routine
  - Lattice Filter Routine
- FAST FOURIER TRANSFORMS :
  - Butterfly
  - 8-point FFT
  - 64-point FFT
- ARITHMETIC FUNCTIONS :
  - Normalization and Denormalization
  - 32 X 32 Multiplication
  - Square Root
  - Division and Inversion
  - Rectangular to Polar Coordinates
  - Sine and Cosine of an Angle
- MACROS, MODULES AND HINTS FOR DSP SOFTWARE DEVELOPMENT

DESCRIPTION

The ST18930/31 DSP Module Library contains the major DSP routines required in the implementation of most DSP applications.

These routines and macros are all written in ST18930/31 source code and can readily be incorporated into the users program.

The DSP Library is available for the IBM-PC, XT, AT and VAX-VMS (1600 BPI magnetic tape) as well as in printed form.

ORDER CODES

ST18930LIB-PC	PC/MS DOS
ST18930LIB-VMS	VAX VMS

SGS-THOMSON MICROELECTRONICS

ST18930SP

ST18930/31 DSP SOFTWARE–PACKAGE

- EFFICIENT SET OF SOFWARE TOOLS WHICH INCLUDES :
  - A Macroassembler
  - A Linker
  - A Functional Simulator
- AVAILABLE FOR VAX OR PC/MS DOS
- MACROASSEMBLER'S FEATURES :
  - Macro Definition and Macro Call
  - Conditional Assembly
  - Data Memory File Generation
  - Multiple Output Format Generation
  - High-level Language Loop Facility
  - Powerful Expression Facility
- LINKER'S FEATURES :
  - Incremental Linker
  - Development of Modular and Relocatable Software
  - Use of Libraries
  - Partial Linking of Group of Modules (Incremental liker)
  - Automatic or Forced Memory Allocation in Relative Sections
  - Absolute Output Cross-references for Debugging
  - Simulation File Generation
- FUNCTIONAL SIMULATOR'S FEATURES :
  - Software Debugger without Hardware Needs
  - 1000 Instructions per Second on a VAX 785
  - Step by Step Execution
  - Breakpoint on Value or Address
  - Access to all Internal Registers and Memories
  - I/O Simulation Files
  - Detailed Help Function

DESCRIPTION

A DSP program must run as fast as possible (real-time constraint). This goal can easily be met with the SGS-THOMSON MICROELECTRONICS DSP family due to their 32-bit instructions and three data-bus structure which allow implementation and execution of sophisticated algorithms at maximum speed. However, a DSP program must also have the characteristics of any other program. It must be fast to develop, easy to read and simple to check. The SGS-THOMSON DSP software tools have been developed with these goals in mind.

The macroassembler allows the programmer to easily develop DSP algorithms at maximum speed. The linker can link a group of modules and generate an executable program. The functional simulator simulates the internal DSP operation for effective development and off-line program verification.

MACROASSEMBLER

The macroassembler allows the programmer to develop DSP algorithms in Assembly language working at maximum speed. The PC configuration needs 640 Kbits of RAM plus a hard disk.

Assembly language is a computer-oriented language for writing programs, consisting of symbolic instructions and assembler directives. In assembly instructions, the user assigns symbolic addresses to memory locations and specifies instructions by means of symbolic (mnemonic) operation codes.

The user specifies instruction operands by means of symbolic addresses and numbers.

Assembler directives are instructions to the assembler rather than instructions which will be translated into object code.

The directives have to control the assembly (END, ORG, MEMORY, INCLUDE, PROGRAM), the data definition (DEF, REF, SET, ASG) the macros (CREATE, DELETE, CHANGE, DEFAULT, LIBRARY), the conditional assembly (IF, ELSE, ELSEIF, REPT), the listing (LIST, PRINT, MAP, CROSS, HEAD, CODE, PAGE, TITLE, INPUT, OUTPUT, LINES) and the generation of binary or object files (HEXA, INTEL, MOTOROLA, NOBIN, TEKTRO, LINK).

Macro calls provide the means to create a macro language that is capable of calling source statements from other locations within the program. A macro call fetches the source statements defined by the macro and substitutes them for the macro as if they had been written in that location in the program. The obvious advantage to using macro code is that less source code must be written, and this in turn means that the programs become easier to read and debug. In addition, macros are executed faster than a comparable absolute code subroutine because no branching is involved.

Macro calls and conditional assembly provide the means to create modular programs. Those programs then can be linked together by using the DSP linker.

LINKER

The linker allows the development of modular and relocatable software. It can use libraries and provide a linking of a group of modules (incremental linker).

It adds two powerful features compared to conventional ones : it can link a group of modules which do not constitute a complete program. Then, this newest group can be used as an input for final linking. It can generate an executable program even when external references are still unsolved. This enables real-time debugging of an incomplete program without having to create empty functions to test.

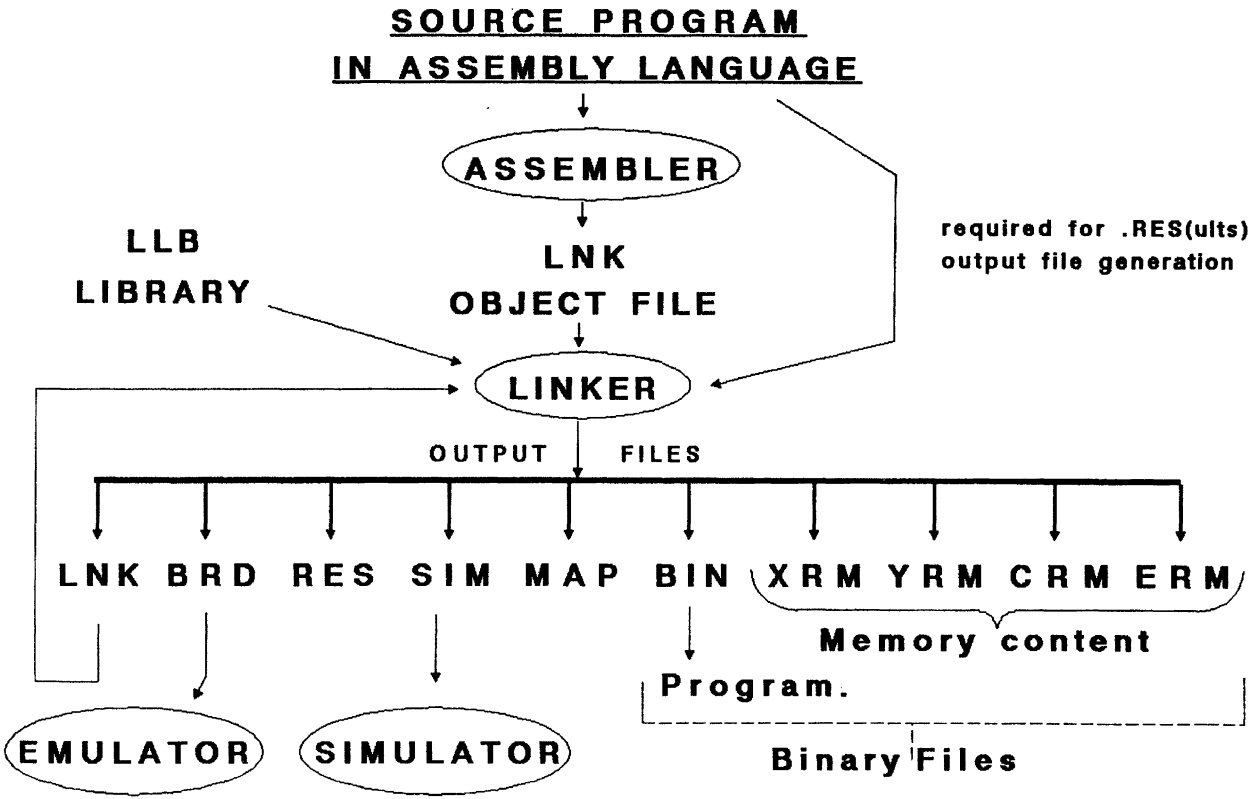
FUNCTIONAL SIMULATION

THE ST18930 Functional Simulator is a software program that simulates the internal operation of the ST18930/31 DSP for effective software development and off-line program verification . Use of the functional simulator allows debugging of ST18930/31 software without the requirement of hardware.

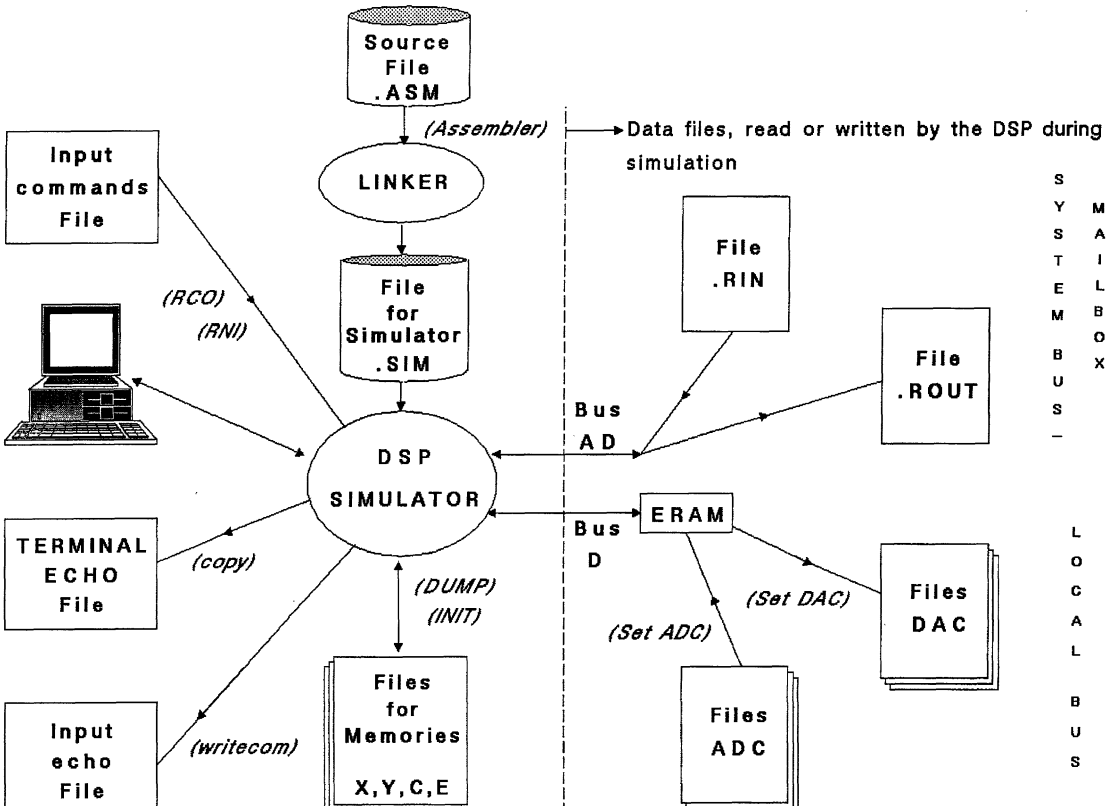
The simulator uses a coded form of the ST18930 DSP object code produced by the ST18930 linker. Simulation of A/D Converters, D/A Converters, and other conventional peripherals is accomplished using associated input and output files.

All internal registers and memories of the ST18930 can be modified during a simulation session. During execution of the program, the internal registers and memories of the simulated ST18930 are modified as the host computer interprets each instruction. Simple or high level breakpoints may be used to suspend execution at a selected point in the program so that the internal registers and memories can be inspected and/or modified.

LINKER OPERATION



SIMULATOR OPERATION



On-line help with the simulator commands is available by entering a simple HELP command.

ORDER CODES

Part Number

ST18930SP-PC Software Package on PC for ST18930/31

ST18930SP-VMS Software Package on VAX VMS for ST18930/31

SGS-THOMSON MICROELECTRONICS

ST18930SPC

ST18930/31 DSP "C" COMPILER

- UPGRADED KERNIGHAM AND RITCHIE "C" DEFINITION, I.E. RESPECT OF ANSI X3J11 STANDARD
- RUNS ON PC OR COMPATIBLE UNDER MS-DOS 3.1 OR LATER
- RUNS ON VAX UNDER VMS OPERATING SYSTEM (for UNIX or ULTRIX operating system contact your sales office)
- "FLOAT" IN RESPECT OF IEEE 754 STANDARD, "DOUBLE" AND "INTEGER" TYPES ALLOWED
- MANY FUNCTIONS IMPLEMENTED : CHARACTER AND STRING HANDLING, MEMORY MANAGEMENT, CONVERSION, MATHEMATICAL, I/O ROUTINES
- SPECIFIC RUN-TIME FOR ACCESS TO PERIPHERALS (mail-box, A/D and D/A converter...)
- SOURCE ASSEMBLER INCLUSION IN SOURCE "C" PROGRAM CAPABILITY
- INTERRUPT HANDLING
- INCLUDES PREPROCESSOR, MACROASSEMBLER AND LINKER-LOADER
- PRODUCES LOADABLE AND RUNNABLE BINARY OBJECT FILES
- HIGH LEVEL SYMBOLIC DEBUGGER

DESCRIPTION

The SGS-THOMSON Microelectronics "C" compiler used with the assembler/linker (included with the compiler) allows the possibility to write "C" source code and produces object code running on the ST18930/31 Digital Signal Processor. It takes into account all the advanced features of the ST18930/31 (parallelism, pipe-line, double precision, complex mode and 32-bit instruction set).

The high level language "C" compiler has been designed to provide the greatest flexibility of use.

User can either run the complete software with only one simple command, or run separately each software included in the package : "C" compiler, optimizer, assembler and linker.

STANDARD

THE SGS-THOMSON "C" compiler is an implementation of the ANSI X3J11 standard, which includes and exceeds Kernigham and Ritchie specification. New possibility for the processor and new class for data are allowed. For example, "CONST" allows ROM implementation for constant data.

LICENSE

The SGS-THOMSON "C" compiler is delivered under license for one user only. Upgrades of new releases will be done to each registered user, free of charge, for a duration of 12 months starting from the purchase date.

ORDER CODES

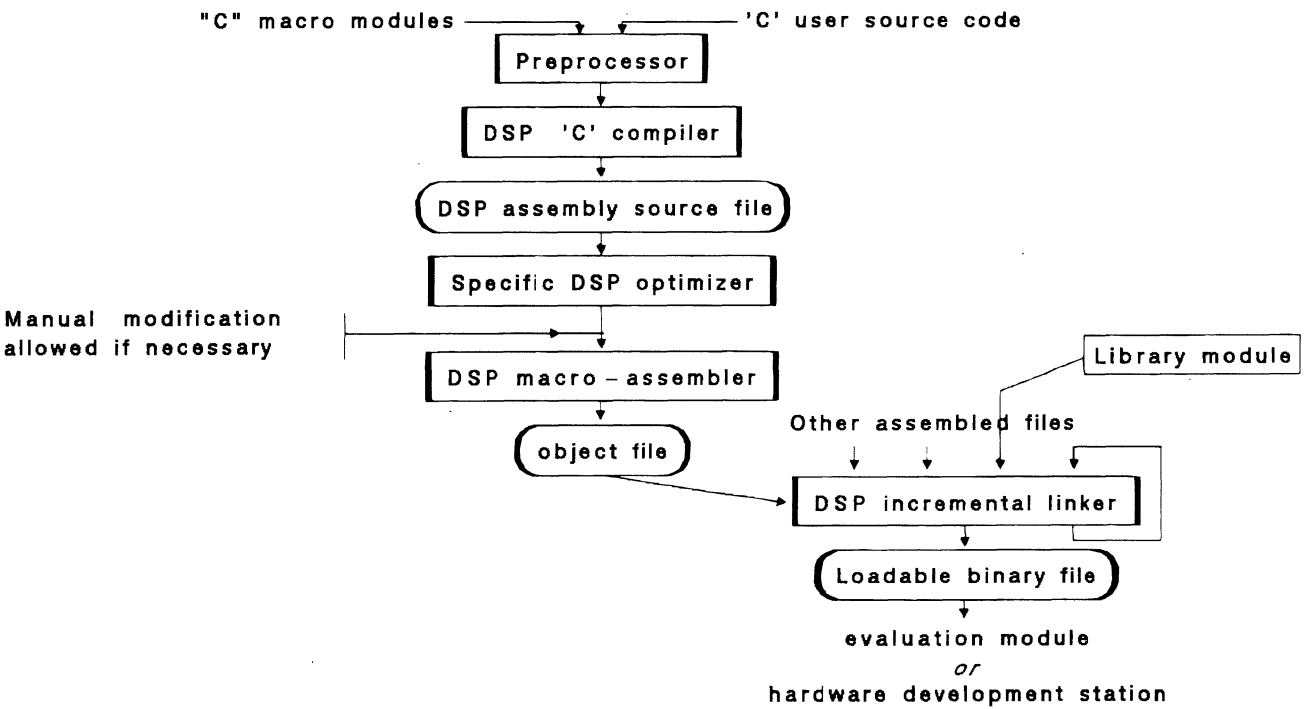
The ST18930SPC "C" compiler includes in the same commercial software-package the "C" compiler software plus the standard ST18930SP software (macroassembler, linker and functional simulator).

Part Number

- ST18930SPC-PC "C" compiler for ST18930/31 on PC/MS DOS

- ST18930SPC-VMS "C" compiler for ST18930/31 on VAX VMS.

ST18930/1
C COMPILER



SGS-THOMSON MICROELECTRONICS

TS68930EMU

TS68930/31 DSP EMULATION BOARD

- FULL SPEED TS68930/31 EMULATION (25MHz)
- USER FRIENDLY MENU
- STEP BY STEP EXECUTION
- SIMPLE AND HIGH LEVEL BREAKPOINTS
- TS68000 BASED MONITOR
- FULL SCREEN SYMBOLIC ASSEMBLER AND DISASSEMBLER EDITOR
- PROGRAM DOWN-LOADING FROM VAX, IBM PC-XT/AT
- PRINTER ECHO
- PROGRAM RAM OF 2K x 32-BIT
- COEFFICIENT RAM OF 512 x 16-BIT
- READ AND MODIFY ALL INTERNAL REGISTERS AND MEMORIES
- EXTERNAL DSP RAM OF 2K x 16-BIT
- TWO RS232 SERIAL LINKS FOR TERMINAL, HOST, PRINTER OR PROM PROGRAMMER
- MULTIPROCESSING REAL-TIME EMULATION ALLOWED

DESCRIPTION

The TS68930EMU Emulation Board is a powerful stand-alone development tool intended for the emulation of the TS68930/31 DSP. The TS68930EMU board has been designed to be compatible with the "C" Compiler, Macro-Assembler, Functional Simulator and Hardware Development System (HDS) tools. The TS68930EMU allows full real-time application development and implementation.

The TS68000 based interactive monitor features a menu-driven display and also supports a full Screen Symbolic Assembler and Disassembler as well as Communication Software enabling Uplink/Downlink with VAX, IBM PC configured as host.

All software required for operation of the TS68930EMU is resident within four on-board EPROMs.

The TS68930EMU board offers two probes for connection to the target application :

- One 84-pin PGA probe for TS68931 emulation
- One 48-pin DIP probe for TS68930 emulation

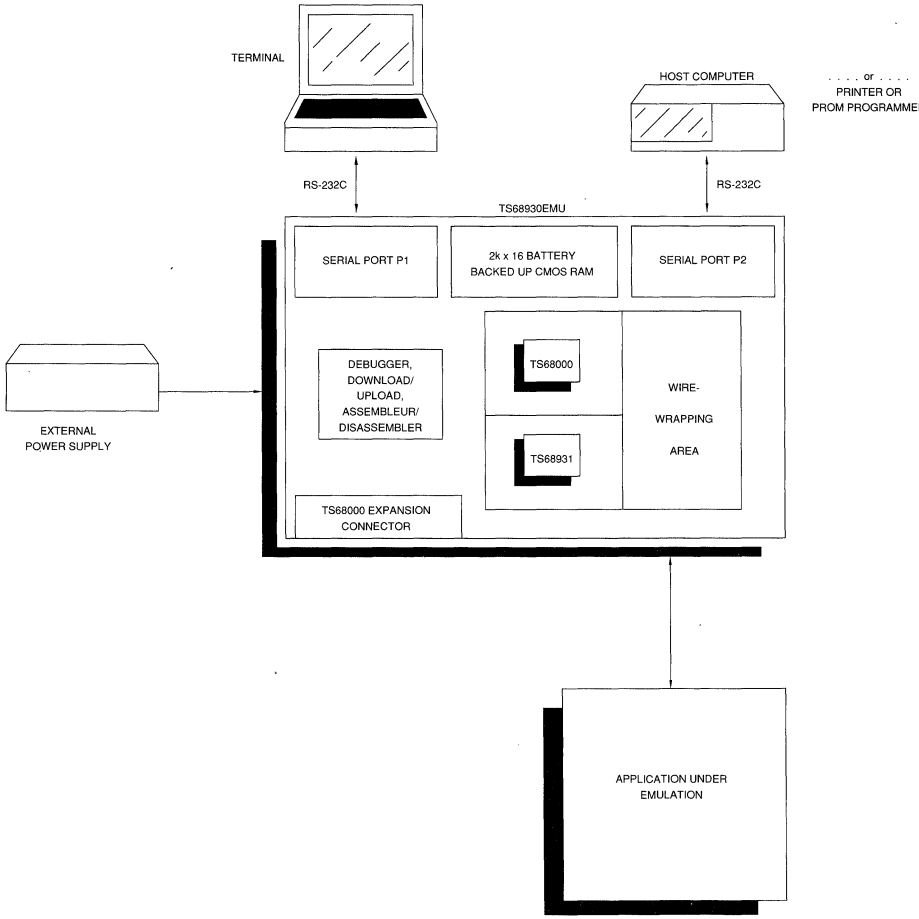
A 2K x 16 battery backed-up CMOS RAM expansion board is also supplied for use with the TS68930EMU to facilitate uploading of Program and Coefficient Memory.

The TS68930EMU board is an excellent low-cost tool for software development, debugging, and real-time emulation fo the TS68930/31.

ORDER CODE

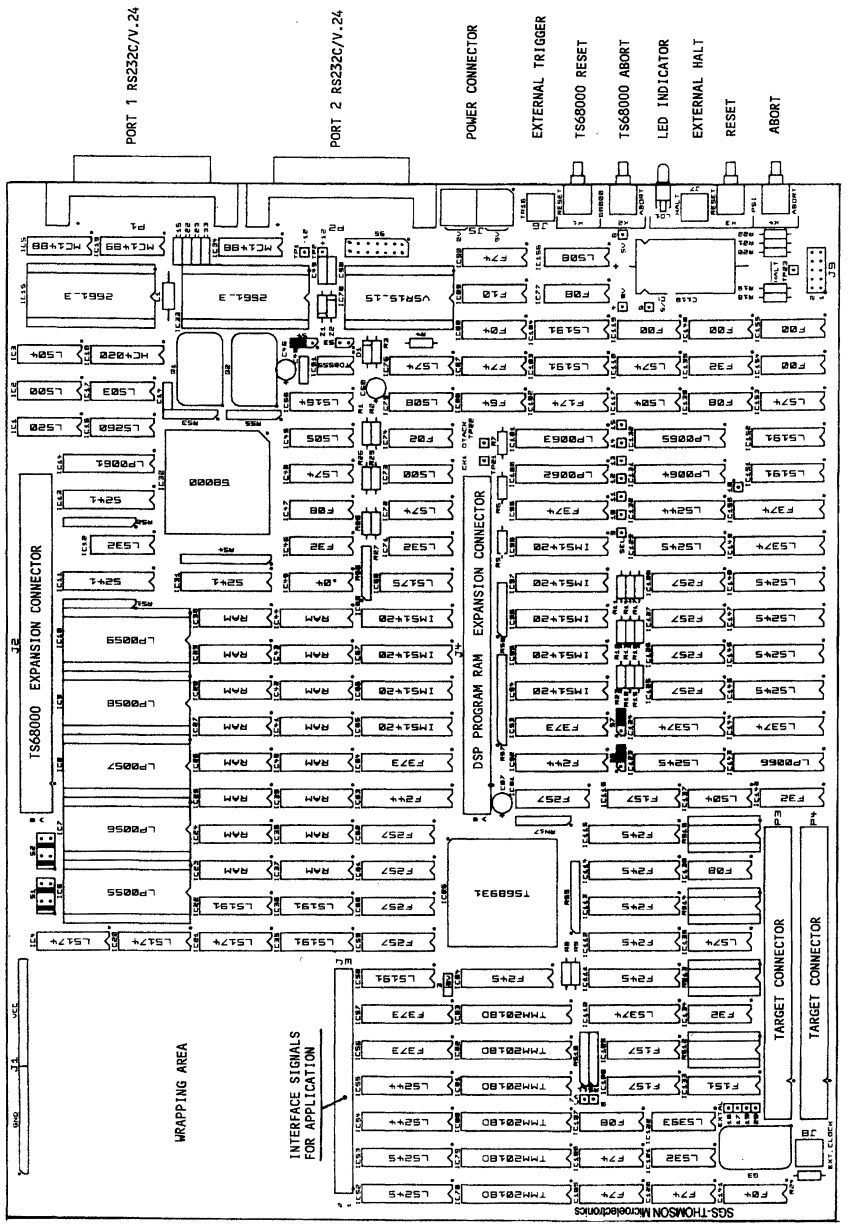
TS68930EMU

Figure 2 : Complete Configuration.



Power requirements :
On board DC/DC converter which provides ± 12V
+ 5V ± 5%/5A
Physical Specifications
290mm x 230mm
Temperature range
Storage : – 40'C to 80'C
Operating : + 5'C to 55'C

Figure 3 : TS68930EMU Board General Arrangement.



M88TS68930EMU-02

TS68930/31 DSP EPROM MODULE

- FULL SPEED TS68930 EMULATION
- PLUG AND FUNCTION COMPATIBLE TO TS68930
- INCLUDES PROGRAM AND COEFFICIENT EPROM's
- VERTICAL AND HORIZONTAL PLUG-IN VERSIONS
- MULTIPROCESSOR CONFIGURATION ALLOWED
- USEFUL DURING PROTOTYPING AND FIELD APPLICATION
- LARGE PROGRAM CAPACITY ALLOWED (up to 8k x 32 bit)
- DELIVERED WITH SIX BLANK EPROMS (2k x 8 bit)
- COMPLEMENTARY TOOL FOR TS68930 DSP FAMILY

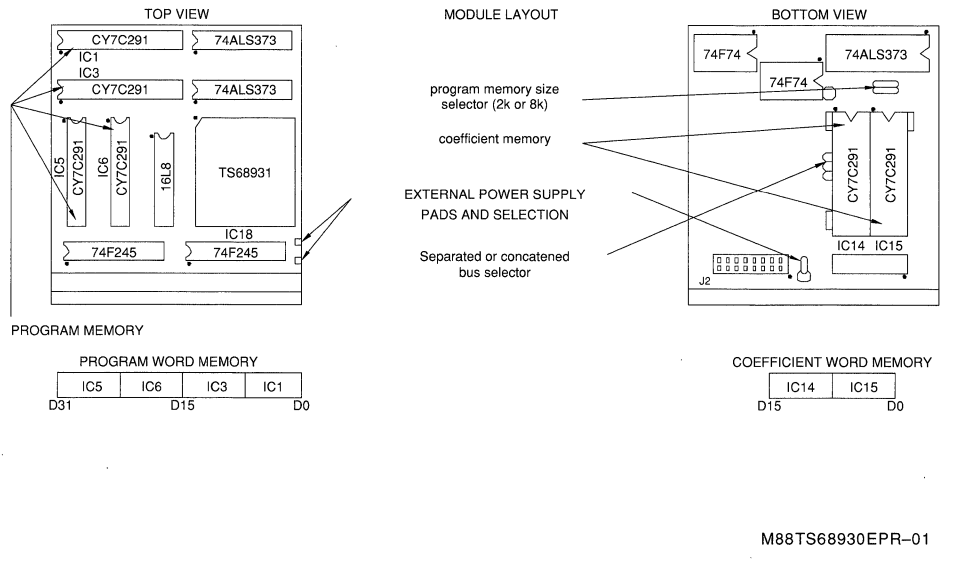
DESCRIPTION

The TS68930EPR EPROM module is a high performance board which permits the replacement of the TS68930 (DSP in ROM version) by the TS68931 (DSP in ROMLESS version) with external coefficient and program Eprom memories. The TS68930EPR is the ideal and complementary tool for debugging an application at the prototype level or when the program length exceeds the 1.3k of the TS68930 ROM Program capacity. Another advantage provided by the TS68930EPR is to manufacture compact prototypes before ordering the final TS68930 masked version, or to develop low-quantity applications eliminating masking cost. The TS68930EPR is designed to physically fit in the same board surface as the TS68930 device.

It allows a complete full speed emulation of the TS68930 even in multi-DSP configurations. Fast buffers are added on the data-bus and may be removed depending of the multiprocessing architecture.

The module is delivered with six blank EPROMs (2k x 8 bit). Suggested references are CYPRESS CY7C291-35WC or any compatible memories. The capacity of the program EPROM memory is 2k x 32 bit, or 8k x 32 bit as compared with 1.3 x 32 bit for the TS68930. The capacity of the coefficient EPROM memory is 512 x 16 bit. The TS68930 is compatible with the use of a crystal on the input pins EXTAL and XTAL, or with an external clock on the input pin EXTAL. The 5 volts power supply can be provided on the DIL-48 socket of the target application, or by an external power supply.

MODULE LAYOUT



Note : The module is delivered with 6 blank EPROMs (2k x 8).
Suggested references : CYPRESS CY7C291–35WC or any compatible memories.

ORDER CODES

TS68930EPR-H horizontal version (surface requirement : 60 x 81 mm, height : 15 mm)

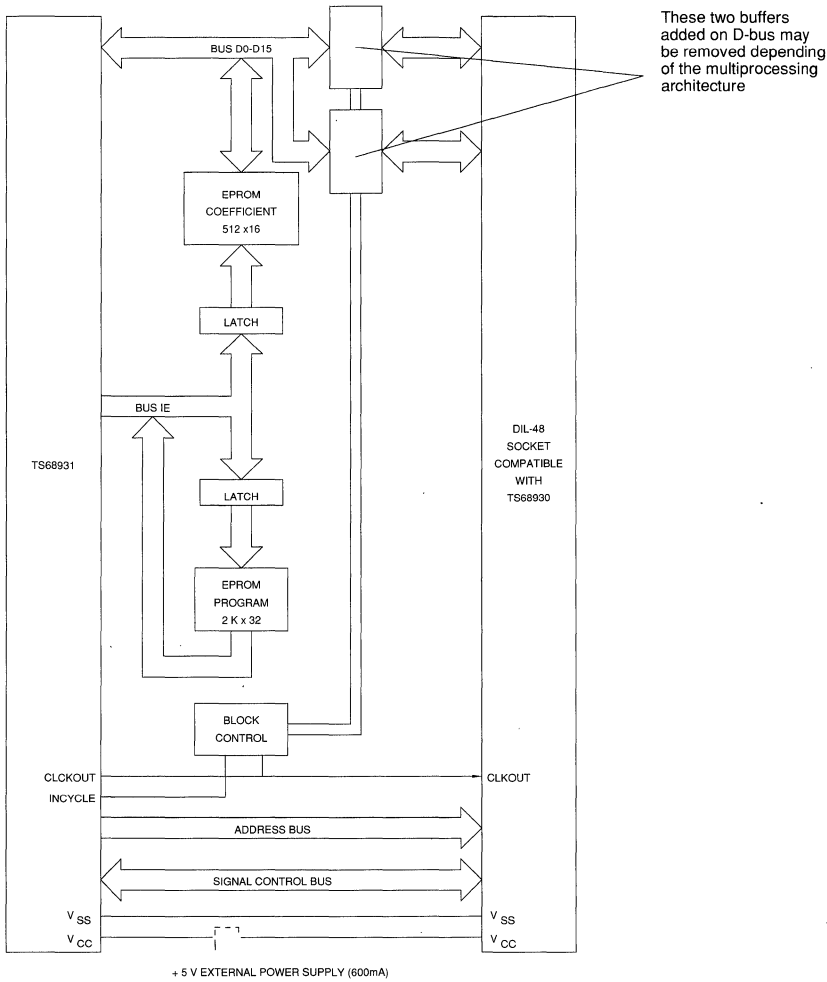
TS68930EPR-V vertical version (surface requirement : DIL 48 socket, height : 78 mm)

Nota : For high quantity without memories, or with Prom or OTP memories, please contact your local SGS-THOMSON sales office and/or distributor.

PROGRAMMATION

Using the TS68930Emulator or HDS monitor with "PROG" menu, the program and coefficients are down-loaded to the Prom-Programmer in byte-wide sections. An EPROM is programmed with each byte-wide section. Six EPROMs are required ; 4 for the 32-bit wide Program memory and 2 for the 16-bit wide coefficient memory. The programmed EPROMs are then inserted in the EPROM-sockets according to the module layout.

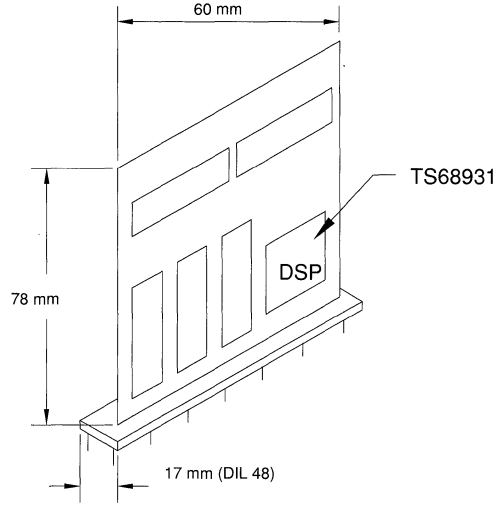
BLOCK DIAGRAM



M88TS68930EPR-02

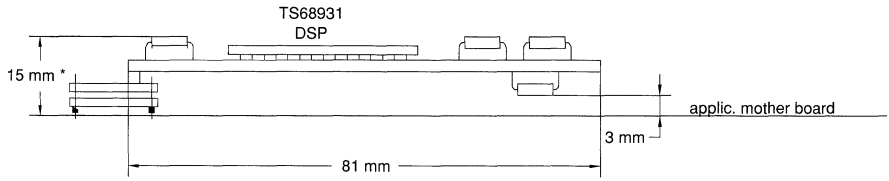
DIMENSION OF THE TS68930EPR MODULE

1) Vertical Module



M88TS68930EPR–03

2) Horizontal Module



M88TS68930EPR–04

* If the TS68930EPR module is plugged into a DIL48 socket increase these value with the height of the DIL socket (3 or 4 mm).

TS68930/31 DSP HARDWARE DEVELOPMENT STATION

- EMULATION/LOGIC ANALYSIS FOR
  - TS68930 MCU VERSION
  - TS68931 MPU VERSION
- MULTIPROCESSING
  - UP TO FOUR EMULATOR BOARDS AND FOUR OPTIONAL DEDICATED LOGICAL ANALYZER BOARDS
- USER-FRIENDLY INTERFACE
  - REDUCED LEARN-TIME
  - MENU DRIVEN
  - SYMBOLIC DEBUGGING
  - RESIDENT ASSEMBLER WITH FULL SCREEN EDITOR
  - CONTROLLED BY STANDARD TERMINALS OR IBM-PC HOSTED
  - DIRECT LINK TO PROM PROGRAMMER
  - CMOS BATTERY BACKUP OF CONFIGURATION (breakpoints, mode...)
  - UPLOAD-DOWNLOAD KERMIT PROTOCOL WITH HOST (VAX, IBM-PC)
- EMULATION FEATURES
  - FULL SPEED (cycle time = 160ns)
  - 64K PROGRAM MEMORY (32 bit wide)
  - 4K EXTERNAL DATA MEMORY, MAPPING ON A WORD BASIS
  - 30 SIMPLE BREAKPOINTS (break at ADDRESS 1)
  - 8 COMPLEX BREAKPOINTS (break after N ADDR. 1 followed by M ADDR.2)
  - SYNCHRO SIGNAL GENERATION AT SELECTED ADDRESSES OR RANGE
  - PSEUDO REAL TIME TRACE OF INTERNAL REGISTERS WITHOUT SLOWING DOWN EXECUTION
- LOGIC ANALYZER
  - REAL-TIME TRACE (2k depth, 95 bits)
  - SYNCHRONOUS ON DSP BUSES
  - ASYNCHRONOUS ON DSP SYSTEM BUS AND ON 15 EXTERNAL INPUTS
  - MIXED MODE SYNCHRONOUS-ASYNCHRONOUS
  - TRIGGERING CONDITIONS
    - ON PROGRAM ADDRESS IN CONJUNCTION WITH MANY DIVERSIFIED CONDITIONS (N times Addr. 1 followed by M times Addr. 2)
    - ON LOCAL DATA BUS VALUE
    - ON EXTERNAL BRANCH DSP INPUTS CONDITIONS
    - ON START OF MAILBOX EXCHANGE
  - BEFORE, AFTER AND WINDOW TRIGGERING
  - TIME MEASUREMENT FUNCTION
  - BREAKPOINT GENERATION ON LOCAL BUS VALUE

DESCRIPTION

The TS68930HDS is mainly intended for real-time multi-DSP applications. It has a menu-driven user interface so no learn time is required to completely and easily use all the system efficiency.

The designer can add emulator and logic analyzer boards to meet exactly his requirement. The TS68930HDS enhances the large range of development tools for the SGS-THOMSON DSP family.

1. GENERAL PRESENTATION OF THE TS68930HDS

The TS68930HDS (Hardware Development Station) is a real-time multiprocessors (up to 4) emulation system which provides a simple but extremely powerful user interface due to its interactive menu-driven organization.

The TS68930HDS is a modular system consisting of :

- a rack with power supplies, fans and standard double-Eurocard 9 slots VMEBUS back-plane
- a 68010 VME bus controller board
- up to four real-time emulator boards with 64k x 32 of program memory
- up to four logic analyzer boards with 2k x 95 bit trace memory associated with each emulator board. These analyzer boards are optional and can be used or not according to the application.

The TS68930HDS includes four programmable RS232C serial ports for connection either to a terminal, printer, Prom or Eprom programmer, or host computer such as Vax or IBM-PC.

This multi-task capability is managed by the 68010 CPU board. In case of power failure or when switching off the system, a large 64k x 8 CMOS RAM with battery back-up permits automatic saving system configuration and user programs and data.

The connector P2 on the VME bus is normally not used by the TS68930HDS boards. But it is always possible on the emulation board and by wire-wrapping to send DSP signals on connector P2. This possibility enables the user to use these signals on a double-Eurocard format application. One possible example is a D/A and A/D conversion board.

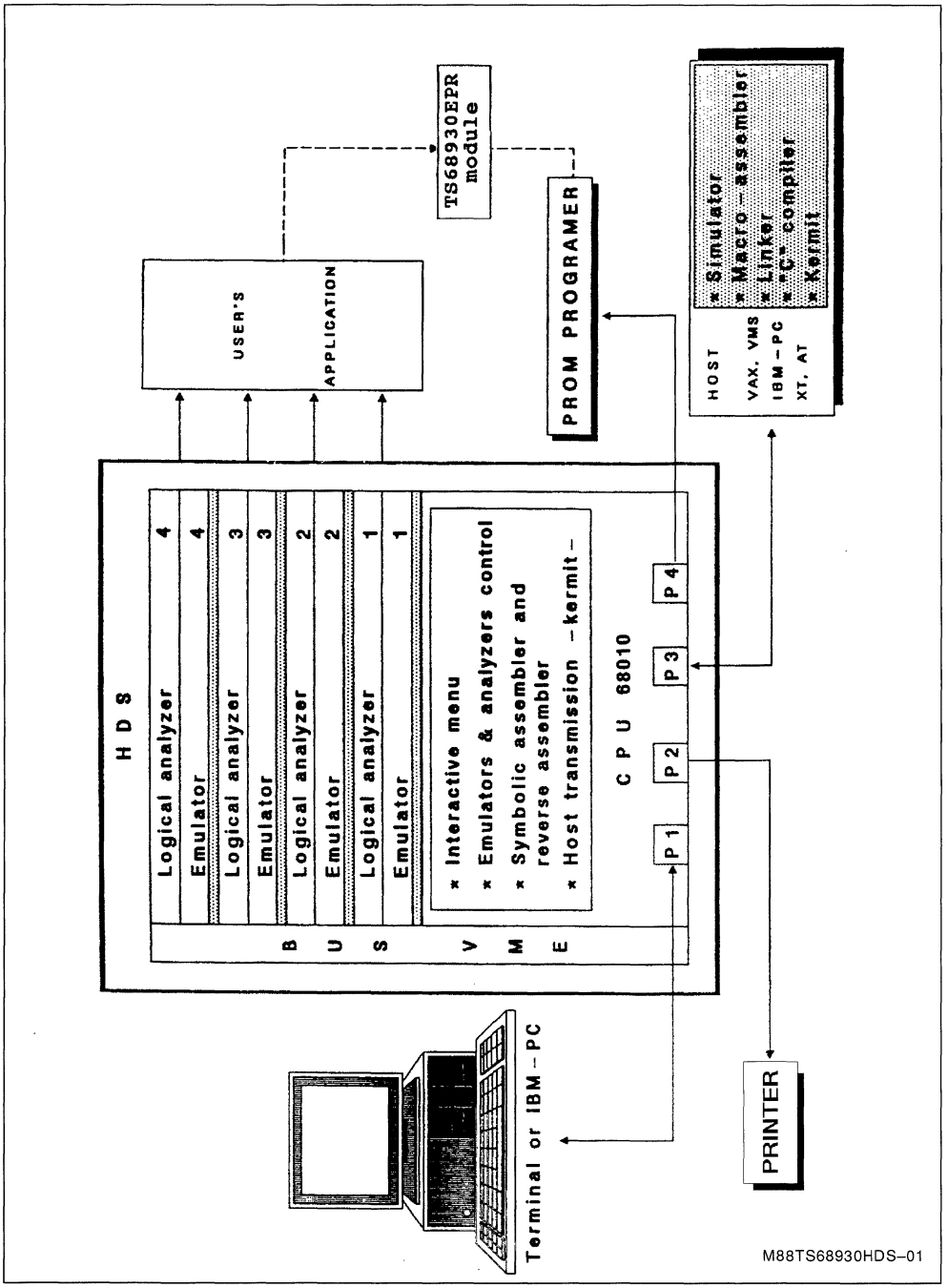
All the software management of the TS68930HDS is written in "C" language modules.

2. ORDER CODES

The basic configuration of the TS68930HDS includes one emulation board with its set of two probes (48-pin for TS68930 and 84-pin for TS68931), and one logic analyzer board with its set of probes.

The TS68930HDS is available in two versions (220V or 110V). The emulation board and logic analyzer boards with their respective probes are also available as separate items to fully use the system efficiency*.

Part Number	Power supply
TS68930HDS-0	220V
TS68930HDS-1	110V


H D S
Logical analyzer 4
Emulator 4
Logical analyzer 3
Emulator 3
Logical analyzer 2
Emulator 2
Logical analyzer 1
Emulator 1
B U S V M E
* Interactive menu
* Emulators & analyzers control
* Symbolic assembler and reverse assembler
* Host transmission - kermit -
C P U 68010
P 1
P 2
P 3
P 4
USER'S APPLICATION
TS68930EPR module
PROM PROGRAMER
HOST
VAX, VMS
IBM - PC
XT, AT
* Simulator
* Macro - assembler
* Linker
* "C" compiler
* Kermit
Terminal or IBM - PC
PRINTER
M88TS68930HDS-01

SGS-THOMSON MICROELECTRONICS

TS68930LIB

TS68930/31 DSP LIBRARY

- MULTIPLICATION/ACCUMULATION ROUTINES
- OPERATIONS ON COMPLEX NUMBERS
- DOUBLE PRECISION SHIFTS (32-bit word)
- DSP FUNCTIONS :
  - Real, Complex and Adaptive Complex FIR
  - Biquadratic Filter Routine
  - Autocorrelation routine
  - Lattice Filter Routine
- FAST FOURIER TRANSFORMS :
  - Butterfly
  - 8-point FFT
  - 64-point FFT
- ARITHMETIC FUNCTIONS :
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  - 32 x 32 Multiplication
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ORDER CODES

TS68930LIB-PC	PC/MS DOS
TS68930LIB-VMS	VAX VMS

OTHER DSP APPLICATION PROGRAMS

CCITT V.22BIS/V.22/V.23/V.21 and BELL 212/103

CCITT V.32

These softwares are not included in the DSP library. They can be obtained through software licence agreement.

SGS-THOMSON MICROELECTRONICS

TS68930SP

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The directives have to control the assembly (END, ORG, MEMORY, INCLUDE, PROGRAM), the data definition (DEF, REF, SET, ASG) the macros (CREATE, DELETE, CHANGE, DEFAULT, LIBRARY), the conditional assembly (IF, ELSE, ELSEIF, REPT), the listing (LIST, PRINT, MAP, CROSS, HEAD, CODE, PAGE, TITLE, INPUT, OUTPUT, LINES) and the generation of binary or object files (HEXA, INTEL, MOTOROLA, NOBIN, TEKTRO, LINK).

Macro calls provide the means to create a macro language that is capable of calling source statements from other locations within the program. A macro call fetches the source statements defined by the macro and substitutes them for the macro as if they had been written in that location in the program. The obvious advantage to using macro code is that less source code must be written, and this in turn means that the programs become easier to read and debug. In addition, macros are executed faster than a comparable absolute code subroutine because no branching is involved.

Macro calls and conditional assembly provide the means to create modular programs. Those programs then can be linked together by using the DSP linker.

LINKER

The linker allows the development of modular and relocatable software. It can use libraries and provide a linking of a group of modules (incremental linker).

It adds two powerful features compared to conventional ones : it can link a group of modules which do not constitute a complete program. Then, this newest group can be used as an input for final linking. It can generate an executable program even when external references are still unsolved. This enables real-time debugging of an incomplete program without having to create empty functions to test.

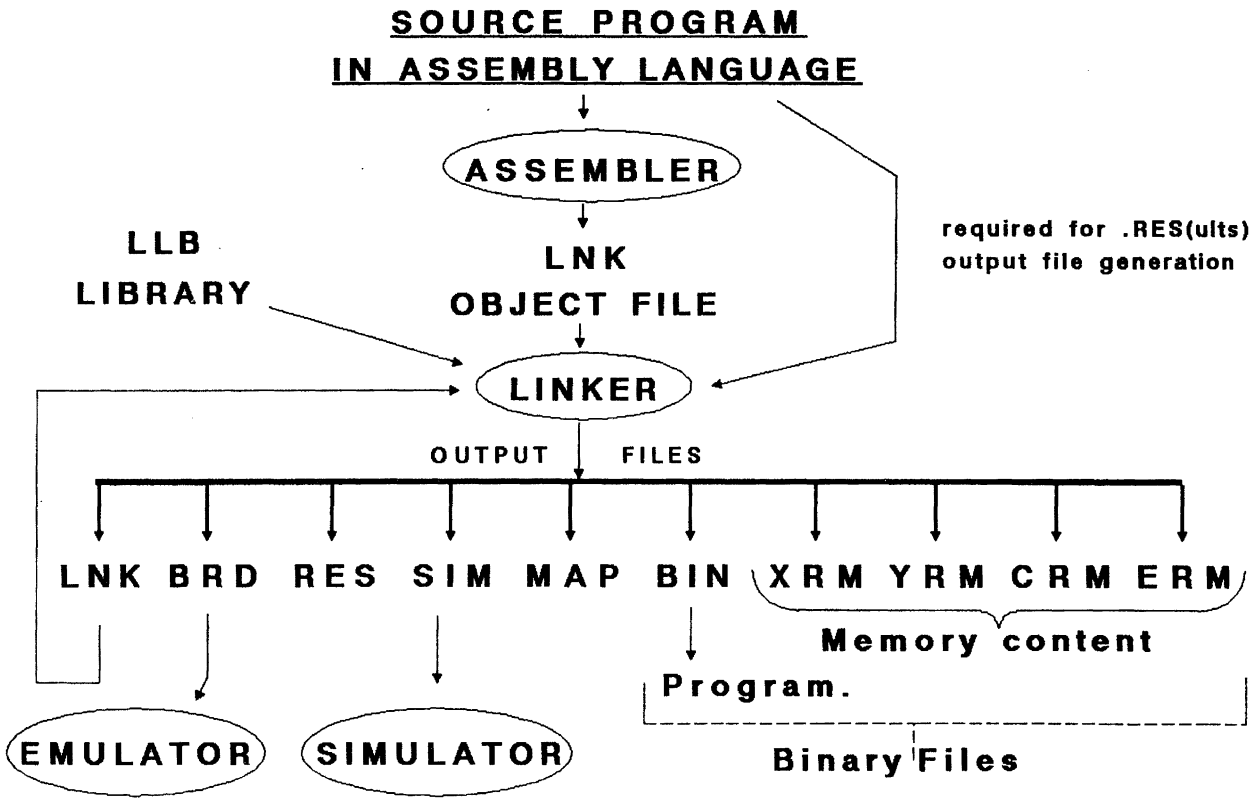
FUNCTIONAL SIMULATION

The TS68930 Functional Simulator is a software program that simulates the internal operation of the TS68930/31 DSP for effective software development and off-line program verification . Use of the functional simulator allows debugging of TS68930/31 software without the requirement of hardware.

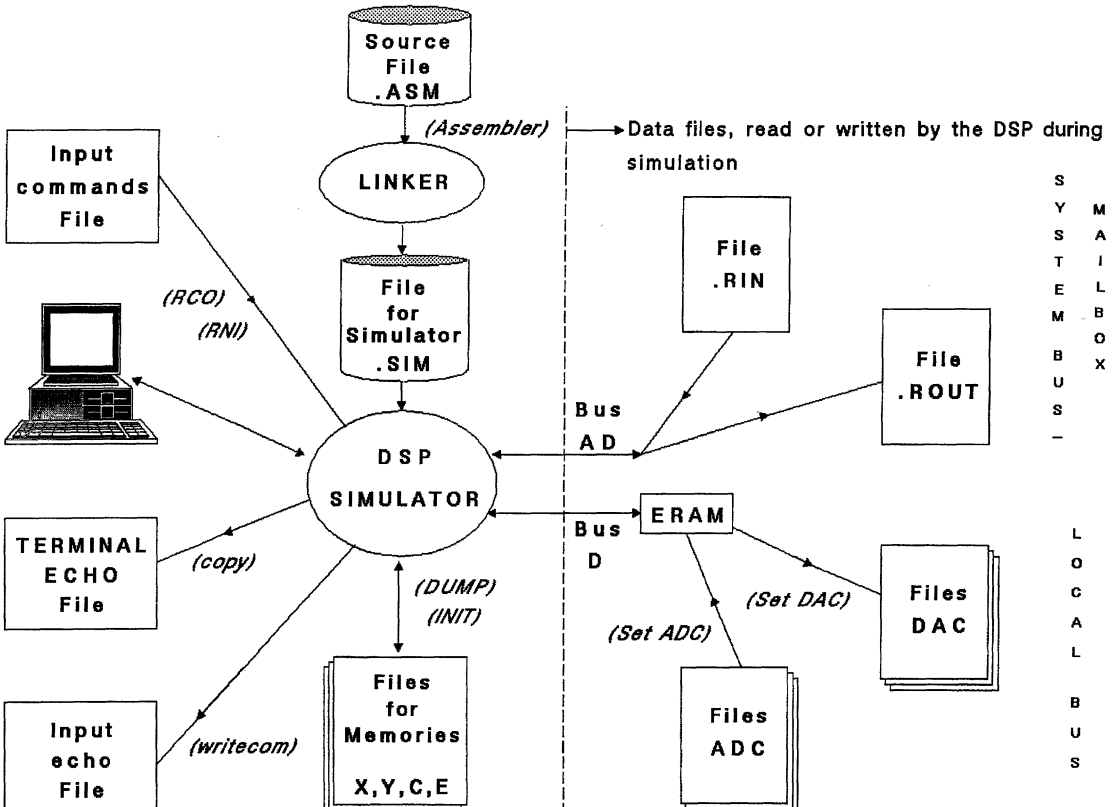
The simulator uses a coded form of the TS68930 DSP object code produced by the TS68930 linker. Simulation of A/D Converters, D/A Converters, and other conventional peripherals is accomplished using associated input and output files.

All internal registers and memories of the TS68930 can be modified during a simulation session. During execution of the program, the internal registers and memories of the simulated TS68930 are modified as the host computer interprets each instruction. Simple or high level breakpoints may be used to suspend execution at a selected point in the program so that the internal registers and memories can be inspected and/or modified.

LINKER OPERATION



SIMULATOR OPERATION



On-line help with the simulator commands is available by entering a simple HELP command.

ORDER CODES

Part Number

TS68930SP-PC Software Package on PC for TS68930/31

TS68930SP-VMS Software Package on VAX VMS for TS68930/31

SGS-THOMSON MICROELECTRONICS

TS68930SPC

TS68930/31 DSP "C" COMPILER

- UPGRADED KERNIGHAM AND RITCHIE "C" DEFINITION, I.E. RESPECT OF ANSI X3J11 STANDARD
- RUNS ON PC OR COMPATIBLE UNDER MS-DOS 3.1 OR LATER
- RUNS ON VAX UNDER VMS OPERATING SYSTEM (for UNIX or ULTRIX operating system contact your sales office)
- "FLOAT" IN RESPECT OF IEEE 754 STANDARD, "DOUBLE" AND "INTEGER" TYPES ALLOWED
- MANY FUNCTIONS IMPLEMENTED : CHARACTER AND STRING HANDLING, MEMORY MANAGEMENT, CONVERSION, MATHEMATICAL, I/O ROUTINES
- SPECIFIC RUN-TIME FOR ACCESS TO PERIPHERALS (mail-box, A/D and D/A converter...)
- SOURCE ASSEMBLER INCLUSION IN SOURCE "C" PROGRAM CAPABILITY
- INCLUDES PREPROCESSOR, MACRO-ASSEMBLER AND LINKER-LOADER
- PRODUCES LOADABLE AND RUNNABLE BINARY OBJECT FILES
- HIGH LEVEL SYMBOLIC DEBUGGER

DESCRIPTION

The SGS-THOMSON MICROELECTRONICS "C" compiler used with the assembler/linker (included with the compiler) allows the possibility to write "C" source code and produces object code running on the TS68930/31 Signal Processor. It takes into account all the advanced features of the TS68930/31 (parallelism, pipe-line, double precision, complex mode and 32-bit instruction set).

The high level language "C" compiler has been designed to provide the greatest flexibility of use.

User can either run the complete software with only one simple command, or run separately each software included in the package : "C" compiler, optimizer, assembler and linker.

STANDARD

THE SGS-THOMSON "C" compiler is an implementation of the ANSI X3J11 standard, which includes and exceeds Kernigham and Ritchie specification. New possibility for the processor and new class for data are allowed. For example, "CONST" allows ROM implementation for constant data.

LICENSE

The SGS-THOMSON "C" compiler is delivered under license for one user only. Upgrades of new releases will be done to each registered user, free of charge, for a duration of 12 months starting from the purchase date.

ORDER CODES

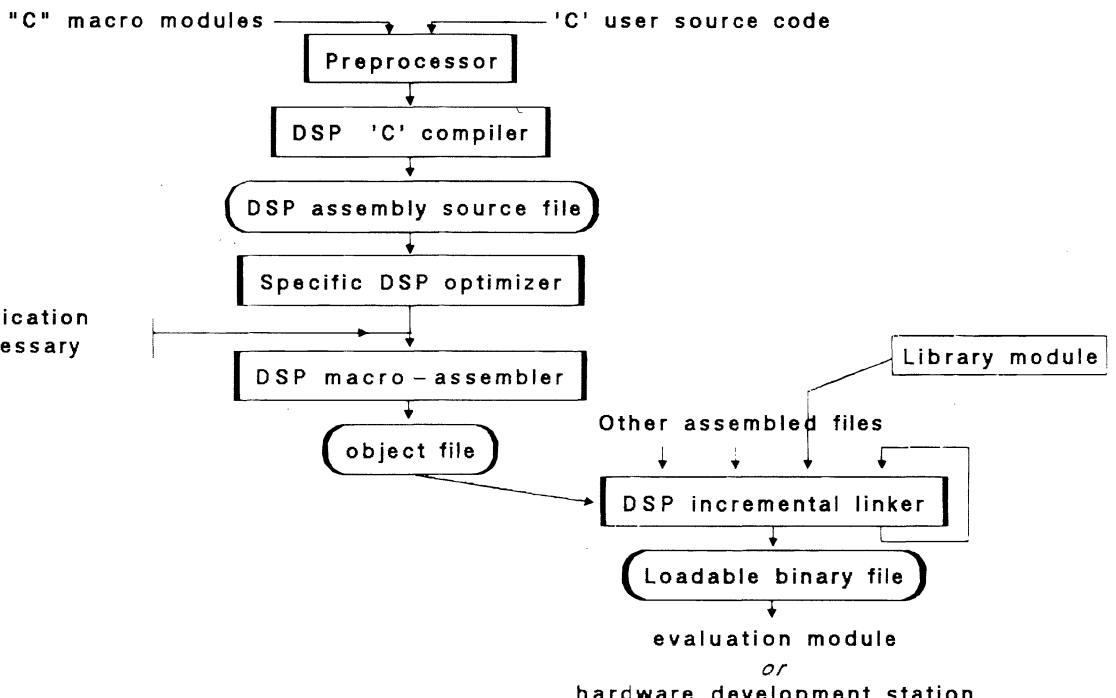
The TS68930SPC "C" compiler includes in the same commercial software-package the "C" compiler software plus the standard TS68930SP software (macroassembler, linker and functional simulator).

Part Number

- TS68930SPC-PC "C" compiler for TS68930/31 on PC/MS DOS

- TS68930SPC-VMS "C" compiler for TS68930/31 on VAX VMS

TS68930/1
C COMPILER



M88TS68930SPC-01

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

DEVELOPMENT OF REAL–TIME ALGORITHMS USING THE SGS–THOMSON DIGITAL SIGNAL PROCESSOR TS68930 AND THE SGS–THOMSON ANALOG FRONT–END TS68950/1/2

TABLE OF CONTENTS

1. INTRODUCTION

The purpose of this application note is to describe a powerful vehicle to execute and check DSP (digital signal processing) algorithms in real-time for modem (or any voice-grade) applications.

THE CONTEXT

Developing a DSP application is a process which can be divided into 3 main steps :

- Digital signal processing software development

  Typically a digital signal processing software development chain includes the following programs :
  - calculation of filter coefficients
  - simulation of transmission lines
  - signal generation programs (sinewaves, noise)
  - spectrum analysis program (fast fourrier transform)

Such a chain is generally available on a mainframe and is used in combination with an high level language to develop and simulate algorithms from a system point of view.

- Translation, coding, optimization

  After being reasonably sure that the algorithm fulfills the specifications it is translated into the assembler language of a digital signal processor such as the SGS-THOMSON Microelectronics TS68930 or ST18930.

- Test in real time

  The final but most important step is to test the behaviour of the algorithm in real time and (very important in signal processing) real world situations. For instance, a digital to analog converter is a perfect device in simulation whereas it has defects such as non-linearities in the real world.

In DSP testing there is no such thing as yes or no. The tests are qualitative appreciation of a real signal (typically : in modem the bit error rate, in speech subjective listening tests, in recognition percentage of recognized words, etc.).

This has for consequence that in order to always improve quality, algorithms are always changed which in turn implies that the 3-step design is not a straightforward process. On the contrary it requires going back and forth between theory, simulation on the main-frame and the tests on the application board.

Therefore development tools must be easy to use and well integrated into a complete chain, particularly to avoid losing time going from one step to another.

THE OBJECT

The execution vehicle described in this application note takes care of the second and third step of an application.

The following assumptions are made relative to the user :

- he/she has all the necessary tools to search and develop algorithms,
- he/she will set-up its own hardware environment as required by the application (such as the type of telephone line),
- the user knows the TS68930.

The execution vehicle contains the following items :

- the TS68930 macro-assembler available on VAX VMS and on MS-DOS machines for developing TS68930 code,
- the macro-assembler libraries,
- the program to download the TS68930 code from the host onto the evaluation board,
- the emulation board for testing and modifying the code,
- the emulation probe to connect the emulation board to the analog interface board,
- an analog interface board [EFRMAFE] consisting of :
  - TS68950 (tx chip)
  - TS68951 (rx chip)
  - TS68952 (time base chip)
- the MAFCOM command language (explained in this application note).

FURTHER REFERENCES

- TS68950 data sheet
- TS68951 data sheet
- TS68952 data sheet
- TS68930 data sheet
- TS68930 DSP user's manual
- TS68930 macro assembler and simulator user's guide
- TS68930EMU user's manual
- EFR MAFE user's manual

2. NOTES AND DEFINITIONS

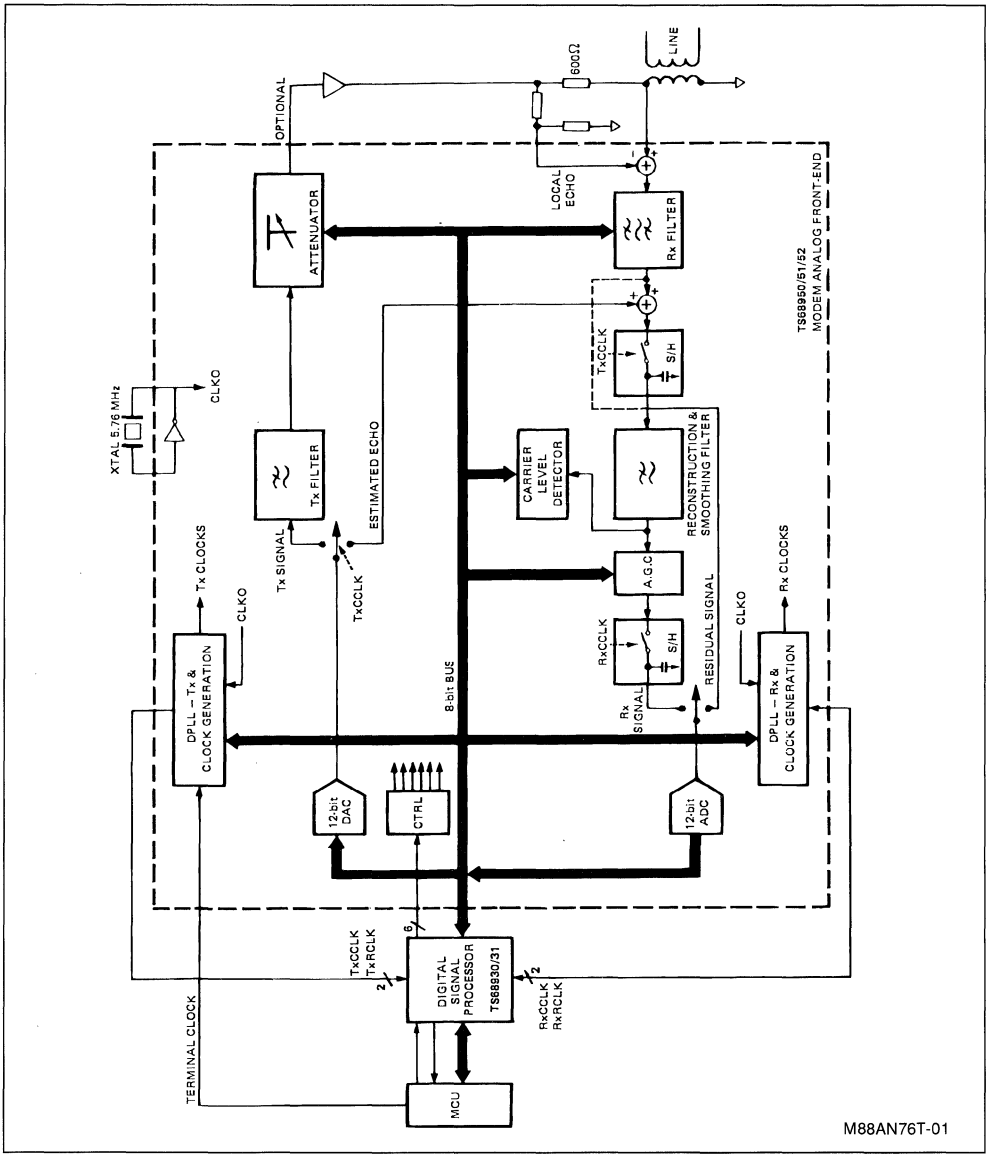
2.1. MAFE

The term MAFE refers to the SGS-THOMSON 3-chip set TS68950/1/2. For a digital signal processor the 3 chips are seen as 1 chip. More precisely :

- the 3 chips are connected in parallel to the processor data, address, control lines,
- hence the processor does not differentiate between chips but rather between registers.

A functional diagram of the 3-chip set is shown in fig. 1.

Figure 1 : The Modem Analog Front-end Chip.



3. THE MAFE REGISTERS

3.1. OVERVIEW OF THE REGISTER SET

The MAFE contains 14 registers :

- 5 registers used to transmit or receive signals ; they all can be directly accessed.
- 1 address register which refers to one of the 8 control registers.
- 8 control registers used for the programmation of the various parameters ; they cannot be directly accessed, instead they are programmed either indirectly or sequentially.

a) SIGNAL REGISTERS

Tx chip : There are 2 registers in which signal samples are transmitted on 12 bits.

- TX SIGNAL SAMPLE
- ESTIMATED ECHO SAMPLE

Rx chip : There are 2 registers in which signal samples are received on 12 bits.

- RX SIGNAL SAMPLE
- RESIDUAL SIGNAL SAMPLE

There is a 1-bit register which indicates the detection of a carrier .

- CARRIER DETECT

b) CONTROL REGISTERS

- 3-bit ADDRESS REGISTER which gives the address of one of the 8 following control registers :
- RC1 - BIT CLOCK / BAUD RATE CLOCK (time base chip)
- RC2 - CONVERSION CLOCK / MULTIPLEXING CLOCK (time base chip)
- RC3 - BAND-PASS/REJECTION/RECONSTRUCTION FILTERS (rx chip)
- RC4 - TRANSMIT ATTENUATION & EXI CONTROL (tx chip)
- RC5 - AGC GAIN (rx chip)
- RC6 - CARRIER LEVEL DETECTOR THRESHOLD (rx chip)
- RC7 - RX CLOCK PHASE SHIFT AMPLITUDE (time base chip)
- RC8 - RX CLOCK PHASE SHIFT PROGRAMMING (time base chip)

3.2. PROGRAMMATION OF THE REGISTER SET

These 7 registers can be directly accessed with the addresses listed in the table below :

Register Addresses				Register Names	
$\overline{CS1}$	CS0	RS0	RS1	R/$\overline{W}$ = 0	R/$\overline{W}$ = 1
0	X	X	X	deselected	deselected
1	0	0	0	TX SIGNAL	RX SIGNAL
1	0	0	1	ESTIM. ECHO	RESIDUAL SIGNAL
1	0	1	0	ADDRESS REG.	CARRIER DETECT
1	0	1	1	CONTROL REG.	
1	1	X	X	deselected	deselected

a) SIGNAL REGISTERS

WRITING TX SIGNAL or ESTIMATED ECHO

It takes 2 accesses since the MAFE has an external 8-bit bus and the samples are transmitted on 12 bits.

READING RX SIGNAL or RESIDUAL SIGNAL

It takes 2 accesses since the MAFE has an external 8-bit bus and the samples are received on 12 bits.

FORMAT (for the 4 signal sample registers)

MAFE Data Bus	D7	D6	D5	D4	D3	D2	D1	D0
FIRST CYCLE	3	2	1	0	X	X	X	X
SECOND CYCLE	11	10	9	8	7	6	5	4

bit 0 = lsb

bit 11 = msb

READING CARRIER DETECT

The active bit is D7.

b) CONTROL REGISTERS

The 8 control registers cannot be directly accessed ; they are programmed either indirectly or sequentially.

Indirect access :

The ADDRESS REGISTER (bit D7-D5) is loaded with the address of the control register to be accessed :

ADDRESS REGISTER (bit D7-D5)	CONTROL REGISTER
000	RC1
001	RC2
010	RC3
011	RC4
100	RC5
101	RC6
110	RC7
111	RC8

The CONTROL data REGISTER can then be written with the programmation word.

It must be noted that after each access the ADDRESS REGISTER is always incremented.

Sequential access :

This method is very useful to program a group of continuous registers as it is the case at initialization time. If there are N registers to program it will take N + 1 accesses compared to 2N accesses with the indirect method.

Since the ADDRESS REGISTER is always incremented after each access, it can be loaded with an address (generally 0) and all control registers can then be programmed in sequence.

Each access a CONTROL data REGISTER is written with a new programmation word.

3.3. DESCRIPTION OF THE CONTROL REGISTERS

TX AND RX CLOCK PARAMETERS : CONTROL REGISTERs RC1 RC2

Code	Control Register RC1		Control Register RC2		
	Bit 7-4	Bit 3-1	Bit 7-5	Bit 4-3	Bit 2
	Bit Clock (kHz) (1)	**Baud Rate Clock** (kHz) (1)	**Multiplexing Clock** (kHz) (1)	**Conversion Clock** (kHz) (1)	**TX Sync**
0	19.2	2.4	1440	9.6	RxCLK
1	16.8	2.0	288	8.0	TxSCLK
2	14.4	1.6	12	7.2	(*)
3	12.0	1.2	9.6	7.2	
4	9.6	0.6	7.2		
5	7.2	0.6	4.8		
6	6.4	0.6	2.4		(*) Tx
7	6.0	0.6	1.2		DPLL
8	4.8				runs
9	3.2				freely
A	2.4				if
B	1.2				there
C	0.6				is no
D	0.6				transition
E	0.6				
F	0.6				

RECEIVE FILTER PARAMETERS : CONTROL REGISTER RC3

Code	Control Register RC3				
	Bit 7-6 (bit 3 = 0)	**Bit 7-6** (bit 3 = 1)	**Bit 5-4**	**Bit 2**	**Bit 1**
	High Pass Filter Sampl. Freq./ – 3dB cut-off (kHz/Hz)	High Pass Filter Sampl. Freq./ – 3dB cut-off/ rejected band (kHz/Hz/Hz)	Low Pass Filter Sampl. Freq./ – 3dB cut-off (kHz/Hz)	Sample & hold (SH2)	REC Filter
0	36/250		72/800	OFF	OFF
1	36/250		144/1600	ON	ON
2	72/500	72/800/370-470	288/3200		
3	144/1600	144/2200/800-1500	288/3200		

(1) All references at 5.76MHz master clock.
(2) High Pass Filter values depends on rejection filter being on.

RECEIVE CLOCK PARAMETERS : CONTROL REGISTERS RC7 RC8

Code	Control Register RC8 Bit 6-4	Control Register RC7 Bit 7-3			
	Rx Clock	Rx Clock Phase Shift Amplitude (degree)			
	Phase Shift	**600**	**1200**	**1600**	**2400**
0		0.75	1.5	2	3
1	Fine LAG (note 1)	1.5	3	4	6
2	Fine LEAD (note 1)	2.25	4.5	6	9
3		3	6	8	12
4	Coarse (note 2)	3.75	7.5	10	15
5	" "	4.5	9	12	18
6	" "	5.25	10.5	14	21
7	" "	6	12	16	24
8		6.75	13.5	18	27
9		7.5	15	20	30
A		8.25	16.5	22	33
B		9	18	24	36
C		9.75	19.5	26	39
D		10.5	21	28	42
E		11.25	22.5	30	45
F		12	24	32	48
10		11.25	22.5	30	45
11		13.5	45	60	90
12		33.75	67.5	90	135
13		45	90	120	180
14		61.25	112.5	150	225
15		67.5	135	180	270
16		78.75	157.5	210	315
17		90	180	240	360
18		101.25	202.5	270	405
19		112.5	225	300	450
1A		123.75	247.5	330	495
1B		135	270	360	540
1C		146.25	292.5		585
1D		157.5	315		630
1E		168.75	337.5		675
1F		180	360		720

Notes : 1. fine = 2 main clock cycles.
2. coarse = as programmed in RC7 bit 7-3.

RECEIVE / TRANSMIT PARAMETERS : CONTROL REGISTERS RC4 RC5 RC6

Code	RC5	RC6	RC4	
	Bit 7-3	Bit 7-5	Bit 7-4	Bit 2-1
	RX AGC Gain (dB)	RX Carrier Level Detection Threshold (dBm)	TX Attenuation (dB)	TX EXI Control
0	0	– 29.85	0	Input disconnected.
1	1.5	– 27.35	2	Transmit Filter i/p
2	3	– 34.15	4	Transmit Atten. o/p
3	4.5	– 46.75	6	Input disconnected.
4	6	– 44.25	8	
5	7.5	– 46.75	10	
6	9	– 44.25	12	
7	10.5		14	
8	12		16	
9	13.5		18	
A	15		20	
B	16.5		22	
C	18		Infinite	
D	19.5		"	
E	21		"	
F	22.5		"	
10	24			
11	25.5			
12	27			
13	28.5			
14	30			
15	31.5			
16	33			
17	34.5			
18	36			
19	37.5			
1A	39			
1B	40.5			
1C	42			
1D	43.5			
1E	45			
1F	46.5			

4. HARDWARE DESCRIPTION

As shown in the functional diagram (figure 2) the SGS-THOMSON Microelectronics family of components for DSP can be directly interconnected without any glue.

The following paragraphs explain the different steps to connect the DSP and the MAFE kit.

4.1. DSP-MAFE DATA BUS CONNECTION

The MAFE external data bus is 8-bit wide [D0-D7] ; this bus is used to write control words, transmit signals or receive signals.

Implementation :

It is connected to the upper part of the DSP local data bus [D8-D15] rather than to the lower part for the following reason :

- in the case of separate buses the programmer will have a larger memory space (cf. appendix A).

Obviously in the case of concatenated buses it does not matter if the MAFE is connected on the upper or lower part of the bus.

4.2. DSP-MAFE ADDRESS BUS CONNECTION

The MAFE has 4 address lines $\overline{CS1}$, CS0, RS0, RS1 and 2 control signals R/$\overline{W}$, $\overline{E}$ allowing the direct control of 7 registers.

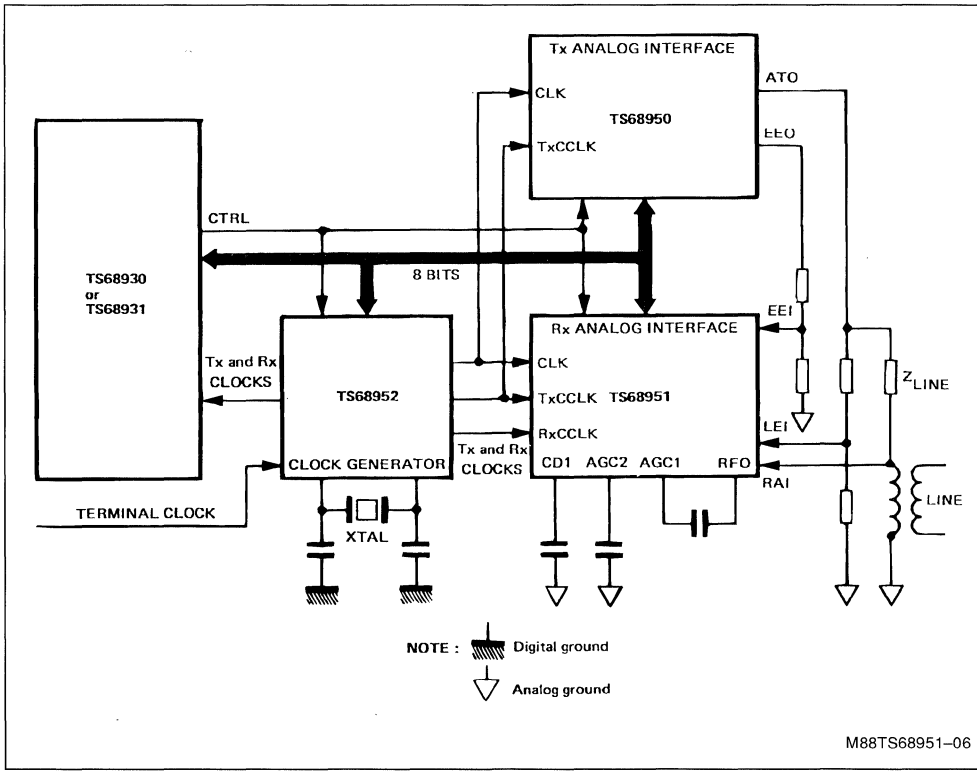
Implementation :

The 4 MAFE address lines are connected to the 4 most significant addresses of the DSP local address bus.

There is a good reason for this ; the address lines A8-A11 are free whereas A0-A7 are multiplexed with the system bus (cf. appendix A).

DSP	A8	A9	A10	A11	$\overline{DS}$	R/$\overline{W}$
MAFE	RS1	RS0	CS0	$\overline{CS1}$	$\overline{E}$	R/$\overline{W}$

Figure 2 : Connection DSP-Mafe.



4.3. TIMING REQUIREMENTS

With reference to the table below and to timing diagram 1 it can be seen that the MAFE has an input data set-up time of 120ns and an output data delay time of 150ns.

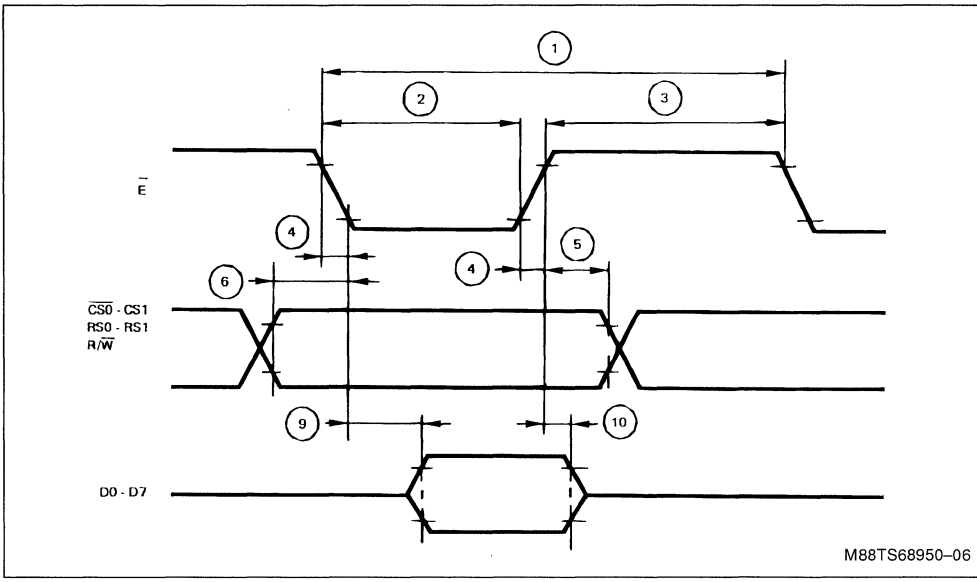
Symbol	Parameter		Min.	Max.	Unit
tcyc	Cycle Time	1	320		ns
twel	Pulse Width $\overline{E}$ Low Level	2	180		ns
tweh	Pulse Width $\overline{E}$ High Level	3	100		ns
thce	Control Signal Hold Time	5	10		ns
tsce	Control Sig. Set-up Time	6	40		ns
tsdi	Input Data Set-up Time	7	120		ns
thdi	Input Data Hold Time	8	10		ns
tddo	Output Data Delay Time	9		150	ns
tdz	Output High-Z Delay	10		80	ns

These 2 timings are too slow for the DSP. Fortunately the DSP has a slow access mode (cf. appendix A) which lengthen any external accesses by 160ns. In this way the DSP and the MAFE can be connected directly.

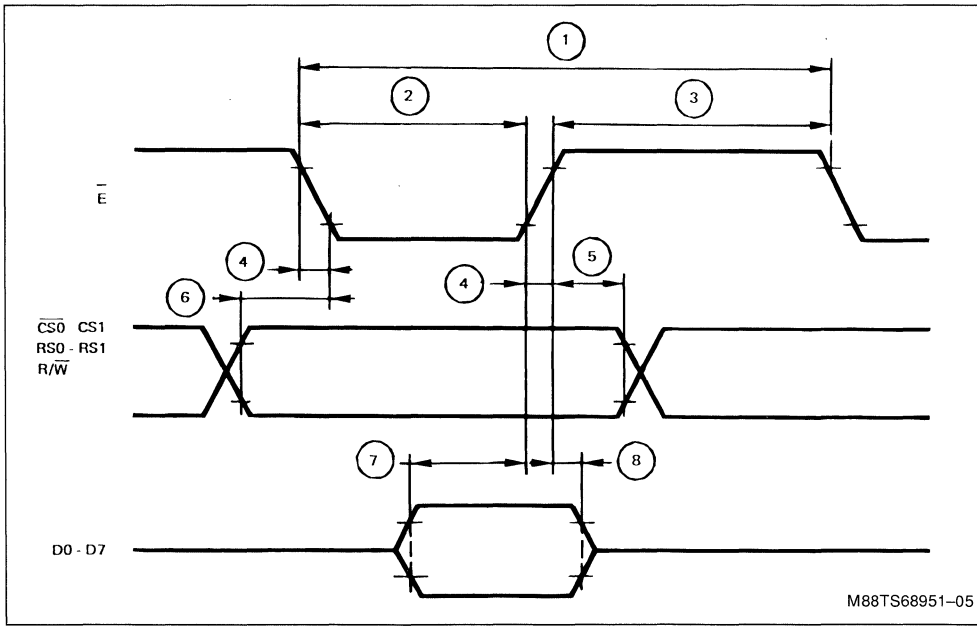
The DSP timing is shown below.

Symbol	Parameter	Min.	Max.	Unit
tpw	$\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Pulse Width	225	240	ns
tah	Address Hold Time	10		ns
tdsw	Data Set-up Time, Write Cycle	185		ns
tdhw	Data Hold Time, Write Cycle	10		ns
tdsr	Data Set-up Time, Read Cycle	20		ns
tdhr	Data Hold Time, Read Cycle	5		ns
tarw	Address Valid to $\overline{WR}$, $\overline{DS}$, $\overline{RD}$ Low	40		ns

WRITE OPERATION

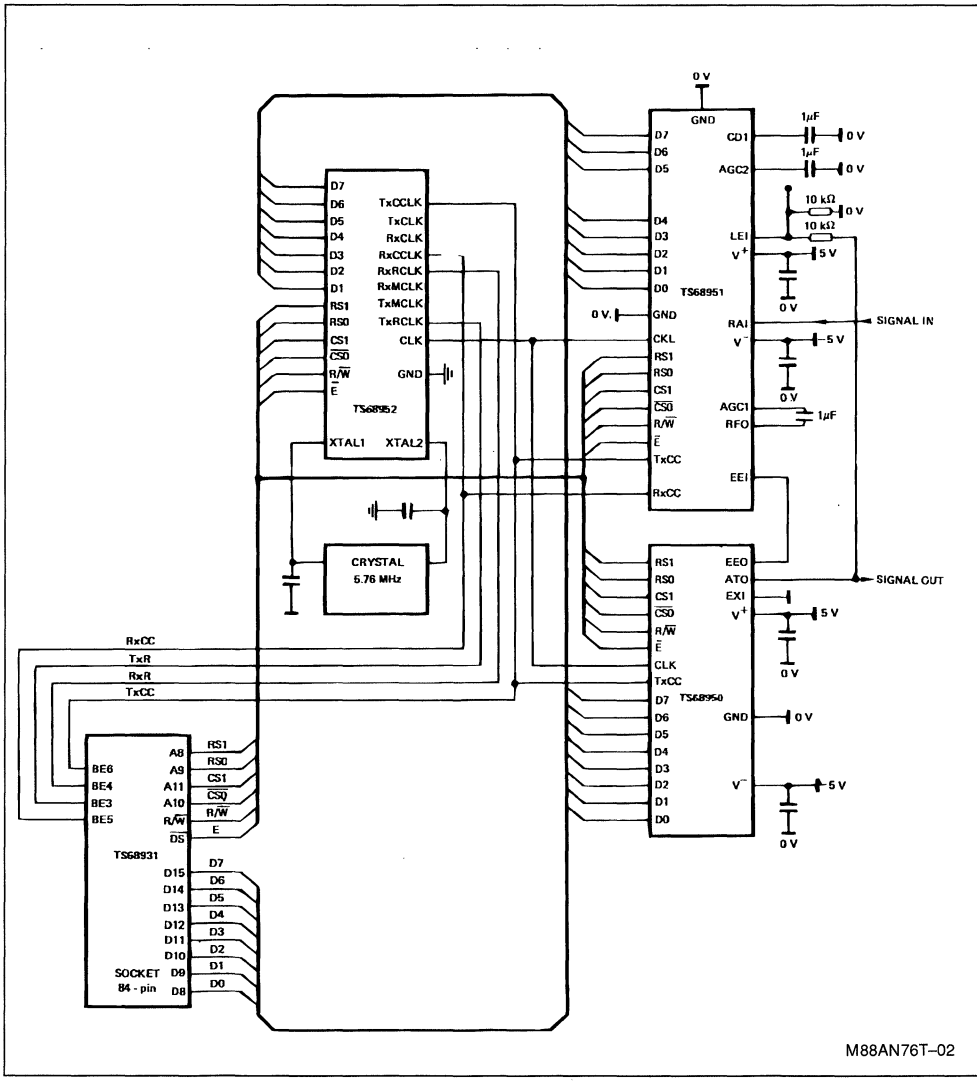


READ OPERATION



Notes : 1. Voltage levels shown are $V_{IL} < 0.4V$, $V_{IH} > 2.4V$, unless otherwise specified.
2. Measurement points shown are 0.8V and 2.2V, unless otherwise specified.

4.4. BLOCK DIAGRAM



5. THE COMMAND LANGUAGE

The command language has been developed with the DSP macro-assembler available on VAX-VMS and MS-DOS.

This command language is used in order to simplify the programmation of the MAFE. In this way the programmation is reduced to a series of commands (ex : TXSO = transmit signal out) instead of having to remember register numbers, bit numbers or specific details.

This command language is one possible command language among many and the user can (and is advised to) use the DSP macro-assembler to create his own language as needed.

The command language is given in program (cf. appendix B.2.).

DEFINITIONS OF PARAMETERS

- ADDIR : direct address in internal memory or register T
- K, BIT, BAUD, MUX, FS, HPF, LPF : hexadecimal value (with reference to tables of paragraph 3.3.)
- RSR : binary value (Example : 101 = rejection filter ON, sample & hold OFF, reconstruction filter ON).

5.1. THE ROUTINES

SIGNAL TRANSFER

	Address	Bits	Syntax
TRANSMIT			
1 - Signal	800	15 - 8	TXSO ADDIR
2 - Estimated echo	900	15 - 8	TXEE ADDIR
RECEIVE			
1 - Signal	800	15 - 8	RXSI ADDIR
2 - Residual Signal	900	15 - 8	RXRES ADDIR
3 - Carrier Detect	A00	15	CD ADDIR

PARAMETER SETTING

	Address	Bits	Syntax
TIME BASE			
1 - Bit Rate, Baud Rate,	0000	15 - 12 11 - 9	RC1 BIT, BAUD\
2 - Mux, Sample Clock	2000	15 - 13 12 - 11	RC2 MUX, FS\
3 - Mux, Sample Clock, Sync	2000	10	RC2 SYNC MUX, FS, K\
4 - RX Phase Shift Amplitude	0000	15 - 11	RXPSA K\
5 - RX Phase Shift Programming	E000	14 - 12	RXDPLL K\
TRANSMIT			
1 - Attenuation	6000	15 - 12	SET_ATT K\
2 - Exi Input	6000	10 - 9	SET_EXI K\
RECEIVE			
1 - HPF, LPF, REJ, SH2, Reconst.	4000	15 - 12 11, 10, 9	RC3 HPF, LPF, RSR\
2 - AGC Gain	8000	15 - 11	SET_AGC K\
3 - CD Threshold	A000	15 - 13	SET_CDth K\

5.2. SIGNAL TRANSFER : NOTES AND COMMENTS

All routines are between a memory location (directly addressed) in the DSP and the wanted MAFE register.

The points to keep in mind are that :

- it takes 2 accesses to read or write a sample,
- the DSP has 16-bit registers and the 12-bit samples are aligned on the left (bit 11 of the sample corresponds to bit 15 of the register),
- the transfer is made on the 8 most significant bits of the bus,
- in slow exchange mode the DSP repeats any instruction only when referring to an external address.

An example is given for receiving signals.

RXSI 10.X (get receive signal and transfer in location 10.X).

Instruction 1 : First read access

OPDI ; LDL $800.E ; ; LSRB L A\

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
b3	b2	b1	b0	X	X	X	X	X	X	X	X	X	X	X	X

DSP DATA BUS D0-D15

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	b3	b2	b1	b0	X	X	X	X

DSP ACCUMULATOR A

Instruction 2 : Second read access

OPDI ; LDL $800.E ;; OR L A F\

WARNING : this instruction is repeated twice (external access in slow access mode). The first time the data on the bus is wrong ; consequently the ALU result is wrong and must be ignored.

The second time the data on the bus is right ; consequently the ALU result is right and must be used (it is done in instruction 3). The FIFO is only used in order not to disturb the accumulator A. If accumulator A was used as ALU destination it would be loaded with a wrong value in the first cycle therefore the OR operation would give a bad result in the second cycle.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
b11	b10	b9	b8	b7	b6	b5	b4	X	X	X	X	X	X	X	X

DSP DATA BUS D0-D15

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
b11	b10	b9	b8	b7	b6	b5	b4	0	0	0	0	0	0	0	0

DSP INTERNAL DATA BUS L0-L15

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0	X	X	X	X

DSP ALU O/P REGISTER D

Instruction 3 :

SVR D 10.X\

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0	X	X	X	X

DSP XRAM LOCATION 10

5.3. PARAMETER SETTING : NOTES AND COMMENTS

The commands refer to a register and not a parameter. As most registers include 1 or several correlated parameters it does not create any problems ; however there are cases when 2 parameters are totally uncorrelated but are in the same register ; so when changing a parameter, the other parameter of the register can get inadvertently changed.

The user must be careful in the following cases :

- command RC2 will put tx sync to zero
- command SET_ATT will put exi to zero
- command SET_EXI will put attenuation to zero.

6. EXAMPLE : THE PROGRAM MAFTEST2

To develop the program MAFTEST2, macros from 3 different libraries have been used :

- the command language MAFCOM (cf. appendix B.2) just described in part 3
- PSIL1 : (cf. appendix B.3) it is a microprocessor type language. In this way programs are quicker to write and more readable than with the DSP assembler language ; the disadvantage however is that it does not make use of the parallelism of the DSP.

  PSIL1 is used for :

  - modules which do not require speed (initialization),
  - developing test programs.
- PSIUTIL : (cf. appendix B. 4) collection of utilities ; for the present time it is made of memory fill and timers.

6.1. DESCRIPTION

The program is divided in 4 small modules :

INITIALIZATION

- clear the rams
- move the sinewave from the CROM into the XRAM
- initialize the DSP with the MAFE access parameters
- initialize the XRAM and YRAM in circular addressing mode
- initialize the MAFE registers.

TRANSMITTER TEST

- WAIT1 : wait for an external clock edge.
  On the negative edge of the transmit sampling clock the program will do the transmit task.
  On the negative edge of the receive sampling clock the program will do the receive task.
- TXMIT : the sinewave stored in the YRAM is read and the samples sent to the signal o/p and echo o/p.
- RECEIVE : the receive signal (ATO being looped back on pin RAI) is stored in the XRAM ; the residual signal (EEO being looped back on pin EEI) is stored in the XRAM.
  Note that the estimated echo output is not smoothed and goes to zero for a small time (8 clock cycles = 1/1.44mHz/8 = 5.55µs).

RECEIVER TEST

The 2 signals stored in stage 1 in XRAM are displayed therefore giving the quality of the receiver path.

The receive signal (ATO being looped back on pin RAI) is added to the estimated echo and is stored in the YRAM ;

the residual signal (EEO being looped back on pin EEI) is stored in the YRAM.

ECHO CANCELLING

The 2 signals stored in stage 2 in YRAM are displayed therefore giving the receiver quality when added with the estimated echo.

Note : Addition and substraction of echo only differs by a 180 degree phase shift.

APPENDIX A - PROGRAMMING THE ACCESS MODE REGISTER (AMR)

The AMR is a 6-bit register (TS68930) 7-bit (TS68931) indicating the circuit I/O configuration.

BIT MEANING :

bit 0 -0 : Fast Exchange : external access in 160ns
1 : Slow Exchange : external access in 320ns

bit 1 -0 : Slave : slave mode on the system bus
1 : Pseudo-Slave : pseudo-slave mode

bit 2 -0 : Separate Bus : the local bus is separated into two 8-bit buses D0-D7 and D8-D15
1 : Concatenated Bus : the local bus is 16-bit wide

bit 3 -0 : memory byte-wide : 1 $\overline{RD}$ pin, 1 $\overline{WR}$ pin
1 : Motorola : 1 Data Strobe, 1 R/$\overline{W}$

bit 4 - 0 : DTACK : BE6 is redefined in DTACK signal for exchanges with a MCU belonging to TS68000 family
1 : BE6 : this pin can be used to test external signals

bit 5 -0 : Bus Available : BE5 is redefined as BA
1 : BE5 : this pin can be used to test external signals

bit 6 - MASK (TS68931 only)
0 : AMR not masked : AMR contents not restored to its initial state
1 : AMR masked : AMR contents restored to its initial state.

When an external HALT is applied, the AMR is forced into a predetermined configuration :

- bit 0 = 0 cycle 160ns
- bit 1 = 1 pseudo-slave mode
- bit 2 = 1 local bus concatenated
- bit 3 = 0 memory byte-wide protocol.

When the external HALT is no longer applied, the AMR contents is restored to its initial state only if bit 6 has been set to 1.

BIT 0 = 1 (SLOW EXCHANGE MODE) :

The MAFE being a slow peripheral it is accessed by the DSP in slow exchange mode.

All control signals start at the same time as in the standard read or write but they last an additional 160ns. In read cycle, the bus is sampled 160ns later.

It must be noted that it is purely an external exchange mode, since

- the TS68930 must be in REAL mode,
- the circuit automatically repeats the instruction where the exchange takes place,
- during this exchange, management of the addresses, of the processing block, of the loop counters are under the responsibility of the programmer who has to take into account the repetition of the instruction.

BIT 1 = 1 (PSEUDO SLAVE)

When the DSP is programmed as slave it can only have 4 bits of external address (A8-A11).

To access the MAFE the AMR must be programmed as follows

INI REAL SAT ; AMR % 1111011\

When the DSP is programmed as pseudo-slave it will have 12 bits of external address (A8-A11 + AD0-AD7) ; the system data bus (AD0-AD7) is then used to supply the lower address lines of the local bus.

BIT 2 = 0 (SEPARATE BUSES)

This feature is useful when accessing an 8-bit device such as the MAFE since :

- when reading, the 8 unused read bits are puts to zero,
- when writing, the 8 unused written bits are put in tri-state.

The bus is selected by the address lines [A10-A11] according to the following table :

A10	A11	Selected Bus	Non Selected Bus
0	0	D0-D7	D8-D15
0	1	D8-D15	D0-D7
1	0	D8-D15	D0-D7
1	1	D8-D15	D0-D7

BIT 3 = 1 (MOTOROLA TYPE SIGNAL R/$\overline{W}$ & $\overline{DS}$)

BIT 4 = 1 (BE6 is used to test TX conversion clock)

BIT 5 = 1 (BE5 is used to test RX conversion clock)

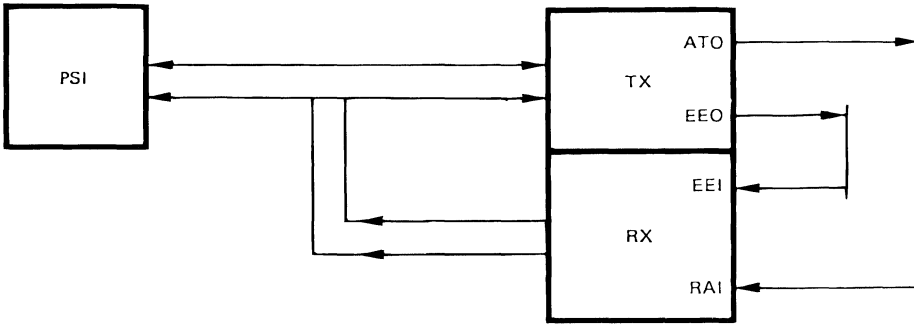
BIT 6 = 1 (for emulation purpose only).

APPENDIX B - PROGRAM LISTINGS

B1 — The test program MAFTEST 2

```
" ##########################################################################
#################### HERE IS THE TEST PROGRAM MAFTEST2 ##################
####################      V1.3  01NOV86          ##############################
#################### AUTHOR :  F.M.J RAYMONDOU ############################
##########################################################################

FUNCTION : TEST THE 4 SIGNALS :
           ATO (TX SIGNAL)
           RAI (RECEIVE SIGNAL),
           EEO (ESTIMATED ECHO )
           EEI (RESIDUAL SIGNAL )
        TEST THE CLOCK GENERATOR
        TEST ATTENUATION ON TRANSMITER & AMPLIFICATION ON RECEIVER
        TEST ECHO CANCELLING PATH

HOW ? : - GENERATION OF A SINEWAVE IN THE PSI

      STAGE1:
      -------
      - SEND IT TO THE 2 TX REGISTERS
      - OUTPUT ATO (WITH ATTENUATION 6DB)
      - OUTPUT EEO (NO ATTENUATION POSSIBLE )
---> CHECK EEO & ATO ON SCOPE: IT IS THE SAME SINEWAVE, ONE SAMPLED (EEO), THE
      OTHER FILTERED & ATTENUATED BY 6 DB (ATO)

      - LOOP BACK ATO TO THE RX INPUT RAI THROUGH A DIVIDER BRIDGE 27 DB
      - AND AMPLIFY INTERNALLY OF 33DB
      - LOOP BACK EEO TO THE RX INPUT EEI
      - STORE THE RX REGISTERS IN THE PSI XRAM

      STAGE2:
      -------
       (NO MORE ATTENUATION NOR AMPLIFICATION BUT ECHO CANCELLING PATH)

      - SEND THE 2 STORED SIGNALS IN XRAM TO THE 2 TX REGISTERS
      - OUTPUT ATO ( NO ATTENUATION )
      - OUTPUT EEO
---->CHECK ATO & EEO :  ATO AFTER 6+27 ATTENUATION & 33DB AMPLIFICATION
                        HAS THE SAME AMPLITUDE THAN EEO

      - LOOP BACK ATO TO THE RX INPUT RAI THROUGH A DIVIDER BRIDGE 27 DB
      - LOOP BACK EEO TO THE RX INPUT EEI
      - INTERNALLY EEO + ATO/27DB == EEO
      - RECEIVE SIGNAL = SMOOTHED EEO
      - RESIDUAL SIGNAL = EEO
      - STORE THE RX REGISTERS IN THE PSI YRAM


      STAGE3:
      ------
      - SEND THEM TO THE TX REGISTERS

---->CHECK ATO & EEO :  ATO = SMOOTHED EEO OF THE FORMER STAGE
                        EEO = EEO OF THE FORMER STAGE
```

```
-------
THEN THE PROGRAM LOOPS ON THIS THREE STAGES

NOTE=ALSO IT CAN BE CHECKED :
        - THE GENERATED CLOCKS
        - AGC1 RECEIVER PIN (RECEIVED SIGNAL BEFORE AMPLIFICATION)
        - EEI & RAI INPUTS
```




```
################################################################################

        .SIMUL
        .MOTOROLA
" DEFINING A 16-POINT SINUSOID"
        .MEMORY HEXA
        CROM($50)= 0000
                CF04
                A57E
                89BE
                8000
                89BE
                A57E
                CF04
                0000
                30FC
                5A82
                7642
                7FFF
                7642
                5A82
                30FC \
        .ENDMEM
        .ASG RC1 = $0000
        .ASG RC2 = $2000
        .ASG RC3 = $4000
        .ASG RC4 = $6000
        .ASG RC5 = $8000
        .ASG RC6 = $A000
        .ASG RC7 = $C000
        .ASG RC8 = $E000

.ASG SAMPLES = 9  "address of timer : number of samples "
.ASG ACQTIME = 10  "address of timer :acquisition before display  "
```

```
"-------------------INITIALISATIONS--------------------------"

      XRAMCLR \
      YRAMCLR \
START:  BLCKMOV $50,16,$10, Y0 \
      INIMAFE \
      INI REAL,SAT ;Y1   $1F  ;X1   $2F \
      INI REAL,SAT ;Y0_C $10  ;X0_C $10 \
      INI REAL,SAT ;Y0_C $10  ;X0_C $10 \
      RC1 A,4 \".............BIT=2.4KHZ ,BAUD=.6KHZ....."
      RC2 4,0 \".............MUX=7.2KHZ ,FS=9.6KHZ......"
      RC3 2,1,0 \".............BANDPASS .5--1.6KHZ........"
      SET_AGC 16 \".........33 DB AMPLIFICATION........"
      SET_ATT 3 \".........6 DB ATTENUATION..........."
      INITIMER SAMPLES.X ,16 \
      INITIMER ACQTIME.X , 2400 \"4 S waiting "


"---------- TRANSMITTER TEST ---------------------------------"

WAIT1:  IFTXC TXMIT \
      IFRXC RECEIVE \
      BRANCH WAIT1 \

TXMIT:  OPIN ; LDL [Y0]+ , T \
      TXSO T \    ".....TX SINEWAVE ON SIGNAL O/P....."
      TXEE T \    ".....TX SINEWAVE ON ECHO O/P....."

      DECTIMER SAMPLES.X \ " one sample less to transmit "
      IFNOZERO WAIT1\
      INITIMER SAMPLES.X , 16 \
      DECTIMER ACQTIME.X \
      IFNOZERO WAIT1 \
      SET_AGC 0 \".....NO AMPLIFICATION ....."
      RC3 2,1,011 \".....SET-UP ECHO CANCELLING ....."
      SET_ATT 0\
      INITIMER ACQTIME.X , 2400 \
      INI REAL,SAT; Y1_C $2F \
      GOTO  WAIT2 \

RECEIVE:RXSI T \ ".....RX ATO ON RAI by a divider bridge........"
      ST T , [X0]+ \ "and store it in XRAM"
      RXRES T \ "....RX EEO ON EEI....."
      ST T , [X0]+ \ "and store it in XRAM"
      GOTO  WAIT1 \


"---------------- RECEIVER TEST ------------------------ "

WAIT2:  IFTXC TX2 \
      IFRXC RX2 \
      BRANCH WAIT2 \

TX2:    OPIN ;  LDL [X0]+ , T \
      TXSO T \   "....TX RR1 ON ATO ....."
      OPIN ;  LDL [X0]+ , T \
      TXEE T \   "....TX RR2 ON EEO....."

      DECTIMER SAMPLES.X \
      IFNOZERO WAIT2 \
      INITIMER SAMPLES.X , 16 \
```

```
        DECTIMER ACQTIME.X \
        IFNOZERO WAIT2 \
        INITIMER ACQTIME.X,2400 \
        GOTO WAIT3 \

RX2:    RXSI T \ ".....RX ATO ON RAI by a divider bridge....."
        ST T , [Y0]+ \ "and store it in YRAM"
        RXRES T \ "....RX EEO ON EEI....."
        ST T , [Y0]+ \ "and store it in YRAM"
        GOTO WAIT2 \

"_____ECHO CANCELLING _____


WAIT3:  IFTXC TX3 \
        BRANCH WAIT3 \

TX3:    OPIN ;  LDL [Y0]+ , T \
        TXSO T \
        OPIN ;  LDL [Y0]+ , T \
        TXEE T \

        DECTIMER SAMPLES.X \
        IFNOZERO WAIT3 \
        INITIMER SAMPLES.X , 16 \
        DECTIMER ACQTIME.X \
        IFNOZERO WAIT3 \
        GOTO START \


.END
```

B.2 — The command language MAFCOM

```
"#####################################################################
###### HERE IS DEFINED THE MAFE COMMAND LANGUAGE MAFCOM ########
#######################    V1.5    jan87    ####################
#### AUTHOR : D.F MARTIN                          ##############
#####################################################################
FUNCTION : THIS LANGUAGE IS  USED TO COMMAND THE MAFE KIT WITH THE
           TS68930 PSI.

S/W DEVELOPMENT TOOLS:- TS68930  MACRO-ASSEMBLER (PSIMAC) ON VAX-VMS .
                - MACRO LIBRARY :PSIL1
                - MACRO LIBRARY :PSIUTIL
S/W DEVELOPMENT TIME : 1 DAY  .

TEST TOOLS:- TS68930  REAL-TIME EMULATOR/EVALUATION BOARD (EVA-PSI )
        - MAFE EVALUATION BOARD (EVM-MAFE)
TEST TIME : 1 WEEK
#####################################################################"

.CROSS
.MAP

"**** SIGNAL REGISTER ADDRESSES ********************************"
.ASG Tx =  $800
.ASG Rx =  $800
.ASG EE =  $900
.ASG RES = $900
.ASG CD =  $A00
"**** CONTROL REGISTER ADDRESSES *******************************"
.ASG RC1 = $0000
.ASG RC2 = $2000
.ASG RC3 = $4000
.ASG RC4 = $6000
.ASG RC5 = $8000
.ASG RC6 = $A000
.ASG RC7 = $C000
.ASG RC8 = $E000


"**** READING & WRITING SIGNAL SAMPLES *******************************"

.LIBRARY TXSO ADDIR \
 LSL 8 ^ADDIR^ A \
 SVR A $800.E \
 LDA ^ADDIR^ \
 SVR A $800.E \
 .ENDMAC

.LIBRARY RXSI ADDIR \
OPDI ;LDL $800.E;;LSRB L A \
OPDI ;LDL $800.E;;OR L A,F \ WARNING : FIFO becomes useless
SVR D ^ADDIR^ \
.ENDMAC

.LIBRARY TXEE  ADDIR \
 LSL 8 ^ADDIR^ A \
 SVR A $900.E \
 LDA ^ADDIR^ \
 SVR A $900.E \
.ENDMAC
```

```
.LIBRARY RXRES ADDIR \
 OPDI ;LDL $900.E ;;LSRB L A \
 OPDI ;LDL $900.E ;;OR L A,F \ WARNING : FIFO becomes useless
 SVR D ^ADDIR^\
.ENDMAC

"**** CARRIER DETECT ******************************"

.LIBRARY CD ADDIR\
 OPDI ;LDL $A00.E ;;TRA L A \
 SVR A ^ADDIR^ \
.ENDMAC


"**** CLOCK CONTROL ******************************"

.LIBRARY RC1 BIT , BAUD \
 OPIM ;LDR RC1,N ; TRA R A \
 SVR A $A00.E \
 OPIM ;LDR ( ($^BIT^ * (2 ** 12 )) + (^BAUD^ * (2 ** 9)) ), N ; TRA R A \
 SVR A $B00.E \
.ENDMAC

.LIBRARY RC2 MUX , FS \   ATTENTION TX_SYNC HAS BEEN PUT TO ZERO
 OPIM ;LDR RC2,N ; TRA R A \
 SVR A $A00.E \
 OPIM ;LDR ( (^MUX^*(2**13))+(^FS^*(2**11)) ),N; TRA R A \
 SVR A $B00.E \
.ENDMAC

.LIBRARY RC2SYNC MUX , FS , K \
 OPIM ;LDR RC2,N ; TRA R A \
 SVR A $A00.E \
 OPIM ;LDR ((^MUX^*(2**13))+(^FS^*(2**11))+(^K^*(2**9))),N; TRA R A \
 SVR A $B00.E \
.ENDMAC

.LIBRARY RXPSA K\
 OPIM ;LDR RC7,N ; TRA R A \
 SVR A $A00.E \
 OPIM ;LDR ( $^K^ * (2 ** 11)), N ; TRA R A \
 SVR A $B00.E \
.ENDMAC

.LIBRARY RXDPLL K\
 OPIM ;LDR RC8,N ; TRA R A \
 SVR A $A00.E \
 OPIM ;LDR (^K^  * (2 ** 12)), N ; TRA R A \
 SVR A $B00.E \
.ENDMAC

"**** TRANSMITTER CONTROL ******************************"

.LIBRARY SET_ATT K\   ATTENTION EXI HAS BEEN PUT TO ZERO
 OPIM ;LDR RC4,N ; TRA R A \
 SVR A $A00.E \
 OPIM ;LDR ( $^K^  * (2 ** 12)), N ; TRA R A \
 SVR A $B00.E \
.ENDMAC
```

```
.LIBRARY SET_EXI K\   ATTENTION ATT HAS BEEN PUT TO ZERO
 OPIM ;LDR RC4,N ; TRA R A \
 SVR A $A00.E \
 OPIM ;LDR (^K^ * (2 ** 9)), N ; TRA R A \
 SVR A $B00.E\
.ENDMAC

"**** RECEIVER CONTROL ******************************"

.LIBRARY RC3  HPF,LPF,RSR\
 OPIM ;LDR RC3,N ; TRA R A \
 SVR A $A00.E \
 OPIM ;LDR (^HPF^ *(2**14)+^LPF^*(2**12)+(%^RSR^ (<<) 9) ), N ; TRA R A \
 SVR A $B00.E \
.ENDMAC

.LIBRARY SET_AGC K\
 OPIM ;LDR RC5,N ; TRA R A \
 SVR A $A00.E \
 OPIM ;LDR ( $^K^  * (2 ** 11)), N ; TRA R A \
 SVR A $B00.E \
.ENDMAC

.LIBRARY SET_CDth K\
 OPIM ;LDR RC6,N ; TRA R A \
 SVR A $A00.E \
 OPIM ;LDR ( $^K^  * (2 ** 13)), N ; TRA R A \
 SVR A $B00.E \
.ENDMAC

"############ INITIALIZATION ##############################"
.LIBRARY INIMAFE \
      LDK 0 \
      STA $0A00.E \
      INI REAL,SAT ;AMR %1111011\
 REPEAT 16 TIMES ; REAL,SAT \
 BEGIN:
      STA $0B00.E \
 END:
.ENDMAC


"############# CLOCK  TEST ############################"
.LIBRARY IFTXC PC_ADDIR \
      BRANCH BE6 ^PC_ADDIR^ \
.ENDMAC

.LIBRARY IFRXC PC_ADDIR \
      BRANCH BE5 ^PC_ADDIR^ \
.ENDMAC
```

B.3 — The library PSIL1

```
"#########################################################################
###### HERE IS DEFINED THE GENERAL LANGUAGE PSIL1 ###############
#######################    V2.21   OCT 86   ######################
#### AUTHOR : D.F MARTIN  (33) 76 49 36 00  X3823  ##############
#########################################################################"
.CROSS
.MAP
"**** OPERATION ON ACCUMULATOR A ******************************
** LDA , STA , ADD , SUB , MSUB , ADDC , AND , OR , XOR , LDK ,COM **
   ASRA , LSRA , RORA , LSLA "

. LIBRARY LDA ADDIR \
 OPDI ;LDL ^ADDIR^ ;; TRA L A \
.ENDMAC

.LIBRARY STA ADDIR \
 SVR A ^ADDIR^\
.ENDMAC

.LIBRARY ADD ADDIR \
 OPDI ;LDL ^ADDIR^ ;; ADD L A A \
.ENDMAC

.LIBRARY SUB ADDIR \
 OPDI ;LDL ^ADDIR^ ;; SUBR L A A \
.ENDMAC

.LIBRARY MSUB ADDIR \
 OPDI ;LDL ^ADDIR^ ;; SUB L A A \
.ENDMAC

.LIBRARY ADDC  ADDIR \
 OPDI ;LDL ^ADDIR^ ;; ADDC L A A \
.ENDMAC

.LIBRARY AND ADDIR \
 OPDI ;LDL ^ADDIR^ ;; AND L A A \
.ENDMAC

.LIBRARY OR ADDIR \
 OPDI ;LDL ^ADDIR^ ;; OR L A A \
.ENDMAC

.LIBRARY XOR ADDIR \
 OPDI ;LDL ^ADDIR^ ;; XOR L A A \
.ENDMAC

.LIBRARY LDK CONSTANT \
 OPIM ;LDR ^CONSTANT^ ,N ; TRA R A \
.ENDMAC

.LIBRARY COM ADDIR \
 OPDI ;LDL ^ADDIR^ ;; COM L A  \
.ENDMAC

.LIBRARY ASRA NN \
OPIN ST A, T\
ASR ^NN^ T A\
.ENDMAC
```

```
.LIBRARY LSRA NN \
OPIN ST A, T\
LSR ^NN^ T A\
.ENDMAC

.LIBRARY RORA NN \
OPIN ST A, T\
ROR ^NN^ T A\
.ENDMAC

.LIBRARY LSLA NN \
OPIN ST A, T\
LSL ^NN^ T A\
.ENDMAC

"**** OPERATION BETWEEN ACCUMULATORS ****************************
"
.LIBRARY HIDE\
OPIN ST A, T; LDL T;; TRA L,B\
.ENDMAC

.LIBRARY SEEK\
OPIN ST B, T; LDL T;; TRA L,A\
.ENDMAC

"**** OPERATION WITHOUT MODIFYING ACCUMULATOR ****************************
** LDD , STD , ADDD , SUBD , MSUBD , ADDCD , ANDD , ORD , XORD , LDKD*
"
. LIBRARY LDD ADDIR \
 OPDI ;LDL ^ADDIR^ ;; TRA L F \
.ENDMAC

.LIBRARY STD ADDIR \
 SVR D ^ADDIR^\
.ENDMAC

.LIBRARY ADDD ADDIR \
 OPDI ;LDL ^ADDIR^ ;; ADD L A F \
.ENDMAC

.LIBRARY SUBD ADDIR \
 OPDI ;LDL ^ADDIR^ ;; SUBR L A F \
.ENDMAC

.LIBRARY MSUBD ADDIR \
 OPDI ;LDL ^ADDIR^ ;; SUB L A F \
.ENDMAC

.LIBRARY ANDD ADDIR \
 OPDI ;LDL ^ADDIR^ ;; AND L A F \
.ENDMAC

.LIBRARY ORD ADDIR \
 OPDI ;LDL ^ADDIR^ ;; OR L A F \
.ENDMAC

.LIBRARY XORD ADDIR \
 OPDI ;LDL ^ADDIR^ ;; XOR L A F \
.ENDMAC
```

```
.LIBRARY LDKD CONSTANT \
 OPIM ;LDR ^CONSTANT^ ,N ; TRA R F \
.ENDMAC

"**** OPERATION MEMORY TO MEMORY ****************************
** MOVE , MOVK*
"
. LIBRARY MOVE SRCADDIR , DSTADDIR \
 OPDI ;LDL ^SRCADDIR^ ;; TRA L F \
 SVR D ^DSTADDIR^\
.ENDMAC

.LIBRARY MOVK CONSTANT , DSTADDIR\
 OPIM ;LDR ^CONSTANT^ ,N ; TRA R F \
 SVR D ^DSTADDIR^\
.ENDMAC

"****  OPERATIONS  WITH INDIRECT ADDRESSING **********************
** LD , ST  , MASK ************************************************"

. LIBRARY LD INDIRADR , REG \
.IF (('^INDIRADR 2 3 ^'(=)'E0') (+) ('^INDIRADR 2 3 ^'(=)'Y1'))
  OPIN ;              ;LDR ^INDIRADR^ ; TRA R ^REG^ \
.ELSE
  OPIN ;LDL ^INDIRADR^ ;              ; TRA L ^REG^ \
.ENDIF
.ENDMAC

.LIBRARY ST  REG , INDIRADR \
 OPIN ST ^REG^ ^INDIRADR^\
.ENDMAC

.LIBRARY MASK INDIRADR , CONSTANT \
 OPIM LDL ^INDIRADR^ ,M ;LDR ^CONSTANT^ ,N ; AND L R A \
.ENDMAC
"ATTENTION : NOT OPERATIONAL WITH POINTERS E0,Y1"

"**** OPERATION ON POINTERS ******************************
 ****** LDP , INCP , DECP , ADDP , INIP **************
"
.LIBRARY LDP  POINTER \
 OPDI ST D ^POINTER^ ;;;\
.ENDMAC

.LIBRARY INCP POINTER \
.IF ( ('^POINTER 1 2 ^'(=)'E0') (+) ('^POINTER 1 2 ^'(=)'Y1') )
  OPIN ;;LDR [^POINTER^]+ ; \
.ELSE
  OPIN ;LDL [^POINTER^]+ ;; \
.ENDIF
.ENDMAC

.LIBRARY DECP POINTER \
.IF ( ('^POINTER 1 2 ^'(=)'E0') (+) ('^POINTER 1 2 ^'(=)'Y1') )
  OPIN ;;LDR [^POINTER^]- ; \
.ELSE
  OPIN ;LDL [^POINTER^]- ;; \
.ENDIF
.ENDMAC
```

```
.LIBRARY ADDP  POINTER  ,NN \
 SVR ^POINTER^ T\
 OPIM LDL T M ;LDR ^NN^  N ; ADD L R F\
 OPDI ST D ^POINTER^ \
.ENDMAC

. LIBRARY INIP POINTER ,VALUE \
.IF ( ('^POINTER^'(=)'Y0') (+) ('^POINTER^'(=)'Y1') )
  INI REAL SAT ; ^POINTER^ ^VALUE^ ; \
.ELSE
  INI REAL SAT ;; ^POINTER^ ^VALUE^  \
.ENDIF
.ENDMAC

"**** OPERATION ON PROGRAM SEQUENCE ******************************
*****GOTO ,IFPOS ,IFNEG ,IFCARRY ,IFZERO ,IFNOZERO ,CALLA , PUSHX,
    PULLX , WAIT ***************************************************"

.LIBRARY GOTO PC_ADDR \
 BRANCH ^PC_ADDR^ \
.ENDMAC

.LIBRARY IFPOS PC_ADDR \
 BRANCH NOSR ^PC_ADDR^ \
.ENDMAC

.LIBRARY IFNEG PC_ADDR \
 BRANCH SR ^PC_ADDR^ \
.ENDMAC

.LIBRARY IFCARRY PC_ADDR \
 BRANCH CR ^PC_ADDR^ \
.ENDMAC

.LIBRARY IFZERO PC_ADDR \
 BRANCH Z ^PC_ADDR^ \
.ENDMAC

.LIBRARY IFNOZERO PC_ADDR \
 BRANCH NOZ ^PC_ADDR^ \
.ENDMAC

.LIBRARY CALLA \
 BRANCH A ; SVPC RAR \
.ENDMAC

.LIBRARY PUSHX PC_ADDR\
 BRANCH ^PC_ADDR^ ; SVPC [X1]-\
.ENDMAC

.LIBRARY PULLX\
 INCP X1\
 LD [X1] , A\
 BRANCH A\
.ENDMAC

.LIBRARY WAIT COND \
  WAIT& : BRANCH  NO^COND^  WAIT&  \
 .ENDMAC
```

```
"***** DO\ENDO********
"
.LIBRARY DO N \
        LDKD ^N^ \
 DOBEG&: OPIN ST D T\
.ENDMAC

.LIBRARY ENDO \
 OPIM LDL T ;LDR 1 ;SUB L R F \
 IFNOZERO (DOBEG& + 1)\
.ENDMAC



"**** OPERATIONS ON AMR ******************************
 ****** AMRSLOW , AMRFAST **************
"
.LIBRARY AMRSLOW \
 INI REAL SAT ;AMR $7F ;\
.ENDMAC

.LIBRARY AMRFAST \
 INI REAL SAT ;AMR $7E ;\
.ENDMAC

"**** INITIALIZE MODE ******************************
 ****** REAL , CMPLX , DBPR **************
"
.LIBRARY REAL \
 INI REAL SAT \
.ENDMAC

.LIBRARY CMPLX \
 INI CMPLX SAT \
.ENDMAC

.LIBRARY DBPR \
 INI DBPR NOSAT \
.ENDMAC

"**** OPERATION ON FLAGS ******************************
 ****** EMPTYFIF , RDYOIN **************
"
.LIBRARY EMPTYFIF \
 INI REAL SAT ;EF 1 ;\
.ENDMAC

.LIBRARY RDYOIN1 \
 INI REAL SAT ;RDYOIN 1 ;\
.ENDMAC




.END
```

B.4 — The library PSIUTIL

```
"#################################################################
################### HERE ARE THE PSI UTILITIES :PSIUTIL ###############
############################### V2.3  7/10/86 ##########################
######################## authorS : D.F.MARTIN , F.RAYMONDOU ############
#################################################################################*"


"################ CLEAR XRAM ########################"
.LIBRARY  XRAMCLR \
      REPEAT 128 TIMES ;REAL SAT\
      INI REAL SAT;          ; X0 $00 \
      LDK 0\
BEGIN:
      OPIN ST A  [X0]+\
END:
.ENDMAC

"################ CLEAR YRAM ########################"
.LIBRARY  YRAMCLR \
      REPEAT 128 TIMES ;REAL SAT\
      INI REAL SAT;Y0 $00     ; \
      LDK 0\
BEGIN:
      OPIN ST A  [Y0]+\
END:
.ENDMAC

"################ CLEAR ERAM FIRST 128 ONLY ############"
.LIBRARY  ERAMCLR \
      REPEAT 128 TIMES ;REAL SAT\
      INI REAL SAT;          ; E0 $00 \
      LDK 0\
BEGIN:
      OPIN ST A  [E0]+\
END:
.ENDMAC

"########## BLOCK MOVE CROM -----> RAM ############"
.LIBRARY BLCKMOV  SRC , LENGTH , DEST ,POINTER \
      LDK ^SRC^ \
      LDP C0 \
      LDK ^DEST^ \
      LDP ^POINTER^ \
REPEAT (^LENGTH^ - 1) TIMES;REAL,SAT  \      "LOOP ; PIPELINE OF 1 "
      OPIN ; LDL  [C0]+  ;; TRA L A \
BEGIN:
      OPIN ST A  [^POINTER^]+ ; LDL  [C0]+  ; ; TRA L A\
END:
      OPIN ST A  [^POINTER^]+  \
      .ENDMAC

"########################################"
.LIBRARY TIMEOUT  K \
       LDK  ^K^ \
 LZOOP&: SI A 1 \
      OPIM LDL T , M; LDR 1 ,N ; SUB L R A \
      IFNOZERO LZOOP& \
.ENDMAC
```

```
"################ TIME OUT from 0 to 1 hour ##########################
######## real : ( T1 X T2 ) X 800ns (5 cycles)
            MAX = 2 ** 32 x 800ns === 3200 s
#############################################################################"
.LIBRARY TIMEOUTD T1 ,T2 \
      LDK  ^T1^ \
      OPIN ST A T ; LDL T ;;TRA L B\
      LDK  ^T2^ \
LZXOOP&:ST A T \
      NOP\ for ease of counting cycles
      OPIM LDL T , M; LDR 1 ,N ; SUB L R A \
      IFNOZERO LZXOOP& \
      ST B T \
      OPIM LDL T , M; LDR 1 ,N ; SUB L R B \
      IFNOZERO (LZXOOP& - 1 )\
.ENDMAC

"#####################################"
.LIBRARY INITIMER ADDIR , K\
      LDK ^K^\
      STA ^ADDIR^\
.ENDMAC

"#####################################"
.LIBRARY DECTIMER ADDIR\
      LDK 1\
      MSUB ^ADDIR^\
      STA ^ADDIR^\
.ENDMAC

"#########################################"
.LIBRARY INICTR ADDIR \
      LDK 0\
      STA ^ADDIR^ \
.ENDMAC

"#########################################"
.LIBRARY INCCTR ADDIR \
      LDK 1 \
      ADD ^ADDIR^ \
      STA ^ADDIR^ \
.ENDMAC
```

DSP APPLICATION NOTE SUMMARY

This summary is the list of all available application notes around SGS-THOMSON digital signal processors family. These application notes will not be printed in the data-book for space reasons, but are listed here for convenience.

- Interfacing the TS68930/31 with D/A converters AM6012, DAC808.
- Interfacing the TS68930/31 with 8031/51 Intel family of processors.
- Examples of mailbox communications between two TS68930 and a Modem Analog Front End (MAFE) chip set.
- Interfacing the TS68930/31 to analog signals.
- Lattice filter implementation with SGS-THOMSON DSP's.
- TS68931 instruction bus optimized interface.
- Sine and cosine implementation with TS68930/31 routines.
- TS68930/31 extended data memory applications schematic.
- Interface schematic for 8086 host processor to the ST18930/31 digital signal processors.
- Digital IIR filter development and evaluation programs for the TS68930/31 digital signal processors.
- Development of real time algorithms using the TS68930/31 DSP and the MAFE chip set.

EUROPE

DENMARK

2730 HERLEV
Herlev Torv, 4
Tel. (45-42) 94.85.33
Telex: 35411
Telefax: (45-42) 948694

FINLAND

LOHJA SF-08150
Karjalankatu, 2
Tel. 12.155.11
Telefax. 12.155.66

FRANCE

94253 GENTILLY Cedex
7 - avenue Gallieni - BP. 93
Tel.: (33-1) 47.40.75.75
Telex: 632570 STMHQ
Telefax: (33-1) 47.40.79.10

67000 STRASBOURG
20, Place des Halles
Tel. (33) 88.75.50.66
Telex: 870001F
Telefax: (33) 88.22.29.32

GERMANY

6000 FRANKFURT
Gutleutstrasse 322
Tel. (49-69) 237492
Telex: 176997 689
Telefax: (49-69) 231957
Teletex: 6997689=STVBP

8011 GRASBRUNN
Bretonischer Ring 4
Neukeferloh Technopark
Tel.: (49-89) 46006-0
Telex: 528211
Telefax: (49-89) 4605454
Teletex: 897107=STDISTR

3000 HANNOVER 1
Eckenerstrasse 5
Tel. (49-511) 634191
Telex 175118418
Teletex: 5118418 csfbeh
Telefax: (49-511) 633552

8500 NÜRNBERG 20
Erlenstegenstrasse, 72
Tel.: (49-911) 59893-0
Telex: 626243
Telefax: (49-911) 5980701

5200 SIEGBURG
Frankfurter Str. 22a
Tel. (49-2241) 660 84-86
Telex: 889510
Telefax: (49-2241) 67584

7000 STUTTGART
Oberer Kirchhaldenweg 135
Tel. (49-711) 692041
Telex: 721718
Telefax: (49-711) 691408

ITALY

20090 ASSAGO (MI)
V.le Milanofiori - Strada 4 - Palazzo A/4/A
Tel. (39-2) 89213.1 (10 linee)
Telex: 330131 - 330141 SGSAGR
Telefax: (39-2) 8250449

40033 CASALECCHIO DI RENO (BO)
Via R. Fucini, 12
Tel. (39-51) 591914
Telex: 512442
Telefax: (39-51) 591305

00161 ROMA
Via A. Torlonia, 15
Tel. (39-6) 8443341
Telex: 620653 SGSATE I
Telefax: (39-6) 8444474

NETHERLANDS

5652 AR EINDHOVEN
Meerenakkerweg 1
Tel.: (31-40) 550015
Telex: 51186
Telefax: (31-40) 528835

SPAIN

08021 BARCELONA
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Tel. (34-3) 4143300-4143361
Telefax: (34-3) 2021461

28027 MADRID
Calle Albacete, 5
Tel. (34-1) 4051615
Telex: 27060 TCCEE
Telefax: (34-1) 4031134

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S-16421 KISTA
Borgarfjordsgatan, 13 - Box 1094
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Telefax: (46-8) 7504950

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Globe Park
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Telex: 847458
Telefax: (44-628) 890391

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R. Henrique Schaumann 286-CJ33
Tel. (55-11) 883-5455
Telex: (391)11-37988 "UMBR BR"
Telefax : 11-551-128-22367

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203-233, New South Head Road
Tel. (61-2) 327.39.22
Telex: 071 126911 TCAUS
Telefax: (61-2) 327.61.76

CHINA

BEIJING
Liason Office
Beijing No. 5 Semiconductor
Device Factory
14 Wu Lu Tong Road
Da Sheng Man Wai
Tel. (861) 2024378
Telex 222722 STM CH

HONG KONG

WANCHAI
22nd Floor - Hopewell centre
183 Queen's Road East
Tel. (852-5) 8615788
Telex: 60955 ESGIES HX
Telefax: (852-5) 8656589

INDIA

NEW DELHI 110001
LiasonOffice
62, Upper Ground Floor
World Trade Centre
Barakhamba Lane
Tel. 3715191
Telex: 031-66816 STMI IN
Telefax: 3715192

MALAYSIA

PULAU PINANG 10400
4th Floor - Suite 4-03
Bangunan FOP-123D Jalan Anson
Tel. (04) 379735
Telefax (04) 379816

KOREA

SEOUL 121
8th floor Shinwon Building
823-14, Yuksam-Dong
Kang-Nam-Gu
Tel. (82-2) 553-0399
Telex: SGSKOR K29998
Telefax: (82-2) 552-1051

SINGAPORE

SINGAPORE 2056
28 Ang Mo Kio - Industrial Park 2
Tel. (65) 4821411
Telex: RS 55201 ESGIES
Telefax: (65) 4820240

TAIWAN

TAIPEI
12th Floor
571, Tun Hua South Road
Tel. (886-2) 755-4111
Telex: 10310 ESGIE TW
Telefax: (886-2) 755-4008

JAPAN

TOKYO 108
Nisseki - Takanawa Bld. 4F
2-18-10 Takanawa
Minato-Ku
Tel. (81-3) 3280-4121
Telefax: (81-3) 3280-4131

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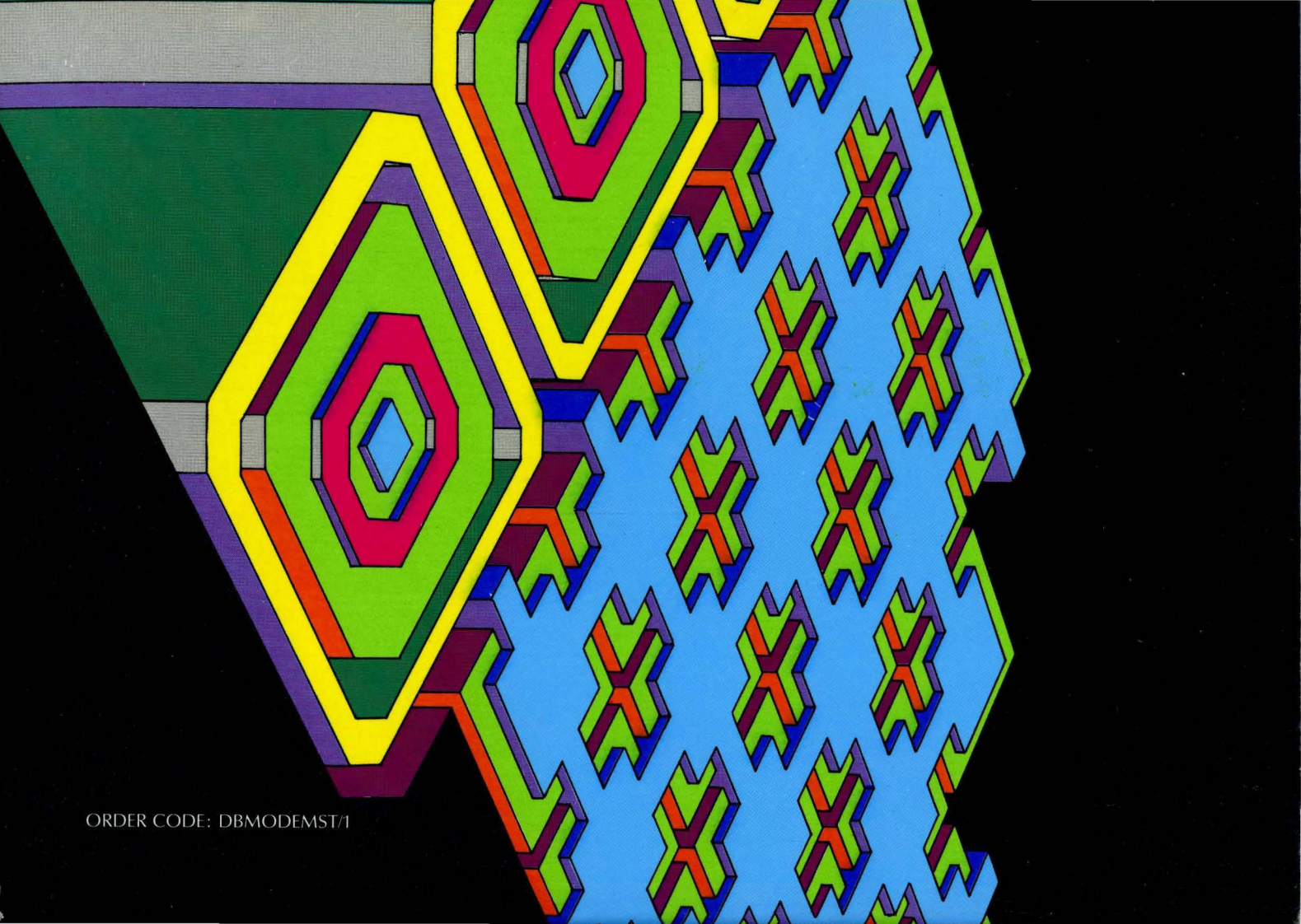

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