HIGH SPEED CMOS

DATABOOK

1st EDITION

SGS-THOMSON MICROELECTRONICS

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INTRODUCTION

High Speed CMOS devices have been established in SGS-THOMSON since 1983. The product range has inevitably expanded and the performance of many products has been improved. These changes are reflected in this new edition of the High Speed CMOS databook. In particular AC parameters for military applications are included for all devices.

Surface mounting technologies are very much in demand in industry consequently almost all devices now are offered with a surface mounting package option which is detailed in the datasheets.

High Speed CMOS offers designers logic integrated circuits with a power consumption lower than other logic integrated circuits and high switching speeds equal to that of LSTTL. These devices also have a better noise margin, and an improved voltage and temperature operating range. Additionally they are pin-to-pin compatible with either LSTTL or conventional CMOS B series. This reduces the need for logical redesign when they are adopted as replacements in designs using LSTTL or CMOS B series devices.

The extensive data provided in this databook makes it easy to evaluate the performace of the product within any required equipment design.

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SELECTION GUIDE

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	NOR		HC02, HC27, HC4002, HC4078
	AND		HC08, HC11, HC21
	OR		HC32, HC4072, HC4075, HC4078
	INVERTER		HCU04, HC04, HCT04
	BUFFER		HCT7007, HC4049B, HC4050B
		3-STATE	HC125, HC126, HC240, HCT240, HC241, HCT241, HC244, HCT244, HC365, HC366, HC367, HC368, HC540, HCT540 HC541, HCT541
		BIDIRECTIONAL	HC242, HC243, HC245, HCT245, HC620, HC623, HC640, HCT640, HC643, HCT643
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	SCHMITT TRIGGER		HC14, HC132
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	D FLIP-FLOP		HC74, HC174, HC175, HC273, HC377
		3-STATE	HC374, HCT374, HC534, HC564, HCT564, HC574, HCT574, HC646, HCT646, HC648, HCT648, HC651, HCT651, HC652, HCT652
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		DECADE	HC160, HC162, HC190, HC192, HC390, HC690, HC692, HC696, HC698, HC4518
		DIVIDER	HC292, HC294, HC4017, HC4020, HC4022, HC4024, HC4040, HC4060, HC40102, HC40103, HC7292, HC7294
MULTIPLEXER		ANALOG	HC4066
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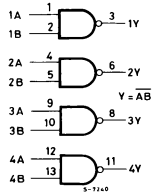
OTHERS	ADDER		HC283
	COMPARATOR		HC85, HC688
	ALU		HC181, HC182
	PARITY TREE		HC280

GATE/BUFFERS

Type Number M54/74	Function	Functional Equivalent LSTTL 54/74	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC00	Quad 2-Input NAND Gate	LS00		4011B	14
HC02	Quad 2-Input NOR Gate	LS02		4001B	14
HC03	Quad 2-Input NAND (Open Drain)	LS03			14
HC04	Hex Inverter	LS04		4069UB	14
HCT04	Hex Inverter	LS04		4069UB	14
HCU04	Hex Inverter (Single Stage)	LS04		4069UB	14
HCT7007	Hex Buffer	LS07			14
HC08	Quad 2-Input AND Gate	LS08		4081B	14
HC10	Triple 3-Input NAND Gate	LS10		4023B	14
HC11	Triple 3-Input AND Gate	LS11		4073B	14
HC14	Hex Schmitt Inverter	LS14		40106B	14
HC20	Dual 4-Input NAND Gate	LS20		4012B	14
HC21	Dual 4-Input AND Gate	LS21		4082B	14
HC27	Triple 3-Input NOR Gate	LS27		4025B	14
HC30	8-Input NAND Gate	LS30		4068B	14
HC32	Quad 2-Input OR Gate	LS32		4071B	14
HC51	Dual 2W-2I AND/OR Invert Gate	LS51		4085B	14
HC86	Quad Exclusive OR Gate	LS86		4030B	14
HC125	Quad Bus Buffer (3-State)	LS125			14
HC126	Quad Bus Buffer (3-State)	LS126			14
HC132	Quad 2-Input Schmitt NAND	LS132		4093B	14
HC133	13 Input NAND Gate	LS133			16
HC240	Octal Bus Buffer (3-State/Inv.)	LS240			20
HCT240	Octal Bus Buffer (3-State/Inv.)	LS240			20
HC241	Octal Bus Buffer (3-State)	LS241			20
HCT241	Octal Bus Buffer (3-State)	LS241			20
HC242	Quad Bus Transceiver (3-State/Inv.)	LS242			14
HC243	Quad Bus Transceiver (3-State)	LS243			14
HC244	Octal Bus Buffer (3-State)	LS244			20
HCT244	Octal Bus Buffer (3-State)	LS244			20
HC245	Octal Bus Transceiver (3-State)	LS245			20
HCT245	Octal Bus Transceiver (3-State)	LS245			20
HC7266	Quad Exclusive NOR Gate	LS266		4077B	14
HC365	Hex Bus Buffer (3-State)	LS365			16
HC366	Hex Bus Buffer (3-State/Inv.)	LS366			16
HC367	Hex Bus Buffer (3-State)	LS367		4503B	16
HC368	Hex Bus Buffer (3-State/Inv.)	LS368			16
HC386	Quad Exclusive OR Gate	LS386		4030B	14
HC540	Octal Bus Buffer (3-State/Inv.)	LS540			20
HCT540	Octal Bus Buffer (3-State/Inv.)	LS540			20
HC541	Octal Bus Buffer (3-State)	LS541			20
HCT541	Octal Bus Buffer (3-State)	LS541			20
HC620	Octal Bus Transceiver (3-State/Inv.)	LS620			20
HC623	Octal Bus Transceiver (3-State)	LS623			20
HC640	Octal Bus Transceiver (3-State/Inv.)	LS640			20
HCT640	Octal Bus Transceiver (3-State/Inv.)	LS640			20
HC643	Octal Bus Transceiver (3-State)	LS643			20
HCT643	Octal Bus Transceiver (3-State)	LS643			20
HC4002	Dual 4-Input NOR Gate		4002B	LS02	14
HC4049B	Hex Buffer/Converter (Inv.)		4049UB		16
HC4050B	Hex Buffer/Converter		4050B		16
HC4072	Dual 4-Input OR Gate		4072B		14
HC4075	Triple 3-Input OR Gate		4075B		14
HC4078	8-Input NOR/OR Gate		4078B		14

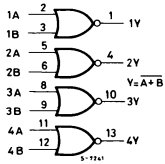
GATE/BUFFERS

HC00



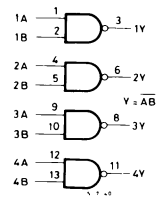
V_{CC} = Pin 14
GND = Pin 7

HC02



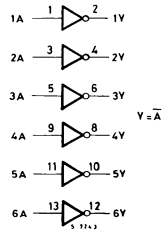
V_{CC} = Pin 14
GND = Pin 7

HC03



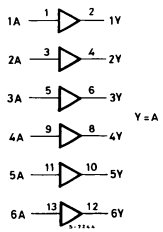
V_{CC} = Pin 14
GND = Pin 7
Open-drain outputs

HC04
HCT04
HCU04 (*)



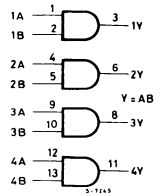
V_{CC} = Pin 14
GND = Pin 7
(*) The internal circuits composed of single stage inverter.

HCT7007



V_{CC} = Pin 14
GND = Pin 7

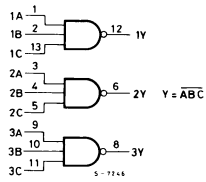
HC08



V_{CC} = Pin 14
GND = Pin 7

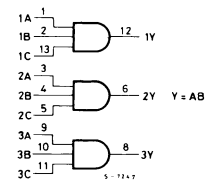
GATE/BUFFERS (Continued)

HC10



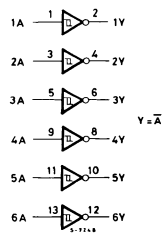
V_{CC} = Pin 14
GND = Pin 7

HC11



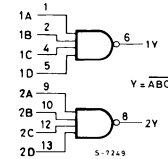
V_{CC} = Pin 14
GND = Pin 7

HC14



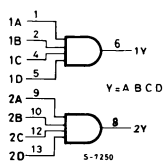
V_{CC} = Pin 14
GND = Pin 7

HC20



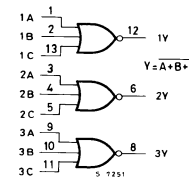
V_{CC} = Pin 14
GND = Pin 7
NC = Pins 3, 11

HC21



V_{CC} = Pin 14
GND = Pin 7
NC = Pins 3, 11

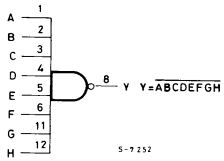
HC27



V_{CC} = Pin 14
GND = Pin 7

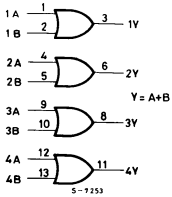
GATE/BUFFERS (Continued)

HC30



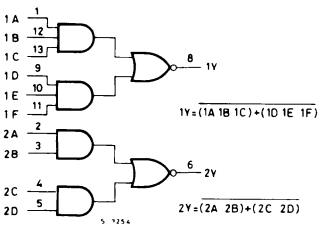
V_{CC} = Pin 14
GND = Pin 7
NC = Pins 9, 10, 13

HC32



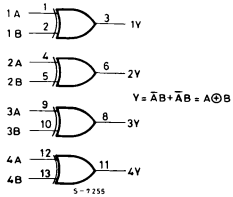
V_{CC} = Pin 14
GND = Pin 7

HC51



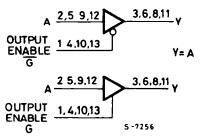
V_{CC} = Pin 14
GND = Pin 7

HC86



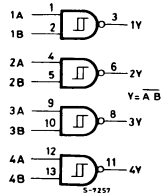
V_{CC} = Pin 14
GND = Pin 7

HC125
HC126



V_{CC} = Pin 14
GND = Pin 7

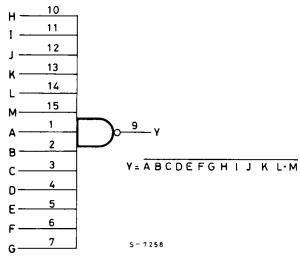
HC132



V_{CC} = Pin 14
GND = Pin 7

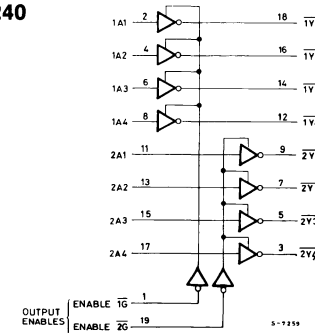
GATE/BUFFERS (Continued)

HC133



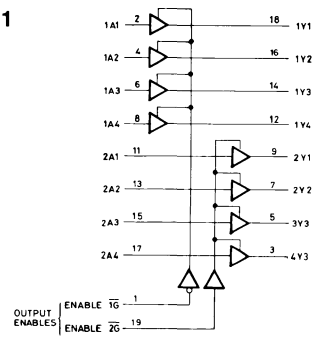
V_{CC} = Pin 16
GND = Pin 8

HC240
HCT240



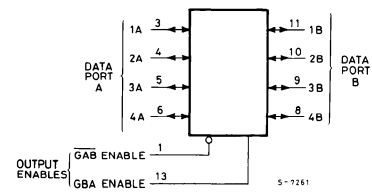
V_{CC} = Pin 20
GND = Pin 10

HC241
HCT241



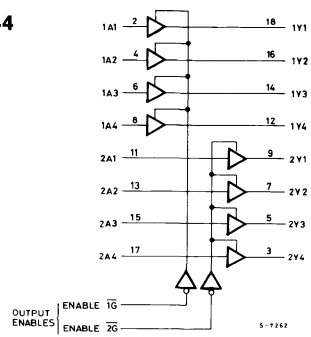
V_{CC} = Pin 20
GND = Pin 10

HC242
HC243



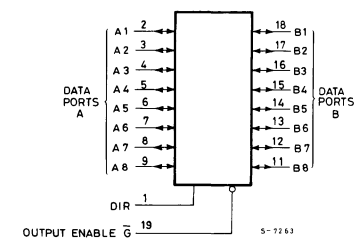
V_{CC} = Pin 14
GND = Pin 7
NC = Pins 2, 12

HC244
HCT244



V_{CC} = Pin 20
GND = Pin 10

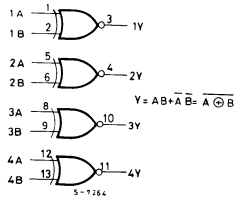
HC245
HCT245



V_{CC} = Pin 20
GND = Pin 10

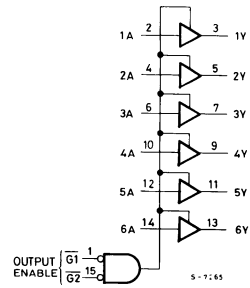
GATE/BUFFERS (Continued)

HC7266



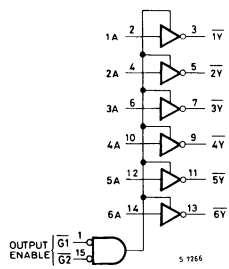
V_{CC} = Pin 14
GND = Pin 7

HC365



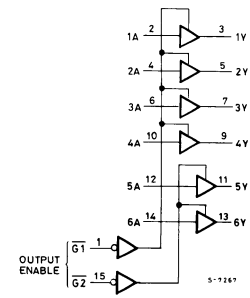
V_{CC} = Pin 16
GND = Pin 8

HC366



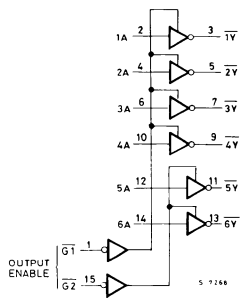
V_{CC} = Pin 16
GND = Pin 8

HC367



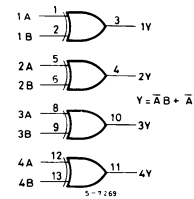
V_{CC} = Pin 16
GND = Pin 8

HC368



V_{CC} = Pin 16
GND = Pin 8

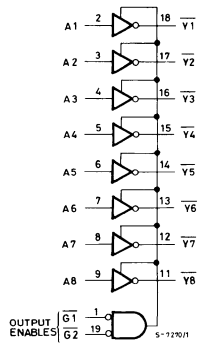
HC386



V_{CC} = Pin 14
GND = Pin 7

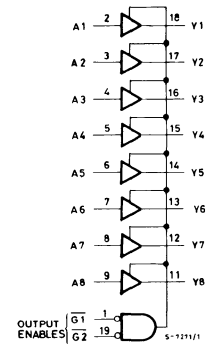
GATE/BUFFERS (Continued)

HC540
HCT540



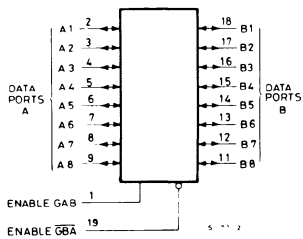
V_{CC} = Pin 20
GND = Pin 10

HC541
HCT541



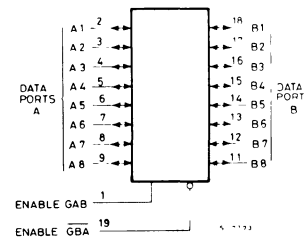
V_{CC} = Pin 20
GND = Pin 10

HC620 (Inverting)



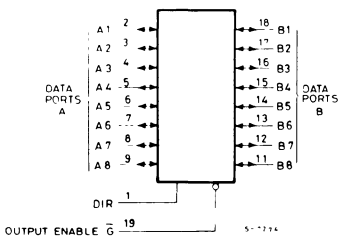
V_{CC} = Pin 20
GND = Pin 10

HC623 (Non Inverting)



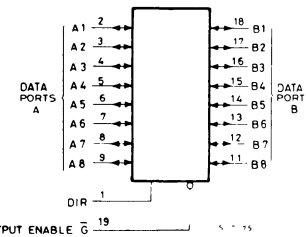
V_{CC} = Pin 20
GND = Pin 10

HC640 (Inverting)
HCT640



V_{CC} = Pin 20
GND = Pin 10

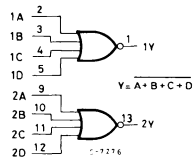
HC643
HCT643



V_{CC} = Pin 20
GND = Pin 10

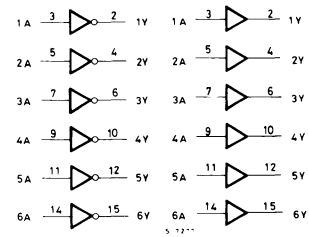
GATE/BUFFERS (Continued)

HC4002



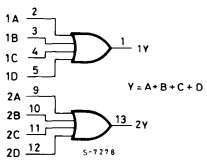
V_{CC} = Pin 14
GND = Pin 7
NC = Pins 6, 8

HC4049B
HC4050B



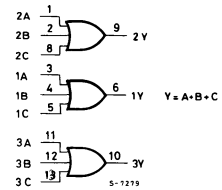
V_{CC} = Pin 1
GND = Pin 8
NC = Pins 13, 16

HC4072



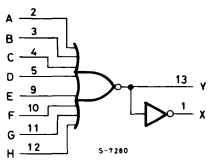
V_{CC} = Pin 14
GND = Pin 7
NC = Pins 6, 8

HC4075



V_{CC} = Pin 14
GND = Pin 7

HC4078

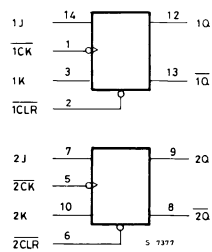


V_{CC} = Pin 14
GND = Pin 7
NC = Pins 6, 8

FLIP-FLOP

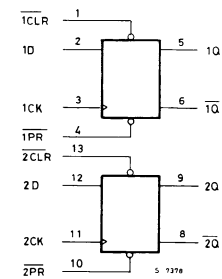
Type Number M54/74	Function	Functional Equivalent LSTTL 54/74	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC73	Dual J-K FLIP-FLOP with Clear	LS73		4027B	14
HC74	Dual D-Type FLIP-FLOP with Preset and Clear	LS74		4013B	14
HC76	Dual J-K FLIP-FLOP with Preset and Clear	LS76		4027B	16
HC107	Dual J-$\overline{K}$ FLIP-FLOP with Clear	LS107		4027B	14
HC109	Dual J-$\overline{K}$ FLIP-FLOP with Preset and Clear	LS109		4027B	16
HC112	Dual J-K FLIP-FLOP with Preset and Clear	LS112		4027B	16
HC113	Dual J-K FLIP-FLOP with Preset	LS113		4027B	14
HC174	Hex D-Type FLIP-FLOP with Clear	LS174		40174B	16
HC175	Quad D-Type FLIP-FLOP with Clear	LS175		40175B	16
HC273	OCTAL D-Type FLIP-FLOP with Clear	LS273			20
HC374	Octal D-Type FLIP-FLOP (3-State)	LS374			20
HCT374	Octal D-Type FLIP-FLOP (3-State)	LS374			20
HC377	Octal D-Type FLIP-FLOP	LS377			20
HC534	Octal D-Type FLIP-FLOP (3-State/Inv.)	LS534			20
HC564	Octal D-Type FLIP-FLOP (Inv./3-State)	LS564			20
HCT564	Octal D-Type FLIP-FLOP (3-State/Inv.)	LS564			20
HC574	Octal D-Type FLIP-FLOP (3-State)	LS574			20
HCT574	Octal D-F/F (3-State)	LS574			20
HC646	Octal Bus Transceiver Register (3-State)	LS646			24
HCT646	Octal Bus Transceiver Register (3-State)	LS646			24
HC648	Octal Bus Transceiver Register (3-State/Inv.)	LS648			24
HCT648	Octal Bus Transceiver Register (3-State/Inv.)	LS648			24
HC651	Octal Bus Transceiver Register (3-State/Inv.)	LS651			24
HCT651	Octal Bus Transceiver Register (3-State/Inv.)	LS651			24
HC652	Octal Bus Transceiver Register	LS652			24
HCT652	Octal Bus Transceiver Register	LS652			24

HC73



V_{CC} = Pin 4
GND = Pin 11

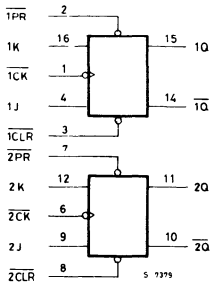
HC74



V_{CC} = Pin 14
GND = Pin 7

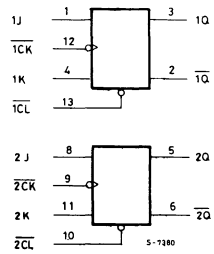
FLIP/FLOP (Continued)

HC76



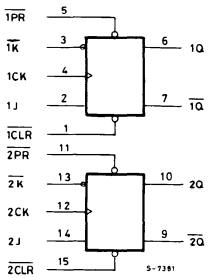
V_{CC} = Pin 5
GND = Pin 13

HC107



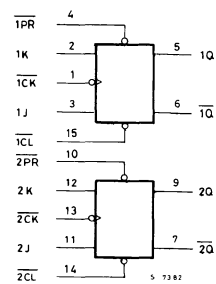
V_{CC} = Pin 14
GND = Pin 7

HC109



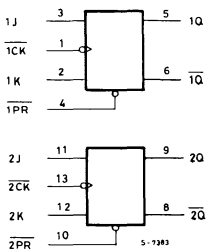
V_{CC} = Pin 16
GND = Pin 8

HC112



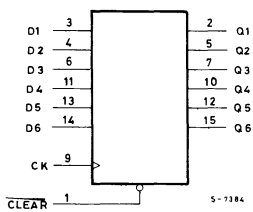
V_{CC} = Pin 16
GND = Pin 8

HC113



V_{CC} = Pin 14
GND = Pin 7

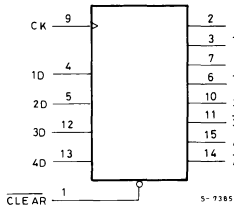
HC174



V_{CC} = Pin 16
GND = Pin 8

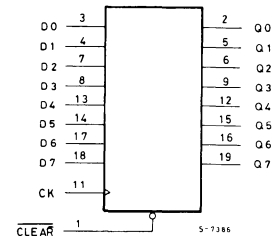
FLIP/FLOP (Continued)

HC175



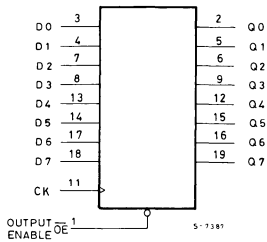
V_{CC} = Pin 16
GND = Pin 8

HC273



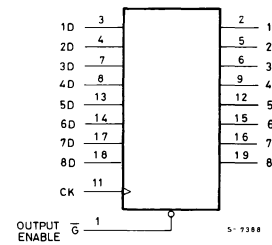
V_{CC} = Pin 20
GND = Pin 10

HC374
HCT374



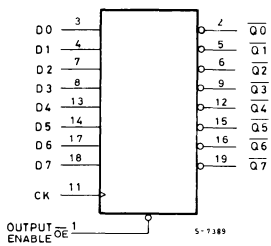
V_{CC} = Pin 20
GND = Pin 10

HC377



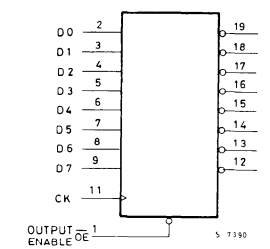
V_{CC} = Pin 20
GND = Pin 10

HC534



V_{CC} = Pin 20
GND = Pin 10

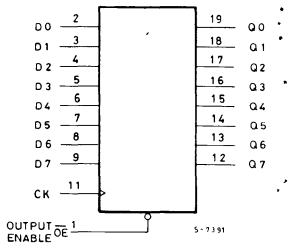
HC564
HCT564



V_{CC} = Pin 20
GND = Pin 10

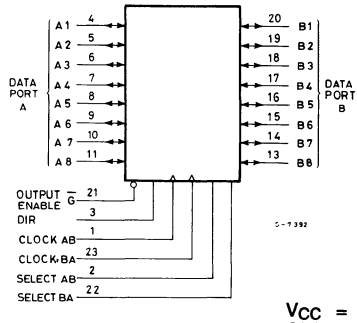
FLIP/FLOP (Continued)

HC574
HCT574



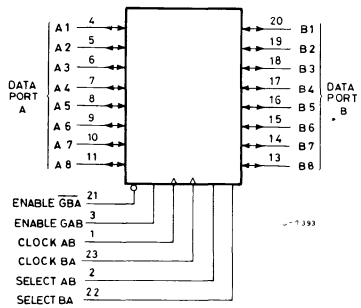
V_{CC} = Pin 20
GND = Pin 10

HC646/HCT646
HC648/HCT648



V_{CC} = Pin 24
GND = Pin 12

HC651/HCT651
HC652/HCT652

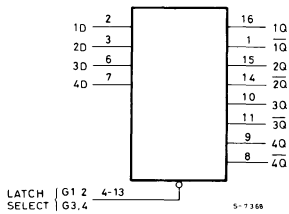


V_{CC} = Pin 24
GND = Pin 12

LATCHES

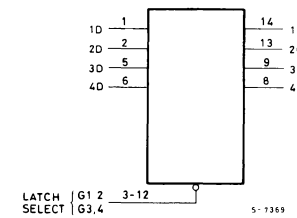
Type Number M54/74	Function	Functional Equivalent LSTTL 54/74	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC75	4-Bit D-Type Latch	LS75		4042B	16
HC77	4-Bit D-Type Latch	LS77		4042B	14
HC259	8 Bit Addressable Latch	LS259		4099B	16
HC279	Quad $\overline{R}$-$\overline{S}$ Latch	LS279			16
HC373	Octal D-Type Latch (3-State)	LS373			20
HCT373	Octal D-Type Latch (3-State)	LS373			20
HC375	Quad D-Type Latch	LS375		4042B	16
HC533	Octal D-Type Latch (3-State/Inv.)	LS533			20
HC563	Octal D-Type Latch (3-State/Inv.)	LS563			20
HCT563	Octal D-Type Latch (3-State/Inv.)	LS563			20
HC573	Octal D-Type Latch (3-State)	LS573			20
HCT573	Octal D-Type Latch (3-State)	LS573			20

HC75



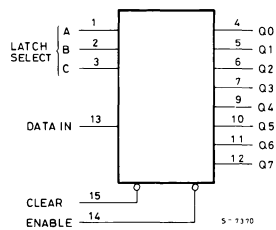
V_{CC} = Pin 5
GND = Pin 12

HC77



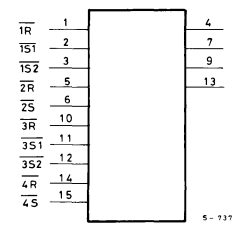
V_{CC} = Pin 4
GND = Pin 11
NC = Pins 7, 10

HC259



V_{CC} = Pin 16
GND = Pin 8

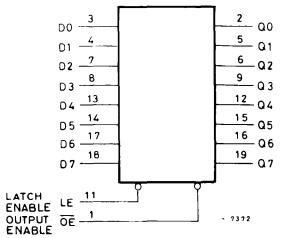
HC279



V_{CC} = Pin 16
GND = Pin 8

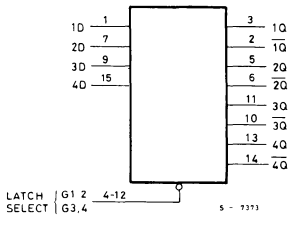
LATCHES (Continued)

HC373
HCT373



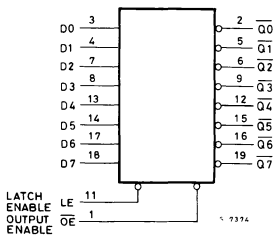
V_{CC} = Pin 20
GND = Pin 7

HC375



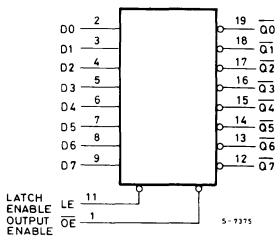
V_{CC} = Pin 16
GND = Pin 8

HC533



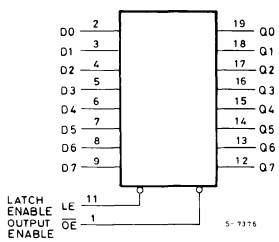
V_{CC} = Pin 20
GND = Pin 10

HC563
HCT563



V_{CC} = Pin 20
GND = Pin 10

HC573
HCT573

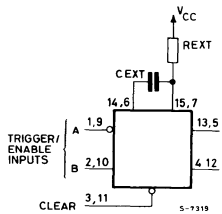


V_{CC} = Pin 20
GND = Pin 10

MULTIVIBRATOR

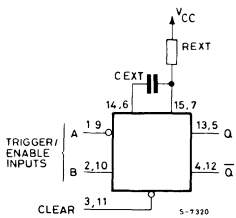
Type Number M54/74	Function	Functional Equivalent LSTTL 54/74	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC123	Dual Retrigg. Monostable Multivib. with Clear	LS123		4538/4098	16
HC221	Dual Monostable Multivib. with Clear	LS221		4538/4098	16
HC423	Dual Retrigg. Monostable Multivib. with Clear	LS423		4538/4098	16
HC4538	Dual Retrigg. Monostable Multivibrator		4538B	LS423	16

HC123



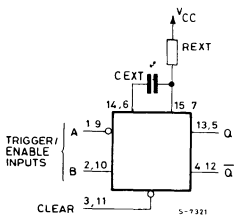
VCC = Pin 16
GND = Pin 8

HC221



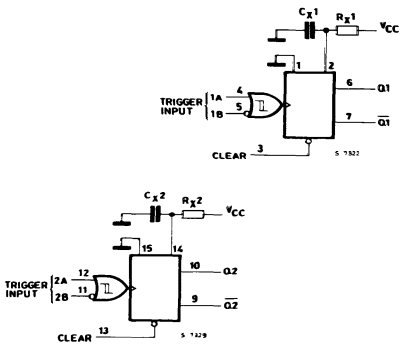
VCC = Pin 16
GND = Pin 8

HC423



VCC = Pin 16
GND = Pin 8

HC4538

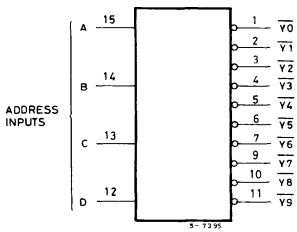


VCC = Pin 16
GND = Pin 8

DECODER/ENCODER

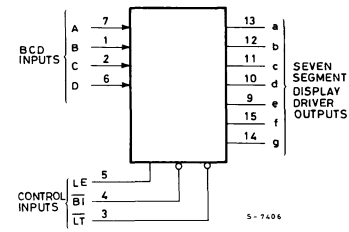
Type Number M54/74	Function	Functional Equivalent LSTTL 54/74	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC42	BCD to Decimal Decoder	LS42		4028B	16
HC131	3 to 8 Line Decoder Latch	LS131			16
HC137	3 to 8 Line Decoder Latch (Inv.)	LS137		4028B	16
HCT137	3 to 8 Line Decoder Latch (Inv.)	LS137		4028B	16
HC138	3 to 8 Line Decoder (Inv.)	LS138		4028B	16
HCT138	3 to 8 Line Decoder (Inv.)	LS138		4028B	16
HC139	Dual 2 to 4 Line Decoder/Demultiplexer	LS139		4556B	16
HC147	10 to 4 Line Priority Encoder	LS147			16
HC148	8 to 3 Line Priority Encoder	LS148			16
HC154	4 to 16 Line Decoder/Demultiplexer	LS154		4515B	24
HC155	Dual 2 to 4 Line Decoder / 3 to 8 Line Dec.	LS155			16
HC237	3 to 8 Line Decoder Latch			4028B	16
HC238	3 to 8 Line Decoder			4028B	16
HC4028	BDC to Decimal Decoder		4028B	LS42	16
HC4511	BDC to 7-Segment L/D/D (Led)		4511B	LS47/48/49	16
HC4514	4 to 16 Line Decoder Latch		4514B	—	24
HC4515	4 to 16 Line Decoder Latch (Inv.)		4515B	LS154	24
HC4543	BCD to 7-Segment L/D/D (LCD)		4543B	LS143	16

HC42



V_{CC} = Pin 16
GND = Pin 8

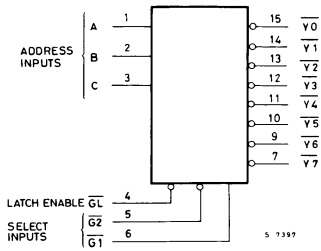
HC131



V_{CC} = Pin 16
GND = Pin 8

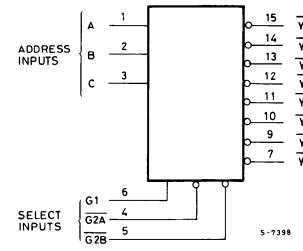
DECODER/ENCODER (Continued)

HC137
HCT137



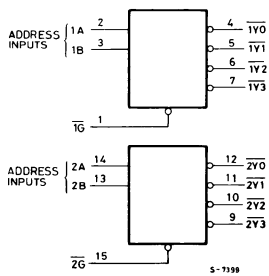
V_{CC} = Pin 16
GND = Pin 8

HC138
HCT138



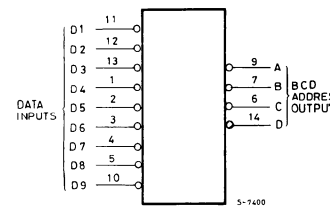
V_{CC} = Pin 16
GND = Pin 8

HC139



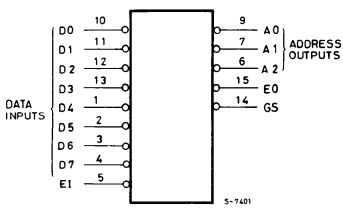
V_{CC} = Pin 16
GND = Pin 8

HC147



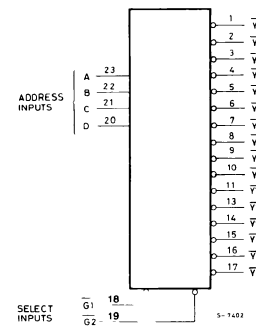
V_{CC} = Pin 16
GND = Pin 8

HC148



V_{CC} = Pin 16
GND = Pin 8

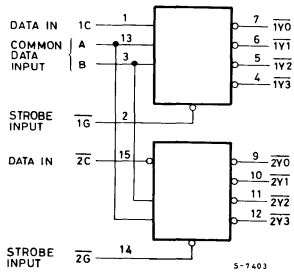
HC154



V_{CC} = Pin 24
GND = Pin 12

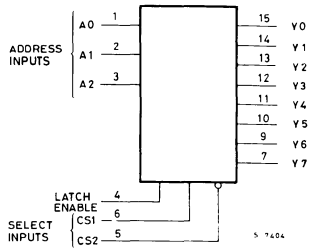
DECODER/ENCODER (Continued)

HC155



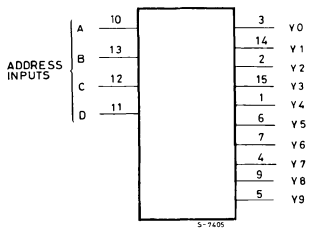
V_{CC} = Pin 16
GND = Pin 8

HC237



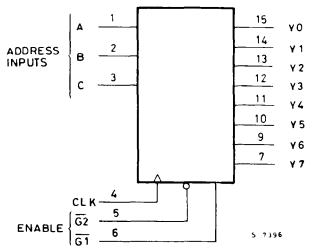
V_{CC} = Pin 16
GND = Pin 8

HC4028



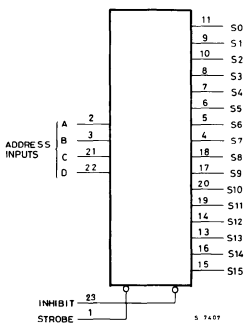
V_{CC} = Pin 16
GND = Pin 8

HC4511



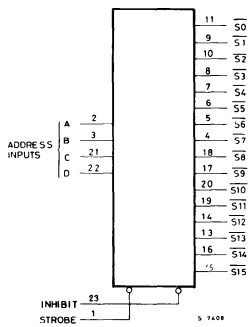
V_{CC} = Pin 16
GND = Pin 8

HC4514



V_{CC} = Pin 24
GND = Pin 12

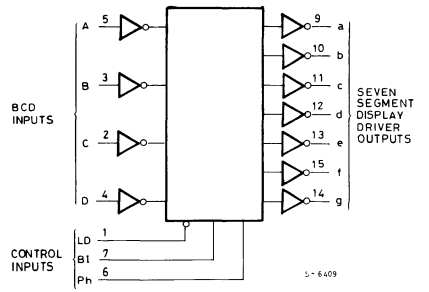
HC4515



V_{CC} = Pin 24
GND = Pin 12

DECODER/ENCODER (Continued)

HC4543

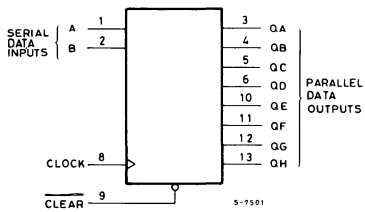


V_{CC} = Pin 16
GND = Pin 8

REGISTER

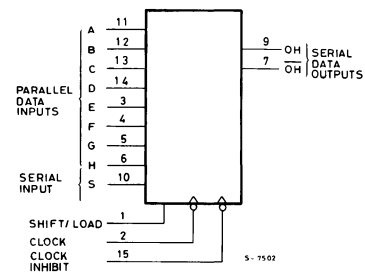
Type Number M54/74	Function	Functional Equivalent LSTTL 54/74	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC164	8 Bit SIPO Shift Register	LS164		4034B	14
HC165	8 Bit PISO Shift Register	LS165		4021B	16
HC166	8 Bit PISO Shift Register	LS166		4021B	16
HC173	Quad D-Type Register (3-State)	LS173			16
HC194	4 Bit PIPO Shift Register	LS194		40194B	16
HC195	4 Bit PIPO Shift Register	LS195		4035B	16
HC299	8 Bit PIPO Shift Register (3-State)	LS299			20
HC323	8 Bit PIPO Shift Register (3-State)	LS323			20
HC595	8 Bit Shift Register Latch (3-State)	LS595		4034B	16
HC597	8 Bit Latch Shift Register	LS597			16
HC670	4 Word x 4 Bit Register File (3-State)	LS670			16
HC4094	8 Bit SIPO Shift Register Latch (3-State)		4094B	LS164	16

HC164



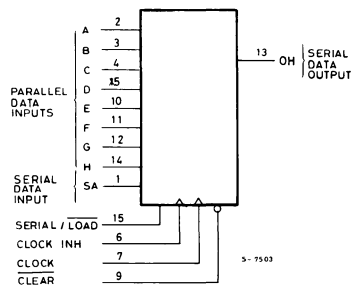
V_{CC} = Pin 14
GND = Pin 7

HC165



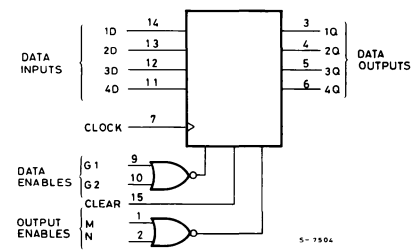
V_{CC} = Pin 16
GND = Pin 8

HC166



V_{CC} = Pin 16
GND = Pin 8

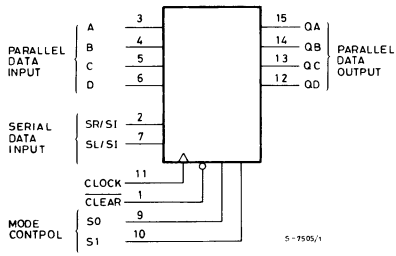
HC173



V_{CC} = Pin 16
GND = Pin 8

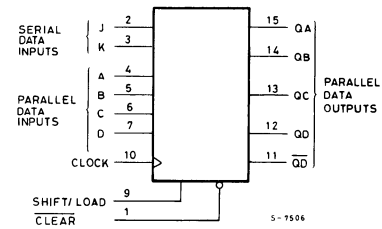
REGISTER (Continued)

HC194



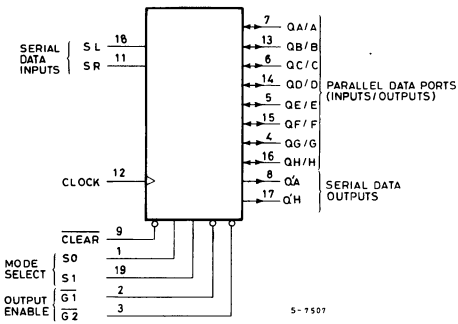
V_{CC} = Pin 16
GND = Pin 8

HC195



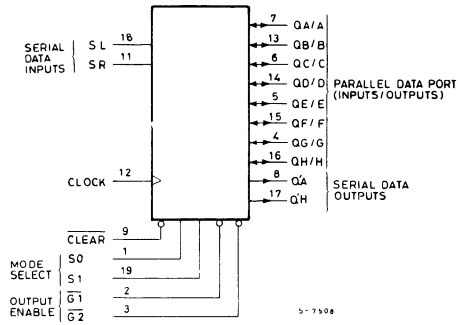
V_{CC} = Pin 16
GND = Pin 8

HC299



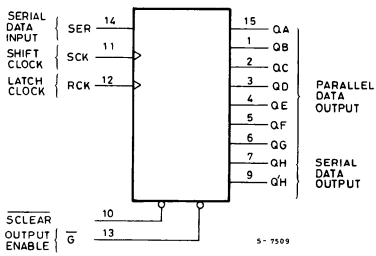
V_{CC} = Pin 20
GND = Pin 10

HC323



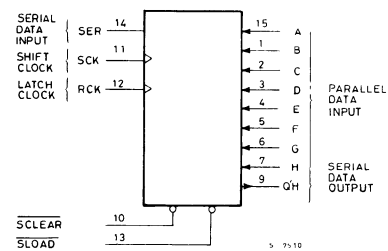
V_{CC} = Pin 20
GND = Pin 10

HC595



V_{CC} = Pin 16
GND = Pin 8

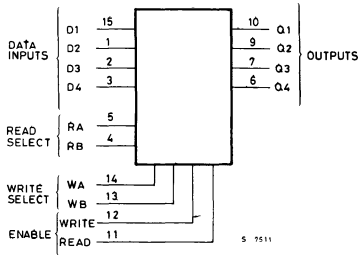
HC597



V_{CC} = Pin 16
GND = Pin 8

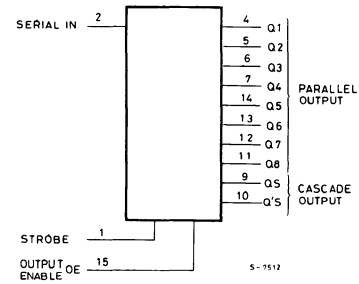
REGISTER (Continued)

HC670



V_{CC} = Pin 16
GND = Pin 8

HC4094

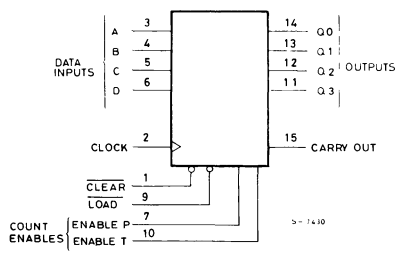


V_{CC} = Pin 16
GND = Pin 8

COUNTERS

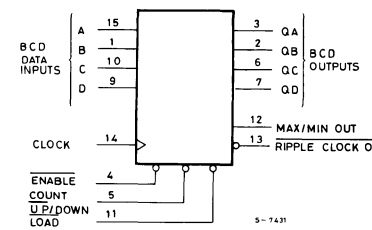
Type Number M54/74	Function	Functional Equivalent LSTTL 54/74	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC160	Sync. Decade Counter with Async. Clear	LS160		40160B	16
HC161	Sync. Binary Counter with Async. Clear	LS161		40161B	16
HC162	Sync. Decade Counter with Sync. Clear	LS162		40162B	16
HC163	Sync. Binary Counter with Sync. Clear	LS163		40163B	16
HC190	BCD Up/Down Counter Sync.	LS190		4510B	16
HC191	4 Bit Binary Up/Down Counter Sync.	LS191		4516B	16
HC192	Sync. Up/Down Decade Counter	LS192		40192B	16
HC193	Sync. Up/Down Binary Counter	LS193		40193B	16
HC292	Programmable Divider/Timer	LS292			16
HC294	Programmable Divider/Timer	LS294			16
HC7292	Programmable Divider/Timer				16
HC7294	Programamble Divider/Timer				16
HC390	Dual Decade Counter	LS390		4518B	16
HC393	Dual Binary Counter	LS393		4520B	14
HC590	8 Bit Binary Counter Register (3-State)	LS590			16
HC690	Decade Counter Register (3-State)	LS690			20
HC691	4 Bit Binary Counter Register (3-State)	LS691			20
HC692	Decade Counter Register (3-State)	LS692			20
HC693	4 Bit Binary Counter Register (3-State)	LS693			20
HC696	U/D Decade Counter Register (3-State)	LS696			20
HC697	U/D 4-Bit Binary Counter/Register (3-State)	LS697			20
HC698	U/D Decade Counter Register (3-State)	LS698			20
HC699	U/D 4-Bit Binary Counter/Register (3-State)	LS699			20
HC4017	Decade Counter/Divider		4017B		16
HC4020	14-Stage Binary Counter		4020B		16
HC4022	Octal Counter/Divider		4022B		16
HC4024	7-Stage Binary Counter		4024B		14
HC4040	12-Stage Binary Counter		4040B		16
HC4060	14-Stage Binary Counter/Oscillator		4060B		16
HC40102	Dual BCD Programmable Down Counter		40102B		16
HC40103	8 Bit Binary Prog. Down Counter		40103B		16
HC4518	Dual Decade Counter		4518B		16
HC4520	Dual 4 Bit Binary Counter		4520B		16

HC160/HC162
HC161/HC163



V_{CC} = Pin 16
GND = Pin 8

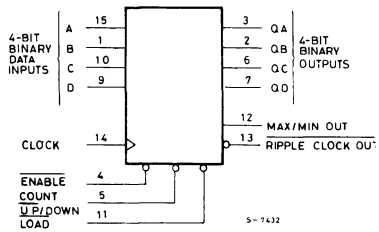
HC190



V_{CC} = Pin 16
GND = Pin 8

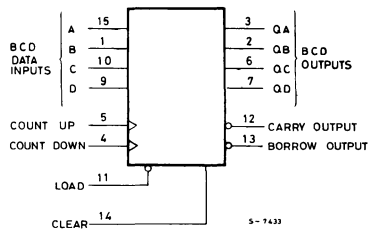
COUNTERS (Continued)

HC191



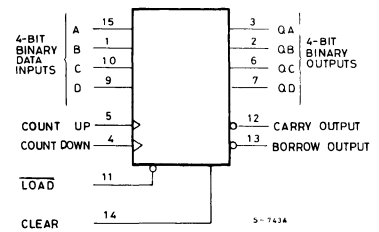
V_{CC} = Pin 16
GND = Pin 8

HC192



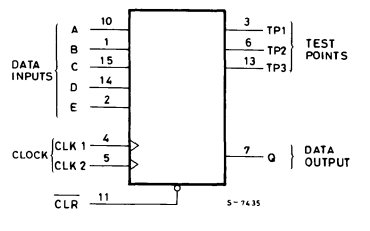
V_{CC} = Pin 16
GND = Pin 8

HC193



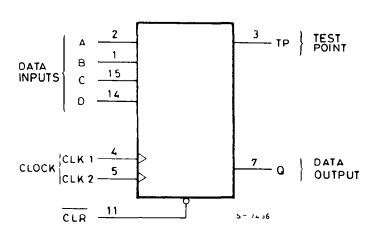
V_{CC} = Pin 16
GND = Pin 8

HC292/HC7292



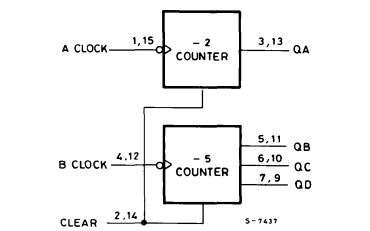
V_{CC} = Pin 16
GND = Pin 8
NC = Pins 9, 12

HC294/HC7294



V_{CC} = Pin 16
GND = Pin 8
NC = Pins 6, 9, 10, 12, 13

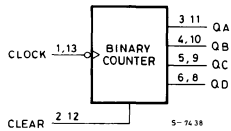
HC390



V_{CC} = Pin 16
GND = Pin 8

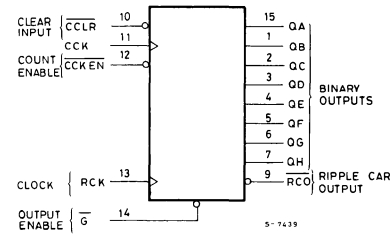
COUNTERS (Continued)

HC393



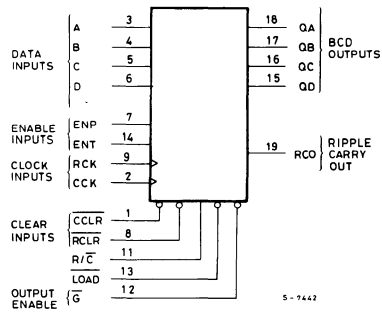
V_{CC} = Pin 14
GND = Pin 7

HC590



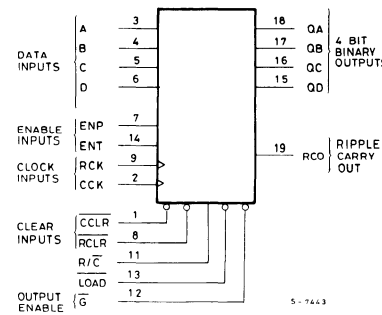
V_{CC} = Pin 16
GND = Pin 8

HC690



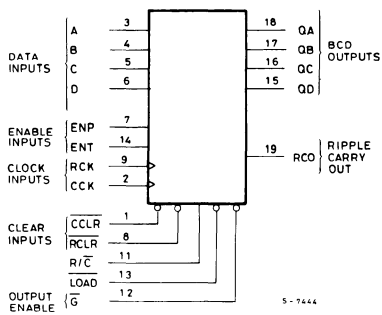
V_{CC} = Pin 20
GND = Pin 10

HC691



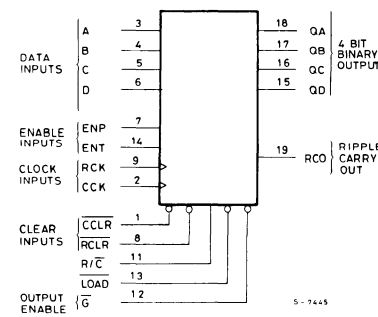
V_{CC} = Pin 20
GND = Pin 10

HC692



V_{CC} = Pin 20
GND = Pin 10

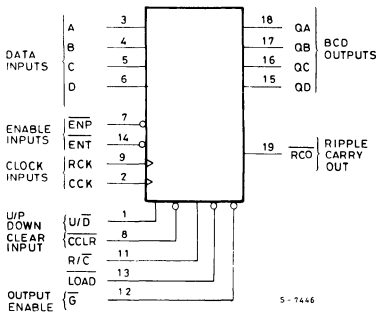
HC693



V_{CC} = Pin 20
GND = Pin 10

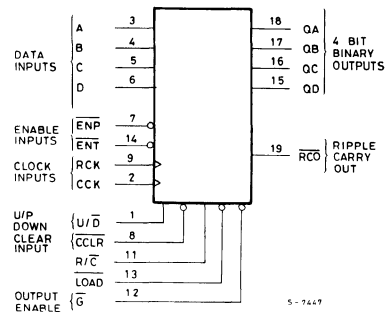
COUNTERS (Continued)

HC696



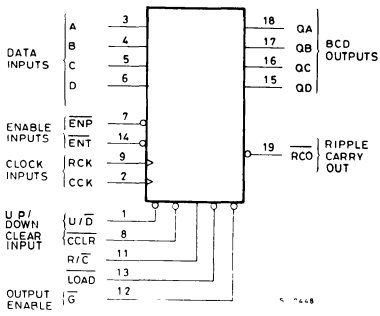
V_{CC} = Pin 20
GND = Pin 10

HC697



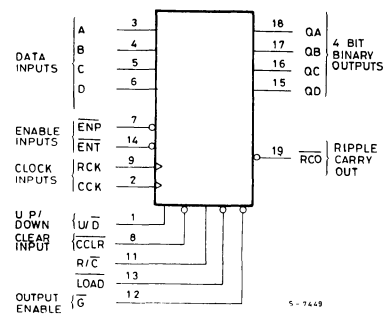
V_{CC} = Pin 20
GND = Pin 10

HC698



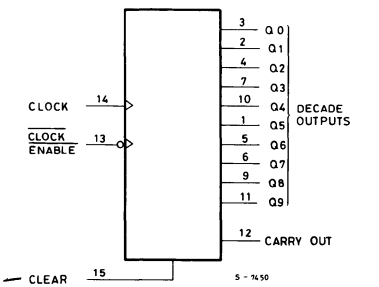
V_{CC} = Pin 20
GND = Pin 10

HC699



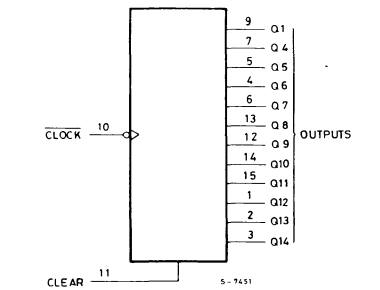
V_{CC} = Pin 20
GND = Pin 10

HC4017



V_{CC} = Pin 16
GND = Pin 8

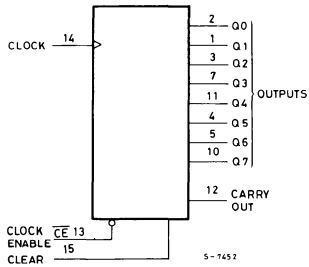
HC4020



V_{CC} = Pin 16
GND = Pin 8

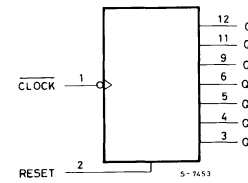
COUNTERS (Continued)

HC4022



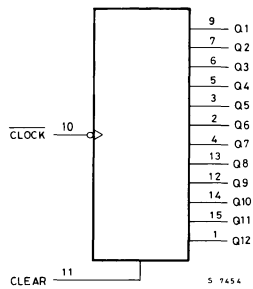
V_{CC} = Pin 16
GND = Pin 8
NC = Pins 6, 9

HC4024



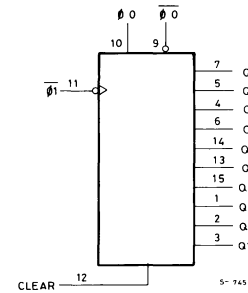
V_{CC} = Pin 14
GND = Pin 7
NC = Pins 8, 10, 13

HC4040



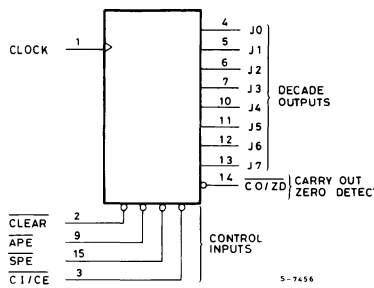
V_{CC} = Pin 16
GND = Pin 8

HC4060



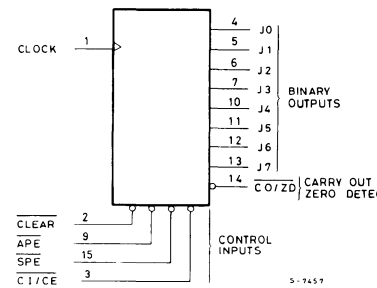
V_{CC} = Pin 16
GND = Pin 8

HC40102



V_{CC} = Pin 16
GND = Pin 8

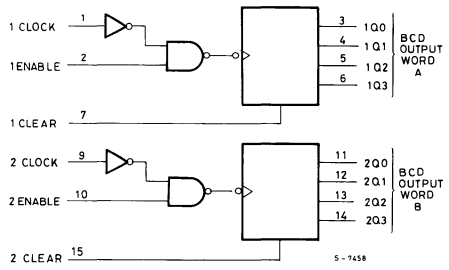
HC40103



V_{CC} = Pin 16
GND = Pin 8

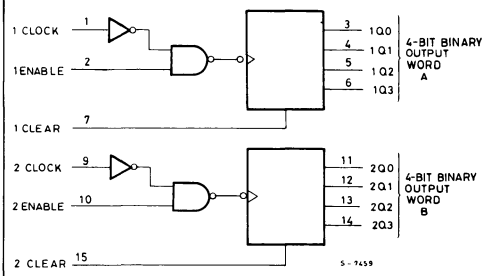
COUNTERS (Continued)

HC4518



V_{CC} = Pin 16
GND = Pin 8

HC4520

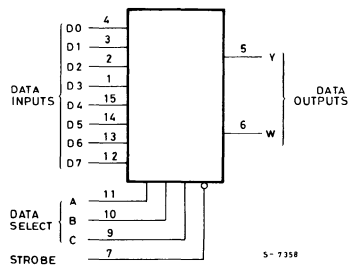


V_{CC} = Pin 16
GND = Pin 8

MULTIPLEXER

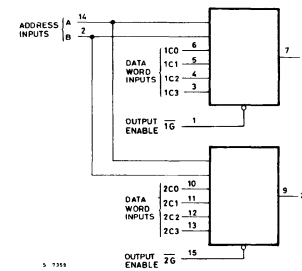
Type Number M54/74	Function	Functional Equivalent LSTTL 54/74	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC151	8-Channel Multiplexer	LS151		4512B	16
HC153	Dual 4-Channel Multiplexer	LS153			16
HC157	Quad 2-Channel Multiplexer	LS157			16
HC158	Quad 2-Channel Multiplexer (Inv.)	LS158			16
HC251	8-Channel Multiplexer (3-State)	LS251		4512B	16
HC253	Dual 4-Channel Multiplexer (3-State)	LS253			16
HC257	Quad 2-Channel Multiplexer (3-State)	LS257			16
HC258	Quad 2-Channel Multiplexer (3-State/Inv.)	LS258			16
HC298	Quad 2-Channel Multiplexer Register	LS298			16
HC354	8-Channel Multiplexer/Register (3-State)	LS354		4512B	20
HC356	8-Channel Multiplexer/Register (3-State)	LS356		4512B	20
HC4066	Quad Bilateral Switch		4066B		14

HC151



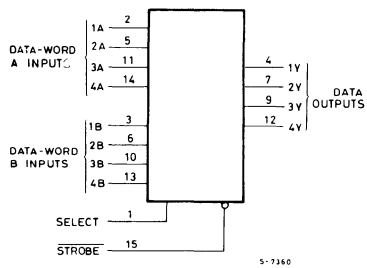
V_{CC} = Pin 16
GND = Pin 8

HC153



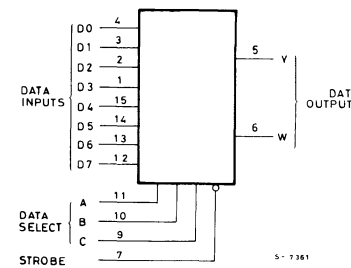
V_{CC} = Pin 16
GND = Pin 8

HC157
HC158



V_{CC} = Pin 16
GND = Pin 8

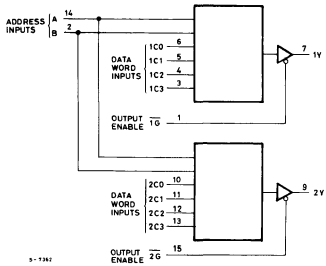
HC251



V_{CC} = Pin 16
GND = Pin 8

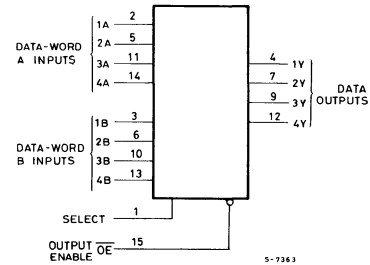
MULTIPLEXER (Continued)

HC253



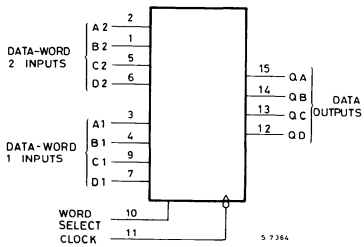
V_{CC} = Pin 16
GND = Pin 8

HC257 (Non Inverting Outputs)
HC258 (Inverting Outputs)



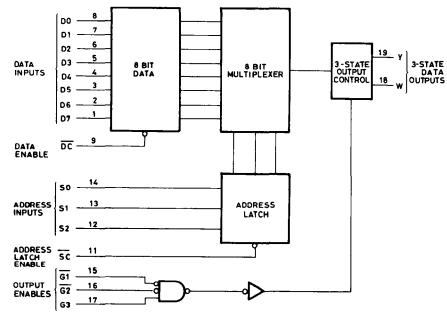
V_{CC} = Pin 16
GND = Pin 8

HC298



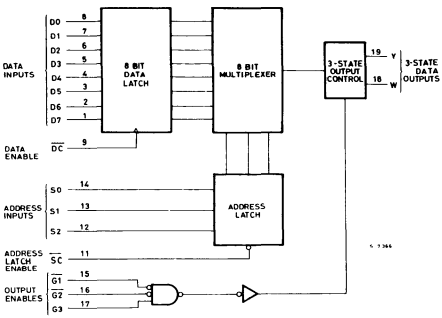
V_{CC} = Pin 16
GND = Pin 8

HC354



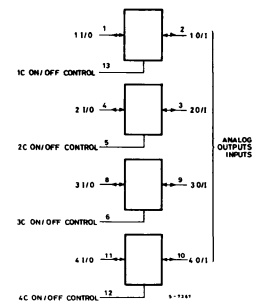
V_{CC} = Pin 20
GND = Pin 10

HC356



V_{CC} = Pin 20
GND = Pin 10

HC4066

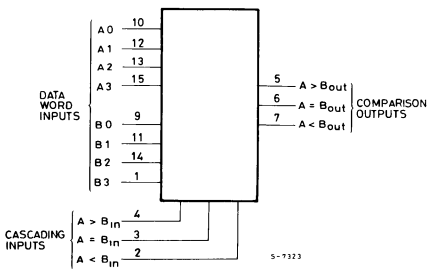


V_{CC} = Pin 14
GND = Pin 7
1I/O: 2I/O: 3I/O: 4I/O = Analog Inputs/Outputs

COMPARATORS

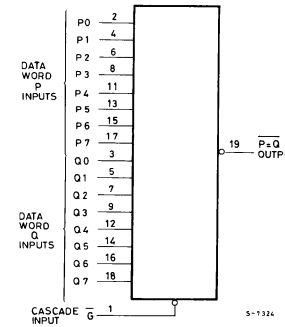
Type Number M54/74	Function	Functional Equivalent LSTTL 54/74	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC85	4-Bit Magnitude Comparator	LS85		4063B/4585B	16
HC688	8-Bit Equality Comparator	LS688			20

HC85



V_{CC} = Pin 16
GND = Pin 8

HC688

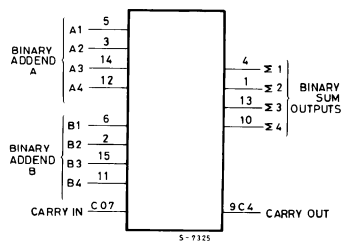


V_{CC} = Pin 20
GND = Pin 10

ADDER

Type Number M54/74	Function	Functional Equivalent LSTTL 54/74	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC283	4-Bit Binary Full-Adder	LS283		4008	16

HC283

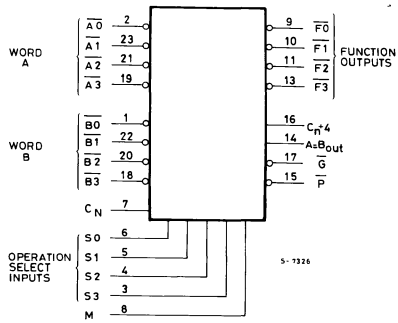


V_{CC} = Pin 16
GND = Pin 8

ALU

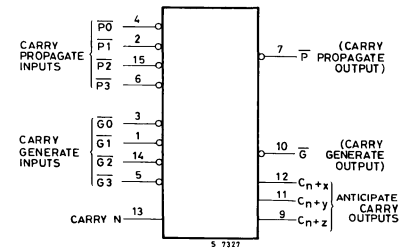
Type Number M54/74	Function	Functional Equivalent LSTTL 54/74	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC181	Arithmetic Logic Unit	LS181		40181B	24
HC182	Look Ahead Carry Generator	LS182		40182B	16

HC181



V_{CC} = Pin 24
GND = Pin 12

HC182

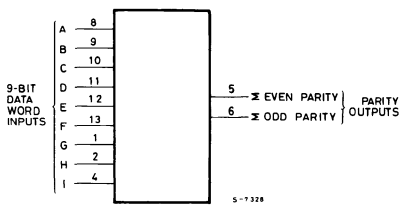


V_{CC} = Pin 16
GND = Pin 8

PARITY TREE

Type Number M54/74	Function	Functional Equivalent LSTTL 54/74	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC280	9-Bit Parity Generator / Checker	LS280		4001B	14

HC280



V_{CC} = Pin 14
GND = Pin 7
NC = Pin 3

GENERAL AND APPLICATION INFORMATION

INTRODUCING HS-C² MOS

The rapid advances recently made in silicon-gate CMOS technology have lead to the introduction of a logic family that sets new and much higher standards of performance.
This family called HS-C²MOS* , exhibits a greatly improved speed/product performance when compared with other existing logic families and allows greater flexibility in both system design and configuration.
The HS-C²MOS family is pin compatible with industry standard LSTTL and many of the CMOS 4000B types. It does, however, have considerable advantages over both LSTTL and earlier generation CMOS in terms of power consumption, speed, noise immunity and supply voltage range.
This new family of high performance devices is being jointly developed and manufactured by ST and Toshiba who between them have many years of production and marketing expertise in the field of CMOS logic. The synergism of two major manufacturers will ensure the rapid introduction of the family into the market place and will guarantee its continuity, and continuing development.
HS-C²MOS will offer to the user a cost-effective and high performance solution to an ever increasing number of applications and open up the way to truly light weight field portable instruments and advanced systems.

High Speed

The HS-C²MOS logic family has been designed to match or better the dynamic characteristics of LSTTL thus giving a high performance family which can be used wherever high speed as well as low power consumption is important. (See Fig. 3)
Propagation delays for the new family are around ten times lower than those for metal-gate CMOS devices and in the order of five times lower than earlier silicon-gate devices.

Fig. 2 - Propagation Delay Time vs. Load Capacitance

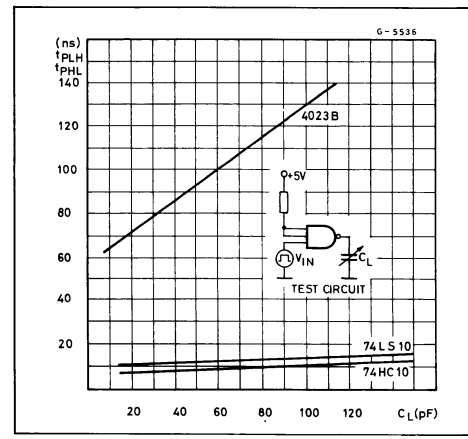


Fig. 1 - Operating Frequency

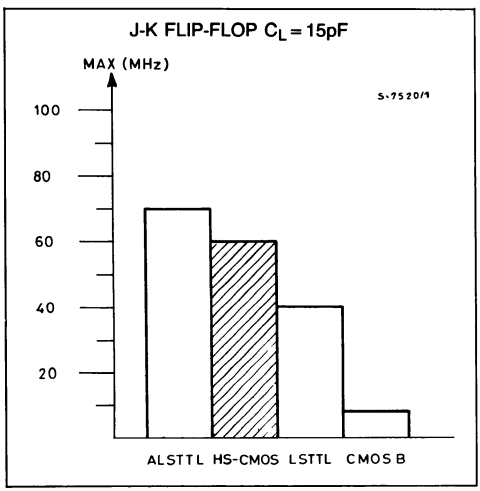
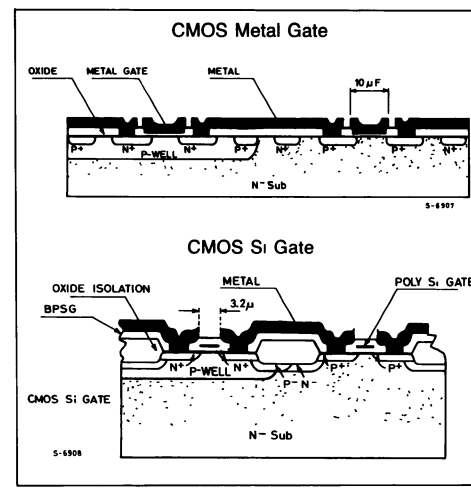


Fig. 3



Low Power

For every reduction in system power there comes a corresponding reduction in system costs. Smaller, lighter power supplies can be used, heatsinks can be eliminated or drastically reduced in size, forced air cooling can often be dispensed with and more devices can be included on a single board. All this translates into better utilization of printed circuit board real-estate and a bottom line that reads "lower costs".
CMOS has an enormous and well established advantage over LSTTL in terms of power consumption. Typical quiescent dissipation per gate for CMOS is in the order of 10 nW whilst for LSTTL a typical value is up around the 8 mW mark. At a system level too the HS-C²MOS family offers a power reduction of more than 100 times when compared with LSTTL.

Fig. 4 - Current Dissipation vs. Operating Frequency

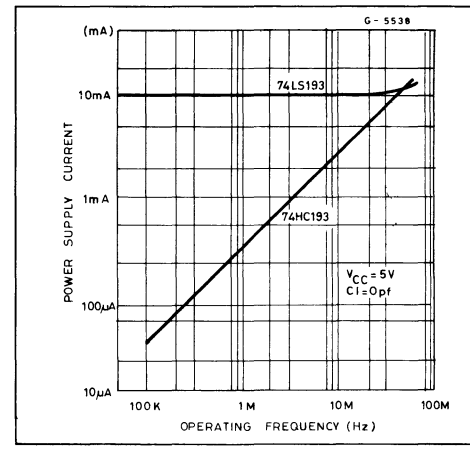
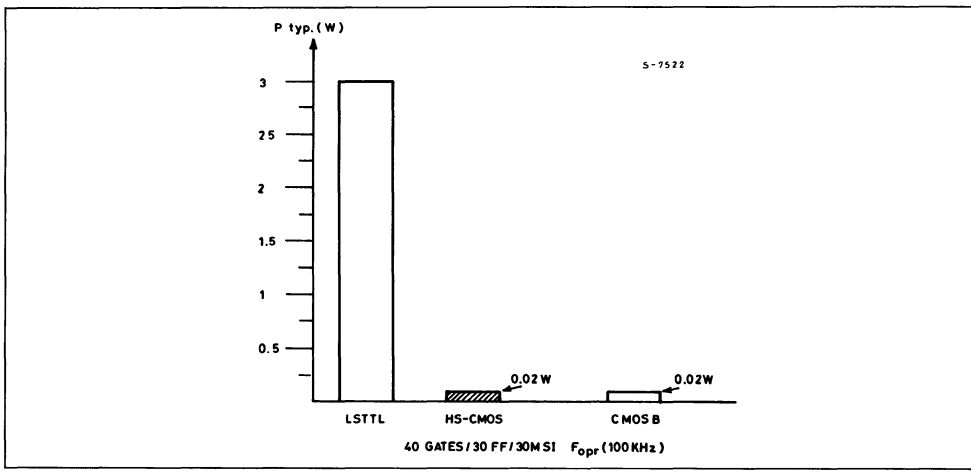


Fig. 5 - Sistem Power Dissipation



Wide Fanout

The output driving capabilities of LSTTL have been matched by the HS-C²MOS family. Each device is able to sink or source up to 4 mA, in other words they can drive up to 10 LSTTL loads. Buffers and bus drivers have increased performance and can in fact drive up to 15 LSTTL loads. This has been achieved while maintaining the low input current, which is characteristic of CMOS, and without sacrificing either speed or noise immunity. Furthermore the design of the HS-C²MOS devices has resulted in equal rise and fall times which results in easier design and allows optimum speed and AC performance to be obtained.

FANOUT FROM HS-C²MOS TO CMOSB, LSTTL, TTL, STLL, ASLTTL

FROM \ TO	54/74HC	CMOSB	LSTTL	TTL	STLL	ALSTTL
54/74HC Standard	4000	4000	10	2	2	20
54/74HC Bus driver	>4000	>4000	15	4	3	30

Fig. 6 - Output Driver Capability

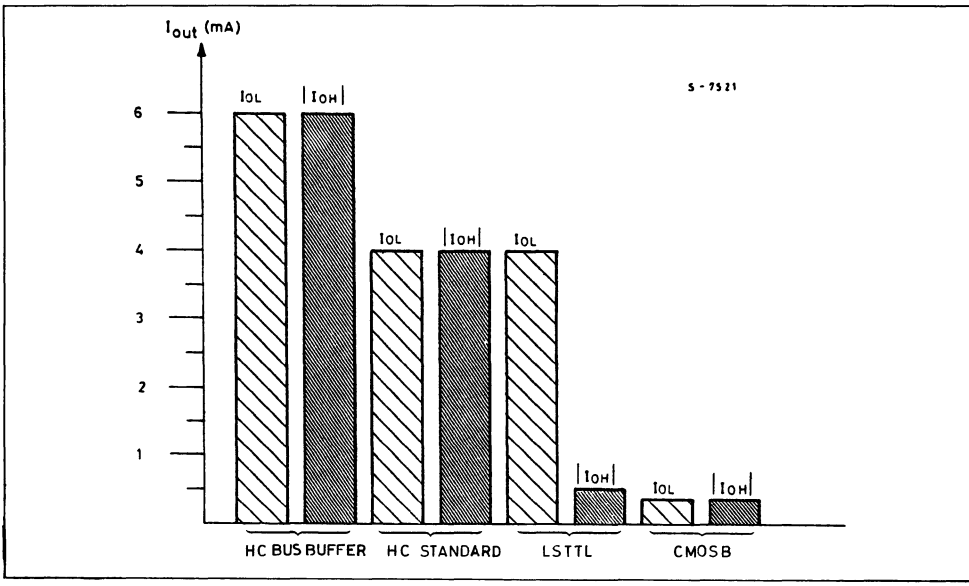
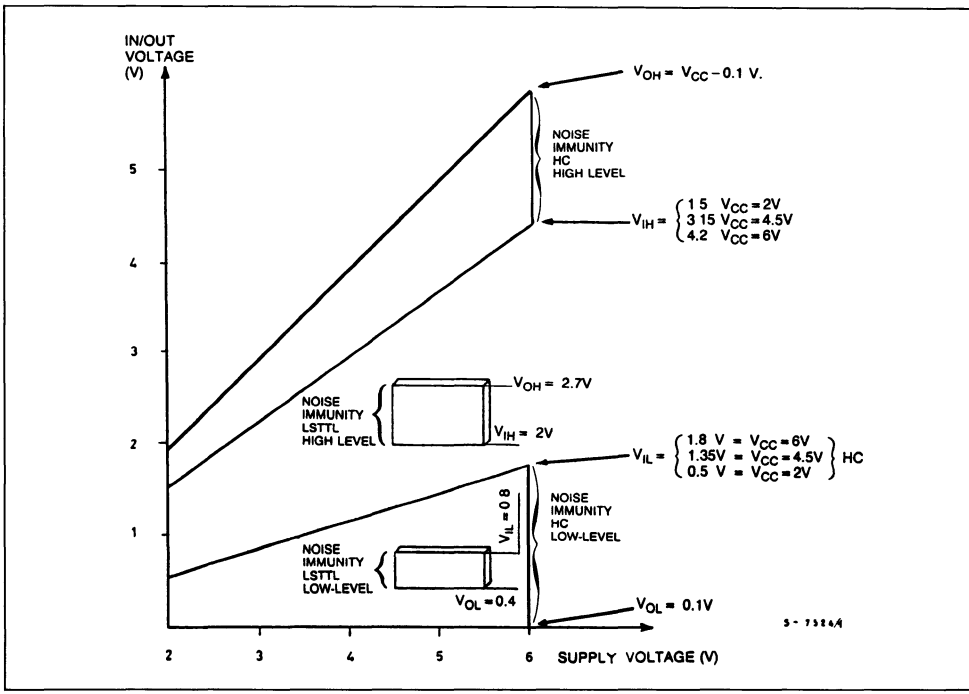


Fig. 7 - High Noise Immunity



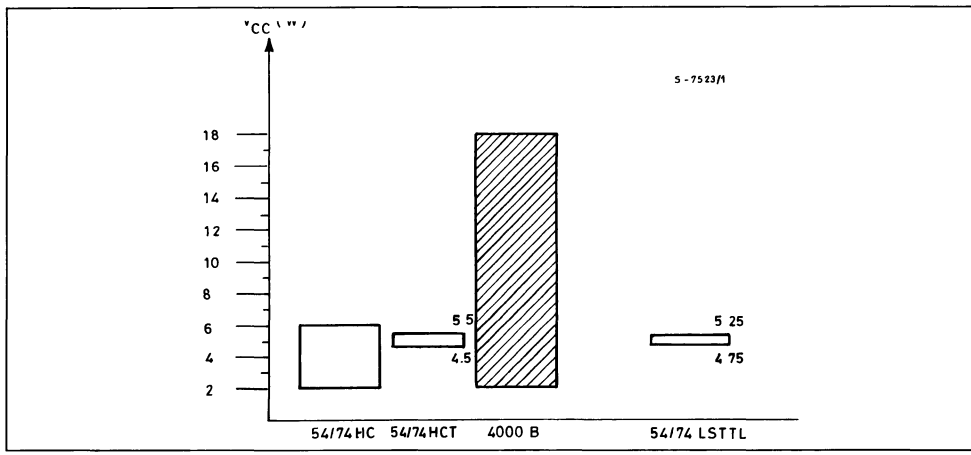
High Noise Immunity

In many applications high immunity to noise is of particular importance. This is why CMOS, with its characteristic high noise immunity, is already to be found in many computer peripherals, industrial circuits, telecommunications applications, and numerous other applications in high noise level environments. The LOW level and HIGH level noise immunity of the HS-C²MOS family is better than 28% in both cases. This is notably better than for LSTTL where the margins are only 8% of V_{CC} at LOW level and 14% of V_{CC} at HIGH level. These figures assume a V_{CC} of 5 V, at higher voltages the superiority of HS-C²MOS becomes even more apparent.

Wide Operating Voltage Range

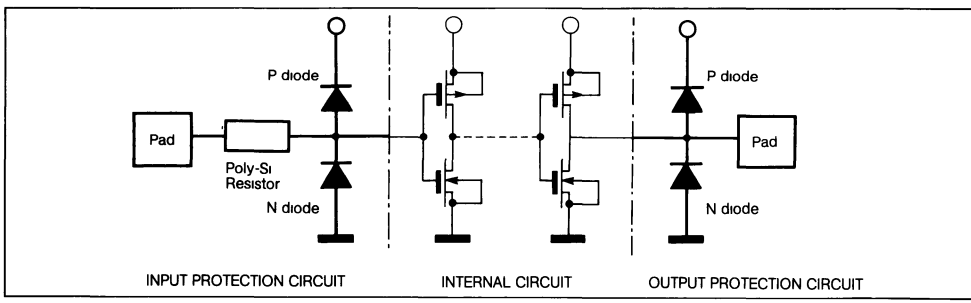
The HS-C²MOS family devices are all capable of working with supply voltages ranging from 2 V up to 6 V. This is an important factor when viewed in the light of future developments, where the trend is towards memories and microprocessors which will work with supply voltages lower than 5 V. With the HS-C²MOS family it is possible to use less precise, and therefore cheaper, power supplies or even low voltage batteries. This, coupled with the exceptionally low power consumption, common to the entire family, opens up the way for a whole new generation of light weight, high performance systems and instruments.

Fig. 8 - Supply Voltage Range



Input Output Protection

The HS-C²MOS, in addition to improved performance and power consumption, also features improved input protection. This has been achieved by employing poly-silicon as a resistor structure at all inputs. The resistor slows down the fast input transients generated by electrostatic discharge and dissipates some of the associated energy. Although these input resistors, in conjunction with the input diode, give improved levels of protection, it is still advisable to follow the usual CMOS handling precautions.



MAIN FEATURES OF THE HS-C² MOS SERIES

High Speed Operation	LSTTL speed f_{max} = 60 MHz typical
Low Power Dissipation	Micro Watt Dissipation. Quiescent Current I_{CC} = 1 μA SSI / 2 μA F/F / 4 μA MSI, T_A = 25°C
High Output Current	Fanout of 10 LSTTL Loads (15 for buffers)
Symmetrical Output Buffer	Equal $\|I_{OH}\|$ and I_{OL}
High Noise Immunity	$V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
Wide Operating Voltage Range (HC)	HC V_{CC} = 2 to 6 V HCT V_{CC} = 4.5 to 5.5V
Pin and Function Compatible with Equivalent LSTTL and Some Popular Types of HCC/HCF 4000 series.	
Wide Range of Products.	
Second Source Available.	

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25 (±35 buffer)	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50 (±70 buffer)	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≤ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (HC)	2 to 6	V
V_{CC}	Supply Voltage (HCT)	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V: 0 to 1000 V_{CC} 4.5V: 0 to 500 V_{CC} 6 V: 0 to 400	ns

COMPARISON OF LOGIC FAMILIES

Parameter	Test Conditions	HS-C² MOS	LSTTL	CMOS B
Propagation Delay Time Gate (C_L = 15 pF)	V_{CC} = 5 V	8 ns (typ)	10 ns (typ)	125 ns (typ)
Maximum Clock Frequency J/KF – F (C_L = 15 pF)	T_A = 25°C	60 MHz (typ)	45 MHz (typ)	7 MHz (typ)
Quiescent Power Dissipation (Gate)	Over all temperature and voltage range	0.01 μW (typ)	8 mW (typ)	0.01 μW (typ)
V_{IH} / V_{IL} Noise Margin	V_{CC} = 5 V Over all temp. range	3.5 V (min) 1.5 V (max)	2 V (min) 0.8 V (max)	3.5 V (min) 1.5 V (max)
$\|I_{OH}\|$ / I_{OL} Output Current (Std.)	Over all temperature and voltage range	4 mA (min) 4 mA (min)	0.4 mA (min) 4 mA (min)	0.36 mA (min) 0.36 mA (min)
Operating Voltage Range		HC 4.5 to 5.5V HCT 2 to 6V	4.75 to 5.25 V	3 to 18 V
Operating Temperature Range	74HC/LS HCF 4000B 54HC/LS HCC 4000B	–40 to 85°C –50 to 125°C	0 to 70°C –55 to 125°C	–40 to 85°C –55 to 125°C

THE HS-C²MOS PROCESS

1. The Si-Gate Process

The M74HCXXX/54HCXXX family achieves its high speed operation, by means of an advance high performance Si-Gate process.
The advantages of Si-Gate versus metal gate CMOS are already well known and described. Here is a brief summary.

- The process uses self aligned source and drain diffusions which have the advantage of reducing gate to source and gate to drain overlap capacitance. This, in turn, reduces the Miller capacitance during the switching of the basic inverter which leads to an increase in speed.
- Better reliability: it has been proved that use of a silicon electrode as a gate of a MOS transistor gives better threshold voltage stability and therefore a more reliable basic structure under voltage stress.
- Recessed oxide isolation allows a thicker field oxide and therefore lower unit capacitance between interconnection and the grounded substrate. A decrease in the parasitic capacitance is therefore obtained and speed performance is improved.

2. The Scaling Theory

Despite its advantages, the use of a Si-Gate process instead of metal gate of equal dimensions is not sufficient to achieve speed performance comparable with LPS logic families.
Therfore a high performance Si-Gate process has been developed based on the "Scaling theory".
The scaling theory of the physical dimensions of the transistor was developed originally by IBM (Dennard ed al.) in 1974.
Scaling is the step which has contributed most to the outstanding improvement in perfomance obtained by the MOS technologies in the last decade.
This theory predicts that if the physical dimensions of a MOS transistor and the power supply voltage values are decreased by a constant factor K, and all the substrate doping levels are increased by the same factor, the DC characteristics of the transistor remain unchanged.
The advantages of such an approach are quite straight forward
- the chip size is reduced by a factor K^2
- the delay times are reduced by a factor K^2

The Scaling theory is easy to explain, but it is much more difficult to obtain in a production enviroment because the progressive reduction of the physical dimensions put severe constaints on the type of equipment and on the spreads allowed in production control.

The recent improvement obtained by equipment manufactures in the field of photolithography and dry etching has been used extensively by ST to obtain a stable, reproducible production process, which is used in the production of all the devices in this new family.

3. The HS-C²MOS Process

The following is a simplified description of the HS-C²MOS process.
After initial oxidation of the starting material, which is N-type, windows are defined in the photoresist material and the initial oxide is removed (fig. 1).
An implantation step is then performed (fig. 2) and after photoresist removal a diffusion step is carried out to define the P-well areas (fig. 3).

Fig. 1 - Starting N-type with Windows in Oxide

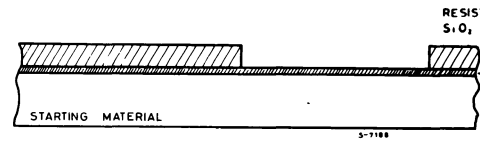


Fig. 2 - P-Well Boron Implantation

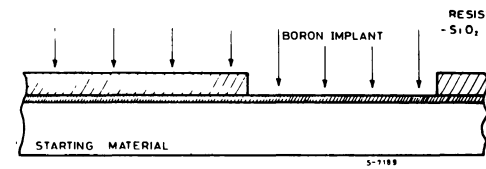


Fig. 3 - P-Well Boron Redistribution

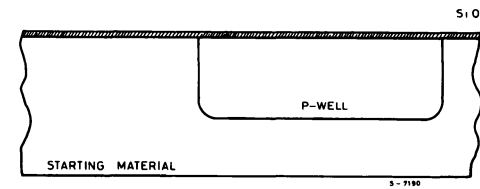


Fig. 4 - Si_3N_4 Deposition

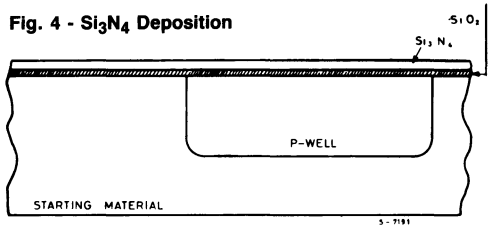


Fig. 5 - Definition of Transistor Area

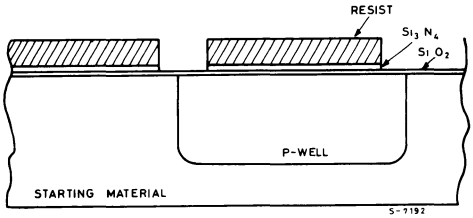
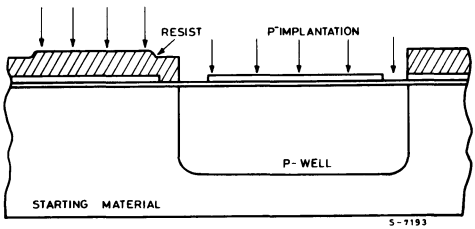


Fig. 6 - P Implantation (Boron)



A-Silicon nitride layer is deposited on all the surface of the wafer (fig. 4) and by a masking step all the active areas (source, drain, gate) of both P-channel and N-channel transistors are defined (fig. 5).
The field threshold values are controlled by successive implantation steps both on the P-well surface (fig. 6) and substrate area (fig. 7).
After these steps the field oxide is grown (fig. 8). During the recessed oxidation step the diffusion of previous implanted dopants is effected.
After Gate oxidation, threshold voltage control of both the P-channel and the N-channel transistor is carried out using two successive masking steps. During these operations surface concentration of the gate areas is obtained to optimize the threshold voltage values against input noise and propagation delay time.
A crystalline silicon layer is deposited on all the surface of the wafer and then masked and etched to define the gates of all the transistors. (fig. 9).
Source and drain predeposition and diffusion of the N-channel transistors is the next step (fig. 10). The source and drain of the P-channel transistors are made, with an additional implantation step (fig. 11).

Contacts are defined and etched (fig. 12), an interconnection layer (metallization) is defined to interconnect all the active elements in the integrated circuits (fig. 13a, b).

Fig. 7 - N Implantation Phospherais

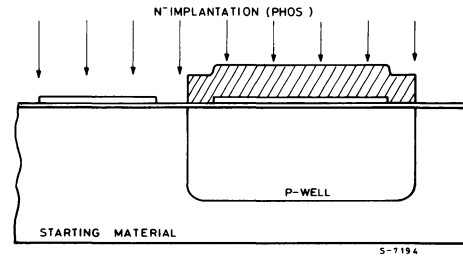


Fig. 8 - Field Oxidation

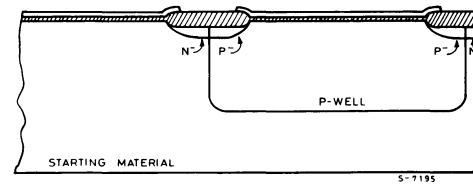


Fig. 9 - Si Poly Gate Definition

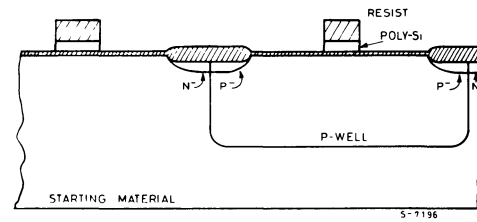


Fig. 10 - N^+ Predeposition and Diffusion

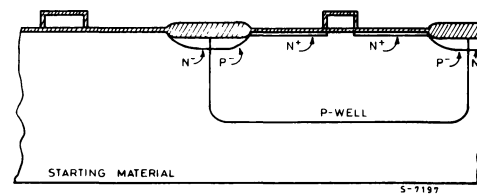


Fig. 11 - P^+ Predeposition and Diffusion

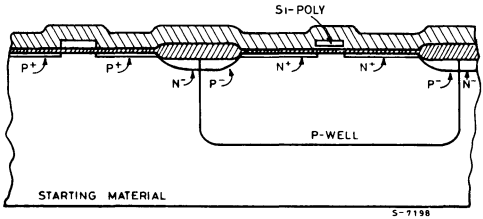


Fig. 12 - Al-Si Deposition $t_{Al\text{-}Si} = 7000$ Å

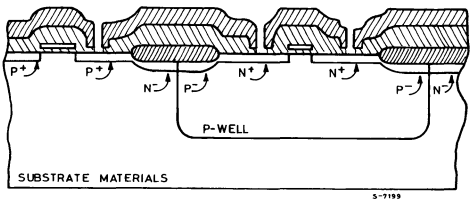


Fig. 13a - Metal Interconnection

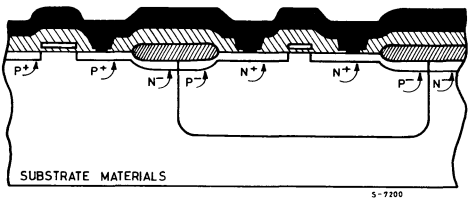
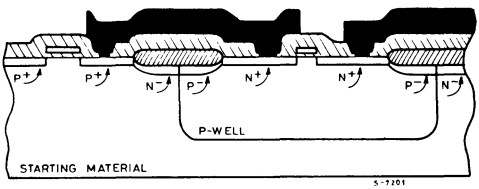


Fig. 13b - Metal Interconnection Definition



Double Layer Glass Passivation

SGS-THOMSON HSCMOS family uses a double layer P-VAPOX and Si_3N_4 passivation that gives improved protection to die encapsulated in plastic packages.

Process Description

The process consists of a two layer film of P-Vapox (phosphorus doped silicon oxide) and Si_3N_4 (silicon nitride), obtained by two different masking and etching steps to avoid defects caused by lack of dielectric integrity.
The process gives good metal step coverage together with PECVD (Plasma Enhanced Chemical Vapox Deposition) to avoid cracking near metal edge and possible hillocks defects.
The double layer enables us, by means of an appropriate oversize, either at the boundaries of the die side or at the bonding pad side, to ensure full sealing of the underlying P-Vapox layer.
This prevents the layer from being exposed to moisture coming from the package. Thus the probability of metal corrosion on the bonding pad due to phosphoric acid is drastically reduced.
As a result the die is provided with a very good humidity immunity.

PROCESS FLOW

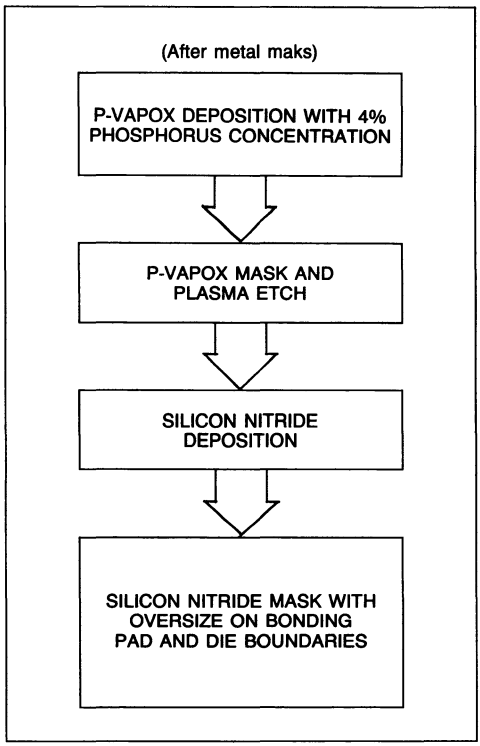


Fig. 14a - Typical Microsection of an HSCMOS Device with Nitride Passivation

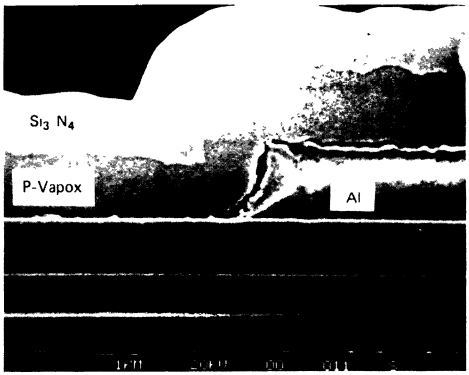


Fig. 14b - Section Along the Scribing line of an HSCMOS Device.

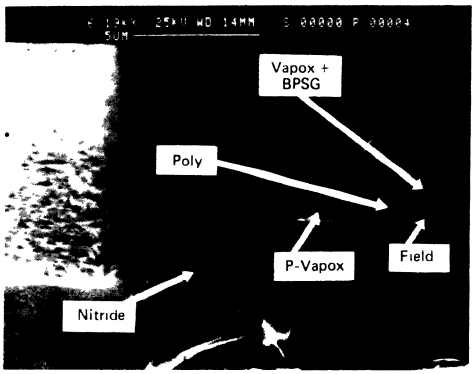
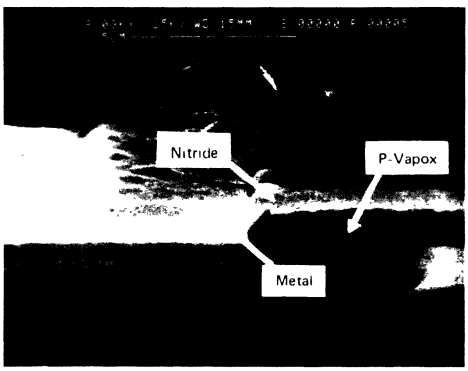


Fig. 14c - Section Along the Pad of an HSCMOS Device.

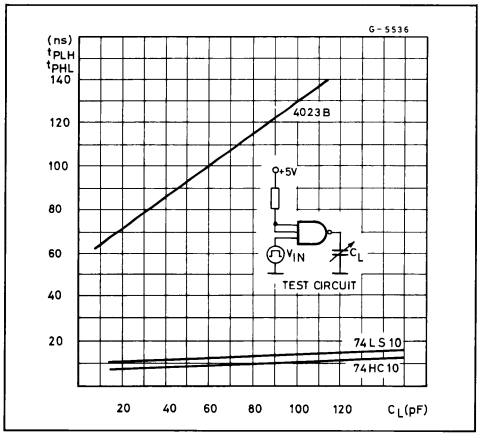


4. Summary

The scaling of the physical transistors combined with the Si-Gate process allows an outstanding improvement in the performace of the active elements and a drastic reduction of the parasitic capacitances.

Circuit performance at HSC²MOS is comparable with LPS devices as shown in the following graph (fig. 15).

Fig. 15 - Propagation delay vs. load Capacitance for 3-Input NAND Gate



INTERFACING TO HS-C²MOS LOGIC

In many applications it will be necessary to interface HC series logic devices with types from other logic families. Two main cases can easily be identified according to whether the supply voltage of the devices to be interfaced is different or not. Where separate supplies are involved a logic level translator may be required. In most other cases only a very simple circuit, if any at all, will be required.

M54/74HC Driven by TTL

When interfacing TTL with HC devices using a common power supply of 4.5 to 5.5V, the guaranteed output-high voltage from TTL is only 2.4V. This is of course lower than the minimum input-high voltage for M54/74HC devices (see fig. 1).
Overcoming this problem is simply a matter of using an external pull-up resistor, Rp, which is the same as the resistor used for open collector output TTL. (See fig. 2).
Table 1 shows maximum and minimum values of Rp for various TTL families. When LSTTL is the driving logic, the value of Rp can be found using the graph shown in fig. 3.
Obviously the output-low level (0.8V) falls well within HC acceptable limits.
With HC devices supplied at more than 3V, the TTL minimum high voltage of 2.4V is enough to guarantee the logic 1 input.

TABLE 1

Rp min	74	74L	Unit
Rp min	390	1.5K	Ω
Rp max	4.7K	27K	Ω

M54/74HCT Driven by TTL

These devices, while retaining the intrinsic advantages of HS-C²MOS technology, allow direct interfacing with TTL devices.

Fig. 2

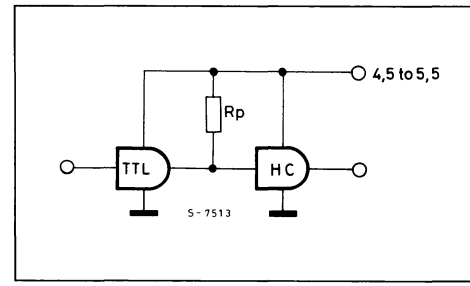


Fig. 3

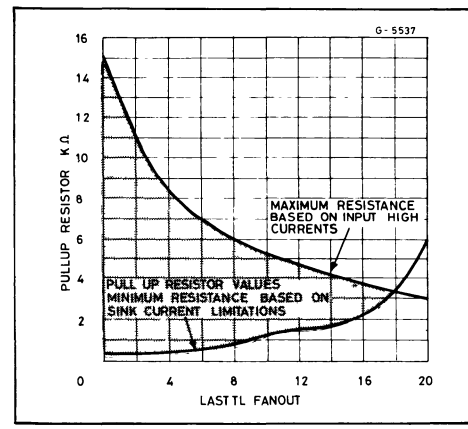
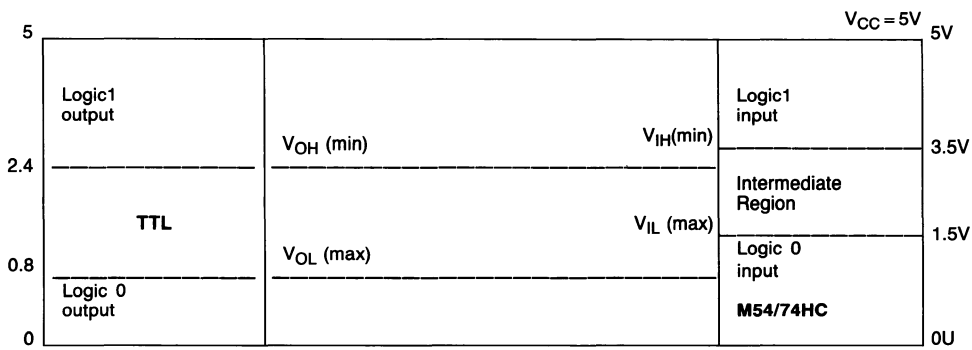


Fig. 1



TTL Driven by M54/74HC

Given that HC devices have output-high levels close to V_{CC} and output-low levels close to 0V, it is obvious that there are no difficulties in driving TTL devices which require 2V minimum input to guarantee a high level and 0.8V maximum input to guarantee a low level. Straightforward connection is therefore possible as is shown in fig. 4. The output drive capability for M54/74HC devices is shown in table 2. This translates into a fan-out of 2 for TTL devices and 10 for LSTTL devices. In the case of bus drivers the fan-out is increased to 15 LSTTL loads.

Fig. 4

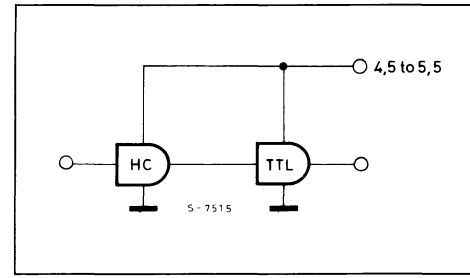


TABLE 2

	M54/74HC	TTL	LSTTL
I_{OH} (V_{OH} = 4.6V.)	−4mA		
I_{OL} (V_{OL} = 0.4V.)	4mA		
I_{IH} (V_{IH} = 5.25V.)		40μA max	20μA max
I_{IL} (V_{IL} = 0.4V.)		−1.6mA max	−0.4mA max

HS-C²MOS EQUIVALENT FAN-OUTS	LSTTL		TTL		S-TTL		ALS-TTL	
	Min.	Typ.	Min.	Typ.	Min.	Typ.	Min.	Typ.
STANDARD OUTPUTS	10	20	02	04	02	04	20	40
BUS DRIVERS OUTPUTS	15	30	04	08	03	06	30	60

Interfacing M54/74HC with NMOS/HMOS

The introduction of fast logic in C-MOS technology will allow the replacement of many bipolar devices currently used to support the majority of NMOS and HMOS LSI devices.
A pull-up resistor is required when HC devices are being driven from NMOS/HMOS devices since the minimum output-high level from NMOS/HMOS is only 2.4V and the minimum V_{IN} to HC devices is 3.4V. (iF. V_{CC} = 5V). Direct connection is possible when HC devices are driving NMOS/HMOS devices. An example of an HC/NMOS system is shown in fig. 5.

Fig. 5 - M4146 is 16384 x 1 Bit Dynamic Memory

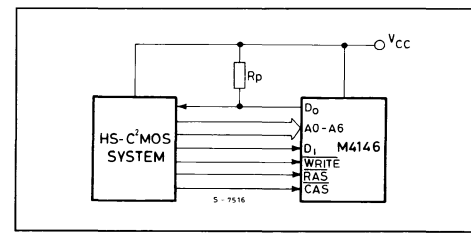
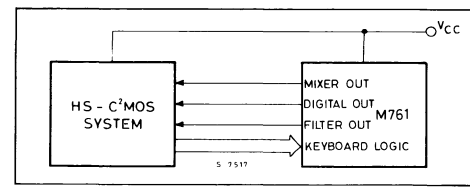


Fig. 6 - M761 is Dual Tone Multifrequency Generator



M54/74HC Interfaced with CMOS LSI

Little need be said on this type of interface since both types of device can be supplied by the same voltage and have equivalent logic levels. Direct connection is therefore possible. An example of an HC/CMOS LSI system is shown in fig. 6.

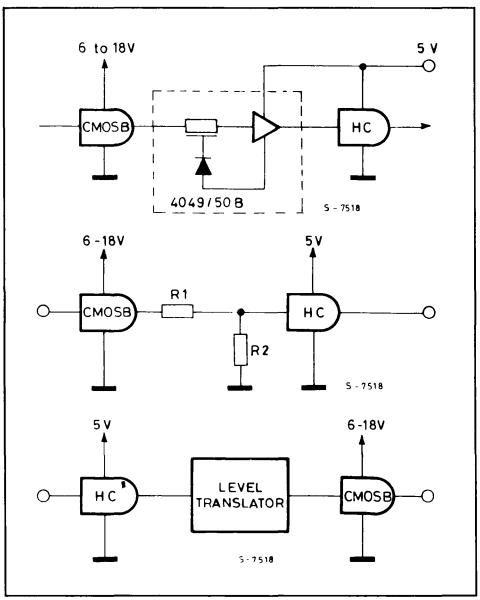
M54/74HC Interfaced with Standard CMOS B

When HC devices are to be connected to CMOSB devices, the level of supply voltage has to be taken into consideration. If the CMOSB supply is between 3 and 6 volts, direct interfacing is possible in both directions. When the supply is outside the HC range, level translators may be required. Fig. 7 shows possible connection configurations.

Interfacing HS-C MOS to ECL

Two of the many possible ways of interfacing between High Speed Logic and ECL logic are shown in fig. 8. In the first case level translators are used, while in the second case the HC logic is supplied by connecting V_{CC} to zero and the ground connection to $-5.2V$.

Fig. 7



Unused Inputs

Unused Inputs should be connected either to $+V_{CC}$ via a limiting resistor of between 100K and 1MΩ or directly to ground, depending on their logic function.

Handling Precautions

In addition to its high performance, HS-C²MOS has improved input and output protection against electrostatic discharge and voltage transients. A poly-silicon resistor on the input is connected to two reverse biased diodes. Two reverse biased diodes are also included on the output as shown in fig. 9. The resistance limits input transients which are then eliminated by the two diodes. The two diodes on the output carry out the same function.
Although HS-C² MOS includes improved protection it is still recommended that all the standard precautions for MOS devices are observed.

Fig. 8

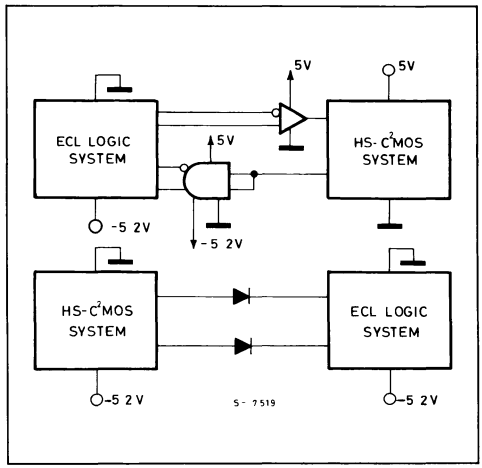
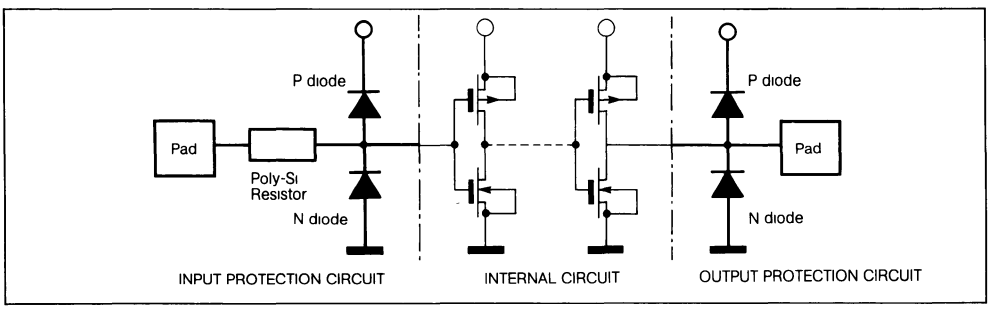


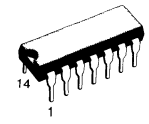
Fig. 9



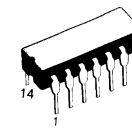
DATASHEETS

QUAD 2-INPUT NAND GATE

- HIGH SPEED
  t_{PD} = 8 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS00
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4mA (MIN)



B1
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

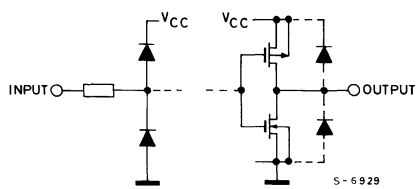
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC00 F1
M74HC00 B1N
M74HC00 F1
M74HC00 C1
M74HC00 M1

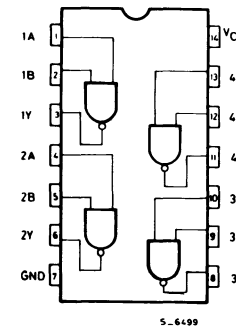
DESCRIPTION

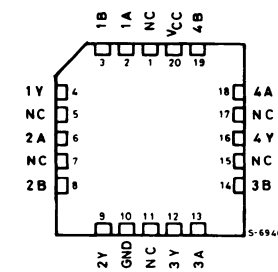
The M54/74HC00 is a high speed CMOS QUAD 2-INPUT NAND GATE fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



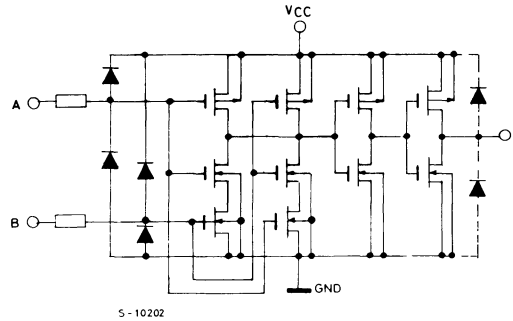
PIN CONNECTIONS (top view)





NC =
No Internal
Connection

CIRCUIT SCHEMATIC (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

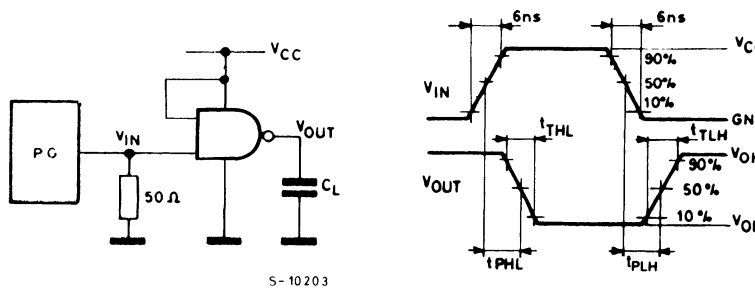
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		9	15	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

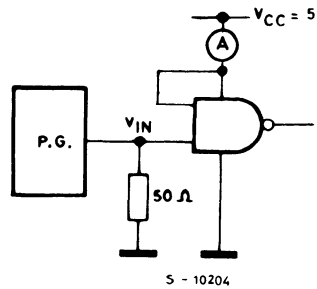
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	40	90	—	115		135	ns
		4.5		—	10	18	—	23		27	
		6.0		—	9	15	—	20		23	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	22	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following equation.
$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per Gate).

SWITCHING CHARACTERISTICS TEST CIRCUIT



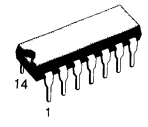
TEST CIRCUIT I_{CC} (Opr.)



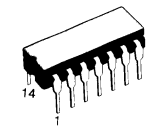
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

QUAD 2-INPUT NOR GATE

- HIGH SPEED
  t_{PD} = 8 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS02



B1
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

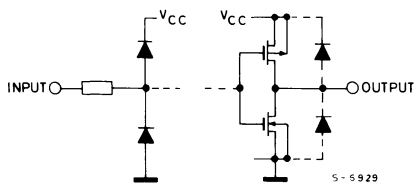
ORDERING NUMBERS:

M54HC02 F1	M74HC02 C1
M74HC02 B1N	M74HC02 M1
M74HC02 F1	

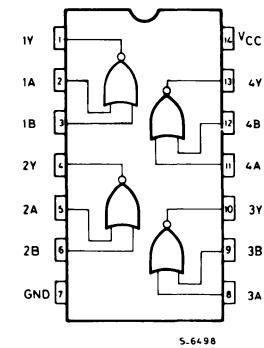
DESCRIPTION

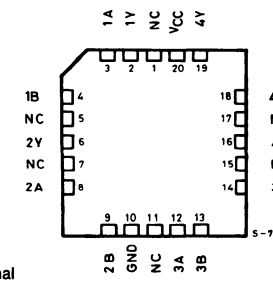
The M54/74HC02 is a high speed CMOS QUAD 2-INPUT NOR GATE fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
The internal circuit is composed of 3 stages including buffer output, which gives high noise immunity and stable output.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



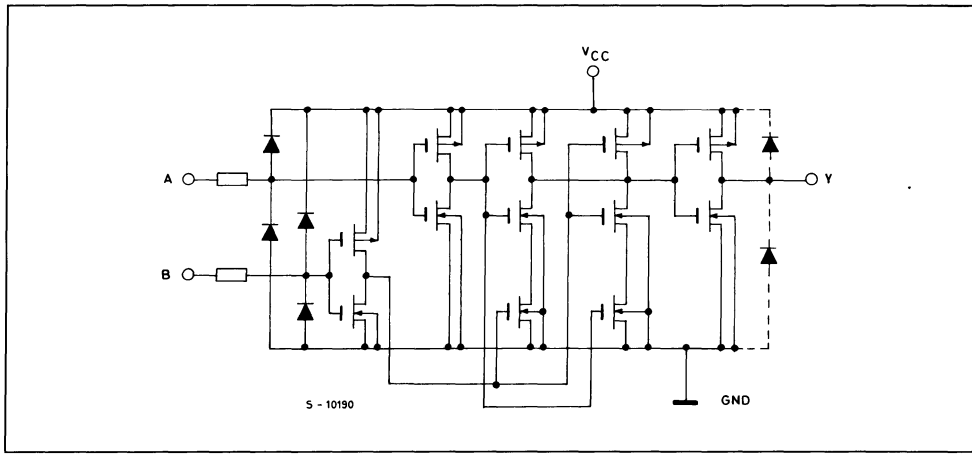
PIN CONNECTIONS (top view)





NC = No Internal Connection

CIRCUIT SCHEMATIC (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400		ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

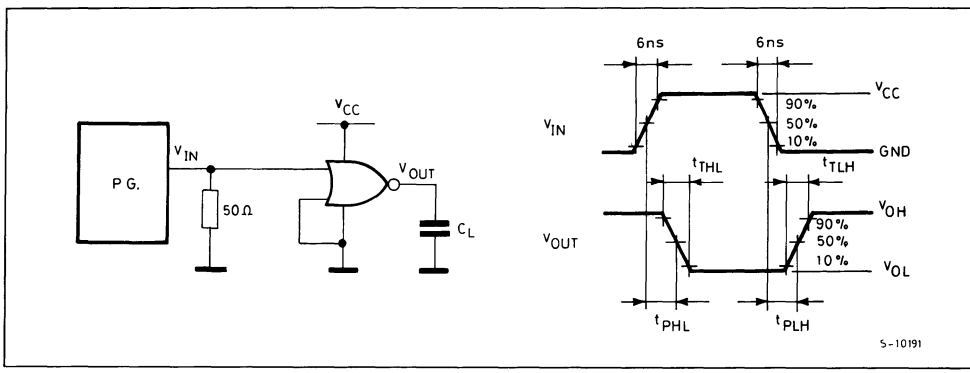
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		9	15	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

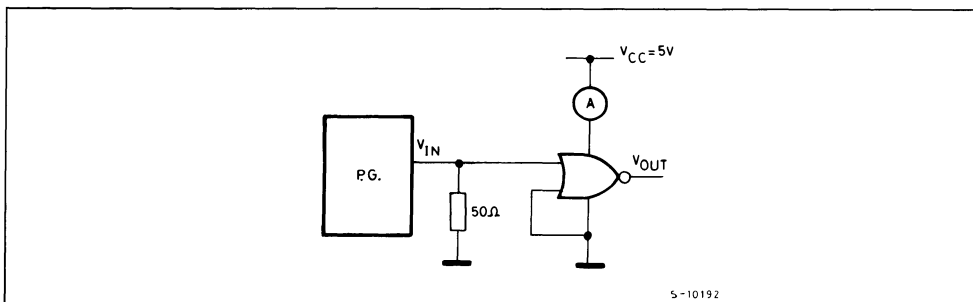
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	40	90	—	115		135	ns
		4.5		—	10	18	—	23		27	
		6.0		—	19	15	—	20		23	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	27	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following equation
I_{CC} (Opr) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



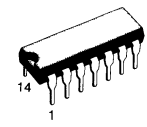
TEST CIRCUIT I_{CC} (Opr.)



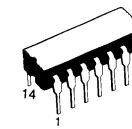
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

QUAD 2-INPUT OPEN DRAIN NAND GATE

- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS03



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

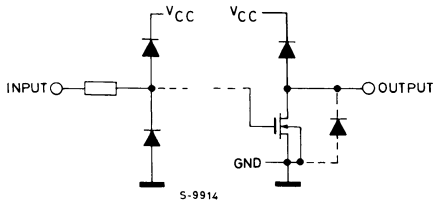
M54HC03 F1	M74HC03 C1
M74HC03 B1N	M74HC03 M1
M74HC03 F1	

DESCRIPTION

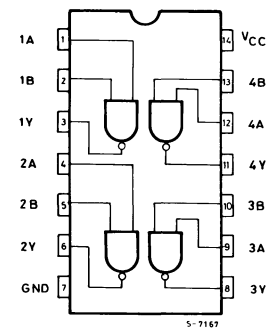
The M54/74HC03 is a high speed CMOS QUAD 2 -INPUT OPEN DRAIN NAND GATE fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

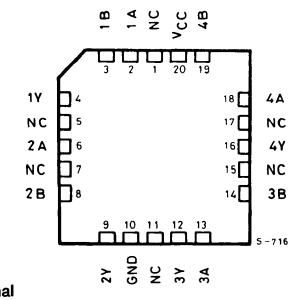
The internal circuit is composed of 3 stages including buffer output, which gives high noise immunity and stable output. This device can, with an external pull-up resistor, be used in wired AND configuration. This device can be also used as a led driver and in any other application requiring a current sink. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





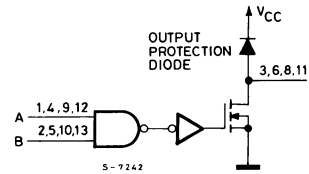
NC = No Internal Connection

TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
L	L	Z
L	H	Z
H	L	Z
H	H	L

Z = HIGH IMPEDANCE

CIRCUIT DIAGRAM



V_{CC} = Pin 14
GND = Pin 7
open-drain outputs

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C
T_L	Lead Temperature	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V: 0 to 1000 V_{CC} 4.5V: 0 to 500 V_{CC} 6 V: 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OL}	Low Level Output Voltage	2.0	V_I	I_O	—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{OZ}	Output Leakage Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±10	
I_{CC}	Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $C_L = 15pF$, Input $t_r = t_f = 6ns$ $T_A = 25°C$)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
t_{TLH} t_{THL}	Output Transition Time			4	8	ns
t_{PLZ} t_{PZL}	Propagation Delay Time	$C_L = 5pF$		8	16	ns
		$C_L = 15pF$		10	20	

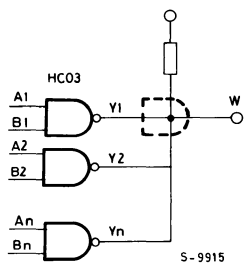
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PZL} t_{PLZ}	Propagation Delay Time	2.0	$R_L = 1K\Omega$	—	52	125	—	155	—	190	ns
		4.5		—	13	25	—	31	—	38	
		6.0		—	11	21	—	26	—	32	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{OUT}	Output Capacitance			—	5	—	—	—	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance			—	17	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained from the equation:
$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ [per Gate]

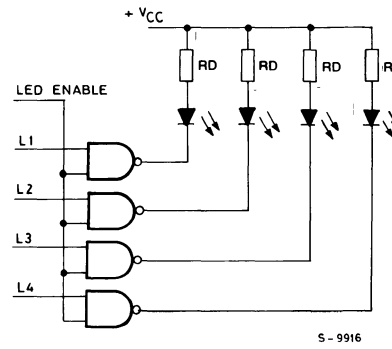
TYPICAL APPLICATIONS

Wired AND



$W = Y1\ Y2\ \ldots\ Yn = \overline{A1B1}\ \overline{A2B2}\ \ldots\ \overline{AnBn} = A1B1 + A2B2 + \ldots AnBn$

LED Driver with Blanking



Typical values
$V_{CC} = 5V$
$V_D = 2V$
$V_{DS} = 0.4V$
$R_D = 120 - 270\Omega$

$I_D = 10 - 20mA$

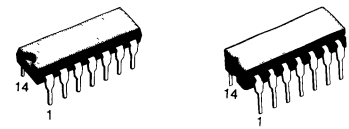
$$R_D = \frac{V_{CC} - V_D - V_{DS}}{I_D} = \frac{5 - 2 - 0.4}{(10 - 20)10^{-3}} = 130 \div 260\Omega$$

SGS-THOMSON MICROELECTRONICS

M54HC04
M74HC04

HEX INVERTER

- HIGH SPEED
  t_{PD} = 8 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS04



B1
Plastic Package

F1
Ceramic Frit Seal Package

M1
Micro Package

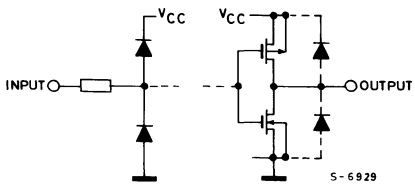
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC04 F1
M74HC04 B1N
M74HC04 F1
M74HC04 C1
M74HC04 M1

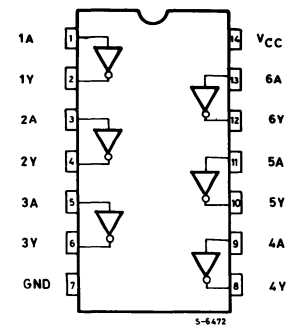
DESCRIPTION

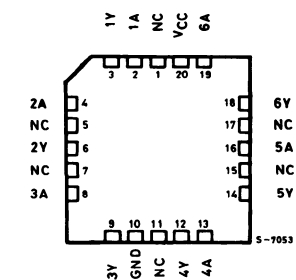
The M54/74HC04 is a high speed CMOS HEX INVERTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output. All inputs are equipped with circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



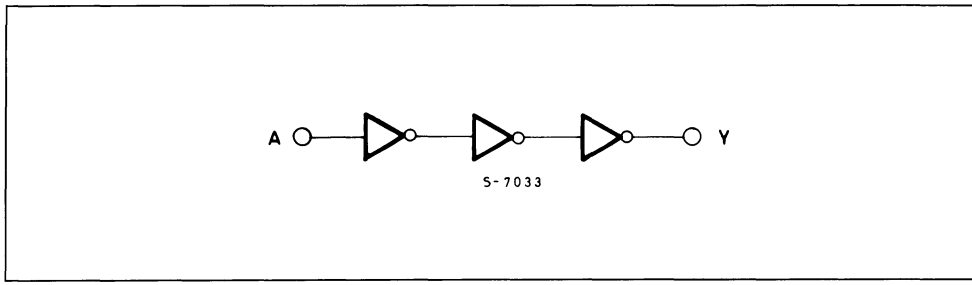
PIN CONNECTIONS (top view)





NC = No Internal Connection

LOGIC DIAGRAM (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

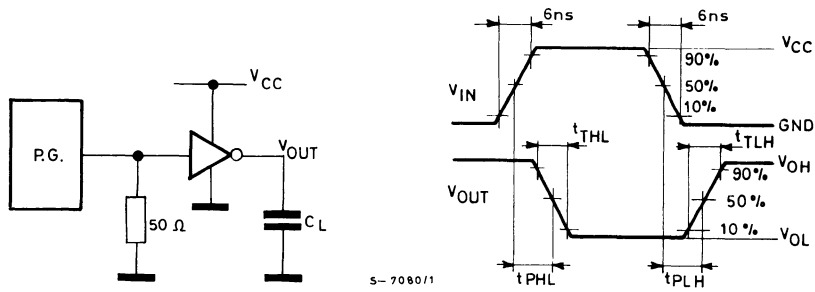
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		9	15	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

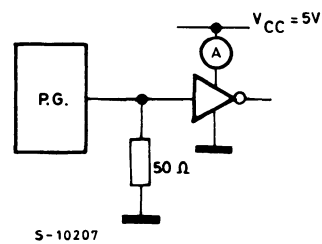
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	40	90	—	115		135	ns
		4.5		—	10	18	—	23		27	
		6.0		—	9	15	—	20		23	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	22	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following equation.
$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per Gate).

SWITCHING CHARACTERISTICS TEST CIRCUIT



TEST CIRCUIT I_{CC} (Opr.)



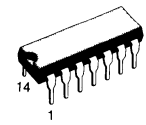
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

SGS-THOMSON MICROELECTRONICS

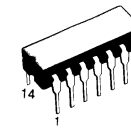
M54HCT04
M74HCT04

HEX INVERTER

- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS04



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HCT04 F1
M74HCT04 B1N
M74HCT04 F1
M74HCT04 C1
M74HCT04 M1

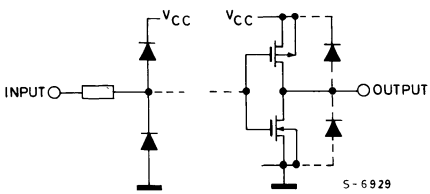
DESCRIPTION

The M54/74HCT04 is a high speed CMOS INVERTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

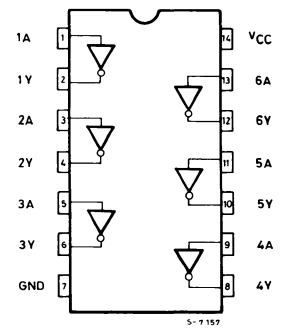
The internal circuit is composed of 3 stages including buffered output, which gives high noise immunity and a stable output.
All inputs are equipped with protection circuits against static discharge and transient excess voltage. This integrated circuit has input and output characteristic that are fully compatible with 54/74 LSTTL logic families.

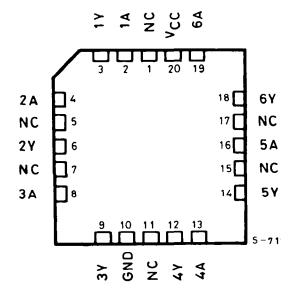
M54HCT/74HCT devices are designed to directly interface HSC²MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



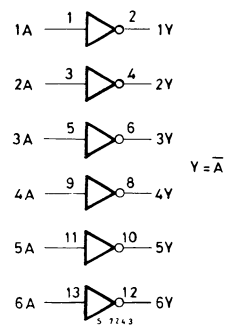
PIN CONNECTIONS (top view)





NC = No Internal Connection

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	4.5 to 5.5		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 4.5 to 5.5V	0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			— 2.0 —	— — —	— — —	— 2.0 —	— — —	— 2.0 —	— — —	V
V_{IL}	Low Level Input Voltage	4.5 to 5.5			— — —	— — —	— 0.8 —	— — —	— 0.8 —	— — —	— 0.8 —	V
V_{OH}	High Level Output Voltage		V_I	I_O								
		4.5	V_{IH}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	V
		4.5	or V_{IL}	−4.0 mA	4.18	4.31	—	4.13	—	4.10		
V_{OL}	Low Level Output Voltage		V_I	I_O								
		4.5	V_{IH}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5	or V_{IL}	4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	5.5	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND		—	—	1	—	10	—	20	μA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin $V_{IN} = 2.4V$ Other Inputs at V_{CC} or GND $I_O = 0$		—	—	2.0	—	2.9	—	3.0	mA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $C_L = 15pF$, Input $t_r = t_f = 6ns$, $T_A = 25°C$)

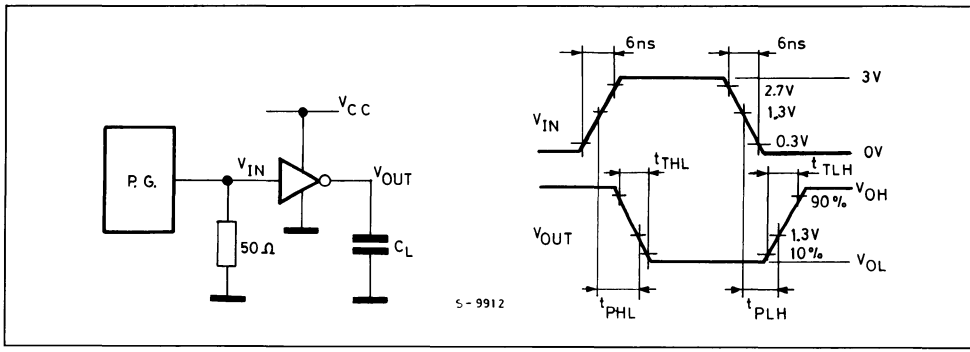
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		10	17	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

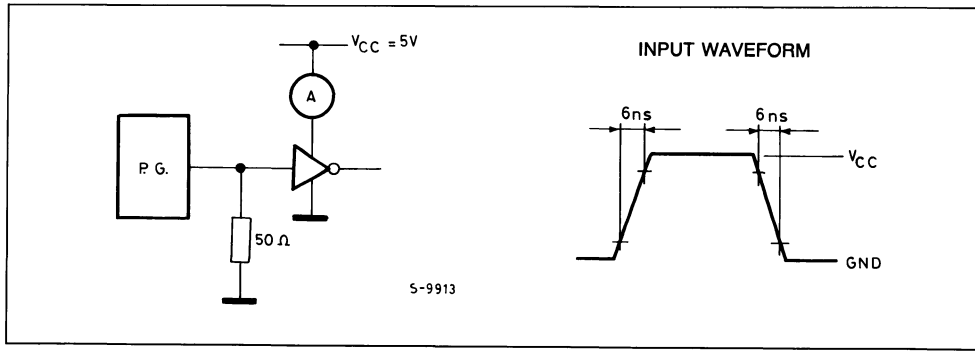
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH}	Output Transition Time	4.5		—	8	15	—	19	—	22	ns
t_{PLH} t_{PHL}	Propagation Delay Time	4.5		—	13	20	—	25	—	30	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	25	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (refer to Test circuit).
Average operating current can be obtained by the following equation: $I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$

SWITCHING CHARACTERISTICS TEST CIRCUIT

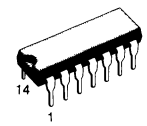


TEST CIRCUIT I_{CC} (Opr.)

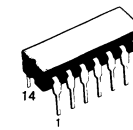


HEX INVERTER (SINGLE STAGE)

- HIGH SPEED
  t_{PD} = 5ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 10% V_{CC} (MIN.)
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (opr) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS04



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

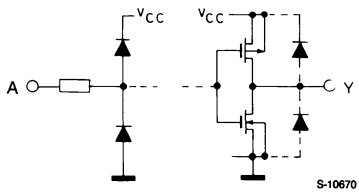
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HCU04 F1
M74HCU04 B1N
M74HCU04 F1
M74HCU04 M1
M74HCU04 C1

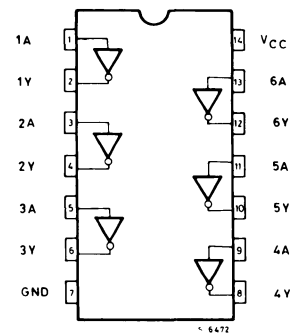
DESCRIPTION

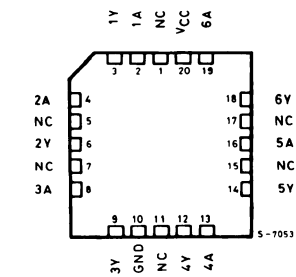
The M54/74HCU04 is a high speed CMOS HEX INVERTER (SINGLE STAGE) fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
As the internal circuit is composed of a single stage inverter, it can be used in crystal oscillators. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

CIRCUIT SCHEMATIC (Per Gate)



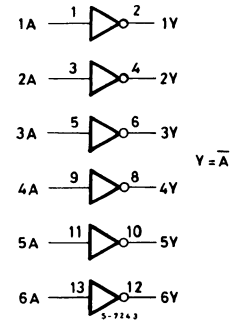
PIN CONNECTION (top view)





NC = No Internal Connection

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW = 65°C derate to 300mW by 10 mW/°C: 65 to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time		NO LIMITS	ns

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.7 3.6 4.8	— — —	— — —	1.7 3.6 4.8	— — —	1.7 3.6 4.8	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.3 0.9 1.2	— — —	0.3 0.9 1.2	— — —	0.3 0.9 1.2	V
V_{OH}	High Level Output Voltage	2.0 4.5 6.0	V_I V_{IH} or V_{IL}	I_O −20 μA	1.8 4.0 5.5	2.0 4.5 5.9	— — —	1.8 4.0 5.5	— — —	1.8 4.0 5.5	— — —	V
		4.5 6.0	V_{CC} or GND	−4.0 mA −5.2 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	
V_{OL}	Low Level Output Voltage	2.0 4.5 6.0	 V_{IH} or V_{IL}	 20 μA	— — —	0.0 0.0 0.1	0.2 0.5 0.5	— — —	0.2 0.5 0.5	— — —	0.2 0.5 0.5	V
		4.5 6.0	V_{CC} or GND	4.0 mA 5.2 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

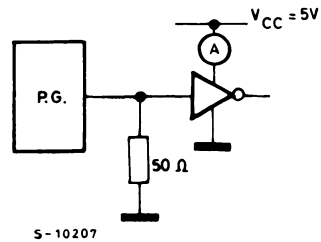
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		7	12	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	32	75	—	95		115	ns
		4.5		—	8	15	—	19		23	
		6.0		—	7	13	—	16		20	
C_{IN}	Input Capacitance			—	9	15	—	15		15	pF
C_{PD} (*)	Power Dissipation Capacitance			—	14	—	—	—			pF

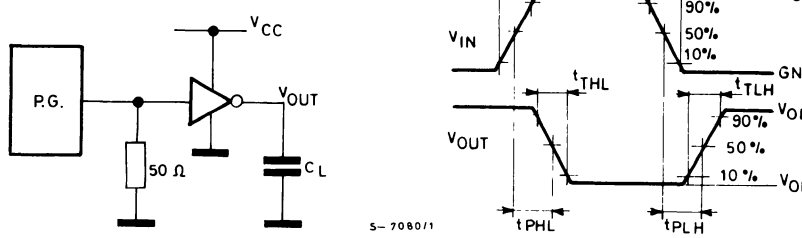
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current is: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

TEST CIRCUIT I_{CC} (Opr)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SWITCHING CHARACTERISTICS TEST CIRCUIT

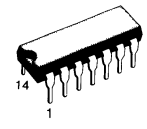


SGS-THOMSON MICROELECTRONICS

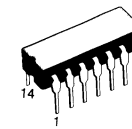
M54HC08
M74HC08

QUAD 2-INPUT AND GATE

- HIGH SPEED
  t_{PD} = 7 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS08



B1
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

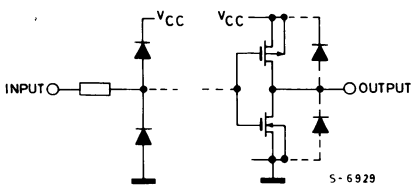
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC08 F1
M74HC08 B1N
M74HC08 F1
M74HC08 C1
M74HC08 M1

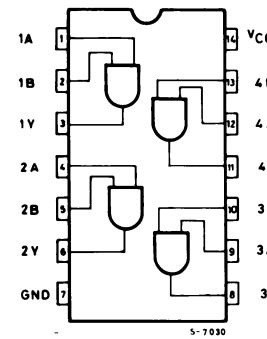
DESCRIPTION

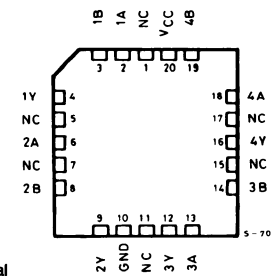
The M54/74HC08 is a high speed CMOS QUAD 2-INPUT AND GATE fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
The internal circuit is composed of 2 stages including buffer output, which gives high noise immunity and stable output.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



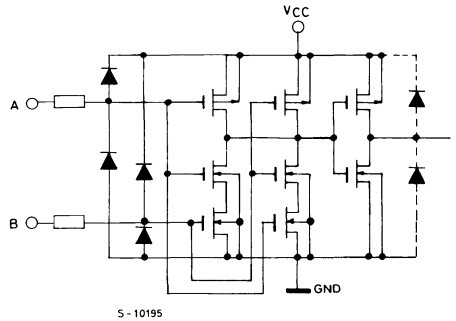
PIN CONNECTIONS (top view)





NC =
No Internal
Connection

CIRCUIT SCHEMATIC (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series Operating Temperature 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		9	15	ns

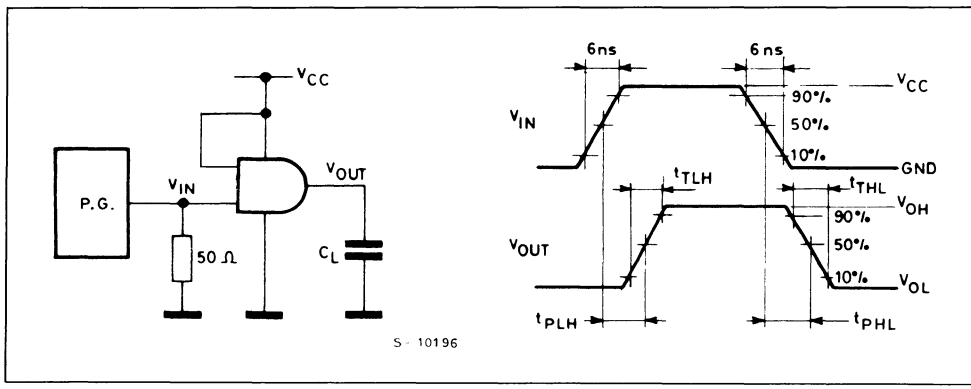
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	40	90	—	115		135	ns
		4.5		—	10	18	—	23		27	
		6.0		—	9	15	—	20		23	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	21	—	—	—			pF

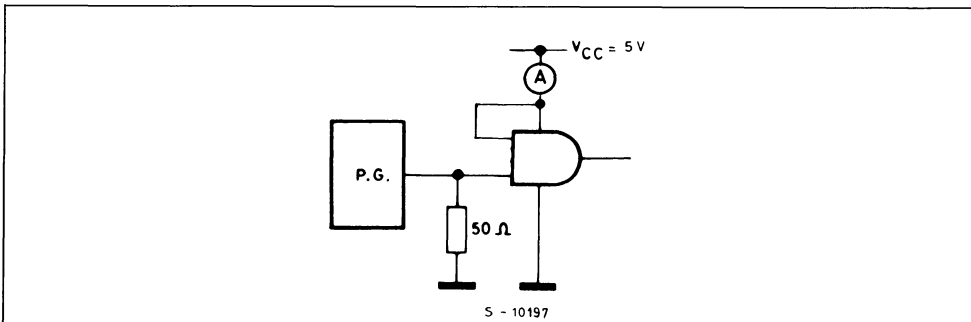
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation:
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



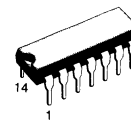
TEST CIRCUIT I_{CC} (Opr.)



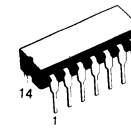
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

TRIPLE 3-INPUT NAND GATE

- HIGH SPEED
  t_{PD} = 8 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS10



B1
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

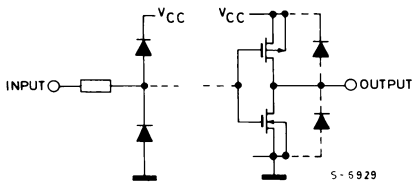
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC10 F1
M74HC10 B1N
M74HC10 F1
M74HC10 C1
M74HC10 M1

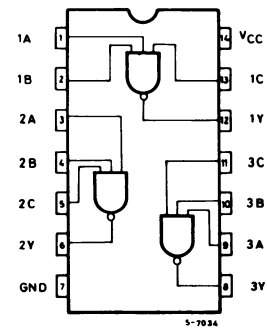
DESCRIPTION

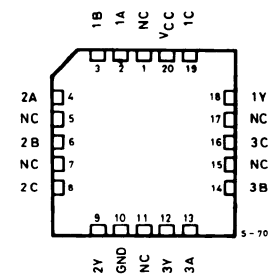
The M54/74HC10 is a high speed CMOS TRIPLE 3-INPUT NAND GATE fabricated with silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



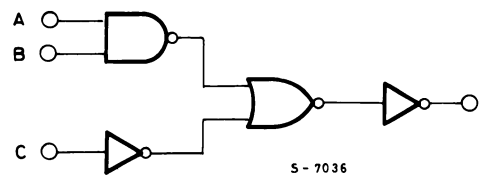
PIN CONNECTIONS (top view)





NC =
No Internal
Connection

LOGIC DIAGRAM (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400		ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

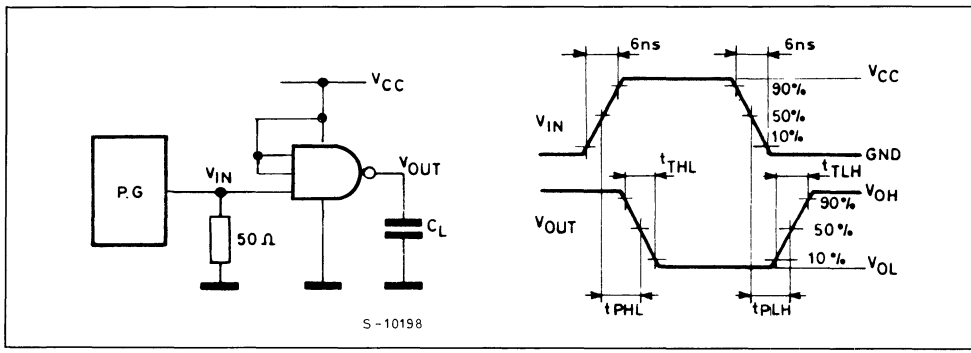
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		9	15	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

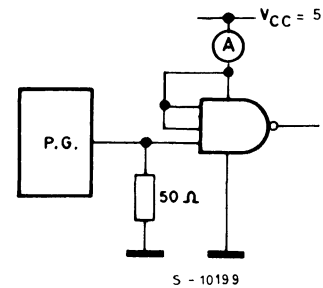
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	44	90	—	115		135	ns
		4.5		—	11	18	—	23		27	
		6.0		—	9	15	—	20		23	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	30	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following equation
I_{CC} (opr.) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/3$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



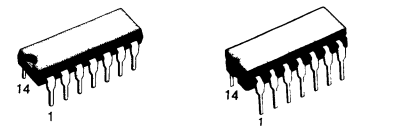
TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

TRIPLE 3-INPUT AND GATE

- HIGH SPEED
  t_{PD} = 10 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS11



B1
Plastic Package

F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

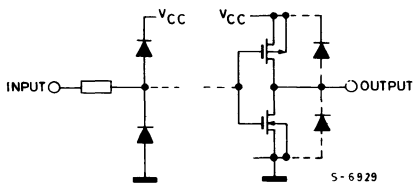
ORDERING NUMBERS:

M54HC11 F1
M74HC11 B1N
M74HC11 F1
M74HC11 C1
M74HC11 M1

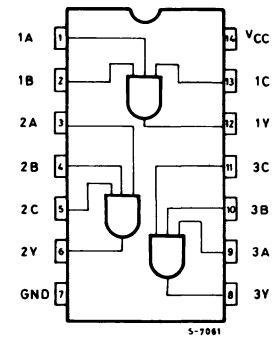
DESCRIPTION

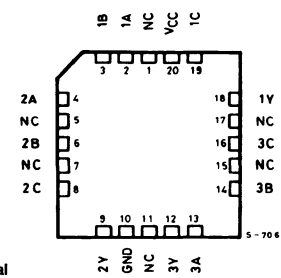
The M54/74HC11 is a high speed CMOS TRIPLE 3-INPUT AND GATE fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
The internal circuit is composed of 3 stages including buffer output, which gives high noise immunity and stable output.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



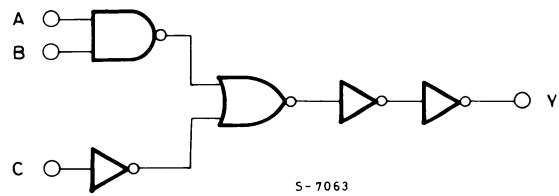
PIN CONNECTIONS (top view)





NC = No Internal Connection

LOGIC DIAGRAM (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

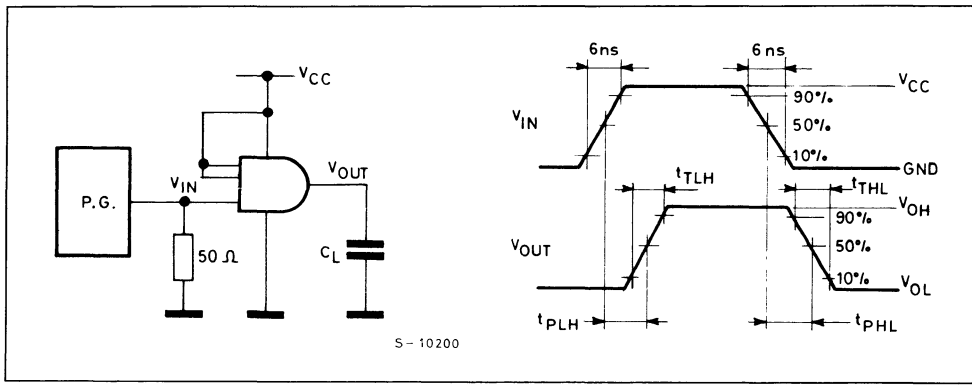
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		11	18	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

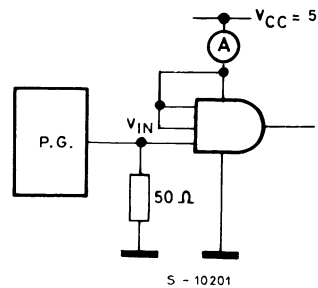
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	56	110	—	140		165	ns
		4.5		—	14	22	—	28		33	
		6.0		—	12	19	—	24		28	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	28	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following equation $I_{CC}(Opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/3$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



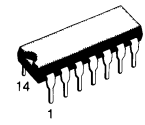
TEST CIRCUIT I_{CC} (Opr.)



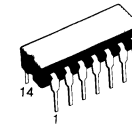
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

HEX SCHMITT INVERTER

- HIGH SPEED
  t_{PD} = 14 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS14



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

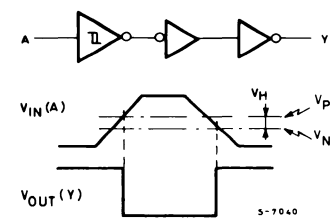
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC14 F1
M74HC14 B1N
M74HC14 F1
M74HC14 C1
M74HC14 M1

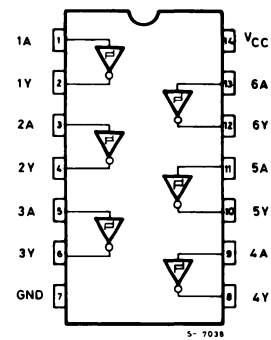
DESCRIPTION

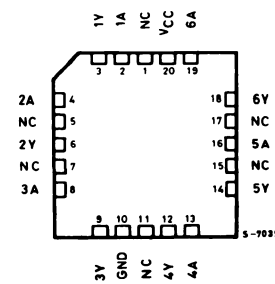
The M54/74HC14 is a high speed CMOS HEX SCHMITT INVERTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. Pin configuration and function are the same as those of the HC04 but all inputs have 20% V_{CC} hysteresis level.
This together with its schmitt trigger function allows it to be used on line receivers with slow rise/fall input signals. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

LOGIC DIAGRAM/WAVEFORM



PIN CONNECTIONS (top view)





NC = No Internal Connection

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time		no limits	

DC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_P	Positive Threshold Voltage	2.0 4.5 6.0		0.8 2.25 3.0	1.25 2.7 3.6	1.5 3.15 4.2	0.8 2.25 3.0	1.5 3.15 4.2	0.8 2.25 3.0	1.5 3.15 4.2	V
V_N	Negative Threshold Voltage	2.0 4.5 6.0		0.4 1.35 1.8	0.75 1.9 2.6	1.0 2.25 3.0	0.4 1.35 1.8	1.0 2.25 3.0	0.4 1.35 1.8	1.0 2.25 3.0	V
V_H	Hysteresis Voltage	2.0 4.5 6.0		0.2 0.4 0.6	0.5 0.8 1.0	1.0 1.4 1.7	0.2 0.4 0.6	1.0 1.4 1.7	0.2 0.4 0.6	1.0 1.4 1.7	V

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
			V_I	I_O	Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	High Level Output Voltage	2.0	V_{IH} or V_{IL}	−20 μA	1.9	2.0	—	1.9	—	1.9	—	V
		4.5			4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

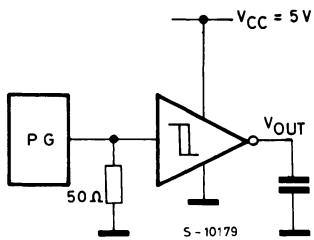
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		14	22	ns

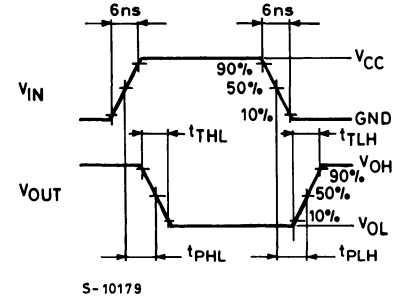
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	68	135	—	170	—	205	ns
		4.5		—	17	27	—	34	—	41	
		6.0		—	14	23	—	29	—	35	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	31	—	—	—	—	—	pF

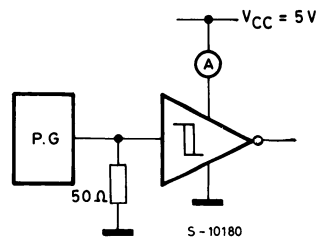
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current is: $I_{CC}(opr) = CPD \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT





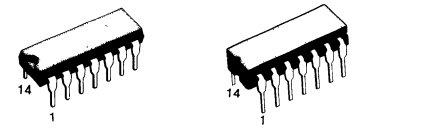
TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

DUAL 4-INPUT NAND GATE

- HIGH SPEED
  t_{PD} = 10 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS20



B1N
Plastic Package

F1
Ceramic Frit Seal Package

M1
Micro Package

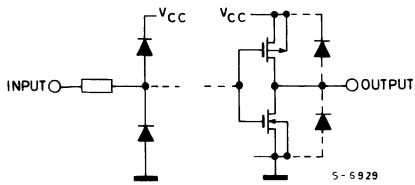
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC20 F1
M74HC20 B1N
M74HC20 F1
M74HC20 C1
M74HC20 M1

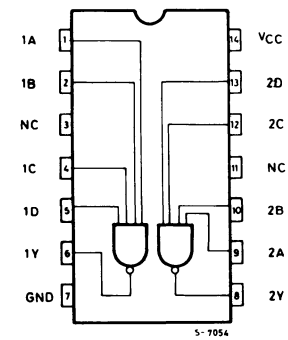
DESCRIPTION

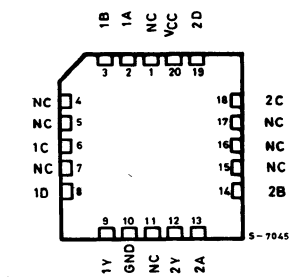
The M54/74HC20 is a high speed CMOS DUAL 4-INPUT NAND GATE fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
The internal circuit is composed of 3 stages including buffered output, which gives high noise immunity and a stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



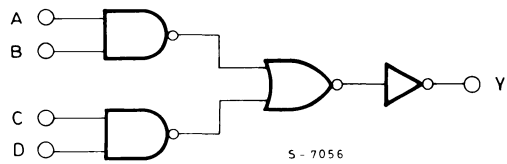
PIN CONNECTIONS (top view)





NC = No Internal Connection

LOGIC DIAGRAM (per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V 4.5V 6 V	0 to 1000 0 to 500 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

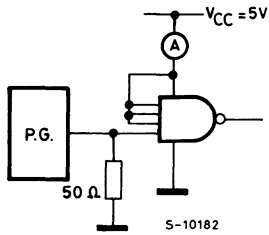
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		11	18	ns

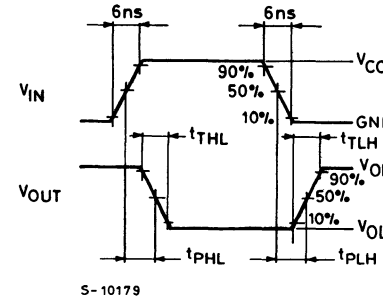
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	44	90	—	115	—	135	ns
		4.5		—	11	18	—	23	—	27	
		6.0		—	9	15	—	20	—	23	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	28	—	—	—	—	—	pF

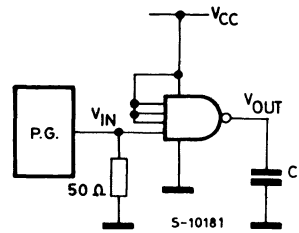
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

SWITCHING CHARACTERISTICS TEST CIRCUIT





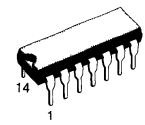
TEST CIRCUIT I_{CC} (Opr.)



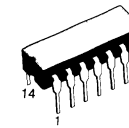
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

DUAL 4-INPUT AND GATE

- HIGH SPEED
  t_{PD} = 11 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS21



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

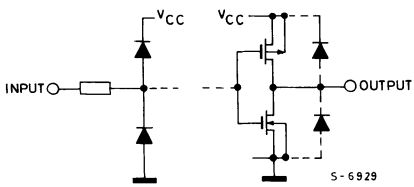
ORDERING NUMBERS:

M54HC21 F1
M74HC21 B1N
M74HC21 F1
M74HC21 C1
M74HC21 M1

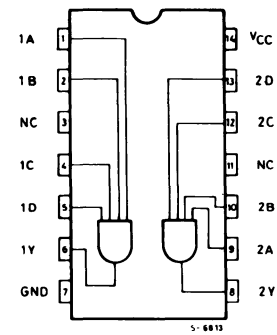
DESCRIPTION

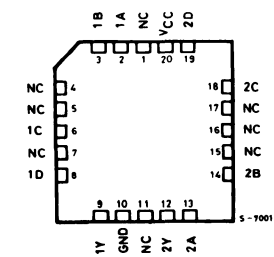
The M54/74HC21 is a high speed CMOS DUAL 4-INPUT AND GATE fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
The internal circuits is composed of 3 stages including buffered output, which gives high noise immunity and a stable output.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



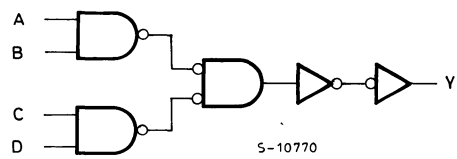
PIN CONNECTIONS (top view)





NC = No Internal Connection

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limit		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC}	2 V: 0 to 1000 4.5V: 0 to 500 6 V: 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

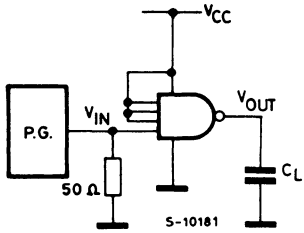
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		11	18	ns

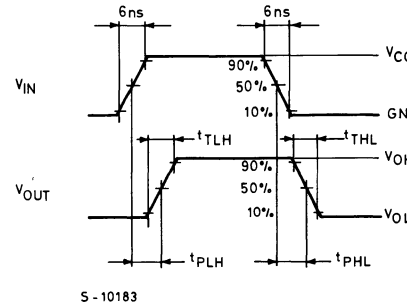
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	52	110	—	140	—	165	ns
		4.5		—	14	22	—	28	—	33	
		6.0		—	12	19	—	24	—	28	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	29	—	—	—	—	—	pF

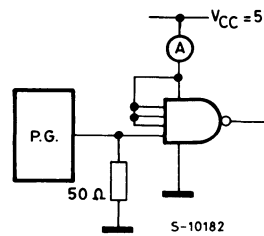
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

SWITCHING CHARACTERISTICS TEST CIRCUIT





TEST CIRCUIT I_{CC} (Opr.)



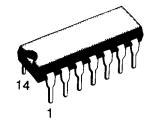
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

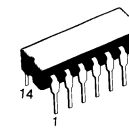
M54HC27
M74HC27

TRIPLE 3-INPUT NOR GATE

- HIGH SPEED
  t_{PD} = 10 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS27



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

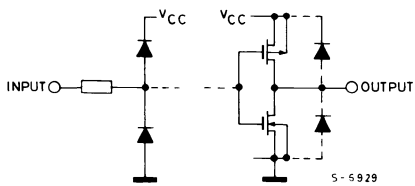
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC27 F1
M74HC27 B1N
M74HC27 F1
M74HC27 C1
M74HC27 M1

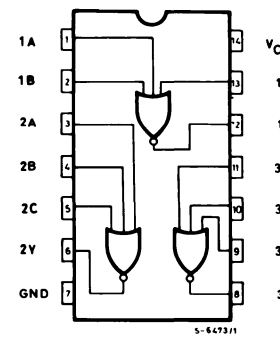
DESCRIPTION

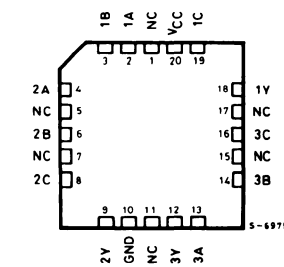
The M54/74HC27 is a high speed CMOS TRIPLE 3-INPUT NOR GATE fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The internal circuit is composed of 3 stages including buffered output, which gives high noise immunity and a stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



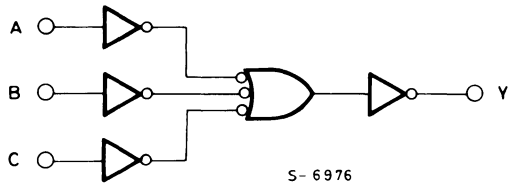
PIN CONNECTIONS (top view)





NC =
No Internal
Connection

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC}	2 V: 0 to 1000 4.5V: 0 to 500 6 V: 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

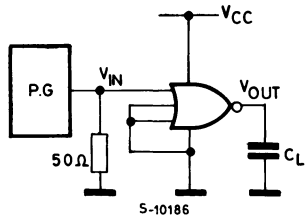
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		9	15	ns

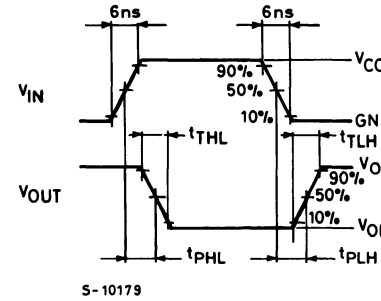
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	44	90	—	115	—	135	ns
		4.5		—	11	18	—	23	—	27	
		6.0		—	9	15	—	20	—	23	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	27	—	—	—	—	—	pF

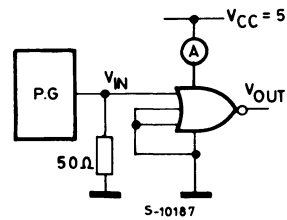
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

SWITCHING CHARACTERISTICS TEST CIRCUIT





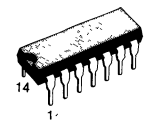
TEST CIRCUIT I_{CC} (Opr.)



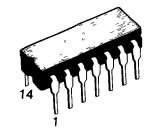
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

8-INPUT NAND GATE

- HIGH SPEED
  t_{PD} = 13 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS30



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

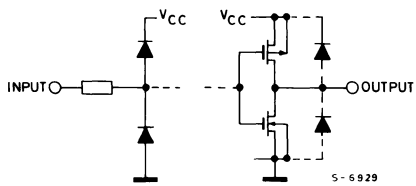
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC30 F1
M74HC30 B1N
M74HC30 F1
M74HC30 C1
M74HC30 M1

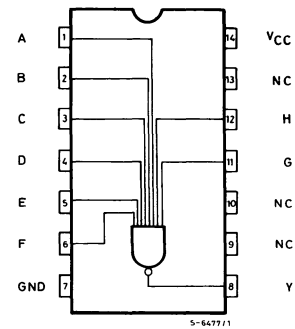
DESCRIPTION

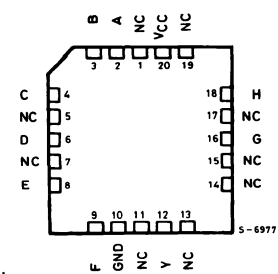
The M54/74HC30 is a high speed CMOS 8-INPUT NAND GATE fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The internal circuit is composed of 5 stages including buffered output, which gives high noise immunity and a stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



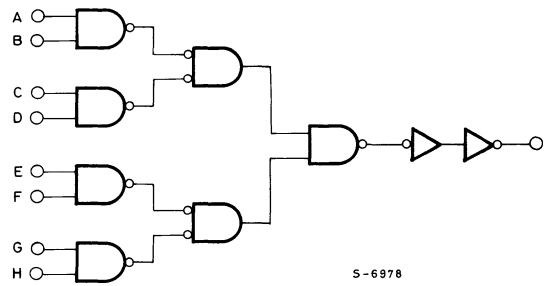
PIN CONNECTIONS (top view)





NC = No Internal Connection

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400		ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

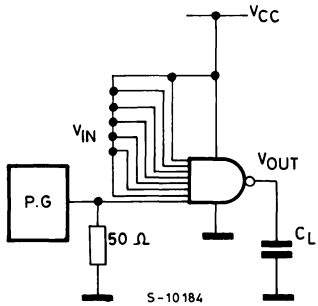
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		13	21	ns

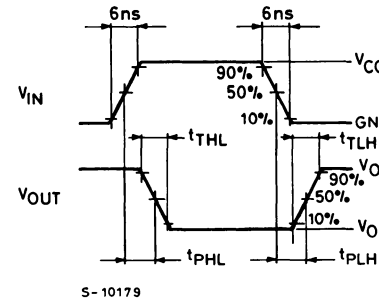
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	64	125	—	155	—	190	ns
		4.5		—	16	25	—	31	—	38	
		6.0		—	14	21	—	26	—	32	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	30	—	—	—	—	—	pF

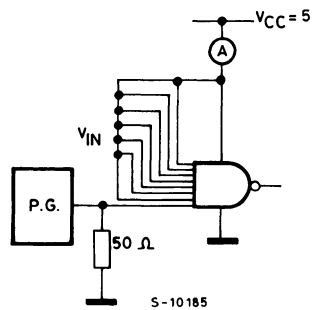
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

SWITCHING CHARACTERISTICS TEST CIRCUIT





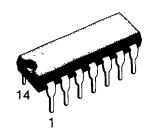
TEST CIRCUIT I_{CC} (Opr.)



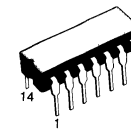
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

QUAD 2-INPUT OR GATE

- HIGH SPEED
  t_{PD} = 8 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS32



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

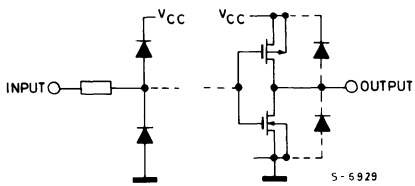
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC32 F1
M74HC32 B1N
M74HC32 F1
M74HC32 C1
M74HC32 M1

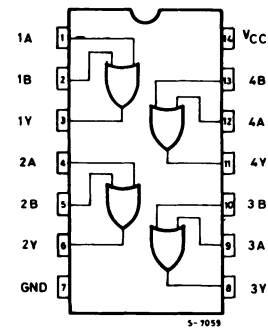
DESCRIPTION

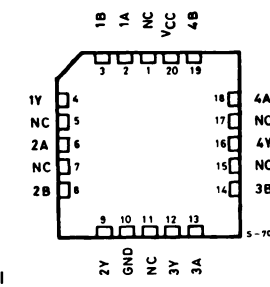
The M54/74HC32 is a high speed CMOS 2-INPUT OR GATE fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The internal circuit is composed of 2 stages including buffered output, which gives high noise immunity and a stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



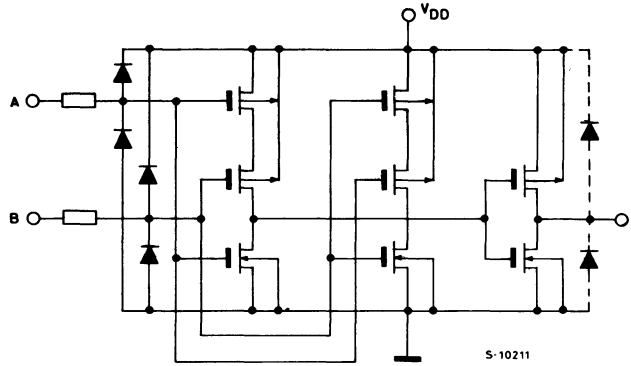
PIN CONNECTIONS (top view)





NC =
No Internal
Connection

CIRCUIT SCHEMATIC (per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC}	2 V: 0 to 1000 4.5V: 0 to 500 6 V: 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

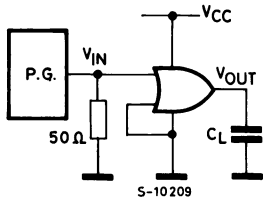
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		9	15	ns

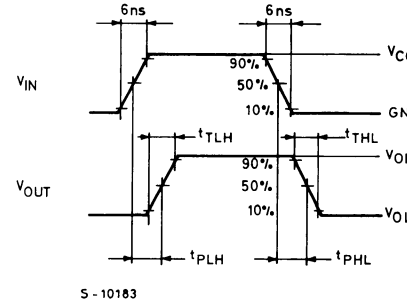
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	40	90	—	115	—	135	ns
		4.5		—	10	18	—	23	—	27	
		6.0		—	9	15	—	20	—	23	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	23	—	—	—	—	—	pF

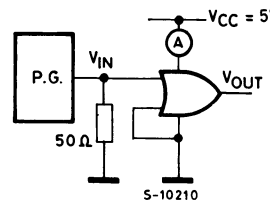
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

SWITCHING CHARACTERISTICS TEST CIRCUIT





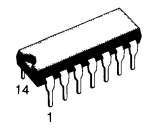
TEST CIRCUIT I_{CC} (Opr.)



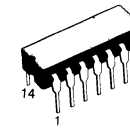
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

BCD-TO-DECIMAL DECODER

- HIGH SPEED
  t_{PD} = 17 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS42



B1N
Plastic Package



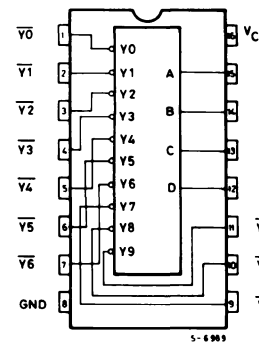
F1
Ceramic Frit Seal Package

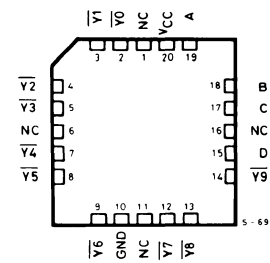
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC42 F1
M74HC42 B1N
M74HC42 F1
M74HC42 C1
M74HC42 M1

PIN CONNECTIONS (top view)



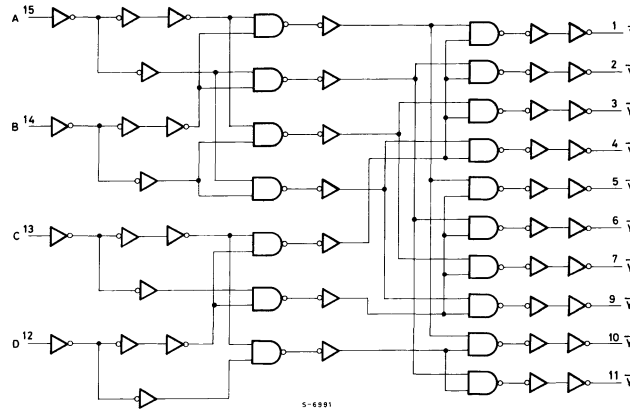


NC = No Internal Connection

DESCRIPTION

The M54/74HC42 is a high speed CMOS BCD-TO-DECIMAL DECODER fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. A BCD code applied to the four inputs A-D selects one of ten decimal outputs $\overline{Y0}$-$\overline{Y9}$, which goes low to fifteen gives a high level at all outputs. This device also can be used as a 3-to-8 LINE DECODER, when the D input is assigned as a disable input. This device is useful for code conversion, address decoding, memory selection, demultiplexing, or readout decoding.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

TRUTH TABLE

CODE No.	BCD INPUTS				DECIMAL OUTPUTS									
	D	C	B	A	$\overline{Y}$	$\overline{Y}1$	$\overline{Y}2$	$\overline{Y}3$	$\overline{Y}4$	$\overline{Y}5$	$\overline{Y}6$	$\overline{Y}7$	$\overline{Y}8$	$\overline{Y}9$
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	H	L	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
10	H	L	H	L	H	H	H	H	H	H	H	H	H	H
11	H	L	H	H	H	H	H	H	H	H	H	H	H	H
12	H	H	L	L	H	H	H	H	H	H	H	H	H	H
13	H	H	L	H	H	H	H	H	H	H	H	H	H	H
14	H	H	H	L	H	H	H	H	H	H	H	H	H	H
15	H	H	H	H	H	H	H	H	H	H	H	H	H	H

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

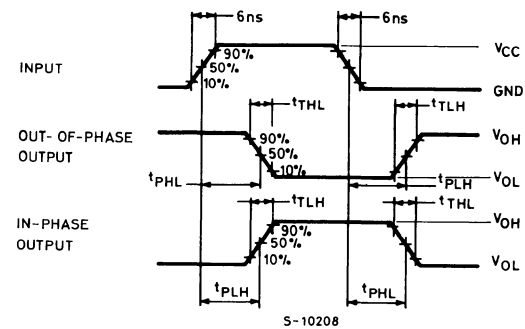
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		15	24	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

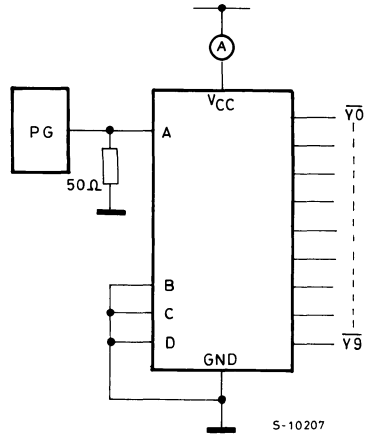
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time	2.0 4.5 6.0		— — —	76 19 16	145 29 25	— — —	180 36 31	— — —	220 44 38	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	67	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following equation I_{CC} (Opr.) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT



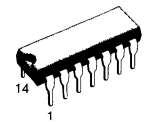
TEST CIRCUIT I_{CC} (Opr.)



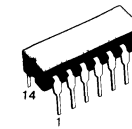
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

DUAL 2 WIDE-2 INPUT AND/OR INVERT GATE

- HIGH SPEED
  t_{PD} = 10 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS51



B1N
Plastic Package



F1
Ceramic Frit Seal Package

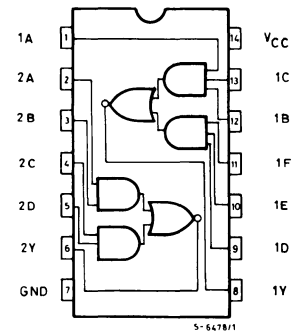
M1
Micro Package

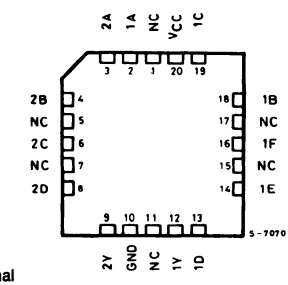
C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC51 F1
M74HC51 B1N
M74HC51 F1
M74HC51 C1
M74HC51 M1

PIN CONNECTIONS (top view)



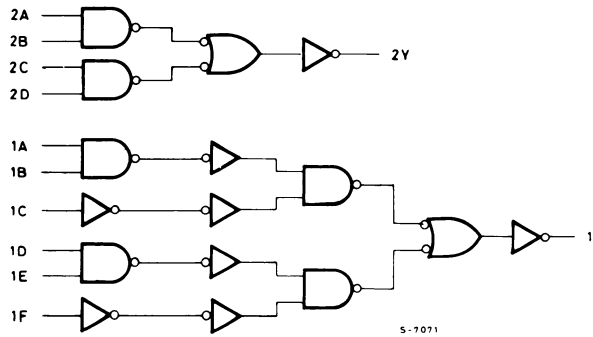


NC =
No Internal
Connection

DESCRIPTION

The M54/74HC51 is a high speed CMOS DUAL 2 WIDE-2 INPUT AND/OR INVERT GATE fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. It contains a 2-WIDE 2-INPUT AND-OR-INVERT GATE and a 2-WIDE 3-INPUT AND-OR-INVERT GATE.
The internal circuit is composed of 3 stages (2-INPUT) or 5 stages (3-INPUT) including buffered output, which gives high noise immunity and a stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0	V_{IL}		5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0	V_{IL}		—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

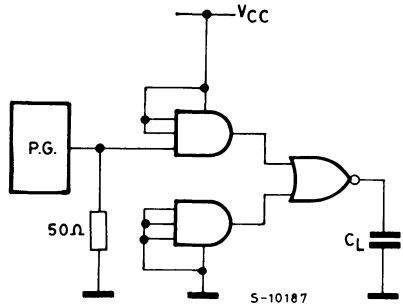
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		10	18	ns

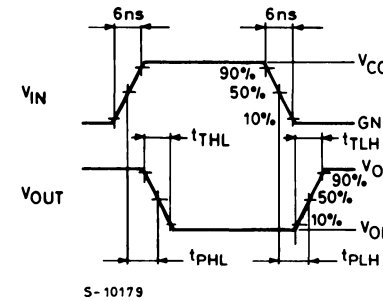
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	52	105	—	130	—	155	ns
		4.5		—	13	21	—	26	—	33	
		6.0		—	11	18	—	22	—	28	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	33	—	—	—	—	—	pF

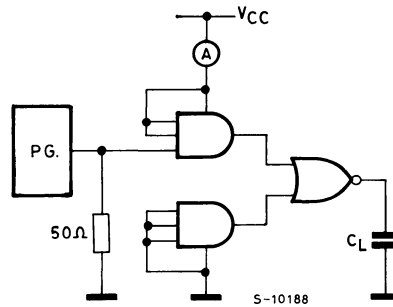
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

SWITCHING CHARACTERISTICS TEST CIRCUIT





TEST CIRCUIT I_{CC} (Opr.)



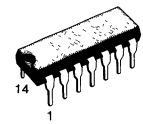
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

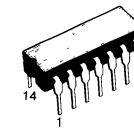
M54HC73
M74HC73

DUAL J-K FLIP FLOP WITH CLEAR

- HIGH SPEED
  f_{MAX} = 60 MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 2 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS73



B1N
Plastic Package



F1
Ceramic Frit Seal Package*

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC73 F1
M74HC73 B1N
M74HC73 F1
M74HC73 C1
M74HC73 M1

DESCRIPTION

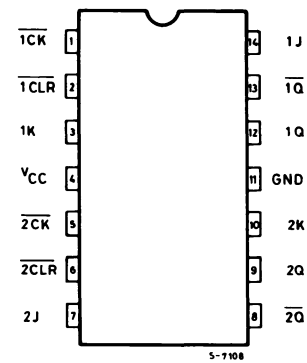
The M54/74HC73 is a high speed CMOS DUAL J-K FLIP FLOP WITH CLEAR fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. Depending on the logic level applied to J and K inputs, this device changes state on the negative going transition of clock input pulse ($\overline{CK}$). The clear function is accomplished independently of the clock condition when the clear input ($\overline{CLR}$) is taken low. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	X	X	X	L	H	CLEAR
H	L	L	↓	Qn	$\overline{Qn}$	NO CHANGE
H	L	H	↓	L	H	—
H	H	L	↓	H	L	—
H	H	H	↓	$\overline{Qn}$	Qn	TOGGLE
H	X	X	↑	Qn	$\overline{Qn}$	NO CHANGE

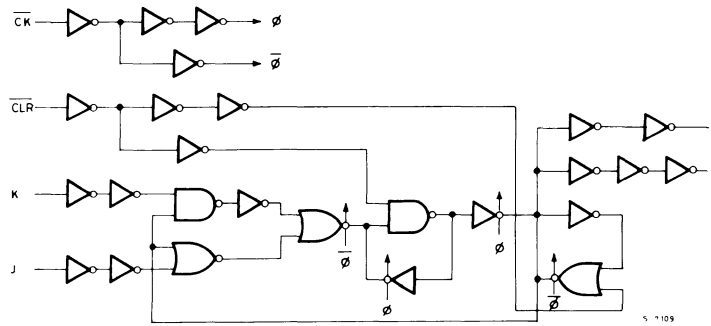
X: DON'T CARE

PIN CONNECTIONS (top view)



FOR CHIP CARRIER
INFORMATION CONTACT SGS-THOMSON

LOGIC DIAGRAM (1/2 of device show)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	2	—	20	—	40	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

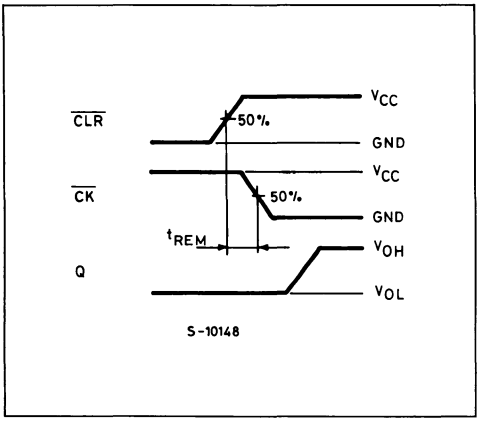
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CK}$-Q, $\overline{Q}$)		16	25	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$-Q, $\overline{Q}$)		20	32	ns
f_{MAX}	Maximum Clock Frequency	33	60		MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

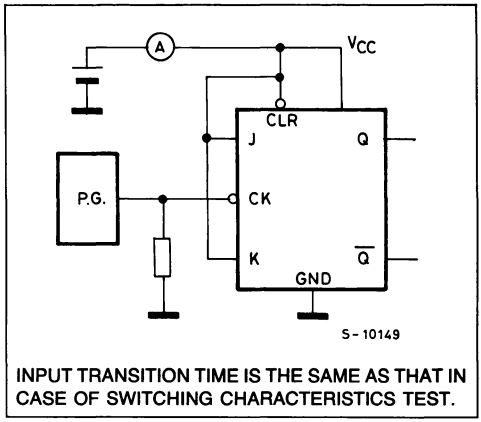
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			-40 to $85°C$ 74HC		-55 to $125°C$ 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	90	—	110	ns
		4.5		—	8	15	—	18	—	22	
		6.0		—	7	13	—	15	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CK}$-Q, $\overline{Q}$)	2.0		—	76	150	—	190	—	225	ns
		4.5		—	19	30	—	38	—	45	
		6.0		—	16	26	—	33	—	38	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$-Q, $\overline{Q}$)	2.0		—	96	185	—	230	—	280	ns
		4.5		—	24	37	—	46	—	56	
		6.0		—	20	31	—	39	—	48	
f_{MAX}	Maximum Clock Frequency	2.0		6	13	—	5	—	4	—	MHz
		4.5		30	52	—	24	—	20	—	
		6.0		35	61	—	28	—	23	—	
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width ($\overline{CK}$)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CL}$)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-Up Time	2.0		—	35	100	—	125	—	150	ns
		4.5		—	9	20	—	25	—	30	
		6.0		—	8	17	—	21	—	26	
t_h	Minimum Hold Time	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{REM}	Minimum Removal Time	2.0		—	5	50	—	65	—	75	ns
		4.5		—	1	10	—	13	—	15	
		6.0		—	1	9	—	11	—	13	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	42	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following equation I_{CC} (Opr.) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per F/F)

SWITCHING CHARACTERISTICS TEST WAVEFORM

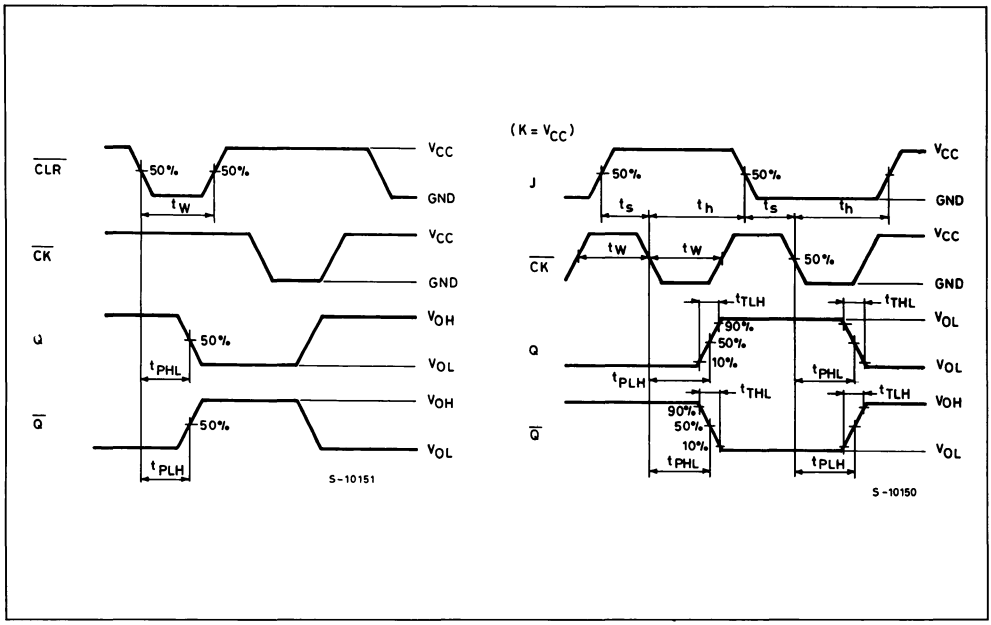


TEST CIRCUIT I_{CC}(Opr)



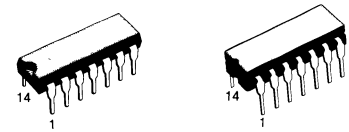
INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SWITCHING CHARACTERISTICS TEST WAVEFORMS



DUAL D TYPE FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED
  f_{MAX} = 53 MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 2 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS74



B1N
Plastic Package

F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC74 F1
M74HC74 B1N
M74HC74 F1
M74HC74 C1
M74HC74 M1

DESCRIPTION

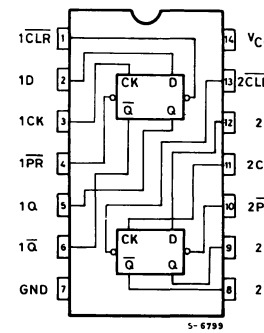
The M54/74HC74 is a high speed CMOS DUAL D TYPE FLOP WITH PRESET AND CLEAR fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. A signal on the D INPUT is transferred to the Q OUTPUT during the positive going transition of the clock pulse. CLEAR and PRESET are independent of the clock and accomplished by a low on the appropriate input. All inputs are equipped with protection circuits againts static discharge and transient excess voltage.

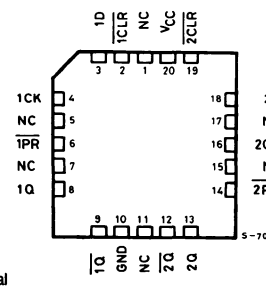
TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Qn	Qn	NO CHANGE

X: DON'T CARE

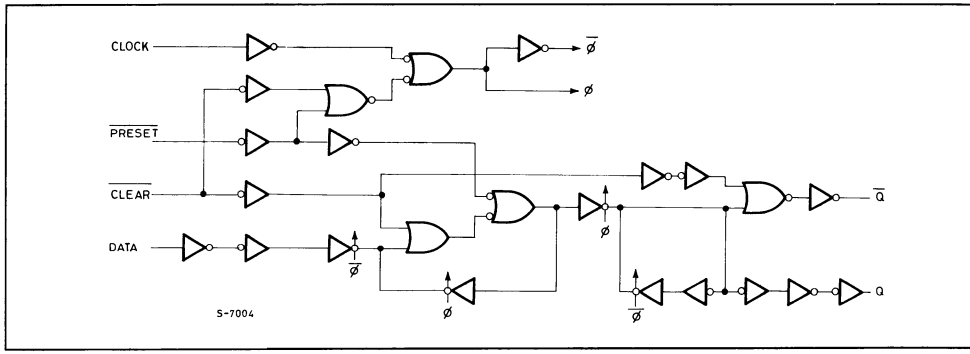
PIN CONNECTIONS (top view)





NC = No Internal Connection

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	20	—	20	—	40	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOCK}$-Q, $\overline{Q}$)		17	28	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$-Q, $\overline{Q}$)		23	36	ns
f_{MAX}	Maximum Clock Frequency	28	46		MHz

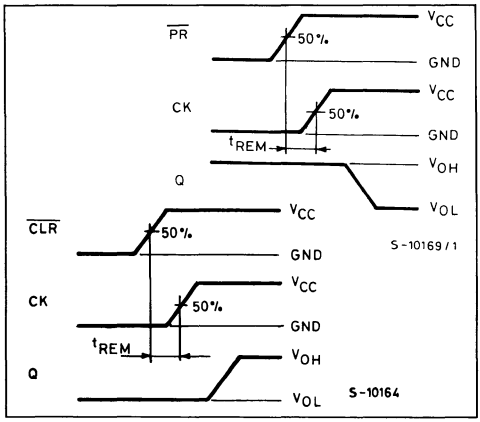
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK-Q, $\overline{Q}$)	2.0 4.5 6.0		— — —	80 20 17	160 32 27	— — —	200 40 34	— — —	240 48 41	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$-Q, $\overline{Q}$)	2.0 4.5 6.0		— — —	104 26 22	205 41 35	— — —	255 51 43	— — —	310 62 53	ns
f_{MAX}	Maximum Clock Frequency	2.0 4.5 6.0		5.4 27 32	12 49 58	— — —	4.4 22 26	— — —	3.6 18 21	— — —	MHz
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CK)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	2.0 4.5 6.0		— — —	40 10 9	100 20 17	— — —	125 25 21	— — —	150 30 26	ns
t_s	Minimum Set-Up Time	2.0 4.5 6.0		— — —	35 9 8	100 20 17	— — —	125 25 21	— — —	150 30 26	ns
t_h	Minimum Hold Time	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
t_{REM}	Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	2.0 4.5 6.0		— — —	45 12 10	100 20 17	— — —	125 25 21	— — —	150 30 26	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	53	—	—	—	—	—	pF

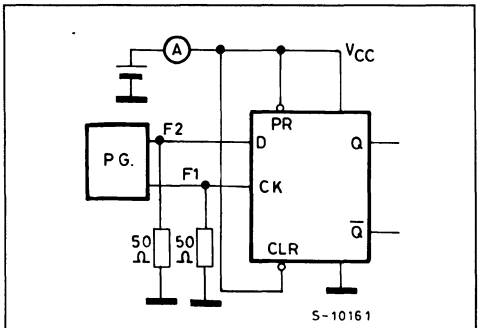
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation:
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ for FLIP/FLOP

SWITCHING CHARACTERISTICS TEST WAVEFORM

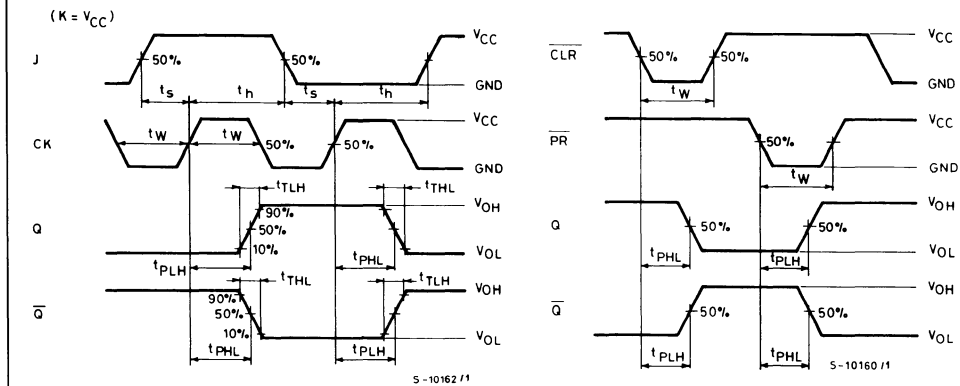


TEST CIRCUIT I_{CC}(Opr)



INPUT TRANSIENT TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.
F2 = F1/2

SWITCHING CHARACTERISTICS TEST WAVEFORM (K = V_{CC})

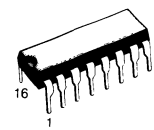


SGS-THOMSON MICROELECTRONICS

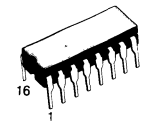
M54HC75
M74HC75

4-BIT D-TYPE LATCH

- HIGH SPEED
  t_{PD} = 15 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 2 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS75



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC75 F1
M74HC75 B1N
M74HC75 F1
M74HC75 C1
M74HC75 M1

DESCRIPTION

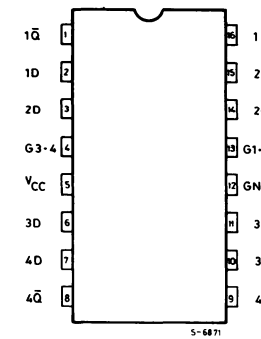
The M54/74HC75 is a high speed CMOS 4-BIT D-TYPE LATCH fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. It contains two groups of 2-bit latches controlled by an enable input (G1 • 2 or G3 •4). These two latch groups can be used in different circuits.
Each latch has Q and $\overline{Q}$ outputs (1Q - 4Q and $1\overline{Q}$ - $4\overline{Q}$). The data applied to the data input is transfered to the Q and $\overline{Q}$ outputs when the enable input is taken high and the outputs will follow the data input as long as the enable input is kept high. When the enable input is taken low, the information data applied to the data input is retained at the outputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUTS		OUTPUTS		FUNCTION
D	G	Q	$\overline{Q}$	
L	H	L	H	—
H	H	H	L	—
X	L	Qn	$\overline{Q}$n	LATCH

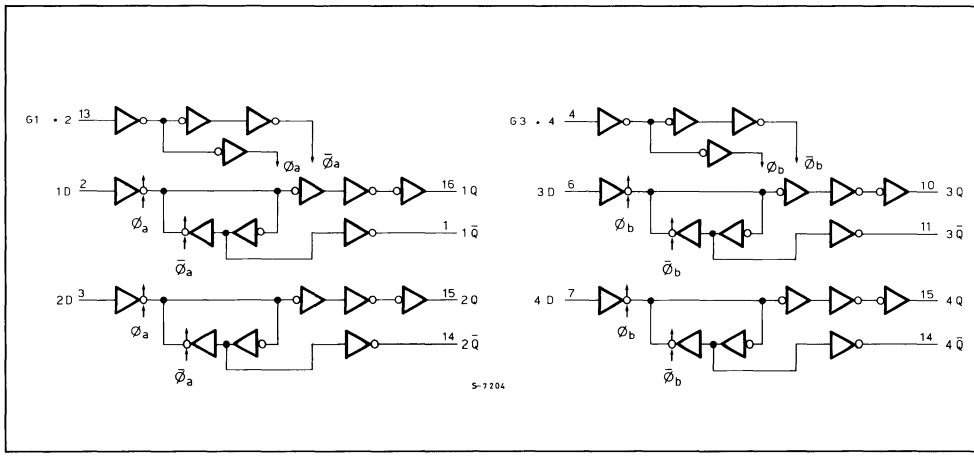
X: DON'T CARE

PIN CONNECTIONS (top view)



FOR CHIP CARRIER
INFORMATION CONTACT SGS-THOMSON

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time		V_{CC} = 2 V	0 to 1000	ns
			V_{CC} = 4.5V	0 to 500	
			V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	2	—	20	—	40	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

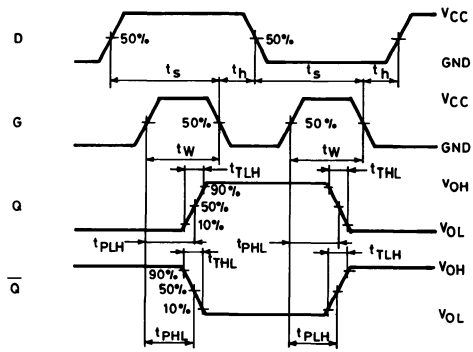
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (DATA-Q, $\overline{Q}$)		12	20	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G-Q, $\overline{Q}$)		15	25	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

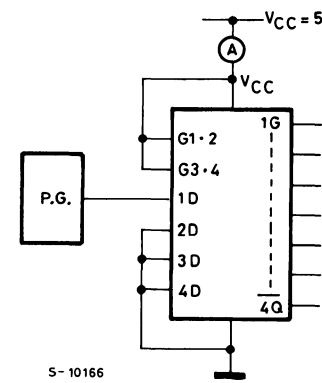
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			-40 to $85°C$ 74HC		-55 to $125°C$ 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA-Q, $\overline{Q}$)	2.0		—	60	120	—	150	—	180	ns
		4.5		—	15	24	—	30	—	36	
		6.0		—	13	20	—	26	—	31	
t_{PLH} t_{PHL}	Propagation Delay Time (G-Q, $\overline{Q}$)	2.0		—	76	145	—	180	—	218	ns
		4.5		—	19	29	—	36	—	44	
		6.0		—	16	25	—	31	—	38	
$t_{W(H)}$	Minimum Pulse Width (G)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-Up Time	2.0		—	5	50	—	65	—	75	ns
		4.5		—	1	10	—	13	—	15	
		6.0		—	1	9	—	11	—	13	
t_h	Minimum Hold Time	2.0		—	—	25	—	30	—	40	ns
		4.5		—	—	5	—	6	—	8	
		6.0		—	—	5	—	6	—	7	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	48	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

SWITCHING CHARACTERISTICS TEST CIRCUIT



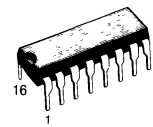
TEST CIRCUIT I_{CC} (Opr)



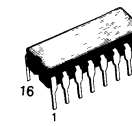
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

DUAL J-K FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED
  f_{MAX} = 60 MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 2 μA (MAX.) at 25°C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN).
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS76



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC76 F1
M74HC76 B1N
M74HC76 F1
M74HC76 C1
M74HC76 M1

DESCRIPTION

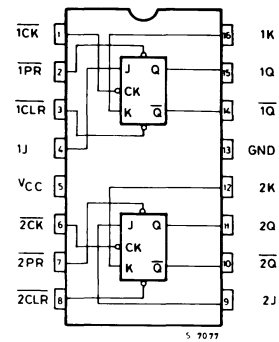
The M54/74HC76 is a high speed CMOS DUAL J-K FLIP FLOP fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. Depending on with the logic level at the J and K inputs this device changes state on the negative going transition of the clock pulse. CLEAR and PRESET are independent of the clock and are accomplished by a logic low on the corresponding input. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUTS					OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	L	↓	Qn	$\overline{Qn}$	NO CHANGE
H	H	L	H	↓	L	H	
H	H	H	L	↓	H	L	
H	H	H	H	↓	$\overline{Qn}$	Qn	TOGGLE
H	H	X	X	↑	Qn	$\overline{Qn}$	NO CHANGE

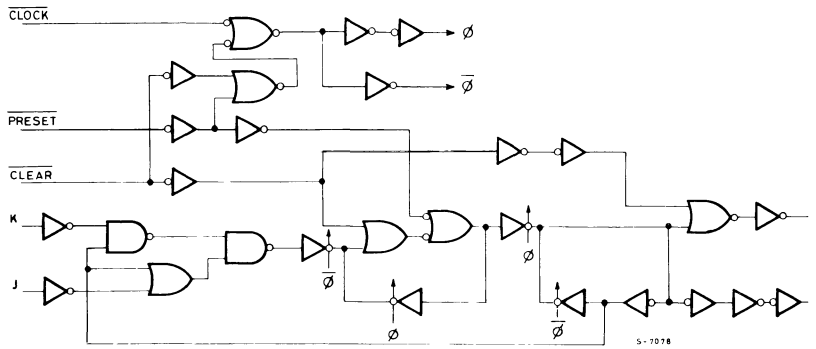
X: DON'T CARE

PIN CONNECTIONS (top view)



FOR CHIP CARRIER
INFORMATION CONTACT SGS-THOMSON

LOGIC DIAGRAM (1/2 Package)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC}	2 V 4.5V 6 V	0 to 1000 0 to 500 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0.0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	2	—	20	—	40	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time $\overline{CLOCK}$-Q, $\overline{Q}$		15	25	ns
t_{PLH} t_{PHL}	Propagation Delay Time $\overline{CLR}$,, $\overline{PR}$-Q, $\overline{Q}$		20	31	ns
f_{MAX}	Maximum Clock Frequency	35	62		MHz

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

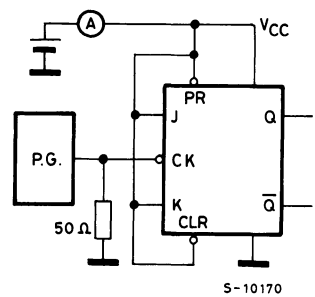
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CK}$ - Q , $\overline{Q}$)	2.0		—	76	145	—	180		220	ns
		4.5		—	18	29	—	36		44	
		6.0		—	15	25	—	31		38	

AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$-Q, $\overline{Q}$)	2.0		—	92	180	—	225	—	270	ns
		4.5		—	23	36	—	45	—	54	
		6.0		—	20	31	—	38	—	46	
f_{MAX}	Maximum Clock Frequency	2.0		6	14	—	5	—	4	—	MHz
		4.5		30	55	—	24	—	20	—	
		6.0		35	65	—	28	—	24	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-up Time	2.0		—	25	75	—	95	—	110	ns
		4.5		—	6	15	—	19	—	22	
		6.0		—	5	13	—	16	—	19	
t_h	Minimum Hold Time	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{REM}	Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	2.0		—	35	100	—	125	—	150	ns
		4.5		—	9	20	—	25	—	30	
		6.0		—	8	17	—	21	—	26	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	47	—	—	—	—	—	pF

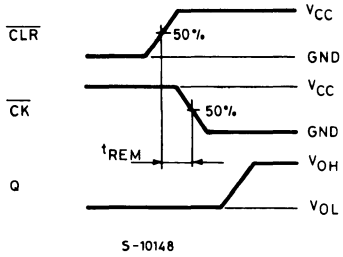
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

TEST CIRCUIT I_{CC} (Opr.)

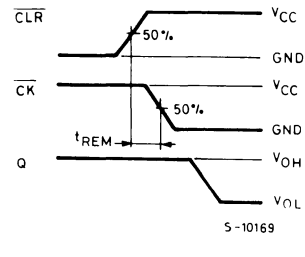


INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

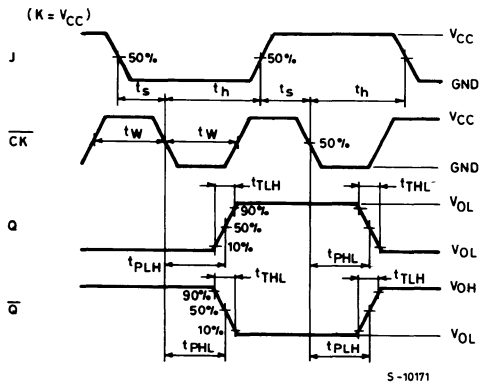
SWITCHING CHARACTERISTICS TEST WAVEFORM



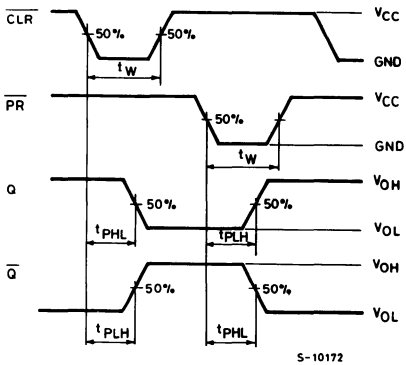
S-10148



S-10169

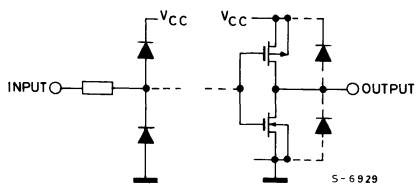


S-10171



S-10172

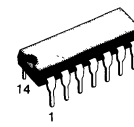
INPUT AND OUTPUT EQUIVALENT CIRCUIT



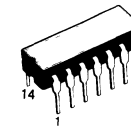
S-6929

4-BIT D-TYPE LATCH

- HIGH SPEED
  t_{PD} = 15 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 2 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS77



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC77 F1
M74HC77 B1N
M74HC77 F1
M74HC77 C1
M74HC77 M1

DESCRIPTION

The M54/74HC77 is a high speed CMOS 4-BIT D-TYPE LATCH fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
It contains two groups of 2-bit latches controlled by an enable input (G1•2 or G3•4). These two latch groups can be used in different circuits.

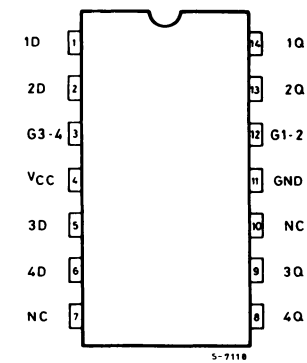
The data applied to the data inputs (1D, 2D, or 3D, 4D) are transfered to the Q outputs (1Q, 2Q, or 3Q, 4Q) respectively when the enable input (G1•2 or G3•4) is taken high. The Q outputs will follow the data inputs as long as the enable input is kept high. When the enable input is taken low, the information data applied to the data inputs is retained at the Q outputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUTS		OUTPUT	FUNCTION
D	G	Q	
L	H	L	—
H	H	H	—
X	L	Q_n	LATCH

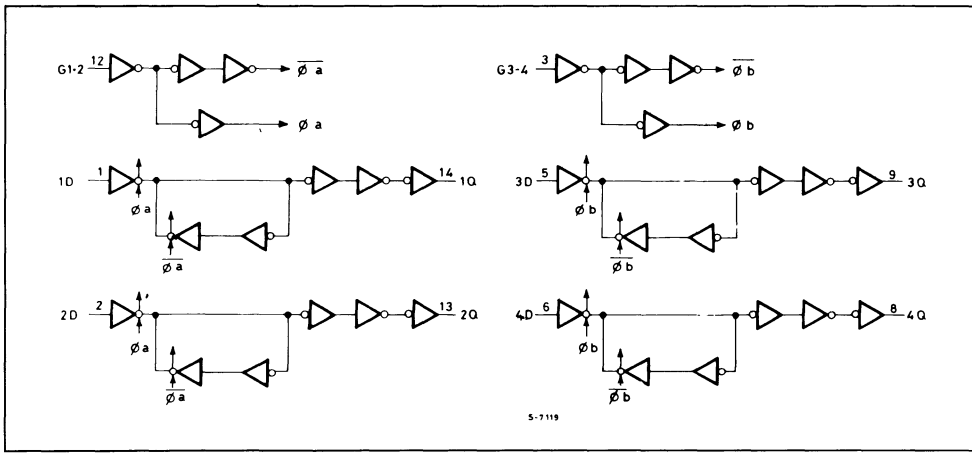
X: DON'T CARE

PIN CONNECTIONS (top view)



FOR CHIP CARRIER
INFORMATION CONTACT SGS-THOMSON

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	2	—	20	—	40	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (DATA-Q)		12	20	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G-Q)		15	25	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

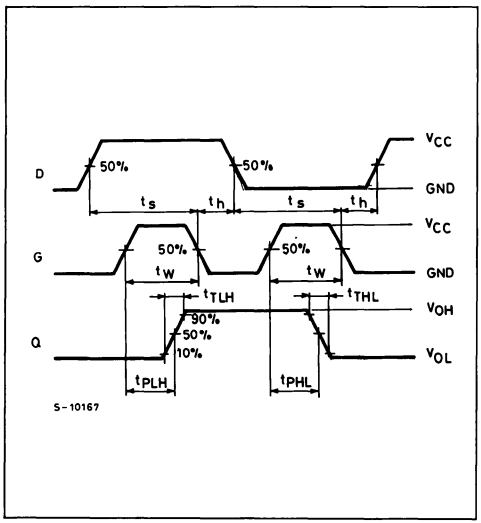
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA-Q)	2.0		—	60	120	—	150	—	180	ns
		4.5		—	15	24	—	30	—	36	
		6.0		—	13	20	—	26	—	31	
t_{PLH} t_{PHL}	Propagation Delay Time (G-Q)	2.0		—	75	145	—	180	—	218	ns
		4.5		—	19	29	—	36	—	44	
		6.0		—	16	25	—	31	—	38	

AC ELECTRICAL CHARACTERISTICS (Continued)

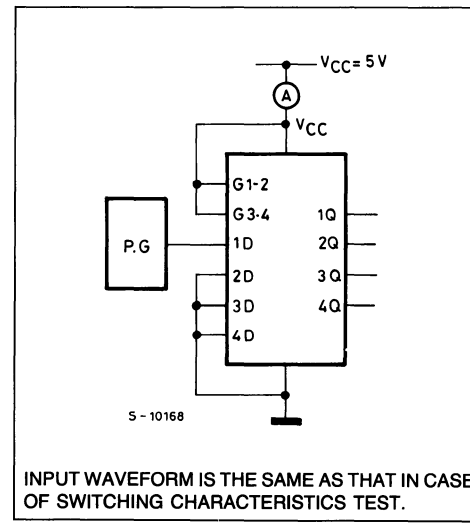
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$t_{W(H)}$	Minimum Pulse Width (G)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-Up Time	2.0		—	5	50	—	65	—	75	ns
		4.5		—	1	10	—	13	—	15	
		6.0		—	1	9	—	11	—	13	
t_h	Minimum Hold Time	2.0		—	—	25	—	30	—	40	ns
		4.5		—	—	5	—	6	—	8	
		6.0		—	—	5	—	6	—	7	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	27	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

SWITCHING CHARACTERISTICS TEST WAVEFORM



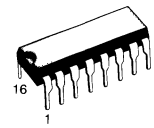
TEST CIRCUIT I_{CC} (Opr.)



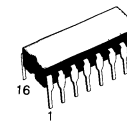
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

4-BIT MAGNITUDE COMPARATOR

- HIGH SPEED
  t_{PD} = 24 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS85



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

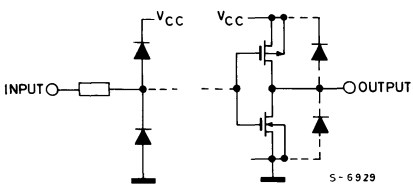
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC85 F1
M74HC85 B1N
M74HC85 F1
M74HC85 C1
M74HC85 M1

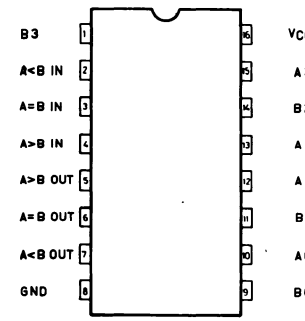
DESCRIPTION

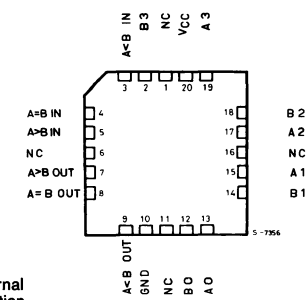
The M54/74HC85 is a high speed CMOS 4-BIT MAGNITUDE COMPARATOR fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This comparator compares two 4-bit words and provides a high voltage level on one of the A > Bout, A = Bout and A < Bout outputs. The comparing bit number is easily expanded by cascading several devices as shown in the typical application. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





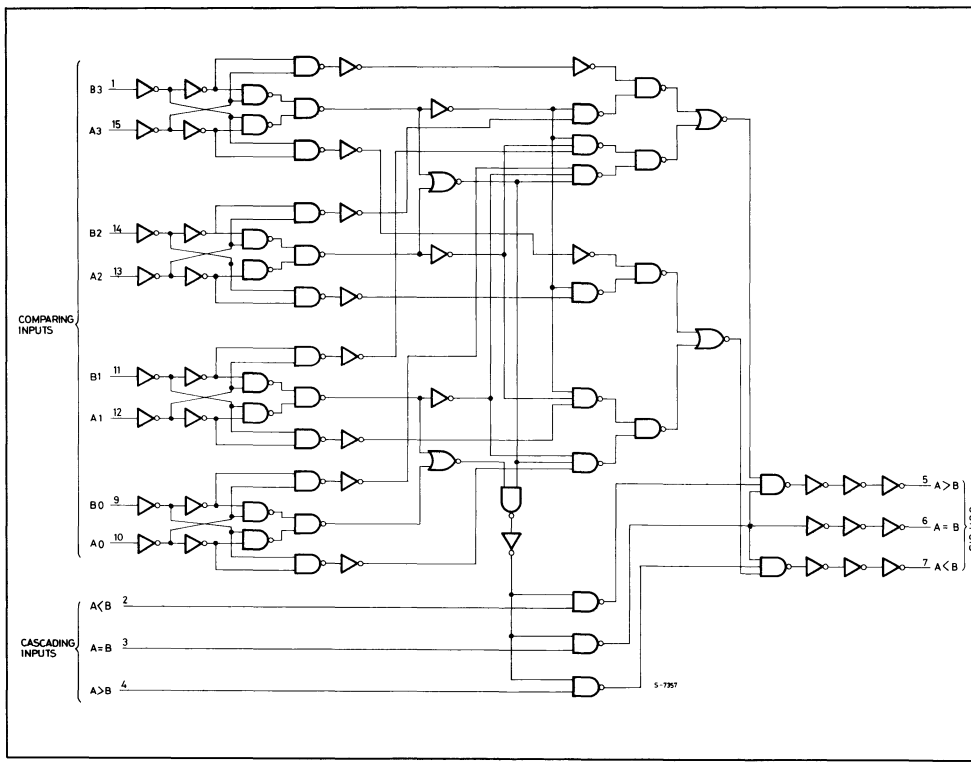
NC =
No Internal
Connection

TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
				A>B	A<B	A=B	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L
				X	X	H	L	L	H
				L	H	L	L	H	L
				H	L	L	H	L	L
				H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3<B3	X	X	X	X	X	X	L	H	L

X: DON'T CARE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0	or		5.9	6.0	—	5.9	—	5.9	—	
		4.5	V_{IL}	−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	

DC SPECIFICATIONS (Continued)

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
			V_I	I_O	Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, - OUT)		26	40	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CASCADE - OUT)		12	20	ns

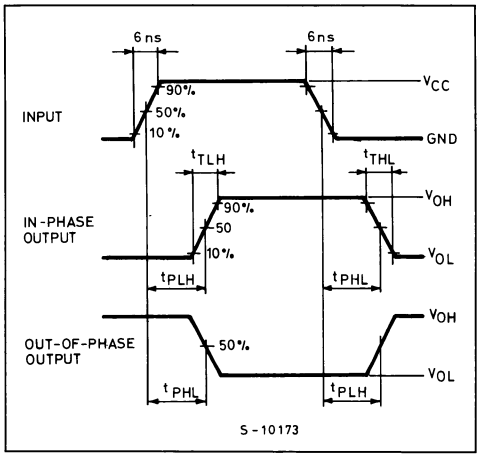
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, - OUT	2.0		—	112	230	—	290	—	345	ns
		4.5		—	28	46	—	58	—	69	
		6.0		—	24	39	—	49	—	59	
t_{PLH} t_{PHL}	Propagation Delay Time (CASCADE-OUT)	2.0		—	60	120	—	150	—	180	ns
		4.5		—	15	24	—	30	—	36	
		6.0		—	13	20	—	26	—	31	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	28	—	—	—	—	—	pF

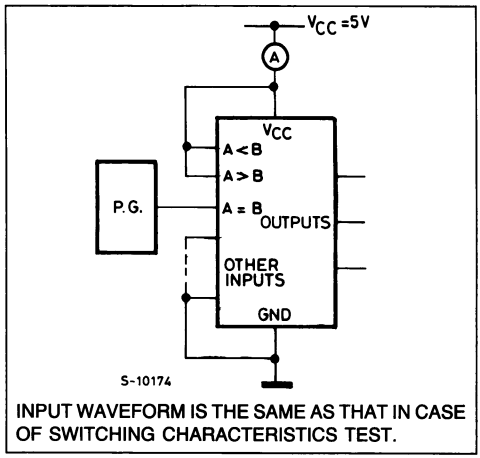
Note (*) C_{PD} is defined as the value of the IC's of internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

Average operating current can be obtained by the following equation: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



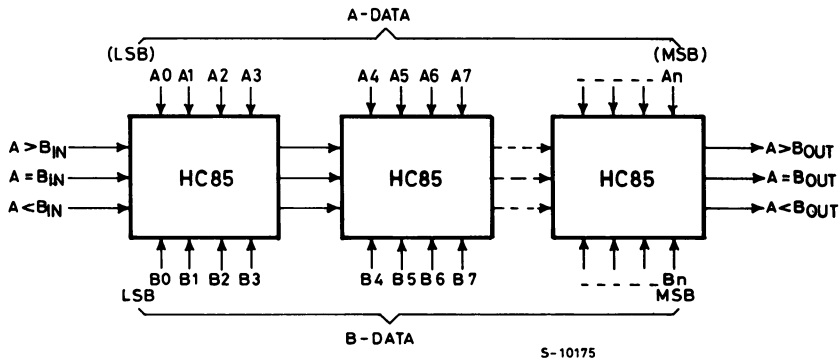
TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TYPICAL APPLICATION

N-BIT CASCADE CONNECTION



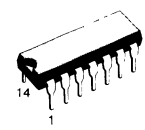
LSB = LOWEST SIGNIFICANT BIT MSB = MOST SIGNIFICANT BIT

COMPARING INPUTS	CASCADING INPUTS			OUTPUTS		
	A>B	A=B	A<B	A>B	A=B	A<B
(A)>(B)	X	X	X	H	L	L
(A)=(B)	H	L	L	H	L	L
	X	H	X	L	H	L
	L	L	H	L	L	H
(A)<(B)	X	X	X	L	L	H

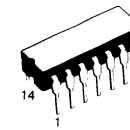
X: DON'T CARE

QUAD EXCLUSIVE OR GATE

- HIGH SPEED
  t_{PD} = 13 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS86



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

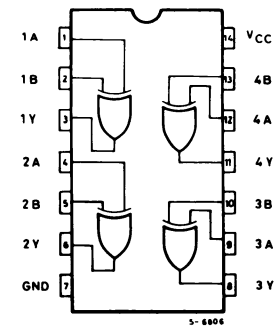
C1
Plastic Chip Carrier

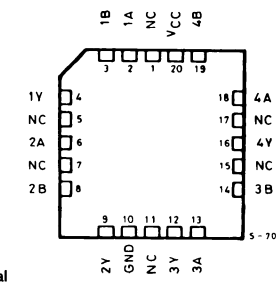
ORDERING NUMBERS:
M54HC86 F1
M74HC86 B1N
M74HC86 F1
M74HC86 C1
M74HC86 M1

DESCRIPTION

The M54/74HC86 is a high speed CMOS QUAD EXCLUSIVE OR GATE fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. Input and output buffer are installed, which enables high noise immunity and stable output.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

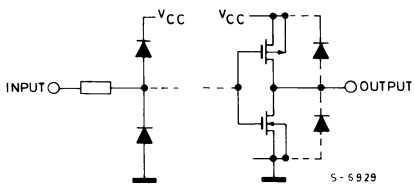
PIN CONNECTIONS (top view)



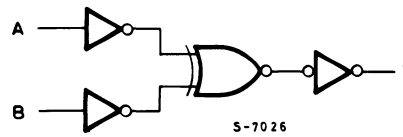


NC =
No Internal
Connection

INPUT AND OUTPUT EQUIVALENT CIRCUIT



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

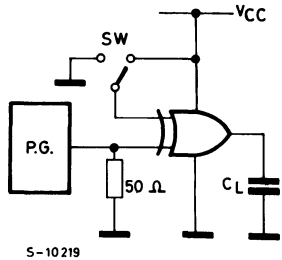
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		12	20	ns

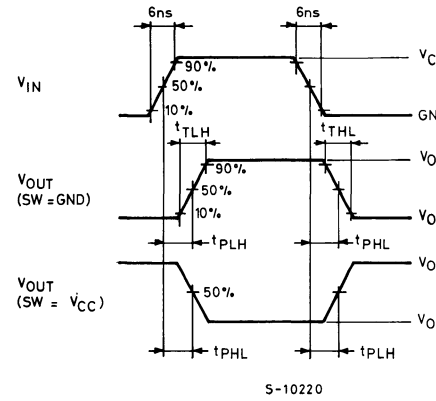
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			-40 to $85°C$ 74HC		-55 to $125°C$ 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	64	120	—	150	—	180	ns
		4.5		—	16	24	—	30	—	36	
		6.0		—	14	20	—	26	—	31	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	34	—	—	—	—	—	pF

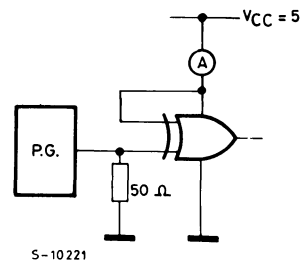
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate).

SWITCHING CHARACTERISTICS TEST CIRCUIT





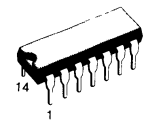
TEST CIRCUIT I_{CC} (Opr)



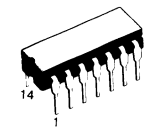
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

DUAL J-K FLIP FLOP WITH CLEAR

- HIGH SPEED
  f_{MAX} = 58 MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 2 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS107



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
SO Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC107 F1
M74HC107 B1N
M74HC107 F1
M74HC107 C1
M74HC107 M1

DESCRIPTION

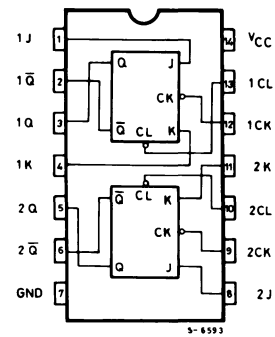
The M54/74HC107 is a high speed CMOS DUAL J-K FLIP-FLOP fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. These flip-flop are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each one has independent J, K, CLOCK, and CLEAR inputs and Q and $\overline{Q}$ outputs. CLEAR is independent of the clock and accomplished by a logic low on the input. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

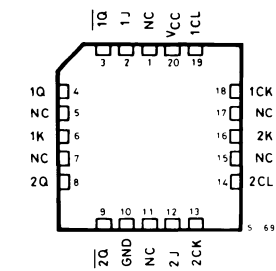
TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{CLEAR}$	$\overline{CLOCK}$	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	NO CHANGE	
H	↓	L	H	L	H
H	↓	H	L	H	L
H	↓	H	H	TOGGLE	
H	↑	X	X	NO CHANGE	

X: DON'T CARE

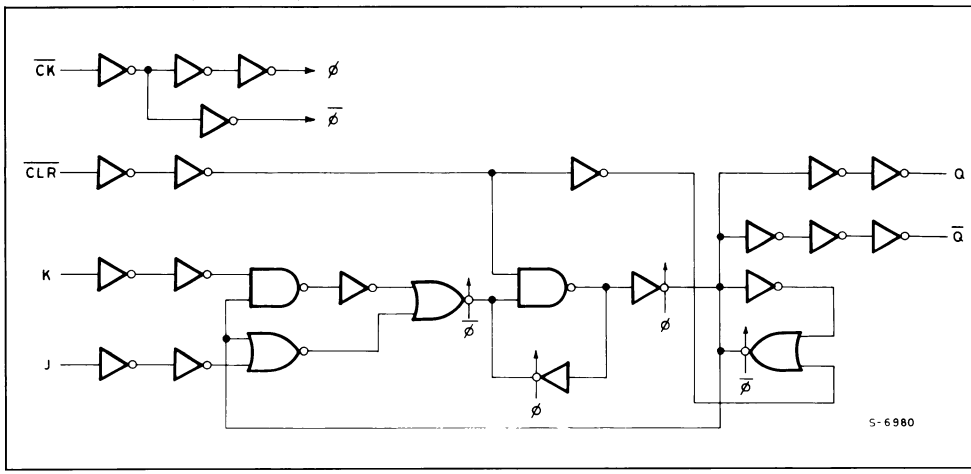
PIN CONNECTIONS (top view)





NC = No Internal Connection

LOGIC DIAGRAM (1/2 Package)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

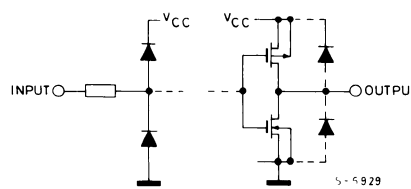
DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0	or		5.9	6.0	—	5.9	—	5.9	—	
		4.5	V_{IL}	−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0	or		—	0	0.1	—	0.1	—	0.1	
		4.5	V_{IL}	4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	2	—	20	—	40	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Q, $\overline{Q}$)		18	29	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$-Q, $\overline{Q}$)		24	36	ns
f_{MAX}	Maximum Clock Frequency	34	58		MHz

INPUT AND OUTPUT EQUIVALENT CIRCUIT

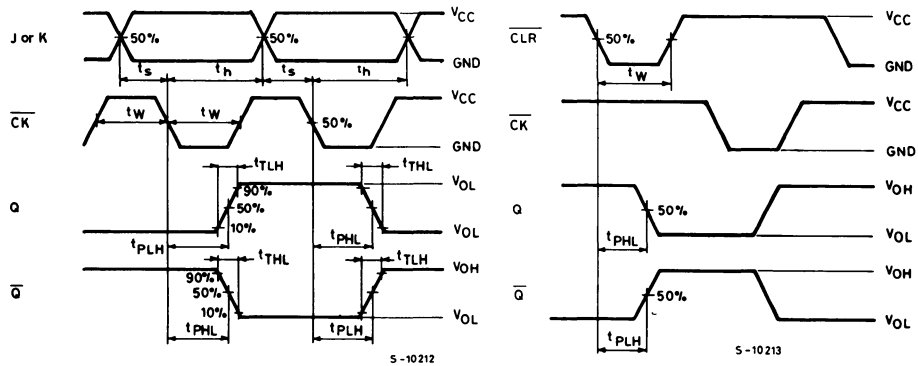


AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

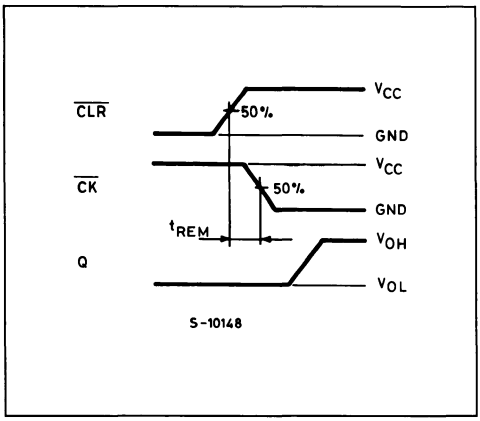
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			-40 to $85°C$ 74HC		-55 to $125°C$ 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOCK}$-Q, $\overline{Q}$)	2.0		—	77	165	—	205	—	250	ns
		4.5		—	21	33	—	41	—	50	
		6.0		—	18	28	—	35	—	43	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$-Q, $\overline{Q}$)	2.0		—	116	220	—	275	—	330	ns
		4.5		—	29	44	—	55	—	66	
		6.0		—	25	37	—	47	—	56	
f_{MAX}	Maximum Clock Frequency	2.0		6	14	—	4.8	—	4.0	—	MHz
		4.5		30	50	—	24	—	20	—	
		6.0		35	58	—	28	—	24	—	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLEAR}$)	2.0		—	40	100	—	125	—	150	ns
		4.5		—	10	20	—	25	—	30	
		6.0		—	9	17	—	21	—	26	
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width ($\overline{CLOCK}$)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-Up Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_h	Minimum Hold Time	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{rem}	Minimum Removal Time ($\overline{CLEAR}$)	2.0		—	—	25	—	30	—	40	ns
		4.5		—	—	5	—	6	—	8	
		6.0		—	—	5	—	6	—	7	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	46	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the following equation.
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ per F/F

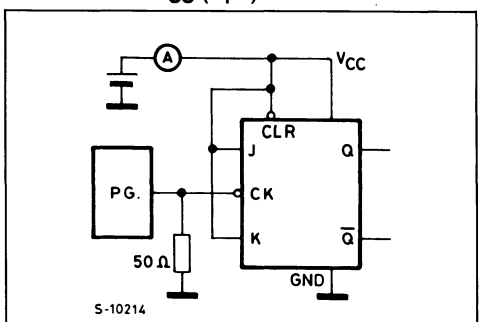
SWITCHING CHARACTERISTICS TEST WAVEFORM



SWITCHING CHARACTERISTICS TEST WAVEFORMS



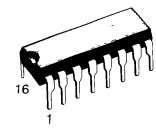
TEST CIRCUIT I_{CC} (Opr.)



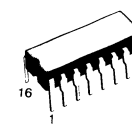
TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

DUAL J-$\overline{K}$ FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED
  f_{MAX} = 60 MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 2 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS109



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC109 F1
M74HC109 B1N
M74HC109 F1
M74HC109 C1
M74HC109 M1

DESCRIPTION

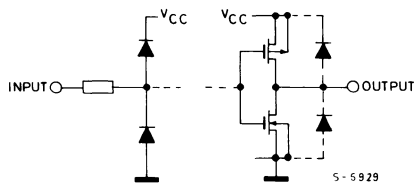
The M54/74HC109 is a high speed CMOS DUAL J-$\overline{K}$ FLIP-FLOP WITH PRESET AND CLEAR fabricated in silicon gate C²MOS technology.

It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

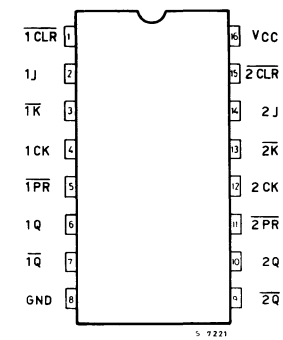
In accordance with the logic level on the J and $\overline{K}$ input is device changes state on positive going transitions of the clock pulse. CLEAR and PRESET are independent of the clock and accomplished by a low logic level on the corrisponding input.

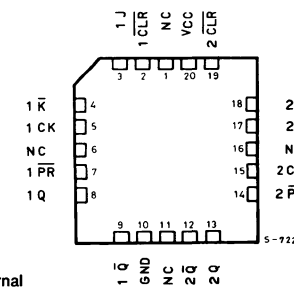
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





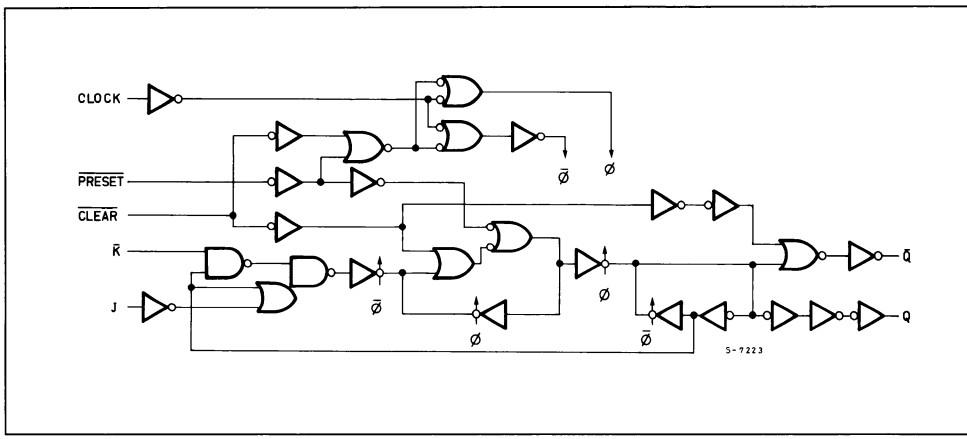
NC =
No Internal
Connection

TRUTH TABLE

INPUTS					OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	J	$\overline{K}$	CK	Q	$\overline{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	H	↑	Qn	$\overline{Q}$n	NO CHANGE
H	H	L	L	↑	L	H	
H	H	H	H	↑	H	L	
H	H	H	L	↑	$\overline{Q}$n	Qn	TOGGLE
H	H	X	X	↓	Qn	$\overline{Q}$n	NO CHANGE

X: DON'T CARE

LOGIC DIAGRAM (1/2 package)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V 4.5V 6 V	0 to 1000 0 to 500 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0 4.5 6.0	V_I V_{IH} or V_{IL}	I_O −20 μA	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	1.9 4.4 5.9	— — —	V
		4.5 6.0		−4.0 mA −5.2 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	
V_{OL}	Low Level Output Voltage	2.0 4.5 6.0	V_{IH} or V_{IL}	20 μA	— — —	0 0 0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
		4.5 6.0		4.0 mA 5.2 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND		—	—	2	—	20	—	40	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

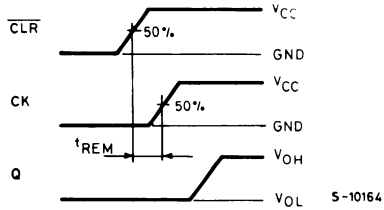
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Q, $\overline{Q}$)		18	29	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$-Q, $\overline{PR}$-Q, $\overline{Q}$)		21	33	ns
f_{MAX}	Maximum Clock Frequency	33	63		MHz

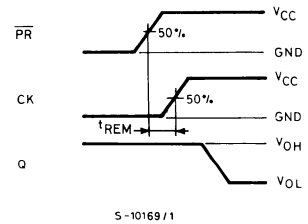
AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

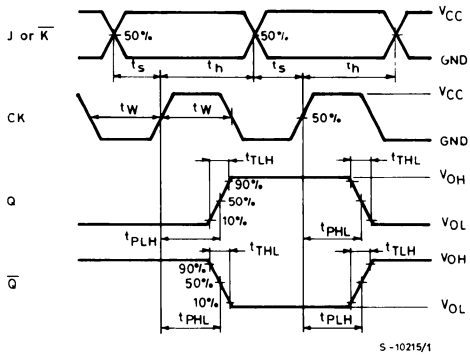
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Q, $\overline{Q}$)	2.0 4.5 6.0		— — —	80 21 18	165 33 28	— — —	205 41 35	— — —	250 50 43	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$-Q, $\overline{Q}$)	2.0 4.5 6.0		— — —	90 24 21	190 38 32	— — —	240 48 41	— — —	285 57 48	ns
f_{MAX}	Maximum Clock Frequency	2.0 4.5 6.0		6 30 35	15 57 67	— — —	4.8 24 28	— — —	4 20 28	— — —	MHz
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CLOCK)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_s	Minimum Set-Up Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_h	Minimum Hold Time	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
t_{REM}	Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	2.0 4.5 6.0		— — —	40 10 9	100 20 17	— — —	125 25 21	— — —	150 30 26	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	47	—	—	—	—	—	pF

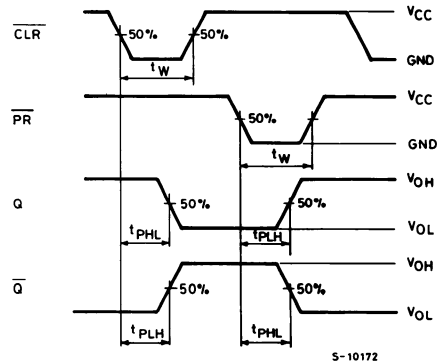
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following equation I_{CC} (Opr.) = $C_{PD} \cdot V_{CC} \cdot f_{IN} \cdot I_{CC}/2$ (per FF)

SWITCHING CHARACTERISTICS TEST WAVEFORM

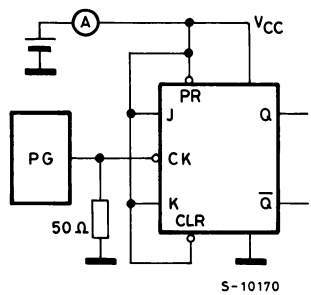








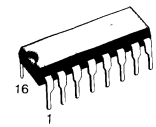
TEST CIRCUIT I_{CC} (Opr.)



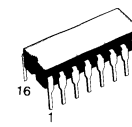
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

DUAL J-K FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED
  f_{MAX} = 59 MHz (Typ.) at V_{CC} = 5V
  LOW POWER DISSIPATION
  I_{CC} = 2 μA at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DEALYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS112



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

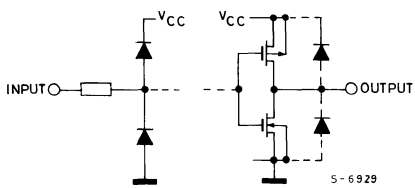
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC112 F1
M74HC112 B1N
M74HC112 F1
M74HC112 C1
M74HC112 M1

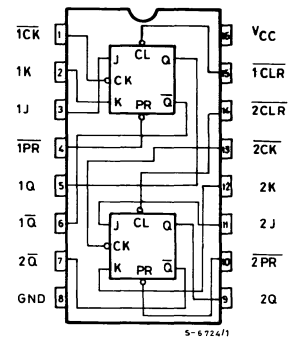
DESCRIPTION

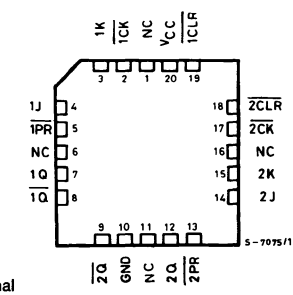
The M54/74HC112 is a high speed CMOS DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The M54HC112/M74HC112 dual JK flip-flop features individual J, K, clock, and asynchronous set and clear inputs for each flip-flop. When the clock goes high, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is high and the bistable will function as shown in the truth table. Input data is transferred to the input on the negative going edge of the clock pulse. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





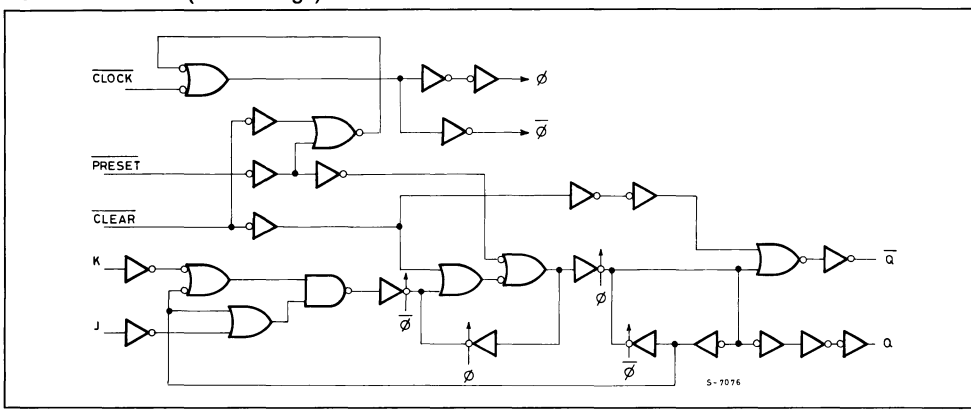
NC = No Internal Connection

TRUTH TABLE

INPUTS					OUTPUT		FUNCTION
$\overline{CLR}$	$\overline{PR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	L	↓	Qn	$\overline{Qn}$	NO CHANGE
H	H	H	L	↓	L	H	
H	H	L	H	↓	H	L	
H	H	H	H	↓	$\overline{Qn}$	Qn	TOGGLE
H	H	X	X	↑	Qn	$\overline{Qn}$	NO CHANGE

X: DON'T CARE

LOGIC DIAGRAM (1/2 Package)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V: 0 to 1000 V_{CC} = 4.5V: 0 to 500 V_{CC} = 6 V: 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1,35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND		—	—	2	—	20	—	40	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input t_r = t_f = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOCK}$-Q, $\overline{Q}$)		16	25	ns
t_{PLH}	Propagation Delay Time $\overline{PR}$, $\overline{CLEAR}$ - Q, $\overline{Q}$		20	31	ns
f_{MAX}	Maximum Clock Frequency	33	58		MHz

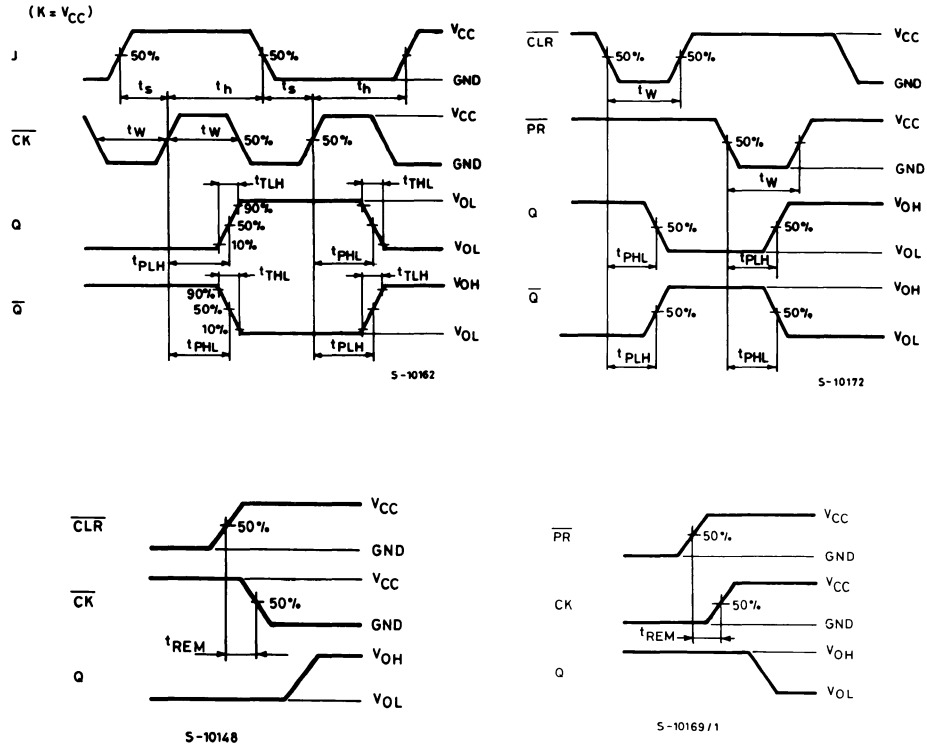
AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	22	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Q, $\overline{Q}$)	2.0		—	76	150	—	190		225	ns
		4.5		—	19	30	—	38		45	
		6.0		—	16	26	—	33		38	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{PR}$, $\overline{CLR}$-Q, $\overline{Q}$)	2.0		—	92	180	—	225		270	ns
		4.5		—	23	36	—	45		54	
		6.0		—	20	31	—	38		46	
f_{MAX}	Maximum Clock Frequency	2.0		6	13	—	4.8	—	4.0	—	MHz
		4.5		30	53	—	24	—	20	—	
		6.0		35	62	—	28	—	24	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
$t_{W(H)}$	Minimum Pulse Width $\overline{CLEAR}$ $\overline{PRESET}$	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_s	Minimum Set-up Time J, K	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_h	Minimum Hold Time J, K	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{REM}	Minimum Removal Time ($\overline{CLEAR}$, $\overline{PRESET}$)	2.0		—	40	100	—	125	—	150	ns
		4.5		—	10	20	—	25	—	30	
		6.0		—	9	17	—	21	—	26	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	54	—	—	—			pF

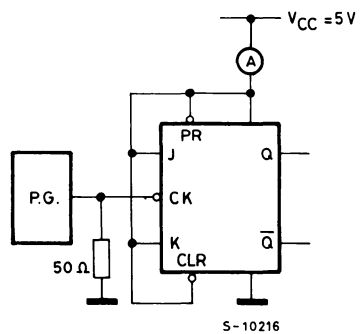
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained the following equation:
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (for 1 Flip/Flop).

SWITCHING CHARACTERISTICS TEST WAVEFORM



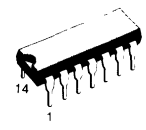
TEST CIRCUIT I_{CC} (Opr.)



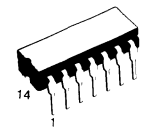
INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

DUAL J-K FLIP FLOP WITH PRESET

- HIGH SPEED
  f_{MAX} = 64 MHz (Typ.) at V_{CC} = 5V
  LOW POWER DISSIPATION
  I_{CC} = 2 μA at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS113



B1N
Plastic Package



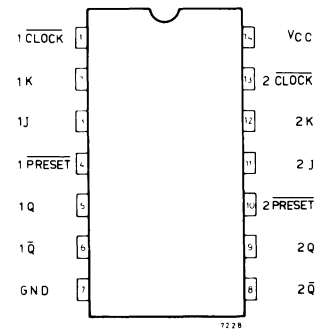
F1
Ceramic Frit Seal Package

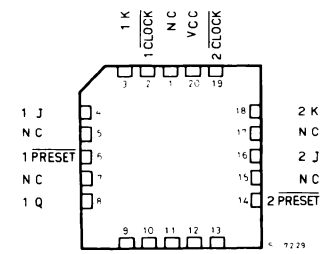
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC113 F1
M74HC113 B1N
M74HC113 F1
M74HC113 C1
M74HC113 M1

PIN CONNECTIONS (top view)





NC = No Internal Connection

DESCRIPTION

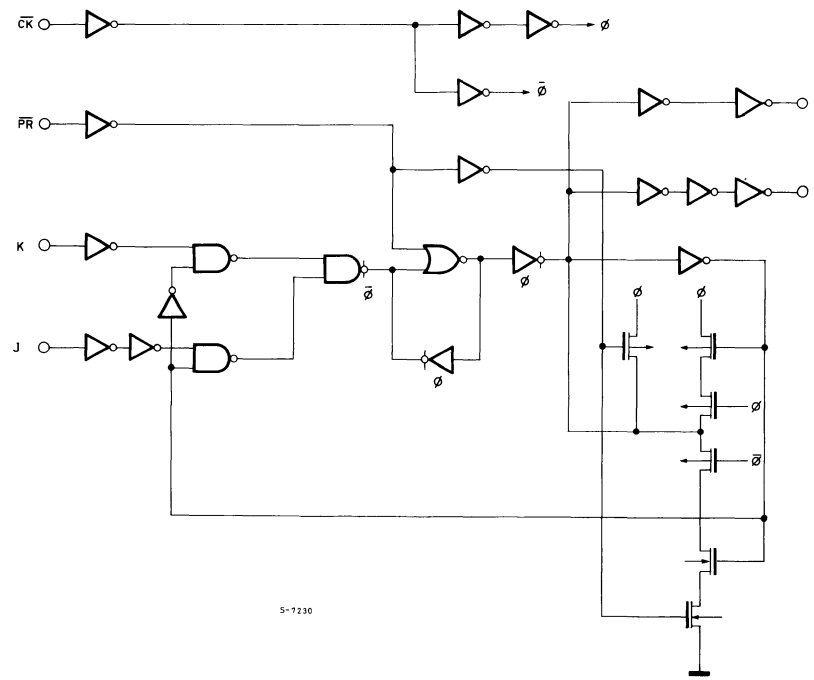
The M54/74HC113 is a high speed CMOS DUAL J-K FLIP FLOP WITH PRESET fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This circuit offers individual J, K, set, and clock inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will function as shown in the thruth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUTS				OUTPUT		FUNCTION
$\overline{PR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	X	X	X	H	L	PRESET
H	L	L	↓	Qn	$\overline{Qn}$	NO CHANGE
H	L	H	↓	L	H	
H	H	L	↓	H	L	
H	H	H	↓	$\overline{Qn}$	Qn	TOGGLE
H	X	X	↑	Qn	$\overline{Qn}$	NO CHANGE

X: DON'T CARE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

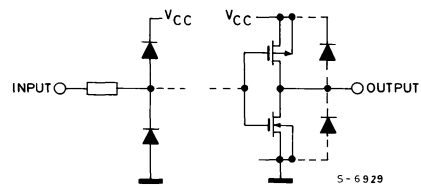
(*) 500 mW = 65° derate to 10 mW/°C from 65°C to 85°C for plastic package

(*) 500 mW = 65° derate to 12 mW/°C from 100 to 125°C for frit-seal package

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series Operating Temperature 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0.0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	2	—	20	—	40	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOCK}$-Q, $\overline{Q}$)		14	23	ns
t_{PHL}	Propagation Delay Time ($\overline{PRESET}$-Q, $\overline{Q}$)		17	27	ns
f_{MAX}	Maximum Clock Frequency	35	64		MHz

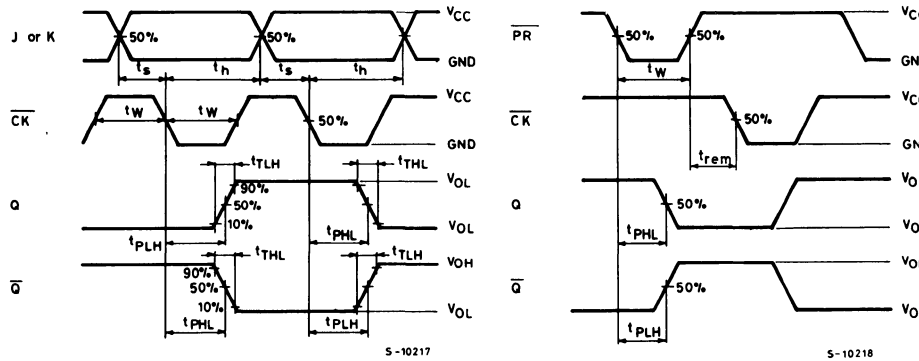
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOCK}$-Q, $\overline{Q}$)	2.0 4.5 6.0		— — —	68 17 14	135 27 23	— — —	170 34 29		205 41 35	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{PRESET}$-Q, $\overline{Q}$)	2.0 4.5 6.0		— — —	80 20 17	160 32 27	— — —	200 40 34		240 48 41	ns
f_{MAX}	Maximum Clock Frequency	2.0 4.5 6.0		6.4 32 38	15 58 68	— — —	5.2 26 31	— — —	4.2 21 25	— — —	MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width ($\overline{CLOCK}$)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
$t_{W(L)}$	Minimum Pulse Width $\overline{PRESET}$	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t_s	Minimum Set-up Time J, K	2.0 4.5 6.0		— — —	25 5 4	75 15 13	— — —	95 19 16		110 22 19	ns
t_h	Minimum Hold Time J, K	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
t_{REM}	Minimum Removal Time ($\overline{PRESET}$)	2.0 4.5 6.0		— — —	0 0 0	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	38	—	—	—			pF

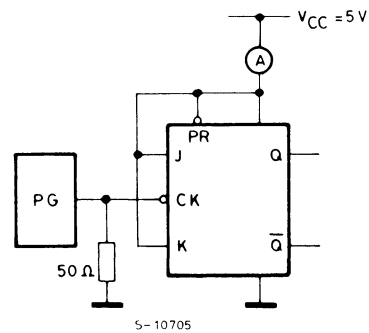
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation:
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (for 1 Flip/Flop).

SWITCHING CHARACTERISTICS TEST WAVEFORM



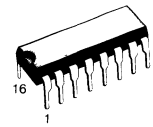
TEST CIRCUIT I_{CC} (Opr.)



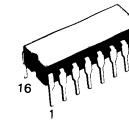
INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

- HIGH SPEED
  t_{PD} = 28 ns (TYP) at V_{CC} = 5V
- LOW POWER DISSIPATION
  STANDBY STATE I_{CC} = 4 μA (MAX.) at T_A = 25°C
  ACTIVE STATE I_{CC} = 200 μA (TYP) at V_{CC} = 5V
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- WIDE OUTPUT PULSE WIDTH RANGE
  t_{WOUT} = 120ns ~ 60s over at V_{CC} = 4.5V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS123



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC123 F1
M74HC123 B1N
M74HC123 F1
M74HC123 C1
M74HC123 M1

DESCRIPTION

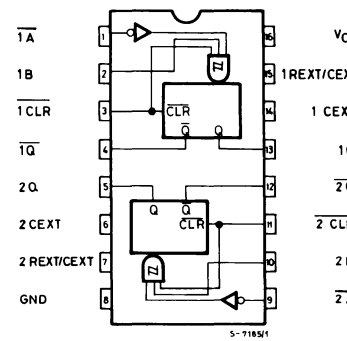
The M54/74HC123 is a high speed CMOS MONOSTABLE multivibrator fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. There are two trigger inputs, $\overline{A}$ INPUT (negative edge) and 8 INPUT (positive edge). These inputs are valid for rising/falling signals, (t_r-t_f-l sec).
The device may also be triggered by using the CLR input (positive-edge) because of the Schmitt-trigger input; after triggering the output maintains the MONOSTABLE state for the time period determined by the external resistor Rx and capacitor Cx. Taking $\overline{CLR}$ low breaks this MONOSTABLE STATE. If the next trigger pulse occurs during the MONOSTABLE period it makes the MONOSTABLE period longer. Limit for values of Cx and Rx:

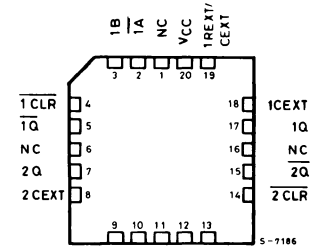
Cx: NO LIMIT

Rx: V_{CC} = 2.0V 5KΩ to 1MΩ
V_{CC} = 3.0V 1KΩ to 1MΩ

All inputs are equipped with protection circuits against static discharge and transient excess voltage

PIN CONNECTIONS (top view)





NC = No Internal Connection

TRUTH TABLE

INPUTS			OUTPUTS		NOTE
$\overline{A}$	B	$\overline{CL}$	Q	$\overline{Q}$	
⊓↓	H	H	⊓	⊔	OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	↓⊓	H	⊓	⊔	OUTPUT ENABLE
L	H	↓⊓	⊓	⊔	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

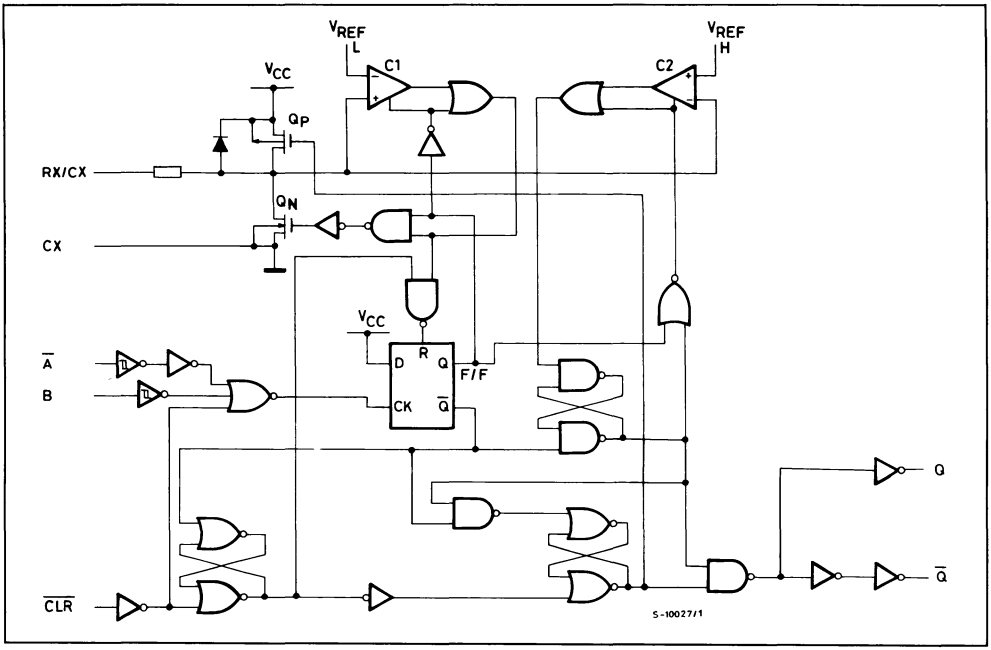
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

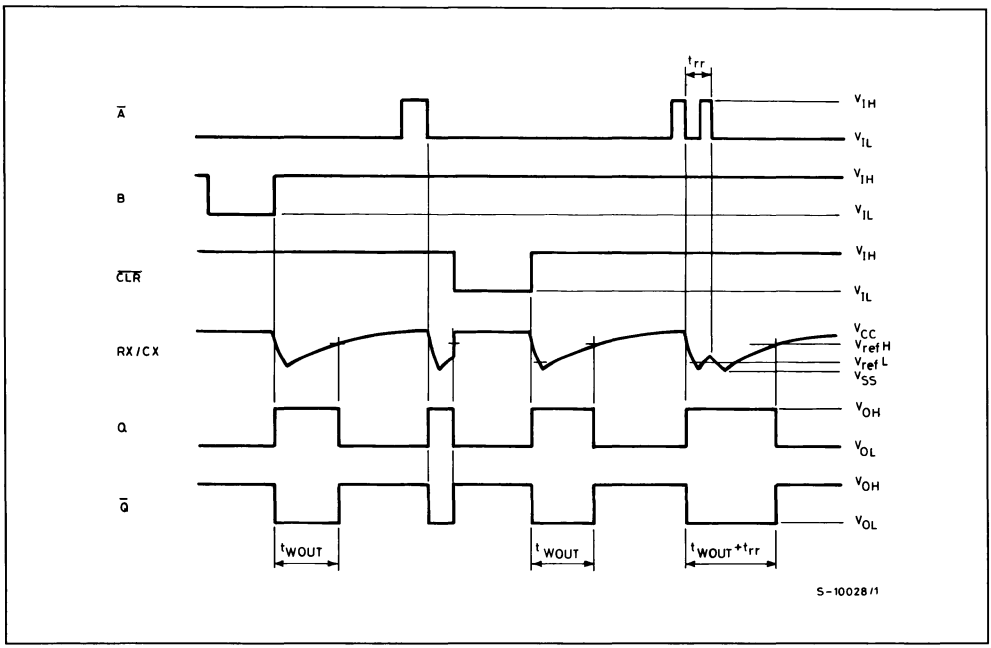
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time ($\overline{CLR}$ only)	V_{CC}	2 V: 0 to 1000 4.5V: 0 to 500 6 V: 0 to 400	ns
Cx	External Capacitor	NO LIMITATION		
Rx	External Resistor	V_{CC}	3 V: 5K to 1M 3 V: 1K to 1M	Ω

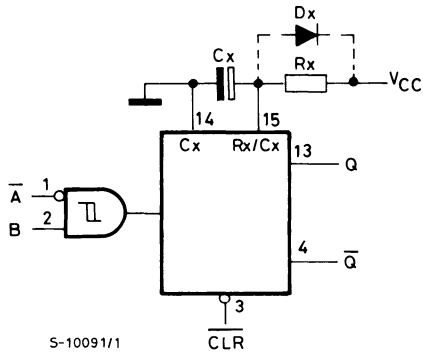
SYSTEM DIAGRAM

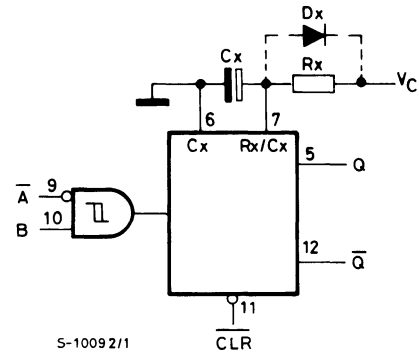


TIMING CHART



BLOCK DIAGRAM





Note:
(1) Cx, Rx, Dx are external components.
(2) Dx is a clamping diode

The external capacitor is charged to V_{CC} in the stand-by state, i.e. no trigger. When the supply voltage is turned off Cx is discharged mainly through an internal parasitic diode (see figures). If Cx is sufficiently large and V_{CC} decreases rapidy, there will be some possibility of damaging the I.C. with a surge current or latch-up. If the voltage supply filter capacitor is large enough and V_{CC} decrease slowly, the surge current is automatically limited and damage the I.C. is avoided. The maximum forward current of the parasitic diode is approximately 20 mA. In cases where Cx is large the time taken for the supply voltage to fall to 0.4 V_{CC} can be calculated as follows:

$t_f \geqq (V_{CC} - 0.7) \cdot Cx/20mA$

In cases where t_f is too short an external clamping diode is required to protect the I.C. from the surge current.

FUNCTIONAL DESCRIPTION

Stand-by state

The external capacitor, Cx, is fully charged to V_{CC} in the stand-by state. Hence, before triggering, transistor Qp and Qn (connected to the Rx/Cx node) are both turned off. The two comparators that control the timing and the two reference voltage sources stop operating. The total supply current is therefore only leakage current.

Trigger operation

Triggering occurs when:

1 st) A is "low" and B has a falling edge;
2 nd) B is "high" and A has a rising edge;
3 rd) A is low and B is high and C1 has a rising edge.

After the multivibrator has been retriggered comparator C1 and C2 start operating and Qn is turned on. Cx then discharges through Qn. The voltage at the node R/C external falls.

When it reaches V_{REFL} the output of comparator C1 becomes low. This in turn resets the flip-flop and Qn is turned off.
At this point C1 stops functioning but C2 continues to operate.
The voltage at R/C external begins to rise with a time constant set by the external components Rx, Cx.
Triggering the multivibrator causes Q to go high after internal delay due to the flip-flop and the gate. Q remains high until the voltage at R/C external rises again to V_{REFH}. At this point C 2 output goes low and O goes low. C 2 stops operating. That means that after triggering when the voltage R/C external returns to V_{REFH} the multivibrator has returned to its MONOSTABLE STATE. In the case where Rx • Cx are large enough and the discharge time of the capacitor and the delay time in the I.C. can be ignored, the width of the output pulse tw (out) is as follows:

$$t_{W(OUT)} = 0.46\ Cx \cdot Rx$$

FUNCTIONAL DESCRIPTION (Continued)

Re-trigger operation

When a second trigger pulse follows the first its effect will depend on the state of the multivibrator. If the capacitor Cx is being charged the voltage level of R/C external falls to Vrefl again and Q remains high i.e. the retrigger pulse arrives in a time shorter than the period Rx • Cx seconds, the capacitor charging time constant. If the second trigger pulse is very close to the initial trigger pulse it is ineffective; i.e., the second trigger must arrive in the capacitor discharge cycle to be ineffective. Hence the minimum time for a second trigger to be effective depends on V_{CC} and Cx.

Reset operation

CL is normally high. If CL is low, the trigger is not effective because Q output goes low and trigger control flip-flop is reset.

Also transistor Op is turned on and Cx is charged quicky to V_{CC}. This means if CL input goes low, the IC becomes waiting state both in operating and non operating state.

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage (Q, $\overline{Q}$ Output)	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	$V_I =$ V_{IH} or V_{IL}	$I_{OH} = -20\mu A$	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		$I_{OH} = -4mA$	4.18	4.31	—	4.13	—	4.10	—	
		6.0		$I_{OH} = -5.2mA$	3.68	5.80	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage (Q, $\overline{Q}$ Output)	2.0	$V_I =$ V_{IH} or V_{IL}	$I_{OL} = 20\ \mu A$	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		$I_{OL} = 4$ mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		$I_{OL} = 5.2$ mA	—	0.18	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{IN}	R/C Terminal Off-State Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA
I_{CC}'	Active State (1) Supply Current	2.0	$V_I = V_{CC}$ or GND Pins 2, 14 $V_{IN} = V_{CC/2}$		—	40	120	—	160	—	200	μA
		4.5			—	0.1	0.3	—	0.4	—	0.5	mA
		6.0			—	0.2	0.6	—	0.8	—	1.0	mA

(1): Per Circuit

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{A}$, B - Q, $\overline{Q}$)		27	41	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$, TRIGGER - Q, $\overline{Q}$)		29	45	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$ - Q, Q)		21	33	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{A}$, B - Q, $\overline{Q}$)	2.0 4.5 6.0		— — —	124 31 26	240 48 41	— — —	300 60 51	— — —	360 72 61	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$ TRIG - Q, Q)	2.0 4.5 6.0		— — —	136 34 29	265 53 45	— — —	335 66 56	— — —	400 80 68	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$ - Q, $\overline{Q}$)	2.0 4.5 6.0		— — —	100 25 21	195 39 33	— — —	245 49 42	— — —	295 59 50	ns
t_{rr}	Minimum Retrigger Time	4.5 6.0	Cx = 100pF Rx = 1KΩ	— —	70 60	— —	— —	— —	— —	— —	ns
		4.5 6.0	Cx = 0.01μF Rx = 1KΩ	— —	1.0 0.9	— —	— —	— —	— —	— —	μs
Δt_{WOUT}	Output Pulse Width Error Between Circuits in Same Package			—	±1	—	—	—	—	—	%
t_{WOUT} (Min)	Output Pulse Width	4.5	Cx = 0 Rx = 1kΩ	—	118	—	—	—	—	—	ns
t_{WOUT}	Output Pulse Width	4.5	Cx = 100pF Rx = 10kΩ	—	1.0	—	—	—	—	—	μs
		4.5	Cx = 0.1μ Rx = 100kΩ	—	4.7	—	—	—	—	—	ms

AC ELECTRICAL CHARACTERISTICS (Continued)

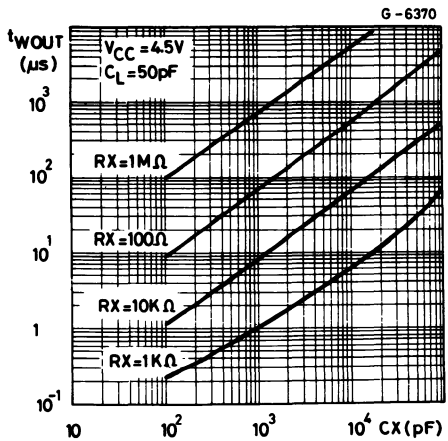
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (Trigger)	2.0		—	40	100	—	125	—	150	ns
		4.5		—	10	20	—	25	—	30	
		6.0		—	9	17	—	21	—	26	
$t_{W(L)}$	Minimum Clear Pulse Width	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	113	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value the IC's of internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}' \cdot Duty/100 + I_{CC}/2$ (per monostable)

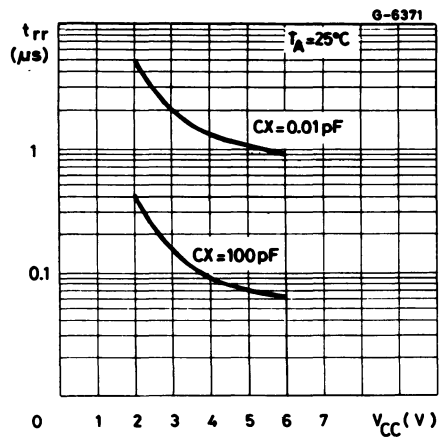
(I_{CC}': Active Supply Current)

(Duty: %)

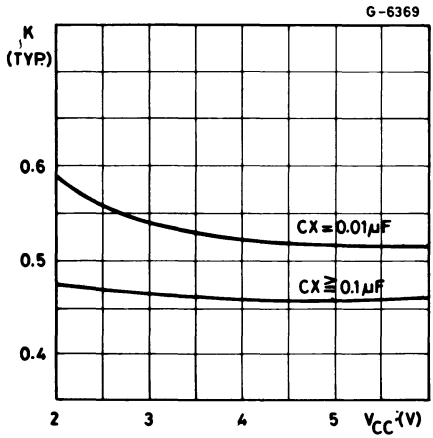
t_{WOUT} - Cx Characteristics (Typ)



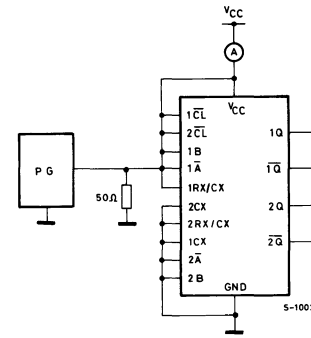
t_{rr} - V_{CC} Characteristics (Typ)



Output Pulse Width Constant,
K-Supply Voltage Rx≥ 10kΩ

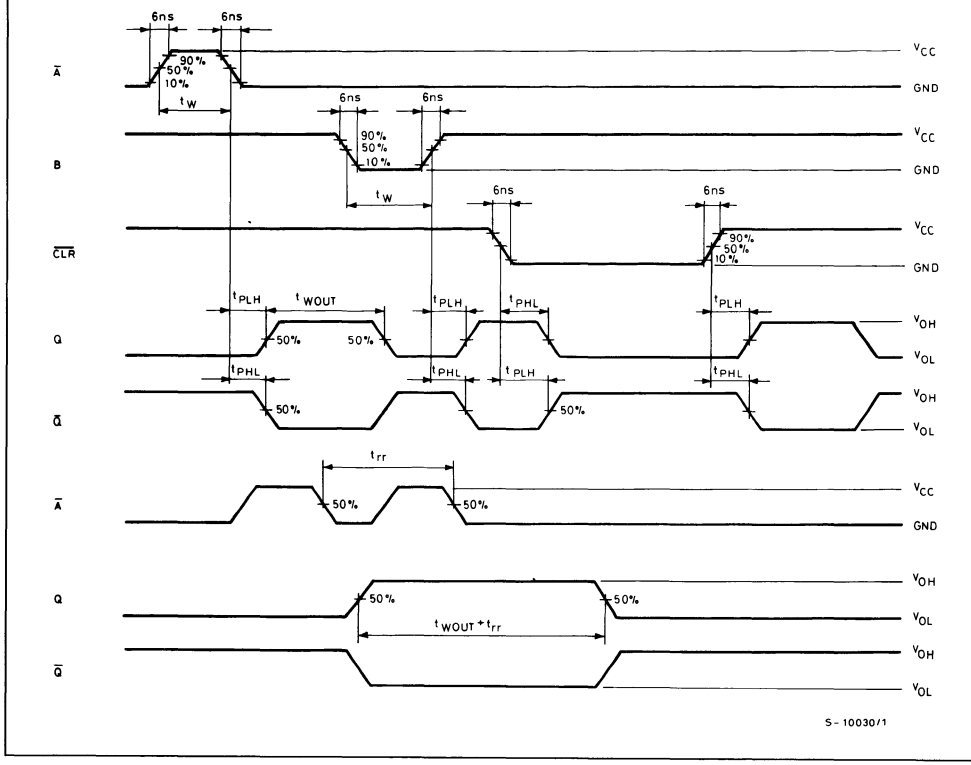


TEST CIRCUIT I_{CC} (Opr)



TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN SASE OF SWITCHING CHARACTERISTICS TESTS.

SWITCHING CHARACTERISTICS TEST WAVEFORM

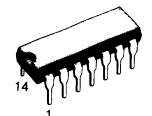


SGS-THOMSON MICROELECTRONICS

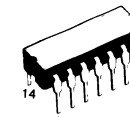
M54/74HC125
M54/74HC126

QUAD BUS BUFFERS (3-STATE)

- HIGH SPEED
  t_{PD} = 10 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS125/126



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX C1
M74HCXXX M1

DESCRIPTION

The M54/74HC125 and the M54/74HC126 are high speed CMOS QUAD BUS BUFFERS (3-STATE) fabricated in silicon gate C²MOS technology.
They have the same high speed performance of LSTTL combined with true CMOS low power consumption.
These devices require the 3-STATE control input G to be taken high to make the output go into the high impedance state.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

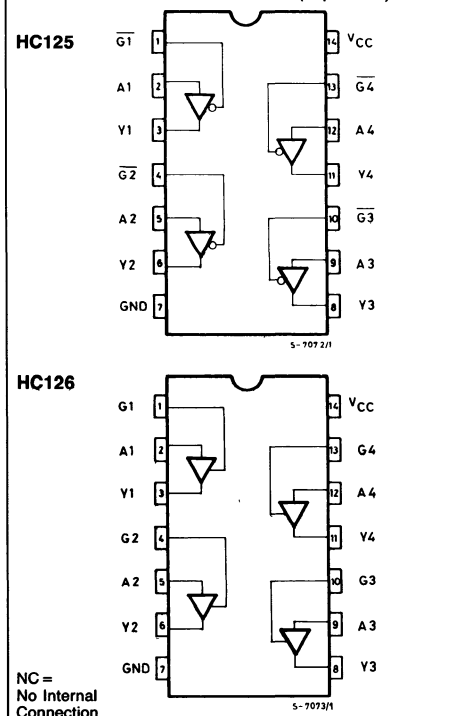
TRUTH TABLES

HC 125		
INPUTS		OUTPUT
A	$\overline{G}$	Y
X	H	Z
L	L	L
H	L	H

HC126		
INPUTS		OUTPUT
A	G	Y
X	L	Z
L	H	L
H	H	H

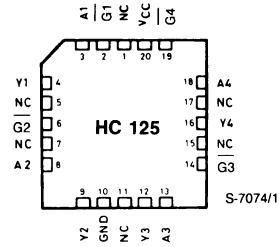
X: DON'T CARE Z: HIGH IMPEDANCE

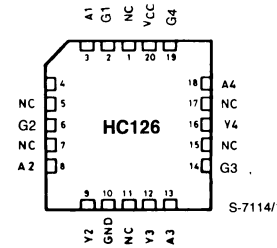
PIN CONNECTIONS (top view)



NC = No Internal Connection

CHIP CARRIER





ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

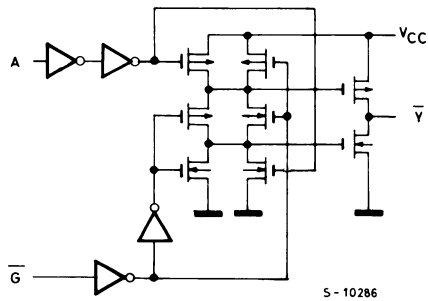
(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

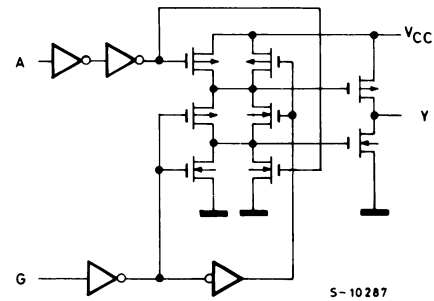
Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

CIRCUIT DIAGRAM

HC125



HC126



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0 4.5 6.0 4.5 6.0	V_I V_{IH} or V_{IL}	I_O −20 μA −6.0 mA −7.8 mA	1.9 4.4 5.9 4.18 5.68	2.0 4.5 6.0 4.31 5.8	— — — — —	1.9 4.4 5.9 4.13 5.63	— — — — —	1.9 4.4 5.9 4.10 5.60	— — — — —	V
V_{OL}	Low Level Output Voltage	2.0 4.5 6.0 4.5 6.0	V_{IH} or V_{IL}	20 μA 6.0 mA 7.8 mA	— — — — —	0.0 0.0 0.0 0.17 0.18	0.1 0.1 0.1 0.26 0.26	— — — — —	0.1 0.1 0.1 0.33 0.33	— — — — —	0.1 0.1 0.1 0.40 0.40	V
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{OZ}	3-State Output Off-State Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	25	60	—	75		90	ns
		4.5		—	7	12	—	15		18	
		6.0		—	6	10	—	13		15	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	52	100	—	125		150	ns
		4.5		—	13	20	—	25		30	
		6.0		—	11	17	—	21		26	
t_{PLH} t_{PHL}	3-State Output	2.0		—	44	90	—	115		135	ns
		4.5	$R_L = 1\ K\Omega$	—	11	18	—	23		27	
		6.0		—	19	15	—	20		23	
t_{PLZ} t_{PHZ}	3-State Output Disable Time	2.0		—	68	120	—	150	—	180	pF
		4.5	$R_L = 1K\Omega$	—	17	24	—	30	—	36	
		6.0		—	4	20	—	26	—	31	
C_{IN}	Input Capacitance			—	5	10	—	10			pF
C_{PD} (*)	Power Dissipation Capacitance			—	34	—	—	—			pF

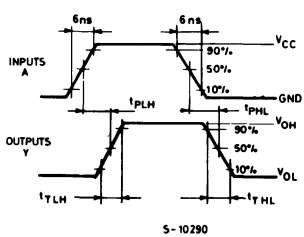
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation.

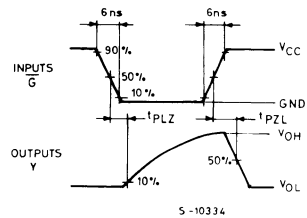
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Circuit)

SWITCHING CHARACTERISTICS TEST WAVEFORM

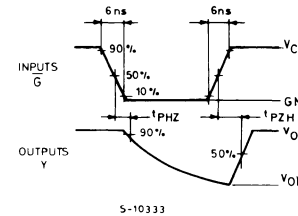
HC125



S-10290

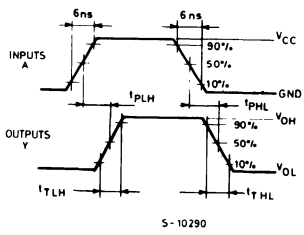


S-10334

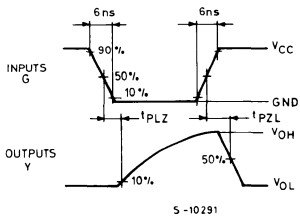


S-10333

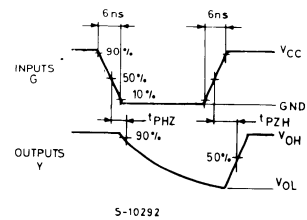
HC126



S-10290



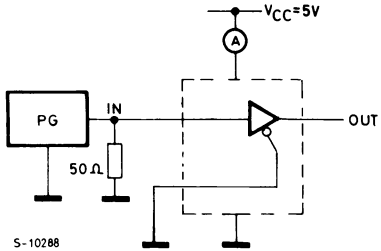
S-10291



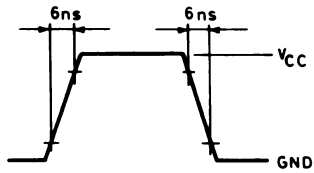
S-10292

TEST CIRCUIT I_{CC} (Opr.)

HC125

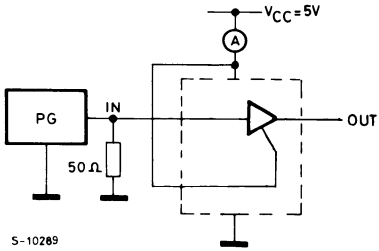


INPUT WAVEFORM

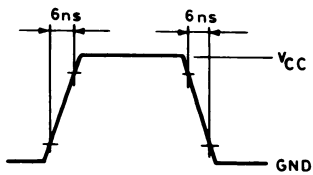


THE OTHER INPUTS ARE CONNECTED TO V_{CC} LINE OR GND LINE.

HC126



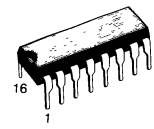
INPUT WAVEFORM



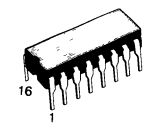
THE OTHER INPUTS ARE CONNECTED TO V_{CC} LINE OR GND LINE.

3 TO 8 LINE DECODER/LATCH

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS131



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

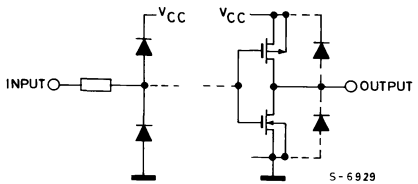
ORDERING NUMBERS:

M54HC131 F1	M74HC131 C1
M74HC131 B1N	M74HC131 M1
M74HC131 F1	

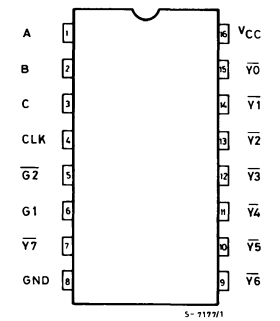
DESCRIPTION

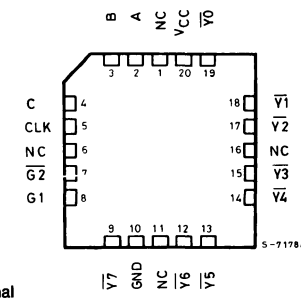
The M54/74HC131 is a high speed CMOS 3 TO 8 LINE DECODER/LATCH fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device is a DECODER/LATCH capable of selecting arbitrarily one of eight outputs by three binary inputs A, B, and C, in this case, the selected output is at logic "low".
Also, when ENABLE input G1 is set low or ENABLE input $\overline{G2}$ is set high, selection is inhibited regardless of other input signals and all the outputs are at high. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





NC = No Internal Connection

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
CLK	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
↑	H	L	L	L	L	L	H	H	H	H	H	H	H
↑	H	L	L	L	H	H	L	H	H	H	H	H	H
↑	H	L	L	H	L	H	H	L	H	H	H	H	H
↑	H	L	L	H	H	H	H	H	L	H	H	H	H
↑	H	L	H	L	L	H	H	H	H	L	H	H	H
↑	H	L	H	L	H	H	H	H	H	H	L	H	H
↑	H	L	H	H	L	H	H	H	H	H	H	L	H
↑	H	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	X	X	X	Outputs corresponding to stored address L: all others H							

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

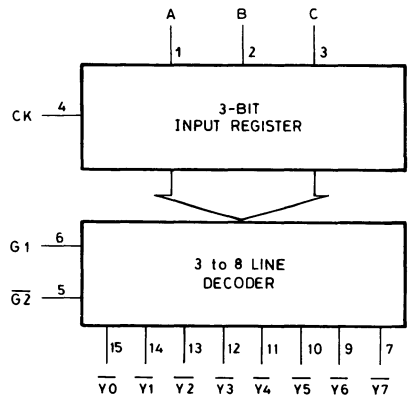
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

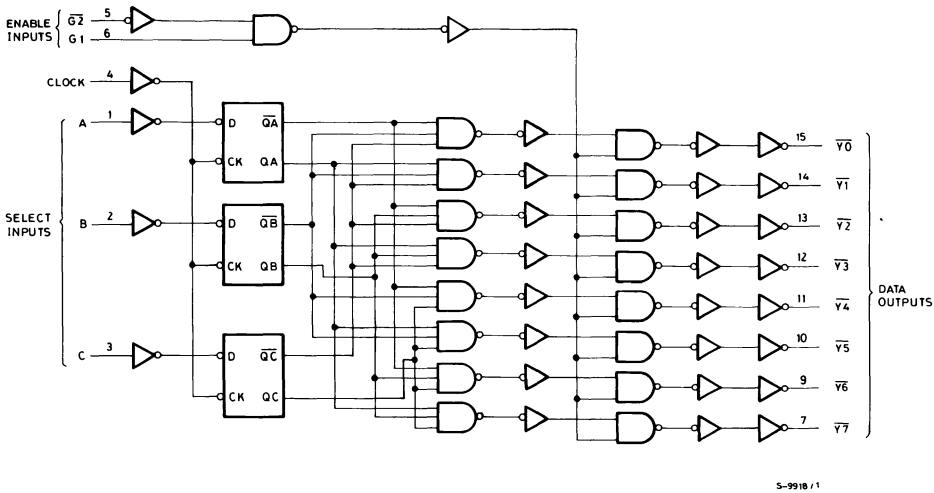
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V: 0 to 1000 V_{CC} 4.5V: 0 to 500 V_{CC} 6 V: 0 to 400	ns

BLOCK DIAGRAM



V_{CC} = 16
GND = 8

LOGIC DIAGRAM



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_{IN}	I_{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	4.0	—	40.0	—	80.0	

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

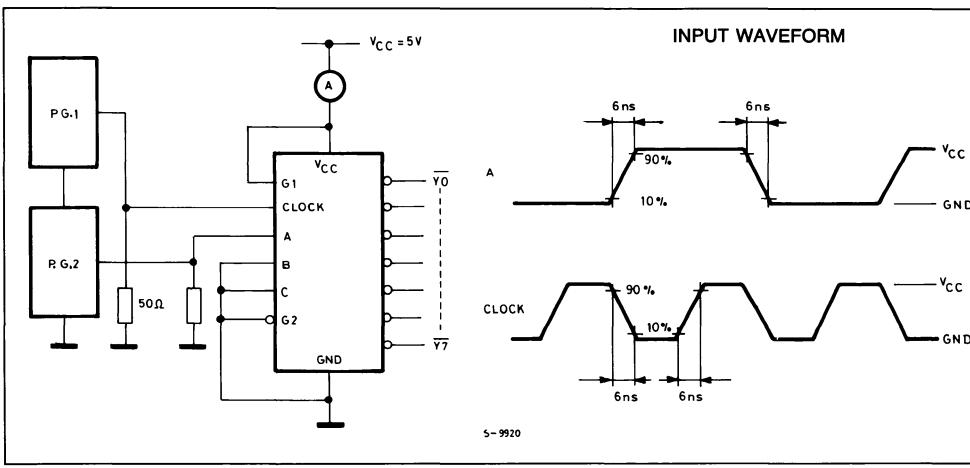
Symbol	Parameter	54HC and 74HC			Unit
		MIN.	TYP.	MAX.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time CLOCK - $\overline{Yn}$		23	36	ns
t_{PLH} t_{PHL}	Propagation Delay Time G1, $\overline{G2}$ - $\overline{Yn}$		15	24	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

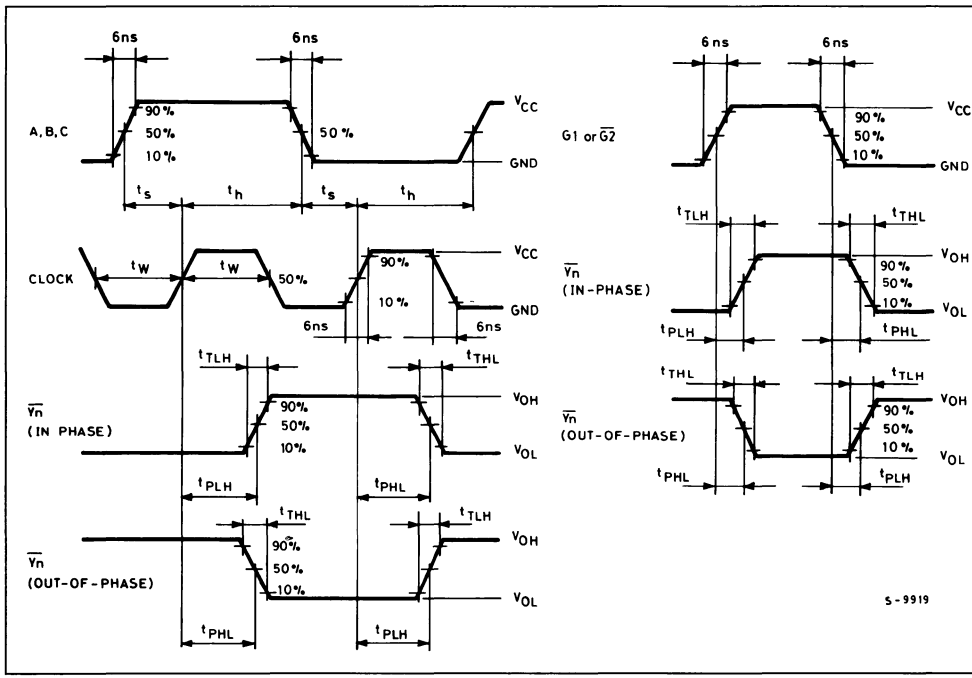
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			-40 to $85°C$ 74HC		-55 to $125°C$ 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - $\overline{Yn}$)	2.0		—	112	210	—	265	—	315	ns
		4.5		—	27	42	—	53	—	63	
		6.0		—	23	36	—	45	—	54	
t_{PLH} t_{PHL}	Propagation Delay Time ($G1$, $\overline{G2}$ $\overline{Yn}$)	2.0		—	72	140	—	175	—	210	ns
		4.5		—	18	28	—	35	—	42	
		6.0		—	16	24	—	30	—	36	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-up Time (A, B, C)	2.0		—	12	50	—	65	—	75	ns
		4.5		—	3	10	—	13	—	15	
		6.0		—	2	9	—	11	—	13	
t_h	Minimum Hold Time (A, B, C)	2.0		—	—	5	—	5	—	5	ns
		4.5		—	—	5	—	5	—	5	
		6.0		—	—	5	—	5	—	5	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	89	—	—	—	—	—	

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (refer to Test circuit).
Average operating current can be obtained by the following: $I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT



SWITCHING CHARACTERISTICS TEST WAVEFORM

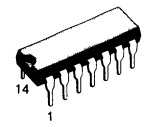


SGS-THOMSON MICROELECTRONICS

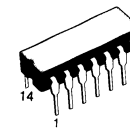
M54HC132
M74HC132

QUAD 2-INPUT SCHMITT NAND GATE

- HIGH SPEED
  t_{PD} = 21 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- HIGH NOISE IMMUNITY
  $V_{H\ (TYP.)}$ = 0.9V at V_{CC} = 5
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS132



B1
Plastic Package



F1
Ceramic Frit Seal Package

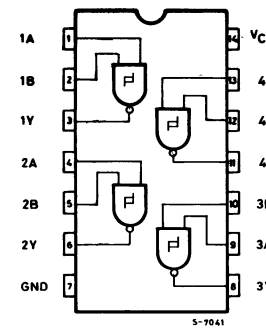
M1
Micro Package

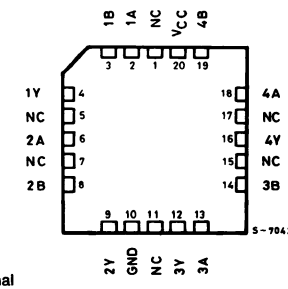
C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC132 F1
M74HC132 B1N
M74HC132 F1
M74HC132 C1
M74HC132 M1

PIN CONNECTIONS (top view)



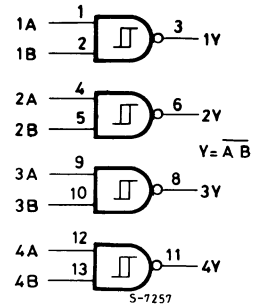


NC = No Internal Connection

DESCRIPTION

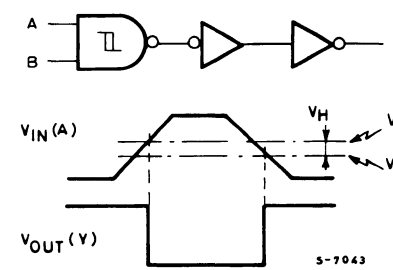
The M54/74HC132 is a high speed CMOS QUAD 2-INPUT SCHMITT NAND GATE fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. Pin configuration and function are identical to those of the M54/74HC00.
The hysterisis characteristics (around 20% V_{CC}) of all inputs allow slowly changing input signals to be transformed into sharply defined jitter-free output signals. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

BLOCK DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

LOGIC DIAGRAM/WAVEFORM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output current per pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW = derate to 10 mW/°C from 65°C to 85°C for plastic package
(*) 500 mW = derate to 12 mW/°C from 100 to 125°C for frit-seal package

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	DC Input Voltage		0 to V_{CC}	V
V_O	DC Output Voltage		0 to V_{CC}	V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125	°C
t_r/t_f	Input Rise fall times		NO LIMITS	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_P	High Level Threshold Voltage	2.0			0.8	1.25	1.5	0.8	1.5	0.8	1.5	—
		4.5			2.25	2.7	3.15	2.25	3.15	2.25	3.15	V
		6.0			3.0	3.6	4.2	3.0	4.2	3.0	4.2	
V_N	Low Level Threshold Voltage	2.0			0.4	0.75	1.0	0.4	1.0	0.4	1.0	
		4.5			1.35	1.9	2.25	1.35	2.25	1.35	2.25	V
		6.0			1.8	2.6	3.0	1.8	3.0	1.8	3.0	
V_H	Hysteresis Voltage	2.0			0.20	0.5	1.0	0.20	1.0	0.20	1.0	
		4.5			0.4	0.8	1.4	0.4	1.4	0.4	1.4	V
		6.0			0.6	1.0	1.7	0.6	1.7	0.6	1.7	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	V
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

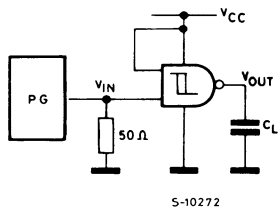
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		13	21	ns

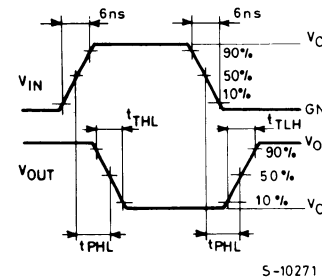
AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	64	125	—	155	—	190	ns
		4.5		—	16	25	—	31	—	38	
		6.0		—	14	21	—	26	—	32	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	34	—	—	—	—	—	pF

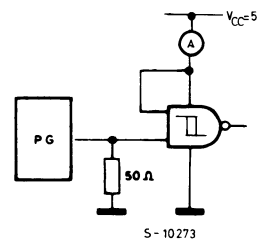
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current is: I_{CC} (Opr.) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT





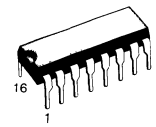
TEST CIRCUIT I_{CC} (Opr.)



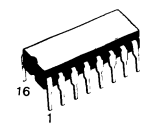
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

13 INPUT NAND GATE

- HIGH SPEED
  t_{PD} = 18 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS133



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

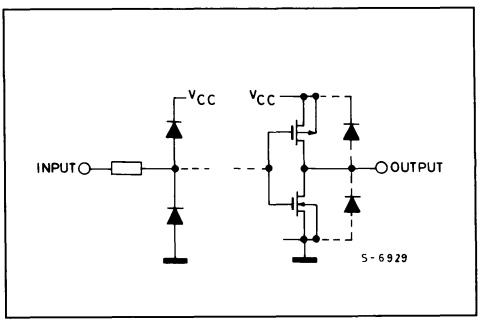
ORDERING NUMBERS:

M54HC133 F1
M74HC133 B1N
M74HC133 F1
M74HC133 C1
M74HC133 M1

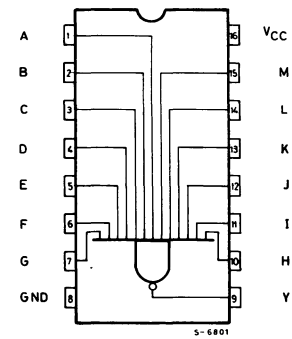
DESCRIPTION

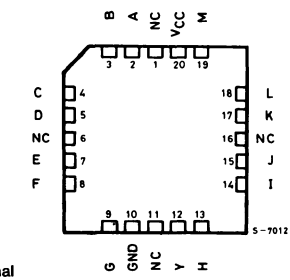
The M54/74HC133 is a high speed CMOS 13-INPUT NAND GATE fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
The internal circuit is composed of 7 stages including buffer output, which gives high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



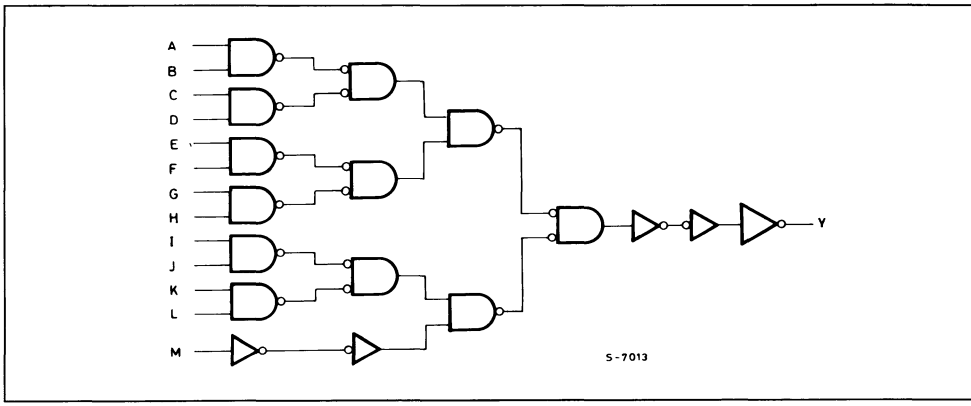
PIN CONNECTIONS (top view)





NC = No Internal Connection

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0 4.5 6.0 4.5 6.0	V_I V_{IH} or V_{IL}	I_O −20 μA −4.0 mA −5.2 mA	1.9 4.4 5.9 4.18 5.68	2.0 4.5 6.0 4.31 5.8	— — — — —	1.9 4.4 5.9 4.13 5.63	— — — — —	1.9 4.4 5.9 4.10 5.60	— — — — —	V
V_{OL}	Low Level Output Voltage	2.0 4.5 6.0 4.5 6.0	V_{IH} or V_{IL}	20 μA 4.0 mA 5.2 mA	— — — — —	0 0 0 0.17 0.18	0.1 0.1 0.1 0.26 0.26	— — — — —	0.1 0.1 0.1 0.33 0.33	— — — — —	0.1 0.1 0.1 0.40 0.40	V
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

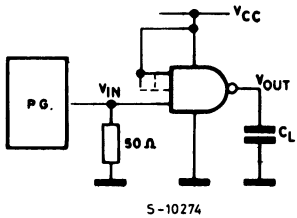
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		17	27	ns

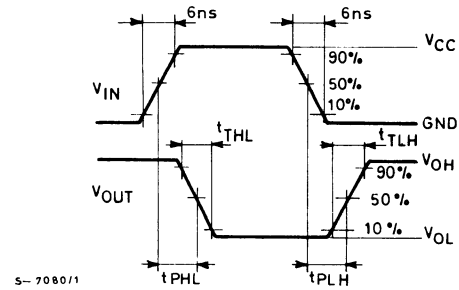
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time	2.0 4.5 6.0		— — —	80 20 17	150 30 26	— — —	190 38 33	— — —	225 45 38	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—		pF
C_{PD} (*)	Power Dissipation Capacitance			—	34	—	—	—	—	—	pF

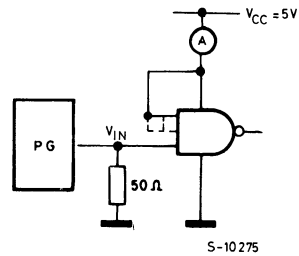
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be abtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT





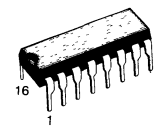
TEST CIRCUIT I_{CC} (Opr.)



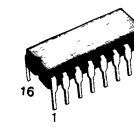
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

3 TO 8 LINE DECODER/LATCH (INVERTING)

- HIGH SPEED
  t_{PD} = 14 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS137



B1N
Plastic Package



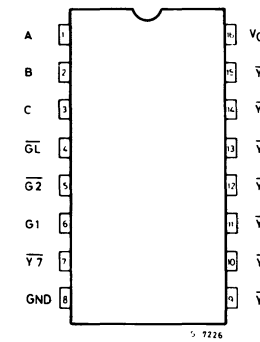
F1
Ceramic Frit Seal Package

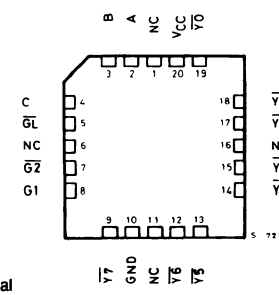
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC137 F1
M74HC137 B1N
M74HC137 F1
M74HC137 C1
M74HC137 M1

PIN CONNECTIONS (top view)



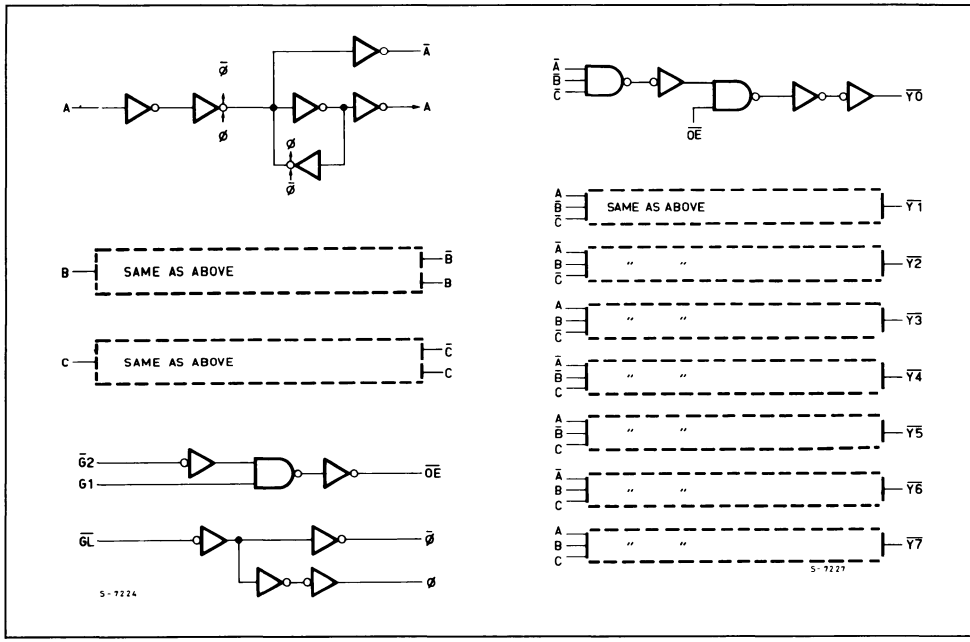


NC = No Internal Connection

DESCRIPTION

The M54/74HC137 is a high speed CMOS 3 TO 8 LINE DECODER/LATCH (INVERTING) fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
This device is a 3 to 8 line decoder with latches on the three address inputs. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B and C) is stored in the latches. As long as $\overline{GL}$ remains high no address changes will be recognized. Output enable pins G1 and $\overline{G2}$, control the state of the outputs independently of the select or latch-enable inputs. All the outputs are high unless G1 and $\overline{G2}$ are low. The HC137 is ideally suited for the implementation of glitch-free decoders in stored-address applications in bus oriented systems.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

LOGIC DIAGRAM



TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Outputs corresponding to stored address L: all others H							

X: DON'T CARE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0	or		5.9	6.0	—	5.9	—	5.9	—	
		4.5	V_{IL}	−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	

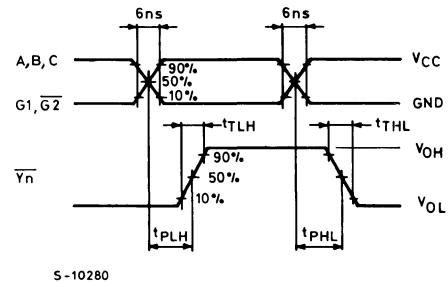
DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
			V_I	I_O	Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

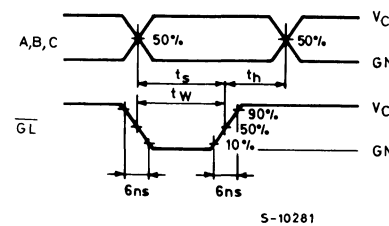
AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G1 - $\overline{Yn}$)		14	23	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{G2}$ - $\overline{Yn}$)		17	26	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{GL}$ - $\overline{Yn}$)		24	38	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A,B,C - $\overline{Yn}$)		21	34	ns

SWITCHING CHARACTERISTICS TEST WAVEFORM



S-10280



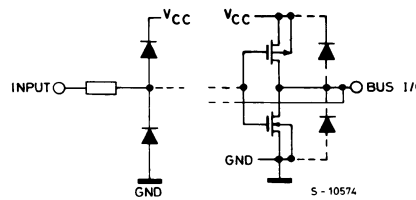
S-10281

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

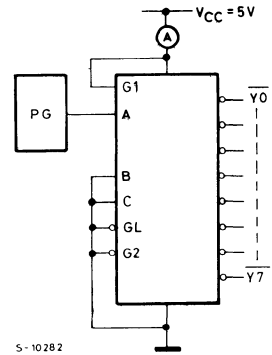
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (G1-$\overline{Yn}$)	2.0		—	72	145	—	180		220	ns
		4.5		—	18	29	—	36		44	
		6.0		—	15	25	—	31		38	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{G2}$-$\overline{Yn}$)	2.0		—	80	155	—	195		235	ns
		4.5		—	20	31	—	39		47	
		6.0		—	17	26	—	33		40	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{GL}$ - $\overline{Yn}$)	2.0		—	112	220	—	275		330	ns
		4.5		—	28	44	—	55		66	
		6.0		—	24	37	—	47		56	
t_{PLH} t_{PHL}	Propagation Delay Time (A,B,C - $\overline{Yn}$)	2.0		—	100	195	—	245		295	ns
		4.5		—	25	39	—	49		59	
		6.0		—	21	33	—	42		50	
$t_{W(L)}$	Minimum Pulse Width ($\overline{GL}$)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_s	Minimum Set-up Time (A,B,C $\overline{GL}$)	2.0		—	10	50	—	65		75	ns
		4.5		—	2	10	—	13		15	
		6.0		—	2	9	—	11		13	
t_h	Minimum Hold Time (A,B,C $\overline{GL}$)	2.0		—	5	25	—	30	—	40	ns
		4.5		—	0	5	—	6	—	8	
		6.0		—	0	5	—	6	—	7	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	65	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

INPUT AND OUTPUT EQUIVALENT CIRCUIT

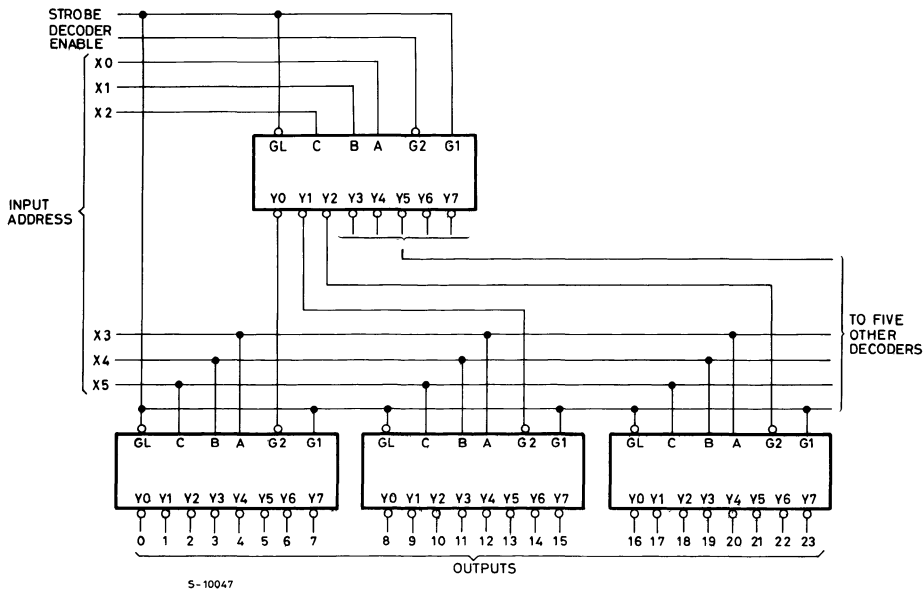


TEST CIRCUIT I_{CC} (Opr.)



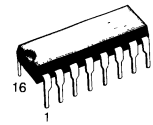
INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

TYPICAL APPLICATION

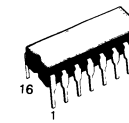


3 TO 8 LINE DECODER/LATCH

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS137



B1N
Plastic Package



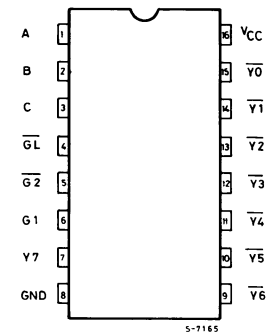
F1
Ceramic Frit Seal Package

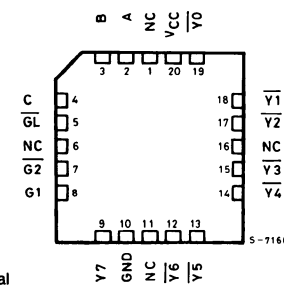
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HCT137 F1
M74HCT137 B1N
M74HCT137 F1
M74HCT137 C1
M74HCT137 M1

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

DESCRIPTION

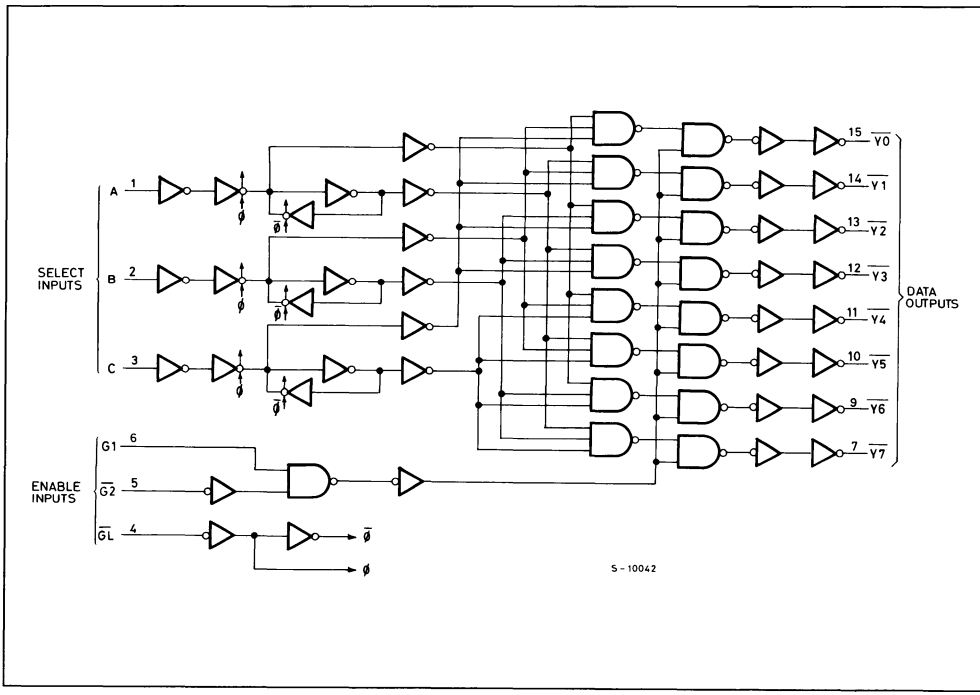
The M54/74HCT137 is a high speed CMOS 3 TO 8 LINE DECODER/LATCH fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device is a three-to eight line decoder with latches on the three address inputs. When GL goes from low to high, the address present at the select inputs (A, B and C) is stored in the latches. As long as GL remains high no address changes will be recognized. Output enable controls, G1 and G2, control the state of the outputs independently of the select or latch-enable inputs.
All of the outputs are high unless G1 is high and G2 is low. The HCT137 is ideally suited for the implementation of glitch-free decoders in stored address applications in bus oriented systems.
All inputs are equipped with protection circuits against static discharge and transient excess voltage. This integrated circuits input and output characteristics are with standard 54/74 LSTTL logic families.
M54HCT/74HCT devices are designed to directly interface HSC²MOS systems with TTL and NMOS components. These devices are also plug in replacements for LSTTL devices giving a reduction of power consumption.

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{GL}$	$\overline{G2}$	G1	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	L	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L
H	L	H	X	X	X	OUTPUT CORRESPONDING TO STORED ADDRESS, L; ALL OTHERS, H							

X: DON'T CARE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

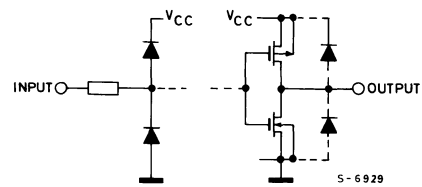
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		4.5 to 5.5	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time		0 to 500	ns

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0	—	—	2.0	—	2.0	—	V
V_{IL}	Low Level Input Voltage	4.5 to 5.5			—	—	0.8	—	0.8	—	0.8	V
V_{OH}	High Level Output Voltage	4.5	V_{IN}	I_{OH}								
			V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	V
				−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
V_{OL}	Low Level Output Voltage	4.5	V_{IN}	I_{OL}								
			V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
				4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current	5.5	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	5.5	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA
I_{CC}			Per input: $V_{IN} = 0.5V$ or 2.4V Other input: V_{CC} or GND		—	—	2.0	—	2.9	—	3.0	mA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

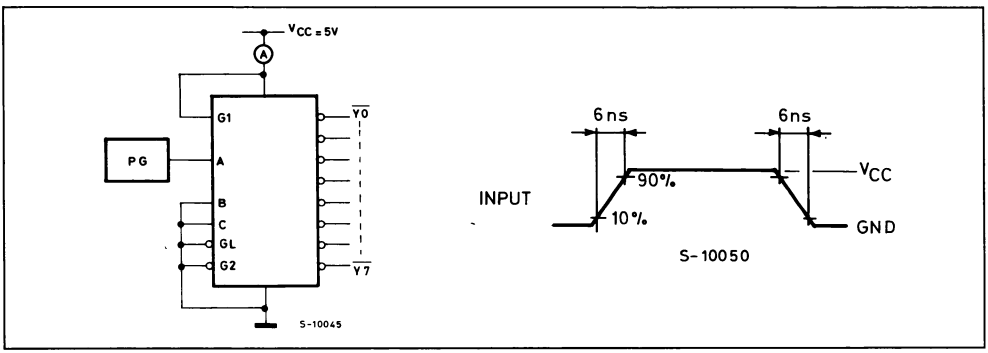
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G1-$\overline{Y}$)		21	34	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{G2}$-$\overline{Y}$)		20	32	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{GL}$-$\overline{Y}$)		29	46	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C-$\overline{Y}$)		25	39	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

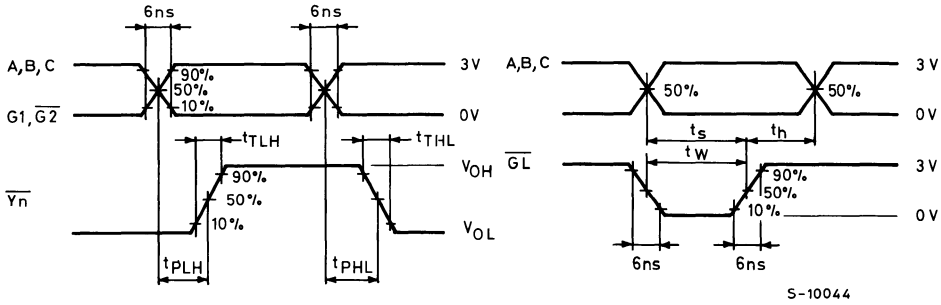
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5		—	8	15	—	19	—	22	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G1-$\overline{Y}$)	4.5		—	25	39	—	49	—	59	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G2-$\overline{Y}$)	4.5		—	24	37	—	46	—	56	ns
t_{PLH} t_{PHL}	Propagation Delay Time (GL-$\overline{Y}$)	4.5		—	34	52	—	65	—	78	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C-$\overline{Y}$)	4.5		—	29	45	—	56	—	68	ns
$t_{W(L)}$	Minimum Pulse Width ($\overline{GL}$)	4.5		—	8	15	—	19	—	22	ns
t_s	Minimum Set-up Time (A, B, C-$\overline{GL}$)	4.5		—	2	10	—	13	—	15	ns
t_h	Minimum Hold Time (A, B, C-$\overline{GL}$)	4.5		—	—	5	—	5	—	5	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	68	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average opeating current can be obtained by the equation: $I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

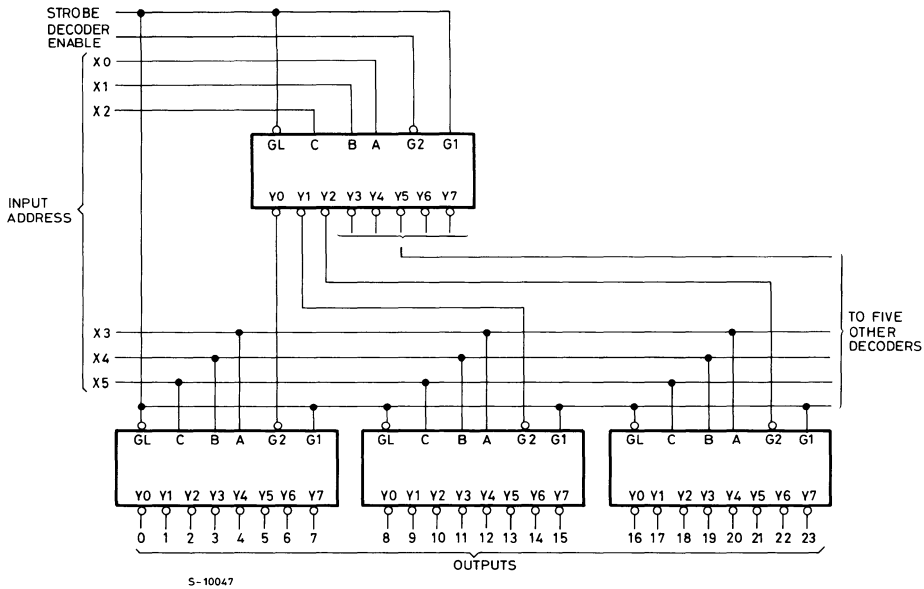
TEST CIRCUIT



SWITCHING CHARACTERISTICS TEST WAVEFORM



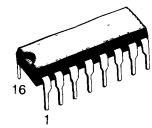
TYPICAL APPLICATION



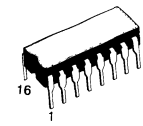
6 Line to 64 Line Decoder with Input Address Storage

3 TO 8 LINE DECODER (INVERTING)

- HIGH SPEED
  t_{PD} = 17ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA at T_A = 25°C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS138



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

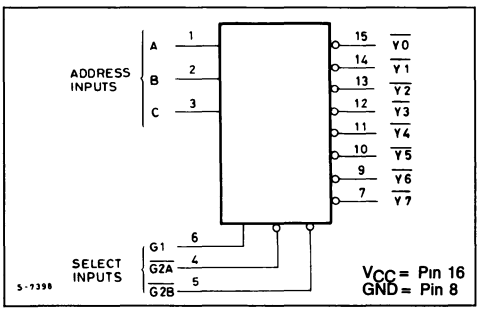
C1
Plastic Chip Carrier

ORDERING NUMBERS:
- M54HC138 F1
- M74HC138 B1N
- M74HC138 F1
- M74HC138 C1
- M74HC138 M1

DESCRIPTION

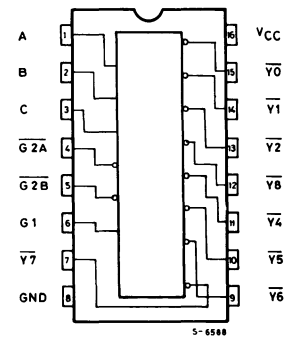
The M54/74HC138 is a high speed CMOS 3 TO 8 LINE DECODER fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. If the device is enabled, 3 binary select inputs (A, B and C) determine which one of the outputs will go low. If enable input G1 is held low or either $\overline{G2A}$ or $\overline{G2B}$ is held high, the decoding function is inhibited and all the 8 outputs go high.
Three enable inputs are provided to ease cascade connection and application of address decoders for memory systems. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

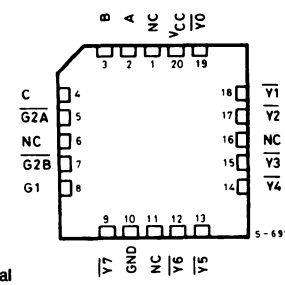
BLOCK DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

PIN CONNECTIONS (top view)





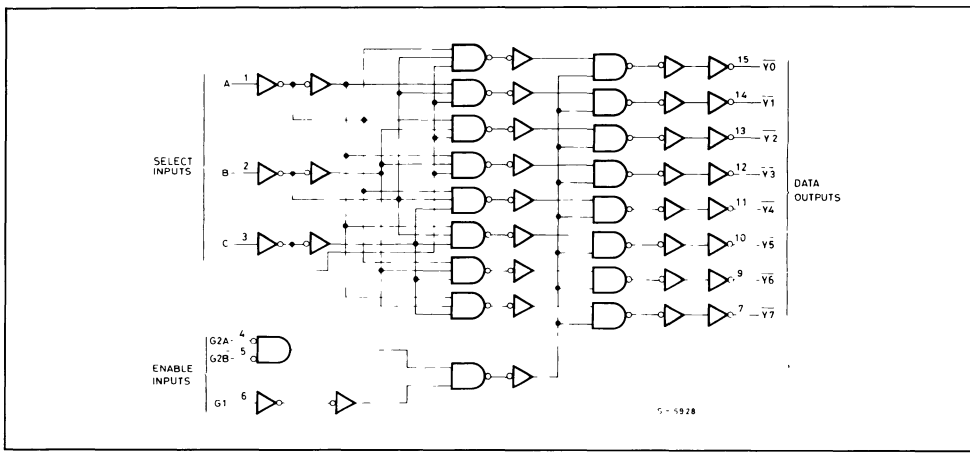
NC =
No Internal
Connection

TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			SELECT											
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	
L	X	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	X	H	X	X	X	H	H	H	H	H	H	H	H	NONE
H	L	L	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y0}$
H	L	L	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y1}$
H	L	L	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y2}$
H	L	L	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y3}$
H	L	L	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y4}$
H	L	L	H	L	H	H	H	H	H	H	L	H	H	$\overline{Y5}$
H	L	L	H	H	L	H	H	H	H	H	H	L	H	$\overline{Y6}$
H	L	L	H	H	H	H	H	H	H	H	H	H	L	$\overline{Y7}$

X: DON'T CARE

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	DC Input Voltage		0 to V_{CC}		V
V_O	DC Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	−55 to 125 −40 to 85		°C
t_r, t_f	Input Rise and Fall Time		V_{CC} = 2 V	0 to 1000	ns
			V_{CC} = 4.5V	0 to 500	
			V_{CC} = 6 V	0 to 400	

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW = derate to 10 mW/°C from 65°C to 85°C for plastic package
(*) 500 mW = derate to 12 mW/°C from 100 to 125°C for frit-seal package

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0 4.5 6.0	V_I V_{IH} or V_{IL}	I_O −20 μA	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	1.9 4.4 5.9	— — —	V
		4.5 6.0		−4.0 mA −5.2 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	
V_{OL}	Low Level Output Voltage	2.0 4.5 6.0	V_{IH} or V_{IL}	20 μA	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
		4.5 6.0		4.0 mA 5.2 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A,B,C-Y)		17	27	ns
t_{PHL}	Propagation Delay Time (G, $\overline{G}$-$\overline{Y}$)		15	23	ns

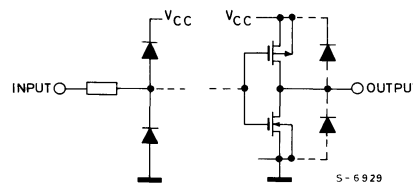
AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (A,B,C-$\overline{Y}$)	2.0		—	84	165	—	205		250	ns
		4.5		—	21	33	—	41		50	
		6.0		—	18	28	—	35		43	
t_{PLH} t_{PHL}	Propagation Delay Time (G, $\overline{G}$-$\overline{Y}$)	2.0		—	72	145	—	180		220	ns
		4.5		—	18	29	—	36		44	
		6.0		—	15	25	—	31		37	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	57	—	—	—			pF

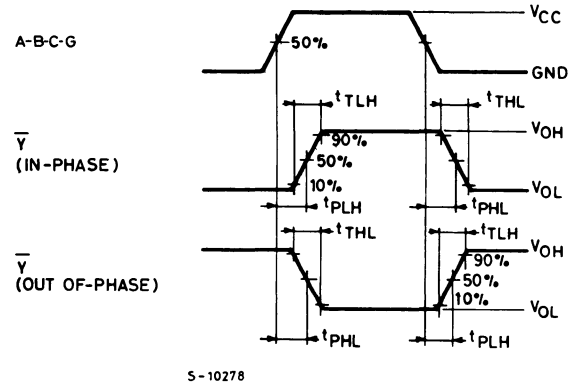
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current is: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

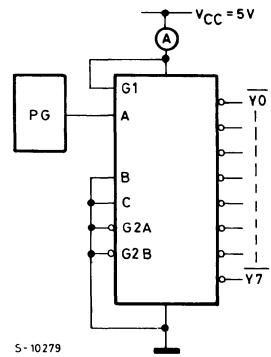
INPUT AND OUTPUT EQUIVALENT CIRCUIT



SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



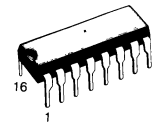
INPUT TRANSITION TIME IS TH SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

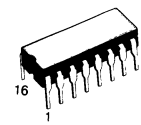
M54HCT138
M74HCT138

3 TO 8 LINE DECODER

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS138



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

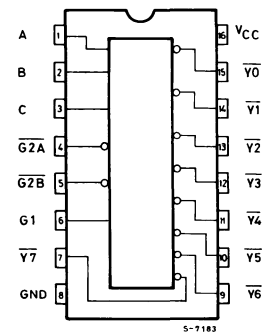
C1
Plastic Chip Carrier

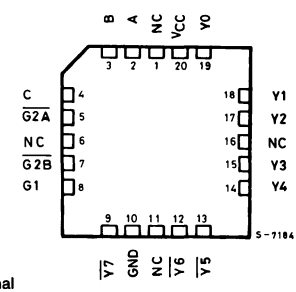
ORDERING NUMBERS:
M54HCT138 F1
M74HCT138 B1N
M74HCT138 F1
M74HCT138 C1
M74HCT138 M1

DESCRIPTION

The M54/74HCT138 is a high speed CMOS 3 TO 8 LINE DECODER fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
If the device is enabled, 3 binary select inputs (A, B and C) determine which one of the outputs will go low.
If enable input G1 is held "Low" or either $\overline{G2A}$ or $\overline{G2B}$ is held "High", the decoding function is inhibited and all the 8 outputs go high.
3 enable inputs are provided to ease cascade connection and application in address decoders for memory systems.
All inputs are equipped with protection circuits against static discharge and transient excess voltage. This integrated circuit has total compatibility, input and output characteristics, with standard 54/74 LSTTL logic families.
M54HCT/74HCT devices are designed to directly interface HSC²MOS systems with TTL and NMOS components. These devices are also plug in replacements for LSTTL devices giving a reduction in power consumption.

PIN CONNECTIONS (top view)





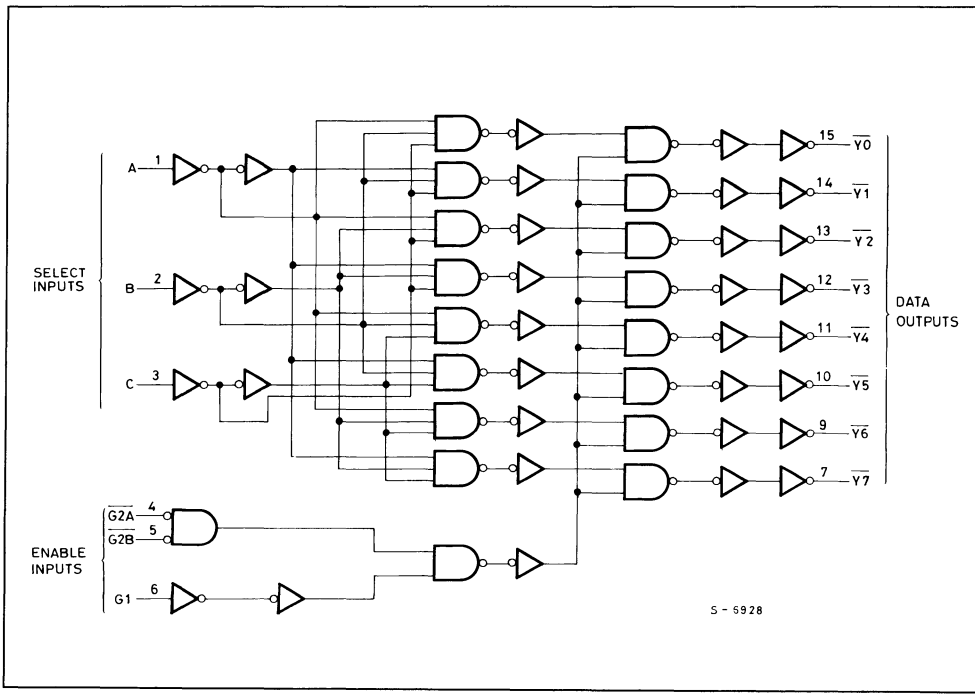
NC = No Internal Connection

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{G2B}$	$\overline{G2A}$	G1	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	L	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	X	X	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

X: DON'T CARE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

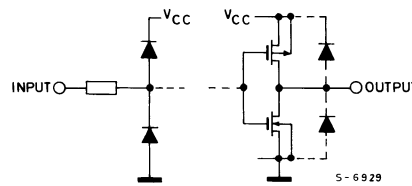
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		4.5 to 5.5	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time		0 to 500	ns

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0	—	—	2.0	—	2.0	—	V
V_{IL}	Low Level Input Voltage	4.5 to 5.5			—	—	0.8	—	0.8	—	0.8	V
V_{OH}	High Level Output Voltage	4.5	V_{IN}	I_{OH}								V
			V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
				−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
V_{OL}	Low Level Output Voltage	4.5	V_{IN}	I_{OL}								V
			V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	
				4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current	5.5	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	5.5	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA
I_{CC}			Per input: $V_{IN} = 0.5V$ or 2.4V Other input: V_{CC} or GND		—	—	2.0	—	2.9	—	3.0	mA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

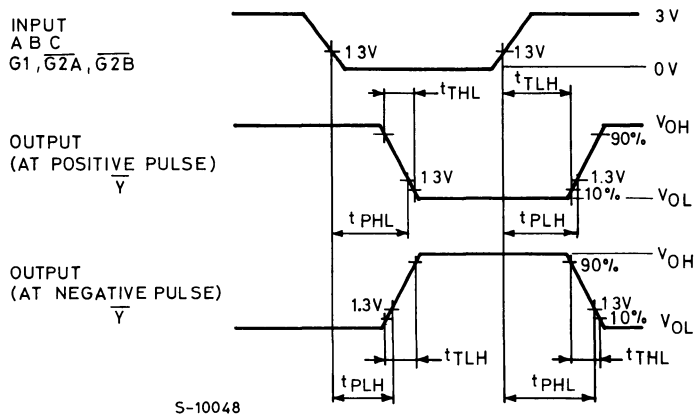
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G1-$\overline{Y}$)		23	36	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G2-$\overline{Y}$)		26	41	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C - $\overline{Y}$)		28	44	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

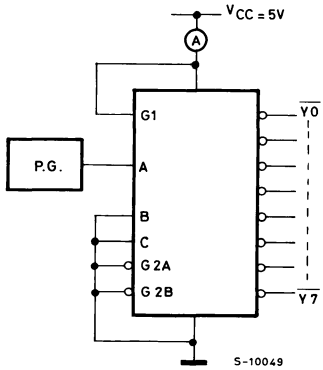
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5		—	8	15	—	19	—	22	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G1-$\overline{Y}$)	4.5		—	25	41	—	51	—	62	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G2-$\overline{Y}$)	4.5		—	30	47	—	59	—	71	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C - $\overline{Y}$)	4.5		—	32	50	—	63	—	75	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	65	—	—	—	—	—	pF

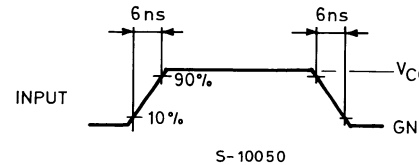
Note (*) C_{PD} is defined as the value of IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained from the equation: $I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



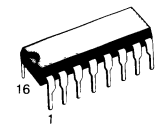
TEST CIRCUIT I_{CC} (Opr.)



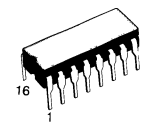


DUAL 2-TO-4 LINE DECODER/DEMULTIPLEXER

- HIGH SPEED
  t_{PD} = 16 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS139



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
SO Micro Package

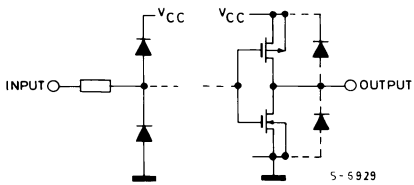
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC139 F1
M74HC139 B1N
M74HC139 F1
M74HC139 C1
M74HC139 M1

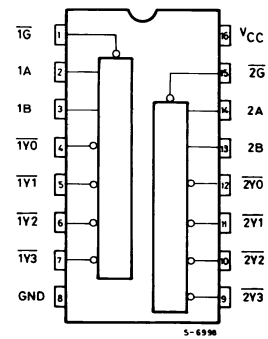
DESCRIPTION

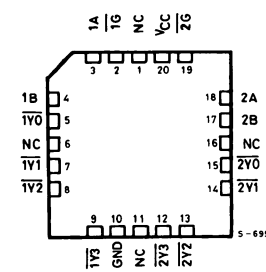
The M54/74HC139 is a high speed CMOS DUAL TWO LINE TO FOUR LINE DECODER/DEMULTIPLEXER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The active low enable input can be used for gating or as a data input for demultiplexing applications. While the enable input is held high, all four outputs are high independently of the other inputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





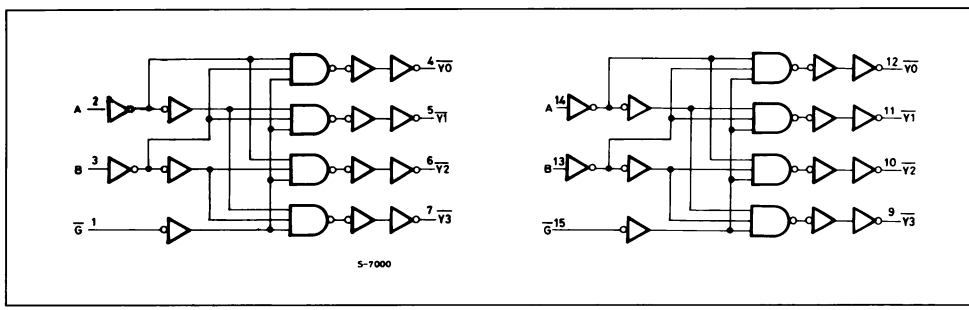
NC =
No Internal
Connection

TRUTH TABLE

INPUTS			OUTPUS				SELECTED OUTPUT
ENABLE	SELECT						
$\overline{G}$	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	
H	X	X	H	H	H	H	NONE
L	L	L	L	H	H	H	$\overline{Y0}$
L	L	H	H	L	H	H	$\overline{Y1}$
L	H	L	H	H	L	H	$\overline{Y2}$
L	H	H	H	H	H	L	$\overline{Y3}$

X: DON'T CARE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

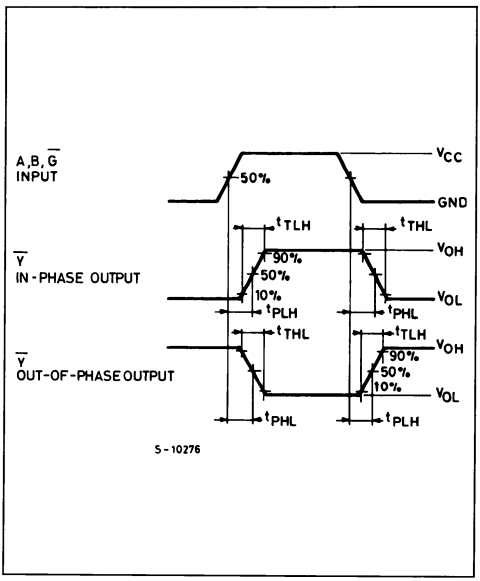
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		16	26	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{G}$-Y)		14	23	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

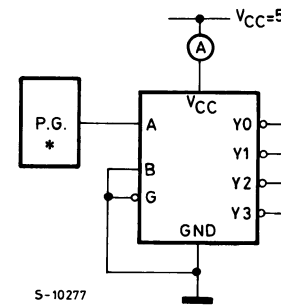
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time A, B-Y	2.0		—	76	150	—	190	—	225	ns
		4.5		—	19	30	—	38	—	45	
		6.0		—	17	26	—	33	—	38	
t_{PLH} t_{PHL}	Propagation Delay Time $\overline{G}$-Y	2.0		—	68	135	—	170	—	205	ns
		4.5		—	17	27	—	34	—	41	
		6.0		—	15	23	—	29	—	35	
C_{IN}	Input Capacitance			—	5	10	—	10	—		pF
C_{PD} (*)	Power Dissipation Capacitance			—	49	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value the IC's of internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be abtained by the following equation.
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT



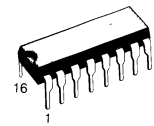
TEST CIRCUIT I_{CC} (Opr.)



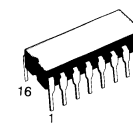
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

10 TO 4 LINE PRIORITY ENCODER

- HIGH SPEED
  t_{PD} = 16 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS147



B1N
Plastic Package



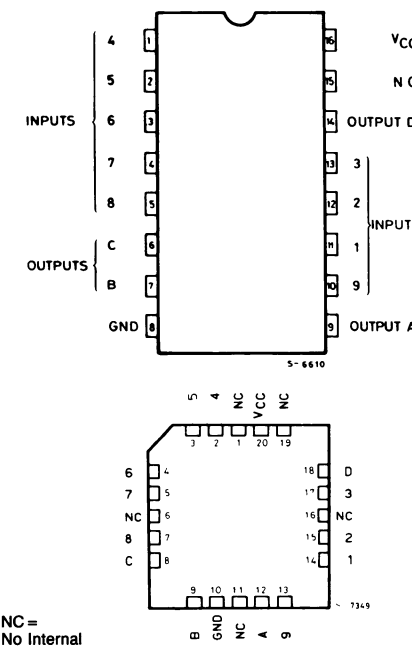
F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC147 F1
M74HC147 B1N
M74HC147 F1
M74HC147 C1
M74HC147 M1

PIN CONNECTIONS (top view)



NC = No Internal Connection

DESCRIPTION

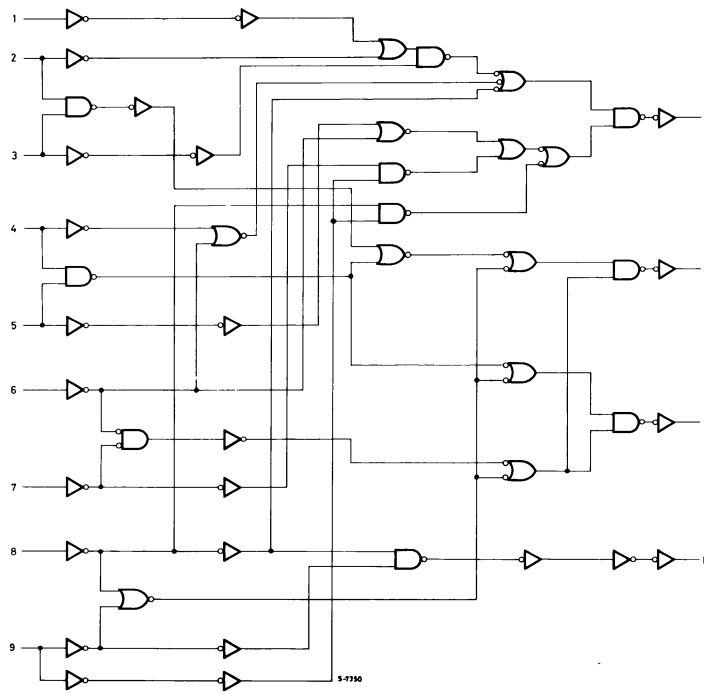
The M54/74HC147 is a high speed CMOS 10 TO 4 LINE PRIORITY ENCODER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
This device features priority encoding of the inputs to ensure that only the highest order data line is encoded. Nine input lines are encoded to a four line BCD output. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level. All data input and outputs are active at the low logic level. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUT									OUTPUT			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

X: DON'T CARE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

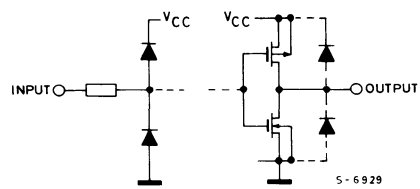
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

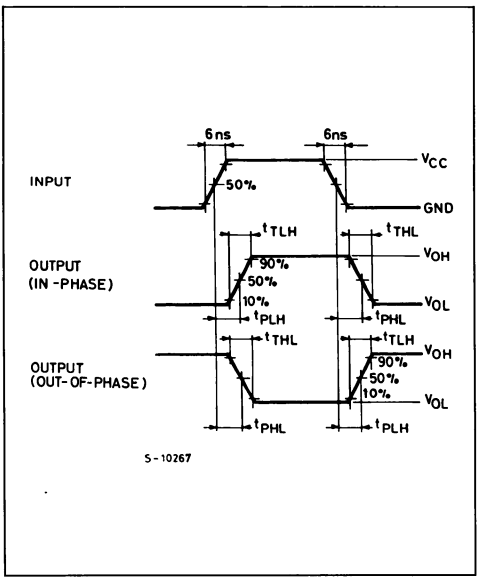
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		16	26	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

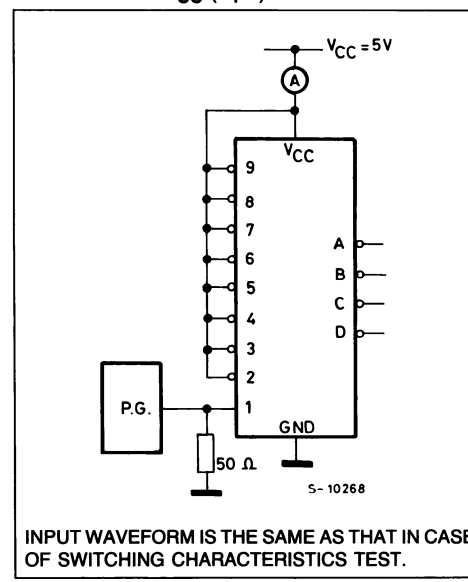
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time Output	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	76	150	—	190	—	225	ns
		4.5		—	19	30	—	38	—	45	
		6.0		—	16	26	—	33	—	38	
C_{IN}	Input Capacitance			—	5	10	—	10	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance			—	37	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be abtained by the following equation.
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT



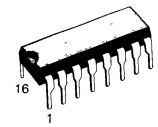
TEST CIRCUIT I_{CC} (Opr.)



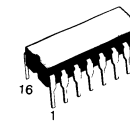
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

8-TO-3 LINE PRIORITY ENCODER

- HIGH SPEED
  t_{PD} = 16 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS148



B1N
Plastic Package



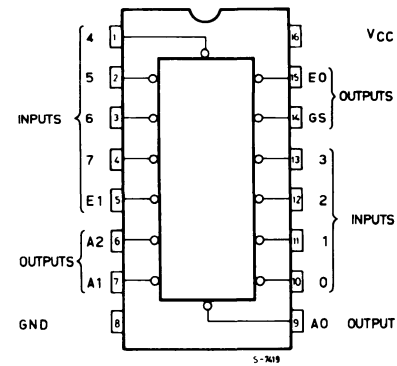
F1
Ceramic Frit Seal Package

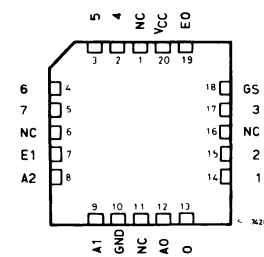
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC148 F1
M74HC148 B1N
M74HC148 F1
M74HC148 C1
M74HC148 M1

PIN CONNECTIONS (top view)





NC = No Internal Connection

DESCRIPTION

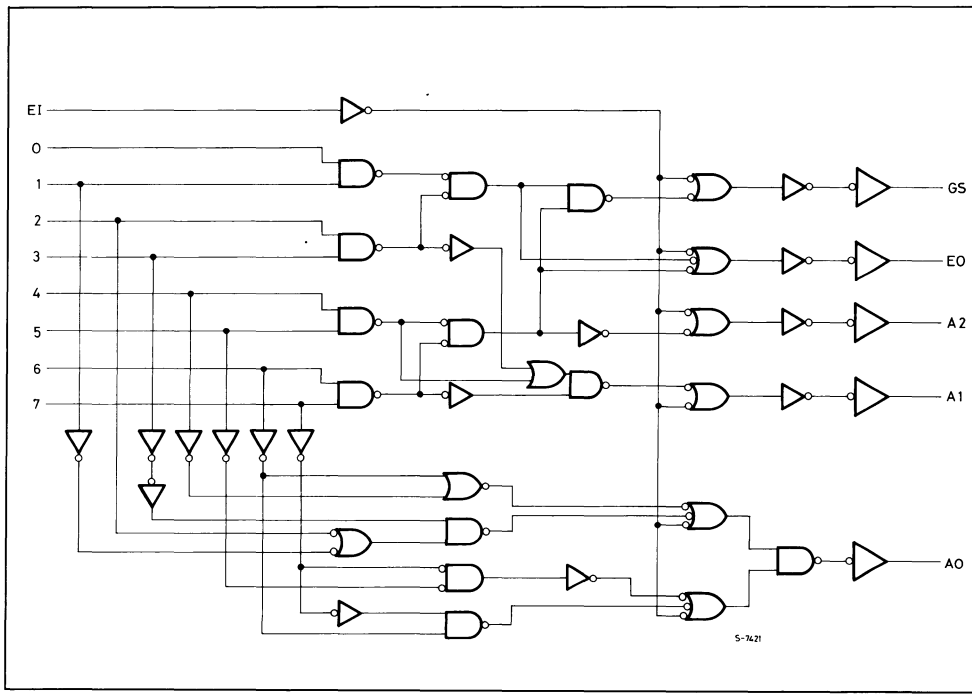
The M54/74HC148 is a high speed CMOS 8-TO-3 LINE PRIORITY ENCODER fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The M54/74HC148 encodes eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. Data inputs and outputs are active at the low logic level.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUT									OUTPUT				
E1	0	1	2	3	4	5	6	7	A2	A1	A0	GS	E0
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

X: DON'T CARE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

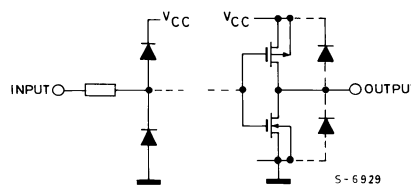
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series Operating Temperature 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

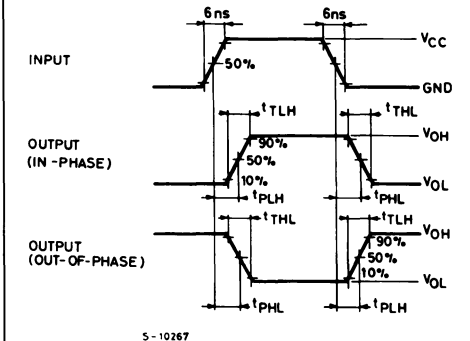
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (IN - A0, A1, A2)		16	25	ns
t_{PLH} t_{PHL}	Propagation Delay Time (IN - EO, GS)		18	28	ns
t_{PLH} t_{PHL}	Propagation Delay Time (E1 - E0)		12	20	ns
t_{PLH} t_{PHL}	Propagation Delay Time (E1 - GS)		12	19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (E1 - A0, A1, A2)		13	21	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

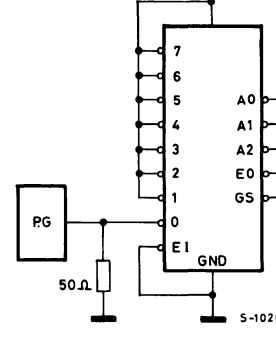
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (IN A0, A1, A2)	2.0 4.5 6.0		— — —	76 19 16	150 30 26	— — —	190 38 33	— — —	225 45 38	ns
t_{PLH} t_{PHL}	Propagation Delay Time (IN, E0, GS)	2.0 4.5 6.0		— — —	84 21 18	165 33 28	— — —	205 41 35	— — —	250 50 43	ns
t_{PLH} t_{PHL}	Propagation Delay Time (IN, E1, E0)	2.0 4.5 6.0		— — —	60 15 13	120 24 20	— — —	150 30 26	— — —	180 36 31	ns
t_{PLH} t_{PHL}	Propagation Delay Time (IN, E1, GS)	2.0 4.5 6.0		— — —	56 14 12	115 23 20	— — —	145 29 25	— — —	175 35 30	ns
t_{PLH} t_{PHL}	Propagation Delay Time (IN E1, A0, A1, A2)	2.0 4.5 6.0		— — —	64 16 14	125 25 21	— — —	155 31 26	— — —	190 38 32	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	57	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value the IC's of internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit).
Average operating current can be obtained by the following equation.
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT



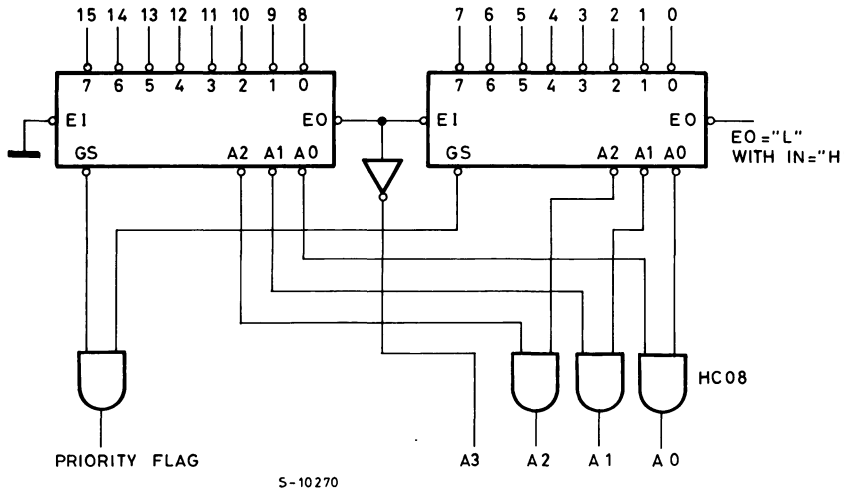
TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TYPICAL APPLICATION

4-BIT CASCADE CONNECTION

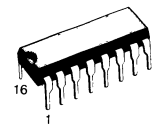


SGS-THOMSON MICROELECTRONICS

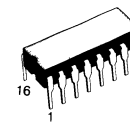
M54HC151
M74HC151

8 CHANNEL MULTIPLEXER

- HIGH SPEED
  t_{PD} = 20 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DEALYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS151



B1N
Plastic Package



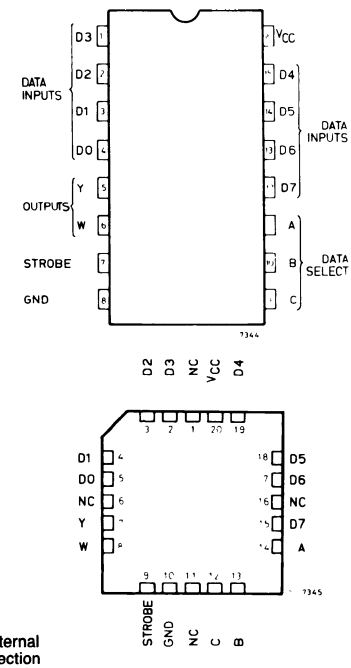
F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC151 F1
M74HC151 B1N
M74HC151 F1
M74HC151 C1
M74HC151 M1

PIN CONNECTIONS (top view)

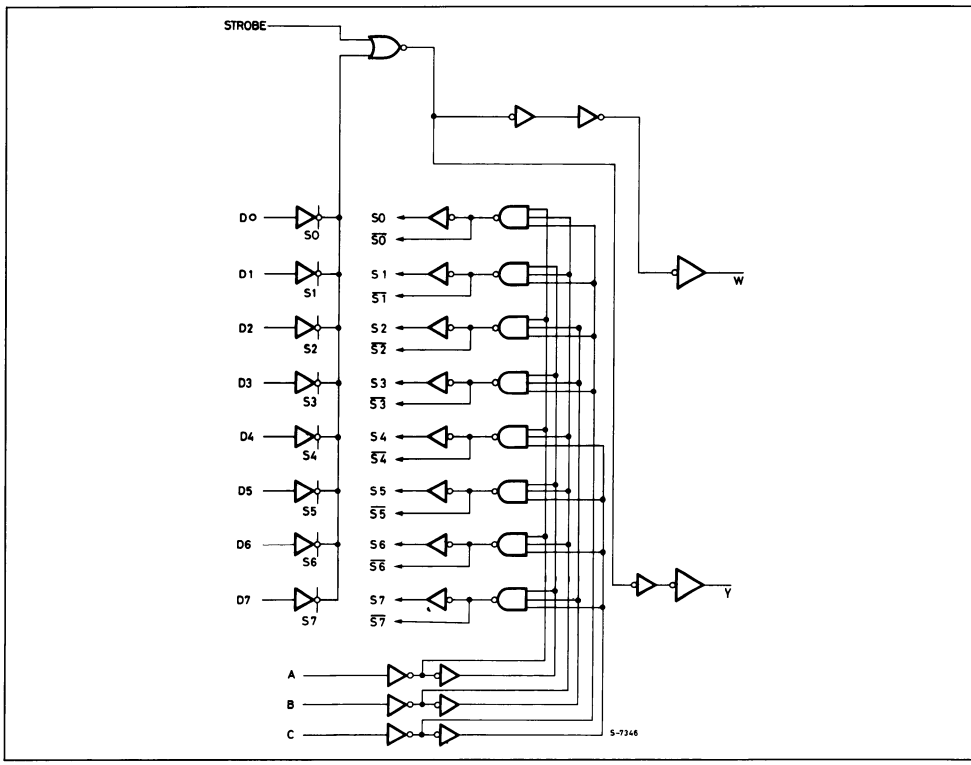


NC = No Internal Connection

DESCRIPTION

The M54/74HC151 is a high speed CMOS 8 CHANNEL MULTIPLEXER fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. It provides, in one package, the ability to select one bit of data from up to eight sources. The HC151 can be used as a universal function generator to generate any logic function of four variables. Outputs Y and W are complementary selection depends on the address inputs A, B and C. The strobe input must be taken low to enable this device, when the strobe is high W output is forced high and consequently Y output goes low.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

LOGIC DIAGRAM



TRUTH TABLE

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	S		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

X: DON'T CARE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

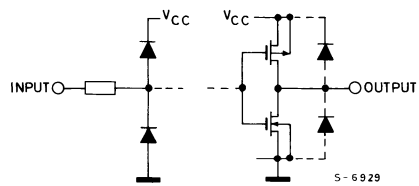
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

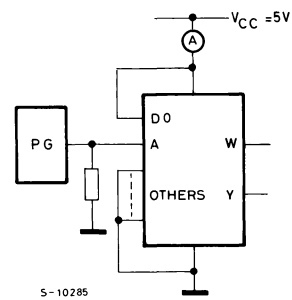
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (D-W)		18	29	ns
t_{PLH} t_{PHL}	Propagation Delay Time (D-Y)		17	27	ns
t_{PLH} t_{PHL}	Propagation Delay Time (STROBE-W)		12	20	ns
t_{PLH} t_{PHL}	Propagation Delay Time (STROBE-Y)		11	18	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A,B,C-W)		22	35	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A,B,C-Y)		21	33	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (D-W)	2.0		—	84	165	—	205	—	250	ns
		4.5		—	21	33	—	41	—	50	
		6.0		—	18	28	—	35	—	43	
t_{PLH} t_{PHL}	Propagation Delay Time (D-Y)	2.0		—	80	160	—	200	—	240	ns
		4.5		—	20	32	—	40	—	48	
		6.0		—	17	27	—	34	—	41	
t_{PLH} t_{PHL}	Propagation Delay Time (STROBE-W)	2.0		—	56	115	—	145	—	175	ns
		4.5		—	14	23	—	29	—	35	
		6.0		—	12	20	—	25	—	30	
t_{PLH} t_{PHL}	Propagation Delay Time (STROBE-Y)	2.0		—	52	105	—	130	—	160	ns
		4.5		—	13	21	—	26	—	32	
		6.0		—	11	18	—	22	—	27	
t_{PLH} t_{PHL}	Propagation Delay Time (A,B,C - W)	2.0		—	104	205	—	255	—	310	ns
		4.5		—	26	41	—	51	—	62	
		6.0		—	22	35	—	43	—	53	
t_{PLH} t_{PHL}	Propagation Delay Time (A,B,C,-Y)	2.0		—	100	195	—	245	—	295	ns
		4.5		—	25	39	—	49	—	59	
		6.0		—	21	33	—	42	—	50	
C_{IN}	Input Capacitance			—	5	10	—	10	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance			—	75	—	—	—	—	—	pF

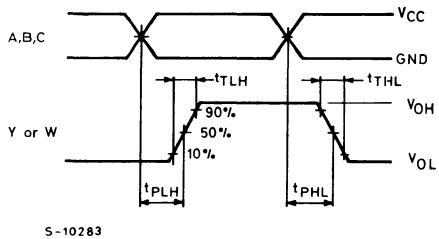
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current is: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

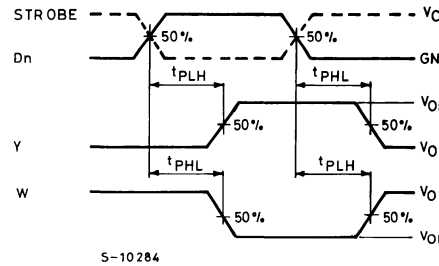
TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

SWITCHING CHARACTERISTICS TEST WAVEFORM





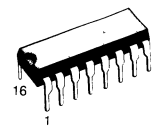
SGS-THOMSON MICROELECTRONICS

M54HC153/253
M74HC153/253

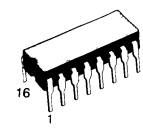
HC153 DUAL 4-CHANNEL MULTIPLEXER
HC253 DUAL 4-CHANNEL MULTIPLEXER 3-STATE OUTPUT

PRELIMINARY DATA

- HIGH SPEED
  t_{PD} = 14 ns (Typ) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS153/253



B1N
Plastic Package



F1
Ceramic Frit Seal Package

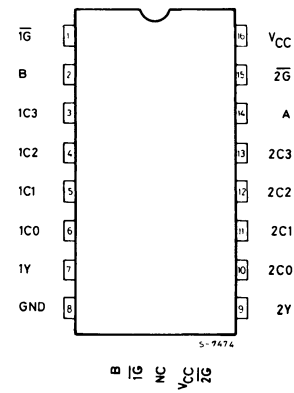
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX M1
M74HCXXX C1

PIN CONNECTION (top view)



NC = No Internal Connection

DESCRIPTION

The M54/74HC153 and M54/74HC253 are high speed CMOS DUAL 4-CHANNEL MULTIPLEXERS fabricated with silicon gate C²MOS technology. Both achieve high speed operation, similar to equivalent LSTTL, while maintaining the CMOS low power dissipation.

The designer has a choice of complementary output (HC153) and 3-state output (HC253).

Each of these data (1C0-1C3, 2C0-2C3) is selected by the two address inputs A and B.

Separate strobe inputs ($1\overline{G}$, $2\overline{G}$) are provided for each of the two four-line sections. The strobe input ($\overline{G}$) can be used to inhibit the data output; the output of HC 153 is fixed at a low level and the output of HC253 is a high impedance, while the strobe input is held low.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

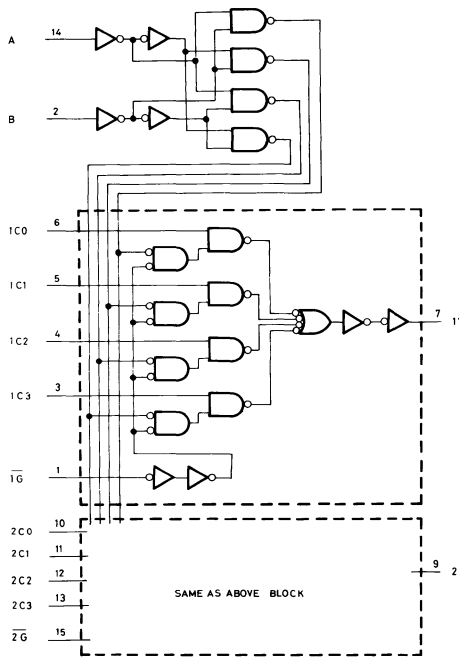
TRUTH TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT Y	
B	A	C_0	C_1	C_2	C_3	$\overline{G}$	HC153	HC253
X	X	X	X	X	X	H	L	Z
L	L	L	X	X	X	L	L	L
L	L	H	X	X	X	L	H	H
L	H	X	L	X	X	L	L	L
L	H	X	H	X	X	L	H	H
H	L	X	X	L	X	L	L	L
H	L	X	X	H	X	L	H	H
H	H	X	X	X	L	L	L	L
H	H	X	X	X	H	L	H	H

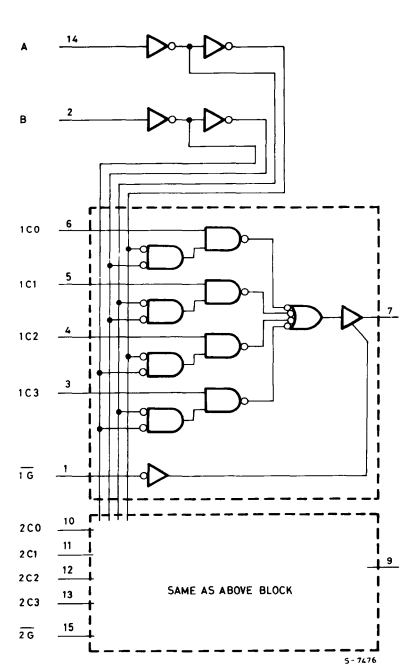
X: DON'T CARE - Z: HIGH IMPEDANCE

LOGIC DIAGRAM

HC153



HC253



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

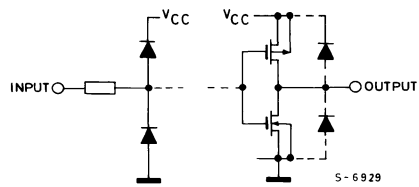
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0 4.5 6.0 4.5 6.0	V_I V_{IH} or V_{IL}	I_O −20 μA −4.0 mA −5.2 mA	1.9 4.4 5.9 4.18 5.68	2.0 4.5 6.0 4.31 5.8	— — — — —	1.9 4.4 5.9 4.13 5.63	— — — — —	1.9 4.4 5.9 4.10 5.60	— — — — —	V
V_{OL}	Low Level Output Voltage	2.0 4.5 6.0 4.5 6.0	V_{IH} or V_{IL}	20 μA 4.0 mA 5.2 mA	— — — — —	0.0 0.0 0.0 0.17 0.18	0.1 0.1 0.1 0.26 0.26	— — — — —	0.1 0.1 0.1 0.33 0.33	— — — — —	0.1 0.1 0.1 0.40 0.40	V
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{OZ}	3-State Output(1) Off-State Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	±0.5	—	±5.0		±10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

Note: 1. Applied only for M54/74HC253

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (C_n - Y)		14	23	ns
t_{PLH}	Propagation Delay Time (A, B-Y) ($\overline{G}$-Y)		21	33	ns
t_{PZH} t_{PZL}	3-State Output Enable Time*		10	17	ns
t_{PHZ} t_{PLZ}	3-State Output Disable Time*		8	14	ns

* Only HC253

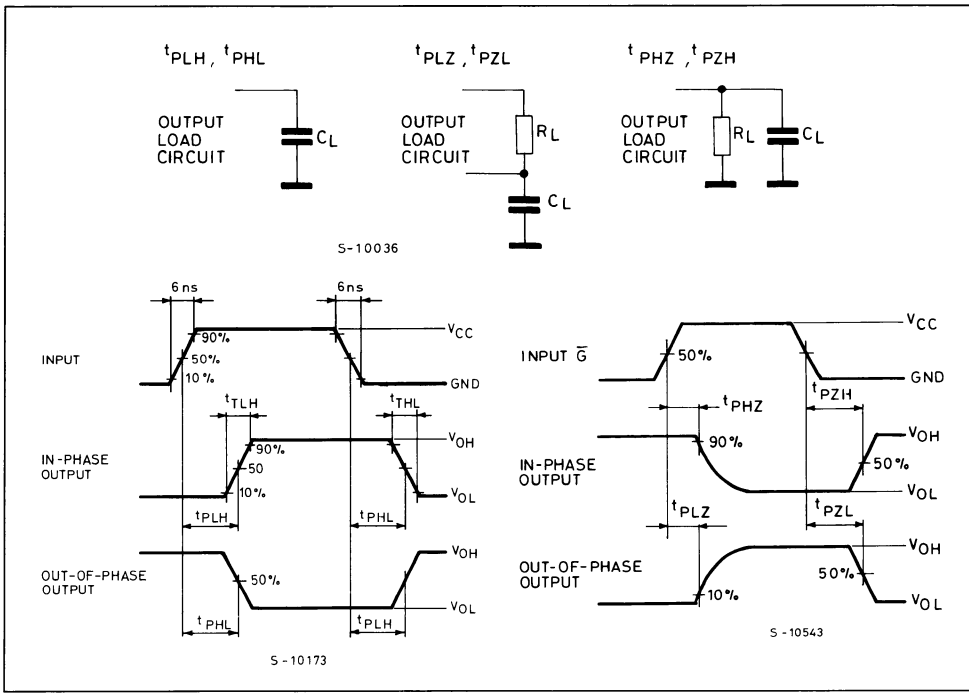
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	25	75	—	95		110	ns
		4.5		—	9	15	—	19		22	
		6.0		—	8	13	—	16		19	
t_{PLH} t_{PHL}	HC153/253 Propagation Delay Time (C_n-Y)	2.0		—	68	130	—	165		195	ns
		4.5		—	17	26	—	33		39	
		6.0		—	14	22	—	28		33	
t_{PLH} t_{PHL}	HC153/253 (A,B - Y)	2.0		—	100	195	—	245		295	ns
		4.5		—	25	39	—	49		59	
		6.0		—	21	33	—	42		50	
t_{PLH} t_{PHL}	HC153 Propagation Delay Time ($\overline{G}$ - Y)	2.0		—	100	195	—	245		295	ns
		4.5		—	25	39	—	49	—	59	
		6.0		—	21	33	—	42	—	50	
t_{PZL} t_{PZH}	HC253 Output Enable Time	2.0	$R_L = 1K\Omega$	—	46	100	—	125		150	ns
		4.5		—	12	20	—	25		30	
		6.0		—	10	17	—	21		26	
t_{PLZ} t_{PHZ}	HC253 Output Disable Time	2.0	$R_L = 1K\Omega$	—	56	115	—	145		175	ns
		4.5		—	14	23	—	29		35	
		6.0		—	12	22	—	25		30	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{OUT}	Output Capacitance		HC253	—	7	—	—	—			
C_{PD} (*)	Power Dissipation Capacitance		HC123	—	56	—	—	—			pF
			HC253	—	56	—	—	—			

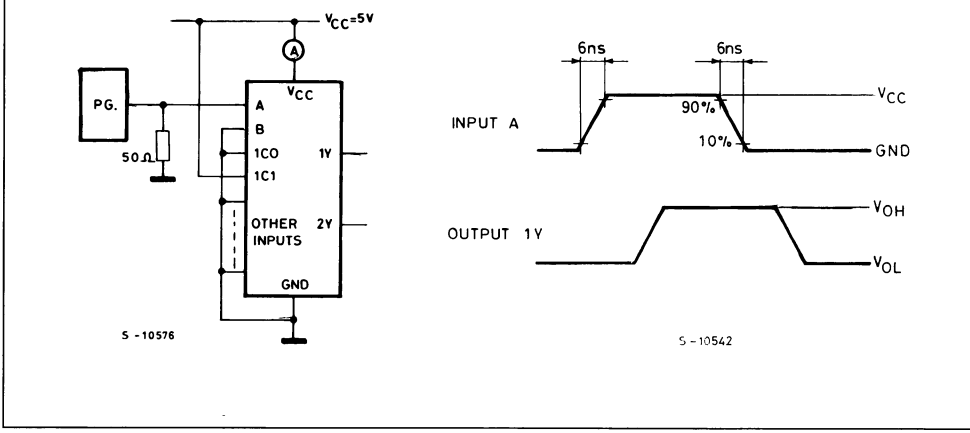
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation hereunder:
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per Circuit)

SWITCHING CHARACTERISTICS TEST WAVEFORM

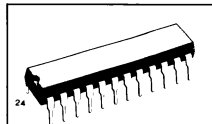


TEST CIRCUIT I_{CC} (Opr.)

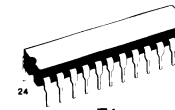


4 TO 16-LINE DECODER/DEMULTIPLEXER

- HIGH SPEED
  t_{PD} = 23 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS154



B1N
Plastic Package



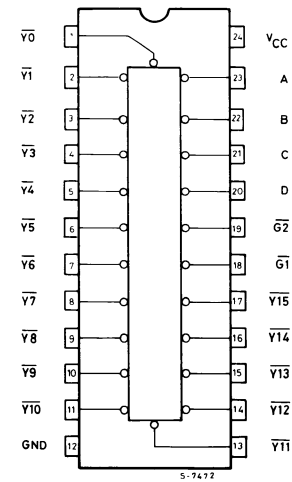
F1
Ceramic Frit Seal Package

M1
Micro Package

ORDERING NUMBERS:

M54HC154 F1	M74HC154 M1
M74HC154 B1N	M74HC154 F1

PIN CONNECTIONS (top view)



DESCRIPTION

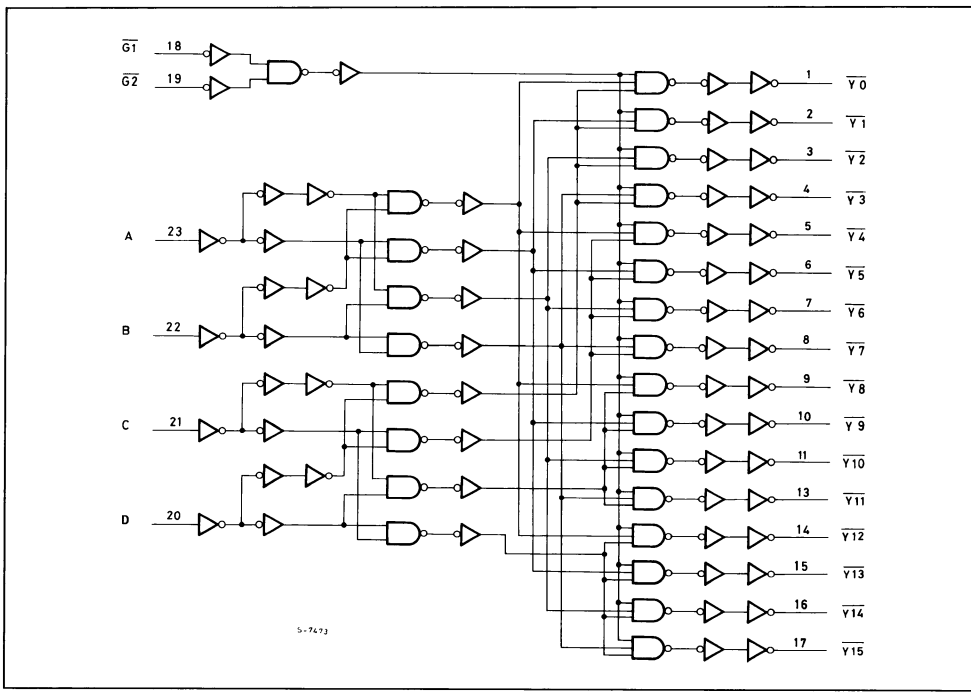
The M54/74HC154 is a high speed CMOS 4 TO 16-LINE DECODER/DEMULTIPLEXER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
A binary code applied to the four inputs (A to D) provides a low level at the selected one of sixteen outputs excluding the other fifteen outputs, when both the strobe inputs, $\overline{G1}$ and $\overline{G2}$, are held low. When either strobe input is held high, the decording function is inhibited to keep all outputs high. The strobe function makes it easy to expand the decoding lines through cascading, and simplifies the design of address decoding circuits in memory control systems.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUTS						SELECTED OUTPUT (L)
$\overline{G_1}$	$\overline{G_2}$	D	C	B	A	
L	L	L	L	L	L	$\overline{Y_0}$
L	L	L	L	L	H	$\overline{Y_1}$
L	L	L	L	H	L	$\overline{Y_2}$
L	L	L	L	H	H	$\overline{Y_3}$
L	L	L	H	L	L	$\overline{Y_4}$
L	L	L	H	L	H	$\overline{Y_5}$
L	L	L	H	H	L	$\overline{Y_6}$
L	L	L	H	H	H	$\overline{Y_7}$
L	L	H	L	L	L	$\overline{Y_8}$
L	L	H	L	L	H	$\overline{Y_9}$
L	L	H	L	H	L	$\overline{Y_{10}}$
L	L	H	L	H	H	$\overline{Y_{11}}$
L	L	H	H	L	L	$\overline{Y_{12}}$
L	L	H	H	L	H	$\overline{Y_{13}}$
L	L	H	H	H	L	$\overline{Y_{14}}$
L	L	H	H	H	H	$\overline{Y_{15}}$
X	H	X	X	X	X	NONE
H	X	X	X	X	X	NONE

X: DON'T CARE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

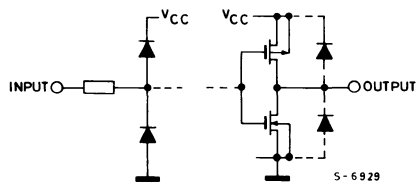
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.32	—	0.37	—	0.40	
		6.0		5.2 mA	—	0.18	0.32	—	0.37	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

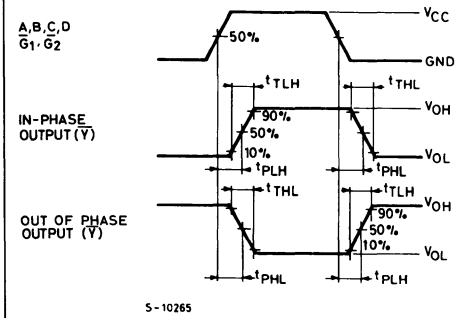
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C, D - $\overline{Y}$)		23	36	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{G1}$, $\overline{G2}$, Y)		19	30	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

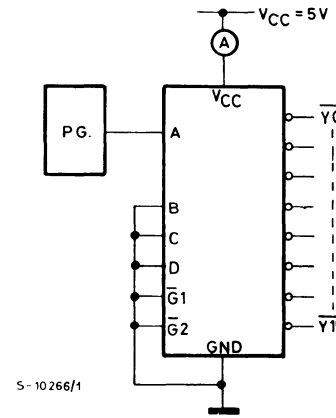
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time A, B, C, D-$\overline{Y}$)	2.0		—	104	200	—	250	—	300	ns
		4.5		—	26	40	—	50	—	60	
		6.0		—	22	34	—	43	—	51	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{G}_1$ $\overline{G}_2$-Y)	2.0		—	88	175	—	220	—	265	ns
		4.5		—	22	35	—	44	—	53	
		6.0		—	19	30	—	37	—	45	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	68	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (refer to Test circuit).
Average operating current can be abtained by equation hereunder.
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT



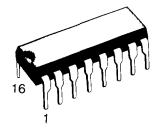
TEST CIRCUIT I_{CC} (Opr.)



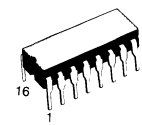
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

DUAL 2-TO-4 LINE DECODER/3 TO 8 LINE DECODER

- HIGH SPEED
  t_{PD} = 18 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS155



B1N
Plastic Package



F1
Ceramic Frit Seal Package

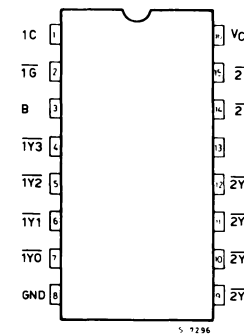
M1
Micro Package

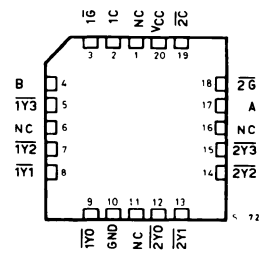
C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC155 F1
M74HC155 B1N
M74HC155 F1
M74HC155 C1
M74HC155 M1

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

DESCRIPTION

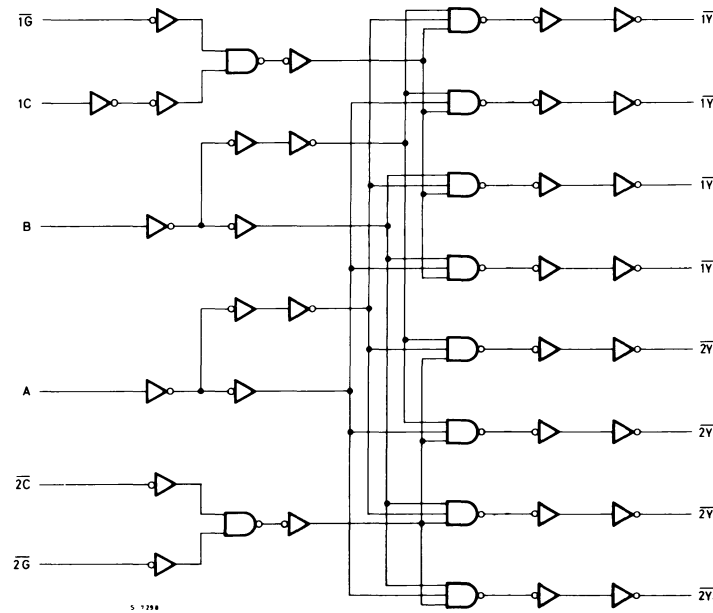
The M54/74HC155 is a high speed CMOS DUAL 2-TO-4 LINE DECODER fabricated in silicon gate C²MOS technology.

It has the same high speed performance of LSTTL combined with true CMOS low power consumption. It features dual 1-TO-4 line demultiplexers with individual strobe inputs (1G and 2G), individual data inputs (1C and $\overline{2C}$) and common binary address inputs (A and B).

When both decoders are enabled by the strobes, the inverted output of 1C data and non-inverted output of $\overline{2C}$ data will be brought to the select output pins of each sections. A 1-TO-8 line demultiplexer can also be easily built up by providing a data signal to both 1C and $\overline{2C}$ inputs; the output order from the msb is 1Y3, 1Y2, 1Y1, 1Y0, 2Y3, 2Y2, 2Y1, 2Y0. This device can be used as a 2-to-4 line decoder or a 3-to-8 line decoder when 1C is held high and $\overline{2C}$ is held low.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

LOGIC DIAGRAM



TRUTH TABLE

INPUTS				OUTPUTS			
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

X: DON'T CARE

INPUTS				OUTPUTS			
B	A	2G	2C	2Y0	2Y1	2Y3	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

X: DON'T CARE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400		ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0		1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0		— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V

DC SPECIFICATIONS (Continued)

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
			V_I	I_O	Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	High Level Output Voltage	2.0	V_{IH} or V_{IL}	−20 μA	1.9	2.0	—	1.9	—	1.9	—	V
		4.5			4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

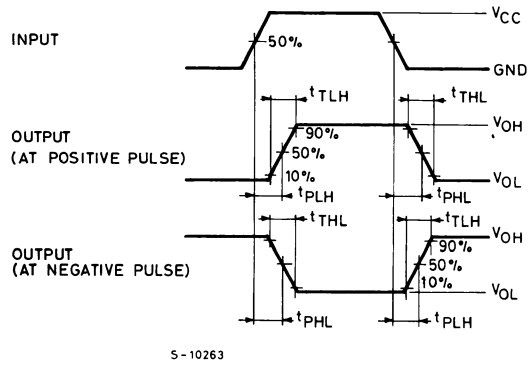
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		19	30	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

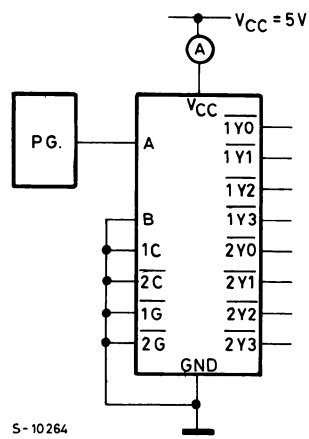
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	88	175	—	220	—	265	ns
		4.5		—	22	35	—	44	—	53	
		6.0		—	19	30	—	37	—	45	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	65	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (refer to Test circuit).
Average operating current can be abtained by equation hereunder.
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST WAVEFORM I_{CC} (Opr.)



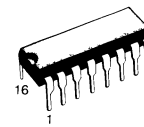
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

SGS-THOMSON MICROELECTRONICS

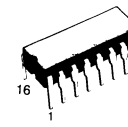
M54HC157/158
M74HC157/158

HC157 QUAD 2-CHANNEL MULTIPLEXER
HC158 QUAD 2-CHANNEL MULTIPLEXER (INV.)

- HIGH SPEED
  t_{PD} = 10 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS157/158



B1N
Plastic Package



F1
Ceramic Frit Seal Package

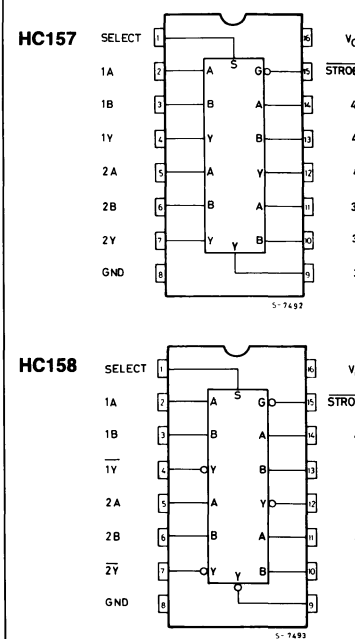
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX C1
M74HCXXX M1

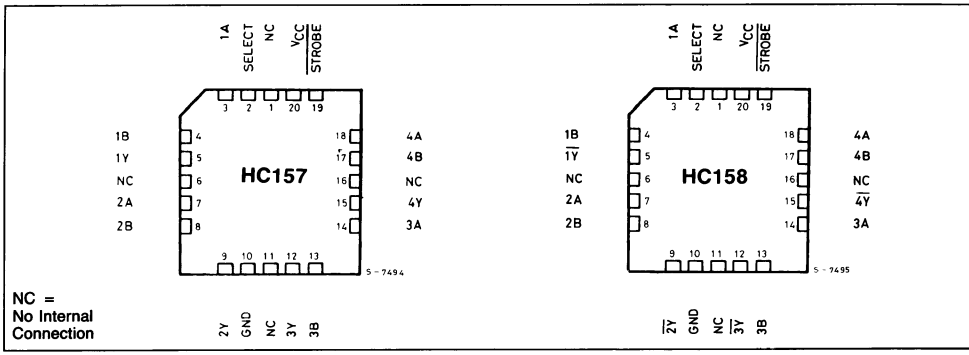
PIN CONNECTIONS (top view)



DESCRIPTION

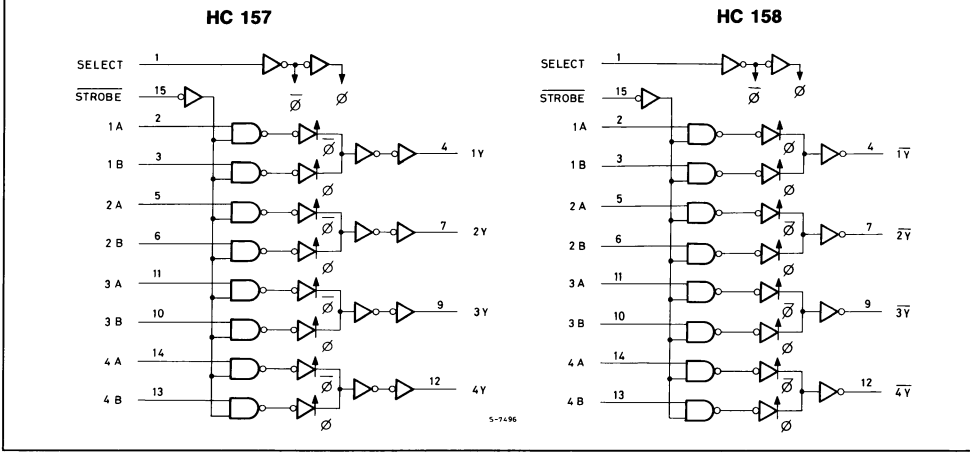
The M54/74HC157 and the M54/74HC158 are high speed CMOS QUAD 2-CHANNEL MULTIPLEXER's fabricated with silicon gate C²MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
These devices consist of four 2-input digital multiplexers with common select and strobe inputs. The HC158 is an inverting multiplexer while the HC157 is a non-inverting multiplexer. When the $\overline{\text{STROBE}}$ input is held High, selection of data is inhibited and all the outputs become Low in the M74HC157 and High in the M74HC158. The SELECT decoding determines whether the A or B inputs get routed to their corresponding Y outputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

CHIP CARRIER



NC =
No Internal
Connection

LOGIC DIAGRAM



TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{\text{STROBE}}$	SELECT	A	B	Y (157)	$\overline{\text{Y}}$ (158)
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

X: DON'T CARE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

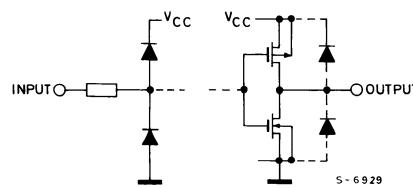
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current *	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND $I_O = 0$		—	—	4	—	40	—	80	μA

* Applicable only to DIR, G, $\overline{G}$ input

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

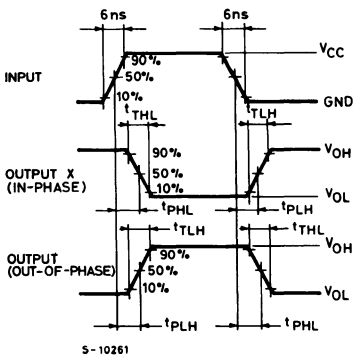
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A, B - $\overline{Y}$) HC158		10	17	ns
t_{PLH} t_{PHL}	Propagation Delay Time (SELECT - $\overline{Y}$) HC158		14	22	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{STROBE}$ - $\overline{Y}$) HC158		14	22	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A, B - Y) HC157		10	17	ns
t_{PLH} t_{PHL}	Propagation Delay Time (SELECT - Y) HC157		15	24	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{STROBE}$ - Y) HC157		14	22	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

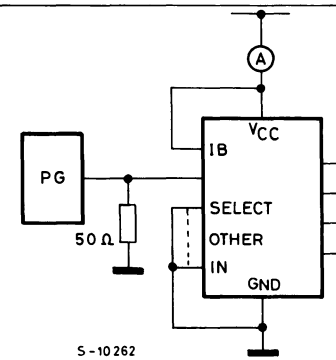
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B - Y) HC157	2.0		—	52	105	—	130	—	160	ns
		4.5		—	13	21	—	26	—	32	
		6.0		—	11	18	—	22	—	27	
t_{PLH} t_{PHL}	Propagation Delay Time (SELECT-Y) HC157	2.0		—	72	140	—	175	—	210	ns
		4.5		—	18	28	—	35	—	42	
		6.0		—	15	24	—	30	—	36	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{STROBE}$-Y) HC157	2.0		—	68	135	—	170	—	205	ns
		4.5		—	17	27	—	34	—	41	
		6.0		—	14	23	—	29	—	35	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B - $\overline{Y}$ HC158	2.0		—	46	100	—	125	—	150	ns
		4.5		—	12	20	—	25	—	30	
		6.0		—	10	17	—	21	—	26	
t_{PLH} t_{PHL}	Propagation Delay Time (SELECT-$\overline{Y}$) HC158	2.0		—	68	135	—	170	—	205	ns
		4.5		—	17	27	—	34	—	41	
		6.0		—	14	23	—	29	—	35	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{STROBE}$-$\overline{Y}$) HC158	2.0		—	64	130	—	165	—	195	ns
		4.5		—	16	26	—	33	—	39	
		6.0		—	14	22	—	28	—	33	
C_{IN}	Input Capacitance			—	6	10	—	10	—		pF
C_{PD} (*)	Power Dissipation Capacitance		HC157	—	53	—	—	—	—	—	pF
			HC158	—	51	—	—	—			

Note (*) C_{PD} is defined as the value the IC's of internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be abtained by the following equation hereunder.
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Channel)

SWITCHING CHARACTERISTICS TEST CIRCUIT



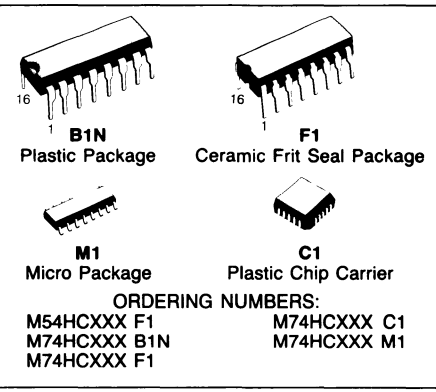
TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SYNCHRONOUS PRESETTABLE 4-BIT COUNTER

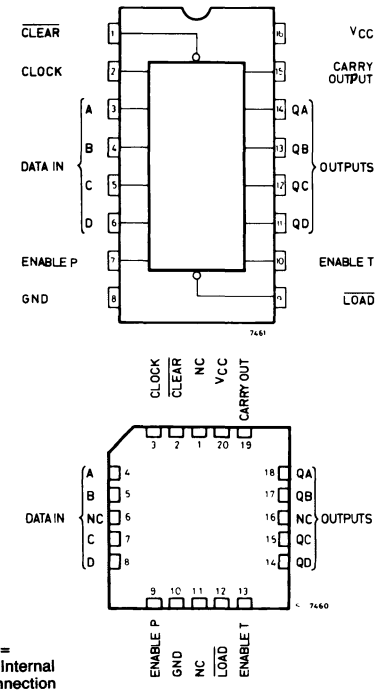
- HIGH SPEED
  f_{MAX} = 50 MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at 25°C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN).
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS160 ~ 163



ORDERING NUMBERS:

M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX C1
M74HCXXX M1

PIN CONNECTIONS (top view)



NC = No Internal Connection

DESCRIPTION

M54/74HC160 Decade, Asynchronous Clear
M54/74HC161 Binary, Asynchronous Clear
M54/74HC162 Decade, Synchronous Clear
M54/74HC163 Binary, Synchronous Clear

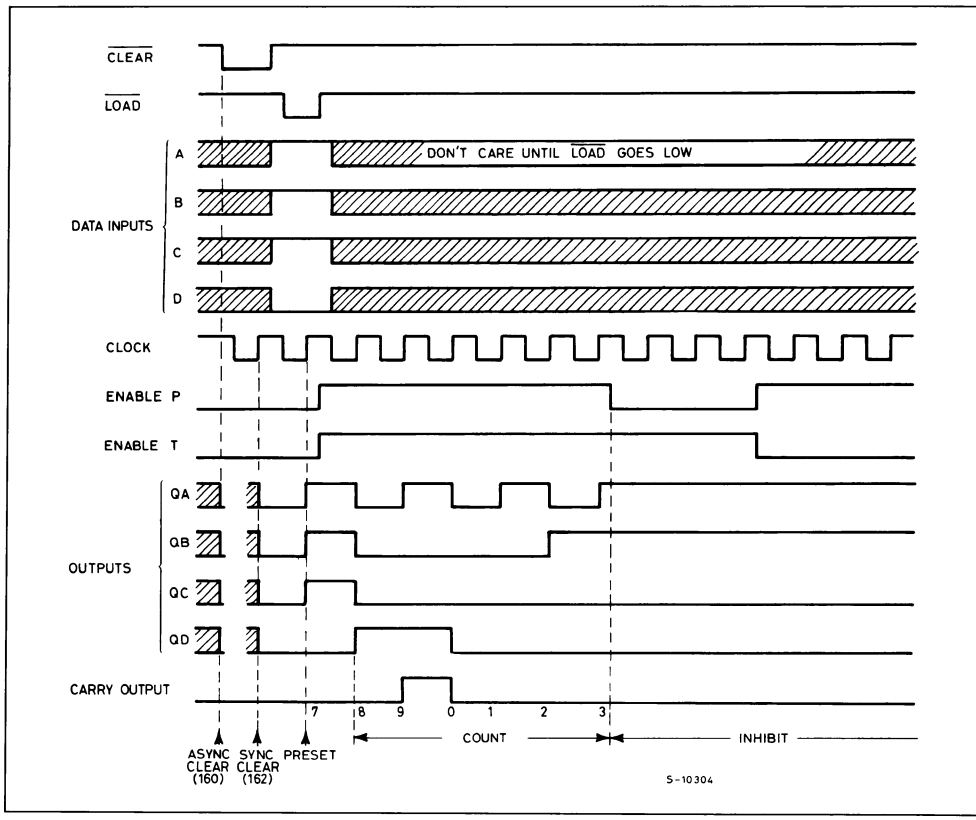
The M54/74HC160, 161, 162 and 163 are high speed CMOS SYNCHRONOUS PRESETTABLE COUNTERS fabricated with silicon gate C²MOS technology.
They have the same the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The M54/74HC160/162 are BCD Decade counters and the M54/74HC161/163 are 4 bit binary counters.
The CLOCK input is active on the rising edge. Both $\overline{\text{LOAD}}$ and $\overline{\text{CLEAR}}$ inputs are active Low.
Presetting of all four IC's is synchronous on the rising edge of the CLOCK.
The function on the M54/74HC162/163 is synchronous to CLOCK, while the M54/74HC160/161 counters are cleared asynchronously.
Two enable inputs (TE and PE) and CARRY output are provided to enable easy cascading of counters, which facilities easy implementation of N-bit counters without using external gates.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

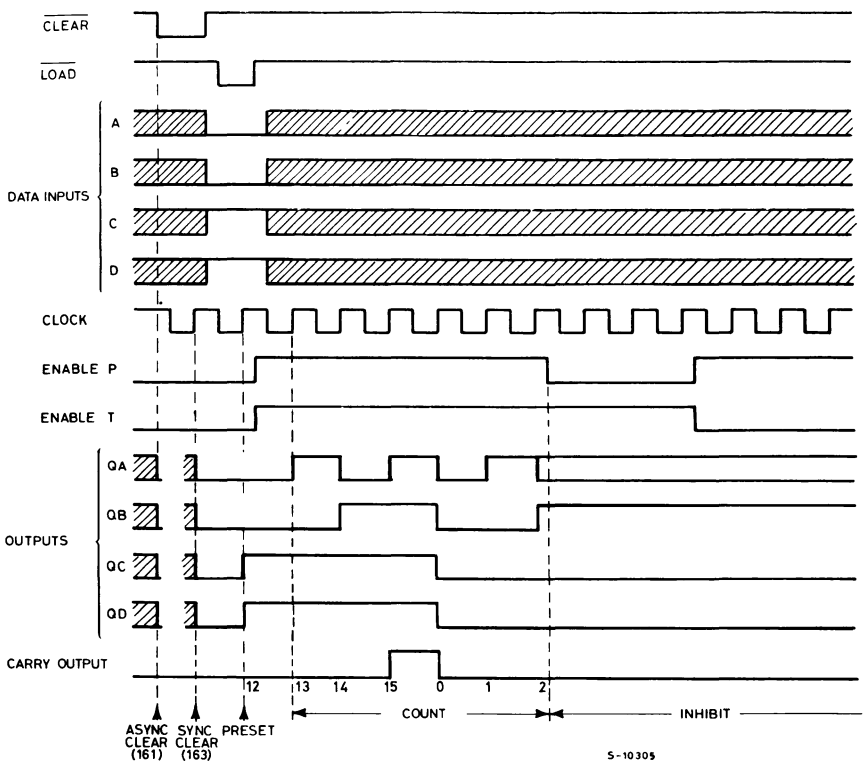
M54/74HC160/161					M54/74HC162/163					OUTPUTS				FUNCTION
INPUTS					INPUTS									
$\overline{CLR}$	$\overline{LD}$	PE	TE	CK	$\overline{CLR}$	$\overline{LD}$	PE	TE	CK	QA	QB	QC	QD	
L	X	X	X	X	L	X	X	X	↑	L	L	L	L	RESET TO "0"
H	L	X	X	↑	H	L	X	X	↑	A	B	C	D	PRESET DATA
H	H	X	L	↑	H	H	X	L	↑	NO CHANGE				NO COUNT
H	H	L	X	↑	H	H	L	X	↑	NO CHANGE				NO COUNT
H	H	H	H	↑	H	H	H	H	↑	COUNT UP				COUNT
H	X	X	X	↓	X	X	X	X	↓	NO CHANGE				NO COUNT

Note X ; DON'T CARE
A, B, C, D ; LOGIC LEVEL OF DATA INPUTS
Carry : CARRY = TE • Q_A • $\overline{Q_B}$ • $\overline{Q_C}$ • Q_D ..... (M54/74HC160/162)
CARRY = TE • Q_A • Q_B • Q_C • Q_D ..... (M54/74HC161/163)

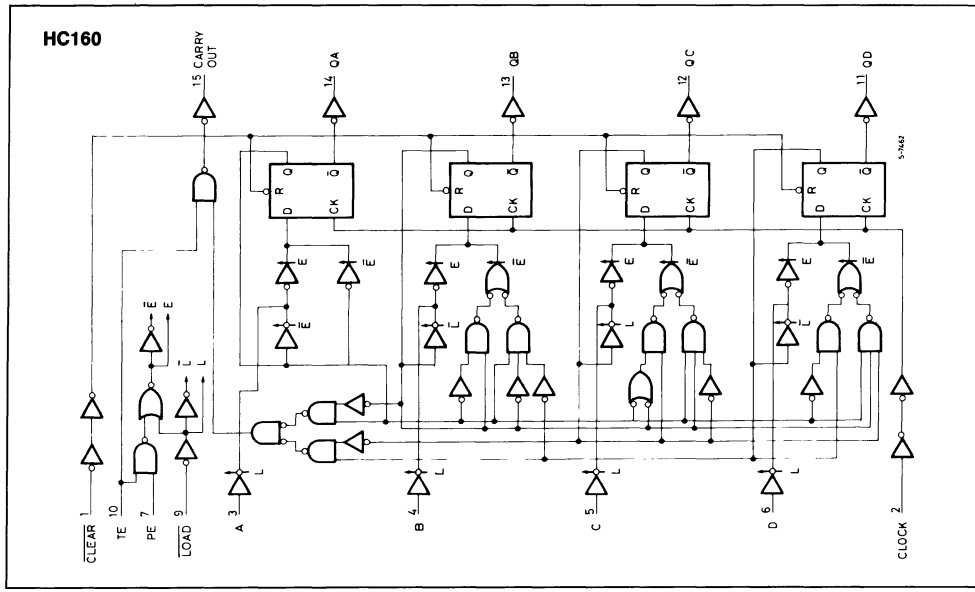
TIMING CHART (HC160/162: DECADE COUNTER)



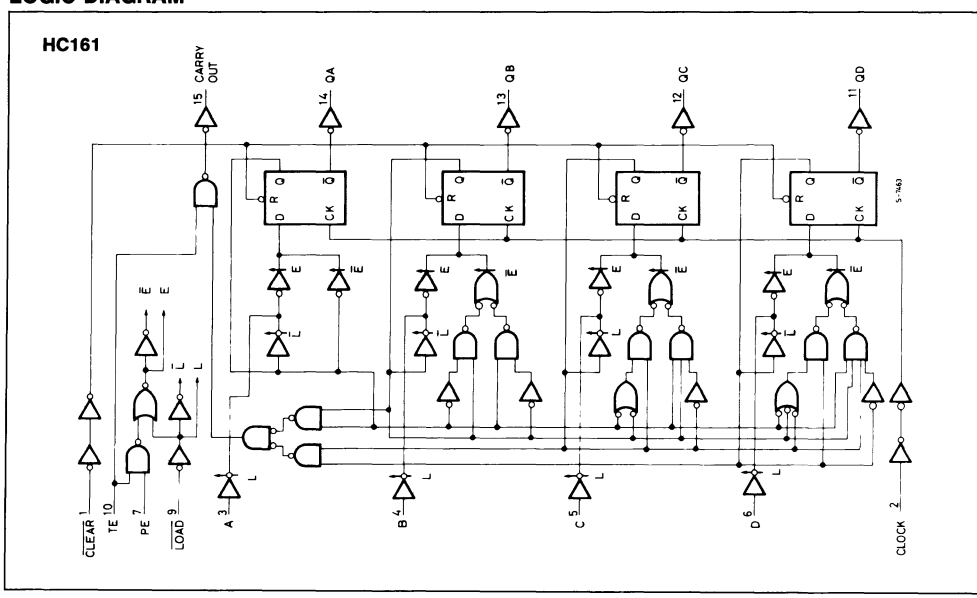
TIMING CHART (HC161/163: BINARY COUNTER)



LOGIC DIAGRAM

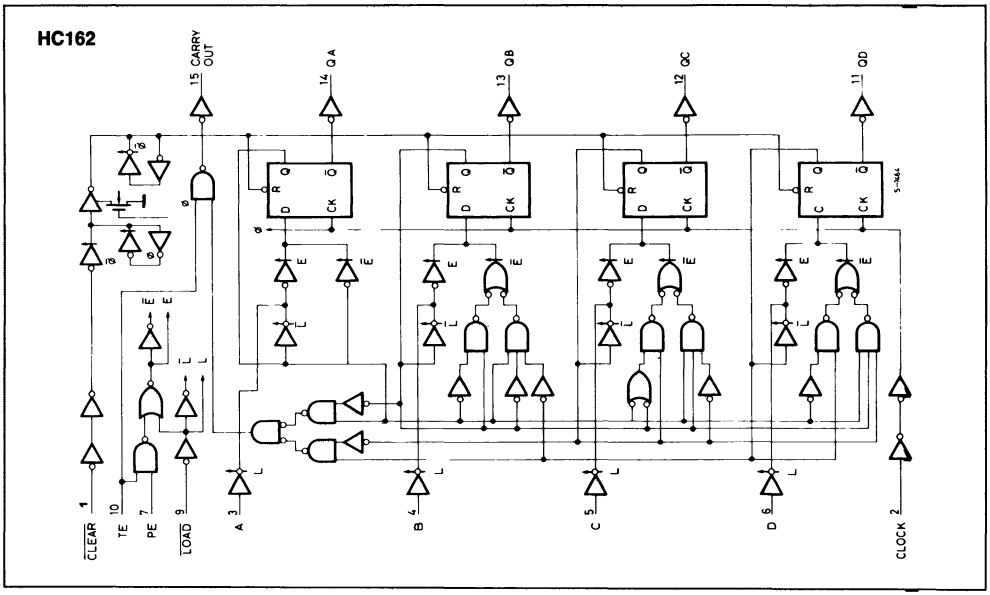


LOGIC DIAGRAM



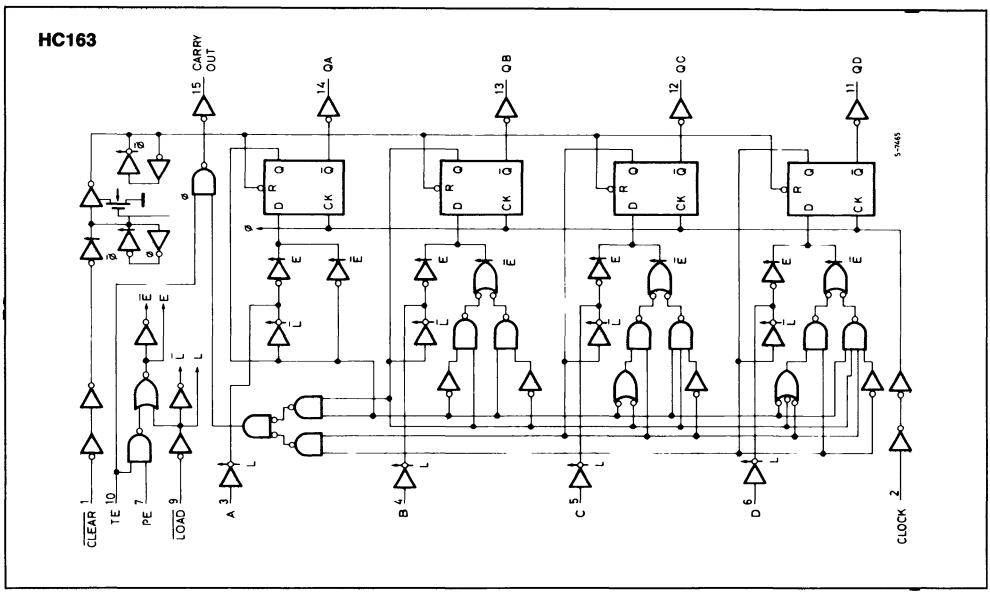
LOGIC DIAGRAM

HC162



LOGIC DIAGRAM

HC163



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

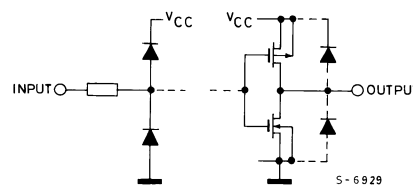
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series Operating Temperature 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Q)		18	28	ns
t_{PHL} t_{PHL}	Propagation Delay Time (CLOCK-CARRY)		22	35	ns
t_{PLH} t_{PHH}	Propagation Delay Time (TE-CARRY)		10	17	ns
t_{PHL}	Propagation Delay ($\overline{CLEAR}$-Q)*		21	33	ns
t_{PHL}	Propagation Delay time ($\overline{CLEAR}$-CARRY)		23	37	ns
f_{MAX}	Maximum Clock Frequency	30	50		MHz

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q)	2.0		—	88	165	—	205	—	250	ns
		4.5		—	22	33	—	41	—	50	
		6.0		—	19	28	—	35	—	43	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-CARRY)	2.0		—	104	200	—	250	—	300	ns
		4.5		—	26	40	—	50	—	60	
		6.0		—	22	34	—	43	—	51	
t_{PLH} t_{PHL}	Propagation Delay Time (TE-CARRY)	2.0		—	52	100	—	125	—	150	ns
		4.5		—	13	20	—	25	—	30	
		6.0		—	11	17	—	21	—	26	
t_{PHL}	Propagation Delay Time ($\overline{\text{CLEAR}}$-Q)•	2.0		—	100	185	—	230	—	280	ns
		4.5		—	25	37	—	46	—	56	
		6.0		—	21	31	—	39	—	48	
t_{PHL}	Propagation Delay Time ($\overline{\text{CLEAR}}$-CARRY)•	2.0		—	112	210	—	265	—	315	ns
		4.5		—	28	42	—	53	—	63	
		6.0		—	24	36	—	45	—	54	
f_{MAX}	Maximum Clock Frequency	2.0		5.4	11	—	4.4	—	3.5	—	MHz
		4.5		27	45	—	22	—	18	—	
		6.0		32	53	—	26	—	21	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{\text{CLEAR}}$)•	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-up Time ($\overline{\text{LOAD}}$ PE, TE	2.0		—	50	125	—	155	—	190	ns
		4.5		—	13	25	—	31	—	38	
		6.0		—	11	21	—	26	—	22	
t_s	Minimum Set-up Time (A,B,C,D)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-up Time ($\overline{\text{CLEAR}}$) ••	2.0		—	35	75	—	95	—	110	ns
		4.5		—	9	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_h	Minimum Hold Time	2.0		—	—	0	—	0	0	0	ns
		4.5		—	—	0	—	0	0	0	
		6.0		—	—	0	—	0	0	0	

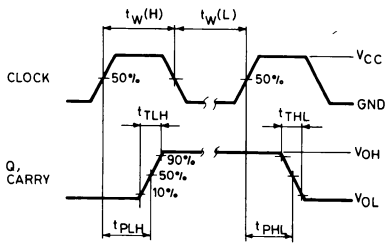
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{REM}	Minimum	2.0		—	5	50	—	65	—	75	
	Time	4.5		—	1	10	—	13	—	15	ns
	(CLEAR)•	6.0		—	1	9	—	11	—	13	
C_{IN}	Input Capacitance			—	5	7.5	—	7.5	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance			—	57	—	—	—	—	—	pF

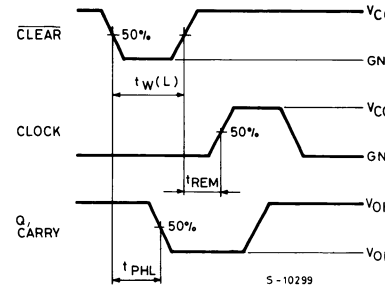
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the following equation.
I_{CC} (Opr) = C_{PD} • V_{CC} • f_{IN} + I_{CC} •: for M54/74HC160/161 only ••: for M54/74HC162/163 only

SWITCHING CHARACTERISTICS TEST WAVEFORM

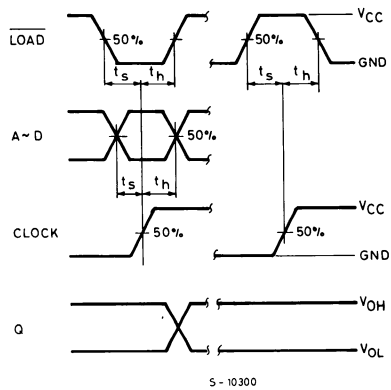
COUNT MODE



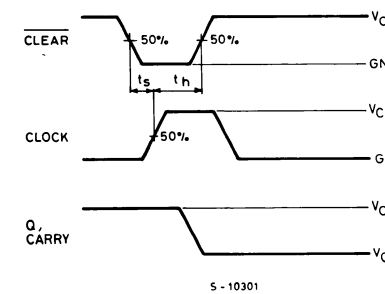
CLEAR MODE (HC160/161)



PRESET MODE

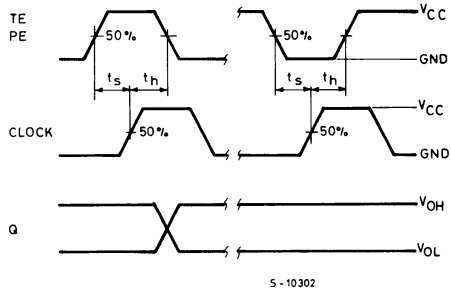


CLEAR MODE (HC162/163)

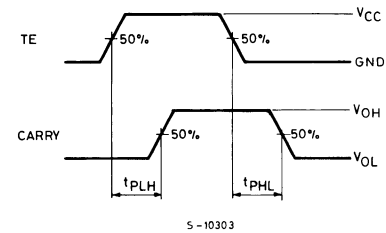


SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)

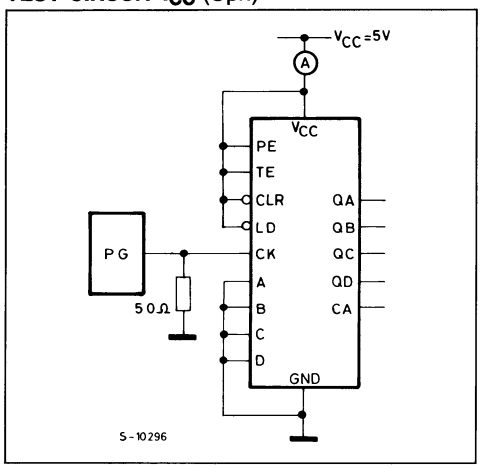
COUNT ENABLE MODE



CASCADE MODE
(Fix Maximum Count)



TEST CIRCUIT I_{CC} (Opr.)



TOTAL OPERATING CURRENT WHEN USING A CAPACITIVE LOAD

When the outputs drive a capacitive load, the total current can be calculated as follows:
For M74HC160/162:

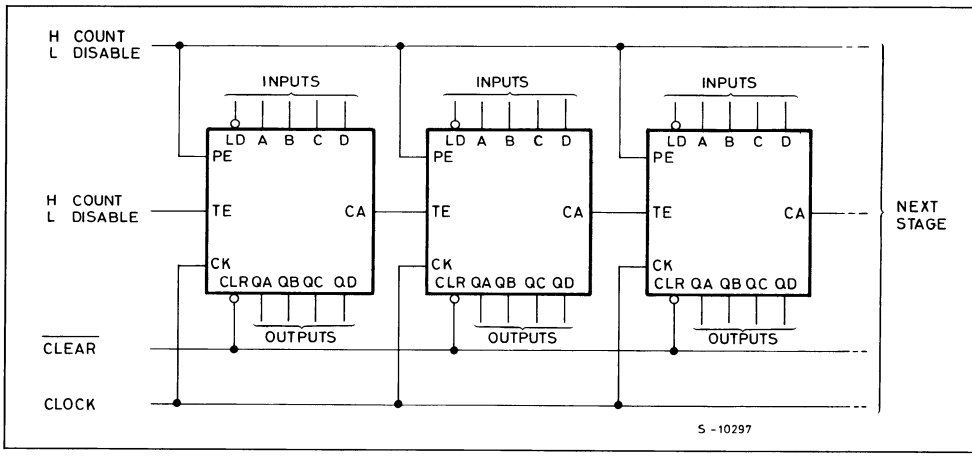
$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \cdot \left(\frac{C_a}{2} + \frac{C_b}{5} + \frac{C_c}{10} + \frac{C_d}{10} + \frac{C_{ca}}{10} \right)$$

For M74HC161/163

$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \cdot \left(\frac{C_a}{2} + \frac{C_b}{4} + \frac{C_c}{8} + \frac{C_d}{16} + \frac{C_{ca}}{16} \right)$$

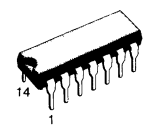
C_a to C_{ca} are the capacitors loading the outputs.

TYPICAL APPLICATION

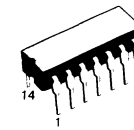


8 BIT SIPO SHIFT REGISTER

- HIGH SPEED
  t_{PD} = 18 ns (TYP) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA at T_A = 25°C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- SYMMETRICAL OUTPUT IMPEDANCE
  I_{OL} = I_{OH}
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS164



B1N
Plastic Package



F1
Ceramic Frit Seal Package

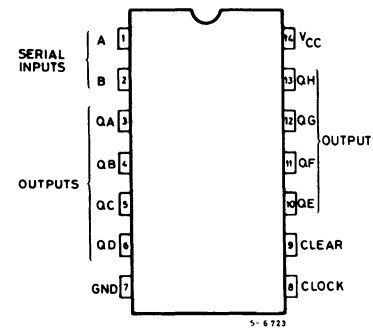
M1
Micro Package

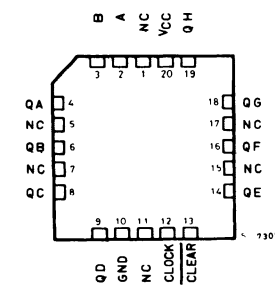
C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC164 F1
M74HC164 B1N
M74HC164 F1
M74HC164 C1
M74HC164 M1

PIN CONNECTIONS (top view)





NC = No Internal Connection

DESCRIPTION

The M54/74HC164 is a high speed CMOS 8 BIT SIPO SHIFT REGISTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

The HC164 is an 8 bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B), either of these inputs can be used as an active high enable for data entry through the other input. An unused input must be high, or both inputs connected together. Each low-to-high transition on the clock input shifts data one place to the right and enters into QA, the logic NAND of the two data inputs ($\overline{A \cdot B}$), the data that existed before the rising clock edge. A low level on the clear input overrides all other inputs and clears the register asynchronously, forcing all Q outputs low.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

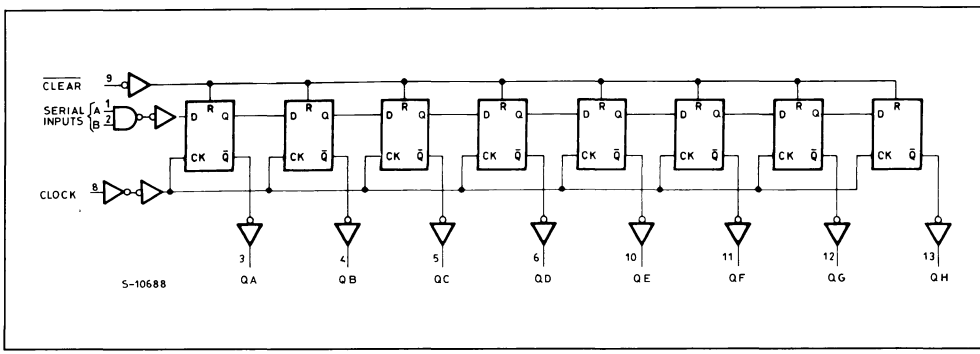
TRUTH TABLE

INPUTS				OUTPUTS			
$\overline{CLEAR}$	CLOCK	SERIAL IN		QA	QB	.....	QH
		A	B				
L	X	X	X	L	L	.....	L
H	↓	X	X	NO CHANGE			
H	↑	L	X	L	QAn	.....	QGn
H	↑	X	L	L	QAn	.....	QGn
H	↑	H	H	H	QAn	.....	QGn

X : DON'T CARE

QAn ~ QGn : THE LEVEL OF QA ~ QG, RESPECTIVELY, BEFORE THE MOST-RECENT POSITIVE TRANSITION OF THE CLOCK.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current Per Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

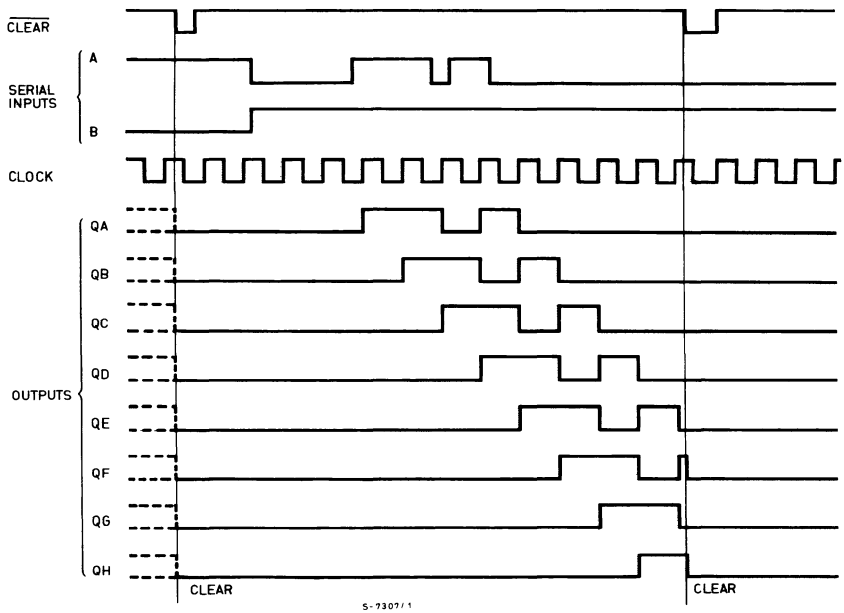
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−55 to 125 −40 to 85		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V 4.5V 6 V	0 to 1000 0 to 500 0 to 400	ns

TIMING CHART



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK-Q)		18	29	ns
t_{PHL}	Propagation Delay Time (CLEAR-Q)		19	30	ns
f_{MAX}	Maximum Clock Frequency	30	51		Mhz

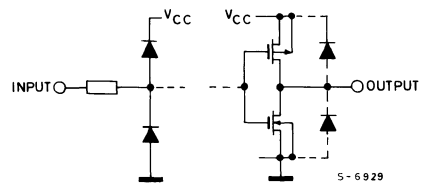
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q)	2.0		—	88	175	—	220		260	ns
		4.5		—	22	35	—	44		52	
		6.0		—	19	30	—	37		44	
t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$-Q)	2.0		—	92	180	—	225		270	ns
		4.5		—	23	36	—	45		54	
		6.0		—	20	31	—	38		46	
f_{MAX}	Maximum Clock Frequency	2.0		5	9	—	4	—	3	—	MHz
		4.5		27	46	—	22	—	18	—	
		6.0		32	54	—	26	—	21	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLEAR}$)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_s	Minimum Set-up Time (A, B)	2.0		—	25	75	—	95		110	ns
		4.5		—	7	15	—	19		22	
		6.0		—	6	13	—	16		19	
t_h	Minimum Hold Time (A, B)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{REM}	Minimum Removal Time ($\overline{CLEAR}$)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	112	—	—	—			pF

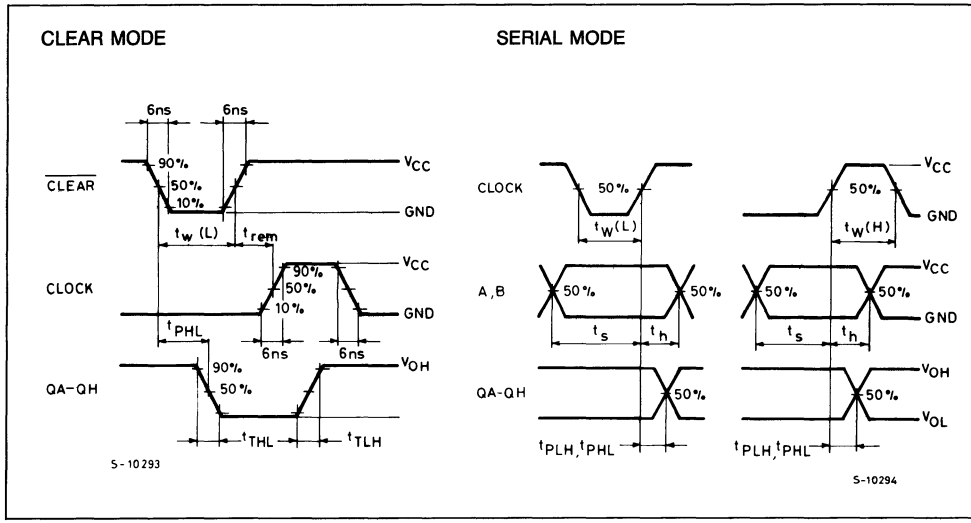
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current is: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

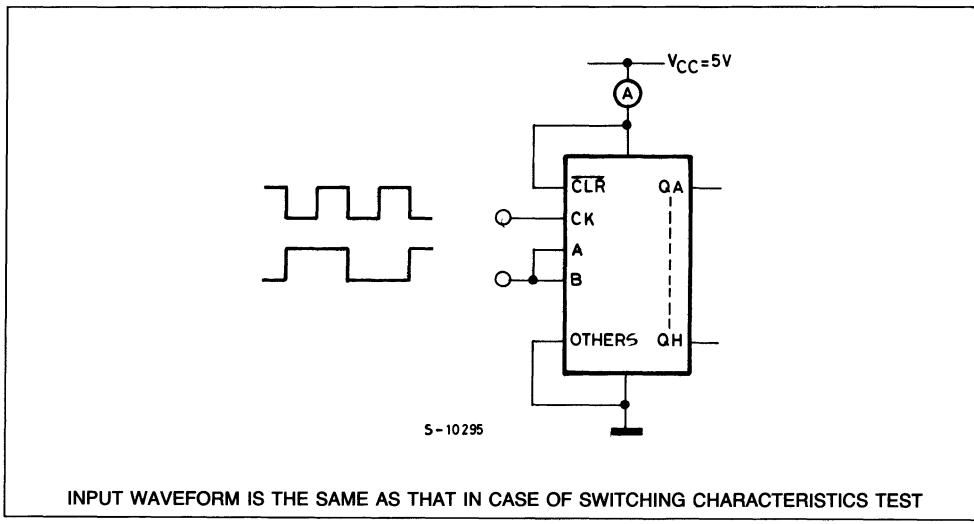
INPUT AND OUTPUT EQUIVALENT CIRCUIT



SWITCHING CHARACTERISTICS TEST WAVEFORM



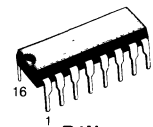
TEST CIRCUIT I_{CC} (Opr.)



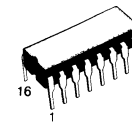
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

8-BIT PISO SHIFT REGISTER

- HIGH SPEED
  t_{PD} = 21 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS165



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC165 F1
M74HC165 B1N
M74HC165 F1
M74HC165 C1
M74HC165 M1

DESCRIPTION

The M54/74HC165 is a high speed CMOS 8-BIT PISO SHIFT REGISTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low consumption.

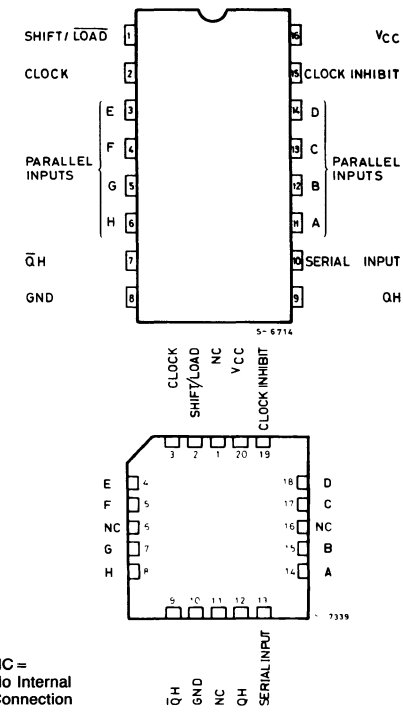
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This device contains eight clocked master-slave RS flip-flops connected as a shift register, with auxiliary gating to provide over-riding asynchronous parallel entry. Parallel data enters when the shift/load input is low. The parallel data can change while shift/load is low, provided that the recommended set-up and hold times are observed. For clocked operation, shift/load must be high. The two clock inputs perform identically; one can be used as a clock inhibit by applying a high signal; to permit this operation clocking is accomplished through a 2 input nor gate.

To avoid double clocking, however, the inhibit signal should only go high while the clock is high. Otherwise the rising inhibit signal will cause the same response as rising clock edge.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)

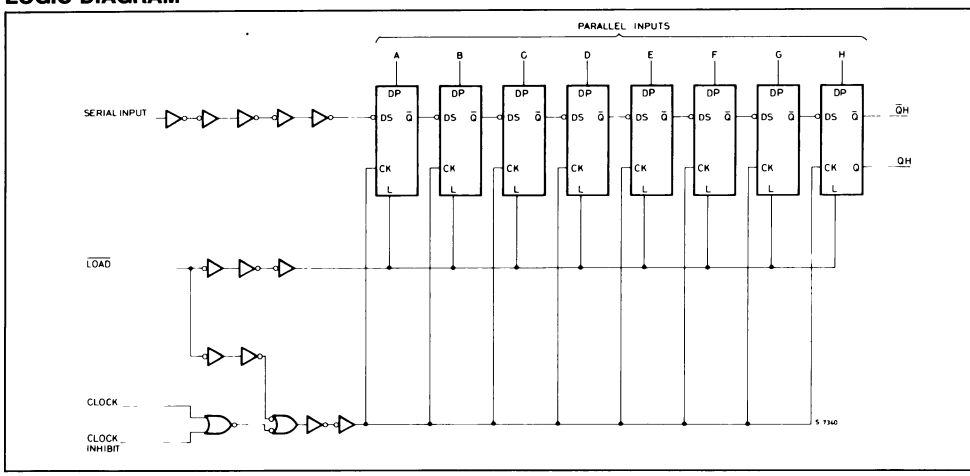


TRUTH TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL IN	PARALLEL A.....H	QA	QB	QH
L	X	X	X	a.....h	a	b	h
H	L	↑	H	X	H	QAn	QGn
H	L	↑	L	X	L	QAn	QGn
H	↓	L	H	X	H	QAn	QGn
H	↓	L	L	X	L	QAn	QGn
H	X	H	X	X	NO CHANGE		
H	H	X	X	X	NO CHANGE		

a.....h: THE LEVEL OF STEADY INPUT VOLTAGE AT INPUTS A THROUGH H RESPECTIVELY
QAn...QGn: THE LEVEL OF QA ~ QG, RESPECTIVELY, BEFORE THE MOST-RECENT POSITIVE TRANSITION OF THE CLOCK.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

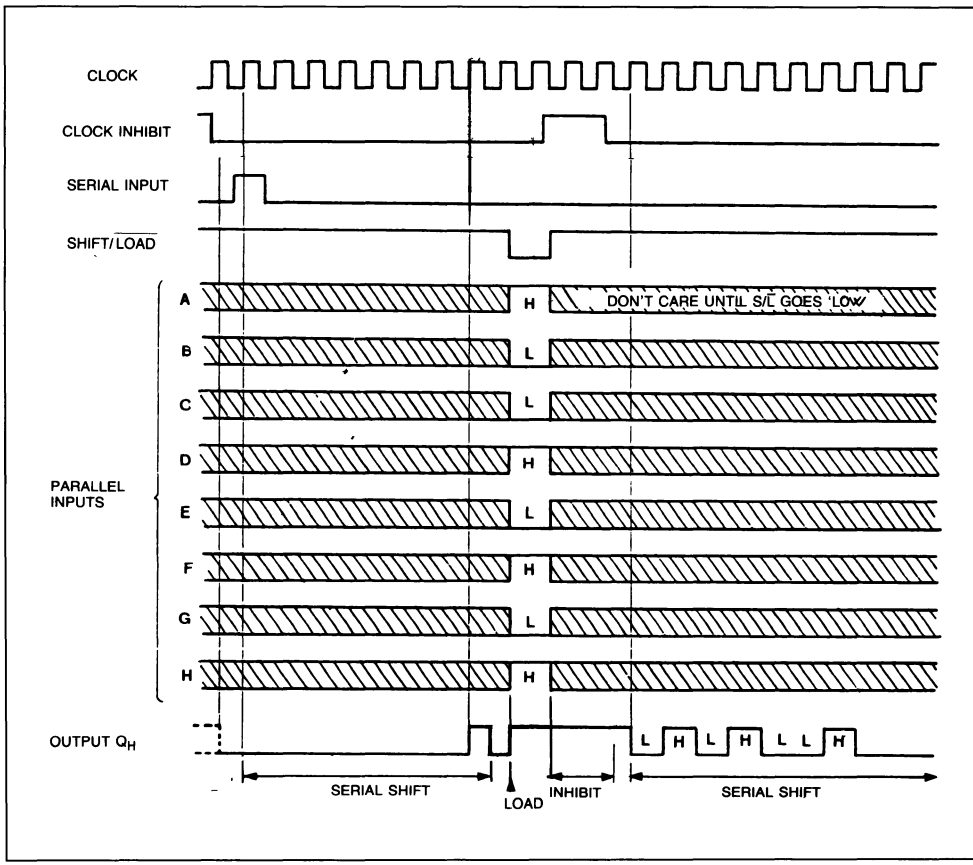
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied. (*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V: 0 to 1000 V_{CC} = 4.5V: 0 to 500 V_{CC} = 6 V: 0 to 400	ns

TIMING CHART



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0.0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - QH - $\overline{QH}$)		21	33	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($CLOCK_{INH}$ - QH, $\overline{QH}$)		21	33	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{S/L}$ - QH, $\overline{QH}$)		22	35	ns
t_{PLH} t_{PHL}	Propagation Delay Time (H_{IN} - QH, $\overline{QH}$)		20	32	ns
f_{MAX}	Maximum Clock Frequency	28	48		MHz

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

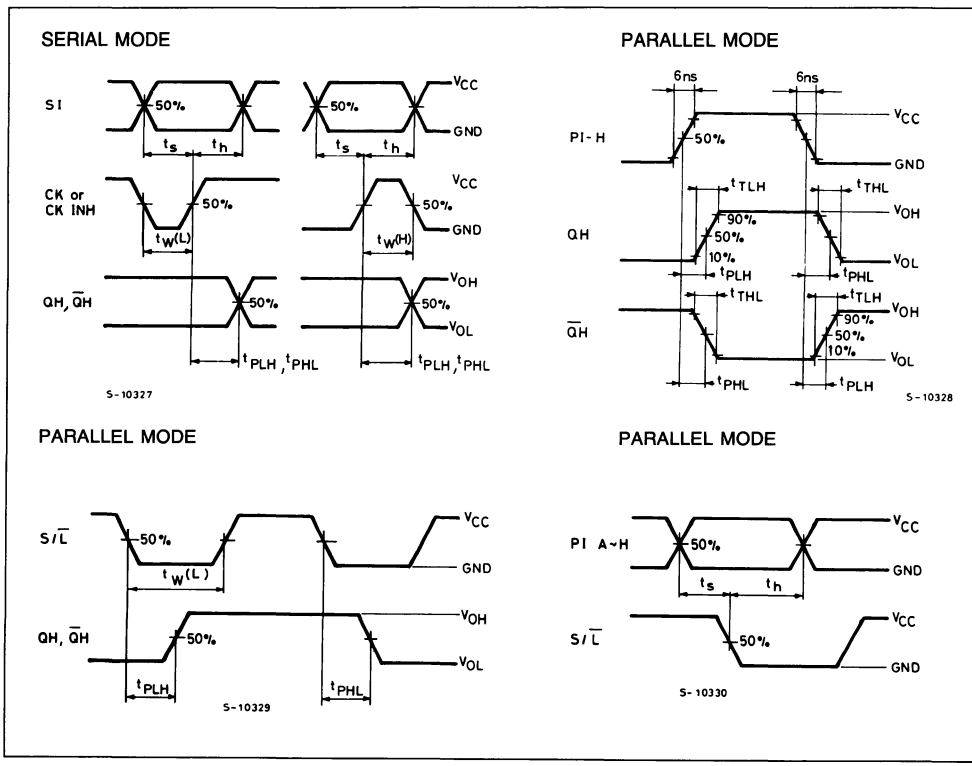
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CK-QH, $\overline{QH}$)	2.0		—	96	190	—	240		285	ns
		4.5		—	24	38	—	48		57	
		6.0		—	20	32	—	41		48	
t_{PLH} t_{PHL}	Propagation Delay Time (CK_{INH} QH, $\overline{QH}$)	2.0		—	96	190	—	240		285	ns
		4.5		—	24	38	—	48		57	
		6.0		—	20	32	—	41		48	
t_{PLH} t_{PHL}	Propagation Delay Time ($S/\overline{L}$ - QH - $\overline{QH}$)	2.0		—	104	200	—	250	—	300	ns
		4.5		—	26	40	—	50	—	60	
		6.0		—	22	34	—	43	—	51	
t_{PLH} t_{PHL}	Propagation Delay Time (H - QH, $\overline{QH}$)	2.0		—	92	180	—	225	—	270	ns
		4.5		—	23	36	—	45	—	54	
		6.0		—	20	31	—	38	—	46	
f_{MAX}	Maximum Clock Frequency	2.0		5	11	—	4	—	3.4	—	MHz
		4.5		25	44	—	20	—	17	—	
		6.0		29	52	—	24	—	20	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CK, CK_{INH})	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
$t_{W(L)}$	Minimum Pulse Width ($S/\overline{L}$)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_s	Minimum Set-up Time ($S/\overline{L}$-CK, CK_{INH})	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-up Time (PI-$S/\overline{L}$)	2.0		—	15	50	—	65		75	ns
		4.5		—	3	10	—	13		15	
		6.0		—	3	9	—	11		13	
t_s	Minimum Set-up Time (SI-CK, CK_{INH})	2.0		—	10	50	—	65		75	ns
		4.5		—	2	10	—	13		15	
		6.0		—	2	9	—	11		13	
t_h	Minimum Hold Time (PI-$S/\overline{L}$)	2.0		—	—	5	—	5	—	5	ns
		4.5		—	—	5	—	5	—	5	
		6.0		—	—	5	—	5	—	5	
t_h	Minimum Hold Time (SI-CK, CK_{INH})	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	

AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{REM}	Minimum Removal Time (CK_{INH}-CK) (CK-CK_{INH})	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 16	ns
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	95	—	—	—			pF

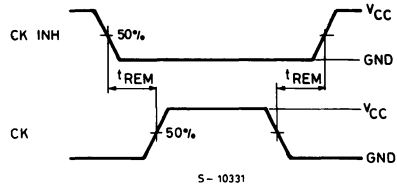
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the following equation.
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

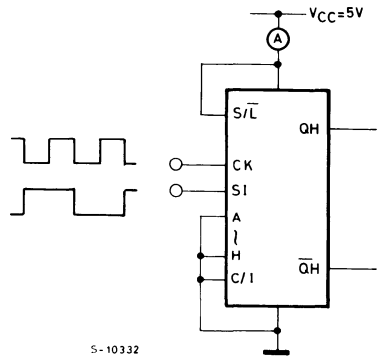


SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)

SERIAL MODE



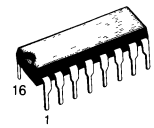
TEST CIRCUIT I_{CC} (Opr.)



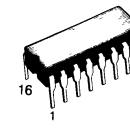
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

8 BIT PISO SHIFT REGISTER

- HIGH SPEED
  f_{MAX} = 50 MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS166



B1N
Plastic Package



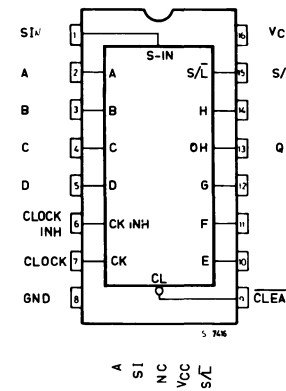
F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC166 F1
M74HC166 B1N
M74HC166 F1
M74HC166 C1
M74HC166 M1

PIN CONNECTIONS (top view)



NC = No Internal Connection

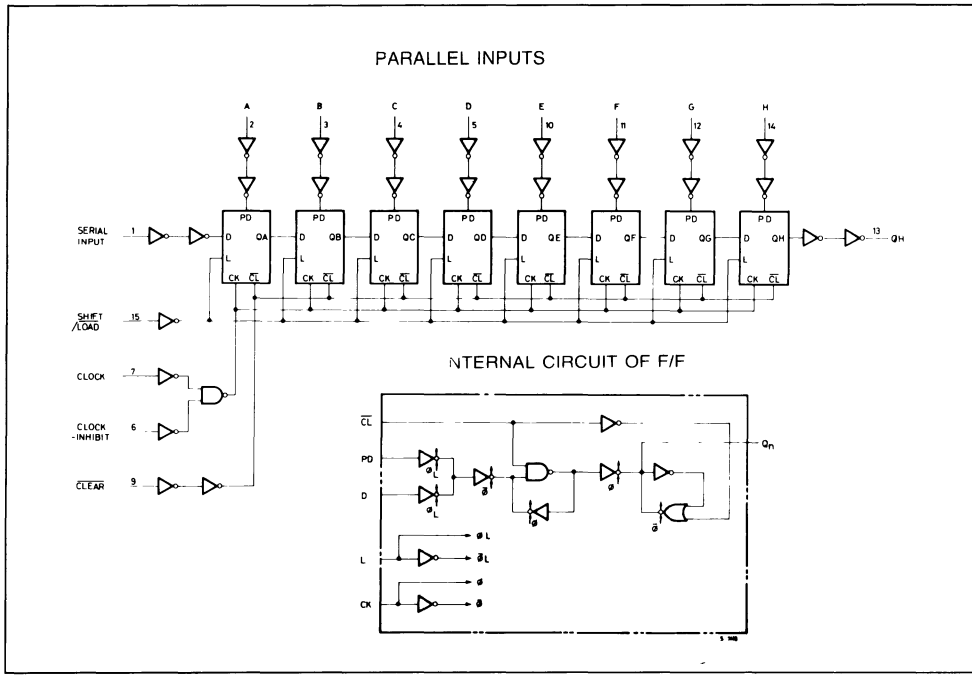
DESCRIPTION

The M54/74HC166 is a high speed C²MOS 8 BIT PISO SHIFT REGISTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

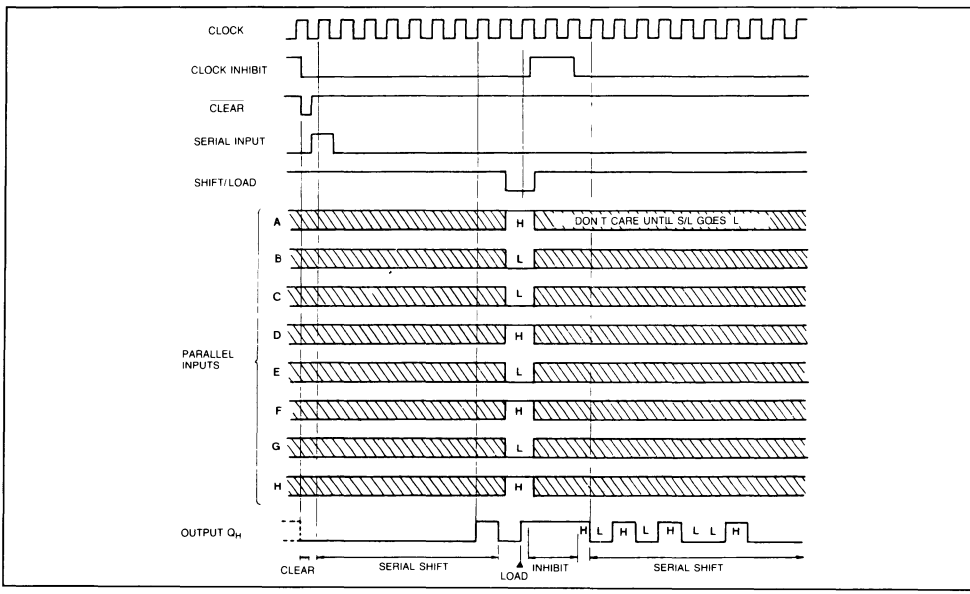
It consists of parallel or serial inputs and a serial-out 8-bit shift register with gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are controlled by the SHIFT/$\overline{\text{LOAD}}$ input. When the SHIFT/$\overline{\text{LOAD}}$ input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting with each clock pulse. When held low, the parallel data inputs are enabled and synchronous loading occurs on the next clock pulse. Clocking is accomplished on the low-to-high level edge of the clock pulse. The CLOCK-INHIBIT input should be changed to the high only while the CLOCK input is held high. A direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero. Functional details are shown in the truth table and the timing chart.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

LOGIC DIAGRAM



TIMING CHART



TRUTH TABLE

INPUTS						INTERNAL OUTPUTS		OUTPUT
$\overline{CLEAR}$	SHIFT/$\overline{LOAD}$	CLOCK INH.	CLOCK	SERIAL IN	PARALLEL A·····H	QA	QB	QH
L	X	X	X	X	X	L	L	L
H	X	X	↓	X	X	NO CHANGE		
H	L	L	↑	X	a ..... h	a	b	h
H	H	L	↑	H	X	H	QAn	QGn
H	H	L	↑	L	X	L	QAn	QGn
H	X	H	X	X	X	NO CHANGE		

X: DON'T CARE

a·····h : THE LEVEL OF STEADY STATE INPUT VOLTAGE AT INPUTS A TROUGH H RESPECTIVELY

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0.0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-QH)		16	25	ns
t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$-QH)		16	25	ns
f_{MAX}	Maximum Clock frequency	33	55		MHz

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

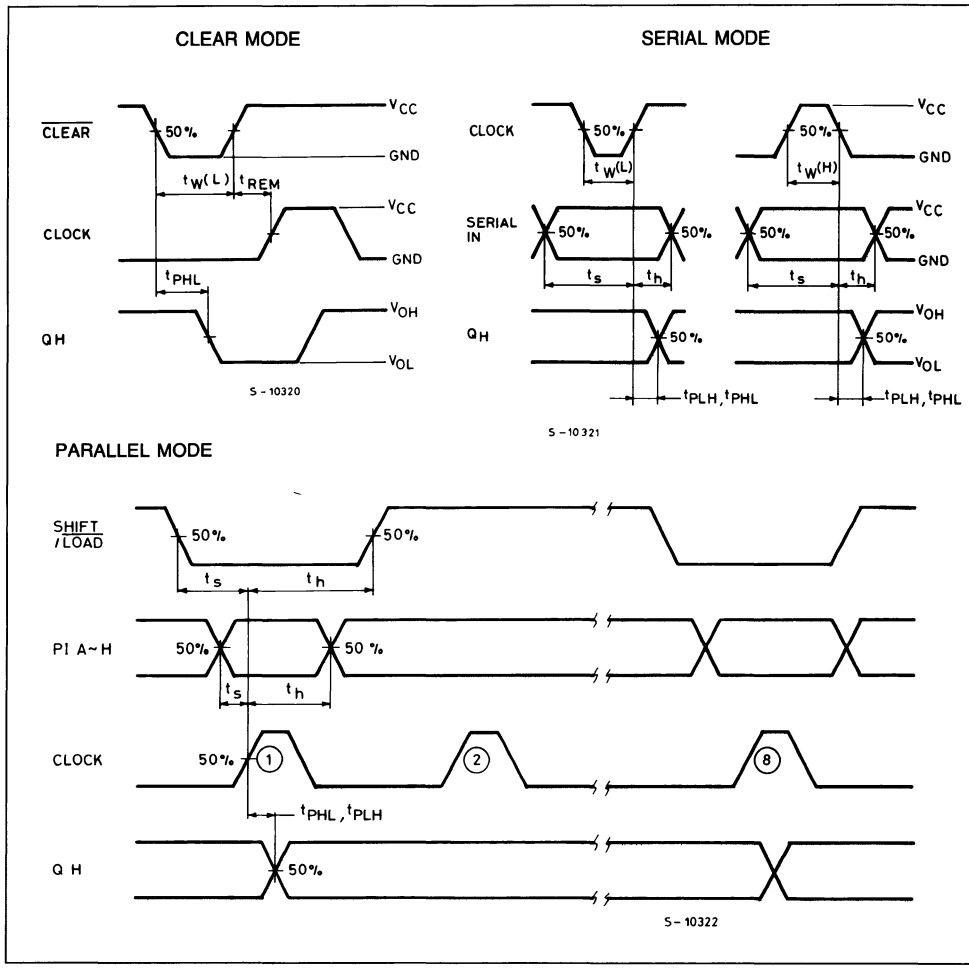
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - QH)	2.0		—	80	150	—	190		225	ns
		4.5		—	20	30	—	38		45	
		6.0		—	17	26	—	33		38	
t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$-QH)	2.0		—	76	150	—	190		225	ns
		4.5		—	19	30	—	38		45	
		6.0		—	16	26	—	32		38	
f_{MAX}	Maximum Clock Frequency	2.0		6	14	—	4.8	—	3.8	—	MHz
		4.5		30	50	—	24	—	19	—	
		6.0		35	60	—	28	—	22	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLEAR}$)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{REM}	Minimum Removal Time ($\overline{CLEAR}$)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_s	Minimum Set-up Time (SI, PI)	2.0		—	20	75	—	95		110	ns
		4.5		—	5	15	—	19		22	
		6.0		—	4	13	—	16		19	
t_s	Minimum Set-up Time ($S/\overline{L}$)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_h	Minimum Hold Time (SI, PI)	2.0		—	—	50	—	65	—	75	ns
		4.5		—	—	10	—	13	—	15	
		6.0		—	—	9	—	11	—	13	
t_h	Minimum Hold Time ($S/\overline{L}$)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	58	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

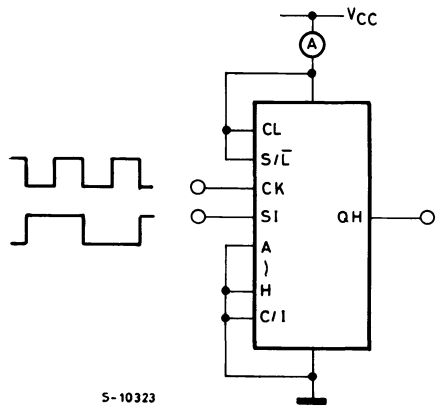
Average operating current can be obtained by the following equation.

$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

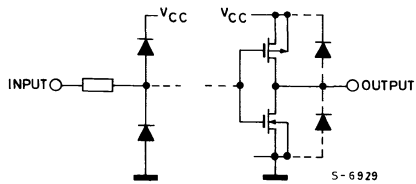


TEST CIRCUIT I_{CC} (Opr.)



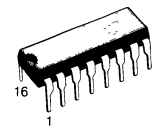
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

INPUT AND OUTPUT EQUIVALENT CIRCUIT

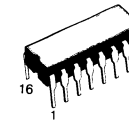


QUAD D-TYPE REGISTER (3-STATE)

- HIGH SPEED
  f_{MAX} = 52 MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (Min.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS173



B1N
Plastic Package



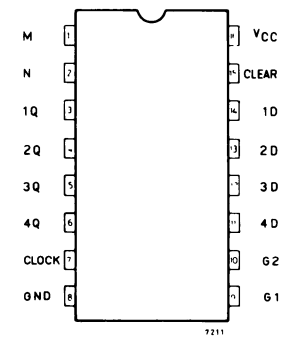
F1
Ceramic Frit Seal Package

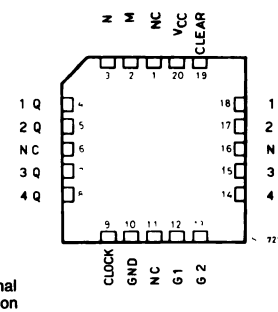
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HCT173 F1
M74HCT173 B1N
M74HCT173 F1
M74HCT173 C1
M74HCT173 M1

PIN CONNECTIONS (top view)





NC = No Internal Connection

DESCRIPTION

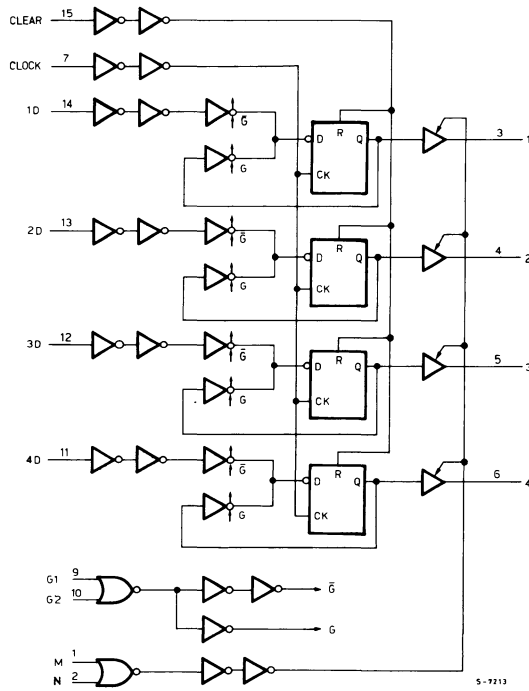
The M54/74HC173 is a high speed CMOS QUAD D-TYPE REGISTER (3-STATE) fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device is composed of a four-bit register including D-type flip-flops and 3-state buffers. The four flip-flops are controlled by a common clock input (CLOCK) and a common reset input (CLEAR). Signals applied to the data inputs (D_1-D_4) are stored at the respective flip-flops on the positive going transition of the clock input, only when both clock control inputs (G_1 and G_2) are held low.
The reset feature is asynchronous and active high. The stored data are provided on each output only when both output control inputs (M and N) are held low, otherwise the outputs go to the high-impedance state.
All inputs are equipped with protection circuits against static discharge and trasient excess voltage.

TRUTH TABLE

CLEAR	CLOCK	DATA ENABLE		Dn	OUTPUT CONTROL		Qn
		G1	G2		M	N	
X	X	X	X	X	H	X	Z
X	X	X	X	X	X	H	Z
H	X	X	X	X	L	L	L
L	↓	X	X	X	L	L	Q0
L	↑	H	X	X	L	L	Q0
L	↑	X	H	X	L	L	Q0
L	↑	L	L	H	L	L	H
L	↑	L	L	L	L	L	L

X: DON'T CARE Z: HIGH IMPEDANCE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

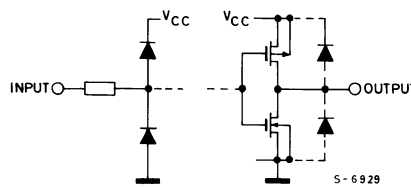
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series Operating Temperature 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		6.0 mA	—	0.17	0.26	—	0.37	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.37	—	0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1		±1	μA
I_{OZ}	3-State Output Off-State Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±10	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND		—	—	4	—	40		80	μA

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

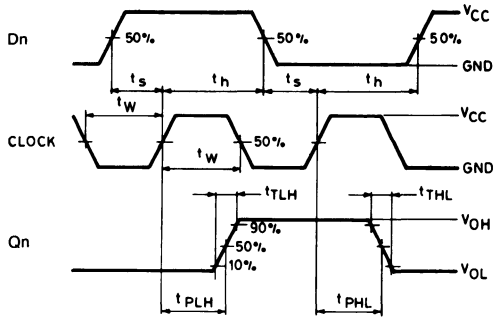
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	25	60	—	75		90	ns
		4.5		—	7	12	—	15		18	
		6.0		—	6	10	—	13		15	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q)	2.0		—	84	165	—	205		250	ns
		4.5		—	21	33	—	41		50	
		6.0		—	18	28	—	35		43	
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR-Q)	2.0		—	84	165	—	205		250	ns
		4.5		—	21	33	—	41		50	
		6.0		—	18	28	—	35		43	
f_{MAX}	Maximum Clock Frequency	2.0		6	12	—	4.8	—	4.0	—	MHz
		4.5		30	50	—	24	—	20	—	
		6.0		35	59	—	28	—	24	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{REM}	Minimum Removal Time (CLEAR)	2.0		—	—	5	—	5		5	ns
		4.5		—	—	5	—	5		5	
		6.0		—	—	5	—	5		5	
t_s	Minimum Set-up Time (G_1, G_2)	2.0		—	40	100	—	125		150	ns
		4.5		—	10	20	—	25		30	
		6.0		—	9	17	—	21		26	
t_s	Minimum Set-up Time (D)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_h t_h	Minimum Hold Time (G_1,G_2,D)	2.0		—	—	0	—	0		0	ns
		4.5		—	—	0	—	0		0	
		6.0		—	—	0	—	0		0	
t_{PZL} t_{PZH}	3-State Output Enable Time	2.0	R_L = 1 KΩ	—	65	120	—	150		180	ns
		4.5		—	13	24	—	30		36	
		6.0		—	11	20	—	26		31	
t_{PLZ} t_{PHZ}	3-State Output Disable Time	2.0	R_L = 1 KΩ	—	84	150	—	190		225	ns
		4.5		—	21	30	—	38		45	
		6.0		—	18	26	—	33		38	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{OUT}	Output Capacitance			—	10	—	—	—			ns
C_{PD} (*)	Power Dissipation Capacitance			—	35	—	—	—			pF

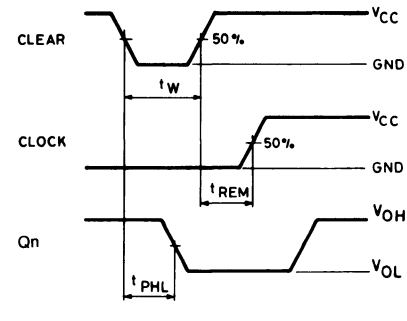
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

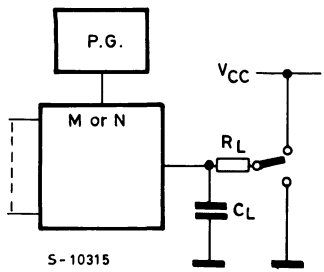
Average operating current can be obtained by the following equation.

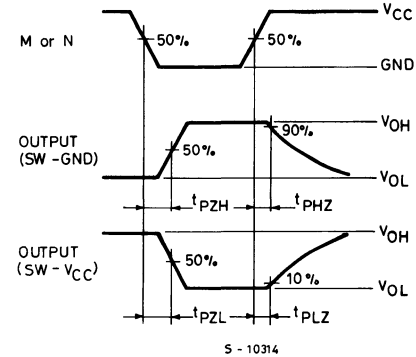
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Circuit)

SWITCHING CHARACTERISTICS TEST WAVEFORM



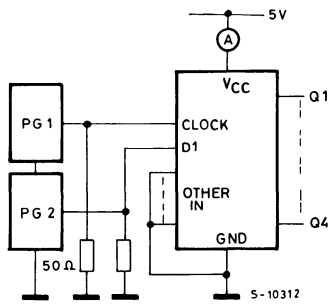


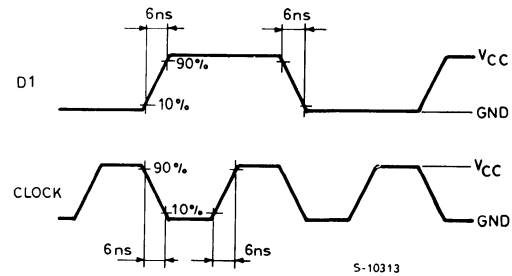




EACH FLIP-FLOP SHALL BE SET HIGH WHEN SWITCH IS CONNECTED TO GND LINE AND IT SHALL BE SET LOW WHEN SWITCH IS CONNECTED TO V_{CC} LINE.

TEST CIRCUIT I_{CC} (Opr.)



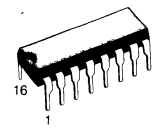


SGS-THOMSON MICROELECTRONICS

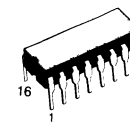
M54HC174
M74HC174

HEX D-TYPE FLIP-FLOP WITH CLEAR

- HIGH SPEED
  f_{MAX} = 48 MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS174



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

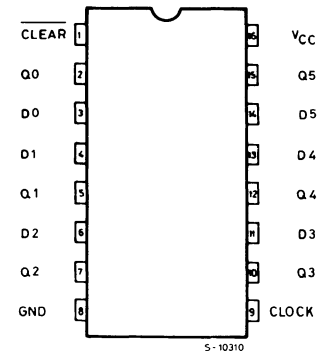
ORDERING NUMBERS:

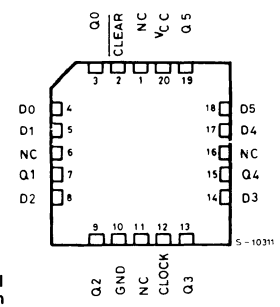
M54HC174 F1
M74HC174 B1N
M74HC174 F1
M74HC174 C1
M74HC174 M1

DESCRIPTION

The M54/74HC174 is a high speed CMOS HEX D-TYPE FLIP-FLOP WITH CLEAR fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
Information signals applied to D inputs are transfered to the Q output on the positive going edge of the clock pulse. When the CLEAR input is held low, the Q outputs are held low independently of the other inputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)





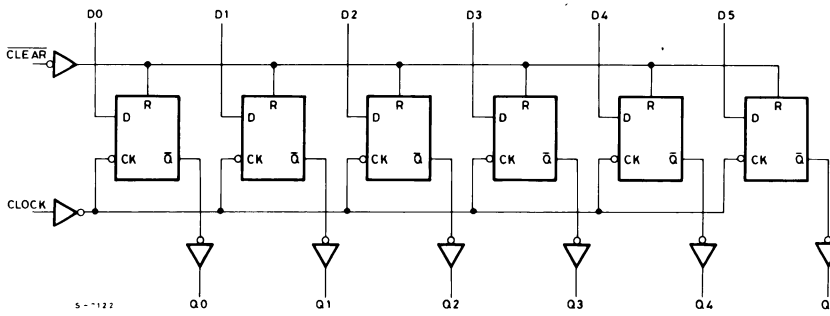
NC = No Internal Connection

TRUTH TABLE

INPUTS			OUTPUT	FUNCTION
CLEAR	D	CLOCK	Q	
L	X	X	L	CLEAR
H	L	↑	L	—
H	H	↑	H	—
H	X	↓	Qn	NO CHANGE

X: DON'T CARE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65 °C to 300 mW by 10 mW/°C: 65 to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V: 0 to 1000 V_{CC} = 4.5V: 0 to 500 V_{CC} = 6 V: 0 to 400	ns

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0.0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK-QH)		19	30	ns
t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$-QH)		19	30	ns
f_{MAX}	Maximum Clock Frequency	30	48		MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

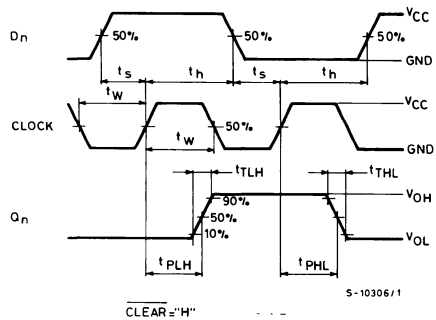
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CK - Q)	2.0		—	92	180	—	225		270	ns
		4.5		—	23	36	—	45		54	
		6.0		—	20	31	—	38		46	
t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$-Q)	2.0		—	92	180	—	225		270	ns
		4.5		—	23	36	—	45		54	
		6.0		—	20	31	—	38		46	
f_{MAX}	Maximum Clock Frequency	2.0		5	11	—	4	—	3	—	MHz
		4.5		27	44	—	22	—	18	—	
		6.0		32	52	—	26	—	21	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
$t_{W(L)}$	Minimum Pulse Width $\overline{CLEAR}$	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_s	Minimum Set-up Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_h	Minimum Hold Time	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{REM}	Minimum Removal Time $\overline{CLEAR}$	2.0		—	16	75	—	95	—	110	ns
		4.5		—	4	15	—	19	—	22	
		6.0		—	3	13	—	16	—	19	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	53	—	—	—			pF

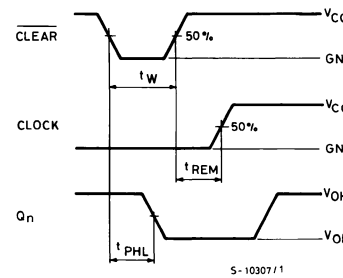
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current is: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per Flip-Flop)

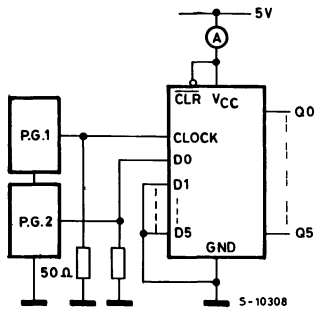
And the total C_{PD} when N pcs of Flip-Flop operate can be gained by the following equation: C_{PD} (total) = 38 + 15•n

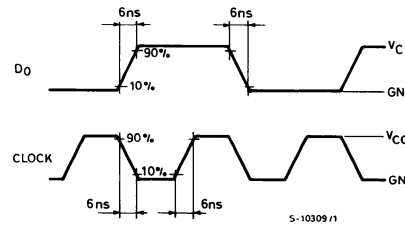
SWITCHING CHARACTERISTICS TEST WAVEFORM





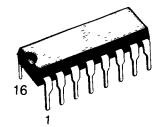
TEST CIRCUIT I_{CC} (Opr.)



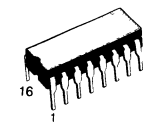


QUAD D-TYPE FLIP-FLOP WITH CLEAR

- HIGH SPEED
  t_{PD} = 18 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS175



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC175 F1
M74HC175 B1N
M74HC175 F1
M74HC175 C1
M74HC175 M1

DESCRIPTION

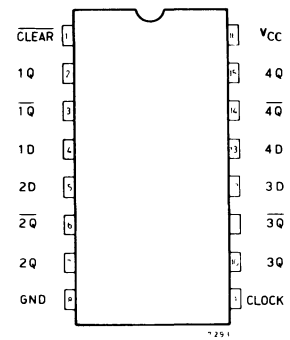
The M54/74HC175 is a high speed CMOS QUAD D-TYPE FLIP-FLOP WITH CLEAR fabricated in silicon gate CMOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
These four flip-flops are controlled by a clock input (CLOCK) and a clear input (CLEAR). The information data applied to the D inputs (1D to 4D) are transfered to the outputs (1Q to 4Q and $\overline{1Q}$ to $\overline{4Q}$) on the positive-going edge of the clock pulse. The reset function is accomplished when the clear input is taken low and all Q outputs are kept low regardless of other input conditions. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

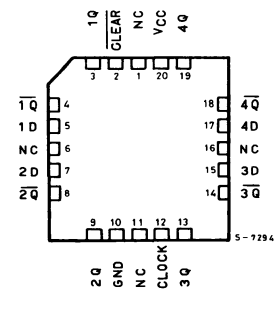
TRUTH TABLE

INPUTS			OUTPUTS		FUNCTION
$\overline{CLEAR}$	D	CLOCK	Q	$\overline{Q}$	
L	X	X	L	H	CLEAR
H	L	↑	L	H	—
H	H	↑	H	L	—
H	X	↓	Qn	$\overline{Qn}$	NO CHANGE

X: DON'T CARE

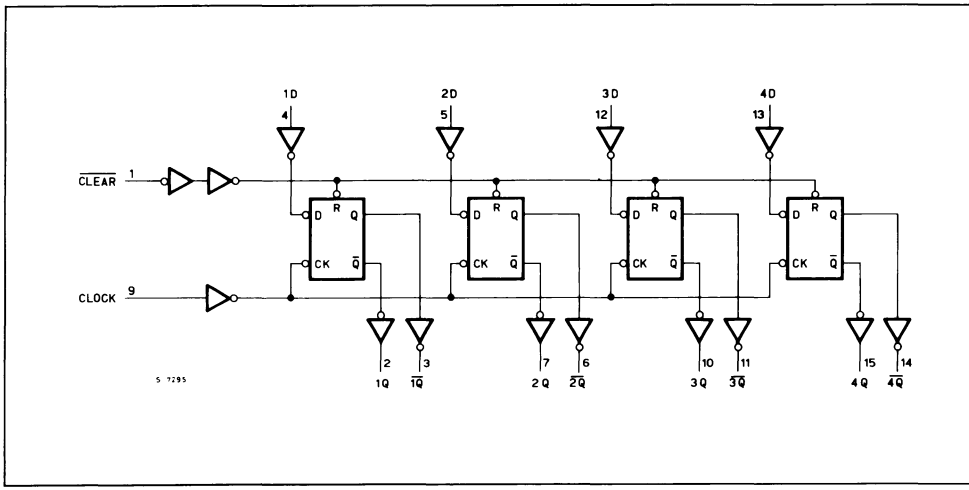
PIN CONNECTIONS (top view)





NC = No Internal Connection

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series Operating Temperature 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Q, $\overline{Q}$)		18	28	ns
t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$-Q, $\overline{Q}$)		20	32	ns
f_{MAX}	Maximum Clock Frequency	33	53		MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

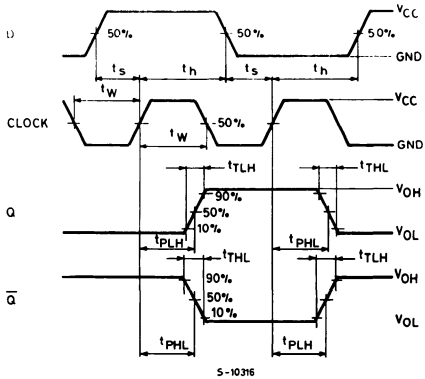
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOCK}$-Q, $\overline{Q}$)	2.0		—	105	165	—	205	—	250	ns
		4.5		—	21	33	—	41	—	50	
		6.0		—	18	28	—	35	—	43	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$-Q, $\overline{Q}$)	2.0		—	115	185	—	230	—	280	ns
		4.5		—	23	37	—	46	—	56	
		6.0		—	20	31	—	39	—	48	
f_{MAX}	Maximum Clock Frequency	2.0		6	12	—	4.8	—	4	—	MHz
		4.5		30	48	—	24	—	20	—	
		6.0		35	56	—	28	—	24	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width ($\overline{CLOCK}$)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
$t_{W(L)}$	Minimum Pulse Width $\overline{CLEAR}$	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-up Time	2.0		—	10	50	—	65	—	75	ns
		4.5		—	3	10	—	13	—	15	
		6.0		—	3	9	—	11	—	13	
t_h	Minimum Hold Time	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{REM}	Minimum Removal Time ($\overline{CLEAR}$)	2.0		—	0	75	—	95	—	110	ns
		4.5		—	0	15	—	19	—	22	
		6.0		—	0	13	—	16	—	19	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	71	—	—	—	—	—	pF

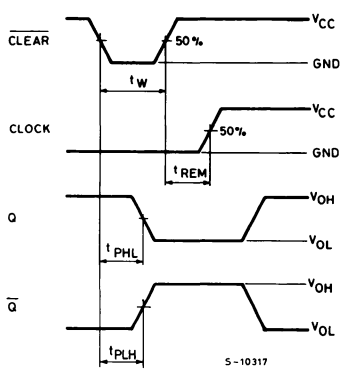
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation.
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (for Flip/Flop).

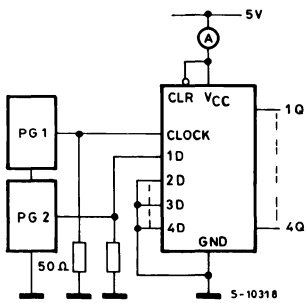
And the total C_{PD} at the time when n pcs of Flip-Flop operate can be gained C_{PD} (total) = $43 + 28 \times n$

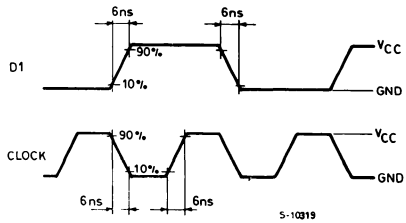
SWITCHING CHARACTERISTICS TEST WAVEFORM





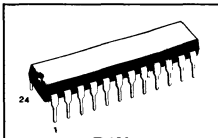
TEST CIRCUIT I_{CC} (Opr.)



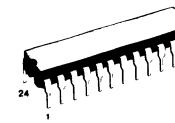


ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS181



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

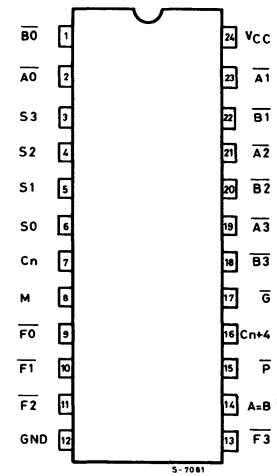
ORDERING NUMBERS:

M54HC181 F1	M74HC181 M1
M74HC181 B1N	M74HC181 F1

DESCRIPTION

The M54/74HC181 is a high speed CMOS ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR fabricated with silicon gate C²MOS technology. It has the same high speed performance of SLTTL combined with true CMOS low power consumption. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (SO, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing aritmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the M54HC182 or M74HC182, full carry look-ahead circuits, high-speed arithmetic operations can be performed. These circuits will accomodate active-high or active-low data, if the pin designations are interpreted as shown below. Subtraction is accomplished by 1,s complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is 1—B—1, which requires an end-around or forced carry to produce A—B. The 181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicated equality (A = B).

PIN CONNECTIONS (top view)



*: Open drain Output Structure

DESCRIPTION (Continued)

The ALU should be in the subtract mode with $C_n = H$ when performing this comparison. The A = B output is open-drain so that it can be wire-AND connected to give a comparison for more that four bits. The carry output (Cn + 4) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively. These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry.

All inputs are equipped with portection circuits against static discharge and transient excess voltage.

PIN DESIGNATIONS

Designations	Pin No.	Function
$\overline{A0}$, $\overline{A1}$, $\overline{A2}$, $\overline{A3}$	2, 23, 21, 19	Word A Inputs
$\overline{B0}$, $\overline{B1}$, $\overline{B2}$, $\overline{B3}$	1, 22, 20, 18	Word B Inputs
S0, S1, S2, S3	6, 5, 4, 3	Function Select Inputs
Cn	7	Inv. Carry Input
M	8	Mode Control Input
$\overline{F0}$, $\overline{F1}$, $\overline{F2}$, $\overline{F3}$	9, 10, 11, 13	Function Outputs
A = B	14	Comparator Outputs
$\overline{P}$	15	Carry Propagate Output
Cn + 4	16	Inv. Carry Output
$\overline{G}$	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
ACTIVE-LOW DATA (Table 1)	$\overline{A0}$	$\overline{B0}$	$\overline{A1}$	$\overline{B1}$	$\overline{A2}$	$\overline{B2}$	$\overline{A3}$	$\overline{B3}$	$\overline{F0}$	$\overline{F1}$	$\overline{F2}$	$\overline{F3}$	Cn	Cn + 4	$\overline{P}$	$\overline{G}$
ACTIVE-HIGH DATA (Table 2)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	Cn	Cn + 4	X	Y

Input Cn	Output Cn + 4	Active-Low data (Figure 1)	Active-High data (Figure 2)
H	H	A ≥ B	A ≤ B
H	L	A < B	A > B
L	H	A > B	A < B
L	L	A ≤ B	A ≥ B

Figure 1

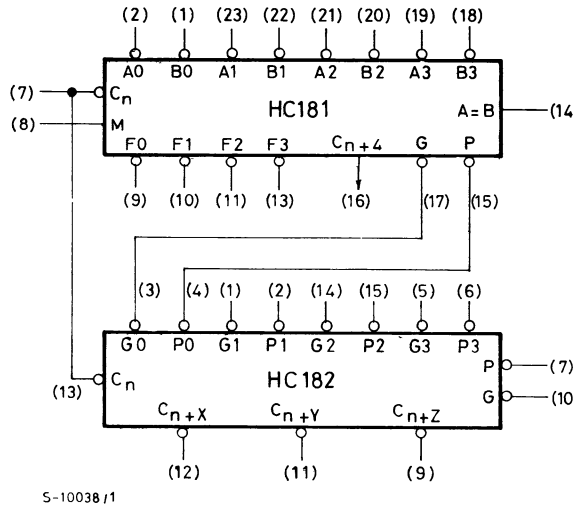


TABLE 1

Selection				Active Low Data		
				M = H	M = L: Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A Minus 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ Minus 1	F = (A$\overline{B}$)
L	L	H	H	F = 1	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $\overline{A+B}$	F = A Plus (A + $\overline{B}$)	F = A Plus (A + $\overline{B}$) Plus 1
L	H	L	H	F = $\overline{B}$	F = AB Plus (A + B)	F = AB Plus (A + $\overline{B}$) Plus 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
H	L	L	L	F = $\overline{A}$B	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H	L	L	H	F = A $\oplus$ B	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = A$\overline{B}$ Plus (A + B)	F = A$\overline{B}$ Plus (A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A$\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	F = A$\overline{B}$ Plus A	F = A$\overline{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

* Each bit is shifted to the next more significant position.

Figure 2

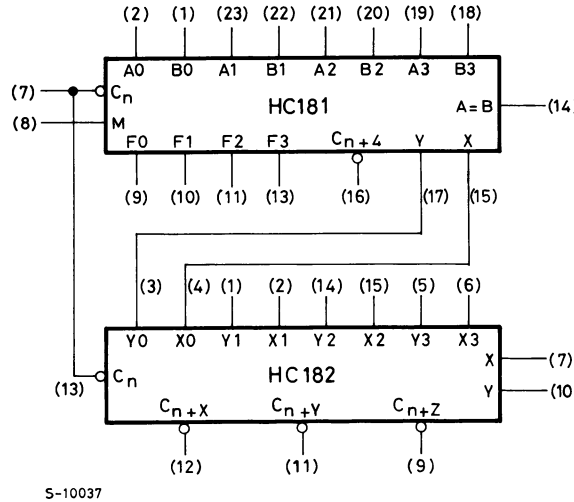
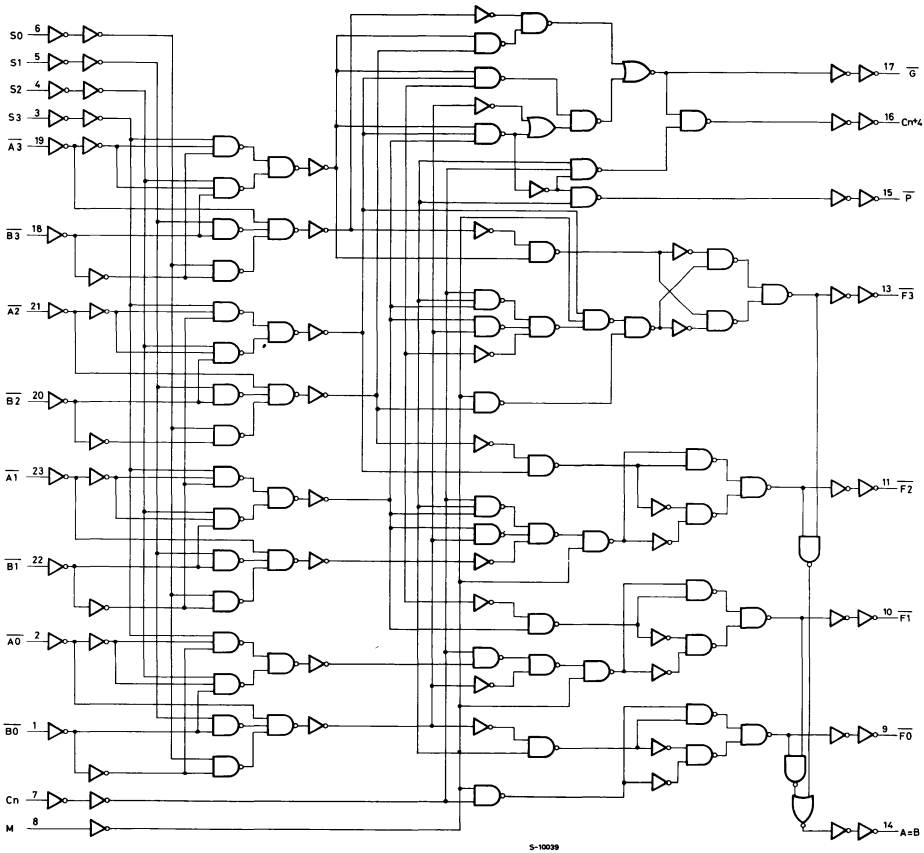


TABLE 2

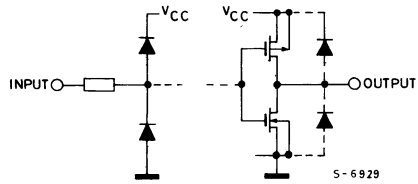
Selection				Active High Data		
				M = H	M = L: Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n = H (no carry)	C_n = L (with carry)
L	L	L	L	$F=\overline{A}$	F = A	F = A Plus 1
L	L	L	H	$F=\overline{A+B}$	F = A + B	F = (A + B) Plus 1
L	L	H	L	$F=\overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
L	L	H	H	F = 0	F = Minus 1 (2's Comp1)	F = Zero
L	H	L	L	$F=\overline{AB}$	F = A Plus A$\overline{B}$	F = A Plus A$\overline{B}$ Plus 1
L	H	L	H	$F=\overline{B}$	F = (A + B) Plus A$\overline{B}$	F = (A + B) Plus A$\overline{B}$ Plus 1
L	H	H	L	F = A⊕B	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
H	L	L	L	$F=\overline{A}+B$	F = A Plus AB	F = A Plus AB Plus 1
H	L	L	H	$F=\overline{A\oplus B}$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) Plus AB	F = (A + $\overline{B}$) Plus AB Plus 1
H	L	H	H	F = AB	F = AB Minus 1	F = AB
H	H	L	L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) Plus A	F = (A + $\overline{B}$) Plus A Plus 1
H	H	H	H	F = A	F = A Minus 1	F = A

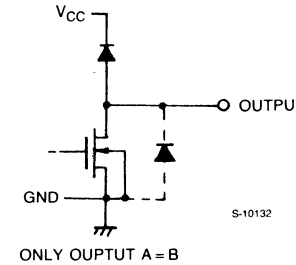
* Each bit is shifted to the next more significant position.

LOGIC DIAGRAM



INPUT AND OUTPUT EQUIVALENT CIRCUIT





ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC}	2 V: 0 to 1000 4.5V: 0 to 500 6 V: 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_{IN}	I_{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	$V_{IH} = V_{IL}$	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0	Any output		5.9	6.0	—	5.9	—	5.9	—	
		4.5	except	−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0	A = B	−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0		I_{OL}	—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IN}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0	or		—	0	0.1	—	0.1	—	0.1	
		4.5	V_{IH}	4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{OZ}	3-State Output Off state Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$		—	—	±0.5	—	±5.0	—	±10	
I_{CC}	Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	4	—	40	—	80	

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (1)		14	23	ns
t_{PLH} t_{PHL}	Propagation Delay Time (2)		27	42	ns
t_{PLH} t_{PHL}	Propagation Delay Time (3)		26	41	ns
t_{PLH} t_{PHL}	Propagation Delay Time (4)		24	37	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (5)		25	39	ns
t_{PLH} t_{PHL}	Propagation Delay Time (6)		24	38	ns
t_{PLH} t_{PHL}	Propagation Delay Time (7)		23	37	ns
t_{PLH} t_{PHL}	Propagation Delay Time (8)		23	37	ns
t_{PLH} t_{PHL}	Propagation Delay Time (9)		30	46	ns
t_{PLH} t_{PHL}	Propagation Delay Time (10)		30	46	ns
t_{PLH} t_{PHL}	Propagation Delay Time (11)		24	37	ns
t_{PZL}	3-State Output•Enable Time (12)		27	42	ns
t_{PLZ}	3-State Output•Disable Time (12)		29	46	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (1)	2.0		—	68	135	—	170	—	205	ns
		4.5		—	17	27	—	34	—	41	
		6.0		—	14	23	—	29	—	35	
t_{PLH} t_{PHL}	Propagation Delay Time (2)	2.0		—	124	240	—	300	—	360	ns
		4.5		—	31	48	—	60	—	72	
		6.0		—	26	41	—	51	—	61	
t_{PLH} t_{PHL}	Propagation Delay Time (3)	2.0		—	120	235	—	295	—	355	ns
		4.5		—	30	47	—	59	—	71	
		6.0		—	26	40	—	50	—	60	
t_{PLH} t_{PHL}	Propagation Delay Time (4)	2.0		—	112	215	—	270	—	325	ns
		4.5		—	28	43	—	54	—	65	
		6.0		—	24	37	—	46	—	55	

AC ELECTRICAL CHARACTERISTICS (Continued)

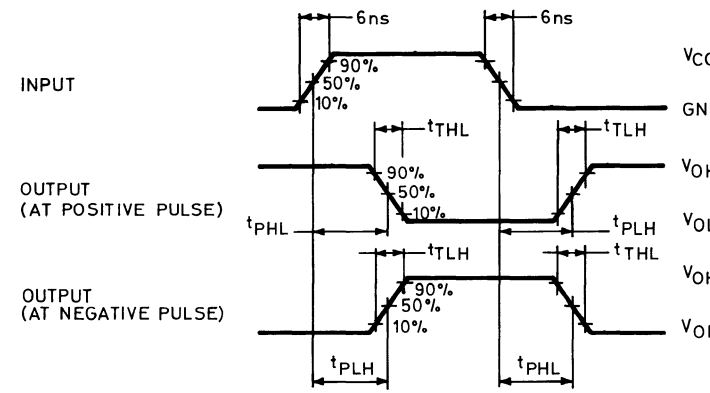
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (5)	2.0		—	116	225	—	280	—	340	ns
		4.5		—	29	45	—	56	—	68	
		6.0		—	25	38	—	48	—	58	
t_{PLH} t_{PHL}	Propagation Delay Time (6)	2.0		—	116	220	—	275	—	330	ns
		4.5		—	29	44	—	55	—	66	
		6.0		—	25	37	—	47	—	56	
t_{PLH} t_{PHL}	Propagation Delay Time (7)	2.0		—	108	210	—	265	—	315	ns
		4.5		—	27	42	—	53	—	63	
		6.0		—	23	36	—	45	—	54	
t_{PLH} t_{PHL}	Propagation Delay Time (8)	2.0		—	108	210	—	265	—	315	ns
		4.5		—	27	42	—	53	—	63	
		6.0		—	23	36	—	45	—	54	
t_{PLH} t_{PHL}	Propagation Delay Time (9)	2.0		—	136	265	—	335	—	400	ns
		4.5		—	34	53	—	66	—	80	
		6.0		—	29	45	—	56	—	68	
t_{PLH} t_{PHL}	Propagation Delay Time (10)	2.0		—	136	265	—	335	—	400	ns
		4.5		—	34	53	—	66	—	80	
		6.0		—	29	45	—	56	—	68	
t_{PLH} t_{PHL}	Propagation Delay Time (11)	2.0		—	112	215	—	270	—	325	ns
		4.5		—	28	43	—	54	—	65	
		6.0		—	24	37	—	46	—	55	
t_{PZL}	3-State Output Enable Time (12)	2.0		—	124	240	—	300	—	360	ns
		4.5	$R_L = 1k\Omega$	—	31	48	—	60	—	72	
		6.0		—	26	41	—	51	—	61	
t_{PLZ}	3-State Output Disable Time (12)	2.0		—	140	260	—	325	—	390	ns
		4.5	$R_L = 1k\Omega$	—	35	52	—	65	—	78	
		6.0		—	30	44	—	55	—	66	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	216	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following equation:
$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

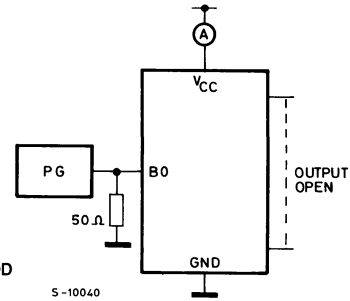
PROPAGATION DELAY TIME TEST CONDITIONS

Test No.	From (Input)	To (Output)	Test Conditions
(1)	Cn	Cn+4	
(2)	Any $\overline{A}$ or $\overline{B}$	Cn+4	M = GND, S0 = S3 = V_{CC}, S1 = S2 = GND ($\overline{SUM}$ mode)
(3)	Any $\overline{A}$ or $\overline{B}$	Cn+4	M = GND, S0 = S3 = GND, S1 = S2 = V_{CC} ($\overline{DIFF}$ mode)
(4)	$\overline{Cn}$	Any $\overline{F}$	M = GND ($\overline{SUM}$ or $\overline{DIFF}$ mode)
(5)	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = GND, S0 = S3 = V_{CC}, S1 = S2 = GND ($\overline{SUM}$ mode)
(6)	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = GND, S0 = S3 = GND, S1 = S2 = V_{CC} ($\overline{DIFF}$ mode)
(7)	Any $\overline{A}$ or $\overline{B}$	$\overline{F}$	M = GND, S0 = S3 = V_{CC}, S1 = S2 = GND ($\overline{SUM}$ mode)
(8)	Any $\overline{A}$ or $\overline{B}$	$\overline{F}$	M = GND, S0 = S3 = GND, S1 = S2 = V_{CC} ($\overline{DIFF}$ mode)
(9)	$\overline{A1}$ or $\overline{B1}$	$\overline{Fi}$	M = GND, S0 = S3 = V_{CC}, S1 = S2 = GND ($\overline{SUM}$ mode)
(10)	$\overline{A1}$ or $\overline{B1}$	$\overline{Fi}$	M = GND, S0 = S3 = GND, S1 = S2 = V_{CC} ($\overline{DIFF}$ mode)
(11)	$\overline{A1}$ or $\overline{B1}$	$\overline{Fi}$	M = V_{CC} (Logic Mode)
(12)	Any $\overline{A}$ or $\overline{B}$	A = B	M = GND, S0 = S3 = GND, S1 = S2 = V_{CC} ($\overline{DIFF}$ mode)

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



Input Condition:
$\overline{A0}$, $\overline{A1}$, $\overline{A2}$, $\overline{A3}$, S0, S3, Cn = V_{DD}
$\overline{B1}$, $\overline{B2}$, $\overline{B3}$, S1, S2, M = GND

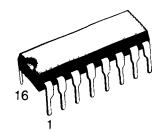
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

SGS-THOMSON MICROELECTRONICS

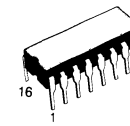
M54HC182
M74HC182

FUNCTION LOOK AHEAD CARRY GENERATOR

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (Max.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  with 54/74LS182



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC182 F1
M74HC182 B1N
M74HC182 F1
M74HC182 M1
M74HC182 C1

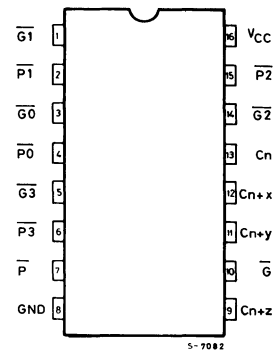
DESCRIPTION

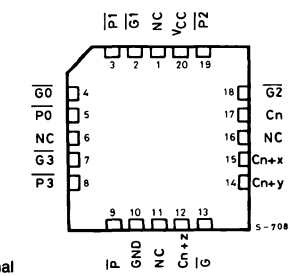
The M54/74HC182 is a high speed CMOS FUNCTION LOOK AHEAD CARRY GENERATOR fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. These circuit are capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin connection table.

When used in conjunction with the HC181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each HC182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALU's are in their true form, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretation of carry functions as explained on the HC181 data sheet are also applicable to and compatible with the look-ahead generator. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION (top view)





NC = No Internal Connection

FUNCTION TABLES

FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
ALL OTHER COMBINATIONS							H

FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{P}$
L	L	L	L	L
ALL OTHER COMBINATIONS				H

FOR Cn+z OUTPUT

INPUTS							OUTPUT
$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	Cn	Cn+z
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
ALL OTHER COMBINATIONS							L

FOR Cn+x OUTPUT

INPUTS			OUTPUT
$\overline{G0}$	$\overline{P0}$	Cn	Cn+x
L	X	X	H
X	L	H	H
ALL OTHER COMBINATIONS			L

FOR Cn+y OUTPUT

INPUTS					OUTPUT
$\overline{G1}$	$\overline{G0}$	$\overline{P1}$	$\overline{P0}$	Cn	Cn+y
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
ALL OTHER COMBINATIONS					L

$Cn+x = G0 + P0Cn$

$Cn+y = G1 + P1G0 + P1P0Cn$

$Cn+z = G2 + P2G1 + P2P1G0 + P2P1P0Cn$

$\overline{G} = \overline{G3 + P3G2 + P3P2G1 + P3P2P1G0}$

$\overline{P} = \overline{P3P2P1P0}$

or

$\overline{Cn+x} = \overline{Y0\ (X0 + Cn)}$

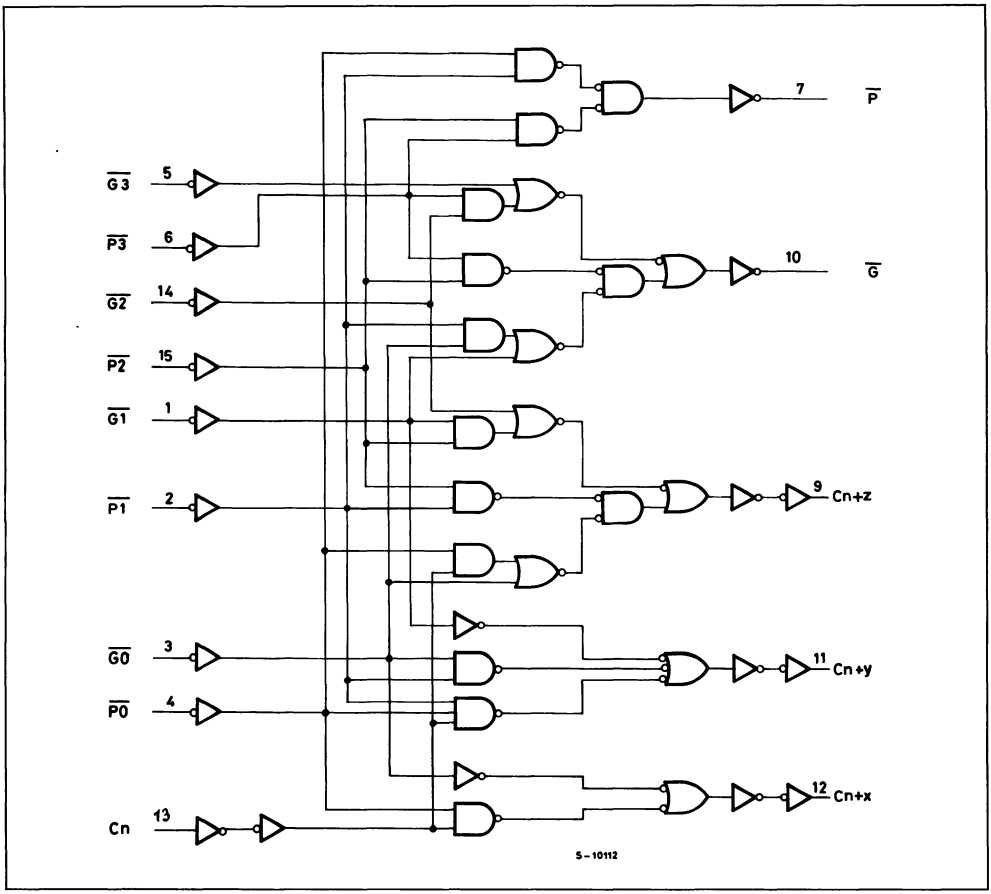
$\overline{Cn+y} = \overline{Y1\ [X1 + Y0(X0 + Cn)]}$

$\overline{Cn+z} = \overline{Y2\ \{X2 + Y1[X1 + Y0(X0 + Cn)]\}}$

$Y = Y3\ (X3 + Y2)\ (X3 + X2 + Y1)\ (X3 + X2 + X1 + Y0)$

$X = X3 + X2 + X1 + X0$

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V: 0 to 1000 V_{CC} = 4.5V: 0 to 500 V_{CC} = 6 V: 0 to 400	ns

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0 4.5 6.0	V_I V_{IH} or V_{IL}	I_O −20 μA	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	1.9 4.4 5.9	— — —	V
		4.5 6.0		−4.0 mA −5.2 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	
V_{OL}	Low Level Output Voltage	2.0 4.5 6.0	V_{IH} or V_{IL}	20 μA	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
		4.5 6.0		4.0 mA 5.2 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

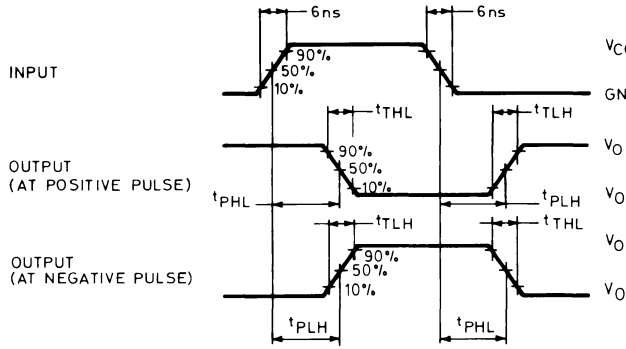
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{G0},\overline{G1},\overline{G2}$, $\overline{P0},\overline{P1},\overline{P2}$ - Cn+x, Cn+y / Cn+Z)		15	25	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{G0},\overline{G1},\overline{G2},\overline{G3}$ / $\overline{P1},\overline{P2},\overline{P3}$ - $\overline{G}$)		18	28	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{P0},\overline{P1},\overline{P2},\overline{P3}$ - $\overline{P}$		17	27	ns
t_{PLH} t_{PHL}	Propagation Delay Time Cu-Cn+x, Cn+y, Cn+z)		16	26	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

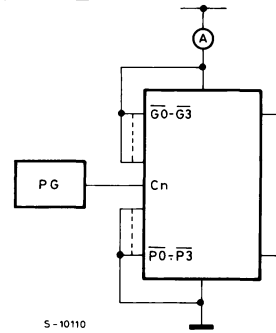
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t_{PLH}	Propagation Delay Time ($\overline{G0},\overline{G1},\overline{G2}$, $\overline{P0},\overline{P1},\overline{P2}$ - Cn+x,Cn+y / Cn+2)	2.0 4.5 6.0		— — —	72 18 15	145 29 25	— — —	180 36 31	 — —	220 44 38	
t_{PLH}	Propagation Delay Time ($\overline{G0},\overline{G1},\overline{G2},\overline{G3}$, $\overline{P0},\overline{P1},\overline{P2}$ - $\overline{G}$)	2.0 4.5 6.0		— — —	84 21 18	165 33 28	— — —	205 41 35	 — —	250 50 43	ns
t_{PLH}	Propagation Delay Time ($\overline{P0},\overline{P1},\overline{P2},\overline{P3}$ - $\overline{P}$)	2.0 4.5 6.0		— — —	80 20 17	155 31 26	— — —	195 39 33	 — —	235 47 40	
t_{PHL}	Propagation Delay Time (Cu-Cn+x, Cn+y,Cn+z)	2.0 4.5 6.0		— — —	76 19 16	150 30 26	— — —	190 38 33	 — —	225 45 38	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	
C_{PD}(*)	Power Dissipation Capacitance			—	88	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current is: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

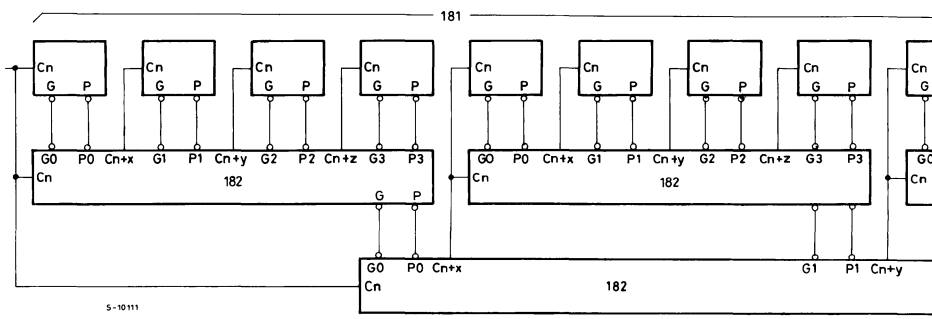


TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

TYPICAL APPLICATION



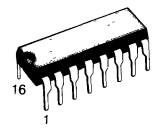
64-BIT ALU, FULL-CARRY LOOK-AHEAD IN THREE LEVELS

SGS-THOMSON MICROELECTRONICS

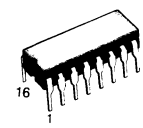
M54/74HC190
M54/74HC191

4-BIT SYNCHRONOUS UP/DOWN COUNTERS

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (Min.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS190/191



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

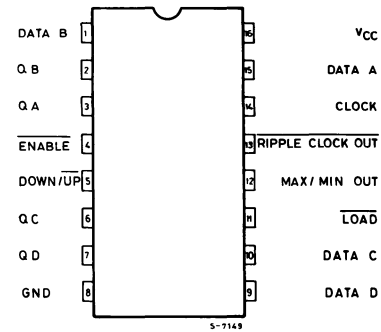
ORDERING NUMBERS:

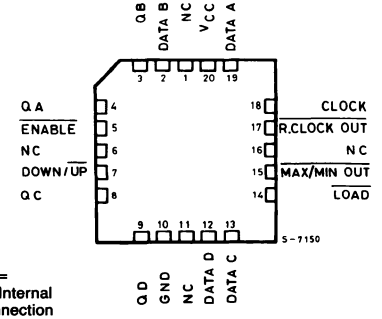
M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX C1
M74HCXXX M1

DESCRIPTION

The M54/74HC190/191 are high speed CMOS 4-BIT SYNCHRONOUS UP/DOWN COUNTERS fabricated in silicon gate C²MOS technology.
They have the same high speed performance of LSTTL combined with true CMOS low power consumption.
State changes of the counter are synchronus with the LOW-to-HIGH transition of the Clock Pulse input.
An asynchronous parallel load input overrides counting and loads the data present on the DATA inputs into the flip-flops, which makes it possible to use the circuits as programmable counters. A count enable input serves as the carry/borrow input in multi-stage counters. Control input, Down/Up, determines whether a circuit counts up or down. A MAX/MIN output and a Ripple Clock output provide overflow/underflow indication and make possible a variety of methods for generating carry/borrow signals in multi-stage counter applications.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)





NC = No Internal Connection

TRUTH TABLE

INPUTS				OUTPUTS				FUNCTION
$\overline{LOAD}$	$\overline{ENABLE}$	D/$\overline{U}$	CLOCK	QA	QB	QC	QD	
L	X	X	X	a	b	c	d	PRESET DATA
H	L	L	↑	UP COUNT				UP COUNT
H	L	H	↑	DOWN COUNT				DOWN COUNT
H	H	X	↑	NO CHANGE				NO COUNT
H	X	X	↓	NO CHANGE				NO COUNT

X : DON'T CARE
a-d:THE LEVEL OF STEADY STATE INPUTS AT INPUTS A THROUGH D RESPECTIVELY.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

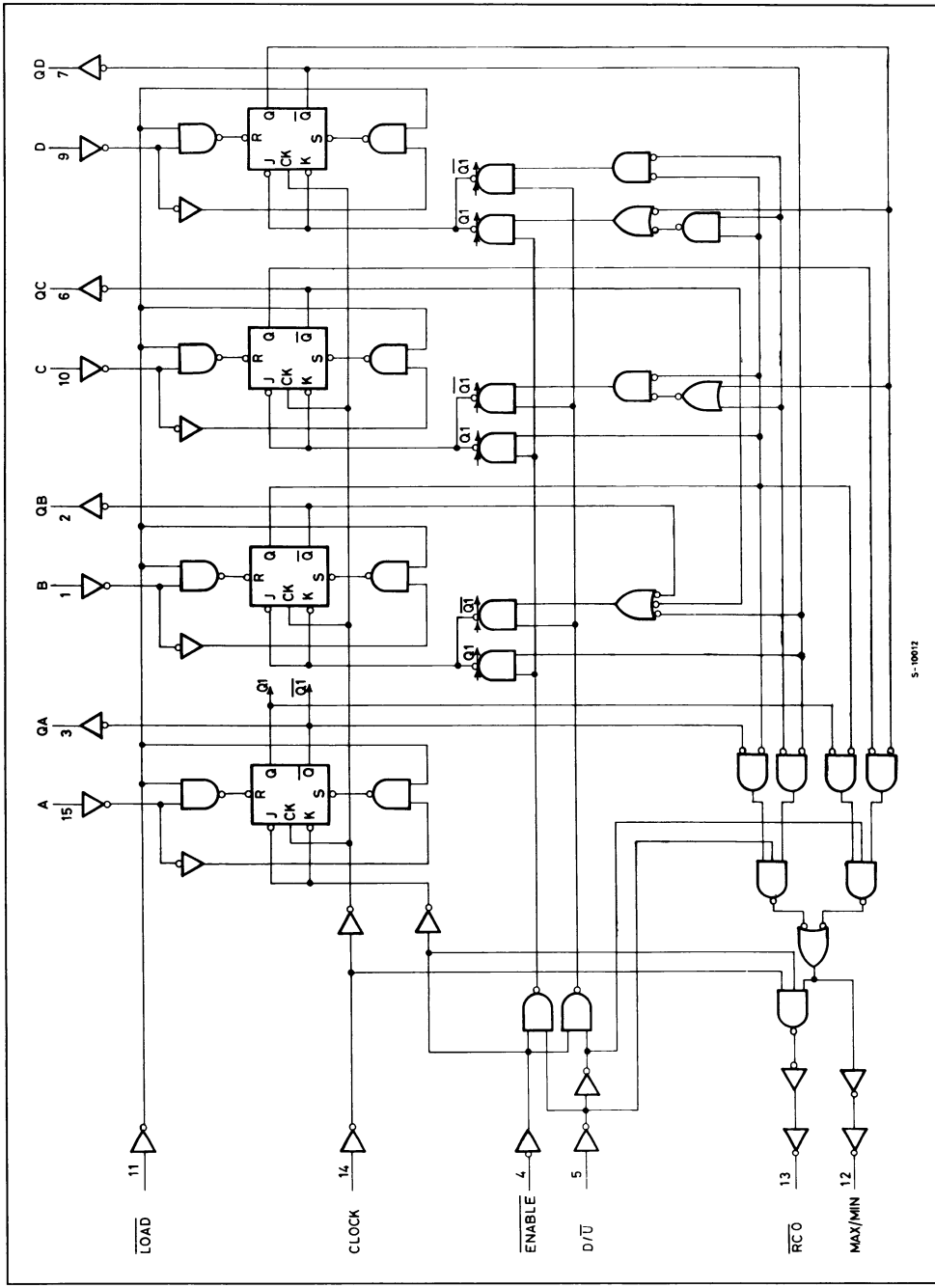
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW:≅65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

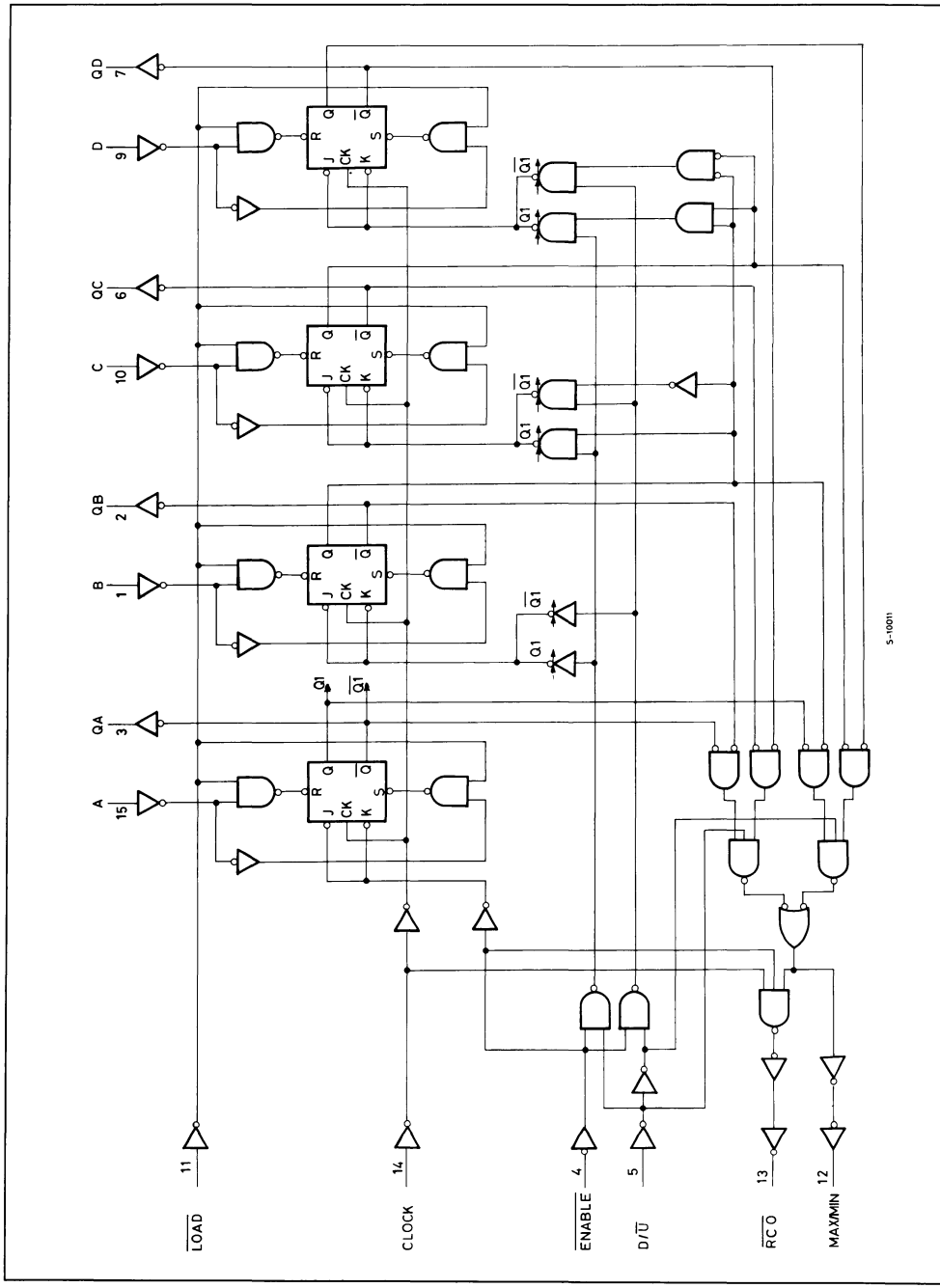
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V 4.5V 6 V	0 to 1000 0 to 500 0 to 400	ns

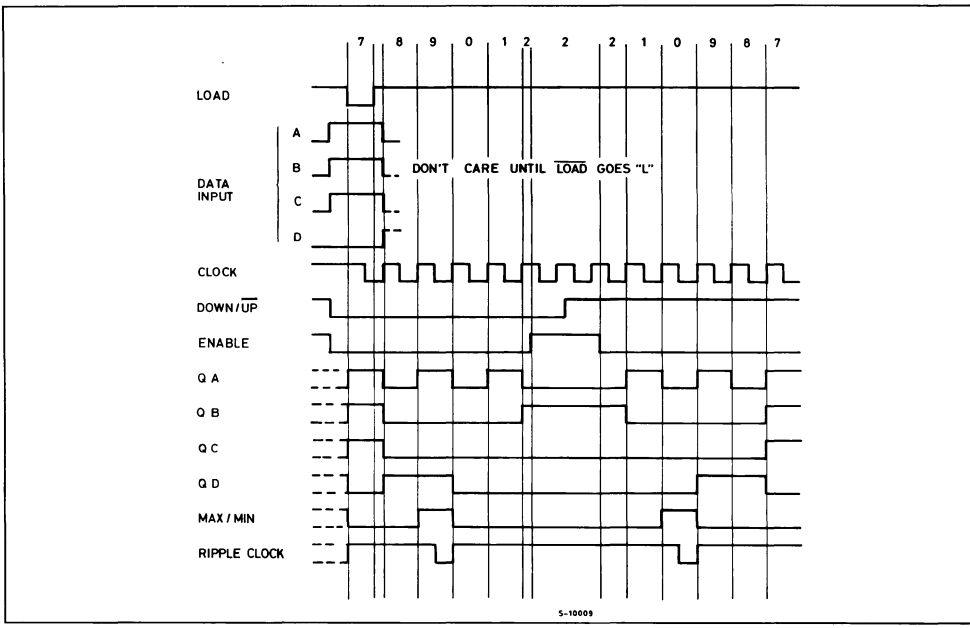
LOGIC DIAGRAM (HC190)



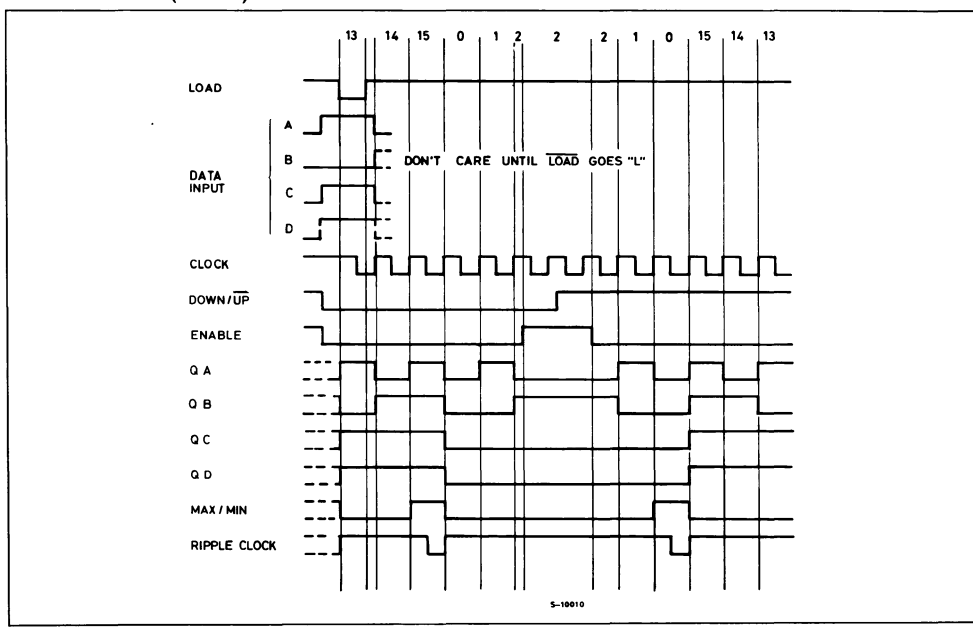
LOGIC DIAGRAM (HC191)



TIMING CHART - (HC190)



TIMING CHART (HC191)



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0	V_{IN}	I_{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5 6.0	V_{IH} or V_{IL}	−20 μA	4.4 5.9	4.5 6.0	— —	4.4 5.9	— —	4.4 5.9	— —	
		4.5 6.0		−4.0 mA −5.2 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	
V_{OL}	Low Level Output Voltage	2.0 4.5 6.0	V_{IH} or V_{IL}	20 μA	— — —	0 0 0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
		4.5 6.0		4.0 mA 5.2 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40	
I_{IN}	Input Leakage Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	4	—	40	—	80	

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Q)		20	31	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-$\overline{RCO}$)		14	22	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-MAX/MIN)		27	42	ns
t_{PLH} t_{PHL}	Propagation Delay Time (LOAD-Q)		23	35	ns
t_{PLH} t_{PHL}	Propagation Delay Time (DATA-Q)		19	30	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{ENABLE}$-$\overline{RCO}$)		14	22	ns
t_{PLH} t_{PHL}	Propagation Delay Time (D/$\overline{U}$-$\overline{RCO}$)		20	31	ns
t_{PLH} t_{PHL}	Propagation Delay Time (D/$\overline{U}$-MAX/MIN)		17	27	ns
f_{MAX}	Maximum Clock Frequency	28	46		MHz

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Q)	2.0		—	92	180	—	225	—	270	ns
		4.5		—	23	36	—	45	—	54	
		6.0		—	20	31	—	38	—	46	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-$\overline{RCO}$)	2.0		—	64	130	—	165	—	195	ns
		4.5		—	16	26	—	33	—	39	
		6.0		—	14	22	—	28	—	33	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-MAX/MIN)	2.0		—	124	240	—	300	—	360	ns
		4.5		—	31	48	—	60	—	72	
		6.0		—	26	41	—	51	—	61	
t_{PLH} t_{PHL}	Propagation Delay Time (LOAD-Q)	2.0		—	104	205	—	255	—	310	ns
		4.5		—	26	41	—	51	—	62	
		6.0		—	22	35	—	43	—	53	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA-Q)	2.0		—	88	175	—	220	—	265	ns
		4.5		—	22	35	—	44	—	53	
		6.0		—	19	30	—	37	—	45	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{ENABLE}$-$\overline{RCO}$)	2.0		—	64	130	—	165	—	195	ns
		4.5		—	16	26	—	33	—	39	
		6.0		—	14	22	—	28	—	33	
t_{PLH} t_{PHL}	Propagation Delay Time (D/$\overline{U}$-$\overline{RCO}$)	2.0		—	92	180	—	225	—	270	ns
		4.5		—	23	36	—	45	—	54	
		6.0		—	20	31	—	38	—	46	
t_{PLH} t_{PHL}	Propagation Delay Time (D/$\overline{U}$-MAX/MIN)	2.0		—	80	160	—	200	—	240	ns
		4.5		—	20	32	—	40	—	48	
		6.0		—	17	27	—	34	—	41	

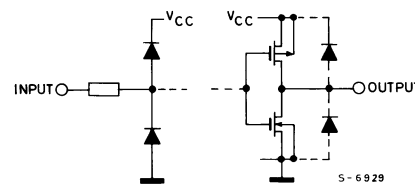
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency	2.0 4.5 6.0		5 25 29	11 42 49	— — —	4 20 24	— — —	— — —	3 17 20	MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0 4.5 6.0		— — —	45 11 9	100 20 17	— — —	125 25 21	— — —	150 30 26	ns
$t_{W(L)}$	Minimum Pulse Width ($\overline{LOAD}$)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{REM}	Minimum Removal Time	2.0 4.5 6.0		— — —	5 1 1	50 10 9	— — —	65 13 11	— — —	75 15 13	ns
t_s	Minimum Set-up Time ($\overline{ENABLE}$-D/$\overline{U}$)	2.0 4.5 6.0		— — —	72 18 15	150 30 26	— — —	190 38 33	— — —	225 45 38	ns
t_h	Minimum Set-up Time (DATA-$\overline{LOAD}$)	2.0 4.5 6.0		— — —	10 3 3	50 10 9	— — —	65 13 11	— — —	75 15 13	ns
t_h	Minimum Hold Time ($\overline{ENABLE}$-D/$\overline{U}$)	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
t_h	Minimum Hold Time (DATA-$\overline{LOAD}$)	2.0 4.5 6.0		— — —	— — —	5 5 5	— — —	5 5 5	— — —	5 5 5	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	124	—	—	—	—	—	pF

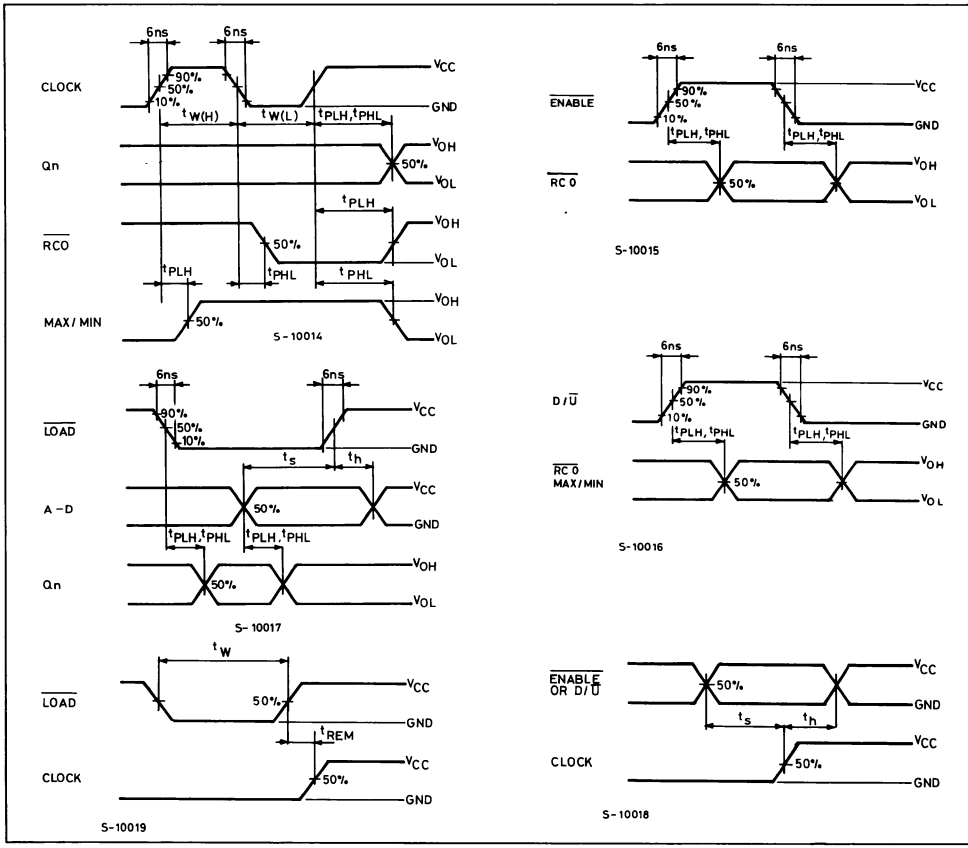
Note (*) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).

Average operating current can be obtained from the equation: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

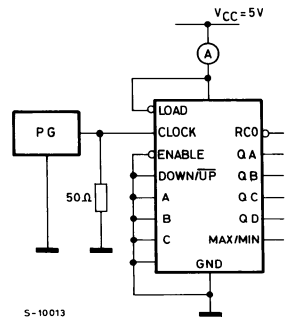
INPUT AND OUTPUT EQUIVALENT CIRCUIT



SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



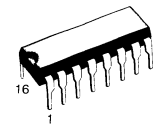
INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

SGS-THOMSON MICROELECTRONICS

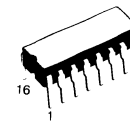
M54/74HC192
M54/74HC193

HC192 - SYNCHRONOUS UP/DOWN DECADE COUNTER
HC193 - SYNCHRONOUS UP/DOWN BINARY COUNTER

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (Min.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS192-193



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX C1
M74HCXXX M1

DESCRIPTION

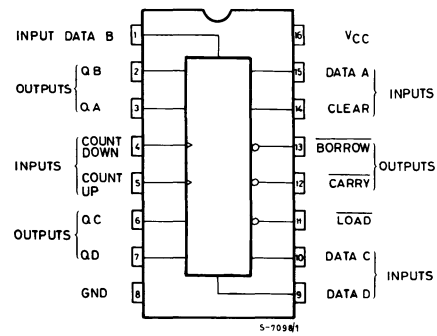
The M54/74HC192/193 are a high speed CMOS SYNCHRONOUS UP/DOWN DECADE COUNTERS fabricated in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. The counter has two separate clock inputs, an UP COUNT input and a DOWN COUNT input. All outputs of the flip-flop are simultaneously triggered on the low to high transition of either clock while the other input is held high. The direction of counting is determined by which input is clocked. This counter may be preset by entering the desired data on the DATA A, DATA B, DATA C, and DATA D input. When the LOAD input is taken low the data is loaded independently of either clock input. This feature allows the counters to be used as divide-by-n counters by modifying the count length with the preset inputs.

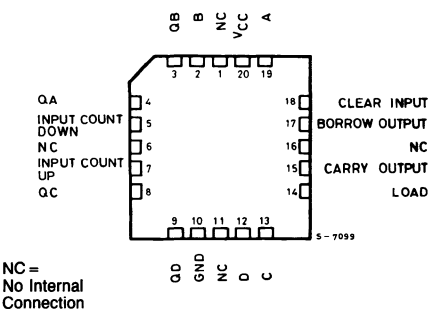
In addition the counter can also be cleared. This is accomplished by inputting a high on the CLEAR input. All 4 internal stages are set to low independently of either COUNT input.

Both a BORROW and CARRY output are provided to enable cascading of both up and down counting functions. The BORROW output produces a negative going pulse when the counter underflows and the CARRY outputs a pulse when the counter overflows. The counter can be cascaded by connecting the CARRY and BORROW outputs of one device to the COUNT UP and COUNT DOWN inputs, respectively, of the next device.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)





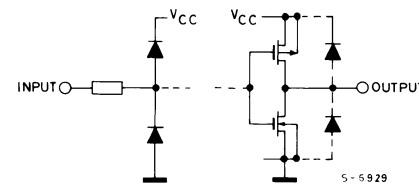
NC = No Internal Connection

TRUTH TABLE

Count Up	Count Down	$\overline{Load}$	Clear	Function
↑	H	H	L	COUNT UP
↓	H	H	L	NO COUNT
H	↑	H	L	COUNT DOWN
H	↓	H	L	NO COUNT
X	X	L	L	PRESET
X	X	X	H	RESET

X = DON'T CARE

INPUT AND OUTPUT EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

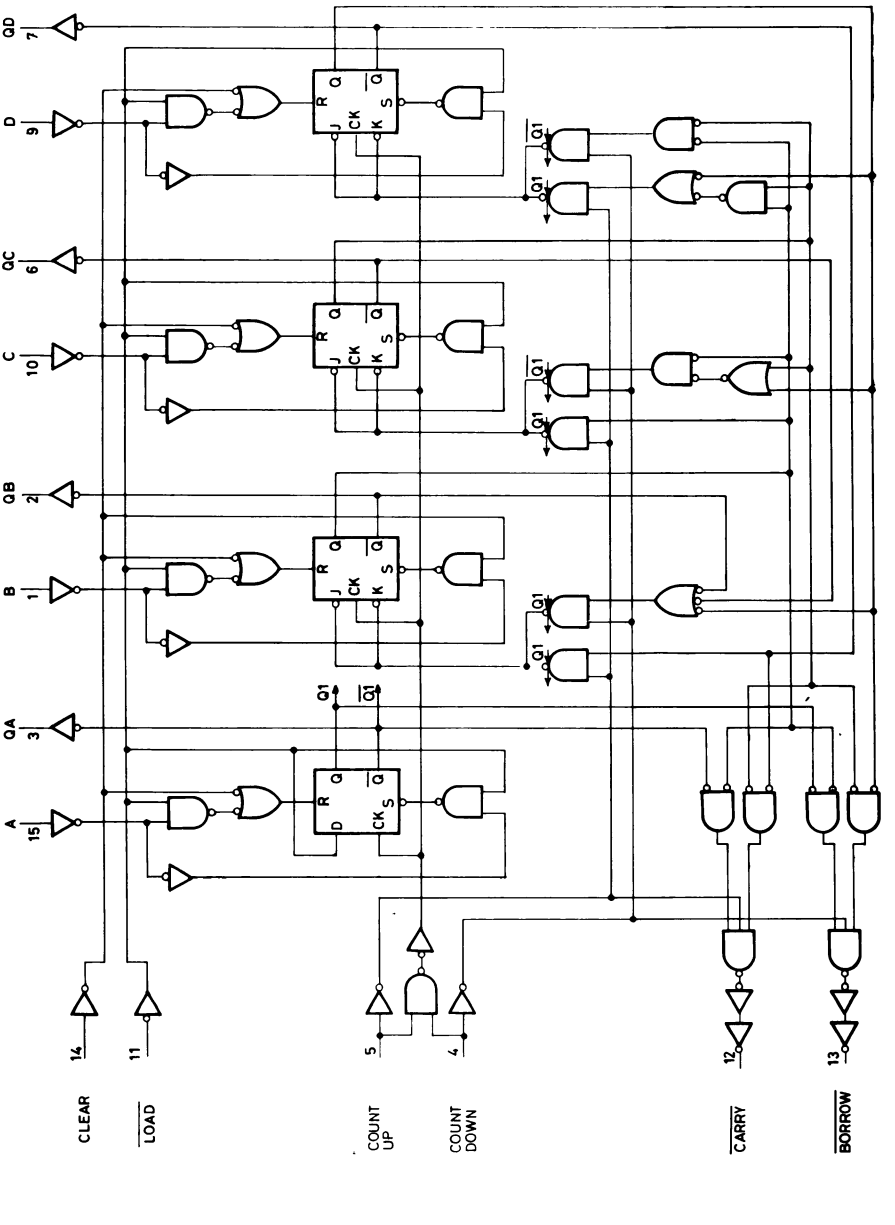
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

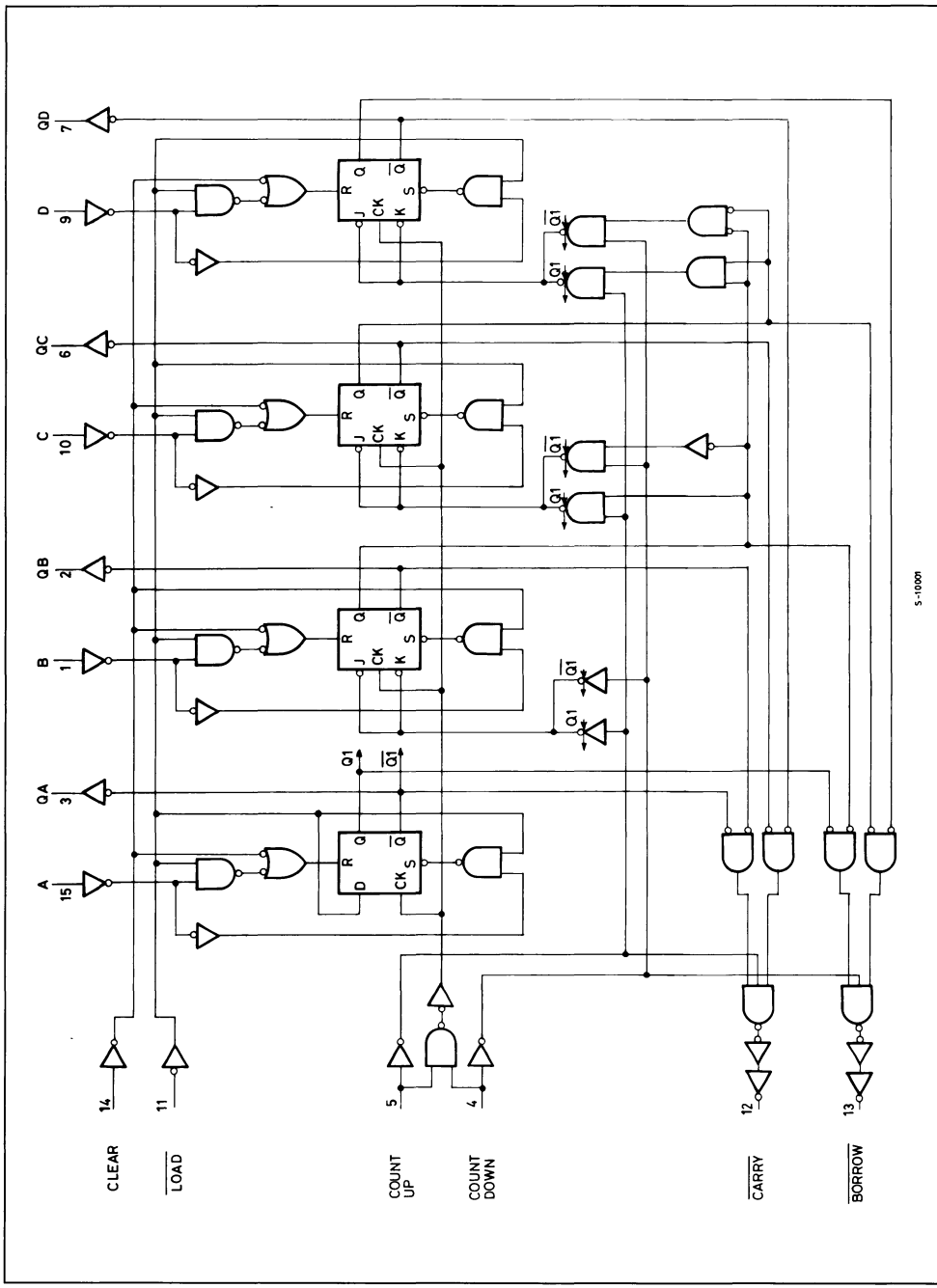
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400		ns

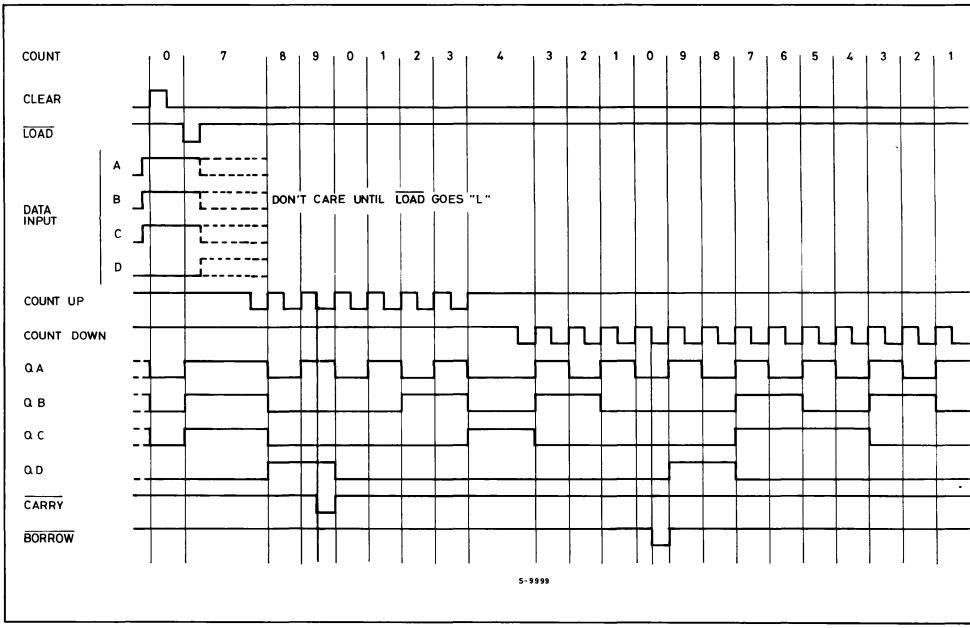
LOGIC DIAGRAM (HC192)



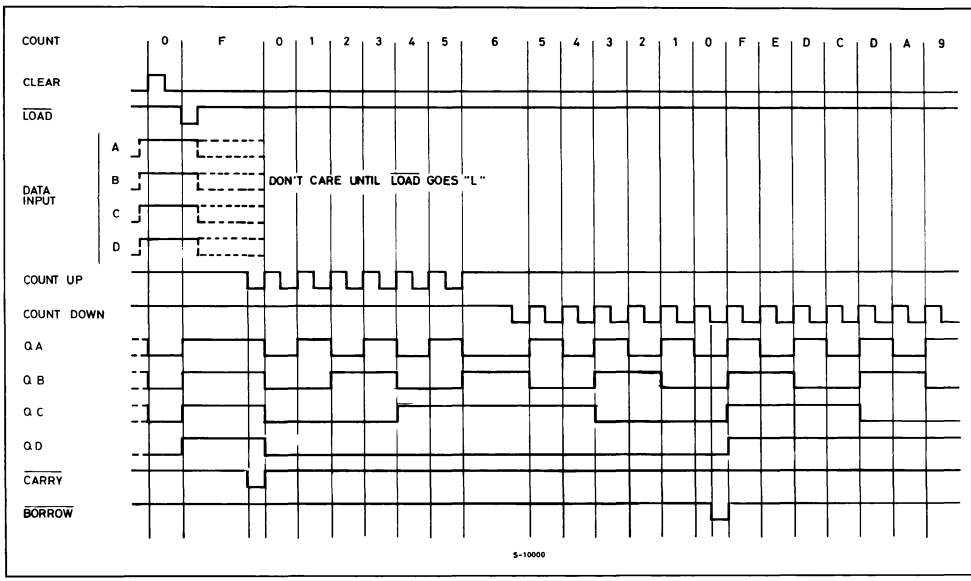
LOGIC DIAGRAM (HC193)



TIMING DIAGRAM (HC192)



TIMING DIAGRAM (HC193)



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_{IN}	I_{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	4	—	40	—	80	

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time	—	4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (UP, DOWN-Q)	—	21	33	ns
t_{PLH} t_{PHL}	Propagation Delay Time (UP-CARRY)	—	15	23	ns
t_{PLH} t_{PHL}	Propagation Delay Time (DOWN-$\overline{\text{BORROW}}$)	—	15	23	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{\text{LOAD}}$-Q)	—	28	44	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{\text{LOAD}}$-CARRY)	—	35	54	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (LOAD-BORROW)		32	49	ns
t_{PLH} t_{PHL}	Propagation Delay Time (ANY IN-Q)		26	40	ns
t_{PLH} t_{PHL}	Propagation Delay Time (ANY IN-CARRY)		38	58	ns
t_{PLH} t_{PHL}	Propagation Delay Time (ANY IN-BORROW)		31	48	ns
t_{PHL}	Propagation Delay Time (CLEAR-Q)		27	43	ns
t_{PLH}	Propagation Delay Time (CLEAR-CARRY)		32	50	ns
t_{PHL}	Propagation Delay Time (CLEAR-BORROW)		32	50	ns
f_{MAX}	Maximum Clock Frequency	18	32		MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (UP, DOWN-Q)	2.0		—	96	190	—	240	—	285	ns
		4.5		—	24	38	—	48	—	57	
		6.0		—	20	32	—	41	—	48	
t_{PLH} t_{PHL}	Propagation Delay Time (UP-CARRY)	2.0		—	76	140	—	175	—	210	ns
		4.5		—	18	28	—	35	—	42	
		6.0		—	15	24	—	30	—	36	
t_{PLH} t_{PHL}	Propagation Delay Time (DOWN-BORROW)	2.0		—	76	140	—	175	—	210	ns
		4.5		—	18	28	—	35	—	42	
		6.0		—	15	24	—	30	—	36	
t_{PLH} t_{PHL}	Propagation Delay Time (LOAD-Q)	2.0		—	128	250	—	315	—	375	ns
		4.5		—	32	50	—	63	—	75	
		6.0		—	27	43	—	54	—	64	

AC ELECTRICAL CHARACTERISTICS (Continued)

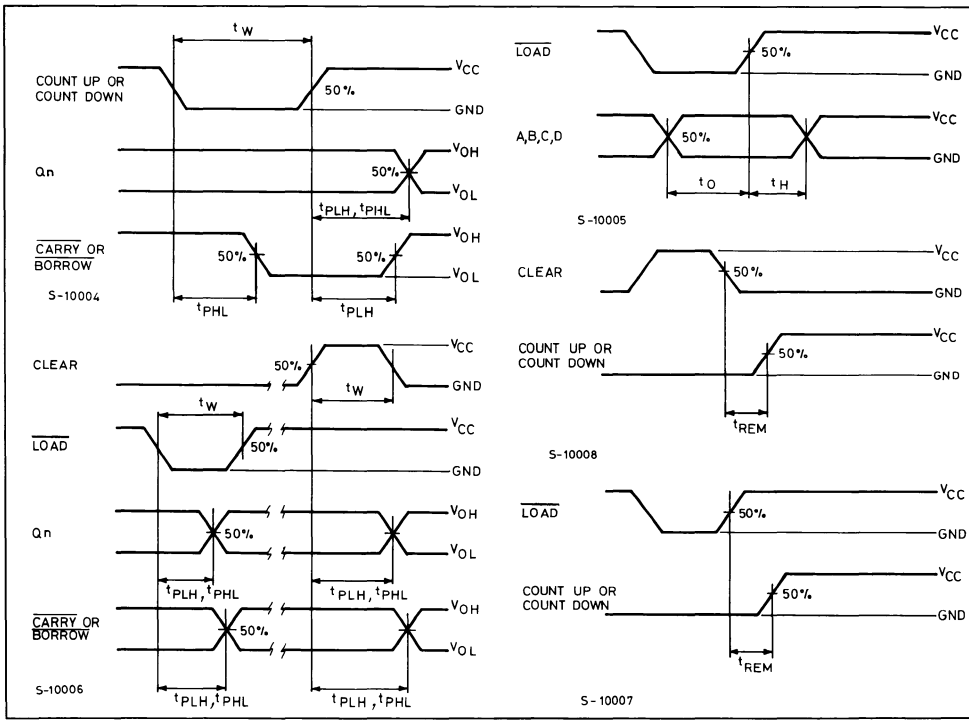
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (LOAD-CARRY)	2.0		—	160	310	—	390	—	465	ns
		4.5		—	40	62	—	78	—	93	
		6.0		—	34	53	—	66	—	79	
t_{PLH} t_{PHL}	Propagation Delay Time (LOAD-BORROW)	2.0		—	144	280	—	350	—	420	ns
		4.5		—	36	56	—	70	—	84	
		6.0		—	31	48	—	60	—	71	
t_{PLH} t_{PHL}	Propagation Delay Time (ANY IN-Q)	2.0		—	116	230	—	290	—	345	ns
		4.5		—	29	46	—	58	—	69	
		6.0		—	25	39	—	49	—	59	
t_{PLH} t_{PHL}	Propagation Delay Time (ANY IN-$\overline{\text{CARRY}}$)	2.0		—	172	330	—	415	—	495	ns
		4.5		—	43	66	—	83	—	99	
		6.0		—	37	56	—	71	—	84	
t_{PLH} t_{PHL}	Propagation Delay Time (ANY IN-$\overline{\text{BORROW}}$)	2.0		—	144	275	—	345	—	415	ns
		4.5		—	36	55	—	69	—	83	
		6.0		—	31	47	—	59	—	71	
t_{PHL}	Propagation Delay Time (CLEAR-Q)	2.0		—	128	245	—	305	—	370	ns
		4.5		—	32	49	—	61	—	74	
		6.0		—	27	42	—	52	—	63	
t_{PLH}	Propagation Delay Time (CLEAR-$\overline{\text{CARRY}}$)	2.0		—	148	285	—	355	—	430	ns
		4.5		—	37	57	—	71	—	86	
		6.0		—	31	48	—	60	—	73	
t_{PHL}	Propagation Delay Time (CLEAR-$\overline{\text{BORROW}}$)	2.0		—	148	285	—	355	—	430	ns
		4.5		—	37	57	—	71	—	86	
		6.0		—	31	48	—	60	—	73	
f_{MAX}	Maximum Clock Frequency	2.0		3	7	—	2.6	—	2	—	MHz
		4.5		16	29	—	13	—	11	—	
		6.0		19	34	—	15	—	13	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	70	150	—	190	—	225	ns
		4.5		—	17	30	—	38	—	45	
		6.0		—	14	26	—	33	—	38	
$t_{W(H)}$	Minimum Pulse Width ($\overline{\text{LOAD}}$)	2.0		—	50	100	—	125	—	150	ns
		4.5		—	12	20	—	25	—	30	
		6.0		—	10	17	—	21	—	26	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0		—	45	100	—	125	—	150	ns
		4.5		—	11	20	—	25	—	30	
		6.0		—	9	17	—	21	—	26	
t_{REM}	Minimum Removal Time ($\overline{\text{LOAD}}$)	2.0		—	20	75	—	95	—	110	ns
		4.5		—	5	15	—	19	—	22	
		6.0		—	4	13	—	16	—	19	
t_{REM}	Minimum Removal Time (CLEAR)	2.0		—	5	50	—	65	—	75	ns
		4.5		—	1	10	—	13	—	15	
		6.0		—	1	9	—	11	—	13	

AC ELECTRICAL CHARACTERISTICS (Continued)

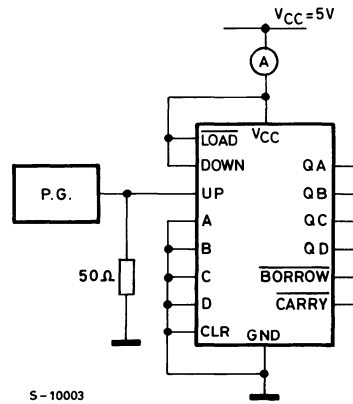
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_s	Minimum Set-up Time (DATA-$\overline{LOAD}$)	2.0		—	40	100	—	125	—	150	ns
		4.5		—	10	20	—	25	—	30	
		6.0		—	9	17	—	21	—	26	
t_h	Minimum Hold Time ($\overline{DATA}$-$\overline{LOAD}$)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	66	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current is: $I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



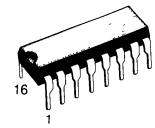
TEST CIRCUIT I_{CC} (Opr.)



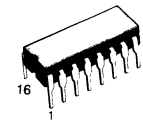
TRANSITION TIME OF INPUT WAVEFORMS IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

4 BIT PIPO SHIFT REGISTER

- HIGH SPEED
  t_{PD} = 13 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN).
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4mA (MIN).
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN).
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS194



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

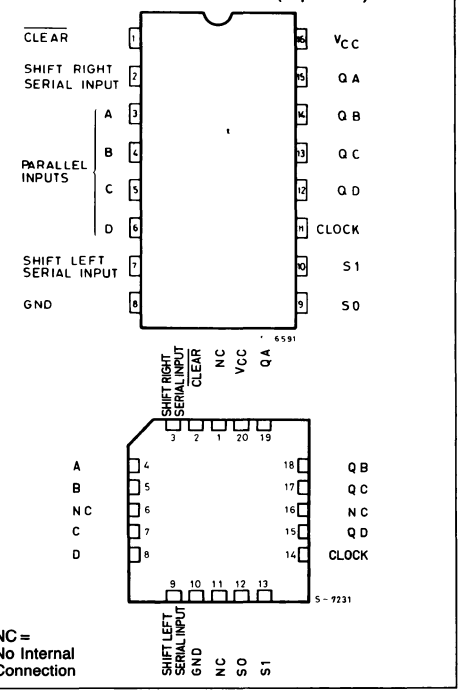
ORDERING NUMBERS:
M54HC194 F1
M74HC194 B1N
M74HC194 F1
M74HC194 C1
M74HC194 M1

DESCRIPTION

The M54/74HC194 is a high speed CMOS 4 BIT PIPO SHIFT REGISTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

This SHIFT REGISTER is designed to incorporate virtually all of the features a system designer may want in a shift register. It features parallel inputs, parallel outputs, right shift and left shift serial inputs, clear line. The register has four distinct modes of operation: PARALLEL (broadside) LOAD; SHIFT RIGHT (in the direction Q_A Q_D); SHIFT LEFT; INHIBIT CLOCK (do nothing). Synchronous parallel loading is accomplished by applying the four data bits and taking both mode control inputs, S0 and S1 high. The data are loaded into their respective flip-flops and appear at the outputs after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the SHIFT RIGHT data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the SHIFT LEFT serial input. Clocking of the flip flops is inhibited when both mode control inputs are low. The mode control inputs should be changed only when the CLOCK input is high. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)



NC = No Internal Connection

TRUTH TABLE

INPUTS										OUTPUTS			
$\overline{CLEAR}$	MODE		CLOCK	SERIAL		PARALLEL				QA	QB	QC	QD
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	↓	X	X	X	X	X	X	QA0	QB0	QC0	QD0
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	QAn	QBn	QCn
H	L	H	↑	X	L	X	X	X	X	L	QAn	QBn	QCn
H	H	L	↑	H	X	X	X	X	X	QBn	QCn	QDn	H
H	H	L	↑	L	X	X	X	X	X	QBn	QCn	QDn	L
H	L	L	X	X	X	X	X	X	X	QA0	QB0	QC0	QD0

X : DON'T CARE
a~d : THE LEVEL OF STEADY STATE INPUT VOLTAGE AT INPUT A ~ D RESPECTIVELY
QAO~QDO : NO CHANGE
QAn~QDn : THE LEVEL OF QA, QB, QC, RESPECTIVELY, BEFORE THE MOST-RECENT POSITIVE TRANSITION OF THE CLOCK.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

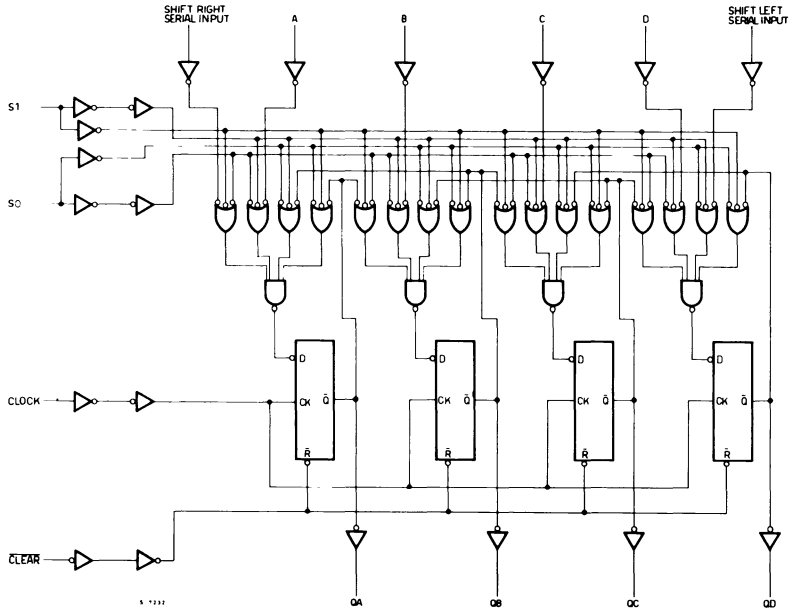
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

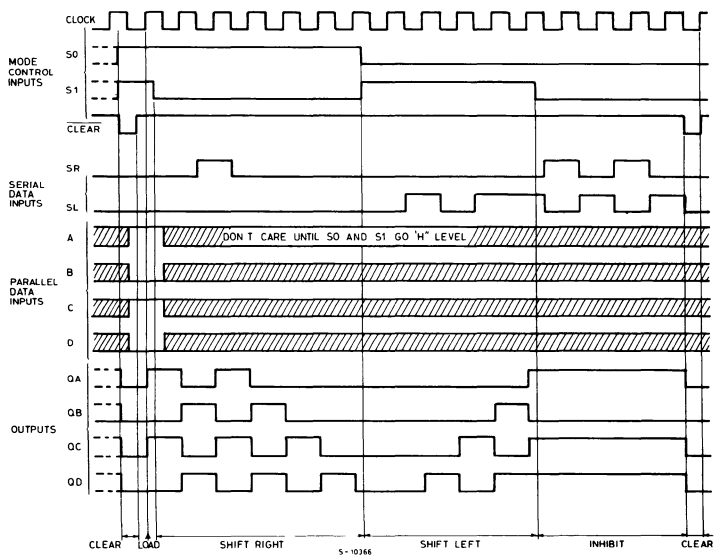
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series Operating Temperature 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

LOGIC DIAGRAM



TIMING CHART



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-QN)		13	21	ns
t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$-Q)		16	25	ns
f_{MAX}	Maximum Clock Frequency	33	55		MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

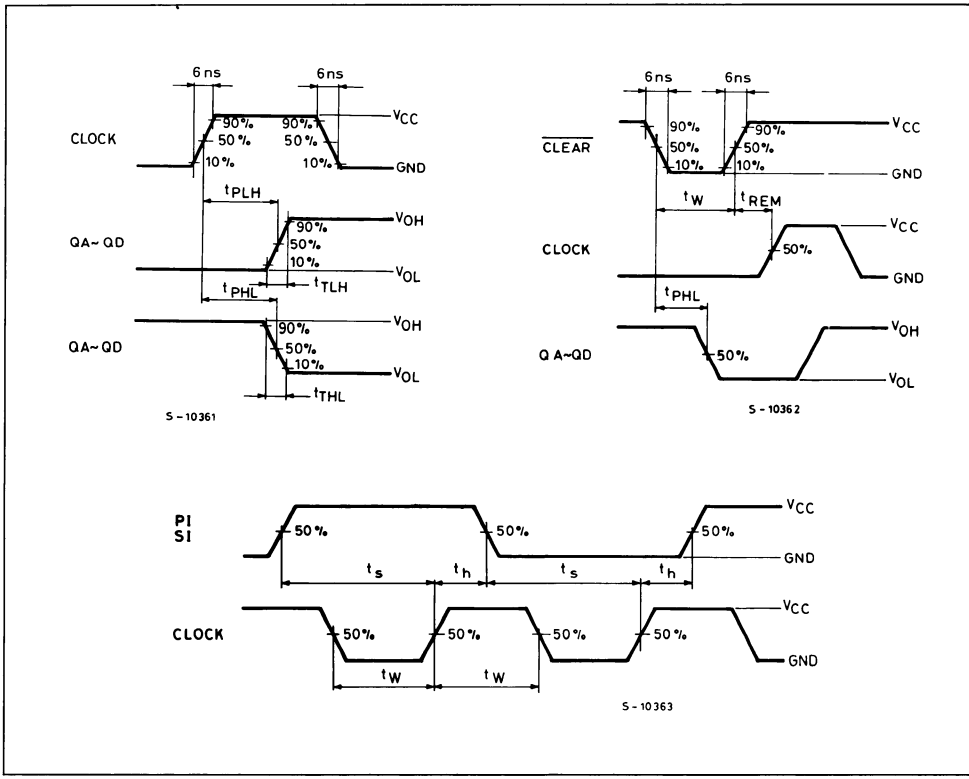
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q,N)	2.0		—	64	130	—	165		195	ns
		4.5		—	16	26	—	33		39	
		6.0		—	14	22	—	28		33	
t_{PLH}	Propagation Delay Time ($\overline{CLEAR}$-Q)	2.0		—	76	150	—	190		225	ns
		4.5		—	19	30	—	38		45	
		6.0		—	16	26	—	33		38	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
f_{MAX}	Maximum Clock Frequency	2.0		6	10	—	4.8	—	4	—	MHz
		4.5		30	50	—	24	—	20	—	
		6.0		35	58	—	28	—	24	—	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLEAR}$)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_s	Minimum Set-up Data Time (SIN-PIN)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_s	Minimum Set-up Data Time (Mode Control-CK)	2.0		—	40	100	—	125	—	150	ns
		4.5		—	10	20	—	25	—	30	
		6.0		—	9	17	—	21	—	26	
t_{REM}	Minimum Removal Time ($\overline{CLEAR}$)	2.0		—	—	25	—	30	—	40	ns
		4.5		—	—	5	—	6	—	8	
		6.0		—	—	5	—	6	—	7	
t_h	Minimum Hold Time SIN/PIN-CK, Mode, Ctr-CK	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	102	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

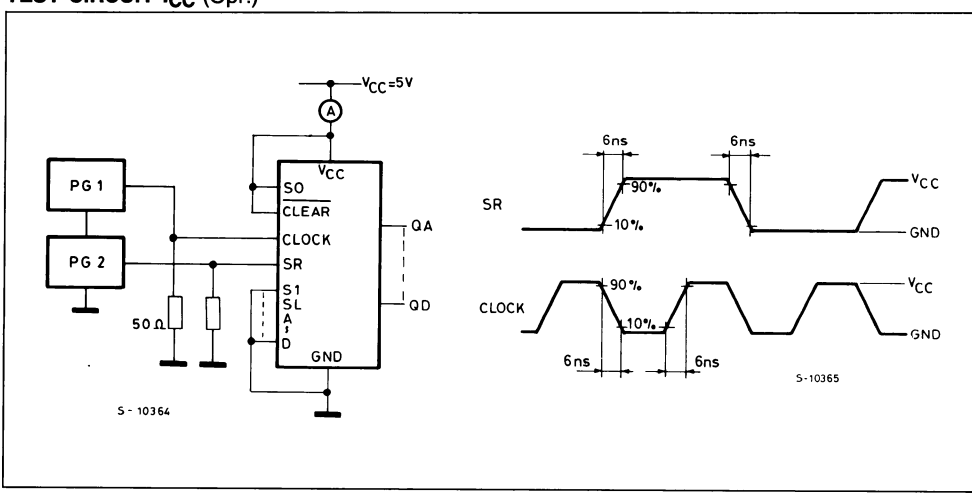
Average operating current can be obtained by the following equation.

$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)

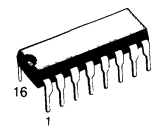


SGS-THOMSON MICROELECTRONICS

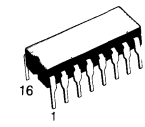
M54HC195
M74HC195

4 BIT PIPO SHIFT REGISTER

- HIGH SPEED
  t_{PD} = 14 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C 6V
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC}(MIN)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4mA (MIN)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS195



B1N
Plastic Package



F1
Ceramic Frit Seal Package

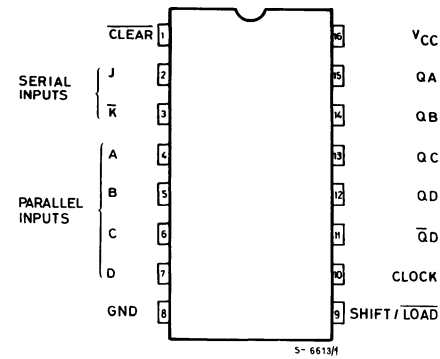
M1
Micro Package

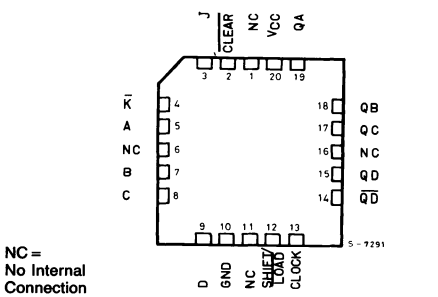
C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC195 F1
M74HC195 B1N
M74HC195 F1
M74HC195 C1
M74HC195 M1

PIN CONNECTIONS (top view)





NC = No Internal Connection

DESCRIPTION

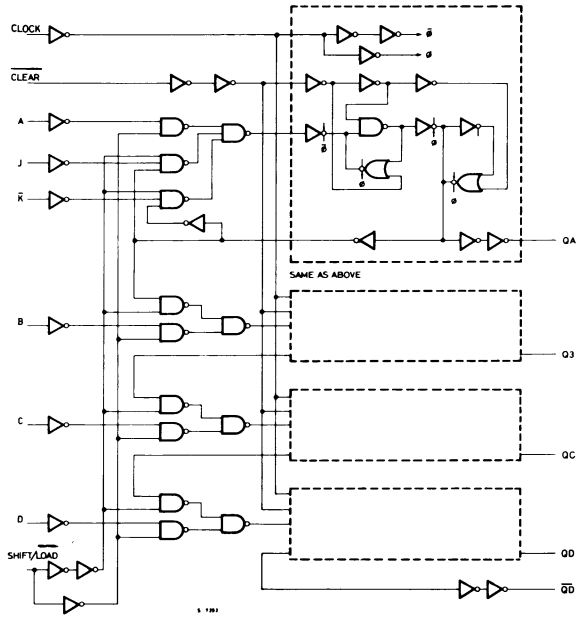
The M54/74HC195 is a high speed CMOS 4 BIT PIPO SHIFT REGISTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

This shift register features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, a SHIFT/$\overline{\text{LOAD}}$ control input, and a direct overriding $\overline{\text{CLEAR}}$. This shift register can operate in two modes: Parallel Load; Shift from QA towards QD.

Parallel loading is accomplished by applying the four bits of data, and taking the SHIFT/$\overline{\text{LOAD}}$ control input low. The data is loaded into the associated flip flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited. Serial shifting occurs synchronously when the SHIFT/$\overline{\text{LOAD}}$ control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs allow the first stage to perform as a J-$\overline{K}$ or TOGGLE flip flop as shown in the truth table.

All inputs are equipped with protection circuits against static discharge transient excess voltage.

LOGIC DIAGRAM

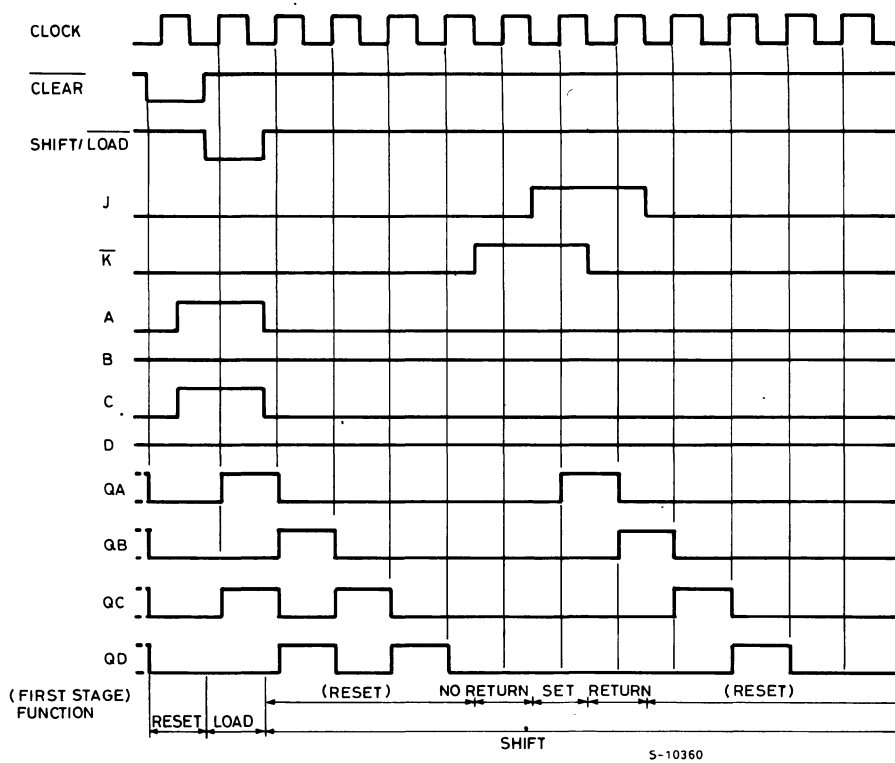


TRUTH TABLE

INPUTS									OUTPUTS				
CLEAR	SHIFT/LOAD	CLOCK	SERIAL		PARALLEL				QA	QB	QC	QD	$\overline{QD}$
			J	K	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↓	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	↑	X	X	X	X	X	X	QA0	QB0	QC0	QD0	$\overline{QD0}$
H	H	↓	L	H	X	X	X	X	QA0	QA0	QBn	QCn	$\overline{QCn}$
H	H	↓	L	L	X	X	X	X	L	QAn	QBn	QCn	$\overline{QCn}$
H	H	↓	H	H	X	X	X	X	H	QAn	QBn	QCn	$\overline{QCn}$
H	H	↓	H	L	X	X	X	X	$\overline{QA}$n	QAn	QBn	QCn	$\overline{QCn}$

X: DON'T CARE; ↑: TRANSITION FROM LOW TO HIGH LEVEL; ↓: TRANSITION FROM HIGH TO LOW LEVEL

TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V: 0 to 1000 V_{CC} = 4.5V: 0 to 500 V_{CC} = 6 V: 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0 4.5 6.0 4.5 6.0	V_I V_{IH} or V_{IL}	I_O −20 μA −4.0 mA −5.2 mA	1.9 4.4 5.9 4.18 5.68	2.0 4.5 6.0 4.31 5.8	— — — — —	1.9 4.4 5.9 4.13 5.63	— — — — —	1.9 4.4 5.9 4.10 5.60	— — — — —	V
V_{OL}	Low Level Output Voltage	2.0 4.5 6.0 4.5 6.0	V_{IH} or V_{IL}	20 μA 4.0 mA 5.2 mA	— — — — —	0.0 0.0 0.0 0.17 0.18	0.1 0.1 0.1 0.26 0.26	— — — — —	0.1 0.1 0.1 0.33 0.33	— — — — —	0.1 0.1 0.1 0.40 0.40	V
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input t_r = t_f = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-QN, QD)		14	23	ns
t_{PHL}	Propagation Delay Time (CL-QN, $\overline{QD}$)		17	27	ns
f_{MAX}	Maximum Clock Frequency	35	56		MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

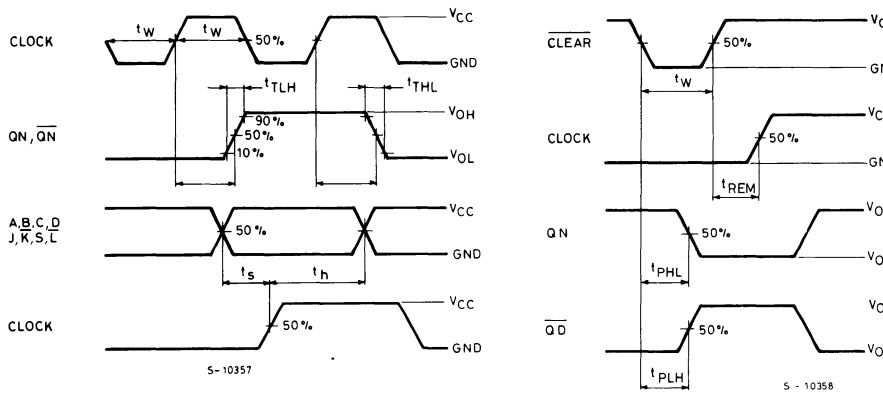
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-QN, $\overline{QD}$)	2.0		—	76	145	—	180		220	ns
		4.5		—	19	29	—	36		44	
		6.0		—	16	25	—	31		38	
t_{PLH} t_{PHL}	Propagation Delay Time (CL-QN, QD)	2.0		—	84	160	—	200		240	ns
		4.5		—	21	32	—	40		48	
		6.0		—	18	27	—	34		41	
f_{MAX}	Maximum Clock Frequency	2.0		6.4	13	—	5.2	—	4.2	—	MHz
		4.5		32	51	—	26	—	21	—	
		6.0		38	60	—	31	—	25	—	
$t_{W(L)}$	Minimum Pulse Width (CL)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CK)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_s	Minimum Set-up Time (PI)	2.0		—	15	50	—	65		75	ns
		4.5		—	4	10	—	13		15	
		6.0		—	3	9	—	11		13	
t_s	Minimum Set-up Time (J, $\overline{K}$, S/$\overline{L}$)	2.0		—	36	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{REM}	Minimum Removal Time	2.0		—	5	25	—	30	—	40	ns
		4.5		—	1	5	—	6	—	8	
		6.0		—	1	5	—	6	—	7	
t_h	Minimum Hold Time (PIN, SIN-CK)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_h	Minimum Hold Time (S/L-CK)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	126	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

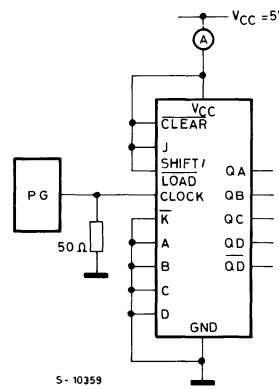
Average operating current can be obtained by the following equation

$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



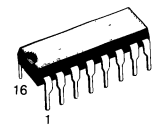
TEST CIRCUIT I_{CC} (Opr.)



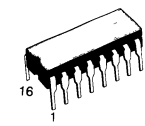
TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

DUAL MONOSTABLE MULTIVIBRATORS

- HIGH SPEED
  t_{PD} = 32 ns (TYP) at V_{CC} = 5V
- LOW POWER DISSIPATION
  STANDBY STATE I_{CC} = 4 μA (MAX.) at T_A = 25°C
  ACTIVE STATE I_{CC} = 200 μA (TYP) at V_{CC} = 5V
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OUTPUT PULSE WIDTH RANGE
  t_{WOUT} = 150ns ~ 60s over at V_{CC} = 4.5V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS221



B1N
Plastic Package



F1
Ceramic Frit Seal Package

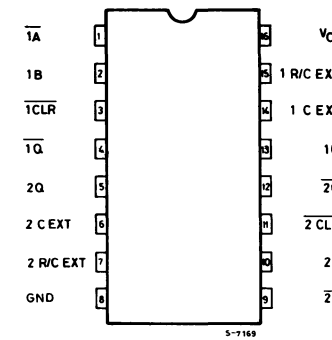
M1
Micro Package

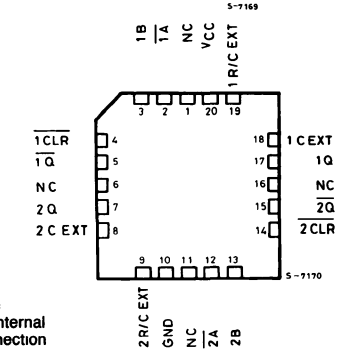
C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC221 F1
M74HC221 B1N
M74HC221 F1
M74HC221 C1
M74HC221 M1

PIN CONNECTIONS (top view)





NC = No Internal Connection

DESCRIPTION

The M54/74HC221 is a high speed CMOS MONOSTABLE multivibrator fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. There are two trigger inputs, A INPUT (negative edge) and B INPUT (positive edge). These inputs are valid for rising/falling signals, (t_r-t_f-I sec).
The device may also be triggered by using the CLR input (positive-edge) because of the Schmitt-trigger input; after triggering the output maintains the MONOSTABLE state for the time period determined by the external resistor Rx and capacitor Cx. Taking $\overline{CLR}$ low breaks this MONOSTABLE STATE. If the next trigger pulse occurs during the MONOSTABLE period it makes the MONOSTABLE period longer. Limit for values of Cx and Rx:

Cx : NO LIMIT

Rx : V_{CC} = 2.0V 5KΩ to 1MΩ
V_{CC} = 3.0V 1KΩ to 1MΩ

All inputs are equipped with protection circuits against static discharge and transient excess voltage

TRUTH TABLE

INPUTS			OUTPUTS		NOTE
$\overline{A}$	B	$\overline{CLR}$	Q	$\overline{Q}$	
↓	H	H	⎍	⎍	OUTPUT ENABLE
X	L	H	L▲	H▲	INHIBIT
H	X	H	L▲	H▲	INHIBIT
L	↑	H	⎍	⎍	OUTPUT ENABLE
L	H	↑	⎍	⎍	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X: DON'T CARE
▲: EXCEPT FOR MONOSTABLE PERIOD

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

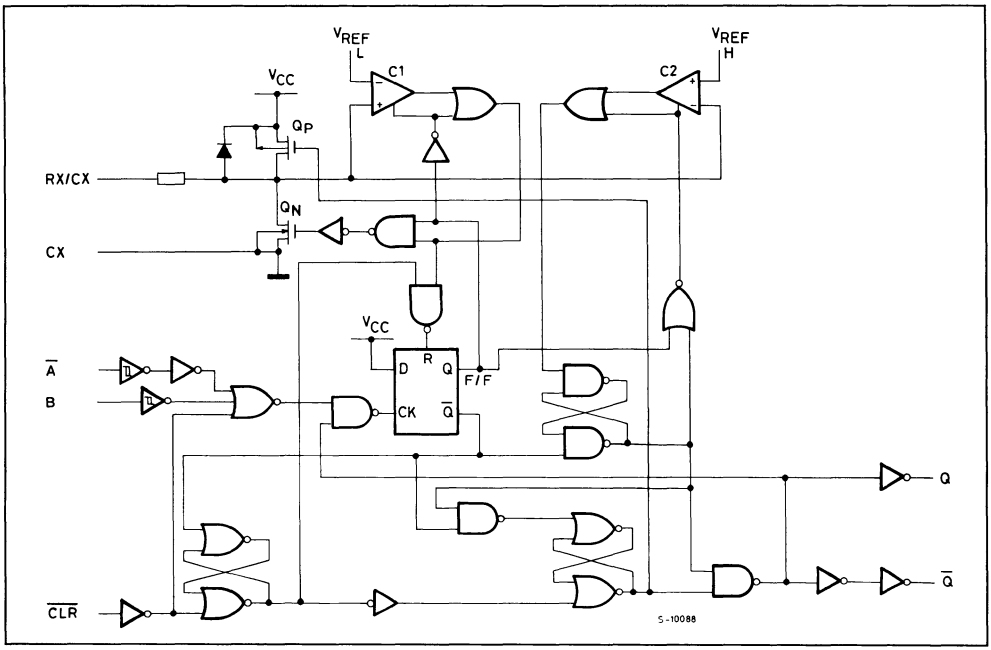
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

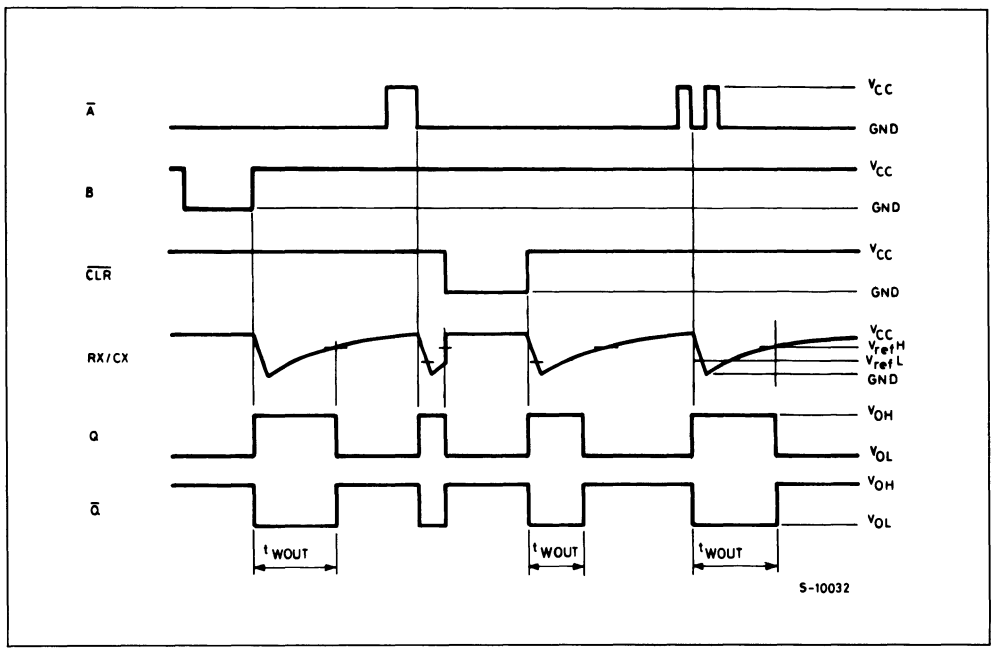
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time ($\overline{CLR}$ only)	V_{CC}	2 V: 0 to 1000 4.5V: 0 to 500 6 V: 0 to 400	ns
Cx	External Capacitor	NO LIMITATION		F
Rx	External Resistor	V_{CC}	3 V: 5K to 1M 3 V: 1K to 1M	Ω

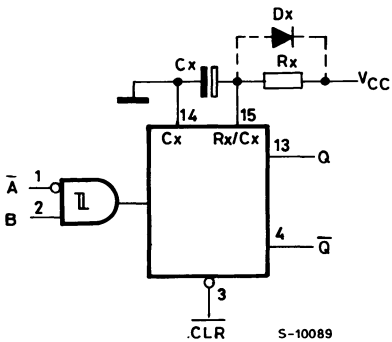
LOGIC DIAGRAM

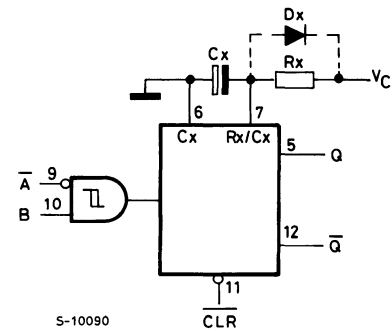


TIMING CHART



BLOCK DIAGRAM





Note:
(1) Cx, Rx, Dx are external components.
(2) Dx is a clamping diode

The external capacitor is charged to V_{CC} in the stand-by state, i.e. no trigger. When the supply voltage is turned off Cx is discharged mainly through an internal parasitic diode (see figures). If Cx is sufficiently large and V_{CC} decreases rapidy, there will be some possibility of damaging the I.C. with a surge current or latch-up. If the voltage supply filter capacitor is large enough and V_{CC} decrease slowly, the surge current is automatically limited and damage the I.C. is avoided. The maximum forward current of the parasitic diode is approximately 20 mA. In cases where Cx is large the time taken for the supply voltage to fall to 0.4 V_{CC} can be calculated as follows:

$t_f \geqq (V_{CC} - 0.7) \cdot Cx/20mA$

In cases where t_f is too short an external clamping diode is required to protect the I.C. from the surge current.

FUNCTIONAL DESCRIPTION

Stand-by state

The external capacitor, Cx, is fully charged to V_{CC} in the stand-by state. Hence, before triggering, transistor Qp and Qn (connected to the Rx/Cx node) are both turned off. The two comparators that control the timing and the two reference voltage sources stop operating. The total supply current is therefore only leakage current.

Trigger operation

Triggering occurs when:
1st) A is "low" and B has a falling edge;
2nd) B is "high" and A has a rising edge;
3rd) A is low and B is high and C1 has a rising edge.

After the multivibrator has been retriggered comparator C1 and C2 start operating and Qn is turned on. Cx then discharges through Qn. The voltage at the node Rx/Cx external falls.
When it reaches V_{REFL} the output of comparator C1 becomes low. This in turn resets the flip-flop and Qn is turned off. At this point C1 stops functioning but C2 continues to operate.
The voltage at R/C external begins to rise with a time constant set by the external components Rx, Cx. Triggering the multivibrator causes Q to go high after internal delay due to the flip-flop and the gate. Q remains high until the voltage at R/C external rises again to V_{REFH}.
At this point C2 output goes low and O goes low. C2 stops operating.
That means that after triggering when the voltage R/C external returns to V_{REFH} the multivibrator has returned to its MONOSTABLE STATE. In the case where Rx • Cx are large enough and the discharge time of the capacitor and the delay time in the I.C. can be ignored, the width of the output pulse tw (out) is as follows:

$$t_{W(OUT)} = 0.70\ Cx \cdot Rx$$

Reset Operation

CL is normally high. If CL is low, the trigger is not effective because Q output goes low and trigger control flip-flop is reset.
Also transistor Qp is turned on and Cx is charged quickly to V_{CC}. This means if CL input goes low, the IC becomes waiting state both in operating and non operating state.

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage (Q, $\overline{Q}$ Output)	2.0 4.5 6.0 4.5 6.0	V_{IN} V_{IH} or V_{IL}	I_O −20 μA −4.0 mA −5.2 mA	1.9 4.4 5.9 4.18 5.68	2.0 4.5 6.0 4.31 5.8	— — — — —	1.9 4.4 5.9 4.13 5.63	— — — — —	1.9 4.4 5.9 4.10 5.60	— — — — —	V
V_{OL}	Low Level Output Voltage (Q, $\overline{Q}$ Output)	2.0 4.5 6.0 4.5 6.0	V_{IH} or V_{IL}	20 μA 4.0 mA 5.2 mA	— — — — —	0 0 0 0.17 0.18	0.1 0.1 0.1 0.26 0.26	— — — — —	0.1 0.1 0.1 0.33 0.33	— — — — —	0.1 0.1 0.1 0.40 0.40	V
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_I	R/C Terminal Off-State Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.5	—	±5	—	±10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA
I_{CC}'	Active-State (1) Supply Current	2.0 4.5 6.0	$V_I = V_{CC}$ $R/C_{ext} = 0.5\ V_{CC}$		— — —	40 0.1 0.2	120 0.3 0.6	— — —	160 0.4 0.8	— — —	200 0.5 1.0	μA mA mA

(1): Per Circuit

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

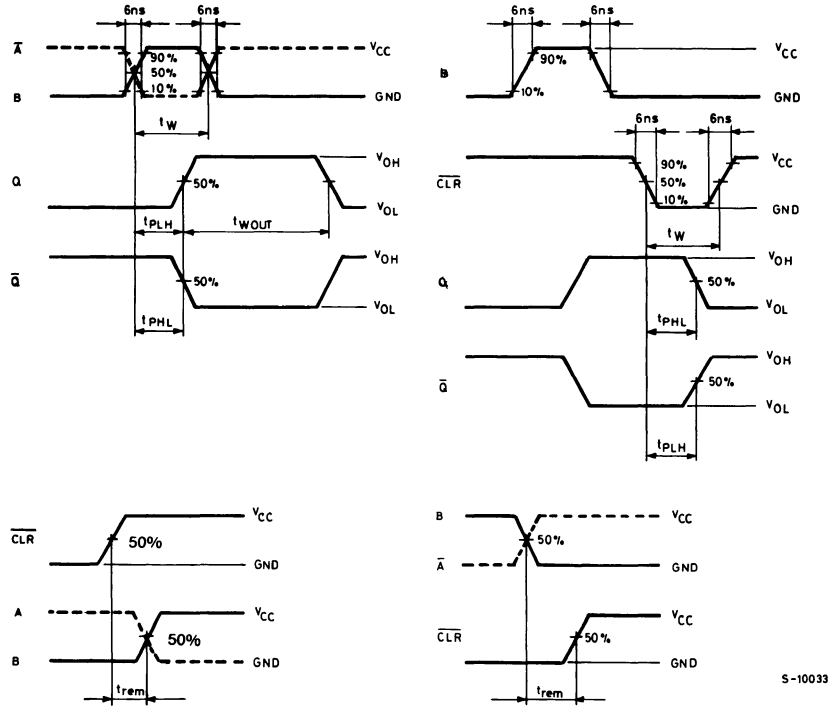
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{A}$, B TRIGGER - Q, $\overline{Q}$)		32	49	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$ TRIGGER - Q, $\overline{Q}$)		35	55	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$ - Q, $\overline{Q}$)		23	37	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

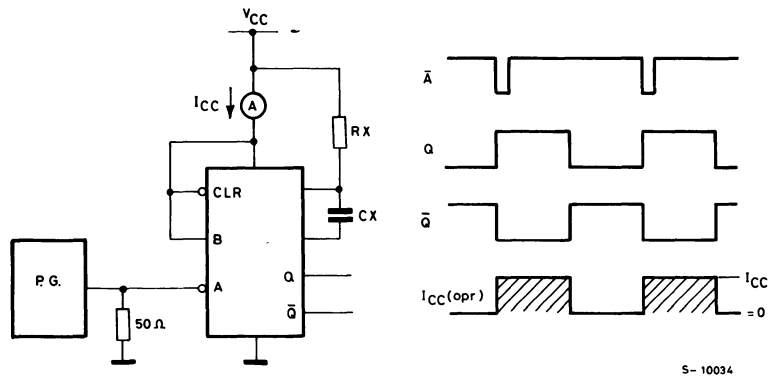
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{A}$,B TRIG. - Q,$\overline{Q}$)	2.0		—	144	280	—	350	—	420	ns
		4.5		—	36	56	—	70	—	84	
		6.0		—	31	48	—	60	—	71	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$ TRIG. - Q,$\overline{Q}$)	2.0		—	164	310	—	390	—	465	ns
		4.5		—	41	62	—	78	—	95	
		6.0		—	35	53	—	66	—	79	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$ - Q,$\overline{Q}$)	2.0		—	108	210	—	265	—	315	ns
		4.5		—	27	42	—	53	—	63	
		6.0		—	23	36	—	45	—	54	
$t_{W(H)}$ $t_{W(L)}$	Minimum Trigger Pulse Width	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
$t_{W(L)}$	Minimum Clear Pulse Width	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
$\Delta t_{W(OUT)}$	Output Pulse Width Error. Between Circuits in Same Package			—	±1	—	—	—	—	—	%
t_{REM}	Minimum Removal Time ($\overline{A}$,B TRIGGER)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{REM}	Minimum Removal Time ($\overline{CLR}$ TRIGGER)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{WOUT} (Min).	Minimum Output Pulse Width	2.0	Cx = 0pF	—	490	1450	—	1825	—	2185	ns
		4.5	Rx = 5kpFΩ(V_{CC} = 2V)	—	190	290	—	365	—	437	
		6.0	Rx = 1kΩ(V_{CC} = 4.5,6V)	—	170	260	—	325	—	373	
t_{WOUT}	Output Pulse Width	2.0	Cx = 0.01μF	72	85	98	72	98	72	98	μs
		4.5	Rx = 10kΩ	72	80	88	72	88	72	88	
		6.0		72	80	88	72	88	72	88	
		2.0	Cx = 0.1μF	0.67	0.75	0.83	0.67	0.83	0.67	0.83	ms
		4.5	Rx = 10kΩ	0.67	0.73	0.79	0.67	0.79	0.67	0.79	
		6.0		0.67	0.73	0.79	0.67	0.79	0.67	0.79	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	109	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test circuit). Average operating current can be obtained by equation hereunder:
$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC'} \cdot Duty/100 + I_{CC}/2$ (per monostable) ($I_{CC'}$: Active Supply Current, Duty: %)

SWITCHING CHARACTERISTICS TEST WAVEFORM



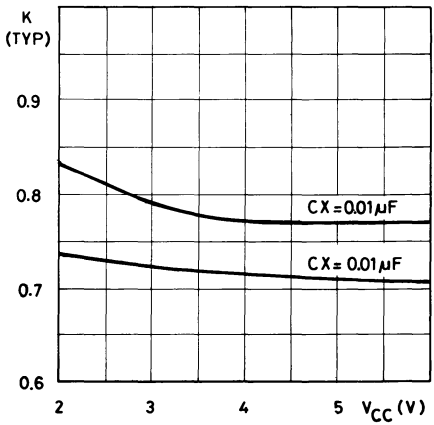
TEST WAVEFORM



Input Transition Time: 6ns
$V_{IH} = V_{CC}$, $V_{IL} = GND$

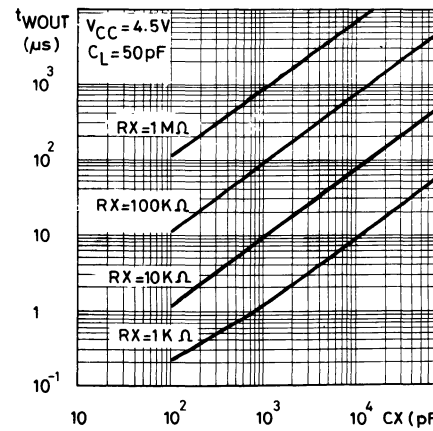
Output Pulse Width Constant
K-Supply voltage

G-6372



t_{W}OUT-Cx Characteristics (Typ).

G-6373

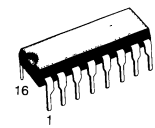


SGS-THOMSON MICROELECTRONICS

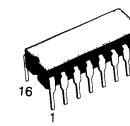
M54HC237
M74HC237

3 TO 8 LINE DECODER LATCH

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (Min.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS237



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

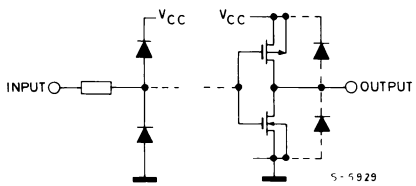
ORDERING NUMBERS:

M54HC237 F1
M74HC237 B1N
M74HC237 F1
M74HC237 C1
M74HC237 M1

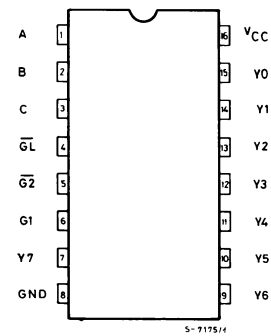
DESCRIPTION

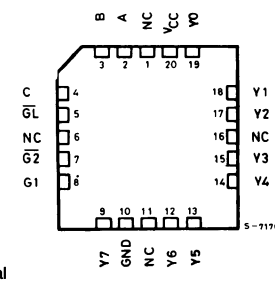
The M54/74HC237 is a high speed CMOS 3 TO 8 LINE DECODER LATCH fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B, C) is stored in the latches. As long as $\overline{GL}$ remains high no address changes will be recognized. Output enable controls, G1 and $\overline{G2}$ control the state of the outputs independantly of the select or latch-enable inputs. All of the outputs are low unless G1 is high and $\overline{G2}$ is low. The 'HC237 is ideally suited for the implementation of glitch-free decoders in stored-address applications in bus oriented systems. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





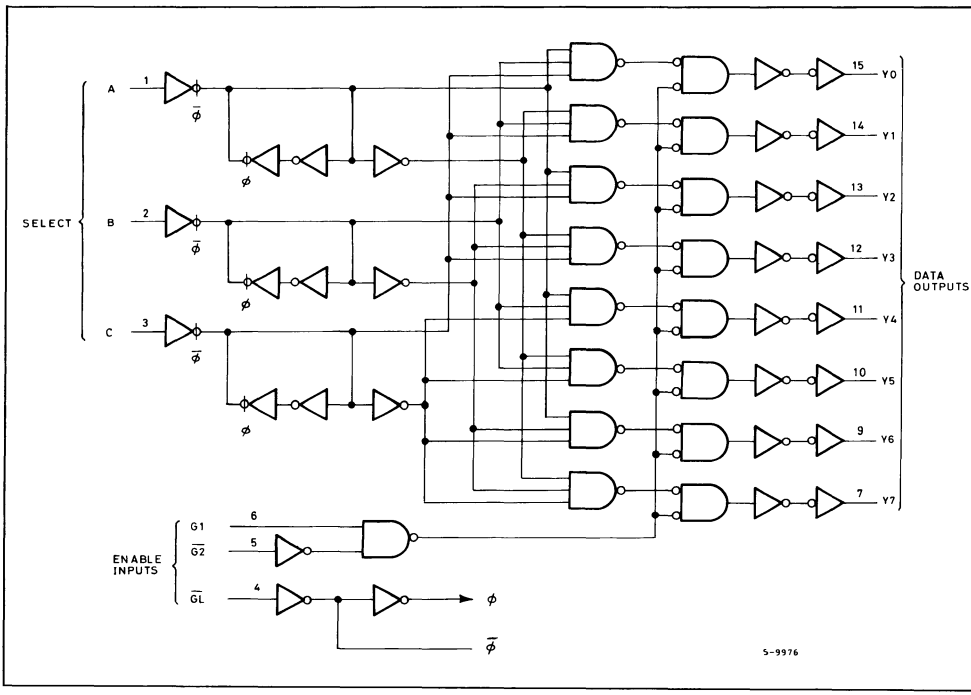
NC = No Internal Connection

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{G1}$	$\overline{G2}$	G1	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	L	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	L	L	H	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	L	H	H	L	L	L	H	L	L	L	L
L	L	H	H	L	L	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H
H	L	H	X	X	X	OUTPUT CORRESPONDING TO STORED ADDRESS, H; ALL OTHERS, L							

X = DON'T CARE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_{IN}	I_{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0	or		5.9	6.0	—	5.9	—	5.9	—	
		4.5	V_{IL}	−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	

DC SPECIFICATIONS (Continued)

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	4	—	40	—	80	

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$)

Symbol	Parameter	Test Condition	54HC and 74HC			Unit
			Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		—	4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C,-Yn)		—	19	30	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{G1}$-Yn)		—	22	34	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G1, $\overline{G2}$-Yn)		—	16	25	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

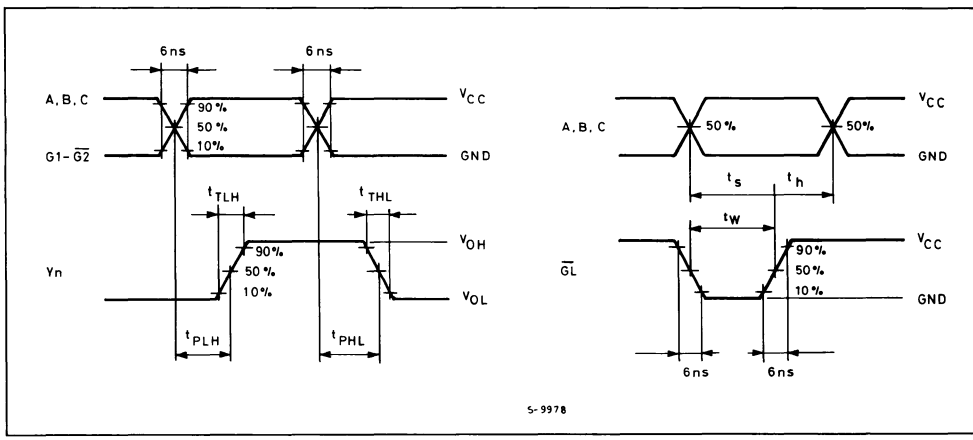
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (Q Outputs)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C,-Yn)	2.0		—	92	180	—	225	—	270	ns
		4.5		—	23	36	—	45	—	54	
		6.0		—	20	31	—	38	—	46	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{G1}$-Yn)	2.0		—	104	200	—	250	—	300	ns
		4.5		—	26	40	—	50	—	60	
		6.0		—	22	34	—	43	—	51	

AC ELECTRICAL CHARACTERISTICS (Continued)

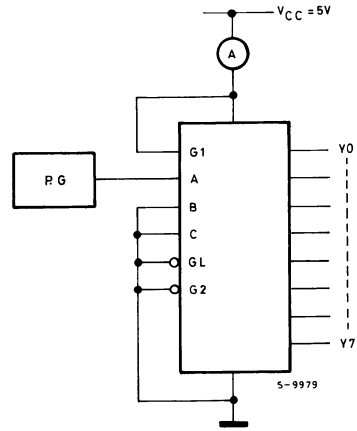
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (G1, $\overline{G2}$-Yn)	2.0		—	76	150	—	190	—	225	ns
		4.5		—	19	30	—	38	—	45	
		6.0		—	16	26	—	33	—	38	
t_W	Minimum Pulse Width	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-up Time	2.0		—	12	50	—	65	—	75	ns
		4.5		—	3	10	—	13	—	15	
		6.0		—	3	9	—	11	—	13	
t_h	Minimum Hold Time	2.0		—	—	25	—	30	—	40	ns
		4.5		—	—	5	—	6	—	8	
		6.0		—	—	5	—	6	—	7	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	68	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current is: $I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

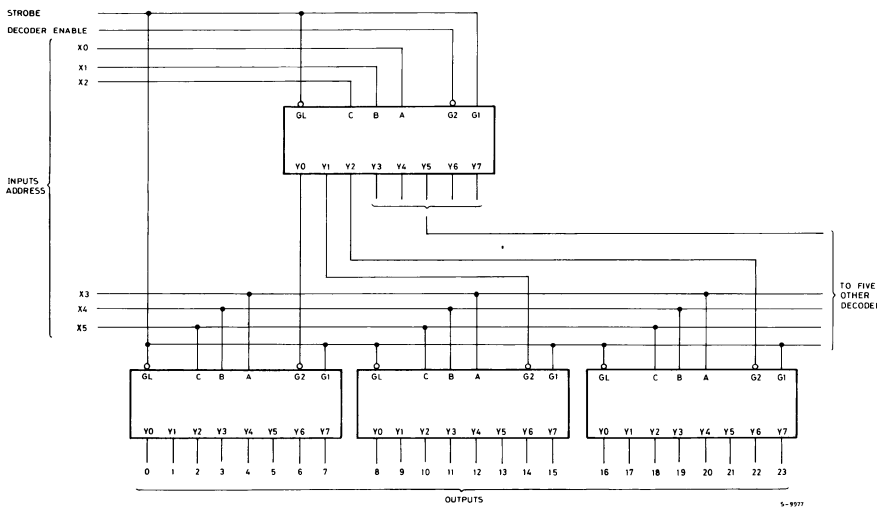


TEST CIRCUIT I_{CC} (Opr.)



INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TYPICAL APPLICATION



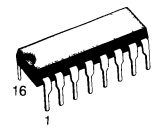
6 Line to 64 Line Decoder with Input Address Storage

SGS-THOMSON MICROELECTRONICS

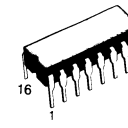
M54HC238
M74HC238

3 TO 8 LINE DECODER

- HIGH SPEED
  t_{PD} = 18 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS238



B1
Plastic Package



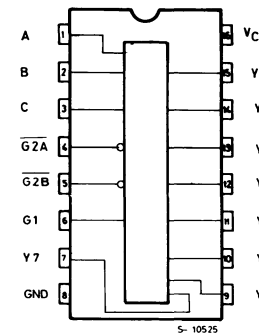
F1
Ceramic Frit Seal Package

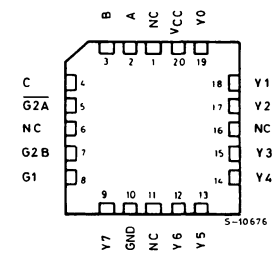
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC238 F1
M74HC238 B1N
M74HC238 F1
M74HC238 M1

PIN CONNECTIONS (top view)





NC = No Internal Connection

DESCRIPTION

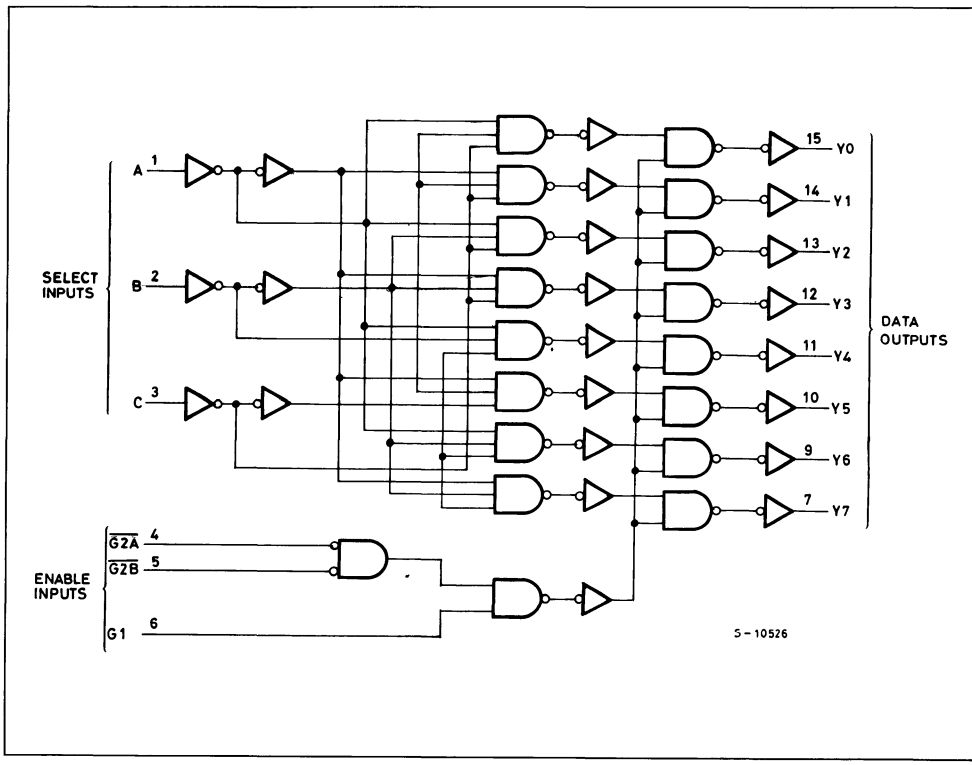
The M54/74HC238 is a high speed CMOS 3 to 8 line decoder fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. If the device is enabled, 3 binary select inputs (A, B and C) determine which one of outputs will go high. Enable input G1 is held "Low" or either G2A or G2B is held "High"decoding function is inhibited and all the 8 outputs go low. Three enable inputs are provided to ease cascade connection and application of this address decoder in memory systems.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			SELECT											
$\overline{G2B}$	$\overline{G2A}$	G1	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	
X	X	L	X	X	X	L	L	L	L	L	L	L	L	NONE
X	H	X	X	X	X	L	L	L	L	L	L	L	L	NONE
H	X	X	X	X	X	L	L	L	L	L	L	L	L	NONE
L	L	H	L	L	L	H	L	L	L	L	L	L	L	Y0
L	L	H	L	L	H	L	H	L	L	L	L	L	L	Y1
L	L	H	L	H	L	L	L	H	L	L	L	L	L	Y2
L	L	H	L	H	H	L	L	L	H	L	L	L	L	Y3
L	L	H	H	L	L	L	L	L	L	H	L	L	L	Y4
L	L	H	H	L	H	L	L	L	L	L	H	L	L	Y5
L	L	H	H	H	L	L	L	L	L	L	L	H	L	Y6
L	L	H	H	H	H	L	L	L	L	L	L	L	H	Y7

X: = DON'T CARE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

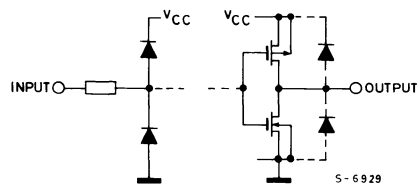
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW = 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series Operating Temperature 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

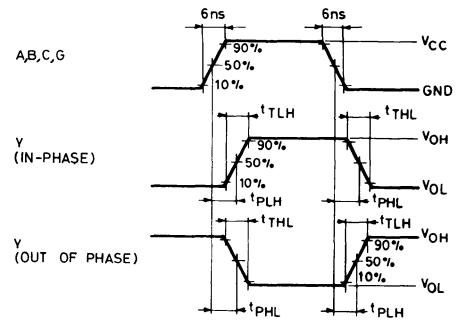
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A,B,C-Y)		18	28	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G1-Y)		17	27	ns
t_{PLH} t_{PHL}	Propagation delay Time ($\overline{G2}$-Y)		19	29	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

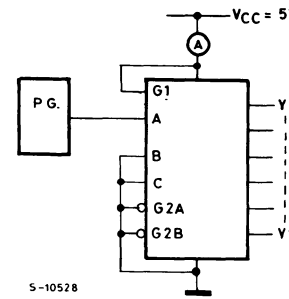
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (A,B,C-Y)	2.0		—	84	165	—	205	—	250	ns
		4.5		—	21	33	—	41	—	50	
		6.0		—	18	28	—	35	—	43	
t_{PLH} t_{PHL}	Propagation Delay Time (G1-Y)	2.0		—	80	155	—	195	—	235	ns
		4.5		—	20	31	—	39	—	47	
		6.0		—	17	26	—	33	—	40	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{G2}$-Y)	2.0		—	88	170	—	215	—	255	ns
		4.5		—	22	34	—	43	—	51	
		6.0		—	19	29	—	37	—	43	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	67	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained from the equation: $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)

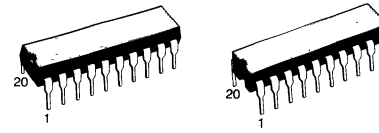


INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

HC240 OCTAL BUS BUFFER WITH INVERTED 3-STATE OUTPUTS
HC241/244 OCTAL BUS BUFFER WITH NON INVERTED 3-STATE OUTPUTS

PRELIMINARY DATA

- HIGH SPEED
  t_{PD} = 12 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS240/244



B1N
Plastic Package

F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX C1
M74HCXXX M1

DESCRIPTION

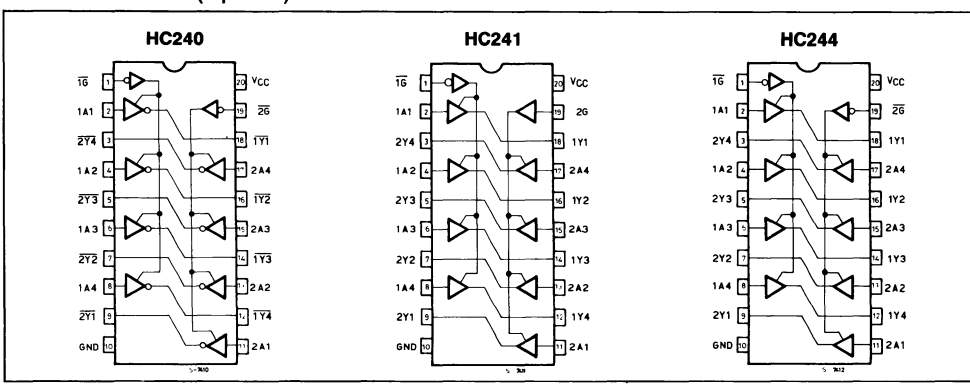
The M54/74HC240, M54/74HC241 and M54HC244 are high speed CMOS OCTAL BUS BUFFER's fabricated in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. The designer has a choice of selected combinations of inverting and non-inverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. Each control input governs four BUS BUFFERs.
These devices are designed to be used with 3-state memory address drivers, etc. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

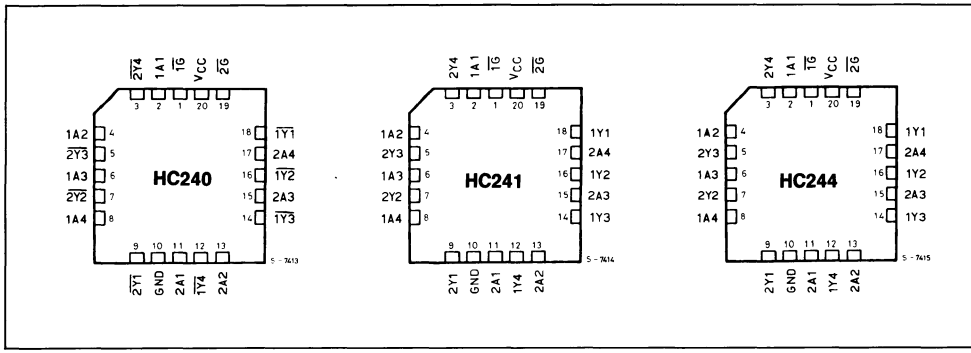
INPUTS			OUTPUTS	
$\overline{G}$	G^{Δ}	An	Yn	$\overline{Y}n^{\Delta\Delta}$
L	H	L	L	H
L	H	H	H	H
H	L	X	Z	Z

X: DON'T CARE Z: HIGH IMPEDANCE
Δ : APPLIED only for M54/74HC241
$\Delta\Delta$: APPLIED only for M54/74HC240

PIN CONNECTION (top view)



CHIP CARRIER



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

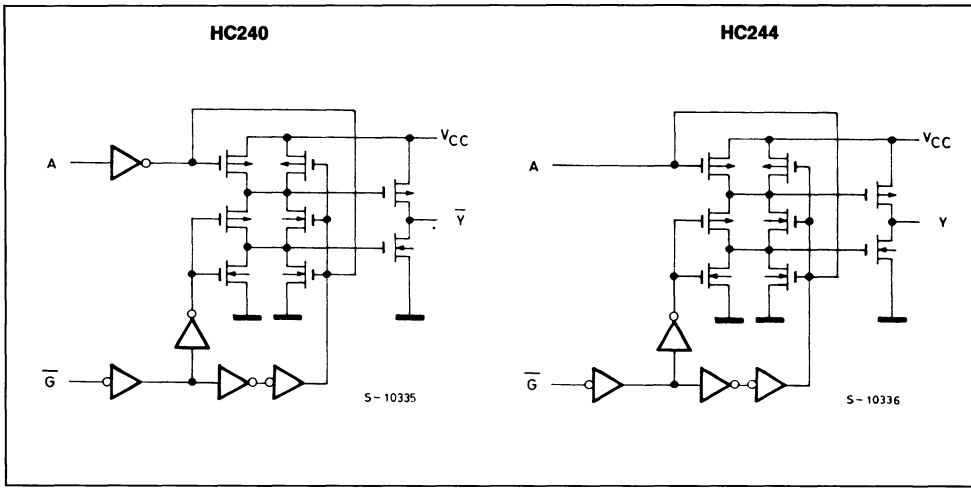
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series Operating Temperature 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

CIRCUIT SCHEMATIC (1/8 PACKAGE)



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{OZ}	3-state Output Off-State Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	±0.5	—	±5.0		±10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND $I_O = 0$		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	25	60	—	75		90	ns
		4.5		—	7	12	—	15		18	
		6.0		—	6	10	—	13		15	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	52	110	—	140		165	ns
		4.5		—	13	22	—	28		33	
		6.0		—	11	19	—	24		28	
t_{PLH} t_{PHL}	Propagation Delay Time**	2.0		—	48	100	—	125		150	ns
		4.5		—	12	20	—	25		30	
		6.0		—	10	17	—	21		26	
t_{PZL} t_{PHL}	Output Enable Time	2.0		—	40	100	—	125		150	ns
		4.5	$R_L = 1k\Omega$	—	10	20	—	25		30	
		6.0		—	9	17	—	21		26	
t_{PZL} t_{PZH}	Output Enable Time *	2.0		—	52	100	—	125	—	150	ns
		4.5	$R_L = 1k\Omega$	—	13	20	—	25	—	30	
		6.0		—	11	17	—	21	—	26	
t_{PZL} t_{PZH}	Output Disable Time	2.0		—	44	150	—	190		225	ns
		4.5	$R_L = 1k\Omega$	—	21	30	—	38		45	
		6.0		—	18	26	—	33		38	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{OUT}	Output Capacitane			—	10	—	—	—			pF
C_{PD} (1)	Power Dissipation Capacitance			—	40	—	—	—			pF

Note (1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

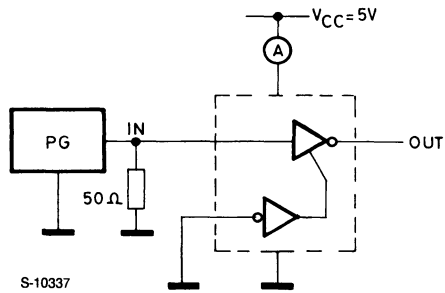
Average operating current can be obtained by the following equation $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Gate)

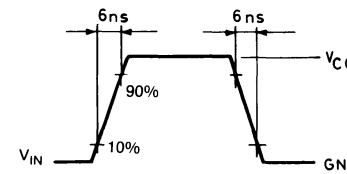
* for M54/74HC241 only

** for M54/74HC240 only

TEST CIRCUIT I_{CC} (Opr.)

HC240

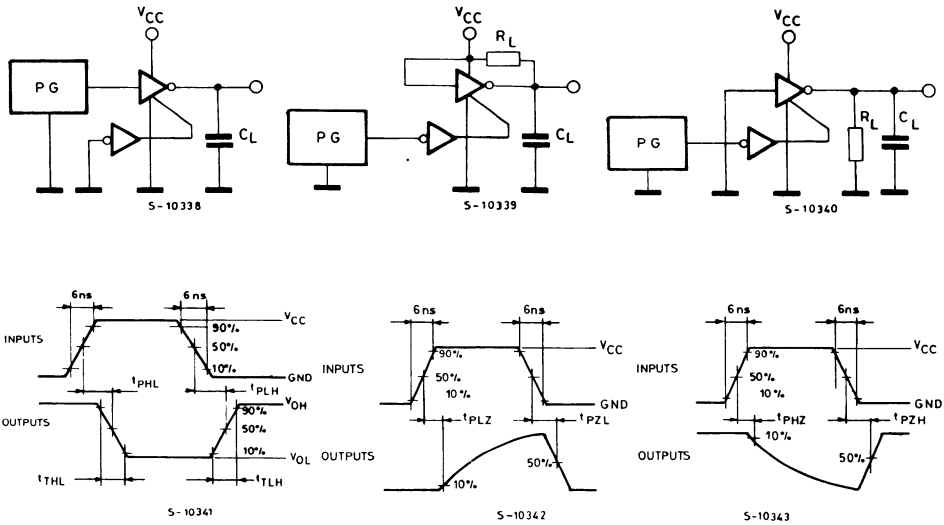




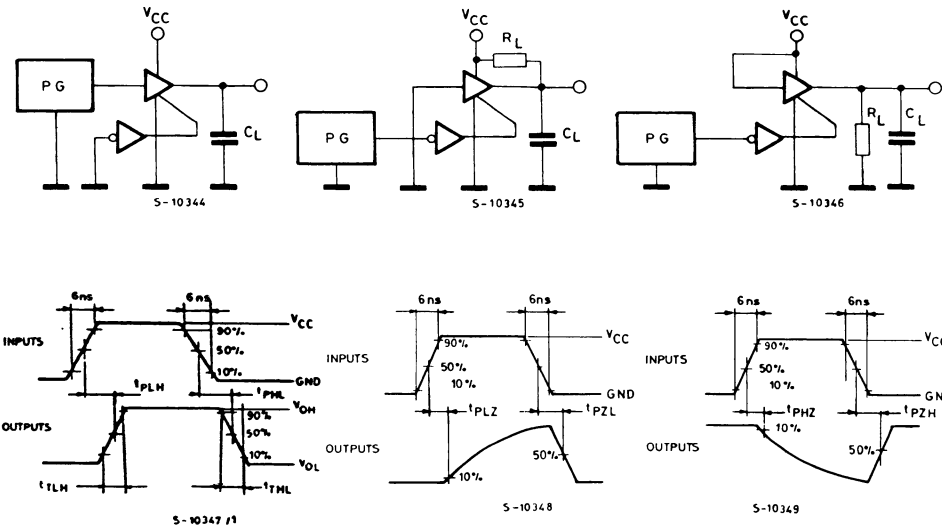
THE OTHER INPUTS ARE CONNECTED TO V_{CC} LINE OR GND LINE

SWITCHING CHARACTERISTICS TEST CIRCUIT

HC240

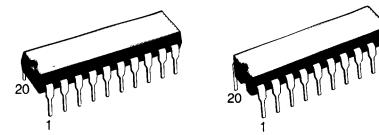


HC241/HC244



HCT240 OCTAL BUS BUFFER WITH INVERTED 3-STATE OUTPUTS
HCT241/4 OCTAL BUS BUFFER WITH NON-INVERTED 3-STATE OUTPUTS

- HIGH SPEED
  t_{PD} = 20 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.), V_{IL} = 0,8 V (MAX)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS240/241/244



B1N
Plastic Package

F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

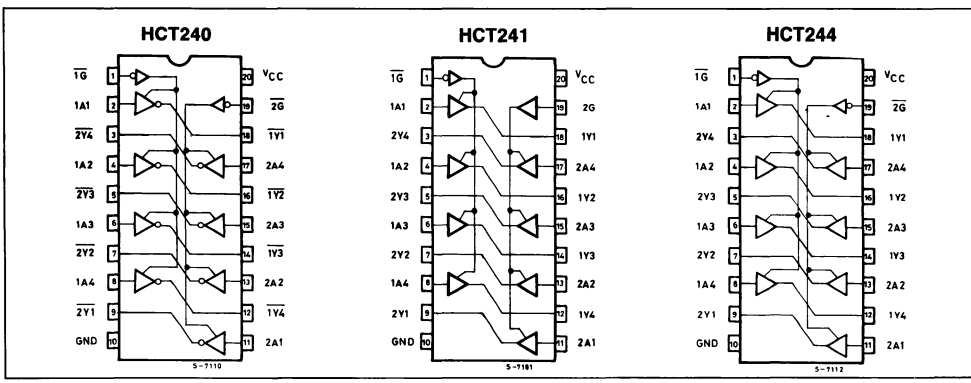
ORDERING NUMBERS:
M54HCTXXX F1
M74HCTXXX B1N
M74HCTXXX F1
M74HCTXXX C1
M74HCTXXX M1

DESCRIPTION

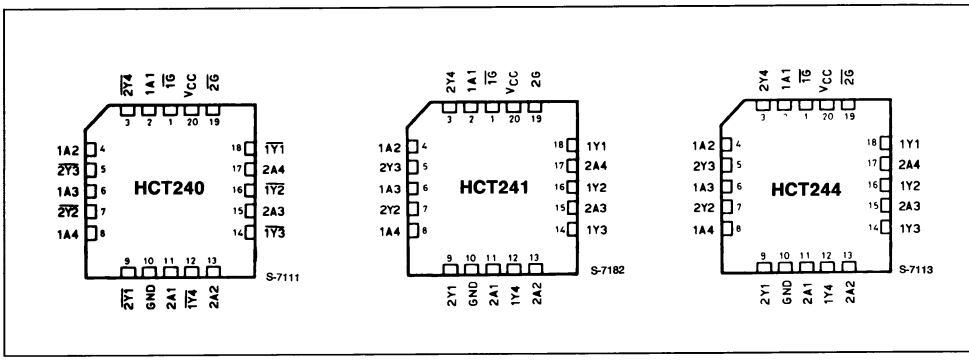
The HCT240, HCT241 and HCT244 are high speed CMOS OCTAL BUS BUFFER's fabricated with silicon C²MOS technology.
These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. Each control input governs four BUS BUFFERs.
These devices are designated to be used with 3-state memory address drivers, etc. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

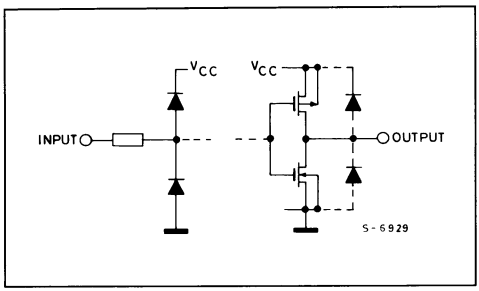
PIN CONNECTIONS (top view)



CHIP CARRIER



INPUT AND OUTPUT EQUIVALENT CIRCUIT



TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{G}$	G △	An	Yn	$\overline{Yn}$ △ △
L	H	L	L	H
L	H	H	H	L
H	L	X	Z	Z

△ : APPLIED ONLY FOR M54/74HCT241
△ △ : APPLIED ONLY FOR M54/74HCT240
X: DON'T CARE
Z: HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		4.5 to 5.5	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 − 55 to 125	°C
t_r, t_f	Input Rise and Fall Time		0 to 500	ns

DC SPECIFICATIONS

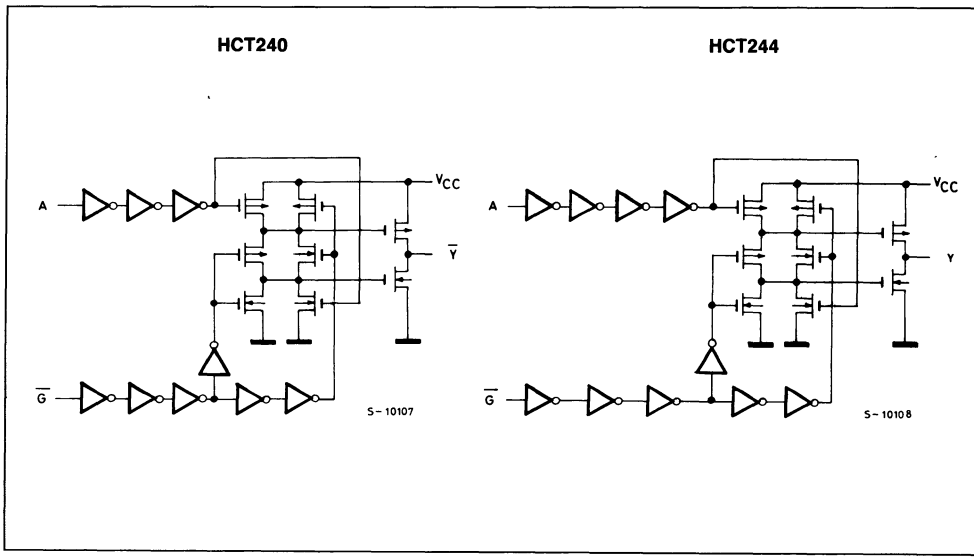
Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0	—	—	2.0	—	2.0	—	V
V_{IL}	Low Level Input Voltage	4.5 to 5.5			—	—	0.8	—	0.8	—	0.8	V
V_{OH}	High Level Output Voltage	4.5	V_{IN}	I_{OH}								
			V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	V
				−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
V_{OL}	Low Level Output Voltage	4.5	V_{IN}	I_{OL}								
			V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	
				6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
I_{OZ}	3-State Output Off-State Current	5.5	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		—	—	±0.5	—	±5.0	—	±10.0	
I_{IN}	Input Leakage Current	5.5	V_{IN} = V_{CC} or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}			V_I = V_{CC} or GND		—	—	4.0	—	40.0	—	80.0	
I_{CC}	Quiescent Supply Current	5.5	Per input: V_{IN} = 0.5V or 2.4V Other input: V_{CC} or GND		—	—	2.0	—	2.9	—	3.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

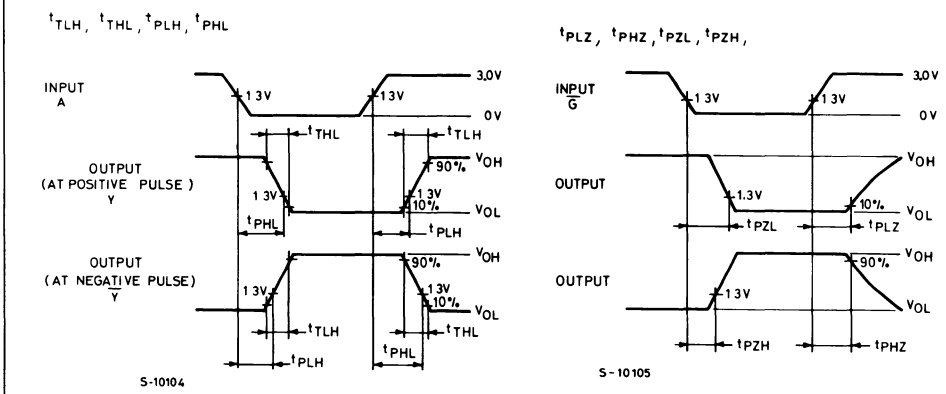
Symbol	Parameter	Test Condition		T_A = 25°C			−40 to 85°C		−55 to 125°C		Unit
			V_{CC}	Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4.5	—	8	12	—	15	—	19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (HCT240)		4.5	—	22	35	—	42	—	53	ns
t_{PLH} t_{PHL}	Propagation Delay Time (HCT241, HCT244)		4.5	—	23	36	—	44	—	54	ns
t_{PZL} t_{PZH}	Output Enable Time	R_L = 1kΩ	4.5	—	23	35	—	43	—	53	ns
t_{PLZ} t_{PHZ}	Output Disable Time	R_L = 1kΩ	4.5	—	30	47	—	57	—	71	ns
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{OUT}	Output Capacitance			—	10	—	—	—	—	—	pF
C_{PD}(1)	Power Dissipation Capacitance	HCT240		—	42	—	—	—	—	—	pF
		HCT241		—	49	—	—	—	—	—	
		HCT244		—	46	—	—	—	——	—	

Note (1) C_{PD} is defined as the value of IC's of internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following equation.
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Gate).

CIRCUIT DIAGRAM

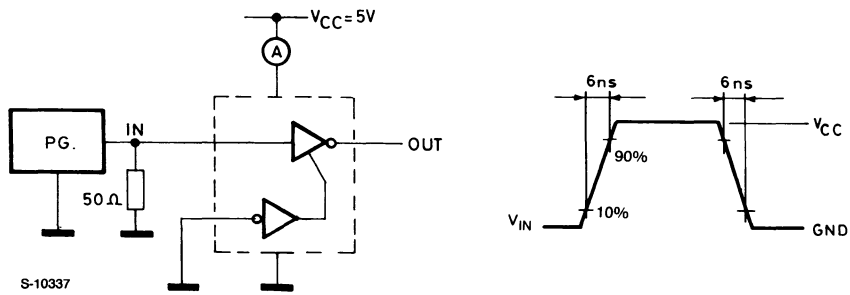


SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)

HCT240



THE OTHER INPUTS ARE CONNECTED TO V_{CC} LINE OR GND LINE.

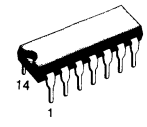
SGS-THOMSON MICROELECTRONICS

M54HC242/243
M74HC242/243

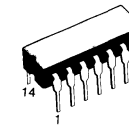
QUAD BUS TRANSCEIVER (3-STATE)

PRELIMINARY DATA

- HIGH SPEED
  t_{PD} = 10 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN).
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN).
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS242/243



B1N
Plastic Package



F1
Ceramic Frit Seal Package

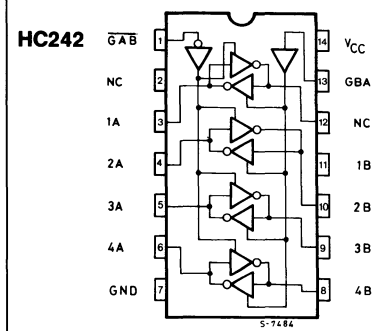
M1
Micro Package

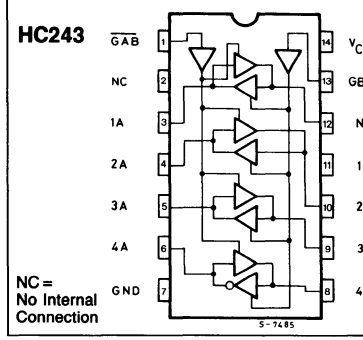
C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX C1
M74HCXXX M1

PIN CONNECTIONS (top view)





NC = No Internal Connection

DESCRIPTION

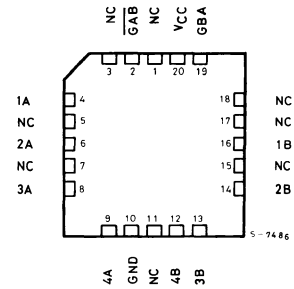
The M54/74HC242 and the M54/74HC243 are high speed CMOS QUAD BUS TRANSCEIVER (3-STATE) fabricated in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

The M54/74HC242,243 are 3-STATE bi-directional inverting and non-inverting buffers and are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation when driving large bus capacitances.

Each device has one active high enable (GBA), and one active low enable ($\overline{GAB}$). GBA enables the A outputs and $\overline{GAB}$ enables the B outputs.

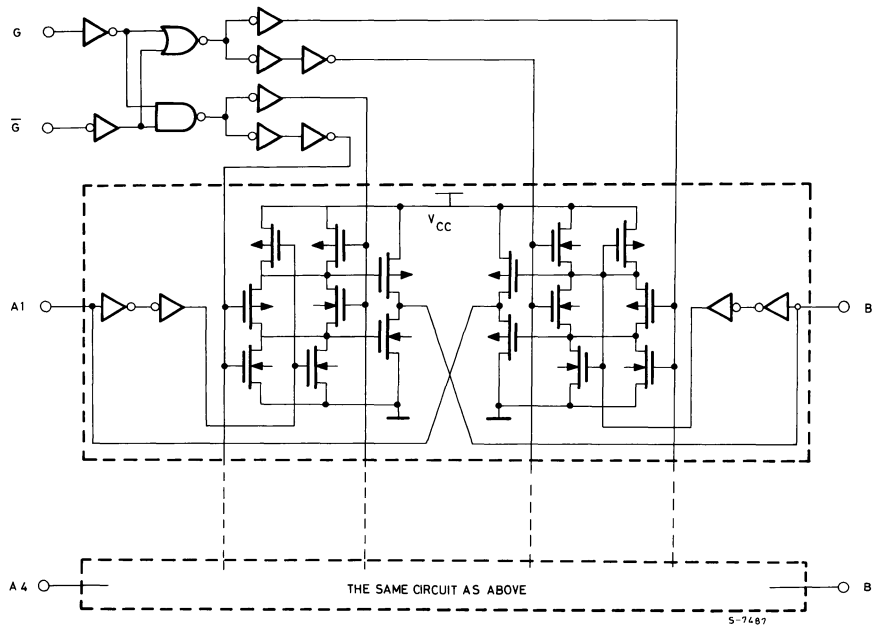
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM



TRUTH TABLE

INPUTS		FUNCTION		OUTPUTS	
$\overline{GAB}$	GAB	A BUS	B BUS	HC242	HC243
H	H	OUTPUT	INPUT	$A=\overline{B}$	A=B
L	L	INPUT	OUTPUT	$B=\overline{A}$	B=A
H	L	HIGH IMPEDANCE		Z	Z
L	H	HIGH IMPEDANCE		Z	Z

Z= HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			-40 to $85°C$ 74HC		-55 to $125°C$ 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	$-20\ \mu A$	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		-6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		-7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	$20\ \mu A$	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	± 0.1	—	± 1.0	—	± 1.0	μA
I_{OZ}	3-State Output Off-State current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	± 0.5	—	± 5.0	—	± 10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$pF, Input $t_r = t_f = 6$ns)

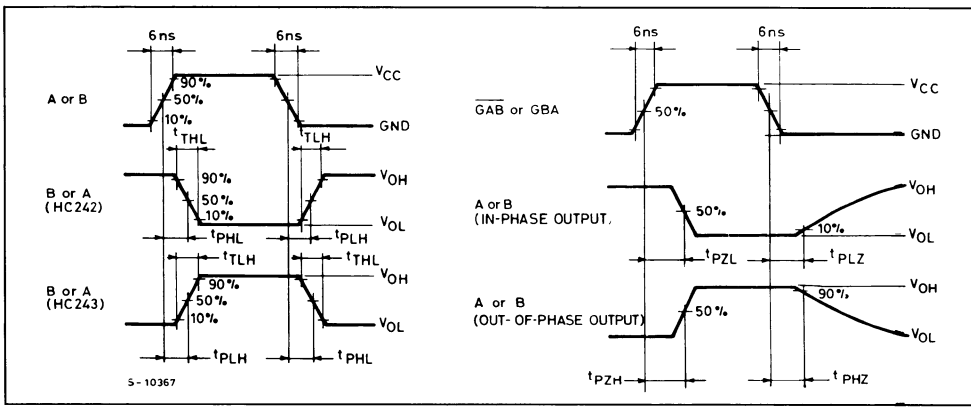
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			-40 to $85°C$ 74HC		-55 to $125°C$ 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time Output	2.0		—	25	60	—	75	—	90	ns
		4.5		—	7	12	—	15	—	18	
		6.0		—	6	10	—	13	—	15	
t_{PLH} t_{PHL}	Propagation Delay Time (HC242)	2.0		—	48	100	—	125	—	150	ns
		4.5		—	12	20	—	25	—	30	
		6.0		—	10	17	—	21	—	26	
t_{PLH} t_{PHL}	Propagation Delay Time (HC243)	2.0		—	44	90	—	115		135	ns
		4.5		—	11	18	—	23	—	27	
		6.0		—	9	15	—	20	—	23	
t_{PZH} t_{PZL}	3-State Output Enable Time	2.0	$R_L = 1k\Omega$	—	72	145	—	180	—	220	ns
		4.5		—	18	29	—	36	—	44	
		6.0		—	15	25	—	31	—	38	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

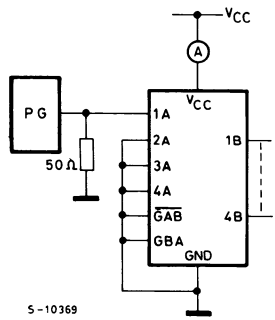
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PHZ} t_{PLZ}	3-State Output Disable Time	2.0	$R_L = 1k\Omega$	—	84	150	—	190	—	225	ns
		4.5		—	21	30	—	38	—	45	
		6.0		—	18	26	—	33	—	38	
C_{IN}	Input Capacitance		$\overline{GAB}$, GBA	—	5	10	—	10	—	10	pF
$C_{I/O}$	Bus Terminal Input Capacitance		An, Bn	—	13	—	—	—	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance		M54/74HC242	—	42	—	—	—	—	—	pF
			M54/74HC243	—	36	—	—	—	—	—	

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current is: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per circuit)

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

C_{PD} CALCULATION

C_{PD} is to be calculated with the following formula by using the measured value of I_{CC} (Opr.) in the test circuit opposite

$$C_{PD} = \frac{I_{CC}\ (Opr.)}{f_{IN} \cdot V_{CC}}$$

In determining the typical value of C_{PD}, a relatively high frequency of 1MHz was applied to f_{IN}, in order to eliminate any error caused by the quiescent supply current

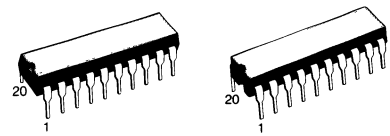
SGS-THOMSON MICROELECTRONICS

M54HC245/640/643
M74HC245/640/643

OCTAL BUS TRANSCEIVER (3-STATE) HC245 NON INVERTING, HC640 INVERTING, HC643 INVERTING/NON INVERTING

PRELIMINARY DATA

- HIGH SPEED
  t_{PD} = 11 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN).
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS245/640/643



B1N
Plastic Package

F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX C1
M74HCXXX M1

DESCRIPTION

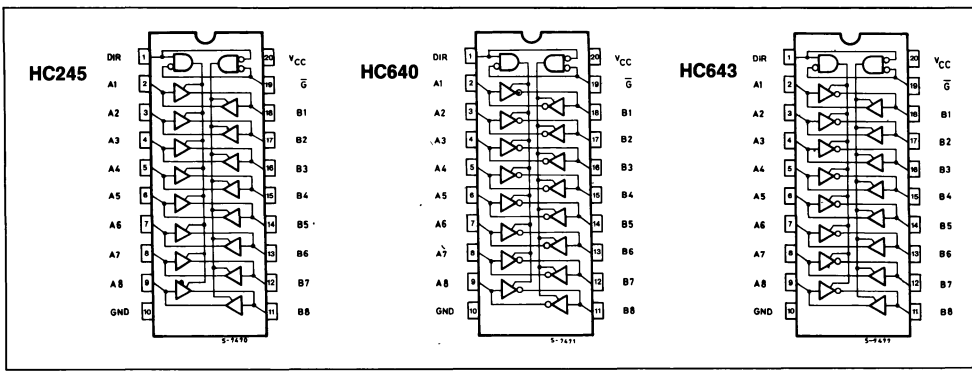
The M54/74HC245, M54HC640 and M54HC643 utilise silicon gate C²MOS technology to achieve operating speed equivalent to LSTTL devices. Along with the low power dissipation and high noise immunity of standard C²MOS integrated circuit, it posseses the driving capability of 15 LSTTL loads. These IC's are intended for two-way asynchronous communication between data buses, and the direction of data transmission is determined by DIR input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

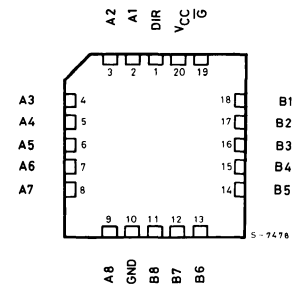
NOTICE FOR APPLICATION

IT IS PROHIBITED TO APPLY A SIGNAL TO A BUS TERMINAL WHEN IT IS IN OUTPUT MODE. AND WHEN A BUS TERMINAL IS FLOATING (HIGH IMPEDANCE STATE), IT IS REQUESTED TO FIX THE INPUT LEVEL BY MEANS OF EXTERNAL PULL DOWN OR PULL UP RESISTOR.

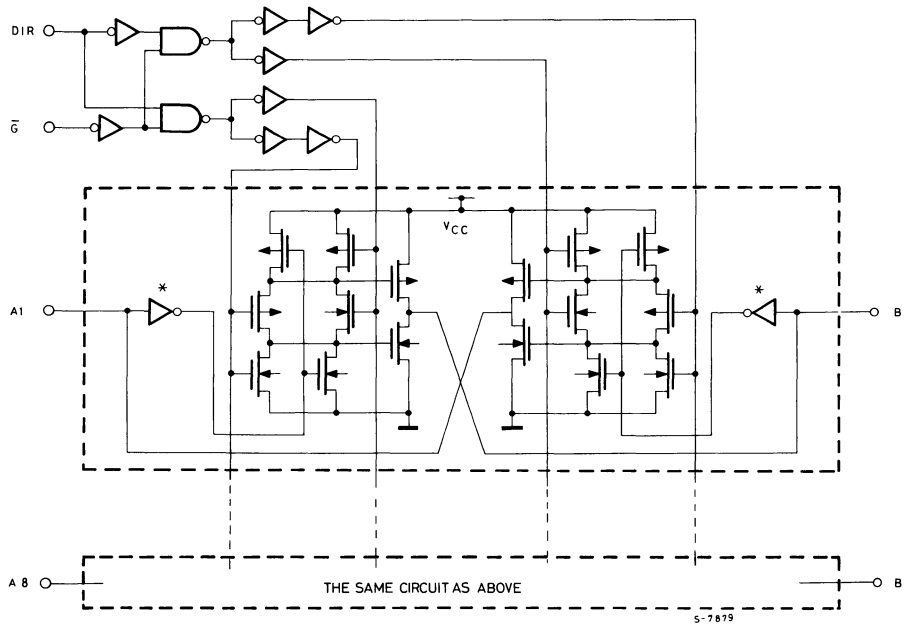
PIN CONNECTION (top view)



CHIP CARRIER



LOGIC DIAGRAM (HC640)



NOTE: IN CASE OF HC245 OR HC643, INPUT INVERTERS MARKED* AT A BUS AND B BUS OR AT B BUS ARE ELIMINATED RESPECTIVELY

TRUTH TABLE

INPUT		FUNCTION		OUTPUT		
$\overline{G}$	DIR	A BUS	B BUS	HC245	HC640	HC643
L	L	OUTPUT	INPUT	A = B	A = $\overline{B}$	A = B
L	H	INPUT	OUTPUT	B = A	B = $\overline{A}$	B = $\overline{A}$
H	X	Z	Z	Z	Z	Z

X: "H" or "L" Z: HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current*	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{OZ}	3-State Output Off-State Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND $I_O = 0$		—	—	4	—	40	—	80	μA

* Applicable only to DIR, G, $\overline{G}$ input

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

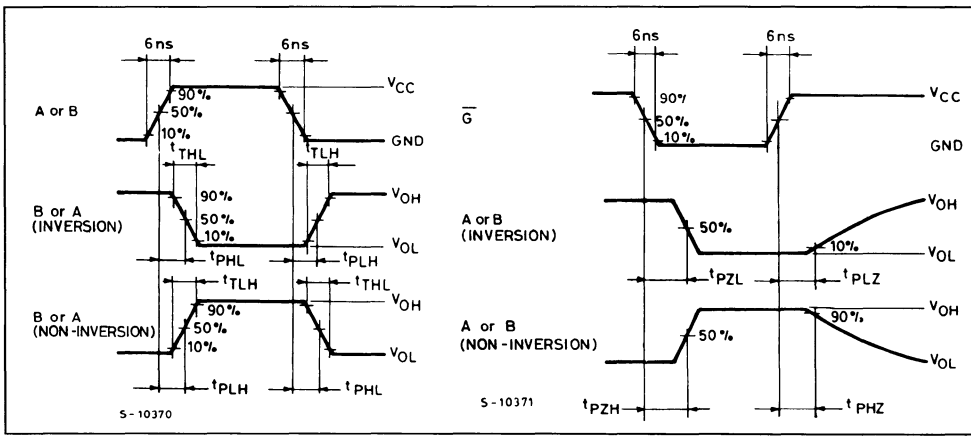
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transitio Time	2.0		—	25	60	—	75	—	90	ns
		4.5		—	7	12	—	15	—	18	
		6.0		—	6	10	—	13	—	15	
t_{PLH} t_{PHL}	Propagation Delay Time (for HC245)	2.0		—	48	90	—	115	—	135	ns
		4.5		—	12	18	—	23	—	27	
		6.0		—	10	15	—	20	—	23	
t_{PLH} t_{PHL}	Propagation Delay Time (for HC640/643)	2.0		—	52	110	—	140	—	165	ns
		4.5		—	13	22	—	28	—	33	
		6.0		—	11	19	—	24	—	28	
t_{PZL} t_{PZH}	3 State Output Enable Time	2.0	$R_L = 1k\Omega$	—	80	160	—	200	—	240	ns
		4.5		—	20	32	—	40	—	48	
		6.0		—	17	27	—	34	—	41	
t_{PLZ} t_{PHZ}	3 State Output Disable Time	2.0	$R_L = 1k\Omega$	—	80	190	—	240	—	285	ns
		4.5		—	25	38	—	48	—	57	
		6.0		—	21	32	—	41	—	48	

AC ELECTRICAL CHARACTERISTICS (Continued)

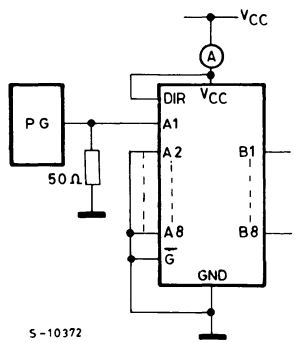
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance		DIR, G, $\overline{G}$	—	5	10	—	10	—	10	pF
$C_{I/O}$	Bus Input Capacitance		A_n, B_n	—	13	—	—	—	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance		HC245	—	33	—	—	—	—	—	pF
			HC640/643	—	40	—	—	—	—	—	

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current is: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Circuit).

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

C_{PD} CALCULATION

C_{PD} is to be calculated with the following formula by using the measured value of I_{CC} (Opr.) in the test circuit opposite.

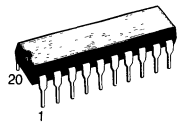
$$C_{PD} = \frac{I_{CC}\ (Opr.)}{f_{IN} \cdot V_{CC}}$$

SGS-THOMSON MICROELECTRONICS

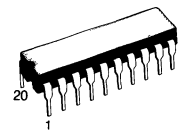
M54HCT245/640/643
M74HCT245/640/643

OCTAL BUS TRANSCEIVER (3-STATE)
HCT245 NON INVERTING, HCT640 INVERTING, HCT643 INVERTING/NON INVERTING

- LOW POWER DISSIPATION
  $I_{CC} = 4\mu A$ (MAX.) at $T_A = 25°C$
- COMPATIBLE WITH TTL OUTPUTS
  $V_{IH} = 2V$ (MIN) $V_{IL} = 0.8V$ (MAX)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ $I_{OL} = 6mA$ (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS245/640/643



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HCTXXX F1
M74HCTXXX B1N
M74HCTXXX F1
M74HCTXXX C1
M74HCTXXX M1

DESCRIPTION

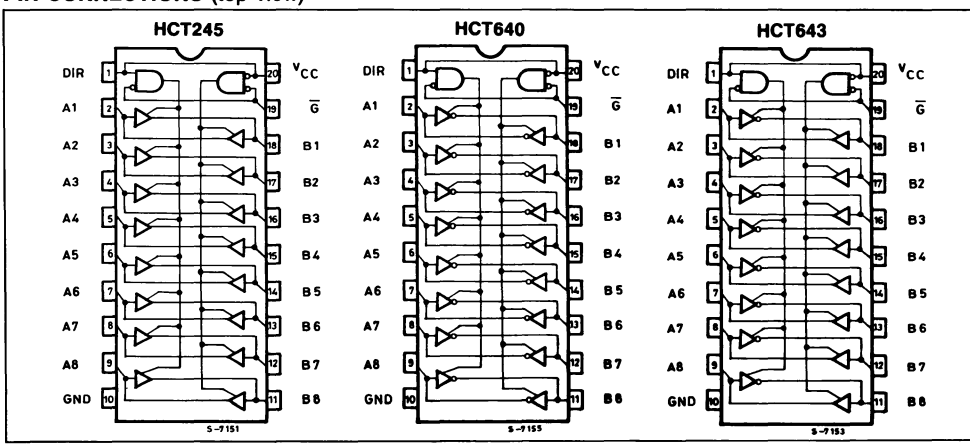
The HCT245, HCT640, and HCT643 utilize silicon gate C²MOS technology to achieve operating speeds equivalent to LSTTL parts.
Along with the low power dissipation and high noise immunity of standard C²MOS integrated circuit, it possesses the capability to drive of 15 LSTTL loads. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
These IC's are intended for two-way asynchronous communication between data buses, and the direction of data transmission is determined by the DIR input.

The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

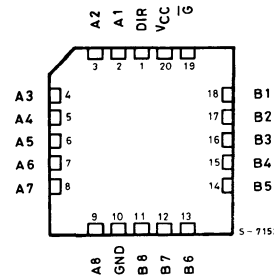
NOTICE FOR APPLICATION

IT IS NOT POSSIBLE TO APPLY A SIGNAL TO A BUS TERMINAL WHEN IT IS IN THE OUTPUT MODE. PULL UP OR PULL DOWN RESISTOR SHOULD BE USED ON HIGH IMPEDANCE (3-STATE) FLOATING BUS TERMINAL

PIN CONNECTIONS (top view)

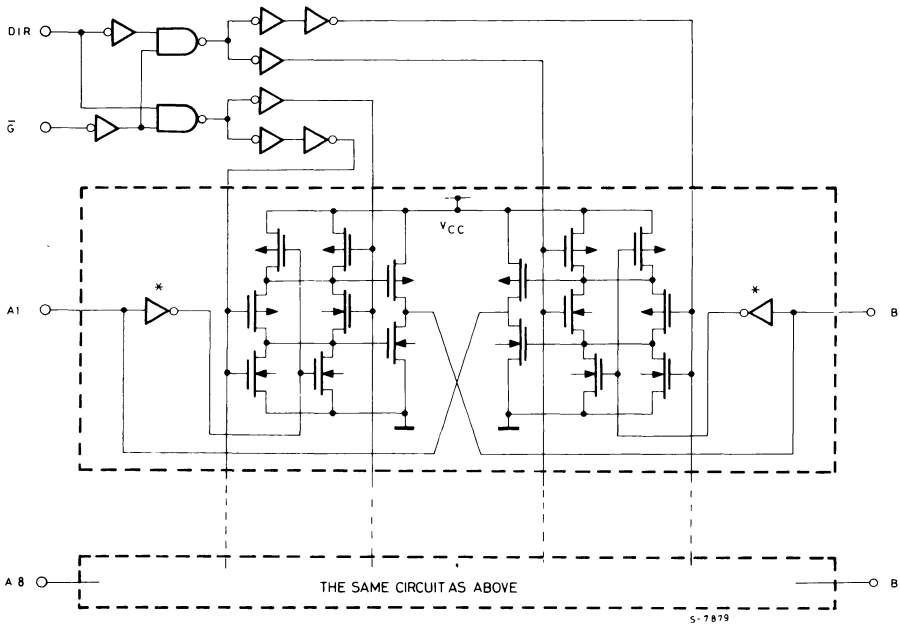


CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM (HCT 640)



NOTE: IN CASE OF HCT245 OR HCT643, INPUT INVERTERS MARKED * AT A BUS OR AT B BUS ARE ELIMINATED RESPECTIVELY.

INPUT		FUNCTION		OUTPUT		
$\overline{G}$	DIR	A BUS	B BUS	HCT245	HCT640	HCT643
L	L	OUTPUT	INPUT	A = B	A = B	A = B
L	H	INPUT	OUTPUT	B = A	B = A	B = A
H	X	Z	Z	Z	Z	Z

X: DON'T CARE
Z: HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		4.5 to 5.5	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time		0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 6.0			2.0	—	—	2.0	—	2.0	—	V
V_{IL}	Low Level Input Voltage	4.5 to 5.5			—	—	0.8	—	0.8	—	0.8	V
V_{OH}	High Level Output Voltage	4.5	V_{IN}	I_{OH}								
			V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	V
				−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
V_{OL}	Low Level Output Voltage	4.5	V_{IN}	I_{OL}								
			V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
				6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
I_{OZ}	3-State Output Off-State Current	5.5	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±10.0	
I_{IN}	Input Leakage Current	5.5	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	5.5	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA
I_{CC}			Per input: $V_{IN} = 0.5V$ or 2.4V Other input: V_{CC} or GND		—	—	2.0	—	2.9	—	3.0	mA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5		—	8	12	—	15	—	18	ns
t_{PLH} t_{PHL}	Propagation Delay Time	4.5		—	19	28	—	35	—	42	ns
t_{PZL} t_{PZH}	3-State Output Enable Time	4.5	$R_L = 1k\Omega$	—	27	42	—	53	—	63	ns
t_{PLZ} t_{PHZ}	3-State Output Disable Time	4.5	$R_L = 1k\Omega$	—	27	40	—	50	—	60	ns

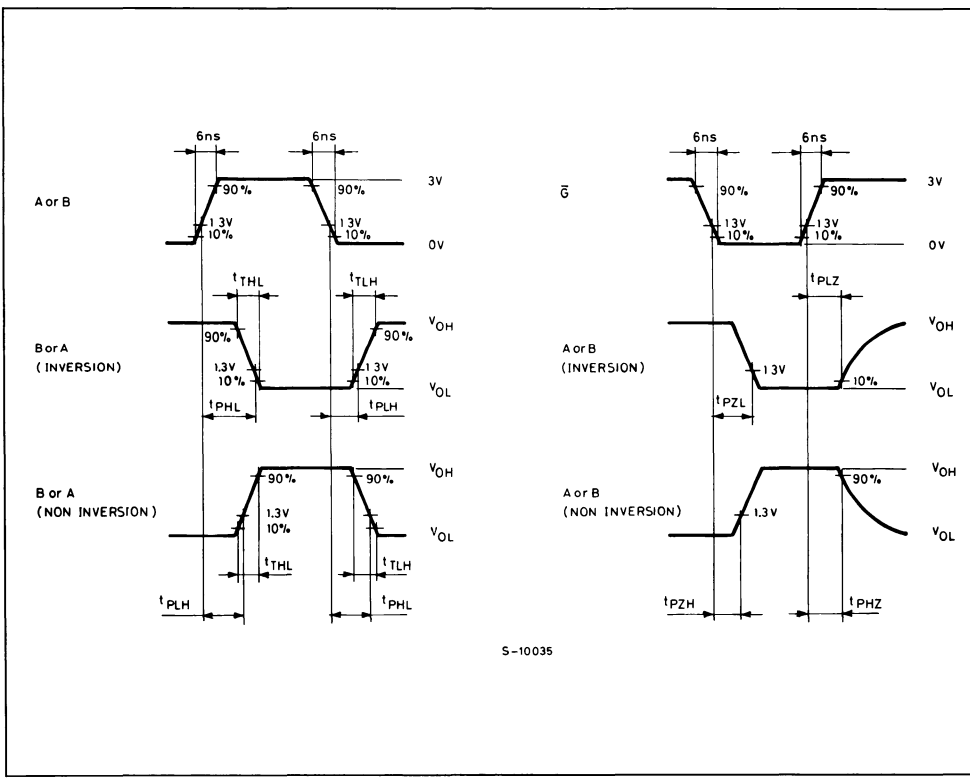
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance		DIR, G, $\overline{G}$,	—	5	10	—	10	—	10	pF
$C_{I/O}$	Bus Inp. Capacit.		An, Bn	—	13	—	—	—	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance		M54/74HCT245	—	46	—	—	—	—	—	pF
			M54/74HCT640/643	—	44	—	—	—	—	—	

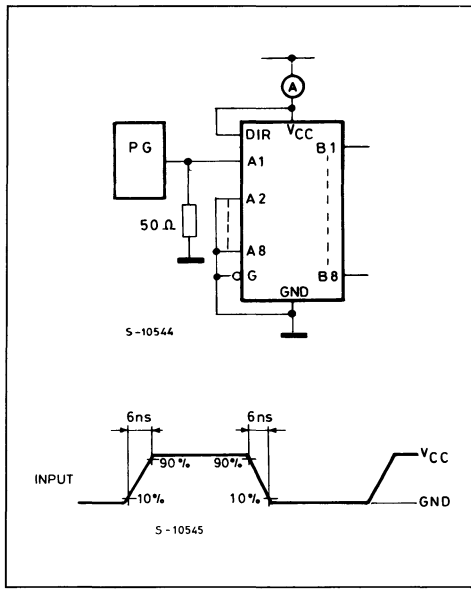
Note (*) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test circuit).

Average operating current can be obtained by the following equation:
$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Gate)

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT



C_{PD} CALCULATION

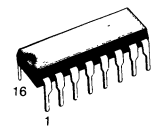
C_{PD} is to be calculated with the following formula by using the measured value of I_{CC} (Opr.) in the test circuit opposite

$$C_{PD} = \frac{I_{CC}\ (Opr.)}{f_{IN} \cdot V_{CC}}$$

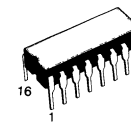
In determining the typical value of C_{PD}, a relatively high frequency of 1MHz was applied to f_{IN}, in order to eliminate any error caused by the quiescent supply current

8-CHANNEL MULTIPLEXER (3-STATE)

- HIGH SPEED
  t_{PD} = 18 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C 6V
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN).
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS251



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC251 F1
M74HC251 B1N
M74HC251 F1
M74HC251 C1
M74HC251 M1

DESCRIPTION

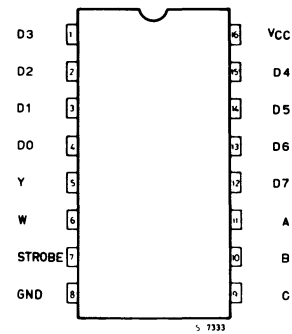
The M54/74HC251 is a high speed CMOS 8-CHANNEL MULTIPLEXER (3-STATE) fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This multiplexer features both true (Y) and complement (W) outputs as well as a STROBE input. The STROBE must be at a low logic level to enable this device. When the STROBE input is high, both outputs are in the high impedance state. When enabled, address information on the data select inputs determines which data input is routed to Y and W. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

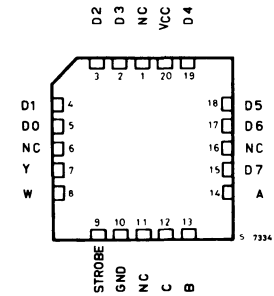
TRUTH TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

Z: HIGH IMPEDANCE X: DON'T CARE

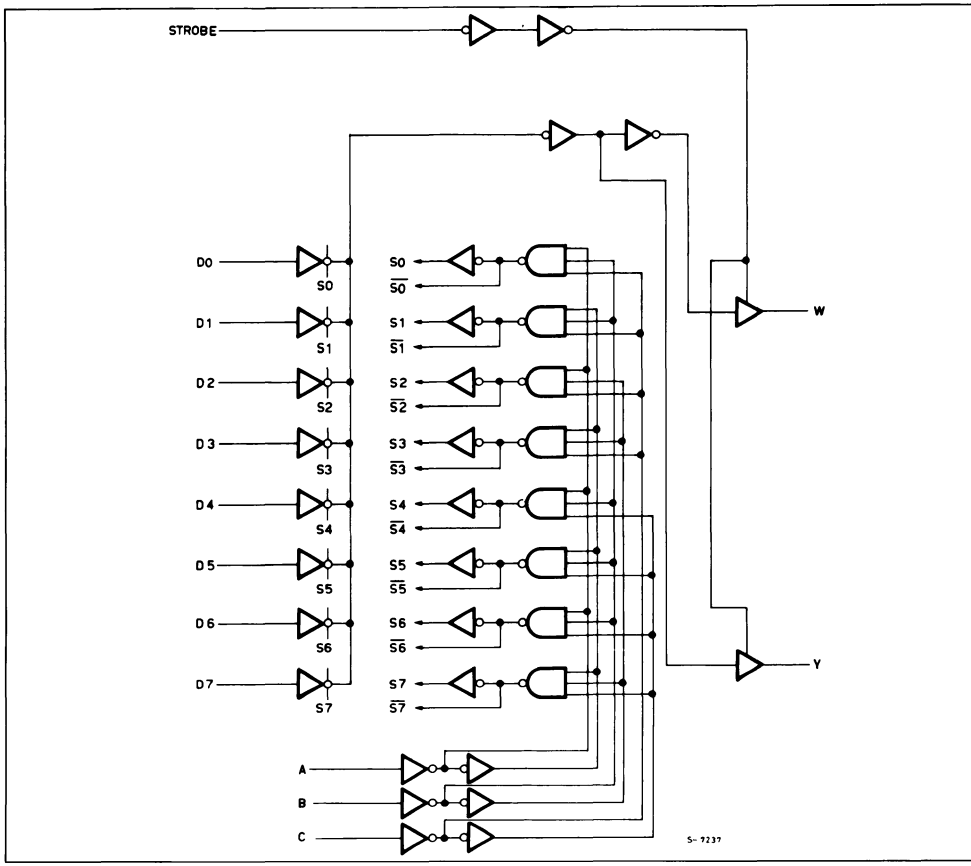
PIN CONNECTIONS (top view)





NC = No Internal Connection

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V: 0 to 1000 V_{CC} = 4.5V: 0 to 500 V_{CC} = 6 V: 0 to 400	ns

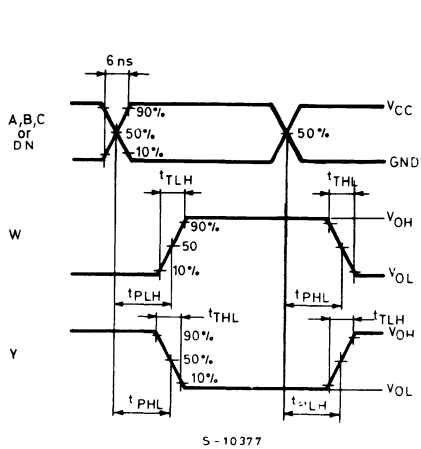
DC SPECIFICATIONS

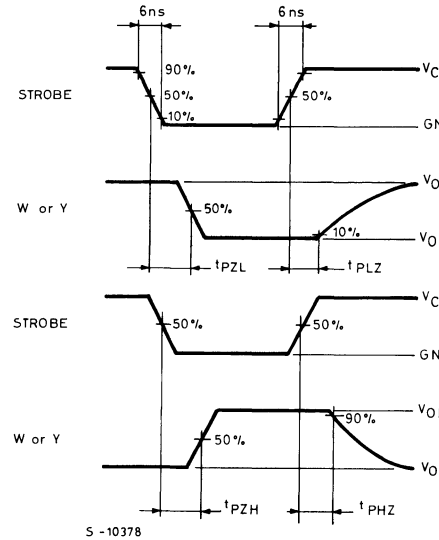
Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{OZ}	3-State Output Off-State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND		—	—	±0.5	—	±5.0	—	±10	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND I_O = 0		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	C_L (pF)	54HC and 74HC			Unit
			Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time	15		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (D - W)	15		18	29	ns
t_{PLH} t_{PHL}	Propagation Delay Time (D - Y)	15		17	27	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C - W)	15		22	35	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C - Y)	15		21	33	ns
t_{PZH} t_{PZL}	3-State Output Enable Time	15		11	18	ns
t_{PHZ} t_{PLZ}	3-State Output Disable Time	5		9	15	ns

SWITCHING CHARACTERISTICS TEST WAVEFORM



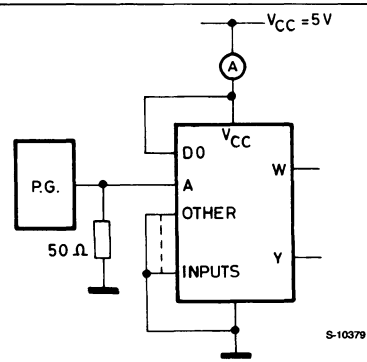


AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (D - W)	2.0		—	76	165	—	205		250	ns
		4.5		—	19	33	—	41		50	
		6.0		—	16	28	—	35		43	
t_{PLH} t_{PHL}	Propagation Delay Time (D - Y)	2.0		—	76	160	—	200		240	ns
		4.5		—	19	32	—	40		48	
		6.0		—	16	27	—	34		41	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C - W)	2.0		—	96	205	—	255		310	ns
		4.5		—	24	41	—	51		62	
		6.0		—	20	35	—	43		53	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C, - Y)	2.0		—	96	195	—	245		295	ns
		4.5		—	24	39	—	49		59	
		6.0		—	20	34	—	42		50	
t_{PZL} t_{PZH}	3 State Output Enable Time	2.0		—	52	105	—	130		160	ns
		4.5		—	13	21	—	26		32	
		6.0		—	11	18	—	22		27	
t_{PLZ} t_{PHZ}	3 State Output Disable Time	2.0		—	60	105	—	130		160	ns
		4.5		—	15	21	—	26		32	
		6.0		—	13	18	—	22		27	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{OUT}	Output Capacitance			—	10	—	—	—	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance			—	100	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to test Circuit)
Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

TEST WAVEFORM I_{CC} (Opr.)



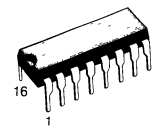
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

SGS-THOMSON MICROELECTRONICS

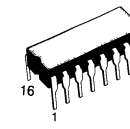
M54HC257/258
M74HC257/258

HC257 QUAD 2-CHANNEL MULTIPLEXER (3-STATE)
HC258 QUAD 2-CHANNEL MULTIPLEXER (3-STATE, INVERTING)

- HIGH SPEED
  t_{PD} = 12 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN).
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS257/258



B1N
Plastic Package



F1
Ceramic Frit Seal Package

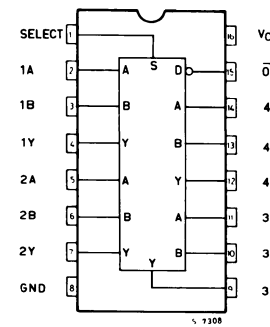
M1
Micro Package

C1
Plastic Chip Carrier

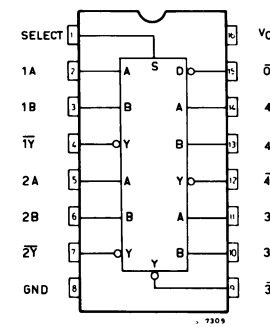
ORDERING NUMBERS:
M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX C1
M74HCXXX M1

PIN CONNECTIONS (top view)

HC257



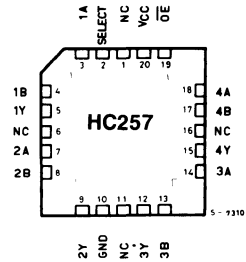
HC258

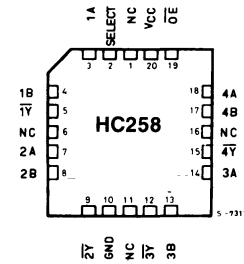


DESCRIPTION

The M54/74HC257 and the M54/74HC258 are high speed CMOS MULTIPLEXERs fabricated with silicon gate C²MOS technology.
They have the same high speed performance of LSTTL combined with true CMOS low power consumption.
These IC's are composed of an independent 2-channel multiplexer with common SELECT and ENABLE INPUT.
The M54/74HC258 is an inverting multiplexer while the M54/74HC257 is a non-inverting multiplexer. When the ENABLE INPUT is held "High", outputs of both IC's become high-impedance state. If SELECT INPUT is held "Low", "A" data is selected, when SELECT INPUT is high "H", "B" data is chosen.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

CHIP CARRIER

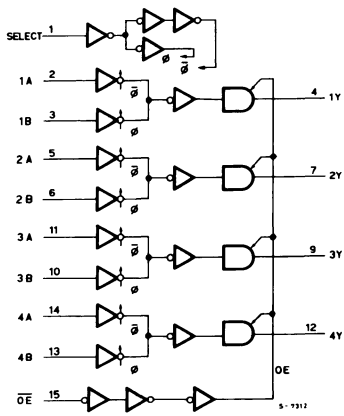




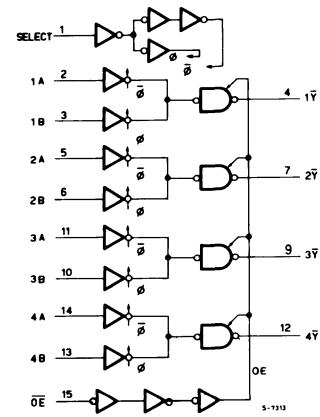
NC = No Internal Connection

LOGIC DIAGRAM

HC257



HC258



TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{OE}$	SELECT	A	B	Y (257)	$\overline{Y}$ (258)
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

X: DON'T CARE Z: HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400		ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
			V_I	I_O	Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_{IH} or V_{IL}	−20 μA	1.9	2.0	—	1.9	—	1.9	—	V
		4.5			4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	

DC SPECIFICATIONS (Continued)

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{OZ}	3-State Output Off-State Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	±0.5	—	±5	—	±10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

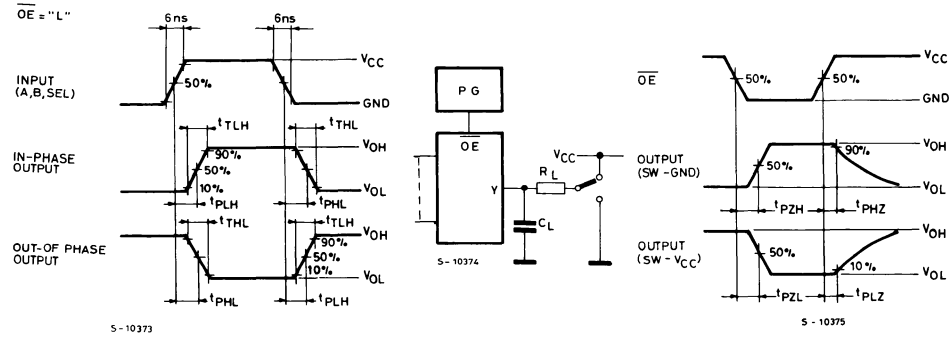
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	23	60	—	75	—	90	ns
		4.5		—	7	12	—	15	—	18	
		6.0		—	6	10	—	13	—	15	
t_{PLH} t_{PHL}	Propagation Delay Time HC257 A,B - Y	2.0		—	50	100	—	125	—	150	ns
		4.5		—	15	20	—	25	—	30	
		6.0		—	13	17	—	21	—	26	
t_{PLH} t_{PHL}	Propagation Delay Time HC257 (SELECT - Y)	2.0		—	80	160	—	200	—	240	ns
		4.5		—	22	32	—	40	—	48	
		6.0		—	19	17	—	34	—	41	
t_{PLH} t_{PHL}	Propagation Delay Time HC258 (A,B - Y)	2.0		—	50	100	—	125	—	150	ns
		4.5		—	15	20	—	25	—	30	
		6.0		—	13	27	—	21	—	26	
t_{PLH} t_{PHL}	Propagation Delay Time HC258 SELECT - $\overline{Y}$	2.0		—	80	160	—	200	—	240	ns
		4.5		—	22	32	—	40	—	48	
		6.0		—	19	27	—	34	—	41	
t_{PZL} t_{PZH}	Output Enable Time	2.0		—	60	110	—	140	—	165	ns
		4.5	$R_L = 1k\Omega$	—	15	22	—	28	—	33	
		6.0		—	13	19	—	24	—	28	

AC ELECTRICAL CHARACTERISTICS (Continued)

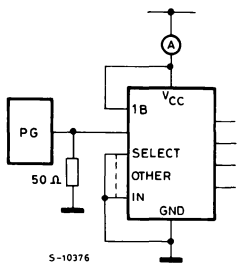
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0 4.5 6.0	$R_L = 1k\Omega$	— — —	44 21 20	140 28 24	— — —	175 35 30		210 42 36	ns
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{OUT}	Output Capacitance			—	60	—	—	—			pF
C_{PD} (*)	Power Dissipation Capacitance		M54/74HC257	—	60	—	—	—			pF
			M54/74HC258	—	59	—	—	—			

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Channel)

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

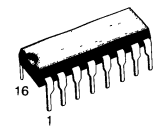
C_{PD} CALCULATION

C_{PD} is to be calculated with the following formula by using the measured value of I_{CC} (Opr.) in the test circuit opposite.

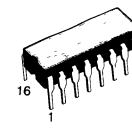
$$C_{PD} = \frac{I_{CC}\ (opr)}{f_{IN} \cdot V_{CC}}$$

8 BIT ADDRESSABLE LATCH

- HIGH SPEED
  t_{PD} = 13 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS259



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC259 F1
M74HC259 B1N
M74HC259 F1
M74HC259 C1
M74HC259 M1

DESCRIPTION

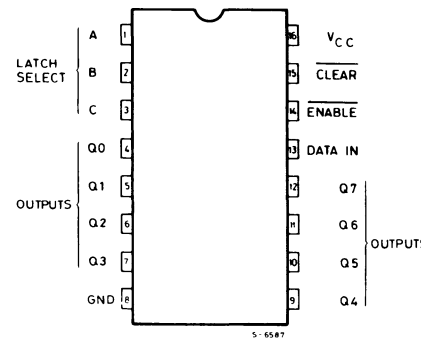
The M54/74HC259 is a high speed CMOS 8 BIT ADDRESSABLE LATCH fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

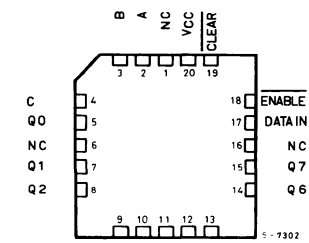
The M54HC259/M74HC259 has single data input (D) 8 latch outupts (Q0-Q7), 3 address inputs (A, B, and C), common enable input (E), and a common CLEAR input. To operate this device as an addressable latch, data is held on the D input, and the address of the latch into which the data is to be entered is held on the A, B, and C inputs. When ENABLE is taken low the data flows through to the addresses output. The data is stored on the positive-going edge of the ENABLE pulse. All unaddressed latches will remain unaffected. With ENABLE in the high state the device is deselected and all latches remain in their previous state, unaffected by changes on the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the ENABLE should be held high (inactive) while the address lines are changing.

If ENABLE is held high and CLEAR is taken low all eight latches are cleared to the low state. If ENABLE is low all latches except the addressed latch will be cleared. The addressed latch will instead follow the D input, effectively implementing a 3-to 8 line decoder.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)





NC = No Internal Connection

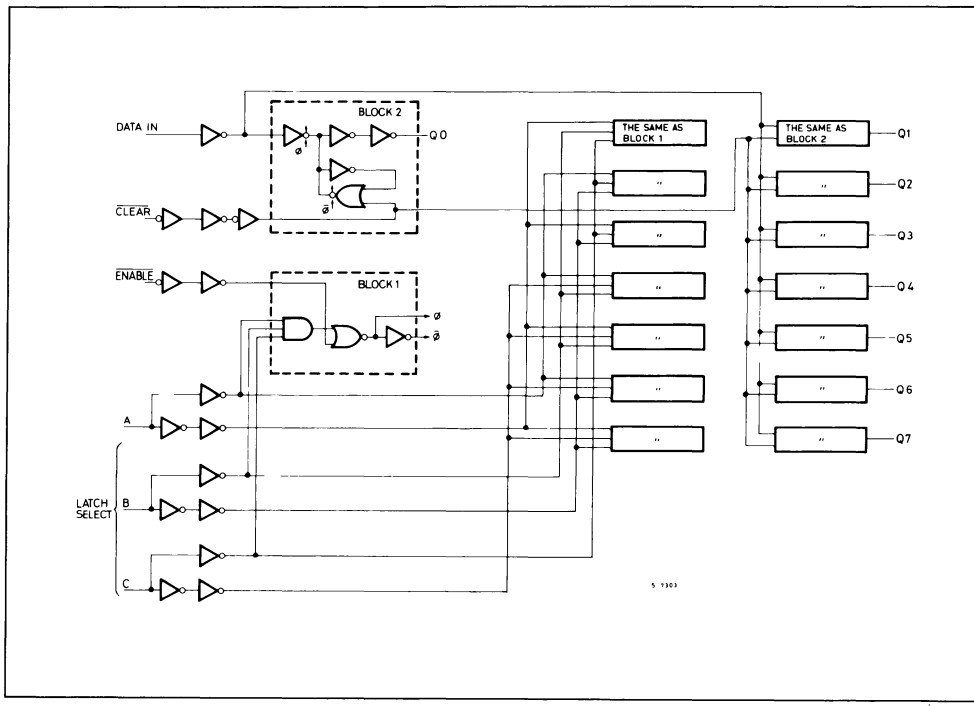
TRUTH TABLE

INPUTS		OUTPUTS OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
$\overline{CLEAR}$	$\overline{G}$			
H	L	D	Qi0	ADDRESSABLE LATCH
H	H	Qi0	Qi0	MEMORY
L	L	D	L	8-LINE DEMULTIPLEXER
L	H	L	L	CLEAR ALL BITS TO 'L'

SELECT INPUTS			LATCH ADDRESSED
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

D: THE LEVEL AT THE DATA INPUT
Qi0: THE LEVEL BEFORE THE INDICATED STEADY-STATE INPUT CONDITIONS WERE ESTABLISHED, (i = 0,1,.....,7).

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

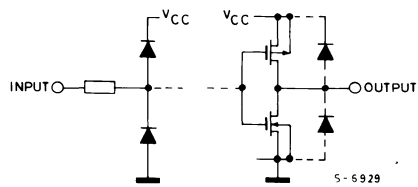
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400		ns

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			-40 to $85°C$ 74HC		-55 to $125°C$ 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	$-20\ \mu A$	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		-4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		-5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	$20\ \mu A$	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	± 0.1	—	± 1.0	—	± 1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - QN)		13	21	ns
t_{PLH} t_{PHL}	Propagation Delay Time (ADD - QN)		21	33	ns
t_{PLH} t_{PHL}	Propagation Delay Time (EN - QN)		18	29	ns
t_{PHL}	Propagation Delay Time (CL - QN)		14	23	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	22	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - QN)	2.0		—	73	130	—	165		195	ns
		4.5		—	16	26	—	33		39	
		6.0		—	14	22	—	28		33	
t_{PLH} t_{PHL}	Propagation Delay Time (ADD - QN)	2.0		—	115	190	—	240		285	ns
		4.5		—	24	38	—	48		57	
		6.0		—	21	32	—	41		48	
t_{PLH} t_{PHL}	Propagation Delay Time (EN - QN)	2.0		—	100	165	—	205		250	ns
		4.5		—	21	33	—	41		50	
		6.0		—	18	28	—	35		43	
t_{PHL}	Propagation Delay Time (CL - QN)	2.0		—	80	135	—	170		205	ns
		4.5		—	17	27	—	34		41	
		6.0		—	15	23	—	29		35	
$t_{W(L)}$	Minimum Pulse Width (CL)	2.0		—	33	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
$t_{W(L)}$	Minimum Pulse Width (EN)	2.0		—	35	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_s	Minimum Set-up Time (DATA)	2.0		—	15	50	—	65		75	ns
		4.5		—	3	10	—	13		15	
		6.0		—	3	9	—	11		13	
t_s	Minimum Set-up Time (ADD)	2.0		—	—	25	—	30	—	40	ns
		4.5		—	—	5	—	6	—	8	
		6.0		—	—	5	—	6	—	7	
t_h	Minimum Hold Time (DATA)	2.0		—	—	25	—	30	—	40	ns
		4.5		—	—	5	—	6	—	8	
		6.0		—	—	5	—	6	—	7	
t_h	Minimum Hold Time (ADD)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	73	—	—	—			pF

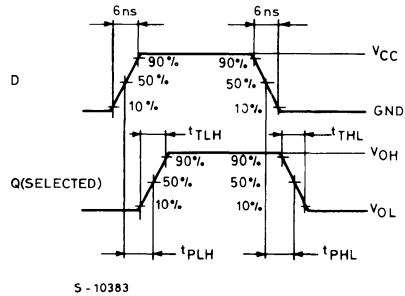
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

Average operating current can be obtained by the following equation.

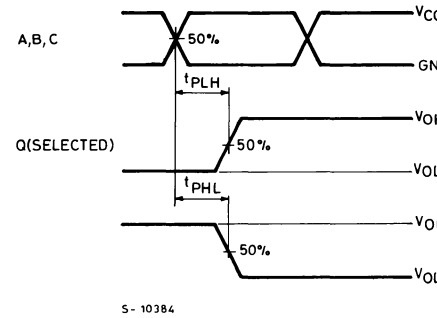
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

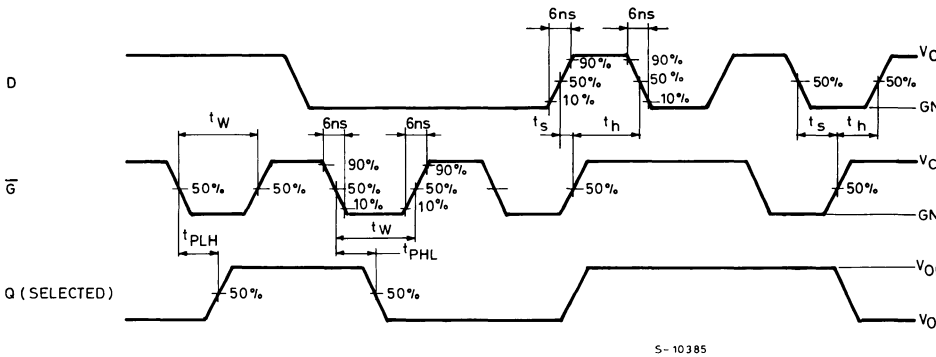
WAVEFORM 1. ($\overline{G}$ = L, $\overline{CLR}$ = H, A ~ C = STABLE)



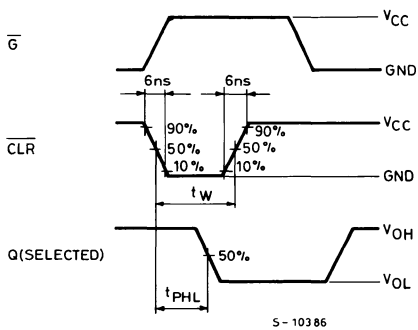
WAVEFORM 2. ($\overline{G}$ = L)



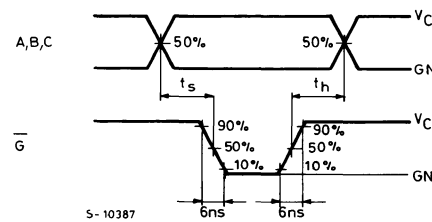
WAVEFORM 3. ($\overline{CLR}$ = H, A ~ C = STABLE)



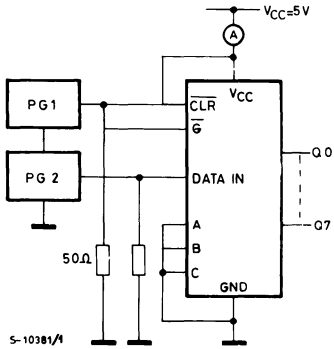
WAVEFORM 4. (D = H, A ~ C-STABLE)

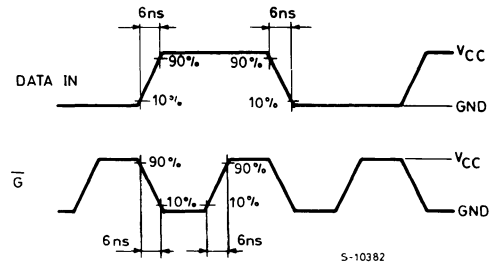


WAVEFORM 5. ($\overline{CLR}$ = H)



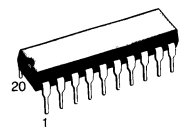
TEST CIRCUIT I_{CC} (Opr.)



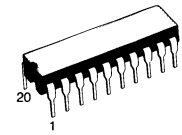


OCTAL D-TYPE FLIP FLOP WITH CLEAR

- HIGH SPEED
  f_{MAX} = 48 MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN).
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS273



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

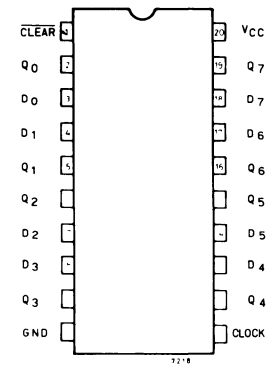
ORDERING NUMBERS:

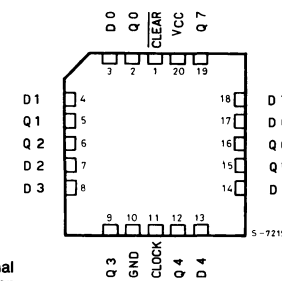
M54HC273 F1
M74HC273 B1N
M74HC273 F1
M74HC273 C1
M74HC273 M1

DESCRIPTION

The M54/74HC273 is a high speed CMOS OCTAL D-TYPE FLIP FLOP WITH CLEAR fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
Information signals applied to D inputs are transfered to the Q outputs on the positive-going edge of the clock pulse.
When the $\overline{CLEAR}$ input is held low, the Q output are in the low logic level independent of the other inputs.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)





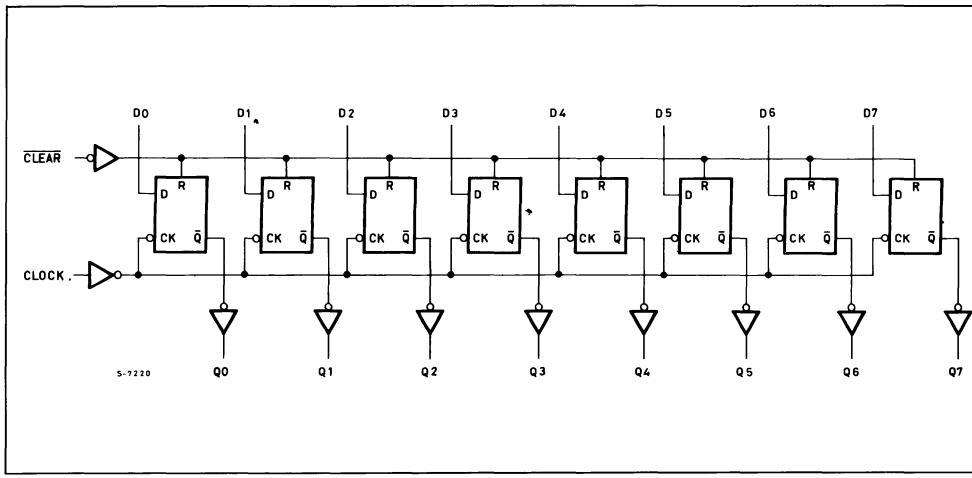
NC = No Internal Connection

TRUTH TABLE

INPUTS			OUTPUT	FUNCTION
$\overline{CLEAR}$	D	CLOCK	Q	
L	X	X	L	CLEAR
H	L	↑	L	
H	H	↑	H	
H	X	↓	Qn	NO CHANGE

X: DON'T CARE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			-40 to $85°C$ 74HC		-55 to $125°C$ 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	$-20\ \mu A$	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		-4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		-5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0.0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	$20\ \mu A$	—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	± 0.1	—	± 1.0	—	± 1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time	—	4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Q)	—	20	31	ns
t_{PHL}	Propagation Delay Time ($\overline{\text{CLEAR}}$-Q)	—	19	30	ns
f_{MAX}	Maximum Clock Frequency	30	48	—	MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	9	15	—	19	—	22	
		6.0		—	8	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q)	2.0		—	92	180	—	225	—	270	ns
		4.5		—	25	36	—	45	—	54	
		6.0		—	22	31	—	38	—	46	
t_{PLH}	Propagation Delay Time ($\overline{CLEAR}$-Q)	2.0		—	92	175	—	220	—	265	ns
		4.5		—	25	35	—	44	—	53	
		6.0		—	22	30	—	37	—	45	
f_{MAX}	Maximum Clock Frequency	2.0		5.4	11	—	4.4	—	3.6	—	MHz
		4.5		27	44	—	22	—	18	—	
		6.0		32	52	—	26	—	21	—	
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLEAR}$)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-up Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	6	13	—	16	—	19	
t_h	Minimum Hold Time	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{REM}	Minimum Removal Time $\overline{CLEAR}$	2.0		—	18	75	—	95	—	110	ns
		4.5		—	5	15	—	19	—	22	
		6.0		—	4	13	—	16	—	19	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	53	—	—	—	—	—	pF

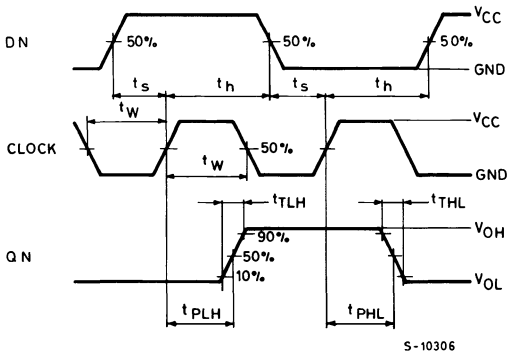
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

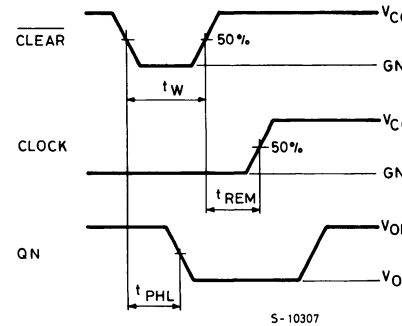
Average operating current is: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per FF)

And the total C_{PD} when n pcs Flip Flop operate can be gained by the following equation.

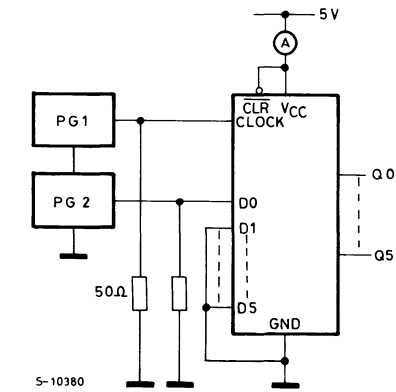
C_{PD} (total) = $38 + 15 \cdot n$

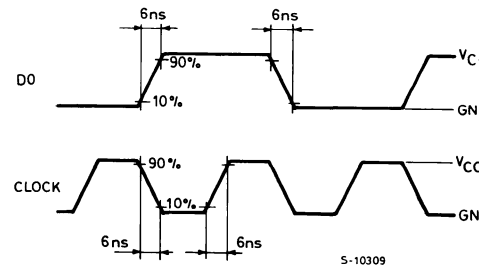
SWITCHING CHARACTERISTICS TEST WAVEFORM





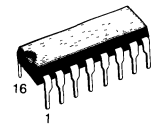
TEST CIRCUIT I_{CC} (Opr.)



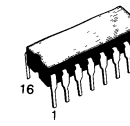


QUAD $\overline{S}$ - $\overline{R}$ LATCH

- HIGH SPEED
  t_{PD} = 13 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 2 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS279



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC279 F1
M74HC279 B1N
M74HC279 F1
M74HC279 C1
M74HC279 M1

DESCRIPTION

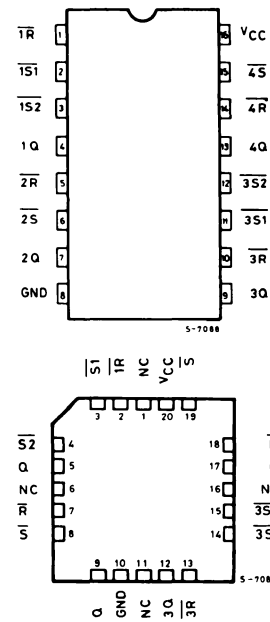
The M54/74HC279 is a high speed CMOS QUAD $\overline{S}$ - $\overline{R}$ LATCH fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUTS		OUTPUT
$\overline{S}$#	$\overline{R}$	Q
H	H	Q0
L	H	H
H	L	L
L	L	H

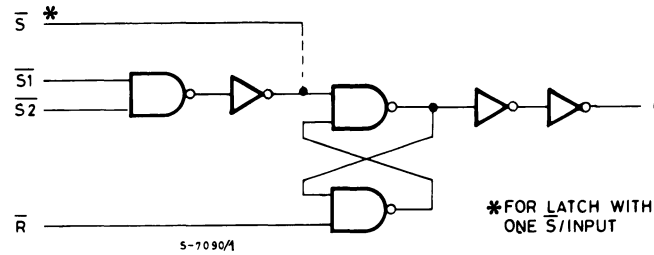
NOTE: Q0 = THE LEVEL OF Q BEFORE THE INDICATED INPUT CONDITION WAS ESTABLISHED.
# FOR LATCHES WITH DOUBLE $\overline{S}$ INPUTS:
H = BOTH $\overline{S}$ INPUTS HIGH
L = ONE OF BOTH INPUTS LOW

PIN CONNECTIONS (top view)



NC =
No Internal
Connection

LOGIC DIAGRAM (For one latch)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0.0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	2	—	20	—	40	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{S}$, $\overline{S}_2$ - Q)		13	21	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{S}$ - Q)		10	17	ns
t_{PHL}	Propagation Delay Time ($\overline{R}$ - Q)		12	20	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

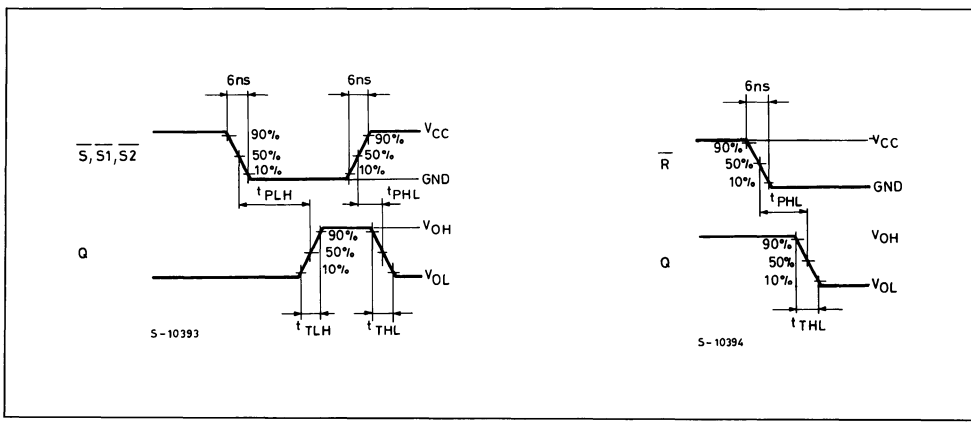
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	22 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{S1}$, $\overline{S2}$ - Q)	2.0 4.5 6.0		— — —	59 16 14	130 26 22	— — —	165 33 28		195 39 33	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{S}$ - Q)	2.0 4.5 6.0		— — —	42 12 11	100 20 17	— — —	125 25 21		150 30 26	ns
t_{PHL}	Propagation Delay Time ($\overline{R}$ - Q)	2.0 4.5 6.0		— — —	50 15 13	120 24 20	— — —	150 30 26		180 36 31	ns
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	26	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

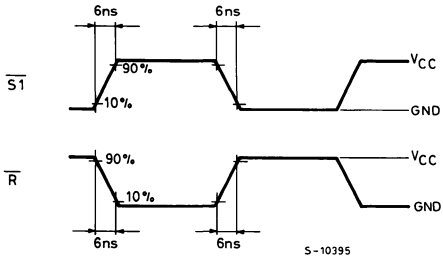
Average operating current can be obtained by the following equation.

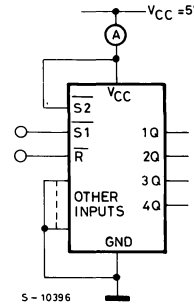
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Latch)

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)

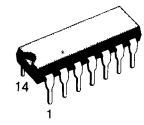




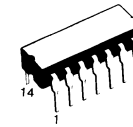
M54HC280
M74HC280

9-BIT PARITY GENERATOR

- HIGH SPEED
  t_{PD} = 26 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C 6V
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN).
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (opr) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS280



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC280 F1
M74HC280 B1N
M74HC280 F1
M74HC280 C1
M74HC280 M1

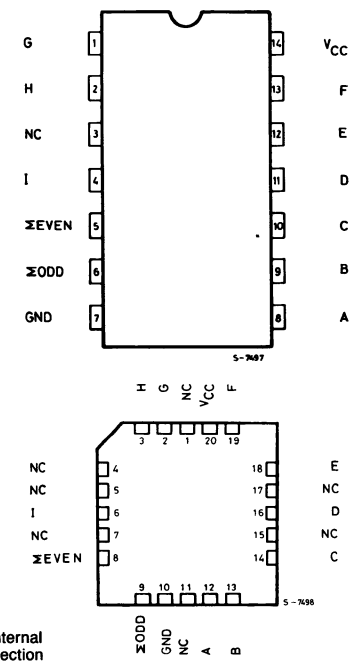
DESCRIPTION

The M54/74HC280 is a high speed CMOS 9-BIT PARITY GENERATOR fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low consumption.
It is composed of nine data inputs (A to I) and odd/even parity outputs (Σ ODD and Σ EVEN).
The nine data inputs control the output conditions. When the number of high level inputs is odd, ΣODD output is kept high and ΣEVEN output low. Conversely, when the number is even, ΣEVEN output is kept high and ΣODD low.
This IC generates either odd or even parity making it flexible application.
The word-length capability is easily expanded by cascading.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

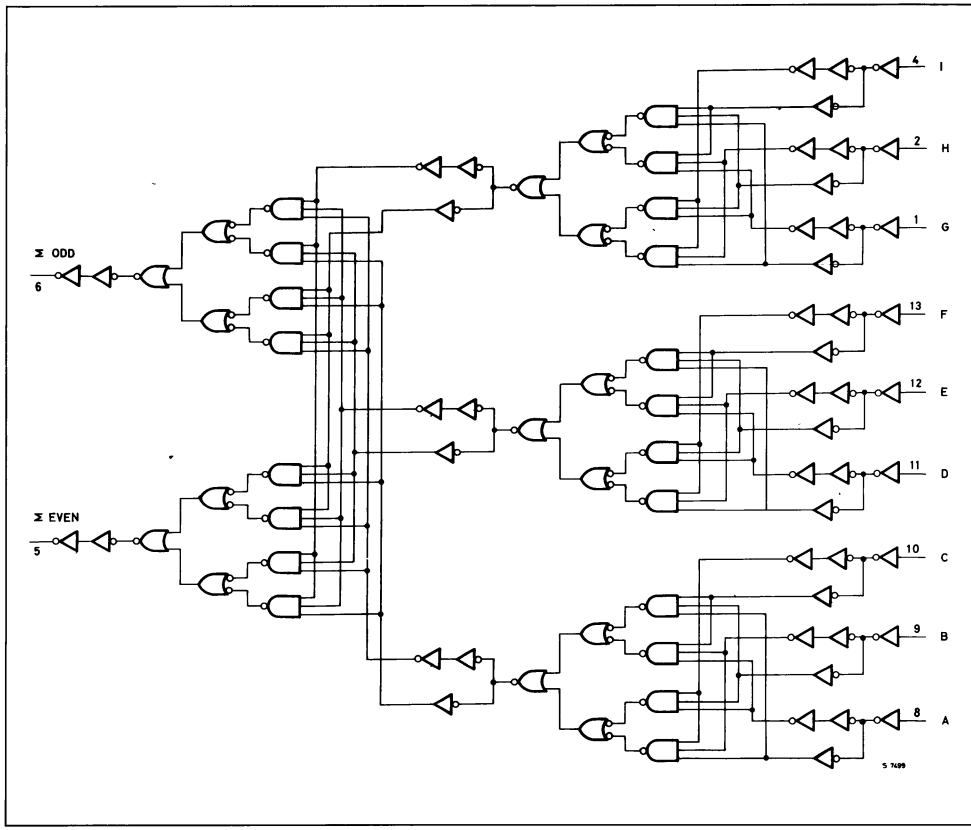
NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	ΣEVEN	ΣODD
0, 2, 4, 6, 8,	H	L
1, 3, 5, 7, 9,	L	H

PIN CONNECTIONS (top view)



NC = No Internal Connection

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V: 0 to 1000 V_{CC} = 4.5V: 0 to 500 V_{CC} = 6 V: 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0 4.5 6.0	V_I V_{IH} or V_{IL}	I_O −20 μA	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	1.9 4.4 5.9	— — —	V
		4.5 6.0		−4.0 mA −5.2 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	
V_{OL}	Low Level Output Voltage	2.0 4.5 6.0	V_{IH} or V_{IL}	20 μA	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
		4.5 6.0		4.0 mA 5.2 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		26	41	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

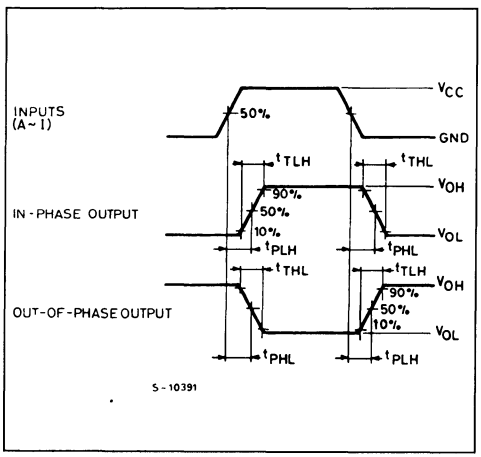
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	124	235	—	295		355	ns
		4.5		—	31	47	—	59		71	
		6.0		—	26	40	—	50		60	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	110	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

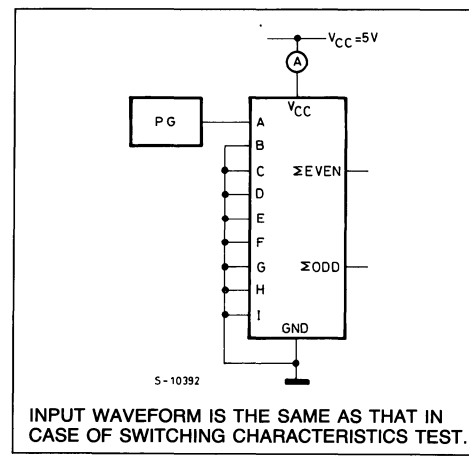
Average operating current can be obtained by the following equation.

$I_{CC\ (Opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



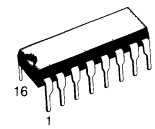
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

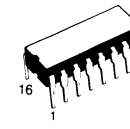
M54HC283
M74HC283

4-BIT BINARY FULL ADDER

- HIGH SPEED
  t_{PD} = 30 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN).
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN).
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- FULL-CARRY LOOK-AHEAD ACROSS THE FOUR BITS
- PARTIAL LOOK-AHEAD WITH THE ECONOMY OF RIPPLY CARRY
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS283



B1N
Plastic Package



F1
Ceramic Frit Seal Package

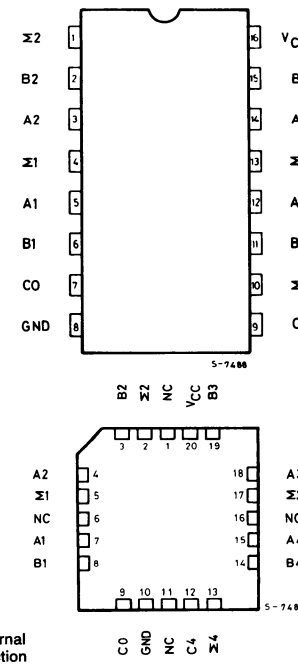
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC283 F1
M74HC283 B1N
M74HC283 F1
M74HC283 C1
M74HC283 M1

PIN CONNECTIONS (top view)



NC = No Internal Connection

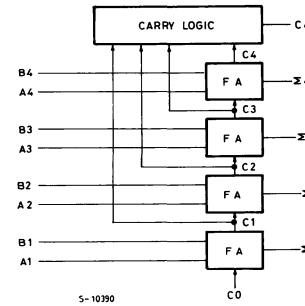
DESCRIPTION

The M54/74HC283 is a high speed CMOS 4-BIT BINARY FULL ADDER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
Sum (Σ) outputs are provided for each bit and a resultant carry (C4) is obtained from the fourth bit. This adder features full internal look ahead across all four bits. A 4 x n binary adder is easily built up by cascading without any additional logic.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

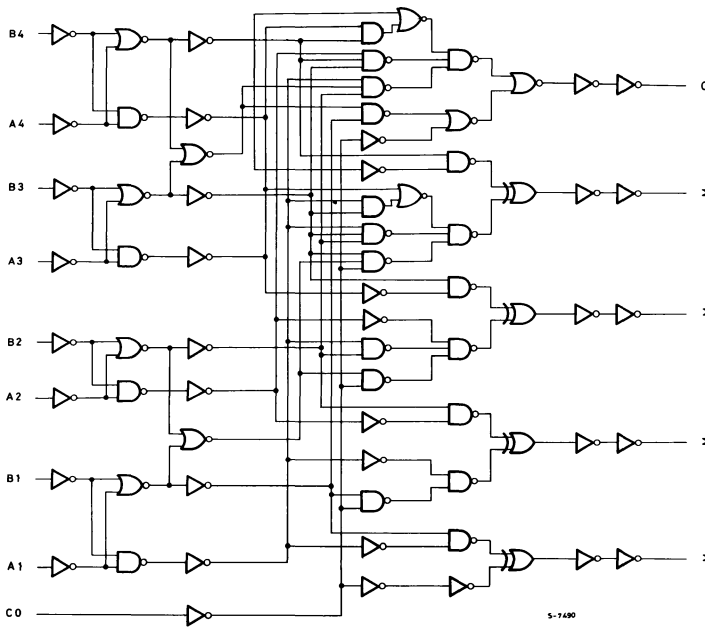
TRUTH TABLE (1 bit)

INPUTS			OUTPUTS	
Bn	An	Cn-1	Σn	Cn
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

BLOCK DIAGRAM



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

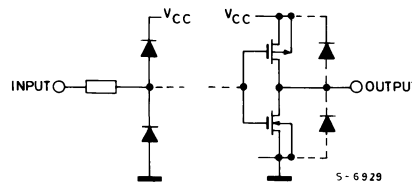
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW/°C: 65 to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

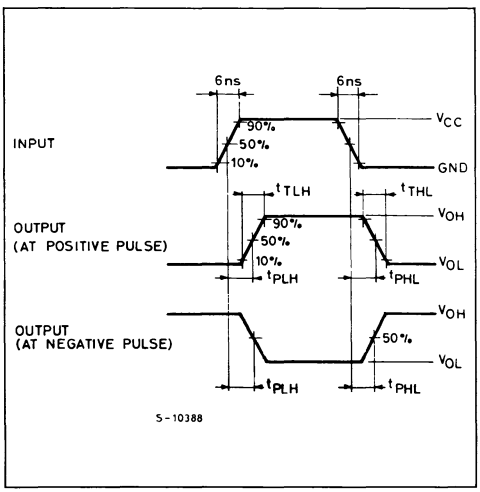
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CO-Σn)		23	36	ns
t_{PLH} t_{PHL}	Propagation Delay Time (C0-C4)		18	29	ns
t_{PLH} t_{PHL}	Propagation Delay Time (An, Bn-Σn)		30	47	ns
t_{PLH} t_{PHL}	Propagation Delay Time (An, Bn-C4)		25	39	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

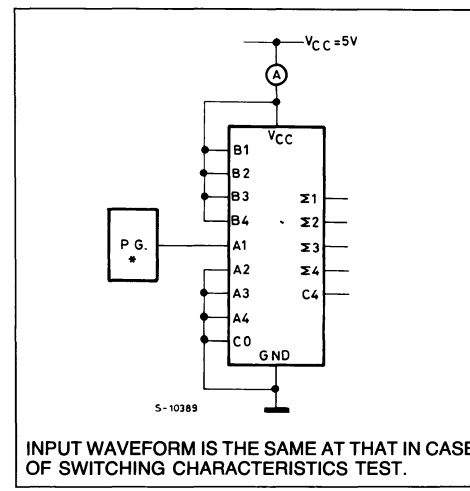
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (C0-Σn)	2.0		—	108	210	—	265		315	ns
		4.5		—	27	42	—	53		63	
		6.0		—	23	36	—	45		54	
t_{PLH} t_{PHL}	Propagation Delay Time (C0-C4)	2.0		—	88	175	—	220		265	ns
		4.5		—	22	35	—	44		53	
		6.0		—	19	30	—	37		45	
t_{PLH} t_{PHL}	Propagation Delay Time (An, Bn-Σn)	2.0		—	140	270	—	340		405	ns
		4.5		—	35	54	—	68		81	
		6.0		—	30	46	—	58		69	
t_{PLH} t_{PHL}	Propagation Delay Time (An, Bn-C4)	2.0		—	116	225	—	280		340	ns
		4.5		—	29	45	—	56		68	
		6.0		—	25	38	—	48		58	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	114	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current is: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



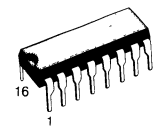
TEST CIRCUIT I_{CC} (Opr.)



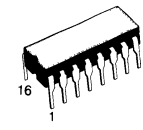
INPUT WAVEFORM IS THE SAME AT THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

PROGRAMMABLE DIVIDER/TIMER

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS292/294



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX C1
M74HCXXX M1

DESCRIPTION

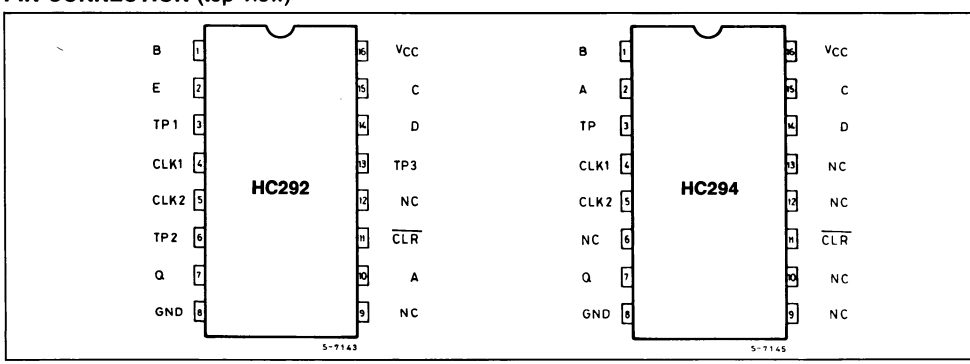
The 54/74HC292 and 54/74HC294 are high speed CMOS PROGRAMMABLE DIVIDER/TIMER fabricated with silicon C²MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
These devices are programmable frequency dividers. Both types have two clock inputs, either one may be used for clock gating. (See the function table). The HC292 can divide from 2^2 to 2^{31}, and the HC294 can divide from 2^2 to 2^{15}. Both types feature an active-low clear input to initialize the state of all flip-flops. To facilitate incoming inspection, test points are provided. (TP1, TP2 and TP3 on the HC292 and TP on the HC294). All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Note: HC292 and HC294 have Q outputs with "Totem pole" configuration the type HC292/HC294 have tests points TP with "Open drain" output configuration.

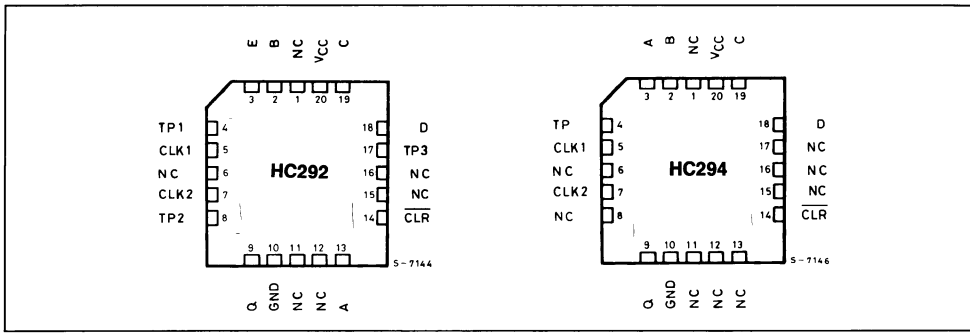
TRUTH TABLE

$\overline{CLEAR}$	CLOCK1	CLOCK2	Q OUTPUT MODE
L	X	X	CLEARED TO L
H		L	UP COUNT
H	L		
H	H	X	NO CHANGE
H	X	H	

PIN CONNECTION (top view)



CHIP CARRIER



ABSOLUTE MAXIMUM RATINGS

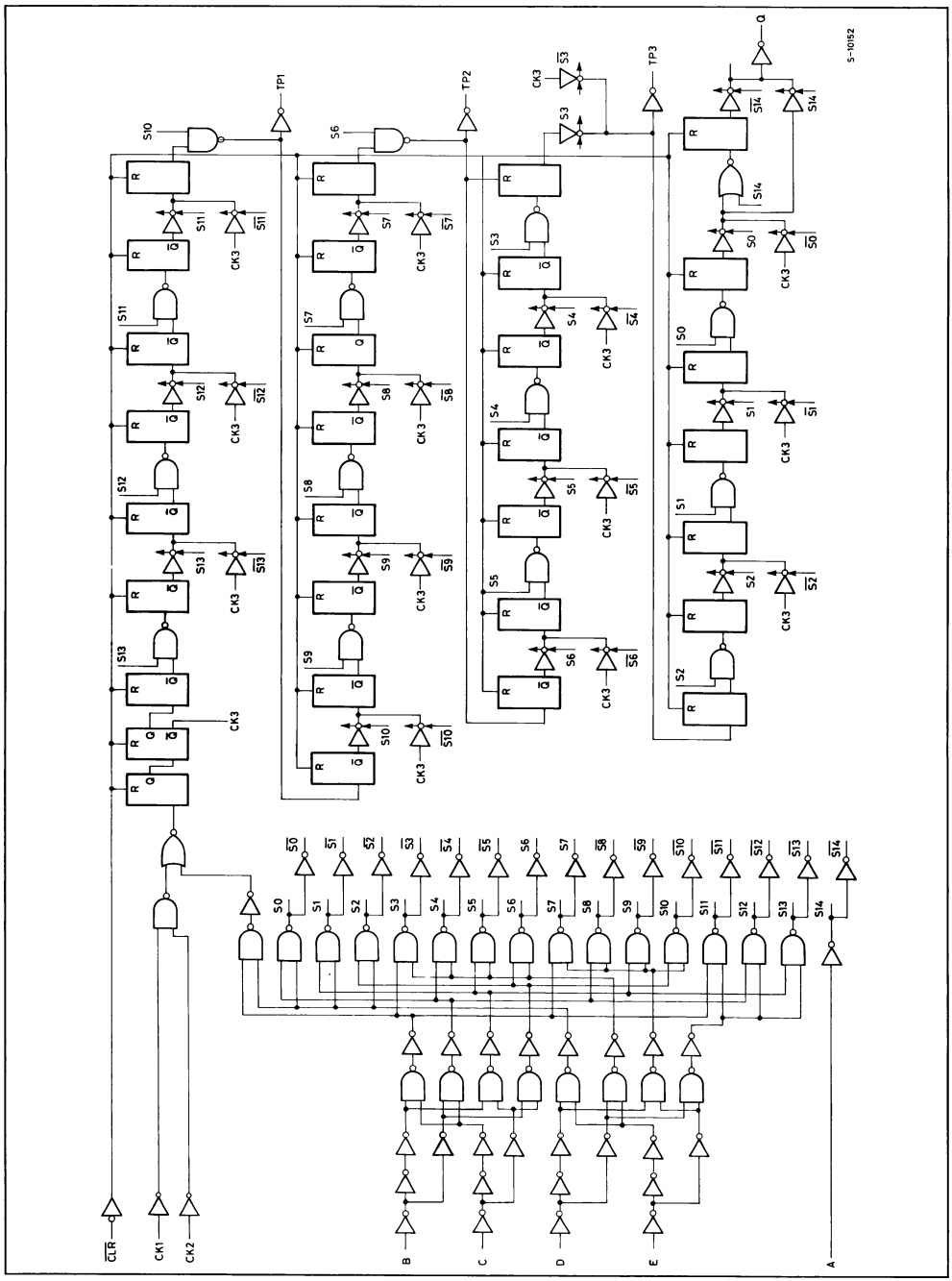
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

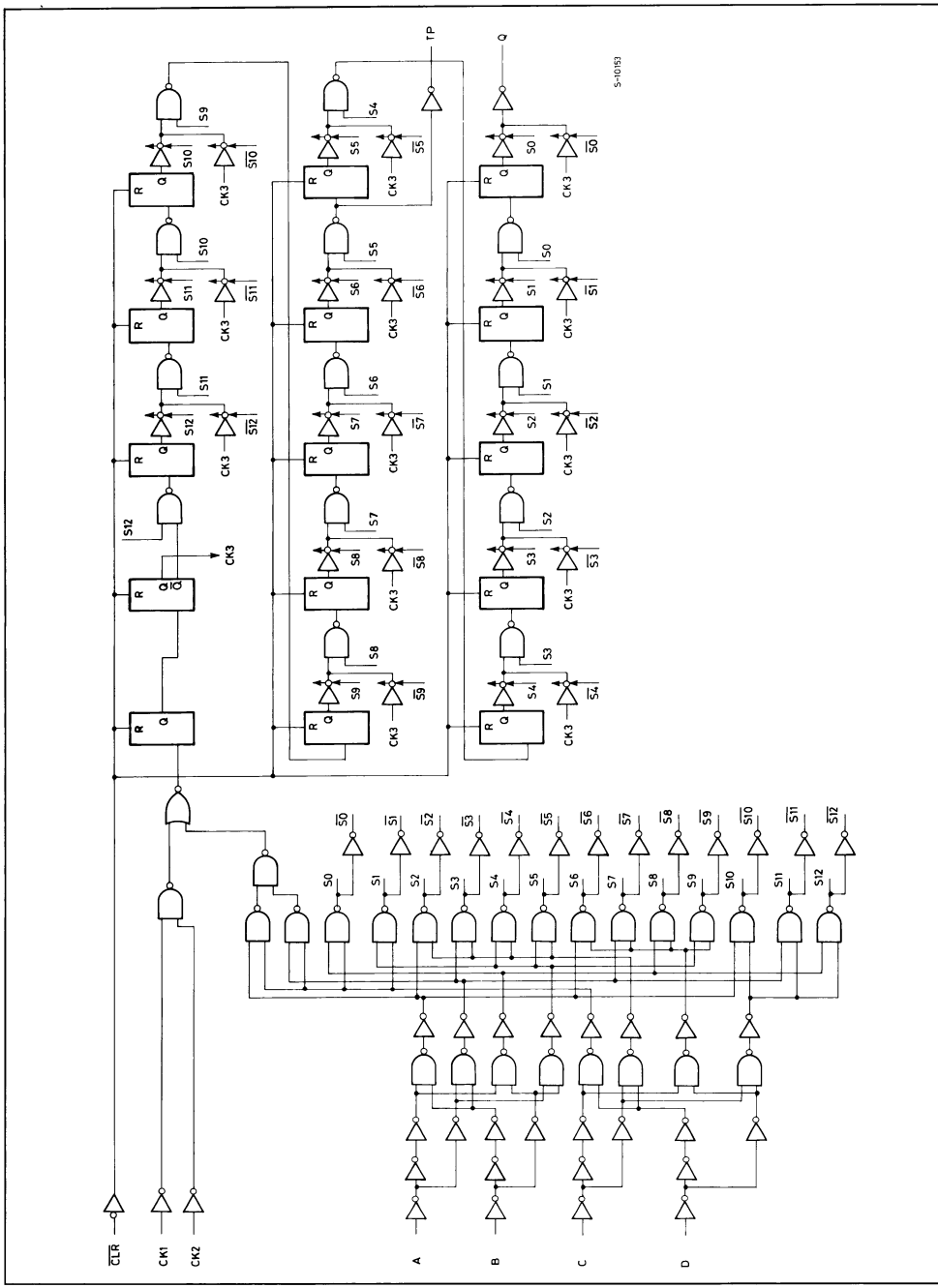
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

LOGIC DIAGRAM (HC292)



LOGIC DIAGRAM (HC294)



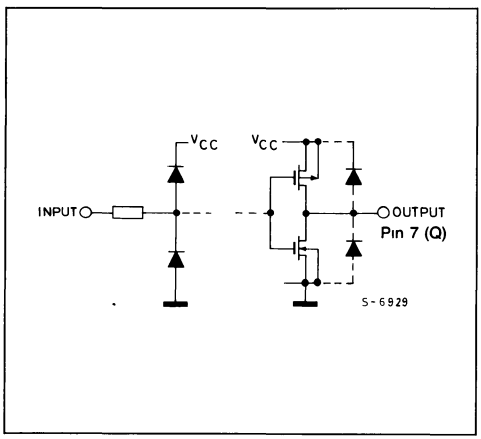
FUNCTION TABLE (HC292)

PROGRAMMING INPUTS					FREQUENCY DIVISION							
					Q		TP1		TP2		TP3	
E	D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	L	2^2	4	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	L	H	H	2^3	8	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	L	L	2^4	16	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	L	H	2^5	32	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	H	L	2^6	64	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	H	H	2^7	128	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	H	L	L	L	2^8	256	2^9	512	2^{17}	131,072	2^2	4
L	H	L	L	H	2^9	512	2^9	512	2^{17}	131,072	2^2	4
L	H	L	H	L	2^{10}	1,024	2^9	512	2^{17}	131,072	2^4	16
L	H	L	H	H	2^{11}	2,048	2^9	512	2^{17}	131,072	2^2	16
L	H	H	L	L	2^{12}	4,096	2^9	512	2^{17}	131,072	2^6	64
L	H	H	L	H	2^{13}	8,192	2^9	512	2^{17}	131,072	2^6	64
L	H	H	H	L	2^{14}	16,384	2^9	512	Disabled Low		2^8	256
L	H	H	H	H	2^{15}	32,768	2^9	512	Disabled Low		2^8	256
H	L	L	L	L	2^{16}	65,536	2^9	512	2^3	8	2^{10}	1,024
H	L	L	L	H	2^{17}	131,072	2^9	512	2^3	8	2^{10}	1,024
H	L	L	H	L	2^{18}	262,144	2^9	512	2^5	32	2^{12}	4,096
H	L	L	H	H	2^{19}	524,288	2^9	512	2^5	32	2^{12}	4,096
H	L	H	L	L	2^{20}	1,048,576	2^9	512	2^7	128	2^{14}	16,384
H	L	H	L	H	2^{21}	2,097,152	2^9	512	2^7	128	2^{14}	16,384
H	L	H	H	L	2^{22}	4,194,304	Disabled Low		2^9	512	2^{16}	65,536
H	L	H	H	H	2^{23}	8,388,608	Disabled Low		2^9	512	2^{16}	65,536
H	H	L	L	L	2^{24}	16,777,216	2^3	8	2^{11}	2,048	2^{18}	262,144
H	H	L	L	H	2^{25}	33,554,432	2^3	8	2^{11}	2,048	2^{18}	262,144
H	H	L	H	L	2^{26}	67,108,864	2^5	32	2^{13}	8,192	2^{20}	1,048,576
H	H	L	H	H	2^{27}	134,217,728	2^5	32	2^{13}	8,192	2^{20}	1,048,576
H	H	H	L	L	2^{28}	268,435,456	2^7	128	2^{15}	32,768	2^{22}	4,194,304
H	H	H	L	H	2^{29}	536,870,912	2^7	128	2^{15}	32,768	2^{22}	4,194,304
H	H	H	H	L	2^{30}	1,073,741,824	2^9	512	2^{17}	131,072	2^{24}	16,777,216
H	H	H	H	H	2^{31}	2,147,483,648	2^9	512	2^{17}	131,072	2^{24}	16,777,216

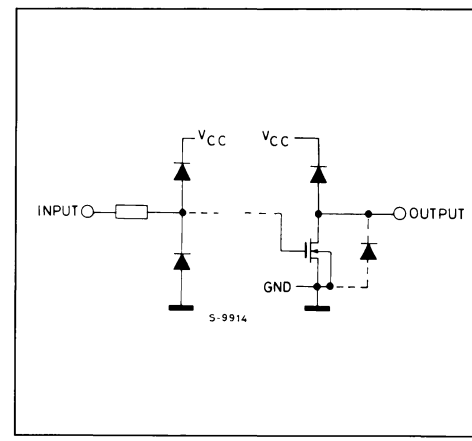
FUNCTION TABLE (HC294)

PROGRAMMING INPUTS				FREQUENCY DIVISION			
				Q		TP	
D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit
L	L	H	L	2^2	4	2^9	512
L	L	H	H	2^3	8	2^9	512
L	H	L	L	2^4	16	2^9	512
L	H	L	H	2^5	32	2^9	512
L	H	H	L	2^6	64	2^9	512
L	H	H	H	2^7	128	Disabled Low	
H	L	L	L	2^8	256	2^2	4
H	L	L	H	2^9	512	2^3	8
H	L	H	L	2^{10}	1,024	2^4	16
H	L	H	H	2^{11}	2,048	2^5	32
H	H	L	L	2^{12}	4,096	2^6	64
H	H	L	H	2^{13}	8,192	2^7	128
H	H	H	L	2^{14}	16,384	2^8	256
H	H	H	H	2^{15}	32,768	2^9	512

INPUT AND OUTPUT EQUIVALENT CIRCUIT
(TOTEM POLE OUTPUT)



INPUT AND OUTPUT EQUIVALENT CIRCUIT
(OPEN DRAIN OUTPUT)



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			-40 to $85°C$ 74HC		-55 to $125°C$ 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage (Q Output)	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	$-20\ \mu A$	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
	*	4.5		-4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		-5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
	#	4.5		1.0 mA		4.18	4.31	—	4.13	—	4.10	—
		6.0		1.3 mA		5.68	5.8	—	5.63	—	5.60	—
V_{OL}	Low Level Output Voltage	2.0			—	0.0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	$20\ \mu A$	—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
	*	4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
	#	4.5		1.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		1.3 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	± 0.1	—	± 1.0	—	± 1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

*: FOR Q OUTPUT
#: FOR TP OUTPUTS

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter		54HC and 74HC			Unit
			Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time Q OUTPUT			4	8	ns
t_{THL}	Output Transition Time TP OUTPUTS			29	45	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK-Q)	HC292		58	89	ns
		HC294		53	81	
t_{PHL}	Propagation Delay Time (CLEAR-Q)	HC292		49	75	ns
		HC294		45	69	
f_{MAX}	Maximum Clock Frequency	HC292	28	56		MHz
		HC294	35	61		

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

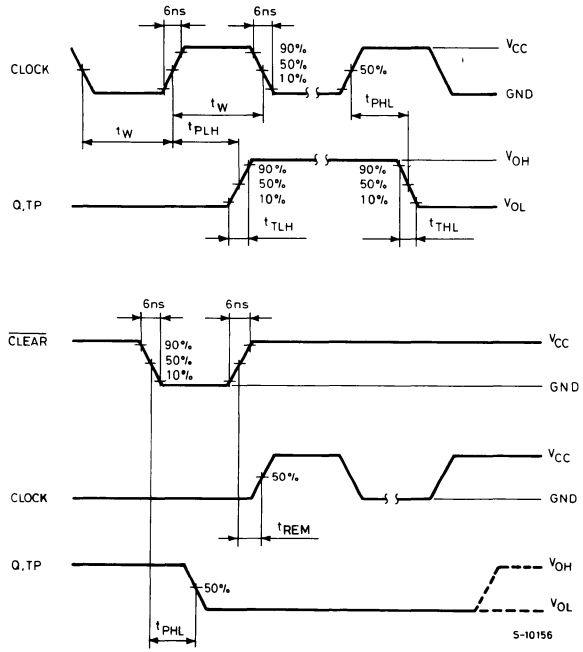
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{THL}	Output Transition Time Q OUTPUT	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{THL}	Output Transition Time TP OUTPUT	2.0		—	132	255	—	320	—	385	ns
		4.5		—	33	51	—	64	—	77	
		6.0		—	28	43	—	55	—	65	
t_{PLH} t_{PHL}	Propagation Delay Time (CK-Q)*	2.0	B = "H"	—	264	500	—	635	—	750	ns
		4.5		—	66	100	—	127	—	150	
		6.0	A = C = D = E = "L"	—	56	85	—	110	—	127	
t_{PLH} t_{PHL}	Propagation Delay Time (CK-Q)**	2.0	B = "H"	—	236	455	—	571	—	676	ns
		4.5		—	59	91	—	115	—	136	
		6.0	A = C = D = "L"	—	50	77	—	100	—	115	
t_{PHL}	Propagation Delay Time ($\overline{CLR}$-Q)*	2.0		—	224	425	—	535	—	640	ns
		4.5		—	56	85	—	107	—	128	
		6.0		—	48	73	—	92	—	109	
t_{PHL}	Propagation Delay Time ($\overline{CLR}$-Q)**	2.0		—	204	390	—	490	—	585	ns
		4.5		—	51	78	—	98	—	117	
		6.0		—	43	67	—	84	—	99	
f_{MAX}	Maximum Clock Frequency*	2.0		5	13	—	4	—	3.4	—	MHz
		4.5		25	51	—	20	—	17	—	
		6.0		29	60	—	24	—	20	—	
f_{MAX}	Maximum Clock Frequency**	2.0		6	14	—	5	—	4.2	—	MHz
		4.5		32	55	—	26	—	21	—	
		6.0		38	65	—	31	—	25	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width CK)	2.0		—	36	100	—	125	—	150	ns
		4.5		—	9	20	—	25	—	30	
		6.0		—	8	17	—	21	—	26	
$t_{W(L)}$	Minimum Pulse Width CLEAR*	2.0		—	60	150	—	190	—	225	ns
		4.5		—	15	30	—	38	—	45	
		6.0		—	13	26	—	33	—	38	
$t_{W(L)}$	Minimum Pulse Width CLEAR**	2.0		—	72	175	—	220	—	265	ns
		4.5		—	18	35	—	44	—	53	
		6.0		—	15	30	—	37	—	45	
t_{REM}	Minimum Removal Time $\overline{CLEAR}$	2.0		—	—	25	—	30	—	40	ns
		4.5		—	—	5	—	6	—	8	
		6.0		—	—	5	—	6	—	7	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance		M54/74HC292	—	22	—	—	—	—	—	pF
			M54/74HC294	—	23	—	—	—	—	—	

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

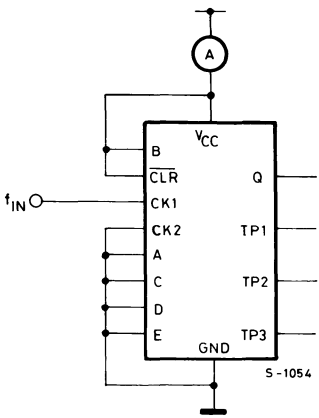
* M54/74HC292
** M54/74HC294

SWITCHING CHARACTERISTICS TEST WAVEFORM

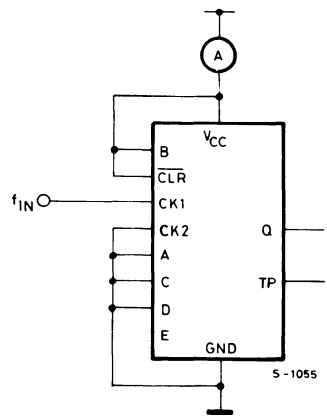


TEST CIRCUIT I_{CC} (Opr.)

HC292



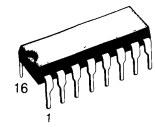
HC294



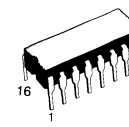
INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

QUAD 2-CHANNEL MULTIPLEXER/REGISTER

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS298



B1N
Plastic Package



F1
Ceramic Frit Seal Package

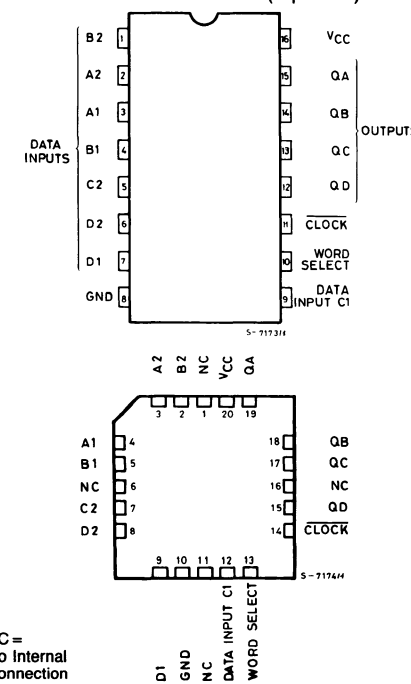
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC298 F1
M74HC298 B1N
M74HC298 F1
M74HC298 C1
M74HC298 M1

PIN CONNECTIONS (top view)



DESCRIPTION

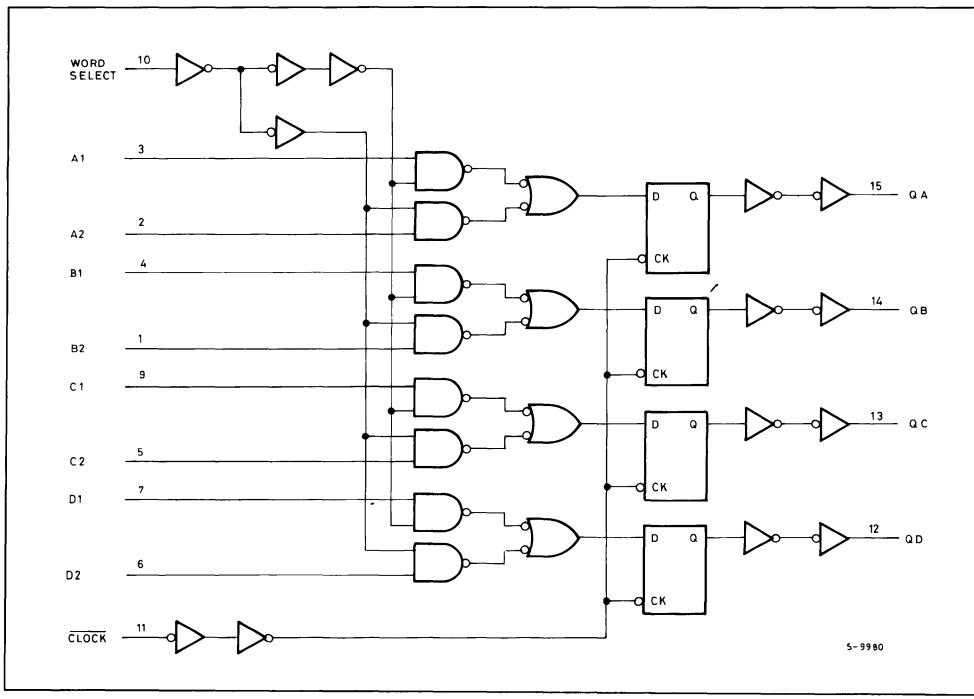
The M54/74HC298 is a high speed CMOS QUAD 2-CHANNEL MULTIPLEXER/REGISTER fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. These circuits are controlled by the signals WORD SELECT and CLOCK. When the WORD SELECT input is taken low Word 1 (A1, B1, C1 and D1) is presented to the input of the flip-flops, and when WORD SELECT is high Word 2 (A2, B2, C2 and D2) is presented to the inputs of the flip-flops. The select word is clocked to the output terminals on the negative edge of the clock pulse.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	QA	QB	QC	QD
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	↑	QA0	QB0	QC0	QD0

X : DON'T CARE (INCLUDING TRANSITION)
a1, a2, ETC. : THE LEVEL OF STEADY-STATE INPUT AT a1, a2, ETC.
QA0, QB0, ETC. : THE LEVEL OF QA, QB, ETC. ENTERED ON THE MOST RECENT NEGATIVE TRANSITION OF THE CLOCK INPUT.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

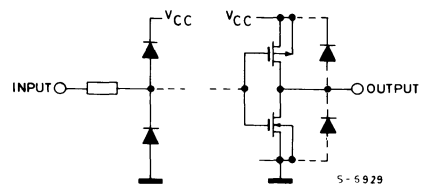
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW:≅65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V 4.5V 6 V	0 to 1000 0 to 500 0 to 400	ns

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_{IN}	I_{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	4	—	40	—	80	

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

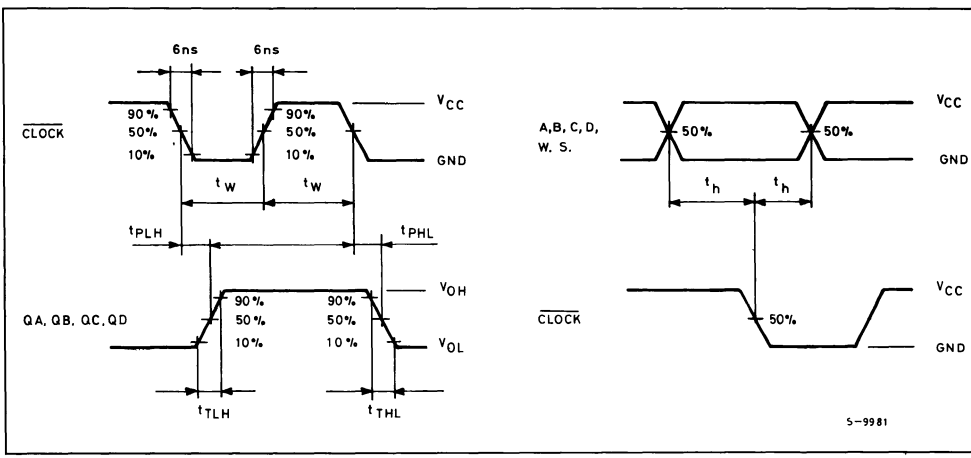
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Q		15	24	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

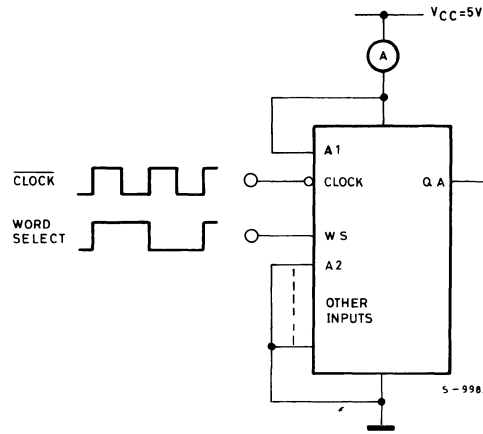
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOCK}$-Q)	2.0		—	72	140	—	175	—	210	ns
		4.5		—	18	28	—	35	—	42	
		6.0		—	15	24	—	30	—	36	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width ($\overline{CLOCK}$)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-up Time (A,B,C,D)	2.0		—	10	50	—	65	—	75	ns
		4.5		—	2	10	—	13	—	15	
		6.0		—	2	9	—	11	—	13	
t_s	Minimum Set-up Time (W.S.)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_h	Minimum Hold Time (A,B,C,D, W.S.)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	47	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test circuit).
Average operating current can be obtained from the equation: $I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per bit)
And the C_{PD} for the operating n-bit can be obtained by the following equation: $C_{PD} = 32 + n \cdot 15$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT

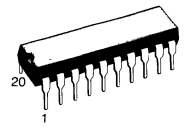


TRANSITION TIME AND V_{IH}, V_{IL} OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

M54/74HC299
M74/74HC323

HC299 8-BIT PIPO SHIFT REGISTER WITH ASYNCHRONOUS CLEAR
HC323 8-BIT PIPO SHIFT REGISTER WITH SYNCRONOUS CLEAR

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (Min.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 6 mA (MIN.) for Q_A, to Q_H,
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.) for Q_A, to Q_H
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS299



B1N
Plastic Package

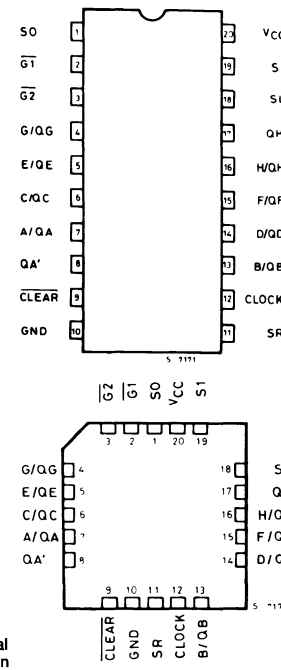
F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HCTXXX F1
M74HCTXXX B1N
M74HCTXXX F1
M74HCTXXX C1
M74HCTXXX M1

PIN CONNECTIONS (top view)

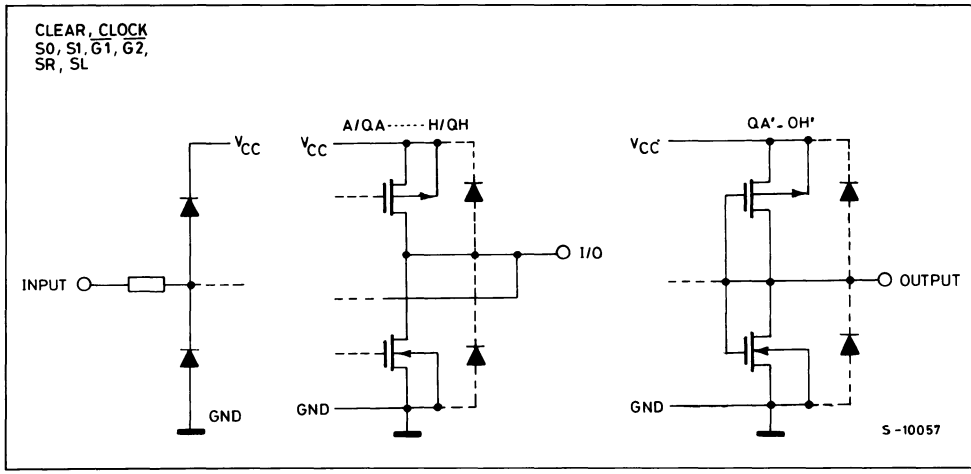


NC = No Internal Connection

DESCRIPTION

The M54/74HC299/323 are high speed CMOS 8-BIT PIPO SHIFT REGISTERS (3-STATE) fabricated with silicon gate C²MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power consumption.
These devices have four modes (HOLD, SHIFT LEFT, SHIFT RIGH and LOAD DATA). Each mode is chosen by two function select inputs (S0, S1). When one or both enable inputs, (G1, G2) are high, the eight input/output terminals are in the high-impedance state; however sequential operation or clearing of the register is not affected.
Clear function on the HC299 is asynchronous to CLOCK, while the HC323 is cleared synchronous to clock.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



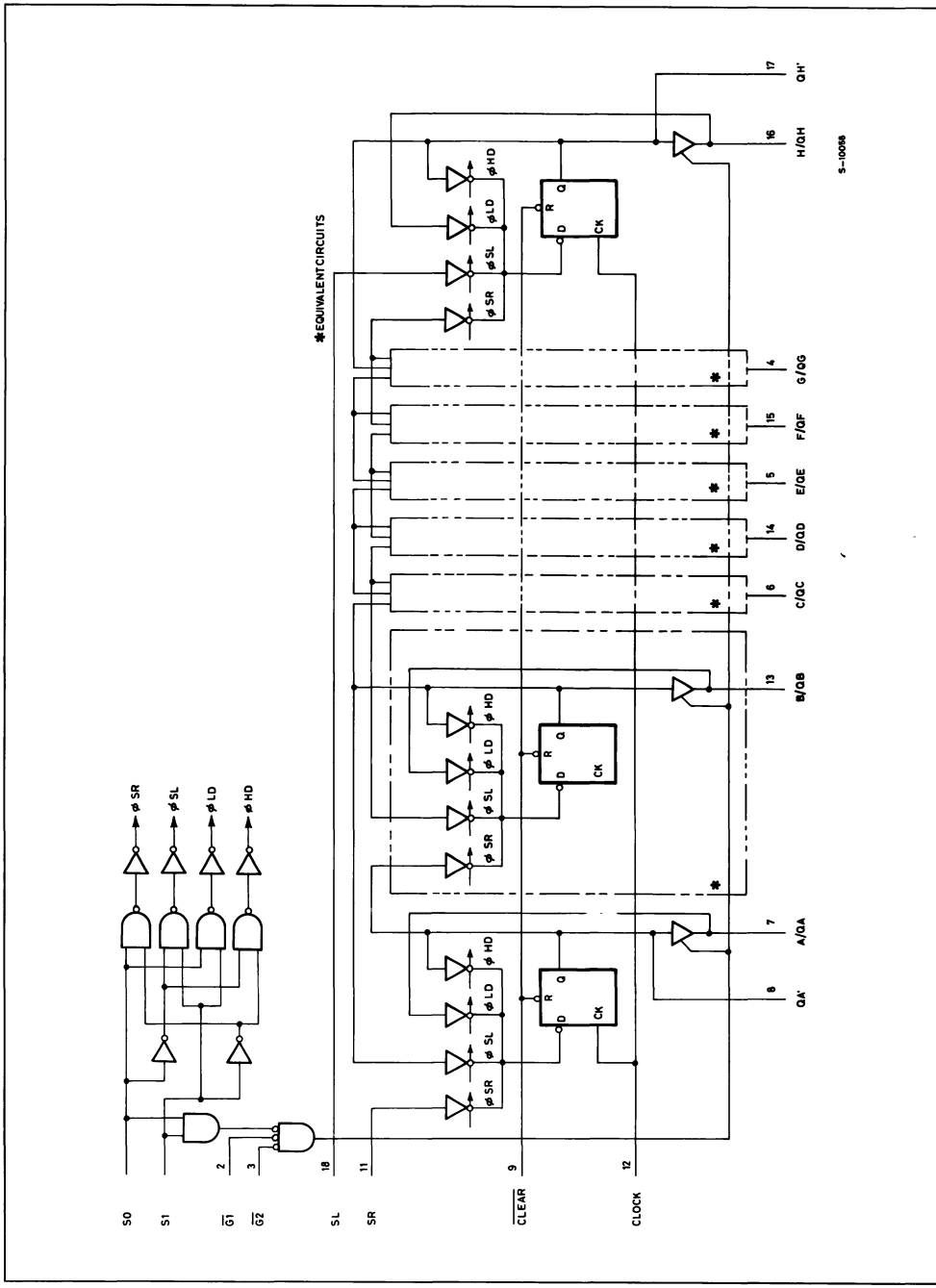
TRUTH TABLE

MODE	INPUTS							INPUTS/OUTPUTS				OUTPUTS	
	CLEAR	FUNCTION SELECT		OUTPUT CONTROL		CLOCK		SERIAL		A/QA	H/QH	QA'	QH'
		S1	S0	G1*	G2*	(299)	(323)	SL	SR				
Z	L	H	H	X	X	X		X	X	Z	Z	L	L
CLEAR	L	L	X	L	L	X	↑	X	X	L	L	L	L
	L	X	L	L	L	X	↑	X	X	L	L	L	L
HOLD	H	L	L	L	L	X		X	X	QA0	QH0	QA0	QH0
SHIFT RIGHT	H	L	H	L	L	↑		X	H	H	QGn	H	QGn
	H	L	H	L	L	↑		X	L	L	QGn	L	QGn
SHIFT LEFT	H	H	L	L	L	↑		H	X	QBn	H	QBn	H
	H	H	L	L	L	↑		L	X	QBn	L	QBn	L
LOAD	H	H	H	X	X	↑		X	X	a	h	a	h

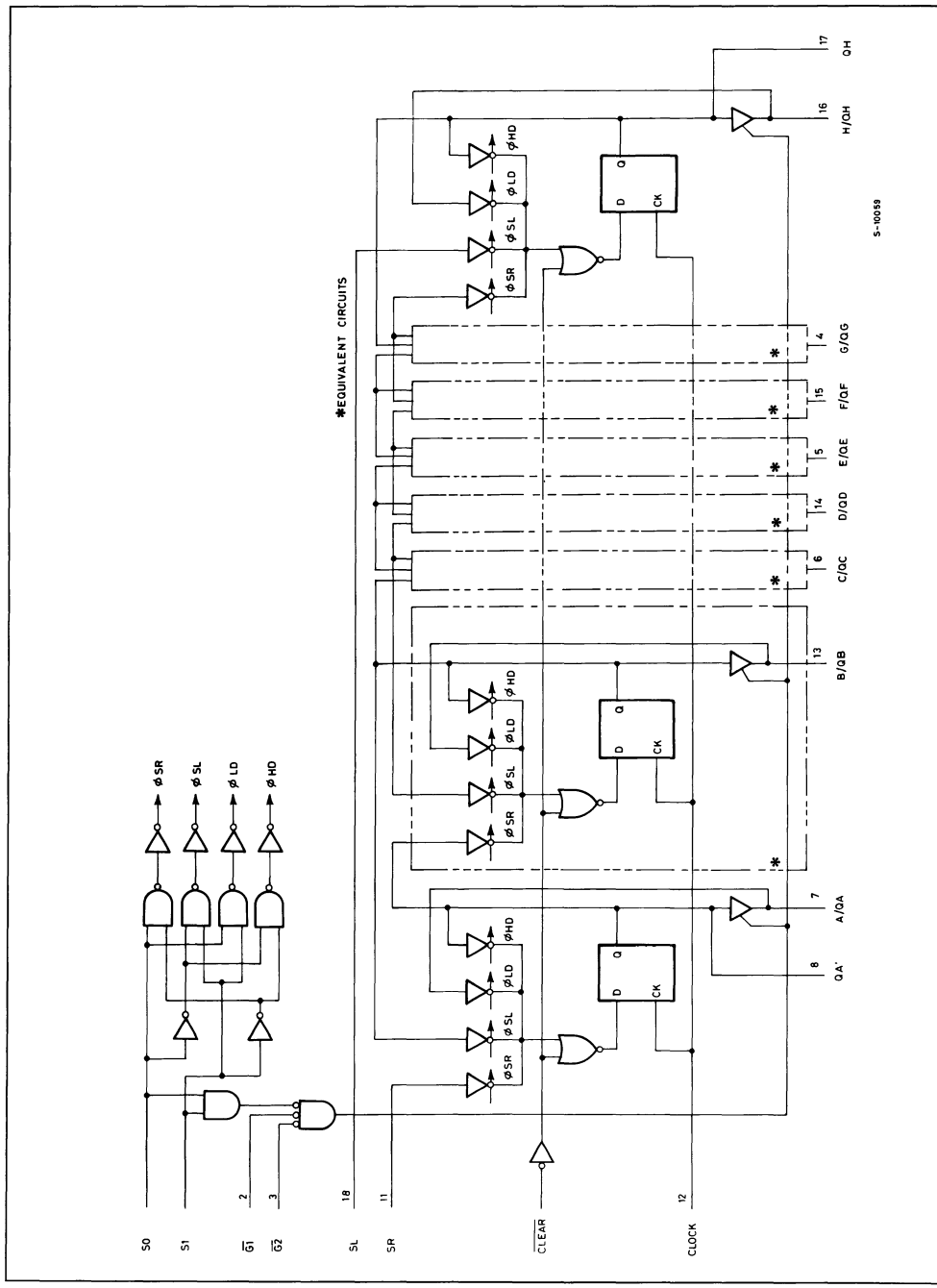
* When one or both output controls are high, the eight, input/output terminals are in the high-impedance state; however sequential operation or clearing of the register is not affected.

Z : HIGH IMPEDANCE
Qno : THE LEVEL OF An BEFORE THE INDICATED STEADY-STATE INPUT CONDITIONS WERE ESTABLISHED.
Qnn : THE LEVEL OF Qn BEFORE THE MOST RECENT ACTIVE TRANSITION INDICATED BY ↓ OR ↑
a,h : THE LEVEL OF THE STEADY-STATE INPUTS A, H, RESPECTIVELY.
X : DON'T CARE

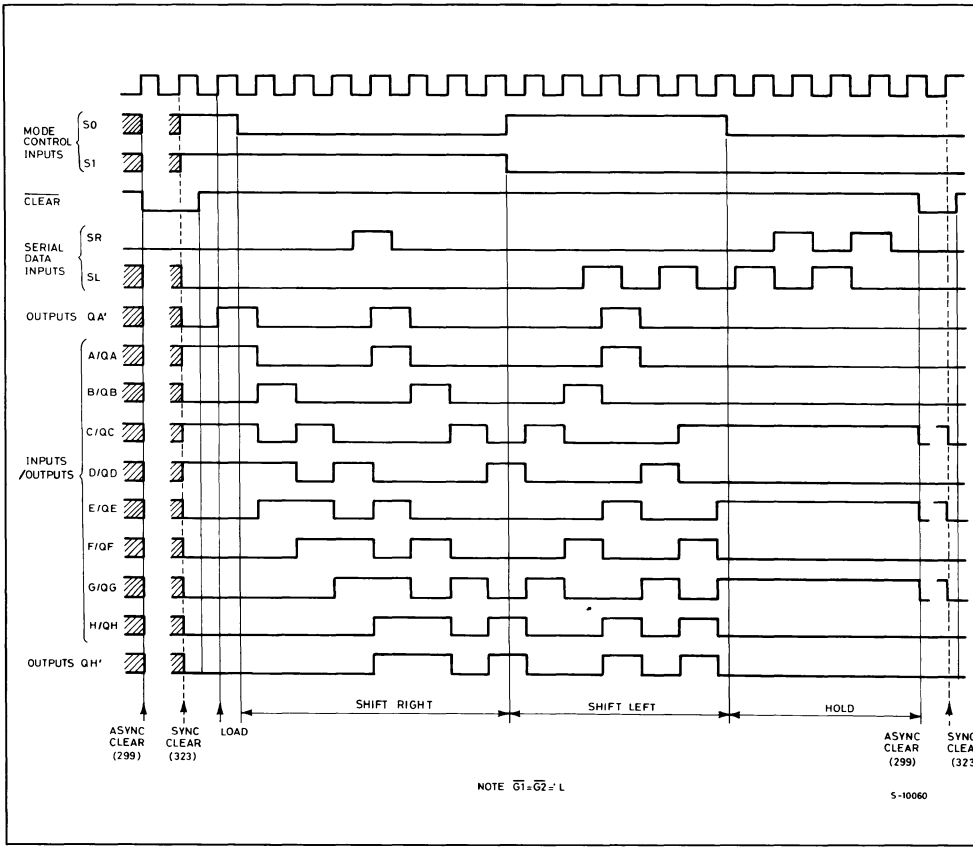
LOGIC DIAGRAM (HC299)



LOGIC DIAGRAM (HC323)



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V: 0 to 1000 V_{CC} = 4.5V: 0 to 500 V_{CC} = 6 V: 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0 4.5 6.0	V_{IN} V_{IH} or V_{IL}	I_{OH} −20 μA	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	1.9 4.4 5.9	— — —	V
		4.5 6.0	Q_A to Q_H	−6.0 mA −7.8 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	
		4.5 6.0	Q_A', Q_H'	−4.0 mA −5.2 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	
V_{OL}	Low Level Output Voltage	2.0 4.5 6.0	V_{IN} V_{IH} or V_{IL}	I_{OH} 20 μA	— — —	0 0 0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
		4.5 6.0	Q_A to Q_H	6.0 mA 7.8 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40	
		4.5 6.0	Q_A', Q_H'	4.0 mA 5.2 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40	
I_{OZ}	3-State Output Off-State Current	6.0	V_{IN} = V_{IL} or V_{IH} V_{OUT} = V_{CC} or GND		—	—	±0.5	—	±5.0	—	±10	μA
I_{IN}	Input Leakage Current	6.0	V_{IN} = V_{CC} or GND		—	—	±0.1	—	±1.0	—	±1.0	
I_{CC}	Quiescent Supply Current	6.0	V_{IN} = V_{CC} or GND		—	—	4	—	40	—	80	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (QA to QH)	2.0		—	25	60	—	75	—	90	ns
		4.5		—	7	12	—	15	—	18	
		6.0		—	6	10	—	13	—	15	
t_{TLH} t_{THL}	Output Transition Time (QA', QH')	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-QA to QH)	2.0		—	120	235	—	295	—	355	ns
		4.5		—	30	47	—	59	—	71	
		6.0		—	26	40	—	50	—	60	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-QA',QH')	2.0		—	120	235	—	295	—	345	ns
		4.5		—	30	47	—	59	—	71	
		6.0		—	26	40	—	50	—	60	
t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$-QA to QH)(1)	2.0		—	116	230	—	290	—	345	ns
		4.5		—	29	46	—	58	—	69	
		6.0		—	25	39	—	49	—	59	
t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$-QA', QH')(1)	2.0		—	116	230	—	290	—	345	ns
		4.5		—	29	46	—	58	—	69	
		6.0		—	25	39	—	49	—	59	
f_{MAX}	Maximum Clock Frequency	2.0		4	8	—	3	—	3	—	MHz
		4.5		20	33	—	16	—	13	—	
		6.0		24	39	—	19	—	15	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
$t_{W(L)}$	Minimum Pulse Width $\overline{CLEAR}$	2.0		—	50	100	—	125	—	150	ns
		4.5		—	12	20	—	25	—	30	
		6.0		—	10	17	—	21	—	26	
t_s	Minimum Set-up Time (SL, SR, A to H)	2.0		—	25	75	—	95	—	110	ns
		4.5		—	6	15	—	19	—	22	
		6.0		—	5	13	—	16	—	19	
t_s	Minimum Set-up Time (S0, S1)	2.0		—	50	125	—	155	—	190	ns
		4.5		—	13	25	—	31	—	38	
		6.0		—	11	21	—	26	—	32	
t_s	Minimum Set-up Time ($\overline{CLEAR}$) (2)	2.0		—	32	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_h	Minimum Hold Time (SL, SR, A to H)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_h	Minimum Hold Time (S0, S1)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	

(1) Apply to M54/74HC299
(2) Apply to M54/74HC323

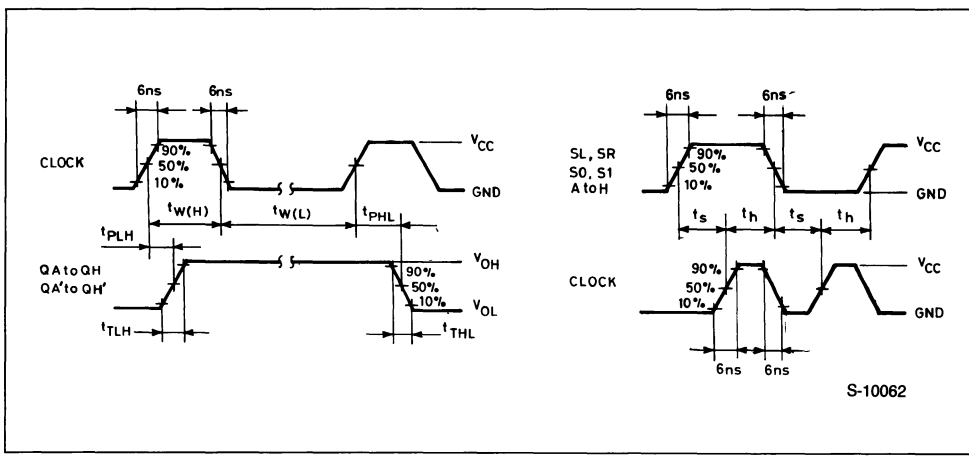
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_h	Minimum Hold Time ($\overline{CLEAR}$) (2)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{REM}	Minimum Removal Time ($\overline{CLEAR}$) (1)	2.0		—	—	25	—	30	—	40	ns
		4.5		—	—	5	—	6	—	8	
		6.0		—	—	5	—	6	—	7	
t_{PZL} t_{PZH}	3-State Output Enable Time	2.0		—	100	195	—	245	—	295	ns
		4.5	$R_L = 1k\Omega$	—	25	39	—	49	—	59	
		6.0		—	21	33	—	42	—	50	
t_{PLZ} t_{PHZ}	3-State Output Disable Time	2.0		—	112	200	—	250	—	300	ns
		4.5	$R_L = 1k\Omega$	—	28	40	—	50	—	60	
		6.0		—	24	34	—	43	—	51	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{OUT}	Output Capacitance (QA to QH)			—	13	—	—	—	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance			—	221	—	—	—	—	—	pF

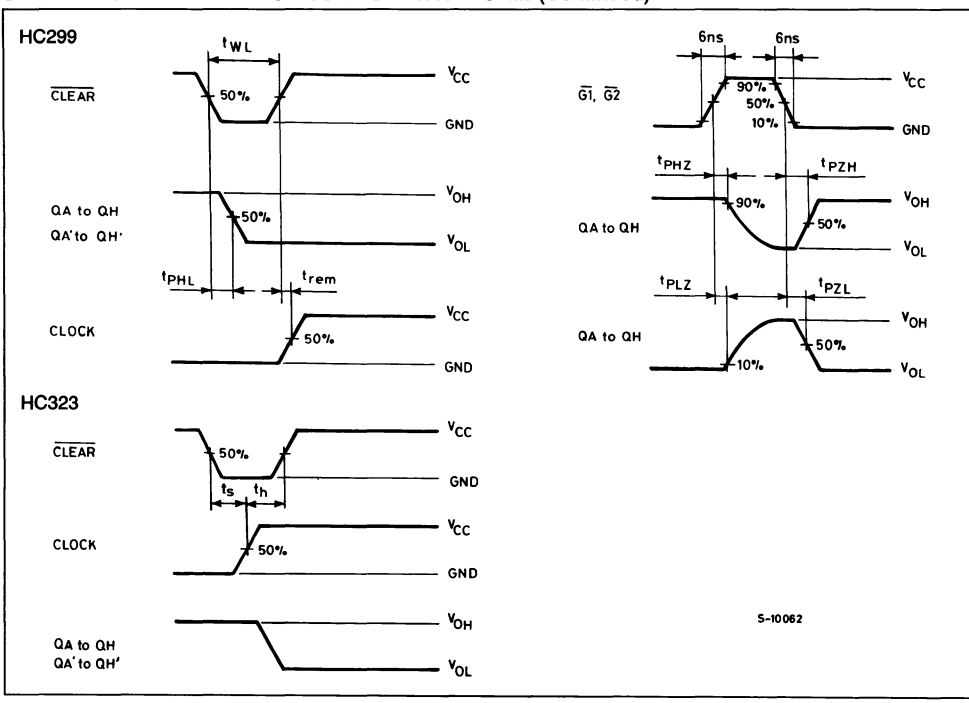
Note (*) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test circuit).
Average opeating current can be obtained from the equation:
$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

(1) Apply to M54/74HC299
(2) Apply to M54/74HC323

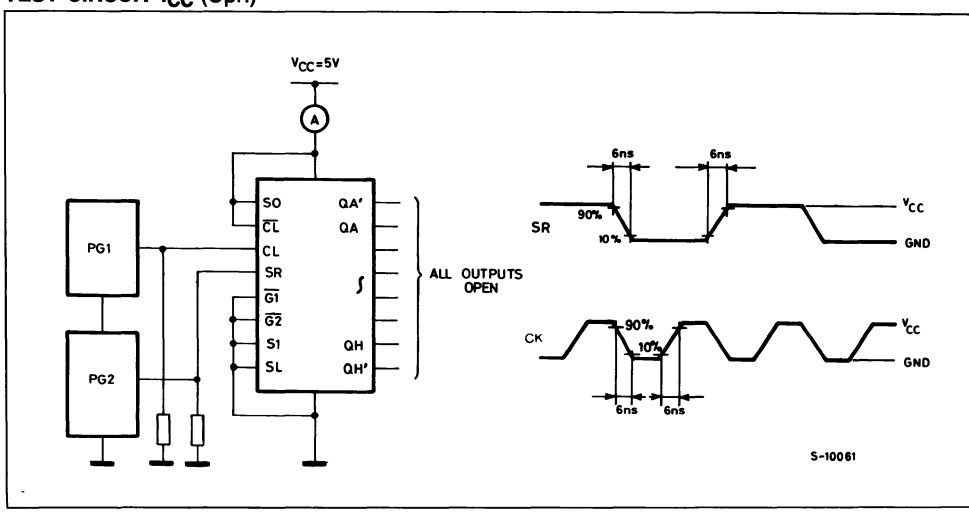
SWITCHING CHARACTERISTICS TEST WAVEFORM



SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)

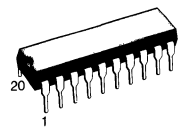


TEST CIRCUIT I_{CC} (Opr.)

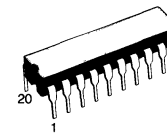


8-CHANNEL MULTIPLEXER/REGISTER (3-STATE)

- HIGH SPEED
  t_{PD} = 33 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN).
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS354



B1N
Plastic Package



F1
Ceramic Frit Seal Package

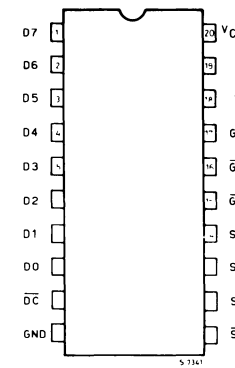
M1
Micro Package

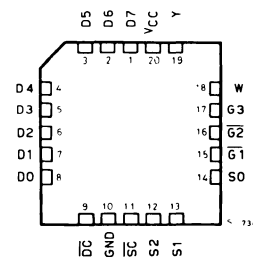
C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC354 F1
M74HC354 B1N
M74HC354 F1
M74HC354 C1
M74HC354 M1

PIN CONNECTIONS (top view)



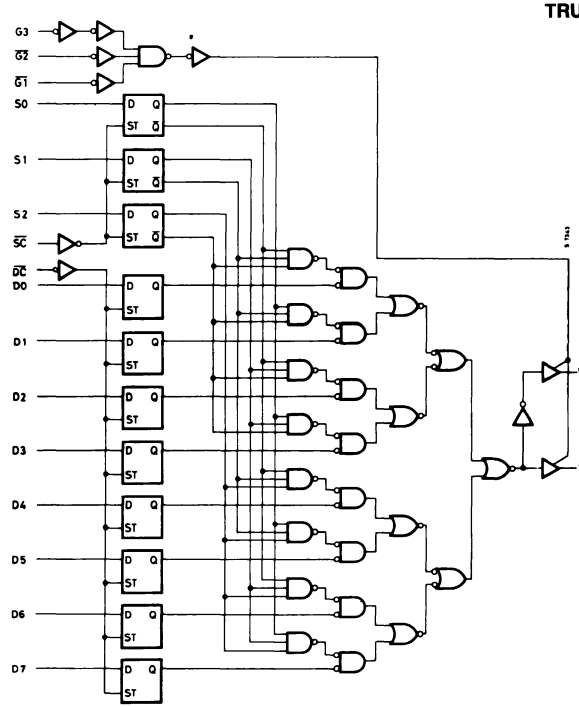


NC = No Internal Connection

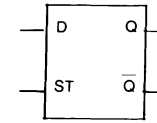
DESCRIPTION

The M54/74HC354 is a high speed CMOS 8-CHANNEL MULTIPLEXER/REGISTER (3-state) fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low consumption.
This device contains an 8 channel digital multiplexer with an 8-bit input data register and a 3-bit address input register with 3-state outputs. The one of eight input data will be provided on the Y output pin (non-inverted output) and W output pin (inverted output) determined by the address data.
The information at the data inputs (D0 to D7) is stored in the 8-bit latch at the negative pulse on $\overline{DC}$ input. The information at the address inputs (S0 to S2) is stored in the 3-bit latch at the negative pulse on $\overline{SC}$ input. These outputs are disabled to be high-impedance when input $\overline{G1}$ is held high, input $\overline{G2}$ is held high or input G3 is held low. This device is suitable for interfacing with bus lines in a bus organized system.
The M54/74HC354 is similar in function to the M54/74HC356, which has an 8-bit flip-flop as the data register instead of an 8-bit latch. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

LOGIC DIAGRAM



TRUTH TABLE OF INTERNAL LATCH



INPUTS		OUTPUTS	
D	ST	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Qn	$\overline{Qn}$

X: DON'T CARE
Qn: DATA STORED AT THE TRAILING EDGE OF THE MOST RECENT ST PULSE

TRUTH TABLE

INPUTS							OUTPUTS	
SELECT*			$\overline{DC}$	OUTPUT ENABLES				
S2	S1	S0		$\overline{G1}$	$\overline{G2}$	G3	W	Y
X X X	X X X	X X X	X X X	H X X	X H X	X X L	Z Z Z	Z Z Z
L	L	L	L	L	L	H	$\overline{D0}$	D0
L	L	L	H	L	L	H	$\overline{D0n}$	D0n
L	L	H	L	L	L	H	$\overline{D1}$	D1
L	L	H	H	L	L	H	$\overline{D1n}$	D1n
L	H	L	L	L	L	H	$\overline{D2}$	D2
L	H	L	H	L	L	H	$\overline{D2n}$	D2n
L	H	H	L	L	L	H	$\overline{D3}$	D3
L	H	H	H	L	L	H	$\overline{D3n}$	D3n
H	L	L	L	L	L	H	$\overline{D4}$	D4
H	L	L	H	L	L	H	$\overline{D4n}$	D4n
H	L	H	L	L	L	H	$\overline{D5}$	D5
H	L	H	H	L	L	H	$\overline{D5n}$	D5n
H	H	L	L	L	L	H	$\overline{D6}$	D6
H	H	L	H	L	L	H	$\overline{D6n}$	D6n
H	H	H	L	L	L	H	$\overline{D7}$	D7
H	H	H	H	L	L	H	$\overline{D7n}$	D7n

X: DON'T CARE - Z: HIGH IMPEDANCE *: THIS COLUMN SHOWS THE INPUT ADDRESS SETUP WITH $\overline{SC}$ LOW.
D0n.....D7n: THE LEVEL OF STEADY-STATE INPUTS AT INPUT D0 THROUGH D7, RESPECTIVELY, BEFORE THE MOST RECENT OF THE LOW-TO-HIGH TRANSITION OF DATA CONTROL.

ABSOLUTE MAXIMUM RATINGS

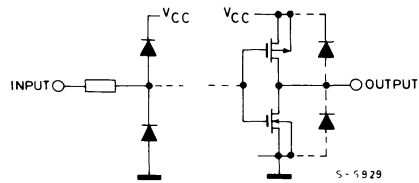
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V V_{CC} 4.5V V_{CC} 6 V	0 to 1000 0 to 500 0 to 400		ns

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0 4.5 6.0	V_I V_{IH} or V_{IL}	I_O −20 μA	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	1.9 4.4 5.9	— — —	V
		4.5 6.0		−6.0 mA −7.8 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	
V_{OL}	Low Level Output Voltage	2.0 4.5 6.0	V_{IH} or V_{IL}	20 μA	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
		4.5 6.0		6.0 mA 7.8 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{OZ}	3 State Output Off-State Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	±0.5	—	±5		±10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

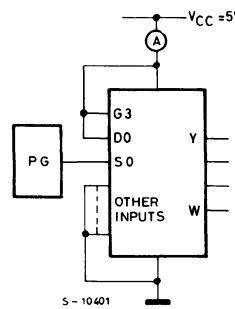
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	25 7 6	60 12 10	— — —	75 15 13		90 18 15	ns
t_{PLH} t_{PHL}	Propagation Delay Time (Dn - Y, W)	2.0 4.5 6.0		— — —	135 34 29	260 52 44	— — —	325 65 55		390 78 66	ns
t_{PLH} t_{PHL}	Propagation Delay Time (DC - Y, W)	2.0 4.5 6.0		— — —	135 34 29	265 53 45	— — —	335 66 56		400 80 68	ns
t_{PLH} t_{PHL}	Propagation Delay Time (Sn-Y, W)	2.0 4.5 6.0		— — —	160 40 34	285 57 48	— — —	355 71 60		430 86 73	ns
t_{PLH} t_{PHL}	Propagation Delay Time (SC-Y,N)	2.0 4.5 6.0		— — —	160 40 34	295 59 50	— — —	370 74 63		445 89 76	ns
$t_{W(L)}$	Minimum Pulse Width (DC)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$t_{W(L)}$	Minimum Pulse Width (SC)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t_s	Minimum Set-up Time (Sn)	2.0 4.5 6.0		— — —	20 5 4	75 15 13	— — —	95 19 16		110 22 19	ns
t_s	Minimum Set-up Time (Dn)	2.0 4.5 6.0		— — —	25 5 4	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_h	Minimum Hold Time (Sn)	2.0 4.5 6.0		— — —	— — —	5 5 5	— — —	5 5 5	 —	5 5 5	ns
t_h	Minimum Hold Time (Dn)	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
t_{PZL} t_{PZH}	Output Enable Time	2.0 4.5 6.0	 $R_L = 1k\Omega$	— — —	68 17 15	125 25 21	— — —	155 31 26		190 38 32	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0 4.5 6.0	 $R_L = 1k\Omega$	— — —	60 22 20	155 31 26	— — —	195 39 33		235 47 40	ns
C_{IN}	Input Capacitance			—	5	10	—	10		10	
C_{OUT}	Output Capacitance			—	10	—	—	—			pF
C_{PD} (*)	Power Dissipation Capacitance			—	84	—	—	—			pF

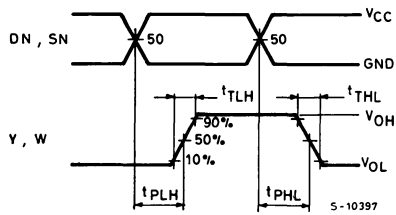
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following equation.
I_{CC} (Opr) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$.

TEST CIRCUIT I_{CC} (Opr.)

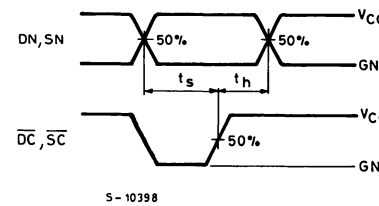


INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

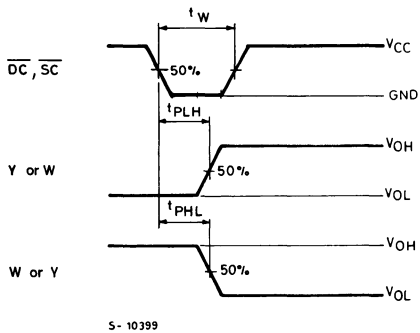
SWITCHING CHARACTERISTICS TEST WAVEFORM



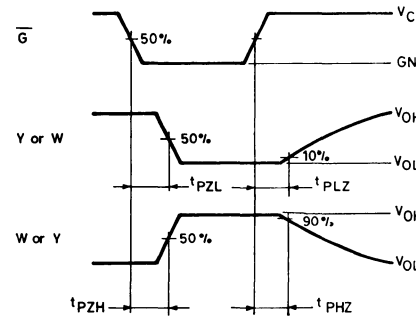
S-10397



S-10398



S-10399



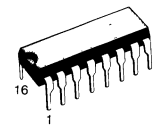
S-10400

SGS-THOMSON MICROELECTRONICS

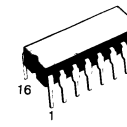
M54HC356
M74HC356

8-CHANNEL MULTIPLEXER/REGISTER WITH LATCHES (3-STATE)

- HIGH SPEED
  t_{PD} = 29 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS356



B1N
Plastic Package



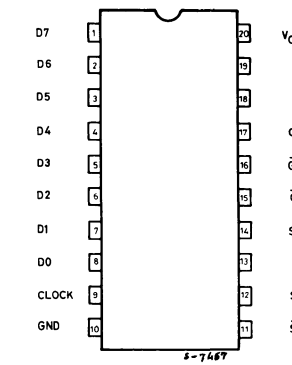
F1
Ceramic Frit Seal Package

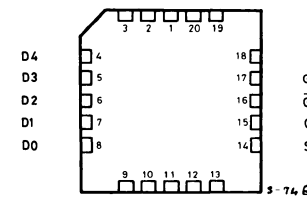
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC356 F1
M74HC356 B1N
M74HC356 F1
M74HC356 C1
M74HC356 M1

PIN CONNECTIONS (top view)





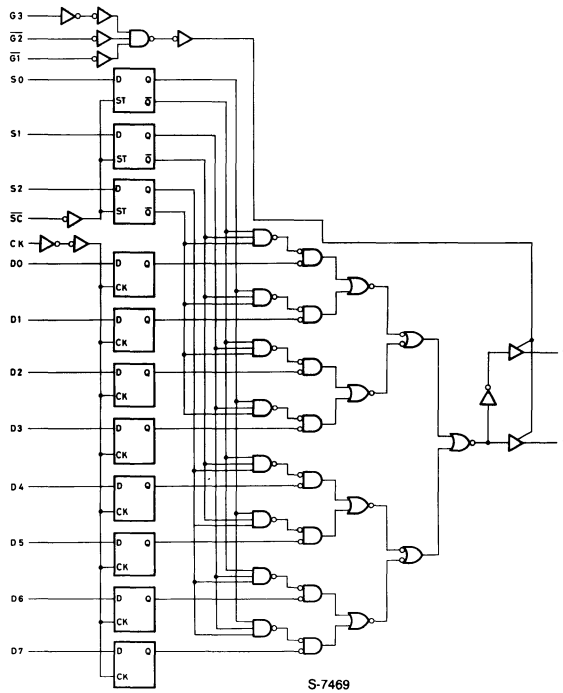
NC =
No Internal
Connection

DESCRIPTION

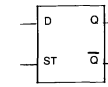
The M54/74HC356 is a high speed CMOS 8-CHANNEL MULTIPLEXER/REGISTER (3-State) fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low consumption.
This device contains an 8 channel digital multiplexer with an 8-bit input data register and a 3-bit address input register with 3-state outputs. The one of eight input data will be provided on the Y output pin (non-inverted output) and W output pin (inverted output) is determineted by the address data.

The information at the data inputs (D0 to D7) is stored in the 8-bit flip-flop at the positive going edge of clock input (CLOCK). The information at the address inputs (S0 to S2) is stored in the 3-bit latch at the negative pulse on $\overline{SC}$ input. These outputs are disabled to be high-impedance when input $\overline{G1}$ is held high, input $\overline{G2}$ is held high or input G3 is held low. This device is suitable for interfacing with bus lines in a bus organized system. The M54/74HC356 is similar in function to the M54/74HC354, which has an 8-bit latch as the data register instead of an 8-bit flip-flop. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

LOGIC DIAGRAM



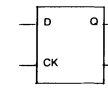
TRUTH TABLE OF INTERNAL LATCH



INPUTS		OUTPUTS	
D	ST	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Qn	$\overline{Qn}$

X: DON'T CARE — Qn: DATA STORED AT THE TRAILING EDGE OF THE MOST RECENT ST PULSE

TRUTH TABLE OF INTERNAL LATCH (FLIP-FLOP)



D	CK	Q
L	↑	L
H	↑	H
X	↓	Qn

X: DON'T CARE
Qn: NO CHANGE

TRUTH TABLE

INPUTS							OUTPUTS	
SELECT*			CLOCK	OUTPUT ENABLES				
S2	S1	S0		$\overline{G1}$	$\overline{G2}$	G3	W	Y
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	↑	L	L	H	$\overline{D0}$	D0
L	L	L	↓	L	L	H	$\overline{D0n}$	D0n
L	L	H	↑	L	L	H	$\overline{D1}$	D1
L	L	H	↓	L	L	H	$\overline{D1n}$	D1n
L	H	L	↑	L	L	H	$\overline{D2}$	D2
L	H	L	↓	L	L	H	$\overline{D2n}$	D2n
L	H	H	↑	L	L	H	$\overline{D3}$	D3
L	H	H	↓	L	L	H	$\overline{D3n}$	D3n
H	L	L	↑	L	L	H	$\overline{D4}$	D4
H	L	L	↓	L	L	H	$\overline{D4n}$	D4n
H	L	H	↑	L	L	H	$\overline{D5}$	D5
H	L	H	↓	L	L	H	$\overline{D5n}$	D5n
H	H	L	↑	L	L	H	$\overline{D6}$	D6
H	H	L	↓	L	L	H	$\overline{D6n}$	D6n
H	H	H	↑	L	L	H	$\overline{D7}$	D7
H	H	H	↓	L	L	H	$\overline{D7n}$	D7n

X: DON'T CARE - Z: HIGH IMPEDANCE *: This column shows the input address setup with SC Low.
D0.....D7: The level of steady-state inputs at input D0 through D7, respectively, at the time of the low-to-high transition of clock

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

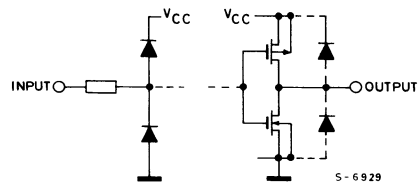
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		7.8		−7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{OZ}	3-State Output Off-State Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	±0.5	—	±5		±10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

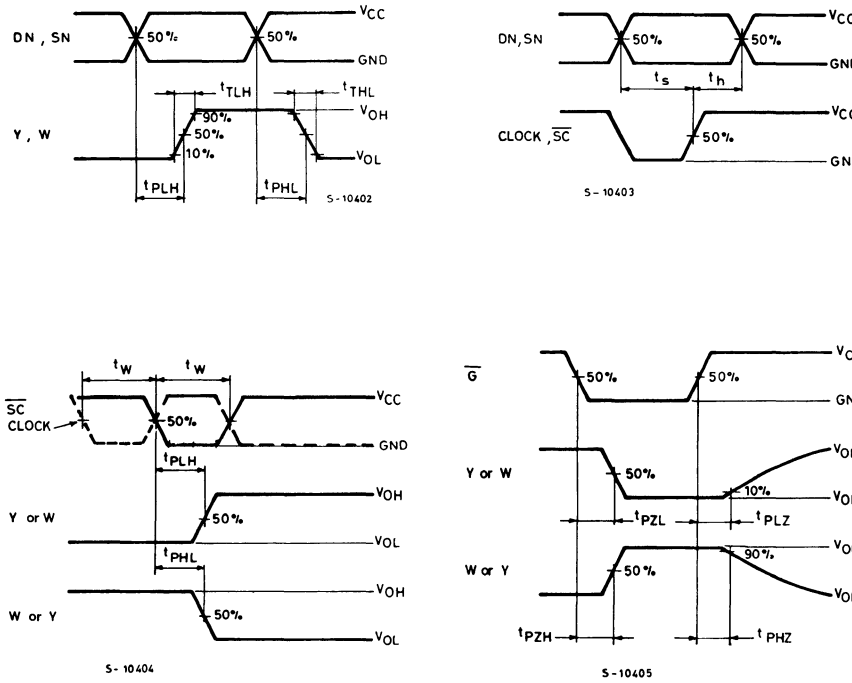
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	25	60	—	75		90	ns
		4.5		—	7	12	—	15		18	
		6.0		—	6	10	—	13		15	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Y, W)	2.0		—	150	265	—	330		400	ns
		4.5		—	36	53	—	66		80	
		6.0		—	31	45	—	56		60	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	160	285	—	355		430	ns
		4.5		—	40	57	—	71		86	
		6.0		—	34	48	—	60		73	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{SC}$ - Y, W)	2.0		—	160	295	—	370		445	ns
		4.5		—	40	59	—	74		89	
		6.0		—	34	50	—	63		76	
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{SC}$)	2.0		—	30	75	—	95		110	
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_s	Minimum Set-up Time (Sn)	2.0		—	25	75	—	95		110	
		4.5		—	5	15	—	19		22	
		6.0		—	4	13	—	16		19	
t_s	Minimum Set-up Time (Dn)	2.0		—	40	75	—	95	—	110	
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_h	Minimum Hold Time (Sn)	2.0		—	—	5	—	5	—	5	
		4.5		—	—	5	—	5	—	5	
		6.0		—	—	5	—	5	—	5	
t_h	Minimum Hold Time (Dn)	2.0		—	—	0	—	0	—	0	
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{PZL} t_{PZH}	Output Enable Time	2.0		—	68	125	—	155	—	190	
		4.5		—	17	25	—	31	—	38	
		6.0	R_L = 1KΩ	—	15	21	—	26	—	22	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0		—	60	155	—	195	—	235	
		4.5		—	22	31	—	39	—	47	
		6.0	R_L = 1KΩ	—	20	26	—	33		40	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{OUT}	Output Capacitance			—	10	—	—	—			
C_{PD} (*)	Power Dissipation Capacitance			—	53	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

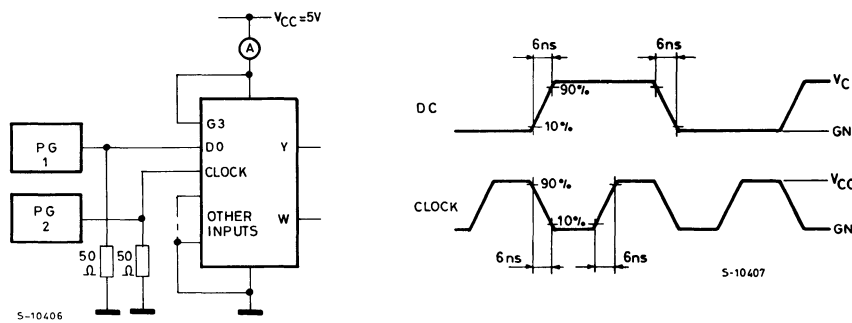
Average operating current can be obtained by the following equation.

$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT WAVEFORM I_{CC} (Opr.)



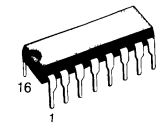
SGS-THOMSON MICROELECTRONICS

M54HC365/366
M74HC365/366

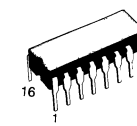
HEX BUS BUFFER (3-STATE)
HC365 NON-INVERTING - HC366 INVERTING

PRELIMINARY DATA

- HIGH SPEED
  t_{PD} = 13 ns (Typ) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS365/366



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
SO Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX C1
M74HCXXX M1

DESCRIPTION

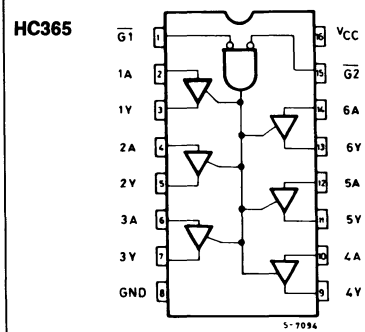
The M54/74HC365 and the M54/74HC366 are high speed CMOS HEX BUS BUFFER fabricated in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption.
All six buffers are controlled by the combination of two enable inputs ($\overline{G1}$ and $\overline{G2}$); all outputs of these buffers are enabled only when both $\overline{G1}$ and $\overline{G2}$ inputs are held low, under all other conditions these output are disabled to be high-impedance.
These outputs are capable of driving up to 15 LSTTL loads. The designer has a choice of non-inverting outputs (HC365) and inverting outputs (HC366). All inputs are equipped with protection circuits against static discharge and transient excess voltage.

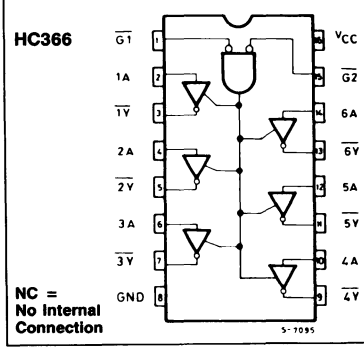
TRUTH TABLE

INPUTS			OUTPUT	
$\overline{G1}$	$\overline{G2}$	An	Yn (365)	$\overline{Yn}$ (366)
L	L	L	L	H
L	L	H	H	L
H	X	X	Z	Z
X	H	X	Z	Z

X: DON'T CARE Z: HIGH IMPEDANCE

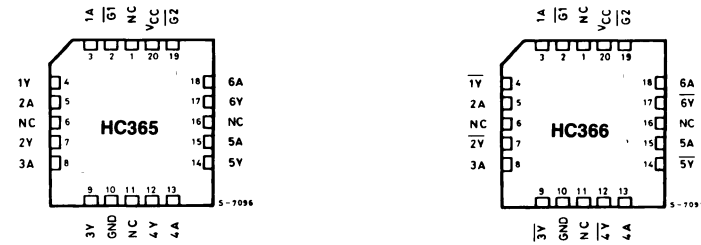
PIN CONNECTION (top view)





NC = No Internal Connection

CHIP CARRIER



NC = No Internal Connection

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

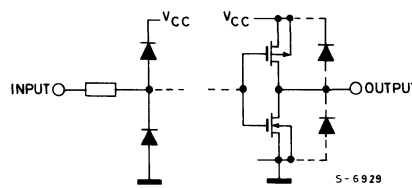
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series Operating Temperature 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{OZ}	3-State Output Off-State Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND $I_O = 0$		—	—	4	—	40	—	80	μA

INPUT AND OUTPUT EQUIVALENT CIRCUIT



AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	25	60	—	75		90	ns
		4.5		—	7	12	—	15		18	
		6.0		—	6	10	—	13		15	
t_{PLH} t_{PHL}	Propagation Delay Time*	2.0		—	60	120	—	150		180	ns
		4.5		—	15	24	—	30		36	
		6.0		—	13	20	—	26		31	
t_{PLH} t_{PHL}	Propagation Delay Time**	2.0		—	56	115	—	145		175	ns
		4.5		—	14	23	—	29		35	
		6.0		—	12	20	—	25		30	
t_{PZL} t_{PZH}	Output Enable Time	2.0		—	76	150	—	190		225	ns
		4.5	$R_L = 1K\Omega$	—	19	30	—	38		45	
		6.0		—	16	26	—	33		38	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0		—	96	175	—	220	—	265	ns
		4.5	$R_L = 1K\Omega$	—	24	35	—	44	—	53	
		6.0		—	20	30	—	37	—	45	
C_{OUT}	Output Capacitance			—	10	—	—	—		10	pF
C_{IN}	Input Capacitance			—	5	10	—	10		10	
C_{PD} (1)	Power Dissipation Capacitance		54/74HC365	—	34	—	—	—			
			54/74HC366		32						

Note (1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

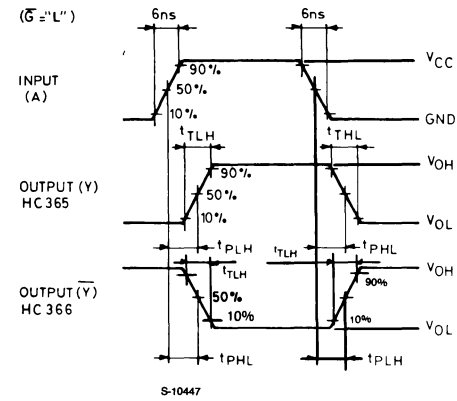
Average operating current can be obtained by the following equation:

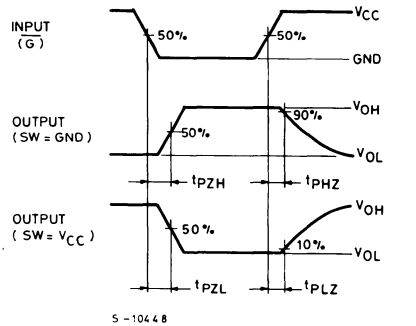
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per Gate)

* M54/74HC365 only

** M54/74HC366 only

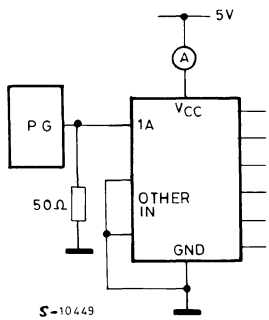
SWITCHING CHARACTERISTICS TEST WAVEFORM





NOTE: SUCH A LOGIC LEVEL SHALL BE APPLIED TO EACH INPUT THAT THE OUTPUT VOLTAGE STAYS IN THE APPOSITE SIDE TO THE SWITCH CONNECTION LEVEL. WHEN THE OUTPUT IS ENABLE.

TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C_{PD} CALCULATION

C_{PD} is to be calculated with the following formula by using the measured value of I_{CC} (Opr.) in the test circuit opposite.

$$C_{PD} = \frac{I_{CC}\ (Opr)}{f_{IN} \cdot V_{CC}}$$

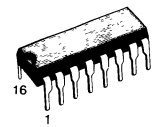
In determining the typical value of C_{PD}, a relatively high frequency of 1MHz was applied to f_{IN}, in order to eliminate any error caused by the quiescent supply current.

SGS-THOMSON MICROELECTRONICS

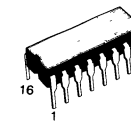
M54HC367/368
M74HC367/368

HEX BUS BUFFER (3-STATE)
HC367 NON-INVERTING, HC368 INVERTING

- HIGH SPEED
  t_{PD} = 13 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C 6V
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN).
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS367/368



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX C1
M74HCXXX M1

DESCRIPTION

The M54/74HC367 and the M54/74HC368 are high speed CMOS HEX BUS BUFFER (3-STATE) fabricated in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. These devices contain six buffers, four buffers are controlled by an enable input ($\overline{G1}$) and the other two buffers are controlled by the other enable input ($\overline{G2}$); the outputs of each buffer group are enabled when $\overline{G1}$ and/or $\overline{G2}$ inputs are held low, and when held high these outputs are disabled to be high-impedance.
These outputs are capable of driving up to 15 LSTTL loads. The designer has a choice of non-inverting outputs (HC367) and inverting outputs (HC368).
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

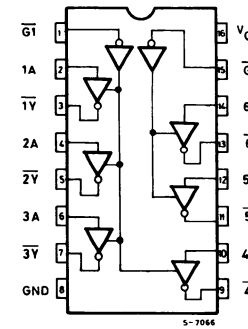
TRUTH TABLE

INPUTS		OUTPUTS	
$\overline{G}$	An	Yn (367)	$\overline{Yn}$ (368)
L	L	L	H
L	H	H	L
H	X	Z	Z

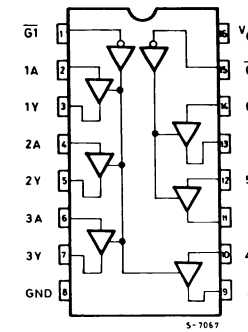
X: DON'T CARE Z: HIGH IMPEDANCE

PIN CONNECTIONS (top view)

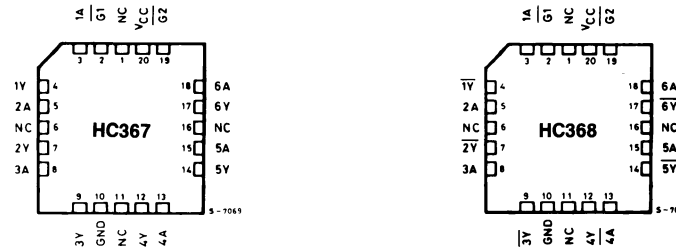
HC367



HC368



CHIP CARRIER



NC = No internal Connection

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

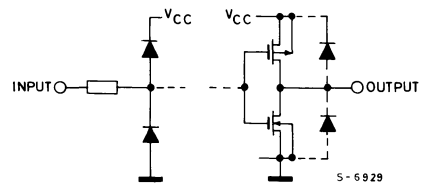
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{OZ}	3-State Output Off-State Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND $I_O = 0$		—	—	4	—	40	—	80	μA

INPUT AND OUTPUT EQUIVALENT CIRCUIT



AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	22	60	—	75	—	90	ns
		4.5		—	8	12	—	15	—	18	
		6.0		—	7	10	—	13	—	15	
t_{PLH} t_{PHL}	Propagation Delay Time *	2.0		—	60	120	—	150	—	180	ns
		4.5		—	15	24	—	30	—	36	
		6.0		—	13	20	—	26	—	31	
t_{PLH} t_{PHL}	Propagation Delay Time **	2.0		—	56	115	—	145	—	175	ns
		4.5		—	14	23	—	29	—	35	
		6.0		—	12	20	—	25	—	30	
t_{PZL} t_{PZH}	Output Enable Time	2.0	R_L = 1KΩ	—	60	120	—	150	—	180	ns
		4.5		—	15	24	—	30	—	36	
		6.0		—	13	20	—	26	—	31	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0	R_L = 1KΩ	—	63	150	—	190	—	225	ns
		4.5		—	20	30	—	38	—	45	
		6.0		—	18	26	—	33	—	38	
C_{IN}	Input Capacitance	—		—	5	10	—	10	—	10	pF
C_{OUT}	Output Capacitance	—		—	10	—	—	—	—	—	
C_{PD} (1)	Power Dissipation Capacitance	—	HC 367	—	34	—	—	—	—	—	pF
		—	HC 368	—	32	—	—	—	—	—	

Note (1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

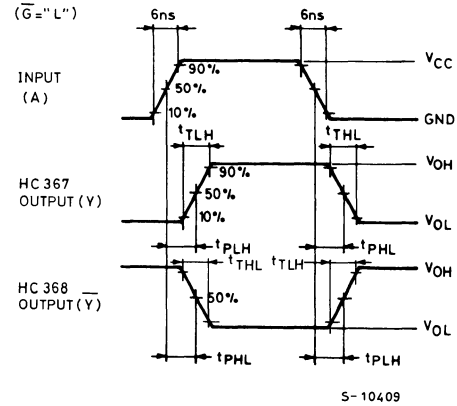
Average operating current can be obtained by the following equation.

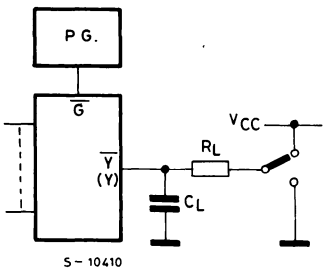
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per circuit).

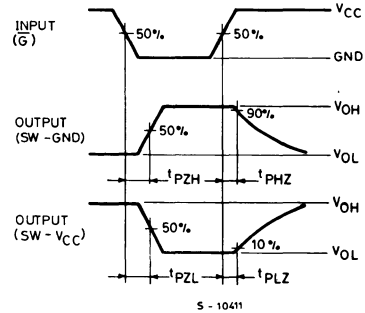
* For M54/74HC367 only

** For M54/74HC368 only

SWITCHING CHARACTERISTICS TEST WAVEFORM

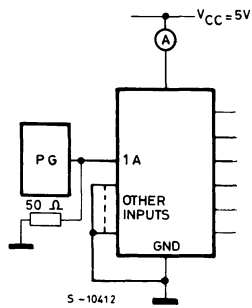






NOTE: SUCH A LOGIC LEVEL SHALL BE APPLIED TO EACH INPUT THAT THE OUTPUT VOLTAGE STAYS IN THE APPOSITE SIDE TO THE SWITCH CONNECTION LEVEL, WHEN THE OUTPUT IS ENABLE

TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

C_{PD} CALCULATION

C_{PD} is to be calculated with the following formula by using the measured value of I_{CC} (Opr.) in the test circuit opposite

$$C_{PD} = \frac{I_{CC}\ (Opr.)}{f_{IN} \cdot V_{CC}}$$

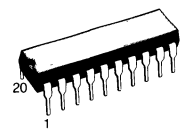
In determining the typical value of C_{PD}, a relatively high frequency of 1 MHz was applied to f_{IN}, in order to eliminate any error caused by the quiescent supply current.

SGS-THOMSON MICROELECTRONICS

M54/74HC373/573
M54/74HC533/563

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT
HC373/573 NON INVERTING, HC533/563 INVERTING

- HIGH SPEED
  t_{PD} = 15 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 74LS373/533/563/573



B1N
Plastic Package

F1
Ceramic Frit Seal Package

M1
Micro Package

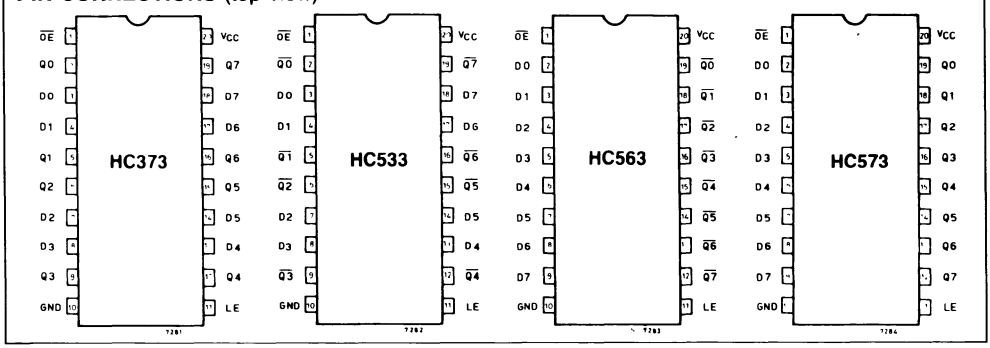
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX C1
M74HCXXX M1

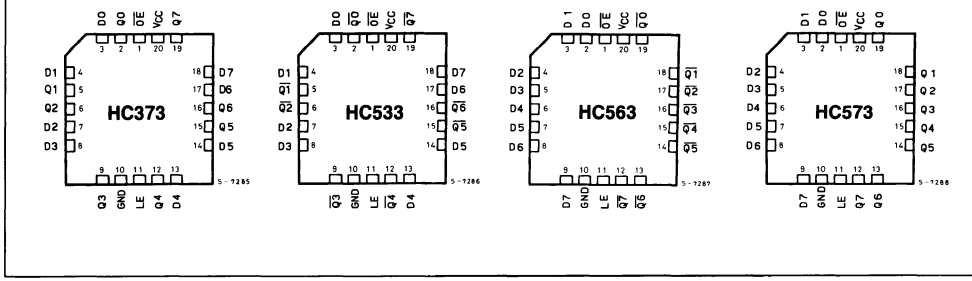
DESCRIPTION

The M54/74HC373, M54/74HC533, M54/74HC563 and M54/74HC573 are high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology.
These ICs achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
These 8-bit D-type latches are controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$). While the LE input is held at a high level, the Q outputs will follow the data input precisely or inversely. When the LE is taken low, the Q outputs will be latched precisely or inversely at the logic level of D input data. While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.
The application designer has a choice of combination of inverting and non-inverting outputs, symmetrical and neighbouring input/output pin layout. The HC373 and the HC573, the HC533 and the HC563 have the same function and the same characteristics respectively, but have different pin layouts. The three-state output configuration and the wide choice of outline make bus-organized systems simple. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

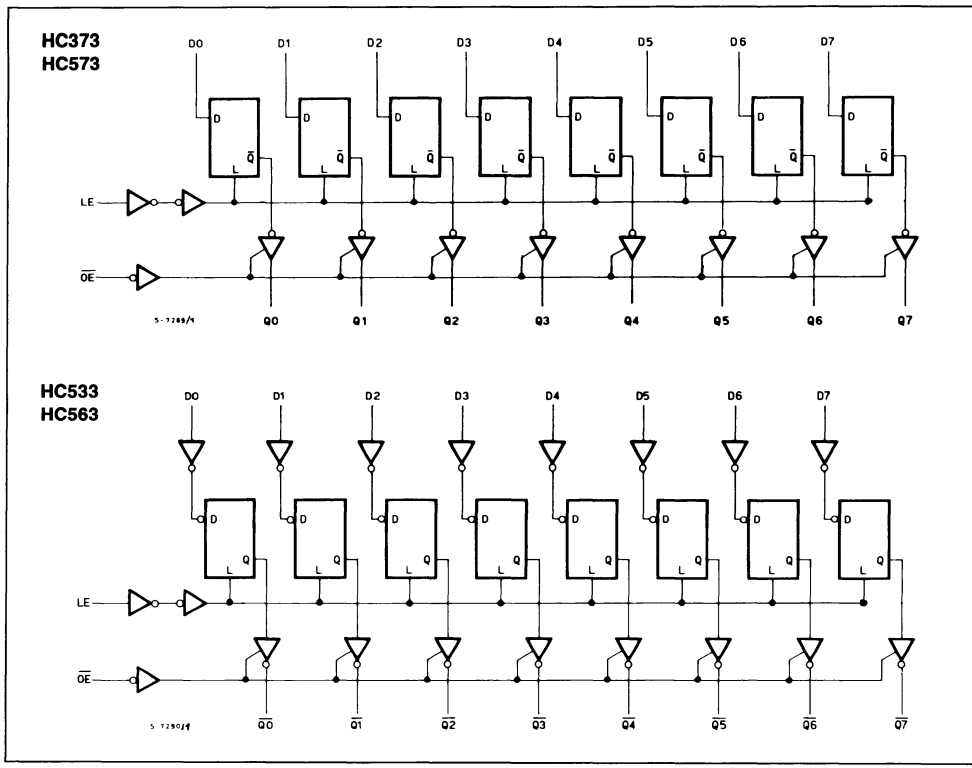
PIN CONNECTIONS (top view)



CHIP CARRIER



LOGIC DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q (HC373) (HC573)	$\overline{Q}$ (HC533) (HC563)
H	X	X	Z	Z
L	L	X	NO CHANGE*	NO CHANGE*
L	H	L	L	H
L	H	H	H	L

X: DON'T CARE Z: HIGH IMPEDANCE

*: Q/$\overline{Q}$ OUTPUTS ARE LATCHED AT THE TIME WHEN THE LE INPUT IS TAKEN LOW LOGIC LEVEL.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

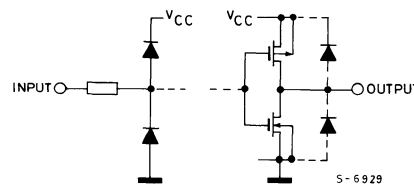
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	4.5 to 5.5		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{OZ}	3-State Output Off-State Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND $I_O = 0$		—	—	4	—	40	—	80	μA

INPUT AND OUTPUT EQUIVALENT CIRCUIT



AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	24	60	—	75	—	90	ns
		4.5		—	8	12	—	15	—	18	
		6.0		—	6	10	—	13	—	15	
t_{PLH} t_{PHL}	Propagation Delay Time (LE - Q, $\overline{Q}$) *	2.0		—	82	175	—	220	—	265	ns
		4.5		—	22	35	—	44	—	53	
		6.0		—	19	30	—	37	—	45	
t_{PLH} t_{PHL}	Propagation Delay Time (LE-Q, $\overline{Q}$) **	2.0		—	75	150	—	190	—	225	ns
		4.5		—	19	30	—	38	—	45	
		6.0		—	16	26	—	33	—	38	
t_{PLH} t_{PHL}	Propagation Delay Time (D-Q, $\overline{Q}$) *	2.0		—	66	145	—	180	—	220	ns
		4.5		—	18	29	—	36	—	44	
		6.0		—	16	25	—	31	—	38	
t_{PLH} t_{PHL}	Propagation Delay Time (D-Q, $\overline{Q}$) **	2.0		—	63	130	—	165	—	195	ns
		4.5		—	16	26	—	33	—	39	
		6.0		—	14	22	—	28	—	33	
$t_{W(H)}$	Minimum Pulse Width (LE)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-up Time	2.0		—	10	50	—	65	—	75	ns
		4.5		—	2	10	—	13	—	15	
		6.0		—	2	9	—	11	—	13	
t_h	Minimum Hold Time	2.0		—	—	50	—	65	—	75	ns
		4.5		—	—	10	—	13	—	15	
		6.0		—	—	9	—	11	—	13	
t_{PZL} t_{PZH}	Output Enable Time *	2.0	R_L = 1KΩ	—	72	150	—	190	—	225	ns
		4.5		—	18	30	—	38	—	45	
		6.0		—	15	26	—	33	—	38	
t_{PZL} t_{PZH}	Output Enable Time **	2.0	R_L = 1KΩ	—	62	140	—	175	—	210	ns
		4.5		—	18	28	—	35	—	42	
		6.0		—	16	24	—	30	—	36	
t_{PZH} t_{PHZ}	Output Disable Time *	2.0	R_L = 1kΩ	—	45	150	—	190	—	225	ns
		4.5		—	22	30	—	38	—	45	
		6.0		—	20	26	—	33	—	37	
t_{PLZ} t_{PHZ}	Output Disable Time **	2.0	R_L = 1KΩ	—	45	150	—	190	—	225	ns
		4.5		—	22	30	—	38	—	45	
		6.0		—	20	26	—	33	—	38	
C_{IN}	Input Capacitance			—	5	10	—	10	—	—	pF
C_{OUT}	Output Capacitance			—	10	—	—	—	—	—	pF
C_{PD} ◆	Power Dissipation Capacitance			—	41	—	—	—	—	—	pF

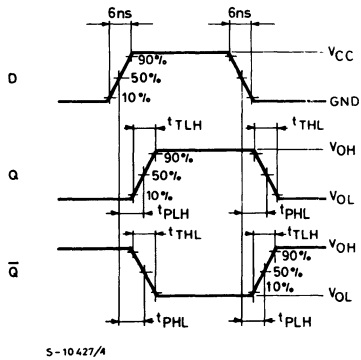
Note ◆ C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

Average operating current can be obtained by the following equation.

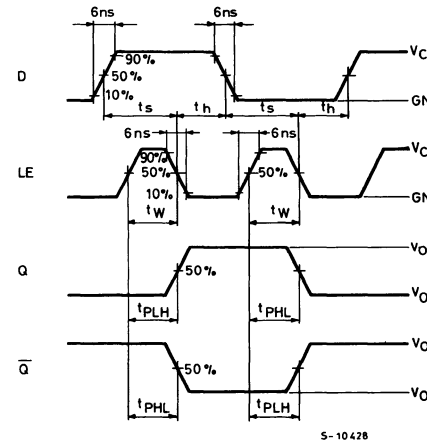
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Latch) * M54/74HC373/533 ** M54/74HC563/573

SWITCHING CHARACTERISTICS TEST WAVEFORM

t_{PLH}, t_{PHL} (D - Q, $\overline{Q}$)



t_{PLH}, t_{PHL} (LE - Q, $\overline{Q}$), t_s, t_h, t_W

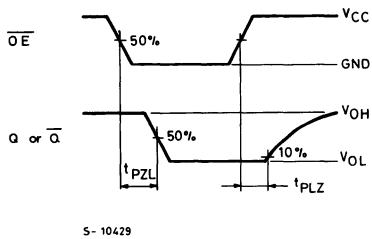


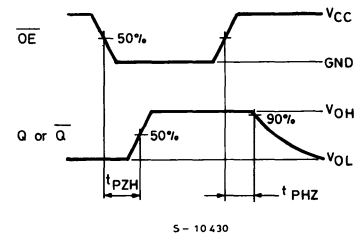
t_{PLZ}, t_{PZL}

The 1KΩ load resistors should be connected between outputs and V_{CC} line and the 50 pF load capacitors should be connected between outputs and GND line. All inputs except $\overline{OE}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{OE}$ in put is held low.

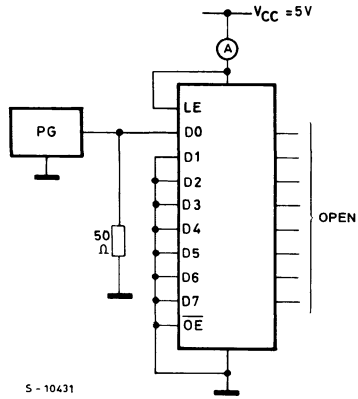
t_{PHZ}, t_{PZH}

The 1KΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while OE input is held low.





TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IN THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

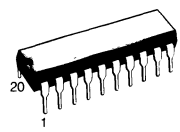
SGS-THOMSON MICROELECTRONICS

M54HCT373
M74HCT373

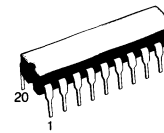
OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

PRODUCT PREVIEW

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2 V (MIN) V_{IL} = 0.8 V (MAX)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS373



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

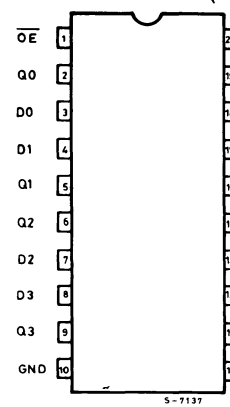
ORDERING NUMBERS:

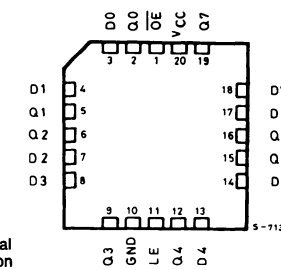
M54HCT373 F1
M74HCT373 B1N
M74HCT373 F1
M74HCT373 C1
M74HCT373 M1

DESCRIPTION

The M54/74HCT373 is a high speed CMOS OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
This 8-bit D-type latch is controlled by a latch enable input (LE) and an output enable input ($\overline{OE}$). While the LE input is held high, the Q outputs will follow the data input precisely. When the LE is taken low, the Q outputs will be latched at the logic level of D input data.
While the $\overline{OE}$ input is low, the eight outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.
The three-state output configuration and the wide choice of outlines makes bus-organized system simple.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.
This integrated circuit has totally compatible, input and output characteristics, with standard 54/74 LSTTL logic families.
M54HCT/74HCT devices are designed to directly interface HSC²MOS systems with TTL and NMOS components. These devices are also plug in replacements for LSTTL devices giving a reduction in power consumption.

PIN CONNECTIONS (top view)





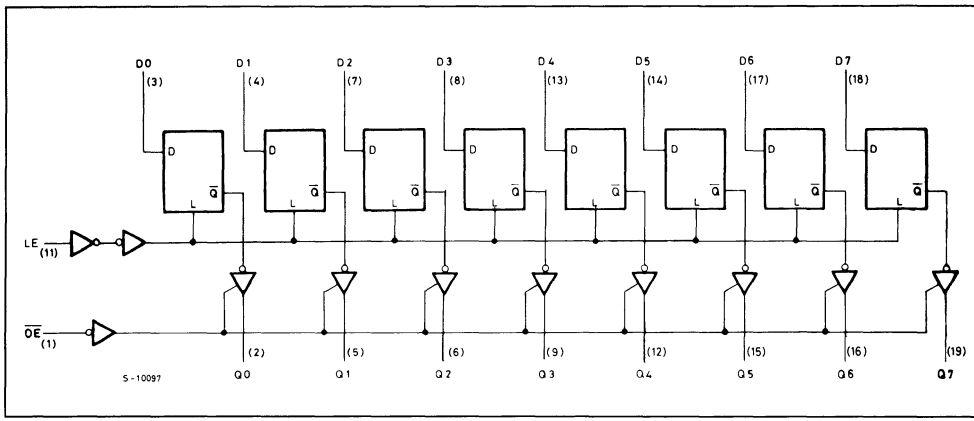
NC = No Internal Connection

TRUTH TABLE

INPUTS			OUTPUTS
$\overline{OE}$	LE	D	Q (HCT373)
H	X	X	Z
L	L	X	No change•
L	H	L	L
L	H	H	H

X: DON'T CARE
Z: HIGH IMPEDANCE
•: Q OUTPUT WAS LATCHED AT THE TIME WHEN THE LE INPUT IS TAKEN LOW LOGIC LEVEL.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time	0 to 500	ns

DC SPECIFICATIONS

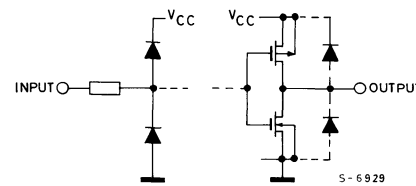
Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0	—	—	2.0	—	2.0	—	V
V_{IL}	Low Level Input Voltage	4.5 to 5.5			—	—	0.8	—	0.8	—	0.8	V
V_{OH}	High Level Output Voltage	4.5	V_{IN}	I_{OH}								V
			V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
				−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
V_{OL}	Low Level Output Voltage	4.5	V_{IN}	I_{OL}								V
			V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	
				6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
I_{OZ}	3-State Output Off-State Current	5.5	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		—	—	±0.5	—	±5.0	—	±10.0	
I_{IN}	Input Leakage Current	5.5	V_{IN} = V_{CC} or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND		—	—	4	—	40	—	80	μA
I_{CC}			Per input: V_{IN} = 0.5V or 2.4V Other input: V_{CC} or GND		—	—	2.0	—	2.9	—	3.0	mA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			-40 to $85°C$ 74HC		-55 to $125°C$ 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5		—	7	12	—	15	—	19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (LE-Q)	4.5		—	23	35	—	44	—	53	ns
t_{PLH} t_{PHL}	Propagation Delay Time (D-Q)	4.5		—	23	35	—	44	—	53	ns
$t_{W(H)}$	Minimum Pulse Width (LE)	4.5		—	8	15	—	19	—	22	ns
t_s	Minimum Set-up Time	4.5		—	0	5	—	6	—	8	ns
t_h	Minimum hold Time	4.5		—	3	10	—	13	—	15	ns
t_{PZH} t_{PZL}	3-State Output Enable Time	4.5	$R_L = 1k\Omega$	—	23	35	—	44	—	53	ns
t_{PLZ} t_{PHZ}	3-State Output Disable Time	4.5	$R_L = 1k\Omega$	—	21	30	—	38	—	45	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{OUT}	Output Capacitance			—	10	—	—	—	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance			—	55	—	—	—	—	—	pF

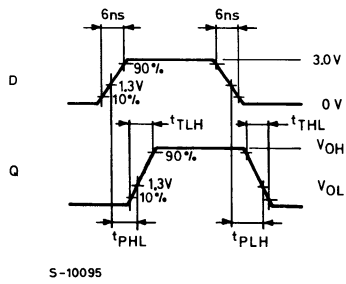
Note (*) C_{PD} is defined as the value of IC's internal equivalent capacitance which is calculated from the operating current consumption without load (refer to Test Circuit).
Average opeating current is: $I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Latch)

INPUT AND OUTPUT EQUIVALENT CIRCUIT

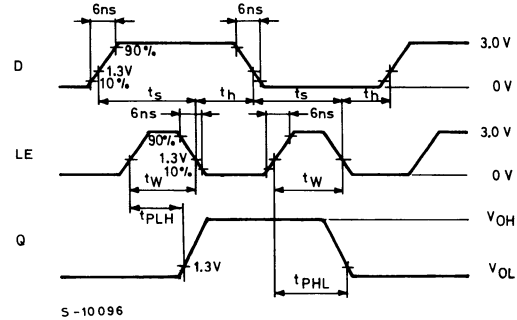


SWITCHING CHARACTERISTICS TEST WAVEFORM

t_{PLH}, t_{PHL} (D-Q)



t_{PLH}, t_{PHL} (LE-Q) t_s, t_h, t_W

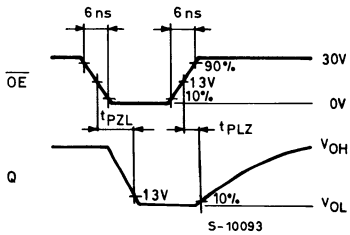


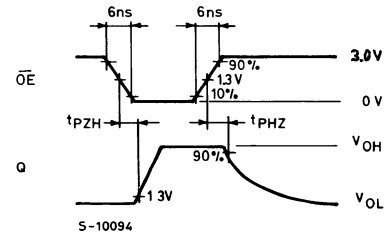
t_{PLZ}, t_{PZL}

The 1KΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line. All inputs except $\overline{OE}$ input should be connected to V_{CC} line to GND line such that outputs will be in low logic level while $\overline{OE}$ input is held low.

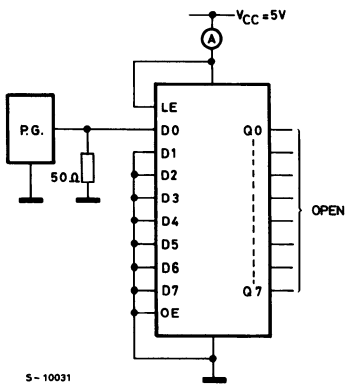
t_{PHZ}, t_{PHL}

The 1KΩ load resistors and the 50pF load capacitors should be connected between each outputs and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ input is held low.

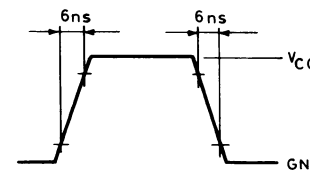




TEST CIRCUIT I_{CC} (Opr.)



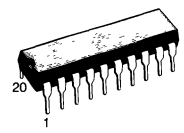
INPUT WAVEFORM



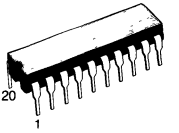
OCTAL D-TYPE FLIP FLOP WITH 3-STATE OUTPUT
HC534/HC564 INVERTING - HC374/HC574 NON-INVERTING

PRELIMINARY DATA

- HIGH SPEED
  f_{MAX} = 55 MHz (Typ) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS374/534/564/574



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

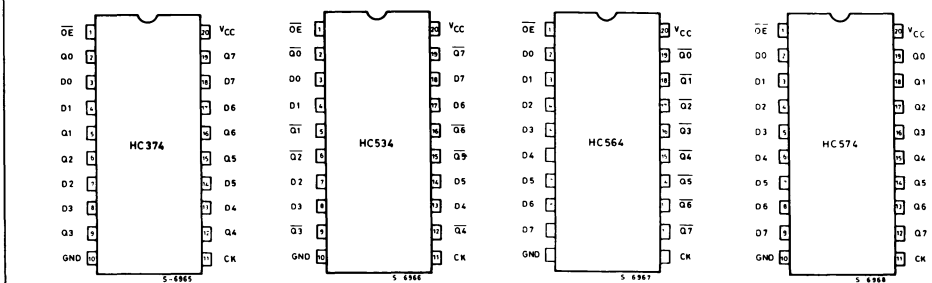
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX C1
M74HCXXX M1

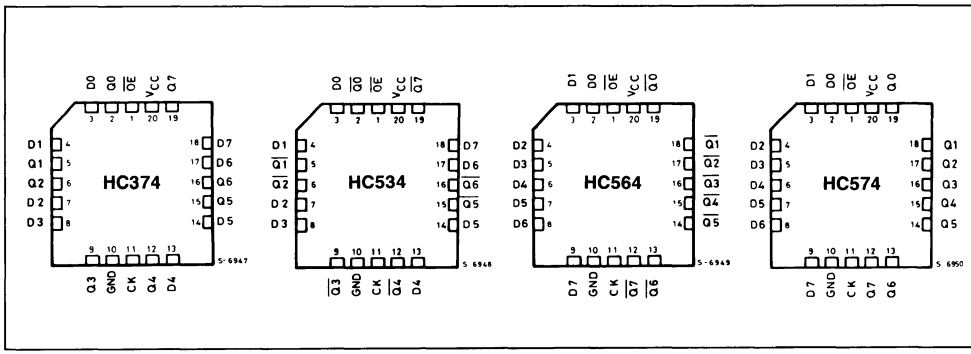
DESCRIPTION

The M54/74HC374, M54/74HC534, M54/74HC564 and M54/74HC574 are high speed CMOS OCTAL D-TYPE FLIP FLOP WITH 3-STATE OUTPUTS fabricated with in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. These 8-bit D-type flip-flops are controlled by a clock input (CK) and an output enable input ($\overline{OE}$). On the positive transition of the clock, the Q outputs will be set to the logic state that were setup at the D inputs (HC374 and HC574) or their complements (HC534 and HC564)
While the $\overline{OE}$ input is low, the eight outputs will be in a normal logic state (high or low logic level), and while high level, the outputs will be in a high impedance state. The output control does not affect the internal operation of flip-flops. That is, the old data can be retained or the new data can be entered even while the outputs are off. The application engineer has a choice of combination of inverting and non-inverting outputs, symmetrical and neighbouring input/output pin layout. The HC374 and HC574 are identical, apart from pin layout as are the HC534 and HC564. The 3-state output configuration and the wide choice of outline make bus-organized systems simple. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION (top view)



CHIP CARRIER



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

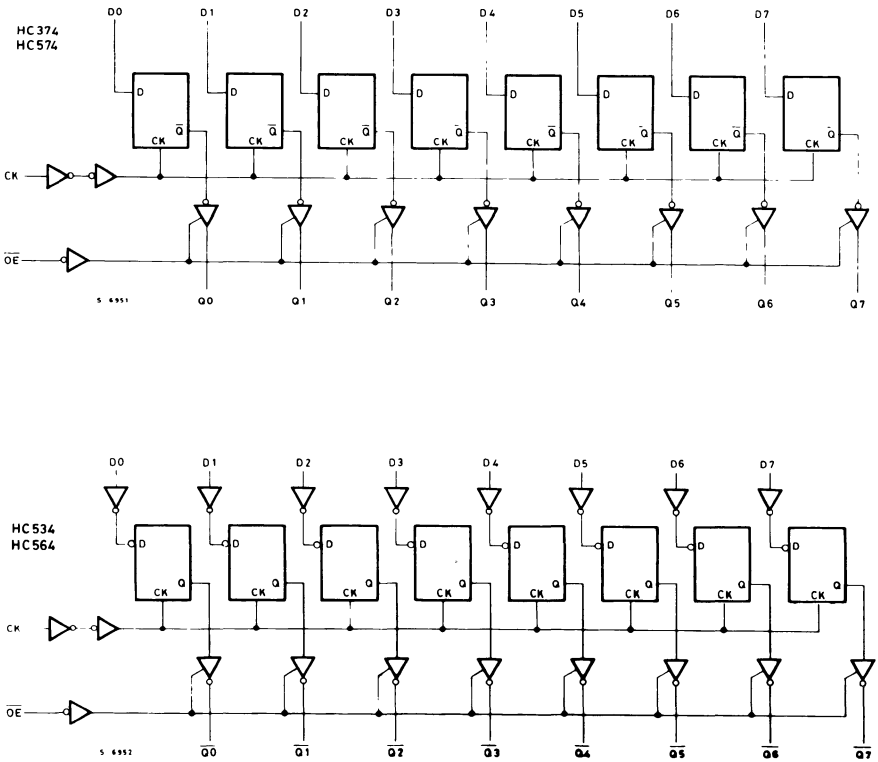
Symbol	Parameter		Limit		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000		ns
		V_{CC} = 4.5V	0 to 500		
		V_{CC} = 6 V	0 to 400		

TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q (HC374, HC574)	$\overline{Q}$ (HC534, HC564)
H	X	X	Z	Z
L	↓	X	NO CHANGE	NO CHANGE
L	↑	L	L	H
L	↑	H	H	L

X: DON'T CARE Z: HIGH IMPEDANCE

LOGIC DIAGRAM



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{OZ}	3-State Output Off-State Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND $I_O = 0$		—	—	4.0	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	24	60	—	75		90	ns
		4.5		—	8	12	—	15		18	
		6.0		—	6	10	—	13		15	
t_{PLH} t_{PHL}	Propagation Delay Time* (CK - Q, $\overline{Q}$)	2.0		—	88	175	—	220		265	ns
		4.5		—	22	35	—	44		53	
		6.0		—	19	30	—	37		44	
t_{PLH} t_{PHL}	Propagation Delay Time** (CK - Q, $\overline{Q}$)	2.0		—	76	150	—	190		225	ns
		4.5		—	19	30	—	38		45	
		6.0		—	16	26	—	33		38	
f_{MAX}	Maximum Clock Frequency	2.0		6	12	—	5	—	4	—	MHz
		4.5		30	50	—	24	—	20	—	
		6.0		35	59	—	28	—	24	—	

AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CK)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t_s	Minimum Set-up Time*	2.0 4.5 6.0		— — —	40 10 9	100 20 17	— — —	125 25 21		150 30 26	ns
t_s	Minimum Set-up Time**	2.0 4.5 6.0		— — —	30 8 7	79 15 13	— — —	95 19 16		110 22 19	ns
t_h	Minimum Hold Time*	2.0 4.5 6.0		— — —	— — —	5 5 5	— — —	5 5 5	— — —	5 5 5	ns
t_h	Minimum Hold Time**	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
t_{PZL} t_{PZH}	Output Enable Time*	2.0 4.5 6.0	$R_L = 1K\Omega$	— — —	72 18 15	150 30 26	— — —	190 38 33	— — —	225 45 38	ns
t_{PZL} t_{PZH}	Output Enable Time**	2.0 4.5 6.0	$R_L = 1K\Omega$	— — —	64 16 14	140 28 24	— — —	175 35 30	— — —	210 42 36	ns
t_{PZL} t_{PZH}	Output Disable Time*	2.0 4.5 6.0	$R_L = 1K\Omega$	— — —	84 21 18	150 30 26	— — —	190 38 33	— — —	225 45 38	ns
t_{PZL} t_{PZH}	Output Disable Time**	2.0 4.5 6.0	$R_L = 1K\Omega$	— — —	84 21 18	150 30 26	— — —	190 38 33	— — —	225 45 38	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (1)	Power Dissipation Capacitance			—	51	—	—	—	—	—	pF

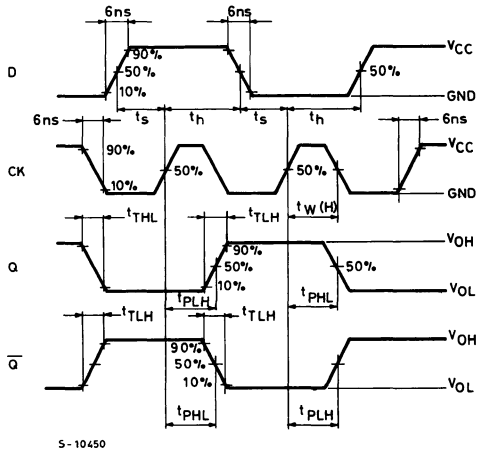
Note (1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

Average operating current can be obtained by the following equation:
$I_{CC\ (Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Flip-Flop)
And the C_{PD} when N pcs of FLIP-FLOP operate, can be gained by the following equation.
C_{PD} (TOTAL) = 34 + 17 × N [pF]

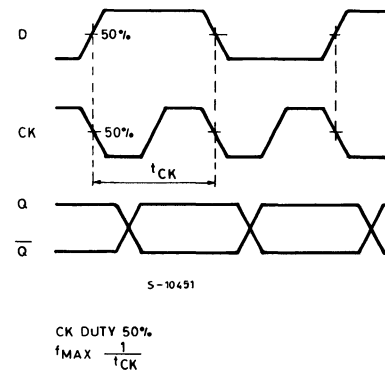
*: for HC374/534
**: for HC564/574

SWITCHING CHARACTERISTICS TEST WAVEFORM

t_{PLH}, t_{PHL}, t_s, t_h, t_w



f_{MAX}



CK DUTY 50%

$f_{MAX} \frac{1}{t_{CK}}$

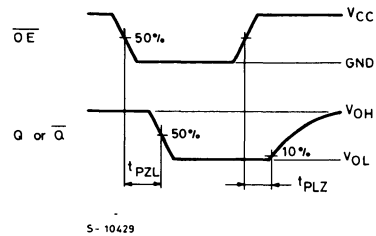
t_{PLZ}, t_{PZL}

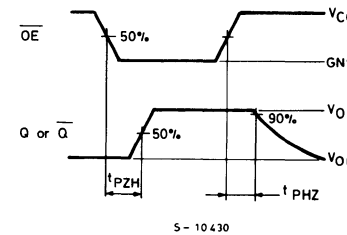
The IKΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line. All inputs except $\overline{OE}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{OE}$ input is held low.

t_{PHZ}, t_{PZH}

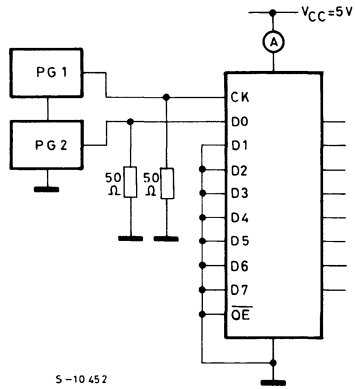
The 1KΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.

All inputs except $\overline{OE}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ input is held low.





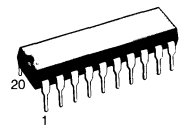
TEST CIRCUIT I_{CC} (Opr.)



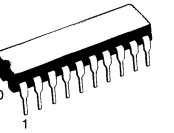
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2 V (MIN) V_{IL} = 0.8 V (MAX.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS374



B1N
Plastic Package



F1
Ceramic Frit Seal Package

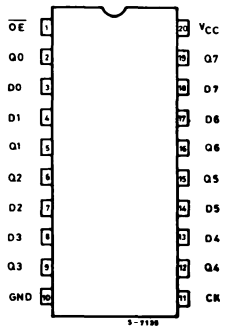
M1
Micro Package

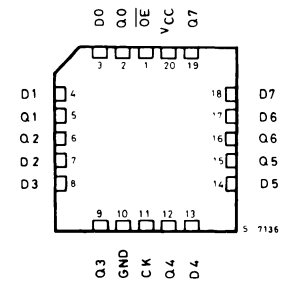
C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HCT374 F1
M74HCT374 B1N
M74HCT374 F1
M74HCT374 C1
M74HCT374 M1

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

DESCRIPTION

The M54/74HCT374 is a high speed CMOS OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This 8-bit D-type flip-flop is controlled by a clock input (CK) and an output enable input ($\overline{OE}$). On the positive transition of the clock, the Q outputs will be set precisely to the logic state that was setup at the D inputs.

While the $\overline{OE}$ input is low, the eight outputs will be in a normal logic state (high or low logic level), and while high, the outputs will be in a high impedance state. The output control does not affect the internal operation of flip-flops. That is, the old data can be retained or the new data can be entered even while the outputs are off.

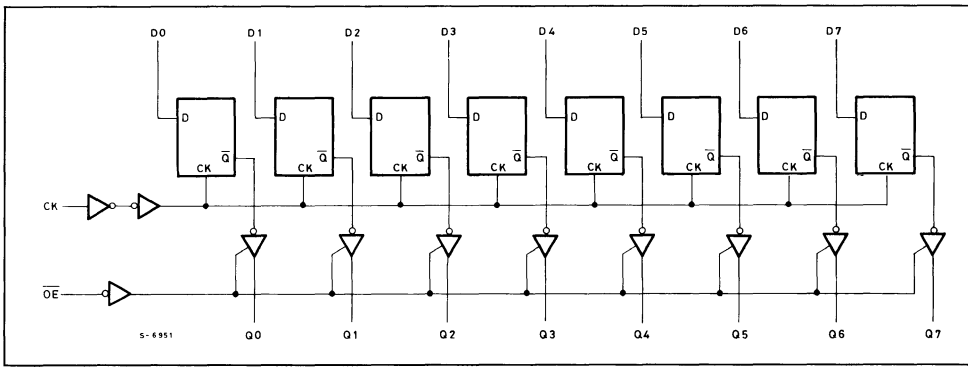
The three-state output configuration and the wide choice of outline will make its application in bus-organized system simple. All inputs are equipped with protection circuits against static discharge and transient excess voltage. This integrated circuit has totally compatibility, input and output characteristic is with standard 54/74 LSTTL logic families.

TRUTH TABLE

INPUTS			OUTPUTS
$\overline{OE}$	CK	D	Q
H	X	X	Z
L	↓	X	NO CHANGE
L	↑	L	L
L	↑	H	H

X: DON'T CARE — Z: HIGH IMPEDANCE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		4.5 to 5.5	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 − 55 to 125	°C
t_r, t_f	Input Rise and Fall Time		0 to 500	ns

DC SPECIFICATIONS

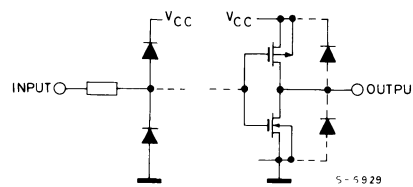
Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			− 40 to 85°C 74HC		− 55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0	—	—	2.0	—	2.0	—	V
V_{IL}	Low Level Input Voltage	4.5 to 5.5			—	—	0.8	—	0.8	—	0.8	V
V_{OH}	High Level Output Voltage	4.5	V_{IN}	I_{OH}								
			V_{IH} or V_{IL}	− 20 μA	4.4	4.5	—	4.4	—	4.4	—	V
				− 6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
V_{OL}	Low Level Output Voltage	4.5	V_{IN}	I_{OL}								
			V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
				6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
I_{OZ}	3-State Output Off-State Current	5.5	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		—	—	±0.5	—	±5.0	—	±10.0	μA
I_{IN}	Input Leakage Current	5.5	V_{IN} = V_{CC} or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND		—	—	4	—	40	—	80	μA
I_{CC}			Per input: V_{IN} = 0.5V or 2.4V Other input: V_{CC} or GND		—	—	2.0	—	2.9	—	3.0	mA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

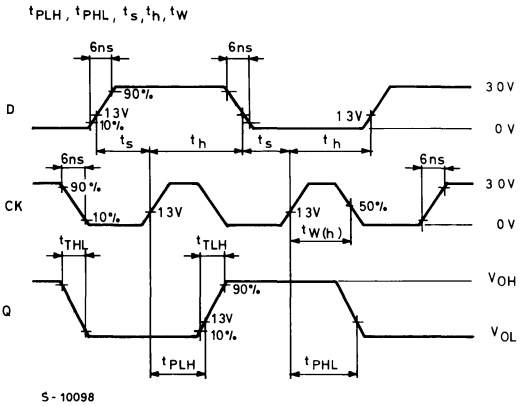
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5		—	7	12	—	15	—	18	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK-Q)	4.5		—	26	40	—	50	—	60	ns
f_{MAX}	Maximum Clock Frequency	4.5		25	38	—	20	—	17	—	MHz
t_W	Minimum Pulse Width	4.5		—	13	25	—	32	—	38	ns
t_s	Minimum Set-up Time	4.5		—	6	15	—	19	—	23	ns
t_h	Minimum hold Time	4.5		—	—	0	—	0	—	0	ns
t_{PZL} t_{PZH}	3-State Output Enable Time	4.5	$R_L = 1k\Omega$	—	27	42	—	53	—	63	ns
t_{PLZ} t_{PHZ}	3-State Output Disable Time	4.5	$R_L = 1k\Omega$	—	22	32	—	40	—	48	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{OUT}	Output Capacitance			—	10	—	—	—	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance			—	60	—	—	—	—	—	pF

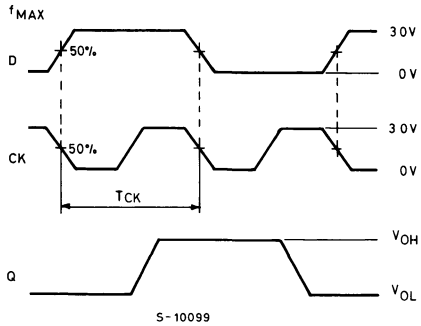
Note (*) C_{PD} is defined as the value of IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average opeating current is: $I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per FLIP/FLOP)
And the C_{PD} when n circuits of FLIP/FLOP operate, can be gained by the following equation. C_{PD} (TOTAL) = 42 + 18•n (pF)

INPUT AND OUTPUT EQUIVALENT CIRCUIT



SWITCHING CHARACTERISTICS TEST WAVEFORM





Duty cycle of CK: 50%

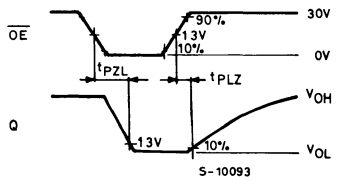
$$f_{MAX} = \frac{1}{T_{CK}}$$

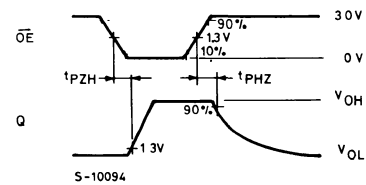
t_{PLZ}, t_{PZL}

The 1KΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line. All inputs except $\overline{OE}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{OE}$ input is held low.

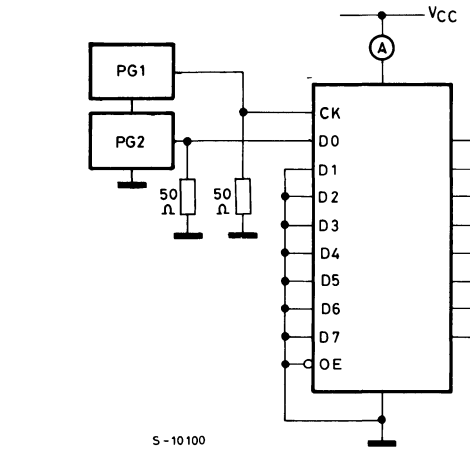
t_{PHZ}, t_{PZH}

The 1KΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ inputs is held low.

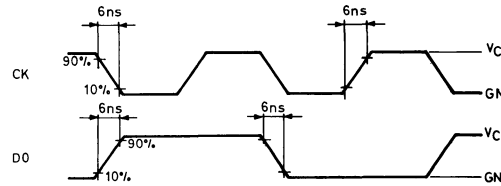




TEST CIRCUIT I_{CC} (Opr.)



S-10100



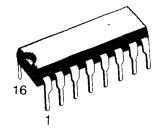
S-10101

SGS-THOMSON MICROELECTRONICS

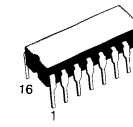
M54HC375
M74HC375

QUAD D TYPE LATCH

- HIGH SPEED
  t_{PD} = 13 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN).
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS375



B1N
Plastic Package



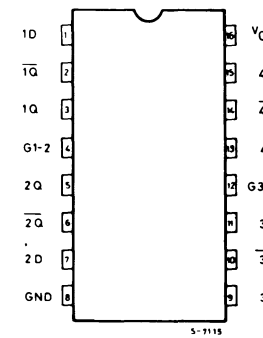
F1
Ceramic Frit Seal Package

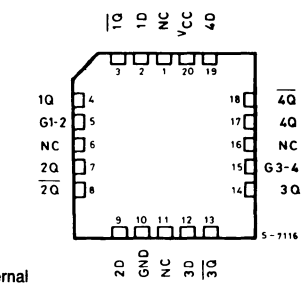
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC375 F1
M74HC375 B1N
M74HC375 F1
M74HC375 C1
M74HC375 M1

PIN CONNECTIONS (top view)





NC = No Internal Connection

DESCRIPTION

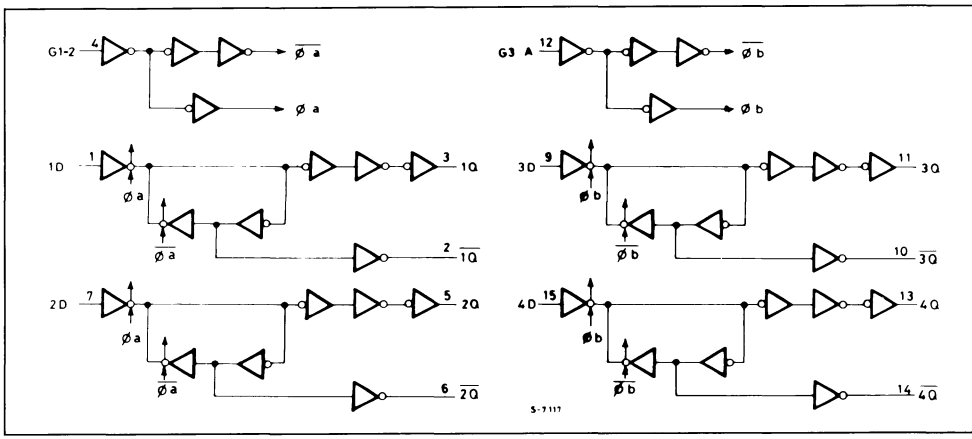
The M54/74HC375 is a high speed CMOS QUAD D TYPE LATCH fabricated in silicon gate C²MOS technology. Is has the same high speed performance of LSTTL combined with true CMOS low power consumption. It contains two groups of 2-bit latches controlled by an enable input (G1·2 or G3·4). These two latch groups can be used in the different circuits. Each latch has Q and $\overline{Q}$ outputs (1Q to 4Q and $1\overline{Q}$ to $4\overline{Q}$). The data applied to the data input is transfered to the Q and $\overline{Q}$ outputs when the enable input is taken high and the outputs will follow the data input as long as the enable input is kept high. When the enable input is taken low, the information data applied to the data input at that time is retained at the outputs.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUTS		OUTPUTS		FUNCTION
D	G	Q	$\overline{Q}$	
L	H	L	H	—
H	H	H	L	—
X	L	Qn	$\overline{Q}$n	LATCH

X: DON'T CARE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V: 0 to 1000 V_{CC} = 4.5V: 0 to 500 V_{CC} = 6 V: 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND		—	—	2	—	20	—	40	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - Q, $\overline{Q}$)		12	20	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G - Q, $\overline{Q}$)		17	27	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

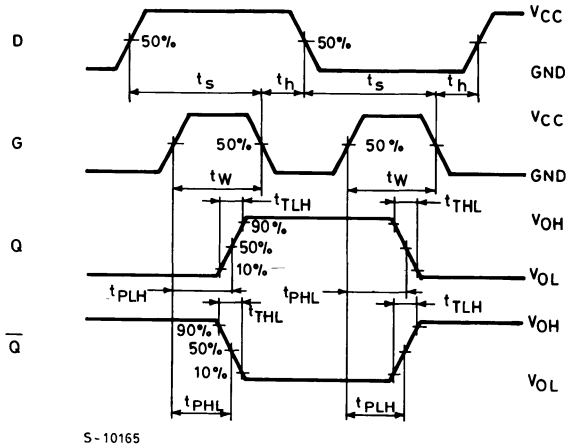
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - Q, $\overline{Q}$)	2.0 4.5 6.0		— — —	60 15 13	120 24 20	— — —	150 30 26	— — —	180 36 31	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G - Q, $\overline{Q}$)	2.0 4.5 6.0		— — —	82 20 17	160 32 27	— — —	200 40 34	— — —	240 48 41	ns
$t_{W(H)}$	Minimum Enable Pulse Width (G)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_s	Minimum Set-up Time	2.0 4.5 6.0		— — —	10 2 2	50 10 9	— — —	65 13 11	— — —	75 15 13	ns
t_h	Minimum Hold Time	2.0 4.5 6.0		— — —	— — —	5 5 5	— — —	5 5 5	— — —	5 5 5	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	48	—	—	—	—		pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

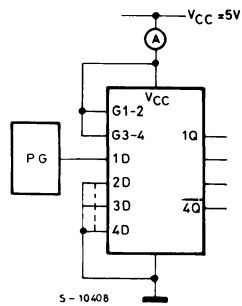
Average operating current can be obtained by the following equation.

$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Circuit)

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)

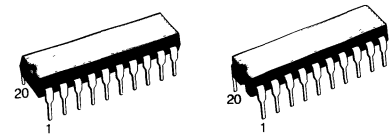


INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

OCTAL-D-TYPE FLIP FLOP

PRELIMINARY DATA

- HIGH SPEED
  f_{MAX} = 55 MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN).
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS377



B1N
Plastic Package

F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC377 F1
M74HC377 B1N
M74HC377 F1
M74HC377 C1
M74HC377 M1

DESCRIPTION

The M54/74HC377 is a high speed CMOS OCTAL-D-TYPE FLIP FLOP fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

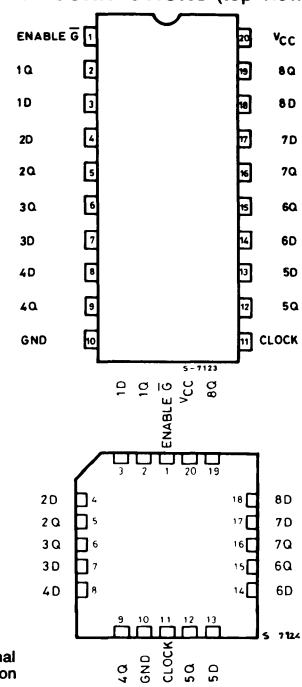
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the enable input $\overline{G}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUTS			OUTPUT
$\overline{G}$	CLOCK	DATA	Q
H	X	X	NO CHANGE
L	↑	L	L
L	↑	H	H
X	↓	X	NO CHANGE

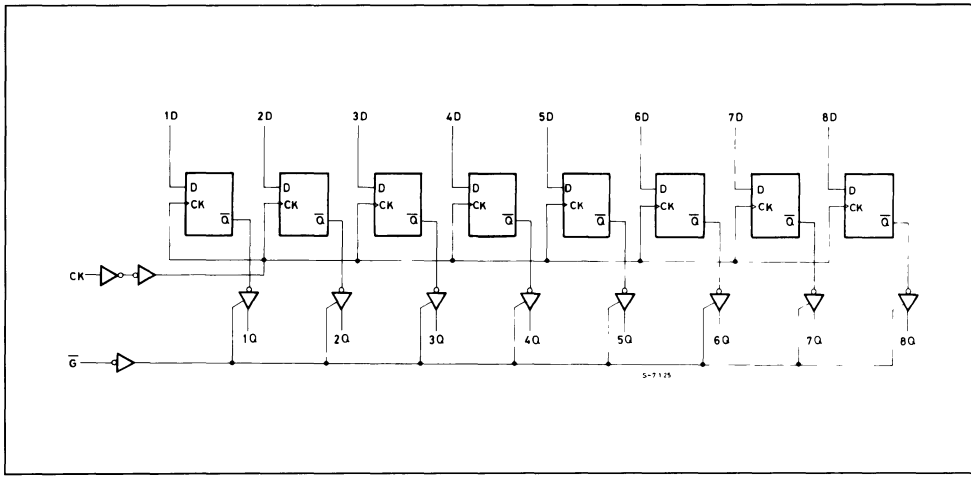
X: DON'T CARE

PIN CONNECTIONS (top view)



NC = No Internal Connection

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0.0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK)		17	27	ns
f_{MAX}	Maximum Clock Frequency	33	55		MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

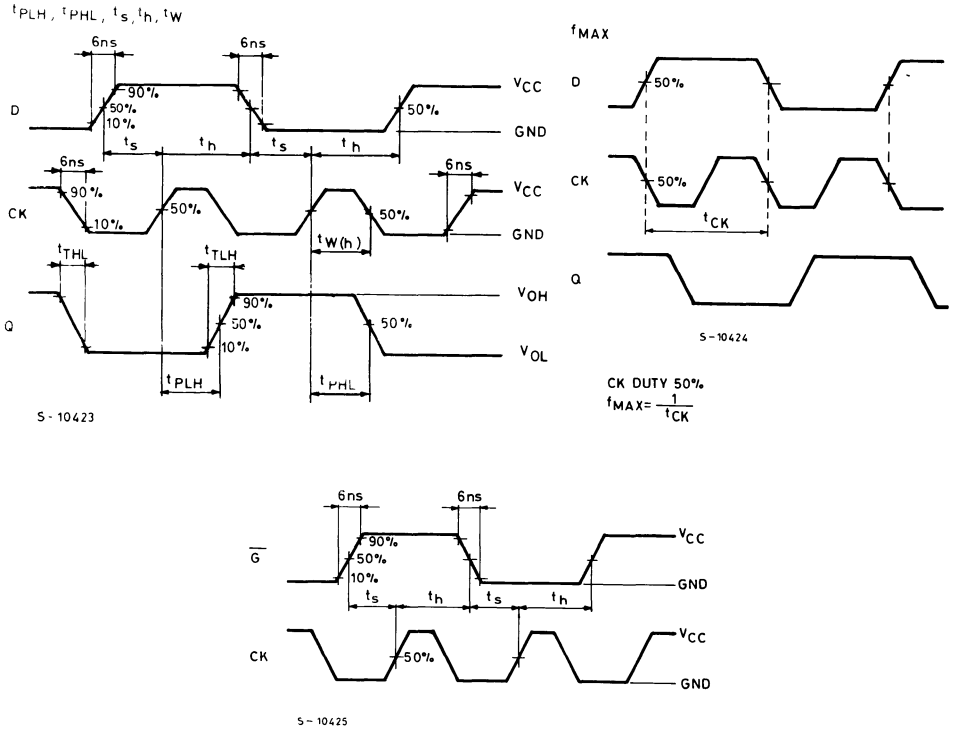
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q)	2.0		—	80	160	—	200	—	240	ns
		4.5		—	20	32	—	40	—	48	
		6.0		—	17	28	—	34	—	41	
f_{MAX}	Maximum Clock Frequency	2.0		6	13	—	4.8	—	4.0	—	MHz
		4.5		30	50	—	24	—	20	—	
		6.0		35	59	—	28	—	24	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-up Time (DATA)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-up Time (ENABLE $\overline{G}$-CK)	2.0		—	48	125	—	155	—	190	ns
		4.5		—	12	25	—	31	—	38	
		6.0		—	10	21	—	26	—	32	
t_h	Minimum Hold Time	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_h	Minimum Hold Time (ENABLE)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	34	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

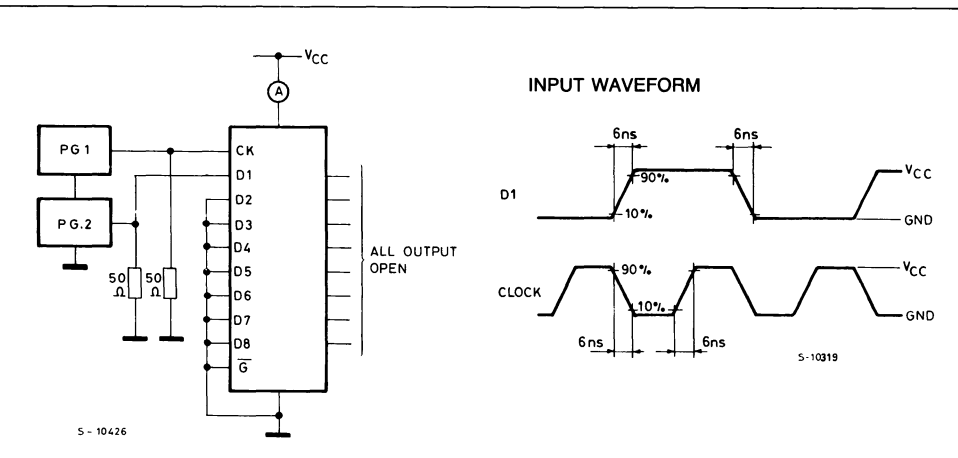
Average operating current can be obtained by the following equation.

$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ per Flip Flop

SWITCHING CHARACTERISTICS TEST WAVEFORM

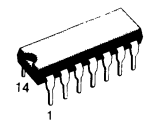


TEST CIRCUIT I_{CC} (Opr.)

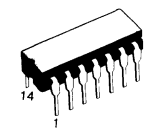


QUAD EXCLUSIVE-OR GATE

- HIGH SPEED
  t_{PD} = 14 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS386



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

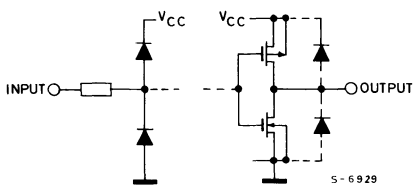
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC386 F1
M74HC386 B1N
M74HC386 F1
M74HC386 C1
M74HC386 M1

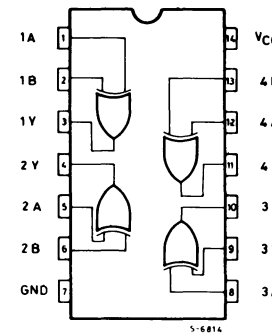
DESCRIPTION

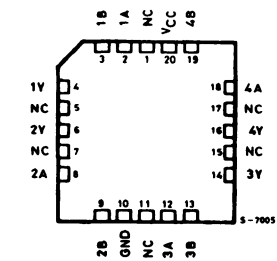
The M54/74HC386 is a high speed CMOS QUAD EXCLUSIVE-OR GATE fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. An output buffer provides high noise immunity and a stable output.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



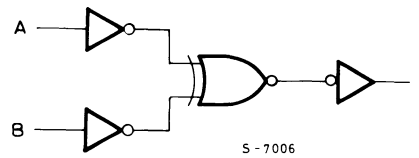
PIN CONNECTIONS (top view)





NC =
No Internal
Connection

LOGIC DIAGRAM (per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

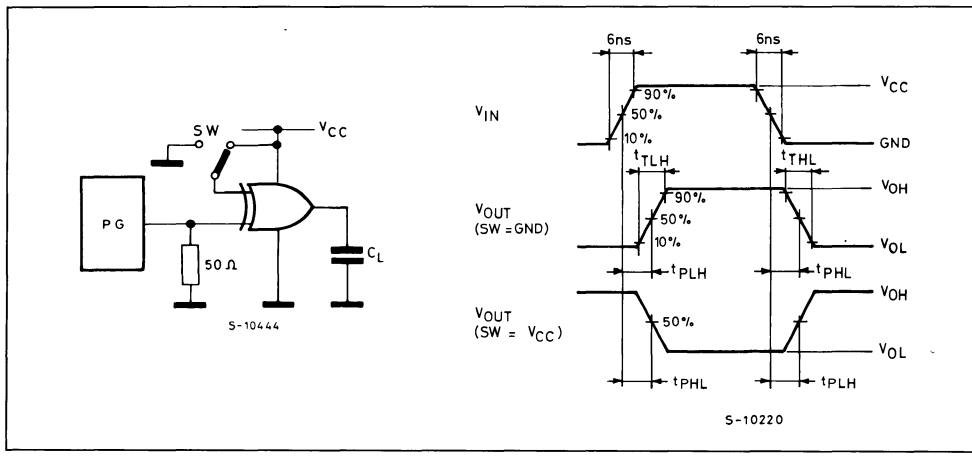
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH}	Propagation Delay Time		12	20	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

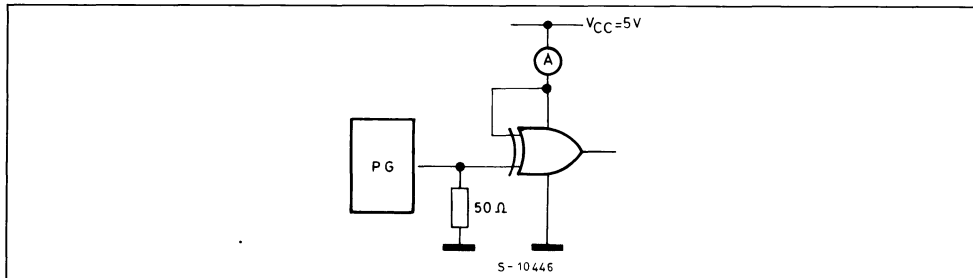
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	60	120	—	150	—	180	ns
		4.5		—	15	24	—	30	—	36	
		6.0		—	13	20	—	26	—	31	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	33	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following equation. I_{CC} (opr.) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate).

SWITCHING CHARACTERISTICS TEST CIRCUIT



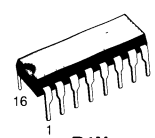
TEST CIRCUIT I_{CC} (Opr.)



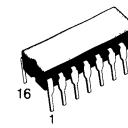
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

DUAL DECADE COUNTER

- HIGH SPEED
  t_{PD} = 13 ns (Typ) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS390



B1N
Plastic Package



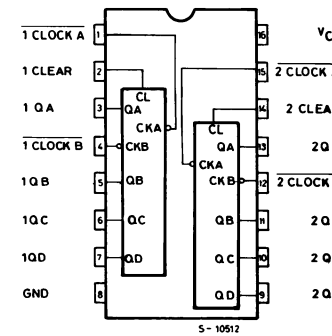
F1
Ceramic Frit Seal Package

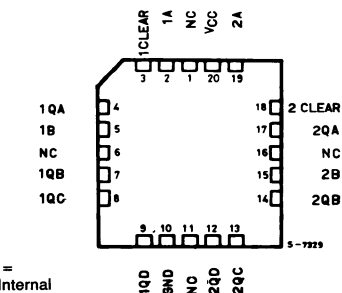
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC390 F1
M74HC390 B1N
M74HC390 F1
M74HC390 C1
M74HC390 M1

PIN CONNECTION (top view)





NC = No Internal Connection

DESCRIPTION

The M54/74HC390 is a high speed CMOS DUAL DECADE COUNTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

This dual decade counter contains two independent ripple carry counters. Each counter is composed of a divide-by-two and divide-by-five counter. The divide-by-two and divide-by-five counters can be cascaded to form dual decade, dual biquinary, or various combinations up to a single divide-by-100 counter.

Each 4-bit counter is incremented on the high to low transition (negative edge) of the clock input, and each has an independent clear input. When clear is set low all four bits of each counter are set to low. This enables count truncation and allows the implementation of divide-by-N counter configurations.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

COUNT	OUTPUTS							
	BCD COUNT *				BI-QUINARY **			
	QD	QC	QB	QA	QA	QD	QC	QB
0	L	L	L	L	L	L	L	L
1	L	L	L	H	L	L	L	H
2	L	L	H	L	L	L	H	L
3	L	L	H	H	L	L	H	H
4	L	H	L	L	L	H	L	L
5	L	H	L	H	H	L	L	L
6	L	H	H	L	H	L	L	H
7	L	H	H	H	H	L	H	L
8	H	L	L	L	H	L	H	H
9	H	L	L	H	H	H	L	L

INPUTS			OUTPUTS			
$\overline{\text{CLOCK A}}$	$\overline{\text{CLOCK B}}$	CLEAR	QA	QB	QC	QD
X	X	H	L	L	L	L
↓	X	L	BINARY COUNT UP			
X	↓	L	QUINARY COUNT UP			

Note: * Output QA is connected to input $\overline{\text{CLOCK B}}$ for BCD count.
** Output QD is connected to input $\overline{\text{CLOCK A}}$ for bi-quinary count.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

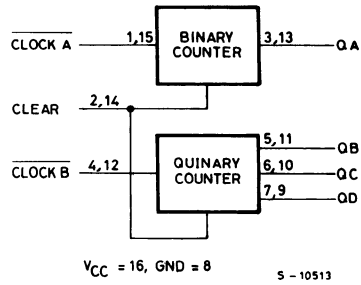
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

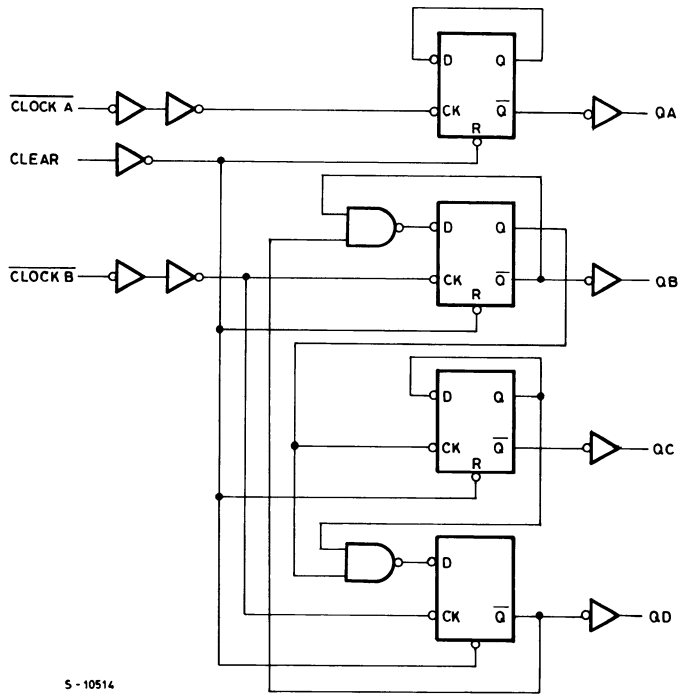
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC}	2 V 4.5V 6 V	0 to 1000 0 to 500 0 to 400	ns

BLOCK DIAGRAM

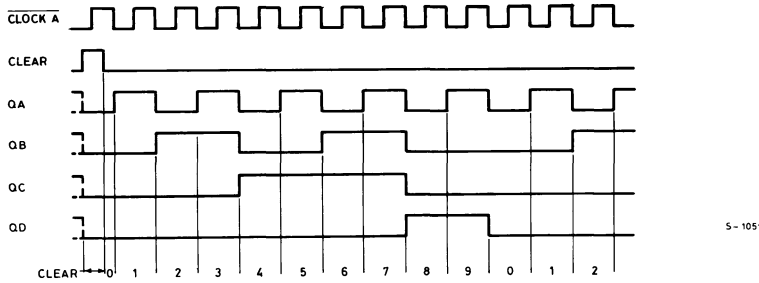


LOGIC DIAGRAM

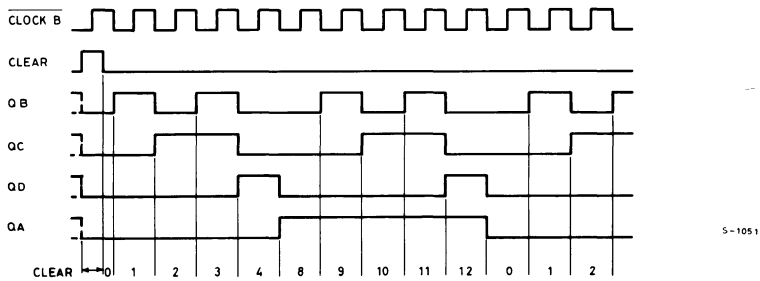


TIMING CHART

(1) BCD COUNT SEQUENCE*



(2) BI-QUINARY COUNT SEQUENCE**



* OUTPUT QA IS CONNECTED TO INPUT $\overline{\text{CLOCK B}}$
** OUTPUT QD IS CONNECTED TO INPUT $\overline{\text{CLOCK A}}$

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	

DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND	—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND	—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time	—	4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{A}$ - QA)	—	13	21	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{B}$ - QB, QD)	—	14	23	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{B}$ - QC)	—	21	33	ns
t_{PHL}	Propagation Delay Time (CL - Q)	—	16	26	ns
f_{MAX}	Maximum Clock Frequency ($\overline{CLOCK\ A}$ - QA)	35	64	—	MHz
f_{MAX}	Maximum Clock Frequency ($\overline{CLOCK\ B}$ - QB)	30	45	—	MHz

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOCK\ A}$ - QA)	2.0 4.5 6.0		— — —	64 16 14	130 26 22	— — —	165 33 28		195 39 33	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOCK\ B}$ (Q_B, Q_N)	2.0 4.5 6.0		— — —	68 17 14	135 27 23	— — —	170 34 29		205 41 35	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOCK\ B}$ - Q_C)	2.0 4.5 6.0		— — —	96 24 20	185 37 31	— — —	230 46 39		280 56 48	ns
t_{PHL}	Propagation Delay Time (CLEAR - Qn)	2.0 4.5 6.0		— — —	76 19 16	150 30 26	— — —	190 38 33		225 45 38	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

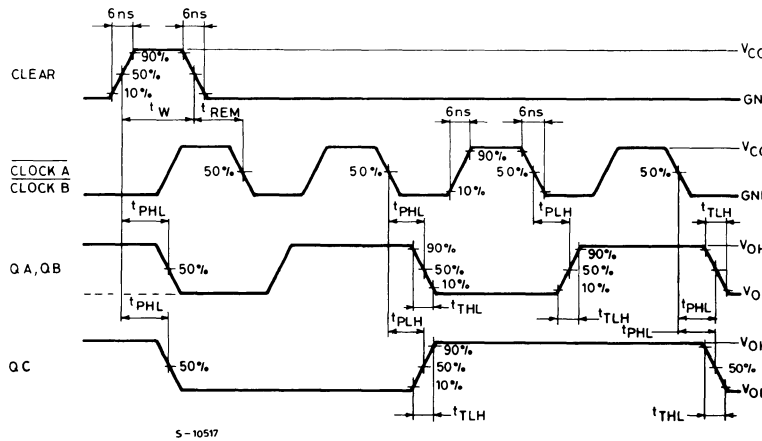
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency ($\overline{CLOCK\ A}$ - QA	2.0 4.5 6.0		6.4 32 28	15 58 68	— — —	5.2 26 31	— — —	4.2 21 25	— — —	MHz
f_{MAX}	Maximum Clock Frequency ($\overline{CLOCK\ B}$ - QB)	2.0 4.5 6.0		5.4 27 32	10 41 48	— — —	4.4 22 26	— — —	3.8 19 22	— — —	MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width ($\overline{CLOCK}$)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
$t_{W(L)}$	Minimum Pulse Width (CLEAR)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t_{REM}	Minimum Removal Time	2.0 4.5 6.0		— — —	5 0 0	25 5 5	— — —	30 6 6	— — —	40 8 7	ns
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	44	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

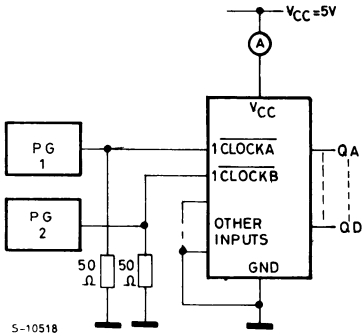
Average operating current can be obtained by the following equation:

$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

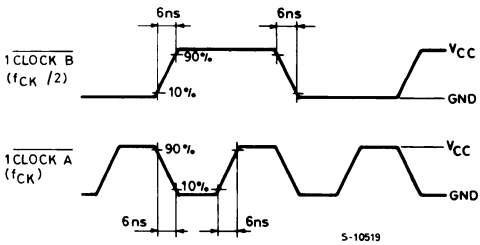
SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM



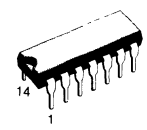
WHEN THE OUTPUTS DRIVE CAPACITIVE LOAD, TOTAL CURRENT CONSUMPTION IS TO BE A SUM OF THE VALUE CALCULATED FROM C_{PD} AND ΔI_{CC} OBTAINED FROM THE FOLLOWING FORMULA.

$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \cdot \frac{Ca}{2} + \frac{fCK}{2} \cdot V_{CC} \left(\frac{2Cb}{5} + \frac{Cc}{5} + \frac{Cd}{5}\right)$$

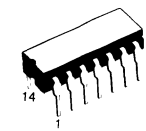
Ca~Cd ARE THE CAPACITANCE AT QA~QD OUTPUT.

DUAL BINARY COUNTER

- HIGH SPEED
  t_{PD} = 14 ns (TYP) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS393



B1N
Plastic Package



F1
Ceramic Frit Seal Package

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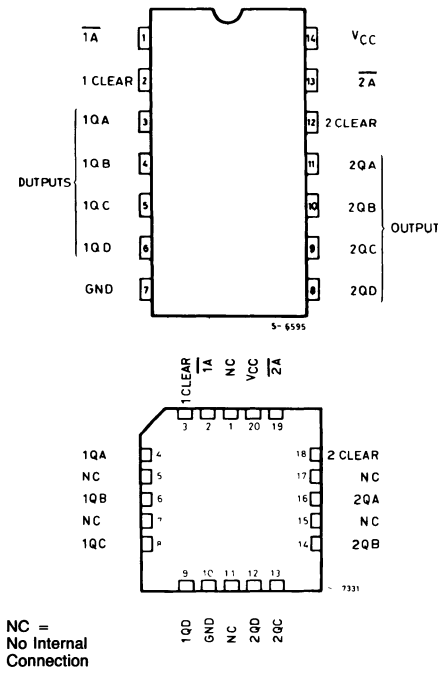
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC393 F1
M74HC393 B1N
M74HC393 F1
M74HC393 C1
M74HC393 M1

PIN CONNECTION (top view)



NC = No Internal Connection

DESCRIPTION

The M54/74HC393 is a high speed CMOS DUAL BINARY COUNTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

This counter circuit contains independent ripple carry counters and two 4-bit ripple carry binary counters, which can be cascaded to create a single divide-by-256 counter.

Each 4-bit counter is incremented on the high to low transition (negative edge) of the clock input, and each has an independent clear input. When clear is set low all four bits of each counter are sec to a low level. This enables count truncation and allows the implementation of divide-by-N counter configurations.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

TRUTH TABLE

COUNT	OUTPUT			
	QD	QC	QB	QA
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

INPUTS		OUTPUTS			
$\overline{CLEAR}$	CLEAR	QA	QB	QC	QD
X	H	L	L	L	L
↓	L	COUNT UP			
↑	L	NO CHANGE			

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

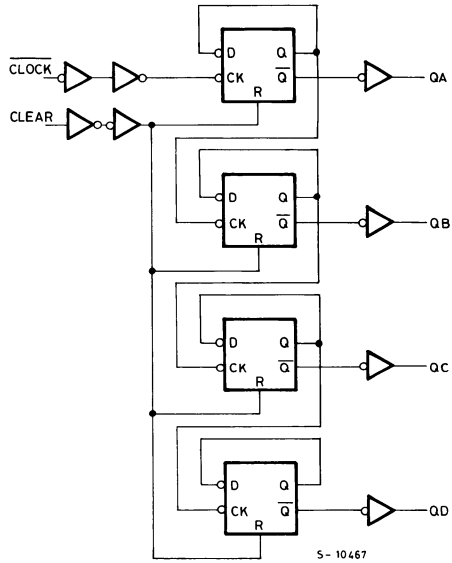
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

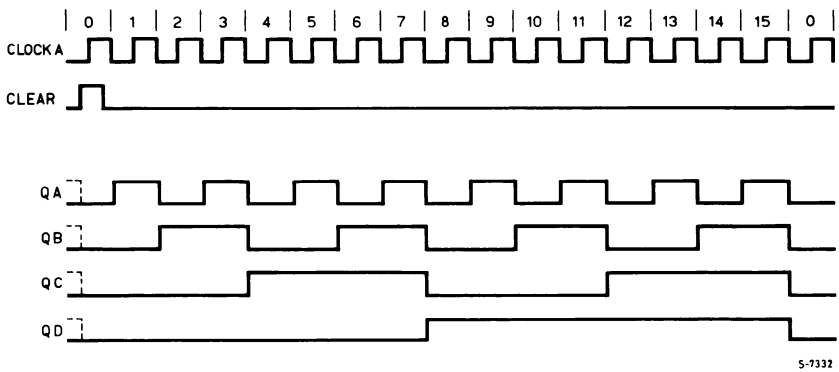
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Limit		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time		V_{CC} = 2 V	0 to 1000	ns
			V_{CC} = 4.5V	0 to 500	
			V_{CC} = 6 V	0 to 400	

LOGIC DIAGRAM



TIMING CHART



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{A}$ - QA)		14	23	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{A}$ - QB)		20	32	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{A}$ - QC)		25	39	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{A}$ - QD)		31	48	ns
f_{MAX}	Maximum Clock Frequency	35	68		MHz

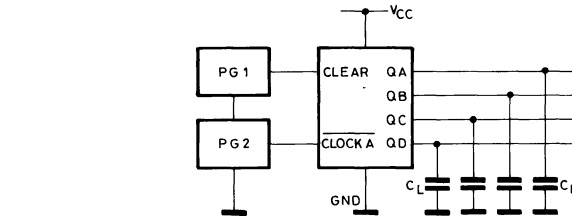
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

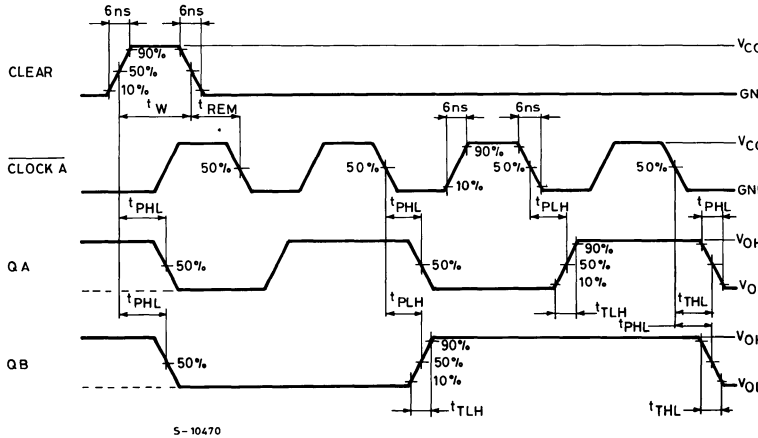
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOCK}$ - QA)	2.0		—	68	135	—	170		205	ns
		4.5		—	17	27	—	34		41	
		6.0		—	14	23	—	29		35	
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR - QB)	2.0		—	92	180	—	225		270	ns
		4.5		—	23	36	—	45		54	
		6.0		—	20	31	—	38		46	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - QC)	2.0		—	116	225	—	280		340	ns
		4.5		—	29	45	—	58		68	
		6.0		—	25	38	—	48		58	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - QD)	2.0		—	140	270	—	340		405	ns
		4.5		—	35	54	—	68		81	
		6.0		—	30	46	—	58		69	
t_{PHL}	Propagation Delay Time (CLEAR - Qn)	2.0		—	76	150	—	190		225	ns
		4.5		—	19	30	—	38		45	
		6.0		—	16	26	—	33		38	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
f_{MAX}	Maximum Clock Frequency	2.0		6.4	16	—	5.2	—	4.2	—	MHz
		4.5		32	62	—	26	—	21	—	
		6.0		38	73	—	31	—	25	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width ($\overline{CLOCK}$)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{REM}	Minimum Removal Time (CLEAR)	2.0		—	—	25	—	30	—	38	ns
		4.5		—	—	5	—	6	—	8	
		6.0		—	—	5	—	5	—	6	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	41	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

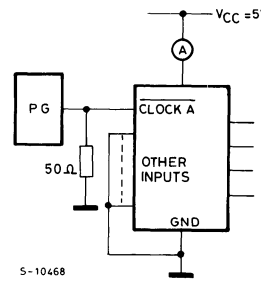
Average operating current can be obtained by the following equation $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM





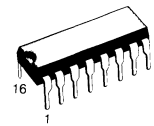
TEST CIRCUIT I_{CC} (Opr.)



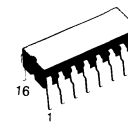
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

- HIGH SPEED
  t_{PD} = 28 ns (TYP) at V_{CC} = 5V
- LOW POWER DISSIPATION
  STANDBY STATE I_{CC} = 4 μA (MAX.) at T_A = 25°C
  ACTIVE STATE I_{CC} = 200 μA (TYP) at V_{CC} = 5V
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS423
- WIDE OUTPUT PULSE WIDTH RANGE
  t_{WOUT} = 120ns to 60s over at V_{CC} = 4.5V



B1N
Plastic Package



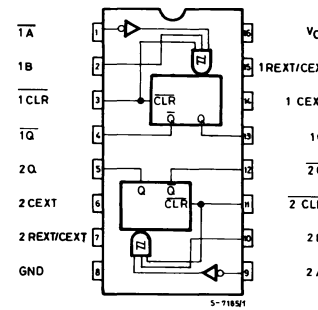
F1
Ceramic Frit Seal Package

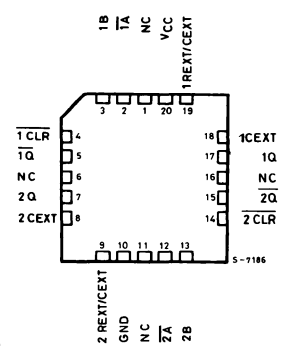
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC423 F1
M74HC423 B1N
M74HC423 F1
M74HC423 C1
M74HC423 M1

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

DESCRIPTION

The M54/74HC423 is a high speed CMOS MONOSTABLE multivibrator fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. There are two trigger inputs, A INPUT (negative edge) and 8 INPUT (positive edge). These inputs are valid for rising/falling signals, (t_r-t_f-I sec).
The device may also be triggered by using the CLR input (positive-edge) because of the Schmitt-trigger input; after triggering the output maintains the MONOSTABLE state for the time period determined by the external resistor Rx and capacitor Cx. Taking $\overline{CLR}$ low breaks this MONOSTABLE STATE. If the next trigger pulse occurs during the MONOSTABLE period it makes the MONOSTABLE period longer. Limit for values of Cx and Rx:

Cx : NO LIMIT

Rx : V_{CC} = 2.0V 5KΩ to 1MΩ
V_{CC} = 3.0V 1KΩ to 1MΩ

All inputs are equipped with protection circuits against static discharge and transient excess voltage

TRUTH TABLE

INPUTS			OUTPUTS		NOTE
$\overline{A}$	B	$\overline{CL}$	Q	$\overline{Q}$	
↓	H	H			OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	↑	H			OUTPUT ENABLE
X	X	L	L	H	INHIBIT

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

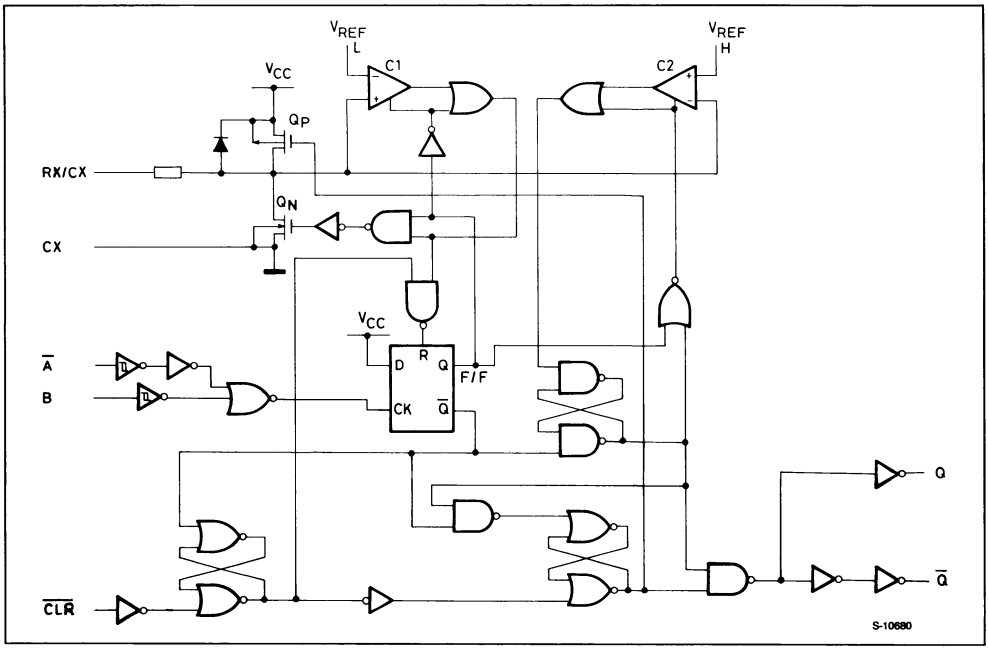
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

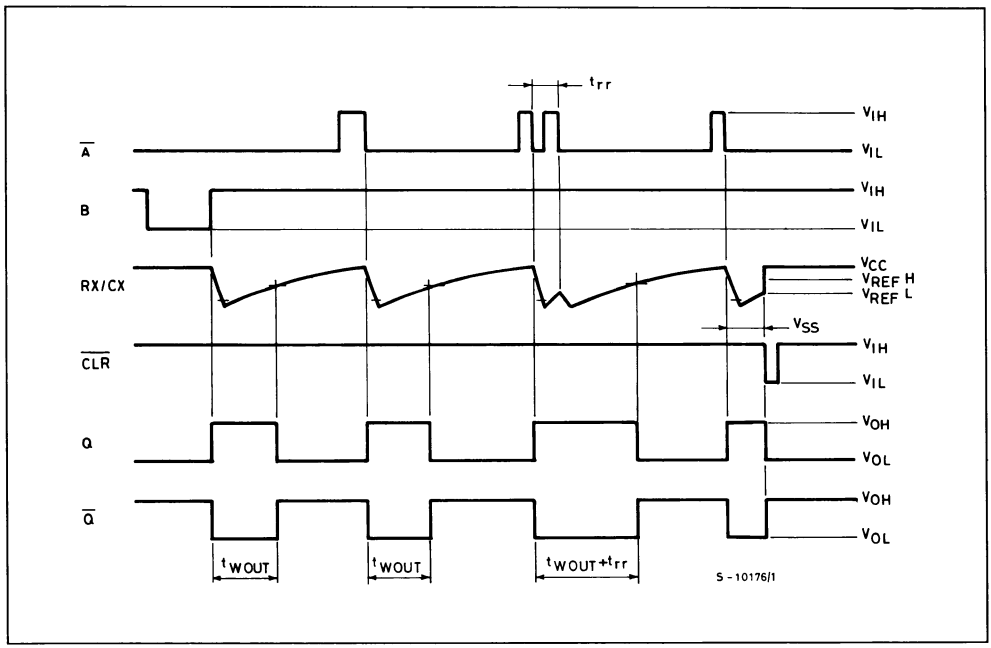
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series Operating Temperature 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time ($\overline{CLR}$ only)	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	
Cx	External Capacitor	NO LIMITATION		F
Rx	External Resistor (V_{CC} = 2.0V) External Resistor (V_{CC} ≧ 3.0V)	V_{CC} = 2 V	5K to 1M	Ω
		V_{CC} = 3 V	1K to 1M	

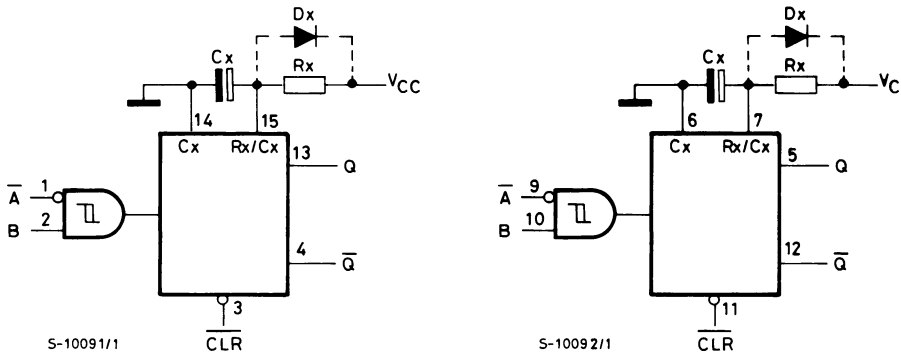
SYSTEM DIAGRAM



TIMING CHART



BLOCK DIAGRAM



Note:
(1) Cx, Rx, Dx are external components.
(2) Dx is a clamping diode

The external capacitor is charged to V_{CC} in the stand-by state, i.e. no trigger. When the supply voltage is turned off Cx is discharged mainly through an internal parasitic diode (see figures). If Cx is sufficiently large and V_{CC} decreases rapidy, there will be some possibility of damaging the I.C. with a surge current or latch-up. If the voltage supply filter capacitor is large enough and V_{CC} decrease slowly, the surge current is automatically limited and damage the I.C. is avoided. The maximum forward current of the parasitic diode is approximately 20 mA. In cases where Cx is large the time taken for the supply voltage to fall to 0.4 V_{CC} can be calculated as follows:

$t_f \geqq (V_{CC} - 0.7) \cdot Cx/20mA$

In cases where t_f is too short an external clamping diode is required to protect the I.C. from the surge current.

FUNCTIONAL DESCRIPTION

Stand-by state

The external capacitor, Cx, is fully charged to V_{CC} in the stand-by state. Hence, before triggering, transistor Qp and Qn (connected to the Rx/Cx node) are both turned off. The two comparators that control the timing and the two reference voltage sources stop operating. The total supply current is therefore only leakage current.

Trigger operation

Triggering occurs when:

1 st) A is "low" and B has a falling edge;
2 nd) B is "high" and A has a rising edge;
3 rd) A is low and B is high and C1 has a rising edge.

After the multivibrator has been retriggered comparator C1 and C2 start operating and Qn is turned on. Cx then discharges through Qn. The voltage at the node Rx/Cx external falls.

When it reaches V_{REFL} the output of comparator C1 becomes low. This in turn resets the flip-flop and Gn is turned off.
At this point C1 stops functioning but C2 continues to operate.
The voltage at R/C external begins to rise with a time constant set by the external components Rx, Cx.
Triggering the multivibrator causes Q to go high after internal delay due to the flip-flop and the gate. Q remains high until the voltage at R/C external rises again to V_{REFH}. At this point C2 output goes low and O goes low. C2 stops operating. That means that after triggering when the voltage Rx/Cx external returns to V_{REFH} the equitivibrator has returned to its MONOSTABLE STATE. In the case where Rx • Cx are large enough and the discharge time of the capacitor and the delay time in the I.C. can be ignored, the width of the output pulse tw (out) is as follows:

$$t_{W(OUT)} = 0.46\ Cx \cdot Rx$$

FUNCTIONAL DESCRIPTION (Continued)

Re-trigger operation

When a second trigger pulse follows the first its effect will depend on the state of the multivibrator. If the capacitor Cx is being charged the voltage level of Rx/Cx external falls to V_{REFL} again and Q remains high i.e. the retrigger pulse arrives in a time shorter than the period Rx • Cx seconds, the capacitor charging time constant. If the second trigger pulse is very close to the initial trigger pulse it is ineffective; i.e., the second trigger must arrive in the capacitor discharge cycle to be ineffective. Hence the minimum time for a second trigger to be effective depends on V_{CC} and C_x.

Reset operation

CL is normally high. If CL is low, the trigger is not effective because Q output goes low and trigger control flip-flop is reset.

Also transistor Op is turned on and Cx is charged quicky to V_{CC}. This means if CL input goes low, the IC becomes waiting state both in operating and non operating state.

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage (Q, $\overline{Q}$ Output)	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_I = V_{IH} = V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage (Q, $\overline{Q}$ Output)	2.0	V_I = V_{IH} = V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{IN}	R/C Terminal Off-State Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA
I_{CC}	Active State (1) Supply Current	2.0	$V_I = V_{CC}$ or GND pins 7, 15 $V_{IN} = V_{CC/2}$		—	40	120	—	160	—	200	μA
		4.5			—	0.1	0.3	—	0.4	—	0.5	mA
		6.0			—	0.2	0.6	—	0.8	—	1.0	mA

(1) Per circuit

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{A}$,B - Q,$\overline{Q}$)		27	41	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$ - Q,$\overline{Q}$)		21	33	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{A}$, B - Q, $\overline{Q}$)	2.0 4.5 6.0		— — —	124 31 26	240 48 41	— — —	300 60 51	— 	360 72 61	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$ - Q, $\overline{Q}$)	2.0 4.5 6.0		— — —	100 25 21	195 39 33	— — —	245 49 42		295 59 50	ns
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width ($\overline{A}$, B)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
$t_{W(L)}$	Minimum Clear Pulse Width	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t_{REM}	Minimum Clear Removal Time	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
Δt_{WOUT}	Output Pulse Width Error Between Circuits in same Package			—	±1	—	—	—	—	—	%
t_{rr}	Minimum Retrigger Time	4.5 6.0	Cx = 100pF Rx = 1kΩ	— —	74 63	— —	— —	— —	— —	— —	ns
		4.5 6.0	Cx = 0.01μF Rx = 1kΩ	— —	1.1 1.0	— —	— —	— —	— —	— —	μs
t_{WOUT} (MIN)	Minimum output Pulse Width	4.5	Cx = 0 Rx = 1kΩ	—	118	—	—	—	—	—	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

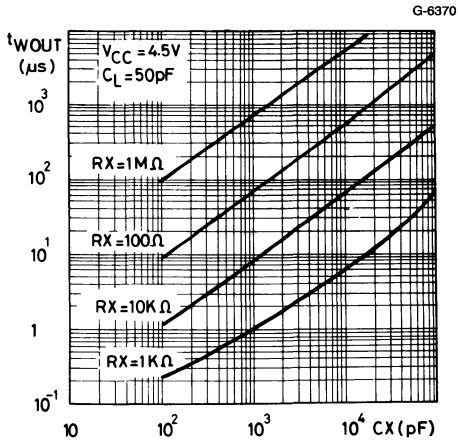
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{WOUT}	Output Pulse Width	4.5	Cx = 100pF Rx = 10kΩ	—	1.0	—	—	—	—	—	μs
	Width	4.5	Cx = 0.1μF R_x = 100kΩ	—	4.7	—	—	—	—	—	ms
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
$C_{PD(*)}$	Power Dissipation Capacitance			—	113	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}' \cdot Duty/100 / + I_{CC}/2$ (per monostable)

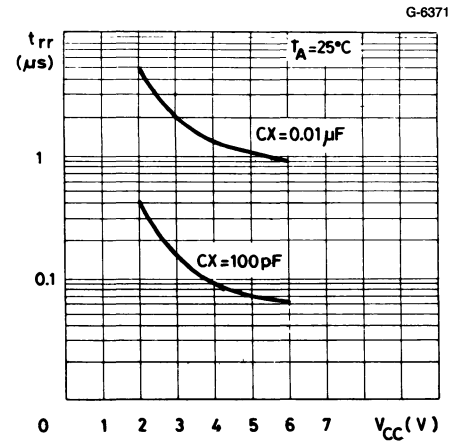
(I_{CC}': Active Supply Current)

(Duty: %)

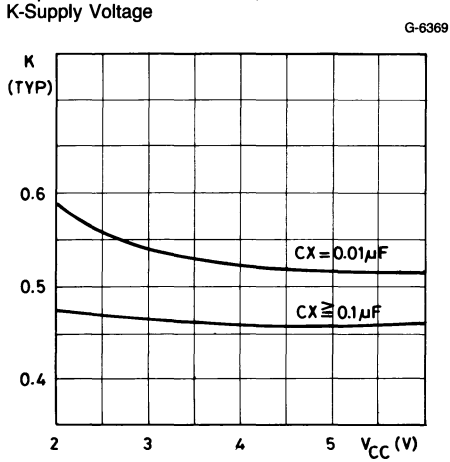
t_{WOUT} - Cx Characteristics (Typ.)



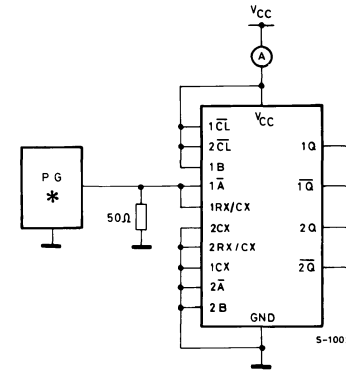
t_{rr} - V_{CC} Characteristics (Typ).



Output Pulse Width Constant,
K-Supply Voltage

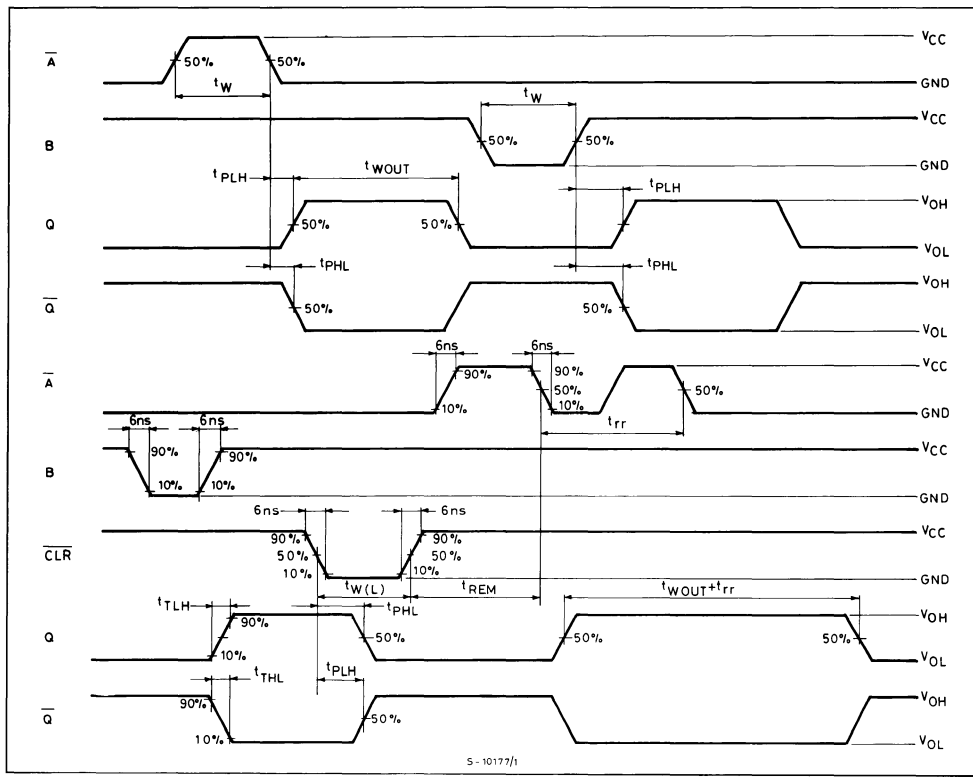


TEST CIRCUIT I_{CC} (Opr.)



TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

SWITCHING CHARACTERISTICS TEST WAVEFORM

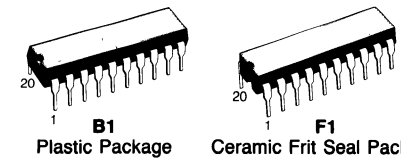


SGS-THOMSON MICROELECTRONICS

M54HC540/541
M74HC540/541

HC540 OCTAL BUS BUFFER INVERTING (3-STATE)
HC541 OCTAL BUS BUFFER (3-STATE)

- HIGH SPEED
  t_{PD} = 11 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS540/541



B1
Plastic Package

F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

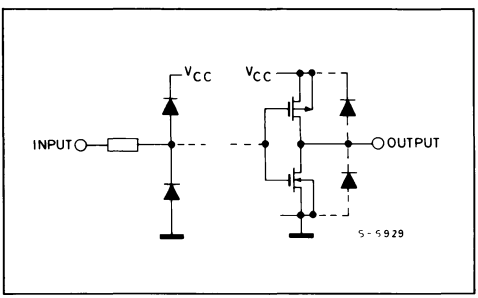
ORDERING NUMBERS:

M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX C1
M74HCXXX M1

DESCRIPTION

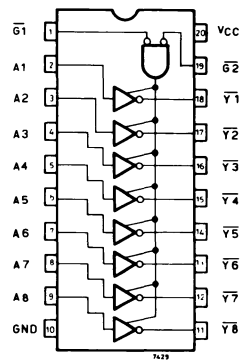
The M54/74HC540/541 are high speed CMOS OCTAL BUS BUFFERS (3-STATE) fabricated in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. The M54/74HC540 is an inverting buffer and the M54/74HC541 is a non-inverting buffer. The 3-STATE control gate operates as a two-input AND such that if either $\overline{G1}$ or $\overline{G2}$ are high, all eight outputs are in the high-impedance state.
In order to enhance PC board layout, the 'HC540 and 'HC541 offers a pinout having inputs and outputs on opposite sides of the package.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT

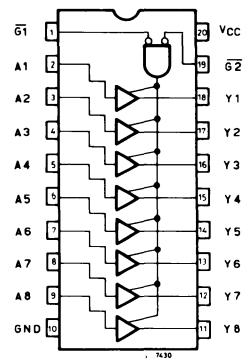


PIN CONNECTIONS (top view)

HC540

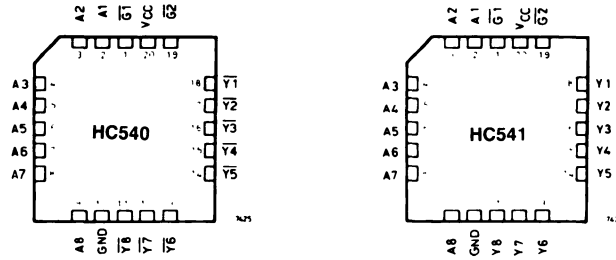


HC541



NC =
No Internal
Connection

CHIP CARRIER

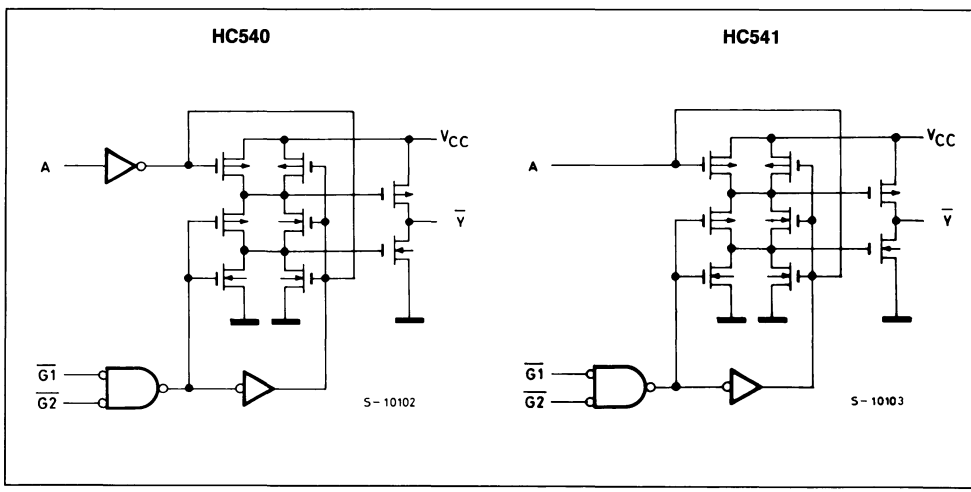


TRUTH TABLE

INPUTS			OUTPUT	
$\overline{G1}$	$\overline{G2}$	An	Yn*	$\overline{Yn}$*
H	X	X	Z	Z
X	H	X	Z	Z
L	L	H	L	L
L	L	L	L	H

X: DON'T CARE Z: HIGH IMPEDANCE
*: Yn.....HC541 $\overline{Yn}$.....HC540

CIRCUIT DIAGRAM (Per Circuit)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400		ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0 4.5 6.0	V_I V_{IH} or V_{IL}	I_O −20 μA	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	1.9 4.4 5.9	— — —	V
		4.5 6.0		−4.0 mA −5.2 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	
V_{OL}	Low Level Output Voltage	2.0 4.5 6.0	V_{IH} or V_{IL}	20 μA	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
		4.5 6.0		4.0 mA 5.2 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40	

DC SPECIFICATIONS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND	—	—	±0.1	—	±1.0	—	±1.0	μA
I_{OZ}	3-Stato Output Off-State Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND	—	—	±0.5	—	±5.0	—	±10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND	—	—	4	—	40	—	80	μA

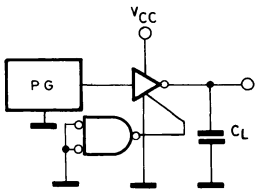
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	25 7 6	60 12 10	— — —	75 15 13		90 18 15	ns
t_{PLH} t_{PHL}	Propagation Delay Time	2.0 4.5 6.0	HC540	— — —	52 13 11	105 21 18	— — —	130 26 22		160 32 27	ns
t_{PLH} t_{PHL}	Propagation Delay Time	2.0 4.5 6.0	HC541		56 14 12	15 23 20	— — —	145 29 25	— — —	135 35 30	ns
t_{PLZ} t_{PHZ}	3-State Output Enable	2.0 4.5 6.0	$R_L = 1K\Omega$	— — —	72 18 15	145 29 25	— — —	180 36 31	— — —	220 44 38	ns
t_{PLZ} t_{PHZ}	3-State Output Disable Time	2.0 4.5 6.0	$R_L = 1K\Omega$	— — —	88 22 19	160 32 27	— — —	200 40 34	— — —	240 48 41	ns
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{OUT}	Output Capacitance			—	10	—	—	—	—	—	pF
C_{PD} (1)	Power Dissipation Capacitance		HC540	—	33	—	—	—	—	—	pF
			HC541	—	36	—	—	—	—	—	

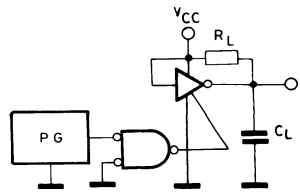
Note (1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the following equation.
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Gate).

SWITCHING CHARACTERISTICS TEST CIRCUIT AND WAVEFORM

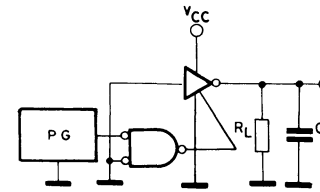
HC540



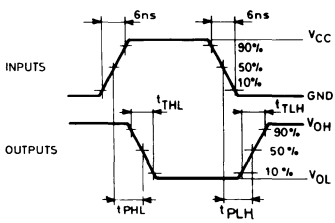
S-10476



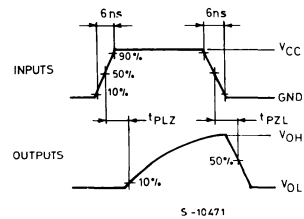
S-10477



S-10478



S-10480



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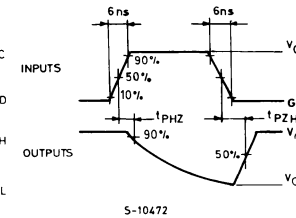
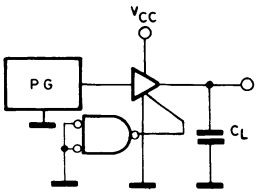
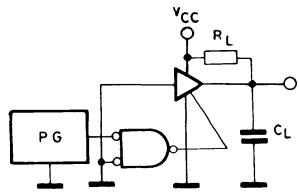


S-10472

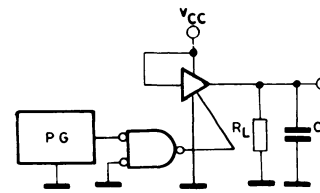
HC541



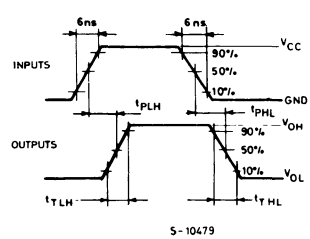
S-10473



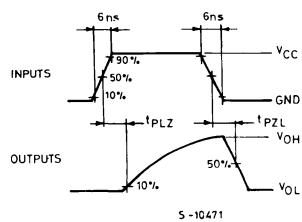
S-10474



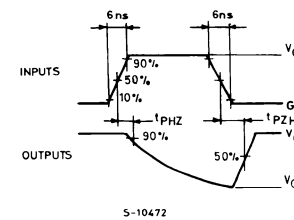
S-10475



S-10479



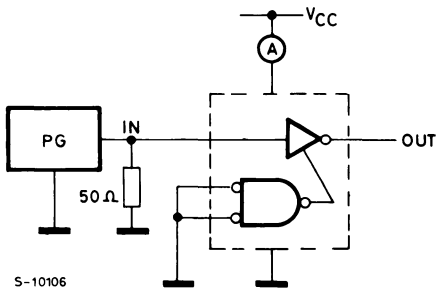
S-10471

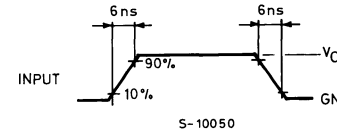


S-10472

TEST CIRCUIT I_{CC} (Opr.)

HC540





THE OTHER INPUTS ARE CONNECTED V_{CC} LINE OR GND LINE.

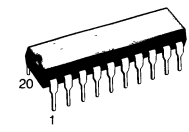
TEST CIRCUIT OF THE HC541 IS THE SAME AS THIS

SGS-THOMSON MICROELECTRONICS

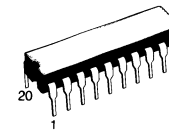
M54/74HCT540
M54/74HCT541

HCT540 OCTAL BUS BUFFER WITH INVERTED 3-STATE OUTPUTS
HCT541 OCTAL BUS BUFFER WITH NON INVERTED 3-STATE OUTPUTS

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2 V (MIN.) V_{IL} = 0.8 V (MAX.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LST540/541



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HCTXXX F1
M74HCTXXX B1N
M74HCTXXX F1
M74HCTXXX C1
M74HCTXXX M1

DESCRIPTION

The M54/74HCT540 and M54/74HCT541 are high speed CMOS OCTAL BUS BUFFER fabricated in silicon gate C²MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
These devices may be used as level converters for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible whith TTL, NMOS and CMOS output voltage levels.
The M54/74HCT540 is a non-inverting type. The M54/74HCT541 is an inverting type. If either G1 or G2 are high, the terminal outputs are in the high-impedance state.

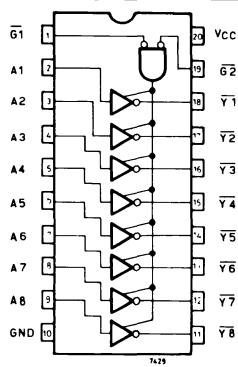
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

NOTICE FOR APPLICATION

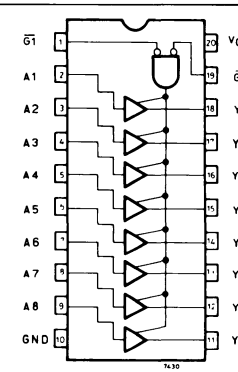
IT IS PROHIBITED TO APPLY A SIGNAL TO BUS TERMINAL WHEN IT IS IN OUTPUT MODE.
AND WHEN A BUS TERMINAL IS FLOATING (HIGH IMPEDANCE STATE), IT IS REQUESTED TO FIX THE INPUT LEVEL BY MEANS OF EXTERNAL PULL DOWN OR PULL UP RESISTOR.

PIN CONNECTION

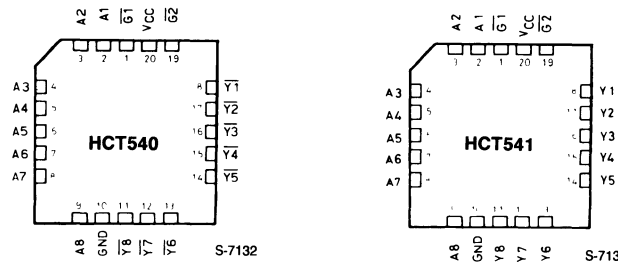
HCT540



HCT541



CHIP CARRIER

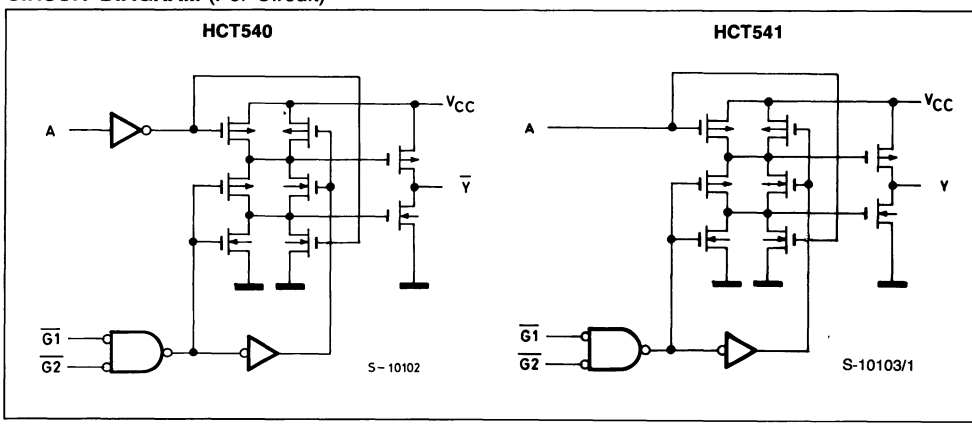


TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{G1}$	$\overline{G2}$	An	Yn*	$\overline{Yn}$*
H	X	X	Z	Z
X	H	X	Z	Z
L	L	H	L	L
L	L	L	L	H

X: DONT'T CARE
Z: HIGH IMPEDANCE
*: Yn ... HCT541
$\overline{Yn}$ ... HCT540

CIRCUIT DIAGRAM (Per Circuit)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		4.5 to 5.5	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time		0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0	—	—	2.0	—	2.0	—	V
V_{IL}	Low Level Input Voltage	4.5 to 5.5			—	—	0.8	—	0.8	—	0.8	V
V_{OH}	High Level Output Voltage	4.5	V_{IN}	I_{OH}								V
			V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
				−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
V_{OL}	Low Level Output Voltage	4.5	V_{IN}	I_{OL}								V
			V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	
				6.0 mA	—	0.17	0.26	—	0.33	—	0.40	

DC SPECIFICATIONS (Continued)

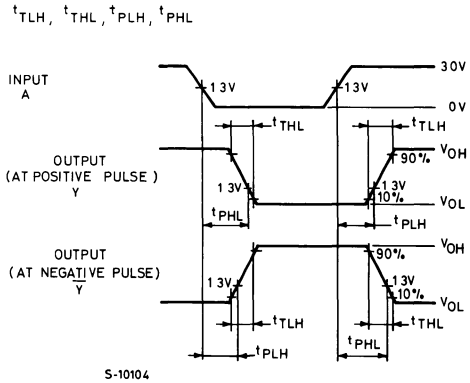
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_{OZ}	3-State Output Off-State Current	5.5	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	—	—	±0.5	—	±5.0	—	±10.0	μA
I_{IN}	Input Leakage Current	5.5	$V_{IN} = V_{CC}$ or GND	—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	5.5	$V_I = V_{CC}$ or GND	—	—	4.0	—	40	—	80	μA
I_{CC}			Per input: $V_{IN} = 0.5V$ or 2.4V Other input: V_{CC} or GND	—	—	2.0	—	2	—	3.0	mA

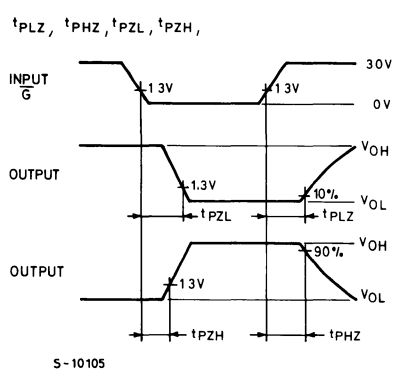
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5		—	7	12	—	15	—	18	ns
t_{PLH} t_{PHL}	Propagation Delay Time	4.5	M54/74HCT540	—	16	26	—	33	—	39	ns
t_{PLH} t_{PHL}	Propagation Delay Time	4.5	M54/74HCT541	—	19	30	—	38	—	45	ns
t_{PZL} t_{PZH}	Output Enable Time	4.5	$R_L = 1k\Omega$	—	23	36	—	45	—	54	ns
t_{PLZ} t_{PHZ}	Output Disable Time	4.5	$R_L = 1k\Omega$	—	23	33	—	41	—	50	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{OUT}	Output Capacitance			—	10	—	—	—	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance		M54/74HCT540	—	37	—	—	—	—	—	pF
			M54/74HCT541	—	39	—	—	—	—	—	

Note (*) C_{PD} is defined as the value of IC's internal equivalent capacitance which is calculated from the operating current consumption without load (refer to Test circuit).
Average operating current is: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Gate)

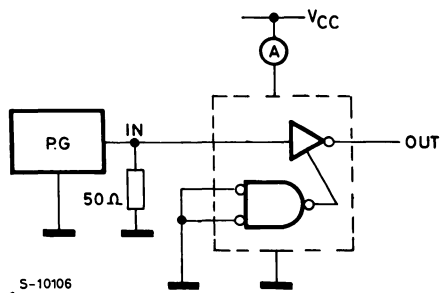
SWITCHING CHARACTERISTICS TEST CIRCUIT AND WAVEFORM

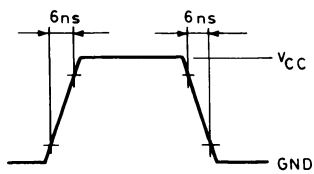




TEST CIRCUIT I_{CC} (Opr.)

HCT540





The other inputs are connected V_{CC} line or GND line.

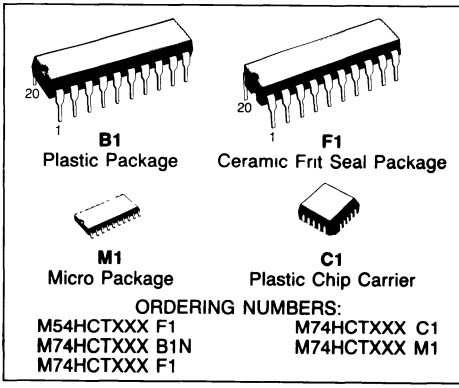
TEST CIRCUIT OF THE HCT541 IS THE SAME AS THIS.

SGS-THOMSON MICROELECTRONICS

M54HCT563/573
M74HCT563/573

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT
HCT563 INVERTING - HCT573 NON-INVERTING

- HIGH SPEED
  t_{PD} = 20 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (Min.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS563/573



ORDERING NUMBERS:

M54HCTXXX F1
M74HCTXXX B1N
M74HCTXXX F1
M74HCTXXX C1
M74HCTXXX M1

DESCRIPTION

These devices are high speed C²MOS OCTAL LATCHES with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology. These ICs achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

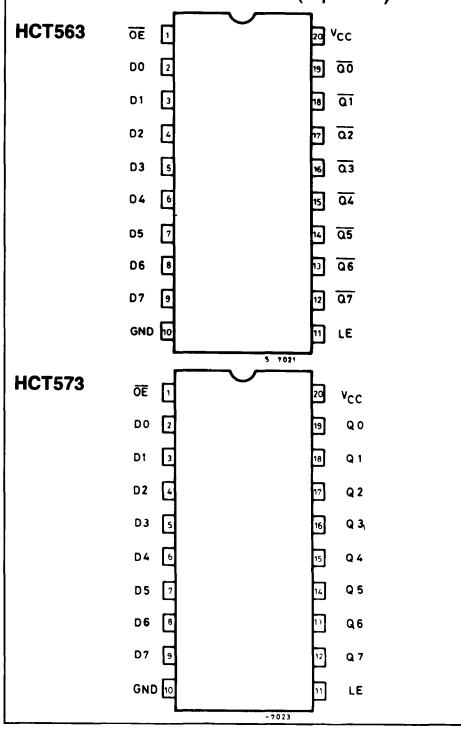
These 8-bit D-type latches are controlled by a latch enable input (LE) and an output enable input ($\overline{OE}$). While the LE input is held high, the Q outputs will follow the data input precisely or inversely. The Q outputs will be latched precisely or inversely at the logic level of D input data the instant LE is taken low.

When the $\overline{OE}$ input is low, the eight outputs will be in a normal logic state (high or low logic level) and when high the outputs will be in a high impedance state.

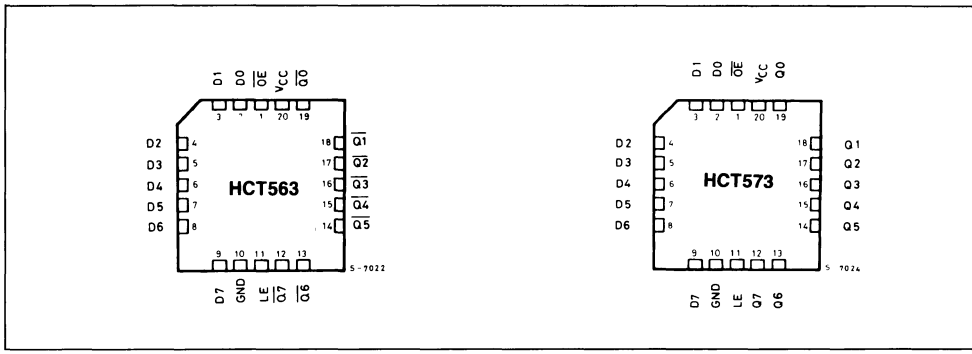
The application designer has a choice of a combination of inverting and non-inverting outputs, symmetrical and neighbouring input/output pin layout. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

These integrated circuits are totally compatible, input and output characteristic, with standard 54/74 LSTTL logic families. M54HCT/74HCT devices are designed to directly interface HSC²MOS system with TTL and NMOS components. These components are also plug in replacements for LSTTL devices but with lower power consumption.

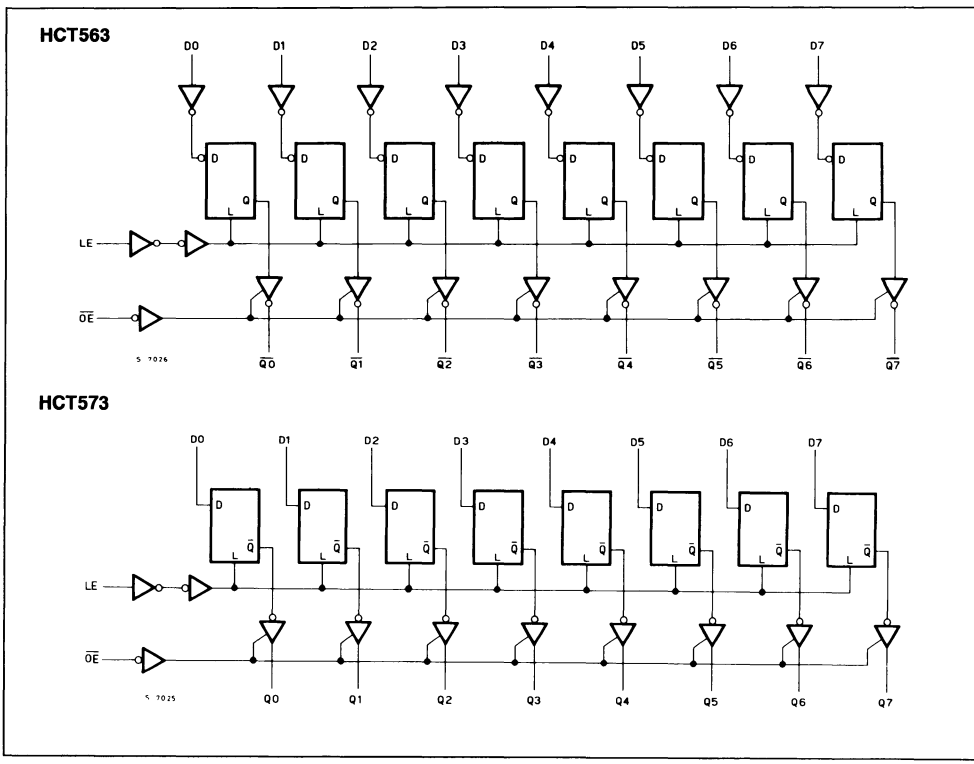
PIN CONNECTIONS (top view)



CHIP CARRIER



LOGIC DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q (HCT573)	$\overline{Q}$ (HCT563)
H	X	X	HZ	HZ
L	L	X	Qn	Qn
L	H	L	L	H
L	H	H	H	L

Qn: Q/$\overline{Q}$ OUTPUTS ARE LATCHED AT THE TIME WHEN THE LE INPUT IS TAKEN LOW LOGIC LEVEL.
X: DON'T CARE HZ= HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

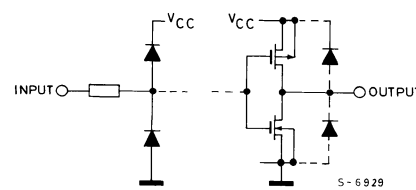
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	4.5 to 5.5		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series Operating Temperature 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 4.5V	0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0	—	—	2.0	—	2	—	V
V_{IL}	Low Level Input Voltage	4.5 to 5.5			—	—	0.8	—	0.8	—	0.8	V
V_{OH}	High Level Output Voltage		V_I	I_O								
		4.5	V_{IH} or V_{IL}	−20 μA	4.4		—	4.4	—	4.4	—	V
		4.5		−6.0 mA	4.18	4.31	—	4.13	—	4.1		
V_{OL}	Low Level Output Voltage	4.5	V_{IH} or V_{IL}	20 μA	—		0.1	—	0.1	—	0.1	V
		4.5		6.0 mA	—	0.17	0.32	—	0.37	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{OZ}	3 State Output Current	5.5			—	—	±0.5	—	±5.0	—	±10	μA
I_{CC}	Quiescent Supply Current	5.5	$V_I = V_{CC}$ or GND $I_O = 0$		—	—	4	—	40	—	80	μA

INPUT AND OUTPUT EQUIVALENT CIRCUIT

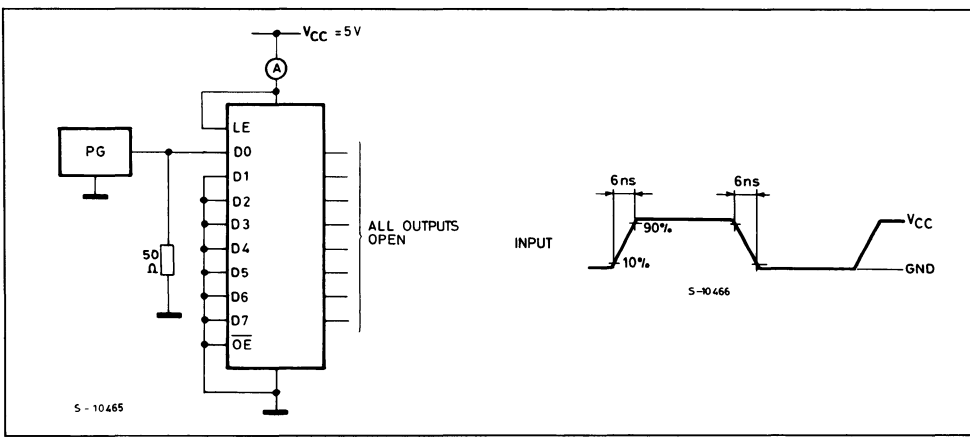


AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5		—	7	12	—	15		18	ns
t_{PLH} t_{PHL}	Propagation Delay Time (LE-Q,$\overline{Q}$)	4.5		—	24	35	—	44		53	ns
t_{PLH}	Propagation Delay Time (D-Q,$\overline{Q}$)	4.5		—	22	35	—	44		53	ns
$t_{W(H)}$	Minimum Pulse Width (LE)	4.5		—	8	15	—	19		22	ns
t_s	Minimum Set-up Time	4.5		—	2	10	—	13		15	ns
t_n	Minimum Hold Time	4.5		—	—	5	—	5		5	ns
t_{PZL} t_{PZH}	3-State Output Enable Time	4.5	R_L = 1KΩ	—	18	35	—	44		53	ns
t_{PLZ} t_{PHZ}	3-State Output Disable Time	4.5	R_L = 1KΩ	—	26	37	—	46		56	ns
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{OUT}	Output Capacitance			—	10	—	—	—	—	—	
C_{PD} (*)	Power Dissipation Capacitance			—	41	—	—	—			

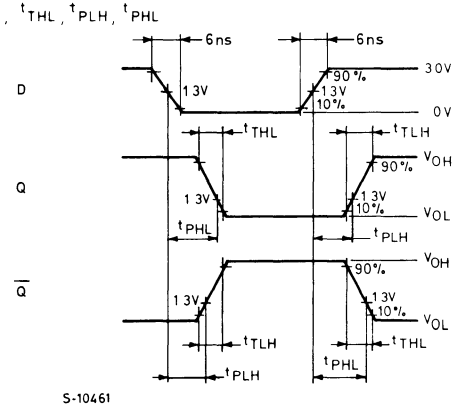
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the following equation.
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per Gate).

TEST CIRCUIT I_{CC} (Opr.)

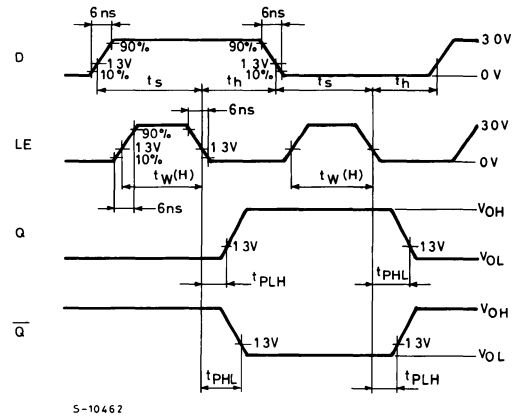


SWITCHING CHARACTERISTICS TEST WAVEFORM

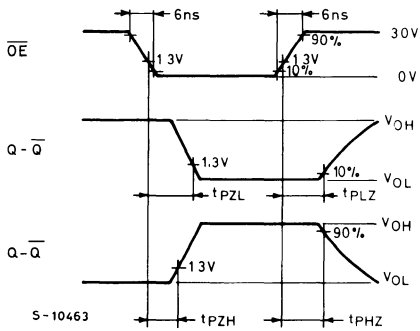
t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

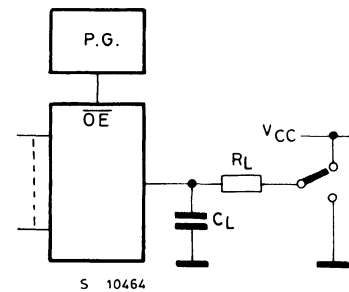


t_{PLH}, t_{PHL} (LE - Q, $\overline{Q}$)
t_s, t_h, t_w



t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}





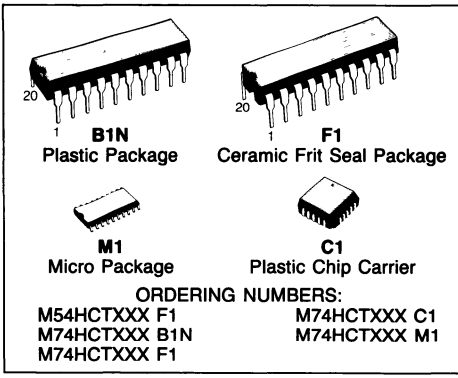
NOTE: EACH FLIP-FLOP WILL BE SET HIGH WHEN SWITCH IS CONNECTED TO GND LINE AND IT WILL BE SET LOW WHEN SWITCH IS CONNECTED TO V_{CC} LINE.

SGS-THOMSON MICROELECTRONICS

M54HCT564/574
M74HCT564/574

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT
HCT564 INVERTING - HCT574 NON-INVERTING

- HIGH SPEED
  f_{MAX} = 45 MHz (TYP) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS564/574



ORDERING NUMBERS:

M54HCTXXX F1
M74HCTXXX B1N
M74HCTXXX F1
M74HCTXXX C1
M74HCTXXX M1

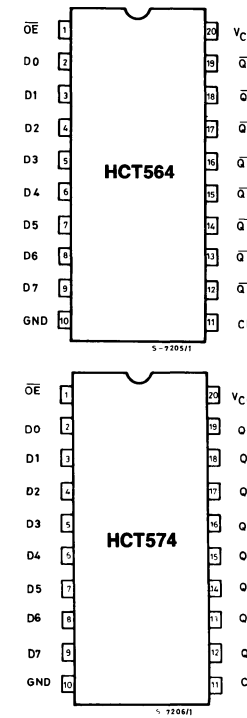
DESCRIPTION

The M54/74HCT564 and M54/74HCT574 are high speed CMOS OCTAL FLIP-FLOPS with 3-STATE OUTPUTS fabricated with silicon gate C²MOS technology. These ICs achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

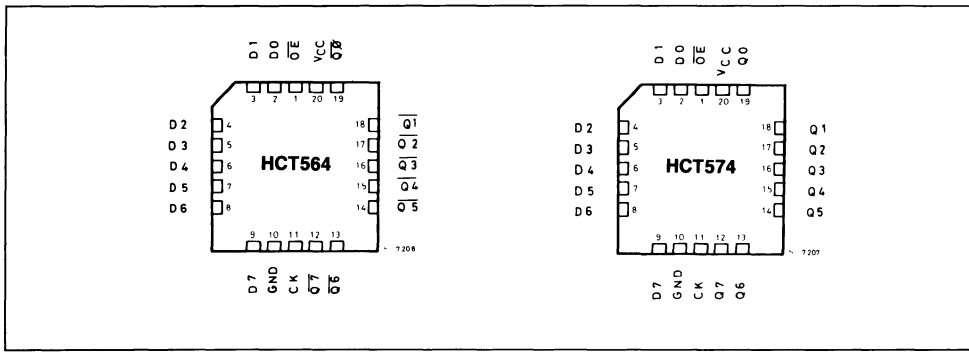
These 8-bit D-type flip-flops are controlled by a clock input (CK) and an output enable input ($\overline{OE}$). On the positive transition of clock, the Q outputs will be set inversely to the logic state that were set-up at the D inputs. While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level), and while high the outputs will be in a high impedance state. The output control does not affect the internal operation of flip-flops. That is, the old data can be retained or the new data can be entered even while the outputs are off. The application engineer has a choice of combination of inverting and non-inverting outputs, symmetrical and neighbouring input/output pin layout. The 3-state output configuration and the wide choice of outline makes bus-organized systems simple. All inputs are equipped with protection circuit against static discharge and transient excess voltage. These integrated circuits are totally compatible, input and output characteristics, with standard 54/74 LSTTL logic families.

M54HCT/74HCT devices are designed to directly interface HSC²MOS system with TTL and NMOS components. These components are also plug in replacements for LSTTL devices but with low power consumption.

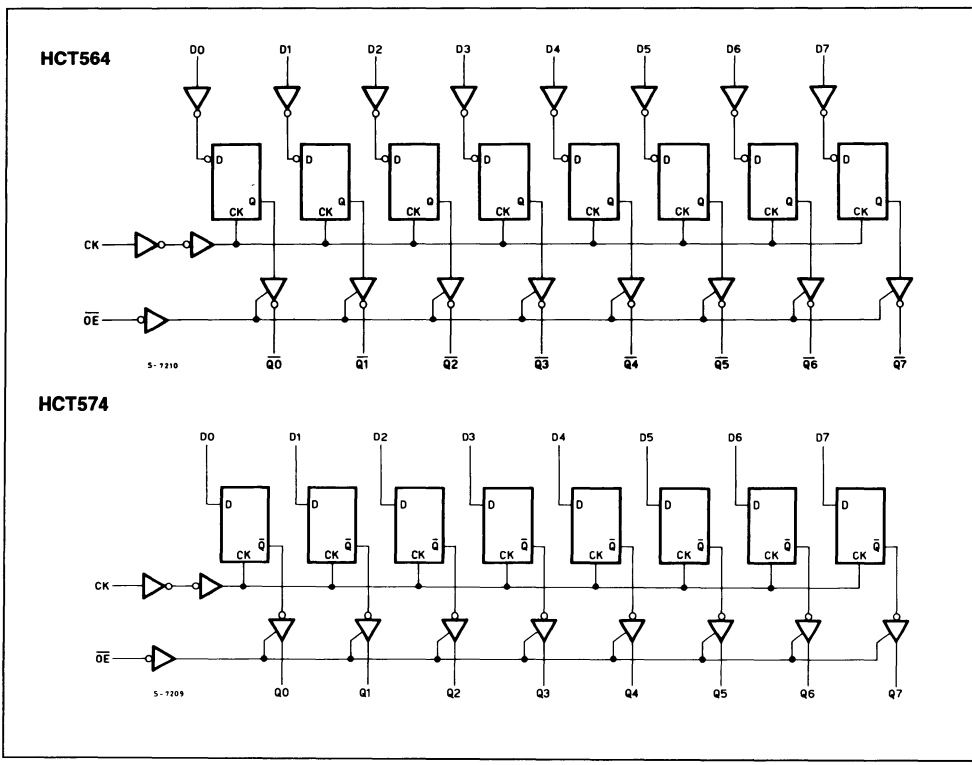
PIN CONNECTION (top view)



CHIP CARRIER



LOGIC DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q (HCT 574)	$\overline{Q}$ (HCT 564)
H	X	X	Z	Z
L	↓	X	NO CHANGE	NO CHANGE
L	↑	L	L	H
L	↑	H	H	L

X: DON'T CARE Z: HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C to 85°C.

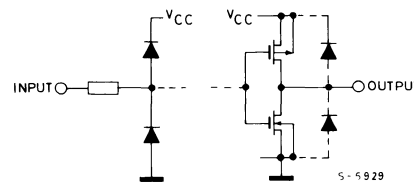
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		4.5 to 5.5	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time		0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 6.0			2.0 5.5	—	—	2.0	—	2	—	V
V_{IL}	Low Level Input Voltage	4.5 to 5.5			—	—	0.8	—	0.8	—	0.8	V
V_{OH}	High Level Output Voltage		V_I	I_O								
		4.5	V_{IH} or V_{IL}	−20 μA	4.4		—	4.4	—	4.4	—	V
		4.5		−6.0 mA	4.18	4.31	—	4.13	—	4.1		
V_{OL}	Low Level Output Voltage	4.5	V_{IH} or V_{IL}	20 μA	—		0.1	—	0.1	—	0.1	V
		4.5		6.0 mA	—	0.17	0.32	—	0.37	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{OZ}	3 State Output Current	5.5			—	—	±0.5	—	±5.0	—	±10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

INPUT AND OUTPUT EQUIVALENT CIRCUIT

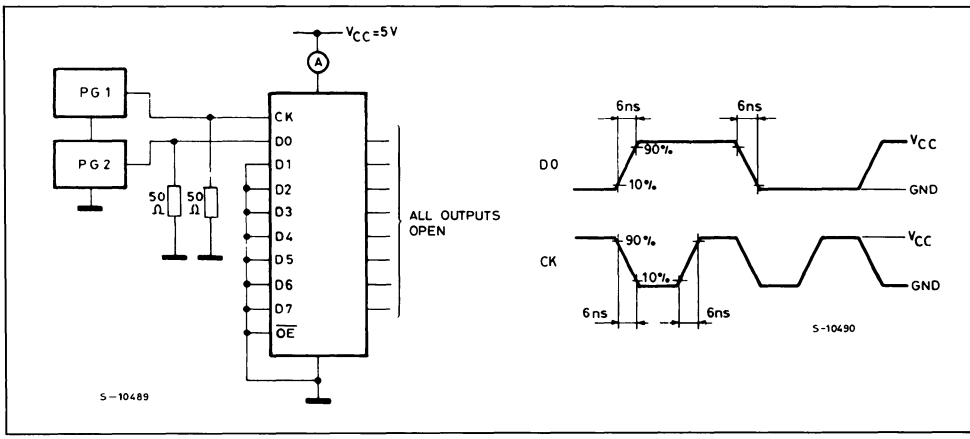


AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

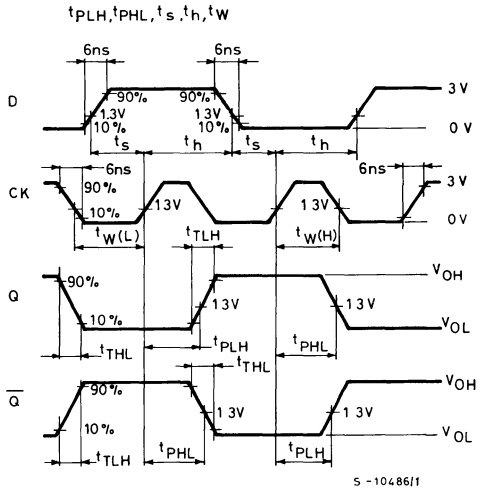
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5		—	7	12	—	15		18	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK-Q)	4.5		—	26	41	—	51		62	ns
f_{MAX}	Maximum Clock Frequency	4.5		25	38	—	20	—	17	—	MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CK)	4.5		—	8	15	—	19	—	22	ns
t_s	Minimum Set-up Time	4.5		—	1	10	—	13		15	ns
t_h	Minimum Hold Time	4.5		—	—	5	—	5		5	ns
t_{PZL} t_{PZH}	3-State Output Enable Time	4.5	R_L = 1KΩ	—	18	35	—	44		53	ns
t_{PLZ} t_{PHZ}	3-State Output Disable Time	4.5	R_L = 1KΩ	—	26	37	—	46		56	ns
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{OUT}	Output Capacitance			—	10	—	—	—	—	—	
C_{PD} (*)	Power Dissipation Capacitance		HCT564 HCT574	— —	60 57	— —	— —	— —	— —	— —	

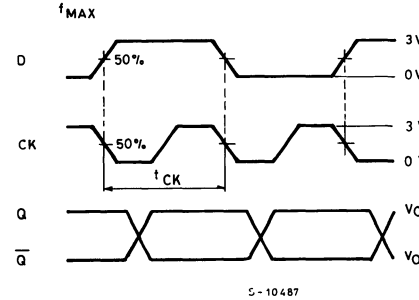
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the following equation.
$I_{CC}(Opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$.

TEST CIRCUIT I_{CC} (Opr.)



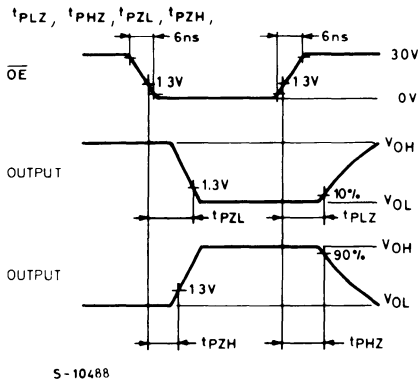
SWITCHING CHARACTERISTICS TEST WAVEFORM

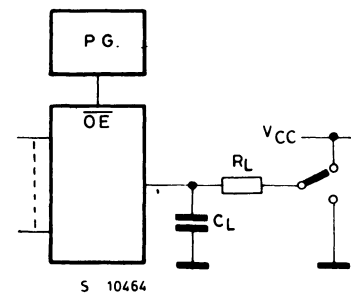




CLOCK DUTY: 50%

$f_{MAX} = \frac{1}{T_{CK}}$





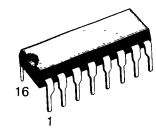
EACH FLIP-FLOP SHALL BE SET HIGH WHEN SWITCH IS CONNECTED TO GND LINE AND IT SHALL BE SET LOW WHEN SWITCH IS CONNECTED TO V_{CC} LINE.

SGS-THOMSON MICROELECTRONICS

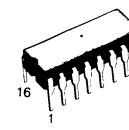
M54HC590
M74HC590

8-BIT BINARY COUNTER REGISTER (3-STATE)

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS (For RCO)
  15 LSTTL LOADS (For QA ~ QH)
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.) For QA ~ QH Output
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN) For RCO Output
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS590



B1N
Plastic Package



F1
Ceramic Frit Seal Package

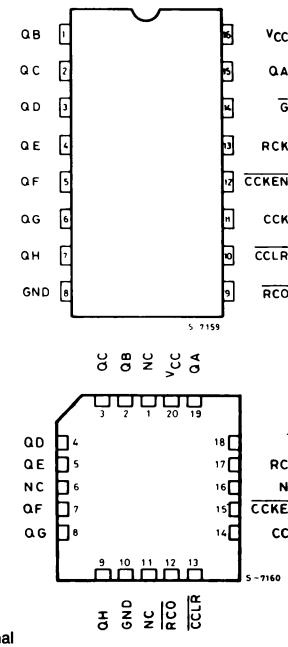
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC590 F1
M74HC590 B1N
M74HC590 F1
M74HC590 C1
M74HC590 M1

PIN CONNECTION (top view)



NC = No Internal Connection

DESCRIPTION

The M54/74HC590 is a high speed CMOS 8-BIT BINARY COUNTER REGISTER (3-STATE) fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
These devices each contain an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features a direct clear input $\overline{CCLR}$ and a count enable input $\overline{CCKEN}$. For cascading, a ripple carry output $\overline{RCO}$ is provided. Expansion is easily accomplished by tying $\overline{RCO}$ of the first stage to $\overline{CCKEN}$ of the second stage, etc. Both the counter and register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the counter state will always be one count ahead of the register. Internal circuitry prevents clocking from the clock enable. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

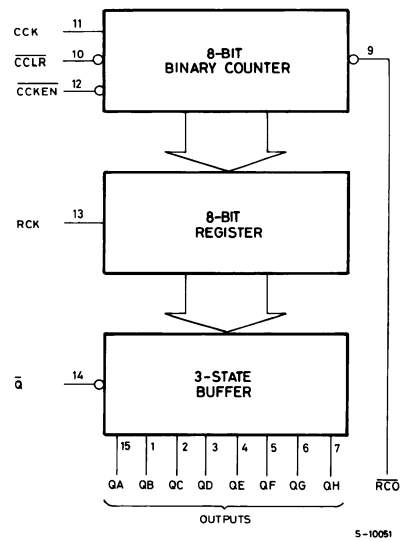
INPUTS					FUNCTION
$\overline{G}$	RCK	$\overline{CCLR}$	$\overline{CCKEN}$	CCK	
H	X	X	X	X	Q OUTPUTS DISABLE
L	X	X	X	X	Q OUTPUTS ENABLE
X	↑	X	X	X	COUNTER DATA IS STORED INTO REGISTER.
X	↓	X	X	X	REGISTER STATE IS NOT CHANGED.
X	X	L	X	X	COUNTER CLEAR
X	X	H	L	↑	ADVANCE ONE COUNT
X	X	H	L	↓	NO COUNT
X	X	H	H	X	NO COUNT

X: DON'T CARE

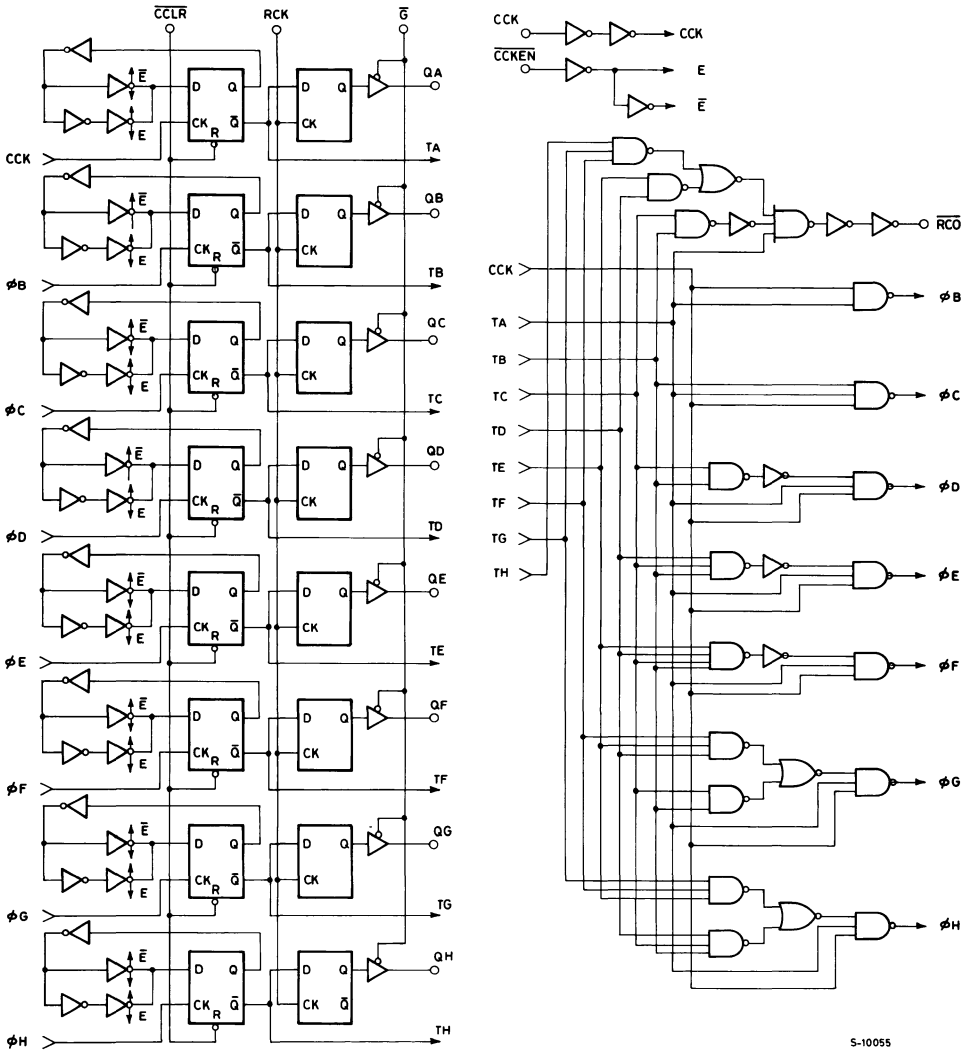
$\overline{RCO} = \overline{QA' \cdot QB' \cdot QC' \cdot QD' \cdot QE' \cdot QF' \cdot QG' \cdot QH'}$

(QA' ~ QH': INTERNAL OUTPUTS OF THE COUNTER)

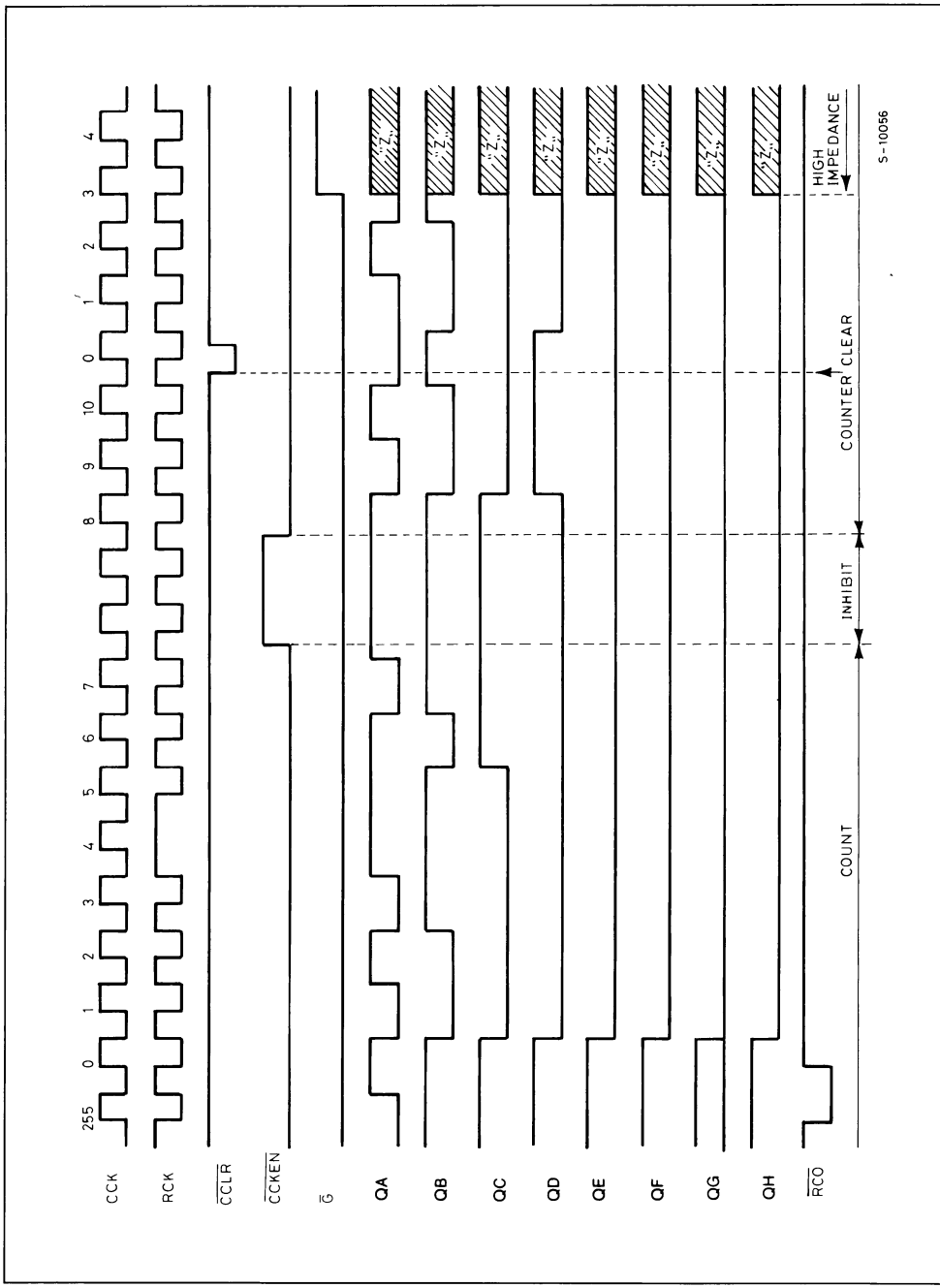
BLOCK DIAGRAM



LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 35 for QA ~ QH ± 20 for $\overline{RCO}$	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C
T_L	Lead Temperature 10sec	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC}	2 V 4.5V 6 V	0 to 1000 0 to 500 0 to 400	ns

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0 4.5 6.0	V_{IN} V_{IH} or V_{IL}	I_{OH} −20 μA	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	1.9 4.4 5.9	— — —	V
		4.5 6.0	QA ~ QH	−6.0 mA −7.8 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	
		4.5 6.0	$\overline{RCO}$	−4.0 mA −5.2 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OL}	Low Level Output Voltage	2.0	V_I	I_O	—	0.0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5	$Q_A \sim Q_H$	6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
		4.5	$\overline{RCO}$	4.0 mA		0.17	0.26	—	0.33	—	0.40	—
		6.0		5.2 mA		0.18	0.26	—	0.33	—	0.40	—
I_{OZ}	3-State Output Off-State Current	6.0	$V_{OUT} = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±10	μA
I_{IN}	Input Leakage Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

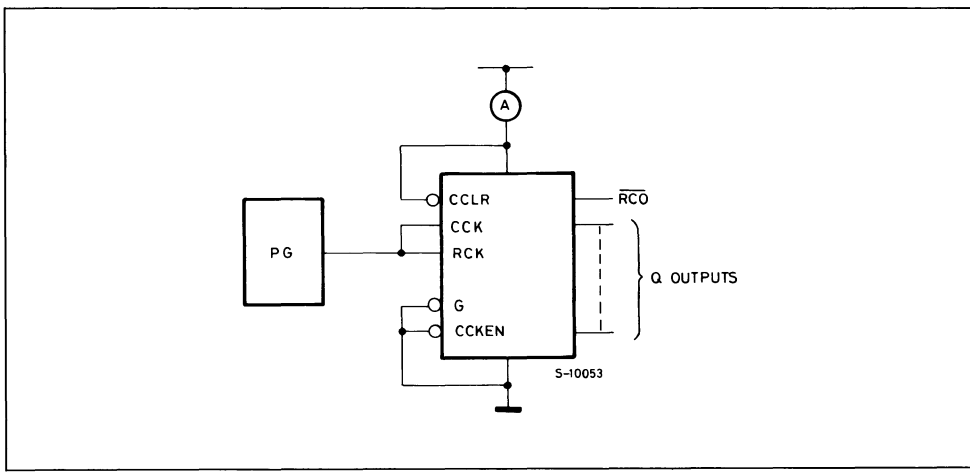
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (Q Outputs)	2.0		—	25	60	—	75		90	ns
		4.5		—	7	12	—	15		18	
		6.0		—	6	10	—	13		15	
t_{TLH} t_{THL}	Output Transition Time ($\overline{RCO}$)	2.0		—	30	75	—	95		110	
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CCK - $\overline{RCO}$)	2.0		—	124	240	—	300		360	
		4.5		—	31	48	—	60		72	
		6.0		—	26	41	—	51		61	
t_{PLH}	Propagation Delay Time ($\overline{CCLR}$-$\overline{RCO}$)	2.0		—	104	200	—	250		300	
		4.5		—	26	40	—	50		60	
		6.0		—	22	34	—	43		51	
t_{PLH} t_{PHL}	Propagation Delay Time (RCK-Q)	2.0		—	92	180	—	225		270	
		4.5		—	23	36	—	45		54	
		6.0		—	20	31	—	38		46	
f_{MAX}	Maximum Clock Frequency	2.0		4	8	—	3	—	2.6	—	MHz
		4.5		20	32	—	16	—	13	—	
		6.0		24	38	—	19	—	15	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CCK, RCK)	2.0		—	48	125	—	155		190	ns
		4.5		—	12	25	—	31		38	
		6.0		—	10	21	—	26		32	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CCLR}$)	2.0		—	92	200	—	250		300	ns
		4.5		—	23	40	—	50		60	
		6.0		—	20	34	—	43		51	

AC ELECTRICAL CHARACTERISTICS (Continued)

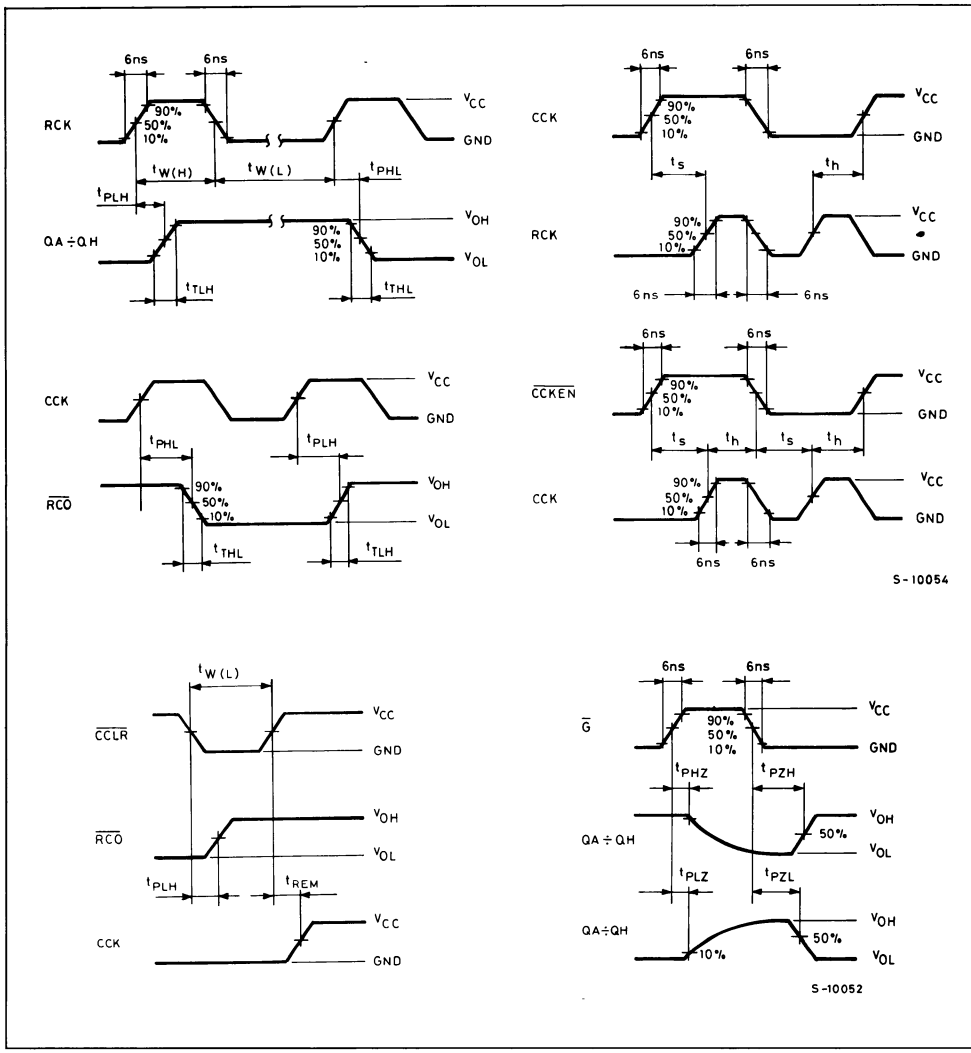
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{rem}	Minimum Removal Time ($\overline{CLEAR}$)	2.0		—	—	5	—	5	—	5	ns
		4.5		—	—	5	—	5	—	5	
		6.0		—	—	5	—	5	—	5	
t_s	Minimum Set-up Time ($\overline{CCKEN}$-CCK)	2.0		—	40	100	—	125	—	150	
		4.5		—	10	20	—	25	—	30	
		6.0		—	9	17	—	21	—	26	
t_s	Minimum Set-up Time (CCK, RCK)	2.0		—	128	245	—	305	—	370	
		4.5		—	32	49	—	61	—	74	
		6.0		—	27	42	—	52	—	63	
t_h	Minimum Hold Time	2.0		—	—	5	—	5	—	5	
		4.5		—	—	5	—	5	—	5	
		6.0		—	—	5	—	5	—	5	
t_{PZL} t_{PZH}	3-State Output Enable Time	2.0	$R_L = 1K\Omega$	—	68	135	—	170	—	205	
		4.5		—	17	27	—	34	—	41	
		6.0		—	14	23	—	29	—	35	
t_{PLZ} t_{PHZ}	3-State Output Disable Time	2.0	$R_L = 1K\Omega$	—	88	155	—	195	—	235	
		4.5		—	22	31	—	39	—	47	
		6.0		—	19	26	—	33	—	40	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD}(1)	Power Dissipation Capacitance			—	95	—	—	—	—	—	

Note (1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following equation: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

TEST WAVEFORM I_{CC} (Opr.)



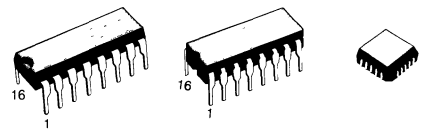
SWITCHING CHARACTERISTICS TEST WAVEFORM



8-BIT SHIFT REGISTER WITH OUTPUT LATCHES (3-STATE)

PRELIMINARY DATA

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS FOR QA to QH
  10 LSTTL LOADS FOR QH'
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 6mA MIN. FOR QA to QH
  4mA Min. FOR QH'
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS595

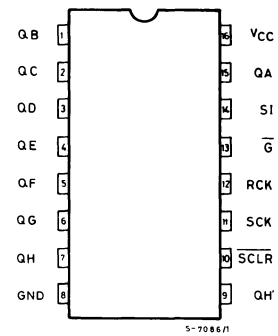


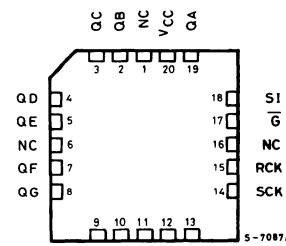
B1N Plastic Package | **F1** Ceramic Package | **C1** Chip Carrier

ORDERING NUMBERS:

M54HC595 F1 — M74HC595 F1
M74HC595 B1N — M74HC595 C1

PIN CONNECTIONS (top view)





NC = No Internal Connection

DESCRIPTION

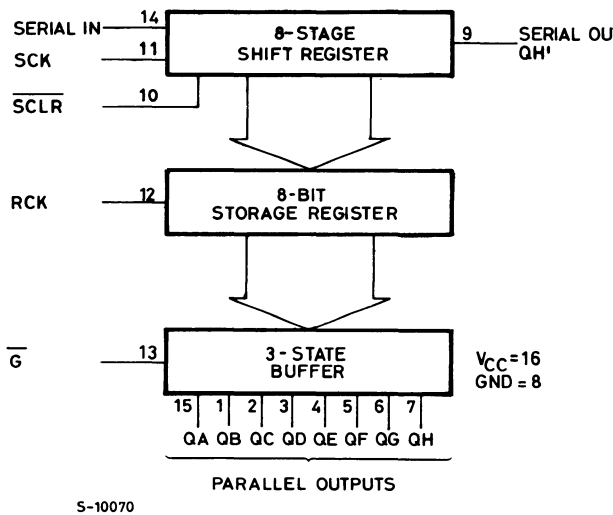
The M54/74HC595 is a high speed CMOS 8-BIT SHIFT REGISTERS/OUTPUT LATCHES (3-STATE) fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has 8 3-STATE outputs. Separate clocks are provided for both the shift register and the storage register.
The shift register has a direct-overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive-edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

TRUTH TABLE

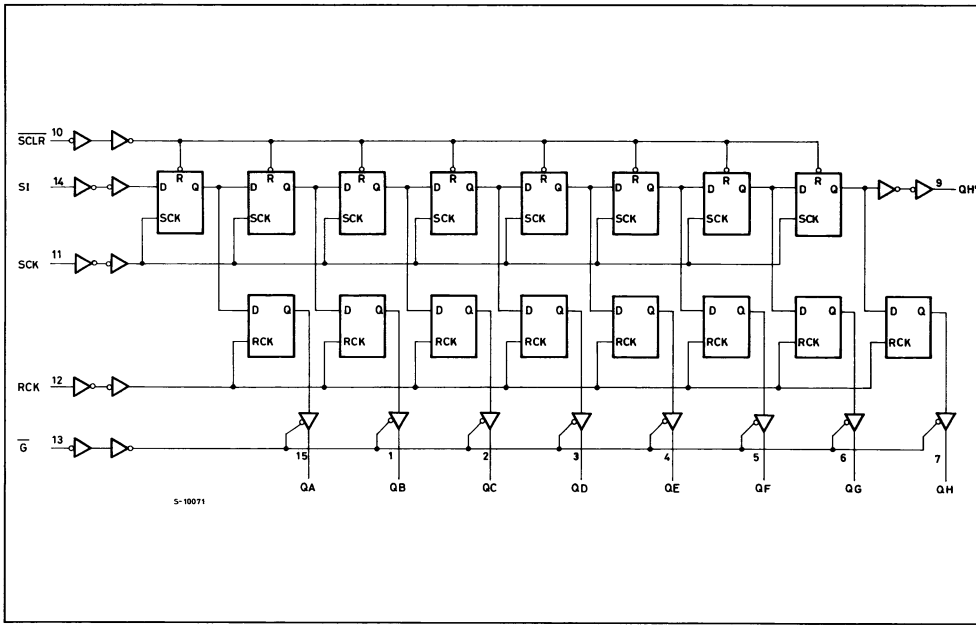
INPUTS					FUNCTION
SI	SCK	$\overline{SCLR}$	RCK	$\overline{G}$	
X	X	X	X	H	QA THRU QH OUTPUTS DISABLE
X	X	X	X	L	QA THRU QH OUTPUTS ENABLE
X	X	L	X	X	SHIFT REGISTER IS CLEARED
L	↑	H	X	X	FIRST STAGE OF S.R. BECOMES "L". OTHER STAGES STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY
H	↑	H	X	X	FIRST STAGE OF S.R. BECMOSE "H". OTHER STAGE STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY
X	↓	H	X	X	STATE OF S.R. IS NOT CHANGED
X	X	X	↑	X	S.R. DATA IS STORED INTO SOTRAGE REGISTER
X	X	X	↓	X	STORAGE REGISTER STATE IS NOT CHANGED

X: DON'T CARE

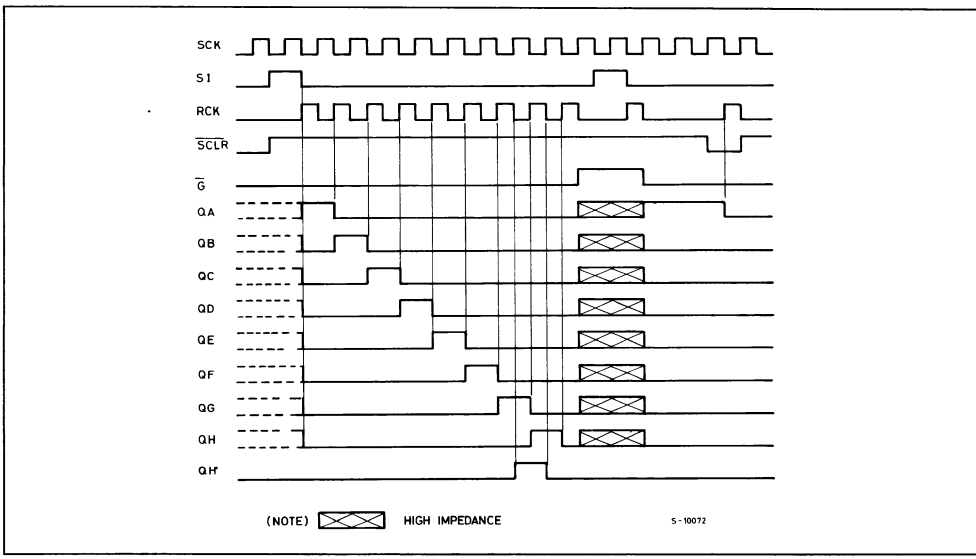
BLOCK DIAGRAM



LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current Per Pin QA-QH	± 35	mA
I_O	DC Output Current Per Pin QH'	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C
T_L	Lead Temperature 10 sec	300	°C

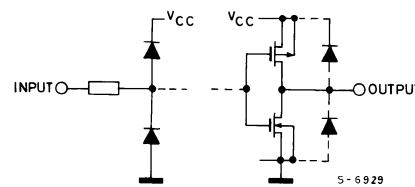
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V 4.5V 6 V	0 to 1000 0 to 500 0 to 400	ns

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage QA-QH	2.0	V_{IN}	I_{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage QA-QH	2.0	V_{IN}	I_{OH}	—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
V_{OH}	High Level Output Voltage QH'	2.0	V_{IN}	I_{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage QH'	2.0	V_{IN}	I_{OH}	—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{OZ}	3-State Output Off state Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	±0.5	—	±0.5	—	±10	
I_{CC}	Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	4	—	40	—	80	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (QA-QH) PARALLEL	2.0		—	25	60	—	75	—	90	ns
		4.5		—	7	12	—	15	—	18	
		6.0		—	6	10	—	13	—	15	
t_{TLH} t_{THL}	Output Transition Time (QH') SERIAL	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (SCK-QH')	2.0		—	80	160	—	200	—	240	ns
		4.5		—	20	32	—	40	—	40	
		6.0		—	17	27	—	34	—	41	
t_{PLH} t_{PHL}	Propagation Delay Time (RCK-QH)	2.0		—	88	175	—	220	—	265	ns
		4.5		—	22	35	—	44	—	53	
		6.0		—	19	30	—	37	—	45	
t_{PHL}	Propagation Delay Time ($\overline{SCLR}$-QH')	2.0		—	88	175	—	220	—	265	ns
		4.5		—	22	35	—	44	—	53	
		6.0		—	19	30	—	37	—	45	
f_{MAX}	Maximum Clock Frequency	2.0		6	12	—	5	—	4	—	MHz
		4.5		30	50	—	25	—	20	—	
		6.0		35	59	—	28	—	24	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (SCK, RCK)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{SCLR}$)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-up Time (SI-SCK)	2.0		—	20	50	—	65	—	75	ns
		4.5		—	5	10	—	13	—	15	
		6.0		—	4	9	—	11	—	13	
t_s	Minimum Set-up Time (SCK-RCK)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-up Time ($\overline{SCLR}$-RCK)	2.0		—	44	100	—	125	—	150	ns
		4.5		—	11	20	—	25	—	30	
		6.0		—	9	17	—	21	—	26	
t_h	Minimum Hold Time	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{REM}	Minimum Clear Removal Time	2.0		—	10	50	—	65	—	75	ns
		4.5		—	2	10	—	13	—	15	
		6.0		—	2	9	—	11	—	13	

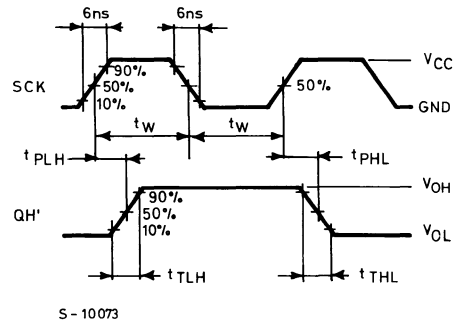
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PZL} t_{PZH}	3-State Output Enable Time	2.0 4.5 6.0	$R_L = 1k\Omega$	— — —	68 17 14	135 27 23	— — —	170 34 29	— — —	205 41 35	ns
t_{PLZ} t_{PHZ}	3-State Output Disable Time	2.0 4.5 6.0	$R_L = 1k\Omega$	— — —	64 21 18	150 30 26	— — —	190 38 33	— — —	225 45 38	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{OUT}	Output Capacitance			—	10	—	—	—	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance			—	254	—	—	—	—	—	pF

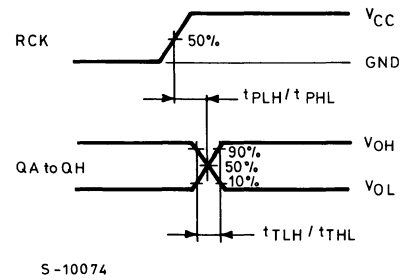
Note (*) C_{PD} is defined as the value of IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average opeating current is: $I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

WAVEFORM 1

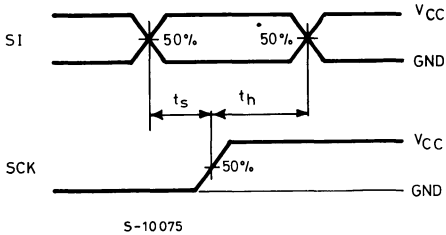


WAVEFORM 2



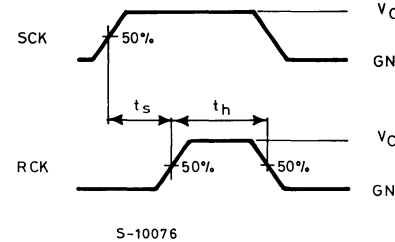
SWITCHING CHARACTERISTICS TEST WAVEFORM

WAVEFORM 3



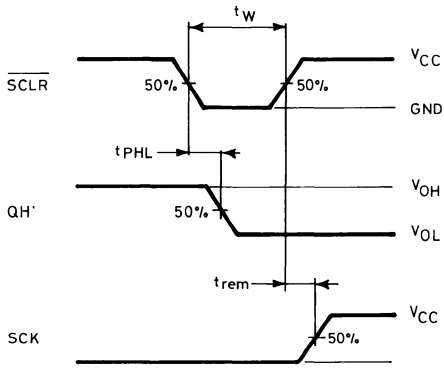
S-10075

WAVEFORM 4



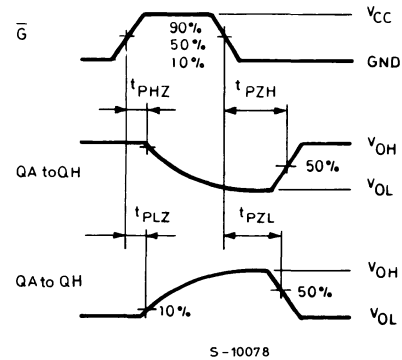
S-10076

WAVEFORM 5



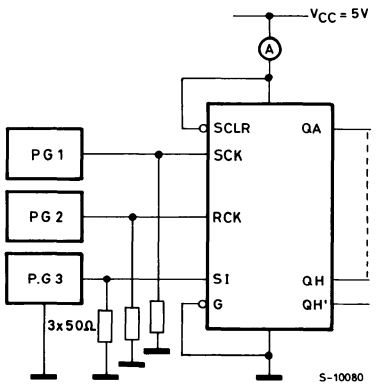
S-10077

WAVEFORM 6



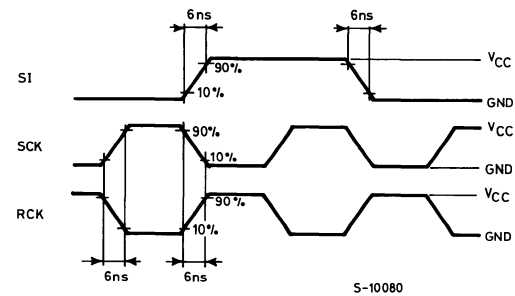
S-10078

TEST CIRCUIT I_{CC} (Opr.)



S-10080

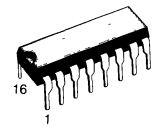
INPUT WAVEFORM



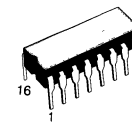
S-10080

8-BIT LATCH/SHIFT REGISTER

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (Min.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS597



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

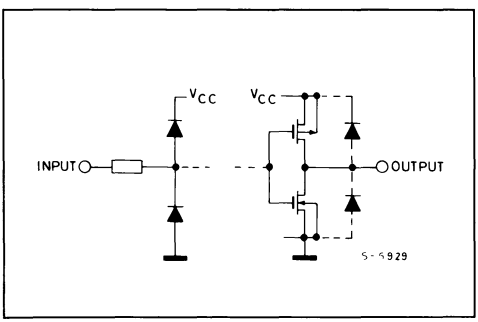
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC597 F1
M74HC597 B1N
M74HC597 F1
M74HC597 C1
M74HC597 M1

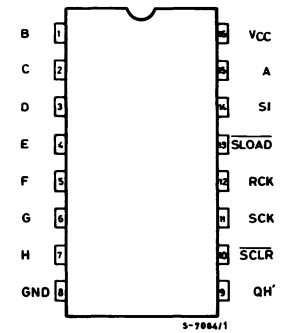
DESCRIPTION

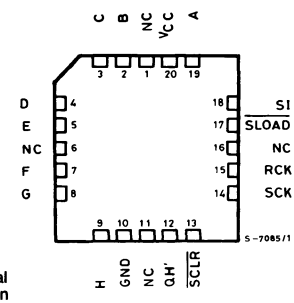
The M54/74HC597 is a high speed CMOS 8-BIT LATCH/SHIFT REGISTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
This devices comes in a 16-pin package and consist of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.
All inputs are equipped with protection circuits against static discharge and transient voltage excess.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





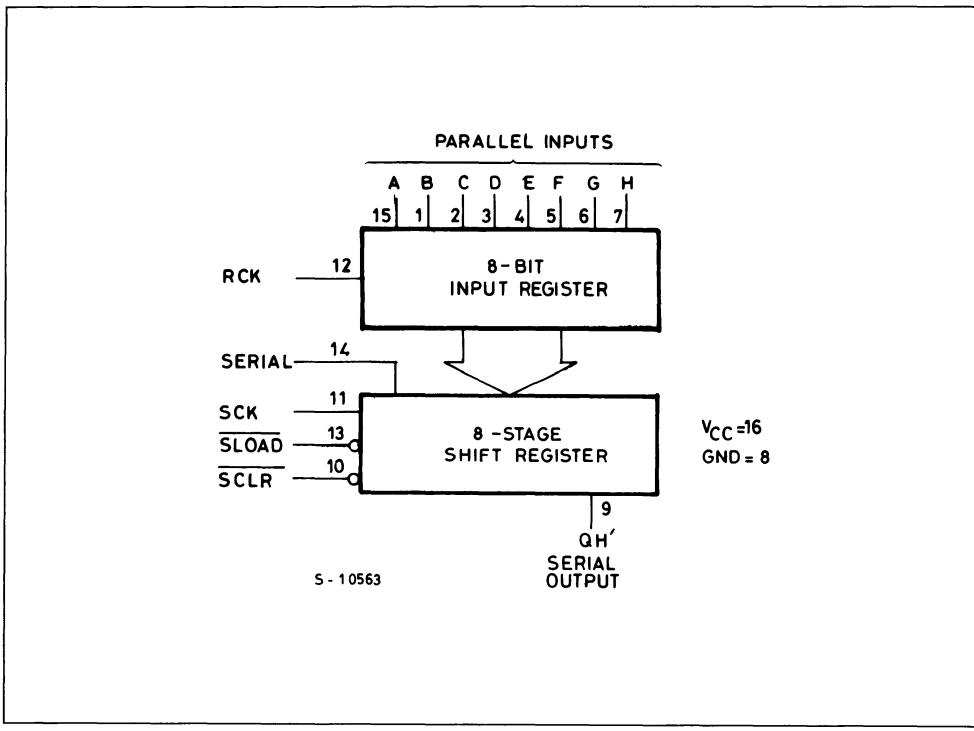
NC = No Internal Connection

TRUTH TABLE

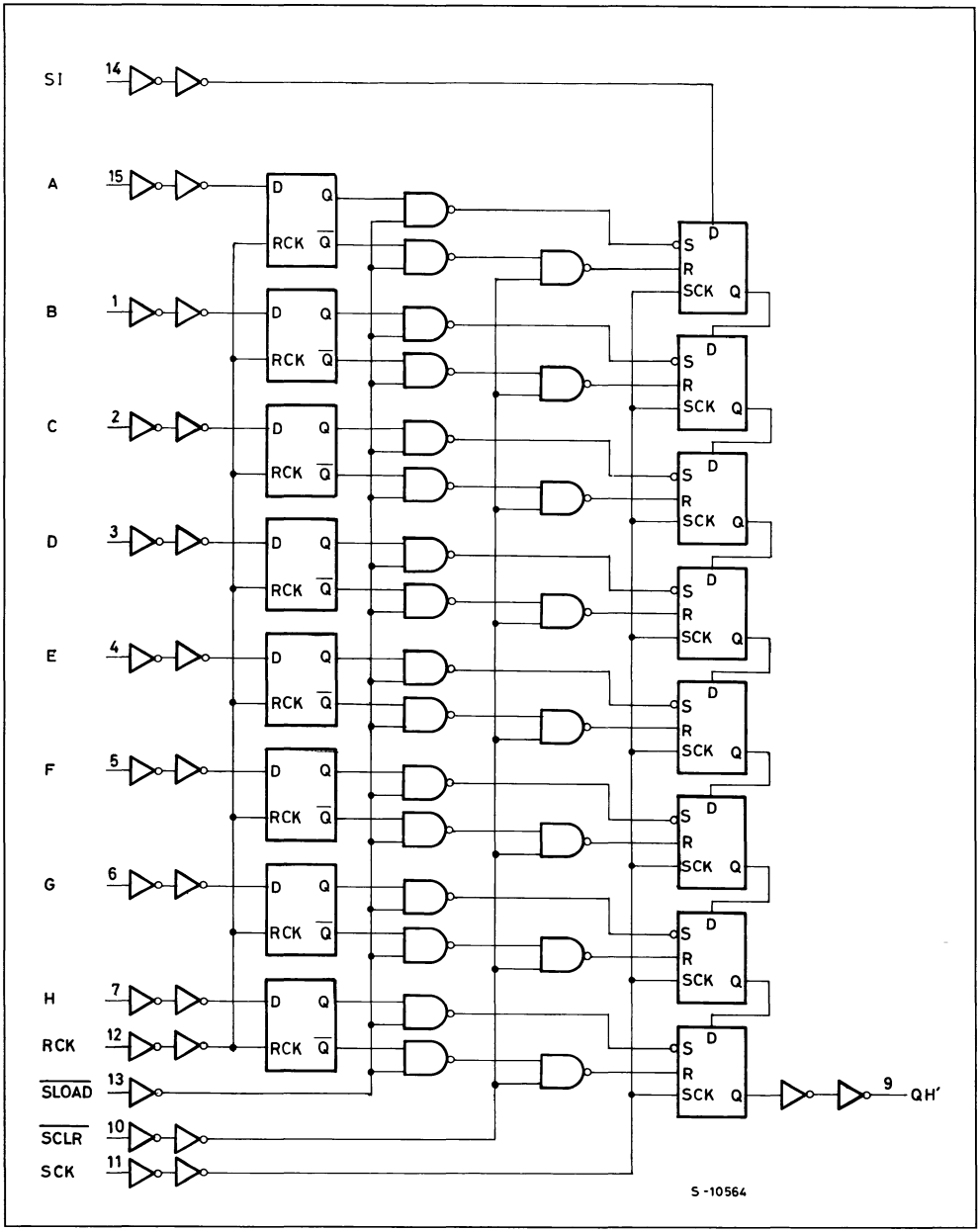
INPUTS					FUNCTION
SI	SCK	$\overline{SCLR}$	$\overline{SLOAD}$	RCK	
X	X	L	H	X	S.R. IS CLEARED TO "L"
X	X	H	L	X	INPUT REGISTER DATA IS STORE INTO S.R.
L	↑	H	H	X	FIRST STAGE OF S.R. BECOMES "L". OTHER STAGES STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY.
H	↑	H	H	X	FIRST STAGE OF S.R. BECOMES "H". OTHER STAGES STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY.
X	↓	H	H	X	STATE OF S.R. IS NOT CHANGED.
X	X	X	X	↑	INPUT DATA ON A~H LINE IS STORED INTO INPUT REGISTER
X	X	X	X	↓	STORAGE REGISTER STATE IS NOT CHANGED.

X= DON'T CARE

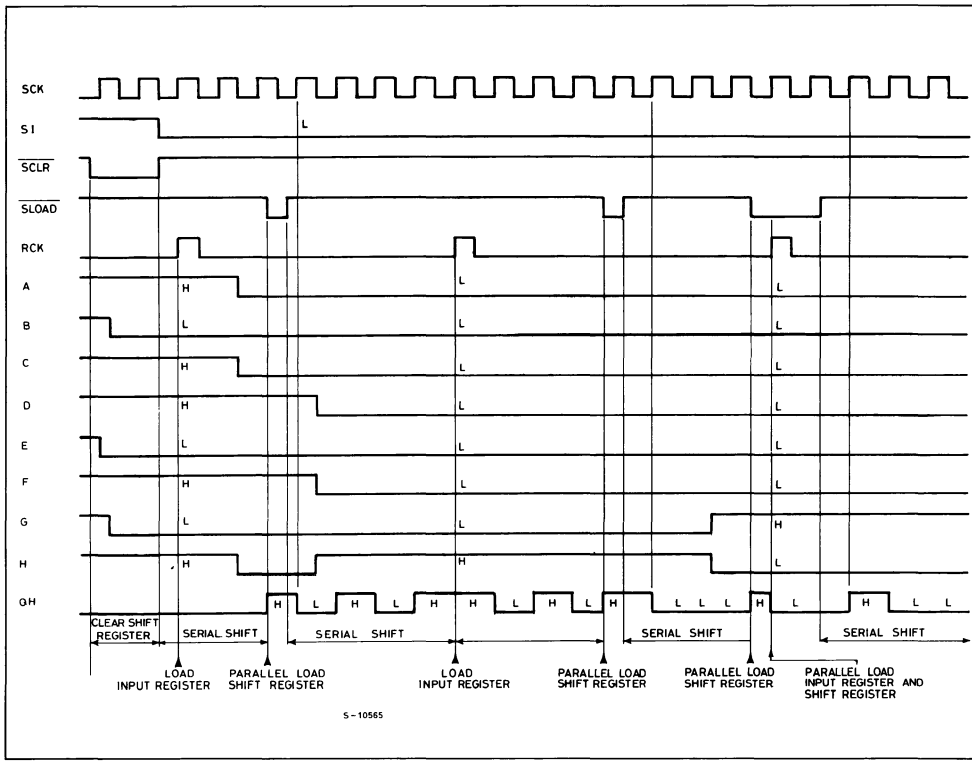
BLOCK DIAGRAM



LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V: 0 to 1000 V_{CC} = 4.5V: 0 to 500 V_{CC} = 6 V: 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0	V_{IN}	I_{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current	6.0	V_{IN} = V_{CC} or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_{IN} = V_{CC} or GND		—	—	4	—	40	—	80	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (SCK - QH')		15	24	ns
t_{PLH} t_{PHL}	Propagation Delay Time (RCK - QH')		23	36	ns
t_{PHL}	Propagation Delay Time ($\overline{SLOAD}$ - QH')		19	30	ns
t_{PHL}	Propagation Delay Time ($\overline{SCLR}$ - QH')		19	30	ns
f_{MAX}	Maximum Clock Frequency	33	60		MHz

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

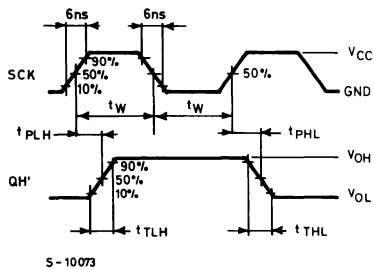
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (SCK-QH')	2.0		—	72	145	—	180	—	220	ns
		4.5		—	18	29	—	36	—	44	
		6.0		—	15	25	—	31	—	37	
t_{PLH} t_{PHL}	Propagation Delay Time (RCK-QH')	2.0	$\overline{SLOAD}$ = L	—	108	210	—	265	—	315	ns
		4.5		—	27	42	—	53	—	63	
		6.0		—	23	36	—	45	—	54	
t_{PHL}	Propagation Delay Time ($\overline{SLOAD}$-QH')	2.0		—	88	175	—	220	—	265	ns
		4.5		—	22	35	—	44	—	53	
		6.0		—	19	30	—	37	—	45	
t_{PHL}	Propagation Delay Time ($\overline{SCLR}$-QH')	2.0		—	92	175	—	220	—	265	ns
		4.5		—	23	35	—	44	—	53	
		6.0		—	20	30*	—	37	—	45	
f_{MAX}	Maximum Clock Frequency	2.0		6	14	—	5	—	4	—	MHz
		4.5		30	55	—	24	—	20	—	
		6.0		35	64	—	28	—	24	—	

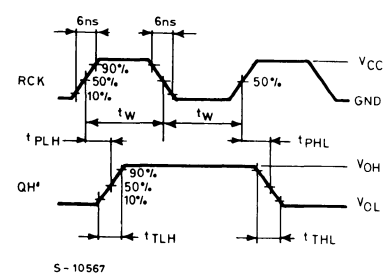
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (SCK, RCK)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
$t_{W(L)}$	Minimum Pulse Width $\overline{SCLR}$,$\overline{SLOAD}$	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_s	Minimum Set-up Time (SI-SCK)	2.0 4.5 6.0		— — —	20 5 4	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_s	Minimum Set-up Time (A...H-RCK)	2.0 4.5 6.0		— — —	20 5 4	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_s	Minimum Set-up Time (RCK-$\overline{SLOAD}$)	2.0 4.5 6.0		— — —	50 13 11	125 25 21	— — —	155 31 26	— — —	190 38 32	ns
t_h	Minimum Hold Time	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
t_{REM}	Minimum Removal Time ($\overline{SCLR}$,$\overline{SLOAD}$)	2.0 4.5 6.0		— — —	10 3 3	50 10 9	— — —	65 13 11	— — —	75 15 13	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	76	—	—	—	—	—	pF

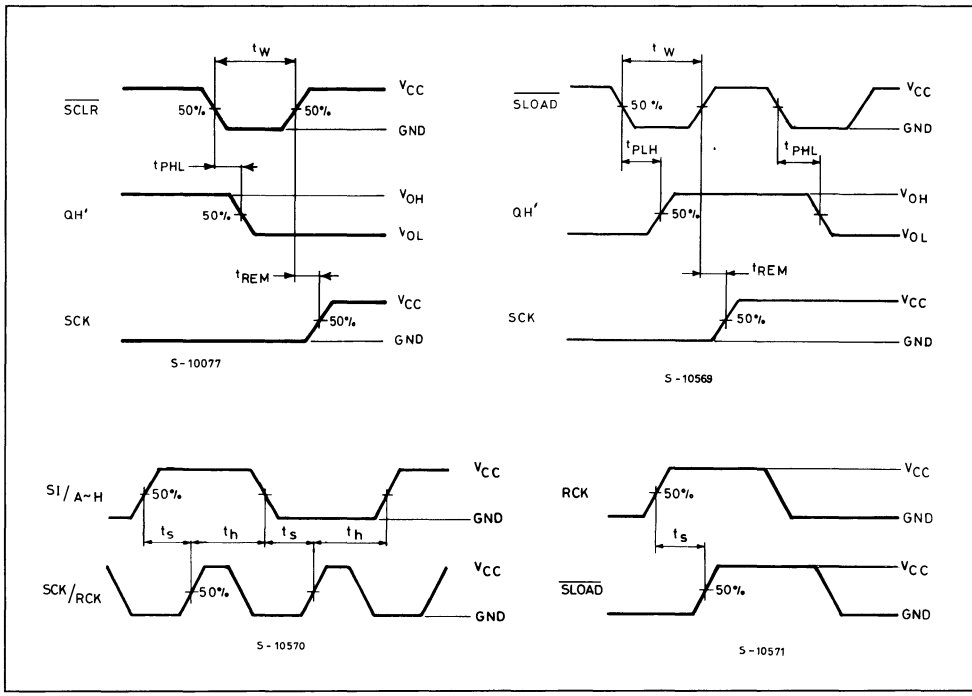
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average opeating current is: $I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

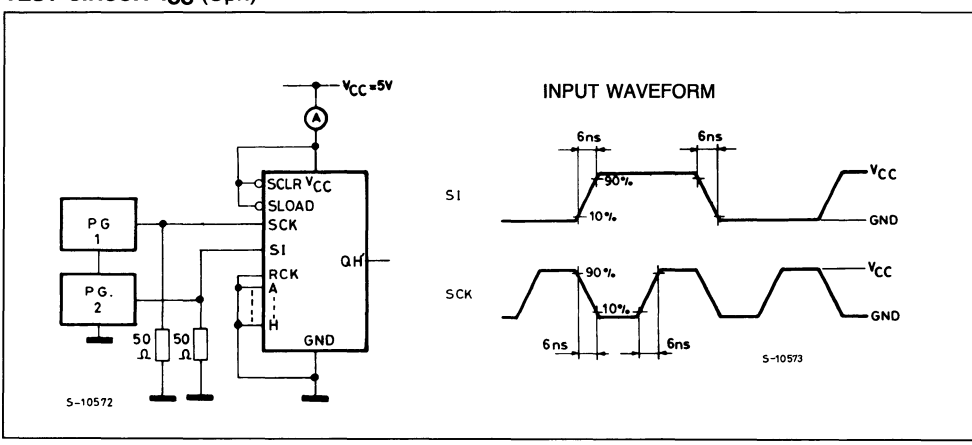




TEST WAVEFORM (Continued)



TEST CIRCUIT I_{CC} (Opr.)

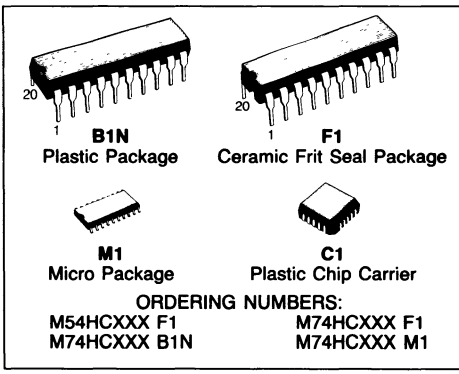


SGS-THOMSON MICROELECTRONICS

M54HC620/623
M74HC620/623

OCTAL BUS TRANSCEIVER
HC620 3-STATE INVERTING HC623 3-STATE, NON INVERTING

- HIGH SPEED
  t_{PD} = 10 ns [620], t_{PD} = 8 ns [623] (TYP) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH LS620/623



ORDERING NUMBERS:

M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX M1

DESCRIPTION

The M54/74HC620/623 are high speed CMOS OCTAL BUS TRANSCEIVERS fabricated in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

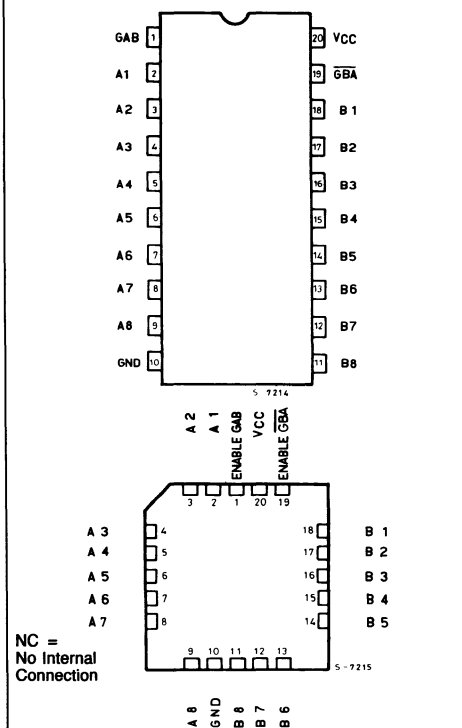
These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{GBA}$ and GAB). The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives these devices the capability to store data by simultaneous enabling of $\overline{GBA}$ and GAB).

Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'HC623 or complementary for the 'HC620. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION (top view)

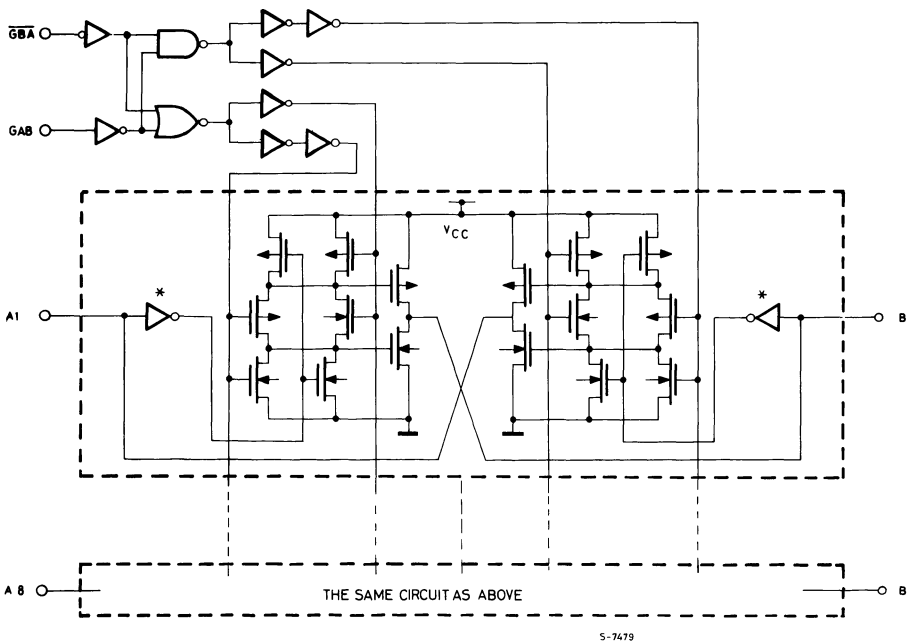


NC = No Internal Connection

TRUTH TABLE

INPUTS		FUNCTION		OUTPUTS	
GAB	$\overline{GBA}$	A Bus	B Bus	HC620	HC623
L	L	Output	Input	$A = \overline{B}$	A = B
H	H	Input	Output	$B = \overline{A}$	B = A
L	H	High Impedance		Z	Z
H	L	High Impedance		Z	Z

LOGIC DIAGRAM



NOTE: IN CASE OF HC623, INPUT INVERTERS MARKED* AT A BUS AND B BUS ARE ELIMINATED RESPECTIVELY

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

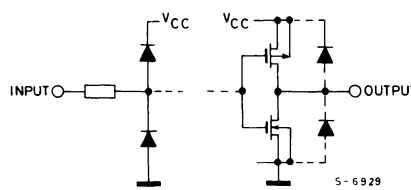
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series Operating Temperature 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0.0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{OZ}	3-State Output Off-State Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND $I_O = 0$		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	25	60	—	75	—	90	ns
		4.5		—	7	12	—	13	—	15	
		6.0		—	6	10	—	13	—	15	
t_{PLH} t_{PHL}	Propagation Delay Time (HC620)	2.0		—	48	100	—	125	—	150	ns
		4.5		—	12	20	—	25	—	30	
		6.0		—	10	17	—	21	—	26	
t_{PLH} t_{PHL}	Propagation Delay Time (HC623)	2.0		—	40	85	—	105	—	130	ns
		4.5		—	10	17	—	21	—	26	
		6.0		—	9	14	—	18	—	22	
t_{PZL} t_{PHZ}	3 State Output Enable Time	2.0	R_L 1KΩ	—	74	150	—	190	—	225	ns
		4.5		—	19	30	—	38		45	
		6.0		—	10	26	—	33	—	38	
t_{PZL} t_{PZH}	Output Disable Time	2.0	$R_L = 1K\Omega$	—	100	180	—	225	—	270	ns
		4.5		—	25	36	—	45	—	54	
		6.0		—	21	31	—	38	—	46	

AC ELECTRICAL CHARACTERISTICS (Continued)

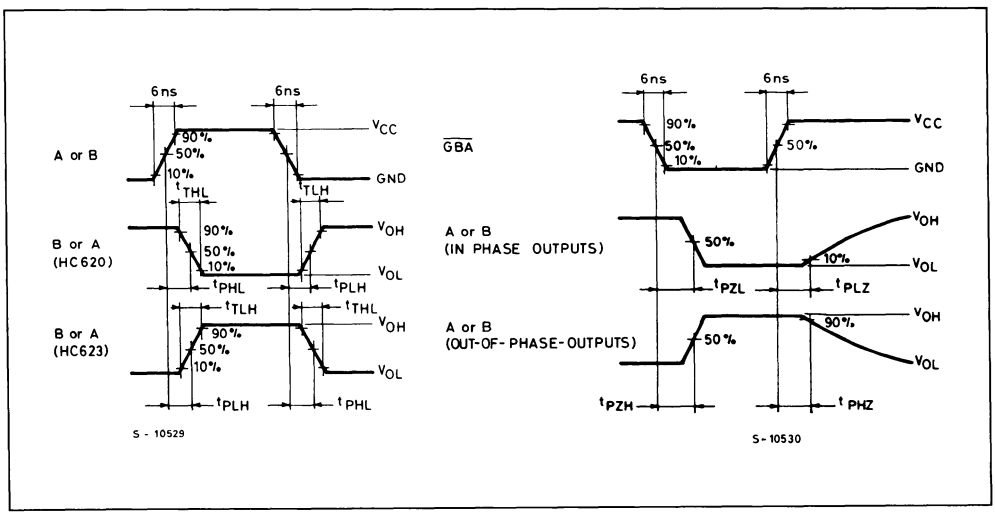
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
$C_{I/O}$	Bus Terminal Input capacitance		An, Bn	—	13	—	—	—	—	—	pF
C_{OUT}	Output Capacitance			—	10	—	—	—	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance		HC620 HC623	— —	— —	40 35	— —	— —			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

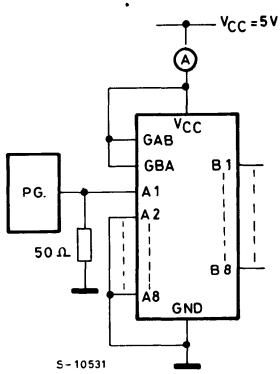
Average operating current is:

$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C_{PD} CALCULATION

C_{PD} is to be calculated with the following formula by using the measured value of I_{CC} (Opr.) in the test circuit opposite.

$$C_{PD} = \frac{I_{CC}\ (Opr.)}{f_{IN} \cdot V_{CC}}$$

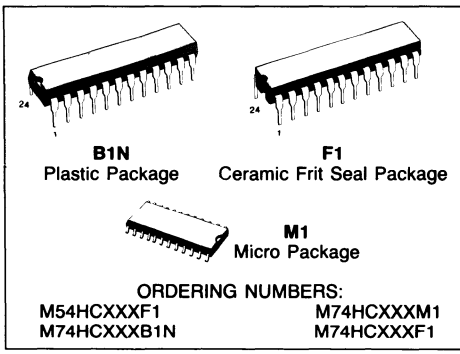
In determining the typical value of C_{PD}, a relatively high frequency of 1MHz was applied to f_{IN}, in order to eliminate any error caused by the quiescent supply current.

SGS-THOMSON MICROELECTRONICS

M54/74HC646
M54/74HC648

HC646 OCTAL BUS TRANSCEIVER/REGISTER (3-STATE)
HC648 OCTAL BUS TRANSCEIVER/REGISTER (INVERTING-3 STATE)

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (Min.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS646/648



ORDERING NUMBERS:

M54HCXXXF1	M74HCXXXM1
M74HCXXXB1N	M74HCXXXF1

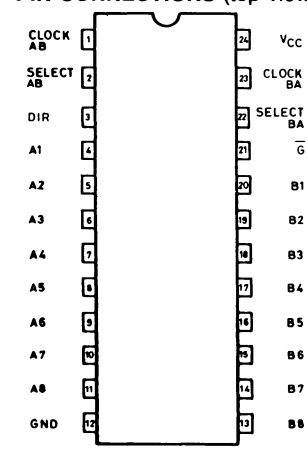
DESCRIPTION

The M54/74HC646/648 are high speed CMOS OCTAL BUS TRANSCEIVERS AND REGISTERS, (3 STATE) fabricated in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

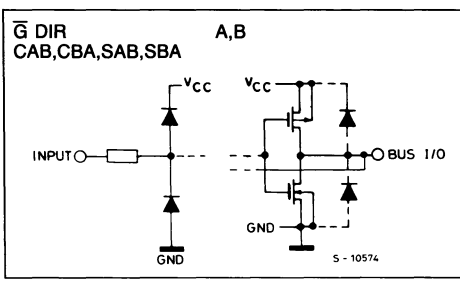
These devices consist of bus transceiver circuits with 3-state output, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (Clock AB - or Clock BA). Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

The select controls (Select AB select BA) can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low).
In the isolation mode (enable $\overline{G}$ high), "A" data may be stored in one register and/or "B" data may be stored in the other register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT



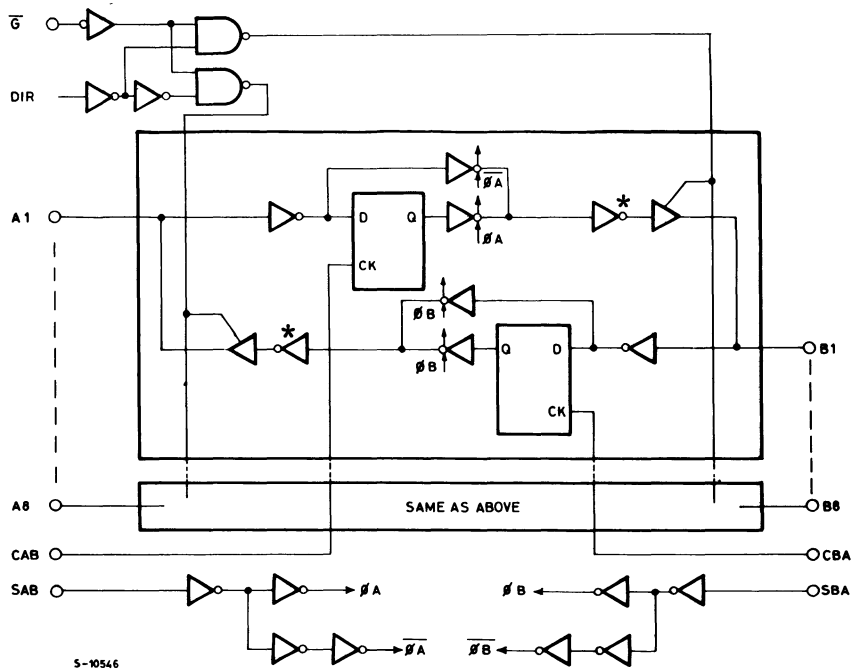
TRUTH TABLE

M54/74HC646 (The truth table for M54/74HC648 is the same as this, but with the outputs inverted)

$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A	B	FUNCTION
H	X					INPUTS	INPUTS	Both the A bus and the B bus are inputs.
		X	X	X	X	Z	Z	The output functions of the A and B bus are disabled.
		↓	↓	X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to the internal flip-flops. Data at the bus will be stored on low to high transition of the clock inputs.
L	H					INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs.
		X	X*	L	X	L H	L H	The data at the A bus are displayed at the B bus.
		↓	X*	L	X	L H	L H	The data at the A bus are displayed at the B bus. The data of A bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X	X*	H	X	X	Qn	The data stored to the internal flip-flops are displayed at the B bus.
		↓	X*	H	X	L H	L H	The data at the A bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus
L	L					OUTPUTS	OUTPUTS	The B bus are inputs and the A bus are outputs.
		X*	X	X	L	L H	L H	The data at the B bus are displayed at the A bus.
		X*	↓	X	L	L H	L H	The data at the B bus are displayed at the A bus. The data of 8 bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X*	X	X	H	Qn	X	The data stored to the internal flip-flops are diplayed at the B bus.
		X*	↓	X	H	L H	L H	The data at the B bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus.

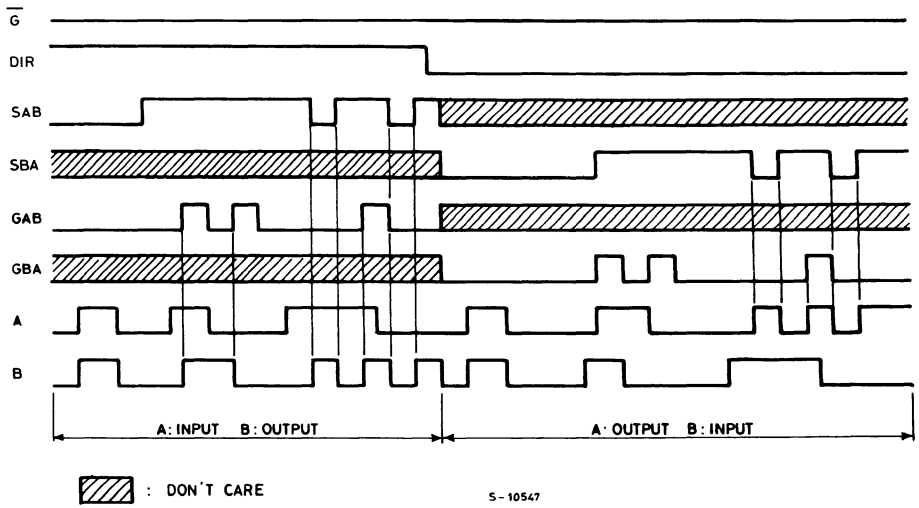
X: DON'T CARE.
Z: HIGH IMPEDANCE.
Qn: THE DATA STORED TO THE INTERNAL FLIP-FLOPS BY MOST RECENT LOW TO HIGH TRANSITION OF THE CLOCK INPUTS.
*: THE DATA AT THE A AND B BUS WILL BE STORED TO THE INTERNAL FLIP-FLOPS ON EVERY LOW TO TRANSITION OF THE CLOCK INPUTS.

LOGIC DIAGRAM (HC648)



NOTE: IN CASE OF M54/74HC646 OUTPUT INVERTER MARKED* AT A BUS AND B BUS ARE ELIMINATED.

TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400		ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0 4.5 6.0	V_{IN} V_{IH} or	I_{OH} −20 μA	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	1.9 4.4 5.9	— — —	V
		4.5 6.0	V_{IL}	−6.0 mA −7.8 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	

DC SPECIFICATIONS (Continued)

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current *	6.0	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{OZ}	3-State Output Off state Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±10	
I_{CC}	Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	4.0	—	40.0	—	80.0	

*: Applicable only to DIR, $\overline{G}$, CAB, SAB, SBA input.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	25	60	—	75	—	90	ns
		4.5		—	7	12	—	15	—	18	
		6.0		—	6	10	—	13	—	15	
t_{PLH} t_{PHL}	Propagation Delay Time (BUS-BUS)	2.0		—	92	180	—	225	—	270	ns
		4.5		—	23	36	—	45	—	54	
		6.0		—	20	31	—	38	—	46	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-BUS)	2.0		—	124	240	—	300	—	360	ns
		4.5		—	31	48	—	60	—	72	
		6.0		—	26	41	—	51	—	61	
t_{PLH} t_{PHL}	Propagation Delay Time (SELECT-BUS)	2.0		—	112	220	—	275	—	330	ns
		4.5		—	28	44	—	55	—	66	
		6.0		—	24	37	—	47	—	56	
$t_{W(H)}$ $t_{W(L)}$	Minimum Clock Pulse Width	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Data Set-up Time	2.0		—	5	50	—	65	—	75	ns
		4.5		—	1	10	—	13	—	15	
		6.0		—	1	9	—	11	—	13	
t_h	Minimum Data Hold Time	2.0		—	—	25	—	30	—	40	ns
		4.5		—	—	5	—	6	—	8	
		6.0		—	—	5	—	5	—	7	

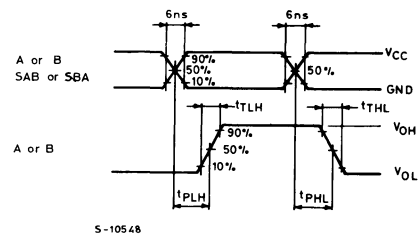
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PZL} t_{PZH}	3-State Output Enable Time ($\overline{G}$, DIR)	2.0 4.5 6.0	$R_L = 1k\Omega$	— — —	104 26 22	205 41 35	— — —	250 50 43	— — —	310 62 53	ns
t_{PLZ} t_{PHZ}	3-State Output Disable Time ($\overline{G}$, DIR)	2.0 4.5 6.0	$R_L = 1k\Omega$	— — —	104 29 25	210 42 36	— — —	250 50 43	— — —	310 60 50	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{OUT}	Output Capacitance		BUS I/O	—	13	—	—	—	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance			—	46	—	—	—	—	—	pF

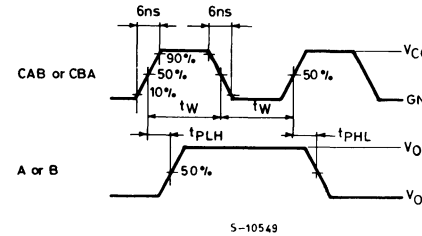
Note (*) C_{PD} is defined as the value of IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average opeating current is: $I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per bit)

SWITCHING CHARACTERISTICS TEST WAVEFORM

WAVEFORM 1

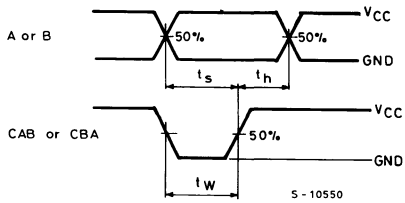


WAVEFORM 2

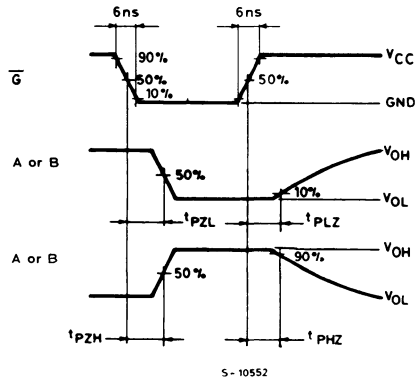


SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)

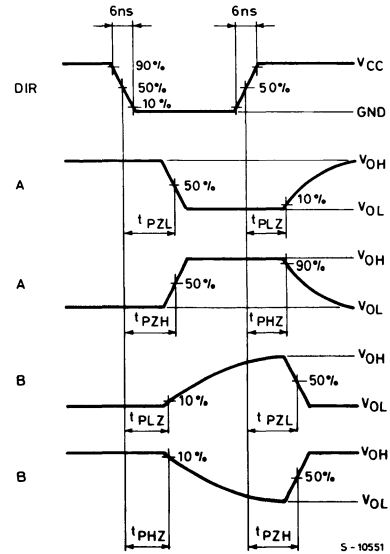
WAVEFORM 3



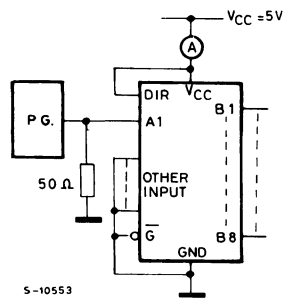
WAVEFORM 4



WAVEFORM 5



TEST CIRCUIT I_{CC} (Opr.)



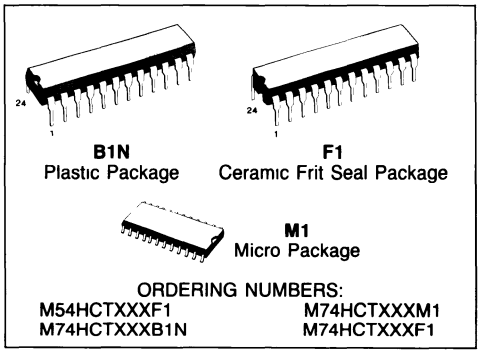
INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

SGS-THOMSON MICROELECTRONICS

M54/74HCT646
M54/74HCT648

HCT646 OCTAL BUS TRANSCEIVER/REGISTER (3-STATE)
HCT648 OCTAL BUS TRANSCEIVER/REGISTER (INVERTING-3 STATE)

- LOW POWER DISSIPATION
  $I_{CC} = 4\mu A$ (MAX.) at $T_A = 25°C$
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN) V_{IL} = 0.8V (MAX.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OL}| = I_{OL}$ = 6mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS646/648



B1N
Plastic Package

F1
Ceramic Frit Seal Package

M1
Micro Package

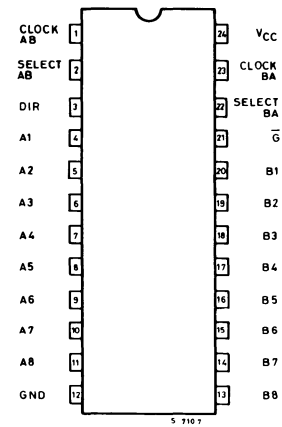
ORDERING NUMBERS:

M54HCTXXXF1	M74HCTXXXM1
M74HCTXXXB1N	M74HCTXXXF1

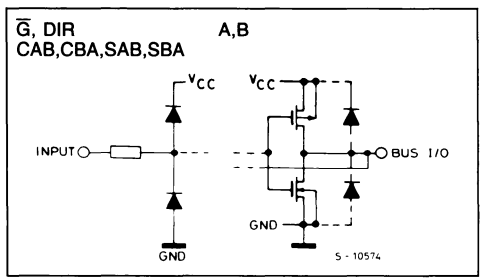
DESCRIPTION

The M54/74HCT646/648 are high speed CMOS OCTAL BUS TRANSCEIVERS AND REGISTERS, (3-STATE), fabricated in silicon gate C²MOS technology. They have the same high speed performance of LSTTL, combined with true CMOS low power consumption. These devices consist of bus transceiver circuits with 3-state output, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the "A" or "B" bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (Clock AB - or Clock BA). Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (Select AB Select BA) can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable $\overline{G}$ is active (low). In the isolation mode (enable $\overline{G}$ high), "A" data may be stored in one register and/or "B" data may be stored in the other register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. All inputs are equipped with protection circuits against static discharge and transient excess voltage. These integrated circuit have totally compatible, input and output characteristics, with standard 54/74 LSTTL logic families. M54HCT/74HCT devices are designed to directly interface HSC² MOS systems with TTL and NMOS components. These devices are also plug in replacements for LSTTL devices giving a reduction in power consumption.

PIN CONNECTIONS (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT



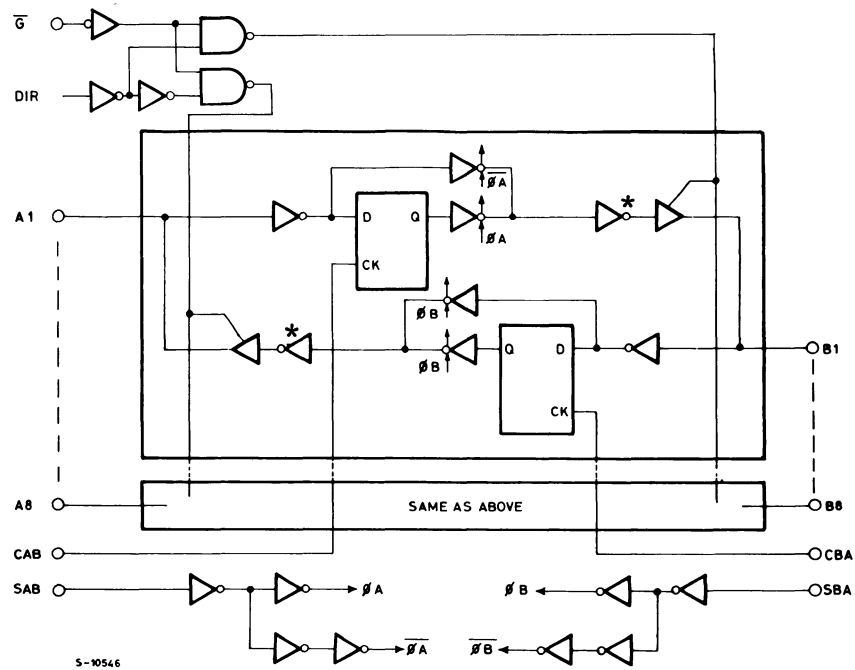
TRUTH TABLE

M54/74HCT646 (The truth table for M54/74HCT648 is the same as this, but with the outputs inverted)

$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A	B	FUNCTION
H	X					INPUTS	INPUTS	Both the A bus and the B bus are inputs.
		X	X	X	X	Z	Z	The output functions of the A and B bus are disabled.
		↑	↑	X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to the internal flip-flops. Data at the bus will be stored on low to high transition of the clock inputs.
L	H					INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs.
		X	X*	L	X	L H	L H	The data at the A bus are displayed at the B bus.
		↑	X*	L	X	L H	L H	The data at the A bus are displayed at the B bus. The data of A bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X	X*	H	X	X	Qn	The data stored to the internal flip-flops are displayed at the B bus.
		↑	X*	H	X	L H	L H	The data at the A bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus
L	L					OUTPUTS	OUTPUTS	The B bus are inputs and the A bus are outputs.
		X*	X	X	L	L H	L H	The data at the B bus are displayed at the A bus.
		X*	↑	X	L	L H	L H	The data at the B bus are displayed at the A bus.The data of 8 bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X*	X	X	H	Qn	X	The data stored to the internal flip-flops are diplayed at the B bus.
		X*	↑	X	H	L H	L H	The data at the B bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus.

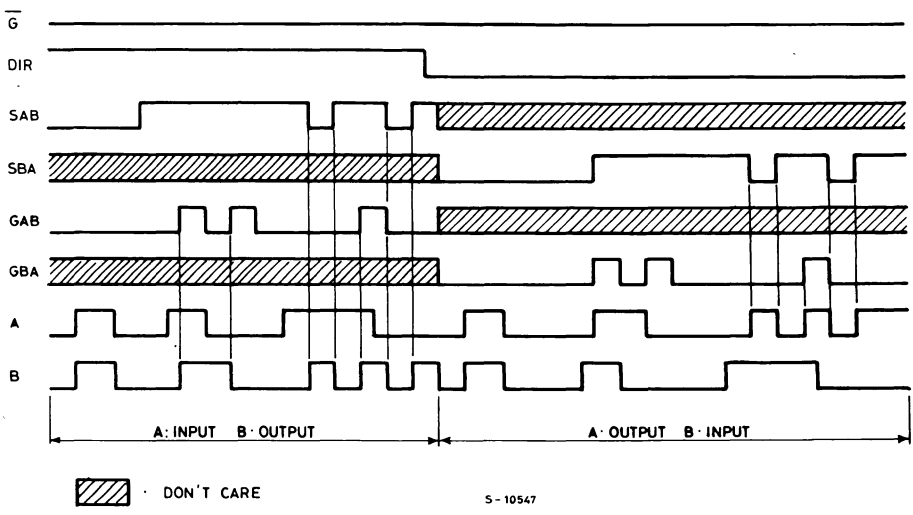
X : DON'T CARE.
Z : HIGH IMPEDANCE.
QN: THE DATA STORED TO THE INTERNAL FLIP-FLOPS BY MOST RECENT LOW TO HIGH TRANSITION OF THE CLOCK INPUTS.
* : THE DATA AT THE A AND B BUS WILL BE STORED TO THE INTERNAL FLIP-FLOPS ON EVERY LOW TO TRANSITION OF THE CLOCK INPUTS.

LOGIC DIAGRAM (HCT648)



NOTE: IN CASE OF M54/74HCT646 OUTPUT INVERTER MARKED * AT A BUS AND B BUS ARE ELIMINATED

TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
Tstg	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Limit	Unit
V_{CC}	Supply Voltage		4.5 to 5.5	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time		0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 6.0			2.0	—	—	2.0	—	2.0	—	V
V_{IL}	Low Level Input Voltage	4.5 to 5.5			—	—	0.8	—	0.8	—	0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I	I_O								V
			V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
				−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	

DC SPECIFICATIONS (Continued)

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OL}	Low Level Output Voltage	4.5	V_I	I_O								
			V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
				6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current*	5.5	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{OZ}	3-State Output Off-State Current	4.5	$V_O = V_{CC}$ or GND $V_I = V_{IH}$ or V_{IL}		—	—	±0.5	—	±5.0	—	±10.0	
I_{CC}	Quiescent Supply Current	5.5	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA
I_{CC}			Per input: $V_{IN} = 2.4V$ or 0.5V Other input: V_{CC} or GND		—	—	2.0	—	2.9	—	3.0	mA

*: Applicable only to DIR, $\overline{G}$, CAB, CBA, SAB, SBA input.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5		—	7	12	—	15	—	18	ns
t_{PLH} t_{PHL}	Propagation Delay Time (BUS-BUS)	4.5		—	20	31	—	39	—	47	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-BUS)	4.5		—	30	46	—	58	—	69	ns
t_{PLH} t_{PHL}	Propagation Delay Time (SELECT-BUS)	4.5		—	31	48	—	60	—	72	ns
$t_{W(H)}$ $t_{W(L)}$	Minimum Clock Pulse Width	4.5		—	11	20	—	25	—	30	ns
t_s	Minimum Data Set-up Time	4.5		—	4	10	—	13	—	15	ns
t_h	Minimum Data Hold Time	4.5		—	—	5	—	5	—	5	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

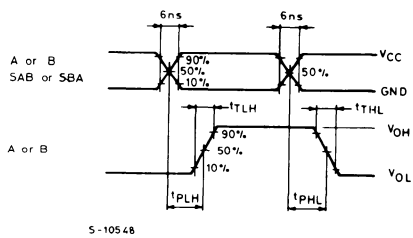
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PZL} t_{PZH}	3-State Output Enable Time ($\overline{G}$, BUS)	4.5	$R_L = 1k\Omega$	—	26	38	—	48	—	57	ns
t_{PLZ} t_{PHZ}	3-State Output Disable Time ($\overline{G}$, BUS)	4.5	$R_L = 1k\Omega$	—	26	38	—	48	—	57	ns
t_{PZL} t_{PZH}	3-State Output Enable Time (DIR- BUS)	4.5	$R_L = 1k\Omega$	—	28	40	—	50	—	60	ns
t_{PLZ} t_{PHZ}	3-State Output Disable Time (DIR-BUS)	4.5	$R_L = 1k\Omega$	—	28	40	—	50	—	60	ns
C_{IN}	Input Capacitance		*	—	5	10	—	10	—	10	pF
C_{OUT}	Output Capacitance		An, Bn	—	13	—	—	—	—	—	pF
C_{PD} (1)	Power Dissipation Capacitance		HCT646	—	55	—	—	—	—	—	pF
			HCT648	—	52	—	—	—	—	—	

*: Applicable only to DIR, $\overline{G}$, CAB, CBA, SAB, SBA input.

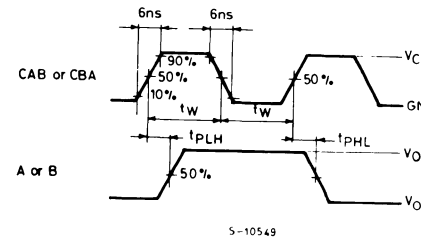
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test circuit).
Average operating current can be obtained from the equation hereunder.
$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per bit)

SWITCHING CHARACTERISTICS TEST WAVEFORM

WAVEFORM 1

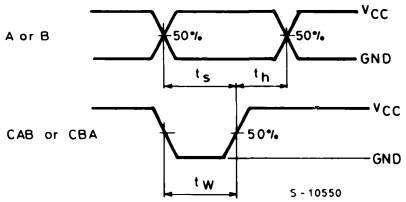


WAVEFORM 2

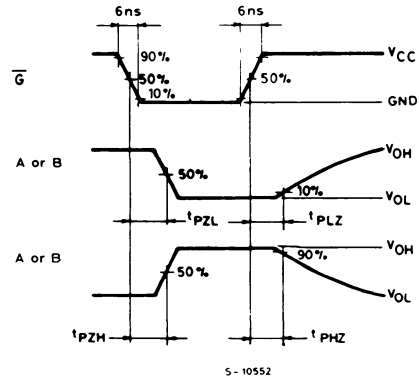


SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)

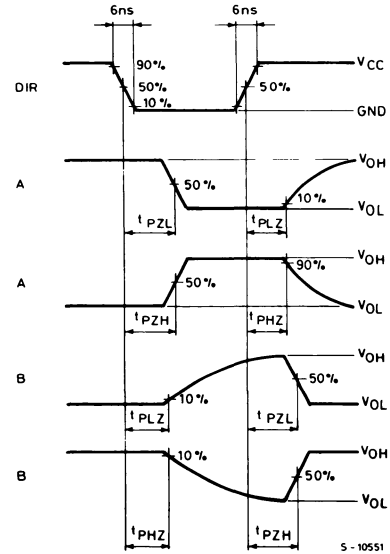
WAVEFORM 3



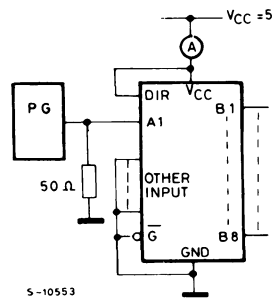
WAVEFORM 4



WAVEFORM 5



TEST CIRCUIT I_{CC} (Opr.)



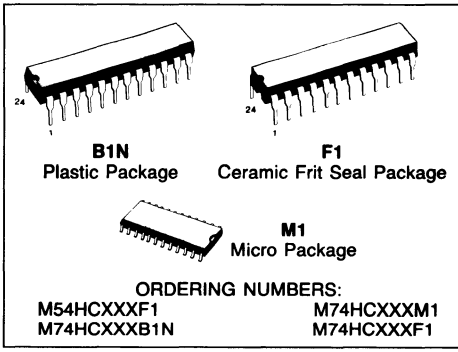
INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

SGS-THOMSON MICROELECTRONICS

M54/74HC651
M54/74HC652

HC651 OCTAL BUS TRANSCEIVER/REGISTER (3-STATE, INV.)
HC652 OCTAL BUS TRANSCEIVER/REGISTER (3-STATE)

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (Min)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS651/652



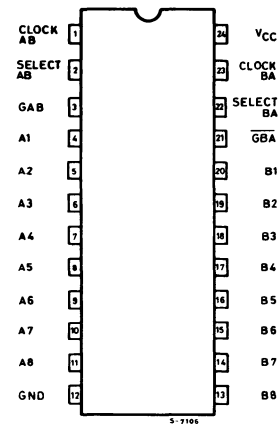
ORDERING NUMBERS:

M54HCXXXF1	M74HCXXXM1
M74HCXXXB1N	M74HCXXXF1

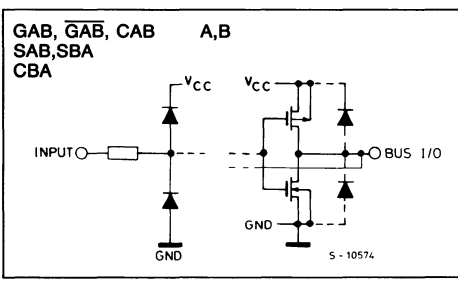
DESCRIPTION

M54/74HC651/652 are high speed CMOS OCTAL BUS TRANSCEIVERS AND REGISTERS (3-STATE), fabricated in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. Enable GAB and $\overline{GBA}$ are provided to control the transceiver functions.
Select AB and Select BA control pins are provided to select whether real-time or stored data is transfered. A low input level selects real-time data, and a high selects stored data.
Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CLOCK AB or CLOCK BA) regardless of the select or enable control pins. When select AB and select BA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{GBA}$. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT



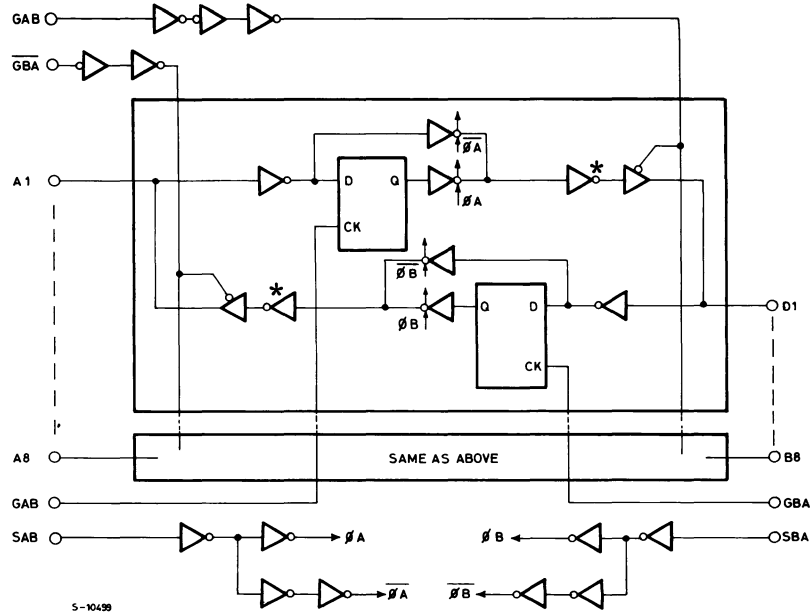
TRUTH TABLE

M54/74HC652 (The truth table for M54/74HC651 is the same as this, but with the outputs inverted)

GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A	B	FUNCTION
L	H					INPUTS	INPUTS	Both the A bus and the B bus are inputs.
		X	X	X	X	Z	Z	The output functions of the A and B bus are disabled.
		↑	↑	X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to the internal flip-flops. Data at the bus will be stored on low to high transition of the clock inputs.
L	L					OUTPUTS	INPUTS	The A bus are outputs and the B bus are inputs.
		X*	X	X	L	L H	L H	The data at the B bus are dipayed at the A bus.
		X*	↑	X	L	L H	L H	The data at the B bus are dispayed at the A bus. The data of the B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X*	X	X	H	Qn	X	The data stored to the internal flip-flops are dispayed at the A bus.
		X*	↑	X	H	L H	L H	The data at the B bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus.
H	H					INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs.
		X	X*	L	X	L H	L H	The data at the A bus are diplayed at the B bus.
		↑	X*	L	X	L H	L H	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X	X*	H	X	X	Qn	The data stored to the internal flip-flops are displayed at the B bus.
		↑	X*	H	X	L H	L H	The data at the A bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus.
H	L					OUTPUTS	OUTPUTS	Both the A bus and the B bus are outputs.
		X	X	H	H	Qn	Qn	The data stored to the internal flip-flops are displayed at the A and B bus respectively.
		↑	↑	H	H	Qn	Qn	The output at the A bus are displayed at the B bus, the output at the B bus are displayed at the A bus respec.

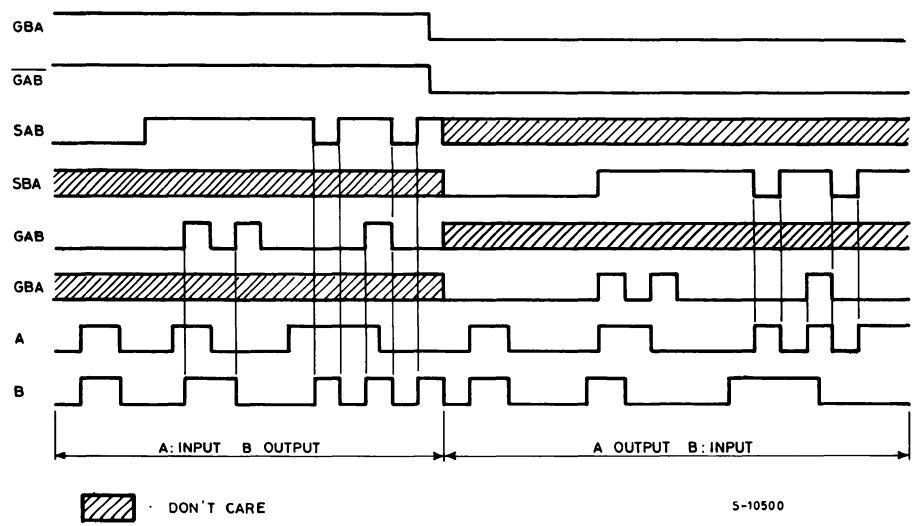
X : DON'T CARE.
Z : HIGH IMPEDANCE.
Qn : THE DATA STORED TO THE INTERNAL FLIP-FLOPS BY MOST RECENT LOW TO HIGH TRANSITION OF THE CLOCK INPUTS.
* : THE DATA AT THE A AND B BUS WILL BE STORED TO THE INTERNAL FLIP-FLOPS ON EVERY LOW TO TRANSITION OF THE CLOCK INPUTS.

LOGIC DIAGRAM (HC652)



NOTE: IN CASE OF M54/74HC652 OUTPUT INVERTER MARKED * AT A BUS AND B BUS ARE ELIMINATED

TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0	or		5.9	6.0	—	5.9	—	5.9	—	
		4.5	V_{IL}	−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−7.8 mA	5.68	5.8	—	5.63	—	5.60	—	

DC SPECIFICATIONS (Continued)

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current*	6.0	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{OZ}	3-State Output Off State Current	6.0	$V_{OUT} = V_{CC}$ or GND $V_I = V_{CC}$ or GND		—	—	±0.5	—	±0.5	—	±10	
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	

*: Applicable only to GAB, $\overline{GBA}$, CAB, CBA, SAB, SBA, inputs.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	25	60	—	75	—	90	ns
		4.5		—	7	12	—	15	—	18	
		6.0		—	6	10	—	13	—	15	
t_{PLH} t_{PHL}	Propagation Delay Time (BUS-BUS)	2.0		—	92	180	—	225	—	270	ns
		4.5		—	23	36	—	45	—	54	
		6.0		—	20	31	—	38	—	46	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-BUS)	2.0		—	124	240	—	300	—	360	ns
		4.5		—	31	48	—	60	—	72	
		6.0		—	26	41	—	51	—	61	
t_{PLH} t_{PHL}	Propagation Delay Time (SELECT-BUS)	2.0		—	112	220	—	275	—	330	ns
		4.5		—	28	44	—	55	—	66	
		6.0		—	24	37	—	47	—	56	
$t_{W(H)}$ $t_{W(L)}$	Minimum Clock Pulse Width	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Data Set-up Time	2.0		—	5	50	—	65	—	75	ns
		4.5		—	1	10	—	13	—	15	
		6.0		—	1	9	—	11	—	13	
t_h	Minimum Data Hold Time	2.0		—	—	25	—	30	—	40	ns
		4.5		—	—	5	—	6	—	8	
		6.0		—	—	5	—	5	—	7	

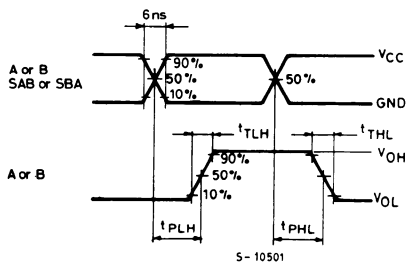
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PZL} t_{PZH}	3-State Output Enable Time	2.0	$R_L = 1k\Omega$	—	100	180	—	225	—	270	ns
		4.5		—	25	36	—	45	—	54	
		6.0		—	21	31	—	38	—	46	
t_{PZL} t_{PZH}	3-State Output Disable Time	2.0	$R_L = 1k\Omega$	—	88	170	—	215	—	255	ns
		4.5		—	22	34	—	43	—	51	
		6.0		—	19	29	—	37	—	43	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{OUT}	Output Capacitance		BUS I/O	—	13	—	—	—	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance			—	46	—	—	—	—	—	

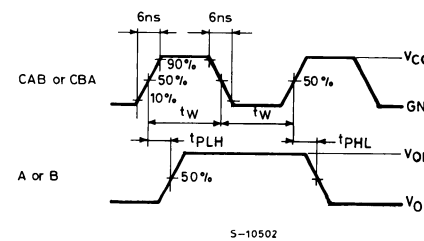
Note (*) C_{PD} is defined as the value of IC's internal equivalent capacitance which is calculated from the operating current consumption without load (refer to Test circuit).
Average operating current can be obtained by equation hereunder.
$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per bit)

SWITCHING CHARACTERISTICS TEST CIRCUIT AND WAVEFORM

WAVEFORM 1

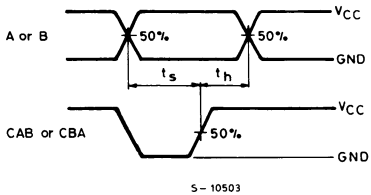


WAVEFORM 2



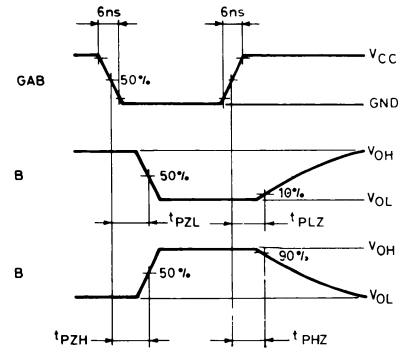
SWITCHING CHARACTERISTICS TEST CIRCUIT AND WAVEFORM (Continued)

WAVEFORM 3



S-10503

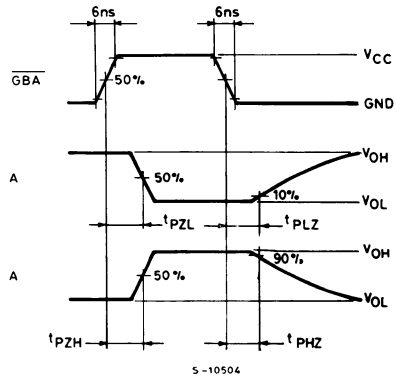
WAVEFORM 4



S-10505

$\overline{GBA}$="H"

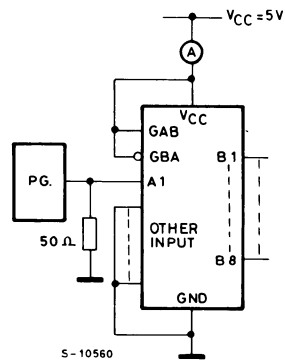
WAVEFORM 5



S-10504

GAB="L"

TEST WAVEFORM I_{CC} (Opr.)



S-10560

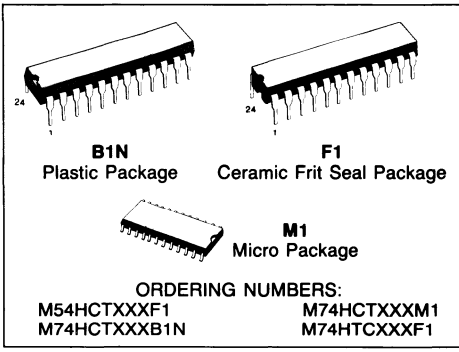
INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

SGS-THOMSON MICROELECTRONICS

M54/74HCT651
M54/74HCT652

HCT651 OCTAL BUS TRANSCEIVER/REGISTER (3-STATE, INV.)
HCT652 OCTAL BUS TRANSCEIVER/REGISTER (3-STATE)

- LOW POWER DISSIPATION
  I_{CC} = 4μA (MAX.) at T_A = 25°C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LST651/652



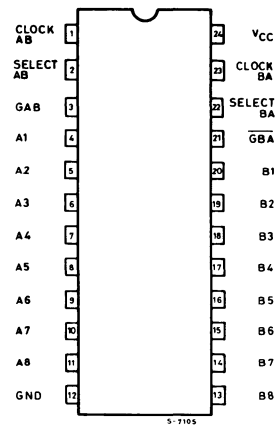
ORDERING NUMBERS:

M54HCTXXXF1	M74HCTXXXM1
M74HCTXXXB1N	M74HTCXXXF1

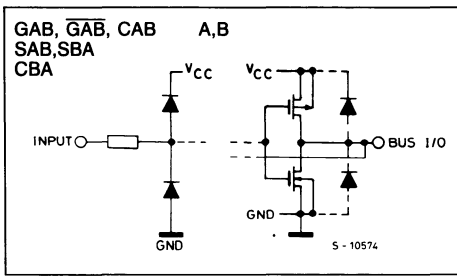
DESCRIPTION

The M54/74HCT651-652 are high speed CMOS OCTAL BUS TRANSCEIVER/REGISTER fabricated in silicon gate C²MOS technology.
They have the same high speed performance of LSTTL combined with true CMOS low power consumption. These devices consists of bus transceiver circuits, D-type flip-flop, and control circuitry arranged for multiplex transmission of data directly from the data bus or from the internal storage registers. Enable GAB and $\overline{GBA}$ are provided to control the transceiver functions. Select AB and select BA control pins are provided to select the real-time or stored data function. Data on the A or B DATA bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CLOCK AB or CLOCK BA) regardless of the select or enable control pins.
When select AB and select BA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{GBA}$. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.
All inputs are equipped with protection circuits against static discharge and transient excess voltage. This integrated circuit has totally compatible, input and output characteristic, with standard 54/74 LSTTL logic families.
M54HCT/74HCT devices are designed to interface directly with HSC²MOS components. These devices are also plug in relacements for LSTTL device giving a reduction in power consumption.

PIN CONNECTIONS (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT



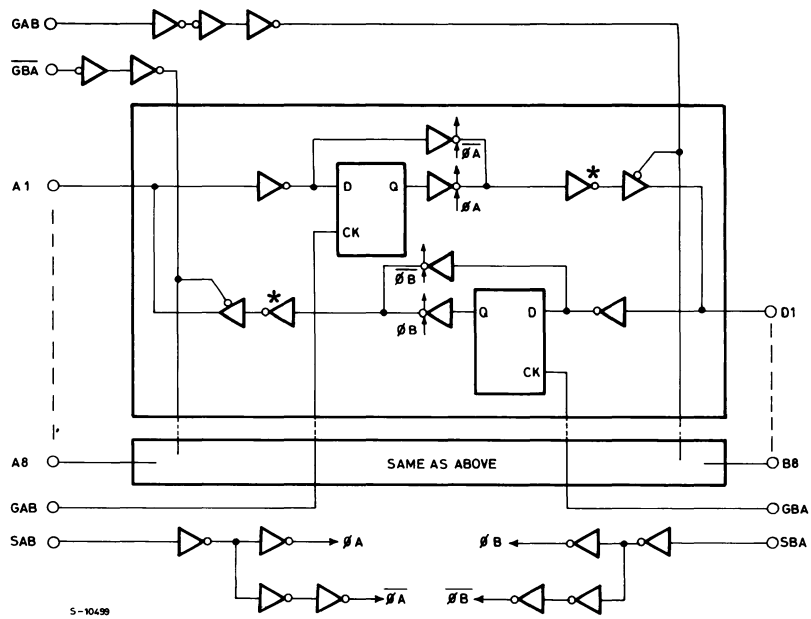
TRUTH TABLE

M54/74HCT652 (The truth table for M54/74HCT651 is the same as this, but with the outputs inverted)

GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A	B	FUNCTION
						INPUTS	INPUTS	Both the A bus and the B bus are inputs.
		X	X	X	X	Z	Z	The output functions of the A and B bus are disabled.
L	H	↓	↓	X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to the internal flip-flops. Data at the bus will be stored on low to high transition of the clock inputs.
						OUTPUTS	INPUTS	The A bus are outputs and the B bus are inputs.
		X*	X	X	L	L H	L H	The data at the B bus are displayed at the A bus.
		X*	↓	X	L	L H	L H	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
L	L	X*	X	X	H	Qn	X	The data stored to the internal flip-flops are dispayed at the A bus.
		X*	↓	X	H	H L	H L	The data at the B bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus.
						INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs.
		X	X*	L	X	L H	L H	The data at the A bus are displayed at the B bus.
		↓	X*	L	X	L H	L H	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
H	H	X	X*	H	X	X	Qn	The data stored to the internal flip-flops are displayed at the B bus.
		↓ X*	H	X	L	L H	H	The data at the A bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus.
						OUTPUTS	OUTPUTS	Both the A bus and the B bus are outputs.
		X	X	H	H	Qn	Qn	The data stored to the internal flip-flops are displayed at the A and B bus respectively.
H	L	↓	↓	H	H	Qn	Qn	The output at the A bus are displayed at the B bus, the output at the B bus are displayed at the A bus respec.

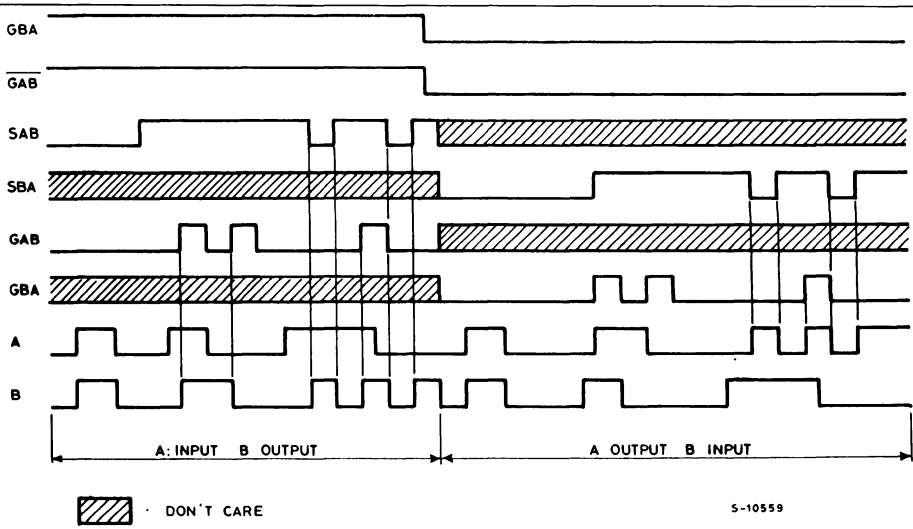
X : DON'T CARE.
Z : HIGH IMPEDANCE.
Qn : THE DATA STORED TO THE INTERNAL FLIP-FLOPS BY MOST RECENT LOW TO HIGH TRANSITION OF THE CLOCK INPUTS.
* : THE DATA AT THE A AND B BUS WILL BE STORED TO THE INTERNAL FLIP-FLOPS ON EVERY LOW TO TRANSITION OF THE CLOCK INPUTS.

LOGIC DIAGRAM (HC651)



NOTE: IN CASE OF M54/74HCT652 OUTPUT INVERTER MARKED * AT A BUS AND B BUS ARE ELIMINTATED

TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		4.5 to 5.5	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time		0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0	—	—	2.0	—	2.0	—	V
V_{IL}	Low Level Input Voltage	4.5 to 5.5			—	—	0.8	—	0.8	—	0.8	V
V_{OH}	High Level Output Voltage	4.5	V_{IN}	I_{OH}								
			V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	V
				−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	

DC SPECIFICATIONS (Continued)

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OL}	Low Level Output Voltage	4.5	V_{IN}	I_{OL}								
			V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
				6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current*	5.5	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{OZ}	3-State Output Off-State Current	5.5	$V_I = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±10.0	μA
I_{CC}	Quiescent Supply Current	5.5	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA
I_C			Per input: $V_{IN} = 2.4V$ or 0.5V Other input: V_{CC} or GND		—	—	2.0	—	2.9	—	3.0	mA

*: Applicable only to GAB, $\overline{GBA}$, CAB, CBA, SAB, SBA input

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5		—	7	12	—	15	—	18	ns
t_{PLH} t_{PHL}	Propagation Delay Time (BUS-BUS)	4.5		—	20	31	—	39	—	47	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-BUS)	4.5		—	30	47	—	58	—	71	ns
t_{PLH} t_{PHL}	Propagation Delay Time (SELECT-BUS)	4.5		—	31	48	—	60	—	72	ns
$t_{W(H)}$ $t_{W(L)}$	Minimum Clock Pulse Width	4.5		—	11	20	—	25	—	30	ns

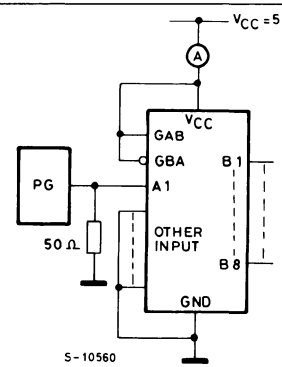
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_s	Minimum Data Set-up Time	4.5		—	4	10	—	13	—	15	ns
t_h	Minimum Data Hold Time	4.5		—	—	5	—	5	—	5	ns
t_{PZL} t_{PZH}	3-State Output Enable Time ($\overline{GBA}$ - BUS)	4.5	$R_L = 1k\Omega$	—	21	30	—	38	—	45	ns
t_{PLZ} t_{PHZ}	3-State Output Disable Time (GBA - BUS)	4.5	$R_L = 1k\Omega$	—	26	38	—	48	—	57	ns
t_{PZL} t_{PZH}	3-State Output Enable Time (GAB - BUS)	4.5	$R_L = 1k\Omega$	—	25	36	—	45	—	54	ns
t_{PLZ} t_{PHZ}	3-State Output Disable Time (GAB - BUS)	4.5	$R_L = 1k\Omega$	—	25	36	—	45	—	54	ns
C_{IN}	Input Capacitance*			—	5	10	—	10	—	10	pF
C_{OUT}	Output Capacitance		BUS I/O	—	13	—	—	—	—	—	
C_{PD} (1)	Power Dissipation Capacitance		HCT651	—	52	—	—	—	—	—	
			HCT652	—	52	—	—	—	—	—	

* Applicable only to GAB, $\overline{GBA}$, CAB, CBA, SAB, SBA input.

Note (1) C_{PD} is defined as the value of IC's internal equivalent capacitance which is calculated from the operating current consumption without load (refer to Test circuit).
Average operating current can be obtained by equation hereunder.
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

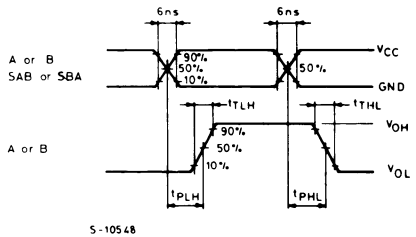
TEST CIRCUIT I_{CC} (Opr.)



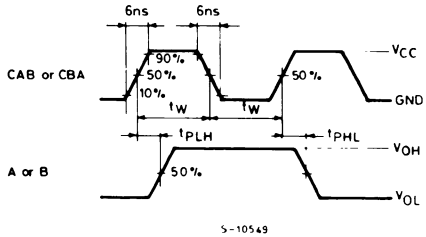
INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

SWITCHING CHARACTERISTICS TEST WAVEFORM

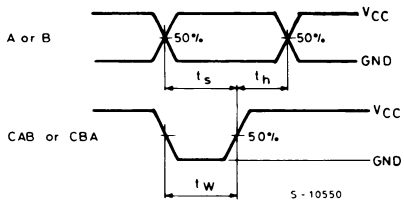
WAVEFORM 1



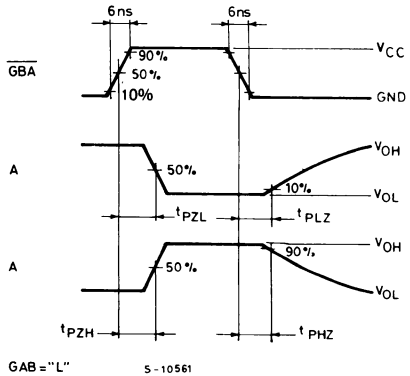
WAVEFORM 2



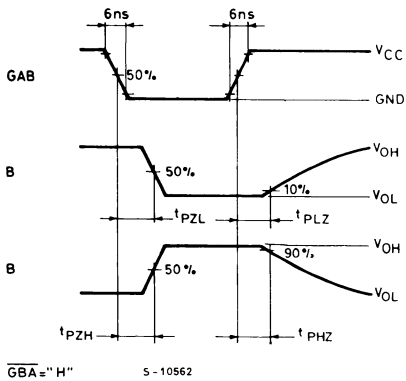
WAVEFORM 3



WAVEFORM 4



WAVEFORM 5



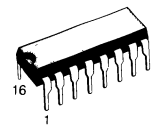
SGS-THOMSON MICROELECTRONICS

M54HC670
M74HC670

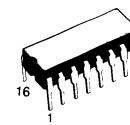
4-WORD X 4-BIT REGISTER FILE (3-STATE)

PRELIMINARY DATA

- HIGH SPEED
  t_{PD} = 21 ns (Typ) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS670



B1N
Plastic Package



F1
Ceramic Frit Seal Package

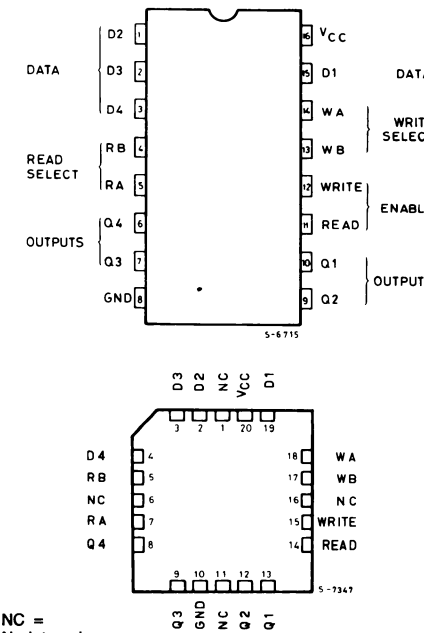
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC670 F1
M74HC670 B1N
M74HC670 F1
M74HC670 C1
M74HC670 M1

PIN CONNECTION (top view)



NC = No Internal Connection

DESCRIPTION

The M54/74HC670 is a high speed CMOS 4 WORD X 4 BIT REGISTER FILE (3-STATE) fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The M54HC/74HC670 is a 4 x 4 Register File organised as four words by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation. The 3-state outputs make it possible to connect up to 128 outputs to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

WRITE FUNCTION TABLE

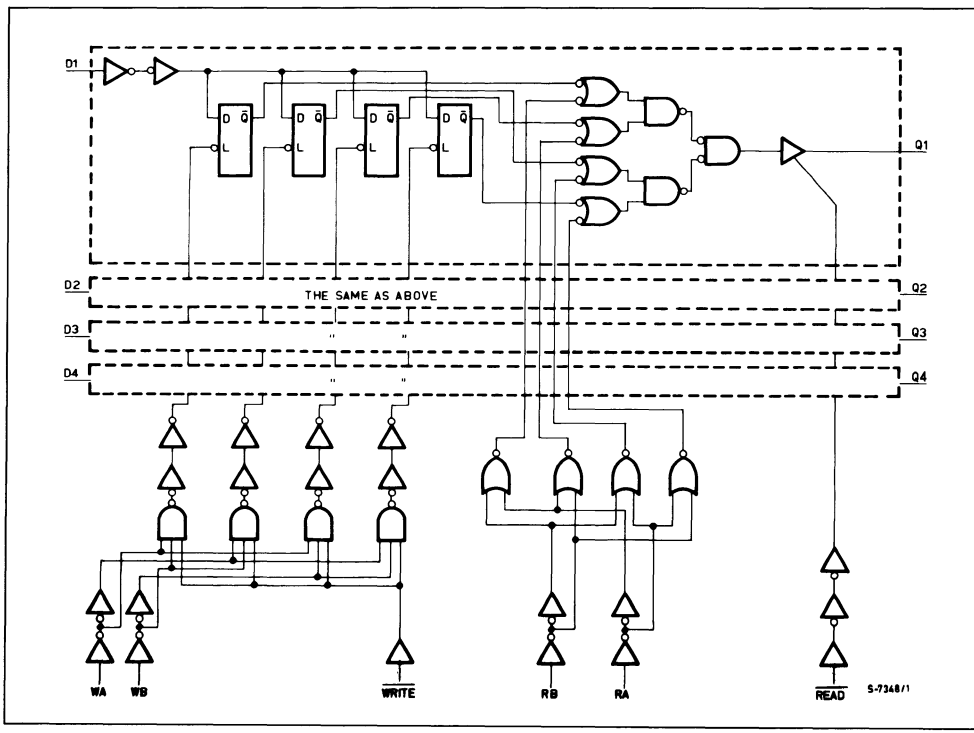
WRITE INPUTS			WORDS			
WB	WA	$\overline{WE}$	0	1	2	3
L	L	L	Q=D	Q0	Q0	Q0
L	H	L	Q0	Q=D	Q0	Q0
H	L	L	Q0	Q0	Q=D	Q0
H	H	L	Q0	Q0	Q0	Q=D
X	X	H	Q0	Q0	Q0	Q0

READ FUNCTION TABLE

READ INPUTS			OUTPUTS			
RB	RA	$\overline{RE}$	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

Notes: 1 *: DON'T CARE. Z: HIGH IMPEDANCE
2 (Q=D)= THE FOUR SELECT INTERNAL FLIP-FLOP OUTPUTS WILL ASSUME THE STATES APPLIED TO THE FOUR EXTERNAL DATA INPUTS.
3 Q0= THE LEVEL OF Q BEFORE THE INDICATED INPUT CONDITIONS WERE ESTABLISHED.
4 W0B1= THE FIRST BIT OF WORD 0, ETC.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

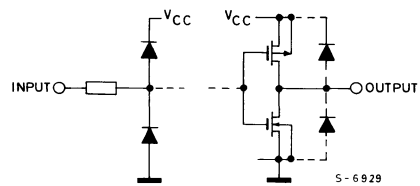
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series Operating Temperature 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{OZ}	3-State Output Off-State Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±5.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND $I_O = 0$		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

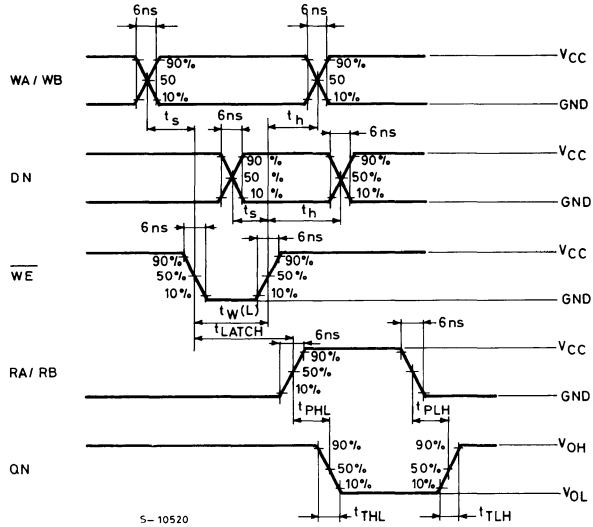
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (RA,RB-Qn)		21	34	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{WE}$-Qn)		24	38	ns
t_{PLH} t_{PHL}	Propagation Delay Time (Dn-Qn)		20	32	ns

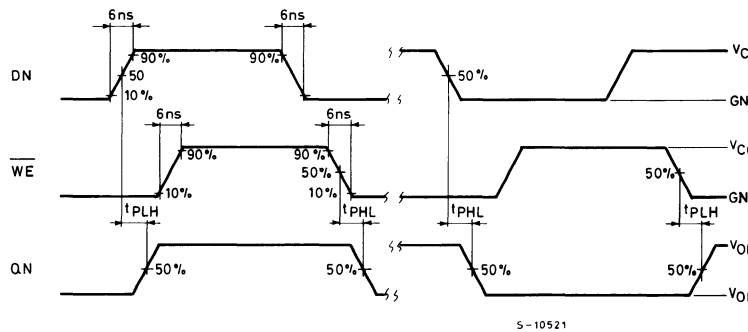
AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (RA,RB-Qn)	2.0		—	100	195	—	245		295	ns
		4.5		—	25	39	—	49		59	
		6.0		—	21	33	—	42		50	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{WE}$-Qn)	2.0		—	112	220	—	275		330	ns
		4.5		—	28	44	—	55		66	
		6.0		—	24	37	—	47		36	
t_{PLH} t_{PHL}	Propagation Delay Time (Dn-Qn)	2.0		—	92	185	—	230		280	ns
		4.5		—	23	37	—	46		56	
		6.0		—	20	31	—	39		48	
$t_{W(L)}$	Minimum Pulse Width ($\overline{WE}$)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_s	Minimum Set-up Time (Dn-$\overline{WE}$)	2.0		—	—	25	—	30		40	ns
		4.5		—	—	5	—	6		8	
		6.0		—	—	5	—	6		7	
t_s	Minimum Set-up Time (WA-WB-$\overline{WE}$)	2.0		—	—	0	—	0		0	ns
		4.5		—	—	0	—	0		0	
		6.0		—	—	0	—	0		0	
t_h	Minimum Hold Time (Dn-$\overline{WE}$)	2.0		—	15	50	—	65	—	75	ns
		4.5		—	2	10	—	13	—	15	
		6.0		—	3	9	—	11	—	13	
t_h	Minimum Hold Time (WA,WB-$\overline{WE}$)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{latch} (1)	Minimum Latch Time ($\overline{WE}$-RA,RB)	2.0		—	20	75	—	95	—	110	ns
		4.5		—	5	15	—	19	—	22	
		6.0		—	4	13	—	16	—	19	
t_{PZL} t_{PZH}	3-State Output Enable Time	2.0		—	52	110	—	140	—	165	
		4.5	R_L = 1KΩ	—	13	22	—	28	—	33	
		6.0		—	11	19	—	24	—	28	
t_{PLZ} t_{PHL}	3-State Output Disable Time	2.0		—	68	120	—	150	—	180	
		4.5	R_L = 1KΩ	—	17	24	—	30	—	36	
		6.0		—	14	20	—	26	—	31	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{OUT}	Output Capacitance			—	10	—	—	—	—	—	pF
C_{PD} (2)	Power Dissipation Capacitance			—	44	—	—	—			pF

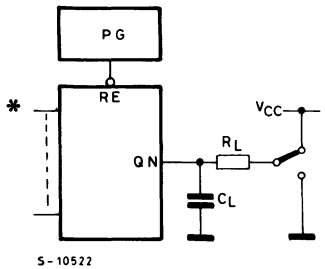
Note:
(1): t_{latch} is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data.
(2):C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load. Average operating current is: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

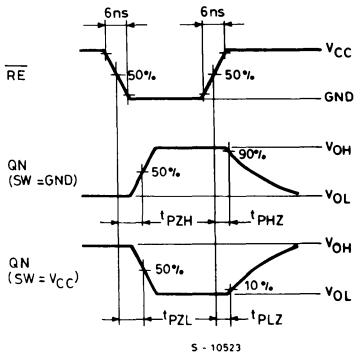
SWITCHING CHARACTERISTICS TEST WAVEFORM





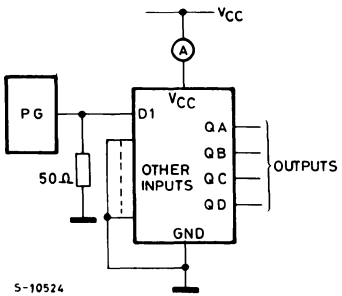
SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)





*: SUCH A LOGIC LEVEL, SHALL BE APPLIED TO EACH INPUT THAT THE OUTPUT VOLTAGE STAYS IN THE APPOSITE SIDE TO THE SWITCH CONNECTION LEVEL. WHEN THE OUTPUT IS ENABLED.

TEST CIRCUIT I_{CC} (Opr.)



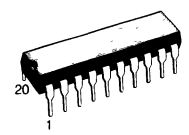
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

SGS-THOMSON MICROELECTRONICS

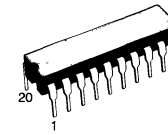
M54HC688
M74HC688

8-BIT EQUALITY COMPARATOR

- HIGH SPEED
  t_{PD} = 21 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS688



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC688 F1
M74HC688 B1N
M74HC688 F1
M74HC688 C1
M74HC688 M1

DESCRIPTION

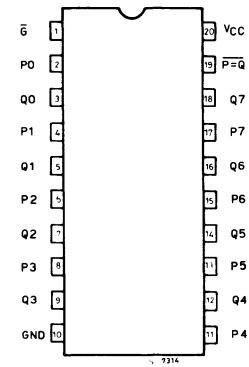
The M54/74HC688 utilizes silicon gate C²MOS technology to achieve operating speeds equivalent to LSTTL devices. Along with the low power dissipation and high noise immunity of standard C²MOS integrated circuit, it possesses the driving capability of 10 LSTTL load. The M54/74HC688 compares bit for bit two 8-bit words applied on inputs P0 - P7 and inputs Q0 - Q7 and indicates whether or not they are equal. A single active low enable is provided to facilitate cascading several packages to enable comparison of words greater than 8 bits. All inputs are equipped with protection circuit against static discharge and transient excess voltage.

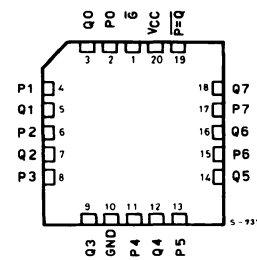
TRUTH TABLE

INPUT		OUTPUT
P,Q	$\overline{G}$	$\overline{P = Q}$
P = Q	L	L
P ≠ Q	L	H
X	H	H

X: DON'T CARE

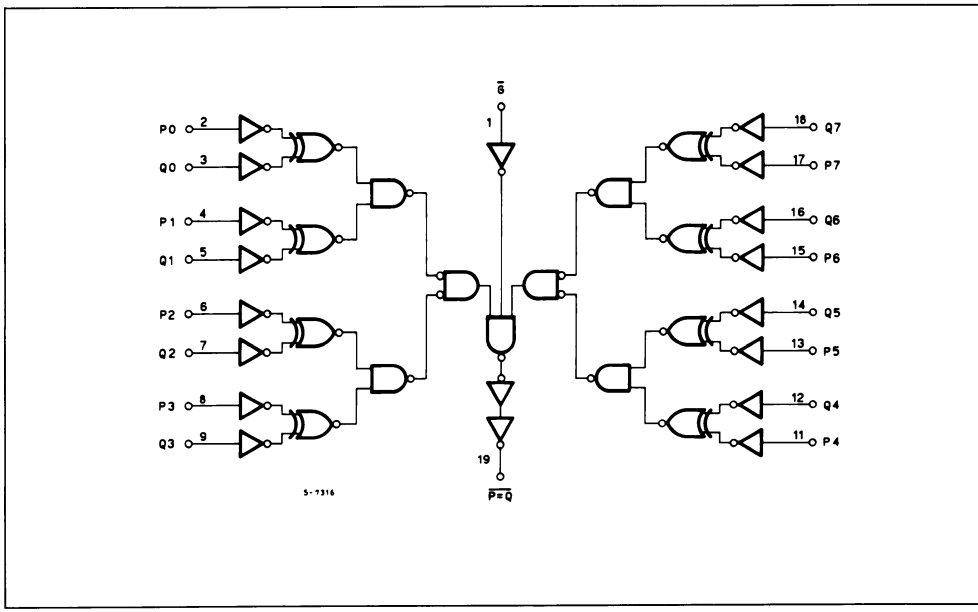
PIN CONNECTIONS (top view)





NC = No Internal Connection

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V: 0 to 1000 V_{CC} = 4.5V: 0 to 500 V_{CC} = 6 V: 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0 4.5 6.0	V_I V_{IH} or V_{IL}	I_O −20 μA	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	1.9 4.4 5.9	— — —	V
		4.5 6.0		−4.0 mA −5.2 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	
V_{OL}	Low Level Output Voltage	2.0 4.5 6.0	V_{IH} or V_{IL}	20 μA	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
		4.5 6.0		4.0 mA 5.2 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input t_r = t_f = 6ns)

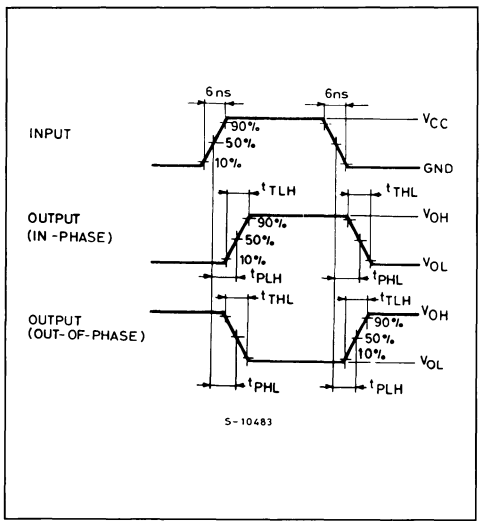
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (P_n Q_n - $\overline{P}$ = $\overline{Q}$)		22	35	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{G}$ - $\overline{P}$ = $\overline{Q}$)		12	20	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

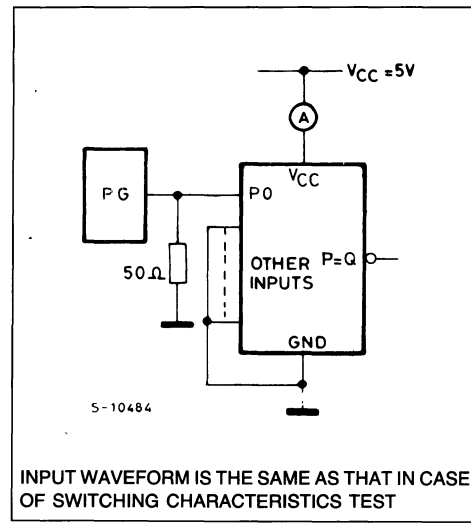
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (Pn, Qn-$\overline{P}$ = Q)	2.0		—	104	190	—	245	—	295	ns
		4.5		—	26	39	—	49	—	59	
		6.0		—	22	33	—	42	—	50	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	60	120	—	150	—	180	ns
		4.5		—	15	24	—	30	—	36	
		6.0		—	13	20	—	26	—	31	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	40	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following equation.
$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$.

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)

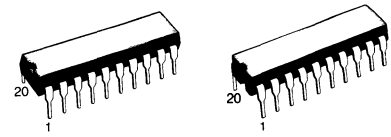


INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

M54/74HC690
M54/74HC691

HC690 DECADE COUNTER/REGISTER (3-STATE)
HC691 4-BIT BINARY COUNTER/REGISTER (3-STATE)

- HIGH SPEED
  f_{MAX} = 33MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS (FOR Q_A to Q_D)
  10 LSTTL LOADS (FOR RCO)
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 6 mA (MIN.) FOR Q_A to Q_D OUTPUT
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.) FOR RCO OUTPUT
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC}(OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH LSTTL 54/74LS690/691



B1N
Plastic Package

F1
Ceramic Frit Seal Package

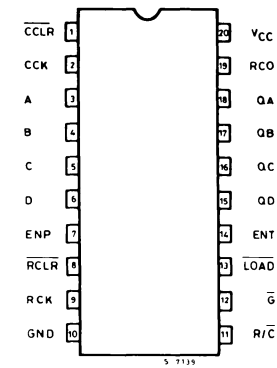
M1
Micro Package

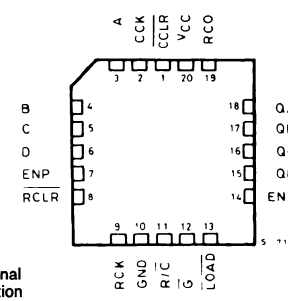
C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HCXXX F1	M74HCXXX C1
M74HCXXX B1N	M74HCXXX M1
M74HCXXX F1	

PIN CONNECTIONS (top view)





NC = No Internal Connection

DESCRIPTION

The HC690/691 are high speed CMOS COUNTER/REGISTER fabricated in silicon gate C²MOS technology.
They have the same high speed performance of LSTTL combined with true CMOS low power consumption.
The internal circuit is composed of 3 stages including buffer output, which offers high noise immunity and stable output.
These devices incorporate a synchronous counter, four-bit D-type register, and quadruple two-line to one-line multiplexers with three-state outputs in a single 20-pin package. The counter can be programmed from the data inputs and have enable P and enable T inputs and a ripple-carry output for easy expansion. The register/counter select input, R/C, selects the counter when low or the register when high for the three-state outputs, QA, QB, QC, and QD.
Individual clock and clear inputs are provided for both the counter and the register. Both clock inputs are positive-edge triggered. The clear lines are active low and is synchronous.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUTS									OUTPUTS				FUNCTION
$\overline{CCLR}$	$\overline{LOAD}$	ENP	ENT	CCK	$\overline{RCLR}$	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	X	X	X	L	L	L	L	L	L	CLEAR COUNTER
H	L	X	X	↑	X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	L	X	↑	X	X	L	L	NO CHANGE				NO COUNT
H	H	X	L	↑	X	X	L	L	NO CHANGE				NO COUNT
H	H	H	H	↑	X	X	L	L	COUNT UP				COUNT UP
H	X	X	X	↓	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	L	X	H	L	L	L	L	L	CLEAR REGISTER
X	X	X	X	X	H	↑	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	H	↓	H	L	NO CHANGE				NO LOAD

X : DON'T CARE

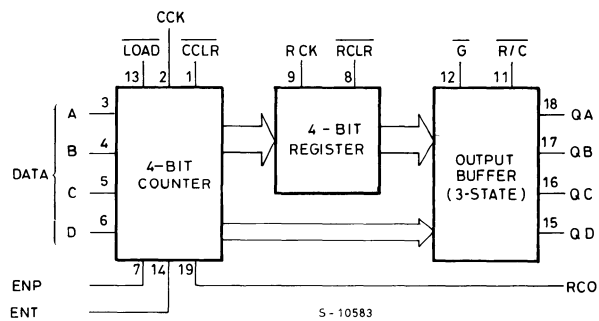
Z : HIGH IMPEDANCE

a-d : THE LEVEL OF STEADY STATE INPUTS AT INPUTS A THROUGH D RESPECTIVELY.

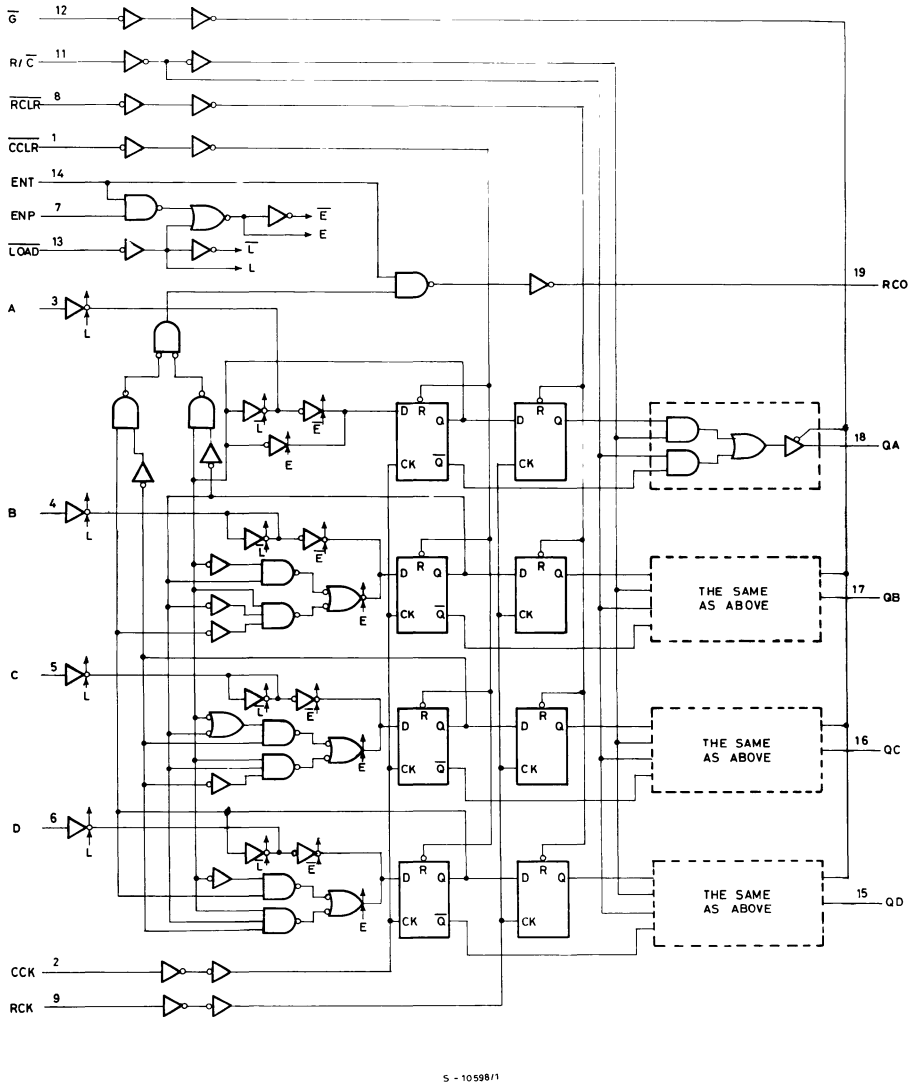
a'-d' : THE LEVEL OF STEADY STATE OUTPUTS AT INTERNAL COUNTER OUTPUTS QA' THROUGH QD' RESPECTIVELY.

HC690 RCO = QA•QD•ENT
HC691 RCO = QA•QB•QC•QD•ENT

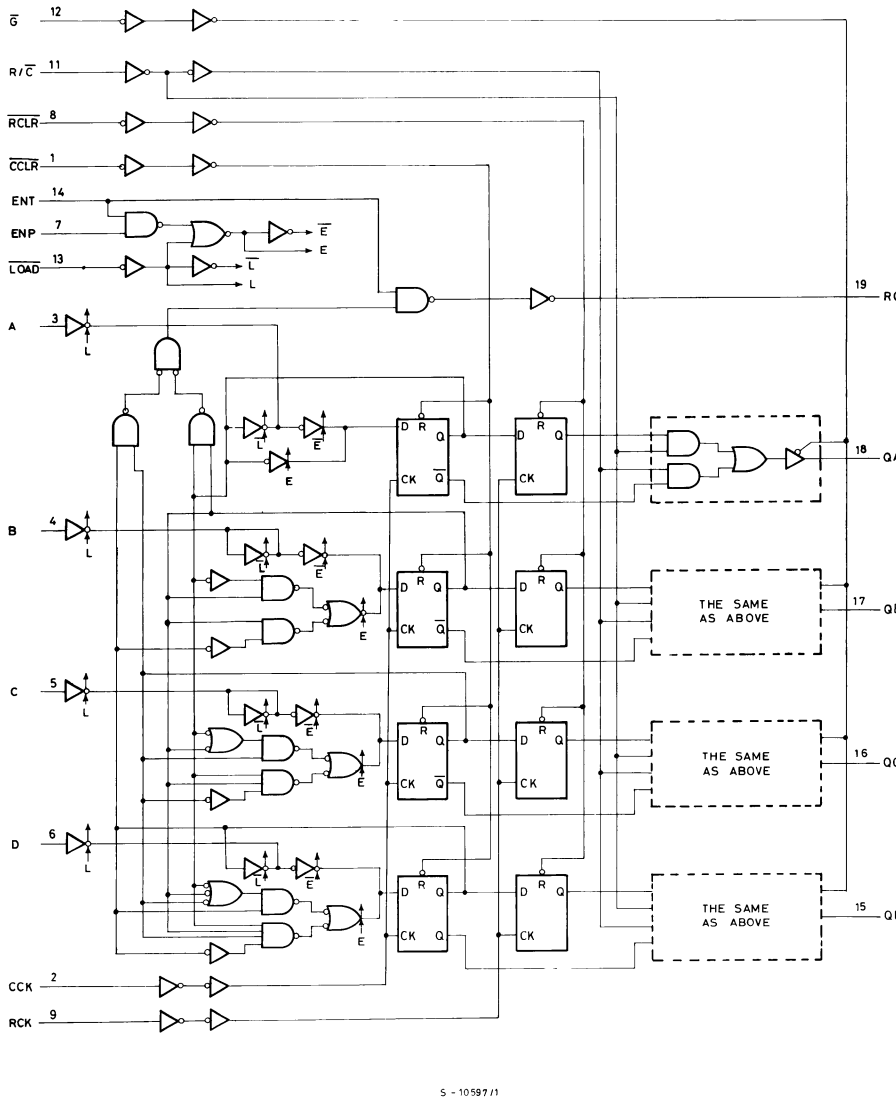
BLOCK DIAGRAM



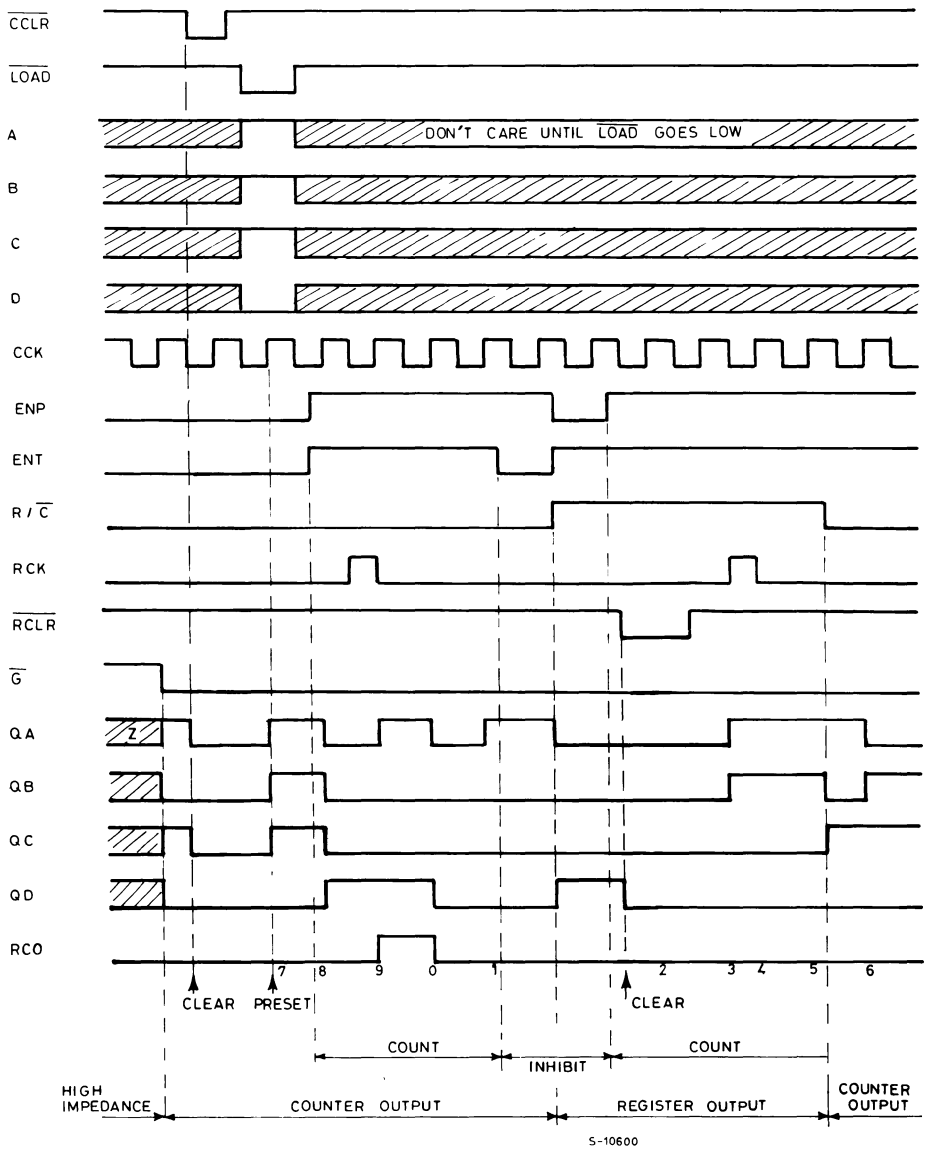
LOGIC DIAGRAM (HC690)



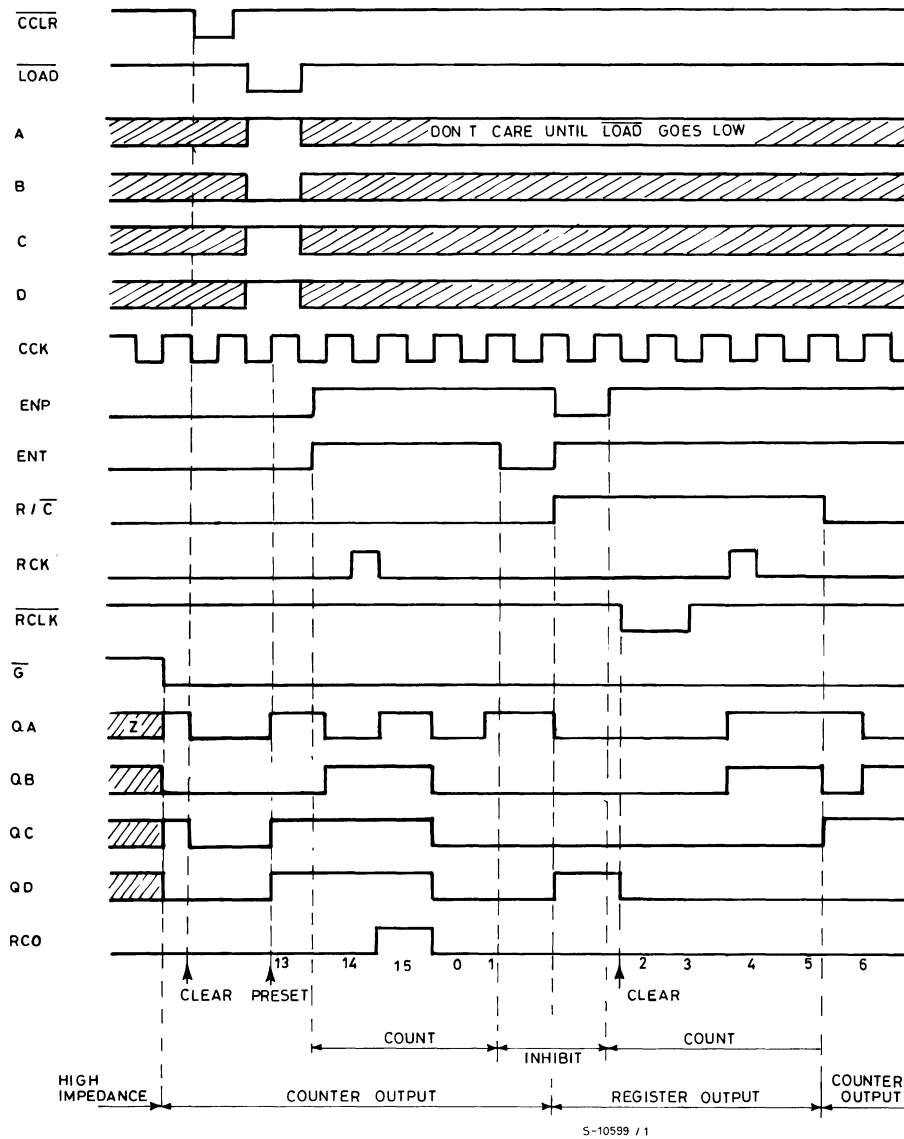
LOGIC DIAGRAM (HC691)



TIMING CHART (HC690)



TIMING CHART (HC691)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin (RCO) (QA to QD)	± 25 ±35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

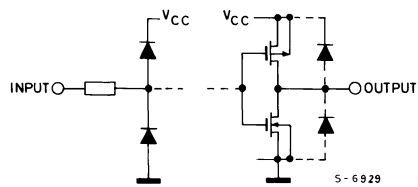
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V 4.5V 6 V	0 to 1000 0 to 500 0 to 400	ns

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_{IN}	I_{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5	Q_A-Q_D	−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
		4.5	RCO	−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IN}	I_{OL}	—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5	Q_A-Q_D	6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
		4.5	RCO	4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{OZ}	3-State Off-State Current	6.0	$V_{IN} = V_{IL}$ or V_{IH} $V_{OUT} = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±10	μA
I_{IN}	Input Leakage Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	
I_{CC}	Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	4.0	—	40.0	—	80.0	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (Q)	2.0		—	25	60	—	75	—	90	ns
		4.5		—	7	12	—	15	—	18	
		6.0		—	6	10	—	13	—	15	
t_{TLH} t_{THL}	Output Transition Time (RCO)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (CCK-Q)	2.0		—	136	265	—	335	—	400	ns
		4.5		—	34	53	—	66	—	80	
		6.0		—	29	45	—	56	—	68	

AC ELECTRICAL CHARACTERISTICS (Continued)

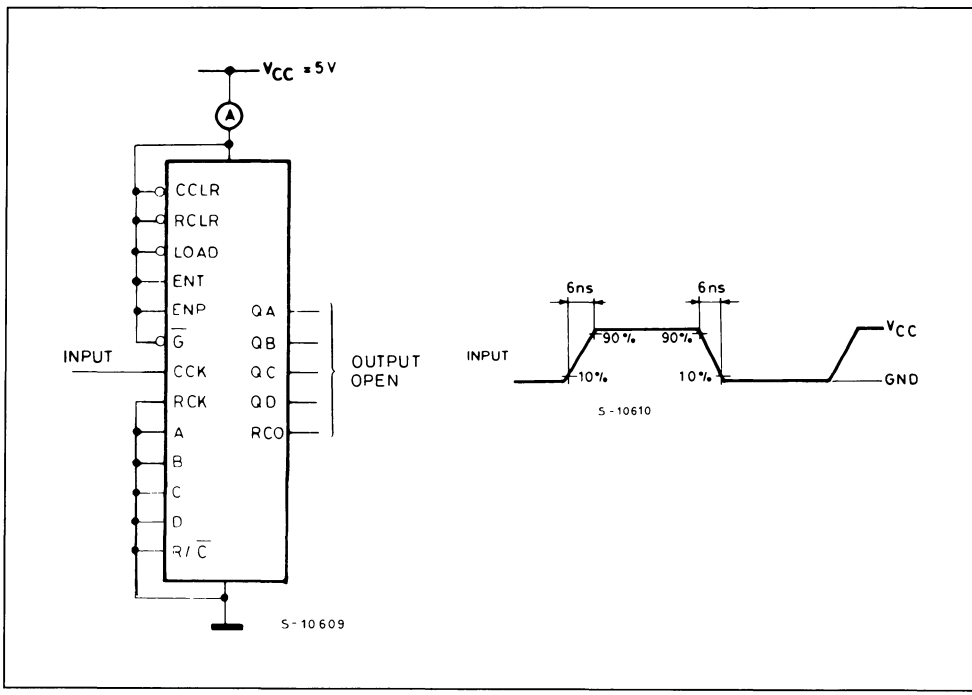
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (RCK-Q)	2.0		—	148	285	—	355	—	430	ns
		4.5		—	37	57	—	71	—	86	
		6.0		—	31	48	—	60	—	73	
t_{PLH} t_{PHL}	Propagation Delay Time (CCK-RCO)	2.0		—	128	250	—	315	—	375	ns
		4.5		—	32	50	—	63	—	75	
		6.0		—	27	43	—	54	—	64	
t_{PLH} t_{PHL}	Propagation Delay Time ($R/\overline{C}$-Q)	2.0		—	104	200	—	250	—	300	ns
		4.5		—	26	40	—	50	—	60	
		6.0		—	22	34	—	43	—	51	
t_{PLH} t_{PHL}	Propagation Delay Time (ENT-RCO)	2.0		—	56	110	—	140	—	165	ns
		4.5		—	14	22	—	28	—	33	
		6.0		—	12	19	—	24	—	28	
t_{PHL}	Propagation Delay Time ($\overline{CCLR}$-Q)	2.0		—	160	305	—	385	—	460	ns
		4.5		—	40	61	—	77	—	92	
		6.0		—	12	52	—	66	—	78	
t_{PLH}	Propagation Delay Time ($\overline{CCLR}$-RCO)	2.0		—	132	255	—	320	—	385	ns
		4.5		—	33	51	—	64	—	77	
		6.0		—	28	43	—	54	—	65	
t_{PHL}	Propagation Delay Time ($\overline{RCLR}$-Q)	2.0		—	148	285	—	355	—	430	ns
		4.5		—	37	57	—	71	—	86	
		6.0		—	31	48	—	60	—	73	
f_{MAX}	Maximum Clock Frequency	2.0		4	8	—	3	—	3	—	MHz
		4.5		20	30	—	16	—	13	—	
		6.0		24	35	—	19	—	15	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CCK, RCK)	2.0		—	40	100	—	125	—	150	ns
		4.5		—	10	20	—	25	—	30	
		6.0		—	9	17	—	21	—	26	
$t_{W(L)}$	Mimum Pulse Width (CCLR, $\overline{RCLR}$)	2.0		—	44	100	—	125	—	150	ns
		4.5		—	11	20	—	25	—	30	
		6.0		—	9	17	—	21	—	26	
t_{REM}	Minimum Removal Time	2.0		—	—	25	—	30	—	40	ns
		4.5		—	—	5	—	6	—	8	
		6.0		—	—	5	—	6	—	7	
t_S	Minimum Set-up Time ($\overline{LOAD}$,ENT,ENP)	2.0		—	80	175	—	220	—	265	ns
		4.5		—	20	35	—	44	—	53	
		6.0		—	17	30	—	37	—	45	
t_S	Minimum Set-up Time (A, B, C, D)	2.0		—	48	125	—	155	—	190	ns
		4.5		—	12	25	—	31	—	38	
		6.0		—	10	21	—	26	—	32	
t_S	Minimum Set-up Time (CCK-RCK)	2.0		—	76	175	—	220	—	265	ns
		4.5		—	19	35	—	44	—	53	
		6.0		—	16	30	—	37	—	45	

AC ELECTRICAL CHARACTERISTICS (Continued)

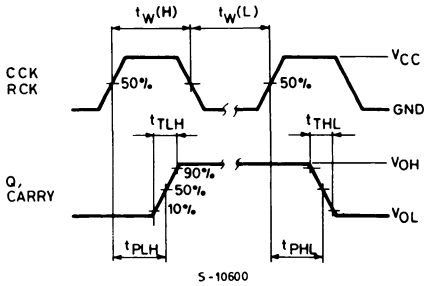
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_h	Minimum Hold Time	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{PZL} t_{PZH}	3-State Output Enable Time	2.0	$R_L = 1k\Omega$	—	72	145	—	180	—	220	ns
		4.5		—	18	29	—	36	—	44	
		6.0		—	15	25	—	31	—	38	
t_{PLZ} t_{PHZ}	3-State Output Disable Time	2.0	$R_L = 1k\Omega$	—	92	170	—	215	—	255	ns
		4.5		—	23	34	—	43	—	51	
		6.0		—	20	29	—	37	—	43	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	80	—	—	—	—	—	

Note (*) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test circuit).
Average operating current can be obtained from the equation:
$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

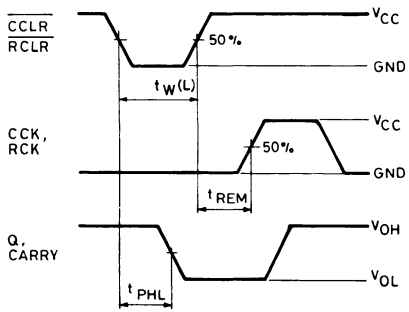
TEST CIRCUIT I_{CC} (Opr.)



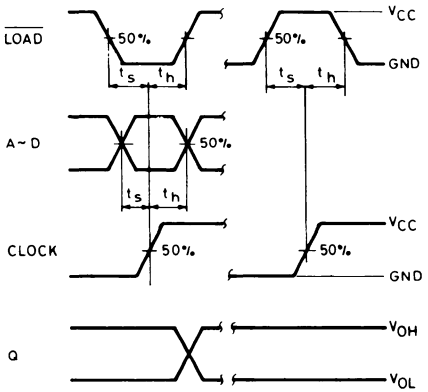
SWITCHING CHARACTERISTICS TEST WAVEFORM



S-10600

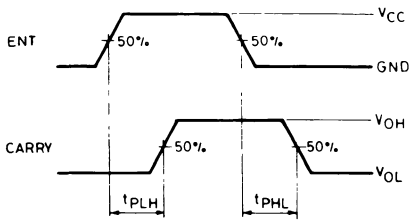


S-10611

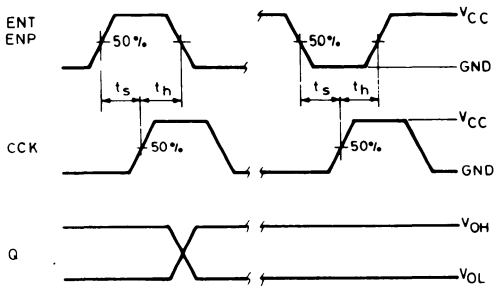


S-10602

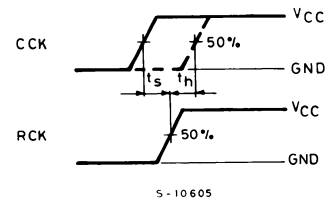
(Fix Maximum Count)



S-10603

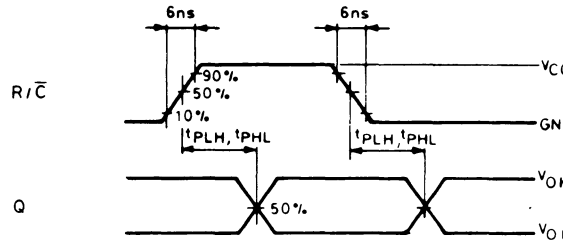


S-10604



S-10605

SWITCHING CHARACTERISTICS (Continued)



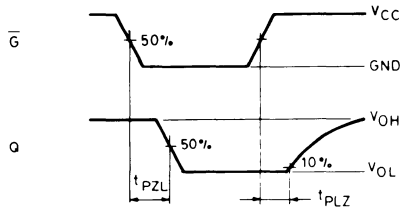
S-10606

t_{PLZ}, t_{PZL}

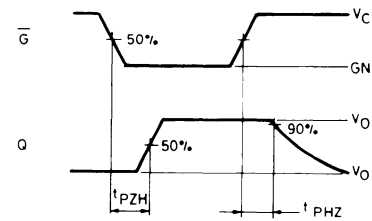
The 1kΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line. All inputs except $\overline{G}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{G}$ input is held low.

t_{PHZ}, t_{PZH}

The 1kΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{G}$ input should be connected to V_{CC} or GND line such that output will be in low logic level while $\overline{G}$ input is held low.



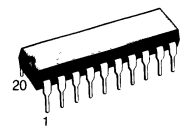
S-10607



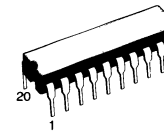
S-10608

HC692 DECADE COUNTER/REGISTER (3-STATE)
HC693 4 BIT BINARY COUNTER/REGISTER (3-STATE)

- HIGH SPEED
  f_{MAX} = 33MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS (FOR Q_A to Q_D)
  10 LSTTL LOADS (FOR RCO)
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.) FOR Q_A to Q_D OUTPUT
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.) FOR RCO OUTPUT
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC}(OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH LSTTL 54/74LS692/693



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

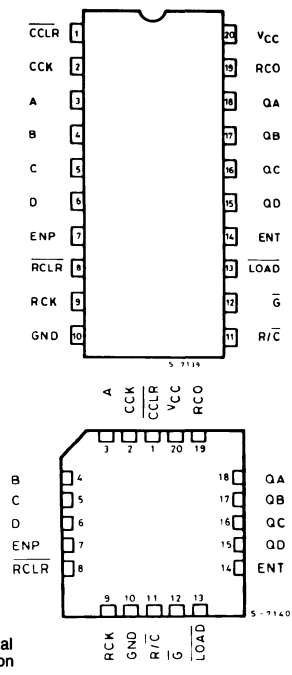
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX C1
M74HCXXX M1

DESCRIPTION

The HC692/693 are high speed CMOS COUNTER/REGISTER fabricated with silicon gate C²MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
HC692 is BCD DECADE COUNTER, HC693 is 4-BIT BINARY COUNTER, these devices also have registers. If the LOAD input ($\overline{LOAD}$) is held "L", DATA input (A-D) are loaded in to the internal counter at positive edge of counter clock input ($\overline{CCK}$). In the counter mode, internal counter counts up at the positive of the counter clock. If the counter clear input ($\overline{CCLR}$) is held "L", the internal counter is cleared synchronously to the counter clock.
The internal counter's outputs are stored in the output register at the positive edge of the register clock (RCK). If the register clear input ($\overline{RCLR}$) is held "L", the register is cleared synchronously to register clock. At this point, the internal counter outputs do not change. The outputs (Q_A-Q_D) select internal counter outputs or register outputs respectively with the output select input ($R/\overline{C}$).
Two enable inputs (ENT and $\overline{ENP}$) and carry output (RCO) are provided to enable easy cascading of the counters, which facilities easy implementation of N-bit counters without using external gates. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)



NC =
No Internal
Connection

TRUTH TABLE

INPUTS									OUTPUTS				FUNCTION
$\overline{CCLR}$	$\overline{LOAD}$	ENP	ENT	CCK	$\overline{RCLR}$	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	↑	X	X	L	L	L	L	L	L	CLEAR COUNTER
H	L	X	X	↑	X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	L	X	↑	X	X	L	L	NO CHANGE				NO COUNT
H	H	X	L	↑	X	X	L	L	NO CHANGE				NO COUNT
H	H	H	H	↑	X	X	L	L	COUNT UP				COUNT UP
X	X	X	X	↓	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	L	↑	H	L	L	L	L	L	CLEAR REGISTER
X	X	X	X	X	H	↑	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	X	↓	H	L	NO CHANGE				NO LOAD

X : DON'T CARE

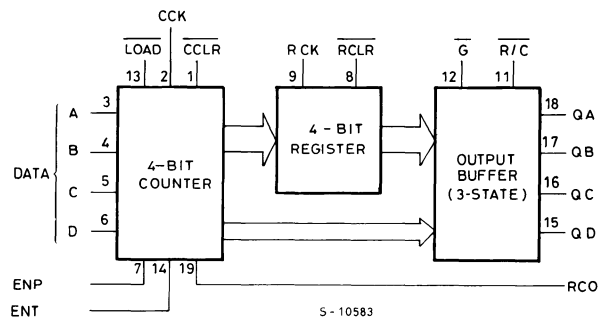
Z : HIGH IMPEDANCE

a-d : THE LEVEL OF STEADY STATE INPUTS AT INPUTS A THROUGH D RESPECTIVELY.

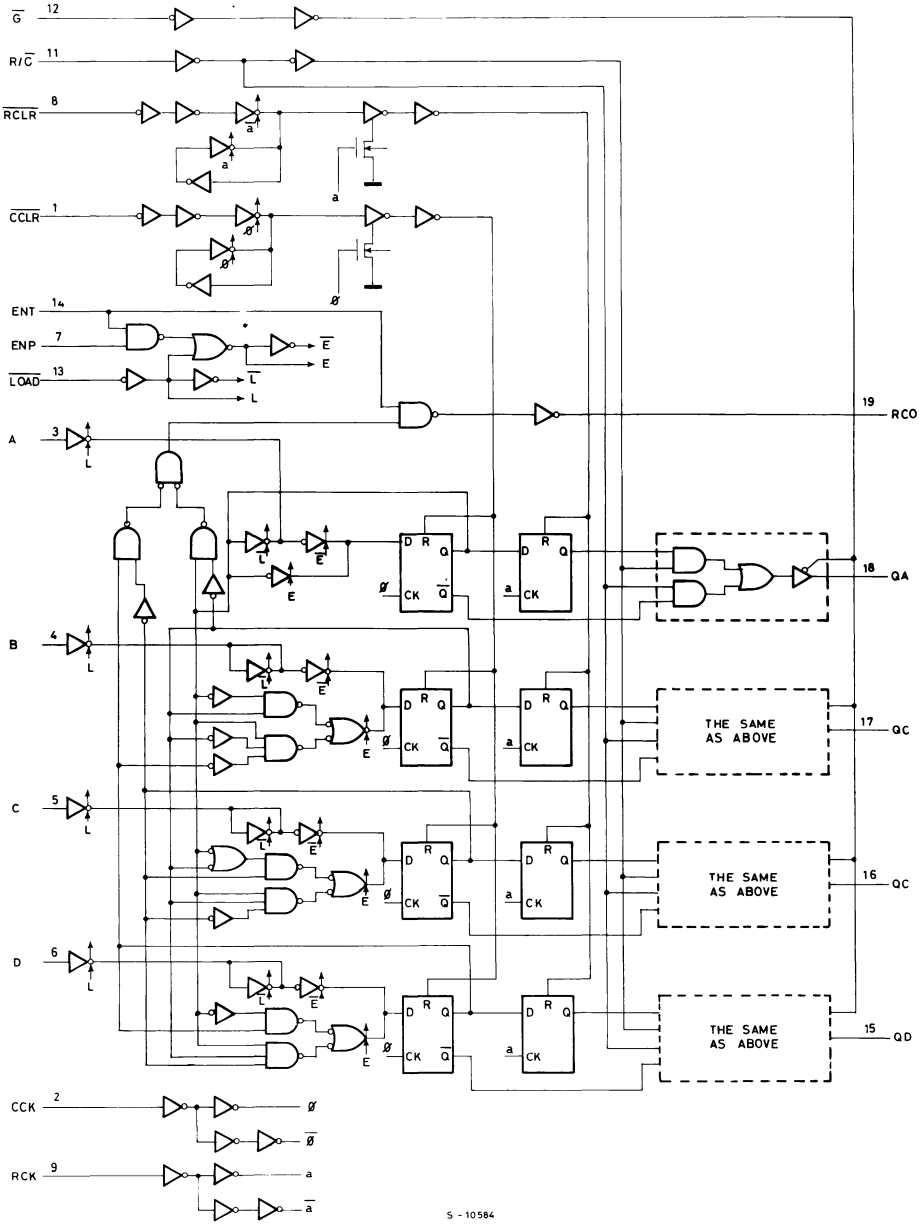
a'-d' : THE LEVEL OF STEADY STATE OUTPUTS AT INTERNAL COUNTER OUTPUTS QA' THROUGH QD' RESPECTIVELY.

HC692 RCO = QA•QD•ENT
HC693 RCO = QA•QB•QC•QD•ENT

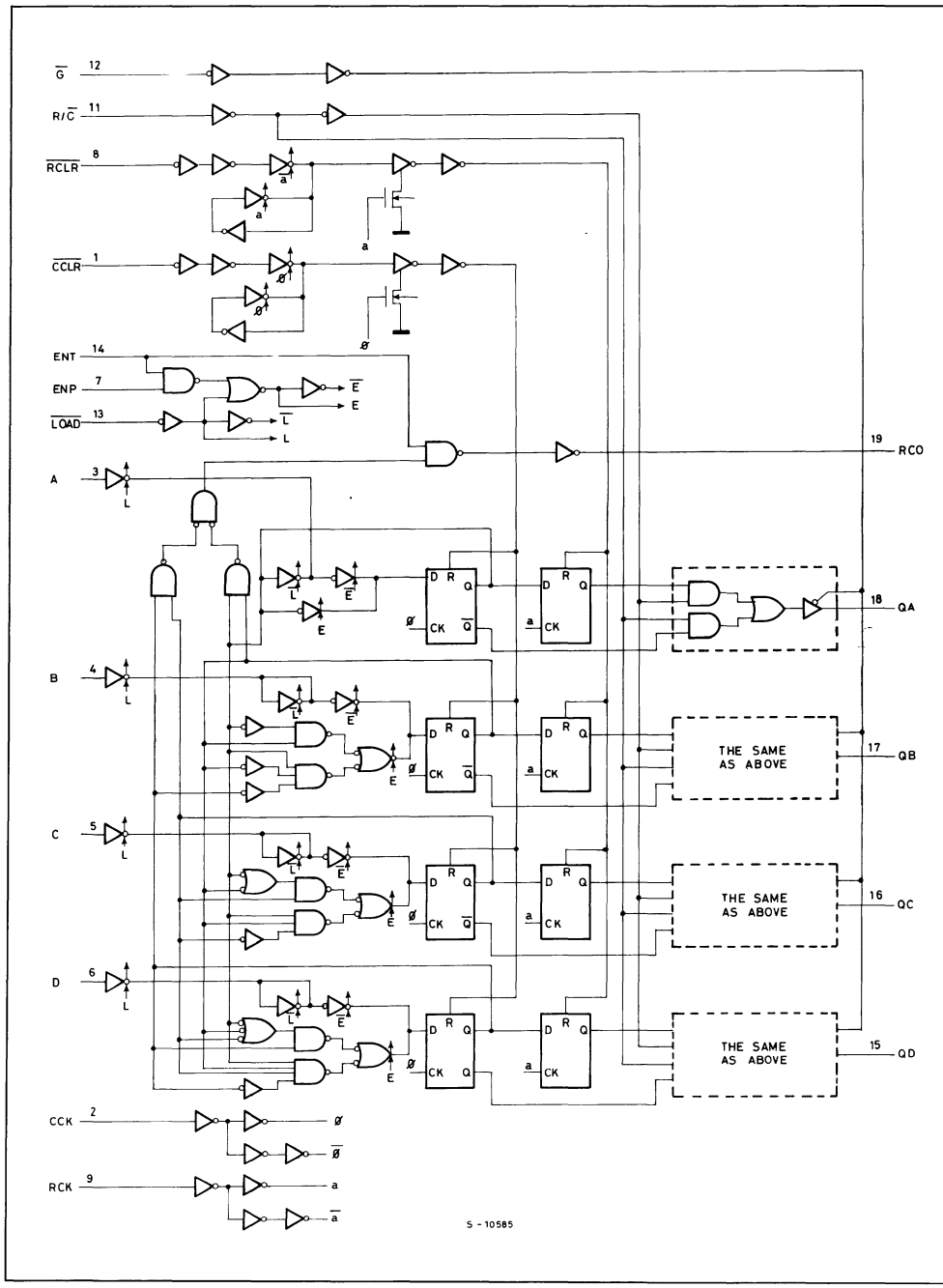
BLOCK DIAGRAM



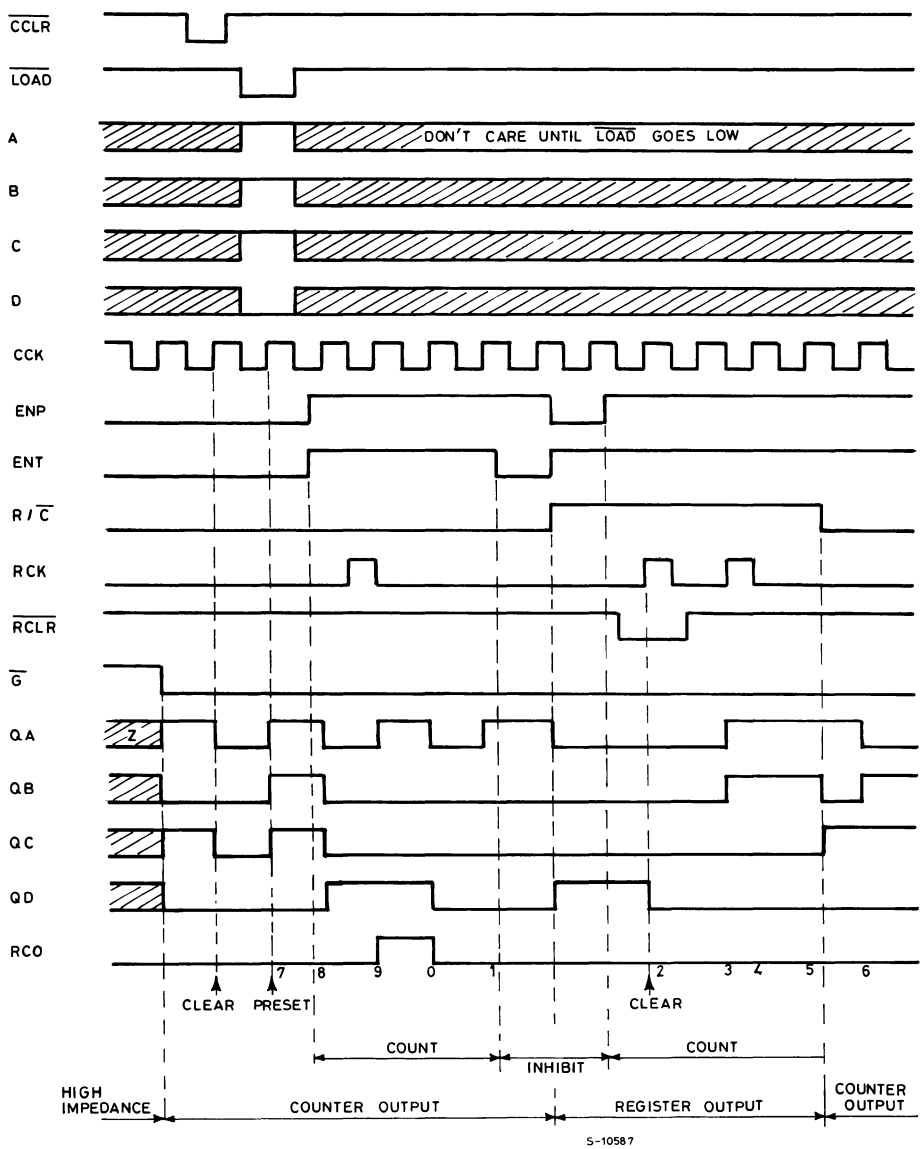
LOGIC DIAGRAM (HC692)



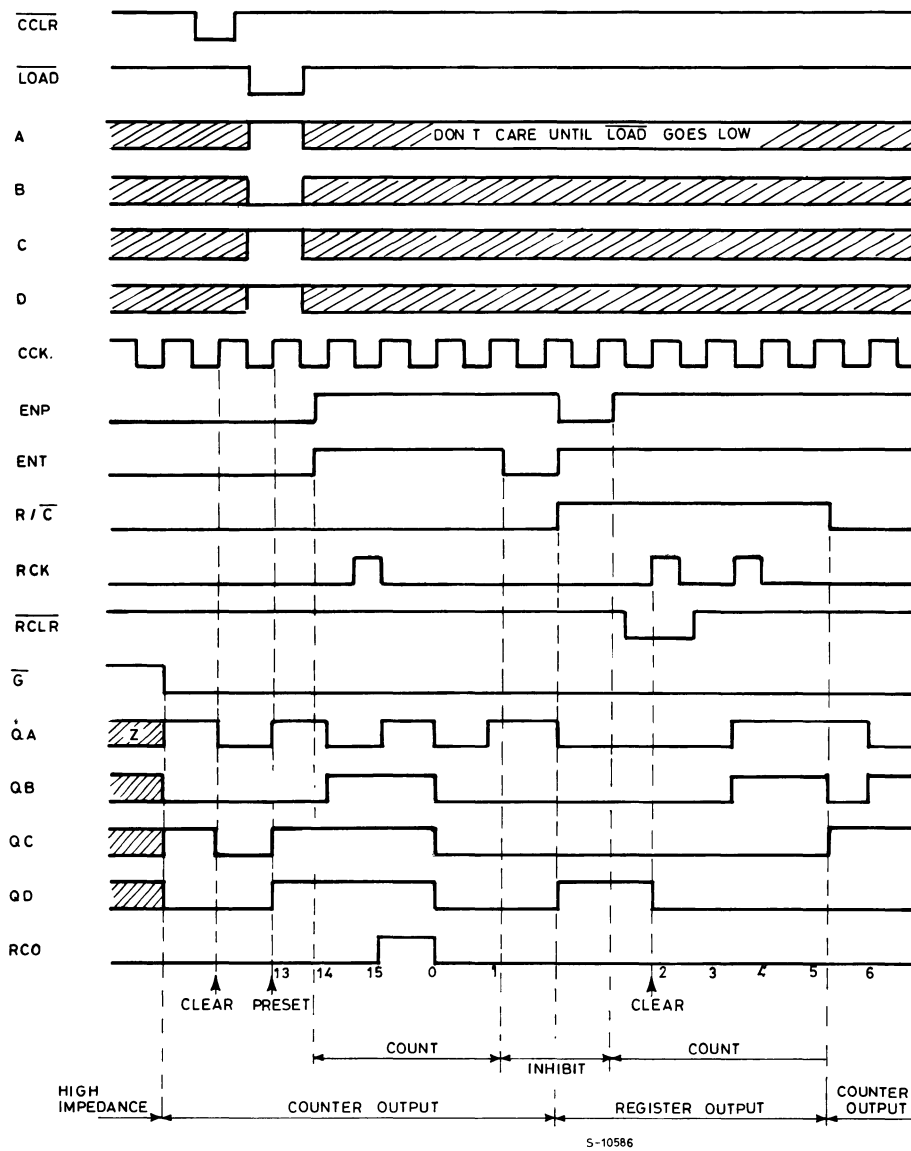
LOGIC DIAGRAM (HC693)



TIMING CHART (HC692)



TIMING CHART (HC693)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		−0.5 to 7	V
V_I	DC Input Voltage		−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage		−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current		± 20	mA
I_{OK}	DC Output Diode Current		± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	(RCO) (QA to QD)	± 25 ±35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current		± 70	mA
P_D	Power Dissipation		500 (*)	mW
T_{stg}	Storage Temperature		−65 to 150	°C

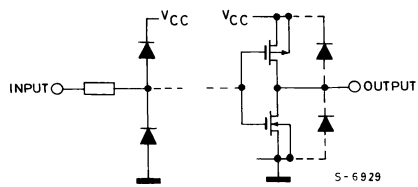
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time		V_{CC} = 2 V	0 to 1000	ns
			V_{CC} = 4.5V	0 to 500	
			V_{CC} = 6 V	0 to 400	

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0 4.5 6.0	V_{IN} V_{IH} or V_{IL}	I_{OH} −20 μA	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	1.9 4.4 5.9	— — —	V
		4.5 6.0	Q_A-Q_D	−6.0 mA −7.8 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	
		4.5 6.0	RCO	−4.0 mA −5.2 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	
V_{OL}	Low Level Output Voltage	2.0 4.5 6.0	V_{IN} V_{IH} or V_{IL}	I_{OL} 20 μA	— — —	0 0 0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
		4.5 6.0	Q_A-Q_D	6.0 mA 7.8 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40	
		4.5 6.0	RCO	4.0 mA 5.2 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40	
I_{OZ}	3-State Off Leak Current	6.0	$V_{IN} = V_{IL}$ or V_{IH} $V_{OUT} = V_{CC}$ or GND		—	—	±0.5	—	±0.5	—	±10	μA
I_{IN}	Input Leakage Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	
I_{CC}	Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	4.0	—	40.0	—	80.0	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

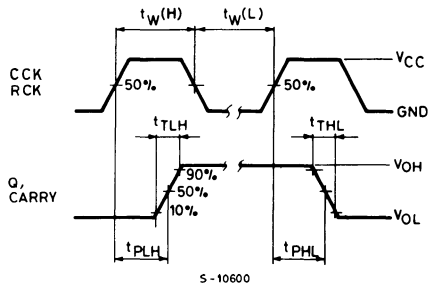
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (Q)	2.0 4.5 6.0		— — —	25 7 6	60 12 10	— — —	75 15 13	— — —	90 18 15	ns
t_{TLH} t_{THL}	Output Transition Time (RCO)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CCK-Q)	2.0 4.5 6.0		— — —	132 33 28	260 52 44	— — —	325 65 55	— — —	390 78 66	ns
t_{PLH} t_{PHL}	Propagation Delay Time (RCK-Q)	2.0 4.5 6.0		— — —	136 34 29	260 52 44	— — —	325 65 55	— — —	390 78 66	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

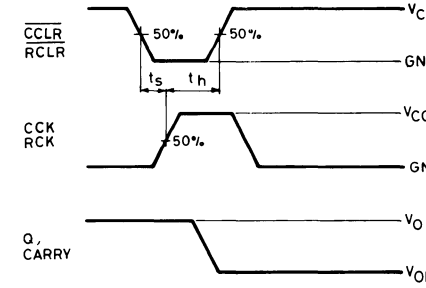
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (CCK-RCO)	2.0		—	108	210	—	265	—	315	ns
		4.5		—	27	42	—	53	—	63	
		6.0		—	23	36	—	45	—	54	
t_{PLH} t_{PHL}	Propagation Delay Time (R/C-Q)	2.0		—	92	180	—	225	—	270	ns
		4.5		—	23	36	—	45	—	54	
		6.0		—	20	31	—	38	—	46	
t_{PLH} t_{PHL}	Propagation Delay Time (ENT-RCO)	2.0		—	48	95	—	120	—	145	ns
		4.5		—	12	19	—	24	—	29	
		6.0		—	10	16	—	20	—	25	
f_{MAX}	Maximum Clock Frequency	2.0		4	8	—	3	—	3	—	MHz
		4.5		20	30	—	16	—	13	—	
		6.0		24	35	—	19	—	15	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CCK, RCK)	2.0		—	48	125	—	155	—	190	ns
		4.5		—	12	25	—	31	—	38	
		6.0		—	10	21	—	26	—	32	
t_s	Minimum Set-up Time ($\overline{LOAD}$,ENT,ENP)	2.0		—	68	150	—	190	—	225	ns
		4.5		—	17	30	—	38	—	45	
		6.0		—	14	26	—	33	—	38	
t_s	Minimum Set-up Time (A, B, C, D)	2.0		—	48	125	—	155	—	190	ns
		4.5		—	12	25	—	31	—	38	
		6.0		—	10	21	—	26	—	32	
t_s	Minimum Set-up Time ($\overline{CCLR}$, $\overline{RCLR}$)	2.0		—	48	125	—	155	—	190	ns
		4.5		—	12	25	—	31	—	38	
		6.0		—	10	21	—	26	—	32	
t_s	Minimum Set-up Time (CCK-RCK)	2.0		—	68	150	—	190	—	225	ns
		4.5		—	17	30	—	38	—	45	
		6.0		—	14	26	—	33	—	38	
t_h	Minimum Data Hold Time	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{PZL} t_{PZH}	3-State Output Enable Time	2.0	$R_L = 1k\Omega$	—	64	130	—	165	—	195	ns
		4.5		—	16	26	—	33	—	39	
		6.0		—	14	22	—	28	—	33	
t_{PLZ} t_{PHZ}	3-State Output Disable Time	2.0	$R_L = 1k\Omega$	—	80	145	—	180	—	220	ns
		4.5		—	20	29	—	36	—	44	
		6.0		—	17	25	—	31	—	38	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{OUT}	Output Capacitance			—	10	—	—	—	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance			—	95	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test circuit).
Average operating current can be obtained from the equation: $I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

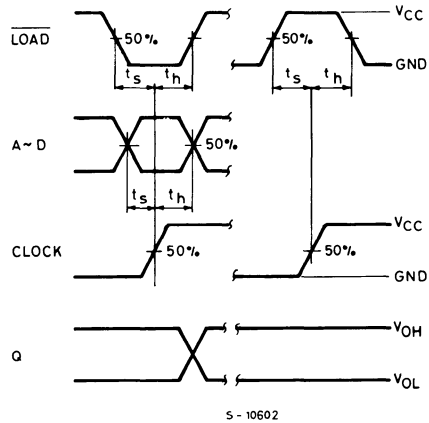
SWITCHING CHARACTERISTICS TEST WAVEFORM



S-10600

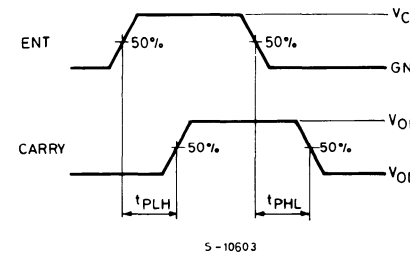


S-10601

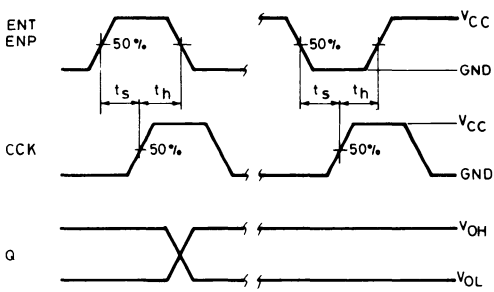


S-10602

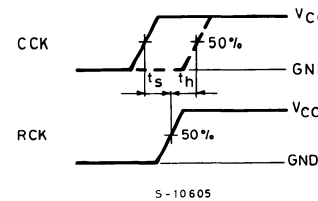
(Fix Maximum Count)



S-10603

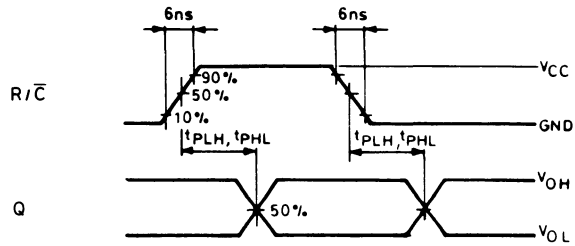


S-10604



S-10605

SWITCHING CHARACTERISTICS (Continued)



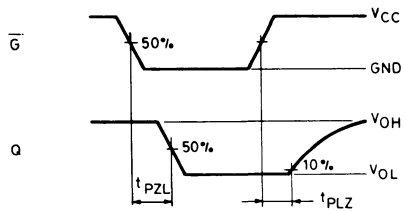
S-10606

t_{PLZ}, t_{PZL}

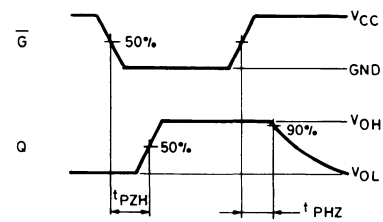
The 1kΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line. All inputs except $\overline{G}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{G}$ input is held low.

t_{PHZ}, t_{PZH}

The 1kΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{G}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{G}$ input is held low.

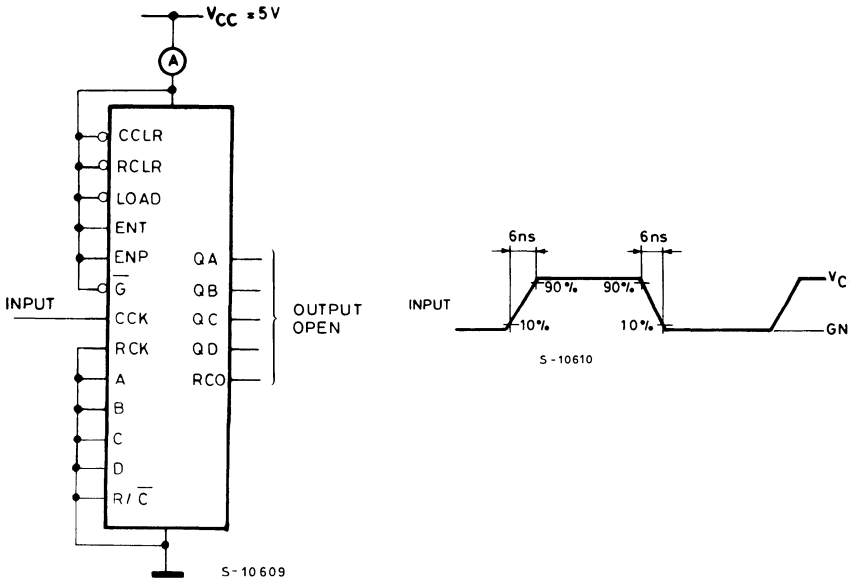


S- 10607



S- 10608

TEST CIRCUIT I_{CC} (Opr.)

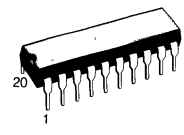


SGS-THOMSON MICROELECTRONICS

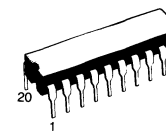
M54/74HC696
M54/74HC697

HC696 U/D DECADE COUNTER/REGISTER (3-STATE)
HC697 U/D 4-BIT BINARY COUNTER/REGISTER (3-STATE)

- HIGH SPEED
  f_{MAX} = 33MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS (FOR Q_A to Q_D)
  10 LSTTL LOADS (FOR RCO)
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.) FOR Q_A to Q_D
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.) FOR RCO OUTPUT
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC}(OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH LSTTL 54/74LS696/697



B1N
Plastic Package



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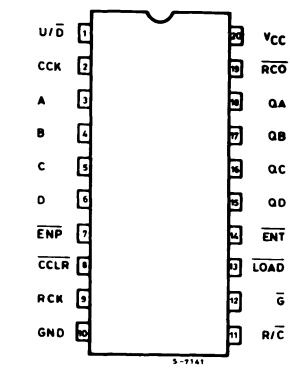
M74HCXXX M1

PIN CONNECTIONS (top view)



NC =
No Internal
Connection

DESCRIPTION

The HC696/697 are high speed CMOS up/down counters fabricated with silicon gate C²MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The HC696 is a BCD DECADE COUNTER, and the HC697 is 4-BIT BINARY COUNTER. Both devices have register. They count on the positive edge of the counter clock input (CCK) when selected by the "Counter Mode". If the input U/D is held "H", the internal counter counts up, and held "L", counts down. The internal counter's outputs are stored in the output register at the positive edge of register clock (RCK). The outputs (QA - QD) are internal counter outputs or register outputs respectively and are selected by R/C. The clear function are cleared asynchronously to the clock. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUTS									OUTPUTS				FUNCTION
$\overline{CCLR}$	$\overline{LOAD}$	$\overline{ENP}$	$\overline{ENT}$	CCK	U/$\overline{D}$	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	X	X	X	L	L	L	L	L	L	CLEAR COUNTER
H	L	X	X	↑	X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	H	X	↑	X	X	L	L	NO CHANGE				NO COUNT
H	H	X	H	↑	X	X	L	L	NO CHANGE				NO COUNT
H	H	L	L	↑	H	X	L	L	COUNT UP				COUNT UP
H	H	L	L	↑	L	X	L	L	COUNT DOWN				COUNT DOWN
H	X	X	X	↓	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	X	↑	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	X	↓	H	L	NO CHANGE				NO LOAD

X : DON'T CARE

Z : HIGH IMPEDANCE

a-d : THE LEVEL OF STEADY STATE INPUT AT INPUTS A THROUGH D RESPECTIVELY.

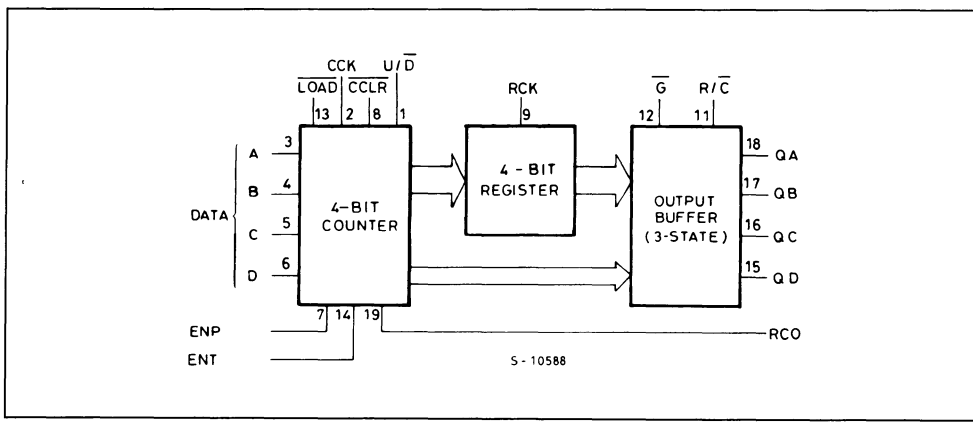
a'-d' : THE LEVEL OF STEADY STATE OUTPUTS AT INTERNAL COUNTER OUTPUTS QA' THROUGH QD' RESPECTIVELY.

$\overline{RCO}$ FUNCTION

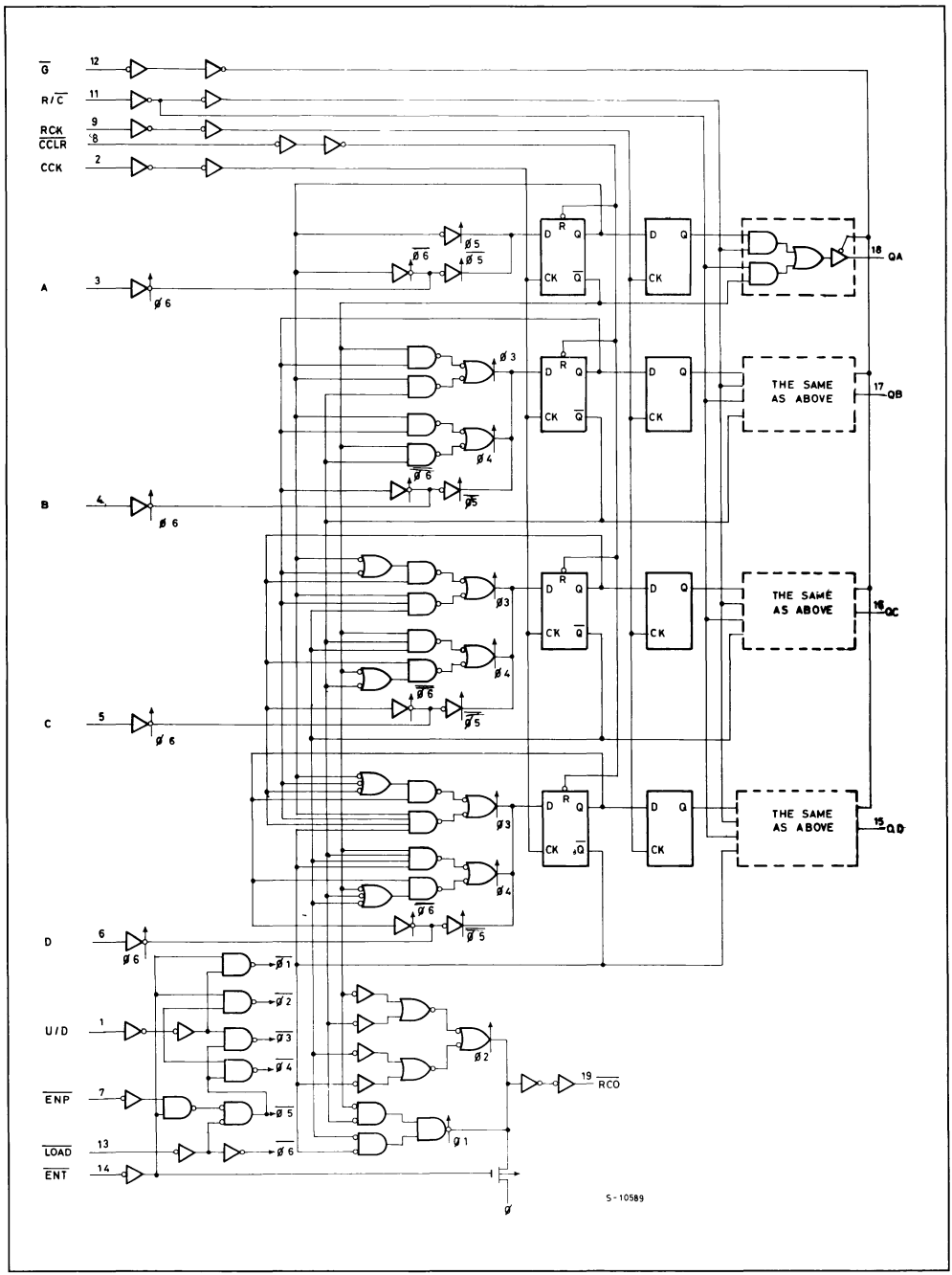
HC696 - $\overline{RCO} = \overline{(UP \cdot QA \cdot QD \cdot ENT + \overline{UP} \cdot \overline{QA} \cdot \overline{QB} \cdot \overline{QC} \cdot \overline{QD} \cdot ENT)}$

HC697 - $\overline{RCO} = \overline{(UP \cdot QA \cdot QB \cdot QC \cdot QD \cdot ENT + \overline{UP} \cdot \overline{QA} \cdot \overline{QB} \cdot \overline{QC} \cdot \overline{QD} \cdot ENT)}$

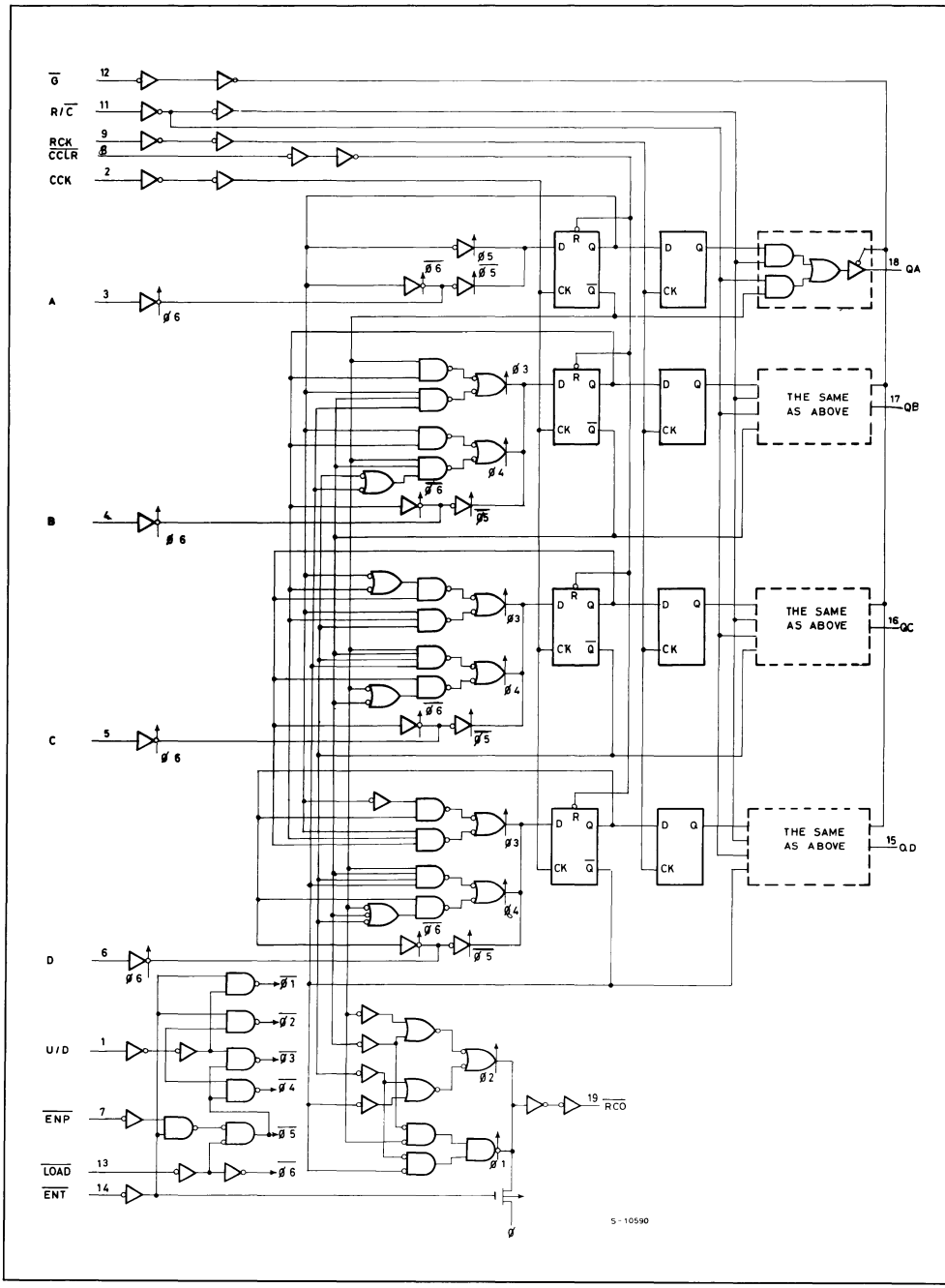
BLOCK DIAGRAM



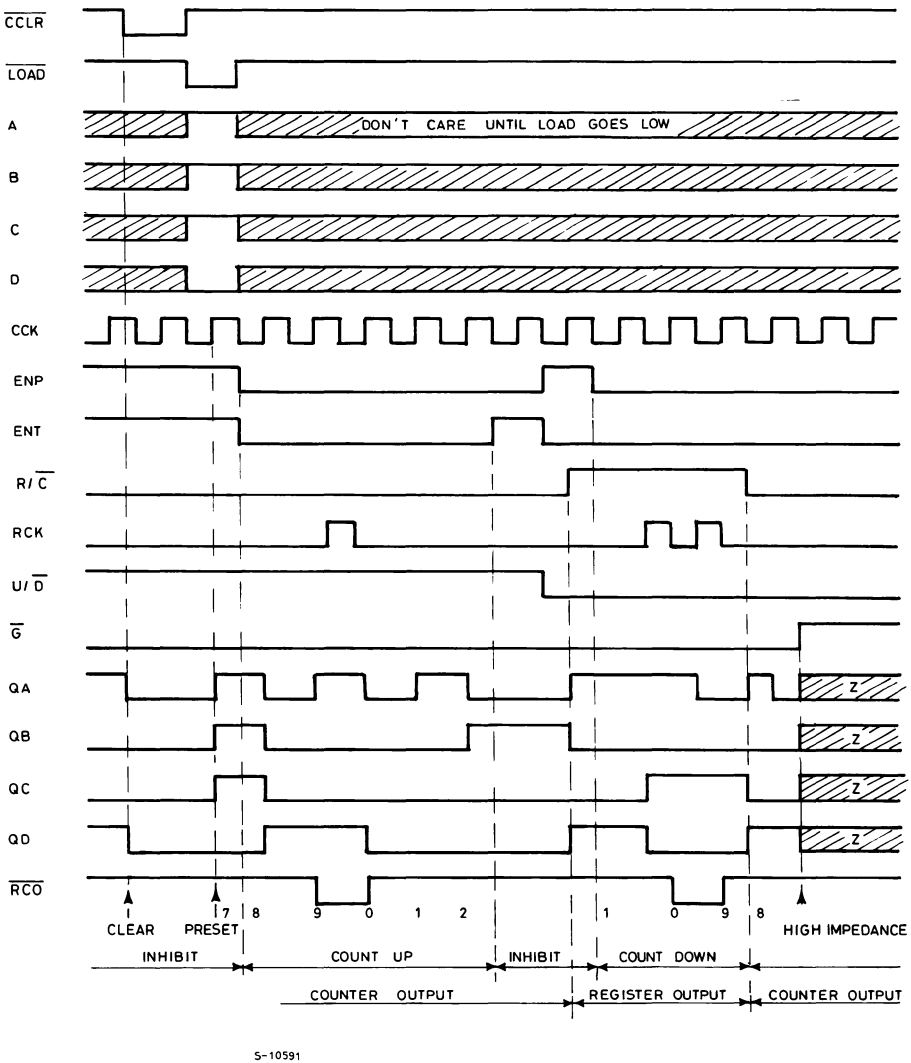
LOGIC DIAGRAM (HC696)



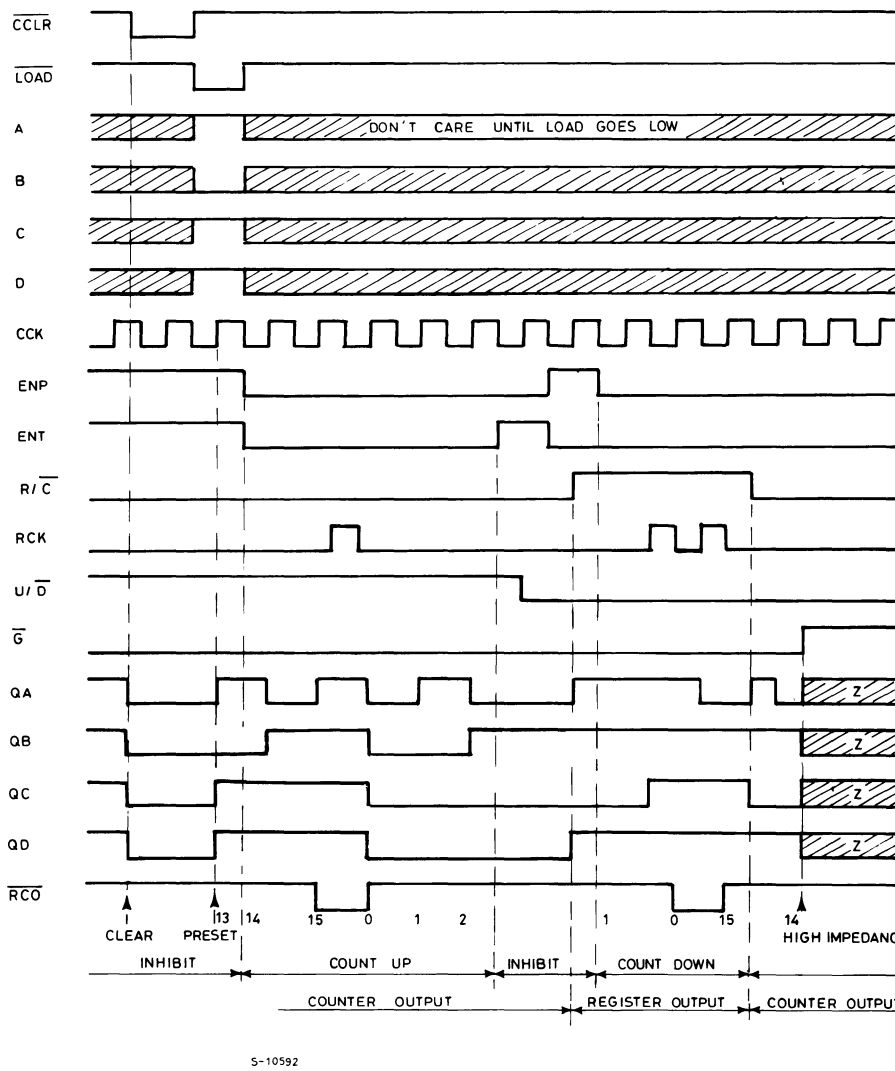
LOGIC DIAGRAM (HC697)



TIMING CHART (HC696)



TIMING CHART (HC697)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin (RCO) (QA to QD)	± 20 ±35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

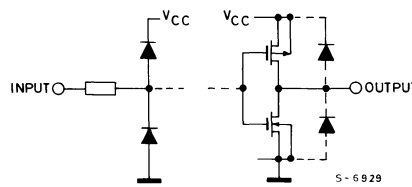
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW:≅65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V 4.5V 6 V	0 to 1000 0 to 500 0 to 400	ns

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_{IN}	I_{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0	or V_{IL}		5.9	6.0	—	5.9	—	5.9	—	
		4.5	Q_A-Q_H	−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
		4.5	RCO	−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IN}	I_{OL}	—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0	or V_{IL}		—	0	0.1	—	0.1	—	0.1	
		4.5	Q_A-Q_H	6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
		4.5	RCO	4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{OZ}	3-State Off Leak Current	6.0	$V_{IN} = V_{IL}$ or V_{IH} $V_{OUT} = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±10	μA
I_{IN}	Input Leakage Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	
I_{CC}	Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	4.0	—	40.0	—	80.0	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (Q)	2.0		—	25	60	—	75	—	90	ns
		4.5		—	7	12	—	15	—	18	
		6.0		—	6	10	—	13	—	15	
t_{TLH} t_{THL}	Output Transition Time ($\overline{RCO}$)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (CCK-Q)	2.0		—	136	260	—	325	—	390	ns
		4.5		—	34	52	—	65	—	78	
		6.0		—	29	44	—	55	—	66	
t_{PLH} t_{PHL}	Propagation Delay Time (RCK-Q)	2.0		—	116	225	—	280	—	340	ns
		4.5		—	29	45	—	56	—	68	
		6.0		—	25	38	—	48	—	58	

AC ELECTRICAL CHARACTERISTICS (Continued)

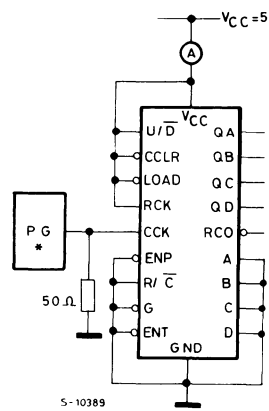
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (CCK-$\overline{RCO}$)	2.0		—	160	305	—	385	—	460	ns
		4.5		—	40	61	—	77	—	92	
		6.0		—	34	52	—	66	—	78	
t_{PLH} t_{PHL}	Propagation Delay Time (R/$\overline{C}$-Q)	2.0		—	100	195	—	245	—	295	ns
		4.5		—	25	39	—	49	—	59	
		6.0		—	21	33	—	42	—	50	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{ENT}$-$\overline{RCO}$)	2.0		—	116	225	—	280	—	340	ns
		4.5		—	29	45	—	56	—	68	
		6.0		—	25	38	—	48	—	58	
t_{PHL}	Propagation Delay Time ($\overline{CCLR}$-Q)	2.0		—	148	285	—	355	—	430	ns
		4.5		—	37	57	—	71	—	86	
		6.0		—	31	48	—	60	—	73	
t_{PHL}	Propagation Delay Time ($\overline{CCLR}$-$\overline{RCO}$)	2.0		—	172	325	—	405	—	490	ns
		4.5		—	43	65	—	81	—	98	
		6.0		—	37	55	—	69	—	83	
f_{MAX}	Maximum Clock Frequency	2.0		4	8	—	3	—	3	—	MHz
		4.5		20	30	—	16	—	13	—	
		6.0		24	35	—	19	—	15	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CCK, RCK)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
$t_{W(L)}$	Mimum Pulse Width ($\overline{CCLR}$)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{REM}	Minimum Removal Time ($\overline{CCLR}$)	2.0		—	—	5	—	5	—	5	ns
		4.5		—	—	5	—	5	—	5	
		6.0		—	—	5	—	5	—	5	
t_s	Minimum Set-up Time ($\overline{LOAD}$,$\overline{ENT}$,$\overline{ENP}$)	2.0		—	96	225	—	280	—	340	ns
		4.5		—	24	45	—	56	—	68	
		6.0		—	20	38	—	48	—	58	
t_s	Minimum Set-up Time (A, B, C, D)	2.0		—	20	75	—	95	—	110	ns
		4.5		—	5	15	—	19	—	22	
		6.0		—	4	13	—	16	—	19	
t_s	Minimum Set-up Time (CCK-RCK)	2.0		—	52	125	—	155	—	190	ns
		4.5		—	13	25	—	31	—	38	
		6.0		—	11	21	—	26	—	32	
t_s	Minimum Set-up Time (U/$\overline{D}$)	2.0		—	64	150	—	190	—	225	ns
		4.5		—	16	30	—	38	—	45	
		6.0		—	14	26	—	33	—	38	
t_h	Minimum Hold Time	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	

AC ELECTRICAL CHARACTERISTICS (Continued)

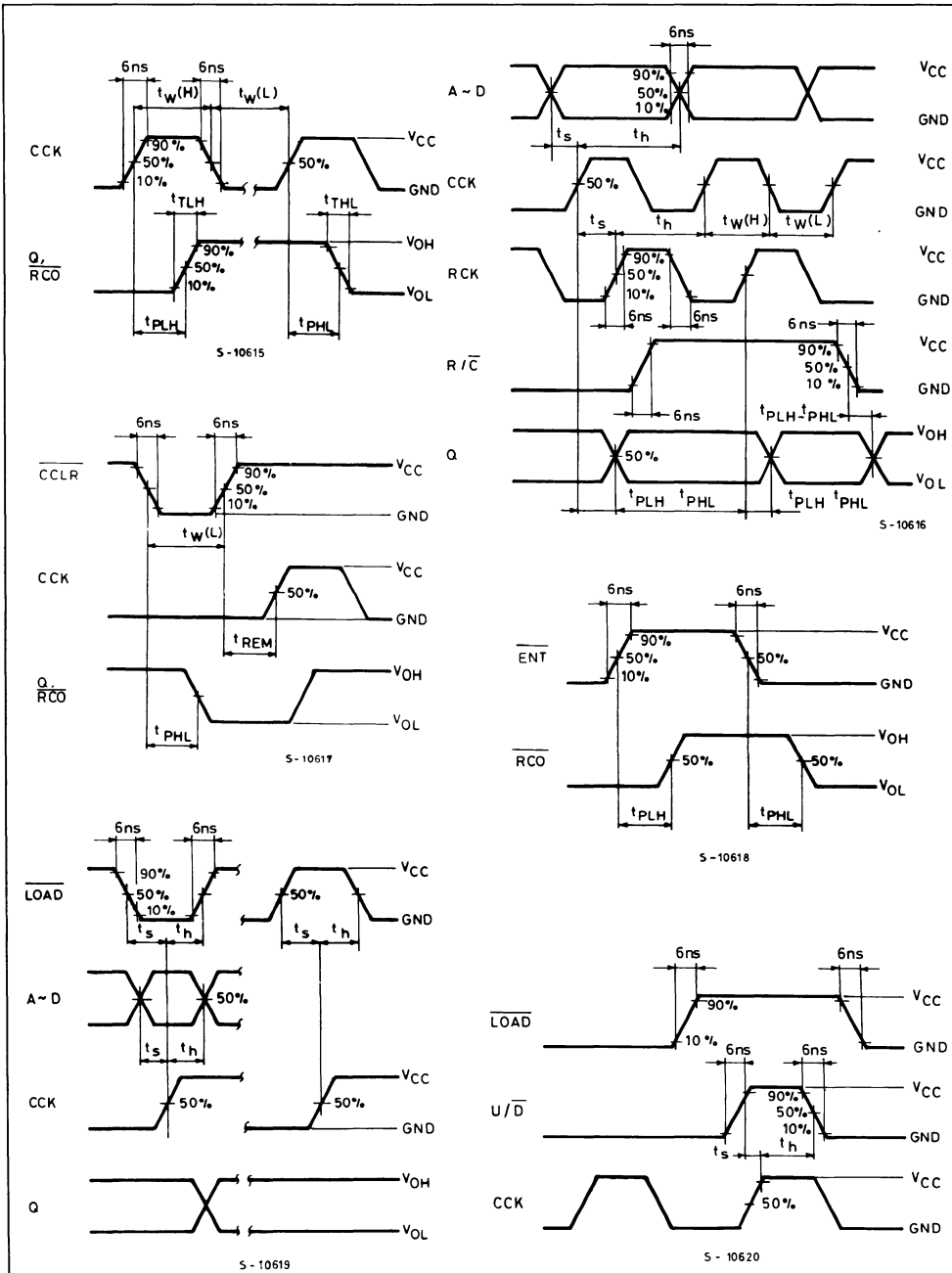
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PZL} t_{PZH}	3-State Output Enable Time	2.0	$R_L = 1k\Omega$	—	64	130	—	165	—	195	ns
		4.5		—	16	26	—	33	—	39	
		6.0		—	14	22	—	28	—	33	
t_{PLZ} t_{PHZ}	3-State Output Disable Time	2.0	$R_L = 1k\Omega$	—	92	185	—	230	—	280	ns
		4.5		—	23	37	—	46	—	56	
		6.0		—	20	31	—	39	—	48	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance		HC696	—	90	—	—	—	—	—	pF
			HC697	—	92	—	—	—	—	—	

Note (*) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained from the equation:
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

TEST CIRCUIT I_{CC} (Opr.)

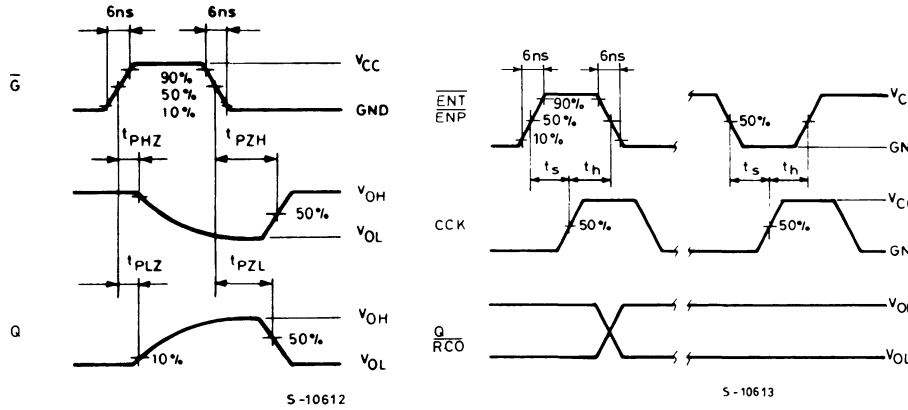


SWITCHING CHARACTERISTICS TEST WAVEFORM



SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)

OUTPUT DISABLE, ENABLE

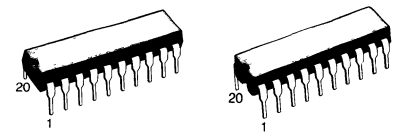


SGS-THOMSON MICROELECTRONICS

M54/74HC698
M54/74HC699

HC698 U/D DECADE COUNTER/REGISTER (3-STATE)
HC699 U/D 4-BIT BINARY COUNTER/REGISTER (3-STATE)

- HIGH SPEED
  f_{MAX} = 33MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS (FOR Q_A to Q_D)
  10 LSTTL LOADS (FOR RCO)
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 6 mA (MIN.) FOR Q_A to Q_D OUTPUT
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.) FOR RCO OUTPUT
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC}(OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH LSTTL 54/74LS698/699



B1N
Plastic Package

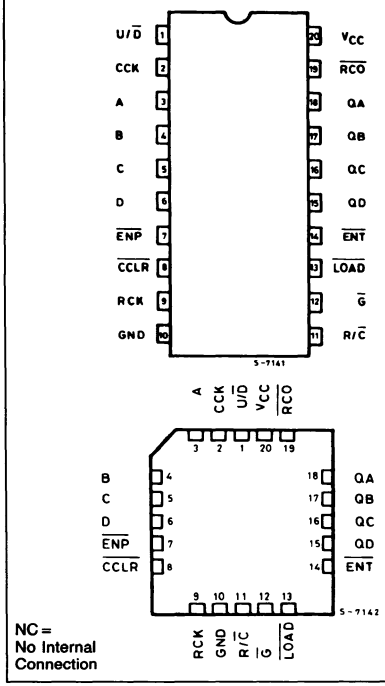
F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX C1
M74HCXXX M1

PIN CONNECTIONS (top view)



NC = No Internal Connection

DESCRIPTION

The HC698/699 are high speed CMOS 4-BIT BINARY/DECADE COUNTER/REGISTER 3-STATE fabricated in silicon gate C²MOS technology.

It has the same high speed performance of LSTTL combined with true CMOS low power consumption. These devices incorporate a synchronous up/down counter, a four-bit D-type register, and quadruple two-line to one-line multiplexers with three-state outputs in a single 20-pin package. The up/down counter is programmable from the data inputs and feautures enable $\overline{P}$ and enable $\overline{T}$ and a ripple-carry output for easy expansion. The register/counter select input, R/C, selects the counter when low or the register when high for the three-state outputs, QA, QB, QC, and QD.

Both the counter clock CCK and register clock RCK are positive-edge triggered. The counter clear $\overline{CCLR}$ is active low and is, synchronous.
All inputs are equipped with protection circuits againts static discharge and transient excess voltage.

TRUTH TABLE

INPUTS									OUTPUTS				FUNCTION
$\overline{CCLR}$	$\overline{LOAD}$	$\overline{ENP}$	$\overline{ENT}$	CCK	U/$\overline{D}$	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	↑	X	X	L	L	L	L	L	L	CLEAR COUNTER
H	L	X	X	↑	X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	H	X	↑	X	X	L	L	NO CHANGE				NO COUNT
H	H	X	H	↑	X	X	L	L	NO CHANGE				NO COUNT
H	H	L	L	↑	H	X	L	L	COUNT UP				COUNT UP
H	H	L	L	↑	L	X	L	L	COUNT DOWN				COUNT DOWN
X	X	X	X	↓	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	X	↑	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	X	↓	H	L	NO CHANGE				NO LOAD

X : DON'T CARE

Z : HIGH IMPEDANCE

a-d : THE LEVEL OF STEADY STATE INPUT AT INPUTS A THROUGH D RESPECTIVELY.

a'-d' : THE LEVEL OF STEADY STATE OUTPUTS AT INTERNAL COUNTER OUTPUTS QA' THROUGH QD' RESPECTIVELY.

$\overline{RCO}$ FUNCTION:

$\overline{RCO} = (UP \cdot QA \cdot QD \cdot ENT + \overline{UP} \cdot \overline{QA} \cdot \overline{QB} \cdot \overline{QC} \cdot \overline{QD} \cdot ENT)$ (HC698)

$\overline{RCO} = (UP \cdot QA \cdot QB \cdot QC \cdot QD \cdot ENT + \overline{UP} \cdot \overline{QA} \cdot \overline{QB} \cdot \overline{QC} \cdot \overline{QD} \cdot ENT)$ (HC699)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current (RCO) Per Output Pin (QA to QD)	± 20 ±35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

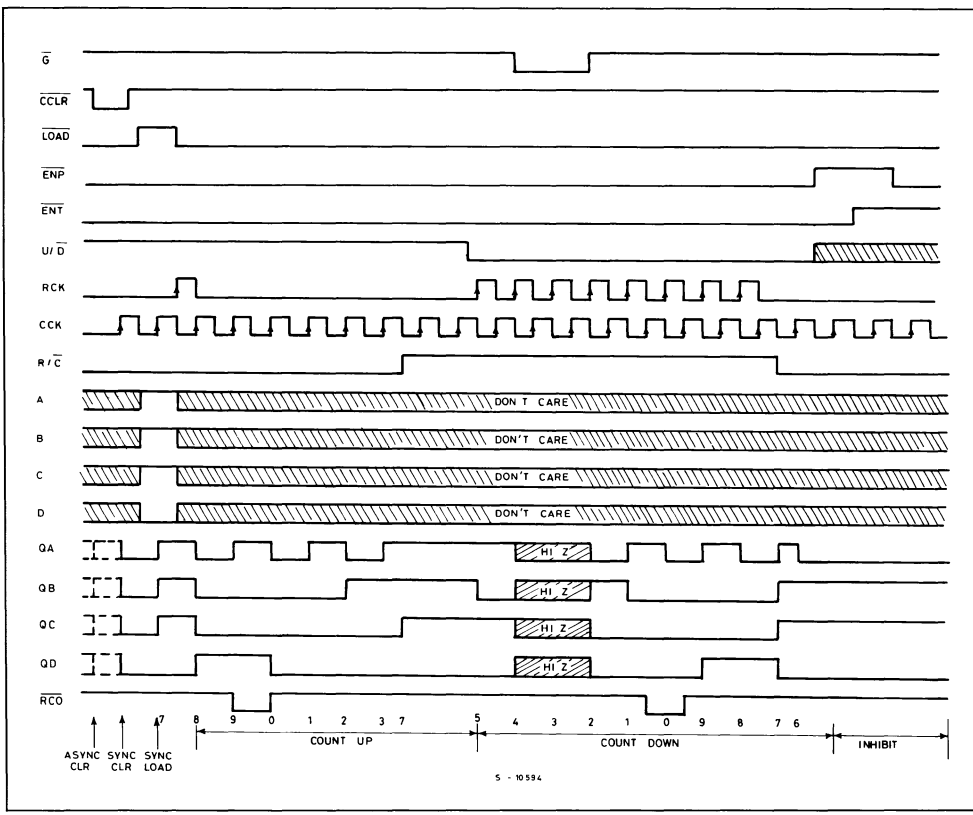
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

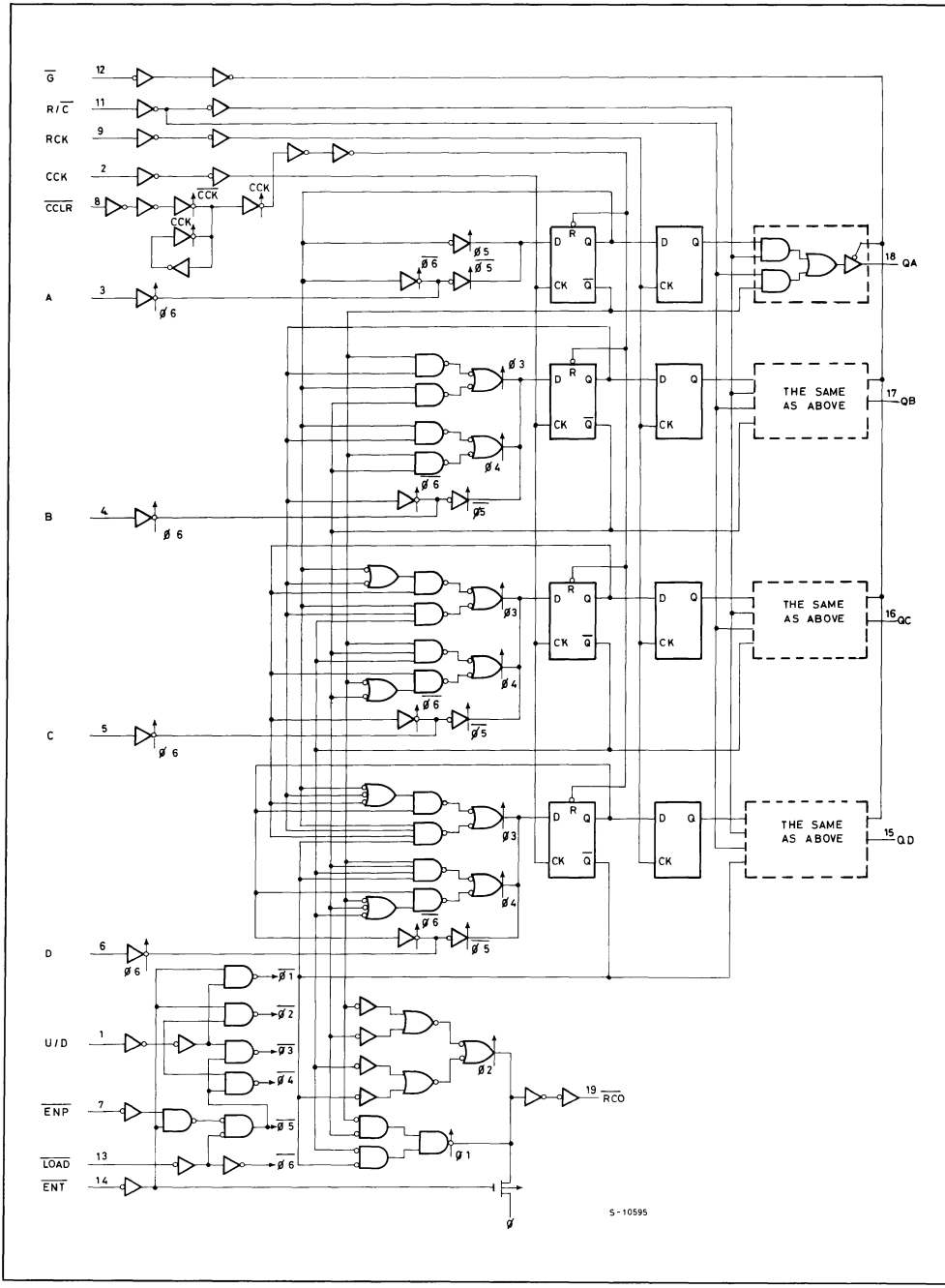
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V: 0 to 1000 V_{CC} 4.5V: 0 to 500 V_{CC} 6 V: 0 to 400	ns

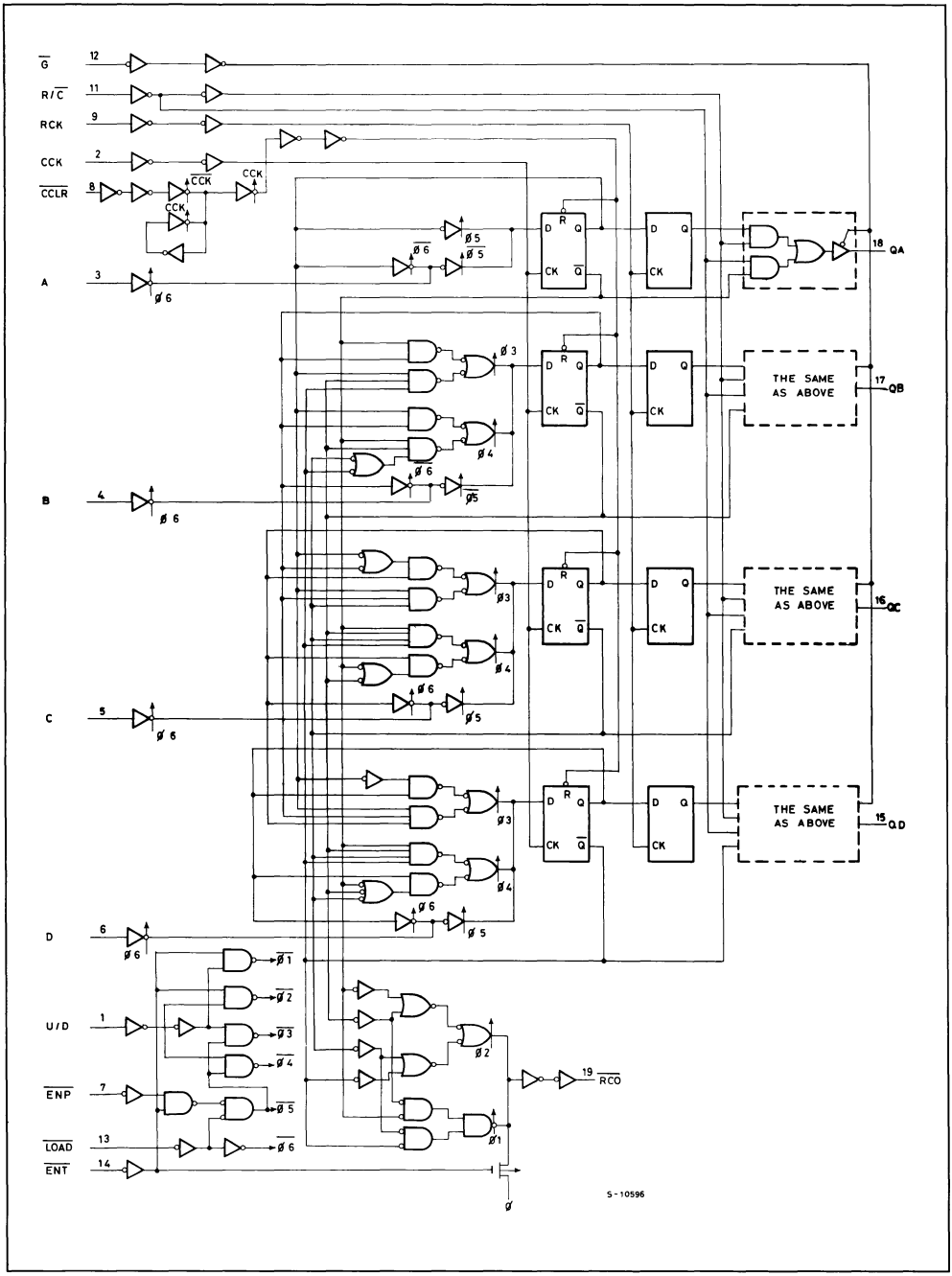
DECADE COUNTER, SYNCHRONOUS CLEAR (HC698)



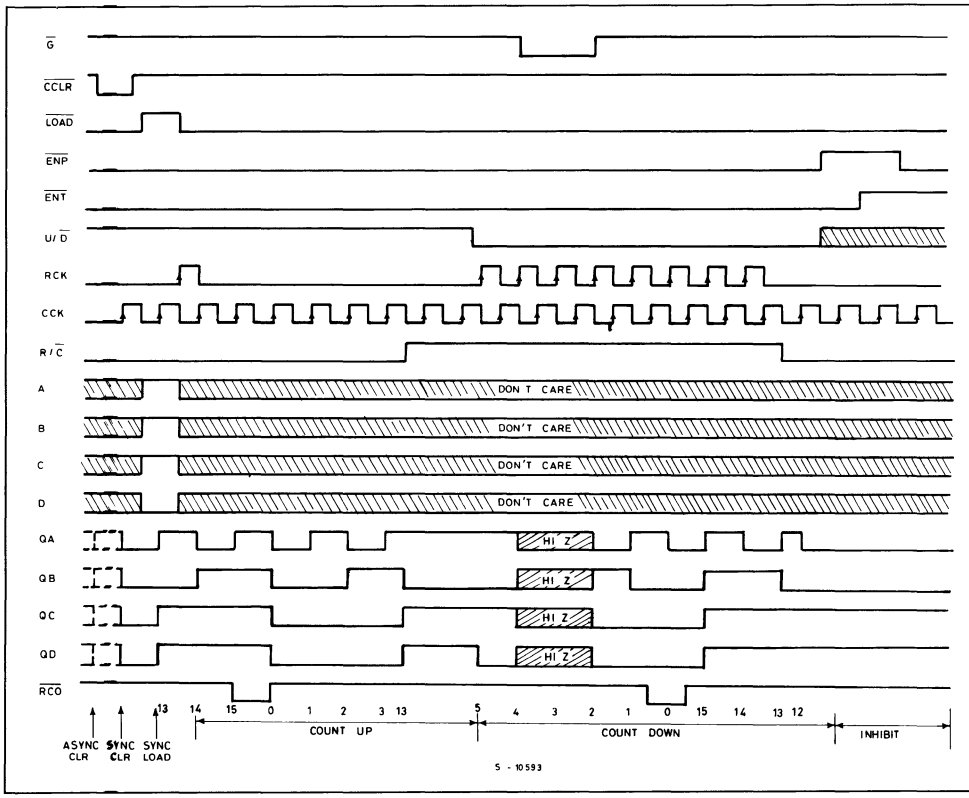
LOGIC DIAGRAM (HC698)



LOGIC DIAGRAM (HC699)



BYNARY COUNTER, SYNCHRONOUS CLEAR (HC699)



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_{IN}	I_{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0	or V_{IL}		5.9	6.0	—	5.9	—	5.9	—	
		4.5	Q_A-Q_H	−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
		4.5	RCO	−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	

DC SPECIFICATIONS (Continued)

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min	Typ	Max	Min	Max	Min	Max	
V_{OL}	Low Level Output Voltage	2.0	V_{IN}	I_{OL}	—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0	or V_{IL}		—	0	0.1	—	0.1	—	0.1	
		4.5	Q_A-Q_H	6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
		4.5	RCO	4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{OZ}	3-State Off Leak Current	6.0	$V_{IN} = V_{IL}$ or V_{IH} $V_{OUT} = V_{CC}$ or GND		—	—	±0.5	—	±0.5	—	±10	μA
I_{IN}	Input Leakage Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	
I_{CC}	Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	4.0	—	40.0	—	80.0	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (Q OUTS)	2.0 4.5 6.0		— — —	25 7 6	60 12 10	— — —	75 15 13	— — —	90 18 15	ns
t_{TLH} t_{THL}	Output Transition Time ($\overline{RCO}$ OUT)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	113 23 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CCK-Q)	2.0 4.5 6.0		— — —	116 29 25	225 45 38	— — —	280 56 48	— — —	338 68 57	ns
t_{PLH} t_{PHL}	Propagation Delay Time (RCK-Q)	2.0 4.5 6.0		— — —	100 25 21	195 39 33	— — —	245 49 42	— — —	293 59 50	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CCK-$\overline{RCO}$)	2.0 4.5 6.0		— — —	144 36 31	275 55 47	— — —	345 69 59	— — —	413 83 70	ns
t_{PLH} t_{PHL}	Propagation Delay Time (R/$\overline{C}$/-Q)	2.0 4.5 6.0		— — —	92 23 20	175 35 30	— — —	220 44 37	— — —	263 53 45	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{ENT}$-$\overline{RCO}$)	2.0 4.5 6.0		— — —	96 24 20	190 38 32	— — —	240 48 41	— — —	285 57 48	ns
t_{PHL}	Propagation Delay Time (CCK-Q) [RESET MODE]	2.0 4.5 6.0		— — —	124 31 26	240 48 41	— — —	300 60 51	— — —	360 72 61	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

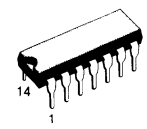
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency (CCK & RCK)	2.0 4.5 6.0		3.5 18 21	7 28 33	— — —	2.8 14 16	— — —	2.4 12 14	— — —	MHz
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CCK-RCK)	2.0 4.5 6.0		— — —	44 11 9	100 20 17	— — —	125 25 21	— — —	150 30 26	ns
t_S	Minimum Set-Up Time ($\overline{ENP}$,$\overline{ENT}$,$\overline{LOAD}$)	2.0 4.5 6.0		— — —	84 21 18	200 40 34	— — —	250 50 43	— — —	300 60 51	ns
t_S	Minimum Set-Up Time (A,B,C,D)	2.0 4.5 6.0		— — —	16 4 3	50 10 9	— — —	60 12 11	— — —	75 15 13	ns
t_S	Minimum Set-Up Time ($\overline{CCLR}$)	2.0 4.5 6.0		— — —	12 3 2.5	50 10 9	— — —	60 12 11	— — —	75 15 13	ns
$t_{S(W)}$	Minimum Set-Up Time inactive (CCLR)	2.0 4.5 6.0		— — —	12 3 2.5	50 10 9	— — —	60 12 11	— — —	75 15 13	ns
t_S	Minimum Set-Up Time (RCK)	2.0 4.5 6.0		— — —	48 12 10	125 25 21	— — —	160 32 27	— — —	188 38 32	ns
t_S	Minimum Set-Up Time ($\overline{UD}$)	2.0 4.5 6.0		— — —	60 15 13	150 30 26	— — —	190 38 32	— — —	225 45 38	ns
t_h	Minimum Hold Time (ALL INPUTS)	2.0 4.5 6.0		— — —	— — —	5 5 5	— — —	5 5 5	— — —	5 5 5	ns
t_{PZL} t_{PZH}	3-State Outputs Enable Time	2.0 4.5 6.0	R_L = 1kΩ	— — —	56 14 12	110 22 19	— — —	140 28 24	— — —	165 33 28	ns
t_{PLZ} t_{PHZ}	3-State Outputs Disable Time	2.0 4.5 6.0	R_L = 1kΩ	— — —	80 20 17	145 29 25	— — —	180 36 21	— — —	221 44 37	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD}	Power Dissipation Capacitance			—	—	113	—	—	—	—	pF

SGS-THOMSON MICROELECTRONICS

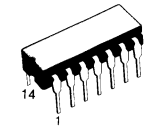
M54HC4002
M74HC4002

DUAL 4-INPUT NOR GATE

- HIGH SPEED
  t_{PD} = 11 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 4002B



B1
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

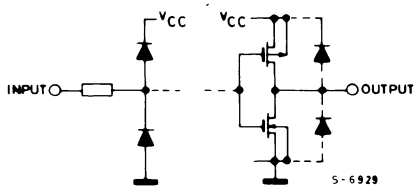
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC4002 F1
M74HC4002 B1N
M74HC4002 F1
M74HC4002 C1
M74HC4002 M1

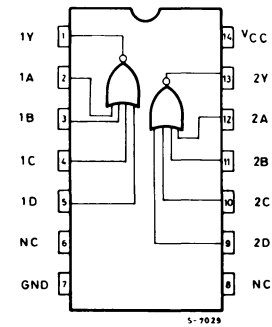
DESCRIPTION

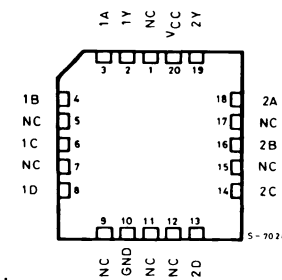
The M54/74HC4002 is a high speed CMOS DUAL 4-INPUT NOR GATE fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The internal circuit is composed of 3 stages including buffer output, which ensures high noise immunity and stable output.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



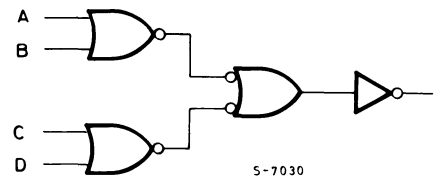
PIN CONNECTIONS (top view)





NC =
No Internal
Connection

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series Operating Temperature 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

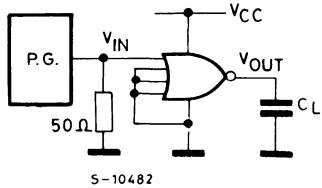
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH}	Propagation Delay Time		11	18	ns

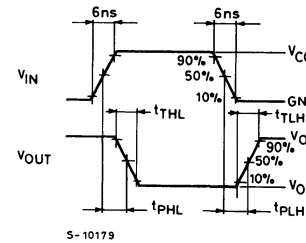
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	52	105	—	130	—	160	ns
		4.5		—	13	21	—	26	—	32	
		6.0		—	11	18	—	22	—	27	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	26	—	—	—	—	—	pF

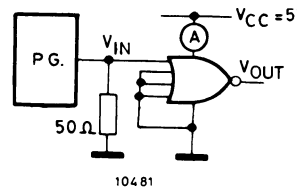
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following equation.
$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate).

SWITCHING CHARACTERISTICS TEST CIRCUIT





TEST CIRCUIT I_{CC} (Opr.)



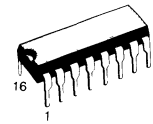
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

SGS-THOMSON MICROELECTRONICS

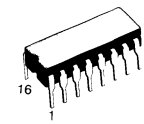
M54HC4017
M74HC4017

DECADE COUNTER/DIVIDER

- HIGH SPEED
  t_{PD} = 21 ns (TYP) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 4017 B



B1N
Plastic Package



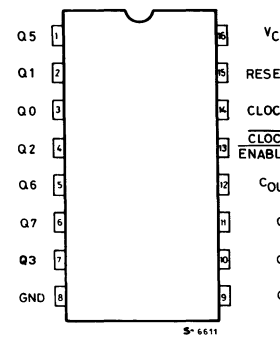
F1
Ceramic Frit Seal Package

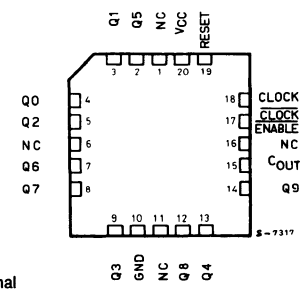
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC4017 F1
M74HC4017 B1N
M74HC4017 F1
M74HC4017 C1
M74HC4017 M1

PIN CONNECTION (top view)





NC = No Internal Connection

DESCRIPTION

The M54/74HC4017 is a high speed CMOS DECADE COUNTER/DIVIDER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

The M54/74HC4017 is a 5-stage Johnson counter with 10 decoded outputs. Each of the decoded outputs is normally low and sequentially goes high on the low to high transition of the clock input. Each output stays high for one clock period of the 10 clock period cycle. The CARRY output goes low to high after OUTPUT 10 goes low, and can be used in conjunction with the CLOCK ENABLE to cascade several stages.

The CLOCK ENABLE input disables counting when in the high state. A RESET input is also provided which when taken high sets all the decoded outputs low.

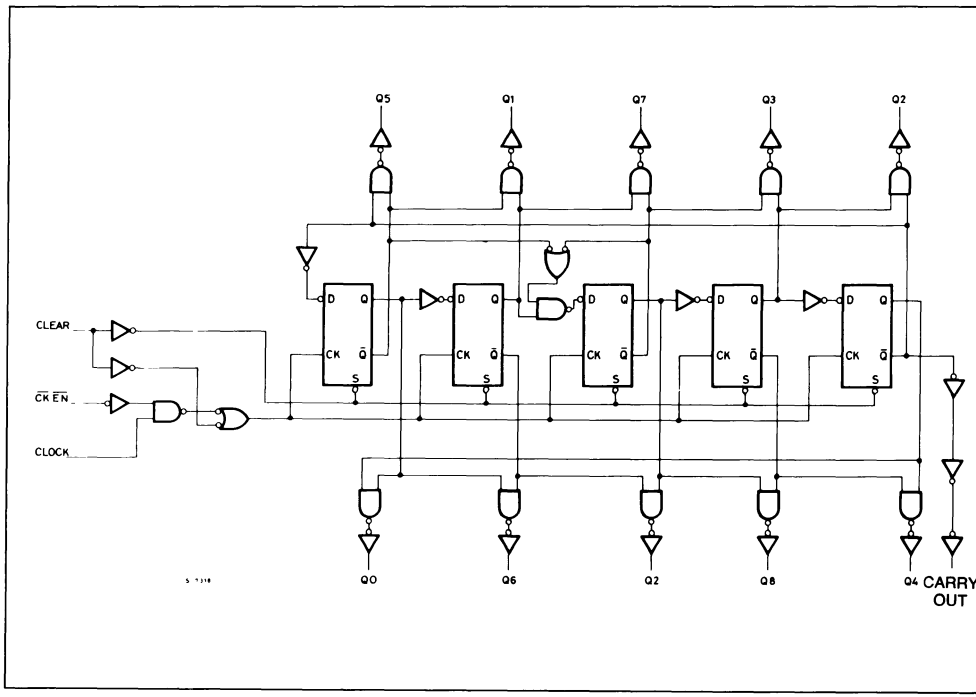
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

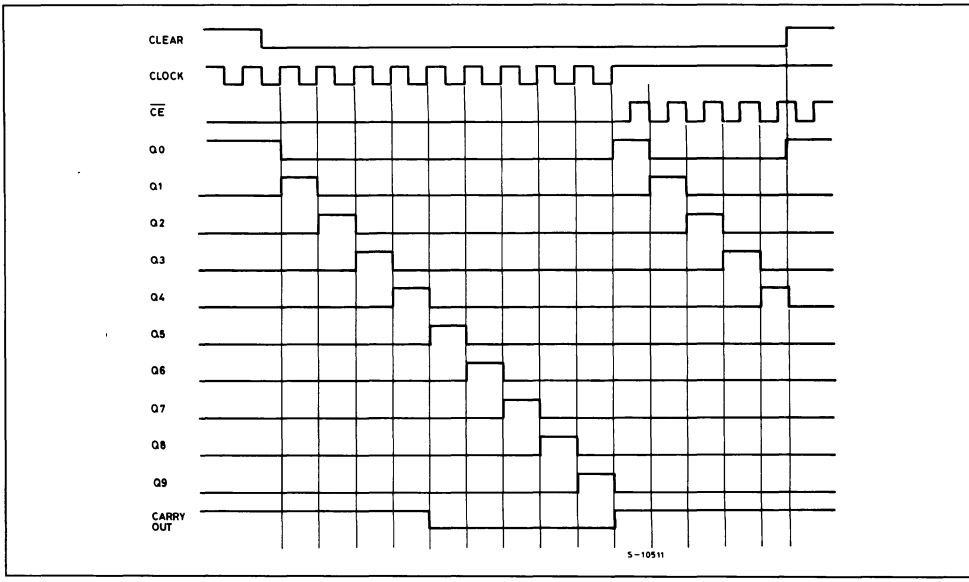
CLOCK	$\overline{\text{CLOCK ENABLE}}$	CLEAR	DECODE OUTPUT (H)
X	X	H	Q0
L	X	L	Qn
X	H	L	Qn
↑	L	L	Qn + 1
↓	L	L	Qn
H	↑	L	Qn
H	↓	L	Qn + 1

X: DON'T CARE Qn: NO CHANGE

LOGIC DIAGRAM



TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series Operating Temperature 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0.0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND $I_O = 0$		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK-QN, CARRY OUT)		21	33	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR-Q - CARRY OUT)		21	33	ns
f_{MAX}	Maximum Clock Frequency	28	45		MHz

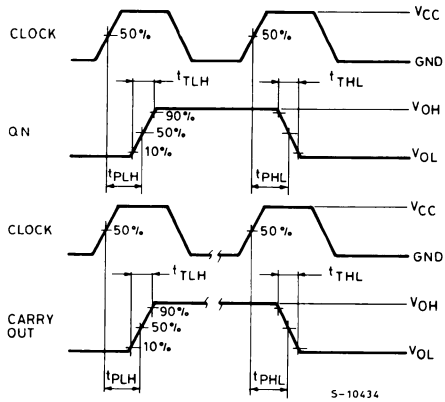
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

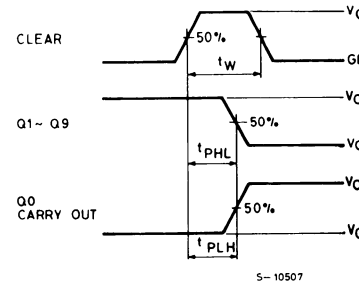
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK,$\overline{CE}$ Q, CARRY)	2.0		—	100	195	—	245	—	295	ns
		4.5		—	25	39	—	49	—	59	
		6.0		—	21	33	—	42	—	50	
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR-Q CARRY OUT)	2.0		—	100	195	—	245	—	295	ns
		4.5		—	25	39	—	49	—	59	
		6.0		—	21	33	—	42	—	50	
f_{MAX}	Maximum Clock Frequency	2.0		5	10	—	4	—	3.4	—	MHz
		4.5		25	41	—	20	—	17	—	
		6.0		29	48	—	24	—	20	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-up Time	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_h	Minimum Hold Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	7	15	—	19	—	22	
		6.0		—	6	13	—	16	—	19	
t_{REM}	Minimum Removal Time (CLEAR)	2.0		—	25	75	—	95	—	110	ns
		4.5		—	6	15	—	19	—	22	
		6.0		—	5	13	—	16	—	19	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	74	—	—	—	—	—	pF

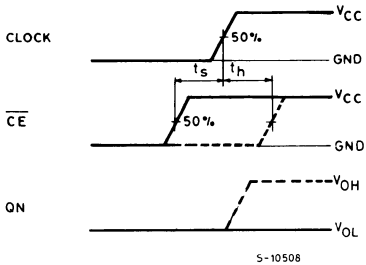
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

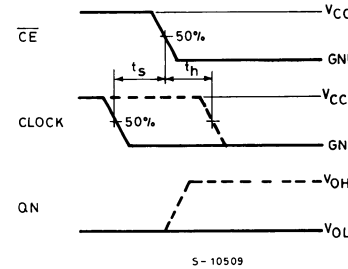
Average operating current can be obtained by the following equation:
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

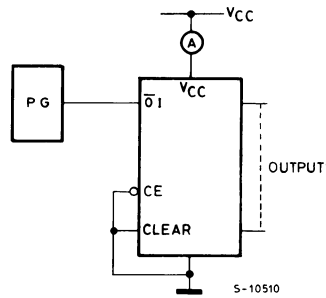








TEST CIRCUIT I_{CC} (Opr.)



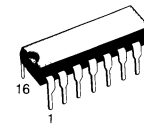
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

SGS-THOMSON MICROELECTRONICS

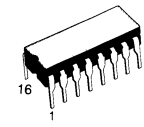
M54HC4020
M74HC4020

14-STAGE BINARY COUNTER

- HIGH SPEED
  f_{MAX} = 60 MHz (TYP) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 4020B



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
SO Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC4020 F1
M74HC4020 B1N
M74HC4020 F1
M74HC4020 C1
M74HC4020 M1

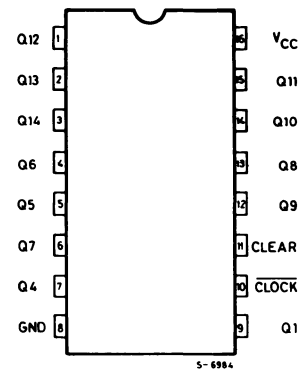
DESCRIPTION

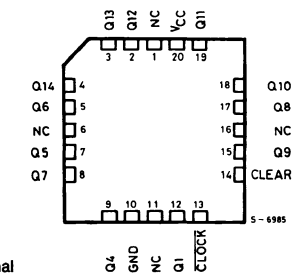
The M54/74HC4020 is a high speed CMOS 14-STAGE BINARY COUNTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low consumption.
A clear input is used to reset the counter to the all low level state. A high level on CLEAR accomplishes the reset function. A negative transition on the CLOCK input increments the counter by one. Twelve kinds of divided output are provided; 1st and 4th stage to 14thstage. The Maximum division available at last stage is 1/16384 x f_{IN} at clock. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

$\overline{CLOCK}$	CLEAR	OUTPUT STATE
X	H	ALL OUTPUTS = "L"
↓	L	NO CHANGE
↑	L	ADVANCE TO NEXT STATE

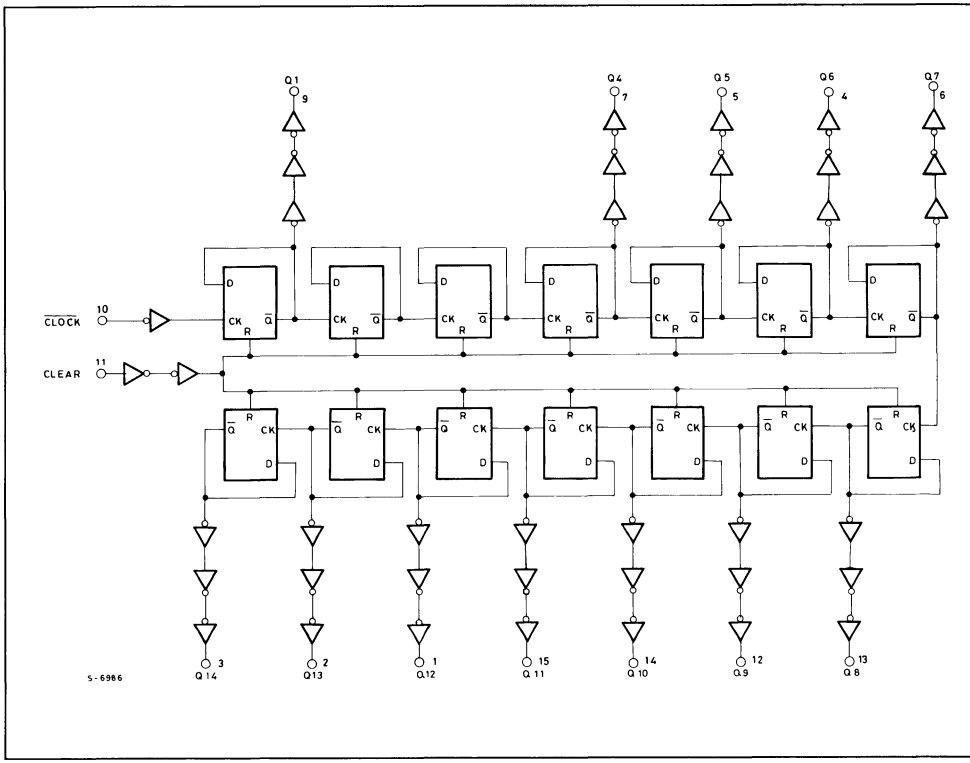
PIN CONNECTION (top view)





NC = No Internal Connection

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

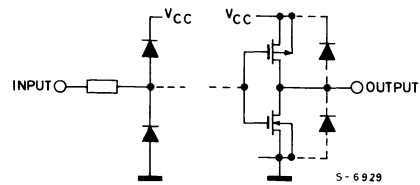
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time		V_{CC} = 2 V	0 to 1000	ns
			V_{CC} = 4.5V	0 to 500	
			V_{CC} = 6 V	0 to 400	

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0	or		5.9	6.0	—	5.9	—	5.9	—	
		4.5	V_{IL}	−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0.0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH}	20 μA	—	0.0	0.1	—	0.1	—	0.1	
		6.0	or		—	0.0	0.1	—	0.1	—	0.1	
		4.5	V_{IL}	4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

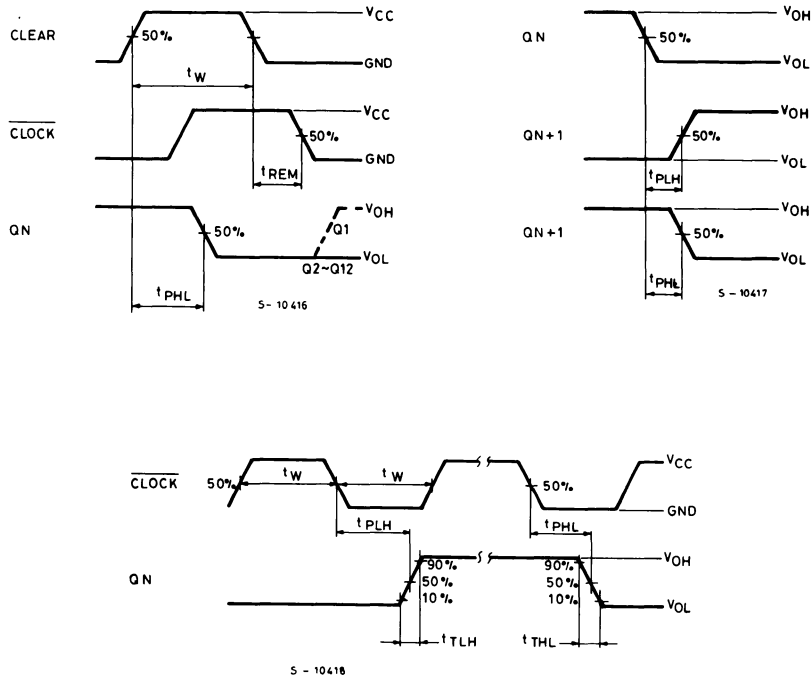
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOCK}$ - Q1)		15	24	ns
t_{PHL} t_{PHL}	Propagation Delay Time (Qn - Qn+1)		7	12	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR)		22	35	ns
f_{MAX}	Maximum Clock Frequency	33	60		MHz

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

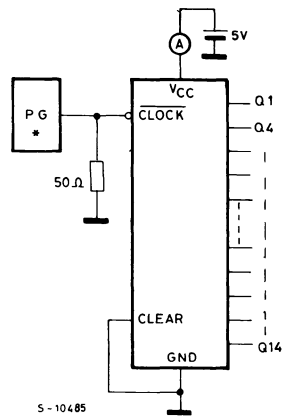
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q1)	2.0 4.5 6.0		— — —	72 18 15	145 29 25	— — —	180 36 31		220 44 38	ns
t_{PLH} t_{PHL}	Propagation Delay Time (Q_n-Q_{n+1})	2.0 4.5 6.0		— — —	35 9 8	75 15 13	— — —	95 19 16		110 22 19	ns
t_{PHL}	Propagation Delay Time (CLEAR)	2.0 4.5 6.0		— — —	104 26 22	205 41 35	— — —	255 51 43		310 62 53	ns
f_{MAX}	Maximum Clock Frequency	2.0 4.5 6.0		6 30 35	14 55 65	— — —	4.8 24 28	— — —	4.0 20 24	— —	MHz
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width ($\overline{CLOCK}$)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0 4.5 6.0		— — —	60 15 13	125 25 21	— — —	155 31 26		190 38 32	ns
t_{REM}	Minimum Removal Time	2.0 4.5 6.0		— — —	— — —	50 10 9	— — —	65 13 11	— — —	75 15 13	ns
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	25	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current is: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr)



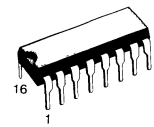
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERIRISTCS TEST

SGS-THOMSON MICROELECTRONICS

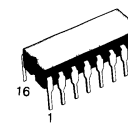
M54HC4022
M74HC4022

OCTAL COUNTER/DIVIDER

- HIGH SPEED
  f_{MAX} = 44 MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN).
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 4022B



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC4022 F1
M74HC4022 B1N
M74HC4022 F1
M74HC4022 C1
M74HC4022 M1

DESCRIPTION

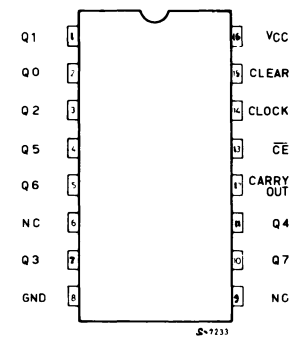
The M54/74HC4022 is a high speed CMOS OCTAL COUNTER/DIVIDER fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. It contains a 4-stage divide-by-8 Johnson counter with 8 decoded outputs (Q0-Q7) and a Carry-out bit. This counter is advanced on the positive edge of the clock signal when CLOCK ENABLE input is held low, or is advanced on the negative edge of clock enable signal when CLOCK input is held high, and the selected one of eight outputs goes high. Holding the CLEAR input high clears the counter to zero regardless of the other input conditions. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

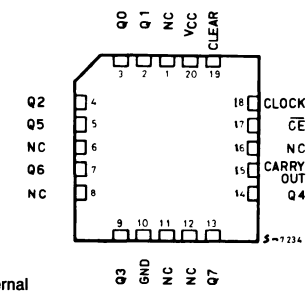
TRUTH TABLE

(X = DON'T CARE)

CLOCK	$\overline{CE}$	CLEAR	DECODER OUTPUT(H)
X	X	H	Q0
L	X	L	NO CHANGE
X	H	L	NO CHANGE
↑	L	L	NO CHANGE + 1
↓	L	L	NO CHANGE
H	↑	L	NO CHANGE
H	↓	L	NO CHANGE + 1

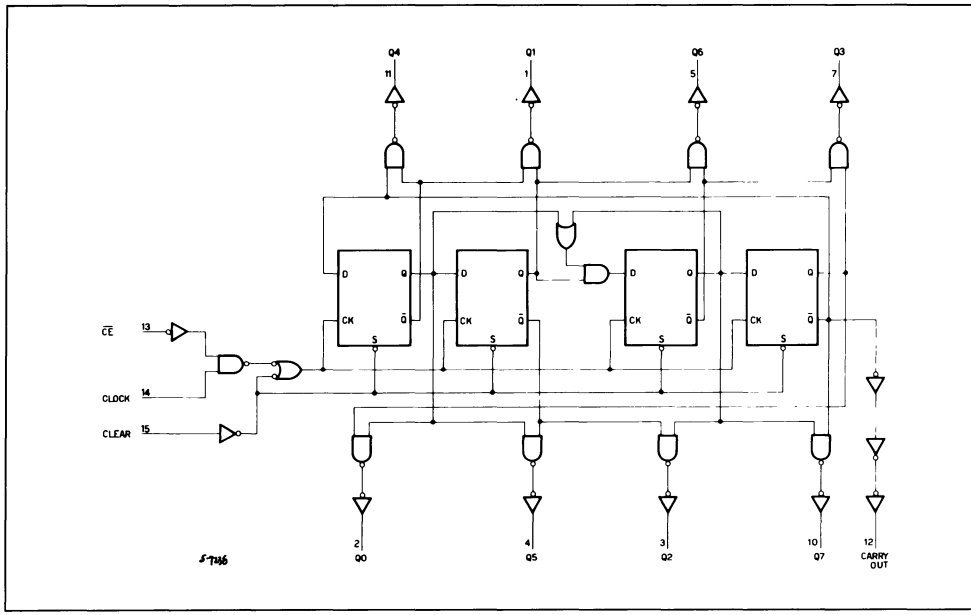
PIN CONNECTIONS (top view)



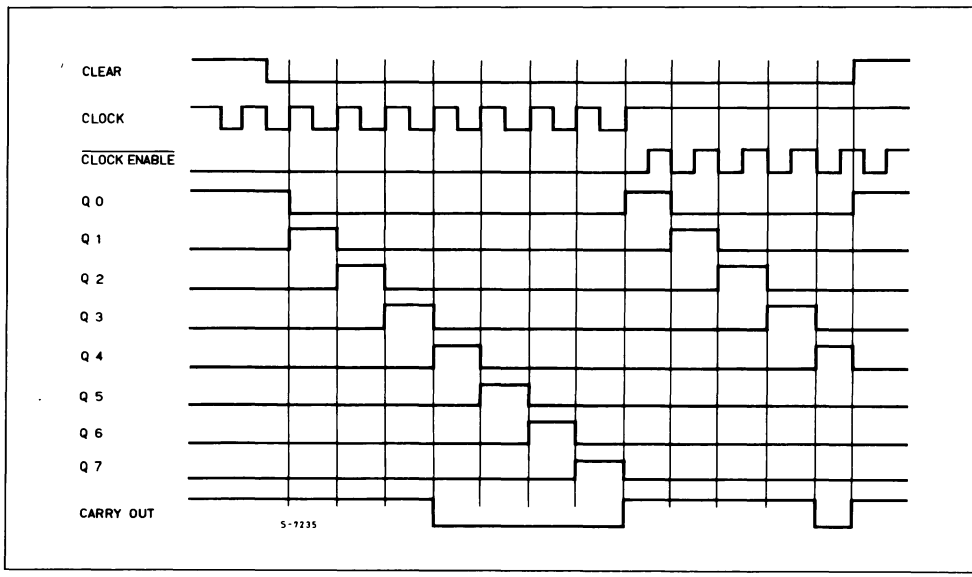


NC = No Internal Connection

LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

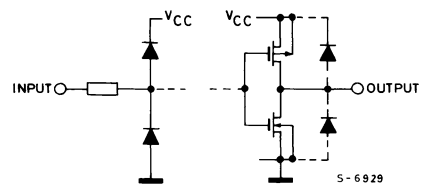
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

INPUT AND OUTUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Q, CARRY)		21	33	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR-Q, CARRY)		21	33	ns
f_{MAX}	Maximum Clock Frequency	28	44		ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

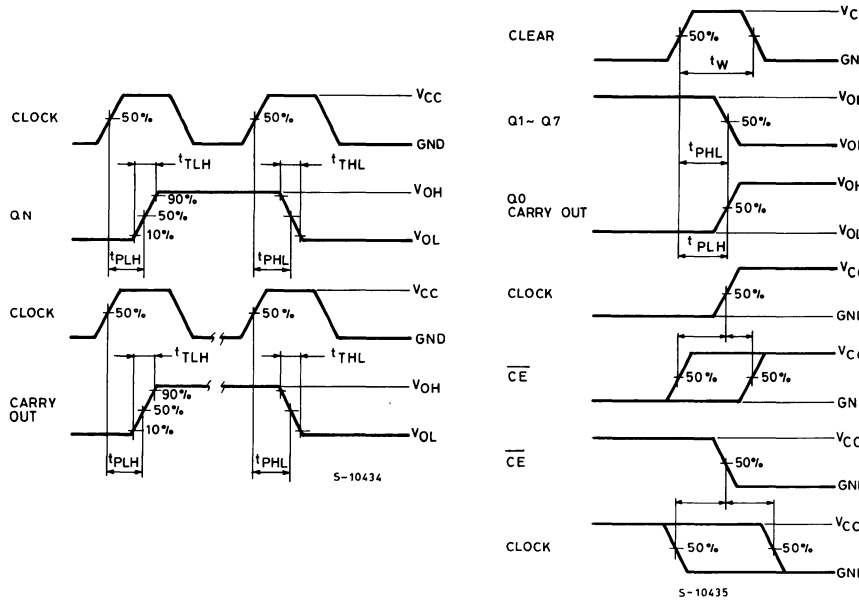
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Q, CARRY)	2.0		—	100	195	—	245	—	295	ns
		4.5		—	25	39	—	49	—	59	
		6.0		—	21	33	—	42	—	50	
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR-Q, CARRY)	2.0		—	100	195	—	245	—	295	ns
		4.5		—	25	39	—	49	—	59	
		6.0		—	21	33	—	42	—	50	
f_{MAX}	Maximum Clock Frequency	2.0		5	10	—	4.0	—	3.4	—	MHz
		4.5		25	40	—	20	—	17	—	
		6.0		29	47	—	24	—	20	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0		—	35	75	—	95	—	110	ns
		4.5		—	9	15	—	19	—	22	
		6.0		—	8	13	—	16	—	19	
t_s	Minimum Set-up Time	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_h	Minimum Hold Time	2.0		—	35	75	—	95	—	110	ns
		4.5		—	9	15	—	19	—	22	
		6.0		—	8	13	—	16	—	19	
t_{REM}	Minimum Removal Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	52	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

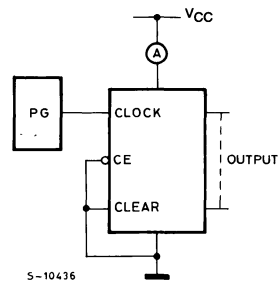
Average operating current can be obtained by the following equation

$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



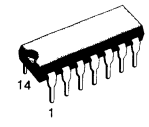
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

SGS-THOMSON MICROELECTRONICS

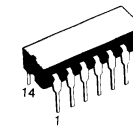
M54HC4024
M74HC4024

7-STAGE BINARY COUNTER

- HIGH SPEED
  t_{PD} = 15 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN).
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 4024B



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC4024 F1
M74HC4024 B1N
M74HC4024 F1
M74HC4024 C1
M74HC4024 M1

DESCRIPTION

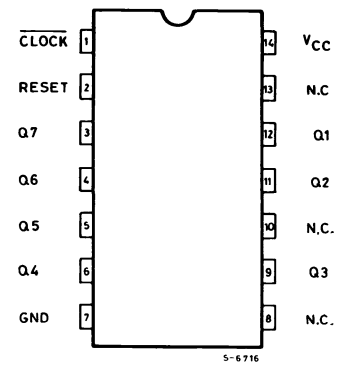
The M54/74HC4024 is a high speed CMOS 7-STAGE BINARY COUNTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.The HC4024 is a 7 stage Counter. This devices is incremented on the falling edge (negative transition) of the input clock, and all its outputs are reset to a low level by applying a logical high on their reset input. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

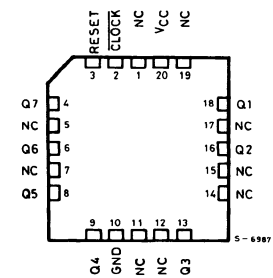
TRUTH TABLE

$\overline{CLOCK}$	CLEAR	OUTPUT STATE
X	H	ALL OUTPUTS = "L"
⊓↓	L	NO CHANGE
⊓↓	L	ADVANCE TO NEXT STATE

X: DON'T CARE

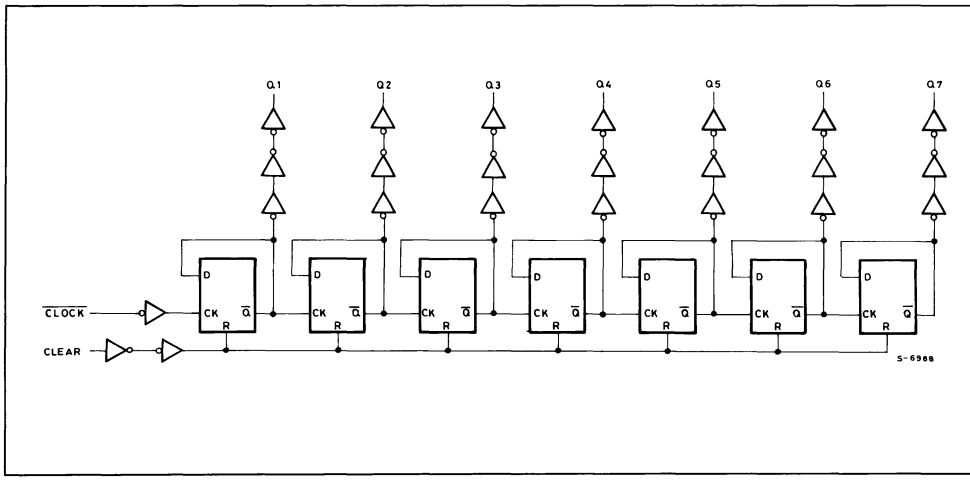
PIN CONNECTIONS (top view)





NC = No Internal Connection

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

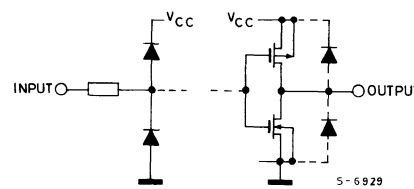
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (QN - QN + 1)		5	9	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK - Q1)		15	24	ns
t_{PHL}	Propagation Delay Time (CL-Q)		20	31	ns
f_{MAX}	Maximum Clock Frequency	33	60		MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

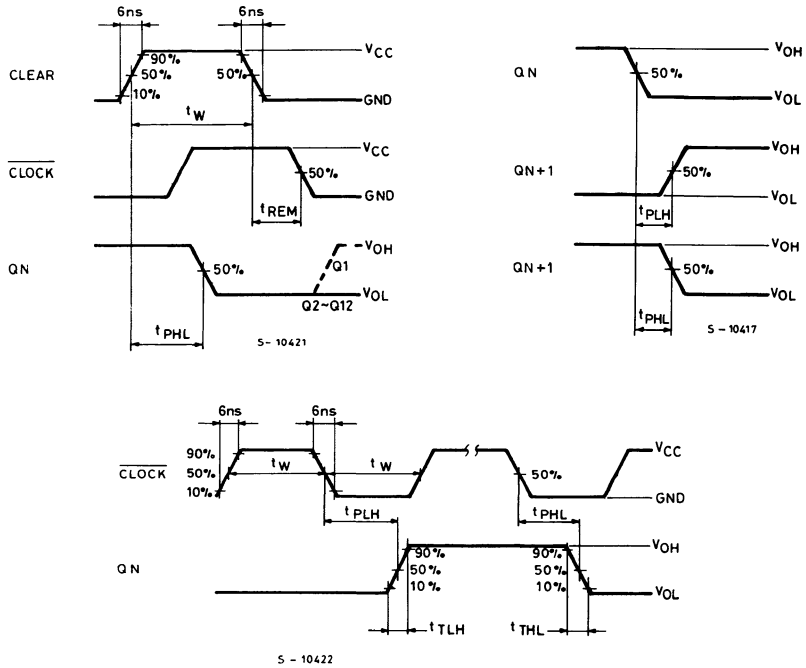
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (Qn - Qn+1)	2.0		—	28	60	—	75	—	90	ns
		4.5		—	7	12	—	15	—	18	
		6.0		—	6	10	—	13	—	15	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOCK}$-Q1)	2.0		—	72	145	—	180	—	220	ns
		4.5		—	18	29	—	36	—	44	
		6.0		—	15	25	—	31	—	38	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$ - Qn)	2.0		—	96	185	—	230	—	280	ns
		4.5		—	24	37	—	46	—	56	
		6.0		—	20	31	—	39	—	48	
f_{MAX}	Maximum Clock Frequency	2.0		6	14	—	4.8	—	4.0	—	MHz
		4.5		30	55	—	24	—	20	—	
		6.0		35	65	—	28	—	24	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{REM}	Minimum Removal Time (CL)	2.0		—	15	50	—	65	—	75	ns
		4.5		—	3	10	—	13	—	15	
		6.0		—	3	9	—	11	—	13	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	42	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following equation: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

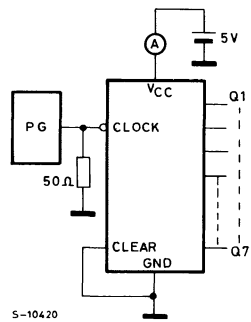
INPUT AND OUTPUT EQUIVALENT CIRCUIT



SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)

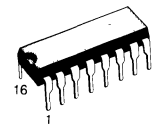


INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

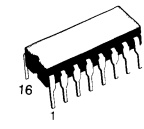
M54HC4028
M74HC4028

BCD-TO-DECIMAL DECODER

- HIGH SPEED
  t_{PD} = 25 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 4028B



B1N
Plastic Package



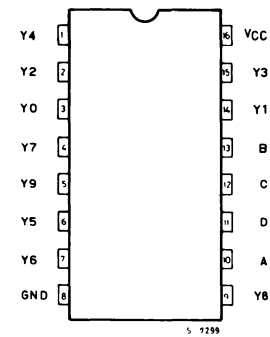
F1
Ceramic Frit Seal Package

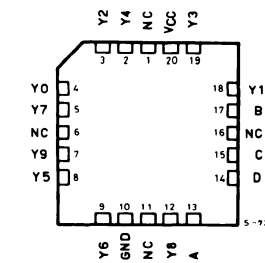
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC4028 F1
M74HC4028 B1N
M74HC4028 F1
M74HC4028 C1
M74HC4028 M1

PIN CONNECTIONS (top view)





NC = No Internal Connection

DESCRIPTION

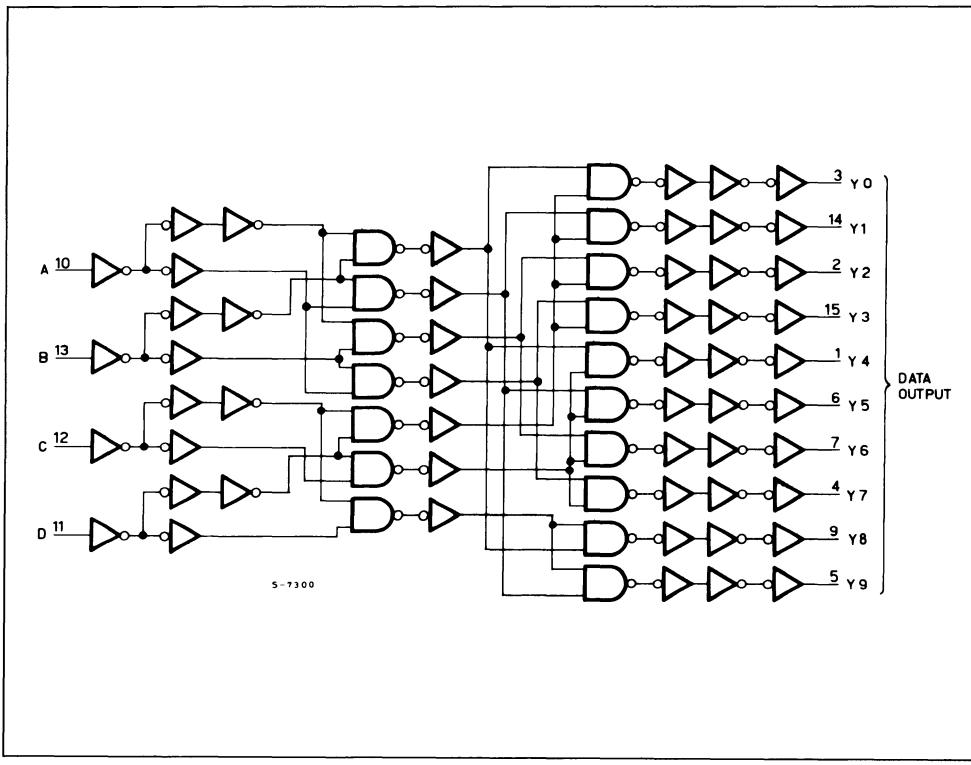
The M54/74HC4028 is a high speed CMOS BCD-TO-DECIMAL DECODER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. A BCD code applied to the four inputs (A to D) provides a high level at the selected one of the decimal decoded outputs. An illegal BCD code such as eleven to fifteen gives a low level at all outputs. The device also can be used as 3-TO-8-LINE DECODER, when D input is assigned as a disable input. The device is useful for code conversion, address decoding, memory selection, demultiplexing, or read out decoding.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUTS				OUTPUTS										SELECTED OUTPUT
D	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	
L	L	L	L	H	L	L	L	L	L	L	L	L	L	Y0
L	L	L	H	L	H	L	L	L	L	L	L	L	L	Y1
L	L	H	L	L	L	H	L	L	L	L	L	L	L	Y3
L	L	H	H	L	L	L	H	L	L	L	L	L	L	Y3
L	H	L	L	L	L	L	L	H	L	L	L	L	L	Y4
L	H	L	H	L	L	L	L	L	H	L	L	L	L	Y5
L	H	H	L	L	L	L	L	L	L	H	L	L	L	Y6
L	H	H	H	L	L	L	L	L	L	L	H	L	L	Y7
H	L	L	L	L	L	L	L	L	L	L	L	H	L	Y8
H	L	L	H	L	L	L	L	L	L	L	L	L	H	Y9
H	X	H	X	L	L	L	L	L	L	L	L	L	L	NOTE
H	H	X	X	L	L	L	L	L	L	L	L	L	L	NOTE

X: DON'T CARE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} +0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} +0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

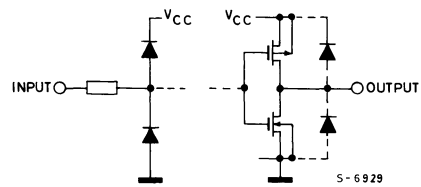
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series Operating Temperature 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0.0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A,B,C-D)		25	39	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

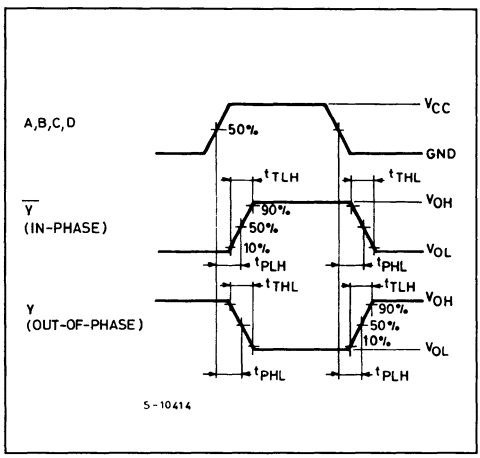
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C, D)	2.0		—	116	225	—	280	—	340	ns
		4.5		—	29	45	—	56	—	68	
		6.0		—	25	38	—	48	—	58	
C_{IN}	Input Capacitance			—	5	10	—	10	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance			—	58	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

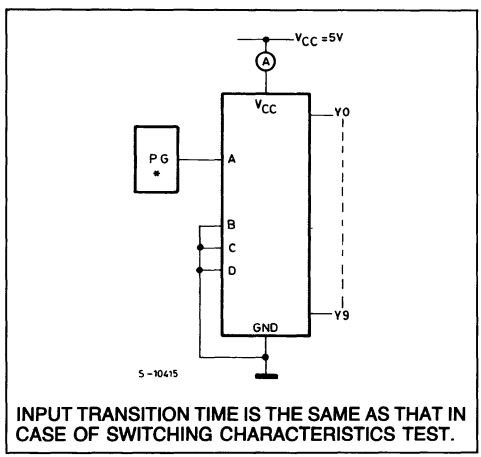
Average operating current can be obtained by the following equation:

$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



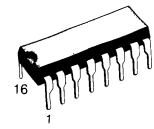
TEST CIRCUIT I_{CC} (Opr.)



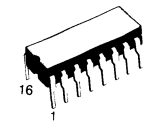
INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

12-STAGE BINARY COUNTER

- HIGH SPEED
  f_{MAX} = 60 MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 4040B



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC4040 F1
M74HC4040 B1N
M74HC4040 F1
M74HC4040 C1
M74HC4040 M1

DESCRIPTION

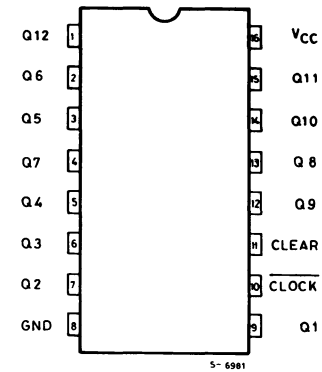
The M54/74HC4040 is a high speed CMOS 12-STAGE BINARY COUNTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low consumption.
A clear input is used to reset the counter to the all low level state. A high level on CLEAR accomplishes the reset function. A negative transition on the CLOCK input increments the counter by one. Each division stage has an output; the final frequency is fx 1/4096.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

$\overline{CLOCK}$	CLEAR	OUTPUT STATE
X	H	ALL OUTPUTS = "L"
↓	L	NO CHANGE
↑	L	ADVANCE TO NEXT STATE

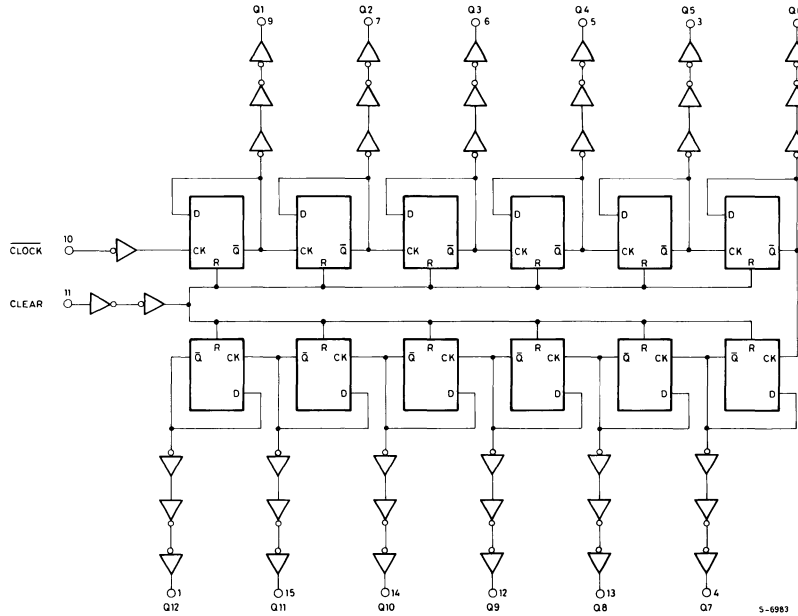
X: DON'T CARE

PIN CONNECTIONS (top view)



NC = No Internal Connection

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limit	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V: 0 to 1000 V_{CC} = 4.5V: 0 to 500 V_{CC} = 6 V: 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q1)		15	24	ns
t_{PLH} t_{PHL}	Propagation Delay Time (Qn - Qn + 1)		7	12	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR)		22	35	ns
f_{MAX}	Maximum Clock Frequency	33	60		MHz

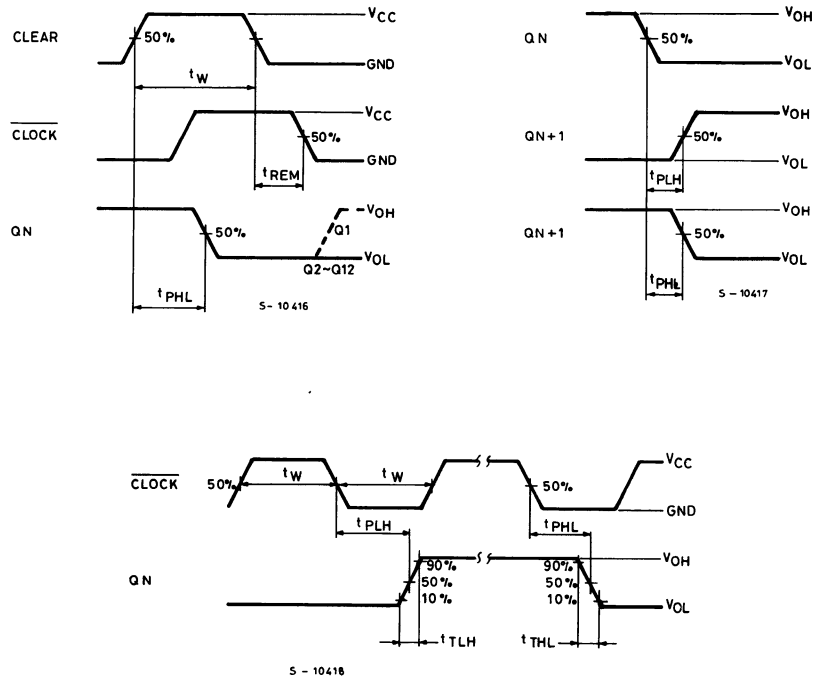
AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q1)	2.0 4.5 6.0		— — —	72 18 15	145 29 25	— — —	180 36 31	— — —	220 44 38	ns
t_{PLH} t_{PHL}	Propagation Delay Time (Qn - Qn + 1)	2.0 4.5 6.0		— — —	35 9 8	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{PHL}	Propagation Delay Time (CLEAR)	2.0 4.5 6.0		— — —	104 26 22	205 41 35	— — —	255 51 43	— — —	310 62 53	ns
f_{MAX}	Maximum Clock Frequency	2.0 4.5 6.0		6 30 35	14 55 65	— — —	4.8 24 28	— — —	4.0 20 24	— — —	MHz
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CLOCK)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0 4.5 6.0		— — —	60 15 13	125 25 21	— — —	155 31 26	— — —	190 38 32	ns
t_{REM}	Minimum Removal Time	2.0 4.5 6.0		— — —	— — —	50 10 9	— — —	65 13 11	— — —	75 15 13	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	32	—	—	—	—	—	pF

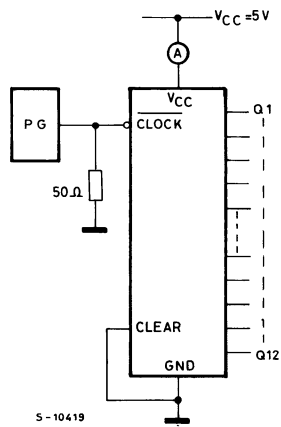
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



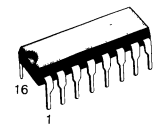
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

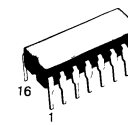
M54/74HC4049B
M54/74HC4050B

HC4049B HEX BUFFER/CONVERTER (INVERTER)
HC4050B HEX BUFFER/CONVERTER

- HIGH SPEED
  t_{PD} = 10 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 4049B/4050B



B1N
Plastic Package



F1
Ceramic Package

M1
Micro Package

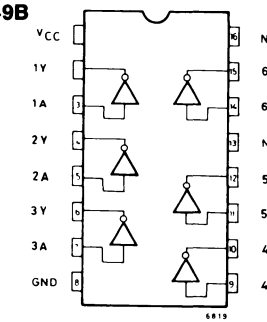
C1
Chip Carrier

ORDERING NUMBERS:

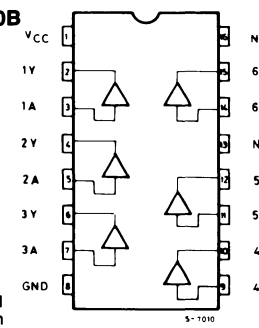
M54HCXXXXB F1
M74HCXXXXB B1N
M74HCXXXXB F1
M74HCXXXXB C1
M74HCXXXXB M1

PIN CONNECTIONS (top view)

HC4049B



HC4050B

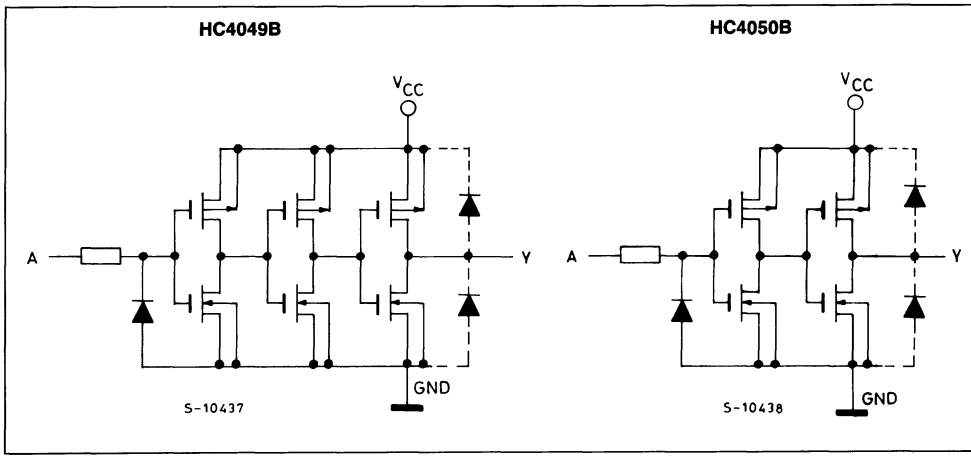


NC = No Internal Connection

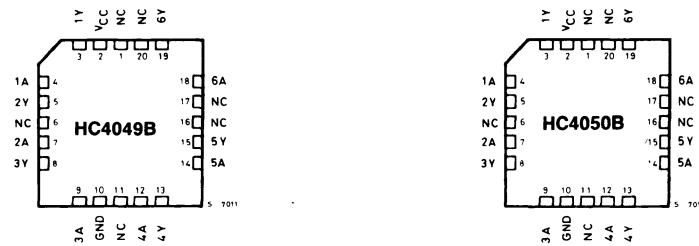
DESCRIPTION

The M54/74HC4049B and the M54/74HC4050B are high speed CMOS HEX BUFFER fabricated in silicon gate C²MOS technology.
They have the same high speed performance of LSTTL combined with true CMOS low power consumption.
The M54/75HC4049B is an inverting buffer, while the M54/74HC4050B is a non-inverting buffer.
The internal circuit is composed of 3 stage or 2-stage inverters, which provides high noise immunity and a stable output.
Input protection circuits are different from those of the high speed CMOS IC's.
The V_{CC} side diodes are designed to allow logic-level convertion from high-level voltages (up to 15V) to low-level voltages.

CIRCUIT SCHEMATIC (Per Gate)



CHIP CARRIER



NC = No Internal Connection

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to 16	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to 15	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V: 0 to 1000 V_{CC} = 4.5V: 0 to 500 V_{CC} = 6 V: 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
		6.0	V_I = 15V		—	—	±0.5	—	±5	—	±5	
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input t_r = t_f = 6ns)

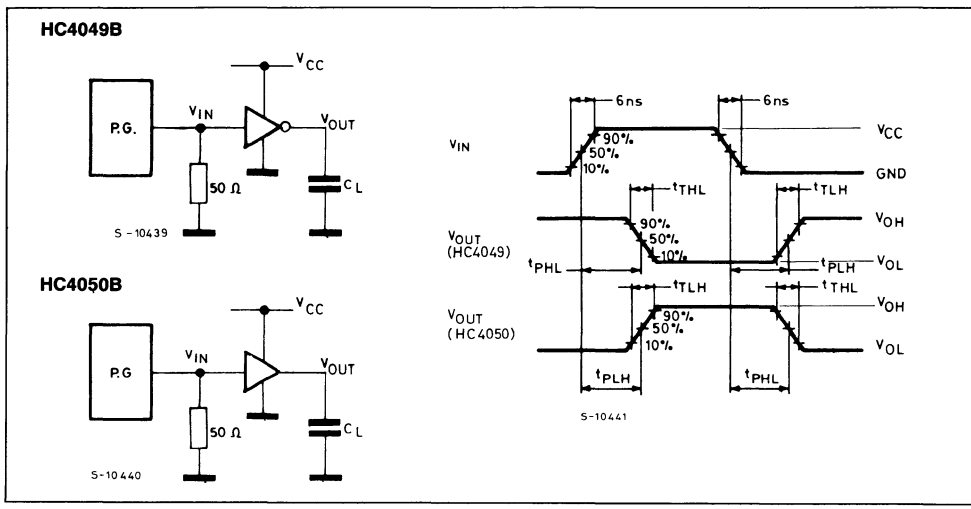
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		7	11	ns
t_{PLH} t_{PHL}	Propagation Delay Time		11	16	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

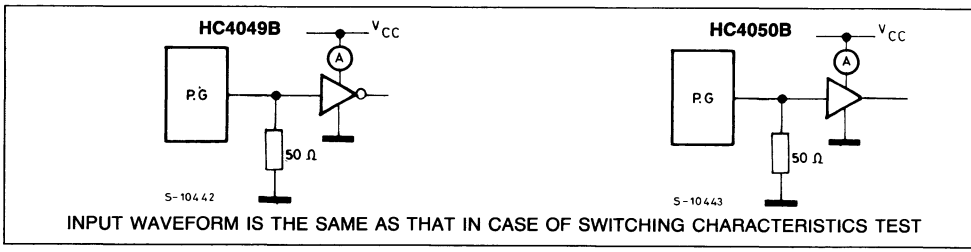
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	24	60	—	75	—	90	ns
		4.5		—	6	12	—	15	—	18	
		6.0		—	5	10	—	13	—	15	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	44	85	—	105	—	130	ns
		4.5		—	11	17	—	21	—	26	
		6.0		—	9	14	—	19	—	22	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	25	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following equation.
$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate).

SWITCHING CHARACTERISTICS TEST CIRCUIT



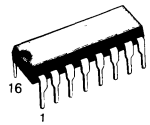
TEST CIRCUIT I_{CC} (Opr.)



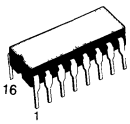
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

14-STAGE BINARY COUNTER/OSCILLATOR

- HIGH SPEED
  f_{MAX} = 60 MHz (TYP) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 4060B



B1N
Plastic Package



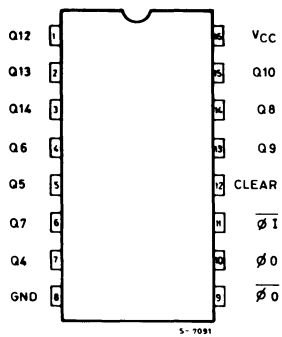
F1
Ceramic Frit Seal Package

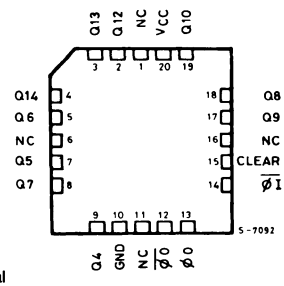
M1
SO Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC4060 F1
M74HC4060 B1N
M74HC4060 F1
M74HC4060 C1
M74HC4060 M1

PIN CONNECTION (top view)





NC = No Internal Connection

DESCRIPTION

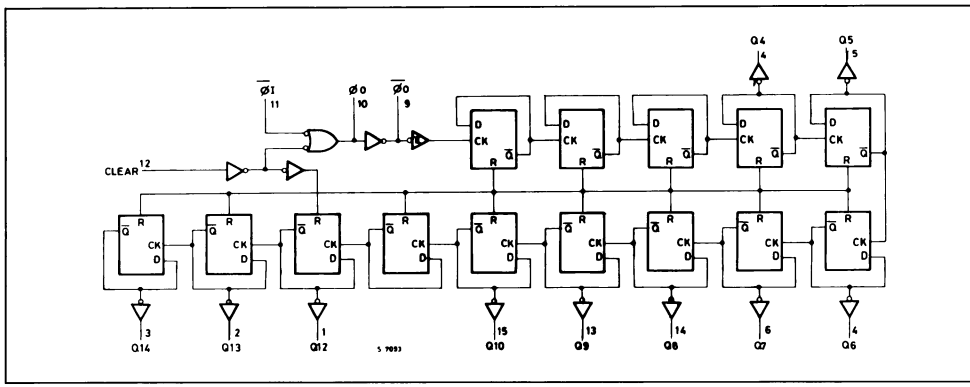
The M54/74HC4060 is a high speed CMOS 14-STAGE BINARY COUNTER/OSCILLATOR fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. It operates ten times faster than metal-gate C²MOS IC (4060B) with the same power dissipation.
The oscillator configuration allows design of either RC or crystal oscillator circuits. A high level on the CLEAR accomplishes the reset function, i.e. all counter outputs are made low and the oscillator is disabled.
A negative transition on the clock input increments the counter. Ten kinds of divided output are provided; 4 to 10 and 12 to 14 stage inclusive. The maximum division available at Q12 is 1/16384 f oscillator.
The $\overline{\emptyset_1}$ input and the CLEAR input are equipped with protection circuits against static dischage and transient excess voltage.

TRUTH TABLE

INPUTS		FUNCTION
$\overline{\emptyset_I}$	CLEAR	
X	H	COUNTER IS RESET TO ZERO STATE $\emptyset_O$ OUTPUT GOES TO HIGH LEVEL $\overline{\emptyset_O}$ OUTPUT GOES TO LOW LEVEL
↓	L	COUNT UP ONE STEP.
↑	L	NO CHANGE.

X: DON'T CARE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400	ns

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage (Q Outputs)	2.0 4.5 6.0 4.5 6.0	V_I V_{IH} or V_{IL}	I_O −20 μA −4.0 mA −5.2 mA	1.9 4.4 5.9 4.18 5.68	2.0 4.5 6.0 4.31 5.8	— — — — —	1.9 4.4 5.9 4.13 5.63	— — — — —	1.9 4.4 5.9 4.10 5.60	— — — — —	V
V_{OL}	Low Level Output Voltage (Q Outputs)	2.0 4.5 6.0 4.5 6.0	V_{IH} or V_{IL}	20 μA 4.0 mA 5.2 mA	— — — — —	0.0 0.0 0.0 0.17 0.18	0.1 0.1 0.1 0.26 0.26	— — — — —	0.1 0.1 0.1 0.33 0.33	— — — — —	0.1 0.1 0.1 0.40 0.40	V
V_{OH}	High Level Output Voltage $\emptyset_0$, $\overline{\emptyset_0}$ Output	2.0 4.5 6.0	V_I V_{IH} or V_{IL}	I_O −20 μA	1.8 4.0 5.5	2.0 4.5 5.9	— — —	1.8 4.0 5.5	— — —	1.8 4.0 5.5	— — —	V
V_{OL}	Low Level Output Voltage $\emptyset_0$, $\overline{\emptyset_0}$ Output	2.0 4.5 6.0	V_{IH} or V_{IL}	20 μA	— — —	0.0 0.0 0.1	0.2 0.5 0.5	— — —	0.2 0.5 0.5	— — —	0.2 0.5 0.5	V
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PHL} t_{PHL}	Propagation Delay Time ($\overline{\varnothing}$ - Q_4)		43	65	ns
t_{PLH} t_{PHL}	Propagation Delay Time (Q_n - Q_{n+1})		7	12	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR - Q_n)		21	34	ns
f_{MAX}	Maximum Clock Frequency	33	60		MHz

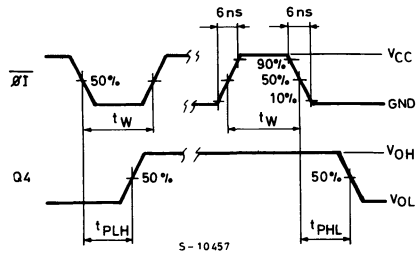
AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time ($\varnothing_I$ - Q_4)	2.0		—	196	370	—	465	—	555	ns
		4.5		—	49	74	—	93	—	111	
		6.0		—	42	63	—	80	—	95	
t_{PLH} t_{PHL}	Propagation Delay Time (Q_n - Q_{n+1})	2.0		—	35	75	—	95	—	110	ns
		4.5		—	9	15	—	19	—	22	
		6.0		—	8	13	—	16	—	19	
t_{PHL}	Propagation Delay Time (CLEAR - Q_n)	2.0		—	100	195	—	245	—	295	ns
		4.5		—	25	39	—	49	—	59	
		6.0		—	21	33	—	42	—	50	
f_{MAX}	Maximum Clock Frequency	2.0		6	13	—	5	—	4	—	MHz
		4.5		30	55	—	24		20	—	
		6.0		35	64	—	28	—	24	—	
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width CLOCK ($\varnothing_I$)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0		—	60	125	—	155	—	190	ns
		4.5		—	15	25	—	31	—	38	
		6.0		—	13	21	—	26	—	32	
t_{REM}	Minimum Removal Time (CLEAR)	2.0		—	40	100	—	125	—	150	ns
		4.5		—	10	20	—	25	—	30	
		6.0		—	9	17	—	21	—	26	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD}(*)	Power Dissipation			—	33	—	—	—	—	—	pF

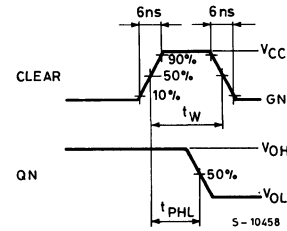
Note (*) C_{PD} is defined as the value of the IC's of internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following equation I_{CC} (Opr.) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

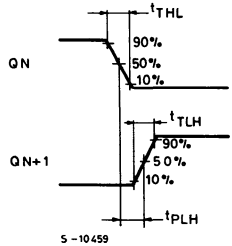
t_{PLH}, t_{PHL} (CLOCK-Q) t_W (CLOCK)

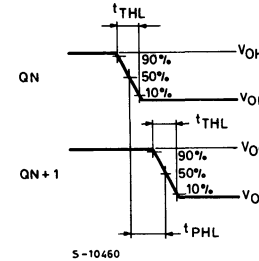


t_{PHL} (CLEAR - Qn), t_W (CLEAR)

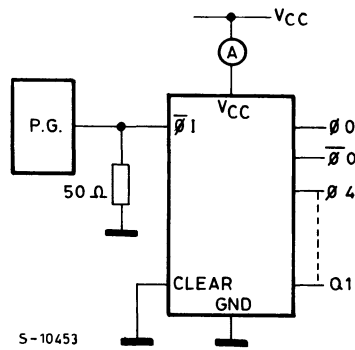


t_{PLH}, t_{PHL} (Qn - Qn+1)





TEST CIRCUIT I_{CC} (Opr.)

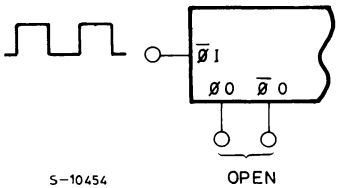


* $\emptyset_I$ INPUT $t_r = t_f = 6$ ns
DUTY = 50%

NOTE: WHEN CR OR CRYSTAL OSCILLATION CIRCUIT IS ADOPTED, THE DYNAMIC POWER DISSIPATION WILL BE GREATER THAN THE MEASURED VALUE FROM THE TEST CIRCUIT SHOWN LEFT, BECAUSE THESE OSCILLION CIRCUITS SPEND MUCH SUPPLY CURRENT

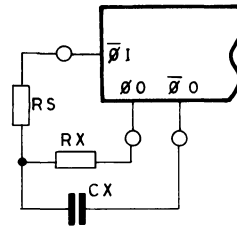
TYPICAL CLOCK DRIVE CIRCUITS

EXTERNAL CLOCK DRIVE



S-10454

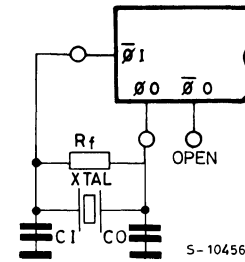
TYPICAL CIRCUIT



R8 : 2RX ~ 10RX

S-10455

TYPICAL CRYSTAL CIRCUIT

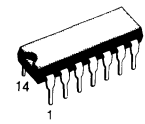


S-10456

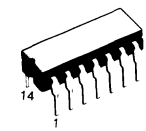
M54HC4066
M74HC4066

QUAD BILATERAL SWITCH

- HIGH SPEED
  t_{PD} = 12 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 4066B



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

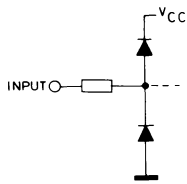
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC4066 F1
M74HC4066 B1N
M74HC4066 F1
M74HC4066 C1
M74HC4066 M1

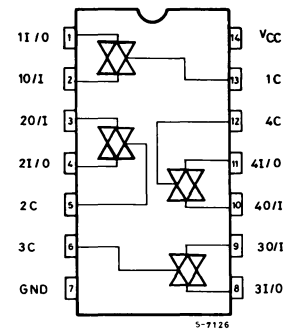
DESCRIPTION

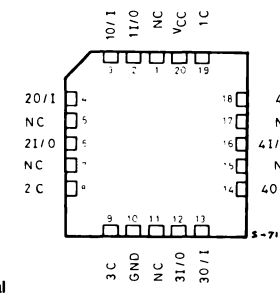
The M54/74HC4066 is a high speed CMOS QUAD BILATERAL SWITCH fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
The C input is provided to control the switch. The switch in on when the C input is held high and off when C is held low.

CONTROL INPUT



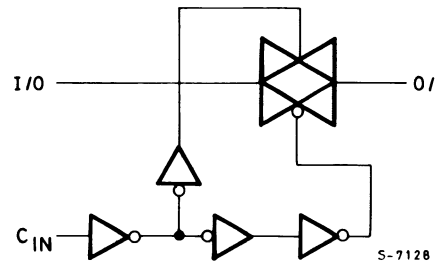
PIN CONNECTIONS (top view)





NC = No Internal Connection

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

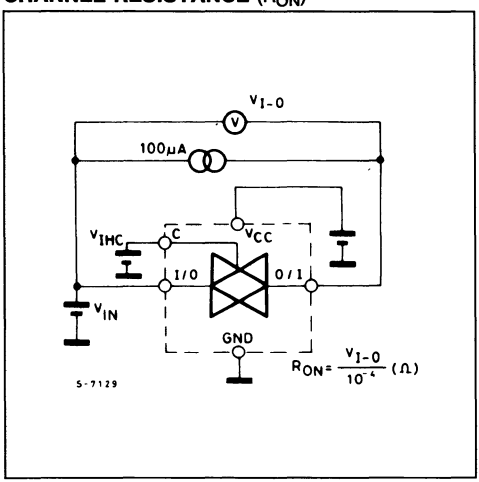
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

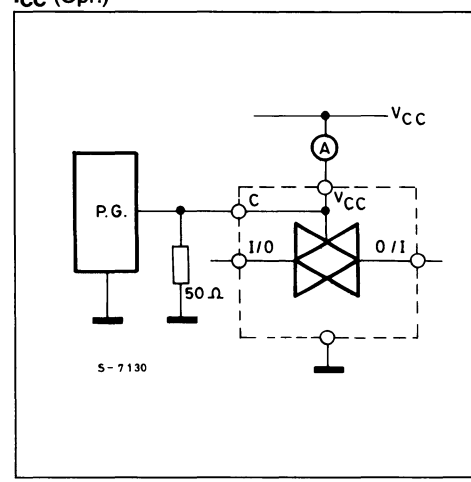
DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Control Input Voltage	2.0 4.5 6.0	Refer to R_{ON} Specification	1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Control Input	2.0 4.5 6.0	$\|I_{OFF}\| \leq 1.0\mu A$	— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
R_{ON}	ON Resistance	2.0 4.5 6.0	$V_{I/O} = 0 \sim V_{CC}$ $I_{I/O} = 100\mu A$	— — —	2000 100 60	— 200 170	— — —	— 250 210	— — —	— 300 250	Ω
ΔR_{ON}	Difference of ON Resistance between Any two of Four Switches	2.0 4.5 6.0	$V_C = V_{IHC}$ $I_{I/O} = 100\mu A$	— — —	50 3 2	— — —	— — —	— — —	— — —	— — —	Ω
I_{OFF}	Input/Output Leakage Current (Switch OFF)	6.0	$V_C = V_{ILC}$ $V_{I/O} = 6V$, $V_{O/I} = 0V$ $V_{I/O} = 0V$, $V_{O/I} = 6V$	—	—	±0.1	—	±0.1	—	±0.1	μA
I_{IN}	Input Leakage Current	6.0		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND	—	—	1	—	10	—	20	μA

CHANNEL RESISTANCE (R_{ON})



I_{CC} (Opr.)



AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

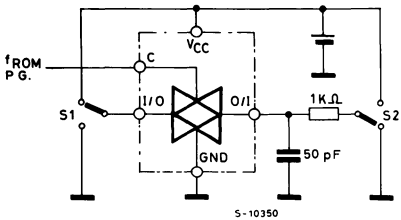
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (Input to output)	2.0 4.5 6.0	$R_L = 10k\Omega$	— — —	13 5 4	50 10 8	— — —	60 12 10	 —	75 15 13	ns
t_{PZH} t_{PZL}	Output Enable Time	2.0 4.5 6.0	$R_L 1k\Omega$	— — —	56 14 12	115 23 20	— — —	140 28 24	— —	173 35 29	ns
t_{PLZ} t_{PHZ}	Output Disable Time	2.0 4.5 6.0	$R_L = 1k\Omega$	— — —	64 16 14	115 23 20	— — —	140 28 24	 —	173 35 29	ns
	Sine Wave Distortion	2.5	$V_{SS} = -2.5V$ $V_{IN} = 0.88V_{RMS}$ $R_L = 10k\Omega$ f = 1kHz	—	0.05	—	—	—	—	—	%
	Frequency Response (Switch ON) $20 \log_{10} \frac{V_{OUT}}{V_{IN}} = -3dB$	2.5	$V_{SS} = -2.5V$ $V_{IN} 0.88V_{RMS}$ $R_L = 1k\Omega$	—	30	—	—	—	—	—	MHz
	Feedthrough Frequency (Switch OFF) $20 \log_{10} \frac{V_{OUT}}{V_{IN}} = -50dB$	2.5	$V_{SS} = -2.5V$ $V_{IN} 0.88V_{RMS}$ $R_L = 1k\Omega$	—	1.0	—	—	—	—	—	
	Crosstalk (Control Input to Signal Output)	2.0 4.5 6.0	$R_{IN} = 1k\Omega$ $R_L 10k\Omega$	— — —	25 60 75	— — —	— — —	— — —	— — —	— — —	mV
	Crosstalk (Between Any Two Switches)	2.5		—	1.5	—	—	—	—	—	MHz
	Maximum Control Input Frequency	2.0 4.5 6.0	$R_L = 1K\Omega$ $C_L = 15pF$ $V_O = 1/2\ V_{CC}$	— — —	20 30 30	— — —	— — —	— — —	— — —	— — —	
C_{IN}	Control Input Capacitance			—	5	10	—	10	—	10	pF
$C_{I/O}$	Switch Input/Output Capacitance			—	6	—	—	—	—	—	pF
C_{I-O}	Feedthrough Capacitance			—	0.5	—	—	—	—	—	pF
C_{PD}(*)	Power Dissipation Capacitance			—	13	—	—	—	—	—	pF

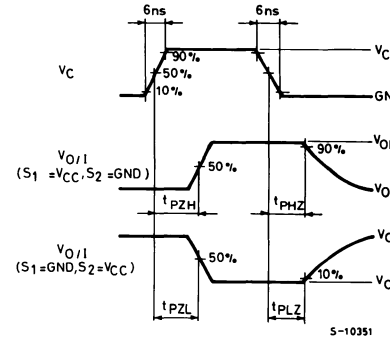
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation.
$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per CHANNEL).

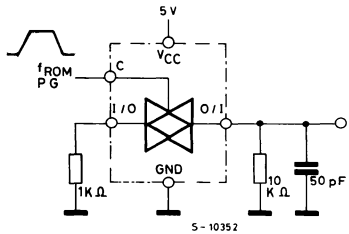
SWITCHING CHARACTERISTICS TEST CIRCUIT

t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}

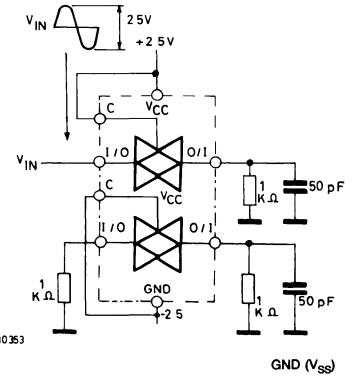




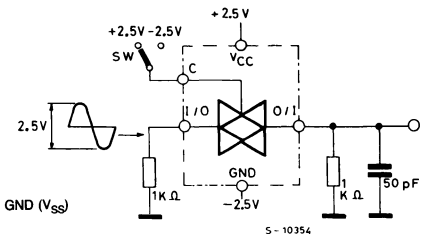
CROSSTALK (CONTROL TO OUTPUT)



CROSSTALK BETWEEN ANY TWO SWITCHES

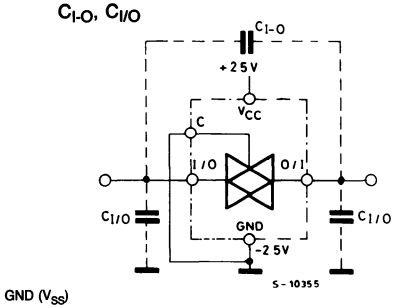


BANDWIDTH AND FEEDTHROUGH ATTENUATION

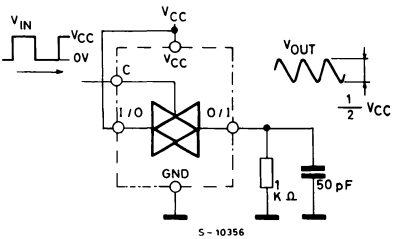


SW	TEST ITEM
+2.5V	-3dB BANDWIDTH TEST
-2.5V	FEEDTHROUGH TEST

C_{I-O}, $C_{I/O}$

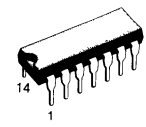


MAXIMUM CONTROL FREQUENCY

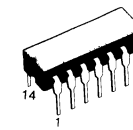


DUAL 4-INPUT OR GATE

- HIGH SPEED
  t_{PD} = 11 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 4072B



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

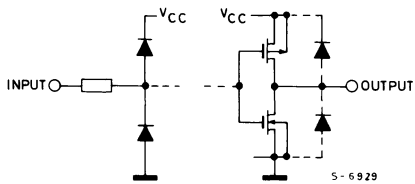
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC4072 F1
M74HC4072 B1N
M74HC4072 F1
M74HC4072 C1
M74HC4072 M1

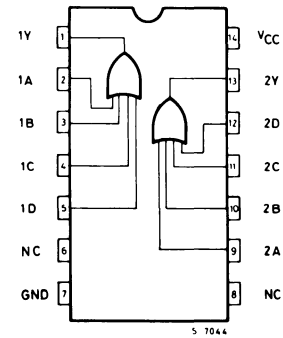
DESCRIPTION

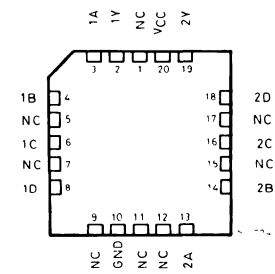
The M54/74HC4072 is a high speed CMOS DUAL 4-INPUT OR GATE fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
The internal circuit is composed of 3 stages including buffer output, which gives high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



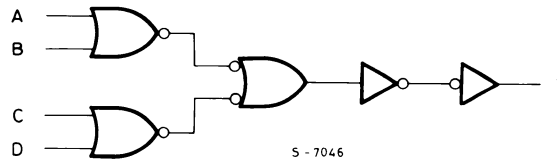
PIN CONNECTIONS (top view)





NC = No Internal Connection

LOGIC DIAGRAM (1/2 of Device Shown)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

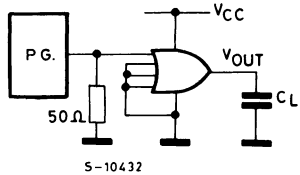
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		11	18	ns

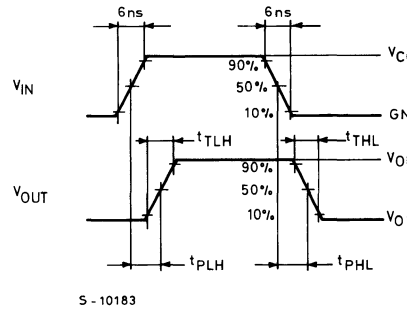
AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	56	110	—	140	—	165	ns
		4.5		—	14	22	—	28	—	33	
		6.0		—	12	19	—	24	—	28	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	28	—	—	—	—	—	pF

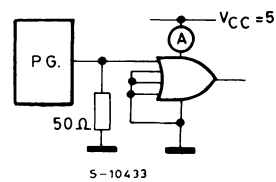
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following equation:
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per Gate).

SWITCHING CHARACTERISTICS TEST CIRCUIT AND WAVEFORM





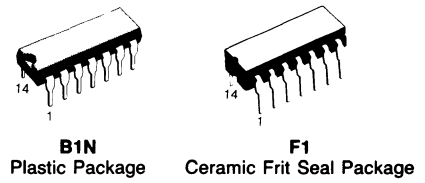
TEST CIRCUIT I_{CC} (Opr)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

TRIPLE 3-INPUT OR GATE

- HIGH SPEED
  t_{PD} = 10 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 4075B



B1N
Plastic Package

F1
Ceramic Frit Seal Package

M1
Micro Package

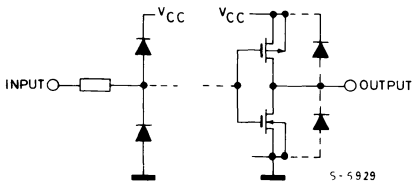
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC4075 F1
M74HC4075 B1N
M74HC4075 F1
M74HC4075 C1
M74HC4075 M1

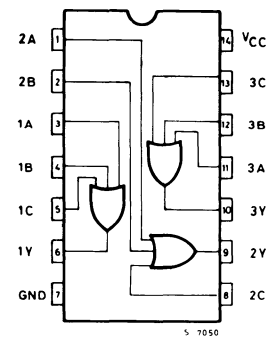
DESCRIPTION

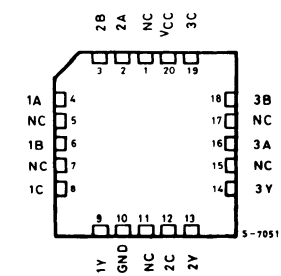
The M54/74HC4075 is a high speed CMOS TRIPLE 3-INPUT OR GATE fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
The internal circuit is composed of 4 stages including buffered output, which gives high noise immunity and a stable output.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



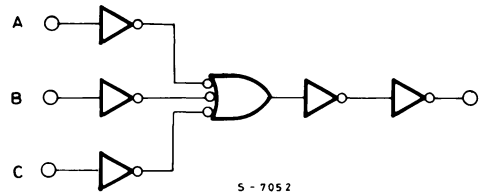
PIN CONNECTIONS (top view)





NC =
No Internal
Connection

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series Operating Temperature 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

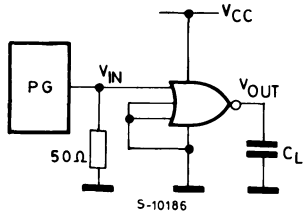
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		10	17	ns

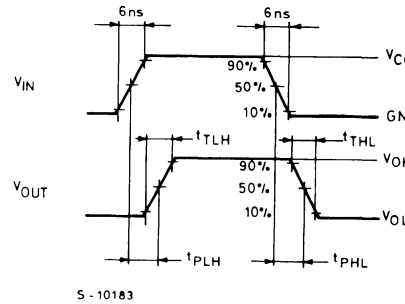
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			-40 to $85°C$ 74HC		-55 to $125°C$ 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	48	100	—	125	—	150	ns
		4.5		—	12	20	—	25	—	30	
		6.0		—	10	17	—	21	—	26	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	30	—	—	—	—	—	pF

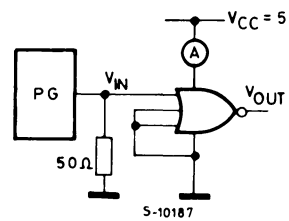
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/3$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT





TEST CIRCUIT I_{CC} (Opr.)



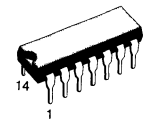
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

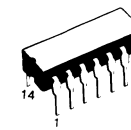
M54HC4078
M74HC4078

8 INPUT NOR/OR GATE

- HIGH SPEED
  t_{PD} = 14 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 4078B



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

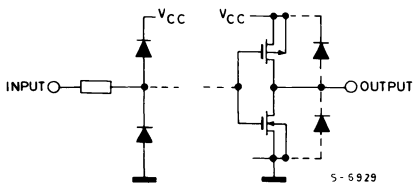
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC4078 F1
M74HC4078 B1N
M74HC4078 F1
M74HC4078 C1
M74HC4078 M1

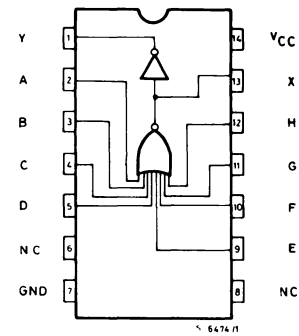
DESCRIPTION

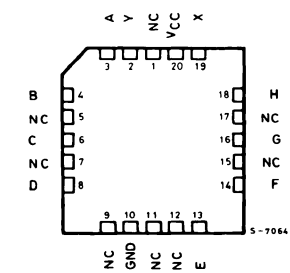
The M54/74HC4078 is a high speed CMOS 8 INPUT NOR/OR GATE fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



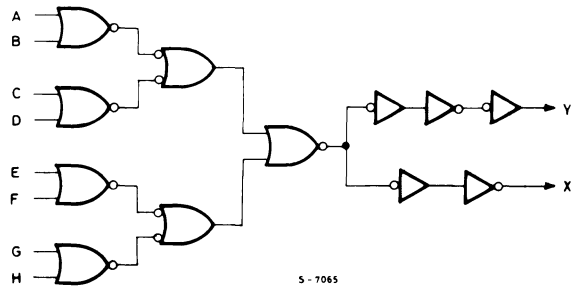
PIN CONNECTIONS (top view)





NC =
No Internal
Connection

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		14	22	ns

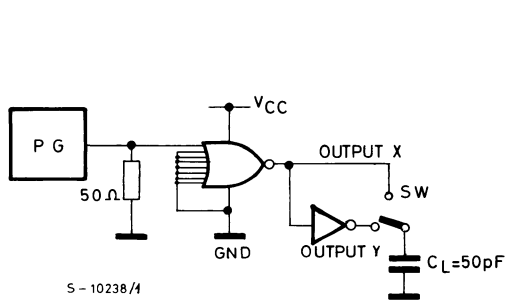
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

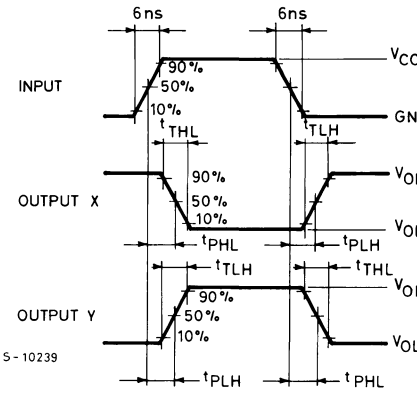
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			-40 to $85°C$ 74HC		-55 to $125°C$ 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	68	130	—	165	—	195	ns
		4.5		—	17	26	—	33	—	39	
		6.0		—	14	22	—	28	—	33	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	66	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

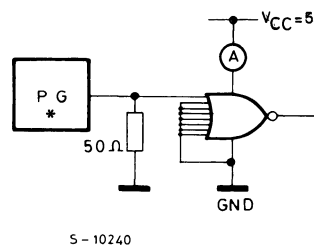
Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$.

SWITCHING CHARACTERISTICS TEST CIRCUIT





TEST CIRCUIT I_{CC} (Opr.)



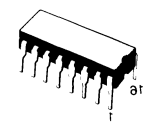
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

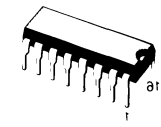
M54HC4094
M74HC4094

8-BIT SIPO SHIFT LATCH REGISTER (3-STATE)

- HIGH SPEED
  f_{MAX} = 42 MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 4094B



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

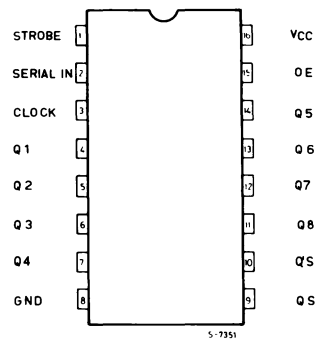
ORDERING NUMBERS:

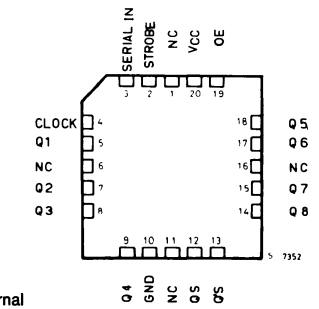
M54HC4094 F1
M74HC4094 B1N
M74HC4094 F1
M74HC4094 C1
M74HC4094 M1

DESCRIPTION

The M54/74HC4094 is a high speed CMOS 8 BIT SIPO SHIFT LATCH REGISTER fabricated with silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device consists of an 8-bit shift register and an 8-bit latch with 3-state output buffer. Data is shifted serially through the shift register on the positive going transition of the clock input signal. The output of the last stage (Qs) can be used to cascade several devices.
Data on the Qs output is transferred to a second output (Qs') on the following negative transition of the clock input signal. The data of each stage of the shift register is provided with a latch, which latches data on the negative going transition of the STROBE input signal. When the STROBE input is held high, data propagates through the latch to a 3-state output buffer.
This buffer is enabled when OUTPUT ENABLE input is taken high. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)





NC = No Internal Connection

TRUTH TABLE

CK	OE	ST	SI	PARA. OUT.		SERI. OUT	
				Q1	Qn	Qs	Qs'
↑	H	H	L	L	Qn-1	Q7	NC
↑	H	H	H	H	Qn-1	Q7	NC
↑	H	L	X	NC	NC	Q7	NC
↑	L	X	X	Z	Z	Q7	NC
↓	H	X	X	NC	NC	NC	Qs
↓	L	X	X	Z	Z	NC	Qs

X: DON'T CARE

NC: NO CHANGE

Z: HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

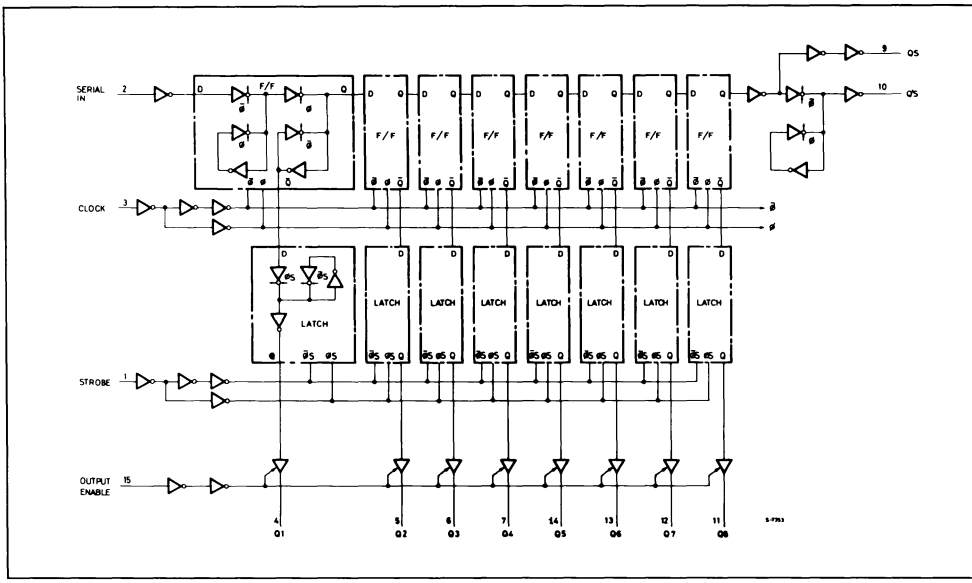
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

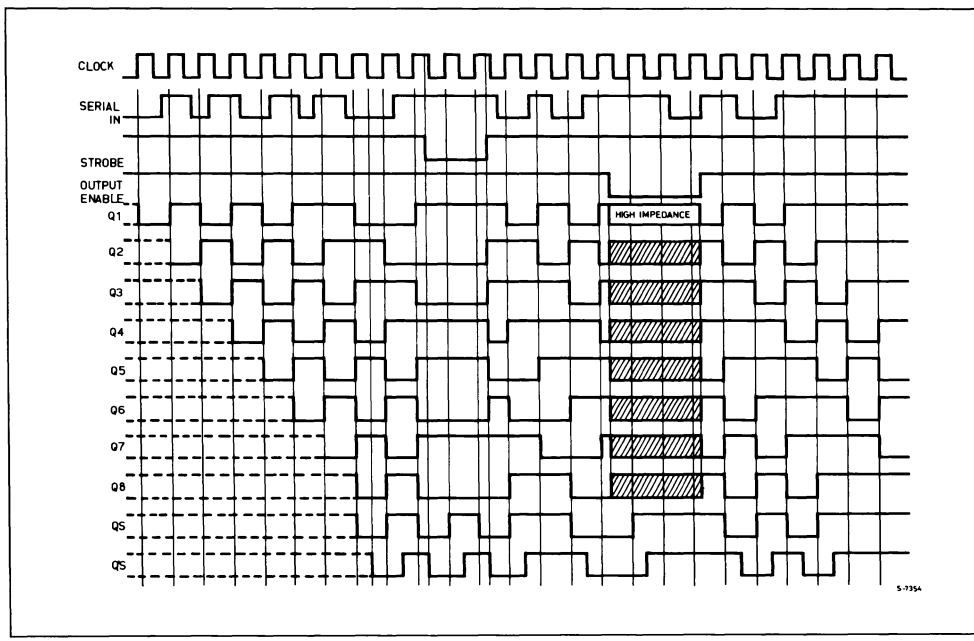
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

LOGIC DIAGRAM



LOGIC DIAGRAM



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0.0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{OZ}	3-State Output Off-State Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	±0.5	—	±5	—	±10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-QN)		31	48	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Qs, Qs')		22	35	ns
t_{PLH}	Propagation Delay Time		23	36	ns
f_{MAX}	Maximum Clock Frequency	22	42		MHz

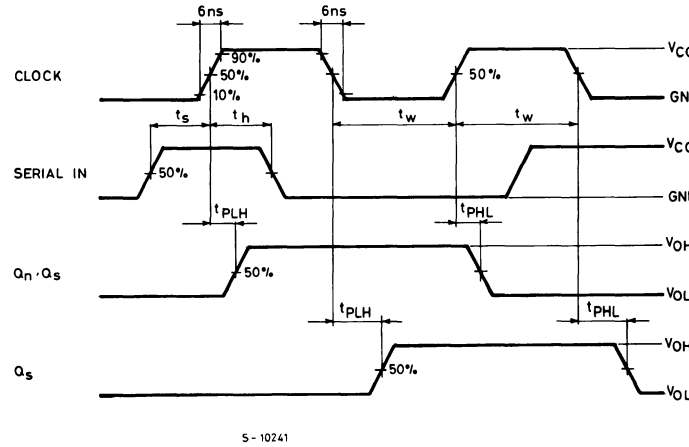
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Qn)	2.0		—	140	270	—	340		405	ns
		4.5		—	35	54	—	68		81	
		6.0		—	30	46	—	58		69	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK, Qs, Qs')	2.0		—	104	200	—	250		300	ns
		4.5		—	26	40	—	50		60	
		6.0		—	22	34	—	43		51	
t_{PLH} t_{PHL}	Propagation Delay Time (STROBE - Qn)	2.0		—	135	210	—	265	—	315	ns
		4.5		—	27	42	—	53	—	63	
		6.0		—	23	36	—	45	—	54	
f_{MAX}	Maximum Clock Frequency	2.0		4	10	—	3.2	—	2.6	—	MHz
		4.5		20	38	—	16	—	13	—	
		6.0		24	45	—	19	—	15	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	35	100	—	125		150	ns
		4.5		—	9	20	—	25		30	
		6.0		—	8	17	—	21		26	
$t_{W(H)}$	Minimum Pulse Width (STROBE)	2.0		—	35	100	—	125		150	ns
		4.5		—	9	20	—	25		30	
		6.0		—	8	17	—	21		26	
t_s	Minimum Set-up Time (SERIAL-IN)	2.0		—	26	75	—	95	—	110	ns
		4.5		—	6	15	—	19	—	22	
		6.0		—	5	13	—	16	—	19	
t_s	Minimum Set-up Time (STROBE)	2.0		—	50	150	—	190	—	225	ns
		4.5		—	13	30	—	38	—	45	
		6.0		—	11	26	—	33	—	38	
t_h	Minimum Hold Time (SERIAL-IN)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_h	Minimum Hold Time (STROBE)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{PZL} t_{PZH}	3-State Output Enable Time	2.0	$R_L = 1k\Omega$	—	76	150	—	190	—	225	ns
		4.5		—	19	30	—	38	—	45	
		6.0		—	16	26	—	33	—	38	
t_{PLZ} t_{PHZ}	3-State Output Disable Time	2.0	$R_L = 1k\Omega$	—	84	150	—	190	—	225	ns
		4.5		—	21	30	—	38	—	45	
		6.0		—	18	26	—	33	—	38	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	167	—	—	—			pF

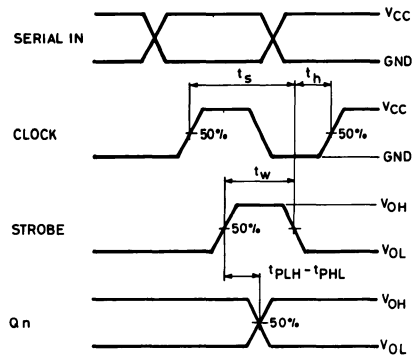
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

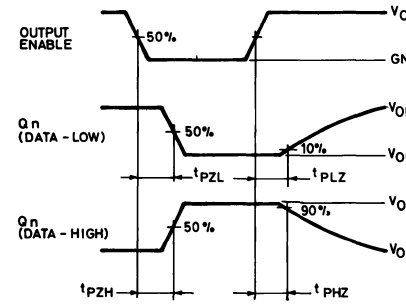
SWITCHING CHARACTERISTICS TEST WAVEFORM



S-10241

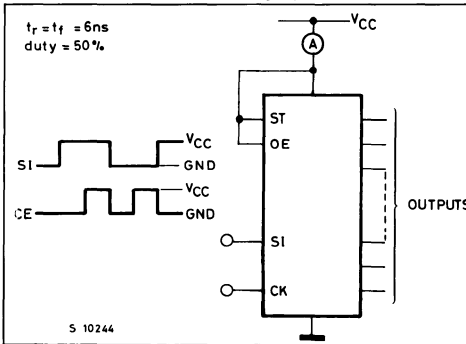


S-10242



S-10243

TEST WAVEFORM I_{CC} (Opr.)



S 10244

C_{PD} CALCULATION

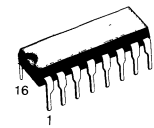
C_{PD} is to be calculated with the following formula by using the measured value of I_{CC} (Opr.) in the test circuit opposite.

$$C_{PD} = \frac{I_{CC}(Opr)}{f_{IN} \cdot V_{CC}}$$

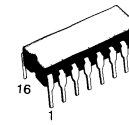
In determining the typical value of C_{PD}, a relatively high frequency of 1MHz was applied to f_{IN}, in order to eliminate any error caused by the quiescent supply current.

BCD TO-7 SEGMENT LATCH/DECODER/DRIVER

- HIGH SPEED
  t_{PD} = 15 ns (Typ) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 20 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 4511B



B1N
Plastic Package



F1
Ceramic Frit Seal Package

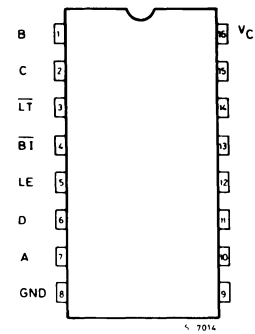
M1
Micro Package

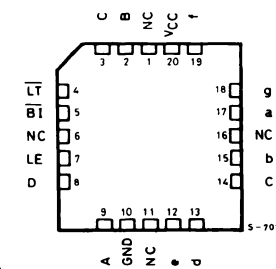
C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC4511 F1	M74HC4511 F1
M74HC4511 B1N	M74HC4511 M1

PIN CONNECTION (top view)





NC = No Internal Connection

DESCRIPTION

The M54/74HC4511 is a high speed CMOS BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER fabricated with silicon gate C²MOS technology. It enables high speed latch and decode operation with identical pin connection and function to standard CMOS 4511B.

The segment output driver, which is CMOS fabricated in silicon gate C²MOS technology, has large I_{OH} capability which enables common cathode Leds to be directly driven.

When lamp test ($\overline{LT}$) is taken "L", all segment outputs will go to "H", and when blanking ($\overline{BI}$) is taken "L" and $\overline{LT}$ is taken "H" all segment outputs will go to "L".

These functions operate regardless of other inputs and are used to test the display.

Input BI is used to pulse-modulate the brightness of the display.

When an error input code (over 10) is applied to the BCD input, all segment outputs will go "L"(turn off).

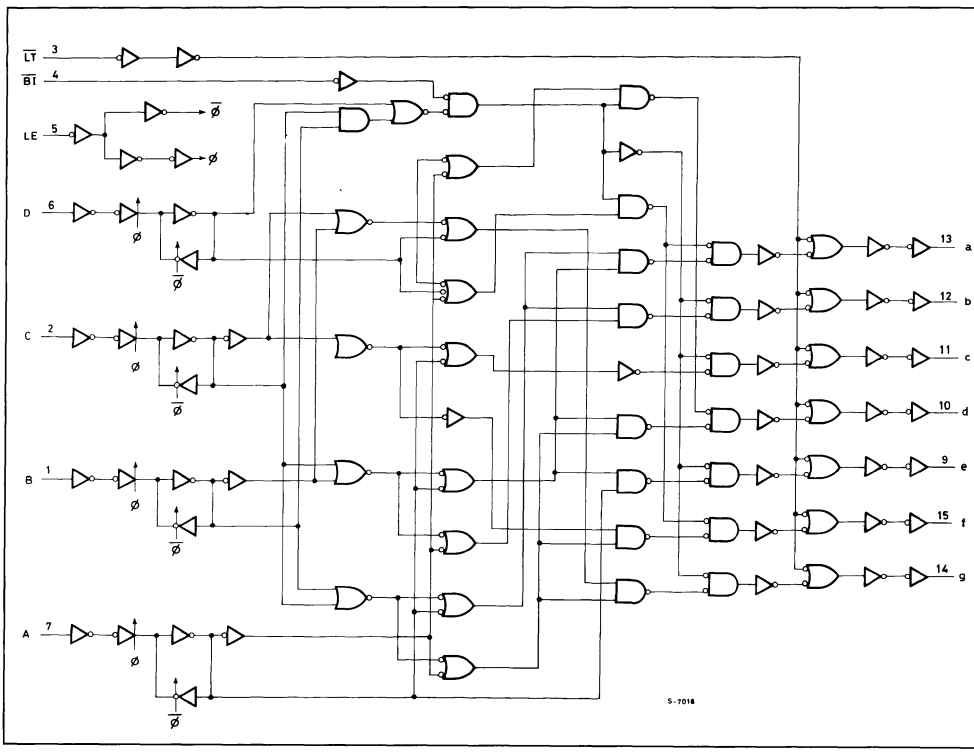
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

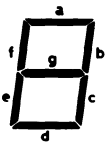
INPUTS							OUTPUTS							DISPLAY MODE
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	BLANK
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	X	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	X	X	L	L	L	L	L	L	L	BLANK
H	H	H	X	X	X	X	Hold the stage at the leading edge of LE							

X: DON'T CARE

LOGIC DIAGRAM



DISPLAY MODE



INPUT CODE											
	A	L	H	L	H	L	H	L	H	L	H
	B	L	L	H	H	L	L	H	H	L	L
	C	L	L	L	L	H	H	H	H	L	L
	D	L	L	L	L	L	L	L	L	H	H
DISPLAY		0	1	2	3	4	5	6	7	8	9

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	+25/−35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	+150/−50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

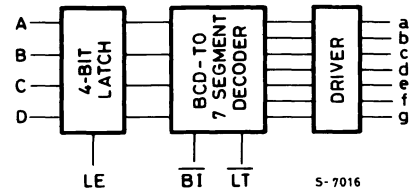
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC}	2 V: 0 to 1000 4.5V: 0 to 500 6 V: 0 to 400	ns

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

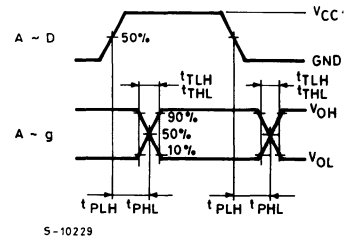
Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−20 mA	3.20	3.80	—	2.90	—			
				−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{BCD}$ - Segment)		46	71	ns
t_{PHL} t_{PLH}	Propagation Delay Time $\overline{BI}$- Segment		28	44	ns
t_{PLH} t_{PHL}	Propagation Delay Time $\overline{LT}$ - Segment		16	26	ns
t_{PHL} t_{PHL}	Propagation Delay Time $\overline{LE}$ - Segment		46	71	ns

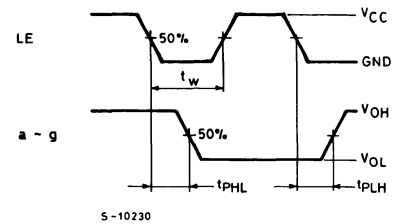
SWITCHING CHARACTERISTICS TEST WAVEFORM

Data Segment Delay Time



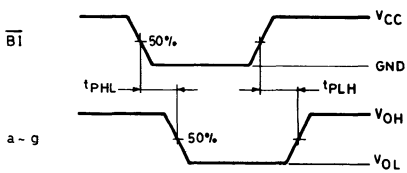
S-10229

LE-Segment Delay Time



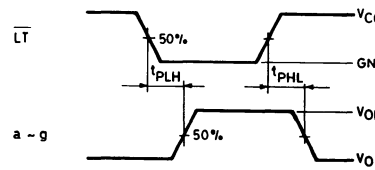
S-10230

$\overline{BI}$-Segment Delay Time



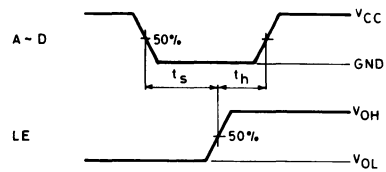
S-10231

$\overline{LT}$-Segment Delay Time



S-10232

Data Set-up/Hold Time



S-10233

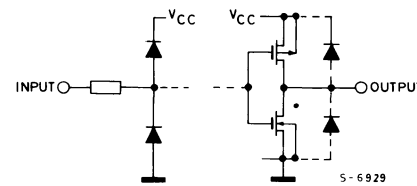
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time Low to High	2.0		—	25	60	—	75		90	ns
		4.5		—	6	12	—	15		18	
		6.0		—	5	10	—	13		15	
t_{THL}	Output Transition Time High to Low	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH}, t_{PHL}	Propagation Delay Time (BCD-Segment)	2.0		—	192	400	—	505		600	ns
		4.5		—	48	80	—	101		120	
		6.0		—	41	68	—	87		102	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{BI}$-Segment)	2.0		—	116	250	—	315		375	ns
		4.5		—	29	50	—	63		75	
		6.0		—	25	43	—	54		64	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{LT}$-Segment)	2.0		—	72	150	—	190		225	ns
		4.5		—	18	30	—	38		45	
		6.0		—	15	26	—	33		38	
t_{PLH} t_{PHL}	Propagation Delay Time (LE-Segment)	2.0		—	192	400	—	505		600	ns
		4.5		—	48	80	—	101		120	
		6.0		—	41	68	—	87		102	
$t_{W(L)}$	Minimum Pulse Width (CLEAR) ($\overline{LE}$)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_s	Minimum Set-up Time	2.0		—	35	75	—	95		110	ns
		4.5		—	9	15	—	19		22	
		6.0		—	8	13	—	16		19	
t_h	Minimum Data Hold Time	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	136	—	—	—			pF

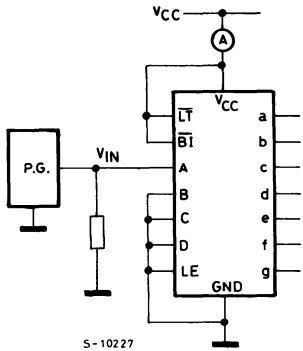
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

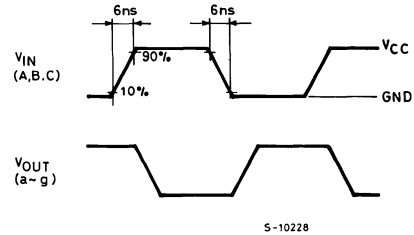
Average operating current is: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

INPUT AND OUTPUT EQUIVALENT CIRCUIT



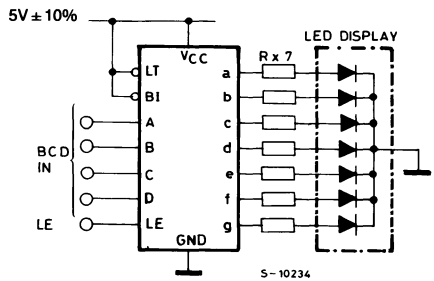
TEST CIRCUIT I_{CC} (Opr.)





APPLICATION CIRCUIT

Static Display Circuit

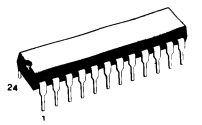


SGS-THOMSON MICROELECTRONICS

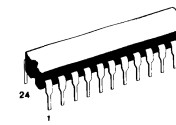
M54/74HC4514
M54/74HC4515

HC4514 4-TO-16 LINE DECODER/LATCH
HC4515 4-TO-16 LINE DECODER/LATCH (INV.)

- HIGH SPEED
  t_{PD} = 24 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 4514B/4515B



B1N
Plastic Package



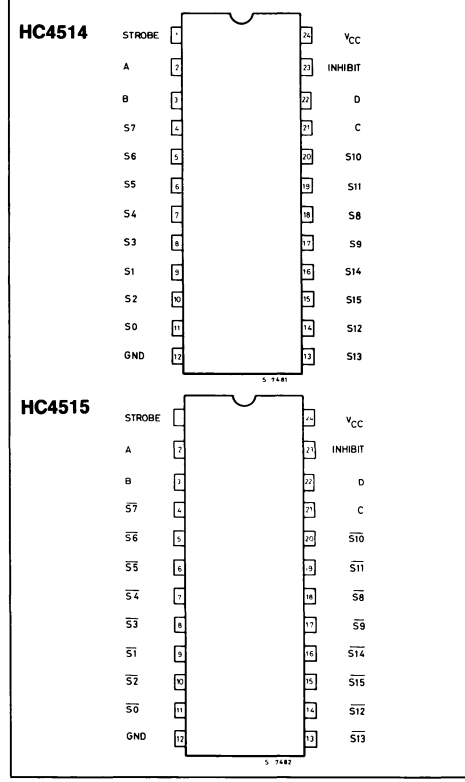
F1
Ceramic Frit Seal Package

M1
Micro Package

ORDERING NUMBERS:

M54HCXXXF1	M74HCXXXM1
M74HCXXXB1N	M74HCXXXF1

PIN CONNECTIONS (top view)



DESCRIPTION

The M54/74HC4514 and the M54/74HC4515 are high speed CMOS 4-LINE TO 16-LINE DECODERS WITH LATCHED INPUTS fabricated in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption.
A binary code stored in the four input latches (A to D) provides a high level (HC4514) or a low level (HC4515) at the selected one of sixteen outputs excluding the other fifteen outputs, when the inhibit input (INHIBIT) is held low. When the inhibit input is held high, all outputs are kept low level (HC4514) or high level (HC4515), while the latch function is available. The data applied to the data inputs are transfered to the Q outputs of latches when the strobe input is held high. When the strobe input is taken low, the information data applied to the data input at a time is retained at the output of the latches. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

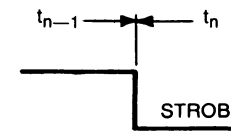
TRUTH TABLE

INPUTS					SELECT OUTPUT HC4514 — 'H' (HC4515 — 'L')
INHIBIT	A	B	C	D	
L	L	L	L	L	S0 ($\overline{S0}$)
L	H	L	L	L	S1 ($\overline{S1}$)
L	L	H	L	L	S2 ($\overline{S2}$)
L	H	H	L	L	S3 ($\overline{S3}$)
L	L	L	H	L	S4 ($\overline{S4}$)
L	H	L	H	L	S5 ($\overline{S5}$)
L	L	H	H	L	S6 ($\overline{S6}$)
L	H	H	H	L	S7 ($\overline{S7}$)
L	L	L	L	H	S8 ($\overline{S8}$)
L	H	L	L	H	S9 ($\overline{S9}$)
L	L	H	L	H	S10 ($\overline{S10}$)
L	H	H	L	H	S11 ($\overline{S11}$)
L	L	L	H	H	S12 ($\overline{S12}$)
L	H	L	H	H	S13 ($\overline{S13}$)
L	L	H	H	H	S14 ($\overline{S14}$)
L	H	H	H	H	S15 ($\overline{S15}$)
H	X	X	X	X	HC4514 — ALL OUTPUTS 'L' (HC4515 — ALL OUTPUTS 'H')

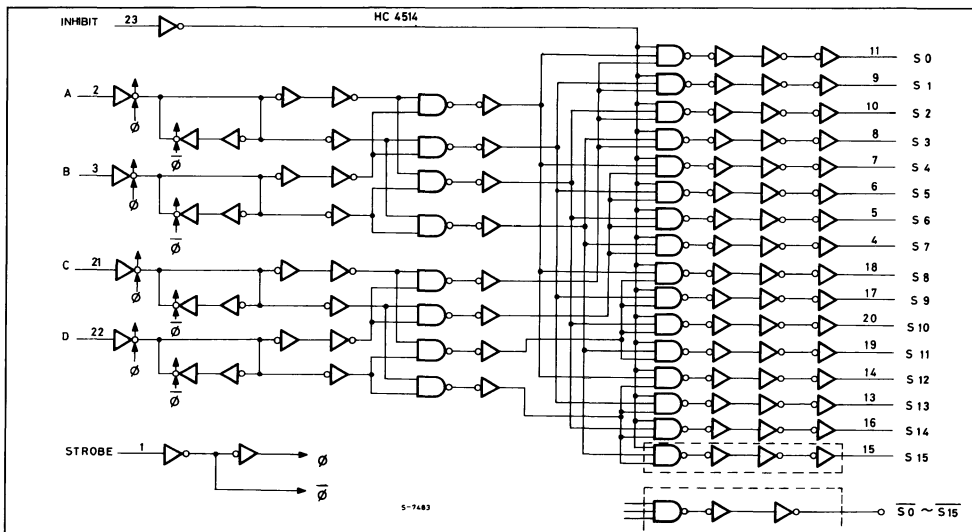
X: DON'T CARE

STROBE = 'H'
REFER TO TRUTH TABLE

STROBE = 'L'
DATA AT THE NEGATIVE GOING TRANSITION OF STROBE SHALL BE PROVIDED ON THE EACH OUPTUT WHILE STROBE IS HELD LOW.



LOGIC DIAGRAM (HC4514)



FOR HC 4515 DEVICE LOGIC DIAGRAM SHOWN AT THE BOTTOM SHALL TAKE THE PLACE OF OUTPUT CIRCUITS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0	or		5.9	6.0	—	5.9	—	5.9	—	
		4.5	V_{IL}	−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	

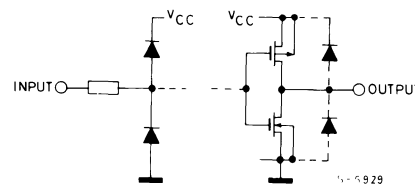
DC SPECIFICATIONS (Continued)

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
			V_I	I_O	Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (Data - Sn, $\overline{Sn}$)		24	37	ns
t_{PLH} t_{PHL}	Propagation Delay Time (STROBE - Sn, $\overline{Sn}$)		27	44	ns
t_{PLH} t_{PHL}	Propagation Delay Time (INHIBIT - Sn, $\overline{Sn}$)		19	30	ns

INPUT AND OUTPUT EQUIVALENT CIRCUIT

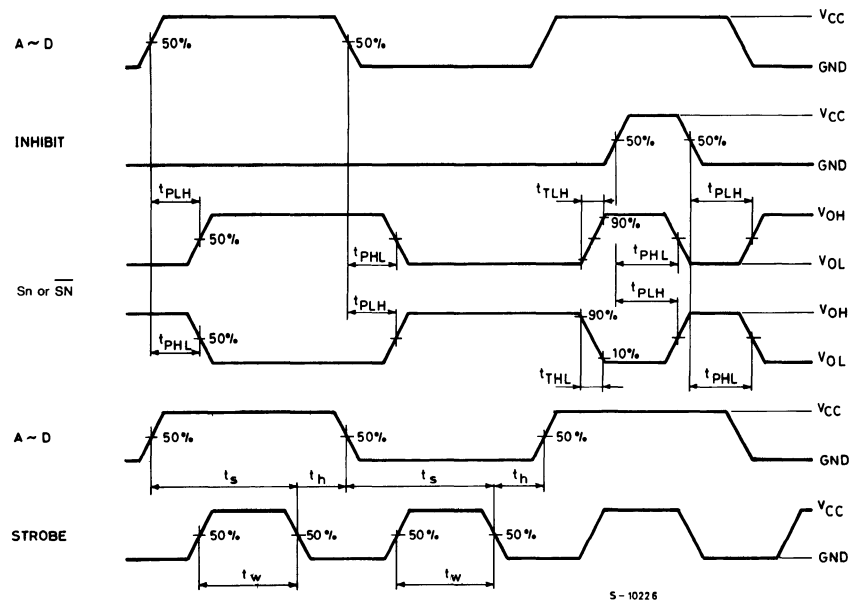


AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

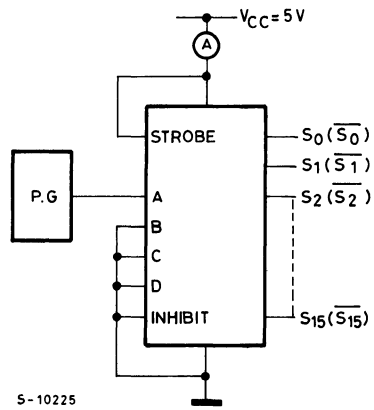
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			− 40 to 85°C 74HC		− 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA-Sn, $\overline{Sn}$)	2.0		—	108	215	—	270	—	325	ns
		4.5		—	27	43	—	54	—	65	
		6.0		—	23	37	—	46	—	55	
t_{PLH} t_{PHL}	STROBE-Sn $\overline{Sn}$)	2.0		—	124	245	—	305	—	370	ns
		4.5		—	31	49	—	61	—	74	
		6.0		—	26	42	—	52	—	63	
t_{PLH} t_{PHL}	INHIBIT-Sn $\overline{Sn}$)	2.0		—	88	175	—	220	—	265	ns
		4.5		—	22	35	—	44	—	53	
		6.0		—	19	30	—	37	—	45	
$t_{W(H)}$	Minimum Pulse Width STROBE	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-Up Time DATA	2.0		—	10	50	—	65	—	75	ns
		4.5		—	4	10	—	13	—	15	
		6.0		—	3	9	—	11	—	13	
t_h	Minimum Hold Time DATA	2.0		—	—	5	—	5	—	5	ns
		4.5		—	—	5	—	5	—	5	
		6.0		—	—	5	—	5	—	5	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance		HC4514	—	69	—	—	—	—	—	pF
			HC4515	—	72	—	—	—	—	—	

Note (*): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating curren can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$.

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



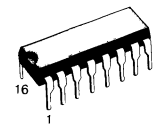
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

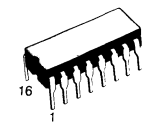
M54/74HC4518
M54/74HC4520

HC4518 DUAL DECADE COUNTER
HC4520 DUAL 4 BIT BINARY COUNTER

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (Min.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 4520B/4518B



B1N
Plastic Package



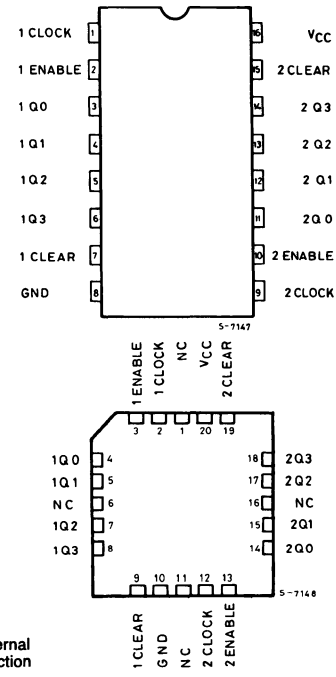
F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HCXXXX F1
M74HCXXXX B1N
M74HCXXXX F1
M74HCXXXX C1
M74HCXXXX M1

PIN CONNECTIONS (top view)



NC = No Internal Connection

DESCRIPTION

The M54/74HC4518/4520 are a high speed CMOS DUAL 4 BIT BINARY COUNTERS fabricated in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption.
They consists of two identical internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable Clock and ENABLE inputs for incrementing on either the positive-going or negative-going transition.
For single-unit operation the ENABLE input is maintained «high» and the counter advances on each positive-going transition of the CLOCK. The counters are cleared by high levels on their clear lines. The counter can be cascaded in the ripple mode by connecting Q4 to the enable input of the subsequent counter while the clock input of the latter is held permanently low.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUTS			FUNCTION
CLOCK	ENABLE	CLEAR	
↑	H	L	INCREMENT COUNTER
L	↓	L	INCREMENT COUNTER
↓	X	L	NO CHANGE
X	↑	L	NO CHANGE
↑	L	L	NO CHANGE
H	↓	L	NO CHANGE
X	X	H	Q0 THRU Q3 = L

X: DON'T CARE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

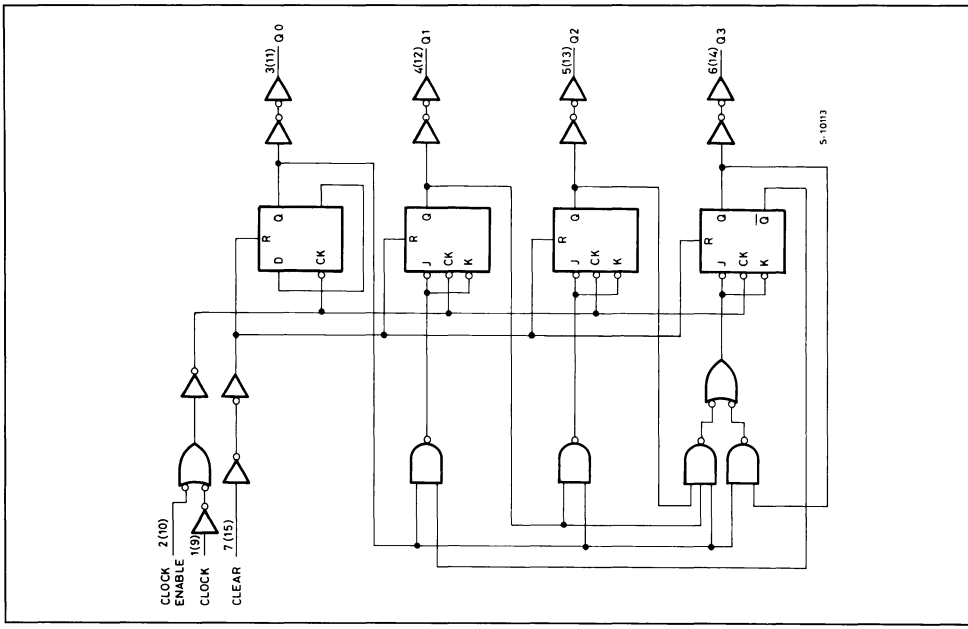
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

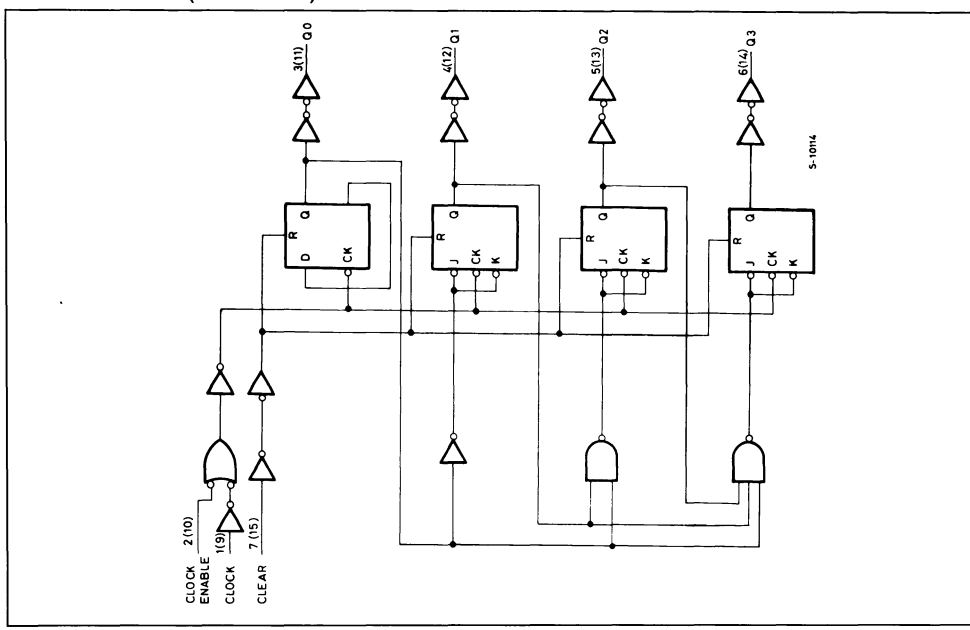
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC}	2 V: 0 to 1000 4.5V: 0 to 500 6 V: 0 to 400	ns

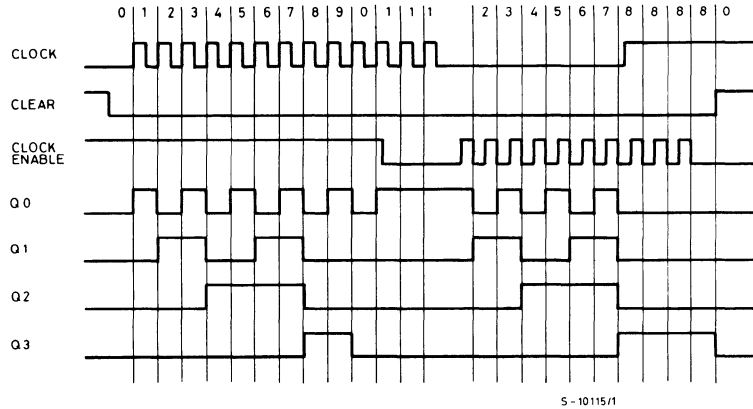
LOGIC DIAGRAM (1/2 HC4518)



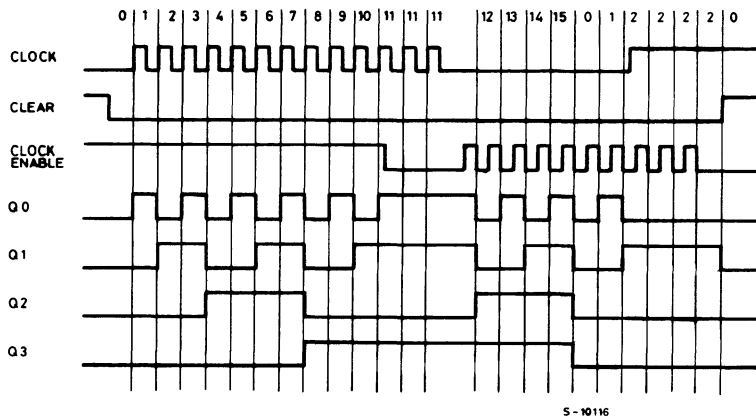
LOGIC DIAGRAM (1/2 HC4520)



TIMING CHART (HC4518)



TIMING CHART (HC4520)



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_{IN}	I_{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	
I_{CC}	Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	4.0	—	40.0	—	80.0	

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

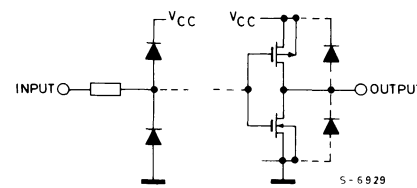
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK, CE-Qn)		21	33	ns
t_{PLH}	Propagation Delay Time (CLEAR-Qn)		23	36	ns
f_{MAX}	Maximum Clock Frequency		53	28	MHz

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

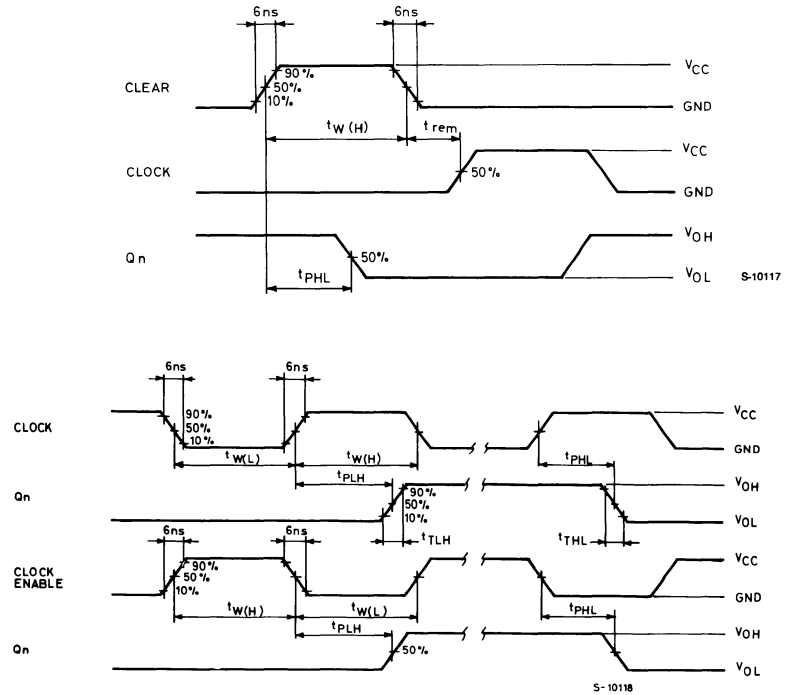
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (CK, CE-Qn)	2.0		—	100	190	—	240	—	285	ns
		4.5		—	25	38	—	48	—	57	
		6.0		—	21	32	—	41	—	48	
t_{PHL}	Propagation Delay Time (CLEAR-Qn)	2.0		—	104	205	—	255	—	310	ns
		4.5		—	26	41	—	51	—	62	
		6.0		—	22	35	—	43	—	53	
f_{MAX}	Maximum Clock Frequency	2.0		5	12	—	4	—	3	—	MHz
		4.5		25	48	—	20	—	17	—	
		6.0		29	56	—	24	—	20	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Clock Pulse Width (CK, CE)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0		—	35	100	—	125	—	150	ns
		4.5		—	9	20	—	25	—	30	
		6.0		—	8	17	—	21	—	26	
t_{REM}	Minimum Removal Time (CLEAR)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance		HC4518	—	145	—	—	—	—	—	pF
			HC4520	—	145	—	—	—	—	—	

Note (*) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test circuit).
Average operating current can be obtained from the equation: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per circuit)

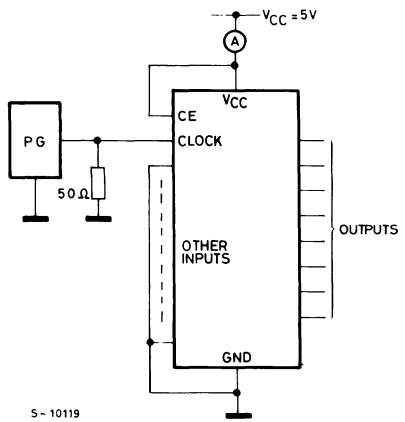
INPUT AND OUTPUT EQUIVALENT CIRCUIT



SWITCHING CHARACTERISTICS TEST WAVEFORMS



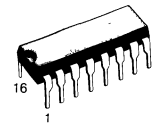
TEST CIRCUIT I_{CC} (Opr.)



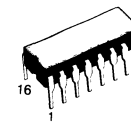
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TESTS

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

- HIGH SPEED
  t_{PD} = 27 ns (TYP) at V_{CC} = 5V
- LOW POWER DISSIPATION
  STANDBY STATE I_{CC} = 4 μA (MAX.) at T_A = 25°C
  ACTIVE STATE I_{CC} = 200 μA (TYP) at V_{CC} = 5V
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OUTPUT PULSE WIDTH RANGE
  t_{WOUT} = 120ns ~ 60s over at V_{CC} = 4.5V
- OUTPUT PULSE WIDTH INDEPENDENT FROM TRIGGER INPUT PULSE WIDTH.
- PIN AND FUNCTION COMPATIBLE WITH 4538B



B1N
Plastic Package



F1
Ceramic Frit Seal Package

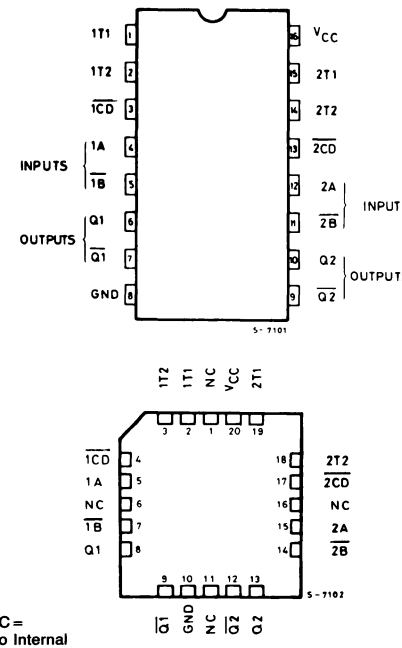
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC123 F1
M74HC123 B1N
M74HC123 F1
M74HC123 C1
M74HC123 M1

PIN CONNECTIONS (top view)



NC = No Internal Connection

DESCRIPTION

The M54/74HC4538 is a high speed CMOS DUAL MONOSTABLE MULTIVIBRATOR fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. Each multivibrator features both a negative, A, and a positive, B, edge triggered input, either of which can be used as an inhibt input. Also included is a clear input that when taken low resets the one shot. The monostable multivibrators are retriggerable. That is, they may be triggered reapeatedly while their outputs are generating a pulse and the pulse will be extended. Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques. The output pulse equation is simply: PW = 0.7 (R)(C) where PW is in seconds, R in Ohms, and C is in Farads.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUTS			OUTPUTS		NOTE
A	$\overline{B}$	$\overline{CD}$	Q	$\overline{Q}$	
↑	H	H			OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	↓	H			OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X: DON'T CARE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

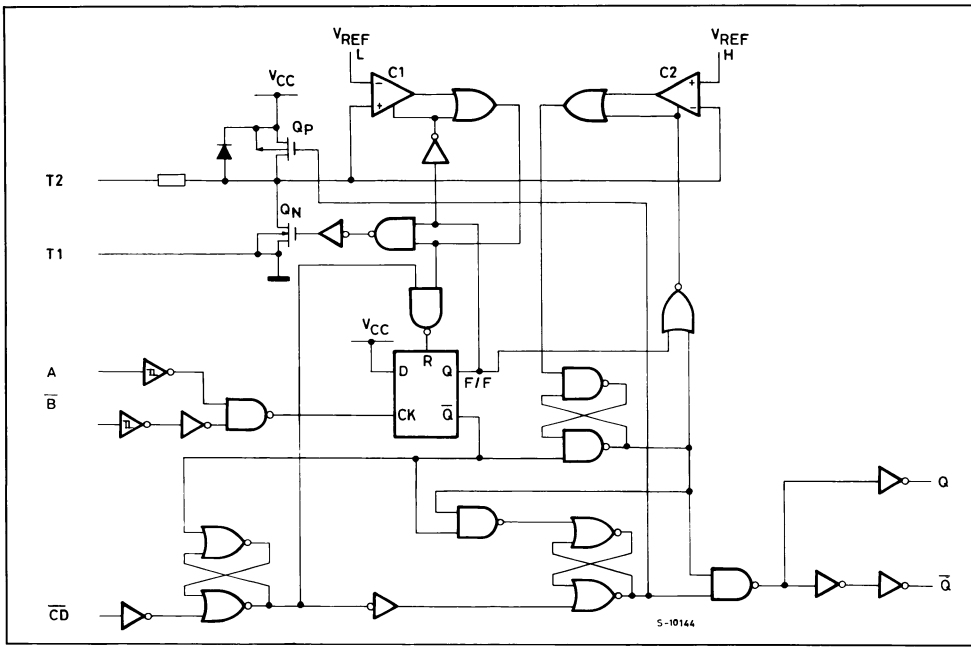
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

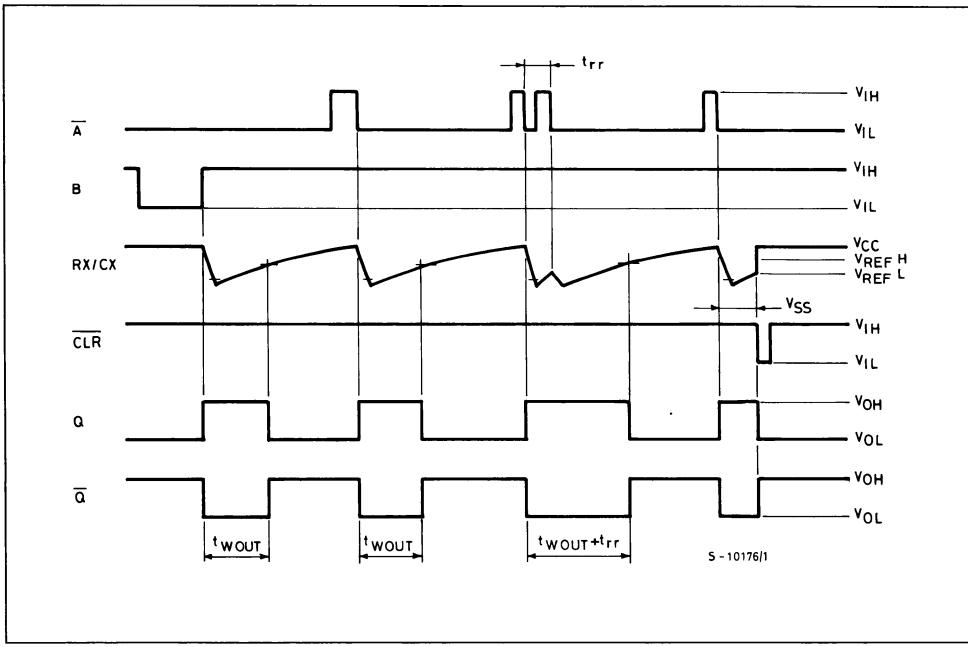
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time ($\overline{CLR}$ only)	V_{CC}	2 V: 0 to 1000 4.5V: 0 to 500 6 V: 0 to 400	ns
Cx	External Capacitor	NO LIMITATION		
Rx	External Resistor	V_{CC}	3 V: 5K to 1M 3 V: 1K to 1M	Ω

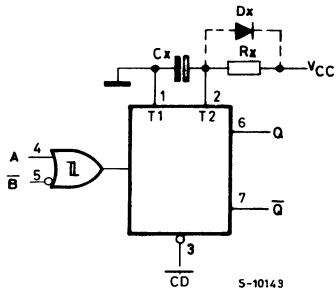
SYSTEM DIAGRAM

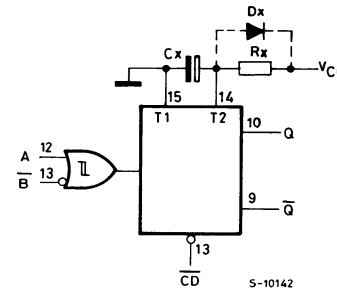


TIMING CHART



BLOCK DIAGRAM





Note:
(1) Cx, Rx, Dx are external components.
(2) Dx is a clamping diode

The external capacitor is charged to V_{CC} in the stand-by state, i.e. no trigger. When the supply voltage is turned off Cx is discharged mainly through an internal parasitic diode (see figures). If Cx is sufficiently large and V_{CC} decreases rapidy, there will be some possibility of damaging the I.C. with a surge current or latch-up. If the voltage supply filter capacitor is large enough and V_{CC} decrease slowly, the surge current is automatically limited and damage the I.C. is avoided. The maximum forward current of the parasitic diode is approximately 20 mA. In cases where Cx is large the time taken for the supply voltage to fall to 0.4 V_{CC} can be calculated as follows:

$t_f \geqq (V_{CC} - 0.7) \cdot Cx/20mA$

In cases where t_f is too short an external champing diode is required to protect the I.C. from the surge current.

FUNCTIONAL DESCRIPTION

Stand-by state

The external capacitor, Cx, is fully charged to V_{CC} in the stand-by state. Hence, before triggering, transistor Qp and Qn (connected to the Rx/Cx node) are both turned off. The two comparators that control the timing and the two reference voltage sources stop operating. The total supply current is therefore only leakage current.

Trigger operation

Triggering occurs when:

1 st) $\underline{A}$ is "low" and $\overline{B}$ has a falling edge;
2 nd) $\overline{B}$ is "high" and A has a rising edge;

After the multivibrator has been retriggered comparator C1 and C2 start operating and Qn is turned on. Cx then discharges through Qn. The voltage at the node Rx/Cx external falls.

When it reaches V_{REFL} the output of comparator C1 becomes low. This in turn resets the flip-flop and Qn is turned off.
At this point C1 stops functioning but C2 continues to operate. The voltage at R/C external begins to rise with a time constant set by the external components Rx, Cx.
Triggering the multivibrator causes Q to go high after internal delay due to the flip-flop and the gate. Q remains high until the voltage at R/C external rises again to V_{REFH}. At this point C2 output goes low and G goes low. C2 stops operating. That means that after triggering when the voltage at R/C external returns to V_{REFH} the multivibrator has returned to its MONOSTABLE STATE. In the case where Rx • Cx are large enough and the discharge time of the capacitor and the delay time in the I.C. can be ignored, the width of the output pulse tw (out) is as follows:

$$t_{W(OUT)} = 0.72\ Cx \cdot Rx$$

FUNCTIONAL DESCRIPTION (Continued)

Re-trigger operation

When a second trigger pulse follows the first its effect will depend on the state of the multivibrator. If the capacitor Cx is being charged the voltage level of Rx/Cx external falls to V_{REFL} again and Q remains high i.e. the retrigger pulse arrives in a time shorter than the period Rx • Cx seconds, the capacitor charging time constant. If the second trigger pulse is very close to the initial trigger pulse it is ineffective; i.e., the second trigger must arrive in the capacitor discharge cycle to be ineffective. Hence the minimum time for a second trigger to be effective, trr (Min.) depends on V_{CC} and Cx.

Reset operation

$\overline{CD}$ is normally high. If $\overline{CD}$ is low, the trigger is not effective because Q output goes low and trigger control flip-flop is reset.

Also transistor Op is turned on and Cx is charged quicky to V_{CC}. This means if $\overline{CD}$ input goes low, the IC becomes waiting state both in operating and non operating state.

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage (Q, $\overline{Q}$ Output)	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage (Q, $\overline{Q}$ Output)	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{IN}	Input Current	6.0	$V_I = V_{CC}$ or GND Rext/Cext		—	—	±0.5	—	±5.0	—	±10	μA
I_{CC}	Quiescent Supply current	6.0	$V_I = V_{CC}$ or GND		—	—	4.0	—	40.0	—	80.0	μA
I_{CC}	Active State (1) Supply Current	2.0	$V_I = V_{CC}$ or GND		—	40	120	—	160	—	—	μA
		4.5	pins 2, 14		—	0.1	0.3	—	0.4	—	—	mA
		6.0	$V_{in} = V_{CC}/2$		—	0.2	0.6	—	0.8	—	—	mA

(1): Per Circuit

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A,$\overline{B}$-Q,$\overline{Q}$)		28	44	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CD}$-Q,$\overline{Q}$)		21	34	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

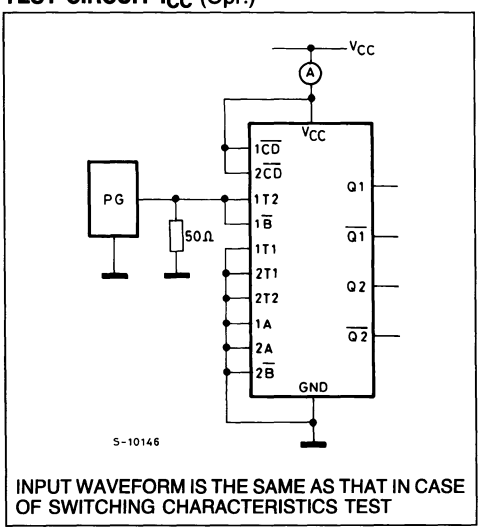
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (A, $\overline{B}$-Q,$\overline{Q}$)	2.0		—	128	250	—	315	—	375	ns
		4.5		—	32	50	—	63	—	75	
		6.0		—	27	43	—	54	—	64	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CD}$-Q, $\overline{Q}$)	2.0		—	100	195	—	245	—	295	ns
		4.5		—	25	39	—	49	—	59	
		6.0		—	21	33	—	42	—	50	
t_{WOUT}	Outpul Pulse Width	3.0	Cx = 12pF	—	210	—		—	—	—	ns
		5.0	Rx = 1kΩ	—	140	—	—	—	—	—	
		3.0	Cx = 100pF	—	1.45	—	—	—	—	—	µs
		5.0	Rx = 10kΩ	—	1.40	—	—	—	—	—	
		3.0	Cx = 1000pF	—	10.5	—	—	—	—	—	µs
		5.0	Rx = 10kΩ	—	10	—	—	—	—	—	
Δt_{WOUT}	Output Pulse Width Error Between Circuits (in Same Package)			—	±1	—	—	—	—	—	%
$t_{W(H)}$ $t_{W(L)}$	Minimum Trigger Pulse Width	2.0	A_{IN}	—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0	$\overline{B}_{IN}$	—	7	13	—	16	—	19	
$t_{W(L)}$	Minimum Clear Pulse Width	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	

AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{rr}	Minimum Retrigger Time	4.5	Cx = 100pF	—	74	—	—	—	—	—	ns
		6.0	Rx = 1KΩ	—	63	—	—	—	—	—	
		4.5	Cx = 0.01μF	—	1.1	—	—	—	—	—	μs
		6.0	Rx = 1KΩ	—	1.0	—	—	—	—	—	
t_{REM}	Minimum Clear Removal time	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	90	—	—	—	—	—	pF

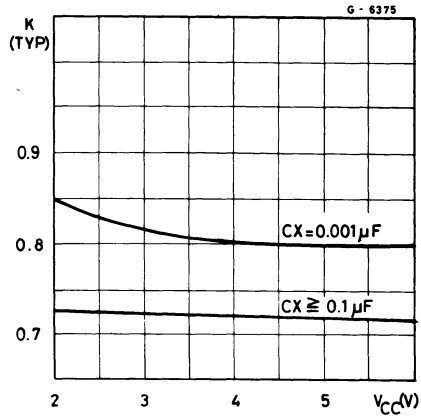
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}' \cdot \text{Duty}/100 + I_{CC}/2$ (per monostable) (I_{CC}': Active Supply Current) (Duty: %)

TEST CIRCUIT I_{CC} (Opr.)

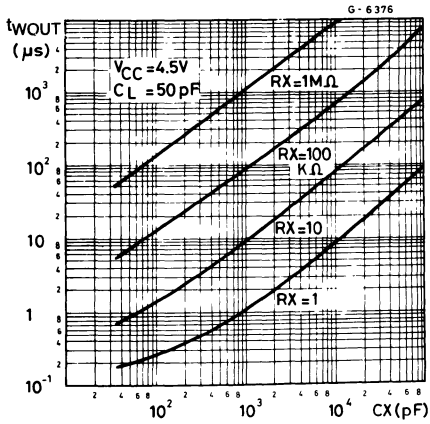


INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

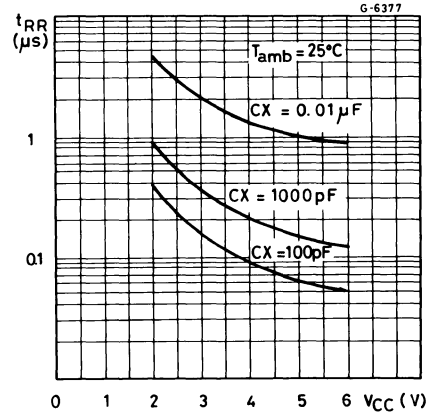
Output Pulse Width Constant
K = Supply Voltage



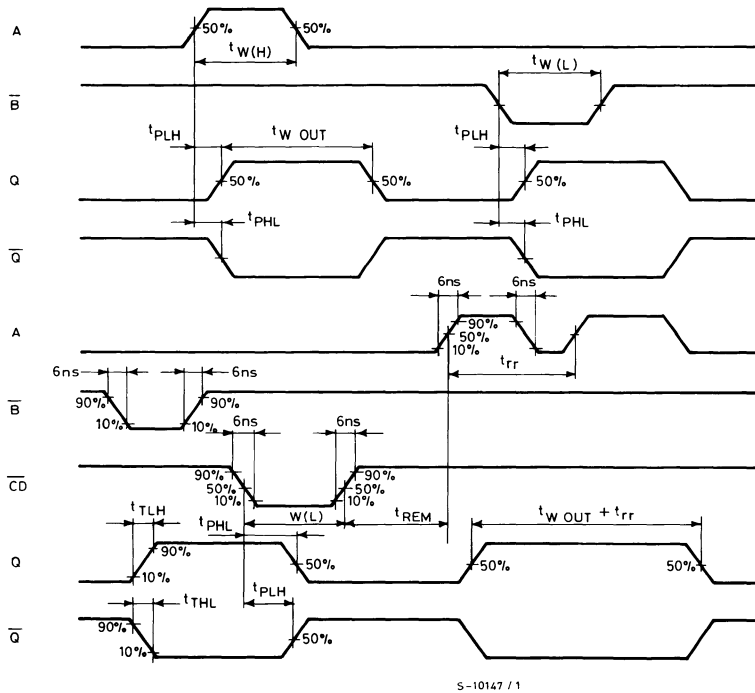
t_{WOUT} - Cx Characteristics (Typ.)



t_{rr} - V_{CC} Characteristics (Typ.)



SWITCHING CHARACTERISTICS TEST WAVEFORM

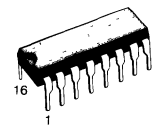


SGS-THOMSON MICROELECTRONICS

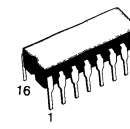
M54HC4543
M74HC4543

BCD-TO-7 SEGMENT LATCH/DECODER/LCD DRIVER

- HIGH SPEED
  t_{PD} = 44 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 4543B



B1N
Plastic Package



F1
Ceramic Frit Seal Package

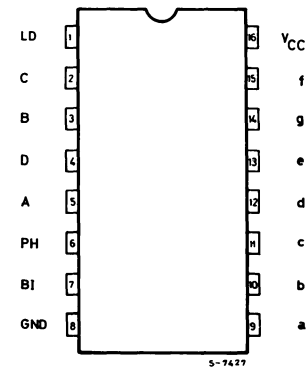
M1
Micro Package

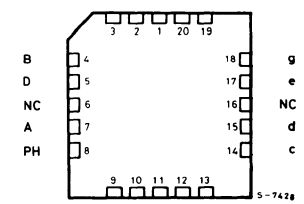
C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC4543 F1
M74HC4543 B1N
M74HC4543 F1
M74HC4543 C1
M74HC4543 M1

PIN CONNECTIONS (top view)





NC = No Internal Connection

DESCRIPTION

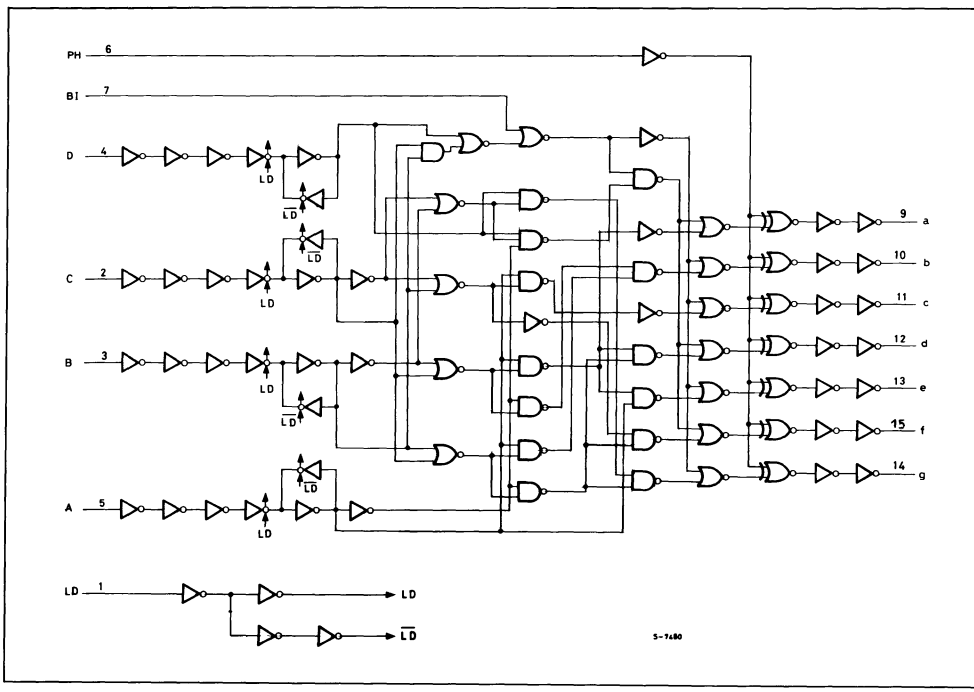
The M54/74HC4543 is a high speed CMOS BCD-TO-7 SEGMENT DECODER WITH LCD DRIVER fabricated in silicon gate C^2MOS technology. High speed latch and decode operation 120 times as fast as standard CMOS 4511B while CMOS low power consumption in maintained. This device consist of BCD-TO-7 segment decoder with a BCD input latch and a 7-segment driver for a liquid crystal display (LCD). When any illegal BCD input signal is applied or input BI is held high, the display is blanked. When driving LCDs, a common square wave signal should be applied not only to the PH input of this device but also to the electrically common back-plane of the display. For other types of readouts, such as light-emitting diode (LED), some additional drivers, such as a transitor array is required. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

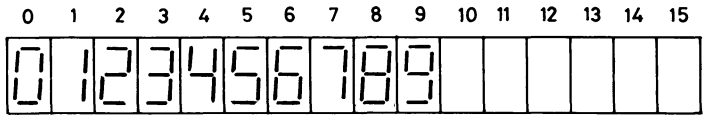
INPUTS							OUTPUTS							DISPLAY
LD	BI	PH	D	C	B	A	a	b	c	d	e	f	g	
X	H	L	X	X	X	X	L	L	L	L	L	L	L	BLANK
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	X	H	X	L	L	L	L	L	L	L	BLANK
H	L	L	H	H	X	X	L	L	L	L	L	L	L	BLANK
L	L	L	X	X	X	X			#	#	#			# # #
↑	↑	H	↑				INVERSE OF ABOVE OUTPUT LEVEL							DISPLAY AS ABOVE

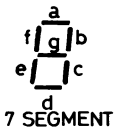
X: DON'T CARE
↑: SAME AS ABOVE COMBINATIONS
#: DEPENDS UPON THE BCD CODE PREVIOUSLY APPLIED WHEN LD = 'H'

LOGIC DIAGRAM



DISPLAY MODE





ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series Operating Temperature 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V V_{CC} 4.5V V_{CC} 6 V	0 to 1000 0 to 500 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

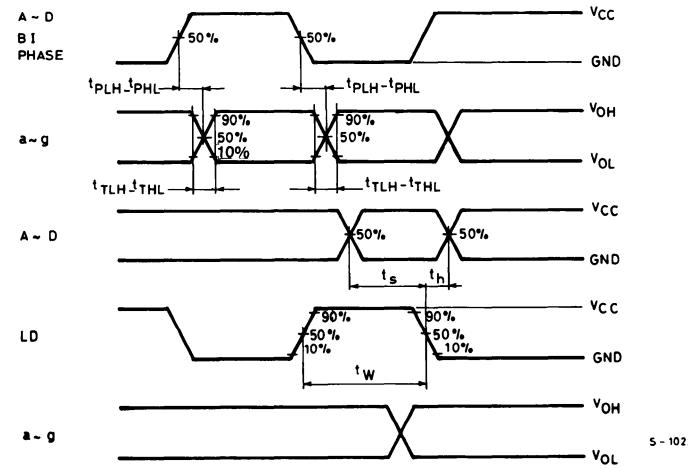
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (BCD - OUT)		44	68	ns
t_{PLH} t_{PHL}	Propagation Delay Time (BI - OUT)		27	42	ns
t_{PLH} t_{PHL}	Propagation Delay Time (PH - OUT)		19	30	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			-40 to $85°C$ 74HC		-55 to $125°C$ 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (BCD - OUT)	2.0		—	200	385	—	485	—	580	ns
		4.5		—	50	77	—	97	—	116	
		6.0		—	43	66	—	83	—	98	
t_{PLH} t_{PHL}	Propagation Delay Time (BI - OUT)	2.0		—	124	240	—	300	—	360	ns
		4.5		—	31	48	—	60	—	72	
		6.0		—	36	41	—	51	—	61	
t_{PHL}	Propagation Delay Time (PH - OUT)	2.0		—	80	175	—	220	—	265	ns
		4.5		—	22	35	—	44	—	53	
		6.0		—	19	30	—	37	—	45	
$t_{W(H)}$	Minimum Pulse Width (LD)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-Up Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_h	Minimum Hold Time	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	30	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value the IC's of internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$.

SWITCHING CHARACTERISTICS TEST WAVEFORM

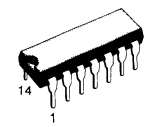


SGS-THOMSON MICROELECTRONICS

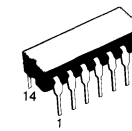
M54HCT7007
M74HCT7007

HEX BUFFER

- LOW POWER DISSIPATION
  $I_{CC} = 1\mu A$ (MAX.) at $T_A = 25°C$
- COMPATIBLE WITH TTL OUTPUTS
  $V_{IH} = 2V$ (MIN) $V_{IL} = 0.8V$ (MAX)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OL}|$ $I_{OL} = 4mA$ (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS07



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

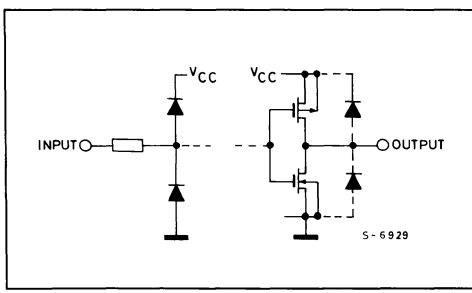
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HCT7007 F1
M74HCT7007 B1N
M74HCT7007 F1
M74HCT7007 C1
M74HCT7007 M1

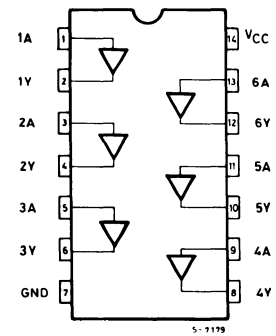
DESCRIPTION

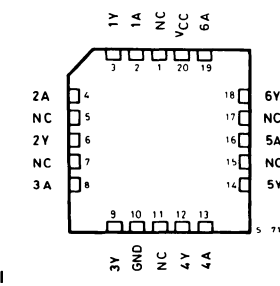
The M54/74HCT7007 is a high speed CMOS HEX BUFFER fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. All inputs are equipped with protection circuits against static discharge and transient excess voltage.
This integrated circuit has totally compatible, input and output characteristic, with standard 54/74 LSTTL logic families.
M54HCT/74HCT devices are designed to directly interface HSC²MOS systems with TTL and NMOS components. These devices are also plug in replacement for LSTTL devices giving a reduction of power consumption.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



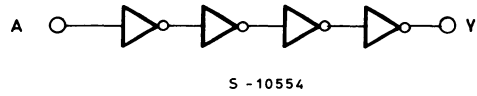
PIN CONNECTIONS (top view)





NC =
No Internal
Connection

CIRCUIT DIAGRAM (Per Circuit)



S - 10554

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current Per Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C
T_L	Lead Temperature 10 sec	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		4.5 to 5.5	V
V_I	DC Input Voltage		0 to V_{CC}	V
V_O	DC Output Voltage		0 to V_{CC}	V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time		0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0	—	—	2.0	—	2.0	—	V
V_{IL}	Low Level Input Voltage	4.5 to 5.5			—	—	0.8	—	0.8	—	0.8	V
V_{OH}	High Level Output Voltage		V_I	I_O								
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	V
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
V_{OL}	Low Level Output Voltage		V_I	I_O								
		4.5	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current	5.5	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	5.5	$V_I = V_{CC}$ or GND		—	—	1.0	—	10	—	20	μA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin $V_{IN} = 2.4V$ Other Input at V_{CC} or GND $I_O = 0$		—	—	2.0	—	2.9	—	3.0	mA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

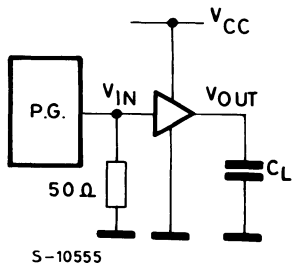
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		14	22	ns

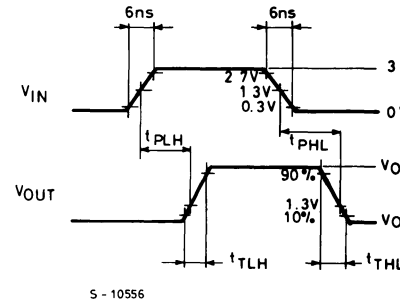
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH}	Output Transition Time	4.5		—	8	15	—	19	—	22	ns
t_{PLH} t_{PHL}	Propagation Delay Time	4.5		—	16	26	—	33	—	39	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	28	—	—	—	—	—	pF

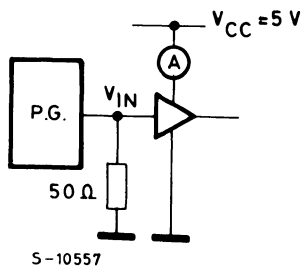
Note (*) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (Refer to Test circuit).
Average operating current can be obtained from the equation: $I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per Buffer)

SWITCHING CHARACTERISTICS TEST CIRCUIT

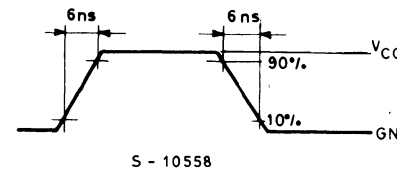




TEST CIRCUIT I_{CC} (Opr.)

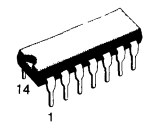


INPUT WAVEFORM

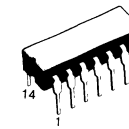


QUAD EXCLUSIVE NOR GATE

- HIGH SPEED
  t_{PD} = 12 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS7266



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC7266 F1
M74HC7266 B1N
M74HC7266 F1
M74HC7266 C1
M74HC7266 M1

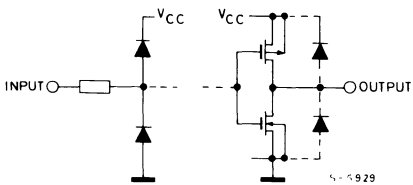
DESCRIPTION

The M54/74HC7266 is a high speed CMOS QUAD EXCLUSIVE NOR GATE fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

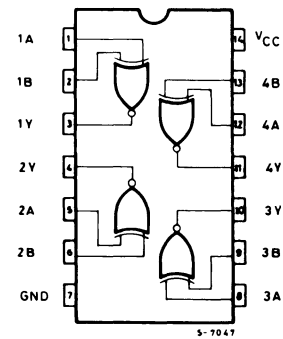
Input and output buffers ensure high noise immunity and stable outputs.

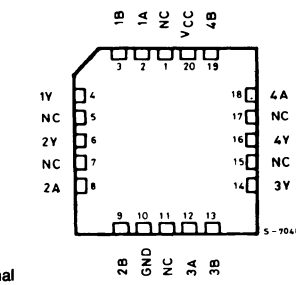
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



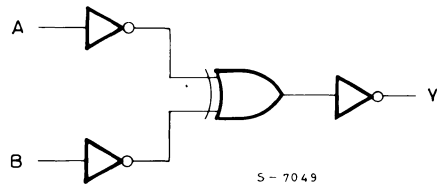
PIN CONNECTIONS (top view)





NC =
No Internal
Connection

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series Operating Temperature 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	1	—	10	—	20	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

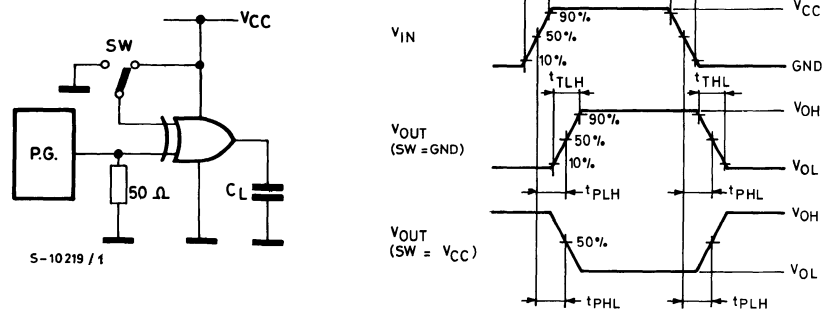
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time		12	19	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

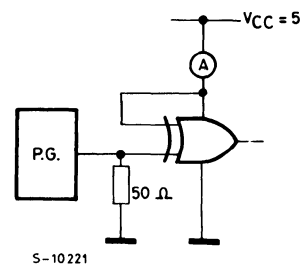
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0		—	22	75	—	90	—	110	ns
		4.5		—	8	15	—	18	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	52	115	—	145	—	173	ns
		4.5		—	13	23	—	29	—	35	
		6.0		—	11	20	—	25	—	29	
C_{IN}	Input Capacitance			—	5	10	—	10	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance			—	34	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate).

SWITCHING CHARACTERISTICS TEST CIRCUIT



TEST CIRCUIT I_{CC} (Opr.)



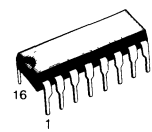
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

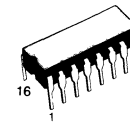
M54/74HC7292
M54/74HC7294

PROGRAMMABLE DIVIDER/TIMER

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS292/294



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HCXXXX F1
M74HCXXXX B1N
M74HCXXXX F1
M74HCXXXX C1
M74HCXXXX M1

DESCRIPTION

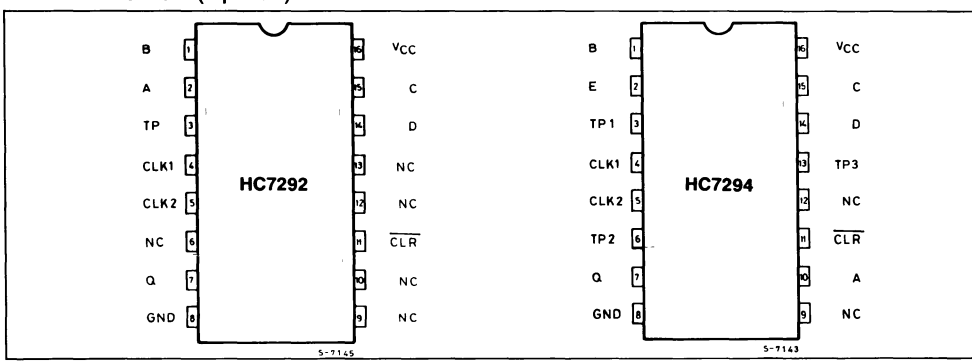
The 54/74HC7292 and 54/74HC7294 are high speed CMOS PROGRAMMABLE DIVIDER/TIMER fabricated with silicon C²MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
These devices are programmable frequency divider. Both types have two clock inputs, either one may be used for clock gating. (See the function table). The HC7292 can divide from 2^2 to 2^{31}, and the HC7294 can divide from 2^2 to 2^{15}. Both types feature an active-low clear input to initialize the state of all flip-flops. To facilitate incoming inspection, test points are provided. (TP1, TP2 and TP3 on the HC7292 and TP on the HC7294). All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Note: HC7292 and HC7294 all have outputs "Totem pole"

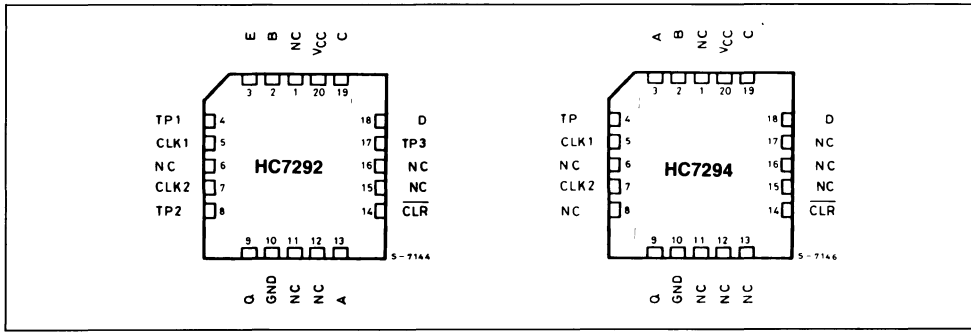
TRUTH TABLE

$\overline{CLEAR}$	CLOCK1	CLOCK2	Q OUTPUT MODE
L	X	X	CLEARED TO L
H		L	UP COUNT
H	L		
H	H	X	NO CHANGE
H	X	H	

PIN CONNECTION (top view)



CHIP CARRIER



ABSOLUTE MAXIMUM RATINGS

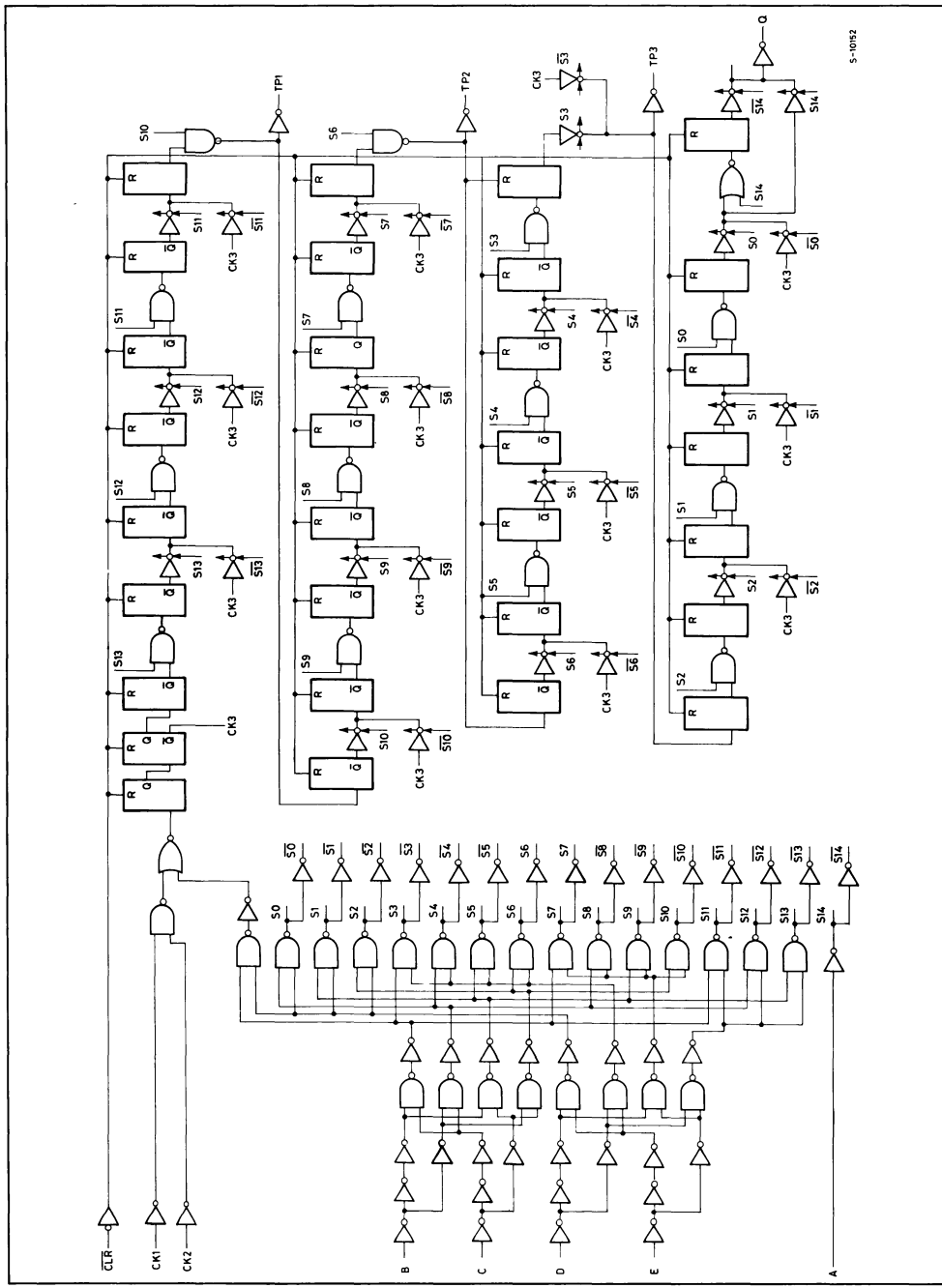
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

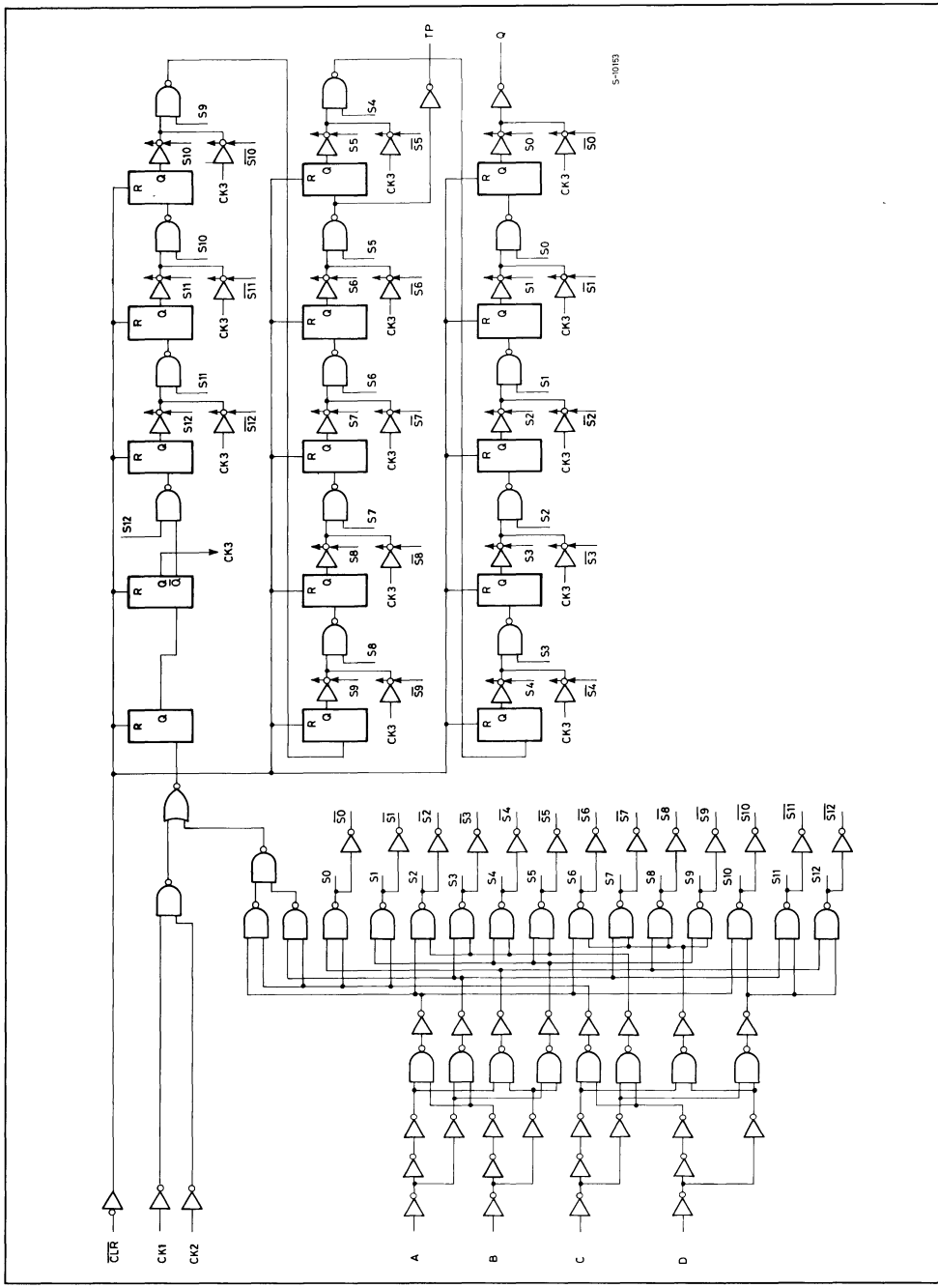
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limit		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series Operating Temperature 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

LOGIC DIAGRAM (HC7292)



LOGIC DIAGRAM (HC7294)



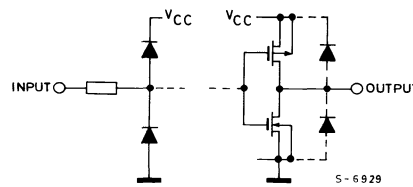
FUNCTION TABLE (HC7292)

PROGRAMMING INPUTS					FREQUENCY DIVISION							
					Q		TP1		TP2		TP3	
E	D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	L	2^2	4	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	L	H	H	2^3	8	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	L	L	2^4	16	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	L	H	2^5	32	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	H	L	2^6	64	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	H	H	2^7	128	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	H	L	L	L	2^8	256	2^9	512	2^{17}	131,072	2^2	4
L	H	L	L	H	2^9	512	2^9	512	2^{17}	131,072	2^2	4
L	H	L	H	L	2^{10}	1,024	2^9	512	2^{17}	131,072	2^4	16
L	H	L	H	H	2^{11}	2,048	2^9	512	2^{17}	131,072	2^2	16
L	H	H	L	L	2^{12}	4,096	2^9	512	2^{17}	131,072	2^6	64
L	H	H	L	H	2^{13}	8,192	2^9	512	2^{17}	131,072	2^6	64
L	H	H	H	L	2^{14}	16,384	2^9	512	Disabled Low		2^8	256
L	H	H	H	H	2^{15}	32,768	2^9	512	Disabled Low		2^8	256
H	L	L	L	L	2^{16}	65,536	2^9	512	2^3	8	2^{10}	1,024
H	L	L	L	H	2^{17}	131,072	2^9	512	2^3	8	2^{10}	1,024
H	L	L	H	L	2^{18}	262,144	2^9	512	2^5	32	2^{12}	4,096
H	L	L	H	H	2^{19}	524,288	2^9	512	2^5	32	2^{12}	4,096
H	L	H	L	L	2^{20}	1,048,576	2^9	512	2^7	128	2^{14}	16,384
H	L	H	L	H	2^{21}	2,097,152	2^9	512	2^7	128	2^{14}	16,384
H	L	H	H	L	2^{22}	4,194,304	Disabled Low		2^9	512	2^{16}	65,536
H	L	H	H	H	2^{23}	8,388,608	Disabled Low		2^9	512	2^{16}	65,536
H	H	L	L	L	2^{24}	16,777,216	2^3	8	2^{11}	2,048	2^{18}	262,144
H	H	L	L	H	2^{25}	33,554,432	2^3	8	2^{11}	2,048	2^{18}	262,144
H	H	L	H	L	2^{26}	67,108,864	2^5	32	2^{13}	8,192	2^{20}	1,048,576
H	H	L	H	H	2^{27}	134,217,728	2^5	32	2^{13}	8,192	2^{20}	1,048,576
H	H	H	L	L	2^{28}	268,435,456	2^7	128	2^{15}	32,768	2^{22}	4,194,304
H	H	H	L	H	2^{29}	536,870,912	2^7	128	2^{15}	32,768	2^{22}	4,194,304
H	H	H	H	L	2^{30}	1,073,741,824	2^9	512	2^{17}	131,072	2^{24}	16,777,216
H	H	H	H	H	2^{31}	2,147,483,648	2^9	512	2^{17}	131,072	2^{24}	16,777,216

FUNCTION TABLE (HC7294)

PROGRAMMING INPUTS				FREQUENCY DIVISION			
				Q		TP	
D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit
L	L	H	L	2^2	4	2^9	512
L	L	H	H	2^3	8	2^9	512
L	H	L	L	2^4	16	2^9	512
L	H	L	H	2^5	32	2^9	512
L	H	H	L	2^6	64	2^9	512
L	H	H	H	2^7	128	Disabled Low	
H	L	L	L	2^8	256	2^2	4
H	L	L	H	2^9	512	2^3	8
H	L	H	L	2^{10}	1,024	2^4	16
H	L	H	H	2^{11}	2,048	2^5	32
H	H	L	L	2^{12}	4,096	2^6	64
H	H	L	H	2^{13}	8,192	2^7	128
H	H	H	L	2^{14}	16,384	2^8	256
H	H	H	H	2^{15}	32,768	2^9	512

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter		54HC and 74HC			Unit
			Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time Q OUTPUT			4	8	ns
t_{TLH} t_{THL}	Output Transition Time TP OUTPUTS			29	45	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK-Q)	HC7292		58	89	ns
		HC7294		53	81	
t_{PHL}	Propagation Delay Time (CLEAR-Q)	HC7292		49	75	ns
		HC7294		45	69	
f_{MAX}	Maximum Clock Frequency	HC7292	28	56		MHz
		HC7294	35	61		

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

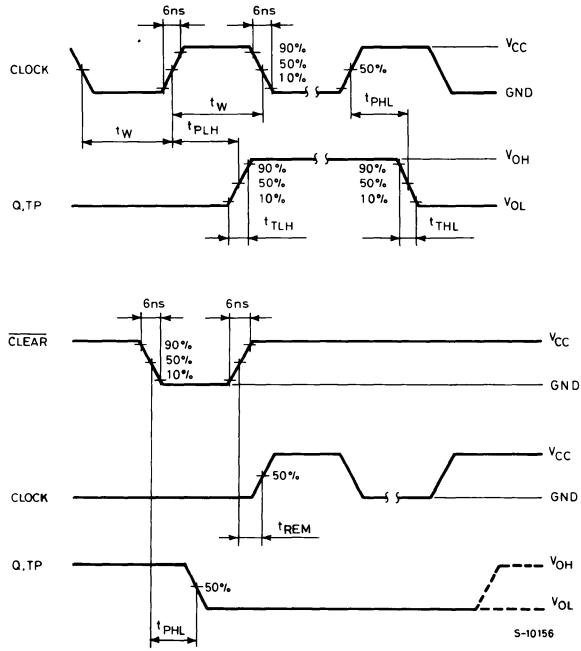
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time Q OUTPUT	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{TLH} t_{THL}	Output Transition Time TP OUTPUT	2.0		—	132	255	—	320		385	ns
		4.5		—	33	51	—	64		77	
		6.0		—	28	43	—	55		65	
t_{PLH} t_{PHL}	Propagation Delay Time (CK-Q)*	2.0	B = "H"	—	264	500	—	635		750	ns
		4.5		—	66	100	—	127		150	
		6.0	A = C = D = E = "L"	—	56	85	—	110		127	
t_{PLH} t_{PHL}	Propagation Delay Time (CK-Q)**	2.0	B = "H"	—	236	455	—	571		676	ns
		4.5		—	59	91	—	115		136	
		6.0	A = C = D = E = "L"	—	50	77	—	100		115	
t_{PHL}	Propagation Delay Time ($\overline{CLR}$-Q)*	2.0		—	224	425	—	535		640	ns
		4.5		—	56	85	—	107		128	
		6.0		—	48	73	—	92		109	
t_{PHL}	Propagation Delay Time ($\overline{CLR}$-Q)**	2.0		—	204	390	—	490		585	ns
		4.5		—	51	78	—	98		117	
		6.0		—	43	67	—	84		99	
f_{MAX}	Maximum Clock Frequency*	2.0		5	13	—	4	—	3.4	—	MHz
		4.5		25	51	—	20	—	17	—	
		6.0		29	60	—	24	—	20	—	
f_{MAX}	Maximum Clock Frequency**	2.0		6	14	—	5	—	4.2	—	MHz
		4.5		32	55	—	26	—	21	—	
		6.0		38	65	—	31	—	25	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width CK)	2.0		—	36	100	—	125		150	ns
		4.5		—	9	20	—	25		30	
		6.0		—	8	17	—	21		26	
$t_{W(L)}$	Minimum Pulse Width CLEAR*	2.0		—	60	150	—	190		225	ns
		4.5		—	15	30	—	38		45	
		6.0		—	13	26	—	33		38	
$t_{W(L)}$	Minimum Pulse Width CLEAR**	2.0		—	72	175	—	220		265	ns
		4.5		—	18	35	—	44		53	
		6.0		—	15	30	—	37		45	
t_{REM}	Minimum Removal Time $\overline{CLEAR}$	2.0		—	—	25	—	30	—	40	ns
		4.5		—	—	5	—	6	—	8	
		6.0		—	—	5	—	6	—	7	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance		M54/74HC7292	—	22	—	—	—			pF
			M54/74HC7294	—	23	—	—	—			

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

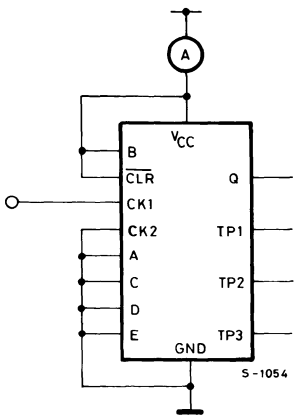
* M54/74HC7292
** M54/74HC7294

SWITCHING CHARACTERISTICS TEST WAVEFORM

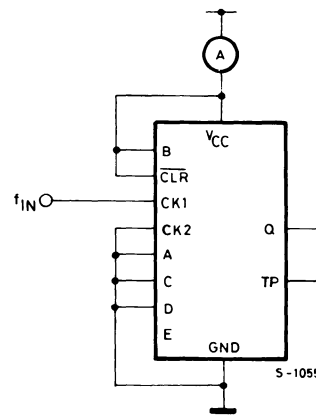


TEST CIRCUIT I_{CC} (Opr.)

HC792



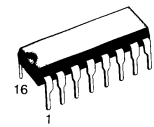
HC794



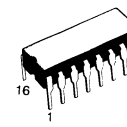
INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

8 STAGE PRESETTABLE SYNCHRONOUS DOWN COUNTERS

- HIGH SPEED
  f_{MAX} = 34 MHz (Typ) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 40102B/40103B



B1N
Plastic Package



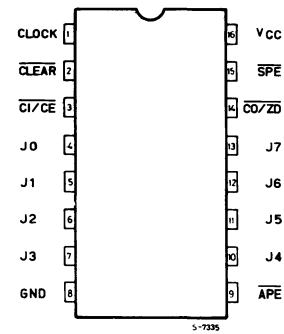
F1
Ceramic Frit Seal Package

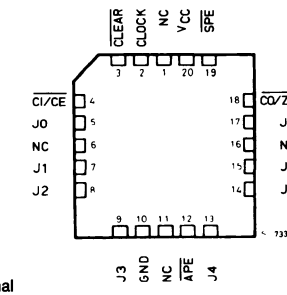
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HCXXXX F1
M74HCXXXX B1N
M74HCXXXX F1
M74HCXXXX C1
M74HCXXXX M1

PIN CONNECTION (top view)





NC = No Internal Connection

DESCRIPTION

The M54/74HC40102/40103 are high speed CMOS 8-STAGE PRESETTABLE SYNCHRONOUS DOWN COUNTERS fabricated with silicon gate C²MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The HC40102, and HC40103 consist of an 8-stage synchronous down counter with a single output which is active when the internal count is zero. The HC40102 is configured as two cascaded 4-bit BCD counters, and the HC40103 contains a single 8-bit binary counter. Each type has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the CARRY-OUT/ZERO-DETECT output are active-low logic. In normal operation, the counter is decremented by one count on each positive transition of the CLOCK. Counting is inhibited when the CARRY-IN/COUNTER ENABLE ($\overline{CI/CE}$) input is high. The CARRY-OUT/ZERO-DETECT ($\overline{CO/ZD}$) output goes low when the count reaches zero if the $\overline{CI/CE}$ input is low, and remains low for one full clock period. When the SYNCHRONOUS PRESET-ENABLE (SPE) input is low, data at the J input is clocked into the counter on the next positive clock transition regardless of the state of the $\overline{CI/CE}$ input.

DESCRIPTION (Continued)

When the ASYNCHRONOUS PRESET-ENABLE ($\overline{APE}$) input is low, data at the J inputs is asynchronously forced into the counter regardless of the state of the $\overline{SPE}$, $\overline{CI/CE}$, or CLOCK inputs. J Inputs J0-J7 represent two 4-bit BCD words for the HC40102 and a single 8-bit binary word for the HC40103. When the CLEAR ($\overline{CLR}$ input is low, the counter is asynchronously cleared to its maximum count ($99_{10}$for the HC40102 and 255_{10} for the HC40103 regardless of the state of any other input.

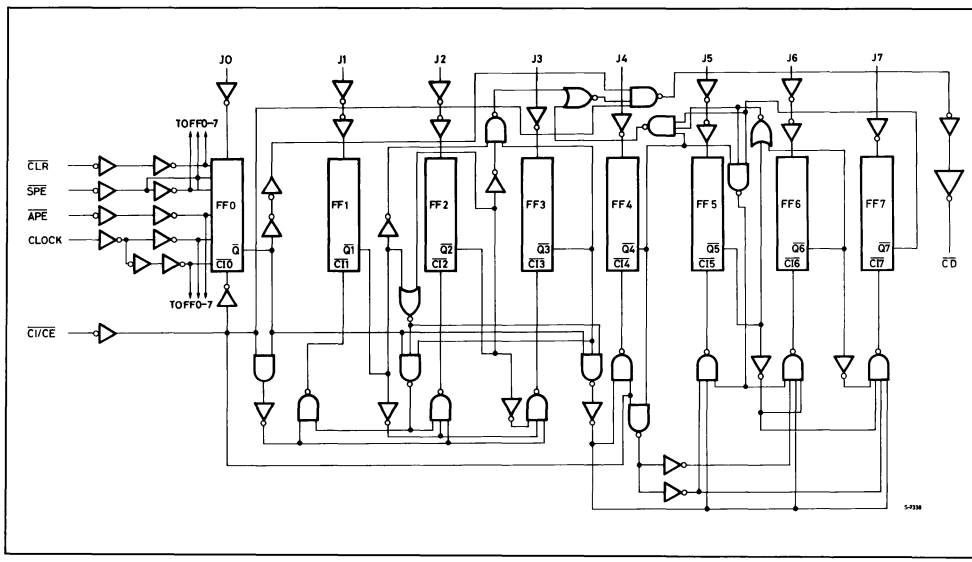
The precedence relationship between control input is indicated in the truth table. If all control inputs are high at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 100 or 256 clock pulses long. The HC40102 and HC40103 may be cascaded using the $\overline{CI/CE}$ input and the $\overline{CO/ZD}$ output, in either a synchronous or ripple mode. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

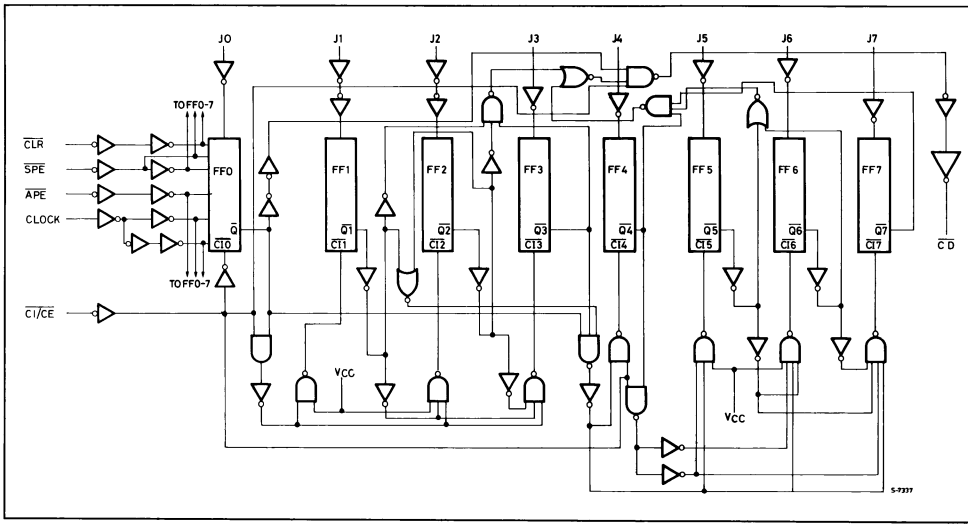
CONTROL INPUTS				MODE	FUNCTIONAL DESCRIPTION
$\overline{CLEAR}$	$\overline{APE}$	$\overline{SPE}$	$\overline{CI/CE}$		
H	H	H	H	COUNT INHIBIT	EVEN IF CLOCK IS GIVEN, NO COUNT IS MADE.
H	H	H	L	REGULAR COUNT	DOWN COUNT AT RISING EDGE OF CLOCK.
H	H	L	X	SYNCHRONOUS PRESET	DATA OF PI TERMINAL IS PRESET AT RISING EDGE OF CLOCK
H	L	X	X	ASYNCHRONOUS PRESET	DATA OF PI TERMINAL IS ASYNCHRONOUSLY PRESET TO CLOCK
L	X	X	X	CLEAR	COUNTER IS SET TO MAXIMUM COUNT.

X. DON'T CARE — MAXIMUM COUNT: "99" FOR HC40102 AND "255" FOR HC40103

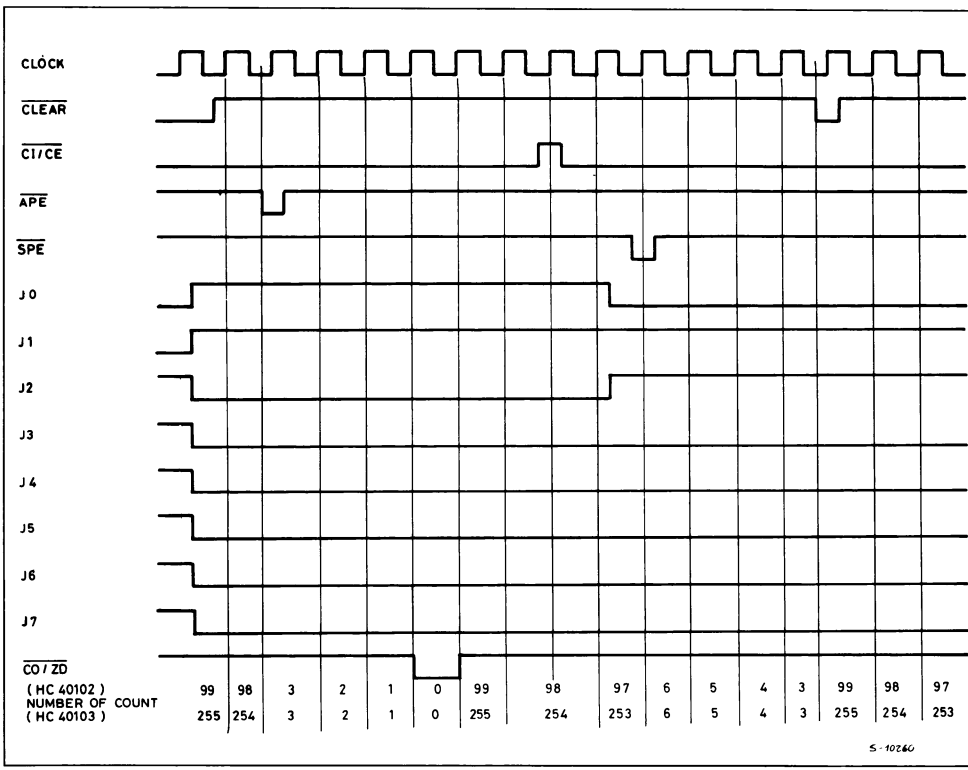
LOGIC DIAGRAM (HC40102)



LOGIC DIAGRAM (HC40103)



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

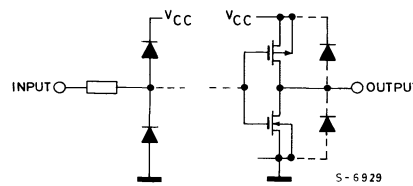
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW:≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC}	2 V 4.5V 6 V	0 to 1000 0 to 500 0 to 400	ns

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time CK-$\overline{CO}$/ZO		27	42	ns
t_{PHL}	Propagation Delay Time ($\overline{APE}$-$\overline{CO}$/ZD)		34	53	ns
t_{PHL}	Propagation Delay Time ($\overline{CL}$-$\overline{CO}$/ZD)		27	42	ns
t_{PHL}	Propagation Delay Time ($\overline{CI}$/$\overline{CE}$-$\overline{CO}$/ZO)		11	18	ns
f_{MAX}	Maximum Clock Frequency	22	34		MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	
		4.5		—	8	15	—	19		22	ns
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - CO/ZD)	2.0		—	128	245	—	305		370	
		4.5		—	32	49	—	61		74	ns
		6.0		—	27	42	—	52		63	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{APE}$ - $\overline{CO/ZD}$)	2.0		—	156	300	—	380		450	
		4.5		—	39	60	—	76		90	ns
		6.0		—	33	52	—	66		76	
t_{PLH}	Propagation Delay Time ($\overline{CL}$ - $\overline{CO/ZD}$)	2.0		—	124	240	—	300		360	
		4.5		—	31	48	—	60		72	ns
		6.0		—	27	41	—	51		61	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CI/CE}$ - $\overline{CO/ZO}$)	2.0		—	56	115	—	145		175	
		4.5		—	14	23	—	29		35	ns
		6.0		—	12	20	—	25		30	
f_{MAX}	Maximum Clock Frequency	2.0		4	8	—	3.2	—	2.6	—	
		4.5		20	31	—	16	—	13	—	MHz
		6.0		24	36	—	18	—	15	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	95		110	
		4.5		—	8	15	—	19		22	ns
		6.0		—	7	13	—	16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CL}$, $\overline{APE}$)	2.0		—	30	75	—	95		110	
		4.5		—	8	15	—	19		22	ns
		6.0		—	7	13	—	16		19	
t_s	Minimum Set-up Time ($\overline{SPE}$ - CK)	2.0		—	30	75	—	95		110	
		4.5		—	7	15	—	19		22	ns
		6.0		—	6	13	—	16		19	
t_s	Minimum Set-up Time ($\overline{CI/CE}$ - CK)	2.0		—	56	125	—	155	—	190	
		4.5		—	14	25	—	31	—	38	ns
		6.0		—	12	21	—	26	—	32	
t_s	Minimum Set up Time (Jn-CK)	2.0		—	30	75	—	95	—	110	
		4.5		—	8	15	—	19	—	22	ns
		6.0		—	7	13	—	16	—	19	
t_h	Minimum Hold Time (All inputs)	2.0		—	—	5	—	5		5	
		4.5		—	—	5	—	5		5	ns
		6.0		—	—	5	—	5		5	
t_{REM}	Minimum Removal Time ($\overline{CL}$ - $\overline{APE}$)	2.0		—	20	75	—	95		110	
		4.5		—	5	15	—	19		22	ns
		6.0		—	4	13	—	16		19	
t_s	Minimum Set-up Time (Jn $\overline{APE}$)	2.0		—	30	75	—	95		110	
		4.5		—	8	15	—	19		22	ns
		6.0		—	7	13	—	16		19	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance		M54/74HC40102	—	110	—	—	—			pF
			M54/74HC40103	—	128	—	—	—			

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the following equation.
I_{CC} (Opr.)•C_{PD}•V_{CC}•f_{IN} + I_{CC}

FUNCTIONAL DESCRIPTION

The HC40102 and HC40103 are 8-stage presettable synchronous down counters. Carry Out/Zero Detect ($\overline{CO/ZD}$) is output at the "L" level for the period of 1 bit when the readout becomes "0". The HC40102 adopts binary coded decimal notation, making setting up to 99 counts possible. While the HC40103 adopts 8-bit binary counter and can set up to 255 counts.

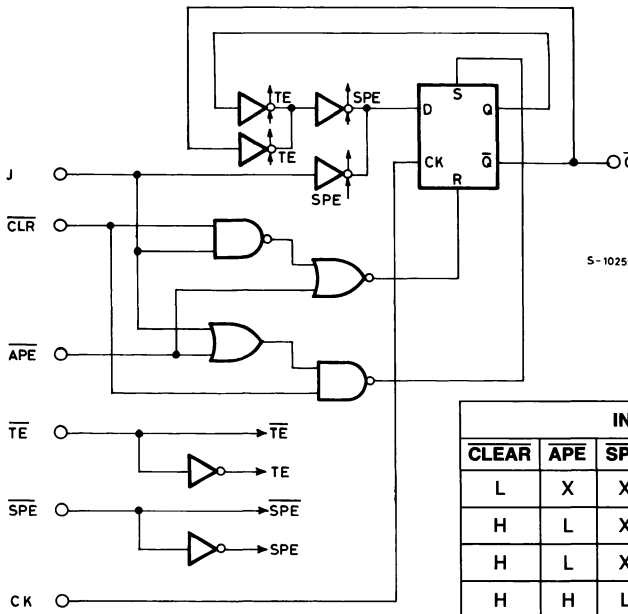
Count operation

At the "H" level of control input of $\overline{CLEAR}$, $\overline{SPE}$ and $\overline{APE}$, the counter carriers out down count operation one by one at the rise of pulse given to CLOCK input. Count operation can be inhibited by setting Carry Input/Clock Enable $\overline{CI/CE}$ to the "H" level.
$\overline{CO/ZD}$ is output at the "L" level when the readout becomes "0", but is not output even if the readout becomes "0" when $\overline{CI/CE}$ is at the "H" level, thus maintaining the "H" level.
Synchronous cascade operation can be carried out by using $\overline{CI/CE}$ input and $\overline{CO/ZD}$ output.

The contents of count jump to maximum count (99 for the HC40102 and 225 for the HC40103) if clock is given when the readout is "0". Therefore, operation of 100-frequency division and that of 256-frequency division are carried out for the HC40102 and HC40103, respectively, when clock input alone is given without various kinds of preset operation.

Preset operation and reset operation

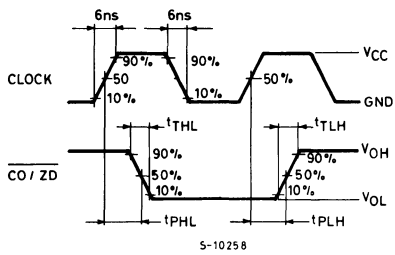
When Clear ($\overline{CLEAR}$) input is set to the "L" level, the readout is set to the maximum count independetly of other inputs. When Asynchronous Preset Enable ($\overline{APE}$) input is set to the "L" level, readouts given on J0 to J7 can be preset asynchronously to counter independently of inputs other than $\overline{CLEAR}$ input. When Synchronous Preset Enable ($\overline{SPE}$) is set to the "L" level, the readouts given on J0 to J7 can be preset to counter synchronously with the rise of clock.
As to these operation modes, refer to the truth table.



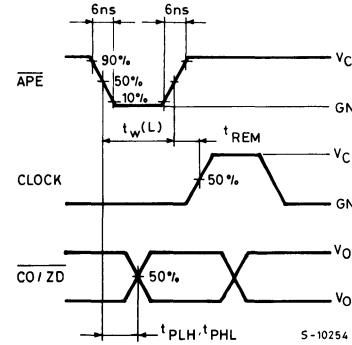
INPUT						OUTPUT
$\overline{CLEAR}$	$\overline{APE}$	$\overline{SPE}$	J	$\overline{TE}$	CLOCK	$\overline{Q}_n+1$
L	X	X	X	X	X	L
H	L	X	L	X	X	L
H	L	X	H	X	X	H
H	H	L	L	X	↑	L
H	H	L	H	X	↑	H
H	H	L	X	X	↓	$\overline{Q}_n$
H	H	H	X	L	↑	Q_n
H	H	H	X	H	X	$\overline{Q}_n$

SWITCHING CHARACTERISTICS TEST WAVEFORM

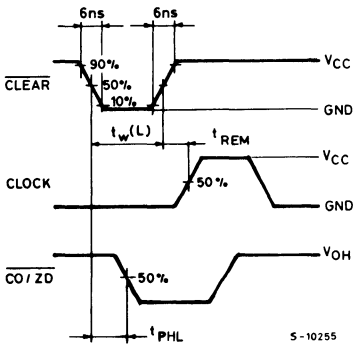
WAVEFORM 1



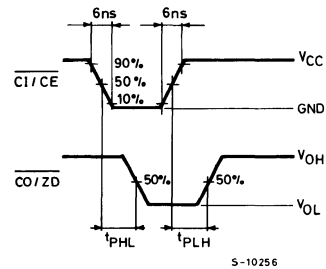
WAVEFORM 2



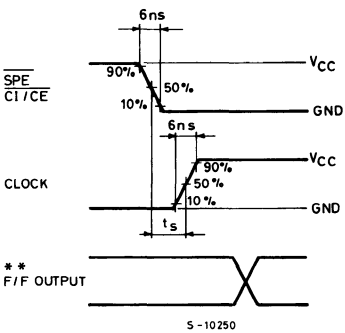
WAVEFORM 3



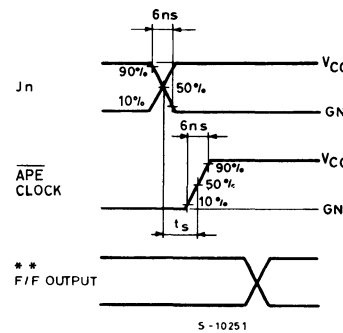
WAVEFORM 4



WAVEFORM 5

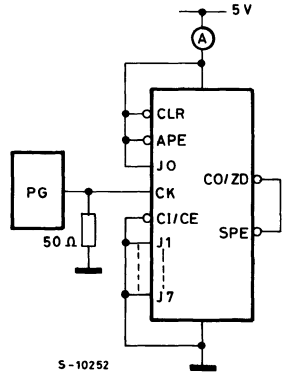


WAVEFORM 6



(** F/F output is internal signal of IC)

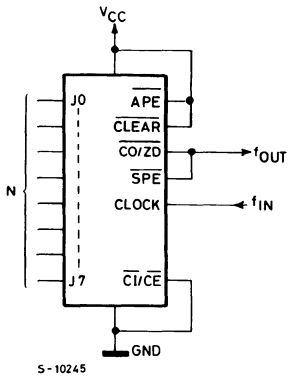
TEST CIRCUIT I_{CC} (Opr.)



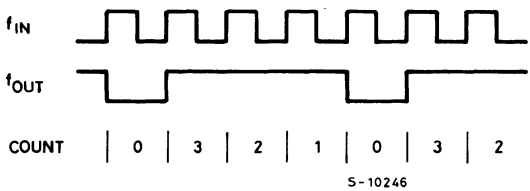
INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

EXAMPLE OF TYPICAL APPLICATION

PROGRAMMABLE DIVIDE-BY-N COUNTER

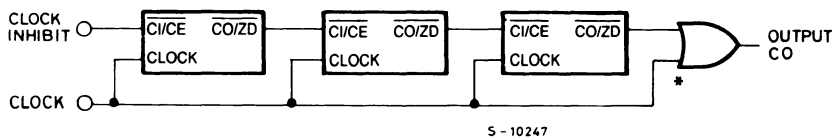


- $f_{OUT} = \frac{f_{IN}}{N+1}$
- Timing chart when N = "3" (JO, J1 = V_{CC}, J2 ~ J7 = GND)



- HC40102 . . 1/2 to 1/100 are dividable
- HC40103 .... 1/2 to 1/256 are dividable

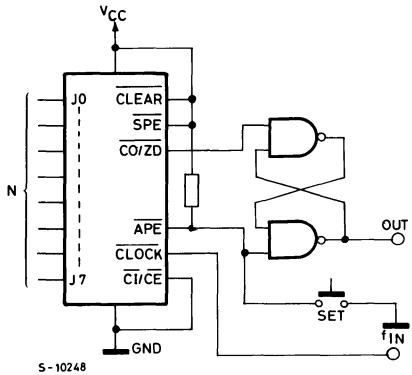
PARALLEL CARRY CASCADING

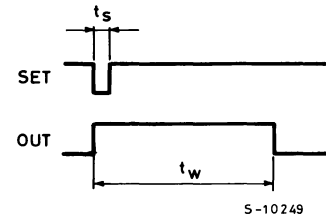


* At synchronous cascade connection, huzzerd occurs at C0 output after its second stage when digit place changes, due to delay arrival. Therefore, take gate from HC32 or the like, not from C0 output at the rear stage directly.

EXAMPLE OF TYPICAL APPLICATION (Continued)

PROGRAMMABLE TIMER



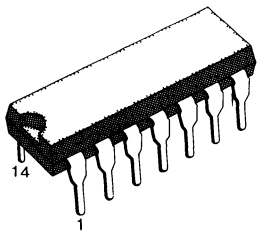


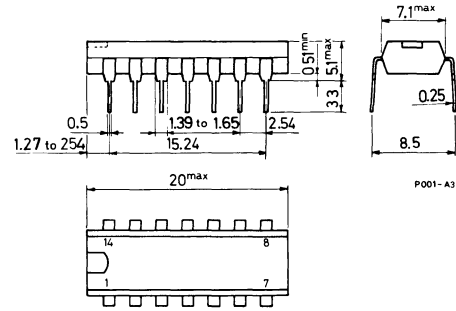
$$t_W = \left(\frac{N}{f_{IN}} + t_S\right)$$

Note: The above formula does not take into account the phase of clock input. Therefore, the real pulse width is the distance between the above formula-$1/f_{IN}$ ~ the above formula.

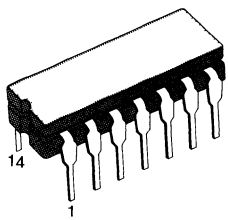
PACKAGES

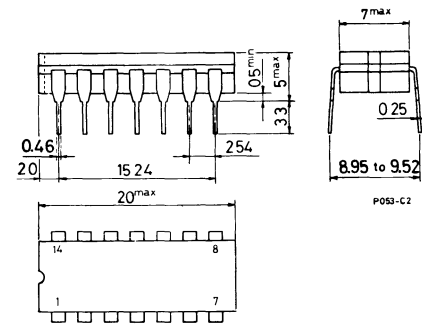
14-LEAD PLASTIC DIP





14-LEAD CERAMIC DIP





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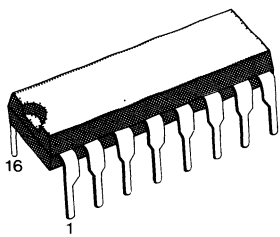

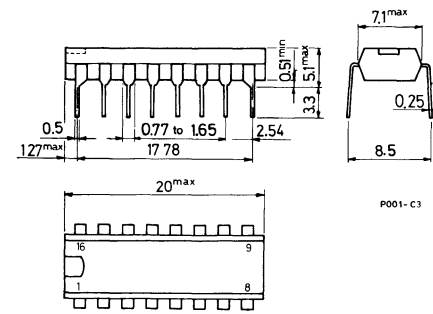

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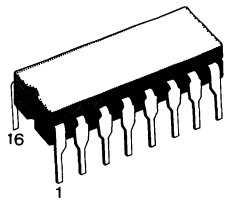

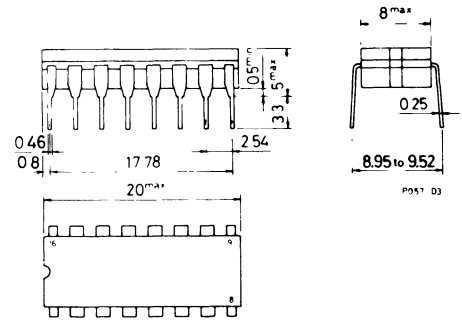

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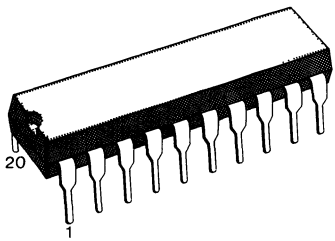

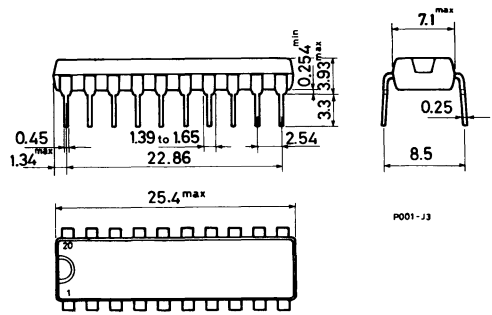

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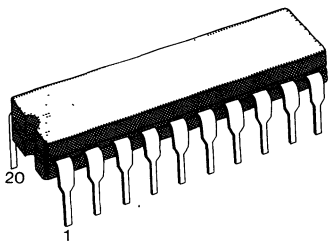
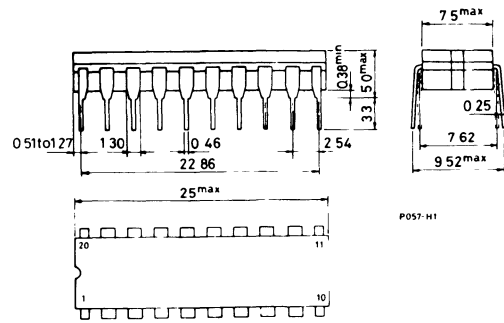
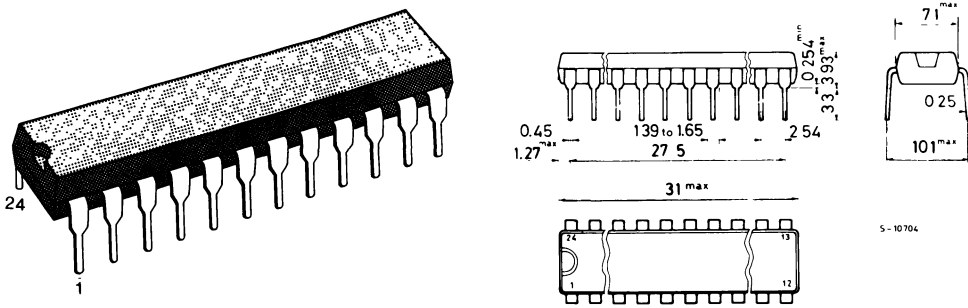
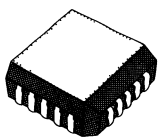


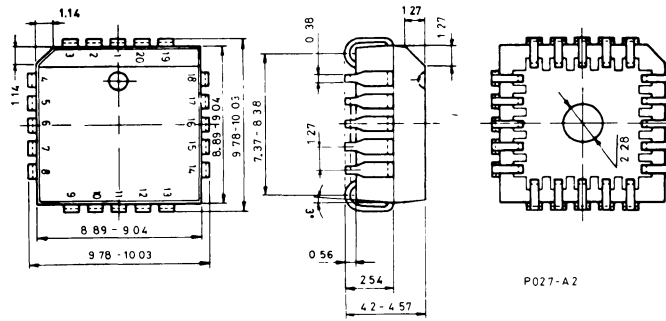


24-LEAD PLASTIC DIP (FOR 24-LEAD CERAMIC DIP CONTACT SGS-THOMSON SALES OFFICE)

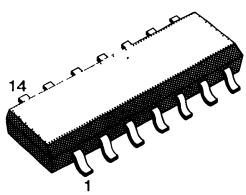


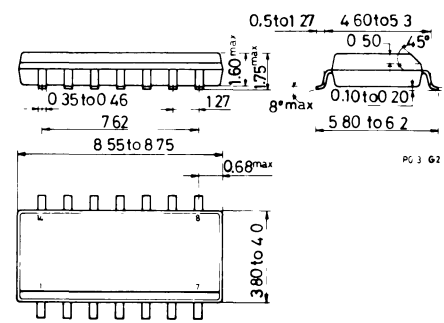
CHIP CARRIER 20 LEAD PLASTIC





14-LEAD PLASTIC DIP MICROPACKAGE





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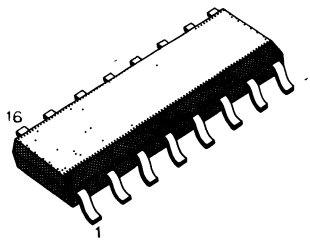

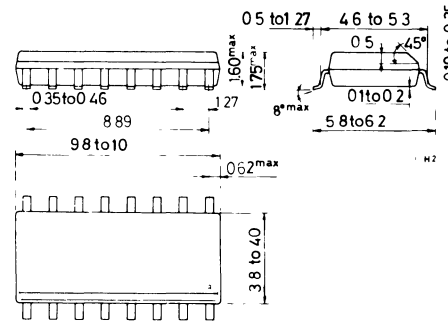

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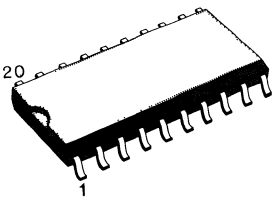

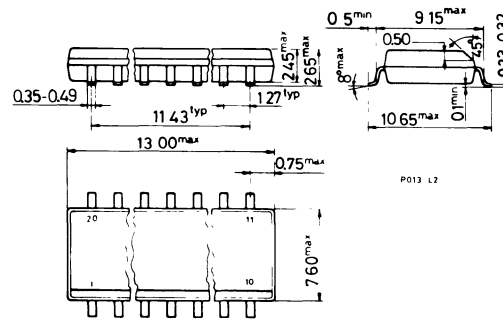

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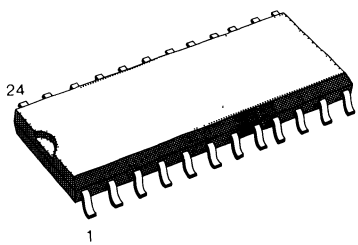
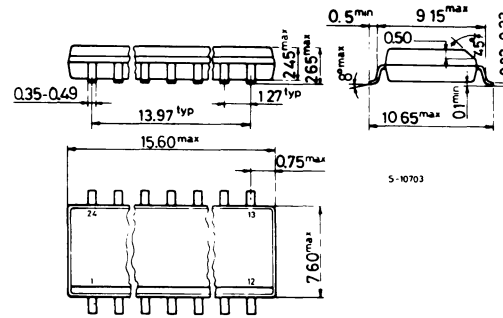




SURFACE MOUNTED

One solution to the important problem of PCB minimization, is that of using surface mounted components. Integrated circuits in SO (Small Outline) packages are made up of standard chips mounted in very small plastic packages.
The advantage given by using these devices are:

PCB Reduction

This is by far the most important advantage since the reduction of PCB size varies from 40% to 60% in comparison with standard boards.

Assembly cost reduction

SO Devices require no preliminary operation such as drilling prior to mounting and can therefore be easily utilized in fully automatic equipment.

Increasing reliability

The following characteristics lead to a higher reliability with respect to the standard packaged counter parts:

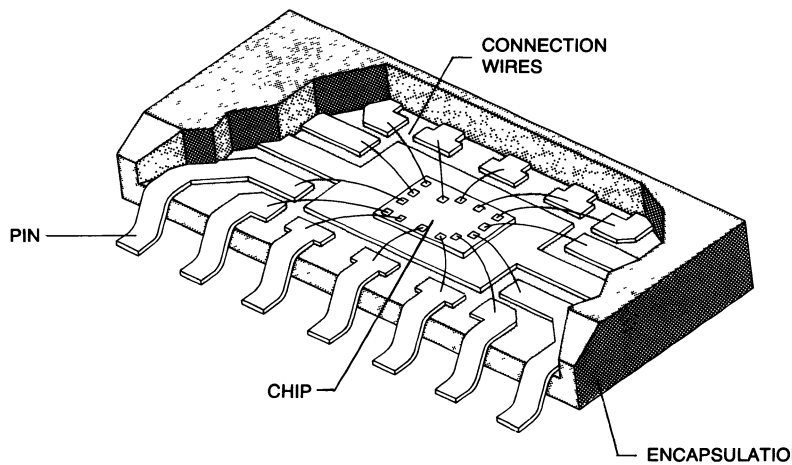
- Fully automatic mounting
- Reduction in the number of PCB's and in the number of interconnections between the boards (comparing a fixed number of device)
- The high density of components mounted on the board makes it more stable thermally.

Noise reduction and improved frequency response

The reduction in length of the bonding wires between the leads and the silicon guarantees a more homogeneous propagation delay between the external pins, with respect to the standard type.

Simplified assembly

The tolerance in positioning of SO packages on PCB's is less critical than the positioning of standard DIP packages.
This makes a considerable simplification in assembly.



RELIABILITY REPORT

THE PRODUCT TECHNOLOGY

The sharp improvement in performance of the 74HC family, in comparison to the standard 4000B family, is mainly due to the 1980's technological progress, and to a systematic layout philosophy, high-speed-oriented.
The fabrication process exploits

- dieletric isolation:
  for higher density and lower parasitic capacitances (speed)
- photolitography scaling down
- tighter doping process control
- silicon gate technology

Even if some of these steps are well known to the semiconductor industry, their unique combination into an effective and reliable process is the key to the 74HC family success.
These circuits are typically employed in professional applications where quality and reliability are a major feature of the set.
A "no compromise" strategy is adopted at each stage of production from development to preproduction, to full production stage; quality and reliability are always priority targets.

We have envisaged 3 main check points:
1) Project validation at design stage
2) Prototypes qualification
3) Final product qualification

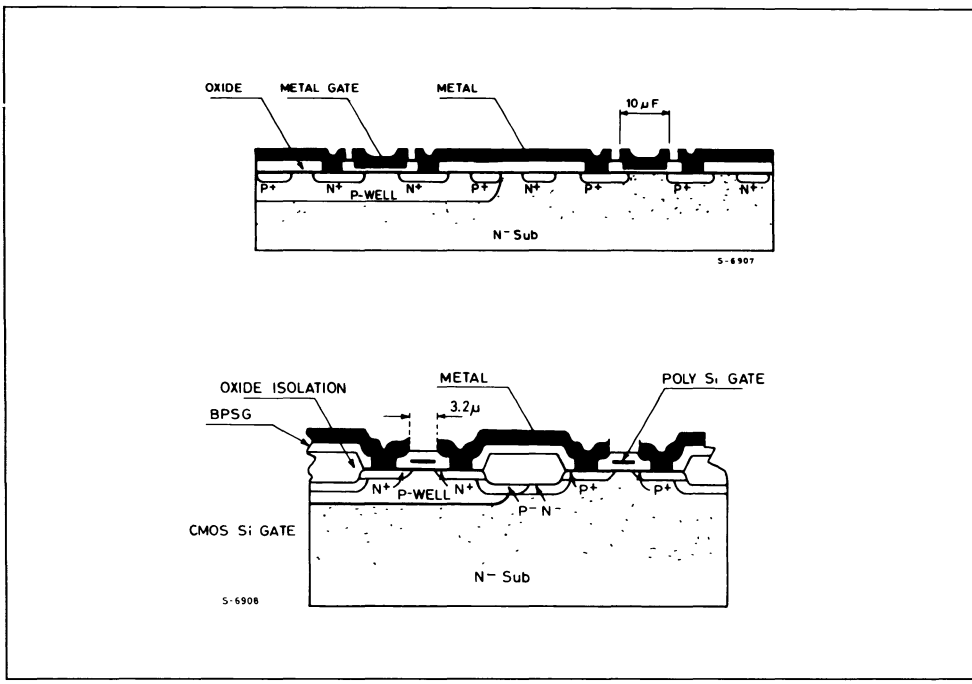
At design stage CAD tools (for simulation and design rules check) and quality council meeting are used for continuous monitoring of quality aspects of the circuits.
Qualification of the prototypes is performed by means of an agreed and fixed set of tests for reliability and product characterisation.

The final outputs are
a) Circuit characterisation manual
b) Circuit qualification report
c) Failure analysis reports (when needed)

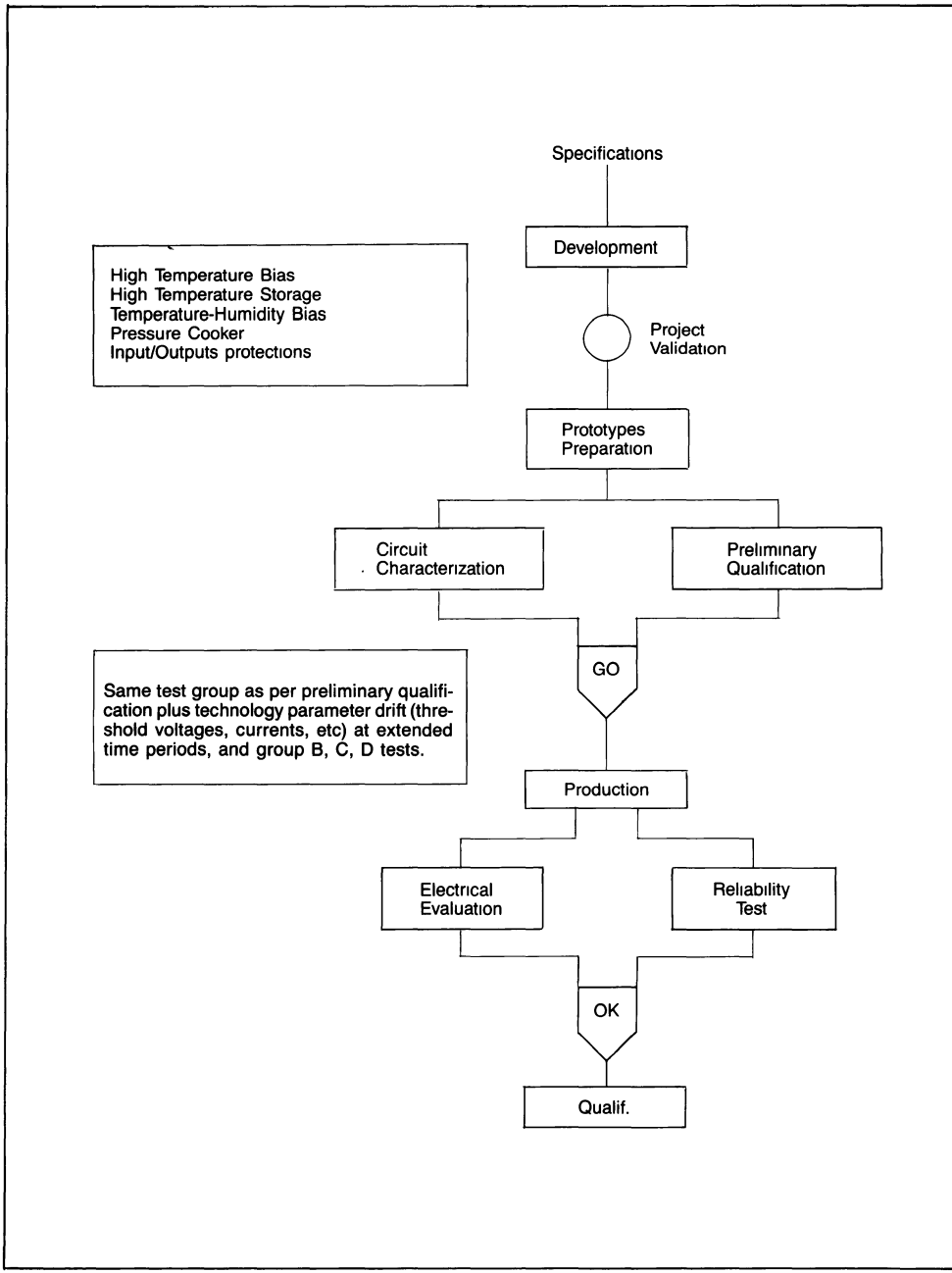
See next page for operative data and flow.

Finally product qualification at production stage is obtained with a set of reliability tests mainly based upon
d) Accelerated temperature life test
e) High temperature storage
f) Temperature-humidity accelerated conditions
g) High voltage stresses (inputs-outputs protection, latch-up)

Both circuit and process parameters are monitored.



PRODUCT QUALIFICATION FLOW CHART



DOUBLE LAYER GLASS PASSIVATION

SGS-THOMSON HSCMOS family uses a double layer P-VAPOX and Si_3N_4 passivation that gives improved protection to die encapsulated in plastic packages.

PROCESS DESCRIPTION

The process consists of a two layer film of P-Vapox (phosphorus doped silicon oxide) and Si_3N_4 (silicon nitride), obtained by two different masking and etching steps to avoid defects caused by lack of dielectric integrity.

The process gives good metal step coverage together with PECVD (Plasma Enhanced Chemical Vapox Deposition) to avoid cracking near metal edge and possible hillocks defects.

The double layer enable us, by means of an appropriate oversize either at the boundaries of the die side or at the bonding pad side, to ensure full sealing of the underlying P-Vapox layer.

This prevents the layer from being exposed to moisture coming from the package. Thus the probability of metal corrosion on the bonding pad due to phosphoric acid is drastically reduced.

As a result the die is provided with a very good humidity immunity.

PROCESS FLOW

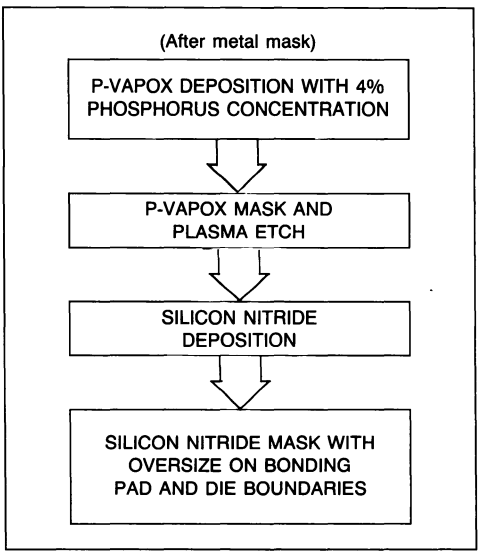


Fig. 1 - Typical microsection of an HSCMOS device with nitride passivation.

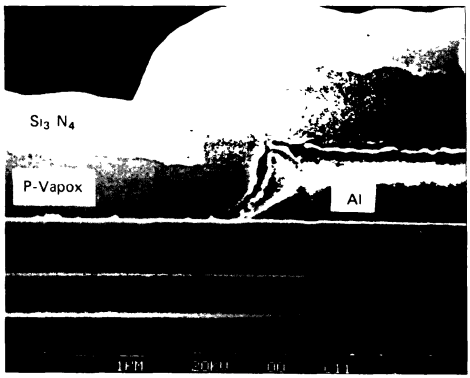


Fig. 2 - Section along the scribing line of an HSCMOS device.

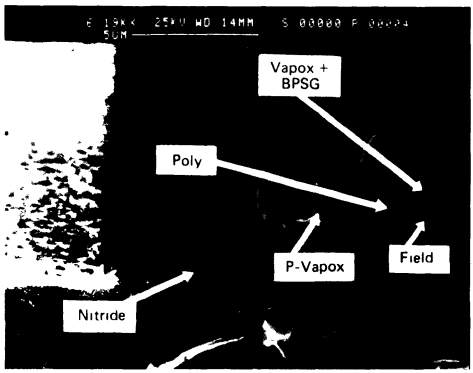
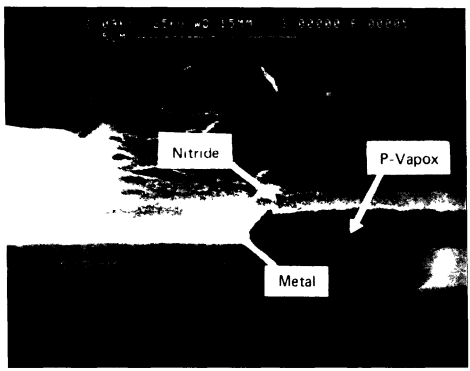


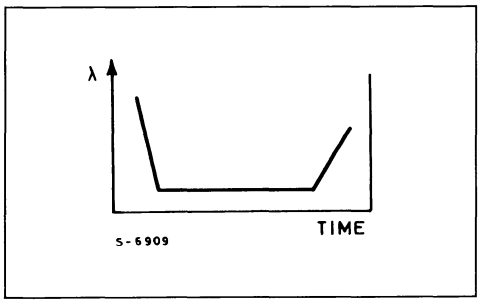
Fig. 3 - Section along the Pad of an HSCMOS device.



RELIABIITY AND FAILURE MECHANISMS

FUNDAMENTALS

- Through accelerated stresses we ascertain the value of the components failure rates, in terms of how many devices (in percent) are expected to fail every 1000 hours of operation (λ or F.R.)
- Failure rate versus time of activity shows the well-known trend.
- Failure rate



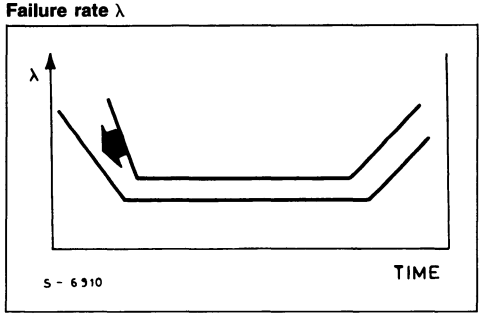
During the first time period the products are affected by the so-called "infant mortality" intrinsic to all semiconductor technologies. End users are very sensitive to this parameter which causes early operation failures to their system.

TARGETS

SGS-THOMSON periodically reviews and publishes lifetime results; at this time a new set of failure rate targets are being defined. These targets are translated into actual required test hours.

The Goal is a steady shift of the limits.

Failure rate λ



TESTS

With accelerated tests we define the failure rate of the products, then, derating the data at different conditions, we know the life expectancy under the actual operating conditions.

In its simplest form the Failure Rate (at a given temperature) is:

$$F.R. = \frac{N}{D \cdot H} \quad (1)$$

Where
N = Number of failures
D = Number of components
H = Number of testing hours

If we intend to determine the Failure Rate at other temperatures an acceleration factor must be considered.

Some tests are accelerated by means of increased temperature, based on the assumption of the Arrhenius law:

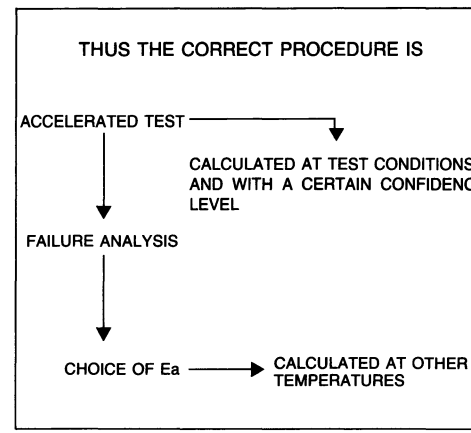
$$F.R. = Ae^{-Ea/KT_J} \quad (2)$$

A = Constant
Ea = Activation energy
K = Boltzman's constant
T_J = Absolute temperature

For two different temp. $F.R.(T_1) = F(T_1, T_2)F.R.(T_2)$

from (2) it is: $F(T_1, T_2) = EXP\left[\frac{-E_a}{K}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$ (3)

Clearly the choice of an appropriate activation energy Ea is of paramount relevance.
The different mechanisms which could lead to circuit failure are characterized by specific activation energies whose values are published in the relevant literature.



Arrhenius equation (2) describes the rate of many processes responsible for degradation and failure of electronic components; it follows that if the transition of an item from an initial stable condition to a defined degraded state occurs by a thermally activated mechanism, then the time for the transition is given by an equation of the form:

MTBF = B EXP (Ea/Kt)

MTBF = Mean time between failures

B = Temperature-independent constant

MTBF can be defined as the time to suffer a device degradation. The dramatic effect of the choice of the Ea value can be seen by plotting equation (2).

The acceleration effect of a 125°C device junction test with respect to 70°C actual device junction operation is equal to 100 (times) for Ea = 1eV and respectively 4 for Ea = 0.3eV.

Some words of caution are needed about published values of Ea:

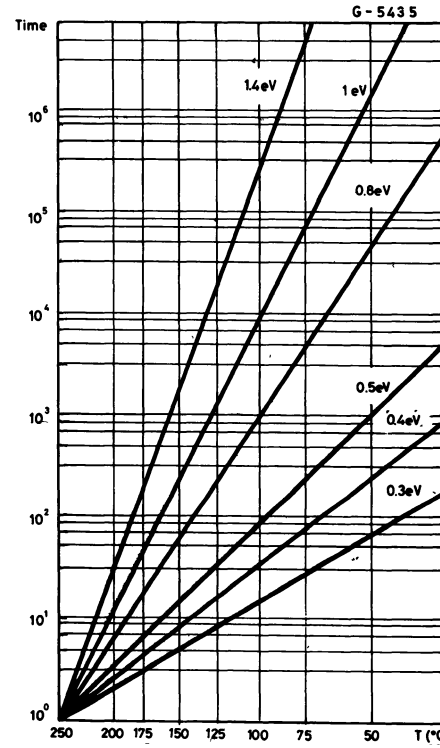
A) They are often related to high temperature test where a single Ea (with high value) mechanism has become significant.

B) They are specifically related to the devices produced by that supplier (and to its technology) and in that period of time.

C) They could be modified by the mutual action of other stresses (voltage, mechanical)

D) Field device-application conditions should be considered.

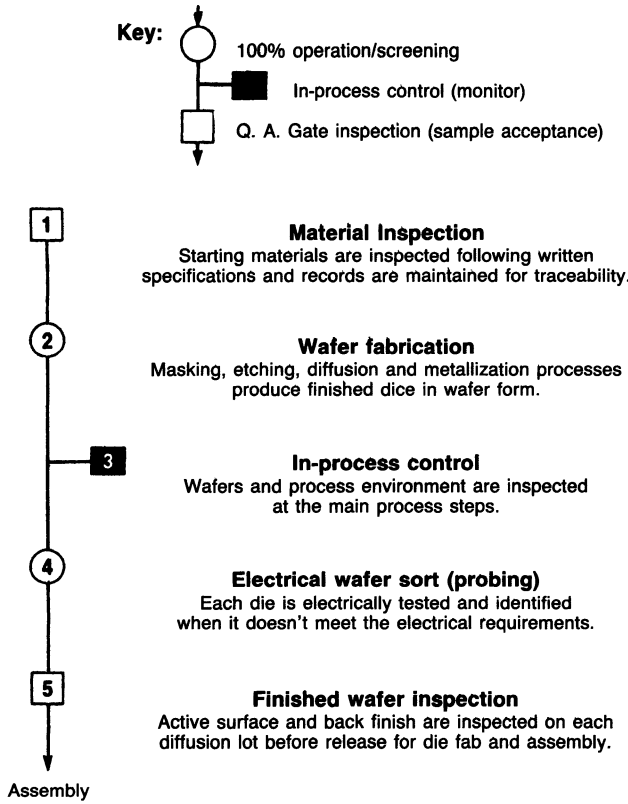
Life-Hours



Main Failure modes and relevant activation energies

FAILURE MODE	ACTIVATION ENERGY (eV)	ACCELERATING
SURFACE CHARGE	1.0 - 1.05	HIGH TEMPERATURES BIAS
IONIC CONTAMINATION	1.0 - 1.4	HIGH TEMPERATURE BIAS
DIELECTRIC DEFECTS	0.3 - 0.6	HIGH TEMPERATURE BIAS
ELECTROMIGRATION	0.5 - 1.2	HIGH TEMPERATURE BIAS
INTERMETALLIC GROWTH	1.0 - 1.05	HIGH TEMPERATURE BIAS, STORAGE
METAL CORROSION	0.3 - 0.8	HIGH HUMIDITY BIAS

WAFER FAB STANDARD PRODUCTION PROCESS FLOW CHART



Material Inspection
Starting materials are inspected following written specifications and records are maintained for traceability.

Wafer fabrication
Masking, etching, diffusion and metallization processes produce finished dice in wafer form.

In-process control
Wafers and process environment are inspected at the main process steps.

Electrical wafer sort (probing)
Each die is electrically tested and identified when it doesn't meet the electrical requirements.

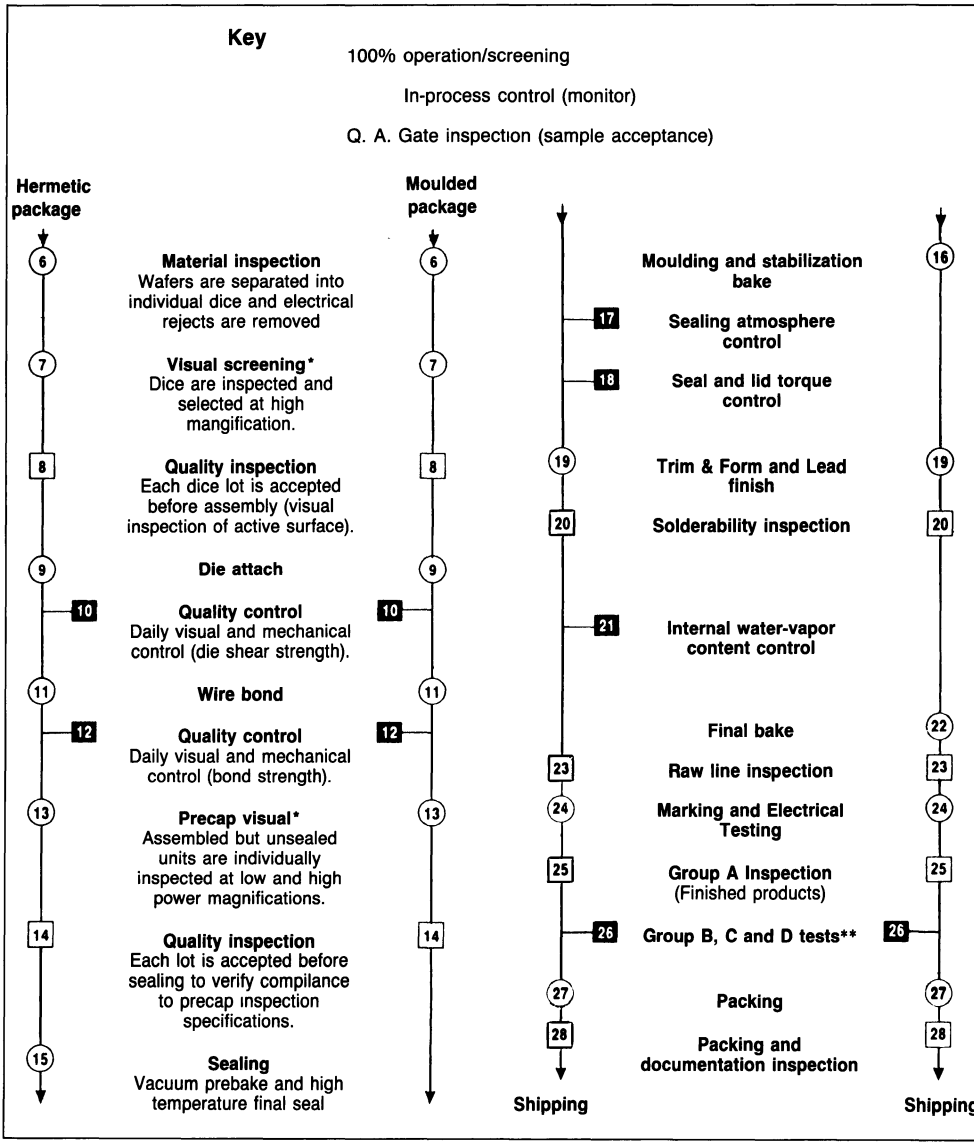
Finished wafer inspection
Active surface and back finish are inspected on each diffusion lot before release for die fab and assembly.

QUALITY INSPECTIONS/MONITORS DURING WAFER FABRICATION

The Table emphasizes the most important fabrication steps with the relevant Quality inspections/monitors performed.

PROCESS STEPS	IN-PROCESS INSPECTIONS/MONITORS
OXIDATION AND DIFFUSION	— Visual — Thickness — CV plot (Stability of ionic concentration and contamination control)
DEPOSITION: Nitride, BPSG, PSG, Poly Si	— Visual — Thickness — Doping content
PHOTO LITHOGRAPHY	— Mask and wafer cleanliness — Visual (alignment and focusing accuracy) — Critical dimensions
ETCHING	— Visual (quality of etching and wafer cleanliness) — Critical dimensions
DOPING BY IMPLANT (P, As, B)	— Sheet resistance (dose and implant uniformity)
DOPING BY DIFFUSION ($POCl_3$, As)	— Sheet resistance
EPITAXIAL GROWTH	— Thickness — Resistivity — Crystal quality (stacking faults, bumps and others)
METALLIZATION	— Visual — SEM (step coverage and film quality) — Thickness — CV plot (stability of ionic concentration and contamination control)
PASSIVATION	— Thickness — Phosphorus concentration — Passivation integrity — Visual
BACK FINISHING	— Wafer thickness — Metal adherence
ELECTRICAL CHARACTERIZATION	— Threshold voltage — Electrical Characteristics: eg. GAIN, leakage current, breakdown voltage, resistivity, etc.
WAFER INSPECTION	— Visual (microscope and/or laser surface inspection system)

ASSEMBLY STANDARD PRODUCTION PROCESS FLOW CHART



* Omitted when the intrinsic quality meets the specified quality level.
** For non military products, these reliability tests can be performed after step 23 on 100% electrically tested samples (when requested).

QUALITY TESTS DURING ASSEMBLY PROCESS

PROCESS STEPS	TESTS	DESCRIPTIONS
10	QUALITY CONTROL (die attach)	MIL STD 883C Method 2010 cond. B (internal visual) and Method 2019 (die shear strength)
12	QUALITY CONTROL (bonding)	MIL STD 883C Method 2010 cond. B (internal visual) and Method 2011 cond. D (bond strength)
14	QUALITY INSPECTION (precap)	MIL STD 883C Method 2010 cond. B (internal visual)
17	SEALING ATMOSPHERE CONTROL	Moisture content: < 200 ppm for Ceramic packages
18	SEAL CONTROL	Fine Leak: MIL STD 883C Method 1014 cond. A1 Helium leak detector after pressurization in He for 2 h at 4.2 atm Limit: $5 \cdot 10^{-8}$ cc/s for ICV* < 0.4 cc $2 \cdot 10^{-7}$ cc/s for ICV ≥ 0.4 cc * ICV = internal cavity volume Gross Leak MIL STD 883C Method 1014 cond. C1 (fluorocarbon gross leak) 5 Torr vacuum for 1h followed by pressurization of the devices immersed in mineral oil at 4.2 atm for 2h, and subsequent immersion in mineral oil at $T_A = 125°C$
	LID TORQUE CONTROL	Ceramic packages only MIL STD 883C Method 2024 (e.g. ≥ 60 kg • cm for seal area values between 1.41 and 1.73 cm^2)
19	TRIM & FORM AND LEAD FINISH	
20	SOLDERABILITY INSPECTION	MIL STD 883C Method 2003 Soldering temperature 245 ± 5°C for 5 ± 0.5 sec. with preconditioning of 1h (1) above boiling distilled water and 5 to 10 sec. in rosin base flux
21	INTERNAL WATER VAPOR CONTENT CONTROL	Dew Point method MIL STD 883C Method 1018 procedure 3 5000 ppm max (dew point temperature less than −15°C) Ceramic packages only.
22	FINAL BAKE	For SMD only (according to internal specifications)

QUALITY TESTS DURING ASSEMBLY PROCESS (Cont'd)

PROCESS STEPS	TESTS	DESCRIPTIONS
23	RAW LINE INSPECTION	External Visual MIL STD 883C Method 2009 Note: at this step some reliability tests (pressure pot, temperature cycling, life test etc.) are performed as a monitor, generally on a weekly basis, to have fast feedback on process behaviour (Real Time Control Tests)
25	GROUP **A** INSPECTION	See below
26	GROUPS **B, C** AND **D** TESTS	Performed on the product family representative types (by rotation); the results are extended to all the other devices of the same family according to the structure similarity concept
28	PACKING AND DOCUMENTATION INSPECTION	Inspection for: — right quantity — right type — right boxing — right labelling — right documentation — various

(1) This preconditioning is going to be substituted by 8h as per MIL-STD-883 C requirements.
Please consult our sales organization for any further information

GROUP A INSPECTION - PRODUCT GUARANTEES (AQLs)

SUBGROUP	PARAMETERS	INSP. LEV.	AQL
A1	Visual and mechanical inspection	I	0.04*
A2 + A3 + A4	Cumulative electrical and inoperative mechanical failures	II	0.04

* 0.065 for SMD (Surface Mounted Devices)
- Guaranteed temperature ranges: according to SGS-THOMSON data books.

GROUPS B, C AND D RELIABILITY TESTS

Every week or every 3 months on raw line material and/or finished products

TEST	MIL-STD-883 C		LTPD
	METHOD	CONDITION	
SUBGROUP 1 physical dimensions	2016	Major dimensions according to data sheet	2 devices (no failure)
SUBGROUP 2 (1) resistance to solvents	2015	1 minute immersion in solvent solution followed by 10 strokes with a soft brush (the procedure shall be repeated 3 times) solvent solution 2.1a only for moulded packages.	4 devices (no failure)
SUBGROUP 3 (1) solderability (*)	2003	Soldering temperature 245 ± 5°C for 5 ± 0.5 sec. with preconditioning of 1 h above boiling distilled water and 5 to 10 sec. in rosin base flux	10
SUBGROUP 4 steady state/operating life test end-point electrical parameters	1005	1000 h at T_A = 125°C, according to detail specification as specified in the applicable device specification; measurements at 0, 168, 500, and 1000 h	5
SUBGROUP 5 (hermetic packages only) temperature cycling constant acceleration seal - fine - gross end-point electrical parameters	1010 2001 1014	test condition C (10 cycles T_A = −65°C to +150°C); 10 minutes at temperature extremes; recovery time max 15 minutes after 1 minute max transfer time test condition E (30000 g) Y1 orientation only (2) test condition A1 test condition C1 (see step 18 pag. 895) as specified in the applicable device specification	10

(*) See note 1 page 896

(1) Performed weekly on finished product

(2) 2000 g for packages, with cavity perimeter of 5 cm or more and/or with a mass of 5 grams or more.

GROUPS B, C AND D RELIABILITY TESTS

Every week or every 3 months on raw line material and/or finished products (continued)

TEST	MIL-STD-883 C		LTPD
	METHOD	CONDITION	
SUBGROUP 6 (1) (moulded packages only)			
pressure pot		T_A = 121°C, 2 atm, 168 h minimum	10
end-point electrical param.		as specified in the applicable device specification	
SUBGROUP 7 (1) (moulded packages only)			
HAST (Highly Accelerated Stress Test)	—	130°C - 85% RH with bias t = 48 h according to detail specification	10
end-point electrical param.		as specified in the applicable device specification	
SUBGROUP 8 (hermetics packages only)			
seal - fine - gross	1014	test condition A1 test condition C1 (see step 18 pag. 895)	
thermal shock	1011	test condition B, 60 cycles (T_A = −55°C to +125°C) 5 minutes at temperature extremes transfer time ⩽ 10 sec.	
seal - fine - gross	1014	test condition A1 test condition C1 (see step 18 pag. 895)	
end-point electrical parameters		as specified in the applicable devide specification	

(1) Performed weekly on finished products
(2) 20000 g for packages, with cavity perimeter of 5 cm or more and/or with a mass of 5 grams or more

GROUPS B, C AND D RELIABILITY TESTS

Every 6 months on raw line material and/or finished products

TEST	MIL-STD-883 C		LTPD
	METHOD	CONDITION	
SUBGROUP 1			
lead integrity	2004	test condition B2 (lead fatigue) - three leads shall be bent, 3 times, simultaneously for at least 15° permanent bend, returning then to the original position	10
seal (hermetic packages only) - fine - gross	1014	 test condition A1 test condition C1 (see step 18 pag. 895)	
SUBGROUP 2 (hermetic packages only)			
thermal shock	1011	test condition B; 15 cycles (T_A = −55°C to +125°C) 5 minutes at temperature extremes transfer time ⩽ 10 sec.	10
temperature cycling	1010	test condition C; 100 cycles (T_A = −65°C to +150°C) 10 minutes at temperature extremes; recovery time max 15 minutes after 1 minute max transfer time	
moisture resistance	1004	Lead bend stress initial conditioning followed by 10 cycles of 24h; T_A = 25°C to 65°C RH = 80% to 100% one 3h cycle at T_A = −10°C	
seal - fine - gross	1014	 test condition A1 test condition C1 (see step 18 pag. 895)	
visual examination		per visual criteria of method 1004 and 1010	
end-point electrical parameters		as specified in the applicable device specification	
SUBGROUP 3 (hermetic packages only)			
mechanical shock	2002	test condition B; 1500 g - 0.5 msec. - 5 blows in each of the 6 orientations - not operating	10
vibration, variable frequency	2007	test condition A; 20 g - 3 orientations f = 20 to 2000 cps; four 4 minutes cycles; 48 minutes total - not operating	
constant acceleration (1) seal - fine - gross	2001 1014	test condition E (30000 g), Y1 orientation only test condition A1 test condition C1 (see step 18 pag. 895)	
visual examination		per visual criteria of Method 1011 or 1010	
end-point electrical parameters		as specified in the applicable device specification	

GROUPS B, C AND D RELIABILITY TESTS

Every 6 months on raw line material and/or finished products (continued)

TEST	MIL-STD-883 C		LTPD
	METHOD	CONDITION	
SUBGROUP 4			
salt atmosphere	1009	test condition A; 10 to 50 gr of NaCl per square meter per day for 24 h at Ta = 35°C	10
seal	1014		
(hermetic packages only)			
- fine		test condition A1	
- gross		test condition C1 (see step 18 pag. 895)	
visual examination		per visual criteria of method 1009	
SUBGROUP 5			
(moulded packages only)			
temperature cycling	1010	test condition C; 100 cycles (T_A = −65 to + 150°C) 10 minutes at temperature extremes; recovery time max 15 minutes after 1 minute max transfer time	5
visual examination		per visual criteria of Method 1010	
end-point electrical parameters		as specified in the applicable device specification	
SUBGROUP 6			
(moulded packages only)			
humidity test	CECC 90000	85°C/85% RH with bias, t = 1000 h according to detail specification	5
end-point electrical parameters		as specified in the applicable device specification; measurements at 0, 168, 500 and 1000 h	
SUBGROUP 7			3 devices 0 failures or 5 devices 1 failure (2)
(hermetic packages only)			
internal water-vapor content	1018	dew point method-procedure 3 (5000 ppm max)	
SUBGROUP 8			
(ceramic packages only)			
lid torque (3)	2024	(see step 18 pag. 895)	10

1) 20000 g for packages with cavity perimeter of 5 cm or more and/or mass of 5 grams or more.
2) Test three devices if one fails test two additional devices with no failure.
3) Lid torque test shall apply only to packages which use a glass-frit seal to lead frame, lead or package body (i.e. wherever frit seal establishes hermeticity or package integrity)

HSCMOS - RESULT SUMMARY

TEST	CONDITION	PLASTIC				CERAMIC				S.O. PACKAGE			
		1987		1H 88		1987		1H 88		1987		1H 88	
		SS	REJ	SS	REJ	SS	REJ	SS	REJ	SS	REJ	SS	REJ
HIGH TEMPERATURE BIAS	1000 hrs	3790	2	1170	1	660	0	390	0	510	0	648	0
	2000 hrs	3790	4	660	1	660	0	240	0	510	0	216	0
TEMPERATURE HUMIDITY BIAS	1000 hrs	2690	1	1146	0					480	0	594	0
	2000 hrs	2690	2	660	0					480	0	180	0
PRESSURE COOKER	168 hrs	4090	2	825	0					2100	1	810	0
	336 hrs	1260	3	550	0					880	1	400	0
THERMAL SHOCKS	200 cyc	450	0	550	0	360	0	180	0				
THERMAL CYCLES	200 cyc	1100	0	725	0	360	0	180	0	550	0	660	0
	1000 cyc	120	0	210	0			60	0			230	0
MECHANICAL SEQUENCE						330	0	120	0				
RESISTANCE TO SOLVENT		450	0	275	0	88	0	60	0	375	0	225	0
SOLDERABILITY		325	0	275	0	180	0	60	0	375	1	225	1
LEAD INTEGRITY		325	0	375	0	165	0	100	0				

FAILURE RATE EVALUATION

PACKAGE	DEVIATION x HOURS AT 125°C	FAIL	FAILURE RATE AT 60% CONFIDENCE LEVEL			
			LAMBDA (x)*	FIT **		
			POINT ESTIMATE	70°C	55°C	40°C
PLASTIC	$8{,}90 \times 10^6$	5	0.071	27.5	9.4	2.9
CERAMIC	$1{,}75 \times 10^6$	0	0.047	18.3	6.2	1.9
S.O. PACKAGE	1.88×10^6	0	0.049	19.0	6.5	2.0

* Lambda (X) = % of failures on 1000 hours of operation
** FIT = Failure in Time. Number of failures on 10^9 Hours of operation
The activation energy, from analisys, was choosen 0.7 eV based on our tests results : the failure rate at lower operating temperature can be estrapolated by the Arrhenius plot.

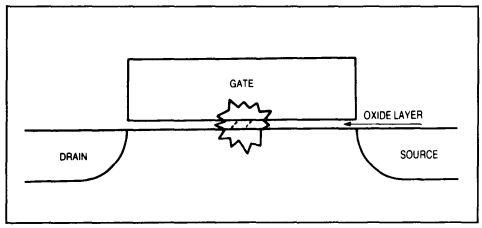
The actual junction temperature should be used; it can be computed using the relationship

$$Tj = T_A = (P \times \Theta_{JA})$$

Where Tj = junction temperature
T_A = ambient temperature
Θ_{JA} = junction to ambient thermal resistance (typically 100 °C/watt for a 16 pin DIP)
P = power actual consumption

ELECTROSTATIC DISCHARGE PROTECTION

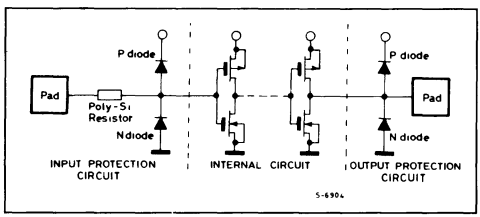
Electronic components have to be protected from the hazard of static electricity, from the manufacturing stage down to where they are utilized.
MOS devices are typically voltage and electrical field sensitive; the thin oxide layers can be destroyed by an electric field.



This happens mostly because a charged conductor, typically a person, is rapidly discharged through the device.
There will be no net charge on any portion of the MOS structure; when the induced high field exceeds the breakdown voltage of the MOS capacitor structure we may have a self-healing breakdown, degradation or catastrophic failure.
The failure hazard is not limited to the gate region but it could occur wherever two conductive areas are separated by a thin insulator.
We have envisaged two sets of precautions: input protection networks and static discharge control (handling).

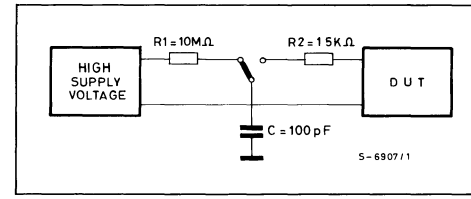
INPUT PROTECTION

The HSCMOS, in addition to improve performance and power consumption, also features improved input protection. This has been achieved by employing poly-silicon as a resistor structure at all inputs.
The resistor slows down the fast input transients generated by electrostatic discharges and dissipates some of the associated energy. Although these input resistors, in conjunction with the input diode, give improved levels of protection, it is still advisable to follow the usual CMOS has handling precautions.



The protection capability has been verified with the following discharge set.

Measurement with the MIL 883C-3015



The testing results are reported below

	MIL-STD-883C (C = 100pF R = 1.5 KΩ)
INPUT +	1.6 KV
INPUT −	1.3 KV
OUTPUT +	>2 KV
OUTPUT −	>2 KV

HANDLING

SGS-THOMSON has chosen a no-compromise strategy in the MOS ESD protection. From the wafer level to the shipping of finished units, each work station and processing of the party is guaranteed. This is achieved through total adoption of shielding and grownding media. Our final shipping is performed in antistatic tubes bags or boxes. The suppliers greatest efforts are in vain if the end user does not provide the same level of protection and care in application.
Here are the basic static control protection rules:

A - handle all components in a static-safe work area.
B - transport all components in static shielding containers.

To comply with the rules the following procedures must be set up.

1 - Static control wrist strap (from a qualified source) used and connected properly.
2 - Each table top must be protected with a conductive mat, properly grounded.
3 - Extensive use of conductive floor mats.
4 - Static control shoe straps, wearing typically insulating footwear, such as with crepe or thick rubber soles.
5 - Ionized air blowers are a necessary part of the protective system, to neutralize static charges on conductive items.
6 - Use only the grounded tip variety of soldering iron.
7 - Single components, tubes, printed circuit cards should always be contained in static shielding bags; keep our parts in the original bags up to the very last moment on the production line.
8 - If bigger containers (tote box) are used for in-plant transport of devices or PC boards they must be electrically conductive, like the carbon loaded ones.

Hanglind (Continued)

9 - All tools, persons, testing machines, which could contact device leads must be conductive and grounded.

10 - Avoid using high dielectric materials (like polystyrene) for sub-assembly construction, storing and transportation.

11 - Follow a proper power supply sequence in testing and application. Supply voltage should be applied before and removed after input signals; insertion and removal from sockets should be done with no power applied.

12 - Filtration, noise suppression, slow voltage surges should be guaranteed on the supply lines.

13 - Any open (floating) input pin is a potential hazard to your circuit: ground or short them to V_{DD} whenever possible.

NOTES

NOTES

NOTES

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