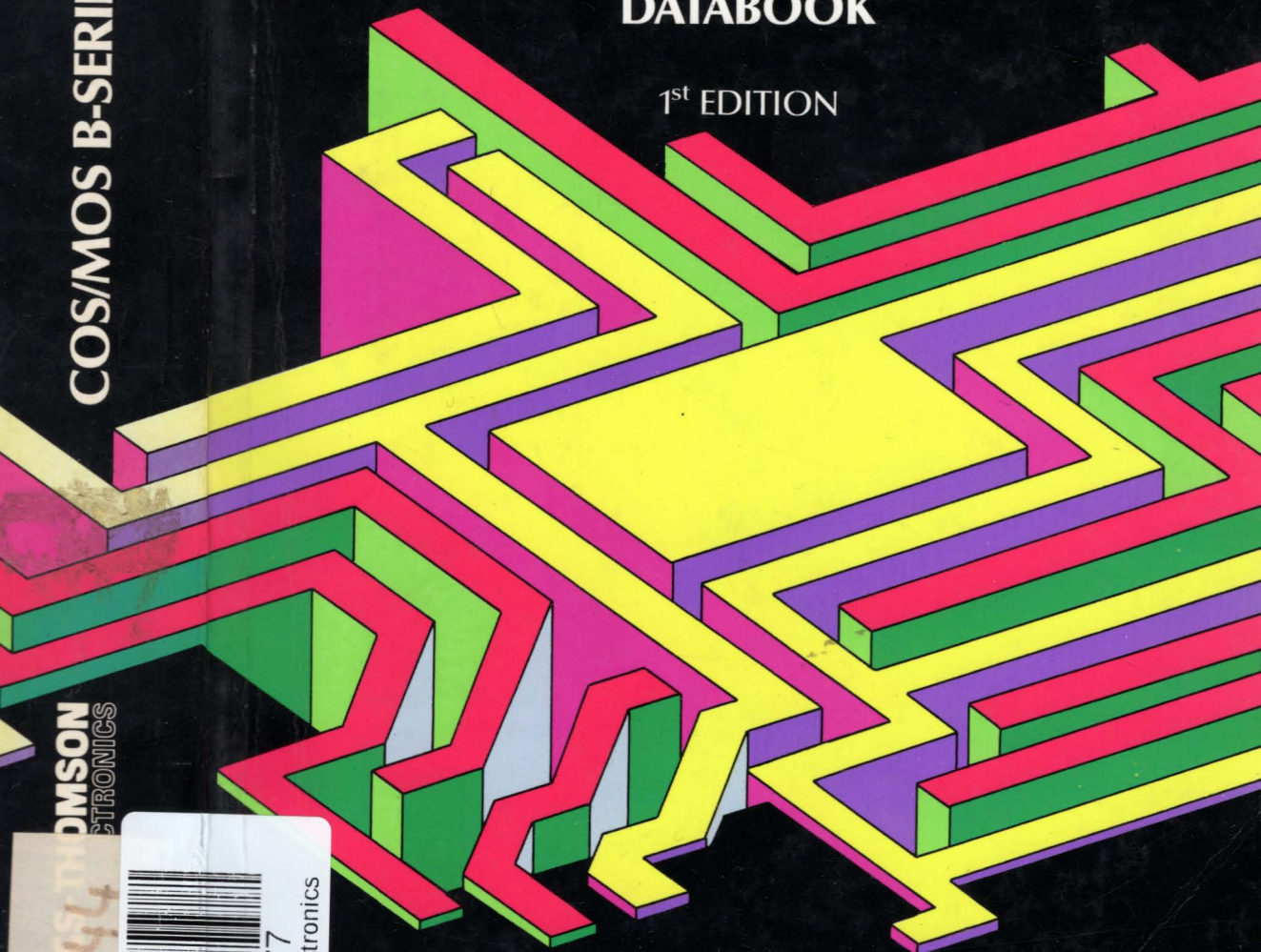
# COS/MOS B-SERIES DEVICES

## DATABOOK

1st EDITION



SGS-THOMSON
MICROELECTRONICS

COS/MOS B-SERIES DEVICES

3144

# COS/MOS B-SERIES DEVICES

## DATABOOK

1st EDITION

SEPTEMBER 1991

**USE IN LIFE SUPPORT DEVICES OR SYSTEMS MUST BE EXPRESSLY AUTHORIZED** 477

SGS-THOMSON PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

# TABLE OF CONTENTS

# INTRODUCTION

This databook contains datasheets on the SGS-THOMSON range of CMOS B-series integrated circuits.

The information on each product, in accordance with EIA/JEDEC specifications, has been specially presented in order that the performance of the product can be readily evalutated within any required equipment design.

The two sections, Military/CECC and Radiation Hardened products, are inlcuded for more stringent device requirements such as Military, Space, Biomedical and other high reliability applications.

New developments in packaging include the PLCC package; all the surface out-line packages (SO) are made to JEDEC standards.

In addition, general considerations that should be taken into account in the operation and application of CMOS B-series integrated circuits are described. Selection guides are included to simplify the task of choosing the best combination of circuits a for system.

The databook also contains the results of the reliability studies made by SGS-THOMSON on its CMOS B-series.

# ALPHANUMERICAL INDEX

# ALPHANUMERICAL INDEX

# ALPHANUMERICAL INDEX

# ALPHANUMERICAL INDEX

# SELECTION GUIDE

## HCC/HCF 4000B/4500B 40100B STANDARD SERIES AND CROSSPOINT SWITCHES

| Function | | Standard Code |
|---|---|---|
| GATE BUFFER | NAND | 4011B, 4012B, 4023B, 4068B, 40107B |
| | NOR | 4000B |
| | AND | 4068B, 4073B, 4081B, 4082B |
| | OR | 4071B, 4072B, 4075B, 4078B |
| | INVERTER | 4069UB, 4502B |
| | BUFFER | 4007UB, 4009UB, 4010B, 4041UB, 4049UB, 4050B, 4502B, 4503B, 40107B |
| | MULTIFUNCTION | 4019B, 4030B, 4048B, 4070B, 4077B, 4085B, 4086B, 4572UB, 4504B |
| | SCHMITT TRIGGER | 4093B, 40106B |
| FLIP-FLOP | J-K FLIP-FLOP | 4027B, 4095B, 4096B |
| | D FLIP-FLOP | 4013B, 4076B, 40174B |
| INTERFACE CIRCUIT | | 4009UB, 4010B, 4504B, 40109B |
| LATCH | | 4042B, 4043B, 4044B, 4099B, 4508B |
| MULTIVIBRATOR | | 4047B, 4098B, 4538B |
| DECODER | | 4028B, 4514B, 4515B, 4555B, 4556B |
| ENCODER | | 4532B, 40147B |
| DISPLAY DRIVER | | 4054B, 4055B, 4056B, 4511B, 4543B |
| | WITH COUNTER | 4026B, 4033B, 40110B |
| REGISTER | SHIFT STATIC | 4006B, 4014B, 4015B, 4021B, 4031B, 4034B, 4035B, 4094B, 4517B, 40100B, 40104B, 40194B |
| | STORAGE | 4076B, 4099B, 40108B, 40208B |
| | FIFO | 40105B |
| COUNTER | SYNCRONOUS | 4017B, 4018B, 4022B, 4029B, 4510B, 4516B, 4518B, 4520B, 4521B, 4522B, 40102B, 40103B, 40160B, 40161B, 40162B, 40163B, 40192B, 40193B |
| | BINARY RIPPLE | 4020B, 4024B, 4040B, 4060B |
| | CLOCK TIMER | 4045B, 4536B, 4541B, 4566B |
| MULTIPLEXER/ DEMULTIPLEXER | ANALOGIC DIGITAL | 4016B, 4019B, 4051B, 4052B, 4053B, 4066B, 4067B, 4097B, 4555B, 4556B |
| | DATA SELECTOR | 4512B, 4529B, 40257B, 4519B |
| ARITHMETIC CIRCUIT | ADDER | 4008B, 4032B, 4038B, 4560B |
| | COMPARATOR | 4030B, 4063B, 4070B, 4077B, 4585B, 40101B |
| | ALU / MULTIPLEXER | 4089B, 4527B, 40181B, 40182B |
| PHASE LOCKED LOOP | | 4046B |
| CROSSPOINT SWITCH | 4x4 | 22100 |
| | 4x4x2 | 22101, 22012 |

# GENERAL AND APPLICATION INFORMATION

## THE PRODUCT FEATURES

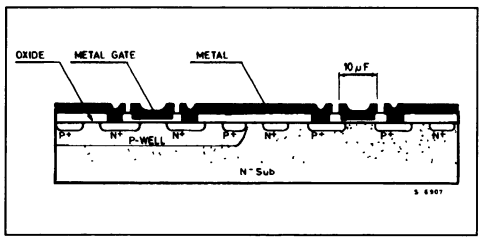
SGS-THOMSON's 4000B family of metal gate CMOS monolithic integrated circuits provides the design engineer with a wide range of products which approache the ideal in performance.

The combination of low power dissipation, flexible power-supply design, high noise immunity and fan - out capability have made this logic family extremely popular.

These products are mainly used in telecommunication and consumer/commodity fields and high reliability applications such as space and biomedical use.

SGS-THOMSON CMOS 4000B family is backed up by one of the most extensive product ranges in the industry, a cost effectiveness together with high-reliability and high quality thus offering the user the best solution to a greater number of applications.

### CMOS Metal Gate




## THE PRODUCT TECHNOLOGY

Although the CMOS 4000B is a mature product family, SGS-THOMSON continuously introduces improvements in the process, according to the present "state of the art".

Ion implantation gives precise control of channel doping allowing a much tighter distribution of device parameters and better reproducibility of the process.

The entire process is tracked using an on-line computer system. Moreover, in line with SGS-THOMSON quality control philosophy, particular attention is paid to upgrading production facilities. All the above factors lead to improvements in reliability, controllability, repeatibility or, in one word, quality.

## THE PRODUCT INFORMATION

The SGS-THOMSON CMOS HCC/HCF 4000B series meets the industry standardized specifications co-ordinated by EIA/JEDEC Solid State Products Council.

The official JEDEC specifications for static parameters are primarily applicable to gates, inverters, high current (inverting) drivers and devices with Medium Scale Integration.

Special types such as analog switches, multiplexers and multivibrators do not have the same input-output standards as the B series specifications but are still given with a B suffix because they satisfy the remaining JEDEC specifications.

**SGS-THOMSON HCC/HCF 4000B types have the following Absolute Maximum Ratings:**

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage: **HCC**<br>**HCF** (1) | –0.5 to 20<br>–0.5 to 18 | V<br>V |
| $V_i$ | Input Voltage | –0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$= Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature: **HCC** types<br>**HCF** types | –55 to + 125<br>–40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | –65 to + 150 | ÉC |

1) During factory testing, the HCF devices are measured applying the same values of supply voltage as for HCC types. Moreover the HCF limits for quiescent current ($I_L$) and input leakage current ($I_{IH}$, $I_{IL}$) are as for the HCC limits.

**The Recommended Operating Conditions are specified as follows:**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply voltage: **HCC**<br>**HCF** (1) | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating temperature: **HCC** types<br>**HCF** types | –55 to + 125<br>–40 to + 85 | °C<br>°C |

1) During factory testing, the HCF devices are measured applying the same values of supply voltage as for HCC types. Moreover the HCF limits for quiescent current ($I_L$) and input leakage current ($I_{IH}$, $I_{IL}$) are as for the HCC limits.

If these ratings are compared with the corresponding JEDEC values shown in table II and III it can be seen that the SGS-THOMSON HCC/HCF 4000B devices have much better limits than those of the JEDEC specifications. The static electrical characteristics of the HCC/HCF 4000B series, excluding special devices such as analog switches, multiplexers, drivers, etc. are shown in table I.

The SGS-THOMSON HCC/HCF 4000B family has the quiescent leakage current ($I_L$), specified at 5, 10, 15, 20 V and the other static electrical characteristics at 5, 10, 15 V for both extended and intermediate temperature ranges.

### HCC/HCF 4000B Series Features

The principal features of the HCC/HCF 4000B series are as follows:

- Operating range of **HCC** 3-18V; **HCF** 3-15V
- Rationalised range of quiescent leakage current ($I_L$) specifications corresponding to gate, buffer and flip-flop, and Medium Scale Integration products.
- Maximum input leakage current ($I_{IH}$, $I_{IL}$) of ± 1 µA at $V_{DD}$= 18V for **HCC**, 15V for **HCF** with $V_I$= 0 to 18V for **HCC**, 0 to 15V for **HCF**, over the full temperature range.
- Input and output logic levels completely independent of temperature.
- Input voltage levels which define a very high DC noise immunity (45% $V_{DD}$ typical).
- Noise margins of 1.0V min. at 5V $V_{DD}$<br>2.0V min. at 10V $V_{DD}$<br>2.5V min. at 15V $V_{DD}$
- Low (400 Ω typical) and constant output impedance in both logical states giving fixed and equal output transition times.
- Output current capable of driving<br>a) two low power TTL loads<br>b) one low power Schottky TTL load<br>c) two HLL loads<br>over the rated temperature range.
- Output current and input threshold independent of the number of inputs parallel together.
- Square transfer voltage characteristics.

### General COS/MOS Characteristics

The main advantages offered by COS/MOS devices over corresponding bipolar devices (DTL, LPS, TTL, ECL, HLL) are:

– Very low quiescent power dissipation (typically 10 nW/gate, 10 vW/MSI)

– Wide operating voltage range (3 to 18V for **HCC**; 3-15V for **HCF**)

– High input impedance (typically $10^{12}$ Ω)

– High DC noise immunity (typically 45% of supply voltage).

This digital family however has slower switching speeds than most bipolar families.
For example the typical propagation times for COS/MOS and other logic families are:

| Propagation Delay Time (ns) | COS/MOS | ECL | LPS | TTL | DTL | HLL |
|---|---|---|---|---|---|---|
| | 35 | 2 | 5 | 10 | 30 | 110 |

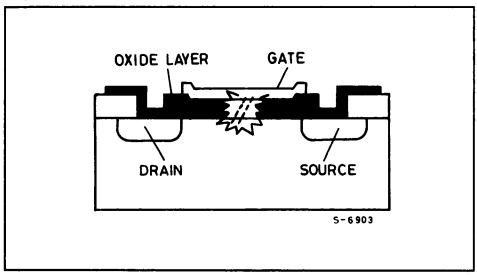
Moreover, due to the high input impedance of the MOS gates, COS/MOS devices require greater care in handling.

The normal gate oxide thickness is 800 to 1000Å with a corresponding breakdown voltage between gate and substrate of 80 to 90V.

The electrostatic potential of the human body is much higher than this range, reaching 12kV with a discharge capacity of approximately 100 pF.

Electronic components have to be protected from the hazard of static electricity, from the manufacturing stage down to where they are utilized. MOS devices are typically voltage and field sensitive; the thin oxide layers can be destroyed by the electric field.

**Fig. A**




This happens mostly because a charged conductor, typically a person, is radiply discharged through the device.

There will be no net charge on any portion of the MOS structure; when the induced high field exceeds the breakdown voltage of the MOS capacitor structure we may have a self-healing break-down, degradation or catastrophic failure.

The failure hazard is not limited to the gate region but it could occur wherever two conductive areas are separated by a thin insulator.

We have envisaged two sets of precautions: input protection networks and static discharge control (handling).

The HCC/HCF 4000B devices use an improved protection network over that used in the **4000A** series. The level of protection for the **4000B** products has been raised to 4 kV, the previous solution for the **4000A** products protected the gate oxide against electrostatic discharges only up to approximately 1 kV. The following figures show the difference between the two input protection networks for a basic inverter:

**Fig. B**

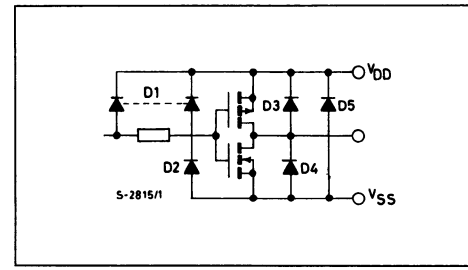
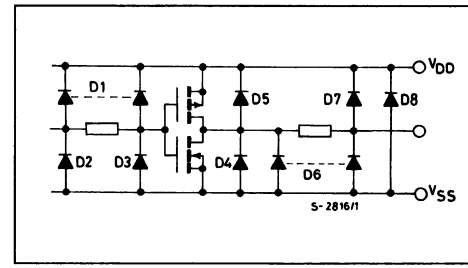
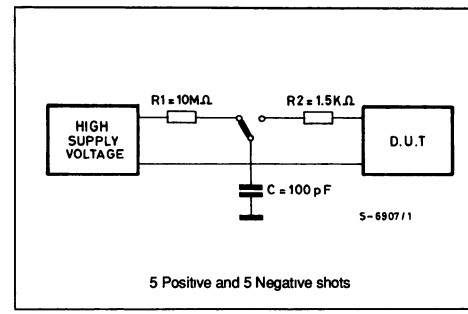



**Fig. C**




The protection capability has been verified with the following discharge set as show in figure below.

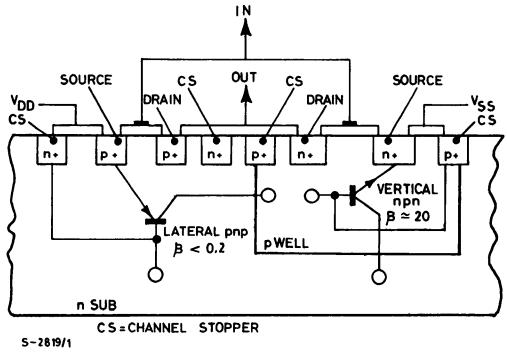
**Measurement to the MIL-STD 883C-3015**




5 Positive and 5 Negative shots

In COS/MOS as in Linear Integrated Circuits a "latch-up" phenomenon may appear. This is caused by an electrical pulse which, acting on an SCR structure of parasitic bipolar transistors inside COS/MOS devices (shown in fig. D), produces a low resistance path between supply voltage and ground that remains after the pulse has ceased leading rapidly to device destruction.

Fig. D




This phenomenon will occur either when $V_{DD}$ is more than the maximum rating and approaches the breakdown voltage of the SCR structure or when any of the following conditions are verified:

a) the product of the gains of the two parasitic transistors is greater than or equal to unity;

b) the base-emitter junction of both transistors is forward biased;

c) supply voltage and input circuits are able to deliver a current equal to the holding current of the SCR (fig. E).

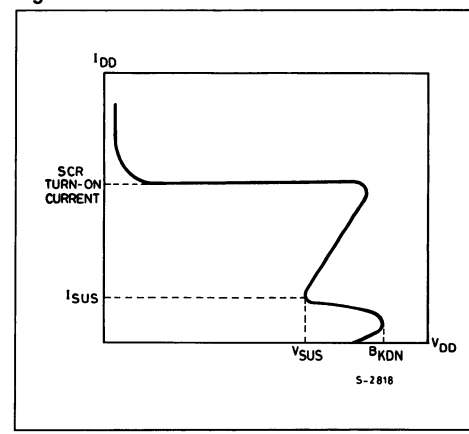
In particular, condition (b) may be caused by:

1) voltages induced through the oxide by base metallization;

2) lateral voltage drops between substrate and P-well due to photo-current generated by radiation. These drops can forward bias the gate-cathode junction of the parasitic SCR.

This effect is particularly significant in buffers which are devices most subject to latch-up due to the combination of large geometry and low silicon resistivity. For these reasons voltage transient or large output current surges occurring during operation near the maximum rating should be avoided.

Fig. E




The B series devices are much better protected against latch-up than the A series because of their higher typical breakdown voltage:

| Characteristics | A series | B series |
|---|---|---|
| $V_{BR}$ | 17 V | 25 V |
| $V_{SUS}$ | 15 V | 22 V |
| $I_{SUS}$ | 10 to 40 mA | 50 to 100 mA |

### B Series Dynamic Switching Parameters

The dynamic electrical characteristics are specified at $T_{amb}$= 25°C under the following conditions:

- load capacitance ($C_L$) of 50 pF and load resistance ($R_L$) of 200 kΩ;
- input pulse amplitude equal to supply voltage ($V_{DD}$);
- input rise and fall times of 20 ns;
- propagation delay times measured from 50% the point of the input voltage to the 50% point of the output voltage;
- transition times measured from 10% to 90% of the supply voltage ($V_{DD}$).

In some devices other time parameters are also specified:

a) Set up time

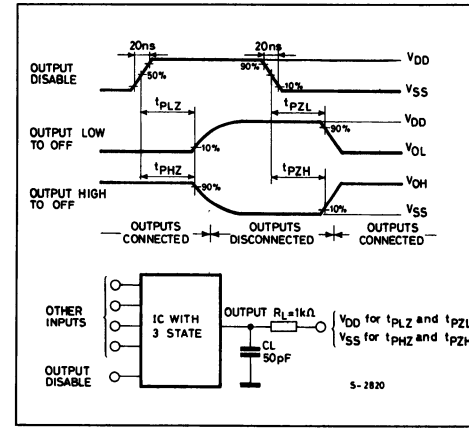
b) Hold time

c) Removal time

d) Tri-state disable delay times.

The figures (F and G) show the meaning of these parameters

Fig. F




The corresponding values of suffix B types are:

$V_{IL}$= 30% $V_{DD}$
$V_{IH}$= 70% $V_{DD}$ for $V_{DD}$= 5V and 10V

and

$V_{IL}$= 27% $V_{DD}$
$V_{IH}$= 73% $V_{DD}$ for $V_{DD}$= 15V

The other main differences between B and UB gates are summarized on the page 20.

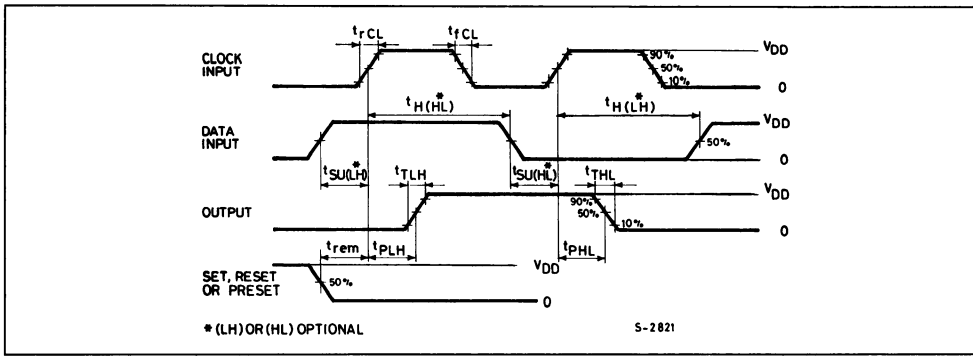
If B and UB gates are presented with slow transition time signals the behaviour of the two types differs. In fact, because of high AC gain of B devices (obtained with the two extra inverters) the outputs tend to develop a few cycles of oscillation between $V_{DD}$ and $V_{SS}$ when input rise or fall time is more than 1 ms at $V_{DD}$= 5V and AC noise is reduced to 2–3 mV within the B device bandwidth.
The unbuffered gates (which have less gain) tend not to oscillate with the same input ramp unless a noise voltage of 200 to 300 mV is present within the device bandwidth.

### Comparison between B and UB devices

The **HCC/HCF 4000B** family also includes suffix UB products that only meet some of the B series electrical specifications.

These have logic outputs that are not buffered, and $V_{IL}$ and $V_{IH}$ that are specified at 20% $V_{DD}$ and 80% $V_{DD}$ respectively for $V_{DD}$= 5V and 10V and 17% $V_{DD}$ and 83% $V_{DD}$ respectively for $V_{DD}$= 15V.

Fig. G



| Characteristics | Buffered | Unbuffered |
|---|---|---|
| Typical Output Impedance | Constant: 400 Ω (typ) at $V_{DD}$= 5V | Variable: Dependent on number of inputs paralleled together |
| Voltage Transfer Characteristic | Square and independent of the number of inputs tied together | Rounded (as A serial) and shifted with different number of inputs paralleled together |
| Propagation Delay | Moderate: 150 ns at $V_{DD}$= 5V<br>65 ns at $V_{DD}$= 10V<br>50 ns at $V_{DD}$= 15V | Fast: 60 ns at $V_{DD}$= 5V<br>30 ns at $V_{DD}$= 10V<br>25 ns at $V_{DD}$= 15V |
| AC Gain | High and constant: ≅ 68 dB | Low and dependent on supply voltage:<br>28 dB at $V_{DD}$= 5V<br>23 dB at $V_{DD}$= 10V<br>18 dB at $V_{DD}$= 15V |
| AC Band Width | Low: 230 kHz at $V_{DD}$= 5V<br>280 kHz at $V_{DD}$= 10V<br>295 kHz at $V_{DD}$= 15V | High: 710 kHz at $V_{DD}$= 5V<br>885 kHz at $V_{DD}$= 10V<br>2800 kHz at $V_{DD}$= 15V |
| Input Capacitance | Low: Average 1 to 2 pF<br>Peak 2 to 4 pF | High: Average 2 to 3 pF<br>Peak 5 to 10 pF |
| Noise Margin | Excellent: 1.0V at $V_{DD}$= 5V<br>2.0V at $V_{DD}$=10V<br>2.5V at $V_{DD}$=15V | Good: 0.5V at $V_{DD}$= 5V<br>1.0V at $V_{DD}$= 10V<br>1.0V at $V_{DD}$= 15V |
| Output Transition Time | 200 ns (typ.) at $V_{DD}$= 5V<br>$C_L$ = 50 pF | 50 to 100 ns at $V_{DD}$= 5V<br>$C_L$ = 50 pF |

## GENERAL OPERATING AND HANDLING INSTRUCTIONS

### Power Source Rules

1) Referring to standard input network protection of fig. B, when separate power supplies are used for $V_{DD}$ and for the device inputs, the $V_{DD}$ supply should always be turned on before the input signal source and the input signal should be turned off before the $V_{DD}$ supply is turned off. This rule will prevent the D1 input protection diode from overdissipation and possible damage when the device power supply is grounded. When the device power supply is an open circuit, violation of this rule can result in undesired circuit operation although device damage may not result; AC inputs can be rectified by D1 input diode to act as a power supply.

2) The steady power-supply operating voltage should be kept within the recommended operating conditions and always below the maximum ratings.

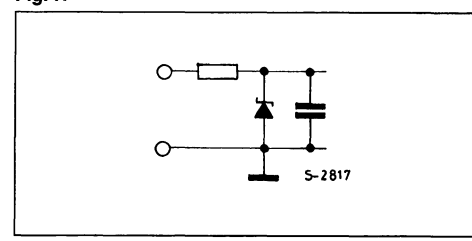
3) The power-supply polarity for COS/MOS circuits should not be reversed. The positive ($V_{DD}$) terminal should never be more than 0.5V negative with respect to the negative ($V_{SS}$) terminal ($V_{DD}$-$V_{SS}$ > −0.5V). Reversal of polarities will forward-bias and short the structural and protection diode between $V_{DD}$ and $V_{SS}$.

4) Power-source current capability should be limited to the minimum value which will assure good logic operation.

5) Large values of resistors in series with $V_{DD}$ or $V_{SS}$ should be avoided; transient turn-on of input protection diodes can result from drops across such resistors during switching.

A good practice is to use a zener protection diode in parallel with the power bus as shown in fig. H below. The zener value should be above the expected maximum regulation excursion, but should not exceed the maximum supply voltge.
A current limiting resistor is included if the supply impedance is lower than the zener power dissipation rating to allow for a given zener voltage.
The shunt capacitor value is chosen to supply required peak current switching transients.

**Fig. H**



**Input Signal Rules**

1) Signals should not be applied to the inputs while the device power supply is off unless the input current is limited to a steady–state value of less than 10mA. Input-signal interfaces that swing the allowable 0.5V above $V_{DD}$ or below $V_{SS}$ should be current-limited to 10mA or less.
Whenever the possibility of exceeding 10mA of input current exists, a resistor in series with the input must be used. The value of this resistor can be as high as 10kΩ without affecting static electrical characteristics. However, speed will be reduced because of the added RC time constant. Particular attention should be given to long input-signal lines where high inductance can increase the likelihood of large-signal pickup in noisy environments. In these cases, series resistance with shunt capacitance at the IC input terminals is recommended. The shunt capacitance should be made as large as possible consistent with the system speed requirements.

2) All COS/MOS inputs should be terminated correctly. When COS/MOS inputs are wired to edge card connectors with COS/MOS drive coming from another PC board, a shunt resistor should be connected to $V_{DD}$ or $V_{SS}$.

3) When COS/MOS circuits are driven by TTL logic a pull-up resistor should be connected from the COS/MOS inputs to 5V.

4) Input signals should be maintained within the recommended input signal swing range.

5) Input rise and fall times for clocked devices must not exceed 15 µs in order to avoid high power consumption, false triggering, etc. With slower inputs a Schmitt trigger must be employed.

**Output Rules**

1) The power dissipation in a COS/MOS package should not exceed the rated value for the ambient temperature specified. The actual dissipation should be calculated when (a) shorting outputs directly to $V_{DD}$ or $V_{SS}$, (b) driving low-impedance loads, or (c) directly driving the base of PNP or NPN bipolar transistors.

2) Output short circuits often result from testing errors or improper board assembly. Shorts on buffer outputs on power supplies greater than 5V can damage COS/MOS devices.

3) COS/MOS, like active pull-up TTL, cannot be connected in the "wire-OR" configuration because an "on" PMOS and an "on" NMOS transistor could be directly shorted across the power-supply rails. For applications with wire OR configurations it is necessary to use devices with tri-state logic outputs.

4) Paralleling gates is recommended only when the gates are within the same IC package.

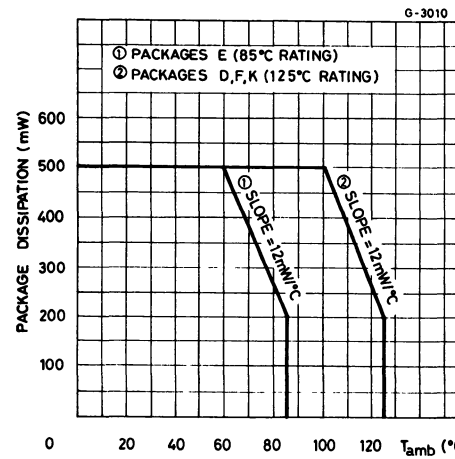
5) Output loads should return to a voltage within the supply-voltage range ($V_{DD}$ to $V_{SS}$).

6) Large capacitive loads (greater than 5000 pF) on COS/MOS buffers of high-current drivers act like short circuits and may over-dissipate output transistors.

7) Output transistors may be over-dissipated by operating buffers as linear amplifiers or using these types as one-shot or astable multivibrators.

8) Shorting of the output to $V_{SS}$ or $V_{DD}$ can cause the device power dissipation to exceed the safe value of 500 mW as shown in fig. I.
This is possible with supply voltage higher than 5V. For cases in which a short circuited load is driven directly (base of PNP or NPN bipolar transistor) the requirements for gate operation must be determined by consulting the published data. Note that a individual output transistor dissipation must be limited to 100 mW.

**Fig. 1 - Standard COS/MOS Thermal Derating Chart**



### Noise Immunity and Noise Margin

*DC Noise Immunity*
The $V_{IL}$ and $V_{IH}$ characteristics define the maximum tolerable noise voltages at an input terminal when input signals are within 50 mV of supply lines.

*Noise Margin*
The noise margin voltage is the maximum voltage that can be added, at an input voltage $V_i = V_{OL}$ or $V_{OH}$ of the preceding stage without upsetting the logic or causing the output to exceed the output voltge $V_O$.

In pratice, DC noise immunity is much more significant than noise margin because the COS/MOS outputs are normally within 50mV of supply lines. Noise immunity increases if the input pulse width becomes less than the propagation delay of the circuit.
This condition is often described as AC noise immunity.

### Handling

SGS-THOMSON has choosen a no-compromise strategy in the MOS ESD protection. From the wafer level to the shipping of finished units, we fully guarantee each work station and processing of the parts.

The supplier best commitment is useless if the end user does not provide the same level of protection and care in application.
Here are the basic static control protection rules to comply with the rules the following procedures should be set up:

a) Handling equipment, trays, table tops and transport carts should be conductive;

b) Metal parts of fixtures, tools, soldering irons and table tops should be grounded to a common point;

c) Operators should use grounded (metal or conductive) plastic wrist straps with a 1MΩ series resistor;

d) Packages should not be removed from their conductive or antistatic carriers until required; this should only be done by a grounded operator. Devices removed should be placed in a conductive tray;

e) All tests should be performed by a grounded operator and after completion of test, devices should be reinserted in conductive carriers;

f) The printed circuit boards should have shorting bars installed prior to assembly (soldering). When possible COS/MOS IC's should be the last component to be installed on printed circuit boards.

**Table I - STATIC ELECTRICAL CHARACTERISTICS (SGS-THOMSON 4000B and UB)**

| Parameter | | Test Conditions | | | | Values | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $V_O$ (V) | $I_O$ (μA) | $V_{DD}$ (V) | $T_{Low}$ | | 25°C | | $T_{High}$ | | |
| | | | | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $I_L$ (gates) | HCC types | 0/ 5 | | | 5 | | 0.25 | | 0.25 | | 7.5 | μA |
| | | 0/10 | | | 10 | | 0.5 | | 0.5 | | 15 | |
| | | 0/15 | | | 15 | | 1 | | 1 | | 30 | |
| | | 0/20 | | | 20 | | 5 | | 5 | | 150 | |
| | HCF types | 0/ 5 | | | 5 | | 1 | | 1 | | 7.5 | |
| | | 0/10 | | | 10 | | 2 | | 2 | | 15 | |
| | | 0/15 | | | 15 | | 4 | | 4 | | 30 | |
| $I_L$ (buffer FF) | HCC types | 0/ 5 | | | 5 | | 1 | | 1 | | 30 | μA |
| | | 0/10 | | | 10 | | 2 | | 2 | | 60 | |
| | | 0/15 | | | 15 | | 4 | | 4 | | 120 | |
| | | 0/20 | | | 20 | | 20 | | 20 | | 600 | |
| | HCF types | 0/ 5 | | | 5 | | 4 | | 4 | | 30 | |
| | | 0/10 | | | 10 | | 8 | | 8 | | 60 | |
| | | 0/15 | | | 15 | | 16 | | 16 | | 120 | |

**Table I - STATIC ELECTRICAL CHARACTERISTICS 4000B and UB** (Cont'd)

| Parameter | | Test Conditions | | | | Values | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $V_O$ (V) | $I_O$ (μA) | $V_{DD}$ (V) | $T_{Low}$ | | 25°C | | $T_{High}$ | | |
| | | | | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $I_L$ (MSI) | HCC types | 0/ 5 | | | 5 | | 5 | | 5 | | 150 | μA |
| | | 0/10 | | | 10 | | 10 | | 20 | | 300 | |
| | | 0/15 | | | 15 | | 20 | | 20 | | 600 | |
| | | 0/20 | | | 20 | | 100 | | 100 | | 3000 | |
| | HCF types | 0/ 5 | | | 5 | | 20 | | 20 | | 150 | |
| | | 0/10 | | | 10 | | 40 | | 40 | | 300 | |
| | | 0/15 | | | 15 | | 80 | | 80 | | 600 | |
| $V_{OH}$ | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | 4.95 | | V |
| | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | 9.95 | | |
| | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | 14.95 | | |
| $V_{OL}$ | | 5/0 | | < 1 | 5 | | 0.05 | | 0.05 | | 0.05 | V |
| | | 10/0 | | < 1 | 10 | | 0.05 | | 0.05 | | 0.05 | |
| | | 15/0 | | < 1 | 15 | | 0.05 | | 0.05 | | 0.05 | |
| $V_{IH}$(B series) | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | 3.5 | | V |
| | | | 1/9 | < 1 | 10 | 7 | | 7 | | 7 | | |
| | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | 11 | | |
| $V_{IL}$ (B series) | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | 1.5 | | 1.5 | V |
| | | | 9/1 | < 1 | 10 | | 3 | | 3 | | 3 | |
| | | | 13.5/1.5 | < 1 | 15 | | 4 | | 4 | | 4 | |
| $V_{IH}$ (UB series) | | | 0.5/4.5 | < 1 | 5 | 4 | | 4 | | 4 | | V |
| | | | 1/9 | < 1 | 10 | 8 | | 8 | | 8 | | |
| | | | 2/13 | < 1 | 15 | 12 | | 12 | | 12 | | |
| $V_{IL}$ (UB series) | | | 4.5/0.5 | < 1 | 5 | | 1 | | 1 | | 1 | V |
| | | | 9/1 | < 1 | 10 | | 2 | | 2 | | 2 | |
| | | | 13/2 | < 1 | 15 | | 3 | | 3 | | 3 | |
| $I_{OH}$ | HCC types | 0/5 | 2.5 | | 5 | –2 | | –1.6 | | –1.15 | | mA |
| | | 0/5 | 4.6 | | 5 | –0.64 | | –0.51 | | –0.36 | | |
| | | 0/10 | 9.5 | | 10 | –1.6 | | –1.3 | | –0.9 | | |
| | | 0/15 | 13.5 | | 15 | –4.2 | | –3.4 | | –2.4 | | |
| | HCF types | 0/5 | 2.5 | | 5 | –1.53 | | –1.36 | | –1.1 | | |
| | | 0/5 | 4.6 | | 5 | –0.52 | | –0.44 | | –0.36 | | |
| | | 0/10 | 9.5 | | 10 | –1.30 | | –1.1 | | –0.90 | | |
| | | 0/15 | 13.5 | | 15 | –3.6 | | –3 | | –2.4 | | |

**Table I - STATIC ELECTRICAL CHARACTERISTICS 4000B and UB** (Cont'd)

| Parameter | | Test Conditions | | | | Values | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $V_O$ (V) | $I_O$ (μA) | $V_{DD}$ (V) | $T_{Low}$ | | 25°C | | $T_{High}$ | | |
| | | | | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $I_{OL}$ | HCC types | 0/5 | 0.4 | | 5 | 0.64 | | 0.51 | | 0.36 | | mA |
| | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | | 0.9 | | |
| | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | | 2.4 | | |
| | HCF types | 0/5 | 0.4 | | 5 | 0.52 | | 0.44 | | 0.36 | | |
| | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | | 0.9 | | |
| | | 0/15 | 1.5 | | 15 | 3.6 | | 3 | | 2.4 | | |
| $I_{IL}$ $I_{IH}$ | HCC types | 0/18 | Any input | | 18 | | ±0.1 | | ±0.1 | | ±1 | μA |
| | HCF types | 0/15 | | | 15 | | ±0.3 | | ±0.3 | | ±1 | |
| $I_{OL}$, $I_{OH}$ | HCC types | 0/18 | | | 18 | | ±0.4 | | ±0.4 | | ±12 | μA |
| | HCF types | 0/15 | | | 15 | | ±1.0 | | ±1.0 | | ±7.5 | |
| $C_I$ | | | | | | | | | 7.5 | | | pF |
| $C_{I\ (UB)}$ | | | | | | | | | 22.5 | | | pF |

## STANDARD JEDEC SPECIFICATIONS

**Table II - ABSOLUTE MAXIMUM RATINGS**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | –0.5 to 18 | V |
| $V_I$ | Input Voltage | –0.5 to $V_{DD}$ +0.5 | V |
| $I_I$ | DC input current (any input) | ± 10 | mA |
| $T_{stg}$ | Storage temperature range | –65 to 150 | °C |

**Table III - RECOMMENDED OPERATING CONDITIONS**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | 3 to 15 | V |
| $V_I$ | Input Voltage; | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating temperature – for extended range devices<br>– for intermediate range devices | –55 to 125<br>–40 to 85 | °C |

## Table IV - STATIC ELECTRICAL JEDEC CHARACTERISTICS

| Parameter | | Test Conditions | | | | Values | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_i$ (V) | $V_O$ (V) | $I_O$ (μA) | $V_{DD}$ (V) | $T_{Low}$ | | 25°C | | $T_{High}$ | | |
| | | | | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $I_L$ (gates) | HCC | | | | 5 | | 0.25 | | 0.25 | | 7.5 | μA |
| | | | | | 10 | | 0.5 | | 0.5 | | 15 | |
| | | | | | 15 | | 1 | | 1 | | 30 | |
| | HCF | | | | 5 | | 1 | | 1 | | 7.5 | |
| | | | | | 10 | | 2 | | 2 | | 15 | |
| | | | | | 15 | | 4 | | 4 | | 30 | |
| $I_L$ (buffer FF) | HCC | | | | 5 | | 4 | | 4 | | 30 | μA |
| | | | | | 10 | | 8 | | 8 | | 60 | |
| | | | | | 15 | | 16 | | 16 | | 120 | |
| | HCF | | | | 5 | | 4 | | 4 | | 30 | |
| | | | | | 10 | | 8 | | 8 | | 60 | |
| | | | | | 15 | | 16 | | 16 | | 120 | |
| $I_L$ (MSI) | HCC | | | | 5 | | 5 | | 5 | | 150 | μA |
| | | | | | 10 | | 10 | | 10 | | 300 | |
| | | | | | 15 | | 20 | | 20 | | 600 | |
| | HCF | | | | 5 | | 20 | | 20 | | 150 | |
| | | | | | 10 | | 40 | | 40 | | 300 | |
| | | | | | 15 | | 80 | | 80 | | 600 | |
| $V_{OL}$ | | 0/ 5 | | < 1 | 5 | | 0.05 | | 0.05 | | 0.05 | V |
| | | 0/10 | | < 1 | 10 | | 0.05 | | 0.05 | | 0.05 | |
| | | 0/15 | | < 1 | 15 | | 0.05 | | 0.05 | | 0.05 | |
| $V_{OH}$ | | 5/0 | | < 1 | 5 | 4.95 | | 4.95 | | 4.95 | | V |
| | | 10/0 | | < 1 | 10 | 9.95 | | 9.95 | | 9.95 | | |
| | | 15/0 | | < 1 | 15 | 14.95 | | 14.95 | | 14.95 | | |
| $V_{IL}$ | | | 0.5/4.5 | < 1 | 5 | | 1.5 | | 1.5 | | 1.5 | V |
| | | | 1/9 | < 1 | 10 | | 3 | | 3 | | 3 | |
| | | | 1.5/13.5 | < 1 | 15 | | 4 | | 4 | | 4 | |
| $V_{IH}$ | | | 4.5/0.5 | < 1 | 5 | 3.5 | | 3.5 | | 3.5 | | V |
| | | | 9/1 | < 1 | 10 | 7 | | 7 | | 7 | | |
| | | | 13.5/1.5 | < 1 | 15 | 11 | | 11 | | 11 | | |
| $I_{OL}$ | HCC | 0/5 | 0.4 | | 5 | 0.64 | | 0.51 | | 0.36 | | mA |
| | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | | 0.9 | | |
| | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | | 2.4 | | |
| | HCF | 0/5 | 0.4 | | 5 | 0.52 | | 0.44 | | 0.36 | | |
| | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | | 0.9 | | |
| | | 0/15 | 1.5 | | 15 | 3.6 | | 3 | | 2.4 | | |
| $I_{OH}$ | HCC | 0/5 | 4.6 | | 5 | –0.25 | | –0.2 | | –0.14 | | mA |
| | | 0/10 | 9.5 | | 10 | –0.62 | | –0.5 | | –0.35 | | |
| | | 0/15 | 13.5 | | 15 | –1.8 | | –1.5 | | –1.1 | | |
| | HCF | 0/5 | 4.6 | | 5 | –0.2 | | –0.16 | | –0.12 | | |
| | | 0/10 | 9.5 | | 10 | –0.5 | | –0.4 | | –0.3 | | |
| | | 0/15 | 13.5 | | 15 | –1.4 | | –1.2 | | –1.0 | | |
| $I_I$ | HCC | 0/15 | | | 15 | | ± 0.1 | | ± 0.1 | | ± 1 | μA |
| | HCF | 0/15 | | | 15 | | ± 0.3 | | ± 0.3 | | ± 1 | μA |
| $C_I$ | | | | | | | | | 7.5 | | | pF |

# MILITARY / CECC PRODUCTS

SGS-THOMSON is a leading supplier of high-reliability integrated circuits devoted to those applications (military, medical, telecom, nuclear instruments, aerospace etc.) where reliability must be guaranteed or certified for each and every lot. The philosophy of "zero failure" in hi-rel products has lead SGS-THOMSON to obtain approval from many important international inspection authorities: ESA/SCC, Italian Ministry of Defence, BSI, CECC, CNET, Association of Electronic Industries in Singapore, and so on.
Two of the additional screening procedures SGS-THOMSON can offer are standardized and are intended to provide the user with:

- a standard process flow to reduce costs and delivery time, due to the totally automated management of the production;
- logic families screened according to military specifications.

The two different screening levels are "SGS-THOMSON PLUS" and MIL STD 883C Lev. B. The former undergoes a level of screening between that of the standard production and the MIL STD 883C. Moreover all screening levels of CECC are available since SGS-THOMSON in an approved manifacturer. G-REL integrated circuits are supplied in hermetically sealed packages that have been developed to meet the requirements of military, aerospace and critical industrial applications.

Packages supplied include:

– ceramic dual in line metal sealed

– ceramic dual in line frit sealed

– ceramic leadless chip carrier

– ceramic flat

## SGS-THOMSON PLUS PROGRAM

CMOS 4000B is available screened according to the SGS-THOMSON PLUS flow chart described in Table 1. The SGS-THOMSON PLUS program is a modification of the MIL STD 883C maintaining a very high quality level with the right ratio quality/price for customers whose production is not intended for military applications demanding lot release and certification. The electrical screening is performed 100% before and after the Burn-in test. All the electrical parameters listed in the datasheets are 100% tested.

Group A acceptance tests are performed as shown in Table 2.

**Table 1- SGS-THOMSON PLUS SCREENING FLOW**

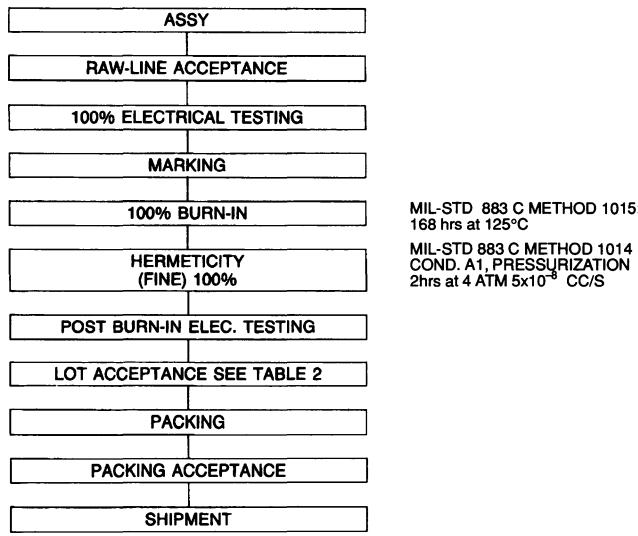


**Table 2 - OUTGOING QUALITY CONTROL**

| Test | Mil Std883c Method | Inspection Level | Acceptable Quality Level (AQL) | Notes |
|---|---|---|---|---|
| VISUAL & MECHANICAL | 2009 | I | 0.04 | CUMULATIVE MAJOR + MINOR DEFECTS |
| INOPERATIVE FAILURES PARAM. DC PARAM. AC | – | II | 0.04 | CUMULATIVE (INOPERATIVE + DC PARAMETERS OVER GUARANTEED TEMPERATURE RANGE) |
| RESISTANCE TO SOLVENTS | 2015 | S3 | 0.65 | |
| SOLDERABILITY | 2003 | S3 | 0.65 | |
| HERMETICITY | 1014 | II | 0.15 | FINE AND GROSS LEACAGES |

**MIL-STD 883 C LEVEL B**

All the HCC devices are available in ceramic packages, processed and screened according to the MIL-STD 883C Lev. B, flow chart shown in Table 3. Quality conformance inspection procedures are conducted as described in the Group A, B, C, and D tests of the MIL-STD 883C Method 5005.
A certificate of conformity is issued and included with each shipment.

**Table 3 - Screening Flow for MIL-STD-883C Lev. B Method 5004**

| Screen | Condition Method | REQMT |
|---|---|---|
| INTERNAL VISUAL | 2010 TEST COND. B | 100% |
| STABILIZATION BAKE | 1008 | 100% |
| TEMPERATURE CYCLING | 1010 TEST COND. C | 100% |
| CONSTANT ACCELERATION | 2001 TEST COND. E | 100% |
| SEAL: FINE GROSS | 1014 | 100% |
| PREBURN-IN ELECTRICAL PARAMETERS | PER APPLICABLE DEVICE SPECIFICATION | * |
| BURN-IN TEST | 1015 168 hrs 125°c | 100% |
| POST-BURN-IN ELECTRICAL PARAMETERS | PER APPLICABLE DEVICE SPECIFICATION | 100% |
| FINAL ELECTRICAL TEST:<br>STATIC TEST:<br>1. 25°C (SUBGROUP I, TABLE I 5005)<br>2. MAX AND MIN. RATED OPERATING TEMP. (SUBGROUP 2, 3 TABLE I 5005)<br>DYNAMIC TESTS AND SWITCHING TEST 25°C (SUBGROUP 4, 9 TABLE I, 5005) | PER APPLICABLE DEVICE SPECIFICATION | <br><br>100%<br>100%<br>100% |
| FUNCTIONAL TEST 25°C (SUBGROUP 7, TABLE I, 5005) | | 100% |
| EXTERNAL VISUAL | 2009 | 100% |

* 100% for devices which require data calculation as defined in MIL-STD-883C METHOD 5004.

## CECC QUALIFIED

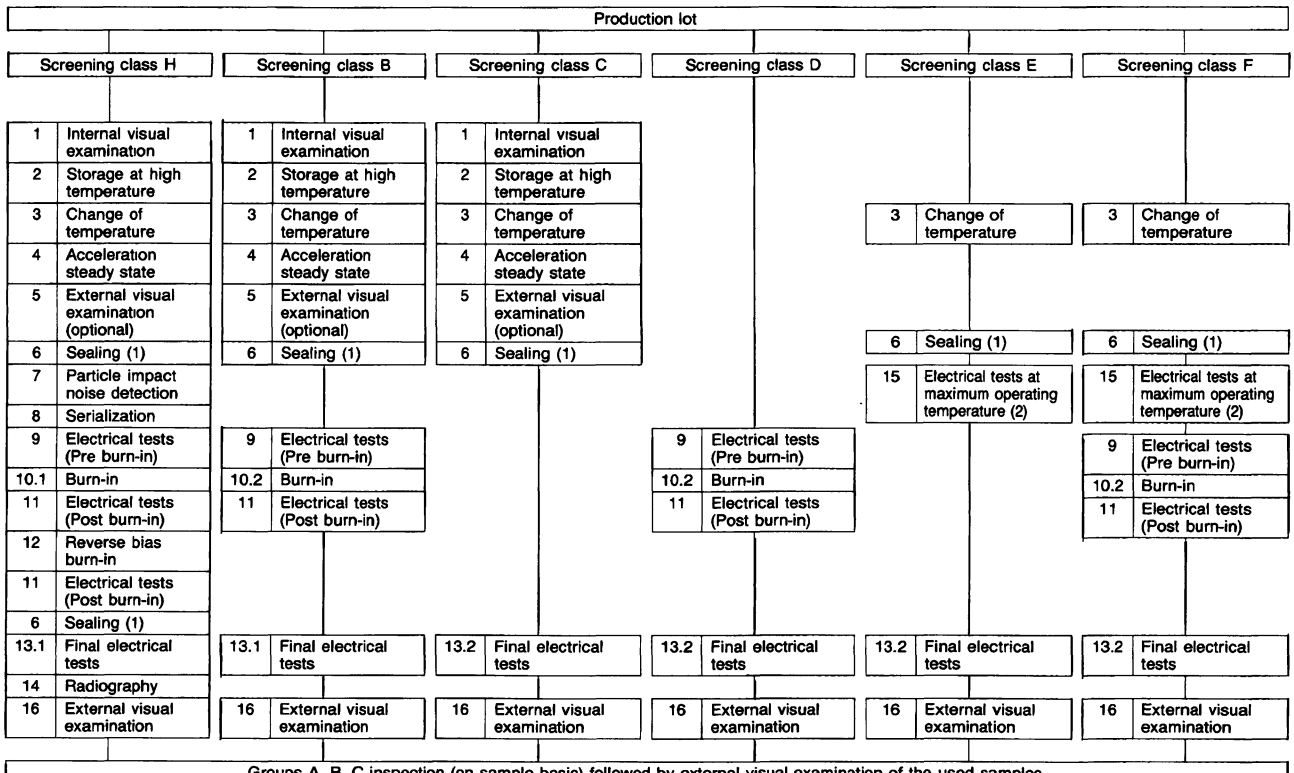
Most of the devices of CMOS 4000B family are available qualified and released according to CECC 90000 specifications. Each shipment is relased with the official CECC certificate and each device shows the official CECC logo. SGS-THOMSON offers screening according to levels B, C, D, E, F, and H. In all cases lot acceptance is made with AQLs according to the assessment level R which is the most severe.

The screening flow of all levels is shown in Tab. 4, 5, and 6.

**Table 4 - CECC SCREENS AND TESTS DESCRIPTION**

| Screen or Test Number | Screen or Test | Reference to CECC 90 000 Unless Otherwise Stated | Conditions |
|---|---|---|---|
| 1 | Internal visual examination | 4.2.1 | See Appendix A of CECC 90 000 |
| 2 | Storage at high temperature | 4.6.1 | $T = T_{stg}$ max.<br>t = 24 hrs min.<br>No final measurement |
| 3 | Change of temperature | 4.6.8 | $T_{min} = T_{stg}$ min.<br>$T_{max} = T_{stg}$ max<br>10 cycles. No final measurement |
| 4 | Acceleration steady state | 4.6.7 | Acceleration = 294 000 $m/s^2$ (30 000 $g_n$) unless otherwise specified<br>Direction = $Y_2$. No final measurement |
| 5 | External visual examination (optional) | 4.2.2 | 4.2.2 |
| 6 | Sealing a: tracer gas method with mass spectrometer<br>b: gross leak | 4.6.9.1<br>4.6.9.2 | Test QK<br>Test QC |
| 7 | Particle impact noise detection | under consideration | under consideration |
| 8 | Serialization | – | – |
| 9 | Electrical test (pre burn-in) | CECC 90 100 | As for Sub-Groups A2 and A3 of relevant DS unless specified |
| 10.1 | Burn-in | – | T = max. operating temperature, t = 240 hrs min.<br>Electrical conditions as specified in the DS |
| 10.2 | Burn-in | – | $T_{amb}$ = 125 °C unless otherwise limited by the technology when a lower limit is specified in the family or DS.<br>$t = 168^{+0}_{-8}$ hrs or any equivalent combination of it.<br>Electrical conditions as specified in the DS |
| 11 | Electrical tests (post burn-in) | – | As for Sub-Groups A2 and A3 of relevant DS unless otherwise specified.<br>The DS will prescribe the maximum deviations allowable from the results recorded in the preceding electrical tests |
| 12 | Reverse bias burn-in | – | $T_{amb}$ = 150 °C unless otherwise limited by the technology when a lower limit is specified in the family or Ds. t = 72 hrs min.<br>Electrical conditions as specified in the DS |
| 13.1 | Final electrical tests | – | As for Sub-Groups A2, A3, A4a, A4b, and A5 of the relevant DS |
| 13.2 | Final electrical tests | – | As for Sub-Groups A2 and A3 of the relevant DS |
| 14 | Radiographic | Under consideration | Under consideration |
| 15 | Electrical tests at max. operating temperature | – | As for Sub-Groups A4a of the relevant DS unless otherwise specified |
| 16 | External visual examination | 4.2.2 | 4.2.2 |

## Table 5 - SCREENING PROCEDURES: FLOW DIAGRAMS (Screen test number at left of each block)




(1) : Applies only for cavity devices (ceramic package)
(2) : Apply only for non-cavity devices (plastic package)

**Table 6 - CECC INSPECTION GROUPS AND TEST CONDITION**

| Examination or test | D<br>ND (1) | Inspection requirements | |
|---|---|---|---|
| GROUP A<br>INSPECTION | | Assessment levels | |
| | | R | |
| | | IL | AQL |
| **Sub-Group A1**<br>Visual examination | ND | I | 0.04 |
| **Sub-Group A2**<br>Verification of the function | ND | II | 0.04 |
| **Sub-Group A3**<br>Static characteristics at 25°C | ND | II | 0.04 |
| **Sub-Group A4a**<br>Static characteristics at maximum operating temperature | ND | II | 0.04 |
| **Sub-Group A4b**<br>Static characteristics at minimum operating temperature | ND | S-4 | 1.0 |
| **Sub-Group A5**<br>Dynamic characteristic at 25°C | ND | II | 0.065 |

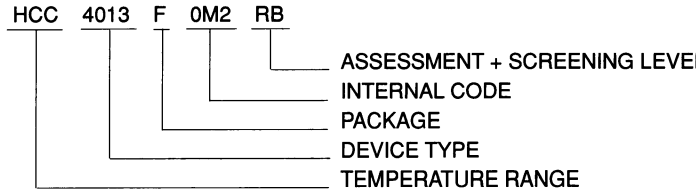
| GROUP B<br>INSPECTION | | Assessment levels | |
|---|---|---|---|
| | | R | |
| | | IL | AQL |
| **Sub-Group B1**<br>Dimensions | ND | S-4 | 1.0 |
| **Sub-Group B2**<br>Solderability | D | S-3 | 2.5 |
| **Sub-Group B3**<br>Sealing test | ND | II | 1.0 |
| **Sub-Group B4**<br>Change of temperature<br>Followed by:<br>1) For cavity packages:<br>Fine and gross leak test<br>2) For non-cavity packages:<br>Damp heat accelerated<br>End point tests:<br>Electrical tests as for Sub-Groups A2 and A3 | ND<br><br>ND<br><br>D | S-4 | 2.5 |
| **Sub-Group B5**<br>Electrical endurance 168hrs<br>End point tests:<br>Electrical tests as for Sub-Groups A2 and A3 | ND | S-4 | 1.5 |

**Note**: 1) D = Destructive test
ND = Non destructive test

For more detailed information see CECC 90-100 issue 2 specs.

# CECC CMOS

**ORDERING CODE:**




**TEMPERATURE RANGE**

| | |
|---|---|
| HCF | Standard ( – 40°C to + 85°C) |
| HCC | Extended ( – 55°C to + 125°C) |

**PACKAGES:**

| | |
|---|---|
| B | Plastic Dual in Line |
| F | Ceramic Dual in Line Frit Seal |
| K @ | Ceramic Flat (For Level RH only) |
| D @ | Ceramic Dual in Line Metal Sealed (For Level RH only) |
| Z @ | Ceramic Leadless Chip Carrier (CLCC - For Level RH only) |

@ = Production plant to be Qualified

**ASSESSMENT + SCREENING LEVELS**

| | |
|---|---|
| RB | See the Screening Levels Table on page 32 |
| RC * | See the Screening Levels Table on page 32 |
| RD | See the Screening Levels Table on page 32 |
| RE | See the Screening Levels Table on page 32 |
| RF | See the Screening Levels Table on page 32 |
| RH @ | See the Screening Levels Table on page 32 |

* = Available on big demand only.

@ = Production plant to be Qualified.

# DETAILED LIST OF APPROVED DEVICES

| Type | CECC Spec. N° | Type | CECC Spec. N° |
|---|---|---|---|
| 4001B | 90104 / 105 | 4060B | 90104 / 213 |
| 4002B | 90104 / 106 | 4066B | 90104 / 138 |
| 4006B | 90104 / 107 | 4068B | 90104 / 139 |
| 4007UB | 90104 / 108 | 4069UB | 90104 / 140 |
| 4008B | 90104 / 109 | 4070B | 90104 / 187 |
| 4011B | 90104 / 110 | 4071B | 90104 / 141 |
| 4012B | 90104 / 111 | 4072B | 90104 / 142 |
| 4013B | 90104 / 112 | 4073B | 90104 / 143 |
| 4014B | 90104 / 113 | 4075B | 90104 / 144 |
| 4015B | 90104 / 114 | 4076B | 90104 / 145 |
| 4016B | 90104 / 115 | 4077B | 90104 / 146 |
| 4017B | 90104 / 170 | 4078B | 90104 / 147 |
| 4018B | 90104 / 171 | 4081B | 90104 / 148 |
| 4019B | 90104 / 172 | 4082B | 90104 / 149 |
| 4020B | 90104 / 116 | 4085B | 90104 / 226 |
| 4021B | 90104 / 117 | 4093B | 90104 / 214 |
| 4022B | 90104 / 118 | 4094B | 90104 / 188 |
| 4023B | 90104 / 119 | 4098B | 90104 / 224 |
| 4024B | 90104 / 120 | 4099B | 90104 / 150 |
| 4025B | 90104 / 121 | 4502B | 90104 / 152 |
| 4027B | 90104 / 122 | 4503B | 90104 / 175 |
| 4028B | 90104 / 123 | 4508B | 90104 / 155 |
| 4029B | 90104 / 124 | 4510B | 90104 / 156 |
| 4030B | 90104 / 125 | 4511B | 90104 / 157 |
| 4032B | 90104 / 126 | 4512B | 90104 / 158 |
| 4034B | 90104 / 127 | 4514B | 90104 / 159 |
| 4035B | 90104 / 128 | 4515B | 90104 / 160 |
| 4038B | 90104 / 129 | 4516B | 90104 / 161 |
| 4040B | 90104 / 130 | 4517B | 90104 / 162 |
| 4042B | 90104 / 185 | 4518B | 90104 / 163 |
| 4043B | 90104 / 186 | 4520B | 90104 / 165 |
| 4044B | 90104 / 132 | 4527B | 90104 / 168 |
| 4046B | 90104 / 212 | 4532B | 90104 / 178 |
| 4047B | 90104 / 225 | 4536B | 90104 / 218 |
| 4049UB | 90104 / 133 | 4538B | 90104 / 179 |
| 4050B | 90104 / 134 | 4555B | 90104 / 199 |
| 4051B | 90104 / 135 | 4556B | 90104 / 181 |
| 4052 | 90104 / 136 | 4585B | 90104 / 203 |
| 4053 | 90104 / 137 | | |

# HARMONIZED SYSTEM OF QUALITY ASSESSMENT FOR ELECTRONIC COMPONENTS
CECC ECQAC

## CERTIFICATE OF APPROVAL OF MANUFACTURER

REGISTRATION NUMBER: **P 0018** ISSUE NUMBER: **3**

OF **SGS-THOMSON Microelectronics S.r.l.**

AT THEIR PLACE(S) OF WORK **Stradale Primosole, 50**
**I-95121 CATANIA**

IN RESPECT OF GENERIC/SECTIONAL SPECIFICATION CECC NUMBER: **90000**
TITLE: **- MONOLITHIC INTEGRATED CIRCUITS**

THE ORGANIZATION, FACILITIES AND INSPECTION PROCEDURES AT THE ABOVE PLACE OF WORK HAVE BEEN FOUND TO COMPLY WITH THE REQUIREMENTS OF DOCUMENT CECC 00 100 FOR QUALITY ASSESSMENT IN RESPECT OF THE FAMILIES OF COMPONENTS LISTED IN THE APPROVAL DOCUMENT(S) **NO 9090SGSC**
THIS CERTIFICATE DOES NOT AUTOMATICALLY ENTITLE THE MANUFACTURER TO USE THE MARK OR CERTIFICATE OF CONFORMITY. THE APPROVAL OF ANY PARTICULAR TYPE OF ELECTRONIC COMPONENT IS THE SUBJECT OF A SEPARATE CERTIFICATE.

PLACE: **MILANO**

DATE: **27 September 1990**

I M Q
ISTITUTO ITALIANO DEL MARCHIO DI QUALITÀ

**CECC**
CENELEC Electronic Components Committee

**ECQAC**
Electronic Components Quality Assurance Committee

NOTE: This certificate is valid only in conjunction with the approval document(s) **No 9090SGSC**

This approval and this Certificate may be suspended or withdrawn in accordance with CECC 00 100 implemented in CEI - CCE 00 100.
They may be suspended or withdrawn if no capability approval or qualification approval of a Components has been granted within one year of its date of issue.
This certificate remains the property of the body which granted it.

**IMQ**
20138 Milano - Via Quintiliano 43

ISTITUTO ITALIANO DEL MARCHIO DI QUALITÀ

Mod 286 - 100 - 5-89 - Ach

SGS-THOMSON MICROELECTRONICS

# RADIATION HARDENED PRODUCTS

Radiation Hardened versions of **HCC 4000** series types are offered by SGS-THOMSON for special applications in Space, Biomedical and Military fields.

These devices are supplied in accordance to the relevant Hi-Rel processing and screening specifications requested in the particular field (MIL 883, SCC9000, etc) and are electrically and mechanically identical to their non-hardened equivalent.

The actual radiation resistance of SGS-THOMSON RAD-HARD C-MOS parts can vary slightly from lot to lot and from type to type, but has repeatedly been demonstrated (see fig. 1) to be far in excess of the limit of 100K rads, normally requested for space and choosen by SGS-THOMSON as a standard reference for certification.

By changing the diffusion of the basic CMOS process, a rad-hard capability of total dose is achieved up to $1.10^5$ rads (Si). These rad-hard devices are processed according to ESA/SCC 9000 specifications and these types are subjected to a special process that monitors the tolerances more efficiently. The flow-chart is shown in Table 1.

The radiation exposure changes the levels of threshold voltages and leakage currents as shown in the figure below, thus a different diffusion process is necessary to monitor the effects of the radiation. Pre-and post-radiation measurements are made of threshold, threshold delta, leakage current and go, no-go functional tests in order to ensure that shift and absolute values are within the specified limits. ESA/SCC screening levels and tests are shown in the following pages.

See list of qualified devices, page 45.

**Fig. 1 - Example of Thereshold drifts versus radiation dose as measured on a sample of SGS-THOMSON RAD-HARD production tested by an independent laboratory. Parts tested were guaranteed to withstand 100K rads, but all show voltage thereshold shifts well inside radiation spec limits even at 300K rads (courtesy Hahn Meithner Institute, Berlin).**

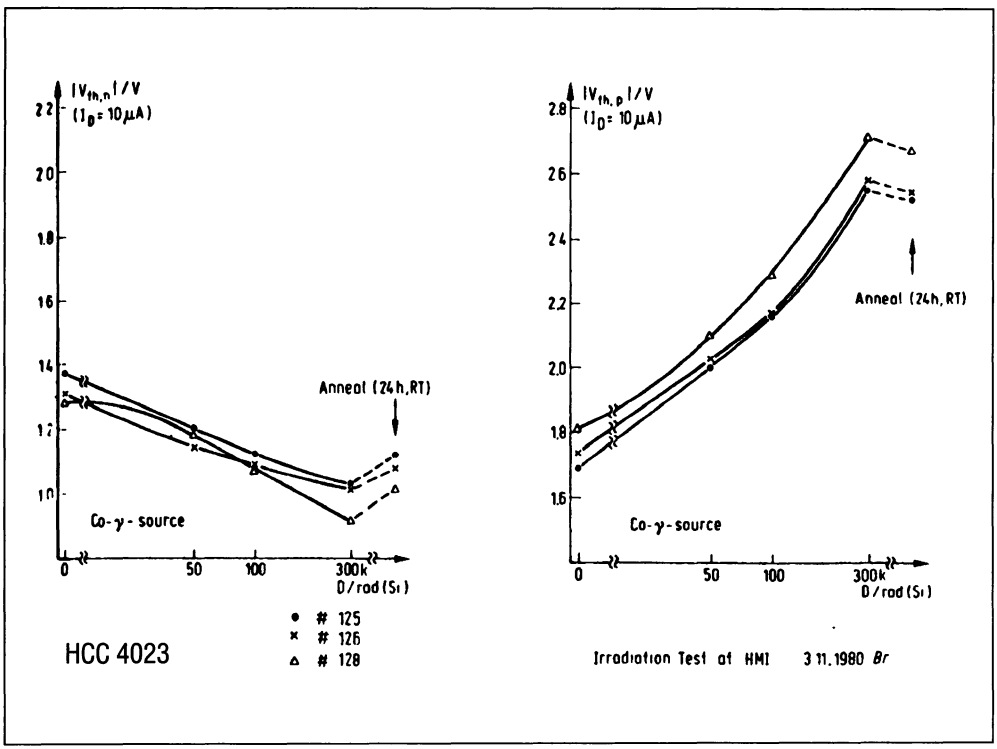


**Table 1 - ESA/SCC GENERIC SPECIFICATION 9000**

CHART II - FINAL PRODUCTION TEST

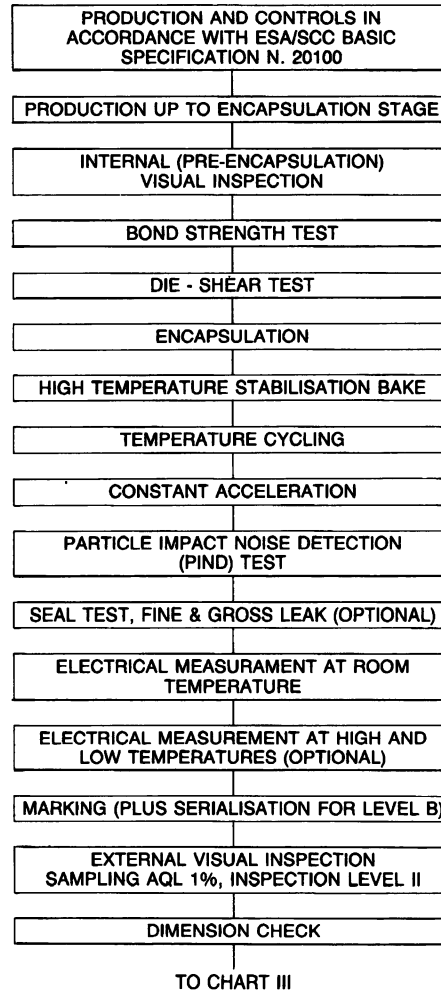
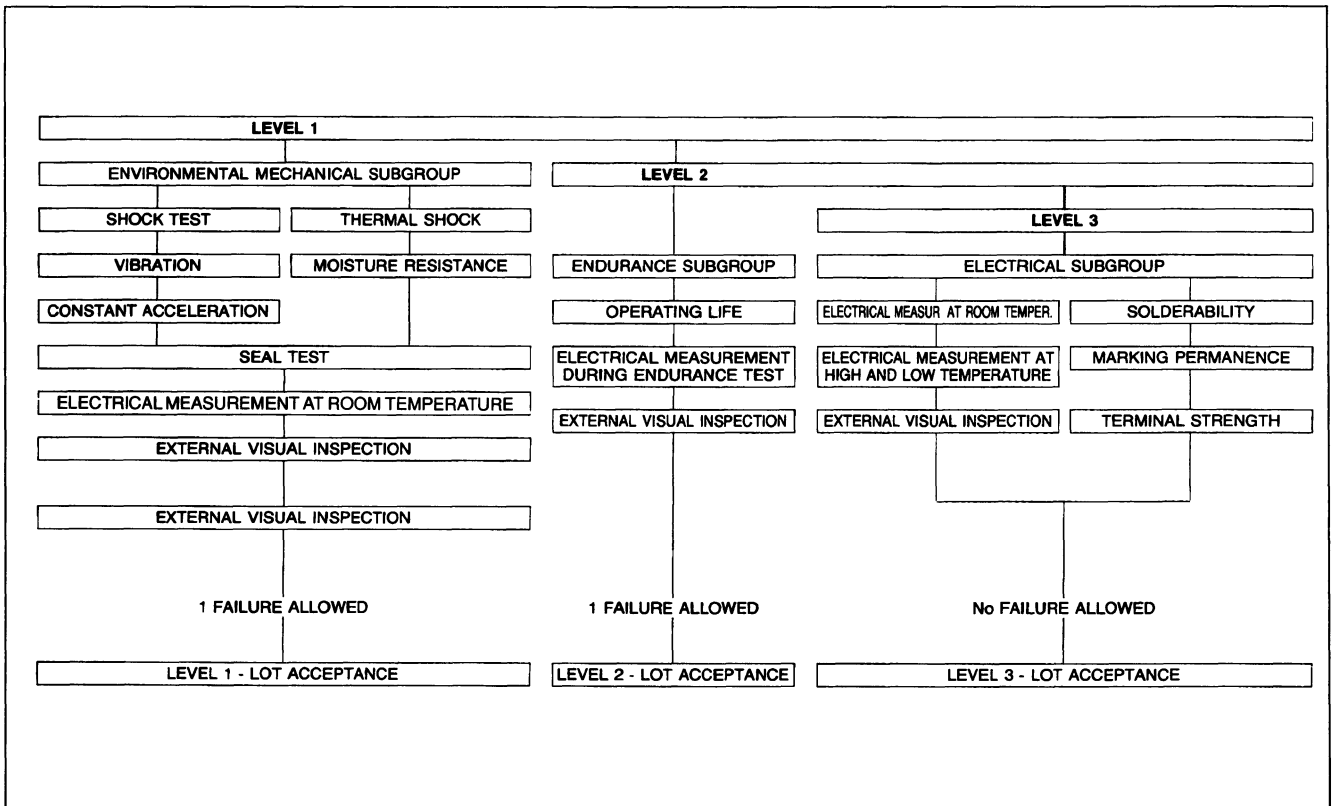


CHART III - BURN-IN – AND ELECTRICAL MEASUREMENTS

| | TESTING LEVELS B | TESTING LEVELS C |
|---|---|---|
| COMPONENTS FROM FINAL PRODUCTION TEST | | |
| PARAMETER DRIFT VALUE (INITIAL MEASUREMENTS) | X | |
| HIGH TEMPERATURE REVERSE BIAS BURN-IN | X | X |
| PARAMETER DRIFT VALUE (INTERMEDIATE MEASUREMENTS) | X | |
| POWER BURN-IN (240 hours - LEVEL "B" / 168 hours - LEVEL "C") | X | X |
| PARAMETER DRIFT VALUE (FINAL MEASUREMENTS) | X | |
| ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES | X | X |
| ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE | X | X |
| RADIOGRAPHIC INSPECTION | X | |
| SEAL TEST (FINE AND GROSS LEAK) | X | X |
| EXTERNAL VISUAL INSPECTION | X | X |
| CHECK FOR LOT FAILURE | X | X |

TO CHART V

CHART V - LOT ACCEPTANCE TEST




Note: Level 1 includes Level 2 and Level 3
Level 2 includes Level 3

european space agency
agence spatiale européenne

# Certificate of Qualification No. 73 D

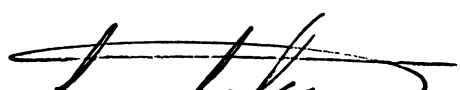
This is to certify that SGS-THOMSON, Rennes, France

has been qualified by ESA for the supply of Integrated Circuits C MOS B Series (See ESA/SCC QPL for Types)

for use in ESA space programmes, according to ESA/SCC Generic Specification 9000 and applicable Detail Specifications (See ESA/SCC QPL)

as recommended by the Space Components Coordination Group.
This certificate is valid until April 1992.

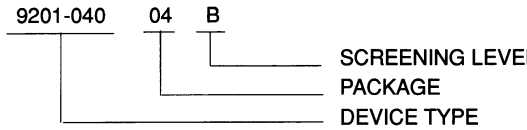
Head of Product Assurance
and Safety Department



Date
9 April 1990

# RADIATION-HARDENED CMOS

**ORDERING CODE:**




**SCREENING LEVELS:**

| | |
|---|---|
| B | See Chart III, Page 41 |
| C | See Chart III, Page 41 |

**PACKAGES:**

| | |
|---|---|
| 01 | Ceramic Flat Gold Plated |
| 02 | Ceramic Flat Tin Plated |
| 03 | Ceramic Dual in Line Metal Sealed Gold Plated |
| 04 | Ceramic Dual in Line Metal Sealed Tin Plated |
| 07 | Leadless Ceramic Chip Carrier (LCCC) |

**MARKING:**

Parts are marked with the ordering code.

# DETAILED LIST OF APPROVED DEVICES

| Type | SCC Spec. N° | Type | SCC Spec. N° | Type | SCC Spec. N° |
|---|---|---|---|---|---|
| 4000B | 9201 / 040 | 4021B | 9306 / 016 | 4069UB | 9401 / 010 |
| 4001B | 9201 / 041 | 4022B | 9204 / 023 | 4070B | 9201 / 048 |
| 4002B | 9201 / 042 | 4023B | 9201 / 045 | 4071B | 9201 / 063 |
| 4006B | 9306 / 013 | 4024B | 9204 / 024 | 4072B | 9201 / 082 |
| 4007UB | 9202 / 038 | 4025B | 9201/046 | 4073B | 9201 / 064 |
| 4008B | 9202 / 039 | 40257B | 9408 / 017 | 4075B | 9201 / 065 |
| 40101B | 9208 / 002 | 4026B | 9406 / 001 | 4076B | 9306 / 022 |
| 40103B | 9204 / 036 | 4027B | 9203 / 022 | 4077B | 9201 / 055 |
| 40104B | 9306 / 040 | 4028B | 9205 / 010 | 4078B | 9201 / 062 |
| 40105B | 9306 / 033 | 4029B | 9204 / 025 | 4081B | 9201 / 052 |
| 40106B | 9409 / 005 | 4030B | 9201 / 047 | 4082B | 9201 / 066 |
| 40107B | 9401 / 013 | 4031B | 9306 / 017 | 4085B | 9201 / 067 |
| 40108B | 9306 / 034 | 4034B | 9306 / 025 | 4086B | 9201 / 068 |
| 40109B | 9407 / 003 | 4035B | 9306 / 018 | 4089B | 9202 / 060 |
| 4011B | 9201 / 043 | 4040B | 9204 / 026 | 4093B | 9409 / 002 |
| 4012B | 9201 / 044 | 4041UB | 9202 / 040 | 4094B | 9306 / 026 |
| 4013B | 9203 / 023 | 4042B | 9202 / 041 | 4098B | 9206 / 003 |
| 4014B | 9306 / 014 | 4043B | 9202 / 042 | 4099B | 9202 / 058 |
| 4015B | 9206 / 015 | 4044B | 9202 / 043 | 4502B | 9401 / 006 |
| 4016B | 9202 / 050 | 4046B | 9202 / 026 | 4503B | 9401 / 030 |
| 40160B | 9204 / 047 | 4047B | 9207 / 003 | 4508B | 9202 / 063 |
| 40161B | 9204 / 054 | 4049B | 9201 / 054 | 4510B | 9204 / 053 |
| 4017B | 9204 / 020 | 4049UB | 9202 / 045 | 4512B | 9408 / 006 |
| 40174B | 9203 / 038 | 4050B | 9202 / 046 | 4514B | 9408 / 012 |
| 4018B | 9204 / 021 | 4051B | 9202 / 047 | 4515B | 9205 / 011 |
| 40181B | 9202 / 068 | 4052B | 9202 / 048 | 4516B | 9204 / 045 |
| 40182B | 9202 / 069 | 4053B | 9202 / 049 | 4518B | 9204 / 013 |
| 4019B | 9202 / 051 | 4060B | 9204 / 052 | 4520B | 9204 / 028 |
| 40193B | 9204 / 041 | 4063B | 9209 / 001 | 4527B | 9408 / 026 |
| 40194B | 9306 / 032 | 4068B | 9408 / 005 | 4532B | 9202 / 065 |
| 4020B | 9204 / 022 | 4067B | 9408 / 009 | 4555B | 9408 / 011 |
| 40208B | 9301 / 009 | 4069B | 9201 / 061 | 4556B | 9408 / 025 |

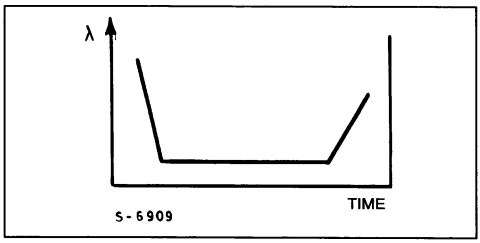
# RELIABILITY REPORT

## RELIABILITY AND FAILURE MECHANISMS FUNDAMENTALS

-Through accelerated stresses we ascertain the value of the components failure rates, in terms of how many devices (in percent) are expected to fail every 1000 hours of operation (λ or F.R.)

-Failure rate versus time of activity shows the well-known trend.

-Failure rate



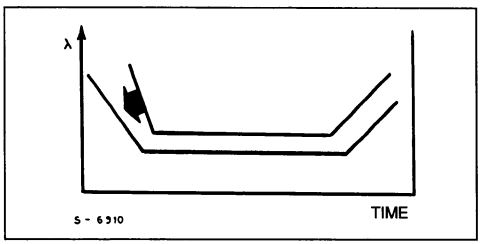

During the first time period the products are affected by the so-called "infant mortality" intrinsic to all semiconductor technologies. End users are very sensitive to this parameter which causes early operational failures in their equipment.

## TARGETS

SGS-THOMSON periodically reviews and publishes lifetime results; at this time a new set of failure rate targets are being defined. These targets are translated into actual required test hours.

The goal is a steady shift of the limits.

**Failure rate λ**




## TESTS

With accelerated tests we define the failure rate of the products, then, derating the data for different conditions, we know the life expectancy under the actual operating conditions.

In its simplest form the failure rate (at a given temperature) is:

$$F.R. = \frac{N}{D \cdot H} \qquad (1)$$

Where N = Number of failures
D = Number of components
H = Number of testing hours

If we intend to determine the failure rate at other temperatures an acceleration factor must be considered.
Some tests are accelerated by means of increased temperature, based on the assumption of the Arrhenius law:

$$F.R. = Ae^{-Ea/KTj} \qquad (2)$$

A = Constant

Ea = Activation energy

K = Boltzman's constant

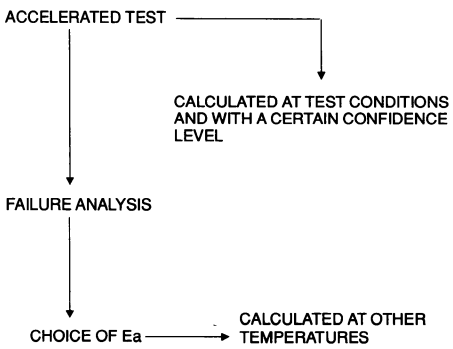
Tj = Junction Absolute temperature

For two different temp. $F.R.(T_1)=F(T_1, T_2)F.R.(T_2)$

from (2) it is: $$F(T_1,T_2) \equiv EXP\left[\frac{-Ea}{K}\left(\frac{1}{T_1}-\frac{1}{T_2}\right)\right] \quad (3)$$

Clearly the choice of an appropriate activation energy, Ea is of paramount importance.
The different mechanisms which could lead to circuit failure are characterized by specific activation energies whose values are published in the relevant literature.

THUS THE CORRECT PROCEDURE IS



Arrhenius equation (2) describes the rate of many processes responsible for degradation and failure of electronic components; it follows that if the transition of an item from an initial stable condition to a defined degraded state occurs by a thermally activated mechanism, then the time for the transition is given by an equation of the form:

MTBF = B EXP (Ea/Kt)

MTBF = Mean time between failure

B = Temperature-independent constant

MTBF can be defined as the time to suffer a device degradation. The dramatic effect of the choice of the Ea value can be seen by plotting equation (2).

The acceleration effect of a 125°C device junction test with respect to 70°C actual device junction operation is equal to a factor of 100 for Ea = 1eV and respectively 4 for Ea = 0.3eV.

Some words of caution are needed about published values of Ea:

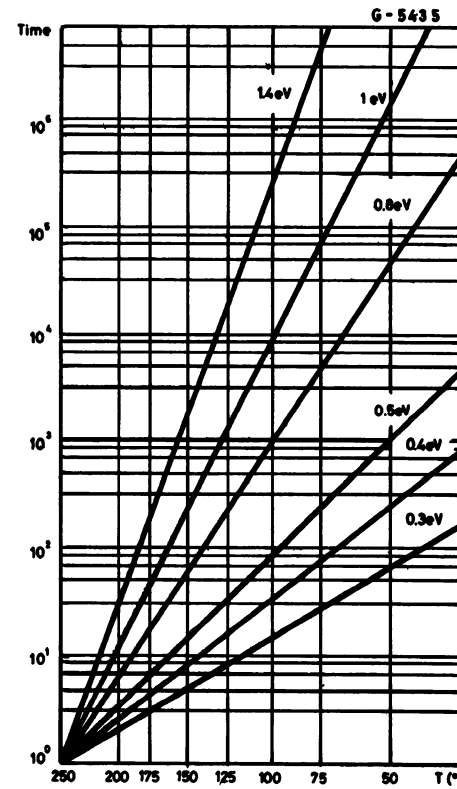
A)They are often related to high temperature test where a single Ea (with high value) mechanism has become significant.

B)They are specifically related to the devices produced by that supplier (and to its technology) and in that period of time.

C)They could be modified by the mutual action of other stresses (voltage, mechanical)

D)Field device-application conditions should be considered.

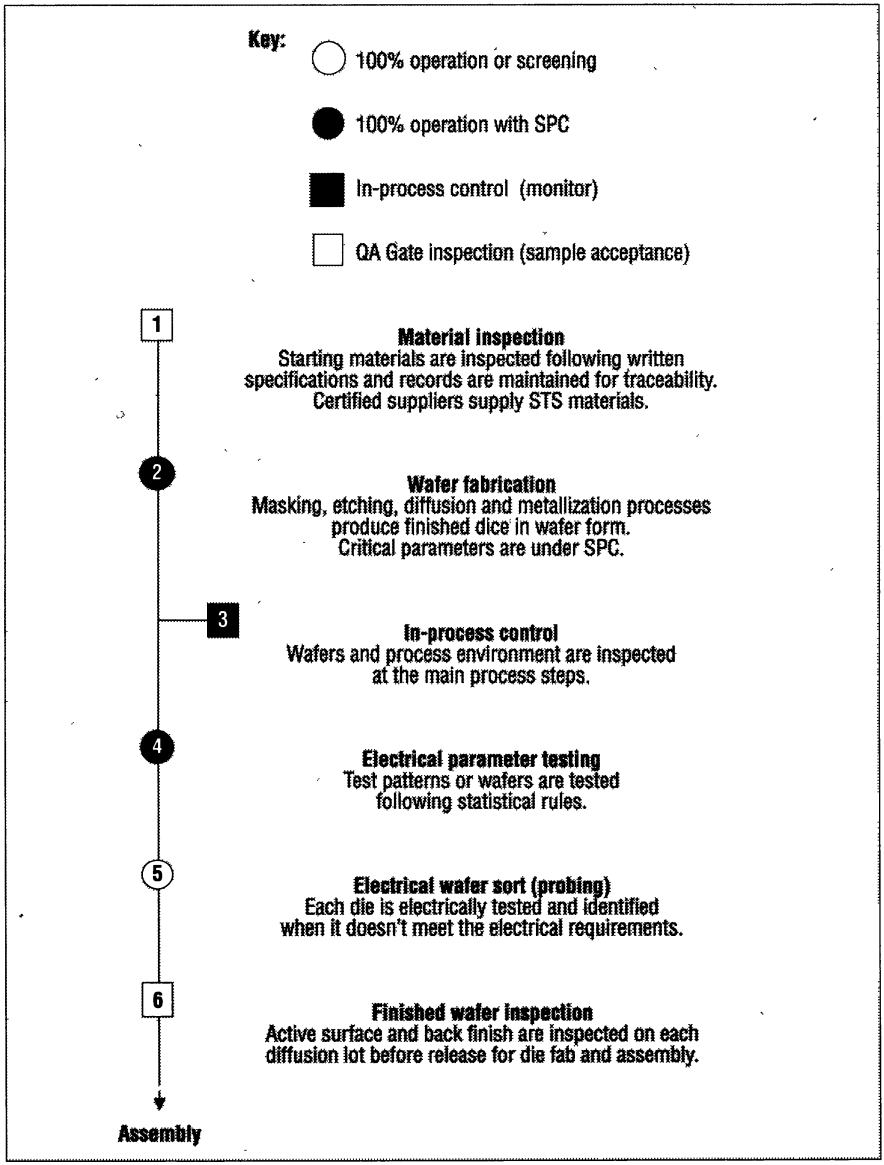
**Life-Hours**




**Main Failure modes and relevant activation energies**

| Failure Mode | Activation Energy (eV) | Accelerating |
|---|---|---|
| SURFACE CHARGE | 1.0 - 1.05 | HIGH TEMPERATURE BIAS |
| IONIC CONTAMINATION | 1.0 - 1.4 | HIGH TEMPERATURE BIAS |
| DIELECTRIC DEFECTS | 0.3 - 0.6 | HIGH TEMPERATURE BIAS |
| ELECTROMIGRATION | 0.5 - 1.2 | HIGH TEMPERATURE BIAS |
| INTERMETALLIC GROWTH | 1.0 - 1.05 | HIGH TEMPERATURE BIAS, STORAGE |
| METAL CORROSION | 0.3 - 0.8 | HIGH HUMIDITY BIAS |

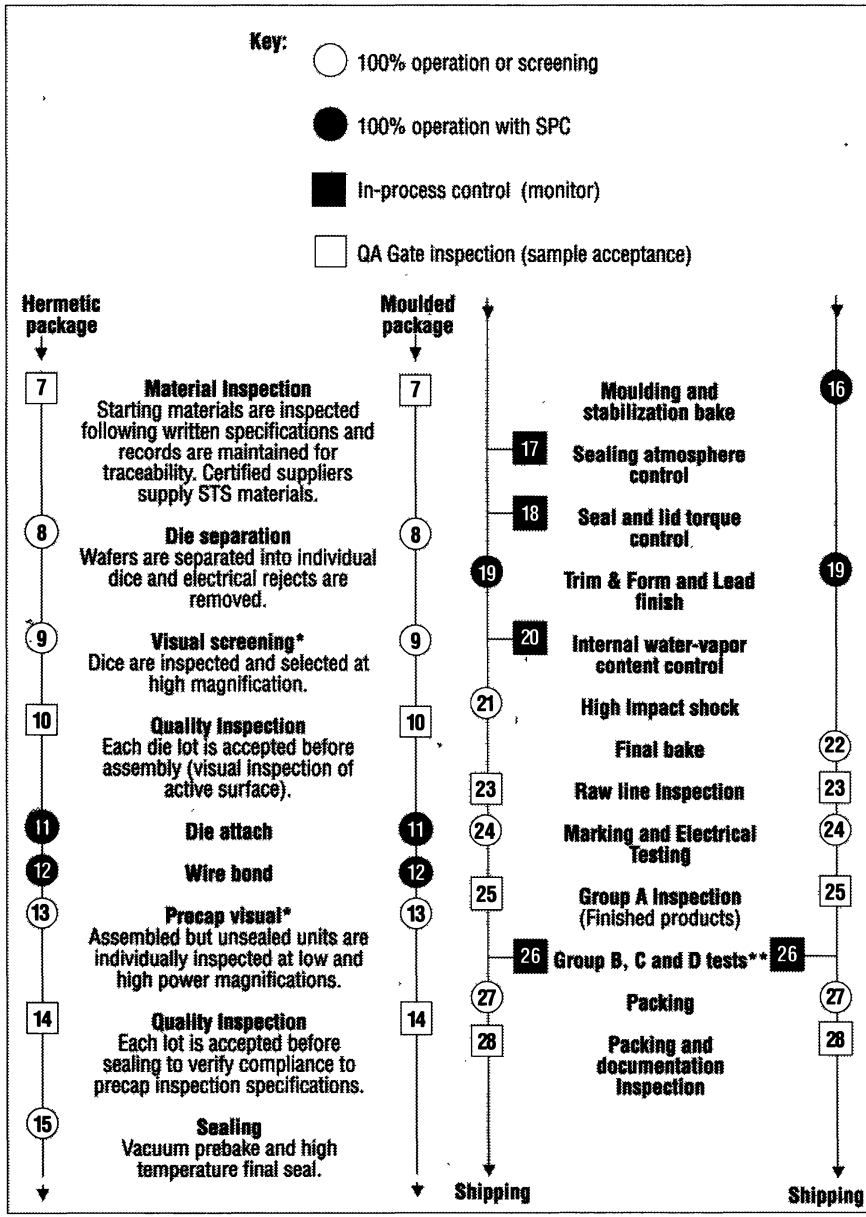
## WAFER FAB TYPICAL PRODUCTION PROCESS FLOW CHART



**In-process control during wafer fabrication**
The table emphasizes the most important fabrication steps with the relevant SPC measures and/or monitors performed.

| PROCESS STEPS | IN-PROCESS INSPECTIONS/MONITORS |
|---|---|
| OXIDATION | – Visual<br>– Thickness<br>– Refractive Index<br>– CV plot (stability of ionic concentration and contamination control) |
| DEPOSITION: Nitride, Poly Si | – Visual<br>– Thickness<br>– Refractive index<br>– Doping content |
| PHOTOLITHOGRAPHY | – Mask and wafer cleanliness<br>– Alignment and focusing accuracy<br>– Critical dimensions |
| ETCHING | – Quality of etching and wafer cleanliness<br>– Critical dimensions |
| DOPING BY IMPLANT (P, As, B) | – Sheet resistance (dose and implant uniformity) |
| DOPING BY DIFFUSION ($POCl_3$, As) | – Sheet resistance<br>– Thickness<br>– CV plot (stability of ionic concentration and contamination control) |
| EPITAXIAL GROWTH | – Thickness<br>– Resistivity<br>– Crystal quality (stacking faults, bumps and others) |
| METALLIZATION | – Wafer cleanliness<br>– Visual<br>– SEM (step coverage and film quality)<br>– Thickness<br>– CV plot (stability of ionic concentration and contamination control) |
| INTERMEDIATE AND FINAL PASSIVATION | – Thickness<br>– Doping content<br>– Passivation integrity (density of pinholes and cracks)<br>– Visual |
| BACK FINISHING | – Wafer thickness<br>– Back metal thickness<br>– Metal adherence |
| ELECTRICAL CHARACTERIZATION | – Main parameters for active and parasitic structures (e. g. threshold voltage, saturation current, $h_{FE}$, resistances, capacitances ...) |
| WAFER INSPECTION | – Visual (microscope and/or laser surface inspection system) |
| ALL DEPOSITIONS AND PHOTOLITHOGRAPHY | – Surface Scan (to detect and to measure foreign particles) |

## ASSEMBLY TYPICAL PRODUCTION PROCESS FLOW CHART




* Omitted when the intrinsic quality meets the specified quality level

** For non military products, these reliability tests can be performed after step 23 on 100% electrically tested samples (when requested)

**In-process control during assembly process**

The table emphasizes the most important fabrication steps with the relevant SPC measures and/or monitors performed.

| PROCESS STEPS | TESTS | DESCRIPTION |
|---|---|---|
| 11 | DIE ATTACH | –Integrated Circuits<br>MIL-STD-883 Method 2010 cond B (internal visual) and Method 2019 (die shear strength); CECC 90000<br>–Discrete Devices<br>MIL-STD-750 Method 2072 (internal visual) and Method 2017 (die shear strength); CECC 50000 |
| 12 | WIRE BOND | – Integrated Circuits<br>MIL-STD-883 Method 2010 cond. B (internal visual) and Method 2011 cond. D (bond strength); CECC 90000<br>– Discrete Devices<br>MIL-STD-750 Method 2072 (internal visual) and Method 2037 (bond strength); CECC 50000 |
| 14 | QUALITY INSPECTION | – Integrated Circuits<br>MIL-STD-883 Methods 2010 cond. B (internal visual); CECC 90000<br>–Discrete Devices<br>MIL-STD-750 Method 2072 (internal visual); CECC 50000 |
| 16 | MOULDING AND STABILIZATION BAKE | – Visual and temperature process control |
| 17 | SEALING ATMOSPHERE CONTROL | Moisture content:<br>< 200 ppm for Ceramic packages<br>< 100 ppm for Metal Can packages |
| 18 | SEAL CONTROL | Fine Leak<br>– Integrated Circuits<br>MIL-STD-883 Method 1014 cond. A1<br>Helium leak detector after pressurization in He for:<br>2h at 5.1 atm Limit: $5 \times 10^{-8}$ cc/s for ICV < 0.05 cc<br>4h at 5.1 atm Limit: $5 \times 10^{-8}$ cc/s for ICV ≥ 0.05 < 0.5 cc<br>2h at 3.0 atm Limit: $1 \times 10^{-7}$ cc/s for ICV ≥ 0.5 < 1cc<br>5h at 3.0 atm Limit: $5 \times 10^{-8}$ cc/s for ICV ≥ 1 < 10cc<br>ICV = Internal Cavity Volume<br>– Discrete Devices<br>MIL-STD-750 Method 1071 cond. H1<br>Helium leak detector after pressurization in He for:<br>2h at 4.1 atm Limit: $5 \times 10^{-8}$ cc/s for ICV < 0.4 cc<br>2h at 4.1 atm Limit: $2 \times 10^{-7}$ cc/s for ICV ≥ 0.4 cc<br>4h at 2.0 atm Limit: $1 \times 10^{-7}$ cc/s for ICV ≥ 0.4 cc<br>Gross Leak<br>– Integrated Circuits<br>MIL-STD-883 Method 1014 cond. C1 (fluorocarbon gross leak)<br>5 Torr vacuum for 30 minutes minimum followed by pressurization of the devices immersed in mineral oil and subsequent immersion in another mineral oil at Ta = 125°C<br>– Discrete Devices<br>MIL-STD-750 Method 1071 cond. C (fluorocarbon gross leak)<br>0.5 Torr vacuum for 1h, except for ICV ≥ 0.1 cc, followed by pressurization of the devices immersed in mineral oil at:<br>4.1 atm for 2h ICV ≤ 0.1 cc or<br>5.1 atm for 2h ICV ≥ 0.1 cc<br>and subsequent immersion in mineral oil at Ta = 125°C |

**In-process control during assembly process** (cont'd)

| PROCESS STEPS | TESTS | DESCRIPTION |
|---|---|---|
| 18 (cont.d) | LID TORQUE CONTROL | Ceramic packages only<br>MIL-STD-883 Method 2024<br>(e.g. ≥ 60 Kg x cm for seal area values between 1.41 and 1.73 $cm^2$) |
| 19 | TRIM & FORM AND LEAD FINISH | – Trim & Form not for Metal Can packages<br>– Dimensions, thickness and contamination control<br>– Solderability control:<br>Aging as per page 51<br>215 ± 5°C for 3 ± 0.5 sec. (SMD only)<br>235 ± 5°C for 2 ± 0.5 sec.<br>245 ± 5°C for 5 ± 0.5 sec. |
| 20 | INTERNAL WATER VAPOR CONTENT CONTROL | Dew Point method MIL-STD-883 Method 1018 procedure 3<br>5000 ppm max (dew point temperature less than - 15°C)<br>Ceramic packages only |
| 21 | HIGH IMPACT SHOCK | Metal Can packages only (except TO3)<br>20000 g minimum; t = 25μ sec. minimum; Y1 axis only |
| 22 | FINAL BAKE | For SMD only (according to internal specifications) |
| 23 | RAW LINE INSPECTION | External Visual<br>– Integrated Circuits<br>MIL-STD-883 Method 2009; CECC 90000<br>– Discrete Devices<br>MIL-STD-750 Method 2071; CECC 50000<br><br>Note: at this step some reliability tests (pressure pot, temperature cycling, life test etc.) are performed as a monitor, generally on a weekly basis, to have fast feedback on process behaviour (Real Time Control Tests) |
| 25 | GROUP A INSPECTION | See page 56 |
| 26 | GROUPS B, C AND D TESTS | Performed on the product family representative types (by rotation); the results are extended to all the other devices of the same family according to the structure similarity concept |
| 28 | PACKING AND DOCUMENTATION INSPECTION | Inspection for:<br>– right quantity<br>– right type<br>– right boxing<br>– right labelling<br>– right documentation<br>– various |

### GROUP A INSPECTION - FINISHED PRODUCT ACCEPTANCE

ICs and Discrete devices

| SUBGROUP | PARAMETERS | MINIMUM SAMPLE SIZE | ACCEPTANCE NUMBER |
|---|---|---|---|
| A1 | Visual and mechanical inspection | 315 | 0 |
| A2+A3+A4 | Cumulative electrical and inoperative mechanical failures | 315 | 0 |

Notes
- This product acceptance is valid for standard production, for agreed customer programs other sampling plans can be applied
- Specified temperature ranges according to SGS-THOMSON databooks

### PPM (RESULTS AND TARGETS)

As a consequence of its quality improvement programmes SGS-THOMSON has continually improved outgoing quality and is pursuing ambitious quality targets.

**PPM values and targets for cumulative electrical failures*** (inoperative mechanical included)

| | | | | | | |
|---|---|---|---|---|---|---|
| CMOS | 1986 | 1987 | 1988 | 1989 | 1990 | 1991 |
| | 75 | 60 | 40 | 30 | 20 | 10 |

* Values referred to the end of each year.

## GROUPS B, C AND D TESTS

### Integrated circuits - Groups B, C and D tests

Every week or every three months on raw line and/or finished products

| SUBGROUP | TEST PROCEDURE | MIL-STD-883 METHOD | CECC 90000 METHOD | SGS-THOMSON TEST CONDITIONS | PACKAGE | | | MINIMUM SAMPLE SIZE | ACCEPTANCE NUMBER (c) | NOTES |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | METAL | CERAMIC | PLASTIC | | | (1) |
| 1 | Physical dimension | 2016 | 4.3 | Data Sheet Drawing | x | x | x | 2 | 0 | |
| 2 | Resistance to solvents | 2015 | 4.4 | 1 minute immersion in solvent solution followed by 10 strokes with a hard brush as per MIL-STD method (the procedure shall be repeated 3 times) | x | x | x | 4 | 0 | |
| 3 | Solderability | 2003 | 4.6.10 Cond 1 | 215 ±5°C 3 ±0.5sec.<br>235 ±5°C 2 ±0.5sec.<br>245 ±5°C 5 ±0.5sec. | –<br>x<br>x | –<br>x<br>x | x<br>x<br>x | 22 | 0 | 2 |
| 4 | Operating Life Test<br>or<br>Intermittent Life Test (for Power devices)<br>end point electrical parameters | 1005<br><br>–<br> | 4.8<br><br>–<br> | 1000 h according to detail spec<br><br>5000 Cycles<br>as per device spec. | x<br><br>–<br>x | x<br><br>–<br>x | x<br><br>x<br>x | 45 | 0 | 3 |
| 5 | Temperature cycling<br>Constant acceleration<br>Seal - fine<br>- gross | 1010<br>2001<br>1014 | 4.6.8<br>4.6.7<br>4.6.9 | 10 cycles Ta = -65°C to + 150°C<br>30000 g<br>see page 38 | x<br>x<br>x | x<br>x<br>x<br>x | –<br>–<br>–<br>– | 22 | 0 | <br>4<br> |
| 6 | Pressure pot<br>end point electrical parameters | – | – | Ta = 121°C, 2 atm, 240 h min.<br>as per device spec. | –<br>– | –<br>– | x<br>x | 22 | 0 | |
| 7 | HAST (Highly Accelerated Stress Test)<br>end point electrical parameters | – | 4.6.3 Cond2 | 130°C/85%RH with bias t=150h according to detail specification<br>as per device spec. | –<br>– | –<br>– | x<br>x | 22 | 0 | |

Notes
1) Sample can be increased according to LTPD table, till c=2
2) Aging of 8h in steam vapor or 16h at 155°C Soldering temperature of 215°C for SMD only
3) Ta such to have $T_J = T_j$ max
4) 20000g for packages with cavity perimeter of 5cm or more and/or with a mass of 5 grams or more

## Integrated circuits - Groups B, C and D tests

Every six months on raw line and/or finished products

| SUBGROUP | TEST PROCEDURE | MIL-STD-883 METHOD | CECC 90000 METHOD | SGS-THOMSON TEST CONDITIONS | PACKAGE | | | MINIMUM SAMPLE SIZE | ACCEPTANCE NUMBER (C) | NOTES |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | METAL | CERAMIC | PLASTIC | | | |
| 1 | Lead integrity | 2004 | 4 6 12 (1) | Tensile test (as per CECC 90000) | x | – | – | 22 | 0 | |
| | | | 4 6 12 (2) | Lead Fatigue Cond B2<br>- wire leads: a force of of 0 229 ± 0 014 Kg for three 90 ± 5° arcs on each lead bending cycle 2 to 5 sec<br>- dual-in-line and power moulded packages the leads shall be bent 3 times simultaneously for at least 15° permanent bend, returning then to the original position | x | x | x | | | 2 |
| | | | | Solder pad adhesion Cond D<br>a force of 0.299 Kg min to each solder pad for 30sec minimum | - | x | - | | | 3 |
| | Seal - fine<br>- gross | 1014 | 4 6.9 | see page 54 | x<br>x | x<br>x | -<br>- | | | |
| 2 | Thermal shock | 1011 | 4 6 8 | Cond B, 15 shocks, Ta = -55 to + 125°C | x | x | - | 22 | 0 | |
| | Temperature cycling | 1010 | 4 6 8 | Cond C; 100 cycles Ta = - 65 to + 150°C | x | x | x | | | 4 |
| | Moisture resistance | 1004 | 4 6 3 | Lead bend conditioning followed by 10 cycles of 24h, Ta = 25°C to 65°C RH = 80% to 100%, one 3h cycle at Ta = -10°C | x | x | - | | | |
| | Seal - fine<br>- gross | 1014 | 4 6 9 | see page 54 | x<br>x | x<br>x | -<br>- | | | |
| | Visual examination | 1004<br>1010 | – | without appraisal of marking | x | x | - | | | |
| | end point electrical parameters | | | as per device spec | x | x | x | | | |
| 3 | Mechanical shock | 2002 | 4 6 4 | Cond B, 1500g, 0 5 msec, 5 blows in each of the 6 orientations; not operating | x | x | – | 22 | 0 | |
| | Vibration, variable frequency | 2007 | 4 6 5 | Cond A, 20g, 3 orientations, f = 20 to 2000 cps, four 4 minutes cycles, 48 minutes total, not operating | x | x | – | | | |
| | Constant accelerations | 2001 | 4 6 7 | Cond E; 30000 g; Y1 onentation only | x | x | – | | | 5 |
| | Seal - fine<br>- gross | 1014 | 4 6 9 | see page 54 | x<br>x | x<br>x | –<br>– | | | |
| | Visual examination | 1010<br>1011 | – | | x | x | | | | |
| | end point electrical parameters | | | as per device spec | x | x | – | | | |
| 4 | Salt atmosphere | 1009 | 4 6 14 | Cond A. 10 to 50 gr of NaCl per m² for 24 h at Ta= 35°C min | x | x | x | 22 | 0 | |
| | Seal - fine<br>- gross | 1014 | 4 6 9 | see page 54 | x<br>x | x<br>x | –<br>– | | | |
| | Visual examination | 1009 | 4 6 14 | | x | x | x | | | |
| 5 | Humidity test | – | 4 6 3<br>Cond 1 | 85°C/85% RH with bias t = 1000h according to detail specification | – | – | x | 45 | 0 | |
| | end point electrical parameters | | | as per device spec | – | – | x | | | |
| 6 | Internal water-vapor content | 1018 | – | Dew point method procedure 3 (5000 ppm max) | x | x | – | 3<br>5 | 0<br>1 | 6 |
| 7 | Lid Torque | 2024 | – | see page 54 | – | x | – | 22 | 0 | 7 |

Notes
1) Sample can be increased according to LTPD table, till c=2
2) Not for SMD
3) Leadless chip carrier only
4) For plastic packages Ta= -65/-40°C according to device type
5) 20000g for packages with cavity perimeter of 5cm or more and/or with a mass of 5 grams or more
6) Test three devices If one fails, test two additional devices with no failure
7) Applied only to packages which use glass-frit seal to lead the frame lead or package body (i e wherever frit seal establishes hermeticity or package integrity)

## LPS - RESULTS SUMMARY

| Test | Condition | Plastic | | | | Ceramic | | | | S.O. Package | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1989 | | 1990 | | 1989 | | 1990 | | 1989 | | 1990 | |
| | | SS | REJ | SS | REJ | SS | REJ | SS | REJ | SS | REJ | SS | REJ |
| HIGH TEMPERATURE BIAS | 1000 hrs<br>2000 hrs | 1971<br>540 | 0<br>0 | 1809<br>513 | 0<br>0 | 620<br>135 | 0<br>0 | 675 | 0 | 738<br>198 | 0<br>0 | 756<br>216 | 0<br>0 |
| TEMPERATURE HUMIDITY BIAS | 1000 hrs<br>2000 hrs | 1951<br>513 | 0<br>0 | 1890<br>378 | 0<br>0 | – | – | – | – | 738<br>180 | 0<br>0 | 918<br>216 | 0<br>0 |
| PRESSURE COOKER | 168 hrs<br>336 hrs | 2125<br>675 | 0<br>0 | 1830<br>630 | 0<br>0 | – | – | – | – | 795<br>275 | 0<br>0 | 810<br>270 | 0<br>0 |
| THERMAL SHOCKS | 200 cyc | 1425 | 0 | 1950 | 0 | 450 | 0 | 375 | 0 | 150 | 0 | 125 | 0 |
| THERMAL CYCLES | 200 cyc<br>1000 cyc | 1070 | 0 | 1110 | 0 | 570 | 0 | 540 | 0 | 580 | 0 | 630 | 0 |
| ENVIRONMENTAL SEQUENCE | | – | – | – | – | 1325 | 0 | 1275 | 0 | – | – | – | – |
| MECHANICAL SEQUENCE | | – | – | – | – | 1325 | 0 | 1275 | 0 | – | – | – | – |
| RESISTANCE TO SOLVENT | | 475 | 1 | 425 | 1 | 350 | 0 | 325 | 0 | 425 | 1 | 375 | 0 |
| SOLDERABILITY | | 475 | 0 | 425 | 0 | 350 | 0 | 325 | 0 | 425 | 2 | 375 | 1 |
| LEAD INTEGRITY | | 475 | 0 | 425 | 0 | 350 | 0 | 325 | 0 | | | | |
| HAST | 96 hrs<br>240 hrs | 175<br>100 | 0<br>0 | 225<br>100 | 0<br>0 | – | – | – | – | 100<br>50 | 0<br>0 | 125<br>75 | 0<br>0 |

## FAILURE RATE EVALUATION (AT 60% CONFIDENCE LEVEL)

| Package | Device x Hours | Fail | Failure Rate FIT * | |
|---|---|---|---|---|
| | | | 125°C | 55°C |
| PLASTIC | $3.78 \times 10^6$ | 0 | 242 | 0.5 |
| CERAMIC | $1.32 \times 10^6$ | 0 | 693 | 1.4 |
| S.O. PACKAGE | $1.49 \times 10^6$ | 0 | 613 | 1.3 |

* FIT = Failure in Time. Number of failures/$10^9$ Hours of operation (or $10^{-9}$). The activation energy, from analysis, was chosen as 0.7 eV based on our tests results: the failure rate at lower operating temperature can be extrapolated from the Arrhenius plot.

The actual junction temperature should be used; it can be computed using the relationship

$$T_j = T_A + (P \times \theta_{JA})$$

Where $T_j$ = Junction temperature
$T_A$ = Ambient temperature
$\theta_{JA}$ = Junction to ambient thermal resistance (typically 100°C/watt for a 16 pin DIP)
$P$ = Power actual consumption

# DATASHEETS

# NOR GATE

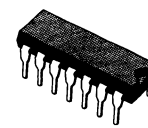
**4000B–DUAL 3 INPUT PLUS INVERTER**
**4001B–QUAD 2 INPUT**
**4002B-DUAL 4 INPUT**
**4025B TRIPLE 3 INPUT**

- PROPAGATION DELAY TIME = 60 ns (typ.) AT $C_L$ = 50 pF, $V_{DD}$ = 10 V
- BUFFERED INPUTS AND OUTPUTS
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20 V FOR HCC DEVICE
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25 °C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N. 13A, " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES "

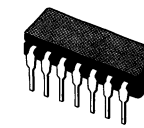
## DESCRIPTION

The **HCC4000B, HCC4001B, HCC4002B** and **HCC4025B** (extended temperature range) and **HCF4000B, HCF4001B, HCF4002B** and **HCF4025B** (intermediate temperature range) are monolithic integrated circuit, available in 14-lead dual in line plastic or ceramic package and plastic micropackage.

The **HCC/HCF4000B, HCC/HCF4001B, HCC/HCF 4002B** and **HCC/HCF4025B** nor gate provide the system designer with direct implementation of the nor function and supplement the existing family of COS/MOS gates. All inputs and outputs are buffered.



**EY**
(Plastic Package)



**F**
(Ceramic Package)

**M1**
(Micro Package)

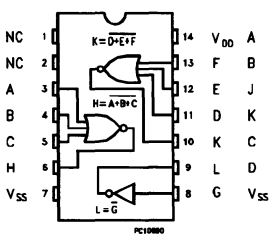
**C1**
(Chip Carrier)

**ORDER CODES :**

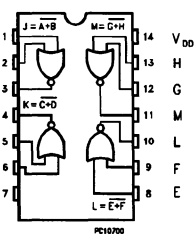
| | |
|---|---|
| HCCXXXXBF | HCFXXXXBM1 |
| HCFXXXXBEY | HCFXXXXBC1 |

## PIN CONNECTIONS

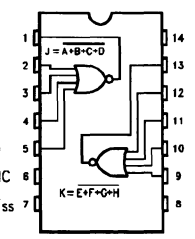
**4000B**



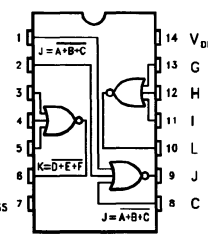

**4001B**




**4002B**




**4025B**



## ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ * | Supply Voltage: **HCC** Types<br>**HCF** Types | -0.5 to +20<br>-0.5 to +18 | V<br>V |
| $V_I$ | Input Voltage | -0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for Top = Full Package Temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

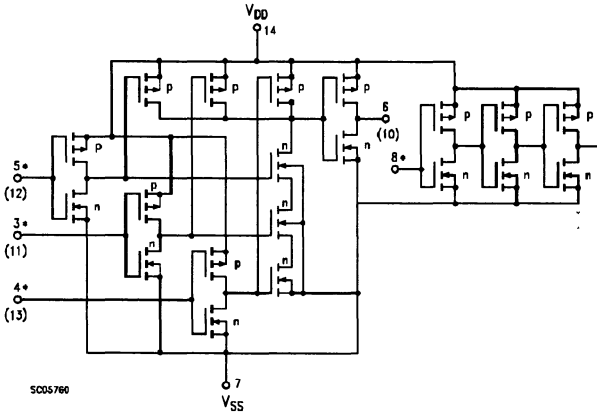
* All voltage values are referred to $V_{SS}$ pin voltage.

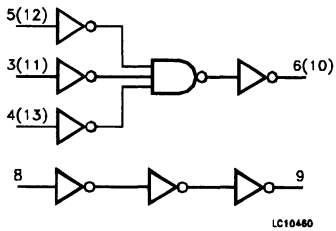
## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage: **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |

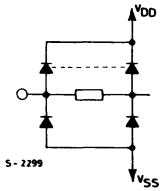
## SCHEMATIC AND LOGIC DIAGRAMS

### 4000B



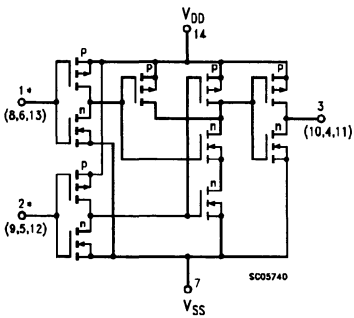



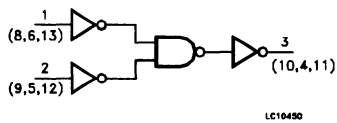

INVERTER AND 1 OF 2 GATES (NUMBERS IN PARANTHESES ARE THERMINAL FOR SECOND GATE)



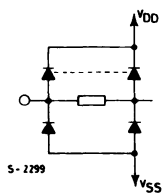

ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

### 4001B



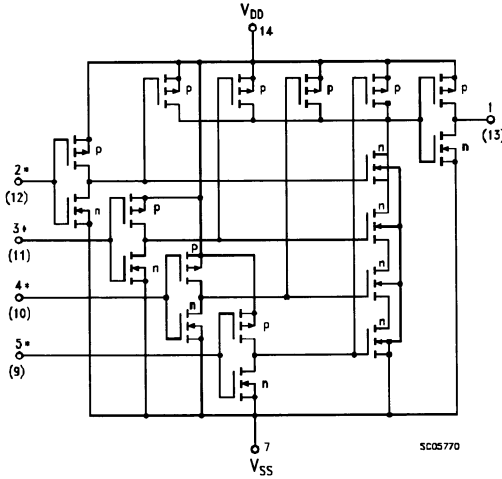

1 OF 4 GATES (NUMBERS IN PARANTHESES ARE THERMINAL FOR OTHER GATE)

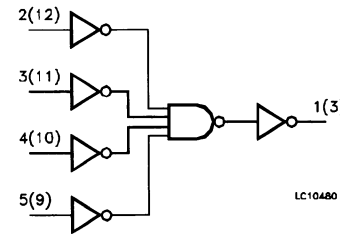


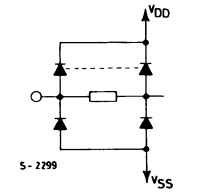

ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

## SCHEMATIC AND LOGIC DIAGRAMS (continued)

### 4002B



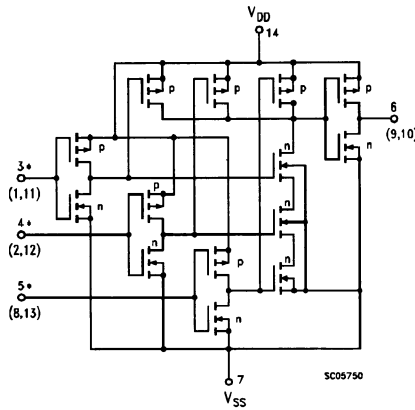



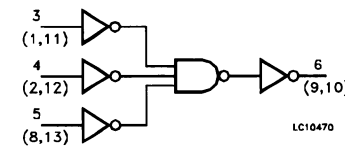



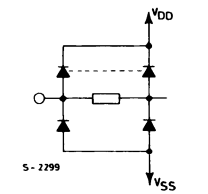

ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

1 OF 2 GATES (NUMBERS IN PARANTHESES ARE THERMINAL FOR SECOND GATE)

### 4025B




ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

INVERTER AND 1 OF 3 GATES (NUMBERS IN PARANTHESES ARE THERMINAL FOR OTHER GATES)

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditios | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{LOW}$ * Min. | $T_{LOW}$ * Max. | 25 °C Min. | 25 °C Typ. | 25 °C Max. | $T_{HIGH}$ * Min. | $T_{HIGH}$ * Max. | |
| $I_L$ | Quiescent Current | HCC Types | 0/5 | | | 5 | | 0.25 | | 0.01 | 0.25 | | 7.5 | μA |
| | | | 0/10 | | | 10 | | 0.5 | | 0.01 | 0.5 | | 15 | |
| | | | 0/15 | | | 15 | | 1 | | 0.01 | 1 | | 30 | |
| | | | 0/20 | | | 20 | | 5 | | 0.02 | 5 | | 150 | |
| | | HCF Types | 0/5 | | | 5 | | 1 | | 0.01 | 1 | | 7.5 | |
| | | | 0/10 | | | 10 | | 2 | | 0.01 | 2 | | 15 | |
| | | | 0/15 | | | 15 | | 4 | | 0.01 | 4 | | 30 | |
| $V_{OH}$ | Output High Voltage | | 0/5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/5 | 2.5 | | 5 | -2 | | -1.6 | -3.2 | | -1.15 | | mA |
| | | | 0/5 | 4.6 | | 5 | -0.64 | | -0.51 | -1 | | -0.36 | | |
| | | | 0/10 | 9.5 | | 10 | -1.6 | | -1.3 | -2.6 | | -0.9 | | |
| | | | 0/15 | 13.5 | | 15 | -4.2 | | -3.4 | -6.8 | | -2.4 | | |
| | | HCF Types | 0/5 | 2.5 | | 5 | -1.53 | | -1.36 | -3.2 | | -1.1 | | |
| | | | 0/5 | 4.6 | | 5 | -0.52 | | -0.44 | -1 | | -0.36 | | |
| | | | 0/10 | 9.5 | | 10 | -1.3 | | -1.1 | -2.6 | | -0.9 | | |
| | | | 0/15 | 13.5 | | 15 | -3.6 | | -3.0 | -6.8 | | -2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ±0.1 | | $±10^{-5}$ | ±0.1 | | ±1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ±0.3 | | $±10^{-5}$ | ±0.3 | | ±1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{LOW}$ = -55 °C for **HCC** device: -40 °C for **HCF** device.

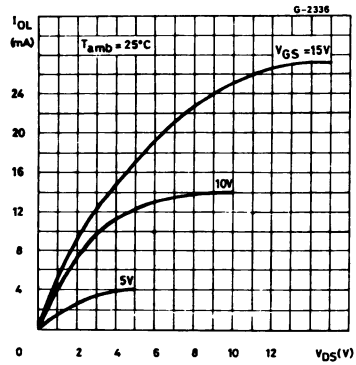
* $T_{HIGH}$ = +125 °C for **HCC** device: +85 °C for **HCF** device.

The Noise Margin for both "1" and "0" level is: 1V min. with $V_{DD}$ = 5 V, 2 V min. with $V_{DD}$ = 10 V, 2.5 V min. with $V_{DD}$ = 15 V

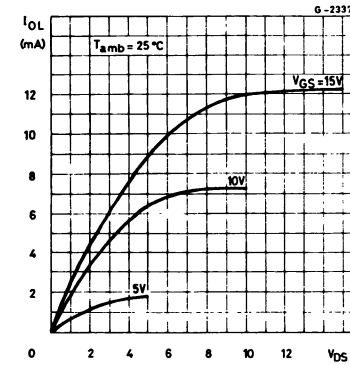
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 KΩ, typical temperature coefficent for all $V_{DD}$ values is 03 %/°C, all input rise and fall times= 20 ns)

| Symbol | Parameter | Test Conditions | Value | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$ $t_{PLH}$ | Propagation Delay Time | | 5 | | 125 | 250 | ns |
| | | | 10 | | 60 | 120 | |
| | | | 5 | | 45 | 90 | |
| $t_{THL}$ $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

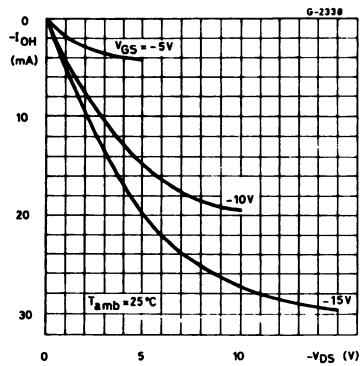
Typical Output Low (sink) Current Characteristics



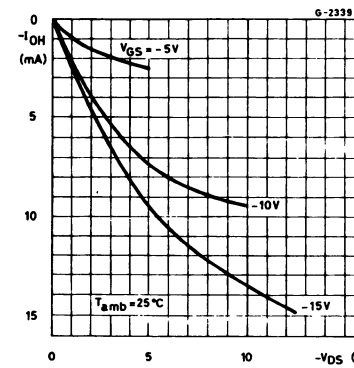

Minimum Output Low (sink) Current Characteristics



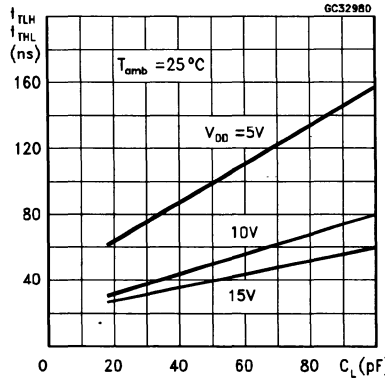

Typical Output High (source) Current Characteristics



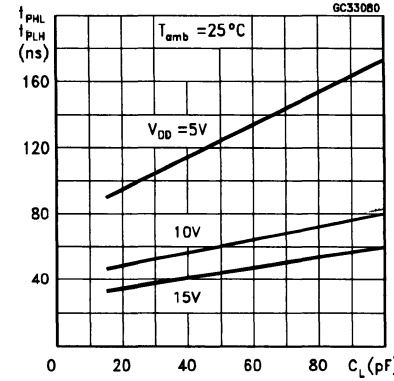

Minimum Output High (sorce) Current Characteristics



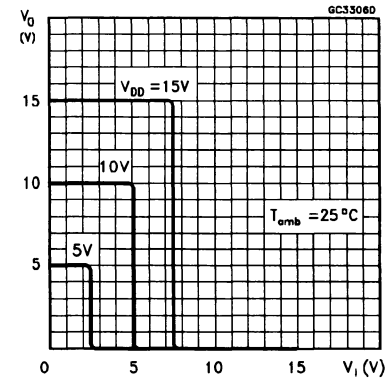
Typical Transition Time vs Load Capacitance



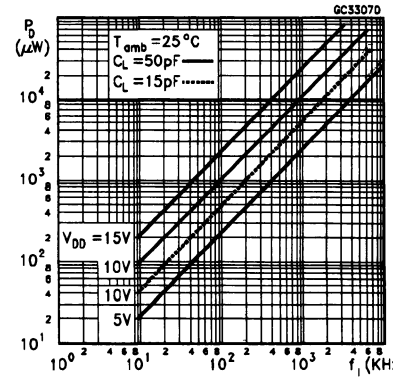

Typical Propagation Delay Time vs Load Capacitance




Typical Voltage Transfer Characteristics as a Function of Temperature

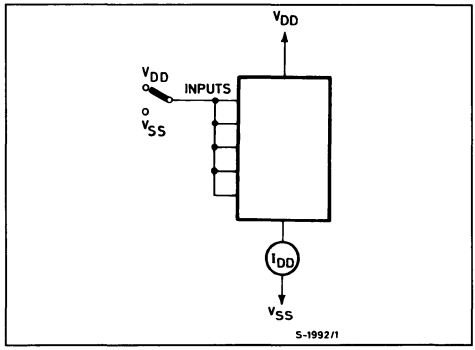



Typical Power Dissipation Per Gate vs Frequency

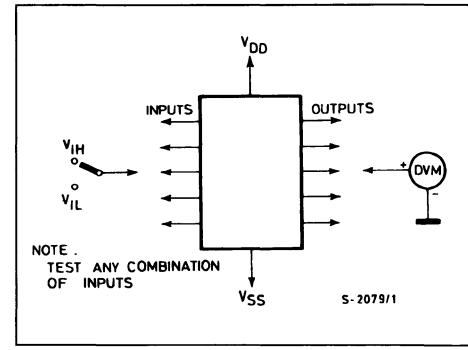


## TEST CIRCUITS

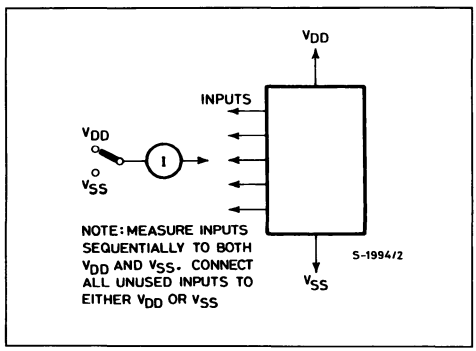
Quiescent Device Current.




Noise Immunity.



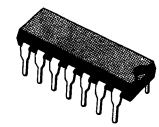

Input Leakage Current.



# HCC/HCF4006B

## 18-STAGE STATIC SHIFT REGISTER

- PERMANENT REGISTER STORAGE WITH CLOCK LINE "HIGH" OR "LOW" ... NO INFORMATION RECIRCULATION REQUIRED
- FULLY STATIC OPERATION
- SHIFTING RATES UP TO 12MHz @ 10V (typ.)
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- INPUT CURRENT OF 100nA AT 18V AND 25 °C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- 5V, 10V, AND 15V PARAMETRIC RATING
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)

**F**
(Ceramic Frit Seal Package)

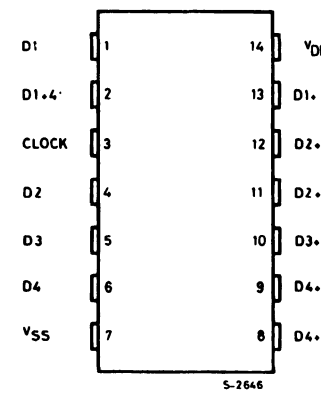
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4006BF HCF4006BM1
HCF4006BEY HCF4006BC1

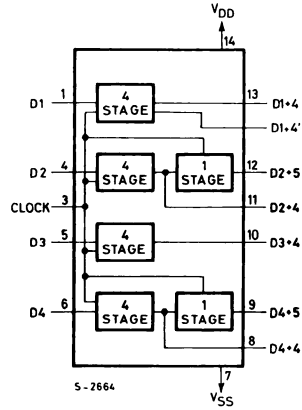
**PIN CONNECTIONS**




### DESCRIPTION

The **HCC4006B** (extended temperature range) and the **HCF4006B** (standard temperature range), are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and plastic micro package. The types are comprised of 4 separate "shift register" sections ; two sections of four stages and two sections of five stages with an output tap at the fourth stage. Each section has an independent "single rail" data path. A common clock signal is used for all stages. Data is shifted to the next stage on negative-going transitions of the clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8, and 9 stages or single register sections of 10, 12, 13, 14, 16, 17 and 18 can be implemented using one **HCC/HCF4006B** package. Longer shift register sections can be assembled by using more than one **HCC/HCF4006B**. To facilitate cascading stages when clock rise and fall times are slow, an optional output ($D_1 + 4'$) that is delayed one-half clock-cycle, is provided (see truth table for output from pin 2).

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

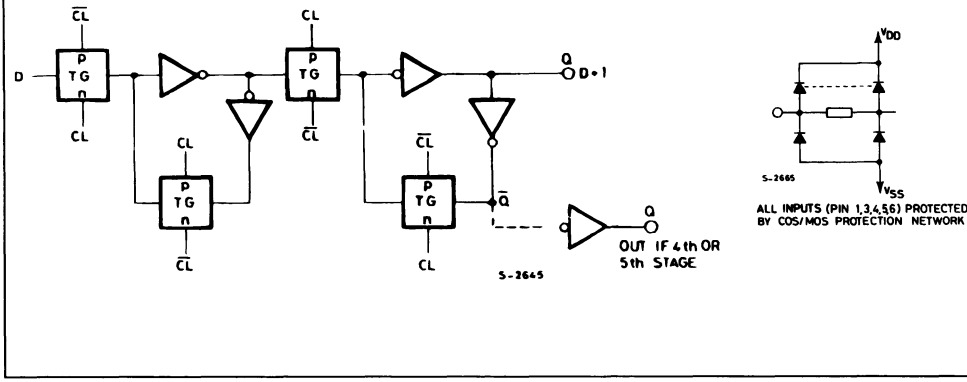
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAM AND TRUTH TABLES (one register stage)




### TRUTH TABLE FOR OUTPUT FROM PIN 2

| $D_1 + 4$ | $CL^{\Delta}$ | $D_1 + 4'$ |
|---|---|---|
| 0 | ⌐ | 0 |
| 1 | ⌐ | 1 |
| X | ⌙ | NC |

### TRUTH TABLE FOR SHIFT REGISTER STAGE

| D | $CL^{\Delta}$ | D + 1 |
|---|---|---|
| 0 | ⌙ | 0 |
| 1 | ⌙ | 1 |
| X | ⌐ | NC |

1 = HIGH
0 = LOW
NC = NO CHANGE
X = DON'T CARE
Δ = LEVEL CHANGE

| Symbol | Parameter | | Test Conditions | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{Low}$* Min | $T_{Low}$* Max | 25° Min | 25° Typ | 25° Max | $T_{High}$* Min | $T_{High}$* Max | |
| $I_L$ | Quiescent Current | HCC Types | 0/5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/5 | | <1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | <1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | <1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | <1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | <1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | <1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | <1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | <1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | <1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | <1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | <1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | <1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | ± $10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | ±$10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | 5 | 7.5 | | | pF | |

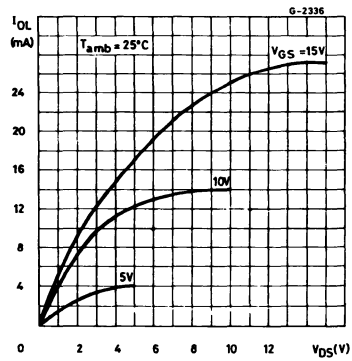
* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5 V min. with $V_{DD}$ = 15V.

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall times = 20ns)

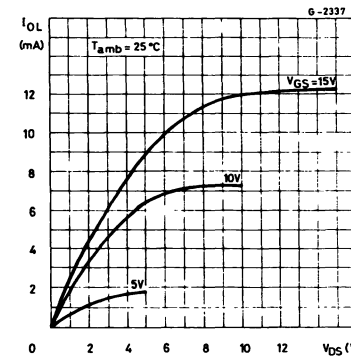
| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time | | 5 | | 200 | | ns |
| | | | 10 | | 100 | | |
| | | | 15 | | 80 | | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | 5 | | 100 | | ns |
| | | | 10 | | 50 | | |
| | | | 15 | | 40 | | |
| $t_w$ | Clock Pulse Width | | 5 | | 100 | | ns |
| | | | 10 | | 45 | | |
| | | | 15 | | 30 | | |
| $t_r$, $t_f$ | Clock Input Rise or Fall Time* | | 5 | | 15 | | µs |
| | | | 10 | | 15 | | |
| | | | 15 | | 15 | | |
| $t_{setup}$ | Data Setup Time | | 5 | | 50 | | ns |
| | | | 10 | | 25 | | |
| | | | 15 | | 20 | | |
| $f_{max}$ | Maximum Clock Input Frequency | | 5 | | 5 | | MHz |
| | | | 10 | | 12 | | |
| | | | 15 | | 16 | | |

* If more than unit is cascaded $t_rCL$ should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

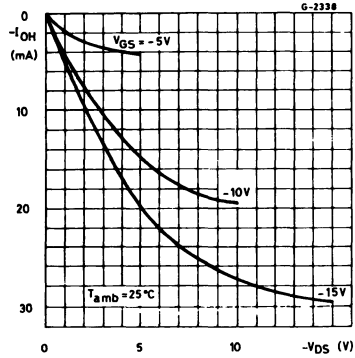
Typical Output Low (sink) Current Characteristics.



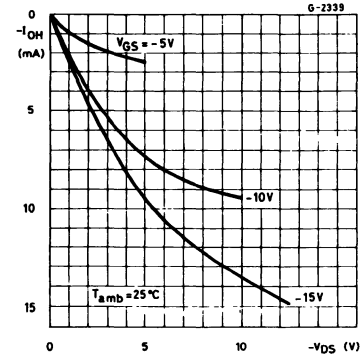

Minimum Output Low (sink) Current Characteristics.



Typical Output High (source) Current Characteristics.

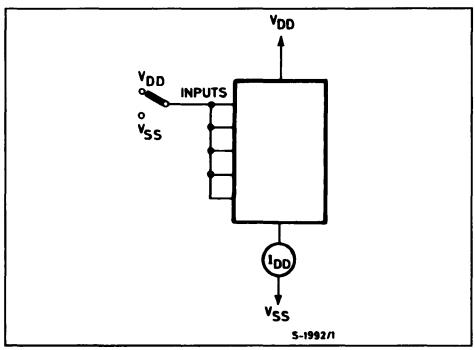



Minimum Output High (source) Current Characteristics.

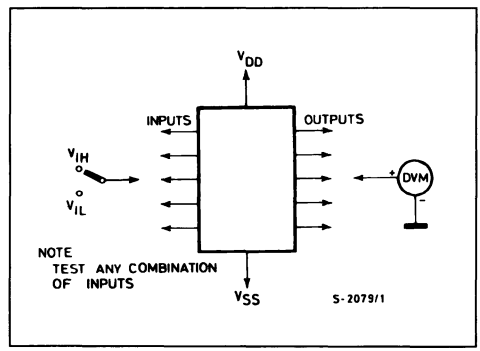



## TEST CIRCUITS

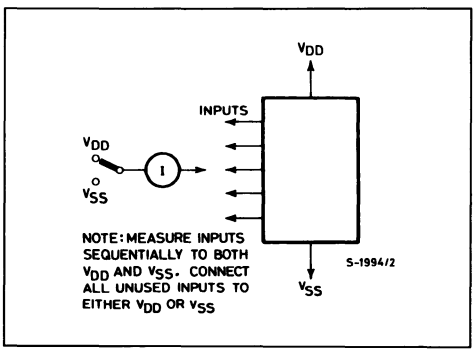
Quiescent Device Current.




Input Voltage.



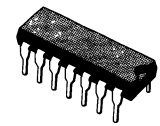

Input Current.



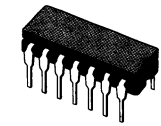
# HCC4007UB
# HCF4007UB

## DUAL COMPLEMENTARY PAIR PLUS INVERTER

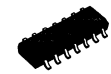
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- MEDIUM SPEED OPERATION $t_{PHL}$, $t_{PLH}$ = 30ns (typ.) AT 10V
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Package)



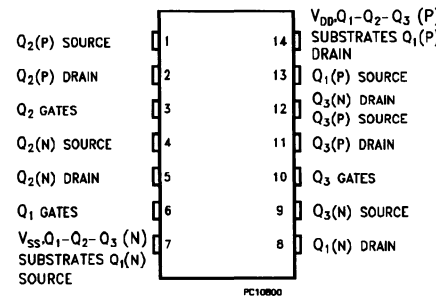
**M1**
(Micro Package)

**C1**
(Chip Carrier)

**ORDER CODES :**

HCC4007UBF HCF4007UBM1
HCF4007UBEY HCF4007UBC1

**PIN CONNECTIONS**

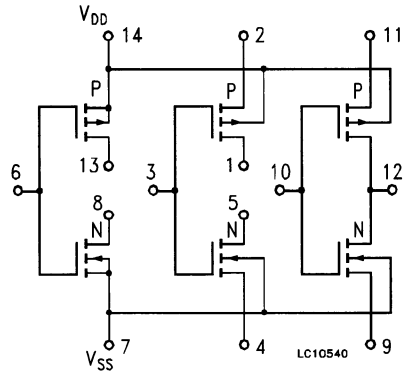



### DESCRIPTION

The HCC4007UB is a monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package and plastic micropackage.

The HCC4007UB type is comprised of three n-channel and three p-channel enhancement type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits as shown in typical applications. More complex functions are possible using multiple packages. Numbers shown in parentheses indicate terminals that are connected together to form the varius configurations listed.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ * | Supply Voltage: **HCC** Types<br>**HCF** Types | -0.5 to +20<br>-0.5 to +18 | V<br>V |
| $V_I$ | Input Voltage | -0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for Top = Full Package Temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |

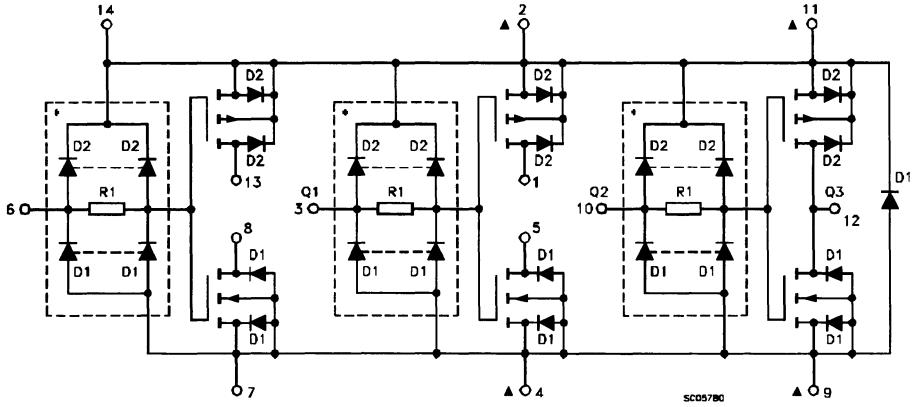
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

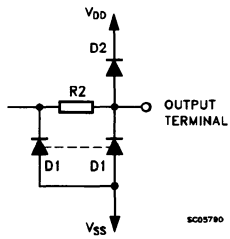
* All voltage values are referred to $V_{SS}$ pin voltage

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage: **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |

**SCHEMATIC DIAGRAM** (showing input, output and parasitic diodes)




▲ COS/MOS OUTPUT PROTECTION NETWORK BETWEEN TERMINAL NOS. 1, 2, 4, 5, 8, 9, 11, 12, 13, AND THE CORRESPONDING DRAINS AND/OR SOURCES

✱ COS/MOS INPUT PROTECTION NETWORK

PARASITIC AND NETWORK COMPONENTS
D1 = N+ TO P WELL
D2 = P+ TO SUBSTRATE
R1 = 1 - 5 KΩ
R2 = 15 - 30 Ω

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditios | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{LOW}$ * Min. | $T_{LOW}$ * Max. | 25 °C Min. | 25 °C Typ. | 25 °C Max. | $T_{HIGH}$ * Min. | $T_{HIGH}$ * Max. | |
| $I_L$ | Quiescent Current | HCC Types | 0/5 | | | 5 | | 0.25 | | 0.01 | 0.25 | | 7.5 | μA |
| | | | 0/10 | | | 10 | | 0.5 | | 0.01 | 0.5 | | 15 | |
| | | | 0/15 | | | 15 | | 1 | | 0.01 | 1 | | 30 | |
| | | | 0/20 | | | 20 | | 5 | | 0.02 | 5 | | 150 | |
| | | HCF Types | 0/5 | | | 5 | | 1 | | 0.01 | 1 | | 7.5 | |
| | | | 0/10 | | | 10 | | 2 | | 0.01 | 2 | | 15 | |
| | | | 0/15 | | | 15 | | 4 | | 0.01 | 4 | | 30 | |
| $V_{OH}$ | Output High Voltage | | 0/5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 4 | | 4 | | | 4 | | V |
| | | | | 1/9 | < 1 | 10 | 8 | | 8 | | | 8 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 12.5 | | 12.5 | | | 12.5 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1 | | | 1 | | 1 | V |
| | | | | 9/1 | < 1 | 10 | | 2 | | | 2 | | 2 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 2.5 | | | 2.5 | | 2.5 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/5 | 2.5 | | 5 | -2 | | -1.6 | -3.2 | | -1.15 | | mA |
| | | | 0/5 | 4.6 | | 5 | -0.64 | | -0.51 | -1 | | -0.36 | | |
| | | | 0/10 | 9.5 | | 10 | -1.6 | | -1.3 | -2.6 | | -0.9 | | |
| | | | 0/15 | 13.5 | | 15 | -4.2 | | -3.4 | -6.8 | | -2.4 | | |
| | | HCF Types | 0/5 | 2.5 | | 5 | -1.53 | | -1.36 | -3.2 | | -1.1 | | |
| | | | 0/5 | 4.6 | | 5 | -0.52 | | -0.44 | -1 | | -0.36 | | |
| | | | 0/10 | 9.5 | | 10 | -1.3 | | -1.1 | -2.6 | | -0.9 | | |
| | | | 0/15 | 13.5 | | 15 | -3.6 | | -3.0 | -6.8 | | -2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ±0.1 | | $±10^{-5}$ | ±0.1 | | ±1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ±0.3 | | $±10^{-5}$ | ±0.3 | | ±1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{LOW}$ = -55 °C for **HCC** device: -40 °C for **HCF** device.

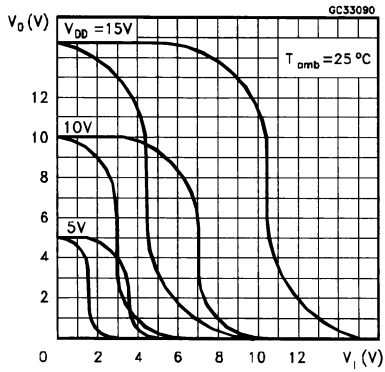
* $T_{HIGH}$ = +125 °C for **HCC** device: +85 °C for **HCF** device.

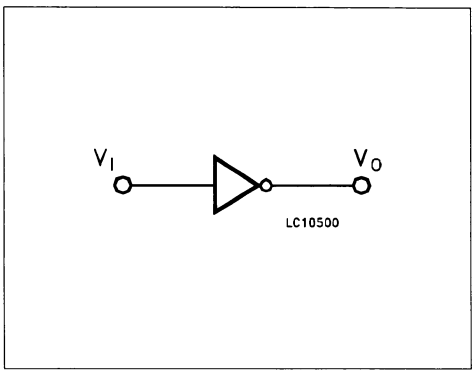
The Noise Margin for both "1" and "0" level is: 1V min. with $V_{DD}$ = 5 V, 2 V min. with $V_{DD}$ = 10 V, 2.5 V min. with $V_{DD}$ = 15 V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 KΩ, typical temperature coefficent for all $V_{DD}$ values is 03 %/°C, all input rise and fall times= 20 ns)

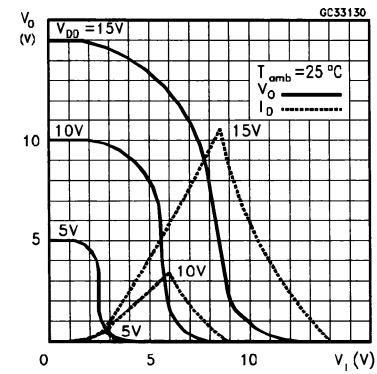
| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time | | 5 | | 55 | 110 | ns |
| | | | 10 | | 30 | 60 | |
| | | | 15 | | 25 | 50 | |
| $t_{TLH}$ $t_{THL}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

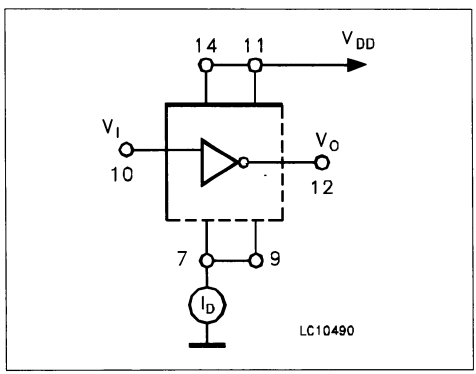
Minimum and Maximum Voltage Transfer Characterisctics for Inverter and test Circuit



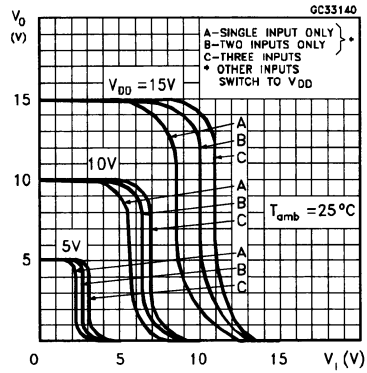



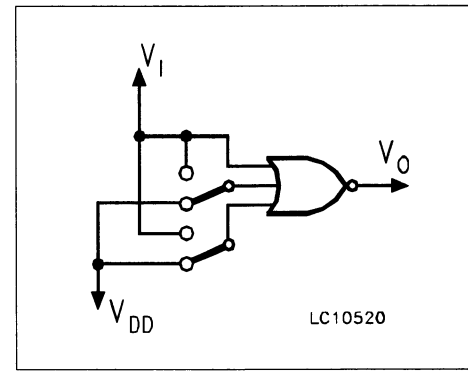

Typical Current and Voltage Transfer Characteristics for Inverter and Test Circuit



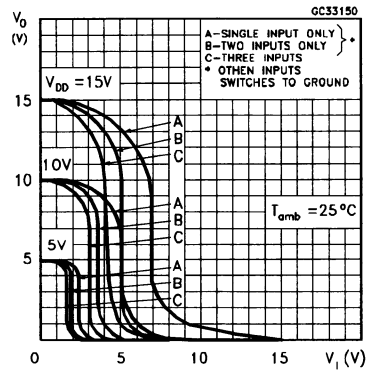



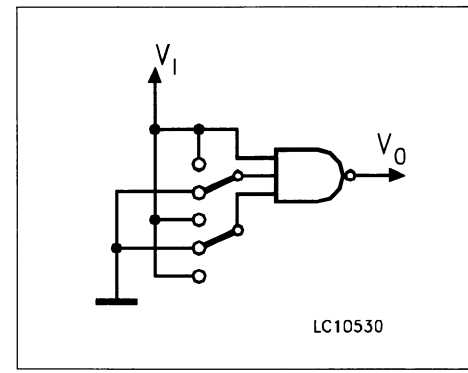
Typical Voltage Transfer Characteristics for NAND Gate and Test Circuit



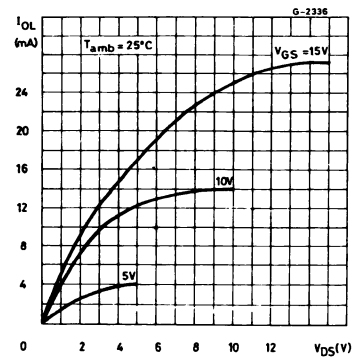




Typical Voltage Transfer Characteristics for NOR Gate and Test Circuit

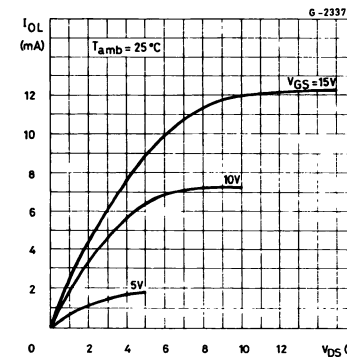


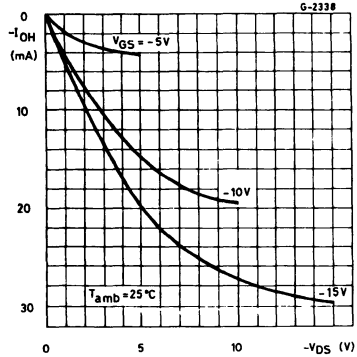

Typical Output Low (Sink) Current Caracteristics



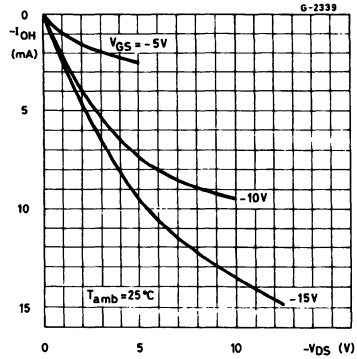

Minimum Output Low (Sink) Current Characteristics



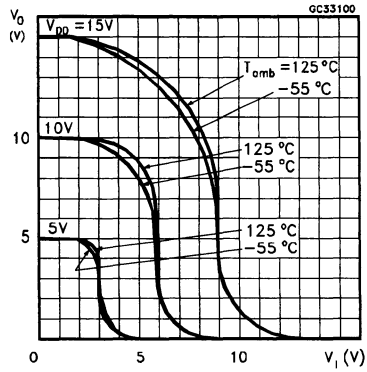
Typical Output High (Source) Current Characteristics



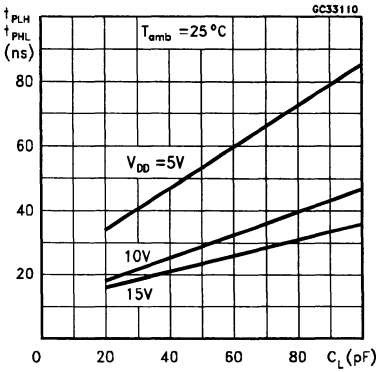

Minimum Output High (Sourrce) Current Characteristics



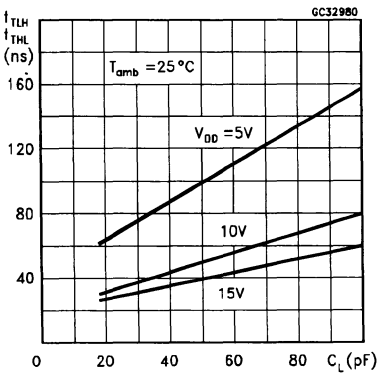

Typical Voltage Transfer Characteristics as a Function of Temperature



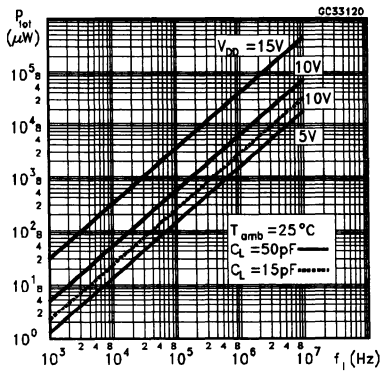

Typical Propagation Delay Time vs. Load Capacitance




Typical Transition Time vs. Load Capacitance

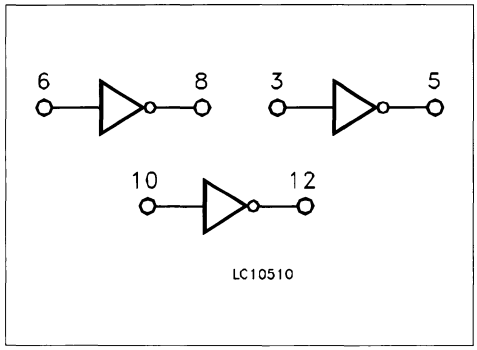



Typical Dissipatio Per Gate vs. Frequency Characteristics

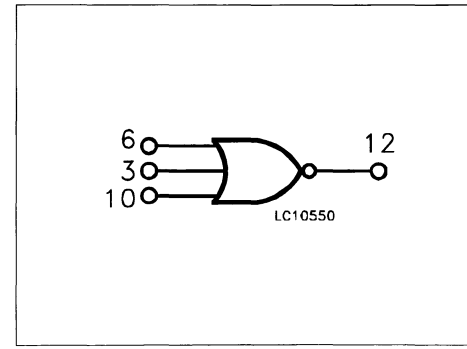


**TYPICAL APPLICATIONS** (Sample COS/MOS logic circuit arrangements using type 4007UB)

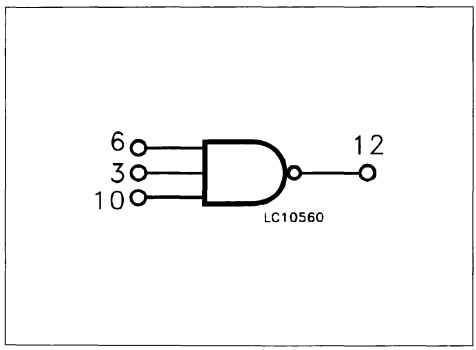
Triple Inverters: (14, 2, 11); (8, 13); (1, 5); (4, 7, 9).



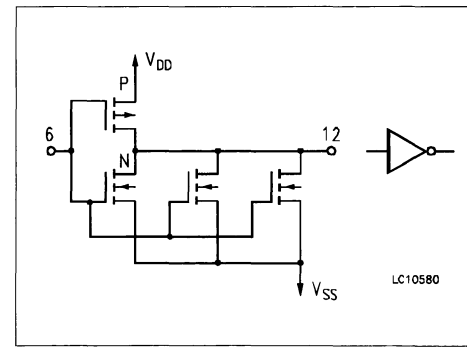

3-Input NOR Gate: (13, 2); (1, 11); (12, 5, 8); (4, 7, 9).



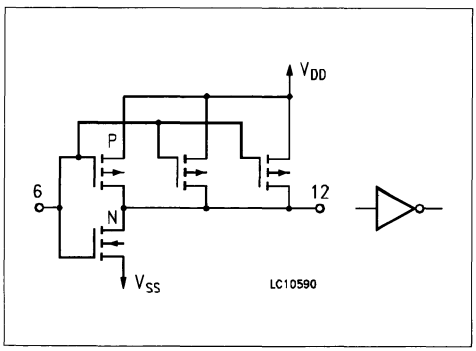

3-Input NAND Gate: (1, 12, 13); (2, 14, 11); (4, 8); (5, 9).



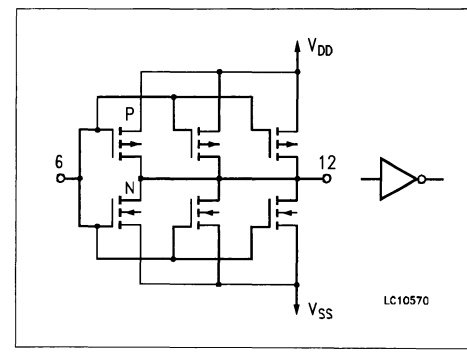

High Sink Current Driver: (6, 3, 10); (8, 5, 12); (11, 14); (4, 7, 9).



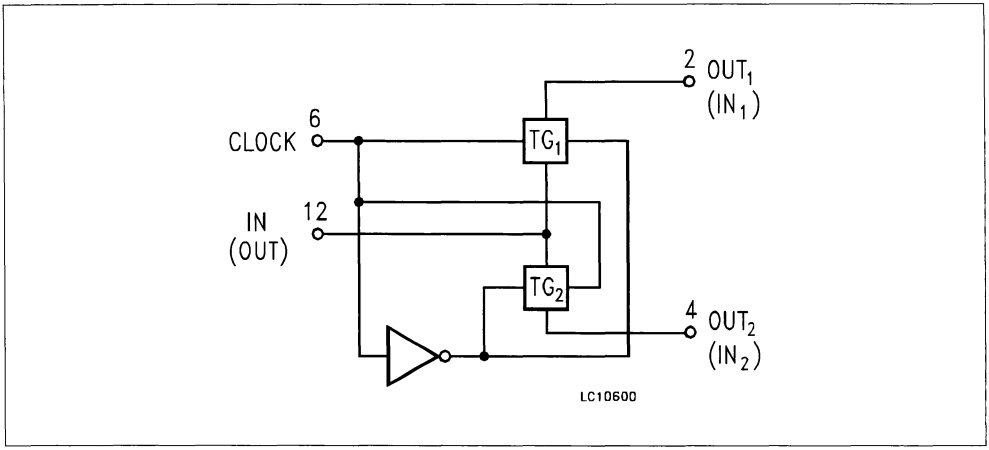

High Source Current Driver: (6, 3, 10); (13, 1, 12); (14, 2, 11); (7, 9).




High Sink and Source Current Driver: (6, 3, 10); (14, 2, 11); (7, 4, 9); (13, 8, 1, 5, 12).

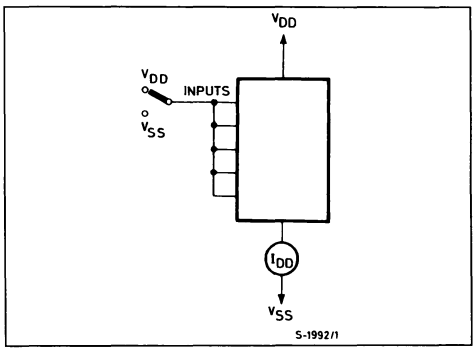


Dual Bidirectional Trasmission Gating: (1, 5, 12); (2, 9); (11, 4); (8, 13, 10); (6, 3).

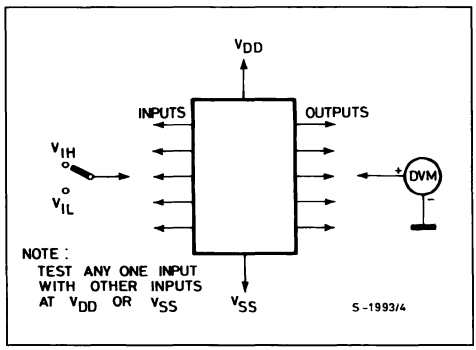



## TEST CIRCUIT

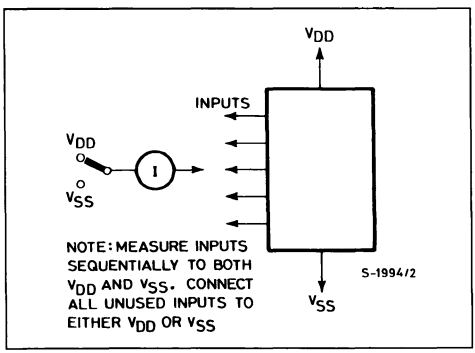
Quiescent Device Current.




Input Voltage.



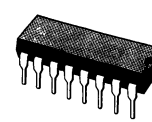

Input Leakage Current.



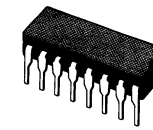
# HCC/HCF4008B

## 4-BIT FULL ADDER WITH PARALLEL CARRY OUTPUT

- 4 SUM OUTPUTS PLUS PARALLEL LOOK-AHERD CARRY-OUTPUT
- HIGH-SPEED OPERATION-SUM IN-TO-SUM OUT 160ns (typ.) : CARRY IN-TO-CARRY OUT 50ns (typ.) AT $V_{DD}$ = 10V, $C_L$ = 50pF
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- 5V, 10V, AND 15V PARAMETRIC RATING
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

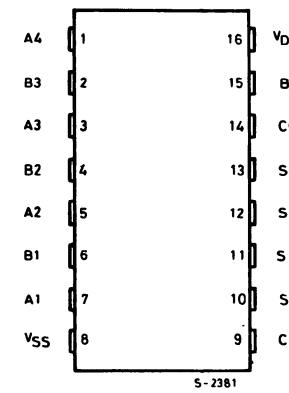
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4008BF HCF4008BM1
HCF4008BEY HCF4008BC1

**PIN CONNECTIONS**




### DESCRIPTION

The **HCC4008B** (extended temperature range) and **HCF4008B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and plastic micropackage.

The **HCC/HCF4008B** types consist of four full adder stages with fast look ahead carry provision from stage to stage. Circuitry is included to provide a fast "parallel-carry-out" to permit high-speed operation in arithmetic sections using several HCC/HCF 4008B's.

**HCC/HCF4008B** inputs include the four sets of bits to be added, $A_1$ to $A_4$ and $B_1$ to $B_4$, in addition to the "Carry In" bit from a previous section. **HCC/HCF4008B** outputs include the four sum bits, $S_1$ to $S_4$. In addition to the high speed "parallel-carry-out" which may be utilized at a succeeding **HCC/HCF4008B** section.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

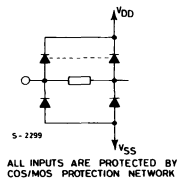
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

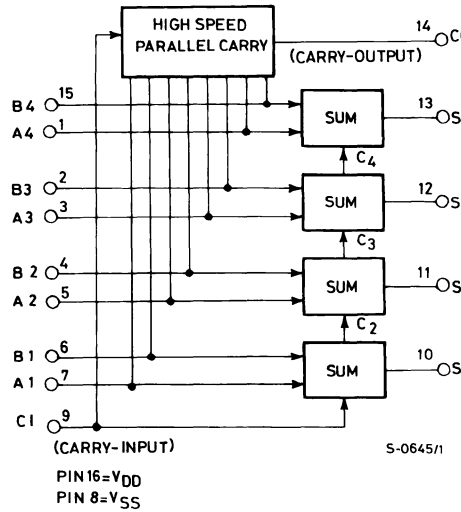
* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAM




## TRUTH TABLE

| $A_i$ | $B_i$ | CI | CO | SUM |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

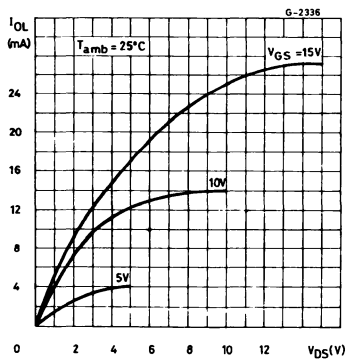
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$= − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$= + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5 V min. with $V_{DD}$ = 15V.

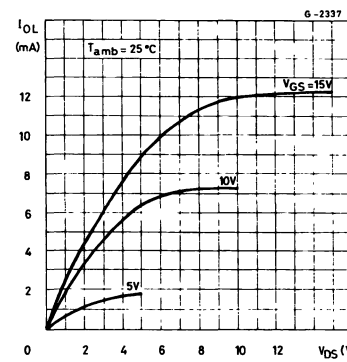
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3 %/°C, all input rise and fall times = 20 ns)

| Symbol | Parameter | | Test Conditions | Value | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time | Sum In to Sum Out | | 5 | | 400 | 800 | ns |
| | | | | 10 | | 160 | 320 | |
| | | | | 15 | | 115 | 230 | |
| | | Carry In to Sum Out | | 5 | | 370 | 740 | |
| | | | | 10 | | 155 | 310 | |
| | | | | 15 | | 115 | 230 | |
| | | Sum In to Carry Out | | 5 | | 200 | 400 | |
| | | | | 10 | | 90 | 180 | |
| | | | | 15 | | 65 | 130 | |
| | | Carry In to Carry Out | | 5 | | 100 | 200 | |
| | | | | 10 | | 50 | 100 | |
| | | | | 15 | | 40 | 80 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | | 5 | | 100 | 200 | ns |
| | | | | 10 | | 50 | 100 | |
| | | | | 15 | | 40 | 80 | |

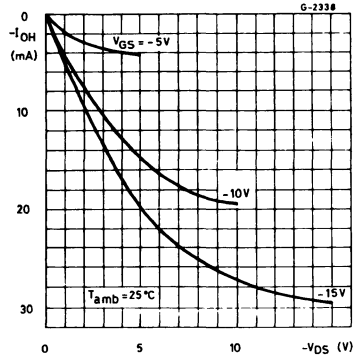
Typical Output Low (sink) Current.



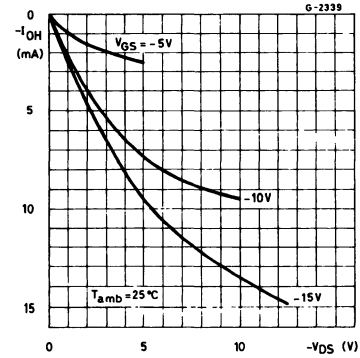

Minimum Output Low (sink) Current Characteristics.



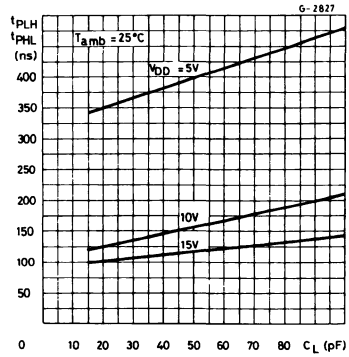
Typical Output High (source) Current Characteristics.



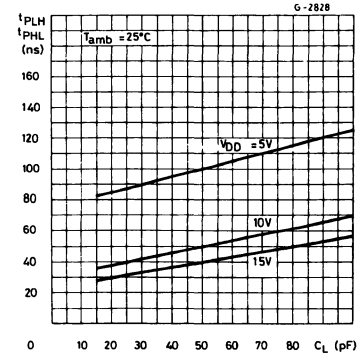

Minimum Output High (source) Current Characteristics.



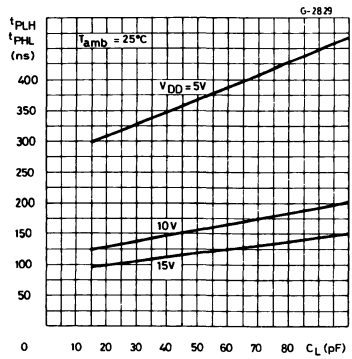

Typical Sum-in to Sum Out Propagation Delay vs. Load Capacitance.



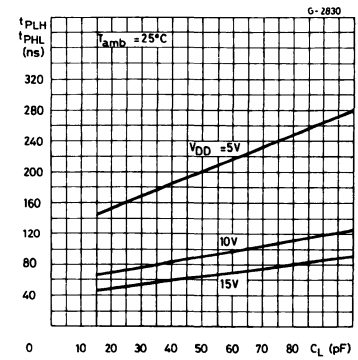

Typical Carry-in to Carry-Out Propagation Delay vs. Load Capacitance.



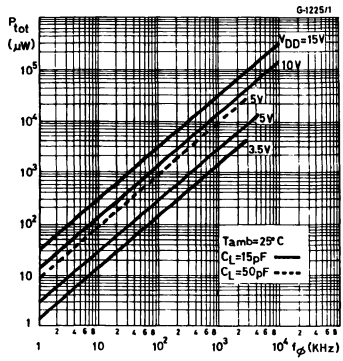

Typical Carry-in to Sum Out Propagation Delay Time vs. Load Capacitance.




Typical Sum-in to Carry-Out Propagation Delay Time vs. Load Capacitance.

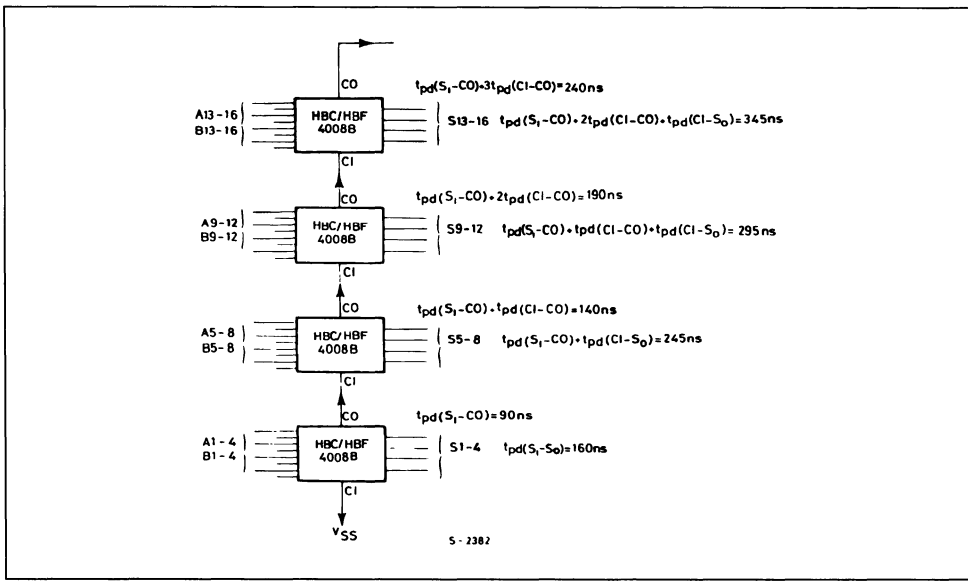


Typical Dynamic Power Dissipation/Package vs. Frequency.




## TYPICAL APPLICATIONS

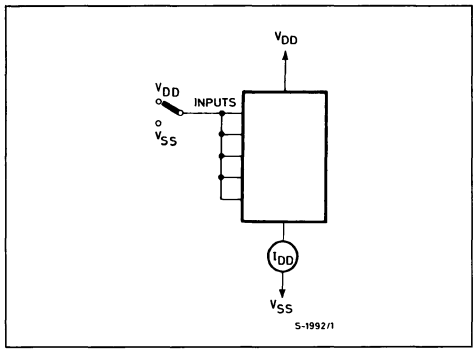
SPEED CHARACTERISTICS OF A 16-BIT ADDER.



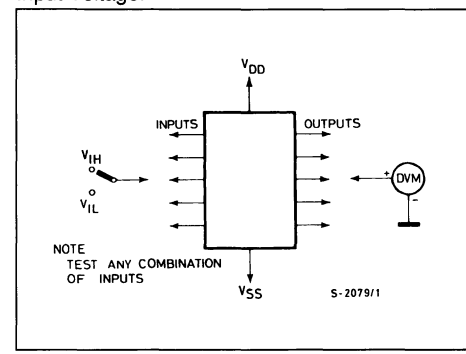

**Notes :** All "A" and "B" input bits occur at t = 0.
All sums settled at t = 345ns.
$C_L$= 50pF, $T_{amb}$ = 25°C, $V_{DD}$-$V_{SS}$ = 10V.

## TEST CIRCUITS

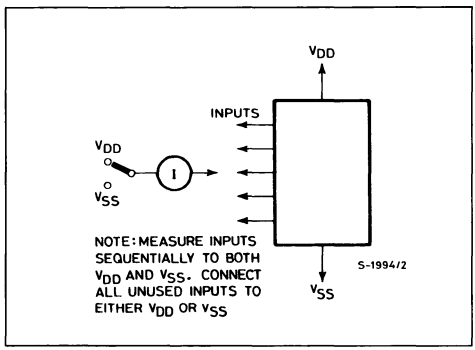
Quiescent Device Current.




Input Voltage.




Input Current.



# HCC/HCF4009UB
# HCC/HCF4010B

## HEX BUFFER/CONVERTERS

**4009UB–INVERTING TYPE**
**4010B–NON INVERTING TYPE**

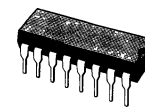
- CMOS TO DTL/TTL HEX CONVERTER
- HIGH-TO-LOW LEVEL LOGIC CONVERSION
- MULTIPLEXER: 1-TO-6 OR 6-TO-1
- HIGH"SINK" AND "SOURCE" CURRENT CAPABILITY
- 5V, 10V AND 15V PARAMETRIC RATINGS
- MAXIMUM INPUT CURRENT OF 100 μA AT 18V OVER FULL
- PACKAGE AND TEMPERATURE RANGE; 100nA AT 18V AND 25°C
- 100% TESTED FOR QUIESCENT CURRENT AT 20V
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N. 13A, " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES "

### DESCRIPTION

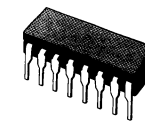
The **HCC4009UB/4010B** (extended temperature range) and the **HCF4009UB/4010B** (intermediate temperature range) are monolithic integrated circuits available in 16-lead dual in line plastic or ceramic packages and plastic micropackage.

The **HCC/HCF4009UB/4010B** are inverting and non-inverting Hex Buffer/Converters, respectively. Both devices can be used as CMOS to TTL or DTL logic-level converters, as current "sink" or "source" drivers or as multiplexer (1 to 6).

**4049UB** and **4050B** are prefered replacements for **4009UB** and **4010B**, respectively, in buffer applications.



**EY**
(Plastic Package)



**F**
(Ceramic Package)

**M1**
(Micro Package)

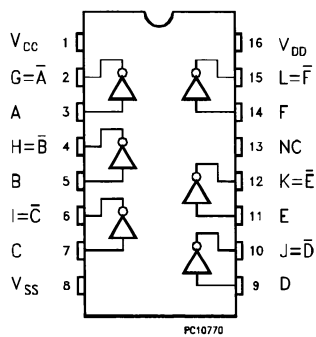
**C1**
(Chip Carrier)

**ORDER CODES :**

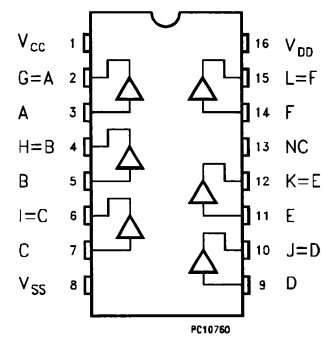
| | |
|---|---|
| HCCXXXXBF | HCFXXXXBM1 |
| HCFXXXXBEY | HCFXXXXBC1 |

### PIN CONNECTIONS

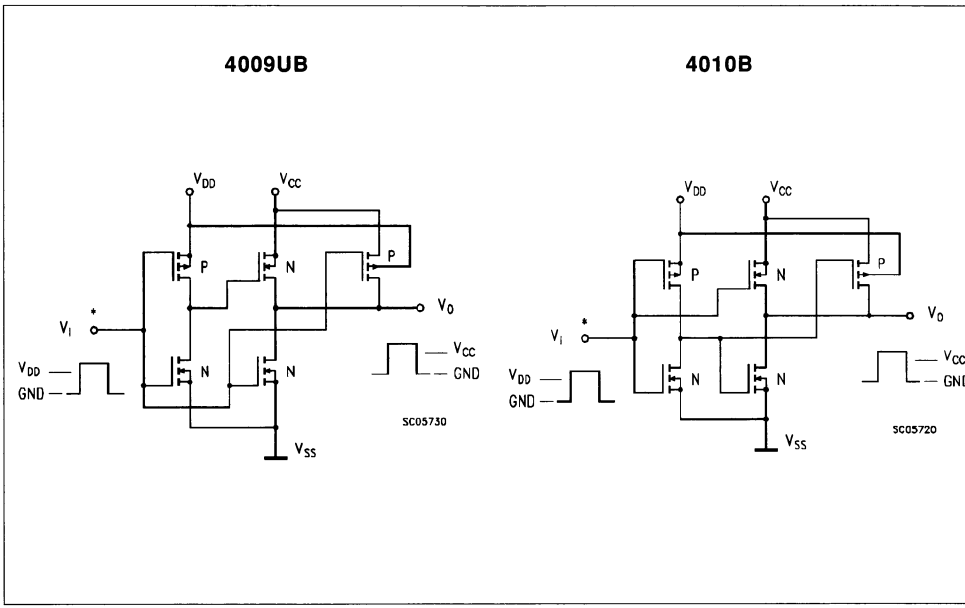
**4009UB**




**4010B**



## SCHEMATIC DIAGRAM: COS/MOS TO DTL OR TTL CONVERTER (1 of 6 identical units)




Connect $V_{CC}$ to DTL or TTL supply and $V_{DD}$ to COS/MOS supply

## ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ * | Supply Voltage: **HCC** Types<br>**HCF** Types | -0.5 to +20<br>-0.5 to +18 | V<br>V |
| $V_I$ | Input Voltage | -0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for Top = Full Package Temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage: **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditios $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{LOW}$ * Min. | $T_{LOW}$ * Max. | 25 °C Min. | 25 °C Typ. | 25 °C Max. | $T_{HIGH}$ * Min. | $T_{HIGH}$ * Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/5 | | | 5 | | 1 | | 0.02 | 1 | | 30 | μA |
| | | | 0/10 | | | 10 | | 2 | | 0.02 | 2 | | 60 | |
| | | | 0/15 | | | 15 | | 4 | | 0.02 | 4 | | 120 | |
| | | | 0/20 | | | 20 | | 20 | | 0.04 | 20 | | 600 | |
| | | HCF Types | 0/5 | | | 5 | | 4 | | 0.02 | 4 | | 30 | |
| | | | 0/10 | | | 10 | | 8 | | 0.02 | 8 | | 60 | |
| | | | 0/15 | | | 15 | | 16 | | 0.02 | 16 | | 120 | |
| $V_{OH}$ | Output High Voltage | | 0/5 | | | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage (4009UB) | | | 0.5 | | 5 | 4 | | 4 | | | 4 | | V |
| | | | | 1 | | 10 | 8 | | 8 | | | 8 | | |
| | | | | 1.5 | | 15 | 12.5 | | 12.5 | | | 12.5 | | |
| $V_{IH}$ | Input High Voltage (4010B) | | | 4.5 | | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 9 | | 10 | 7 | | 7 | | | 7 | | |
| | | | | 13.5 | | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage (4009UB) | | | 4.5 | | 5 | | 1 | | | 1 | | 1 | V |
| | | | | 9 | | 10 | | 2 | | | 2 | | 2 | |
| | | | | 13.5 | | 15 | | 2.5 | | | 2.5 | | 2.5 | |
| $V_{IL}$ | Input Low Voltage (4010B) | | | 0.5 | | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 1 | | 10 | | 3 | | | 3 | | 3 | |
| | | | | 1.5 | | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/5 | 2.5 | | 5 | -1 | | -0.8 | -1.6 | | -0.58 | | mA |
| | | | 0/5 | 4.6 | | 5 | -0.25 | | -0.2 | -0.4 | | -0.15 | | |
| | | | 0/10 | 9.5 | | 10 | -0.55 | | -0.45 | -0.9 | | -0.33 | | |
| | | | 0/15 | 13.5 | | 15 | -1.65 | | -1.5 | -3 | | -1.1 | | |
| | | HCF Types | 0/5 | 2.5 | | 5 | -0.9 | | -0.8 | -1.6 | | -0.65 | | |
| | | | 0/5 | 4.6 | | 5 | -0.23 | | -0.2 | -0.4 | | -0.18 | | |
| | | | 0/10 | 9.5 | | 10 | -0.5 | | -0.45 | -0.9 | | -0.38 | | |
| | | | 0/15 | 13.5 | | 15 | -1.6 | | -1.5 | -3 | | -1.25 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/5 | 0.4 | | 5 | 3.75 | | 3 | 4 | | 2.1 | | mA |
| | | | 0/10 | 0.5 | | 10 | 10 | | 8 | 10 | | 5.6 | | |
| | | | 0/15 | 1.5 | | 15 | 30 | | 24 | 36 | | 16 | | |
| | | HCF Types | 0/5 | 0.4 | | 5 | 3.6 | | 3 | 4 | | 2.4 | | |
| | | | 0/10 | 0.5 | | 10 | 0.96 | | 8 | 10 | | 6.4 | | |
| | | | 0/15 | 1.5 | | 15 | 40 | | 24 | 36 | | 1.9 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | | 0/18 | | | 18 | | ±0.1 | | $±10^{-5}$ | ±0.1 | | ±1 | μA |
| $C_I$ | Input Capacitance | 4009UB | | Any Input | | | | | | 15 | 22.6 | | | pF |
| | | 4010B | | | | | | | | 5 | 7.5 | | | |

* $T_{LOW}$ = -55 °C for **HCC** device: -40 °C for **HCF** device.

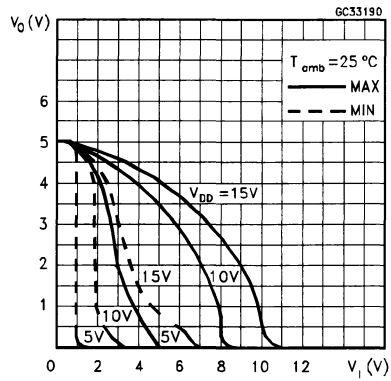
* $T_{HIGH}$ = +125 °C for **HCC** device: +85 °C for **HCF** device.

The Noise Margin for both "1" and "0" level is: 1V min. with $V_{DD}$ = 5 V, 2 V min. with $V_{DD}$ = 10 V, 2.5 V min. with $V_{DD}$ = 15 V

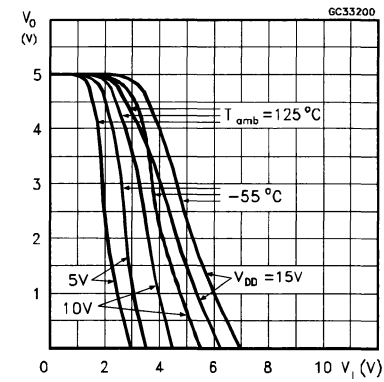
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 KΩ, typical temperature coefficent for all $V_{DD}$ values is 03 %/°C, all input rise and fall times= 20 ns)

| Symbol | Parameter | Test Conditions | | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | $V_{DD}$ (V) | $V_I$ (V) | $V_{CC}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$ | Propagation Delay Time (4009UB) | 5 | 5 | 5 | | 70 | 140 | ns |
| | | 10 | 10 | 10 | | 40 | 80 | |
| | | 10 | 10 | 5 | | 35 | 70 | |
| | | 15 | 15 | 15 | | 30 | 60 | |
| | | 15 | 15 | 5 | | 30 | 60 | |
| $t_{PLH}$ | Propagation Delay Time (4010B) | 5 | 5 | 5 | | 100 | 200 | ns |
| | | 10 | 10 | 10 | | 50 | 100 | |
| | | 10 | 10 | 5 | | 50 | 100 | |
| | | 15 | 15 | 15 | | 35 | 70 | |
| | | 15 | 15 | 5 | | 35 | 70 | |
| $t_{PHL}$ | Propagation Delay Time (4009UB) | 5 | 5 | 5 | | 30 | 60 | ns |
| | | 10 | 10 | 10 | | 20 | 40 | |
| | | 10 | 10 | 5 | | 15 | 30 | |
| | | 15 | 15 | 15 | | 15 | 30 | |
| | | 15 | 15 | 5 | | 10 | 20 | |
| $t_{PHL}$ | Propagation Delay Time (4010B) | 5 | 5 | 5 | | 65 | 130 | ns |
| | | 10 | 10 | 10 | | 35 | 70 | |
| | | 10 | 10 | 5 | | 30 | 70 | |
| | | 15 | 15 | 15 | | 25 | 50 | |
| | | 15 | 15 | 5 | | 20 | 40 | |
| $t_{TLH}$ | Transition Time | 5 | 5 | 5 | | 150 | 350 | ns |
| | | 10 | 10 | 10 | | 75 | 150 | |
| | | 15 | 15 | 15 | | 55 | 110 | |
| $t_{THL}$ | Transition Time | 5 | 5 | 5 | | 35 | 70 | ns |
| | | 10 | 10 | 10 | | 20 | 40 | |
| | | 15 | 15 | 15 | | 15 | 30 | |

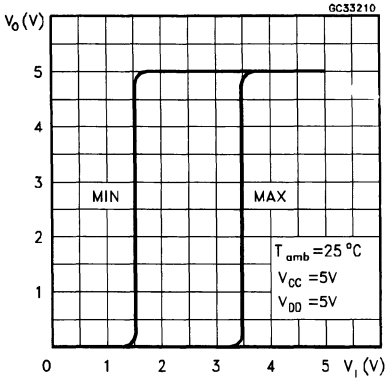
Minimum and Maximum Voltage Transfer Characteristics for 4009UB



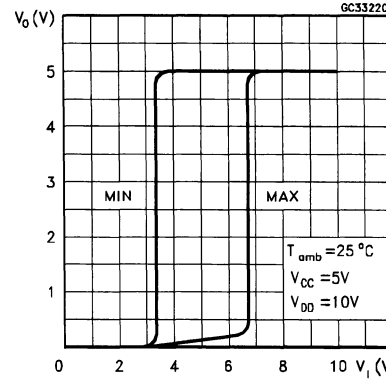

Typical Voltage Transfer Characteristics As a Function of Temperature for 4009UB



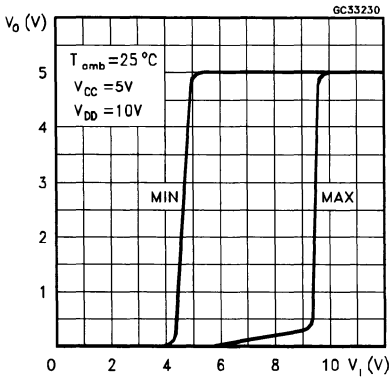
Minimum and Maximum Voltage Transfer Characteristics for 4010B



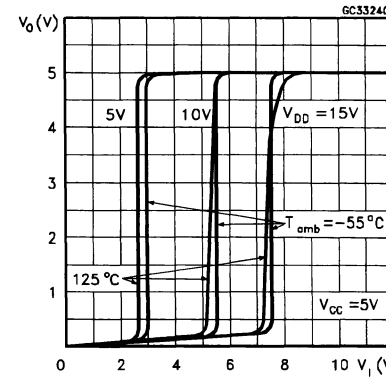

Minimum and Maximum Voltage Transfer Characteristics for 4010B



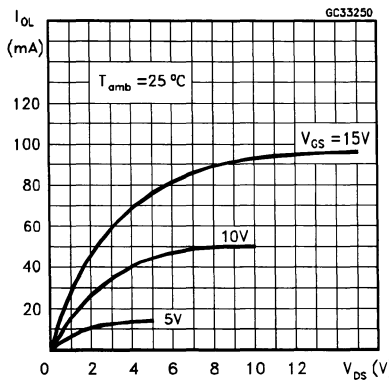

Minimum and Maximum Voltage Transfer Characteristics for 4010B



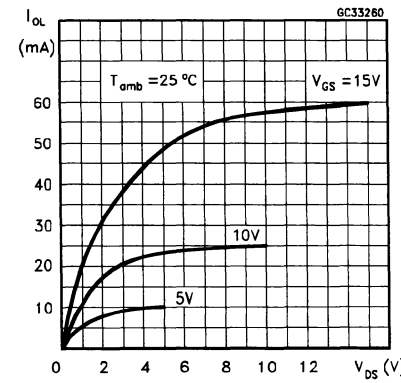

Typical Voltage Transfer Characteristics As a Function ot Temperature for 4010B



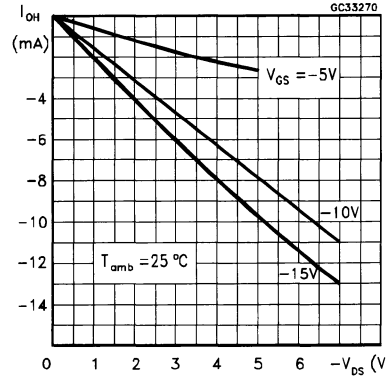

Typical Output Los (sink) Current Characteristics



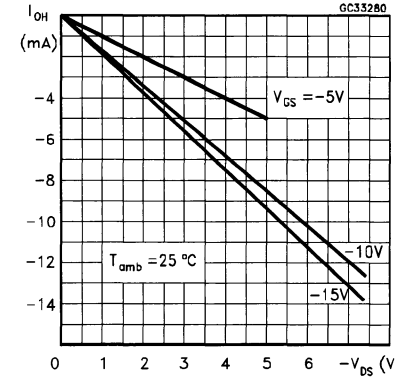

Minimum output Low (sink) Current Characteristics



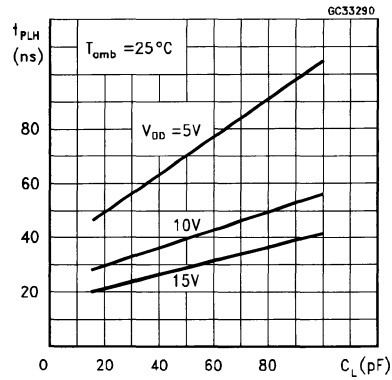
Typical Output High (source) Current Characteristics



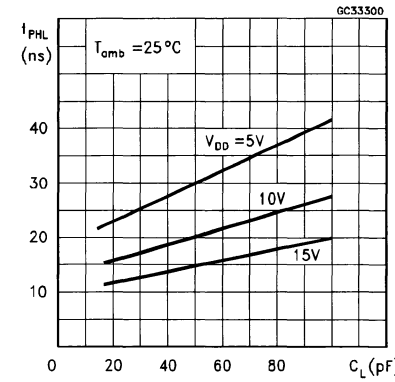

Minimum output High (source) Current Characteristics



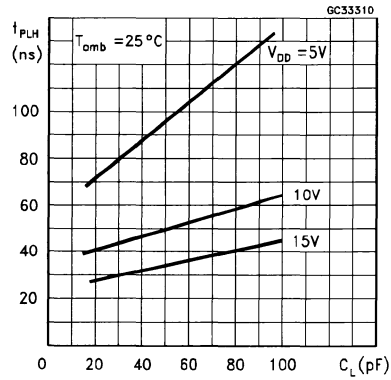

Typical Low to High Propagation Delay Time vs Load Capacitance for 4009UB



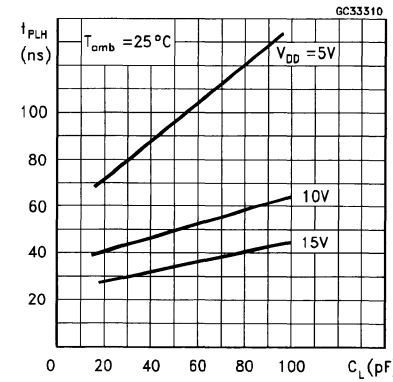

Typical High to Low Propagation Delay Time vs Load Capacitance for 4009UB



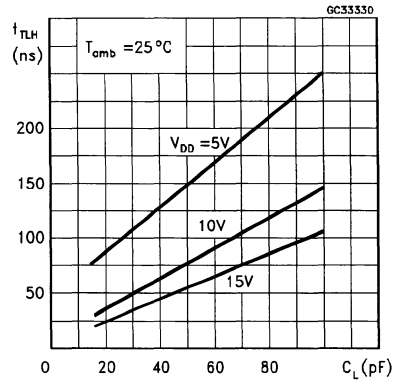

Typical Low to High Propagation Delay Time vs Load Capacitance for 4010B



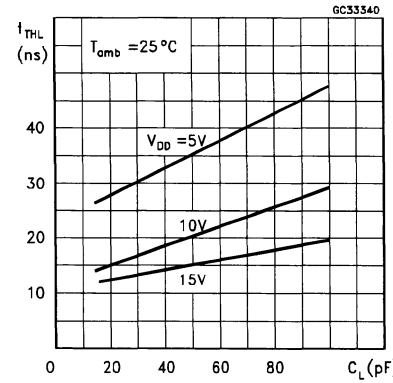

typical High to Low Propagation Delay Time vs Load Capacitance for 4010B



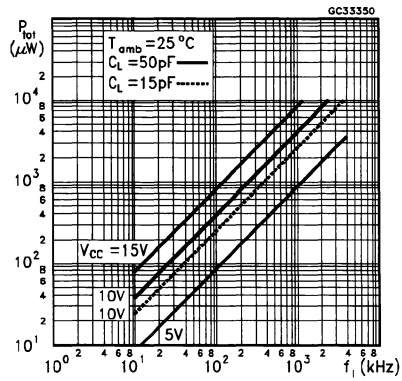
Typical Low to High Transition Time vs Load Capacitance




Typical High to Low Transition Time vs Load Capacitance

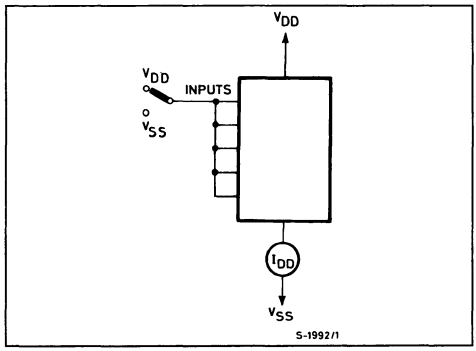



Typical Dissipation Characteristics

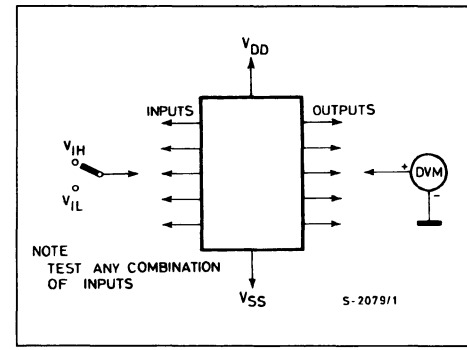


## TEST CIRCUITS

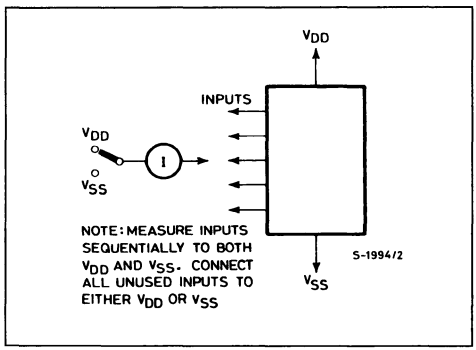
Quiescent Device Current.




Noise Immunity.




Input Leakage Current.

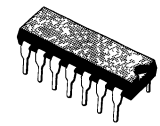


# HCC4011B/12B/23B
# HCF4011B/12B/23B

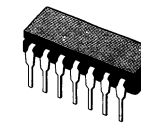
## NAND GATES

**QUAD 2 INPUT HCC/HCF 4011B**
**DUAL 4 INPUT HCC/HCF 4012B**
**TRIPLE 3 INPUT HCC/HCF 4023B**

- PROPAGATION DELAY TIME = 60ns (typ.) AT $C_L$ = 50pF, $V_{DD}$ = 10V
- BUFFERED INPUTS AND OUTPUTS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- 5V, 10V AND 15V PARAMETRIC RATINGS
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

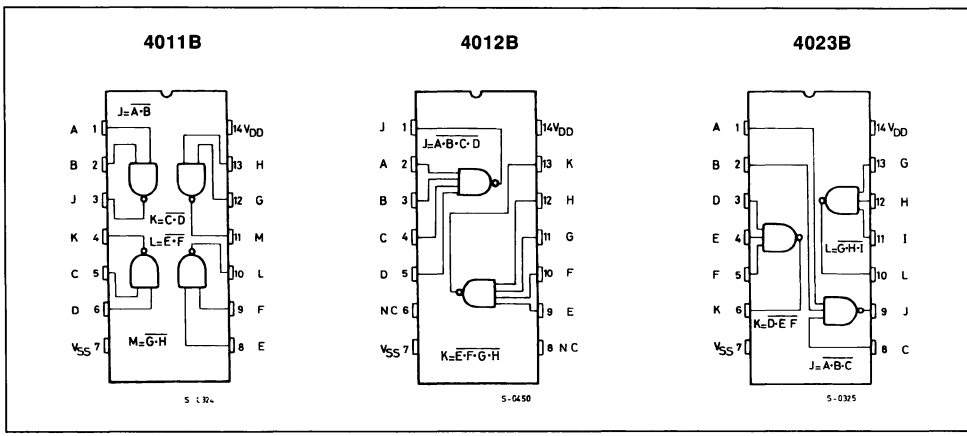
HCC40XXBF HCF40XXBM1
HCF40XXBEY HCF40XXBC1

### DESCRIPTION

The **HCC4011B, HCC4012B** and **HCC4023B** (extended temperature range) and **HCF4011B, HCF4012B** and **HCF4023B** (intermediate temperature range) are monolithic, integrated circuit, available in 14-lead dual in-line plastic or ceramic package and plastic micropackage.

The **HCC/HCF4011B, HCC/HCF4012B** and **HCC/HCF4023B** NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of COS/MOS gates. All inputs and outputs are buffered.

### PIN CONNECTIONS



## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

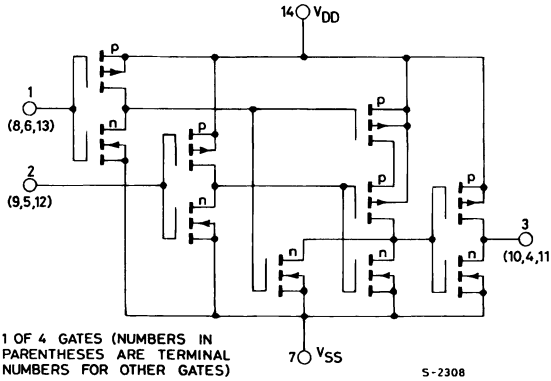
* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

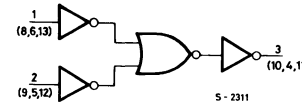
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

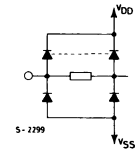
## SCHEMATIC AND LOGIC DIAGRAMS

### 4011B



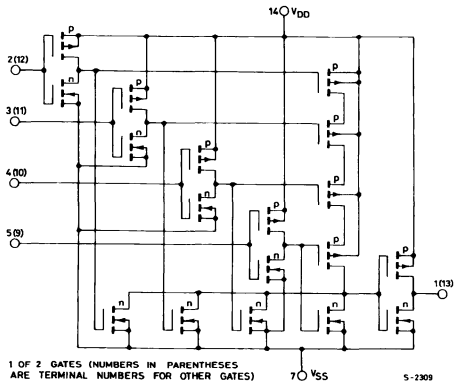

1 OF 4 GATES (NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR OTHER GATES)



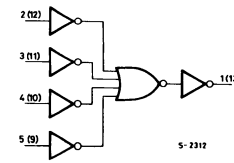



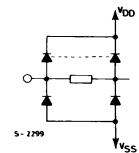

ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

### 4012B



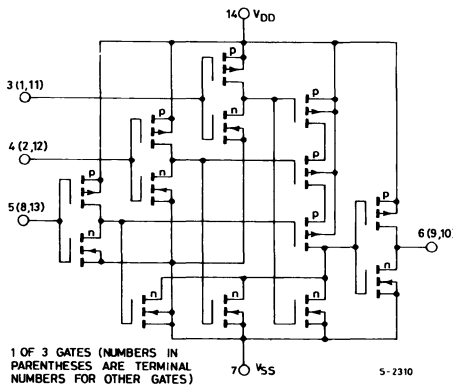

1 OF 2 GATES (NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR OTHER GATES)



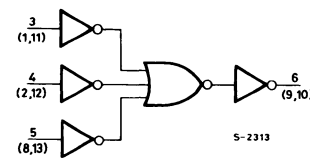



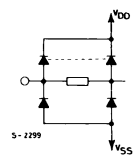

ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

### 4023B




1 OF 3 GATES (NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR OTHER GATES)




ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/5 | | | 5 | | 0.25 | | 0.01 | 0.25 | | 7.5 | μA |
| | | | 0/10 | | | 10 | | 0.5 | | 0.01 | 0.5 | | 15 | |
| | | | 0/15 | | | 15 | | 1 | | 0.01 | 1 | | 30 | |
| | | | 0/20 | | | 20 | | 5 | | 0.02 | 5 | | 150 | |
| | | HCF Types | 0/ 5 | | | 5 | | 1 | | 0.01 | 1 | | 7.5 | |
| | | | 0/10 | | | 10 | | 2 | | 0.01 | 2 | | 15 | |
| | | | 0/15 | | | 15 | | 4 | | 0.01 | 4 | | 30 | |
| $V_{OH}$ | Output High Voltage | | 0/5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1 5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

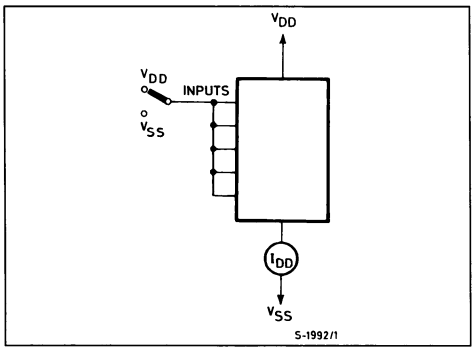
* $T_{LOW}$ = − 55°C for **HCC** device − 40°C for **HCF** device
* $T_{HIGH}$ = + 125°C for **HCC** device + 85°C for **HCF** device
The Noise Margin for both "1" and "0" level is : 1V min with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V with $V_{DD}$ = 15V.

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall times = 20ns)

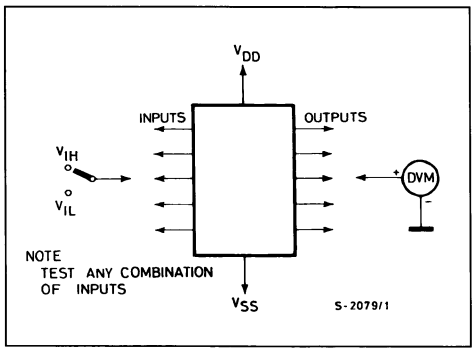
| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time | | 5 | | 125 | 250 | ns |
| | | | 10 | | 60 | 120 | |
| | | | 15 | | 45 | 90 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

**TEST CIRCUITS**

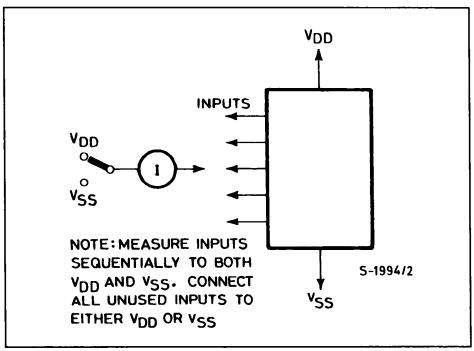
Quiescent Device Current.



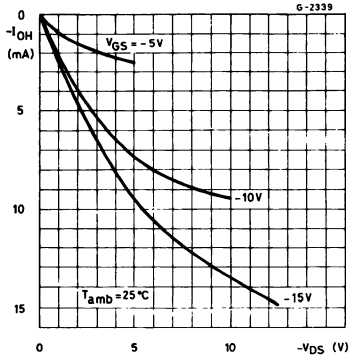

Noise Immunity.



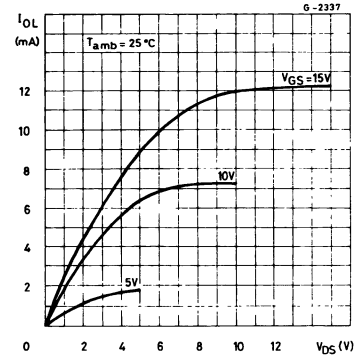

Input Leakage Current.



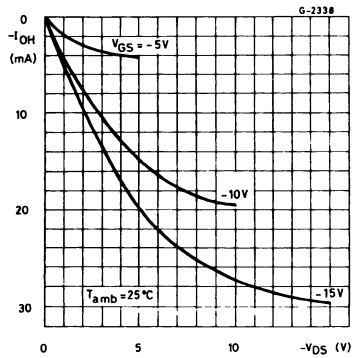
Minimum Output High (source) Current Characteristics.



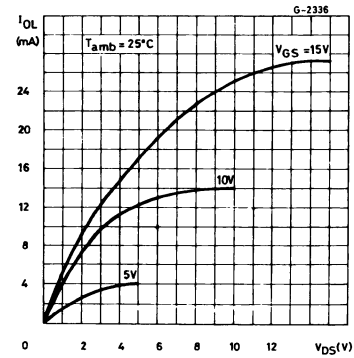

Minimum Output Low (sink) Current Characteristics.



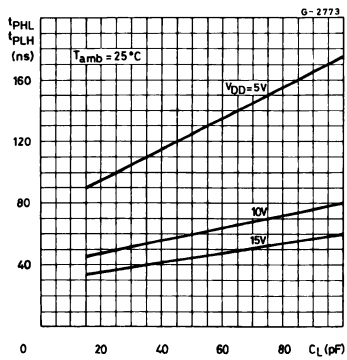

Typical Output High (source) Current Characteristics.



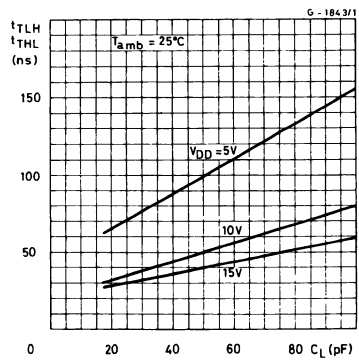

Typical Output Low (sink) Current Characteristics.



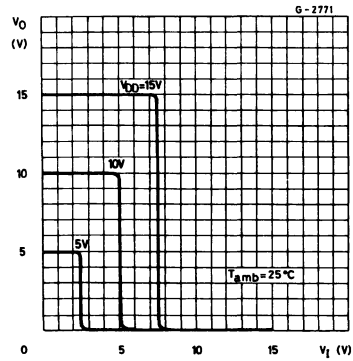

Typical Propagation Delay Time per Gate as a Function of Load Capacitance.



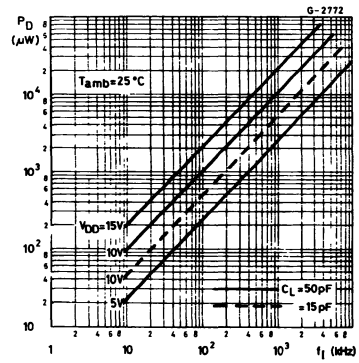

Typical Transition Time vs. Load Capacitance.



Typical Voltage Transfer Characteristics.




Typical Power Dissipation/gate vs Frequency.

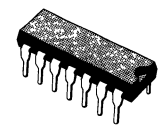


SGS-THOMSON MICROELECTRONICS

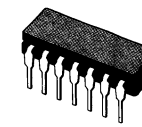
# HCC/HCF4013B

## DUAL 'D' – TYPE FLIP–FLOP

- SET-RESET CAPABILITY
- STATIC FLIP-FLOP OPERATION - RETAINS STATE INDEFINITELY WITH CLOCK LEVEL EITHER "HIGH" OR "LOW"
- MEDIUM-SPEED OPERATION - 16MHz (typ.) CLOCK TOGGLE RATE AT 10V
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

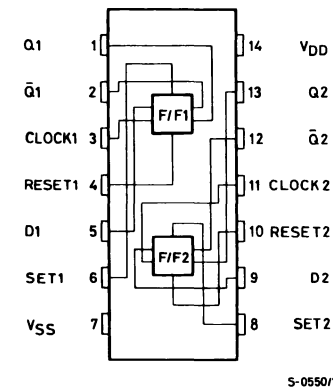
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

| | |
|---|---|
| HCC4013BF | HCF4013BM1 |
| HCF4013BEY | HCF4013BC1 |

**PIN CONNECTIONS**




### DESCRIPTION

The **HCC4013B** (extended temperature range) and **HCF4013B** (intermediate temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and plastic micropackage.

The **HCC/HCF4013B** consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications, and, by connecting $\overline{Q}$ output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the $\overline{Q}$ output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

## ABSOLUTE MAXIMUM RATINGS

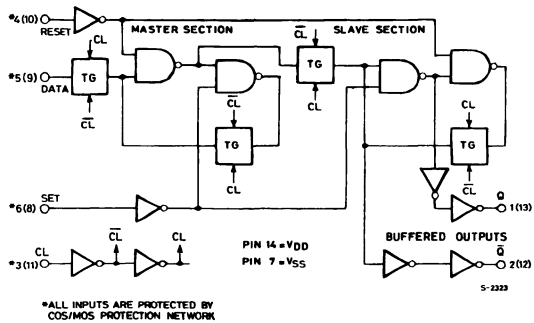
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | – 0.5 to + 20<br>– 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | – 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | – 55 to + 125<br>– 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storasge Temperature | – 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltages are with respect to $V_{SS}$ (GND).

## RECOMMENDED OPERATING CONDITIONS

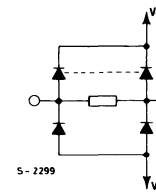
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | – 55 to + 125<br>– 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAM AND TRUTH TABLE (one of two identical flip–flops)




| CL$^{\Delta}$ | D | R | S | Q | $\overline{Q}$ | |
|---|---|---|---|---|---|---|
| ⎍ | 0 | 0 | 0 | 0 | 1 | |
| ⎍ | 1 | 0 | 0 | 1 | 0 | |
| ⎎ | X | 0 | 0 | Q | $\overline{Q}$ | NO CHANGE |
| X | X | 1 | 0 | 0 | 1 | |
| X | X | 0 | 1 | 1 | 0 | |
| X | X | 1 | 1 | 1 | 1 | |

LOGIC 0 = LOW
LOGIC 1 = HIGH
Δ = LOW LEVEL
X = DON'T CARE
N(N)= FF1/FF2 TERMINAL ASSIGNEMENT



**STATIC ELECTRICAL CHARACTERISTICS** (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/5 | | | 5 | | 1 | | 0.02 | 1 | | 30 | μA |
| | | | 0/10 | | | 10 | | 2 | | 0.02 | 2 | | 60 | |
| | | | 0/15 | | | 15 | | 4 | | 0.02 | 4 | | 120 | |
| | | | 0/20 | | | 20 | | 20 | | 0.04 | 20 | | 600 | |
| | | HCF Types | 0/5 | | | 5 | | 4 | | 0.02 | 4 | | 30 | |
| | | | 0/10 | | | 10 | | 8 | | 0.02 | 8 | | 60 | |
| | | | 0/15 | | | 15 | | 16 | | 0.02 | 16 | | 120 | |
| $V_{OH}$ | Output High Voltage | | 0/5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$= − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$= + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5 V min. with $V_{DD}$ = 15V.

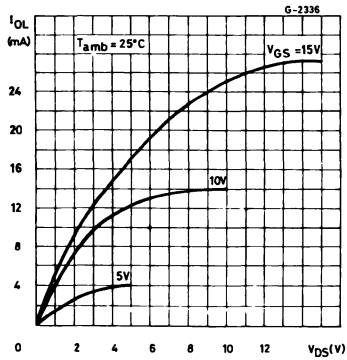
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ = 0.3%/°C values, all input rise and fall time = 20ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time (clock to Q or $\overline{Q}$ outputs) | | 5 | | 150 | 300 | ns |
| | | | 10 | | 65 | 130 | |
| | | | 15 | | 45 | 90 | |
| $t_{PLH}$ | Propagation Delay Time (set to Q or reset to $\overline{Q}$) | | 5 | | 150 | 300 | ns |
| | | | 10 | | 65 | 130 | |
| | | | 15 | | 45 | 90 | |
| $t_{PHL}$ | Propagation Delay Time (set to Q or reset to Q) | | 5 | | 200 | 400 | ns |
| | | | 10 | | 85 | 170 | |
| | | | 15 | | 60 | 120 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $f_{CL}$* | Maximum Clock Input Frequency | | 5 | 3.5 | 7 | | MHz |
| | | | 10 | 8 | 16 | | |
| | | | 15 | 12 | 24 | | |
| $t_W$ | Cock Pulse Width | | 5 | 140 | 70 | | ns |
| | | | 10 | 60 | 30 | | |
| | | | 15 | 40 | 20 | | |
| $t_r$, $t_f$** | Clock Input Rise or Fall Time | | 5 | | | 15 | μs |
| | | | 10 | | | 4 | |
| | | | 15 | | | 1 | |
| $t_W$ | Set or Reset Pulse Width | | 5 | 180 | 90 | | ns |
| | | | 10 | 80 | 40 | | |
| | | | 15 | 50 | 25 | | |
| $t_{setup}$ | Data Setup Time | | 5 | 40 | 20 | | ns |
| | | | 10 | 20 | 10 | | |
| | | | 15 | 15 | 7 | | |

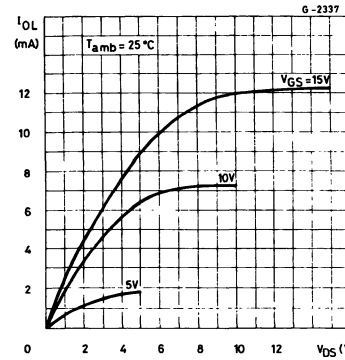
*Input tr, tf = 5ns.

** If more than unit is cascaded in a parallel clocked application, $t_r$ should be made less than or equal to the sum of the fixed propagation delay time at 15pF and the transition time of the carry output driving stage for the estimated capacitive load.

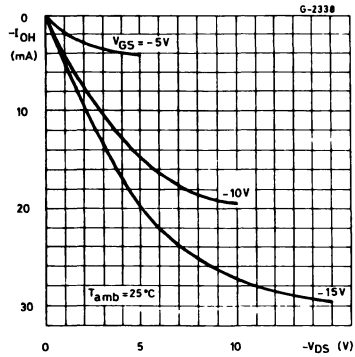
Typical Output Low (sink) Current Characteristics.



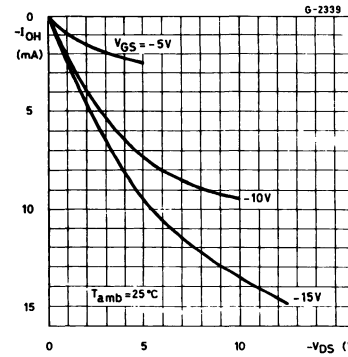

Minimum Output Low (sink) Current Characteristics.



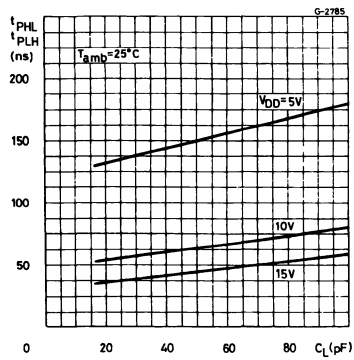

Typical Output High (source) Current Characteristics.



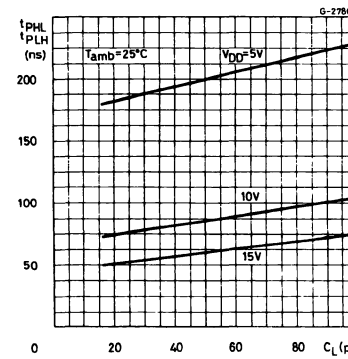

Minimum Output High (source) Current Characteristics.



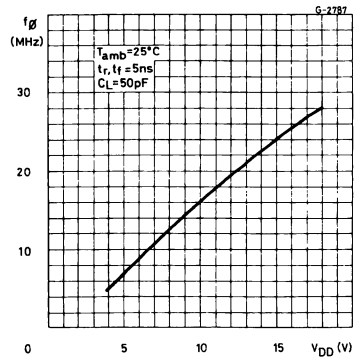

Typical Propagation Delay Time vs. Load Capacitance (CLOCK or SET to Q, CLOCK or RESET to $\overline{Q}$).



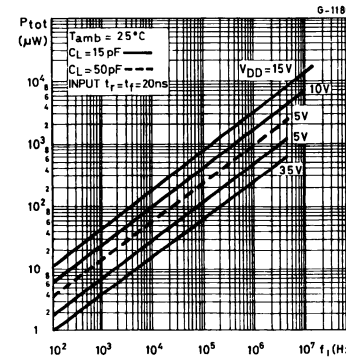

Typical Propagation Delay Time vs. Load Capacitance (SET to $\overline{Q}$ or RESET to Q).



Typical Maximum Clock Frequency vs. Supply Voltage.

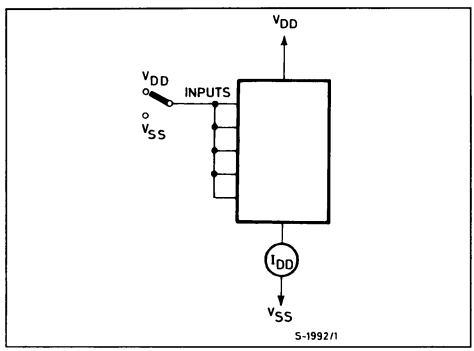



Typical Power Dissipation Device vs. Frequency.

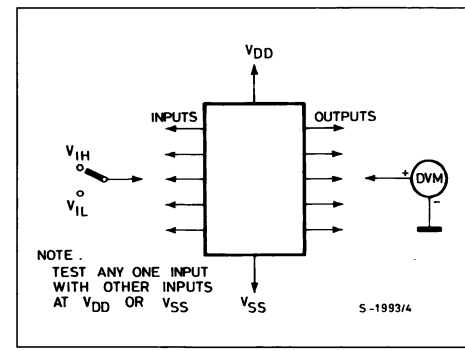



## TEST CIRCUITS

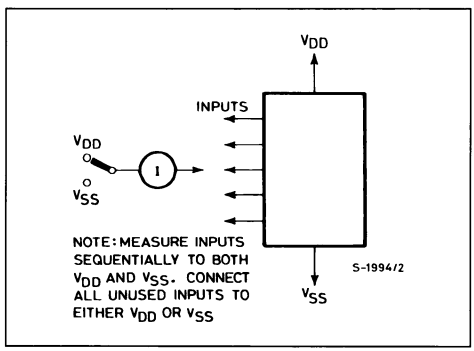
Quiescent Device Current.




Noise Immunity.




Input Leakage Current.



# HCC/HCF4014B
# HCC/HCF4021B

## 8-STAGE STATIC SHIFT REGISTERS

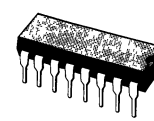
**4014B SYNCHRONOUS PARALLEL OR SERIAL INPUT/SERIAL OUTPUT**

**4021B ASYNCHRONOUS PARALLEL INPUT OR SYNCHRONOUS SERIAL INPUT/SERIAL OUTPUT**

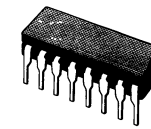
- MEDIUM-SPEED OPERATION-12MHz (typ.) CLOCK RATE AT $V_{DD} - V_{SS} = 10V$
- FULLY STATIC OPERATION
- 8 MASTER-SLAVE FLIP-FLOPS PLUS OUTPUT BUFFERING AND CONTROL GATING
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

### DESCRIPTION

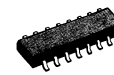
The **HCC4014B, HCC4021B** (extended temperature range) and the **HCF4014B, HCF4021B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF4014B** and **HCC/HCF4021B** series types are 8-stage parallel-or serial-input/serial-output registers having common CLOCK and PARALLEL/SERIAL CONTROL inputs, a single SERIAL data input, and individual parallel "JAM" inputs to each register stage. Each register stage is a D type, master-slave flip-flop in addition to an output from stage 8, "Q" outputs are also available from stages 6 and 7. Parallel as well as serial entry is made into the register synchronously with the positive clock line transition in the **HCC/HCF4014B**. In the **HCC/HCF4021B** serial entry is synchronous with the clock but parallel entry is asynchronous. In both types, entry is controlled by the PARALLEL/SERIAL CONTROL input. When the PARALLEL/SERIAL CONTROL input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the PARALLEL/SERIAL CONTROL input is high, data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line. In the **HCC/HCF4021B**, the CLOCK input of the internal stage is "forced" when asynchronous parallel entry is made. Register expansion using multiple package is permitted.



**EY**
(Plastic Package)



**F**
(Ceramic Package)



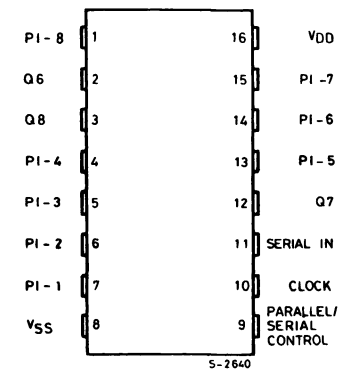
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

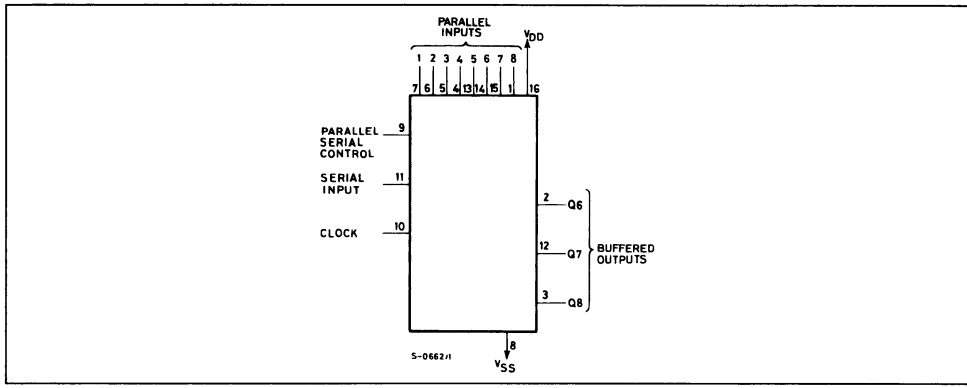
**ORDER CODES :**

HCC40XXBF HCF40XXBM1
HCF40XXBEY HCF40XXBC1

**PIN CONNECTIONS**



## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

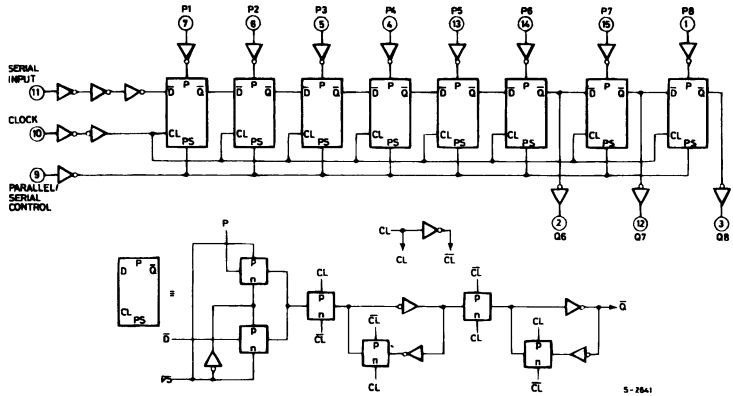
* All voltage values are referred to $V_{SS}$ pin voltage.

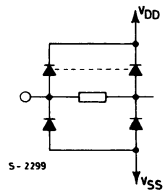
## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAMS

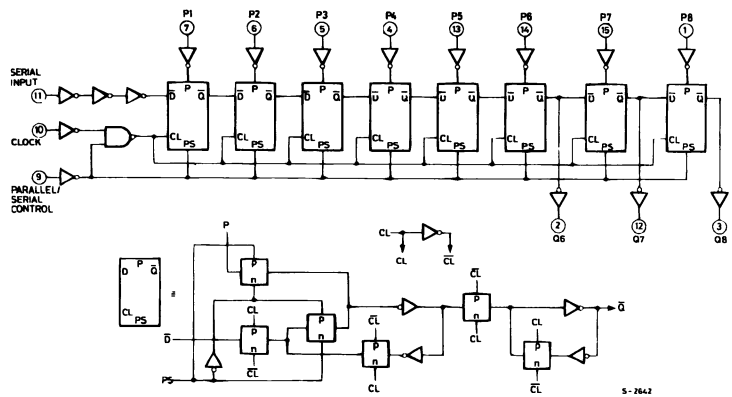
### 4014B

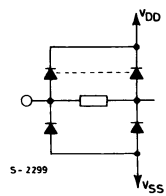



ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

### 4021B




ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

## TRUTH TABLES

HCC/HCF 4014B

| CL | Serial Input | Parallel/ Serial Control | PI–1 | PI–n | $Q_1$ (internal) | $Q_n$ | |
|---|---|---|---|---|---|---|---|
| ⎍ | X | 1 | 0 | 0 | 0 | 0 | |
| ⎍ | X | 1 | 1 | 0 | 1 | 0 | |
| ⎍ | X | 1 | 0 | 1 | 0 | 1 | |
| ⎍ | X | 1 | 1 | 1 | 1 | 1 | |
| ⎍ | 0 | 0 | X | X | 0 | $Q_n-1$ | |
| ⎍ | 1 | 0 | X | X | 1 | $Q_n-1$ | I |
| ⎺_ | X | X | X | X | $Q_1$ | $Q_n$ | NC |

X = don't care case.
NC = no change.

HCC/HCF4021B

| CL | Serial Input | Parallel/ Serial Control | PI–1 | PI–n | $Q_1$ (internal) | $Q_n$ | |
|---|---|---|---|---|---|---|---|
| X | X | 1 | 0 | 0 | 0 | 0 | |
| X | X | 1 | 0 | 1 | 0 | 1 | |
| X | X | 1 | 1 | 0 | 1 | 0 | |
| X | X | 1 | 1 | 1 | 1 | 1 | |
| ⎍ | 0 | 0 | X | X | 0 | $Q_n-1$ | |
| | 1 | 0 | X | X | 1 | $Q_n-1$ | I |
| ⎺_ | X | 0 | X | X | $Q_1$ | $Q_n$ | NC |

X = don't care case.
NC = no change

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |

* $T_{Low}$ = – 55°C for **HCC** device – 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is · 1V min with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2 5 V min with $V_{DD}$ = 15V

## STATIC ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | – 2 | | – 1.6 | – 3.2 | | – 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | – 0.64 | | – 0.51 | – 1 | | – 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | – 1.6 | | – 1.3 | – 2.6 | | – 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | – 4.2 | | – 3.4 | – 6.8 | | – 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | – 1.53 | | – 1.36 | – 3.2 | | – 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | – 0.52 | | – 0.44 | – 1 | | – 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | – 1.3 | | – 1.1 | – 2.6 | | – 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | – 3.6 | | – 3.0 | – 6.8 | | – 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = – 55°C for **HCC** device . – 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is . 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2 5 V min with $V_{DD}$ = 15V.

## DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ = 0.3%/°C values, all input rise and fall time = 20ns)

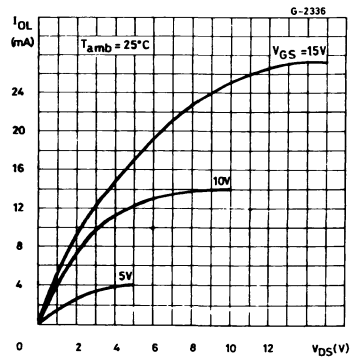
| Symbol | Parameter | Test Conditions | $V_{DD}$ (V) | Value Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **CLOCKED OPERATION** | | | | | | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time | | 5 | | 160 | 320 | ns |
| | | | 10 | | 80 | 160 | |
| | | | 15 | | 60 | 120 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $f_{CL}$* | Maximum Clock Input Frequency | | 5 | 3 | 6 | | MHz |
| | | | 10 | 6 | 12 | | |
| | | | 15 | 8.5 | 17 | | |
| $t_W$ | Clock Pulse Width | | 5 | 180 | 90 | | ns |
| | | | 10 | 80 | 40 | | |
| | | | 15 | 50 | 25 | | |

* If more than one unit is cascaded $t_rCL$ should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage of the estimated capacitive load.

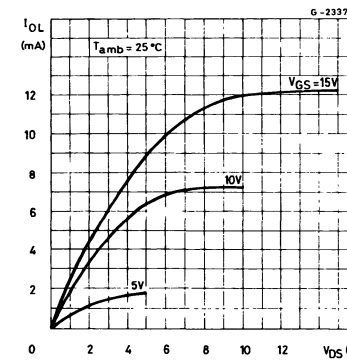
| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| **CLOCKED OPERATION** | | | | | | | |
| $t_r$, $t_f$ | Clock Input Rise or Fail Time | | 5 | | | 15 | µs |
| | | | 10 | | | 15 | |
| | | | 15 | | | 15 | |
| $t_{setup}$ | Setup Time, serial Input (ref to CL) | | 5 | 120 | 60 | | ns |
| | | | 10 | 80 | 40 | | |
| | | | 15 | 60 | 30 | | |
| $t_{setup}$ | Setup Time, parallel Inputs (4014B) (ref. to CL) | | 5 | 80 | 40 | | ns |
| | | | 10 | 50 | 25 | | |
| | | | 15 | 40 | 20 | | |
| $t_{setup}$ | Setup Time, parallel Inputs (4021B) (ref. to P/S) | | 5 | 50 | 25 | | ns |
| | | | 10 | 30 | 15 | | |
| | | | 15 | 20 | 10 | | |
| $t_{setup}$ | Setup Time, parallel/serial Control (4014B) (ref. to CL) | | 5 | 180 | 90 | | ns |
| | | | 10 | 80 | 40 | | |
| | | | 15 | 60 | 30 | | |
| $t_{hold}$ | Hold Time, serial in, parallel in, parallel/serial Control | | 5 | 0 | | | ns |
| | | | 10 | 0 | | | |
| | | | 15 | 0 | | | |
| $t_{WH}$ | P/S Pulse Widht (4021B) | | 5 | 160 | 80 | | ns |
| | | | 10 | 80 | 40 | | |
| | | | 15 | 50 | 25 | | |
| $t_{rem}$ | P/S Removal, time (4021B) (ref. to CL) | | 5 | 280 | 140 | | ns |
| | | | 10 | 140 | 70 | | |
| | | | 15 | 100 | 50 | | |

* If more than one unit is cascaded $t_rCL$ should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage of the estimated capacitive load.

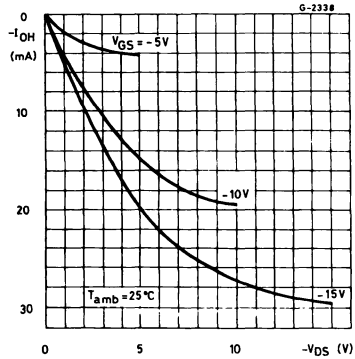
Typical Output Low (sink) Current Characteristics.



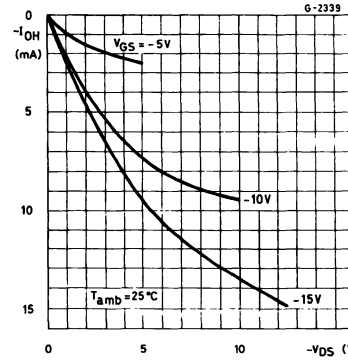

Minimum Output Low (sink) Current Characteristics.



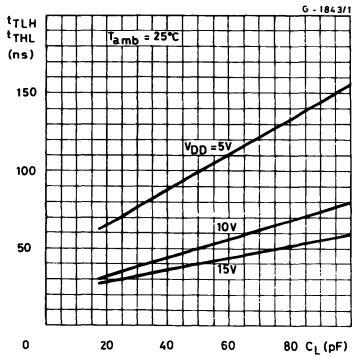
Typical Output High (source) Current Characteristics.



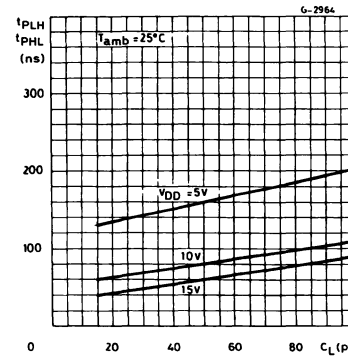

Minimum Output High (source) Current Characteristics.



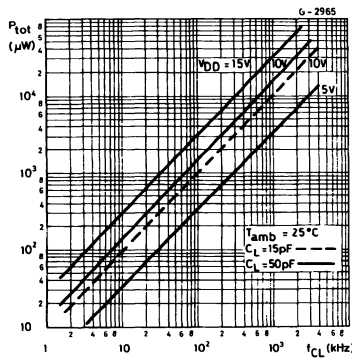

Typical Transition Time vs. Load Capacitance.




Typical Propagation Delay Time vs. Load Capacitance.

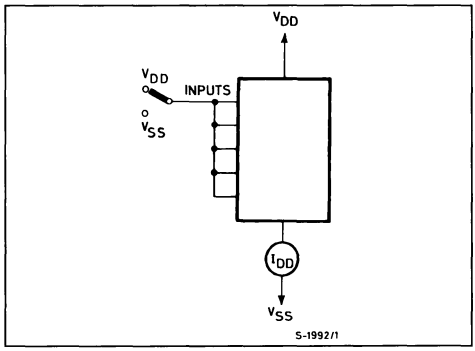



Typical Dynamic Power Dissapating vs. Clock Input Frequency.

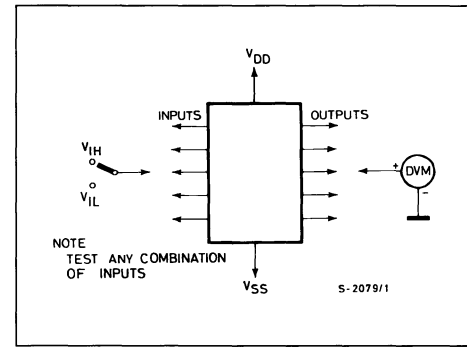


## TEST CIRCUITS

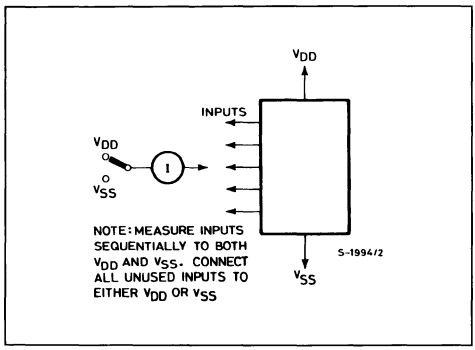
Quiescent Device Current.



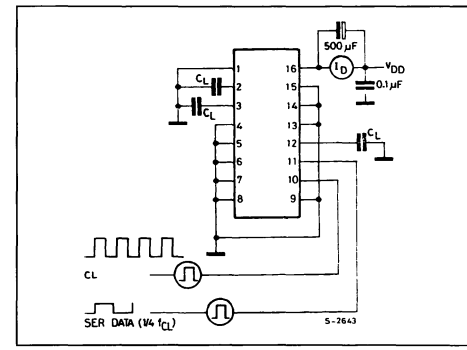

Noise Immunity.




Input Leakage Current.




Dynamic Power Dissipation.



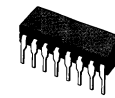
SGS-THOMSON MICROELECTRONICS

# HCC/HCF4015B

## DUAL 4-STAGE STATIC SHIFT REGISTER WITH SERIAL INPUT/PARALLEL OUTPUT

- MEDIUM SPEED OPERATION : 12MHz (typ.) CLOCK RATE AT $V_{DD}$ - $V_{SS}$ = 10V
- FULLY STATIC OPERATION
- 8 MASTER-SLAVE FLIP-FLOPS PLUS INPUT AND OUTPUT BUFFERING
- HIGH NOISE IMMUNITY
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

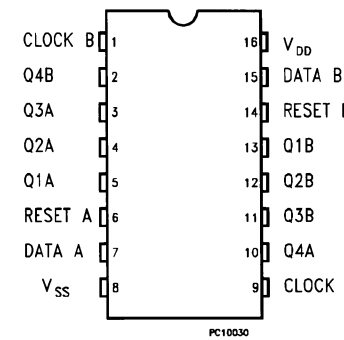
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4015BF HCF4015BM1
HCF4015BEY HCF4015BC1

**PIN CONNECTIONS**

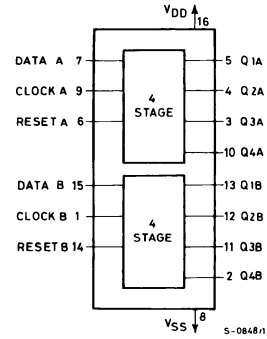



### DESCRIPTION

The **HCC4015B** (extended temperature range) and **HCF4015B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and plastic micropackage.

The **HCC/HCF4015B** consists of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent CLOCK and RESET inputs as well as a single serial DATA input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the DATA input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one **HCC/HCF4015B** package, or to more than 8 stages using additional **HCC/HCF4015B**'s is possible.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storasge Temperature | − 65 to + 150 | °C |

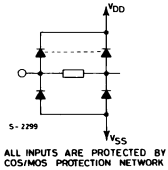
Stresses above those listed under "Absolute Maximum Ratings "may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

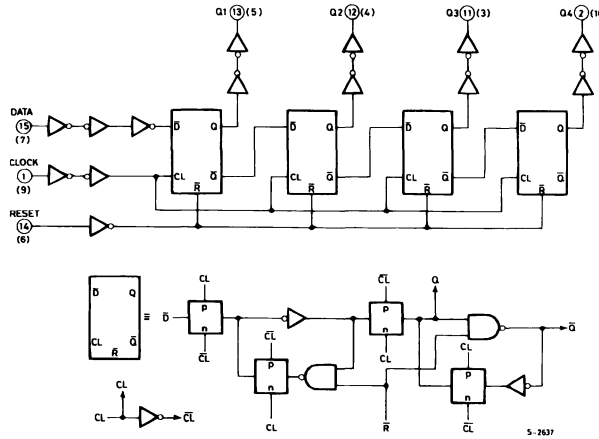
* All voltage values are referred to $V_{SS}$ pin voltage

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAMS AND TRUTH TABLE




| CL | D | R | $Q_1$ | $Q_n$ |
|---|---|---|---|---|
| ⌐¯ | 0 | 0 | 0 | $Q_{n-1}$ |
| ⌐¯ | 1 | 0 | 1 | $Q_{n-1}$ |
| ¯⌐ | X | 0 | $Q_1$ | $Q_n$ (no. change) |
| X | X | 1 | 0 | 0 |

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1 5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | – 2 | | – 1 6 | – 3.2 | | – 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | – 0.64 | | – 0.51 | – 1 | | – 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | – 1.6 | | – 1.3 | – 2.6 | | – 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | – 4.2 | | – 3.4 | – 6.8 | | – 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | – 1.53 | | – 1.36 | – 3.2 | | – 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | – 0.52 | | – 0.44 | – 1 | | – 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | – 1.3 | | – 1.1 | – 2.6 | | – 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | – 3.6 | | – 3.0 | – 6.8 | | – 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1 3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

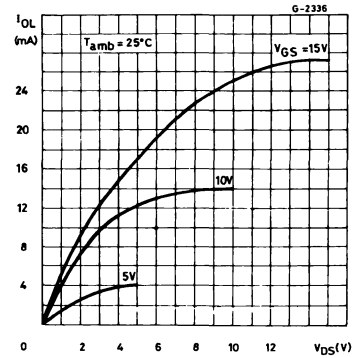
* $T_{Low}$= – 55°C for **HCC** device : – 40°C for **HCF** device
* $T_{High}$= + 125°C for **HCC** device : + 85°C for **HCF** device
The Noise Margin for both "1" and "0" level is . 1V min with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2 5 V min with $V_{DD}$ = 15V.

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3 %/°C, all input rise and fall times = 20 ns)

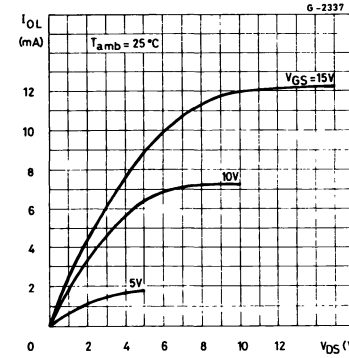
| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| **CLOCKED OPERATION** | | | | | | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time (carry out or decoded out lines) | | 5 | | 160 | 320 | ns |
| | | | 10 | | 80 | 160 | |
| | | | 15 | | 60 | 120 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time (carry out or decoded out lines) | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $f_{CL}$ | Maximum Clock Input Frequency | | 5 | 3 | 6 | | MHz |
| | | | 10 | 6 | 12 | | |
| | | | 15 | 8.5 | 17 | | |
| $t_W$ | Clock Pulse Width | | 5 | 180 | 90 | | ns |
| | | | 10 | 80 | 40 | | |
| | | | 15 | 50 | 25 | | |
| $t_r$, $t_f$* | Clock Input Rise or Fall Time | | 5 | | | 15 | µs |
| | | | 10 | | | 15 | |
| | | | 15 | | | 15 | |
| $t_{setup}$ | Data Setup Time | | 5 | 70 | 35 | | ns |
| | | | 10 | 40 | 20 | | |
| | | | 15 | 30 | 15 | | |
| **RESET OPERATION** | | | | | | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time | | 5 | | 200 | 400 | ns |
| | | | 10 | | 100 | 200 | |
| | | | 15 | | 80 | 160 | |
| $t_W$ | Reset Pulse Width | | 5 | 200 | 100 | | ns |
| | | | 10 | 80 | 40 | | |
| | | | 15 | 60 | 30 | | |

* If more than unit is cascaded in the parallel clocked application, $t_rCL$ should be made less than or equal to the sum of the fixed propagation delay at 15pF and the transition time of the carry output driving stage for the estimated capacitive load

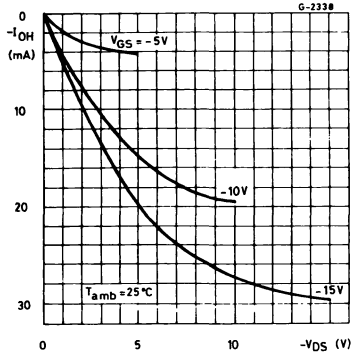
Typical Output Low (sink) Current Characteristics.



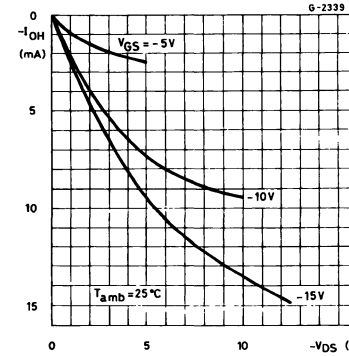

Minimum Output Low (sink) Current Characteristics.



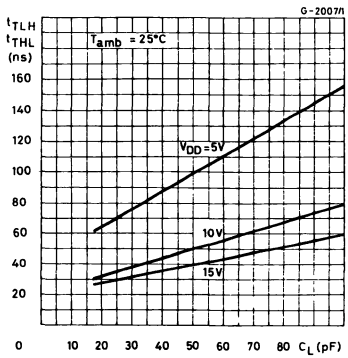

Typical Output High (source) Current Characteristics.



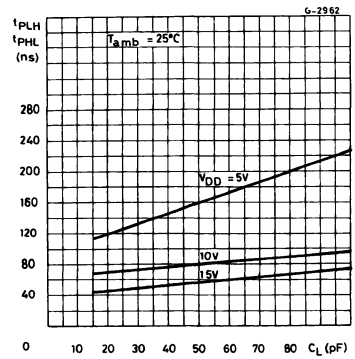

Minimum Output High (source) Current Characteristics.



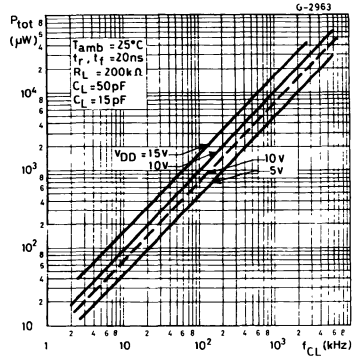

Typical transition Time vs. Load Capacitance.




Typical propagation Delay Time vs. Load Capacitance..

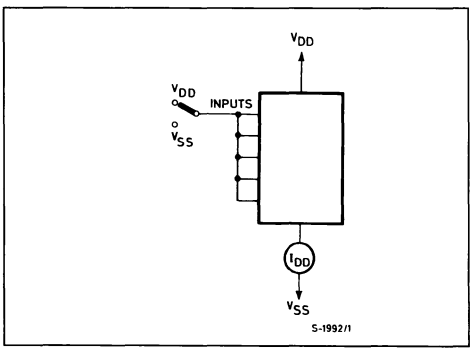


Typical Dynamic Power Dissipation vs. Frequency.

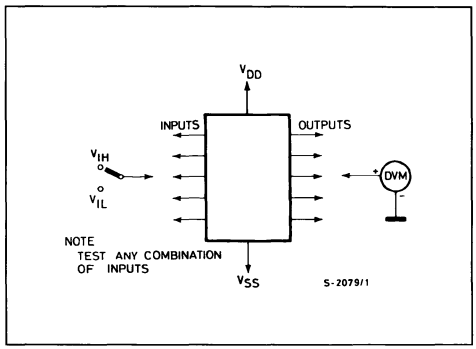



## TEST CIRCUITS

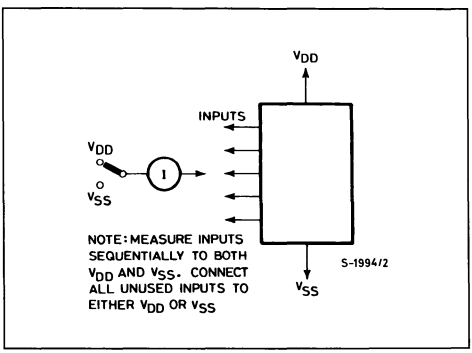
Quiescent Device Current.



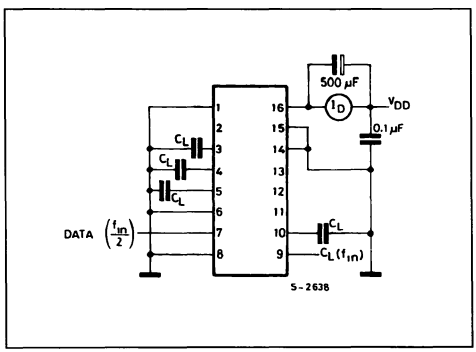

Input current.




Input Voltage.




Power Dissipation.



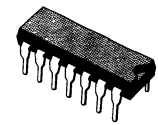
# QUAD BILATERAL SWITCH

- 20V DIGITAL OR ± 10V PEAK-TO-PEAK SWITCHING
- 280Ω TYPICAL ON RESISTANCE FOR 15V OPERATION
- SWITCH ON RESISTANCE MATCHED TO WITHIN 10Ω TYP. OVER 15V SIGNAL INPUT RANGE
- HIGH ON/OFF OUTPUT-VOLTAGE RATIO : 65dB TYP. @ $f_{is}$ = 10kHz, $R_L$ = 10kΩ
- HIGH DEGREE OF LINEARITY : < 0.5% DISTORTION TYP. @ $f_{is}$ = 1KHz, $V_{is}$ = 5 $V_{pp}$, $V_{DD}$ - $V_{SS} \geq$ 10V, $R_L$ = 10kΩ
- EXTREMELY LOW OFF SWITCH LEAKAGE RESULTING IN VERY LOW OFFSET CURRENT AND HIGH EFFECTIVE OFF RESISTANCE: 100pA TYP. @ $V_{DD}$ - $V_{SS}$ = 18V, $T_{amb}$ = 25°C
- EXTREMELY HIGH CONTROL INPUT IMPEDANCE (control circuit isolated from signal circuit $10^{12}$Ω typ.)
- LOW CROSSTALK BETWEEN SWITCHES : 50dB TYP. @ $f_{is}$ = 0.9MHz, $R_L$ = 1kΩ
- MATCHED CONTROL-INPUT TO SIGNAL-OUTPUT CAPACITANCE : REDUCES OUTPUT SIGNAL TRANSIENTS
- FREQUENCY RESPONSE' SWITCH ON = 40MHz (typ.)
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

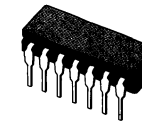
## DESCRIPTION

The **HCC4016B** (extended temperature range) and **HCF4016B** (intermediate temperature range) are monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package and plastic micropackage.

The **HCC/HCF4016B** Series types are quad bilateral switches intended for the transmission or multiplexing of analog or digital signals. Each of the four independent bilateral switches has a single control signal input which simultaneously biases both the p and n device in a given switch ON or OFF.



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

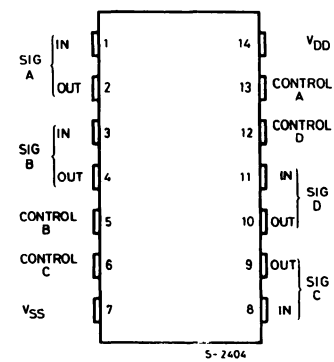
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

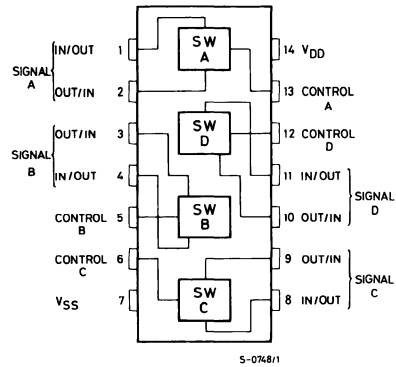
**ORDER CODES :**

| | |
|---|---|
| HCC4016BF | HCF4016BM1 |
| HCF4016BEY | HCF4016BC1 |

**PIN CONNECTIONS**



## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for external periods may affect device reliability.

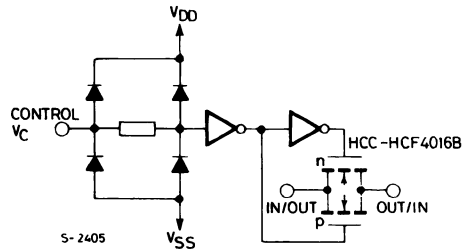
* All voltage values are referred to $V_{SS}$ pin voltage

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## SCHEMATIC DIAGRAM

1 OF 4 IDENTICAL SECTION




## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions | $V_C = V_{DD}$ | $V_{SS}$ (V) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Device Current (all switches on or all switches off) | HCC Types | | | | 5 | | 0.25 | | 0.01 | 0.25 | | 7.5 | μA |
| | | | | | | 10 | | 0.5 | | 0.01 | 0.5 | | 15 | |
| | | | | | | 15 | | 1 | | 0.01 | 1 | | 30 | |
| | | | | | | 20 | | 5 | | 0.02 | 5 | | 150 | |
| | | HCF Types | | | | 5 | | 1 | | 0.01 | 1 | | 7.5 | |
| | | | | | | 10 | | 2 | | 0.01 | 2 | | 15 | |
| | | | | | | 15 | | 4 | | 0.01 | 4 | | 30 | |
| **SWITCH** | | | | | | $V_{IS}$ | | | | | | | | |
| $R_{ON}$ | Resistance | HCC | $R_L$ = 10kΩ• | + 7.5 | − 7.5 | + 7.5 | | 360 | | 200 | 400 | | 600 | Ω |
| | | | | | | − 7.5 | | 360 | | 200 | 400 | | 600 | |
| | | | | | | ± 0.25 | | 775 | | 280 | 850 | | 1230 | |
| | | HCF | | | | + 7.5 | | 370 | | 200 | 400 | | 520 | |
| | | | | | | − 7.5 | | 370 | | 200 | 400 | | 520 | |
| | | | | | | ± 0.25 | | 790 | | 280 | 850 | | 1080 | |
| | | HCC | $R_L$ = 10kΩ• | + 5 | − 5 | + 5 | | 600 | | 250 | 660 | | 960 | |
| | | | | | | − 5 | | 600 | | 250 | 660 | | 960 | |
| | | | | | | ± 0.25 | | 1870 | | 580 | 2000 | | 2600 | |
| | | HCF | | | | + 5 | | 610 | | 250 | 660 | | 840 | |
| | | | | | | − 5 | | 610 | | 250 | 660 | | 840 | |
| | | | | | | ± 0.25 | | 1900 | | 580 | 2000 | | 2380 | |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device
* $T_{High}$ = + 125°C for **HCC** device · + 85°C for **HCF** device.

## STATIC ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | | Test Conditions | $V_C$ = $V_{DD}$ | $V_{SS}$ (V) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **SWITCH** (continued) | | | | | | | | | | | | | | |
| $R_{ON}$ | Resistance | HCC | $R_L$ = 10kΩ• | + 15 | 0 | + 15<br>+ 0.25<br>+ 9.3 | | 360<br>360<br>775 | | 200<br>200<br>300 | 400<br>400<br>850 | | 600<br>600<br>1230 | Ω |
| | | HCF | $R_L$ = 10kΩ• | + 15 | 0 | + 15<br>+ 0.25<br>+ 9.3 | | 370<br>370<br>790 | | 200<br>200<br>300 | 400<br>400<br>800 | | 520<br>520<br>1080 | Ω |
| | | HCC | $R_L$ = 10kΩ• | + 10 | 0 | + 10<br>+ 0.25<br>+ 5.6 | | 600<br>600<br>1870 | | 250<br>250<br>560 | 660<br>660<br>2000 | | 960<br>960<br>2600 | Ω |
| | | HCF | $R_L$ = 10kΩ• | + 10 | 0 | + 10<br>+ 0.25<br>+ 5.6 | | 610<br>610<br>1900 | | 250<br>250<br>560 | 660<br>660<br>2000 | | 840<br>840<br>2380 | Ω |
| ΔON | Resistance ΔRON (between any 2 of 4 switches) | | $R_L$ = 10kΩ• | + 7.5 | − 7.5 | ± 7.5 | | | | 10 | | | | Ω |
| | | | $R_L$ = 10kΩ• | + 5 | − 5 | ± 5 | | | | 15 | | | | Ω |
| Input or Output Leakage Current Switch OFF (effective off resistance) | | HCC | | $V_{DD}$ +18 | $V_C$ = $V_{SS}$ 0 | | | ± 0.1 | | $10^{-5}$ | ± 0.1 | | 1 | μA |
| | | HCF | | $V_{DD}$ + 15 | $V_C$ = $V_{SS}$ 0 | | | ± 0.3 | | $10^{-5}$ | ± 0.3 | | 1 | μA |
| $C_I$ | Input Capacitance | | $V_{CC}$ = $V_{SS}$ = − 5 | | | + 5 | | | | 4 | | | | pF |
| $C_O$ | Output Capacitance | | $V_{CC}$ = $V_{SS}$ = − 5 | | | + 5 | | | | 4 | | | | pF |
| $C_{IO}$ | Feedthrough | | $V_{CC}$ = $V_{SS}$ = − 5 | | | + 5 | | | | 0.2 | | | | pF |
| **CONTROL** ($V_C$) | | | | | | | | | | | | | | |
| $V_{TH}$ | Switch Threshold Voltage | | $I_{IS}$ = 10μA | | | 5 | 1 | | 1 | 2.25 | | 1 | | V |
| | | | $I_{IS}$ = 10μA | | | 10 | 2 | | 2 | 4.5 | | 2 | | V |
| | | | $I_{IS}$ = 10μA | | | 15 | 2 | | 2 | 6.75 | | 2 | | V |
| $I_I$ | Input Current | HCC Types | $V_{IS} \leq V_{DD}$ | | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | $V_{IS} \leq V_{DD}$ | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | μA |
| $C_I$ | Input Capacitance | | | | | | | | | 5 | 7.5 | | | pF |

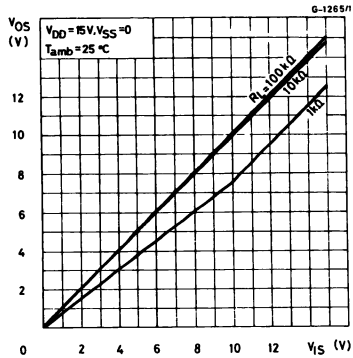
* $T_{Low}$= − 55°C for **HCC** device − 40°C for **HCF** device.
* $T_{High}$= + 125°C for **HCC** device . + 85°C for **HCF** device.

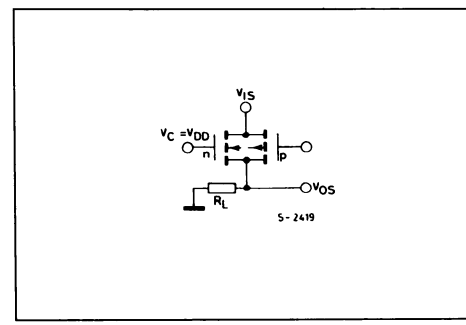
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF all input square wave rise and fall time = 20ns)

| Parameter | Test Conditions | | | | | | | Value | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | $V_C$ (V) | $R_L$ (kΩ) | $f_I$ (KHz) | $V_I$ (V) | $V_{SS}$ (V) | $V_{DD}$ (V) | | Typ. | Max. | |
| **SWITCH** | | | | | | | | | | |
| $t_{pd}$ Propagation Delay Time (signal intput to output) | = $V_{DD}$ | 10 | | 10sq. Wave | GND | 5 | | 40 | 100 | ns |
| | | | | | | 10 | | 20 | 50 | |
| | | | | | | 15 | | 15 | 40 | |
| Crosstalk Between any 2 of 4 Switches (f @ − 50dB) 20 log 10 $\frac{V_{O(B)}}{V_{I(A)}}$ = − 50dB | $V_{C(A)} = V_{DD} = +5$ $V_{C(B)} = V_{SS} = -5$ | 1 | | $V_{I(A)}$ Δ = 5p-p | | | | 0.9 | | MHz |
| Frequency Response Switch "ON" (sine wave input) At 20 log 10 $\frac{V_O}{V_I}$ = − 3dB | = $V_{DD}$ = + 5 | 1 | | 5p-p | − 5 | | | 40 | | MHz |
| Feedtrough (switch OFF) At 20 log 10 $\frac{V_O}{V_I}$ = − 50dB | = $V_{SS}$ = − 5 | 1 | | − 5p-p | | 5 | | 1.25 | | MHz |
| Sine Wave Distortion | = $V_{DD}$ = 5 | 10 | 1 | 5p-p | − 5 | | | 0.4 | | % |
| **CONTROL** ($V_C$) | | | | | | | | | | |
| Propagation Delay : (turn on control to output) | $V_{DD} - V_{SS}$ (sq. wawe) | 1 | | $V_{DD}$ or $V_{SS}$ | | 5 | $V_{DD}-V_{SS}$ = 10V | 35 | 70 | ns |
| | | | | | | 10 | | 20 | 40 | |
| | | | | | | 15 | | 15 | 30 | |
| Max. Allowable Control Input Repetition Rate | 10 (sq. wawe) | 1 | | $V_{DD}$ | GND | 10 | | 10 | | MHz |
| Crosstalk (control input to signal output) | 10 (sq. wave) | 10 | | | GND | 10 | | 50 | | mV |

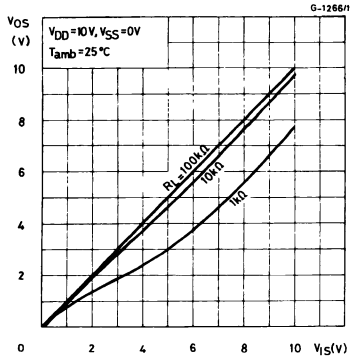
(Δ) Symmetrical about OV

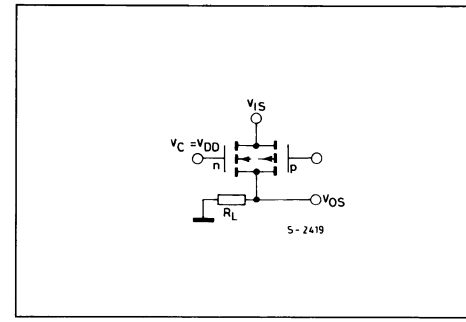
Typical "ON" Characteristics for 1 of 4 switches with $V_{DD}$ = + 15V, $V_{SS}$ = 0V, and Test Circuit.



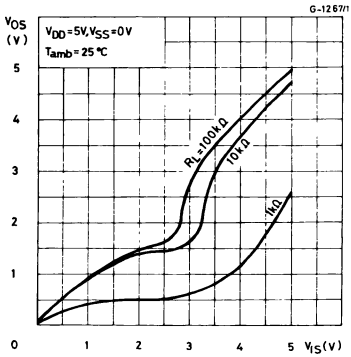



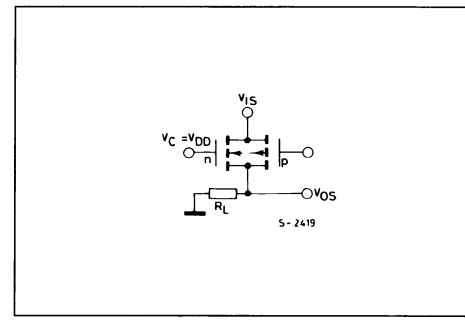
Typical "ON" Characteristics for 1 of 4 switches with $V_{DD}$ = + 10V, $V_{SS}$ = 0V, andTest Circuit.



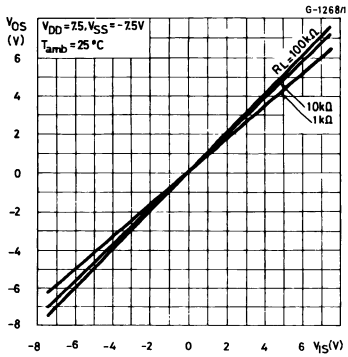



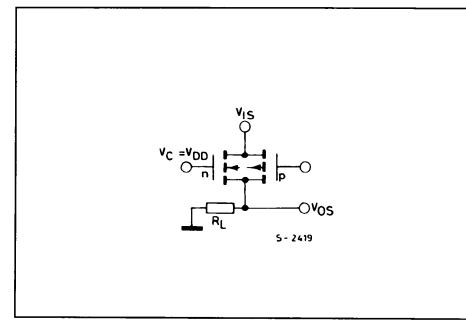

Typical "ON" Characteristics for 1 of 4 switches with $V_{DD}$ = + 5V, $V_{SS}$ = 0V, and Test Circuit.



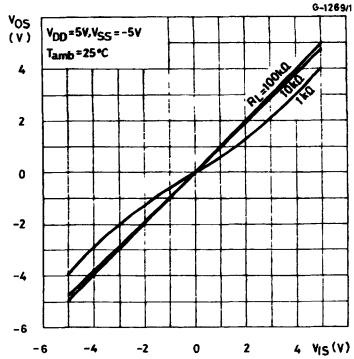



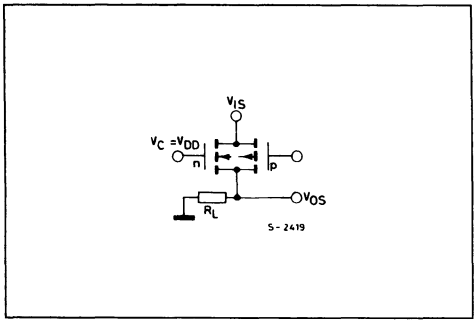

Typical "ON" Characteristics for 1 of 4 switches with $V_{DD}$ = + 7.5V, $V_{SS}$ = – 7.5V, and Test Circuit.



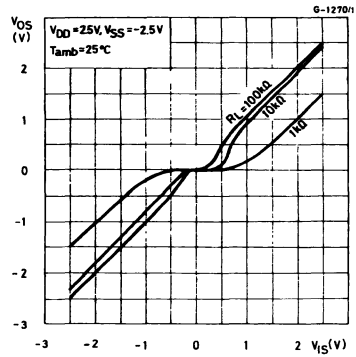



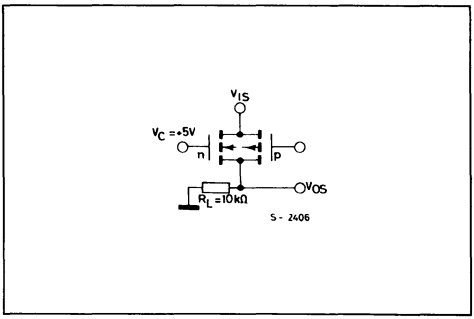
Typical "ON" Characteristics for 1 of 4 switches with $V_{DD}$ = + 5V, $V_{SS}$ = – 5V, and Test Circuit.



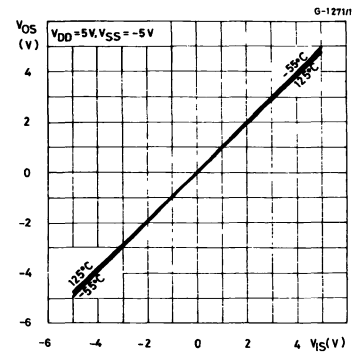



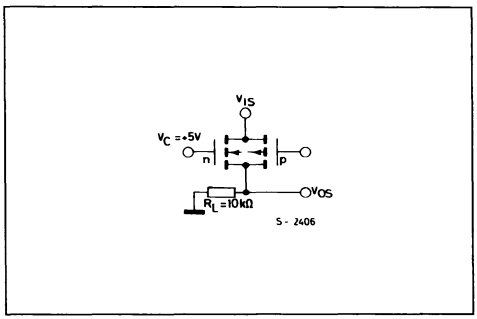

Typical "ON" Characteristics for 1 of 4 switches with $V_{DD}$ = + 2.5V, $V_{SS}$ = – 2.5V, and Test Circuit.



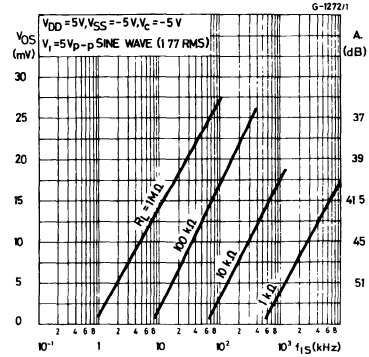



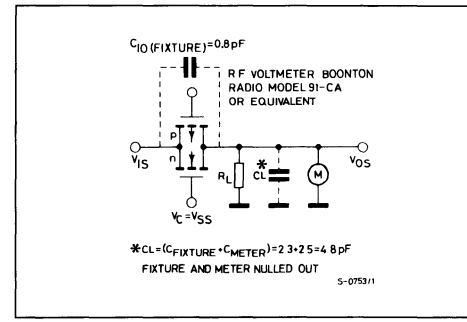

Typical "ON" Characteristics as function of temp.for 1 of 4 switches with $V_{DD}$ = + 5V and Test Circuit.



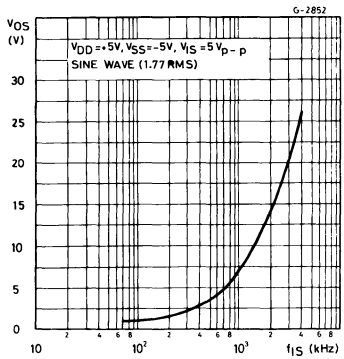



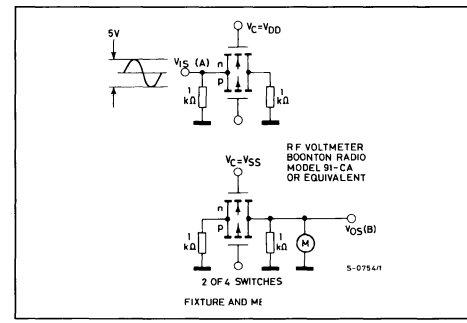
Typical feedthru vs. frequency-switch "OFF" and Test Circuit.



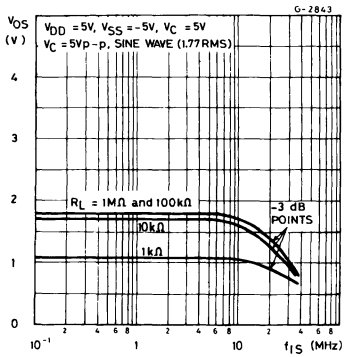



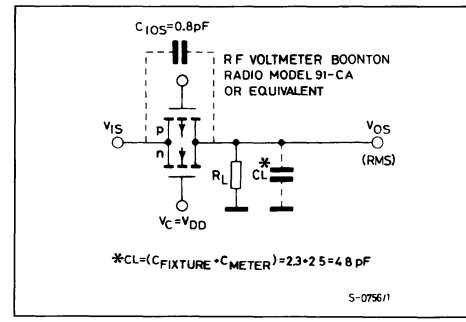

Typical Crosstalk between Switch Circuits in the Same Package.




Typical Switch Frequency response-switch " ON" and Test Circuit.



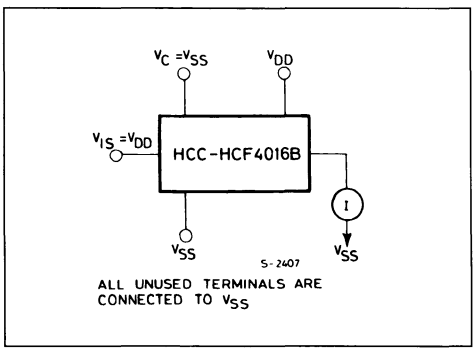
## TYPICAL "ON" RESISTANCE CHARACTERISTICS, $T_{amb}$ = 25°C

| Characteristic* | Supply Conditions | | Load Conditions | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | $R_L$ = 1 kΩ | | $R_L$ = 10 kΩ | | $R_L$ = 100 kΩ | |
| | $V_{DD}$ (V) | $V_{SS}$ (V) | Value (Ω) | $V_{IS}$ (V) | Value (Ω) | $V_{IS}$ (V) | Value (Ω) | $V_{IS}$ (V) |
| $R_{ON}$ | + 15 | 0 | 200 | + 15 | 200 | + 15 | 180 | + 15 |
| | | | 200 | 0 | 200 | 0 | 200 | 0 |
| $R_{ON}$ (max) | + 15 | 0 | 300 | + 11 | 300 | + 9.3 | 320 | + 9.2 |
| $R_{ON}$ | + 10 | 0 | 290 | + 10 | 250 | + 10 | 240 | + 10 |
| | | | 290 | 0 | 250 | 0 | 300 | 0 |
| $R_{ON}$ (max) | + 10 | 0 | 500 | + 7.4 | 560 | + 5.6 | 610 | +5.5 |
| $R_{ON}$ | + 5 | 0 | 860 | + 5 | 470 | + 5 | 450 | + 5 |
| | | | 600 | 0 | 580 | 0 | 800 | 0 |
| $R_{ON}$ (max) | + 5 | 0 | 1.7k | + 4.2 | 7k | + 2.9 | 33k | +2.7 |
| $R_{ON}$ | + 2.5 | − 2.5 | 590 | + 2.5 | 450 | + 2.5 | 490 | + 2.5 |
| | | | 720 | − 2 5 | 520 | − 2.5 | 520 | − 2.5 |
| $R_{ON}$ (max) | + 2.5 | − 2.5 | 232k | ± 0.25 | 300k | ± 0.25 | 870k | ± 0.25 |

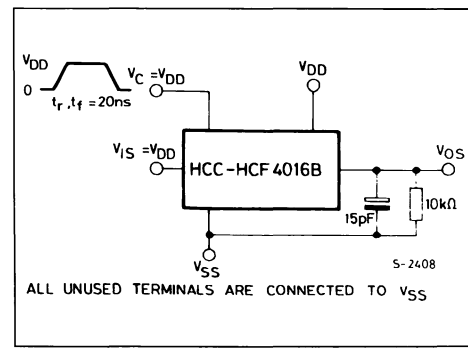
* Variation from a perfect switch, $R_{ON}$= 0Ω.

## TEST CIRCUITS

"OFF" Switch Input or Put Leakage Current.

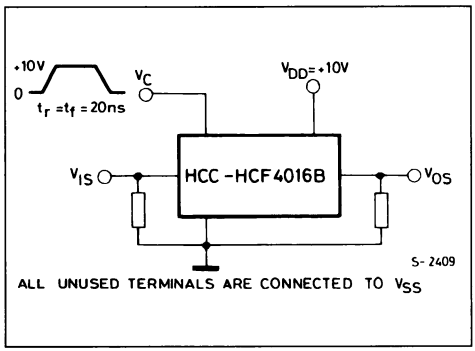



Square-Wave Response.

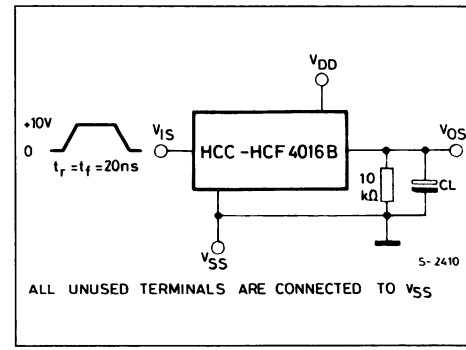


**TEST CIRCUITS** (continued)

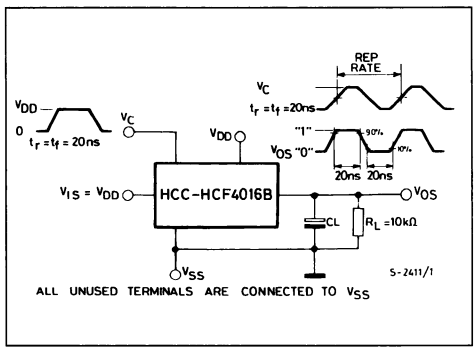
Crosstalk-control Input to Signal Output.



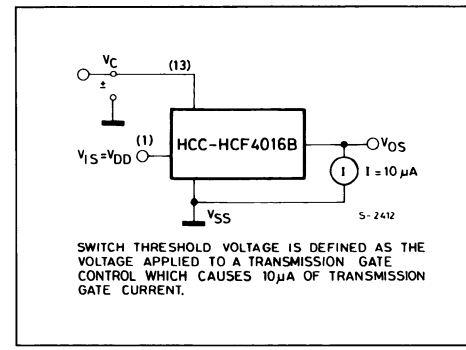

Propagaton Delay Time Signal Input ($V_{IS}$) to Signal Output ($V_{OS}$).



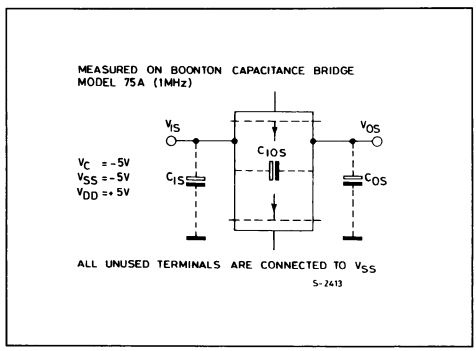

Max Allowable Control-input Repetition Rate.



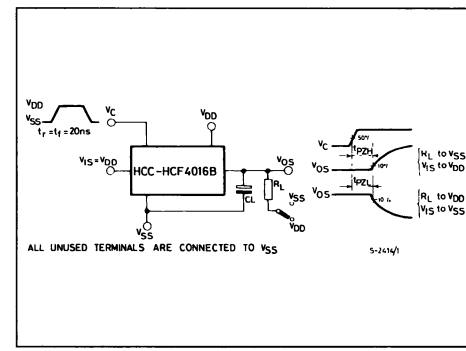

Switch Treshold Voltage.




Capacitance $C_{IOS}$ and $C_{OS}$.




Turn-On Propagation Delay-control Input to Output.



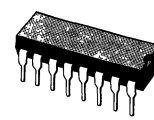
# HCC/HCF4017B
# HCC/HCF4022B

## COUNTERS/DIVIDERS

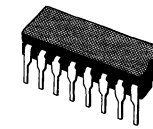
**4017B DECADE COUNTER WITH 10 DECODED OUTPUTS**

**4022B OCTAL COUNTER WITH 8 DECODED OUTPUTS**

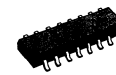
- FULLY STATIC OPERATION
- MEDIUM SPEED OPERATION-12MHz (typ.) AT $V_{DD}$ = 10V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)



**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

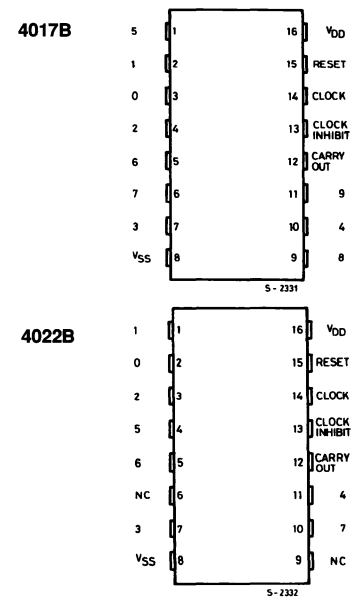
HCC40XXBF HCF40XXBM1
HCF40XXBEY HCF40XXBC1

### DESCRIPTION

The **HCC4017B/4022B** (extended temperature range) and **HCF4017B/4022B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and plastic micro package.

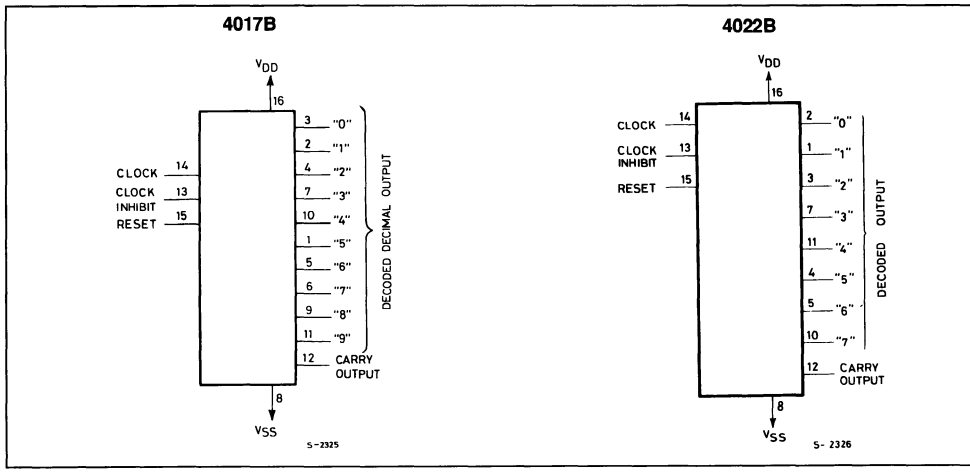
The **HCC/HCF4017B** and **HCC/HCF4022**B are 5-stage and 4-stage Johnson counters having 10 and 8 decoded outputs, respectively. Inputs include a CLOCK, a RESET, and a CLOCK INHIBIT signal. Schmitt trigger action in the CLOCK input circuit provides pulse shaping that allows unlimited clock input pulse rise and fall times. These counters are advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. A high RESET signal clears the counter to its zero count. Use of the Johnson decade-counter configuration permits high-speed operation, 2-input decimal-decode gating, and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A CARRY-OUT signal completes one cycle every

### PIN CONNECTIONS



10 clock input cycles in the **HCC/HCF4017B** or every 8 clock input cycles in the **HCC/HCF4022B** and is used to ripple-clock the succeeding device in a multi-device counting chain.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | – 0.5 to + 20<br>– 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | – 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | – 55 to + 125<br>– 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | – 65 to + 150 | °C |

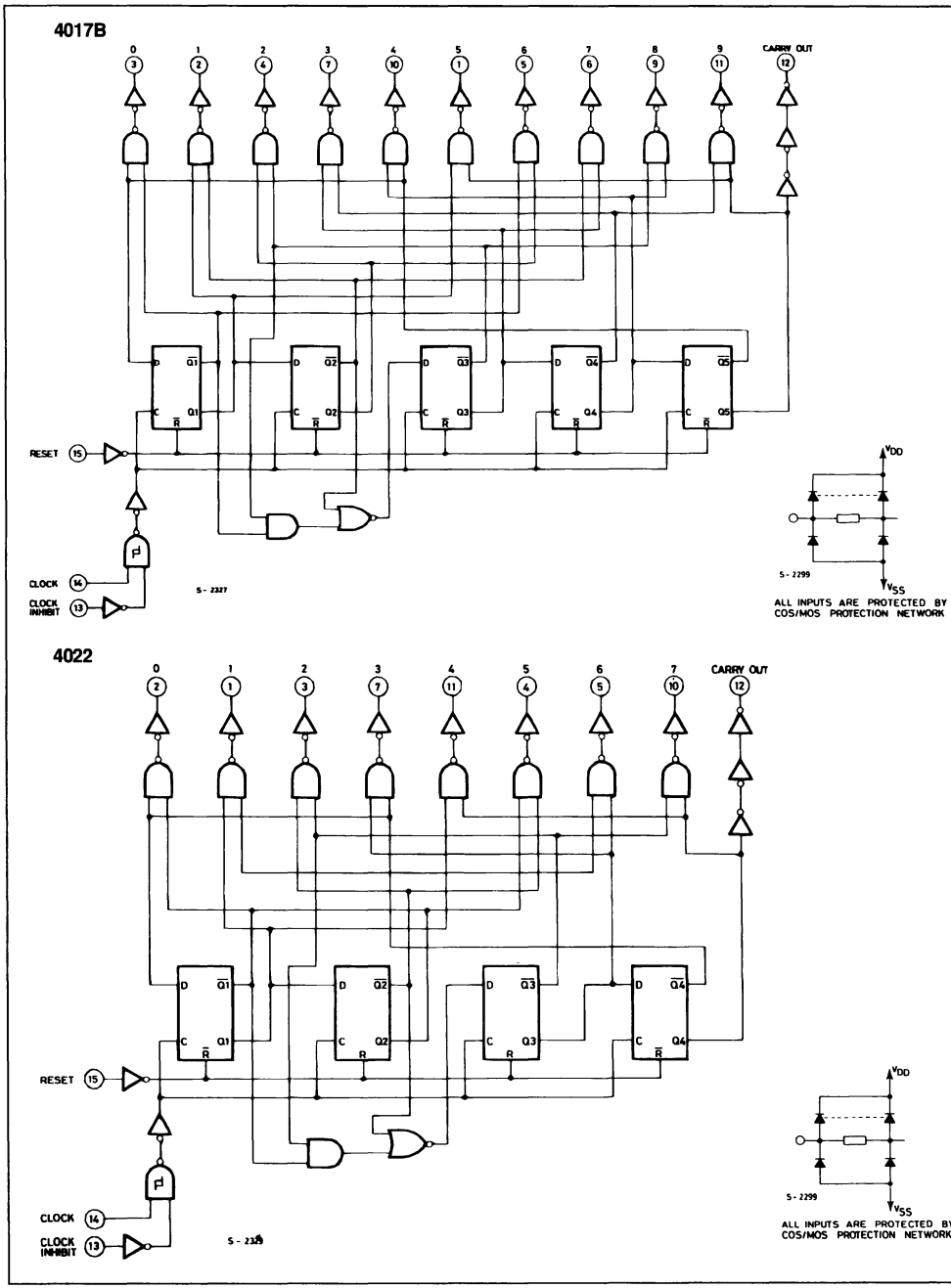
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltages values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

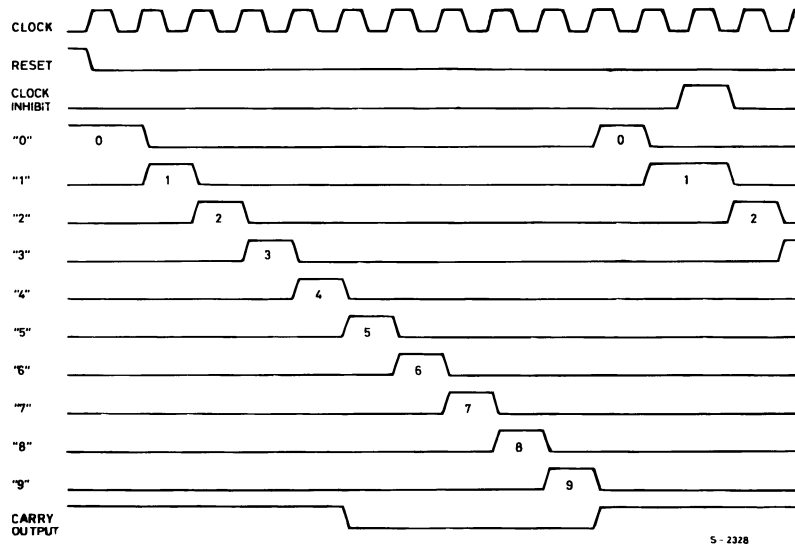
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | – 55 to + 125<br>– 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAMS

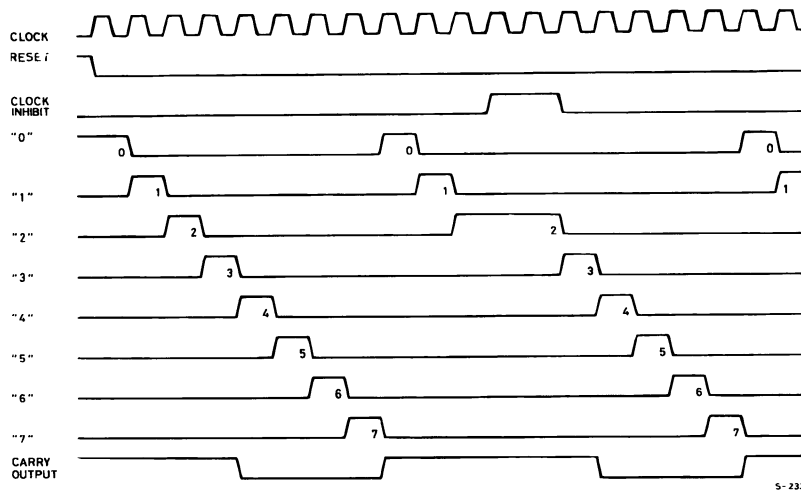


## TIMING DIAGRAMS

### 4017B




### 4022B



**STATIC ELECTRICAL CHARACTERISTICS** (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

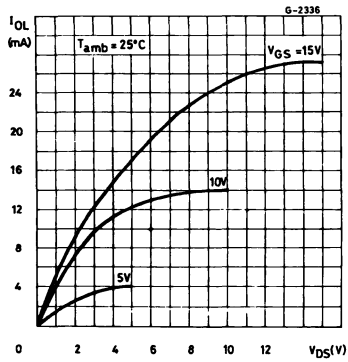
* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min width $V_{DD}$ = 5V, 2V min. width $V_{DD}$ = 10V, 2.5V min. width $V_{DD}$ = 15V.

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ = 0.3%/°C values, all input rise and fall time = 20ns)

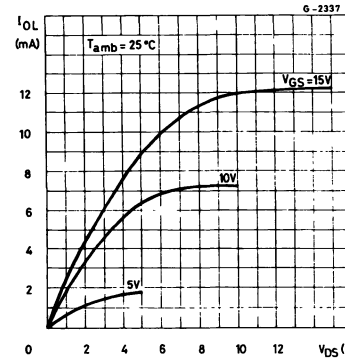
| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| **CLOCKED OPERATION** | | | | | | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time Decode Out | | 5 | | 325 | 650 | ns |
| | | | 10 | | 135 | 270 | |
| | | | 15 | | 85 | 170 | |
| | Carry Out | | 5 | | 300 | 600 | ns |
| | | | 10 | | 125 | 250 | |
| | | | 15 | | 80 | 160 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time Carry Out or Decoded Out Line | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $f_{CL}$* | Maximum Clock Input Frequency | | 5 | 2.5 | 5 | 5 | MHz |
| | | | 10 | 5 | 10 | | |
| | | | 15 | 5.5 | 11 | | |
| $t_W$ | Minimum Clock Pulse Width | | 5 | | 100 | 200 | ns |
| | | | 10 | | 45 | 90 | |
| | | | 15 | | 30 | 60 | |
| $t_r$, $t_f$ | Clock Input Rise or Fall Time | | 5 | Unlimited | | | µs |
| | | | 10 | | | | |
| | | | 15 | | | | |
| $t_{setup}$ | Data Setup Time Minimum Clock Inhibit | | 5 | | 115 | 230 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 35 | 7.5 | |
| **RESET OPERATION** | | | | | | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time Carry Out or Decode Out Lines | | 5 | | 265 | 530 | ns |
| | | | 10 | | 115 | 230 | |
| | | | 15 | | 85 | 170 | |
| $t_W$ | Minimum Reset Pulse Width | | 5 | | 130 | 260 | ns |
| | | | 10 | | 55 | 110 | |
| | | | 15 | | 30 | 60 | |
| $t_{rem}$ | Minimum Reset Removal Time | | 5 | | 200 | 400 | ns |
| | | | 10 | | 140 | 280 | |
| | | | 15 | | 75 | 150 | |

* Measured with respect to carry output line.

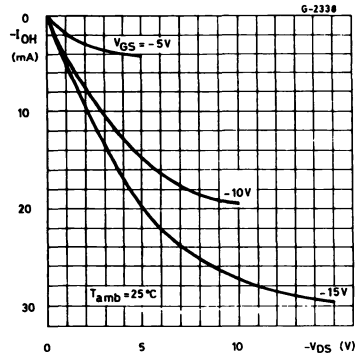
Typical Output Low (sink) Current Characteristics.



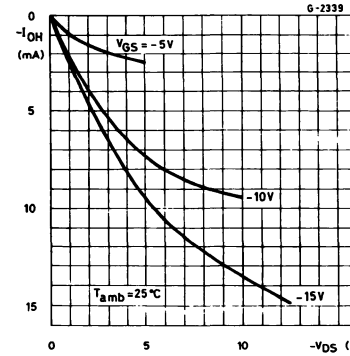

Minimum Output Low (sink) Current Characteristics.




Typical Output High (source) Current Characteristics.

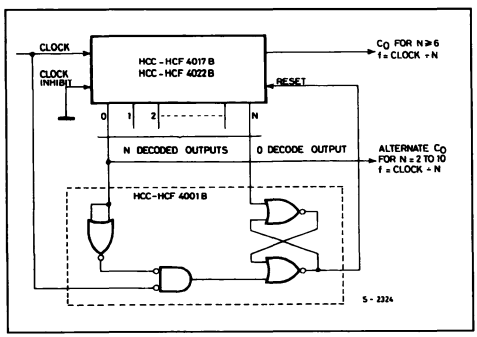



Minimum Output High (source ) Current Characteristics.




## TYPICAL APPLICATIONS

Divide by N Counter (N ≤ 10) with N Decoded Outputs.

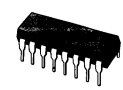



When the $N^{th}$ decoded output is reached ($N^{th}$ clock pulse) the S-R flip-flop (constructed from two NOR gates of the **HCC/HCF4001B**) generates a reset pulse which clears the **HCC/HCF4017B** to its zero count. At this time, if the $N^{th}$ decoded output is greater than or equal to 6, the $C_{OUT}$ line goes high to clock the next **HCC/HCF4017B** counter section. The "0" decoded output also goes high at this time. Coincidence of the clock low and decoded "0" output high resets the S-R flip flop to enable the **HCC/HCF4017B**. If the $N^{th}$ decoded output is less than 6, the $C_{OUT}$ line will not go high and, therefore, cannot be used. In this case "0" decoded output may be used to perform the clocking function for the next counter.

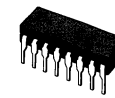
# HCC/HCF4018B

## PRESETTABLE DIVIDE-BY-N COUNTER

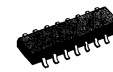
- MEDIUM SPEED OPERATION - 10MHz (typ.) AT $V_{DD} - V_{SS} = 10V$
- FULLY STATIC OPERATION
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)



**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4018BF HCF4018BM1
HCF4018BEY HCF4018BC1

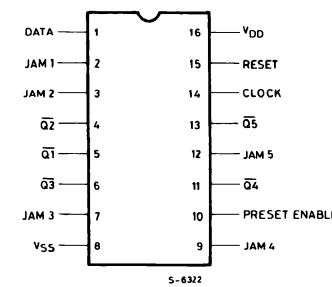
### DESCRIPTION

**The HCC4018B** (extended temperature range) and **HCF4018B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and plastic micropackage.

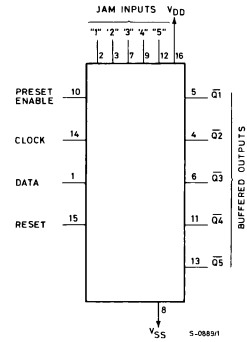
The **HCC/HCF4018B** types consist of 5 Johnson-Counter stages, buffered Q outputs from each stage, and counter preset control gating. CLOCK, RESET, DATA, PRESET ENABLE, and 5 individual JAM inputs are provided. Divide by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the Q5, Q4, Q3, Q2, Q1 signals, respectively, back to the DATA input.

Divide-by-9, 7, 5, or 3 counter configurations can be implemented by the use of a **HCC/HCF4011B** gate package to properly gate the feedback connection to the DATA input. Divide-by-functions greater than 10 can be achieved by use of multiple **HCC/HCF 4018B** units. The counter is advanced one count at the positive clock-signal transition. Schmitt Trigger action on the clock line permits unlimited clock rise and fall times. A high RESET signal clears the counter to an all-zero condition. A high PRESENT-ENABLE signal allows information on the JAM inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

### PIN CONNECTIONS



## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0 5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0 5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

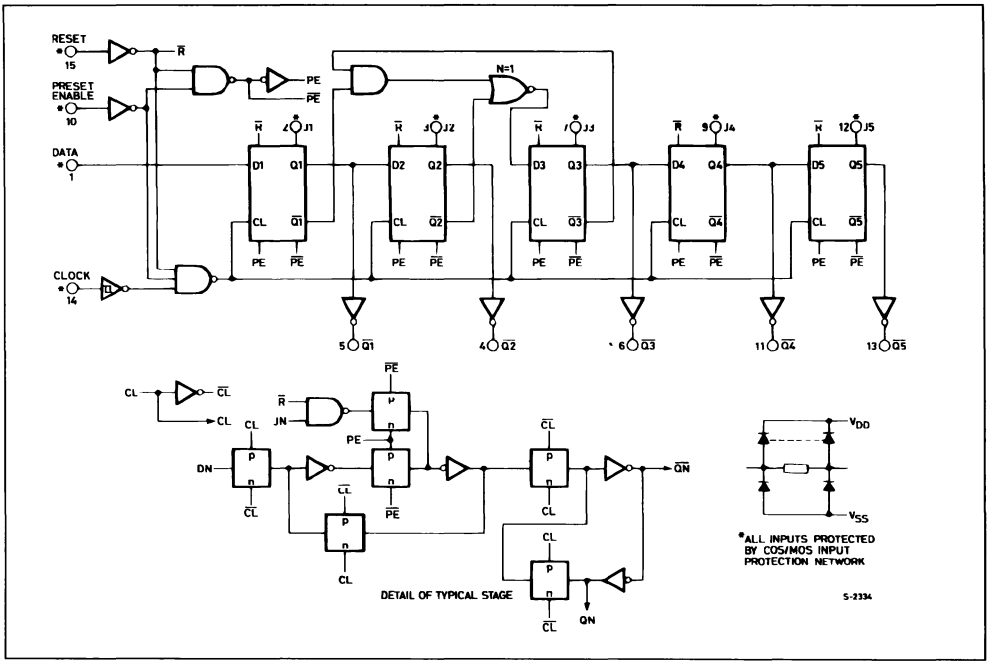
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are refered to $V_{SS}$ pin voltage

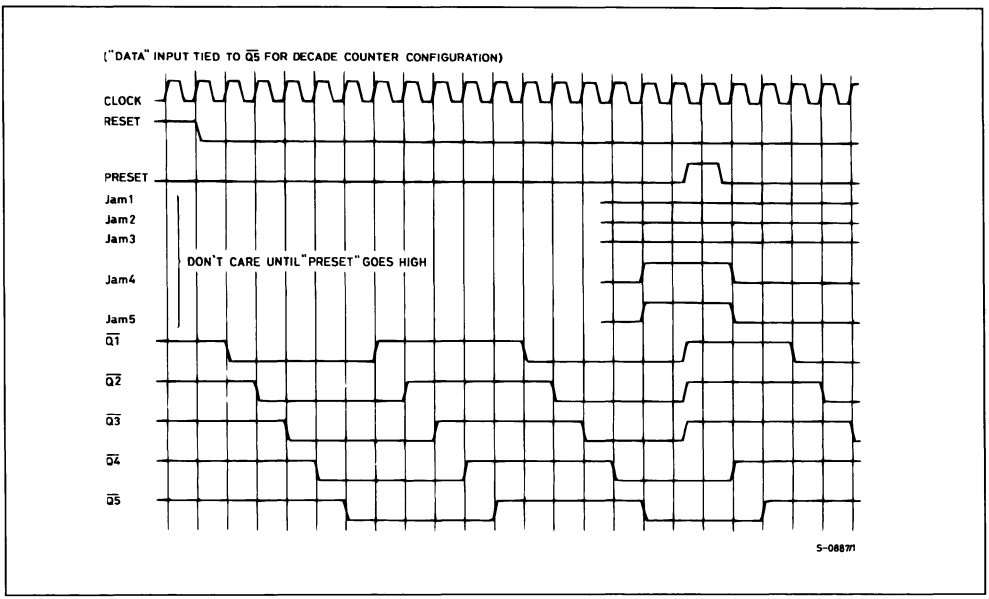
## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAM




## TIMING DIAGRAM



## STATIC ELECTRICAL CHARACTERISTICS (under recommended operating conditions)

| Symbol | Parameter | | Test Conditions | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | |
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

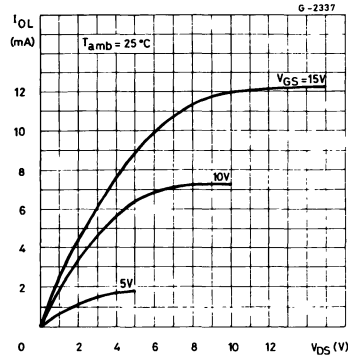
* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device
* $T_{High}$ = +125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2.5 V min. with $V_{DD}$ = 15V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall times = 20ns)

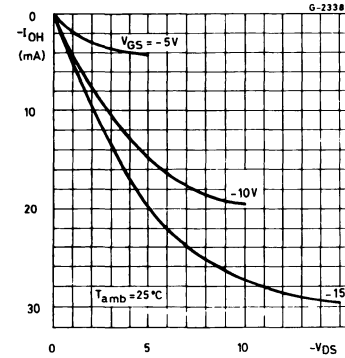
| Symbol | Parameter | Test Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time | 5 | | 200 | 400 | ns |
| | | 10 | | 90 | 180 | |
| | | 15 | | 65 | 130 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | 5 | | 100 | 200 | ns |
| | | 10 | | 50 | 100 | |
| | | 15 | | 40 | 80 | |
| $f_{CL}$ | Maximum Clock Input Frequency | 5 | 3 | 6 | | MHz |
| | | 10 | 7 | 14 | | |
| | | 15 | 8.5 | 17 | | |
| $t_W$ | Clock Input Width | 5 | 160 | 80 | | ns |
| | | 10 | 70 | 35 | | |
| | | 15 | 50 | 25 | | |
| $t_r$, $t_f$ | Clock Input Rise or Fall Time | 5 | Unlimited | | | µs |
| | | 10 | | | | |
| | | 15 | | | | |
| $t_{setup}$ | Data Input Set-up Time | 5 | 40 | 20 | | ns |
| | | 10 | 12 | 6 | | |
| | | 15 | 6 | 3 | | |
| $t_H$ | Data Input Hold-time | 5 | 140 | 70 | | ns |
| | | 10 | 80 | 40 | | |
| | | 15 | 60 | 30 | | |
| **PRESET* OR RESET OPERATION** | | | | | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time (reset or reset to Q) | 5 | | 275 | 550 | ns |
| | | 10 | | 125 | 250 | |
| | | 15 | | 90 | 180 | |
| $t_W$ | Preset or Reset Pulse Width | 5 | 160 | 80 | | ns |
| | | 10 | 70 | 35 | | |
| | | 15 | 50 | 25 | | |
| $t_{rem}$ | Preset or Reset Removal Time | 5 | 80 | 40 | | ns |
| | | 10 | 30 | 15 | | |
| | | 15 | 20 | 10 | | |

* At PRESET ENABLE OR JAM inputs

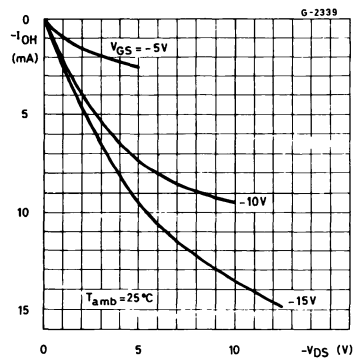
Typical Output Low (sink) Current Characteristics.



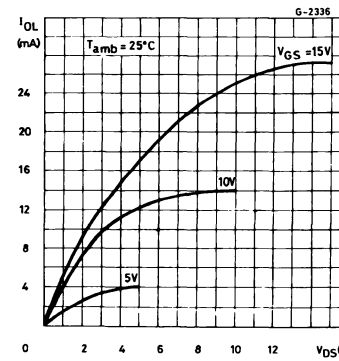

Typical Output high (source) Current Characteristics.




Minimum Output High (source) Current Characteristics.




typical Output low (sink) Current Characteristics.



## TYPICAL APPLICATIONS

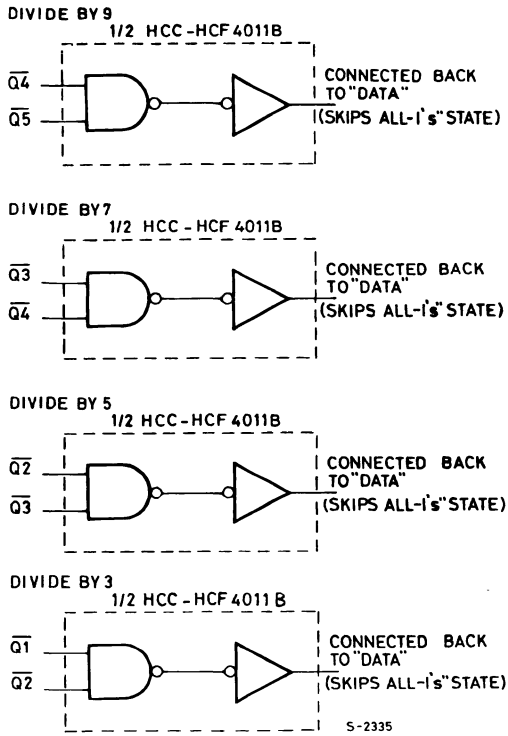
External connections for divide by 10, 9, 8, 7, 6, 5, 4, 3, 2 operation.

DIVIDE BY 10 $\overline{Q}_5$
DIVIDE BY 8 $\overline{Q}_4$
DIVIDE BY 6 $\overline{Q}_3$
DIVIDE BY 4 $\overline{Q}_2$
DIVIDE BY 2 $\overline{Q}_1$

CONNECTED BACK TO "DATA"

NO CONNECTED

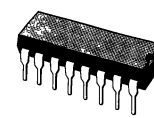
NO EXTERNAL COMPONENTS REQUIRED



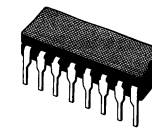
# HCC/HCF4019B

## QUAD AND/OR SELECT GATE

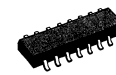
- MEDIUM SPEED OPERATION : $t_{PHL} = t_{PLH}$ = 60ns (typ.) AT $C_L$ = 50pF, $V_{DD}$ = 10V
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)



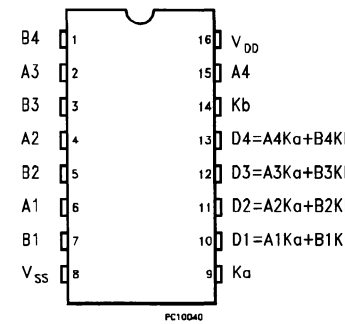
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4019BF HCF4019BM1
HCF4019BEY HCF4019BC1

**PIN CONNECTIONS**




### DESCRIPTION

The **HCC4019B** (extended temperature range) and **HCF4019B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and plastic micro package.

The **HCC/HCF4019B** types are comprised of four AND/OR select gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits $K_a$ and $K_b$. In addition to selection of either channel A or channel B information, the control bits can be applied simultaneously to accomplish the logical A+B function.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | – 0.5 to + 20<br>– 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | – 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | – 55 to + 125<br>– 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | – 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability

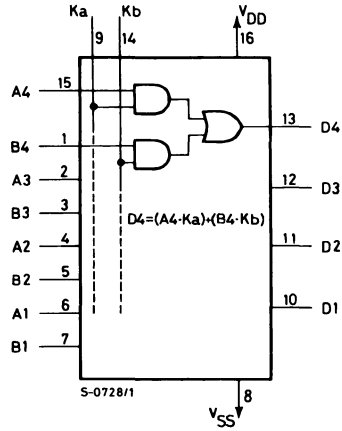
* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | – 55 to + 125<br>– 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAMS

**4019B**




## TRUTH TABLE

| Ka | Kb | An | Bn | DN |
|---|---|---|---|---|
| 1 | X | 1 | X | 1 |
| 1 | X | 0 | X | 0 |
| X | 1 | X | 1 | 1 |
| X | 1 | X | 0 | 0 |
| 0 | 0 | X | X | 0 |

X = Don't care

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

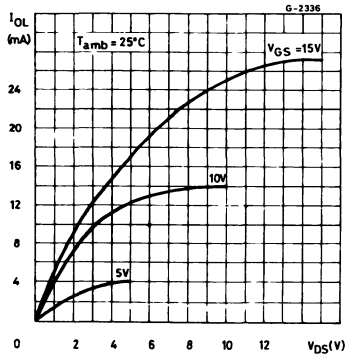
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 1 | | 0.02 | 1 | | 30 | μA |
| | | | 0/10 | | | 10 | | 2 | | 0.02 | 2 | | 60 | |
| | | | 0/15 | | | 15 | | 4 | | 0.02 | 4 | | 120 | |
| | | | 0/20 | | | 20 | | 20 | | 0.04 | 20 | | 600 | |
| | | HCF Types | 0/ 5 | | | 5 | | 4 | | 0.02 | 4 | | 30 | |
| | | | 0/10 | | | 10 | | 8 | | 0.02 | 8 | | 60 | |
| | | | 0/15 | | | 15 | | 16 | | 0 02 | 16 | | 120 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0 05 | | | 0.05 | | 0 05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3 5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1 5 | | 1 5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1 6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0 64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13 5 | | 15 | − 4 2 | | − 3.4 | − 6 8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1 36 | − 3 2 | | − 1 1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0 9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2 4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1 6 | | 1 3 | 2.6 | | 0 9 | | |
| | | | 0/15 | 1.5 | | 15 | 4 2 | | 3.4 | 6 8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1 1 | 2.6 | | 0 9 | | |
| | | | 0/15 | 1.5 | | 15 | 3 6 | | 3.0 | 6.8 | | 2 4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0 1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | All A and B Inputs | | | | | | | | 5 | 7 5 | | | pF |
| | | Ka and Kb Inputs | | | | | | | | 10 | 15 | | | pF |

* $T_{Low}$= − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$= + 125°C for **HCC** device + 85°C for **HCF** device
The Noise Margin for both "1" and "0" level is : 1V min with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2.5 V min with $V_{DD}$ = 15V

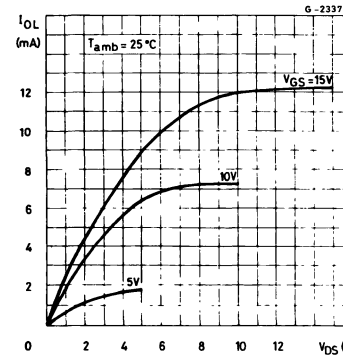
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3 %/°C, all input rise and fall times = 20 ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time | | 5 | | 150 | 300 | ns |
| | | | 10 | | 60 | 120 | |
| | | | 15 | | 50 | 100 | |
| $t_{TLH}$, $t_{THL}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

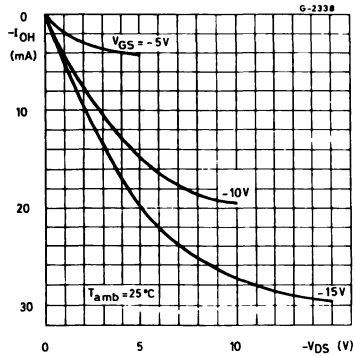
Typical Output Low (sink) Current Characteristics.



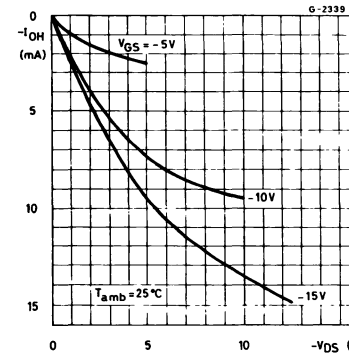

Minimum Output Low (sink) Current Characteristics.




Typical Output High (source) Current Characteristics.

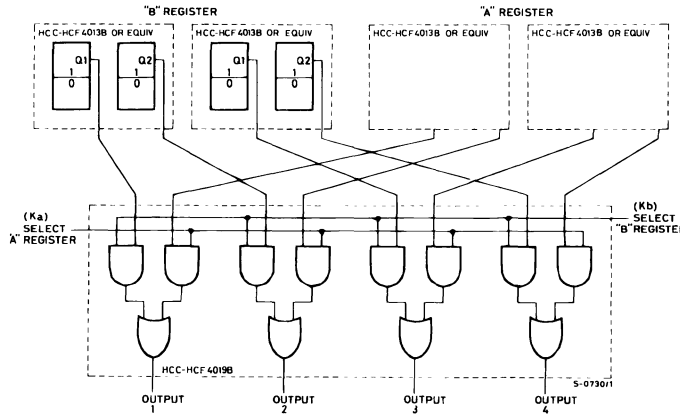



Minimum Output High (source) Current Characteristics.

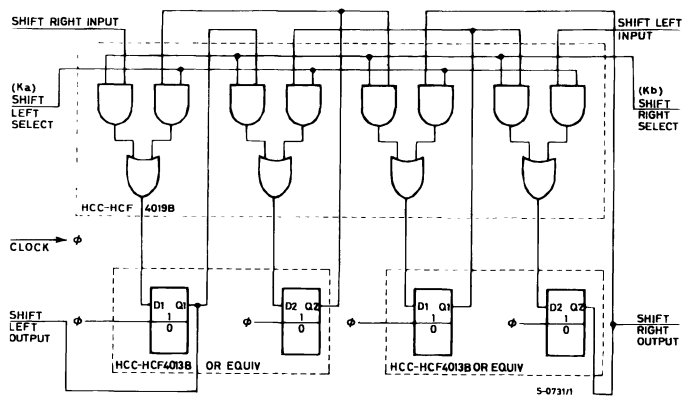


## TYPICAL APPLICATIONS

AND-OR SELECTED GATING.

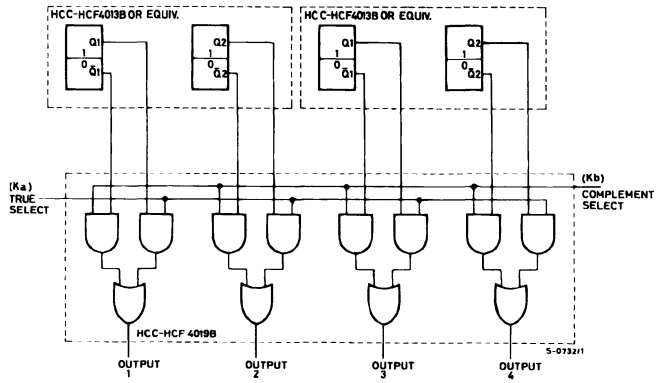



SHIFT LEFT SHIFT RIGHT REGISTER.

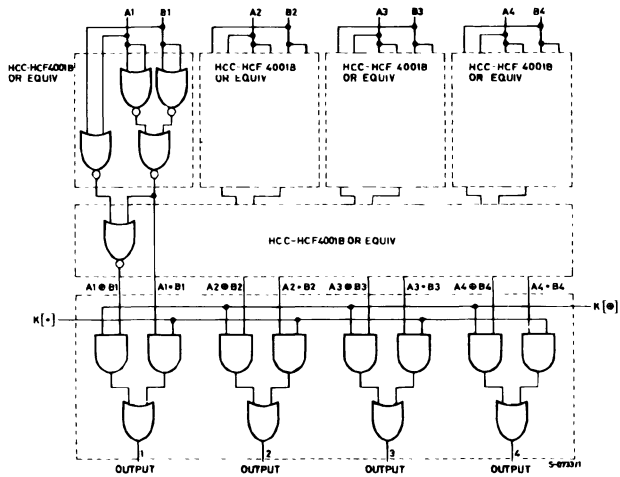


**TYPICAL APPLICATIONS** (continued)

TRUE COMPLEMENT SELECTOR.




AND-OR EXCLUSIVE-OR SELECTOR.

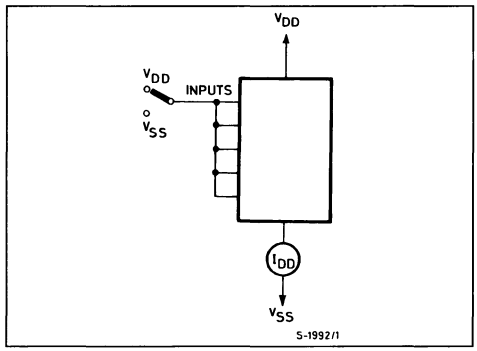



**TRUTH TABLE**

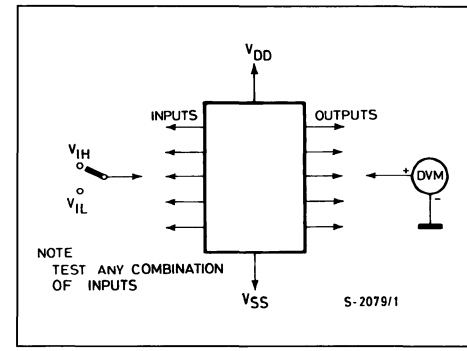
| K [•] | K [⊕] | OUT |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | A – B |
| 0 | 1 | A ⊕ B |
| 1 | 1 | A + B |

## TEST CIRCUITS

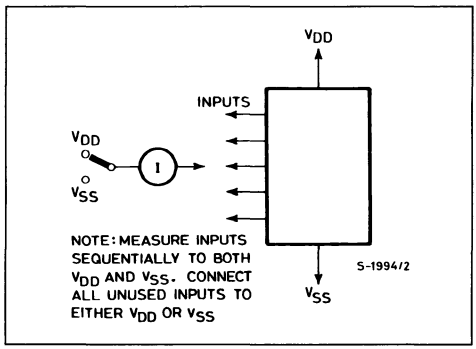
Quiescent Device Current.



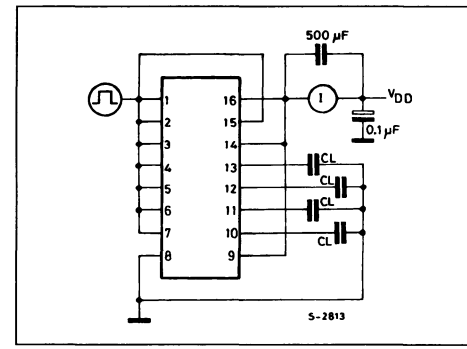

Input Voltage.




Input Leakage Current.




Dynamic Power Dissipation.

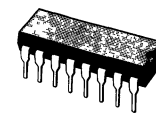


# HCC4020B/24B/40B
# HCF4020B/24B/40B

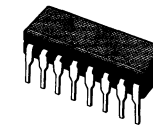
## RIPPLE-CARRY BINARY COUNTER/DIVIDERS

**4020B - 14 STAGE**
**4024B - 7 STAGE**
**4040B - 12 STAGE**

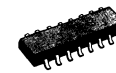
- MEDIUM-SPEED OPERATION
- FULLY STATIC OPERATION
- COMMON RESET
- BUFFERED INPUTS AND OUTPUTS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT
- CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Package)



**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

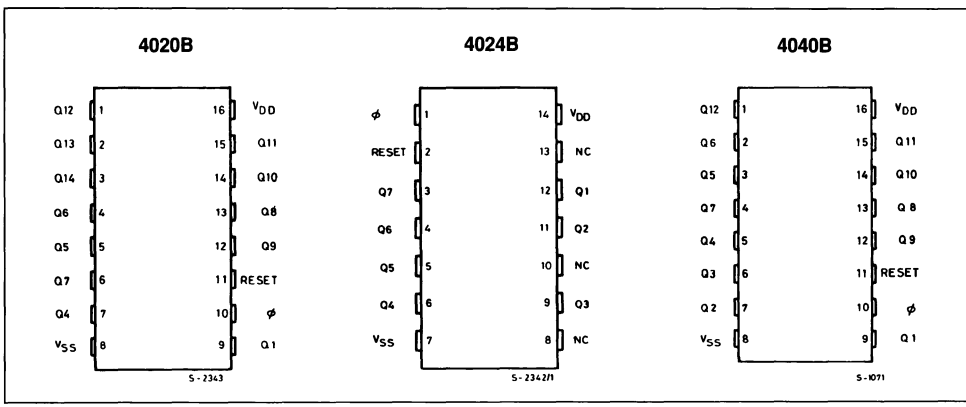
HCC40XXBF HCF40XXBM1
HCF40XXBEY HCF40XXBC1

### DESCRIPTION

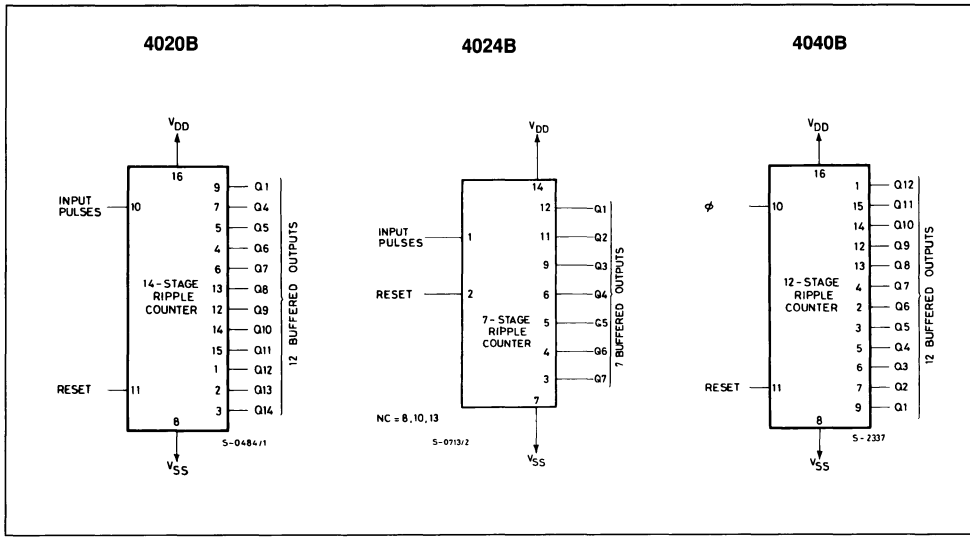
The **HCC4XXXB** (extended temperature range) and **HCF4XXXB** (intermediate temperature range) are monolithic integrated circuits, available in 14-lead dual in-line for **4024B** and 16-lead dual in-line for **4020B, 4040B** plastic or ceramic package and plastic micropackage.

The **HCC/HCF4020B, 4024B**, and **4040B** are ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of a counter advances one count on the negative transition of each input pulse ; a high level on the RESET line resets the counter to its all zeros stage. Schmitt trigger action on the input-pulse line permits unlimited clock rise and fall times. All inputs and outputs are buffered.

### PIN CONNECTIONS



## FUNCTIONAL DIAGRAMS




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability

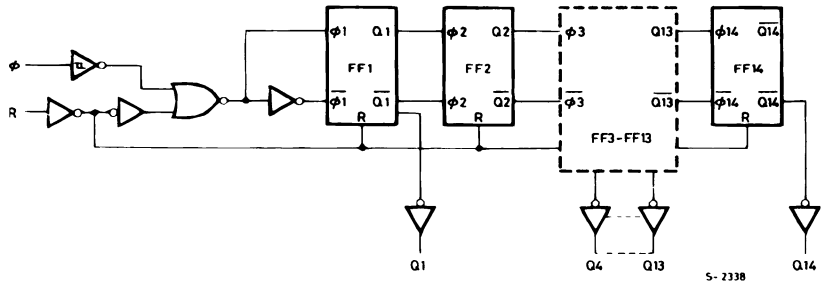
* All voltage values are refered to $V_{SS}$ pin voltage

## RECOMMENDED OPERATING CONDITIONS

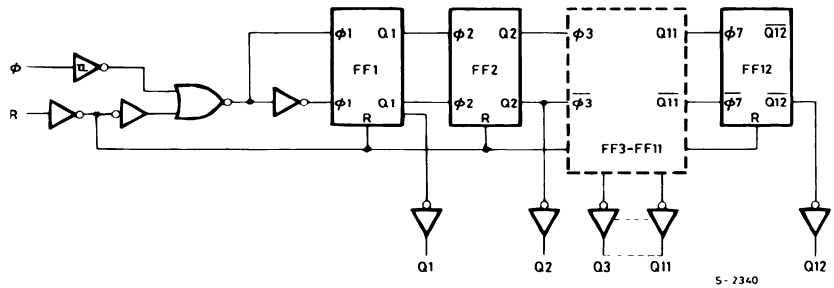
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAMS

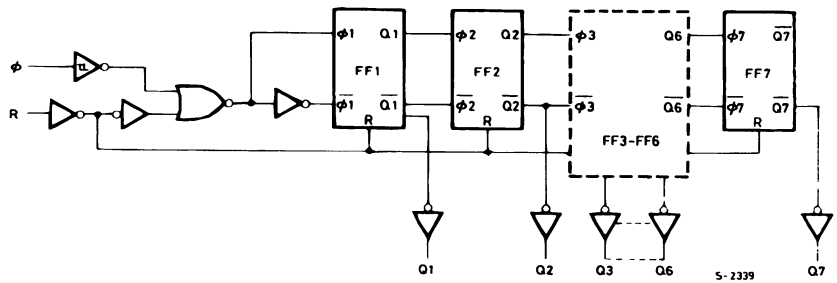
### 4020B

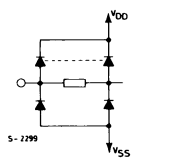



### 4040B




### 4024B




ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

**STATIC ELECTRICAL CHARACTERISTICS** (over recommended operating conditions)

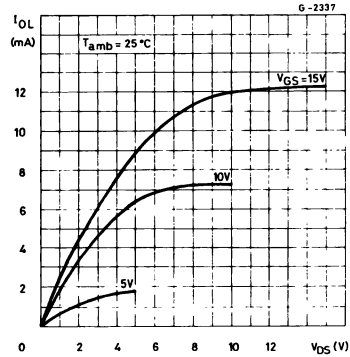
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$= − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$= + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5 V min. with $V_{DD}$ = 15V.

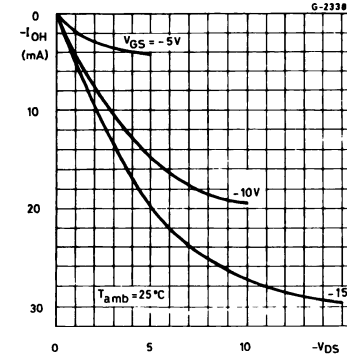
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ = 0.3%/°C values, all input rise and fall time = 20ns).

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| **INPUT-PULSE OPERATION** | | | | | | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time (Ø to Q1 Out) | | 5 | | 180 | 360 | ns |
| | | | 10 | | 80 | 160 | |
| | | | 15 | | 65 | 130 | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time Qn to $Q_{n+1}$ | | 5 | | 100 | 200 | ns |
| | | | 10 | | 40 | 80 | |
| | | | 15 | | 30 | 60 | |
| $t_{TLH}$, $t_{THL}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_W$ | Minimum Input Pulse Width | | 5 | | 70 | 140 | ns |
| | | | 10 | | 30 | 60 | |
| | | | 15 | | 20 | 40 | |
| $t_r$, $t_f$ | Input Pulse Rise and Fall Time | | 5 | Unlimited | | | µs |
| | | | 10 | | | | |
| | | | 15 | | | | |
| $f_{max}$ | Maximum Clock Input Frequency | | 5 | 3.5 | 7 | | MHz |
| | | | 10 | 8 | 16 | | |
| | | | 15 | 12 | 24 | | |
| **RESET OPERATION** | | | | | | | |
| $t_{PHL}$ | Propagation Delay Time | | 5 | | 140 | 280 | ns |
| | | | 10 | | 60 | 120 | |
| | | | 15 | | 50 | 100 | |
| $t_W$ | Minimum Reset Pulse Width | | 5 | | 100 | 200 | ns |
| | | | 10 | | 40 | 80 | |
| | | | 15 | | 30 | 60 | |
| $t_{rem}$ | Reset Removal Time | | 5 | | 175 | 350 | ns |
| | | | 10 | | 75 | 150 | |
| | | | 15 | | 50 | 100 | |

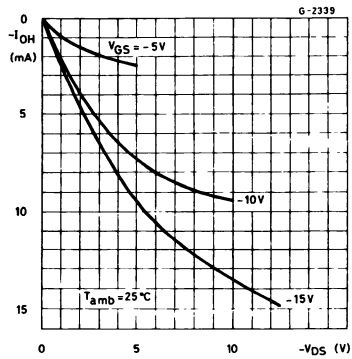
Minimum Output Low (sink) Current Characteristics.



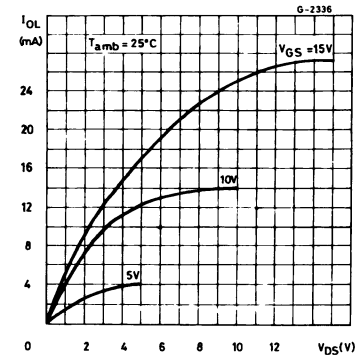

Typical Output Low (source) Current Characteristics.



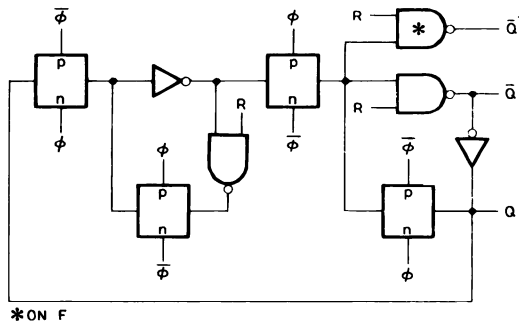

Minimum Output High (source) Current Characteristics.




Typical Output High (sink) Current Characteristics.




Details of Typical Flip-flop Stage.



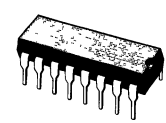
SGS-THOMSON MICROELECTRONICS

# HCC/HCF4026B
# HCC/HCF4033B

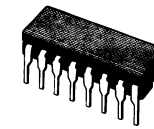
## DECADE COUNTERS/DIVIDERS WITH DECODED 7-SEGMENT DISPLAY OUTPUTS

**WITH; DISPLAY ENABLE 4026B**
**RIPPLE BLANKING 4033B**

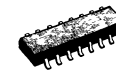
- COUNTER AND 7-SEGMENT DECODING IN ONE PACKAGE
- EASILY INTERFACED WITH 7-SEGMENT DISPLAY TYPES
- FULLY STATIC COUNTER OPERATION : DC TO 6MHz (typ.) AT $V_{DD}$ = 10V
- IDEAL FOR LOW-POWER DISPLAYS
- DISPLAY ENABLE OUTPUT - 4026B
- "RIPPLE BLANKING" AND LAMP TEST - 4033B
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATING
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)



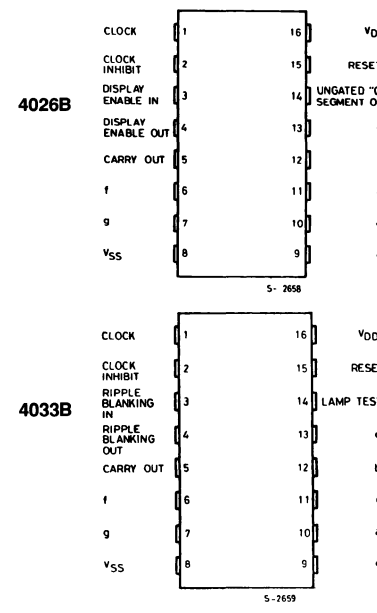
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC40XXBF HCF40XXBM1
HCF40XXBEY HCF40XXBC1

**PIN CONNECTIONS**




### DESCRIPTION

The **HCC4026B/4033B** (extended temperature range) and **HCF4026B/4033B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF4026B** and **HCC/HCF4033B** each consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output for driving one stage in a numerical display. These devices are particularly advantageous in display applications where low power dissipation and/or low package count are important. Inputs common to both types are CLOCK, RESET, & CLOCK INHIBIT ; common outputs are CARRY OUT and the seven decoded outputs (a, b, c, d, e, f, g). Additional inputs and outputs for the **HCC/HCF4026B** include DISPLAY ENABLE input and DISPLAY ENABLE and UNGATED "C-SEGMENT" outputs. Signals peculiar to the **HCC/HCF4033B** are RIPPLE-BLANKING INPUT AND LAMP TEST INPUT and a RIPPLE-BLANKING OUTPUT. A high RESET signal clears the

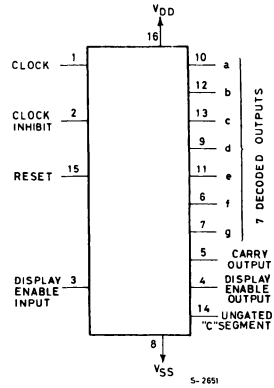
decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. Antilock gating is provided on the JOHNSON counter, thus assuring proper counting sequence. The CARRY-OUT ($C_{out}$) signal completes one cycle every ten CLOCK INPUT cycles and is used to clock the succeeding decade directly in a multi-decade counting chain. The seven decoded outputs (a, b, c, d, e, f, g) illuminate the proper segments in a seven segment display device used for representing the decimal numbers 0 to 9. The 7-segment outputs go high on selection in the **HCC/HCF4033B** ; in the **HCC/HCF4026B** these outputs go high only when the DISPLAY ENABLE IN is high.

**HCC/HCF4026B** - When the DISPLAY ENABLE IN is low the seven decoded outputs are forced low regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing. The CARRY OUT and UNGATED "C-SEGMENT" signals are not gated by the DISPLAY ENABLE and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

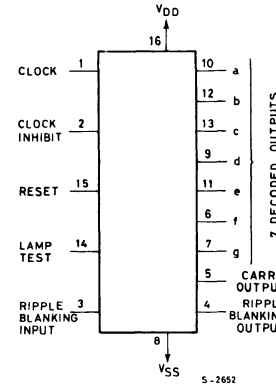
**HCC/HCF4033B** - The **HCC/HCF4033B** has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.07000 in an eight digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI terminal of the **HCC/HCF4033B** associated with the most significant digit in the display to a low-level voltage and connecting the RBO terminal of that stage to the RBI terminal of the **HCC/HCF4033B** in the next-lower significant position in the display. This procedure is continued for each succeeding **HCC/HCF4033B** on the integer side of the display. On the fraction side of the display the RBI of the **HCC/HCF4033B** associated with the least significant bit is connected to a low-level voltage and the RBO of that **HCC/HCF4033B** is connected to the RBI terminal of the **HCC/HCF4033B** in the next more-significant-bit position. Again, this procedure is continued for all **HCC/HCF4033B's** on the fraction side of the display. In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a high level voltage (instead of to the RBO of the next more-significant-stage). For example : optional zero → 0.7346. Likewise, the zero in a number such as 763.0 can be displayed by connecting the RBI of the **HCC/HCF4033B** associated with it to a high-level voltage. Ripple blanking of non-significant zeros provides an appreciable savings in display power. The **HCC/HCF4033B** has a LAMP TEST input which, when connected to a high-level voltage, overrides normal decoder operation and enables a check to be made on possible display malfunctions by putting the seven outputs in the high state.

## FUNCTIONAL DIAGRAMS

**4026B**




**4033B**




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storasge Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

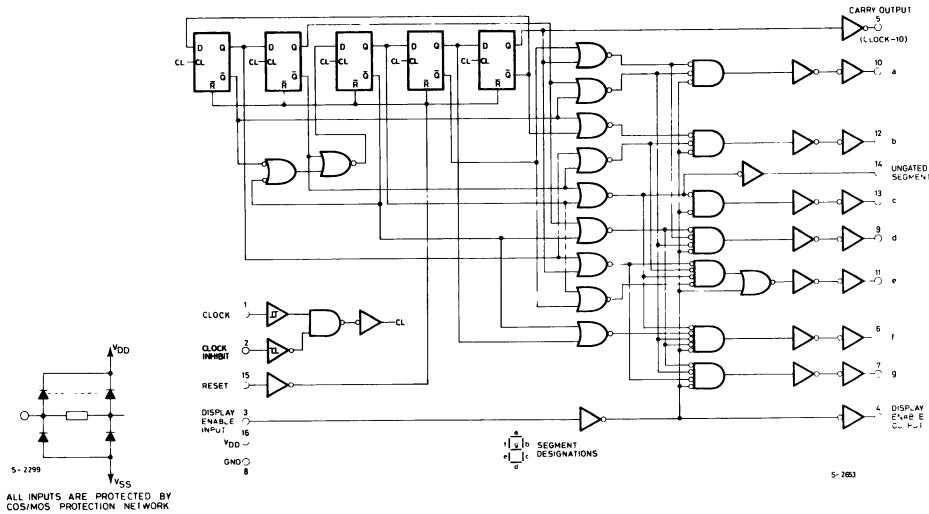
* All voltages values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

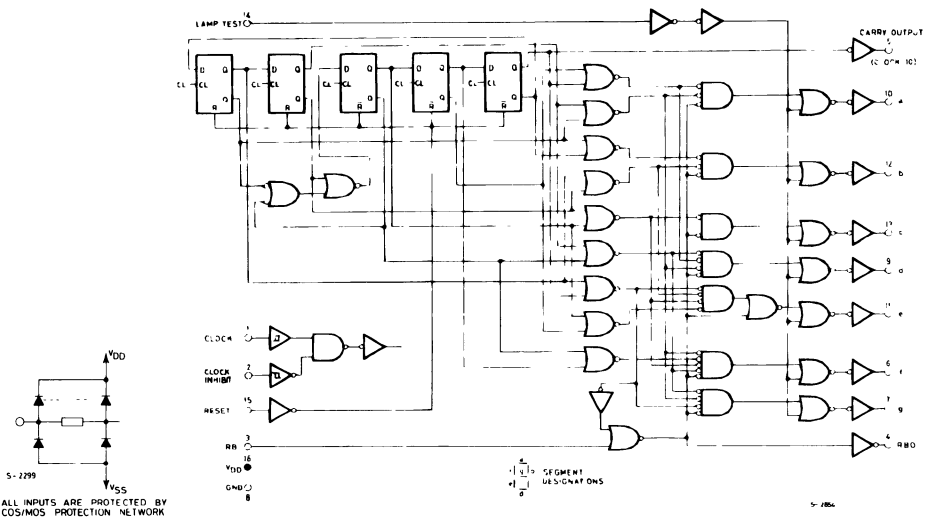
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAMS

### 4026B

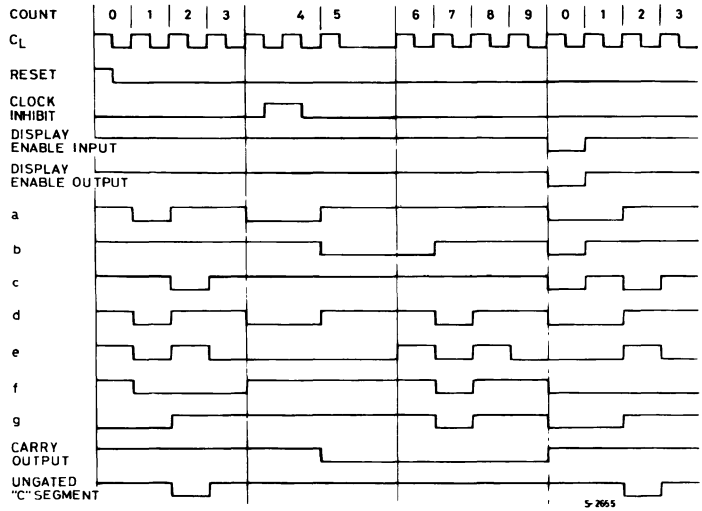



### 4033B

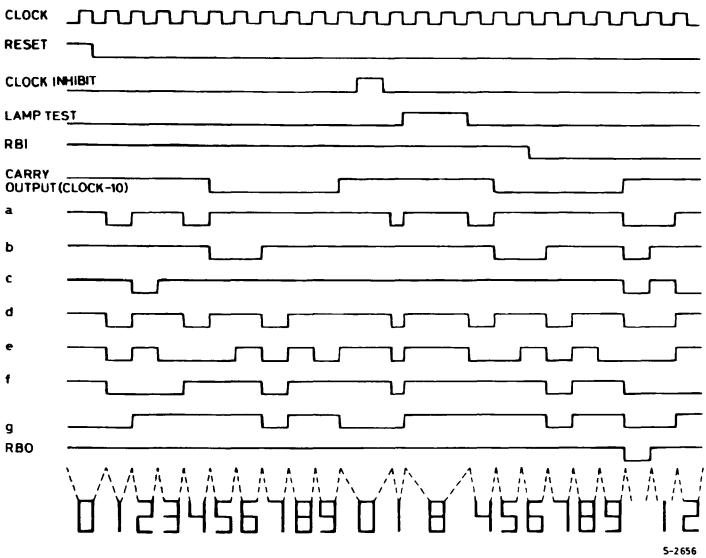


## TIMING DIAGRAMS

**4026B**




**4033B**



## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14 95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0 05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0 1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

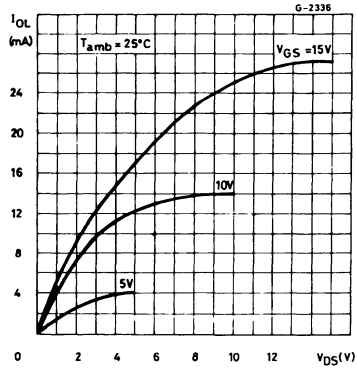
(*) $T_{Low}$= − 55°C for **HCC** device . − 40°C for **HCF** device
$T_{High}$= + 125°C for **HCC** device + 85°C for **HCF** device
The Noise Margin for both "1" and "0" level is . 1V min with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2 5V min with $V_{DD}$ = 15V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall times = 20ns)

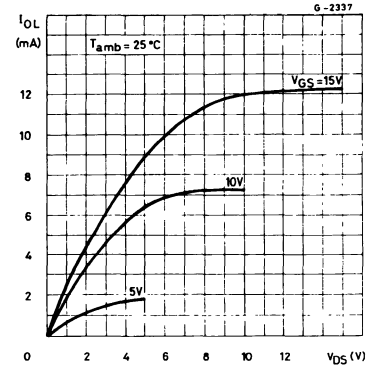
| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| **CLOCKED OPERATION** | | | | | | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time Carry Out Line | | 5 | | 250 | 500 | ns |
| | | | 10 | | 100 | 200 | |
| | | | 15 | | 75 | 150 | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time Decode Out Lines | | 5 | | 350 | 700 | ns |
| | | | 10 | | 125 | 250 | |
| | | | 15 | | 90 | 180 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time Carry Out Line | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 25 | 50 | |
| $f_{CL}$* | Maximum Clock Input Frequency | | 5 | 2.5 | 5 | | MHz |
| | | | 10 | 5.5 | 11 | | |
| | | | 15 | 8 | 16 | | |
| $t_{WC}$ | Clock Pulse Width | | 5 | | 110 | 270 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_r$, $t_f$ | Clock Input Rise or Fall Time | | 5<br>10<br>15 | Unlimited | | | µs |
| **RESET OPERATION** | | | | | | | |
| $t_{PLH}$, | Propagation Delay Time Carry Out Line | | 5 | | 275 | 550 | ns |
| | | | 10 | | 120 | 240 | |
| | | | 15 | | 80 | 160 | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time Decode Out Lines | | 5 | | 300 | 600 | ns |
| | | | 10 | | 125 | 250 | |
| | | | 15 | | 90 | 180 | |
| $t_{WR}$ | Reset Pulse Width | | 5 | | 100 | 120 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 25 | 50 | |
| $t_{rem}$ | Reset Removal Time | | 5 | | 0 | 30 | ns |
| | | | 10 | | 0 | 15 | |
| | | | 15 | | 0 | 10 | |

* Measured with respect to carry output line.

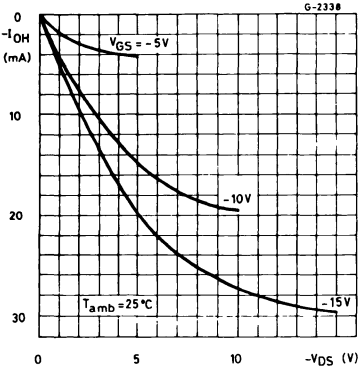
Typical Output Low (sink) Current.



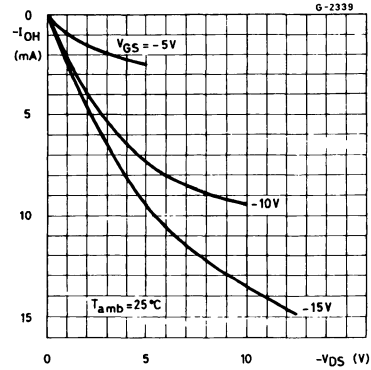

Minimum Output Low (sink) Current Characteristics.




Typical Output High (source) Current Characteristics.

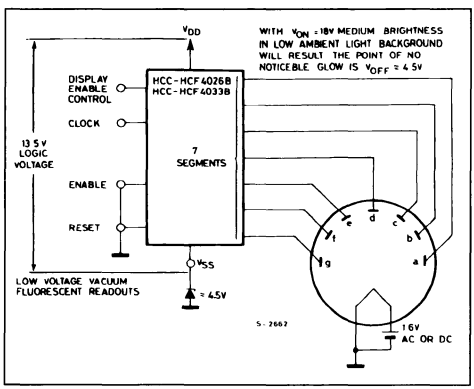



Minimum Output High (source) Current Characteristics.

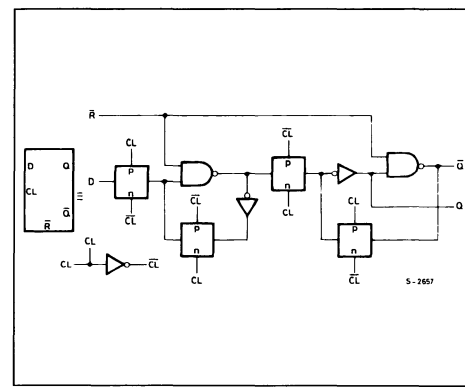



## TYPICAL APPLICATIONS

Interfacing with Filament Fluorescent Display.

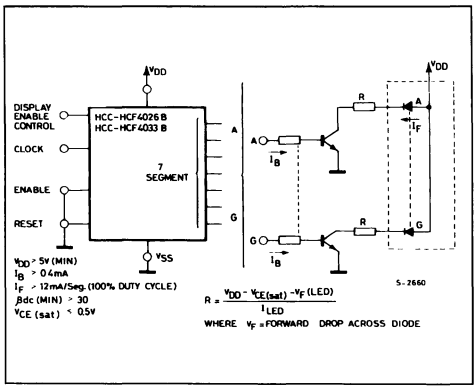



Detail of Typical Flip-flop Stage for Both Types.

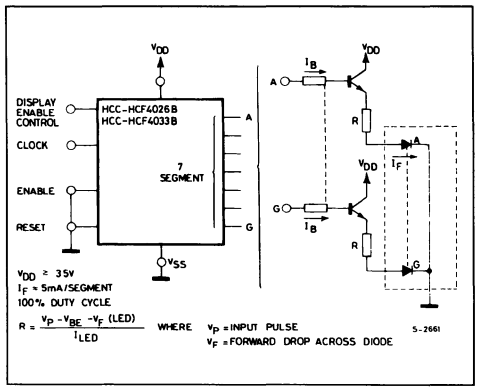


## TYPICAL APPLICATIONS (continued)

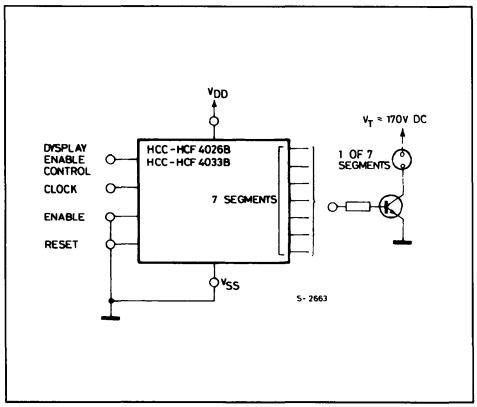
Interfacing with LED Displays (display common anode).



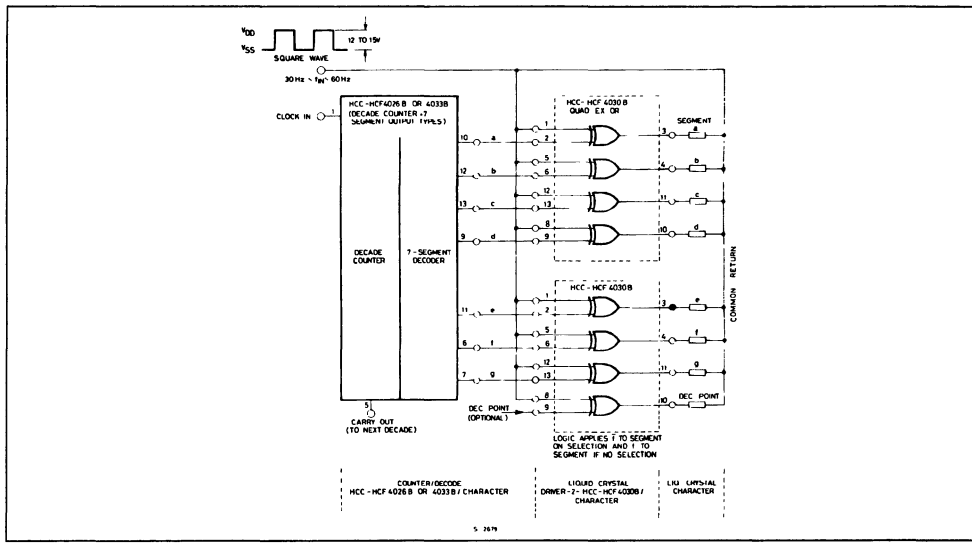

(Display Common Cathode).




Interfacing with NIXIE Tube.

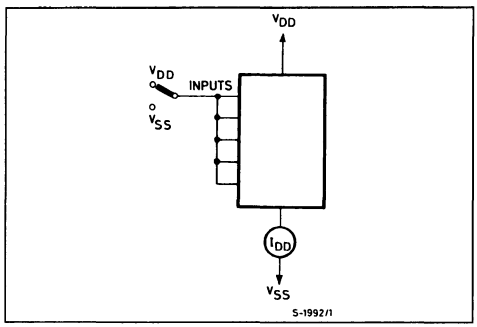


Interfacing with Liquid Cristal Displays.

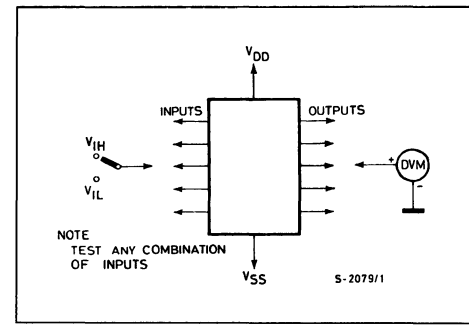



## TEST CIRCUITS

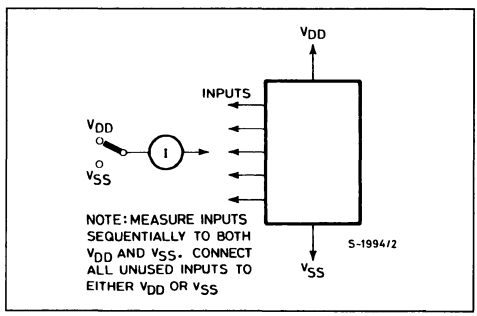
Quiescent Device Current.




Input Voltage.

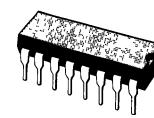



Input Current.

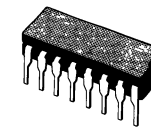


# DUAL-J-K MASTER-SLAVE FLIP-FLOP

- SET-RESET CAPABILITY
- STATIC FLIP-FLOP OPERATION - RETAINS STATE INDEFINITELY WITH CLOCK LEVEL EITHER "HIGH" OR "LOW"
- MEDIUM SPEED OPERATION - 16MHz (typ. clock toggle rate at 10V)
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES".



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

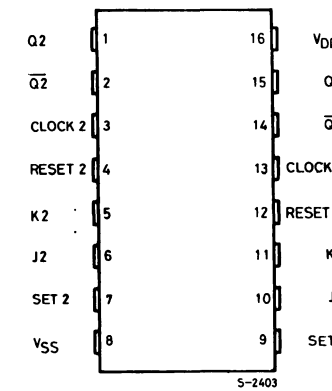
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4027BF HCF4027BM1
HCF4027BEY HCF4027BC1

## PIN CONNECTIONS



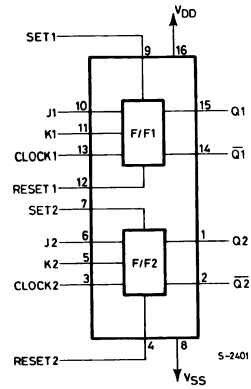

## DESCRIPTION

The **HCC4027B** (extended temperature range) and **HCF4027B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and plastic micro package.

The **HCC/HCF4027B** is a single monolithic chip integrated circuit containing two identical complementary-symmetry J-K master-slave flip-flops. Each flip-flop has provisions for individual J, K, Set, Reset, and Clock input signals, Buffered Q and Q signals are provided as outputs. This input-output arrangement provides for compatible operation with the **HCC/HCF4013B** dual D-type flip-flop.

The **HCC/HCF4027B** is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop ; changes in the flip-flop state are synchronous with the positive-going transition of the clock pulse. Set and reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for external periods may affect device reliability

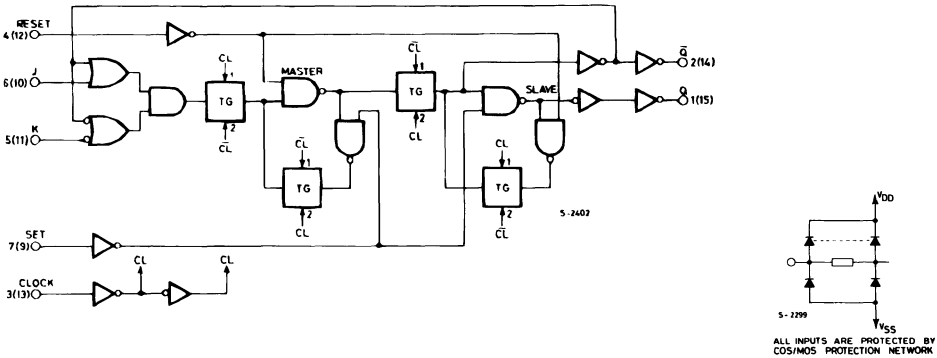
* All voltage values are referred to $V_{SS}$ pin voltage

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature · **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAM AND TRUTH TABLE

ONE OF TWO IDENTICAL J-K FLIP-FLOPS




## TRUTH TABLE

| Present State | | | | | CL$^{\Delta}$ | Next State | | |
|---|---|---|---|---|---|---|---|---|
| Inputs | | | | Output | | Outputs | | |
| J | K | S | R | Q | | Q | $\overline{Q}$ | |
| I | X | O | O | O | ⎍ | I | O | |
| X | O | O | O | I | ⎍ | I | O | |
| O | X | O | O | O | ⎍ | O | I | |
| X | I | O | O | I | ⎍ | O | I | |
| X | X | O | O | X | ⎎ | | | ← No Change |
| X | X | I | O | X | X | I | O | |
| X | X | O | I | X | X | O | I | |
| X | X | I | I | X | X | I | I | |

LOGIC I = HIGH LEVEL
LOGIC O = LOW LEVEL
Δ - LEVEL CHANGE
X - DON'T CARE

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 1 | | 0.02 | 1 | | 30 | μA |
| | | | 0/10 | | | 10 | | 2 | | 0.02 | 2 | | 60 | |
| | | | 0/15 | | | 15 | | 4 | | 0.02 | 4 | | 120 | |
| | | | 0/20 | | | 20 | | 20 | | 0.04 | 20 | | 600 | |
| | | HCF Types | 0/ 5 | | | 5 | | 4 | | 0.02 | 4 | | 30 | |
| | | | 0/10 | | | 10 | | 8 | | 0 02 | 8 | | 60 | |
| | | | 0/15 | | | 15 | | 16 | | 0.02 | 16 | | 120 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0 5/4.5 | < 1 | 5 | 3 5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1 1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0 1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

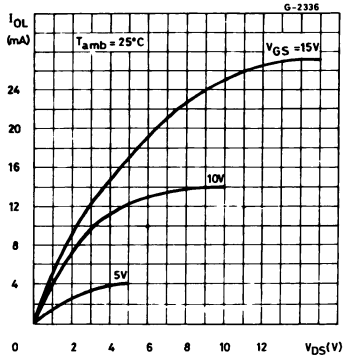
* $T_{Low}$= − 55°C for **HCC** device − 40°C for **HCF** device.
* $T_{High}$= + 125°C for **HCC** device . + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is . 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5 V min with $V_{DD}$ = 15V.

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ = 0.3%/°C values, all input rise and fall time = 20ns)

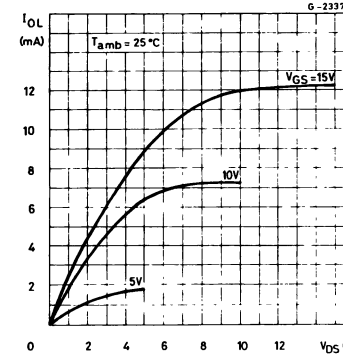
| Symbol | Parameter | | Test Conditions | Value | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time | Clock to Q or $\overline{Q}$ Outputs | | 5 | | 150 | 300 | ns |
| | | | | 10 | | 65 | 130 | |
| | | | | 15 | | 45 | 90 | |
| $t_{PLH}$ | Propagation Delay Time | Set to Q or Reset to $\overline{Q}$ | | 5 | | 150 | 300 | ns |
| | | | | 10 | | 65 | 130 | |
| | | | | 15 | | 45 | 90 | |
| $t_{PHL}$ | Propagation Delay Time | Set to $\overline{Q}$ or Reset to Q | | 5 | | 200 | 400 | |
| | | | | 10 | | 85 | 170 | |
| | | | | 15 | | 60 | 120 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | | 5 | | 100 | 200 | ns |
| | | | | 10 | | 50 | 100 | |
| | | | | 15 | | 40 | 80 | |
| $t_W$ | Pulse Width | Clock | | 5 | 140 | 70 | | ns |
| | | | | 10 | 60 | 30 | | |
| | | | | 15 | 40 | 20 | | |
| $t_W$ | Pulse Width | Set or Reset | | 5 | 180 | 90 | | |
| | | | | 10 | 80 | 40 | | |
| | | | | 15 | 50 | 25 | | |
| $t_r$,$t_f$ | Clock Input Rise or Fall Time | | | 5 | | | 15 | µs |
| | | | | 10 | | | 4 | |
| | | | | 15 | | | 1 | |
| $t_{setup}$ | Setup Time | Data | | 5 | 200 | 100 | | ns |
| | | | | 10 | 75 | 35 | | |
| | | | | 15 | 50 | 25 | | |
| $f_{max}$ | Maximum Clock Input Frequency * | Toggle Mode | | 5 | 3.5 | 7 | | MHz |
| | | | | 10 | 8 | 16 | | |
| | | | | 15 | 12 | 24 | | |

* Input tr, tf = 5ns.

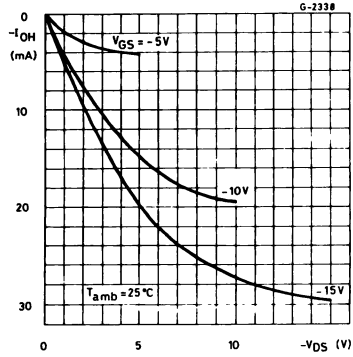
Typical Output Low (sink) Current Characteristics.



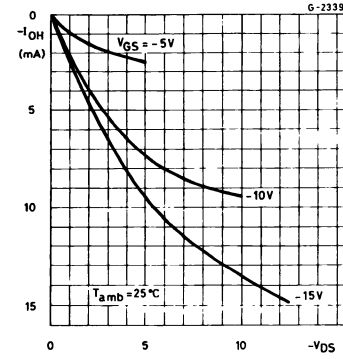

Minimum Output Low (sink) Current Characteristics.



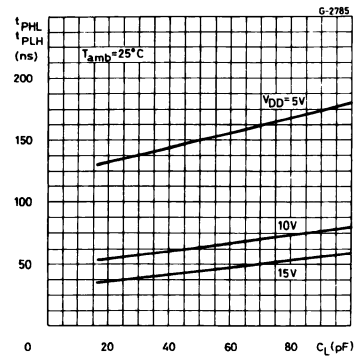

Typical Output High (source) Current Characteristics.



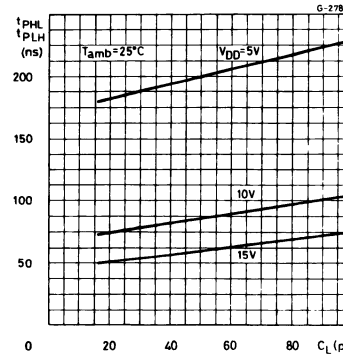

Minimum Output High (source) Current Characteristics.



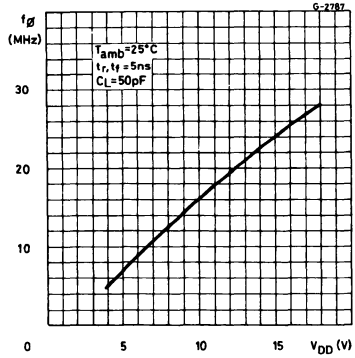

Typical Propagation Delay Time vs.Load Capacitance (CLOCK or SET to Q, CLOCK or RESET to $\overline{Q}$).



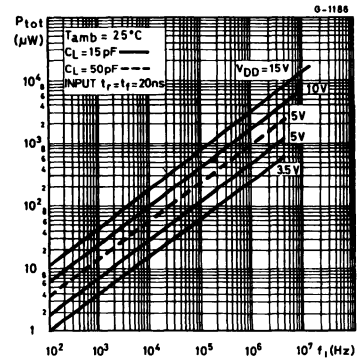

Typical Propagation Delay Time vs. Load Capacitance (SET to $\overline{Q}$ or RESET to Q).



Typical Maximum Clock Frequency vs. Supply Voltage (Toggle Mode).

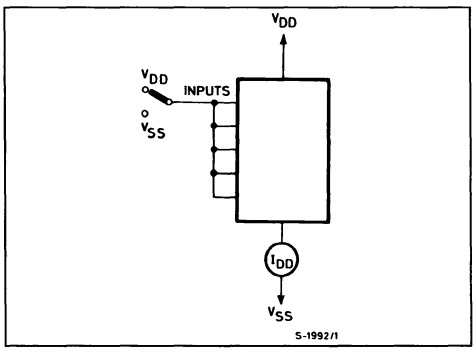



Typical Dynamic Power Dissipation/ Per Device vs.Frequency.

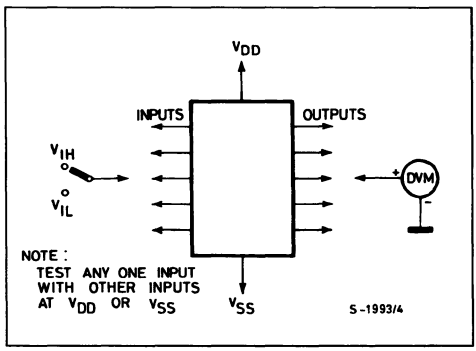



## TEST CIRCUITS

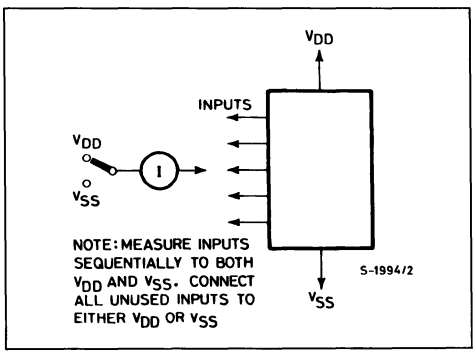
Quiescent Device Current.




Input Voltage.



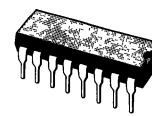

Input Leakage Current.



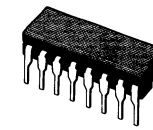
# HCC/HCF4028B

## BCD-TO-DECIMAL DECODER

- BCD-TO-DECIMAL DECODING OR BINARY-TO-OCTAL DECODING
- HIGH DECODED OUTPUT DRIVE CAPABILITY
- "POSITIVE LOGIC" INPUTS AND OUTPUTS : DECODED OUTPUTS GO HIGH ON SELECTION
- MEDIUM-SPEED OPERATION : $t_{PHL}$, $t_{PLH}$ = 80ns (typ.) @ $V_{DD}$ = 10V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

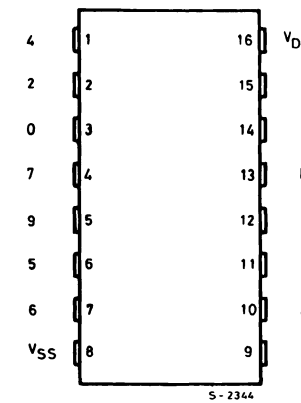
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4028BF HCF4028BM1
HCF4028BEY HCF4028BC1

**PIN CONNECTIONS**

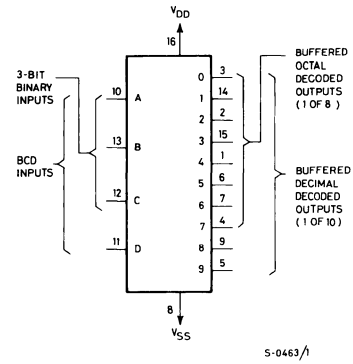



### DESCRIPTION

The **HCC4028B** (extended temperature range) and **HCF4028B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and plastic micropackage.

The **HCC/HCF4028B** types are BCD-to-decimal or binary-to-octal decoders consisting of buffering on all 4 inputs, decoding-logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D, results in a high level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in octal code at output 0 to 7 if D = "0". High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage · **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

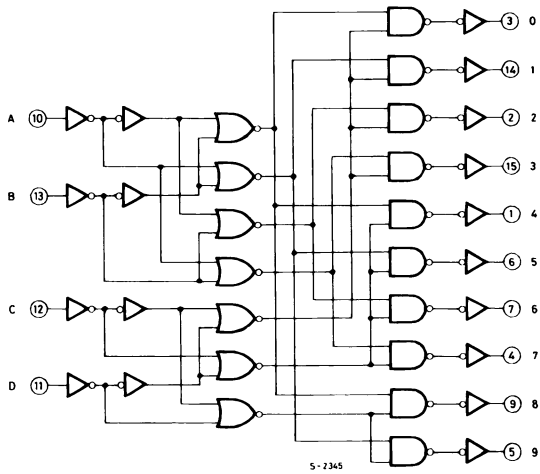
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to $V_{SS}$ pin voltage

## RECOMMENDED OPERATING CONDITIONS

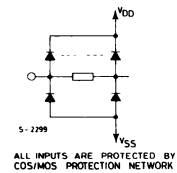
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAM AND TRUTH TABLE




| D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

WHERE 1 = HIGH LEVEL



## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

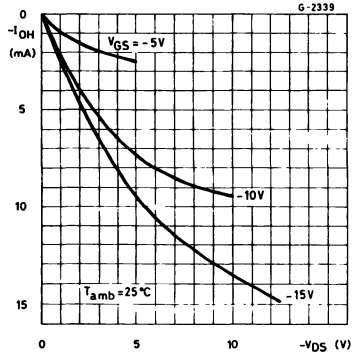
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0 04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4 95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9 95 | | 9 95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14 95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0 05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0 05 | | | 0 05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1 5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/5 | 2 5 | | 5 | – 2 | | – 1 6 | – 3.2 | | – 1 15 | | mA |
| | | | 0/5 | 4.6 | | 5 | – 0.64 | | – 0.51 | – 1 | | – 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | – 1.6 | | – 1 3 | – 2.6 | | – 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | – 4.2 | | – 3.4 | – 6.8 | | – 2 4 | | |
| | | HCF Types | 0/5 | 2.5 | | 5 | – 1.53 | | – 1.36 | – 3.2 | | – 1.1 | | |
| | | | 0/5 | 4.6 | | 5 | – 0.52 | | – 0.44 | – 1 | | – 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | – 1.3 | | – 1.1 | – 2.6 | | – 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | – 3.6 | | – 3.0 | – 6 8 | | – 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1 6 | | 1.3 | 2.6 | | 0 9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0 9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6 8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = – 55°C for **HCC** device – 40°C for **HCF** device
* $T_{High}$ = + 125°C for **HCC** device · + 85°C for **HCF** device
The Noise Margin for both "1" and "0" level is . 1V min with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2 5 V min with $V_{DD}$ = 15V

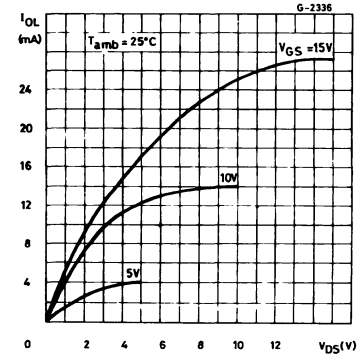
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall times = 20ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time (clock to "out") | | 5 | | 175 | 350 | ns |
| | | | 10 | | 80 | 160 | |
| | | | 15 | | 60 | 120 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

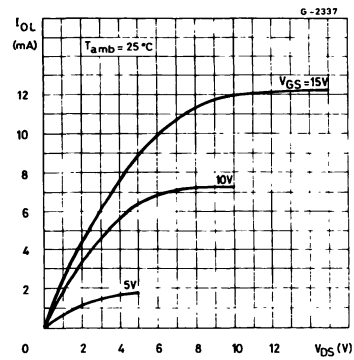
Minimum Output High (source) Current Characteristics.



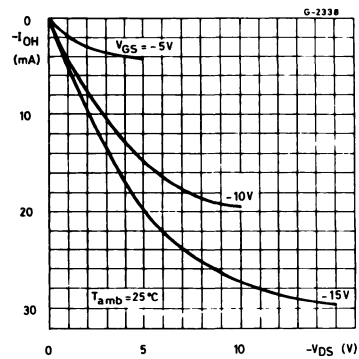

Typical Output Low (sink) Current.



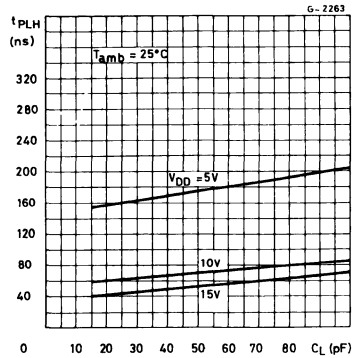

Minimum Output Low (Sink) Current Characteristics.



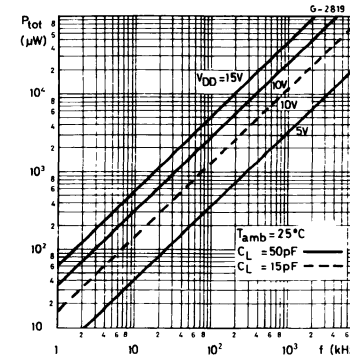

Typical Output High (source) Current Characteristics.



Typical Propagation Delay Time as a Function load Capacitance.




Typical Dynamic Power Dissipation as a Function of Input Frequency .




## TYPICAL APPLICATIONS

The circuit shown in fig. 1 converts any 4-bit code to a decimal or hexadecimal code Fig 2 shows a number of codes and the decimal or hexadecimal number in these codes which must be applied to the input pins of the HCC/HCF4028B to select a particular output. For example : in order to get a "high" on output n8 the input must be either an 8 expressed in 4-bit binary code, a 15 expressed in 4-bit gray code, or a 5 expressed in excess-3code.

**Figure 1** : Code Conversion Circuit.

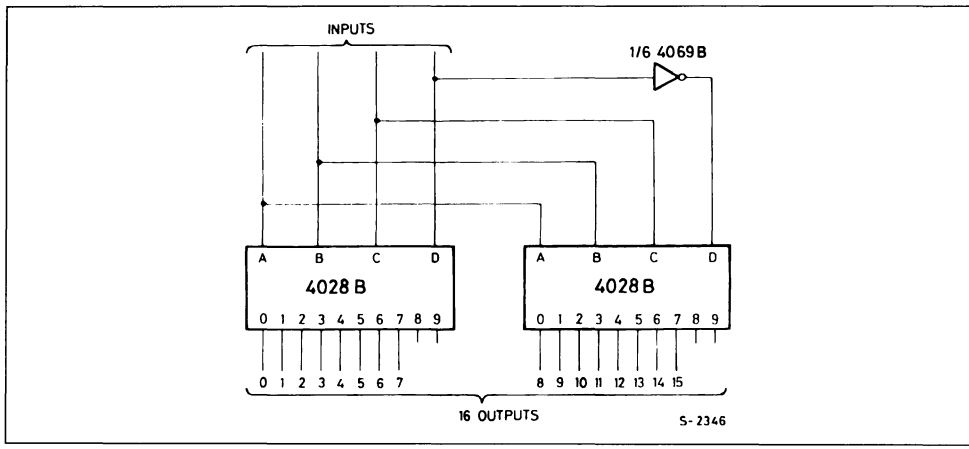


**Figure 2** : Code Conversion Chart.

| INPUTS | | | | INPUT CODES | | | | | | OUTPUT NUMBER | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Hexa Decimal | | Decimal | | | | | | | | | | | | | | | | | | | | |
| D | C | B | A | 4 BIT BINARY | 4 BIT GRAY | EXCESS 3 | EXCESS 3 GRAY | AIKEN | 4221 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 0 | 0 | 0 | 0 | 0 | 0 | | | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | | | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 2 | 3 | | 0 | 2 | 2 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 3 | 2 | 0 | 3 | 3 | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 4 | 7 | 1 | 4 | 4 | | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 5 | 6 | 2 | | | 3 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 6 | 4 | 3 | 1 | | 4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 7 | 5 | 4 | 2 | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 8 | 15 | 5 | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 9 | 14 | 6 | | | 5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 10 | 12 | 7 | 9 | | 6 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 11 | 13 | 8 | | 5 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 12 | 8 | 9 | 5 | 6 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 13 | 9 | | 6 | 7 | 7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 14 | 11 | | 8 | 8 | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 15 | 10 | | 7 | 9 | 9 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**TYPICAL APPLICATIONS** (continued)

**Figure 3 :** 6-bit binary to 1 of 64 Adress Decoder.

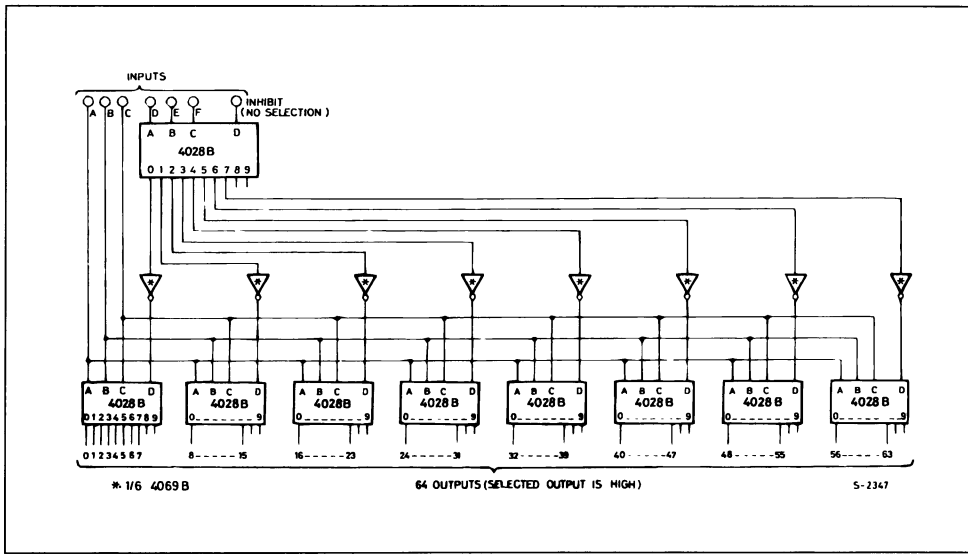
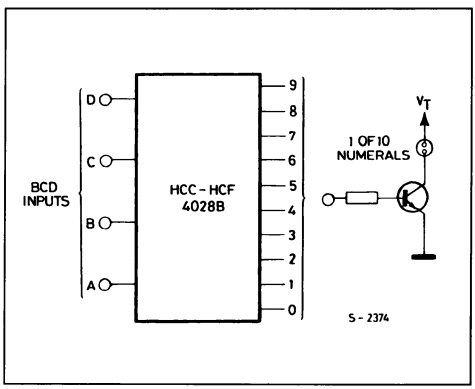
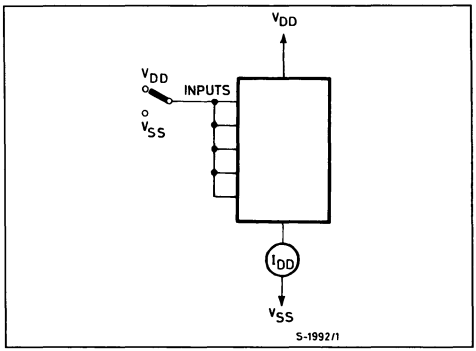



**Figure 4** : Neon Readout (nixie tube) Display Application.

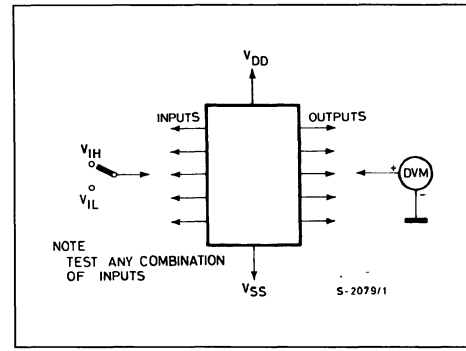


## TEST CIRCUITS

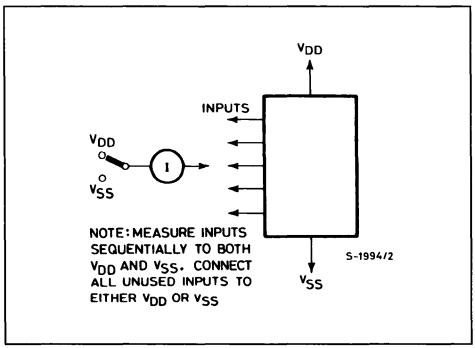
Quiescent Device Current.



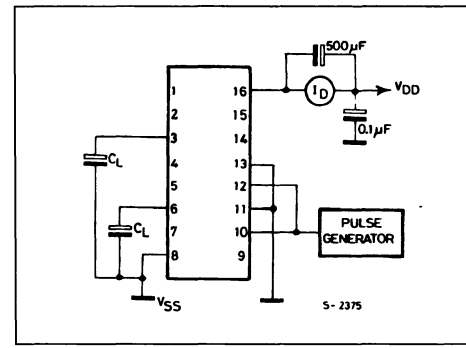

Noise Immunity.



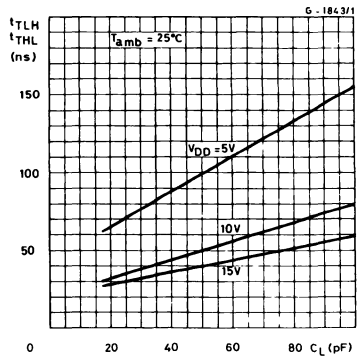

Input Leakage Current.




Dynamic Power Dissipation.




Typical Transition Time vs. Load Capacitance.

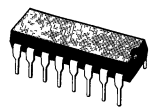


SGS-THOMSON
MICROELECTRONICS

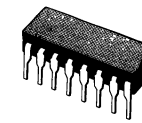
# HCC4029B
# HCF4029B

## PRESETTABLE UP/DOWN COUNTER BINARY OR BCD DECADE

- MEDIUM SPEED OPERATION - 8MHz (typ.) @ $C_L$ = 50pF AND $V_{DD}$-$V_{SS}$ = 10V
- MULTI-PACKAGE PARALLEL CLOCKING FOR SYNCHRONOUS HIGH SPEED OUTPUT RESPONSE OR RIPPLE CLOCKING FOR SLOW CLOCK INPUT RISE AND FALL TIMES
- "PRESET ENABLE" AND INDIVIDUAL "JAM" INPUTS PROVIDED
- BINARY OR DECADE UP/DOWN COUNTING
- BCD OUTPUTS IN DECADE MODE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Package)

**M1**
(Micro Package)

**C1**
(Chip Carrier)

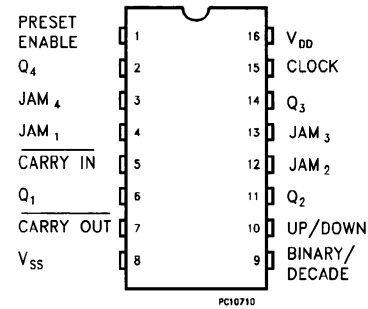
**ORDER CODES :**

| | |
|---|---|
| HCC4029BF | HCF4029BM1 |
| HCF4029BEY | HCF4029BC1 |

### DESCRIPTION

The **HCC4029B** (extended temperature range) and **HCF4029B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF4029B** consists of a four-stage binary or BCD-decade up/down counter with provisions for look-ahead carry in both counting modes. The inputs consist of a single CLOCK, CARRY-IN (CLOCK ENABLE), BINARY/DECADE, UP/DOWN, PRESET ENABLE, and four individual JAM signals. Q1, Q2, Q3, Q4 and a CARRY OUT signal are provided as outputs. A high PRESET ENABLE signal allows information on the JAM INPUTS to preset the counter to any state asynchronously with the clock. A low on each JAM line, when the PRESET-ENABLE signal is high, resets the counter to its zero count. The counter is advanced one count at the positive transition of the clock when the CARRY-IN and PRESET ENABLE signals, are low. Advancement is inhibited when the CARRY-IN or PRESET ENABLE signals are high. The CARRY-OUT signal is normally high and goes

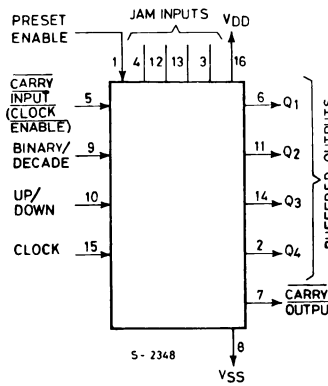
### PIN CONNECTIONS




NC = No Internal Connection

counter reaches its maximum count in the UP mode or the minimum count in the DOWN mode provided the CARRY-IN signal is low. The CARRY-IN signal in the low state can thus be considered a CLOCK ENABLE. The CARRY-IN terminal must be connected to $V_{SS}$ when not in use. Binary counting is accomplished when the BINARY/DECADE input is high ; the counter counts in the decade mode when the BINARY/DECADE input is low. The counter counts Up when to UP/DOWN INPUT is high, and Down when the UP/DOWN INPUT is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement as shown in cascading counter packages. Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ * | Supply Voltage. **HCC** Types<br>**HCF** Types | -0.5 to +20<br>-0.5 to +18 | V<br>V |
| $V_i$ | Input Voltage | -0 5 to $V_{DD}$ + 0 5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for Top = Full Package Temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |

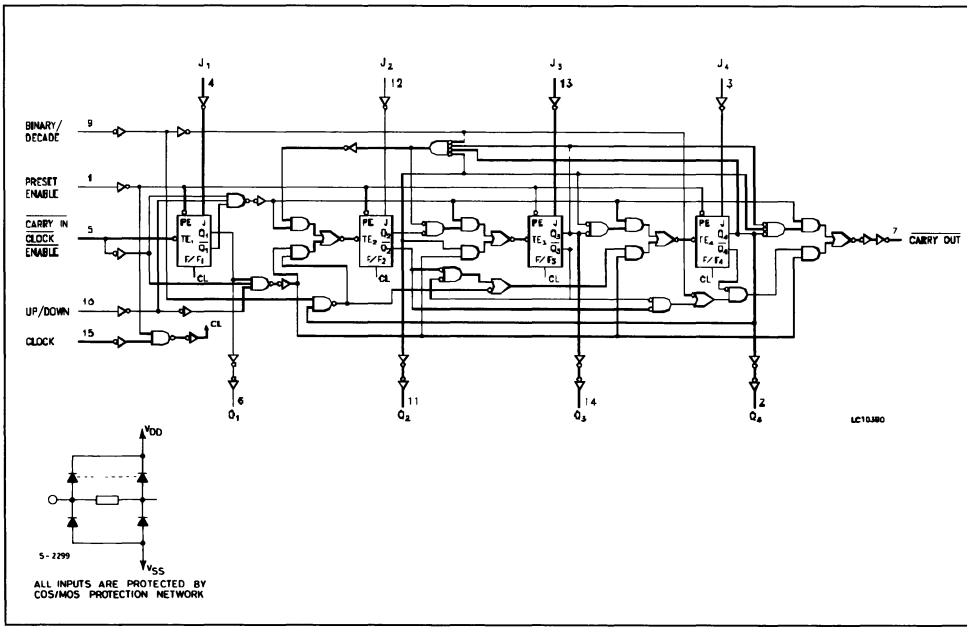
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for external periods may affect device reliability.

All voltage values are referred to $V_{SS}$ pin voltage

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage: **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |

## LOGIC DIAGRAMS




## TRUTH TABLES

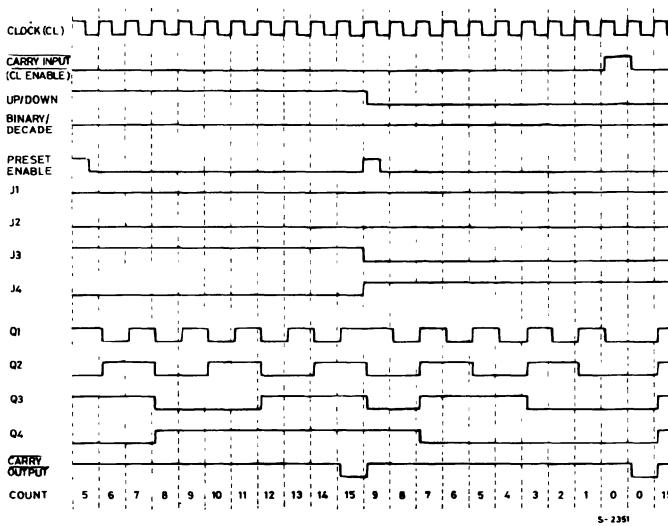
| CLOCK | TE | PE | J | Q | $\overline{Q}$ |
|---|---|---|---|---|---|
| X | X | O | O | O | I |
| ⌐ | O | I | X | $\overline{Q}$ | Q |
| X | X | O | I | I | O |
| ⌐ | I | I | X | Q | $\overline{Q}$ NC |
| ⌐ | X | I | X | Q | $\overline{Q}$ NC |

X DON'T CARE

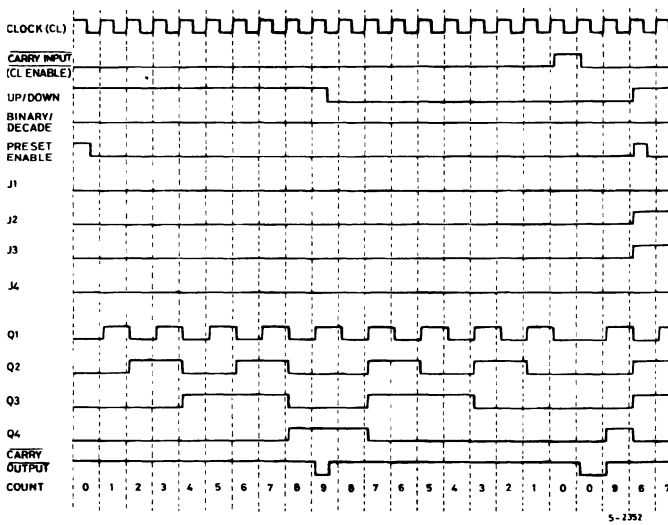
| Control Input | Logic Level | Action |
|---|---|---|
| BIN/DEC (B/D) | I | Binary Count |
| | O | Decade Count |
| UP/DOWN (U/D) | I | Up Count |
| | O | Down Count |
| Preset Enable (PE) | I | Jam In |
| | O | No Jam |
| Carry In (CI) (Clock Enable) | I | No Counter Advance at Pos. Clock Transition |
| | O | Advance Counter at Pos. Clock Transition |

## TIMING DIAGRAMS

Binary Mode




Decade Mode



## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditios | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{LOW}$ * | | 25 °C | | | $T_{HIGH}$ * | | |
| | | | | | | | Min. | Max. | Min. | Typ. | Max. | Min. | Max. | |
| $I_L$ | Quiescent Current | HCC Types | 0/5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/5 | 2.5 | | 5 | -2 | | -1.6 | -3.2 | | -1.15 | | mA |
| | | | 0/5 | 4.6 | | 5 | -0.64 | | -0.51 | -1 | | -0.36 | | |
| | | | 0/10 | 9.5 | | 10 | -1.6 | | -1.3 | -2.6 | | -0.9 | | |
| | | | 0/15 | 13.5 | | 15 | -4.2 | | -3.4 | -6.8 | | -2.4 | | |
| | | HCF Types | 0/5 | 2.5 | | 5 | -1.53 | | -1.36 | -3.2 | | -1.1 | | |
| | | | 0/5 | 4.6 | | 5 | -0.52 | | -0.44 | -1 | | -0.36 | | |
| | | | 0/10 | 9.5 | | 10 | -1.3 | | -1.1 | -2.6 | | -0.9 | | |
| | | | 0/15 | 13.5 | | 15 | -3.6 | | -3.0 | -6.8 | | -2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ±0.1 | | $±10^{-5}$ | ±0.1 | | ±1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ±0.3 | | $±10^{-5}$ | ±0.3 | | ±1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{LOW}$ = -55 °C for **HCC** device: -40 °C for **HCF** device.

* $T_{HIGH}$ = +125 °C for **HCC** device: +85 °C for **HCF** device.

The Noise Margin for both "1" and "0" level is. 1V min. with $V_{DD}$ = 5 V, 2 V min. with $V_{DD}$ = 10 V, 2.5 V min. with $V_{DD}$ = 15 V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 KΩ, typical temperature coefficent for all $V_{DD}$ values is 03 %/°C, all input rise and fall times= 20 ns)

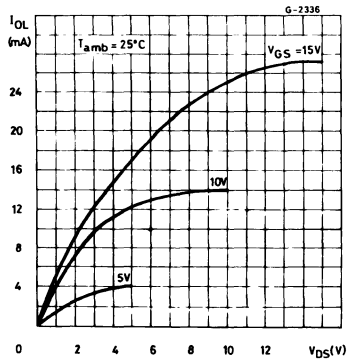
| Symbol | Parameter | Test Conditions | Value | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (Q Outputs) | | 5 | | 250 | 500 | ns |
| | | | 10 | | 120 | 240 | |
| | | | 15 | | 90 | 180 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (Carry Output) | | 5 | | 280 | 560 | ns |
| | | | 10 | | 130 | 260 | |
| | | | 15 | | 95 | 190 | |
| $t_{TLH}$ $t_{THL}$ | Transition Time (Q Outputs, Carry Output) | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_W$ | Minimum Clock Pulse Width | | 5 | | 90 | 180 | ns |
| | | | 10 | | 45 | 90 | |
| | | | 15 | | 30 | 60 | |
| $t_r$, $t_f$ ** | Clock Rise and Fall Time | | 5 | | | 15 | µs |
| | | | 10 | | | 15 | |
| | | | 15 | | | 15 | |
| $t_{setup}$ * | Minimum Setup Time (Carry Input) | | 5 | | 30 | 60 | ns |
| | | | 10 | | 10 | 20 | |
| | | | 15 | | 6 | 12 | |
| $t_{setup}$ | Minimum Setup Time (B/D or UD) | | 5 | | 170 | 340 | |
| | | | 10 | | 70 | 140 | |
| | | | 15 | | 50 | 100 | |
| $f_{max}$ | Maximum Clock Input Frequency | | 5 | 2 | 4 | | MHz |
| | | | 10 | 4 | 8 | | |
| | | | 15 | 5.5 | 11 | | |
| **PRESET ENABLE** | | | | | | | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (Q Outputs) | | 5 | | 235 | 470 | ns |
| | | | 10 | | 100 | 200 | |
| | | | 15 | | 80 | 160 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (Carry Output) | | 5 | | 320 | 640 | |
| | | | 10 | | 145 | 290 | |
| | | | 15 | | 105 | 210 | |
| $t_W$ | Minimum Preset Enable (Pulse Width) | | 5 | | 65 | 130 | ns |
| | | | 10 | | 35 | 70 | |
| | | | 15 | | 25 | 50 | |
| $t_{rem}$ * | Minimum Preset Enable (Removal Time) | | 5 | | 100 | 200 | ns |
| | | | 10 | | 55 | 110 | |
| | | | 15 | | 40 | 80 | |
| **CARRY INPUT** | | | | | | | |
| $t_{PHL}$ $t_{PLH}$ | Propagation Delay Time (Carry Output) | | 5 | | 170 | 340 | ns |
| | | | 10 | | 70 | 140 | |
| | | | 15 | | 50 | 100 | |
| $t_{setup}$ *** | Minimum Setup Time (Carry In) | | 5 | | 25 | 50 | ns |
| | | | 10 | | 15 | 30 | |
| | | | 15 | | 12 | 25 | |
| $t_{hold}$ | Minimum Hold Time (Carry In) | | 5 | | 100 | 200 | |
| | | | 10 | | 35 | 70 | |
| | | | 15 | | 30 | 60 | |

* From Up/Down, Binary/Decade, Carry In or Preset Enable Control Inputs to Clock Edge

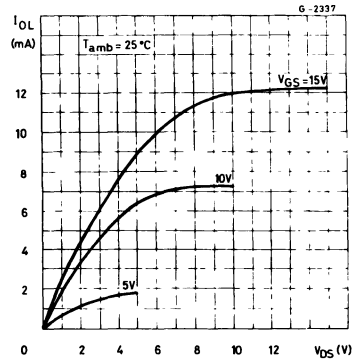
** If more than one unit is cascated in the parallel clocked application tr should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitance load.

*** From Carry in to Clock Edge.

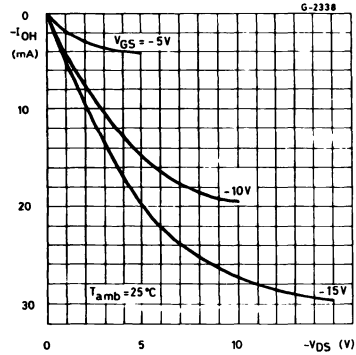
Typical Output Low (sink) Current Characteristics.



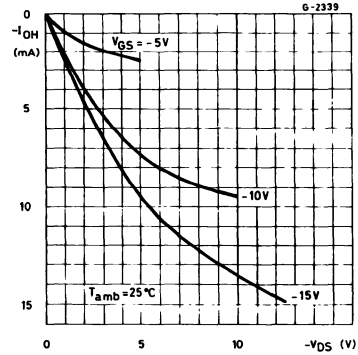

Minimum Output Low (sink) Current Characteristics.




Typical Output High (source) Current Characteristics.

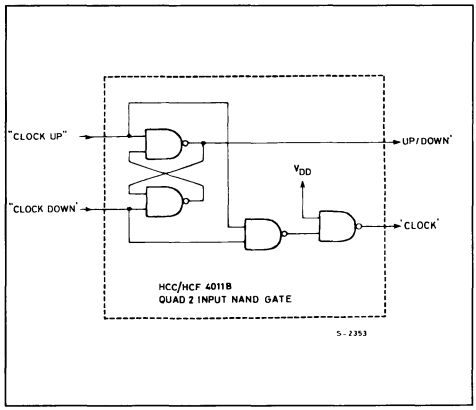



Minimum Output High (source) Current Characteristics.



## APPLICATIONS

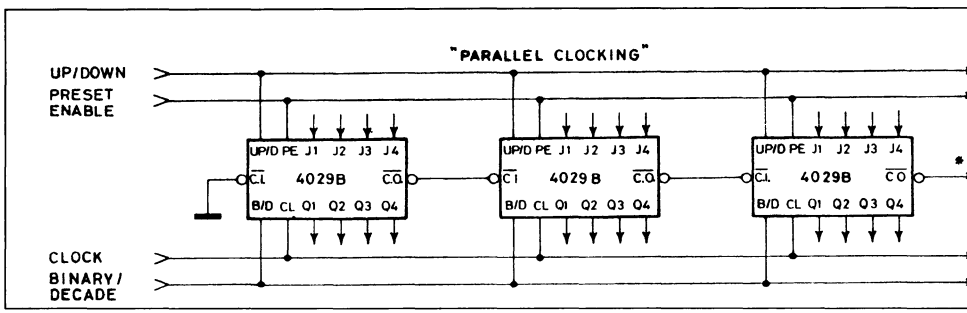
Conversion of Clock up, Clock Down Input Signals to Clock and Up/Down Inputs Signals.



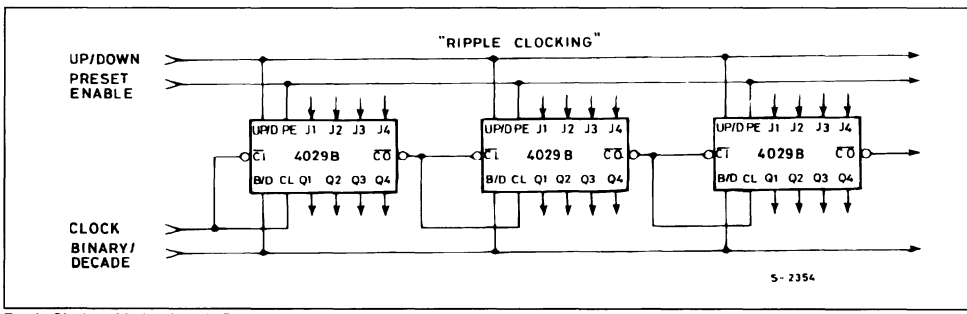

The **HCC/HCF4029B** CLOCK and UP/DOWN inputs are used directly in most applications. In applications where CLOCK UP and CLOCK DOWN inputs are provided, conversion to the **HCC/HCF4029B** CLOCK and UP/DOWN inputs can easily be realized by use of the circuit.

**HCC/HCF4029B** changes count on positive transitions of CLOCK UP or CLOCK DOWN inputs. For the gate configuration shown below, when counting up the CLOCK DOWN input must be maintained high and conversely when counting down the CLOCK UP input must be maintained high.

Cascading Counter Packages.




* CARRY-OUT lines at the 2nd, 3rd, et., stages may have a negative-going glitch pulse resulting from differential delays of different **HCC/HCF4029B** IC's. These negative-going glitches do not affect proper **HCC/HCF4029B** operation However, if the CARRY-OUT signals are used to trigger other edge-sensitive logic devices, such as FF's or counters, the CARRY-OUT signals should be gated with the clock signal using a 2-input NOR gate such as **HCC/HCF4001B**



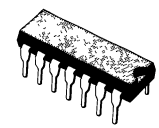

Ripple Clocking Mode : The Up/Down control can be changed at any count. The only restriction on changing the Up/Down control is that the clock input to the first counting stage must be high.

SGS-THOMSON MICROELECTRONICS

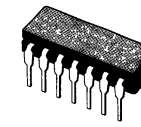
# HCC/HCF4030B

## QUAD EXCLUSIVE-OR GATE

- MEDIUM-SPEED OPERATION – $t_{PHL} = t_{PLH}$ = 60ns (typ.) @ $C_L$ = 50pF and $V_{DD} - V_{SS}$ = 10V
- LOW OUTPUT IMPEDANCE : 500Ω (typ.) @ $V_{DD} - V_{SS}$ = 10V
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

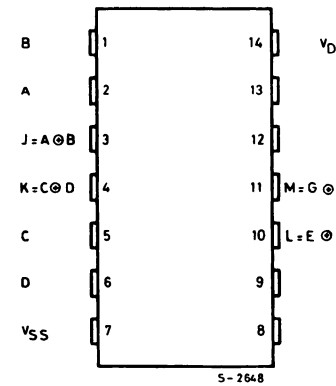
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4030BF HCF4030BM1
HCF4030BEY HCF4030BC1

**PIN CONNECTIONS**

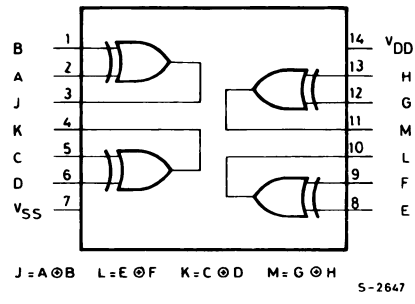



### DESCRIPTION

The **HCC4030B** (extended temperature range) and **HCF4030B** (intermediate temperature range) are monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package and plastic micro package.

The **HCC/HCF4030B** types consist of four independent exclusive-OR gates integrated on a single monolithic silicon chip. Each exclusive-OR gate consists of four n-channel and four p-channel enhancement-type transistors. All inputs and outputs are protected against electrostatic effects.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage: **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability

* All voltages are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

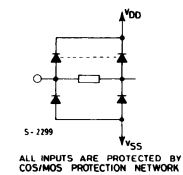
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## TRUTH TABLE

One of Four Identical Gates

| A | B | J |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |

Where "1" = High level
"0" = Low level.



## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

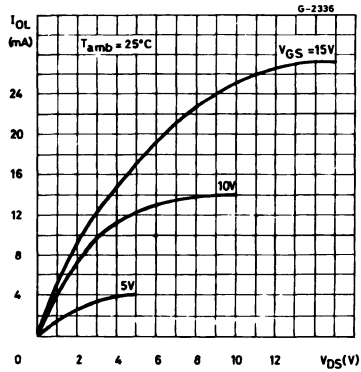
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 1 | | 0.02 | 1 | | 30 | μA |
| | | | 0/10 | | | 10 | | 2 | | 0.02 | 2 | | 60 | |
| | | | 0/15 | | | 15 | | 4 | | 0.02 | 4 | | 120 | |
| | | | 0/20 | | | 20 | | 20 | | 0.04 | 20 | | 600 | |
| | | HCF Types | 0/ 5 | | | 5 | | 4 | | 0.02 | 4 | | 30 | |
| | | | 0/10 | | | 10 | | 8 | | 0.02 | 8 | | 60 | |
| | | | 0/15 | | | 15 | | 16 | | 0.02 | 16 | | 120 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2.5 V min. with $V_{DD}$ = 15V.

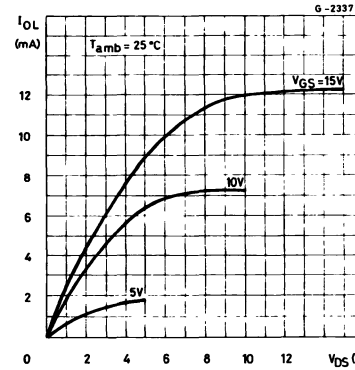
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ = 0.3%/°C values, all input rise and fall time = 20ns)

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time | 5 | | 140 | 280 | ns |
| | | 10 | | 65 | 130 | |
| | | 15 | | 50 | 100 | |
| $t_{TLH}$, $t_{THL}$ | Transition Time | 5 | | 100 | 200 | ns |
| | | 10 | | 50 | 100 | |
| | | 15 | | 40 | 80 | |

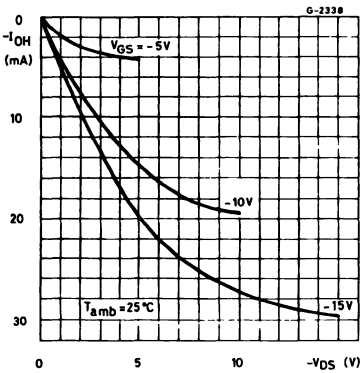
Typical Output Low (sink) Current Characteristics.



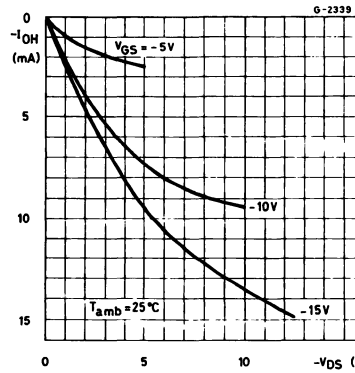

Minimum Output Low (sink) Current Characteristics.




Typical Output High (source) Current Characteristics.

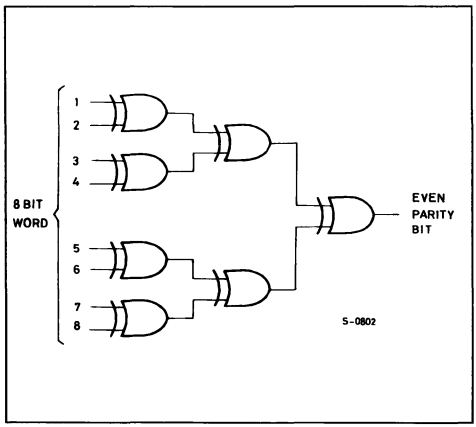



Minimum Output High (source) Current Characteristics.

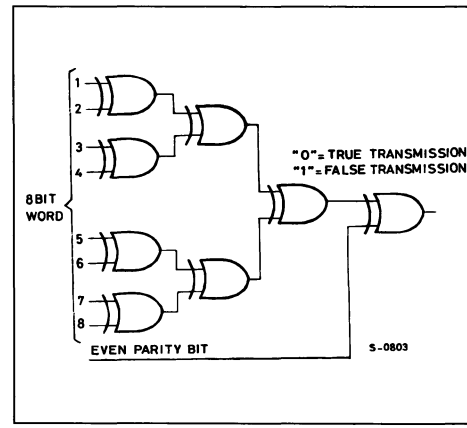


## TYPICAL APPLICATIONS

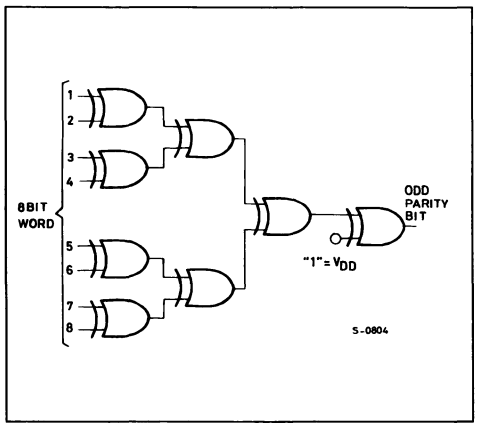
EVEN-PARITY-BIT GENERATOR
(1-3/4 x **HCC/HCF4030B**).



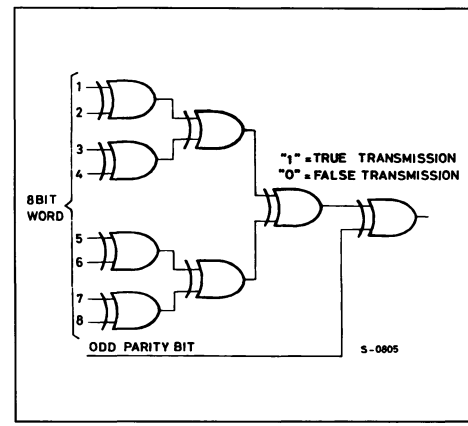

EVEN-PARITY-CHECKER
(2 x **HCC/HCF4030B**).




ODD-PARITY-BIT GENERATOR
(2 x **HCC/HCF4030B**).

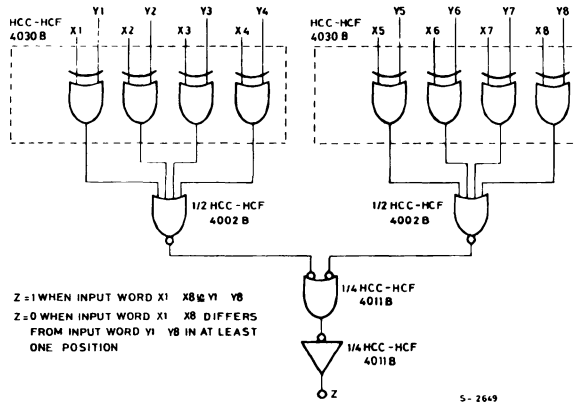



ODD-PARITY CHECKER
(2 x **HCC/HCF4030B**).



## TYPICAL APPLICATIONS (continued)

### 8-BIT COMPARATOR




### 8-BIT TWO'S COMPLEMENT ADDER-SUBSTRACTOR

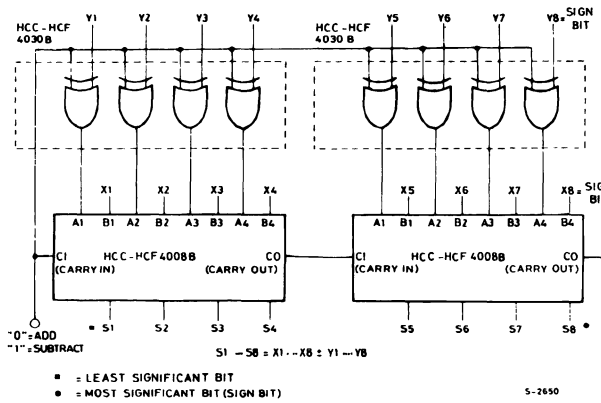


**Table 1 :** Two's Complement Numbers and Their Equivalent Decimal Values.

| $X_8$ | $X_7$ | $X_6$ | $X_5$ | $X_4$ | $X_3$ | $X_2$ | $X_1$ | | | $X_8$ | $X_7$ | $X_6$ | $X_5$ | $X_4$ | $X_3$ | $X_2$ | $X_1$ | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | = −1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | = | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | = −2 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | = | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | = −3 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | = | 3 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | = −4 |
| | | | | | | | | | | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | = −5 |
| | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | = | 126 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | = −127 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | = | 127 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = −128 |

The two's complement adder-substractor can add or substract any two of the numbers in table 1. For example :

a)

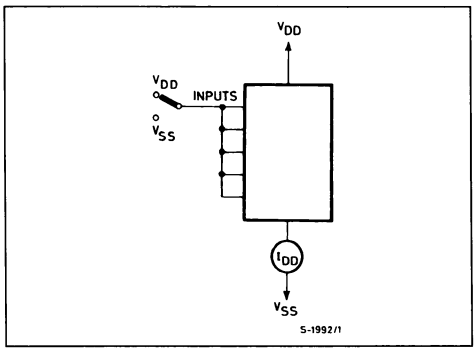
| | | SIGN BIT | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| + = | | | | | | | | | |
| −5 | X | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 + |
| | Y | 1 | 1 | 1 | 1 | 1 | 0 | 1 | −5 + |
| | CI | | | | | | | 0 | |
| | S | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 = −3 |
| | CO | | | | | | | | |

b)

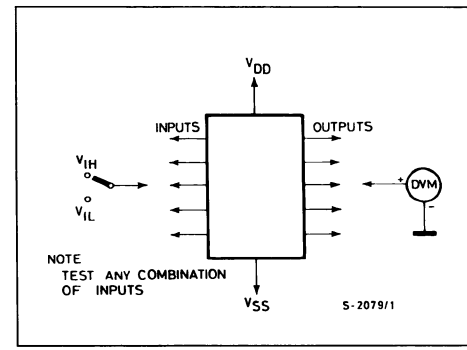
| | | SIGN BIT | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| − = | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 −2 + |
| −5 | Y | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 −5 |
| | Y | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 + |
| | CL | | | | | | | | 1 |
| | S | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 = 3 |
| | CO | | | | | | | | |

## TEST CIRCUITS

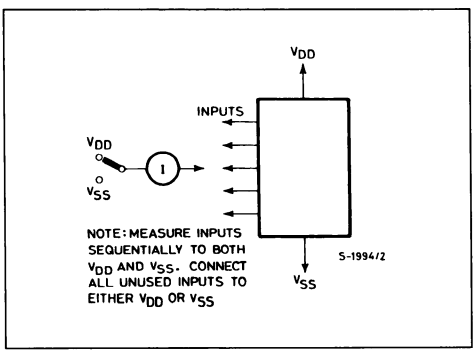
Quiescent Device Current.




Input Voltage.

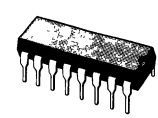



Input Leakage Current.

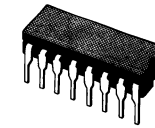


# 64-STAGE STATIC SHIFT REGISTER

- FULLY STATIC OPERATION : DC to 16MHz (TYP.) @ $V_{DD} - V_{SS} = 15V$
- STANDARD TTL DRIVE CAPABILITY ON Q OUTPUT
- RECIRCULATION CAPABILITY
- THREE CASCADING MODES :
  DIRECT CLOCKING FOR HIGH-SPEED OPERATION
  DELAYED CLOCKING FOR REDUCED CLOCK DRIVE REQUIREMENTS
  ADDITIONAL 1/2 STAGE FOR SLOW CLOCKS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA at 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



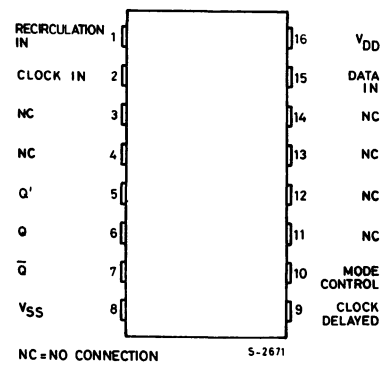
**F**
(Ceramic Package)

**C1**
(Chip Carrier)

**ORDER CODES :**

HCC4031BF HCF4031BEY
HCF4031BC1

**PIN CONNECTIONS**



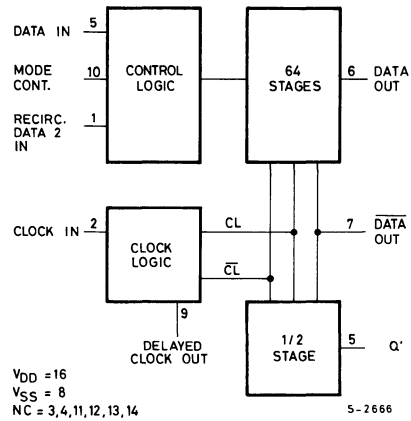

## DESCRIPTION

The **HCC4031B** (extended temperature range) and **HCF4031B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package.

The **HCC/HCF4031B** is a static shift register that contains 64 D-type, master-slave flip-flop stages and one stage which is a D-type master flip-flop only (referred to as a 1/2 stage). The logic level present at the DATA input is transferred into the first stage and shifted one stage at each positive-going clock transition. Maximum clock frequencies up to 16 Megahertz (typical) can be obtained. Because fully static operation is allowed, information can be permanently stored with the clock line in either the low or high state. The **HCC/HCF4031B** has a MODE CONTROL input that, when in the high state, allows operation in the recirculating mode. The MODE CONTROL input can also be used to select between two separate data sources. Register packages can be cascaded and the clock lines driven directly for high-speed operation. Alternatively, a delayed clock output ($CL_D$) is provided that enables cascading

register packages while allowing reduced clock drive fan-out and transition-time requirements. A third cascading option makes use of the Q' output from the 1/2 stage, which is available on the next negative-going transition of the clock after the Q output occurs. This delayed output, like the delayed clock $CL_D$, is used with clocks having slow rise and fall times.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

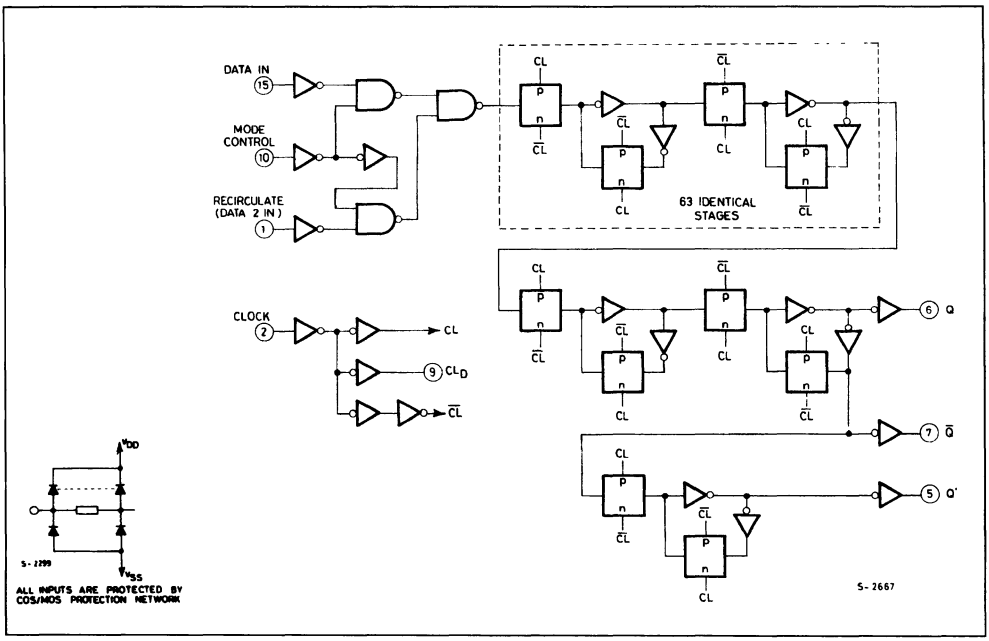
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to $V_{SS}$ pin voltage

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage · **HCC** Types<br>**HCF** Types | 3 to + 18<br>3 to + 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAM AND TRUTH TABLES




## INPUT CONTROL CIRCUIT

| Data | Recirc. | Mode | Bit Into Stage 1 |
|---|---|---|---|
| 1 | X | 0 | 1 |
| 0 | X | 0 | 0 |
| X | 1 | 1 | 1 |
| X | 0 | 1 | 0 |

## TYPICAL STAGE

| Data | CL | Data + 1 |
|---|---|---|
| 0 | ⎍ | 0 |
| 1 | ⎍ | 1 |
| X | ⎎ | NC |

1 = HIGH LEVEL

0 = LOW LEVEL
X = DON'T CARE

## OUTPUT FROM Q' (pin 5)

| Data + 64 | CL | Data + 64.5 |
|---|---|---|
| 0 | ⎎ | 0 |
| 1 | ⎎ | 1 |
| X | ⎍ | NC |

NC = NO CHANGE

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Source Current (Source) Q, $\overline{Q}$, Q $CL_D$ | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current Q | HCC Types | 0/ 5 | 0.4 | | 5 | 2.56 | | 2.04 | 4 | | 1.44 | | mA |
| | | | 0/10 | 0.5 | | 10 | 6.4 | | 5.2 | 10.4 | | 3.6 | | |
| | | | 0/15 | 1.5 | | 15 | 16.8 | | 13.6 | 27.2 | | 9.6 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 2.08 | | 1.74 | 4 | | 1.43 | | |
| | | | 0/10 | 0.5 | | 10 | 5.01 | | 4.42 | 10.4 | | 3.74 | | |
| | | | 0/15 | 1.5 | | 15 | 13.6 | | 11.56 | 27.2 | | 9.52 | | |
| $I_{OL}$ | Output Sink Current $\overline{Q}$, Q' $CL_D$ | HCC Types | 0/ 5 | 0.4 | | 5 | 0 64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is . 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5 V min. with $V_{DD}$ = 15V.

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall times = 20ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$, $t_{PLH}$, $t_{PLH}$ | Propagation Delay Time : Clock to Q, Clock to Q | | 5 | | 250 | 500 | ns |
| | | | 10 | | 110 | 220 | |
| | | | 15 | | 90 | 180 | |
| $t_{PHL}$, $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time : Clock to Q' Clock to Q | | 5 | | 190 | 380 | ns |
| | | | 10 | | 80 | 160 | |
| | | | 15 | | 65 | 130 | |
| | Clock to $CL_D$ | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_{THL}$', $t_{TLH}$ | Transition Time : (any output, except $Qt_{THL}$) | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_{THL}$ | Q, | | 5 | | 50 | 100 | ns |
| | | | 10 | | 25 | 50 | |
| | | | 15 | | 20 | 40 | |
| $t_{setup}$ | Data Setup Time | | 5 | | 30 | 60 | ns |
| | | | 10 | | 15 | 30 | |
| | | | 15 | | 10 | 20 | |
| $t_{hold}$ | Data Hold Time | | 5 | | 30 | 60 | ns |
| | | | 10 | | 15 | 30 | |
| | | | 15 | | 10 | 20 | |
| $t_W$ | Clock Pulse Width | | 5 | | 120 | 240 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $f_{max}$ | Maximum Clock Input Frequency** | | 5 | 2 | 4 | | MHz |
| | | | 10 | 5 | 10 | | |
| | | | 15 | 6 | 12 | | |
| $t_r$, $t_f$ | Clock Input Rise or Fall Time* | | 5 | | | 1000 | µs |
| | | | 10 | | | 1000 | |
| | | | 15 | | | 200 | |

* If more than one unit is cascaded in the parallel clocked application, trCL should be made less than or equal to the sum of the propagation delay at 50pF and the transmition time of the output driving stage.

* * Maximum Clock Frequency for Cascaded Units;

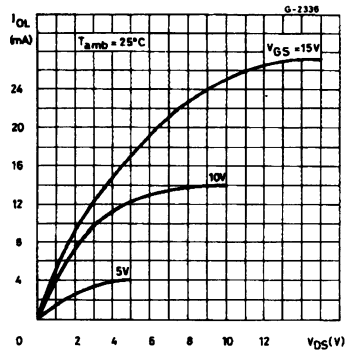
a) Using Delayed Clock Feature in Recirculation Mode

$$fmax = \frac{1}{(n\text{-}1)\ \text{CLD prop delay} + \text{Q prop delay} + \text{set-up time}}$$ where n = number of packages

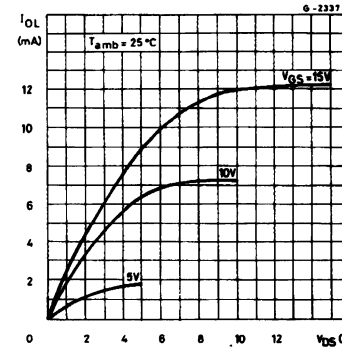
b) Not Usng Delaye Clock :

$$fmax = \frac{1}{\text{propagation delay} + \text{set-up time}}$$

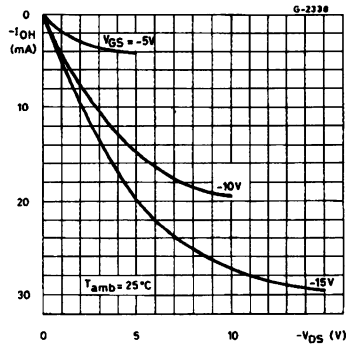
Typical Output Low (sink) Current Characteristics.



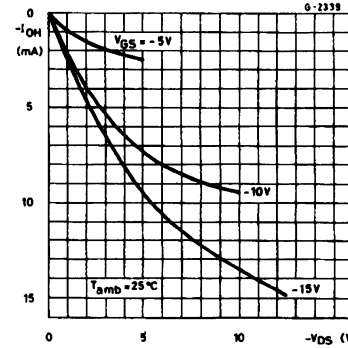

Minimum Output Low (sink) Current Characteristics.




Typical Output High (source) Current Characteristics.

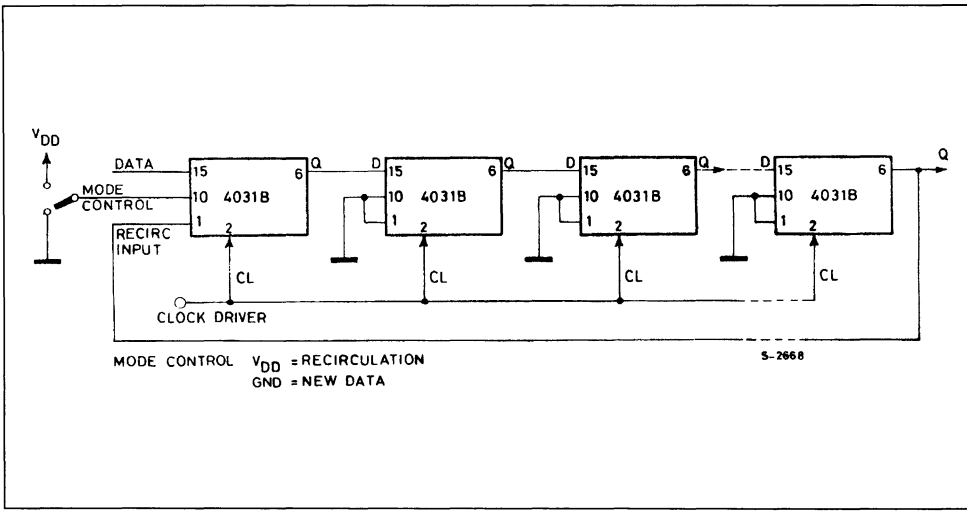



Minimum Output High (source) Current Characteristics.

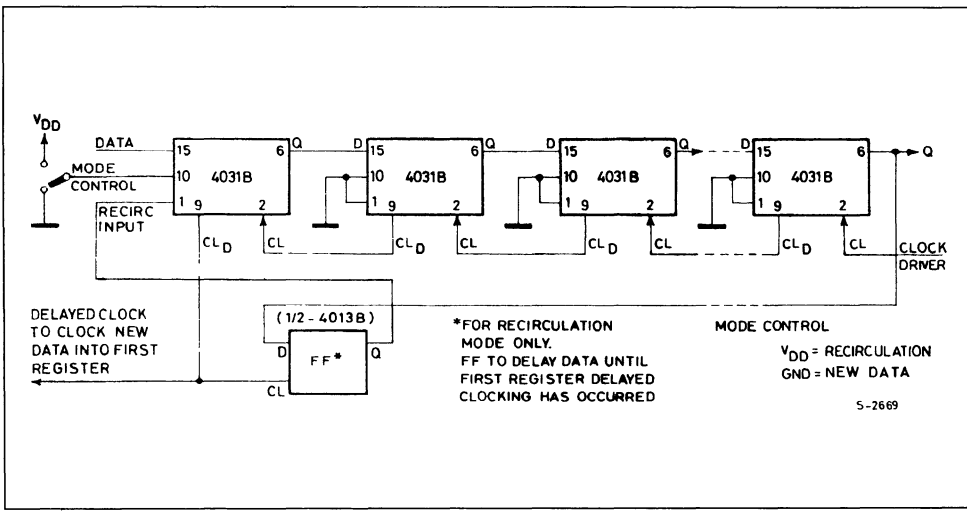


## TYPICAL APPLICATIONS

CASCADING USING DIRECT CLOCKING FOR HIGH SPEED OPERATION (SEE CLOCK RISE AND FALL TIME REQUIREMENT).

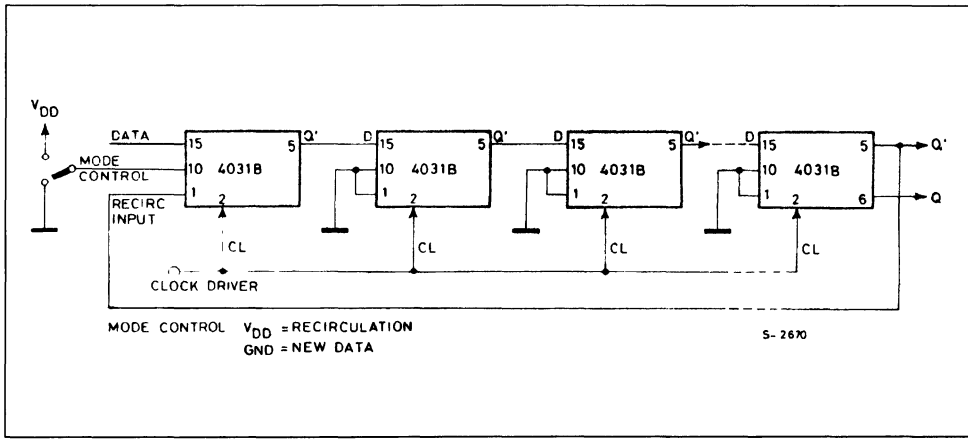



CASCADING USING DELAYED CLOCKING FOR REDUCED CLOCK DRIVE REQUIREMENTS.



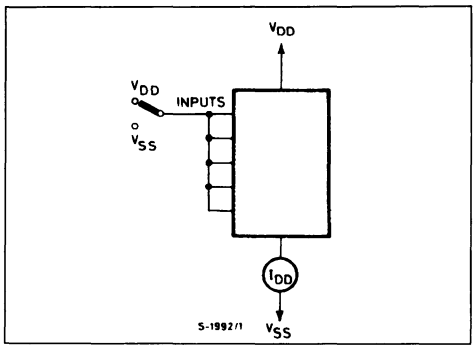
**TYPICAL APPLICATIONS** (continued)

CASCADING USING HALF- CLOCK-PULSE DELAYED DATA OUTPUT (Q') TO PERMIT USE OF SLOW RISE AND FALL TIME CLOCK INPUTS.

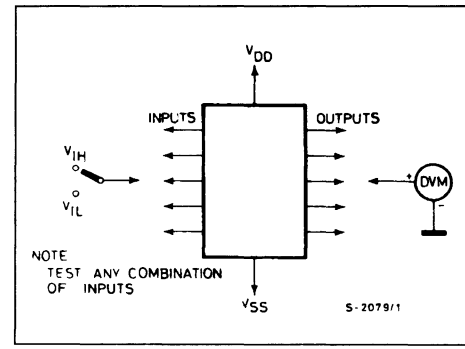



## TEST CIRCUITS

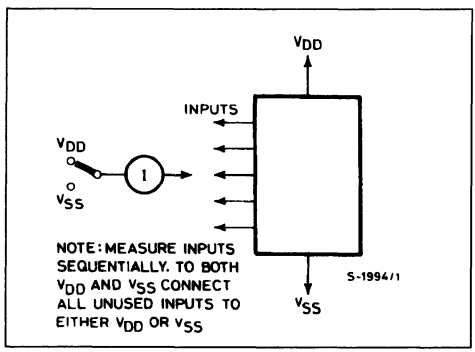
Quiescent Device Current.




Noise Immunity.




Input Leakage Current.

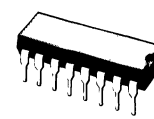


SGS-THOMSON MICROELECTRONICS

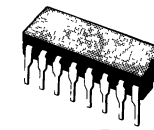
# HCC/HCF4032B
# HCC/HCF4038B

## TRIPLE SERIAL ADDERS

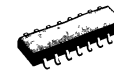
- INVERT INPUTS ON ALL ADDERS FOR SUM COMPLEMENTING APPLICATIONS
- FULLY STATIC OPERATION...DC TO 10MHz (typ.) @ $V_{DD}$ = 10V
- BUFFERED INPUTS AND OUTPUTS
- SINGLE-PHASE CLOCKING
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATING
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Package)



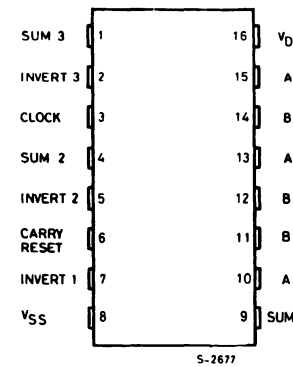
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC40XXBF HCF40XXBM1
HCF40XXBEY HCF40XXBC1

### PIN CONNECTIONS

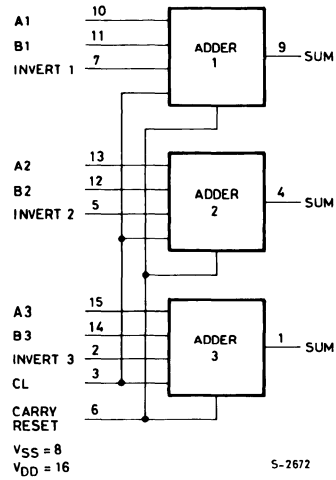



### DESCRIPTION

The **HCC/4032B/4038B** (extended temperature range) and **HCF4032B/4038B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and plastic micro package.

The **HCC/HCF4032B** and **HCC/HCF4038B** types consist of three serial adder circuits with common CLOCK and CARRY-RESET inputs. Each adder has two provisions for two serial DATA INPUT signals and an INVERT command signal. When the command signal is a logical "1", the sum is complemented. Data words enter the adder with the least significant bit first ; the sign bit trails. The output is the MOD 2 sum of the input bits plus the carry from the previous bit position. The carry is only added at the positive-going clock transition for the **HCC/HCF4032B** or at the negative-going clock for the **HCC/HCF4038B**, thus, for spike-free operation the input data transitions should occur as soon as possible after the triggering edge. The CARRY is reset to a logical "0" at the end of each word by applying a logical "1" signal to a CARRY-RESET input one-bit-position before the application of the first bit of the next word.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

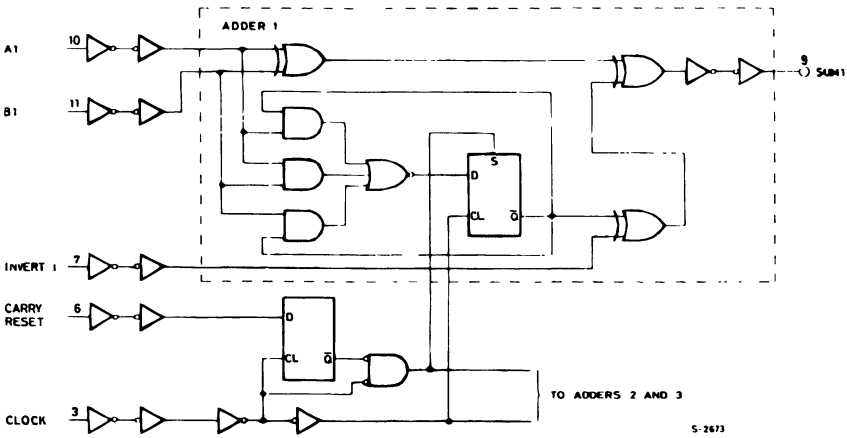
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltage values are referred to $V_{SS}$ pin voltage.

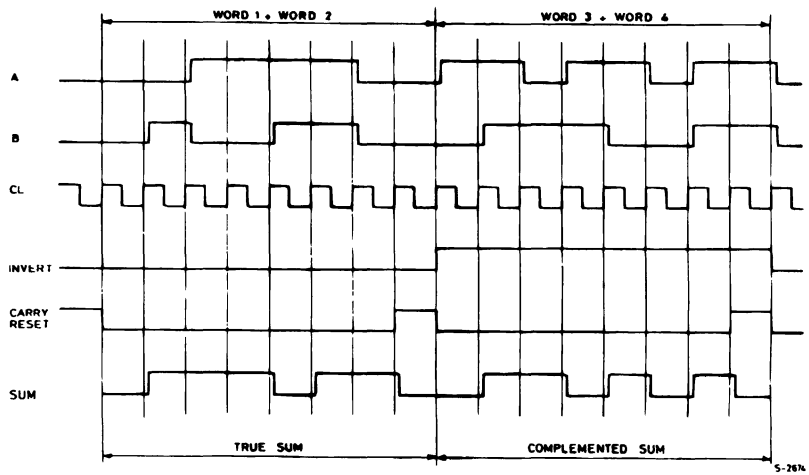
## RECOMMENDED OPERATING CONDITIONS

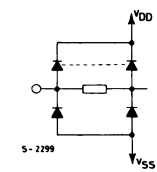
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC AND TIMING DIAGRAMS
(one of three serial adders)

**4032B**



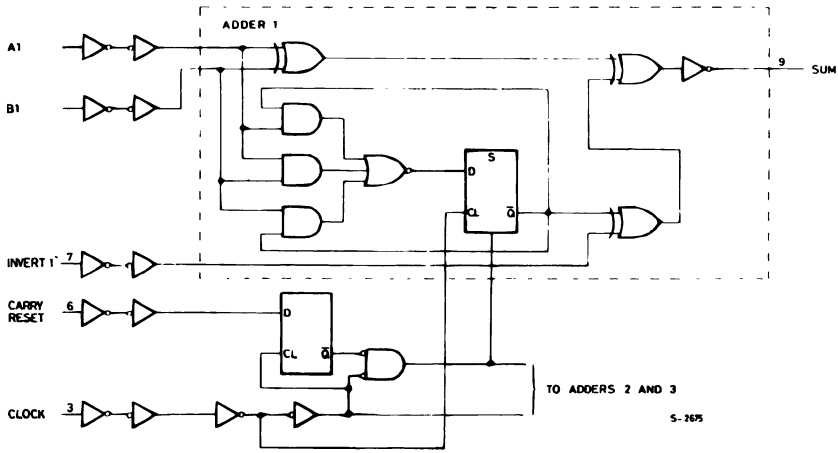



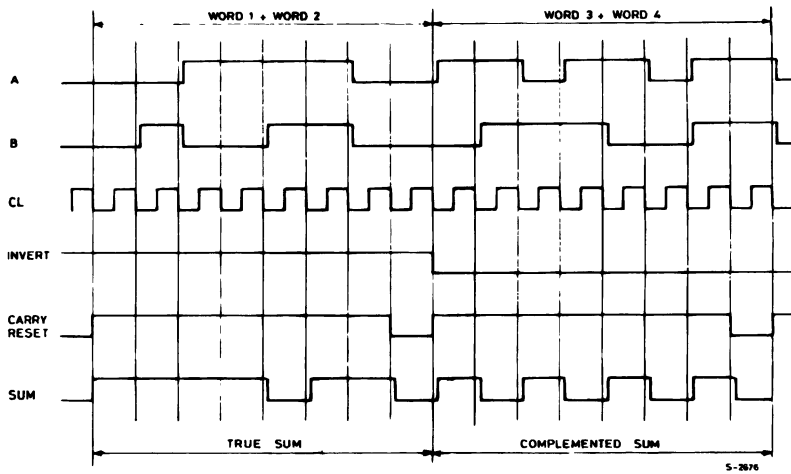

ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

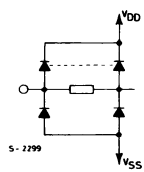
| | | | | | |
|---|---|---|---|---|---|
| WORD 1 | 0.0111100 = | + 60 | WORD 3 | 1.1011011 = | − 37 |
| WORD 2 | 0.0110010 = | + 50 | WORD 4 | 1.1001110 = | − 50 |
| | 0.1101110 = | + 110 | | 1.0101001 = | − 87 |

## LOGIC AND TIMING DIAGRAMS (continued)

### 4038B




ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

| | | | | | |
|---|---|---|---|---|---|
| WORD 1 | 1.1000011 = | −61 | WORD 3 | 0.0100100 = | +36 |
| WORD 2 | 1.1001101 = | −51 | WORD 4 | 0.0110001 = | +49 |
| | 1.0010000 = | −112 | | 0.1010101 = | +85 |

**STATIC ELECTRICAL CHARACTERISTICS** (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

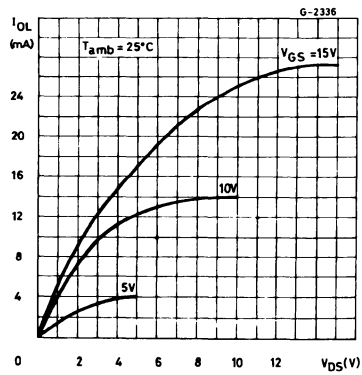
* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, all input rise and fall time = 20ns)

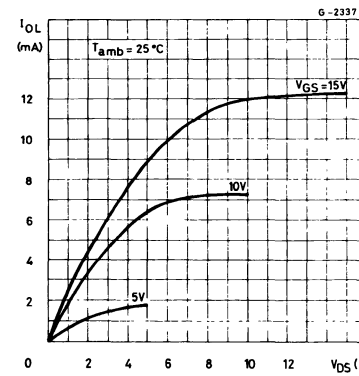
| Symbol | Parameter | Test Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time A, B, or Inverter Inputs to Sum Outputs | | 5 | | 260 | 520 | ns |
| | | | 10 | | 120 | 240 | |
| | | | 15 | | 90 | 180 | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time (clock input to sum outputs) | | 5 | | 325 | 650 | |
| | | | 10 | | 175 | 350 | |
| | | | 15 | | 150 | 300 | |
| $t_{THL}$, $t_{THL}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_{hold}$ | Data Input Hold Time (clock edge to A, B, or reset inputs) | | 5 | | 120 | 200 | ns |
| | | | 10 | | 50 | 80 | |
| | | | 15 | | 40 | 60 | |
| $f_{max}$ | Maximum Clock Input Frequency | | 5 | 2.5 | 4.5 | | MHz |
| | | | 10 | 5 | 10 | | |
| | | | 15 | 7.5 | 15 | | |
| $t_r$, $t_f$* | Clock Input Rise or Fall Time | | 5 | | | 500 | µs |
| | | | 10 | | | 500 | |
| | | | 15 | | | 500 | |

* If more than one unit is cascaded $t_r$ should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving state for the estimated capacitive load

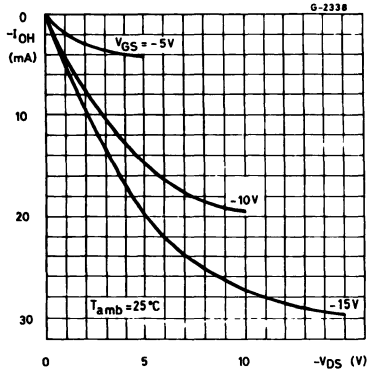
Typical Output Low (sink) Current.



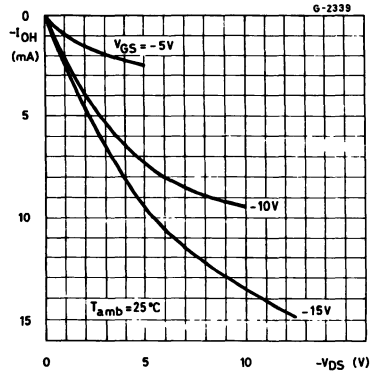

Minimum Output Low (sink) Current Characteristics.



Typical Output High (source) Current Characteristics.

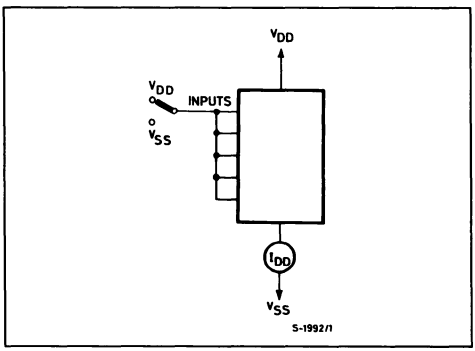



Minimum Output High (source) Current Characteristics.

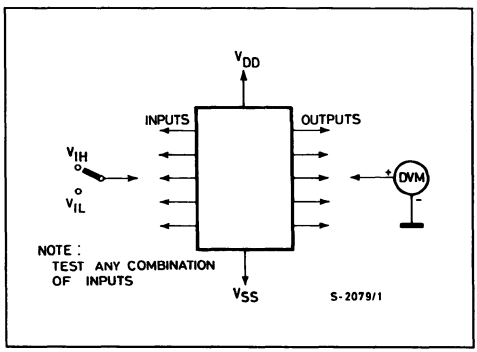



## TEST CIRCUITS

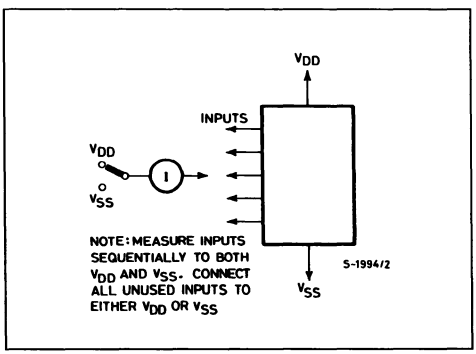
Quiescent Device Current.




Input Voltage.




Input Current.

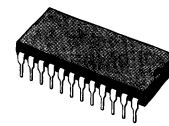


SGS-THOMSON MICROELECTRONICS

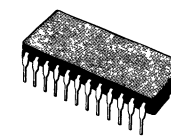
# HCC/HCF4034B

## 8-STAGE STATIC BIDIRECTIONAL PARALLEL/SERIAL INPUT/OUTPUT BUS REGISTER

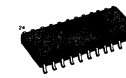
- BIDIRECTIONAL PARALLEL DATA INPUT
- PARALLEL OR SERIAL INPUTS/PARALLEL OUTPUTS
- ASYNCHRONOUS OR SYNCHRONOUS PARALLEL DATA LOADING
- PARALLEL DATA-INPUT ENABLE ON "A" DATA LINES (3-state output)
- DATA RECIRCULATION FOR REGISTER EXPANSION
- MULTIPACKAGE REGISTER EXPANSION
- FULLY STATIC OPERATIONAL DC-TO-5MHz (typ.) AT $V_{DD}$ = 10V
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

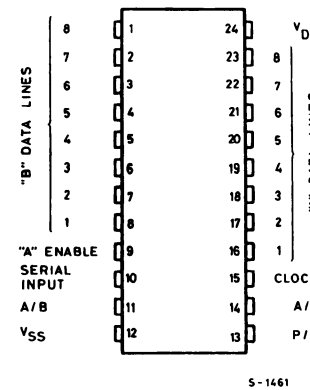


**M1**
(Micro Package)

**ORDER CODES :**

HCC4034BF HCF4034BEY
HCF4034BM1

### PIN CONNECTIONS




S-1461

### DESCRIPTION

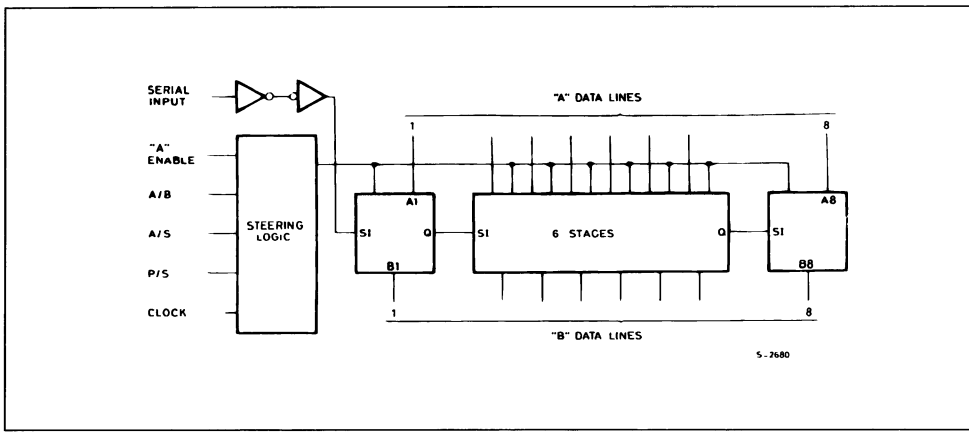
The **HCC4034B** (extended temperature range) and **HCF4034B** (intermediate temperature range) are monolithic integrated circuits, available in 24-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF4034B** is a static eight-stage parallel-or serial-input parallel-output register. It can be used to : 1) bidirectionally transfer parallel information between two buses ; 2) convert serial data to parallel form and direct the parallel data to either of two buses ; 3) store (recirculate) parallel data, or 4) accept parallel data from either of two buses and convert that data to serial form. Inputs that control the operations include a single-phase CLOCK (CL), A DATA ENABLE (AE), ASYNCHRONOUS/SYNCHRONOUS (A/S), A-BUS-TO-B-BUS/B-BUS-TO-A-BUS (A/B), and PARALLEL/ SERIAL (P/S). Data inputs include 16 bidirectional parallel data lines of which the eight A data lines are inputs (3-state outputs) and the B data lines are outputs (inputs) depending on the signal level on the A/B input. In addition, an input for SERIAL DATA is also provided. All register stages are D-type master-slave flip-flops with separate

master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave. Isolation from external noise and the effects of loading is provided by output buffering.

**PARALLEL OPERATION** – A high P/S input signal allows data transfer into the register via the parallel data lines synchronously with the positive transition of the clock provided the A/S input is low. If the A/S input is high the transfer is independent of the clock. The direction of data flow is controlled by the A/B input. When this signal is high the A data lines are inputs (and B data lines are outputs) ; a low A/B signal reverses the direction of data flow. The AE-input is an additional feature which allows many registers to feed data to a common bus. The A DATA lines are enabled only when this signal is high. Data storage through recirculation of data in each register stage is accomplished by making the A/B signal high and the AE signal low.

**SERIAL OPERATION** – A low P/S signal allows serial data to transfer into the register synchronously with the positive transition of the clock. The A/S input is internally disabled when the register is in the serial mode (asynchronous serial operation is not allowed). The serial data appears as output data on either the B lines (when A/B is high) or the A lines (when A/B is low and the AE signal is high). Register expansion can be accomplished by simply cascading **HCC/HCF4034B** packages.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | – 0 5 to + 20<br>– 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | – 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | – 55 to + 125<br>– 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | – 65 to + 150 | °C |

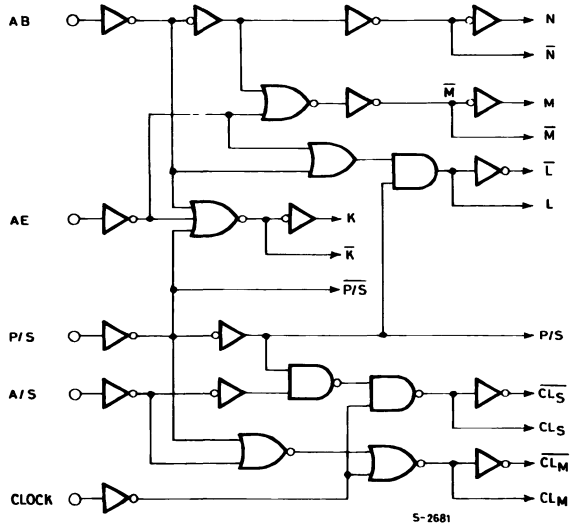
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for external periods may affect device reliability

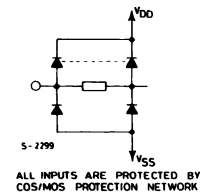
## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAMS

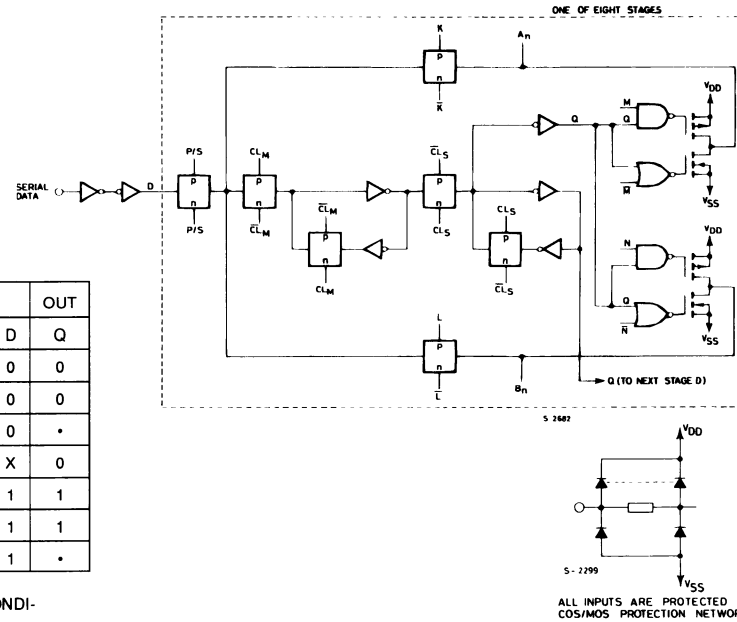
STEERING LOGIC



## LOGIC DIAGRAM AND TRUTH TABLE

REGISTER STAGE (1 of 8 stages)




| INPUTS | | | OUT |
|---|---|---|---|
| $\overline{CL}_M$ ▲ | $\overline{CL}_S$ ▲ | D | Q |
| ↓ | ↓ | 0 | 0 |
| ↑ | ↓ | 0 | 0 |
| ↓ | ↑ | 0 | • |
| ↑ | ↑ | X | 0 |
| ↓ | ↓ | 1 | 1 |
| ↑ | ↓ | 1 | 1 |
| ↓ | ↑ | 1 | • |

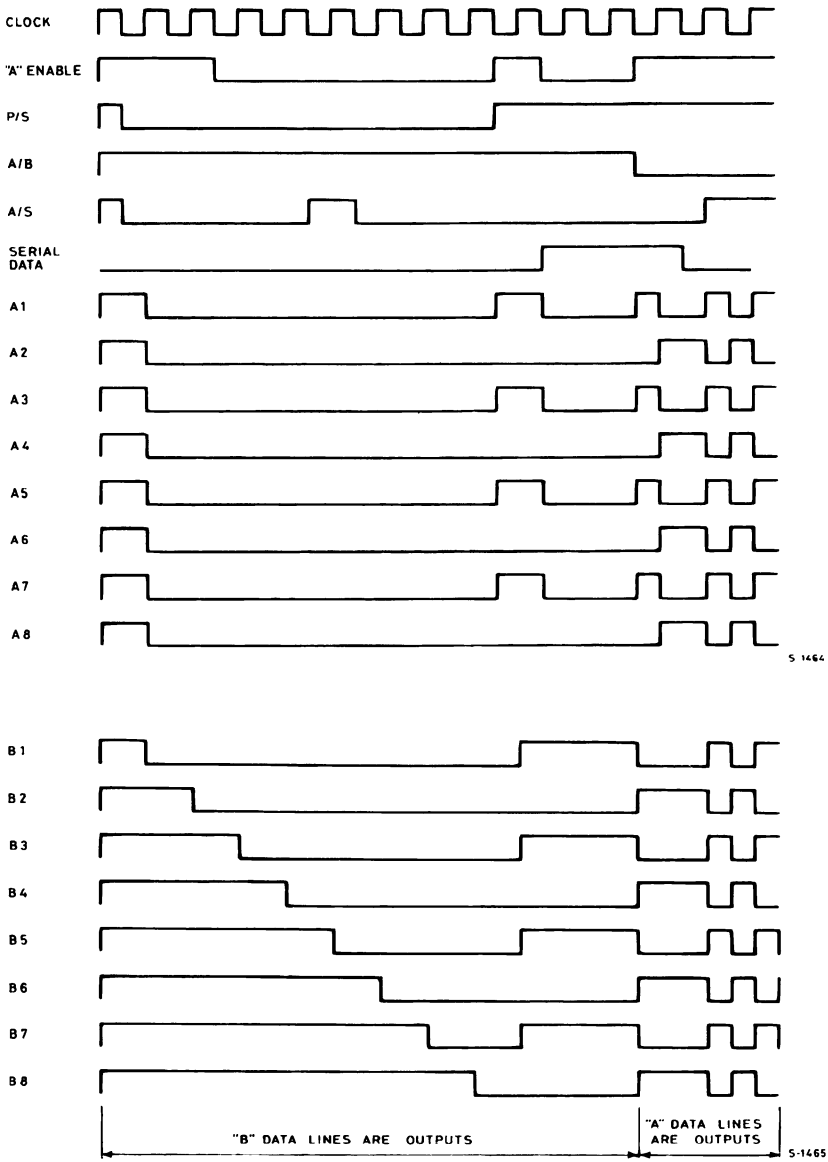
▲ = LEVEL CHANGE
• = INVALID CONDI-

## FOR REGISTER INPUT-LEVELS AND RESULTING REGISTER OPERATION

| "A" Enable | P/S | A/B | A/S | Operation* |
|---|---|---|---|---|
| 0 | 0 | 0 | X | Serial Mode ; Synch. Serial Data Input, "A" Parallel Data Outputs Disabled |
| 0 | 0 | 1 | X | Serial Mode ; Synch. Serial Data Input, "B" Parallel Data Output |
| 0 | 1 | 0 | 0 | Parallel Mode ; "B" Synch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled |
| 0 | 1 | 0 | 1 | Parallel Mode ; "B" Asynch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled |
| 0 | 1 | 1 | 0 | Parallel Mode ; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Synch. Data Recirculation |
| 0 | 1 | 1 | 1 | Parallel Mode ; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Asynch. Data Recirculation |
| 1 | 0 | 0 | X | Serial Mode ; Synch. Serial Data Input, "A" Parallel Data Output |
| 1 | 0 | 1 | X | Serial Mode ; Synch. Serial Data Input, "B" Parallel Data Output |
| 1 | 1 | 0 | 0 | Parallel Mode ; "B" Synch. Parallel Data Input, "A" Parallel Data Output |
| 1 | 1 | 0 | 1 | Parallel Mode ; "B" Asynch. Parallel Data Input, "A" Parallel Data Output |
| 1 | 1 | 1 | 0 | Parallel Mode ; "A" Synch. Parallel Data Input, "B" Parallel Data Output |
| 1 | 1 | 1 | 1 | Parallel Mode ; "A" Asynch. Parallel Data Input, "B" Parallel Data Outpu |

* Outputs change at positive transition of clock in the serial mode and when the A/S control inputs is "low" in the parallel mode

## TIMING DIAGRAM



## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Values $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0 04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4 95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9 95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0 05 | | | 0 05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0 05 | | | 0 05 | | 0 05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9 5 | | 10 | − 1.6 | | − 1 3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0 52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3 6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0 64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0 52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1 3 | | 1.1 | 2 6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $I_{OH}$ | 3-State Output Leakage Current | HCC Types | 0/18 | 0/18 | | 18 | | ± 0.4 | | $±10^{-4}$ | ± 0.4 | | ± 12 | μA |
| | | HCF Types | 0/15 | 0/15 | | 15 | | ± 1.0 | | $±10^{-4}$ | ± 1.0 | | ± 7.5 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

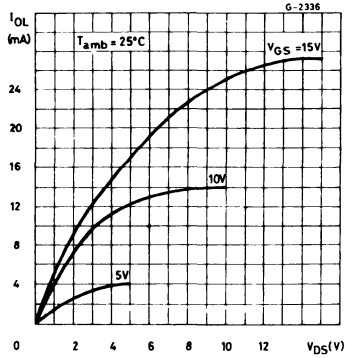
* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall times = 20ns)

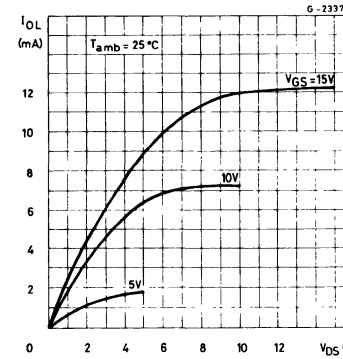
| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time : A (B) Parallel Data in to B (A) Parallel Data Out | | 5 | | 350 | 700 | ns |
| | | | 10 | | 120 | 240 | |
| | | | 15 | | 85 | 170 | |
| $t_{PLZ}$, $t_{PHZ}$ $t_{PZL}$, $t_{PZH}$ | 3-state Propagation Delay Time A/B or AE to "A" OUT | | 5 | | 200 | 400 | ns |
| | | | 10 | | 80 | 160 | |
| | | | 15 | | 60 | 120 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_{setup}$ | Data Setup Time Serial Data to Clock | | 5 | | 80 | 160 | ns |
| | | | 10 | | 30 | 60 | |
| | | | 15 | | 20 | 40 | |
| | Parallel Data to Clock | | 5 | | 25 | 50 | ns |
| | | | 10 | | 15 | 30 | |
| | | | 15 | | 10 | 20 | |
| $t_w$ | High-level Pulse Width, AE, P/S, A/S | | 5 | | 175 | 350 | ns |
| | | | 10 | | 70 | 140 | |
| | | | 15 | | 40 | 80 | |
| $f_{CL}$ | Maximum Clock Frequency | | 5 | 2 | 4 | | MHz |
| | | | 10 | 5 | 10 | | |
| | | | 15 | 7 | 14 | | |
| $t_W$ | Clock Pulse Width | | 5 | | 125 | 250 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 35 | 70 | |
| $t_r$, $t_f$* | Clock Input Rise or Fall Time | | 5,10,15 | | | 15 | µs |

* If more than one unit is cascaded. $t_r$ should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

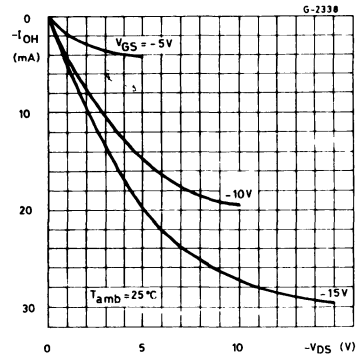
Typical Output Low (sink) Current Characteristics.



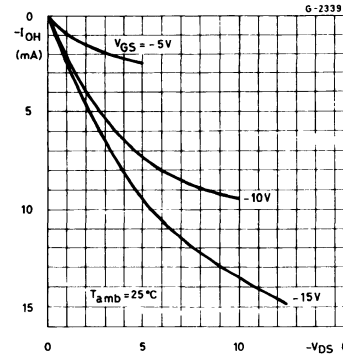

Minimum Output Low (sink) Current Characteristics.




Typical Output High (source) Current Characteristics.

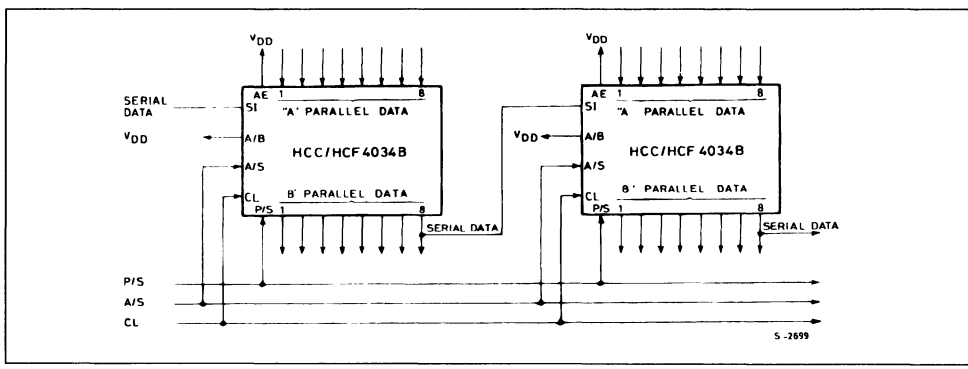



Minimum Output High (source) Current Characteristics.



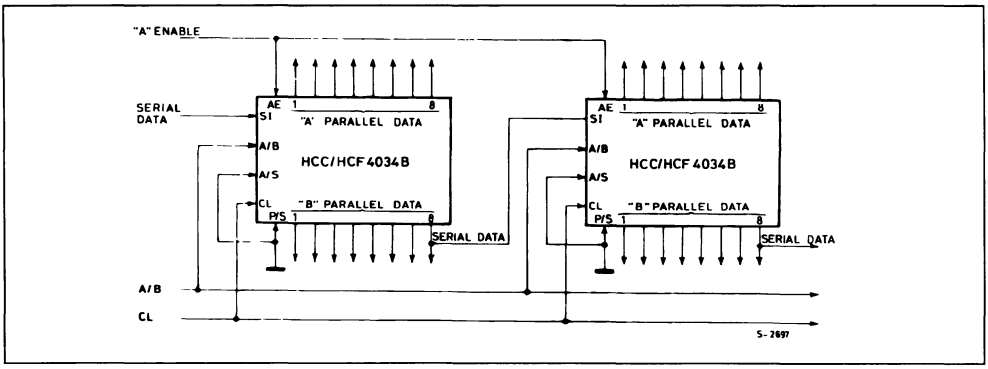

## TYPICAL APPLICATIONS

16-BIT PARALLEL IN/PARALLEL OUT PARALLEL IN/SERIAL OUT, SERIAL IN/PARALLEL OUT, SERIAL IN/SERIAL OUT REGISTER.

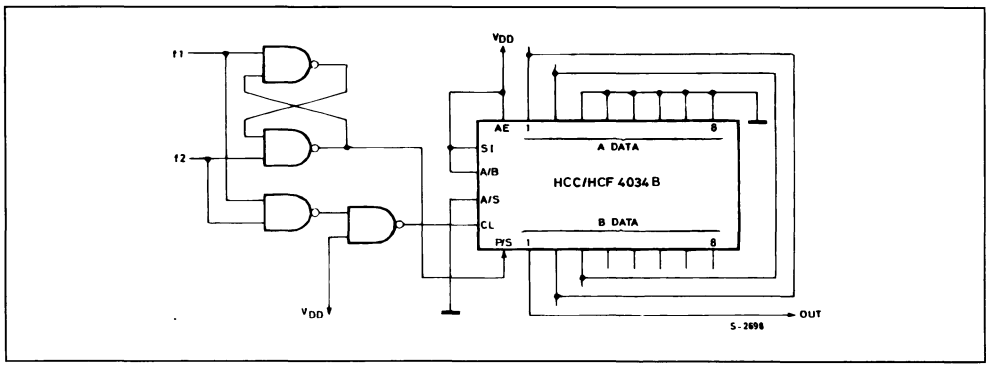


**TYPICAL APPLICATIONS** (continued)

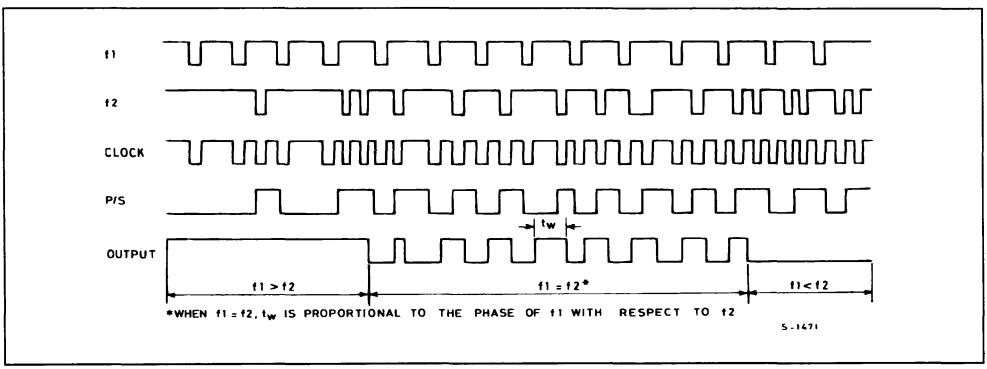
16-BIT SERIAL IN/GATED PARALLEL OUT REGISTER




FREQUENCY AND PHASE COMPARATOR.

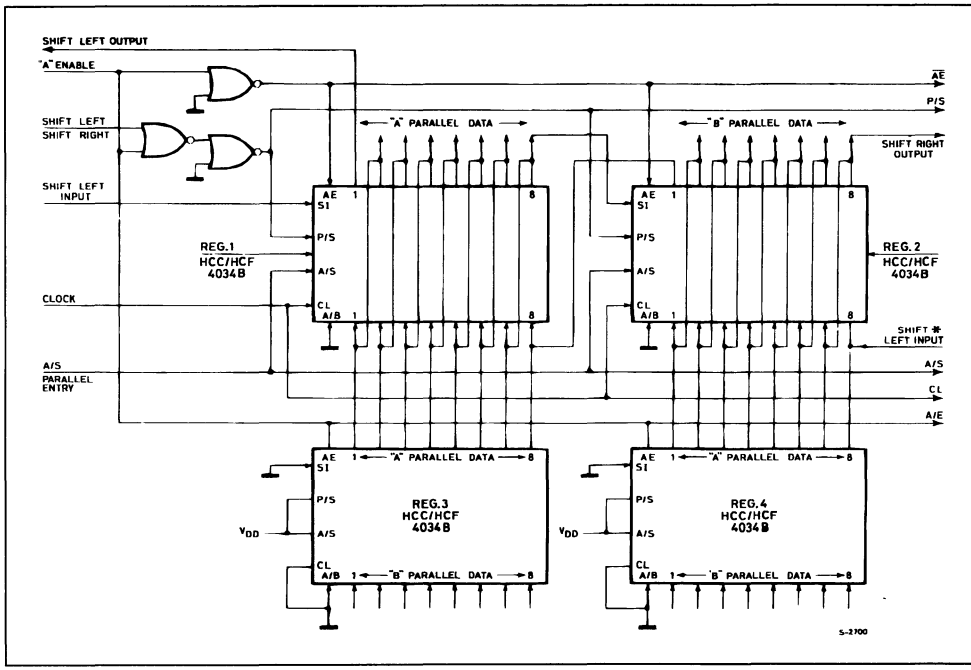



TIMING DIAGRAM



## TYPICAL APPLICATIONS (continued)

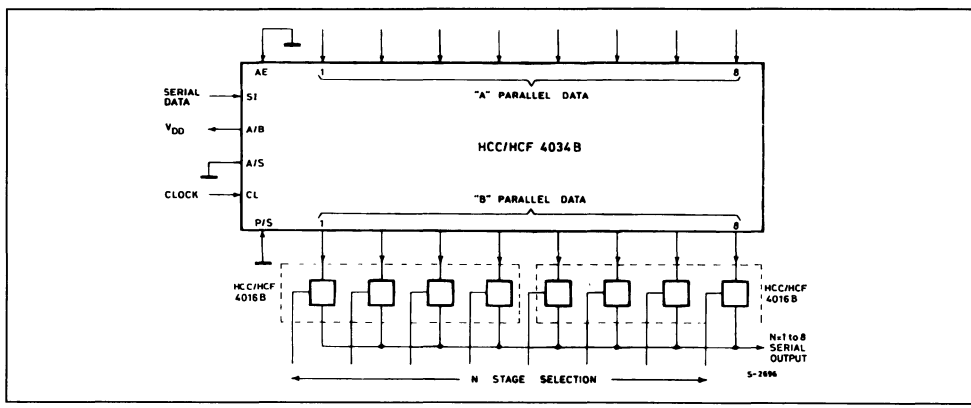
SHIFT RIGHT/SHIFT LEFT WITH PARALLEL INPUTS




A "High" ("Low") on the Shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines on Reg. 1 and 2 and enables the "A" data lines on registers 3 and 4 and allows parallel data into registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading. When parallel inputs are not used Reg. 3 and 4 and associated logic are not required.

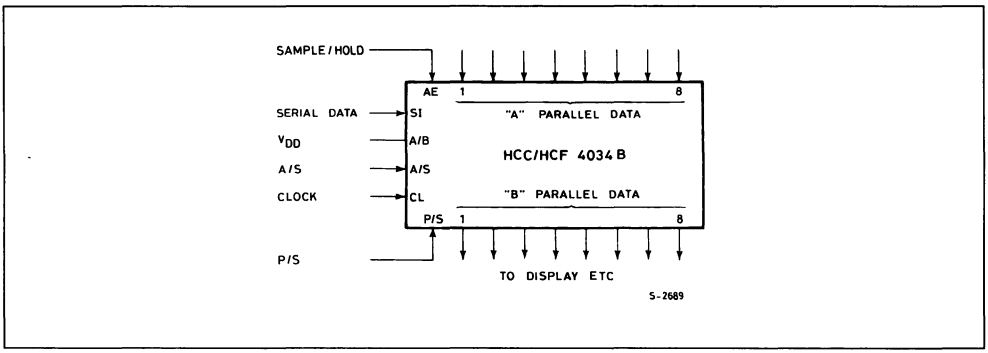
* Shift Left input must be disabled during parallel entry.

N-STAGE REGISTER WITH FIXED SERIAL OUTPUT LINE

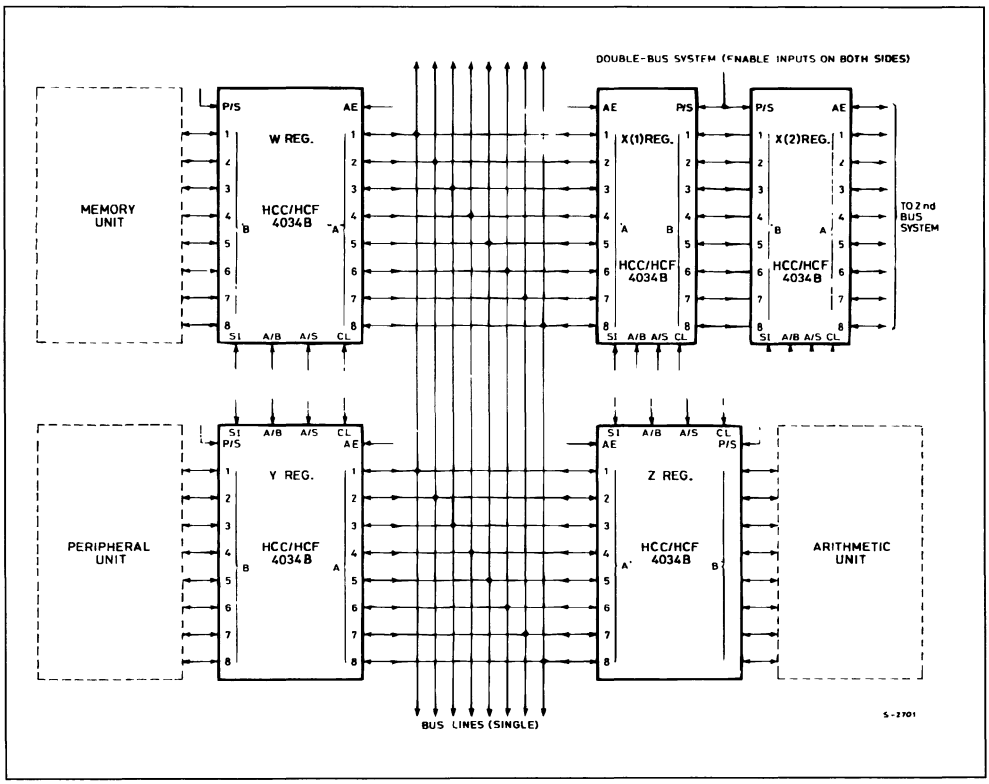


**TYPICAL APPLICATIONS** (continued)

SAMPLE AND HOLD REGISTER-SERIAL/PARALLEL IN-PARALLEL OUT



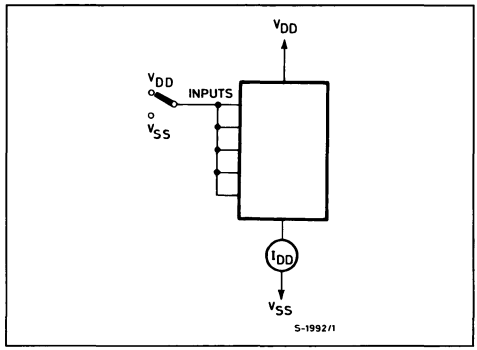

SINGLE-AND DOUBLE-BUS SYSTEMS



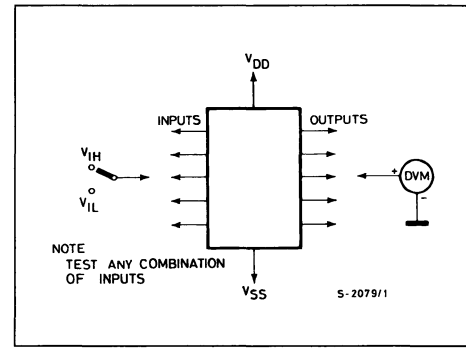

The "A" enable (AE) and A/B signals control all combinations of transfer between the registers and bus systems

## TEST CIRCUITS

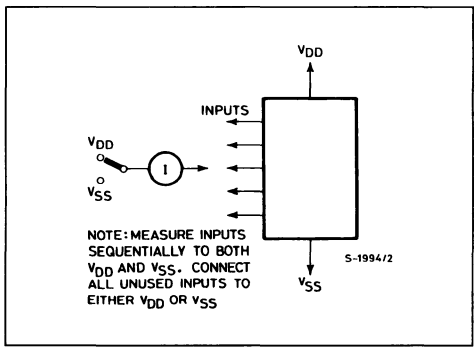
Quiescent Device Current.




Noise Immunity.




Input Leakage Current.

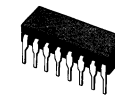


# 4-STAGE PARALLEL IN/PARALLEL OUT SHIFT REGISTER

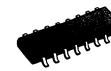
- 4-STAGE CLOCKED SHIFT OPERATION
- SYNCHRONOUS PARALLEL ENTRY ON ALL 4 STAGES
- $J\overline{K}$ INPUTS ON FIRST STAGE
- ASYNCHRONOUS TRUE/COMPLEMENT CONTROL ON ALL OUTPUTS
- STATIC FLIP-FLOP OPERATION ; MASTER-SLAVE CONFIGURATION
- BUFFERED INPUTS AND OUTPUTS
- HIGH SPEED 12MHz (typ.) AT $V_{DD}$ = 10V
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURR 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

Whith $J\overline{K}$ inputs connected together, the first stage becomes a D flip-flop. An asynchronous common RESET is also provided.

**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)



**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

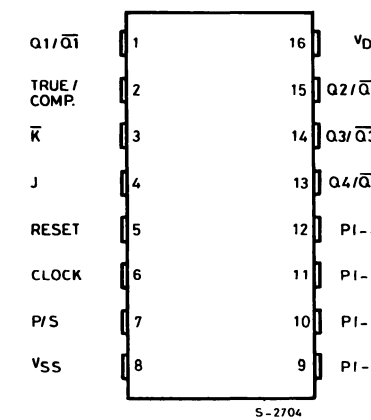
**ORDER CODES :**

HCC4035BF HCF4035BM1
HCF4035BEY HCF4035BC1

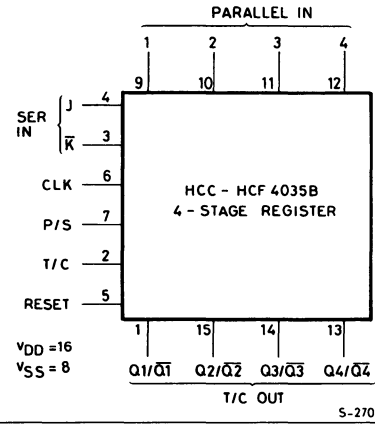
## DESCRIPTION

The **HCC4035B** (extended temperature range) and **HCF4035B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF4035B** is a four-stage clocked signal serial register with provision for synchronous PARALLEL inputs to each stage and SERIAL inputs to the first stage via $J\overline{K}$ logic. Register stages 2, 3, and 4 are coupled in a serial D flip-flop configuration when the register is in the serial mode (PARALLEL/SERIAL control low). Parallel entry into each register stage is permitted when the PARALLEL/SERIAL control is high. In the parallel or serial mode information is transferred on positive clock transitions. When the TRUE/COMPLEMENT control is high, the true contents of the register are available at the output terminals. When the TRUE/COMPLEMENT control is low, the outputs are the complements of the data in the register. The TRUE/COMPLEMENT control functions asynchronously with respect to the CLOCK signal. $J\overline{K}$ input logic is provided on the first stage SERIAL input to minimize logic requirements particularly in counting and sequence-generation applications.

**PIN CONNECTIONS**



## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

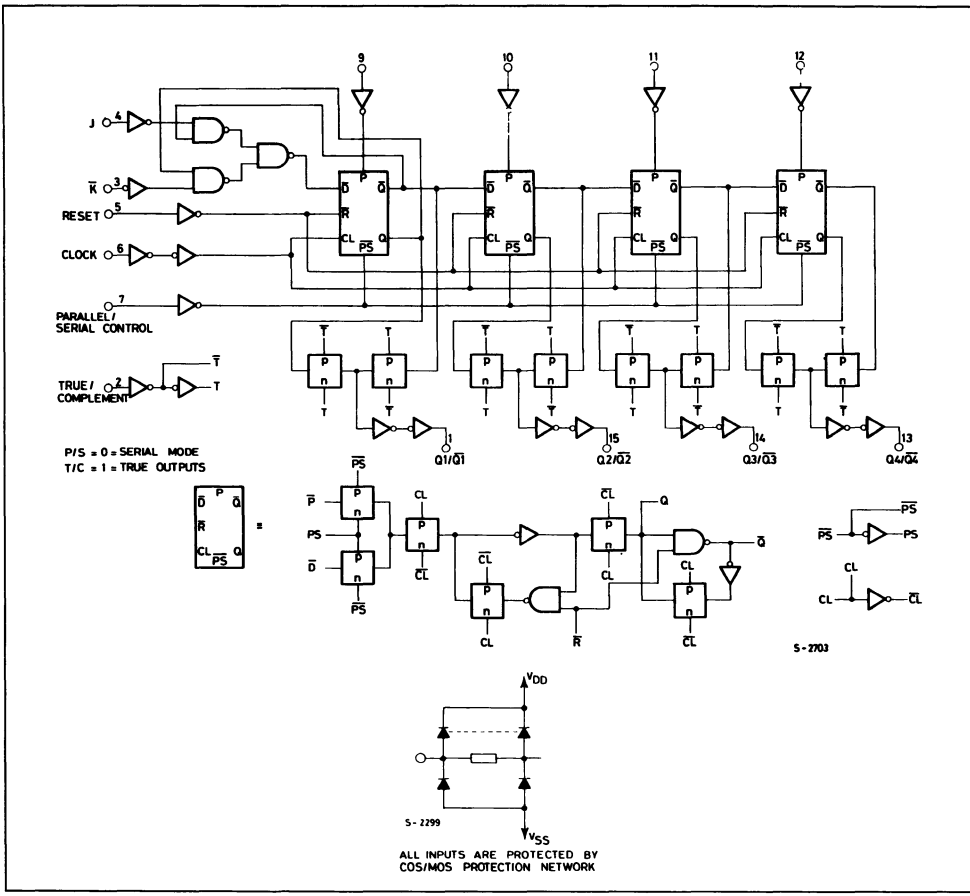
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage: **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |

## LOGIC DIAGRAM




## TRUTH TABLE

FIRST STAGE

| Clock (ø) | $t_{n-1}$ (inputs) | | | | $t_n$ (outputs) |
|---|---|---|---|---|---|
| | J | $\overline{K}$ | R | $Q_{n-1}$ | $Q_n$ |
| ⎍⎍ | 0 | X | 0 | 0 | 0 |
| ⎍⎍ | 1 | X | 0 | 0 | 1 |
| ⎍⎍ | X | 0 | 0 | 1 | 0 |
| ⎍⎍ | 1 | 0 | 0 | $Q_{n-1}$ | $\overline{Q_{n-1}}$ Toggle Mode |
| ⎍⎍ | X | 1 | 0 | 1 | 1 |
| ⎍⎍ | X | X | 0 | $Q_{n-1}$ | $Q_{n-1}$ |
| X | X | X | 1 | X | 0 |

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

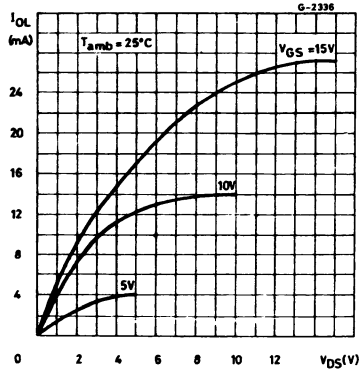
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.4 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input leakage Curent | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device . + 85°C for **HCF** device
The Noise Margin for both "1" and "0" level is : 1V min with $V_{DD}$ = 5 V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.

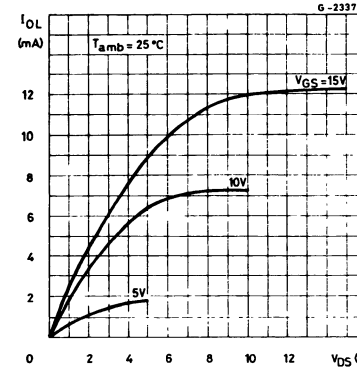
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ = 0.3%/°C, all input rise and fall time = 20ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| **CLOCKED OPERATION** | | | | | | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time | | 5 | | 250 | 500 | ns |
| | | | 10 | | 100 | 200 | |
| | | | 15 | | 75 | 150 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $f_{CL}$ | Maximum Clock Input Frequency | | 5 | 2 | 4 | | MHz |
| | | | 10 | 6 | 12 | | |
| | | | 15 | 8 | 16 | | |
| $t_W$ | Clock Pulse Width | | 5 | | 100 | 200 | ns |
| | | | 10 | | 45 | 90 | |
| | | | 15 | | 30 | 60 | |
| $t_r$, $t_f$ | Clock Input Rise or Fall Time | | 5 | | 15 | | µs |
| | | | 10 | | 15 | | |
| | | | 15 | | 15 | | |
| $t_{setup}$ | Data Setup Time J/K Lines | | 5 | | 110 | 220 | ns |
| | | | 10 | | 40 | 80 | |
| | | | 15 | | 30 | 60 | |
| $t_{setup}$ | Data Setup Time Parallel-In-Lines | | 5 | | 70 | 140 | ns |
| | | | 10 | | 25 | 50 | |
| | | | 15 | | 20 | 40 | |
| **RESET OPERATION** | | | | | | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time | | 5 | | 230 | 460 | ns |
| | | | 10 | | 100 | 200 | |
| | | | 15 | | 80 | 160 | |
| $t_W$ | Reset Pulse Width | | 5 | | 125 | 250 | ns |
| | | | 10 | | 55 | 110 | |
| | | | 15 | | 40 | 40 | |

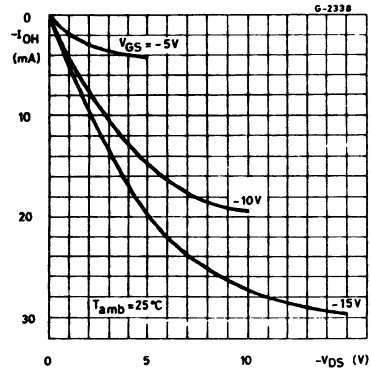
Typical Output Low (sink) Current Characteristics.



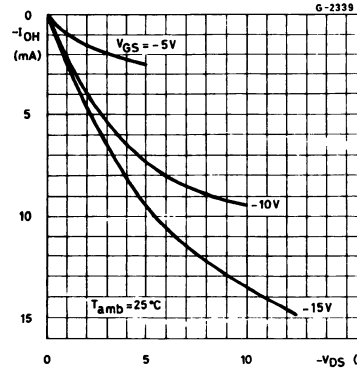

Minimum Output Low (sink) Current Characteristics.




Typical Output High (source) Current Characteristics.

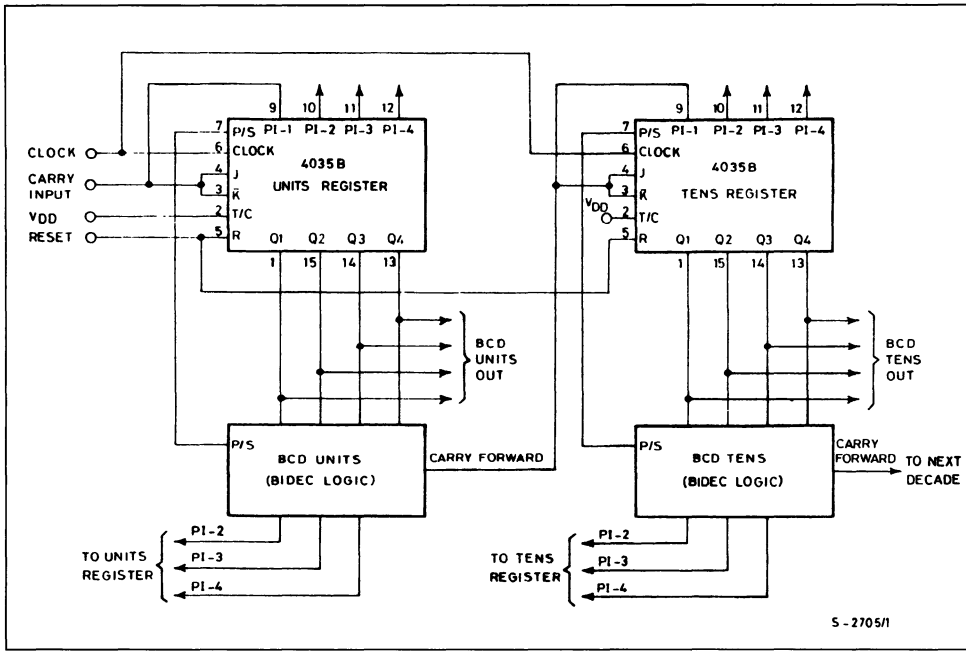



Minimum Output High (source) Current Characteristics.



## TYPICAL APPLICATIONS

BINARY-TO-BCD CONVERTER

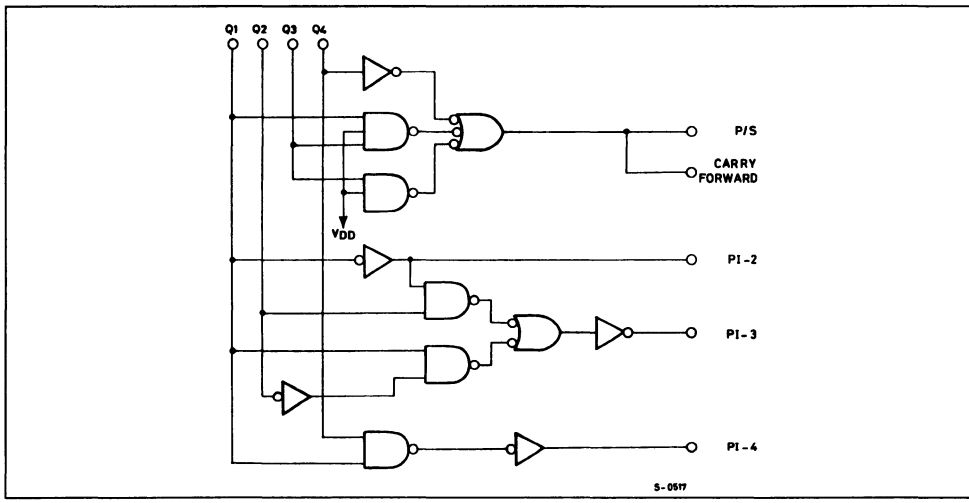



EXAMPLE OF BINARY-TO-BCD CONVERSION

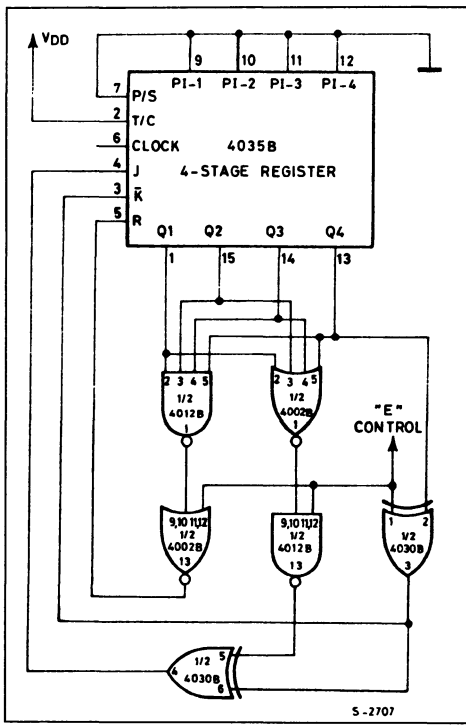
| | | | | | | | | Units Register | | | | Tens Register | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 1 | 2 | 4 | 8 | 1 | 2 | 4 | 8 |
| | LSB | | | | | MSB | | | | | | | | | |
| 58 = | 0 | 1 | 0 | 1 | 1 | 1 | | | | | | | | | |
| Shift | | | | | | | | | | | | | | | |
| Shift | | | | | | | | | | | | | | | |
| | | | 0 | 1 | 0 | 1 | 1 | 1 | | | | | | | |
| Shift | | | | | | | | | | | | | | | |
| | | | | 0 | 1 | 0 | 1 | 1 | 1 | | | | | | |
| Add * 3 to Unit Decade & Shift | | | | | | | | | 1 | 1 | | | | | |
| | | | | | 0 | 1 | 0 | 0 | 1 | 0 | 1 | | | | |
| Shift | | | | | | | | | | | | | | | |
| | | | | | | | 0 | 1 | 0 | 0 | 1 | 0 | 1 | | |
| Add * 3 Units Decade & Shift | | | | | | | | | 1 | 1 | | | | | |
| | | | | | | | | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| * From Left to Right | | | | | | | | | | 8 | | | | 5 | |

## TYPICAL APPLICATIONS

BIDEC LOGIC




DOUBLE SEQUENCE GENERATOR



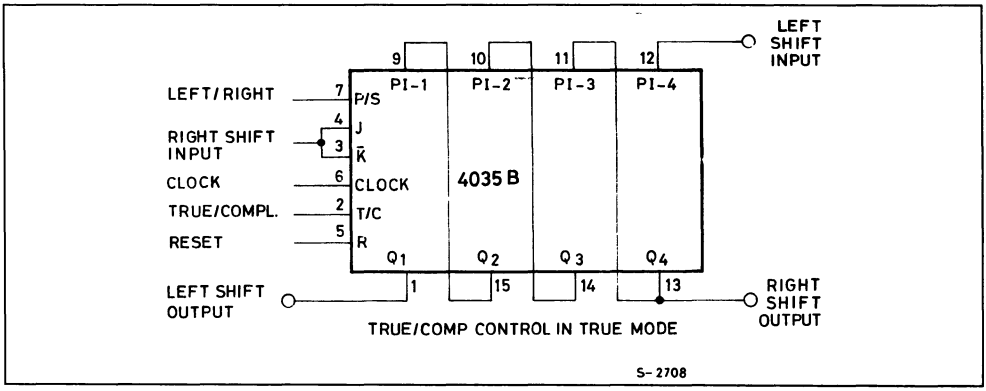

STATE SEQUENCES

Using a control line (E) two different state sequences can be generated. For example, suppose the following two sequences are desired on command (control line E).

| | Control = E = 0 | | | | | 1 | | | |
|---|---|---|---|---|---|---|---|---|---|
| | $Q_1$ A | $Q_2$ B | $Q_3$ C | $Q_4$ D | | $Q_1$ A | $Q_2$ B | $Q_3$ C | $Q_4$ D |
| 0 | 0 | 0 | 0 | 0 | 15 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 14 | 0 | 0 | 1 | 1 |
| 2 | 0 | 1 | 0 | 0 | 13 | 1 | 0 | 1 | 1 |
| 5 | 1 | 0 | 1 | 0 | 10 | 0 | 1 | 0 | 1 |
| 10 | 0 | 1 | 0 | 1 | 5 | 1 | 0 | 1 | 0 |
| 4 | 0 | 0 | 1 | 0 | 11 | 1 | 1 | 0 | 1 |
| 9 | 1 | 0 | 0 | 1 | 6 | 0 | 1 | 1 | 0 |
| 3 | 1 | 1 | 0 | 0 | 12 | 0 | 0 | 1 | 1 |
| 6 | 0 | 1 | 1 | 0 | 9 | 1 | 0 | 0 | 1 |
| 13 | 1 | 0 | 1 | 1 | 2 | 0 | 1 | 0 | 0 |
| 11 | 1 | 1 | 0 | 1 | 4 | 0 | 0 | 1 | 0 |
| 7 | 1 | 1 | 1 | 0 | 8 | 0 | 0 | 0 | 1 |
| 14 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 12 | 0 | 0 | 1 | 1 | 3 | 1 | 1 | 0 | 0 |
| 8 | 0 | 0 | 0 | 1 | 7 | 1 | 1 | 1 | 0 |

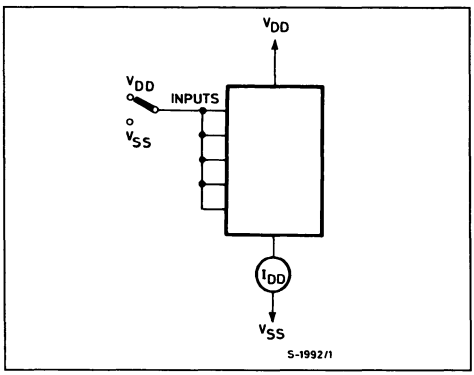
## TYPICAL APPLICATIONS

SHIFT LEFT/SHIFT RIGHT REGISTER

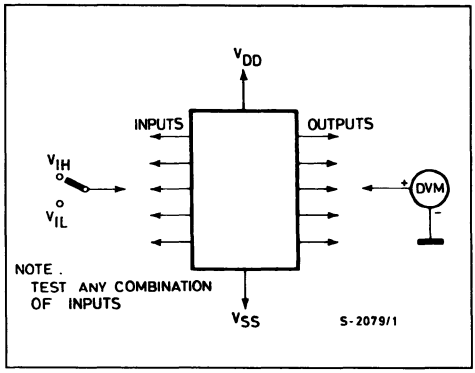



## TEST CIRCUITS

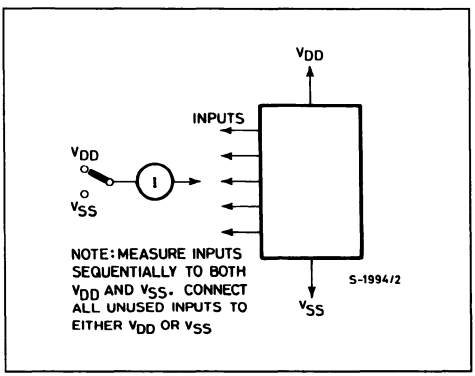
Quiescent Device Current.




Input Voltage.

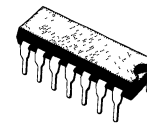



Input Current.

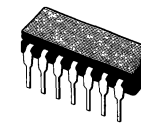


# QUAD TRUE/COMPLEMENT BUFFER

- BALANCED SINK AND SOURCE CURRENT ; APPROXIMATELY 4 TIMES STANDARD "B" DRIVE
- EQUALIZED DELAY TO TRUE AND COMPLEMENT OUTPUTS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100 % TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

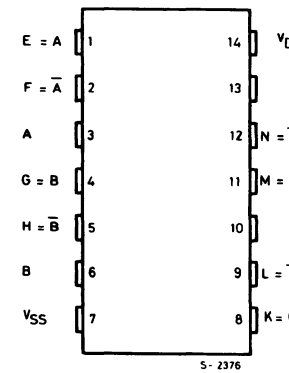
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4041BF HCF4041BM1
HCF4041BEY HCF4041BC1

## PIN CONNECTIONS

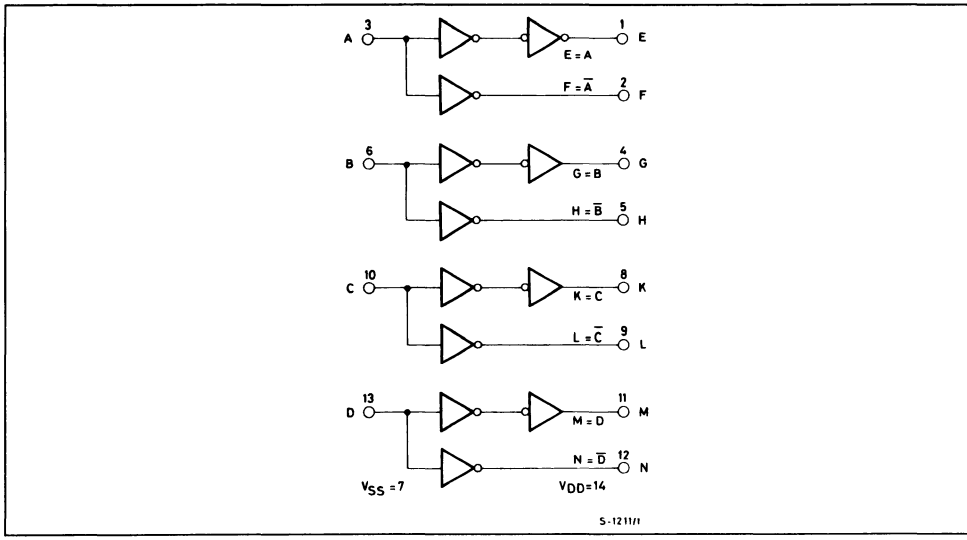



## DESCRIPTION

The **HCC4041UB** (extended temperature range) and **HCF4041UB** (intermediate temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and plastic micro package.

The **HCC/HCF4041UB** types are quad true/complement buffers consisting of n- and p-channel units having low channel resistance and high current (sourcing and sinking) capability. The **HCC/HCF4041UB** is intended for use as a buffer, line driver, or COS/MOS-to-TTL driver. It can be used as an ultra-low power resistor-network driver for A/D and D/A conversion, as a transmission-line driver, and in other applications where high noise immunity and low-power dissipation are primary design requirements.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

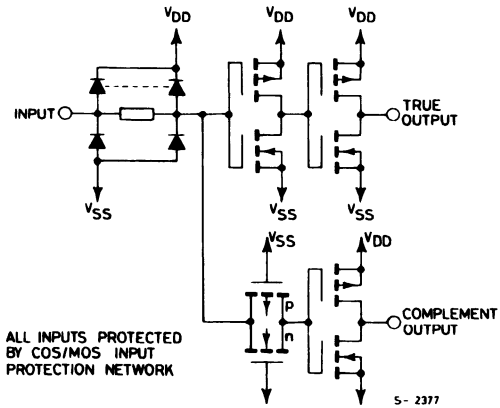
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to + 18<br>3 to + 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## SCHEMATIC DIAGRAM




## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 1 | | 0.02 | 1 | | 30 | μA |
| | | | 0/10 | | | 10 | | 2 | | 0.02 | 2 | | 60 | |
| | | | 0/15 | | | 15 | | 4 | | 0.02 | 4 | | 120 | |
| | | | 0/20 | | | 20 | | 20 | | 0.04 | 20 | | 600 | |
| | | HCF Types | 0/ 5 | | | 5 | | 4 | | 0.02 | 4 | | 30 | |
| | | | 0/10 | | | 10 | | 8 | | 0.02 | 8 | | 60 | |
| | | | 0/15 | | | 15 | | 16 | | 0.02 | 16 | | 120 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 4 | | 4 | | | 4 | | V |
| | | | | 1/9 | < 1 | 10 | 8 | | 8 | | | 8 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 12.5 | | 12.5 | | | 12.5 | | |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.

## STATIC ELECTRICAL CHARACTERISTICS (continued)

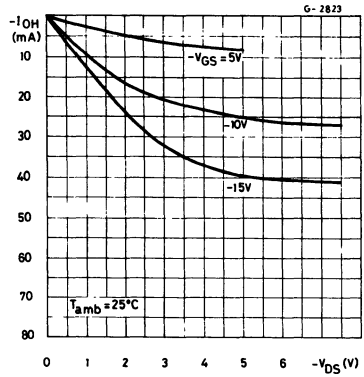
| Symbol | Parameter | | Test Conditions | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1 | | | 1 | | 1 | V |
| | | | | 9/1 | < 1 | 10 | | 2 | | | 2 | | 2 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 2.5 | | | 2.5 | | 2.5 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 8.4 | | − 6.4 | − 12.8 | | − 4.6 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 2.1 | | − 1.6 | − 3.2 | | − 1.2 | | |
| | | | 0/10 | 9.5 | | 10 | − 6.25 | | − 5 | − 10 | | − 3.5 | | |
| | | | 0/15 | 13.5 | | 15 | − 24 | | − 19 | − 38 | | − 13 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 6.8 | | − 5.44 | − 12.8 | | − 4.08 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 1.7 | | − 1.36 | − 3.2 | | − 1.02 | | |
| | | | 0/10 | 9.5 | | 10 | − 5.31 | | − 4.25 | − 10 | | − 3.18 | | |
| | | | 0/15 | 13.5 | | 15 | −20.18 | | −16.15 | −38 | | −12.11 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 2.1 | | 1.6 | 3.2 | | 1.2 | | |
| | | | 0/10 | 0.5 | | 10 | 6.25 | | 5 | 10 | | 3.5 | | |
| | | | 0/15 | 1.5 | | 15 | 24 | | 19 | 38 | | 13 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 1.7 | | 1.36 | 3.2 | | 1.02 | | |
| | | | 0/10 | 0.5 | | 10 | 5.31 | | 4.25 | 10 | | 3.18 | | |
| | | | 0/15 | 1.5 | | 15 | 20.13 | | 16.15 | 38 | | 12.11 | | |
| $I_{IH}$, $I_{IL}$ | Input leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 15 | 22.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device − 40°C for **HCF** device
* $T_{High}$ = + 125°C for **HCC** device · + 85°C for **HCF** device
The Noise Margin for both "1" and "0" level is · 1V min with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2 5V min with $V_{DD}$ = 15V

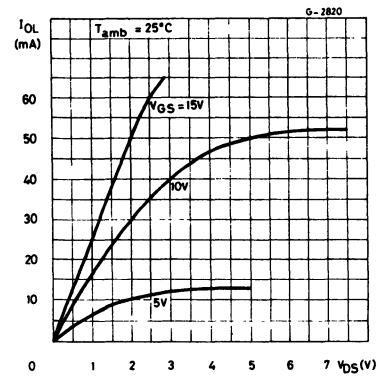
## DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3 %/°C, all input rise and fall times = 20ns)

| Symbol | Parameter | Test Conditions | Value | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time | | 5 | | 60 | 120 | ns |
| | | | 10 | | 35 | 70 | |
| | | | 15 | | 25 | 50 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | 5 | | 40 | 80 | ns |
| | | | 10 | | 20 | 40 | |
| | | | 15 | | 15 | 30 | |

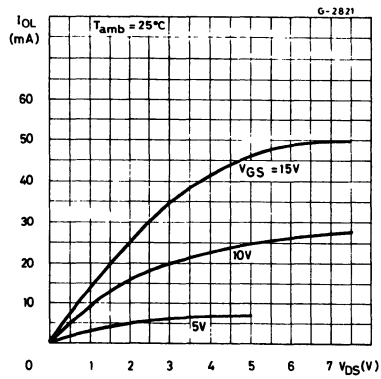
Minimum Output High (source) Current Characteristics.



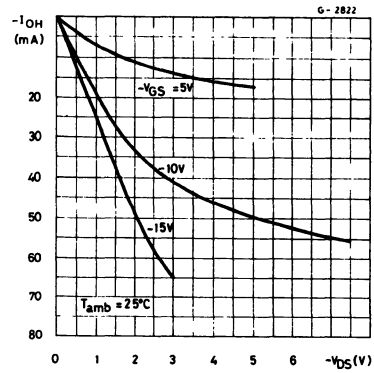

Typical Output Low (sink) Current.



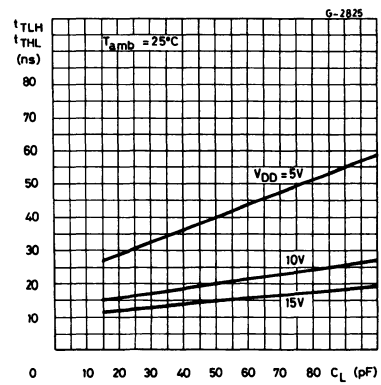

Minimum Output Low (sink) Current Characteristics.



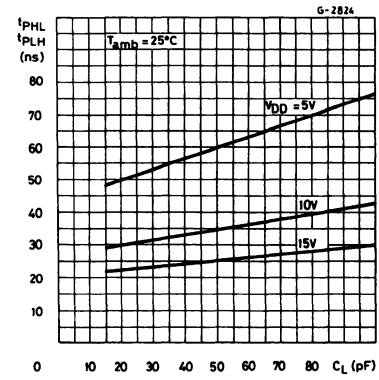

Typical Output High (source) Current Characteristics.



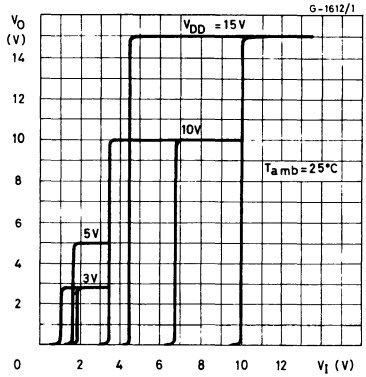

Typical Transition Time vs. Load Capacitance.

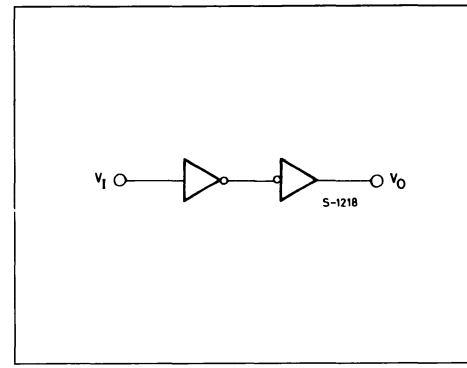



Typical Propagation Delay Time vs. Load Capacitance.

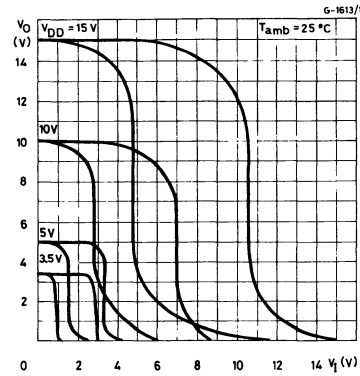


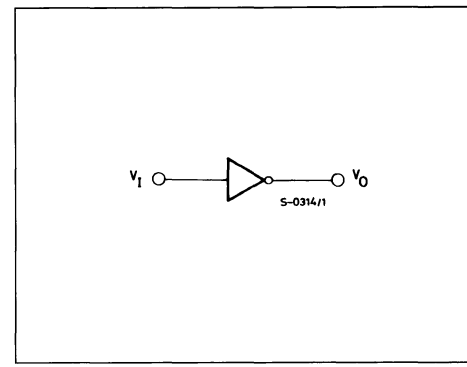
Minimum and Maximum Transfer Characteristics-true Output-and Test Circuit.



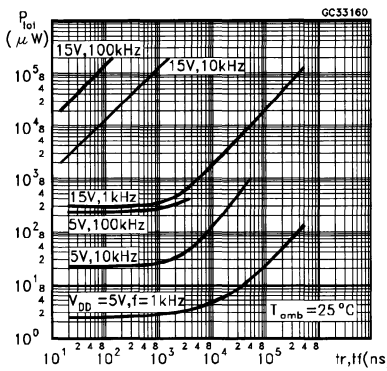




Minimum Maximum Transfer Characteristics Complement Output-and Test Circuit.

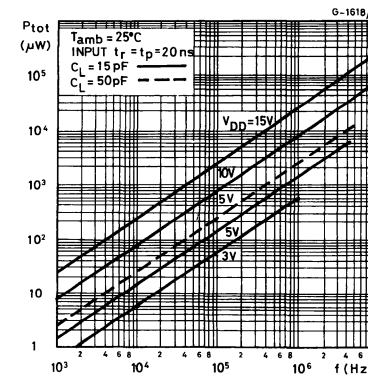



Typical Power Dissipation vs. Input Rise and Fall Time per Output Pair.

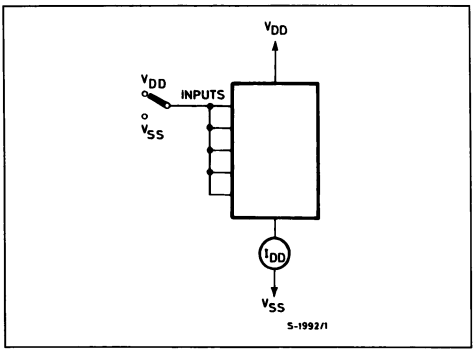



Typical Power Dissipation vs. Frequency per Output Pair.

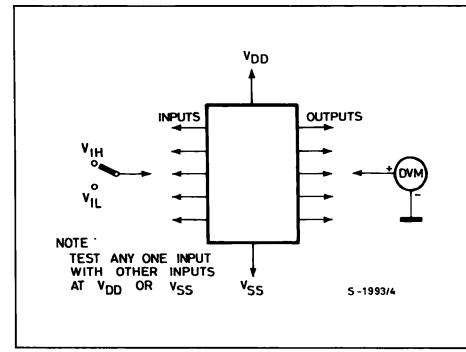


## TEST CIRCUITS

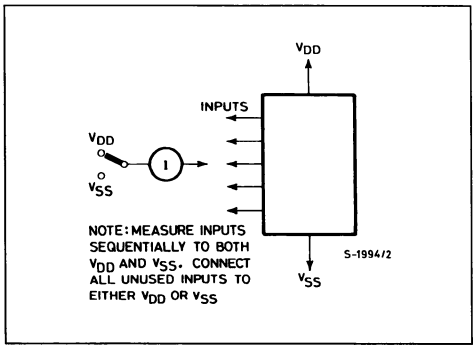
Quiescent Device Current.




Noise Immunity.



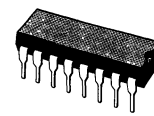

Input Leakage Current.



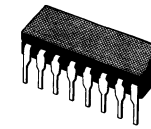
# HCC/HCF4042B

## QUAD CLOCKED "D" LATCH

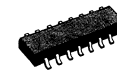
- CLOCK POLARITY CONTROL
- Q AND $\overline{Q}$ OUTPUTS
- COMMON CLOCK
- LOW POWER TTL COMPATIBLE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Package)



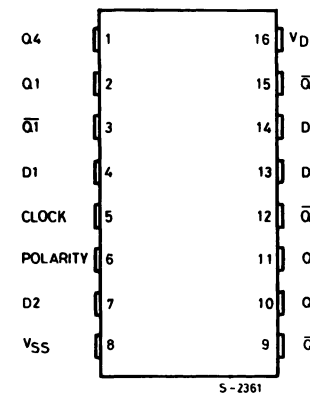
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

| | |
|---|---|
| HCC4042BF | HCF4042BM1 |
| HCF4042BEY | HCF4042BC1 |

**PIN CONNECTIONS**



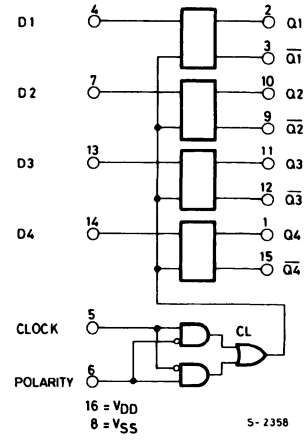

### DESCRIPTION

The **HCC4042B** (extended temperature range) and **HCF4042B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and plastic micro package.

The **HCC/HCF4042B** types contain four latch circuits, each strobed by a common clock. Complementary buffered outputs are available from each circuit. The impedance of the n- and p-channel output devices is balanced and all outputs are electrically identical.

Information present at the data input is transferred to outputs Q and $\overline{Q}$ during the CLOCK level which is programmed by the POLARITY input. For POLARITY = 0 the transfer occurs during the 0 CLOCK level and for POLARITY = 1 the transfer occurs during the 1 CLOCK level. The outputs follow the data input providing the CLOCK and POLARITY levels defined above are present. When a CLOCK transition occurs (positive for POLARITY = 0 and negative for POLARITY = 1) the information present at the input during the CLOCK transition is retained at the outputs until an opposite CLOCK transition occurs.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

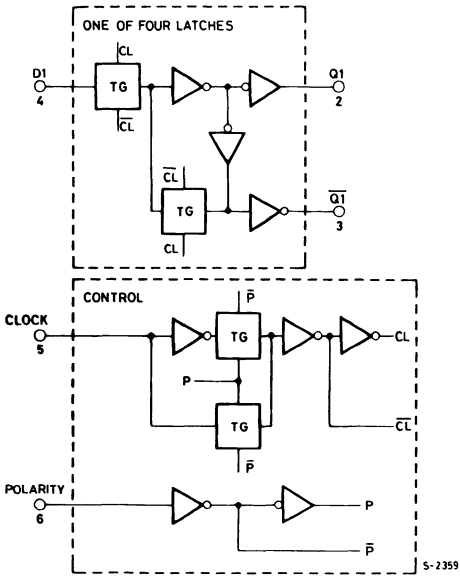
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltage values are referred to $V_{SS}$ pin voltage.

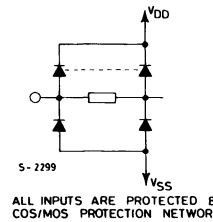
## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage **HCC** Types<br>: **HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC BLOCK DIAGRAM AND TRUTH TABLE




| Clock | Polarity | Q |
|---|---|---|
| 0 | 0 | D |
| ⎍⎺ | 0 | Latch |
| 1 | 1 | D |
| ⎺⎍ | 1 | Latch |




## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | |
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 1 | | 0.02 | 1 | | 30 | μA |
| | | | 0/10 | | | 10 | | 2 | | 0.02 | 2 | | 60 | |
| | | | 0/15 | | | 15 | | 4 | | 0.02 | 4 | | 120 | |
| | | | 0/20 | | | 20 | | 20 | | 0.04 | 20 | | 600 | |
| | | HCF Types | 0/5 | | | 5 | | 4 | | 0.02 | 4 | | 30 | |
| | | | 0/10 | | | 10 | | 8 | | 0.02 | 8 | | 60 | |
| | | | 0/15 | | | 15 | | 16 | | 0.02 | 16 | | 120 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |

* $T_{Low}$ = − 55°C for **HCC** device . − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2 5V min. with $V_{DD}$ = 15V.

## STATIC ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | | Test Conditions | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | – 2 | | – 1.6 | – 3.2 | | – 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | – 0.64 | | – 0.51 | – 1 | | – 0 36 | | |
| | | | 0/10 | 9.5 | | 10 | – 1.6 | | – 1.3 | – 2.6 | | – 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | – 4.2 | | – 3.4 | – 6.8 | | – 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | – 1.53 | | – 1.36 | – 3.2 | | – 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | – 0.52 | | – 0.44 | – 1 | | – 0 36 | | |
| | | | 0/10 | 9.5 | | 10 | – 1.3 | | – 1.1 | – 2.6 | | – 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | – 3.6 | | – 3.0 | – 6.8 | | – 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0 4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input leakage Curent | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = – 55°C for **HCC** device : – 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is . 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V

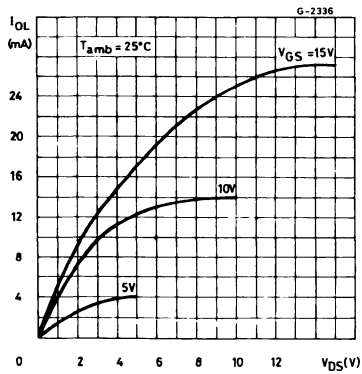
## DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall times = 20ns)

| Symbol | Parameter | | Test Conditions | Value | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time | Data in to Q | | 5 | | 110 | 220 | ns |
| | | | | 10 | | 55 | 110 | |
| | | | | 15 | | 40 | 80 | |
| | | Data in to $\overline{Q}$ | | 5 | | 150 | 300 | |
| | | | | 10 | | 75 | 150 | |
| | | | | 15 | | 50 | 100 | |
| | | Clock to Q | | 5 | | 225 | 450 | |
| | | | | 10 | | 100 | 200 | |
| | | | | 15 | | 80 | 160 | |
| | | Clock to $\overline{Q}$ | | 5 | | 250 | 500 | |
| | | | | 10 | | 115 | 230 | |
| | | | | 15 | | 90 | 180 | |

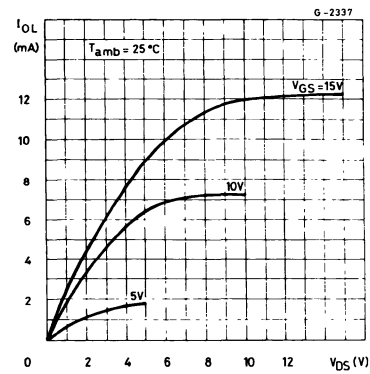
## DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_W$ | Clock Pulse Width | | 5 | 200 | 100 | | ns |
| | | | 10 | 100 | 50 | | |
| | | | 15 | 60 | 30 | | |
| $t_{setup}$ | Setup Time | | 5 | 50 | 0 | | ns |
| | | | 10 | 30 | 0 | | |
| | | | 15 | 25 | 0 | | |
| $t_{hold}$ | Hold Time | | 5 | 120 | 60 | | ns |
| | | | 10 | 60 | 30 | | |
| | | | 15 | 50 | 25 | | |
| $t_r$,$t_f$ | Clock Input Rise or Fall Time | | 5 | Not Rise or Fall Time Sensitive | | | µs |
| | | | 10 | | | | |
| | | | 15 | | | | |

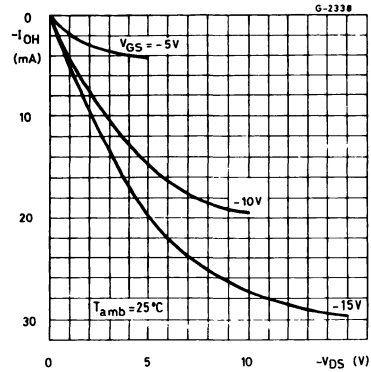
Typical Output Low (sink) Current Characteristics.



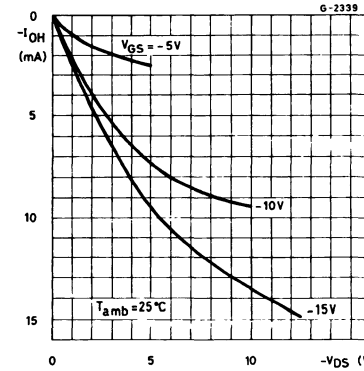

Minimum Output Low (sink) Current Characteristics.



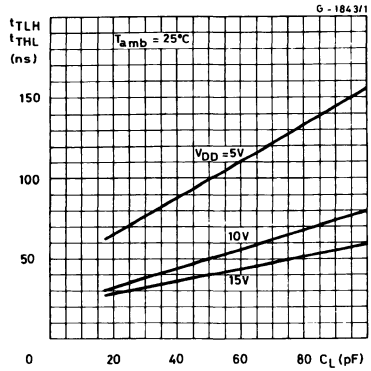
Typical Output High (source) Current Characteristics.



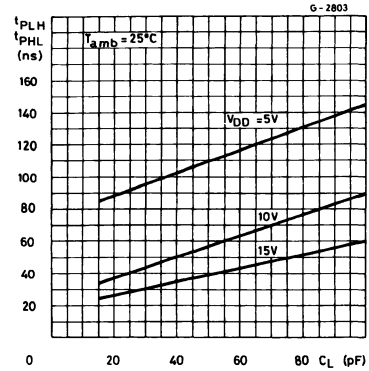

Minimum Output High (source) Current Characteristics.



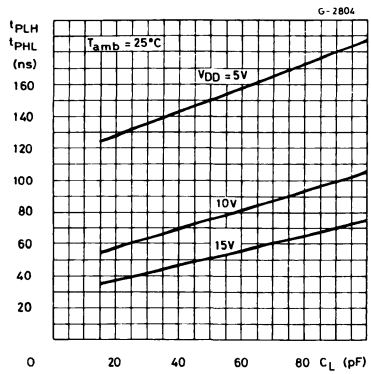

Typical Transition Time vs. Load Capacitance.



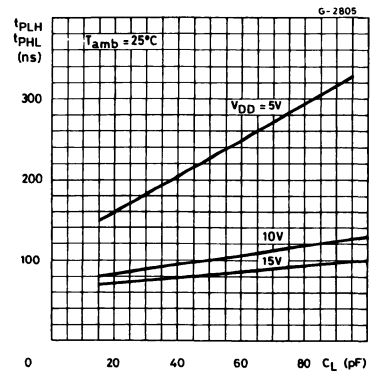

Typical Propagation Delay Time vs. Load Capacitance (data to Q).



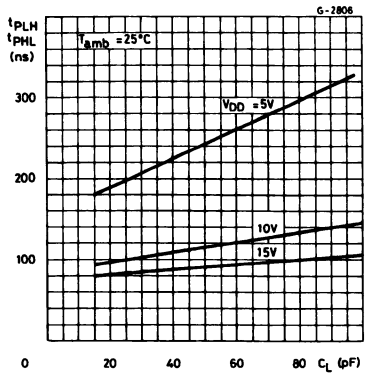

Typical Propagation Delay Time vs. Load Capacitance (data to $\overline{Q}$).



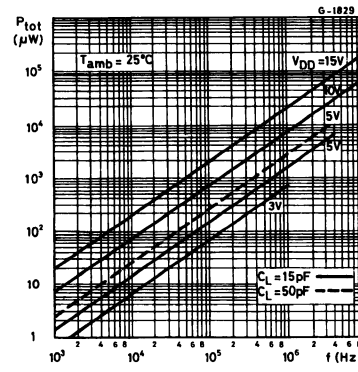

Typical Propagation Delay Time vs. Load Capacitance (clock to Q).



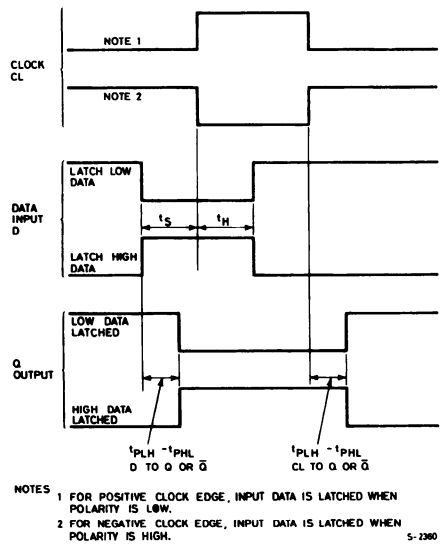
Typical Propagation Delay Time vs. Load Capacitance (clock to $\overline{Q}$).




Typical Power Dissipation/device vs. Frequency.

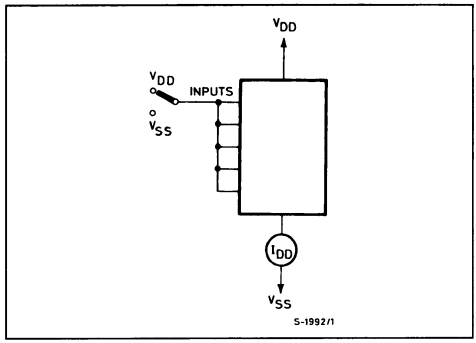



Dynamic Test Parameters.

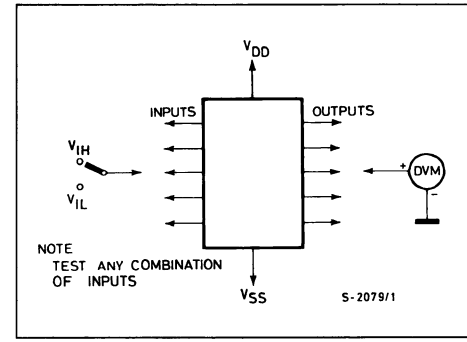


## TEST CIRCUITS

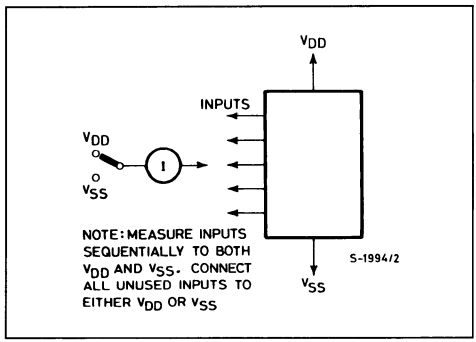
Quiescent Device Current.




Noise Immunity.




Input Leakage Current.



SGS-THOMSON MICROELECTRONICS

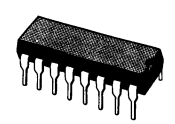
# HCC/HCF4043B HCC/HCF4044B

## QUAD 3-STATE R-S LATCHES

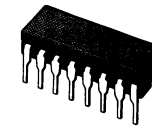
**QUAD NOR R-S LATCH-4043B**

**QUAD NAND R-S LATCH-4044B**

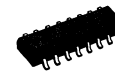
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 3-LEVEL OUTPUTS WITH COMMON OUTPUT ENABLE
- SEPARATE SET AND RESET INPUT FOR EACH LATCH
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- NOR AND NAND CONFIGURATIONS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)



**M1**
(Micro Package)

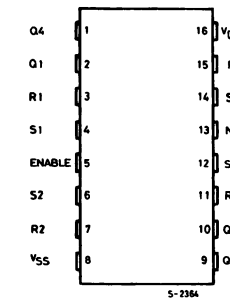
**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

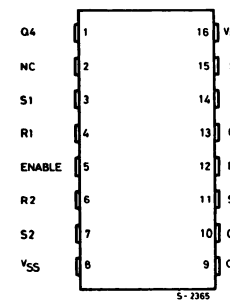
HCC40XXBF HCF40XXBM1
HCF40XXBEY HCF40XXBC1

**PIN CONNECTIONS**

**4043B**



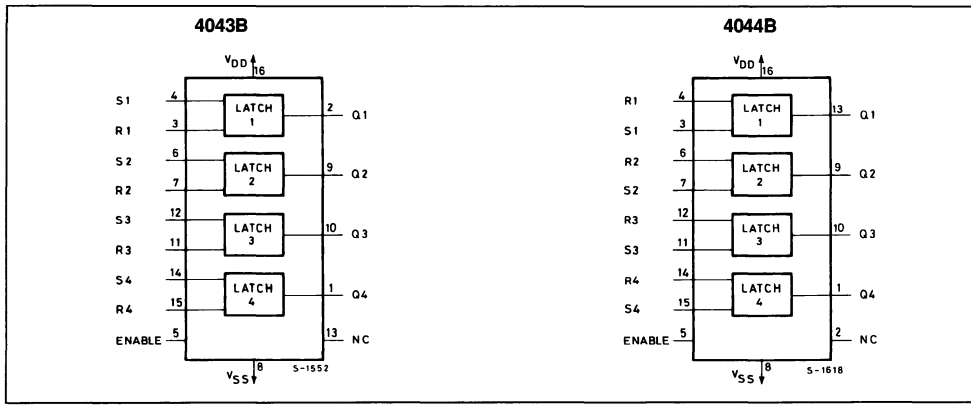

**4044B**




### DESCRIPTION

The **HCC4043B, HCC4044B**, (extended temperature range) and the **HCF4043B, HCF4044B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and plastic micropackage. The **HCC/HCF4043B** types are quad cross-coupled 3-state COS/MOS NOR latches and the **HCC/HCF4044B** types are quad cross-coupled 3-state COS/MOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are controlled by a common ENABLE input. A logic "1" or "high" on the ENABLE input connects the latch states to the Q outputs. A logic "0" or "low" on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common bussing of the outputs.

## FUNCTIONAL DIAGRAMS




## ABSOLUTE MAXIMUM RATINGS

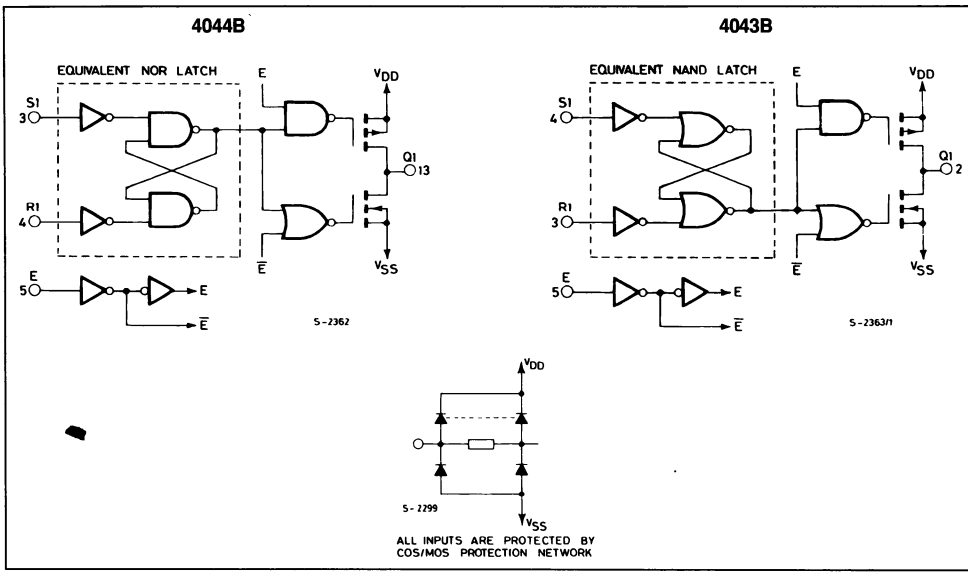
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAMS




## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | |
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 1 | | 0.02 | 1 | | 30 | μA |
| | | | 0/10 | | | 10 | | 2 | | 0.02 | 2 | | 60 | |
| | | | 0/15 | | | 15 | | 4 | | 0.02 | 4 | | 120 | |
| | | | 0/20 | | | 20 | | 20 | | 0.04 | 20 | | 600 | |
| | | HCF Types | 0/ 5 | | | 5 | | 4 | | 0.02 | 4 | | 30 | |
| | | | 0/10 | | | 10 | | 8 | | 0.02 | 8 | | 60 | |
| | | | 0/15 | | | 15 | | 16 | | 0.02 | 16 | | 120 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |

* $T_{Low}$ = – 55°C for **HCC** device : – 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.

## STATIC ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | – 2 | | – 1.6 | – 3.2 | | – 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | – 0.64 | | – 0.51 | – 1 | | – 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | – 1.6 | | – 1.3 | – 2.6 | | – 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | – 4.2 | | – 3.4 | – 6.8 | | – 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | – 1.53 | | – 1.36 | – 3.2 | | – 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | – 0.52 | | – 0.44 | – 1 | | – 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | – 1.3 | | – 1.1 | – 2.6 | | – 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | – 3.6 | | – 3.0 | – 6.8 | | – 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $I_{OH}$ | 3-state Output | HCC Types | 0/18 | 0/18 | | 18 | | ± 0.4 | | $\pm 10^{-4}$ | ± 0.4 | | ± 12 | μA |
| | | HCF Types | 0/15 | 0/15 | | 15 | | ± 1.0 | | $\pm 10^{-4}$ | ± 1.0 | | ± 7.5 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = – 55°C for **HCC** device : – 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.

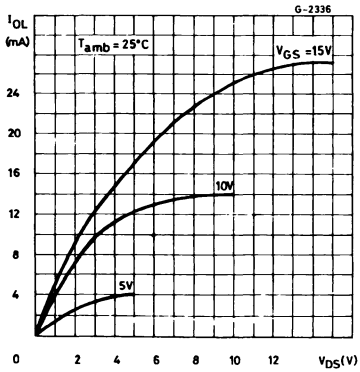
## DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall times = 20ns)

| Symbol | Parameter | Test Conditions | $V_{DD}$ (V) | Value Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time (SET or RESET to Q) | | 5 | | 150 | 300 | ns |
| | | | 10 | | 70 | 140 | |
| | | | 15 | | 50 | 100 | |
| $t_{PZH}$, $t_{PHZ}$ | 3-state Propagation Delay Time (ENABLE to Q) | | 5 | | 115 | 230 | ns |
| | | | 10 | | 55 | 110 | |
| | | | 15 | | 40 | 80 | |

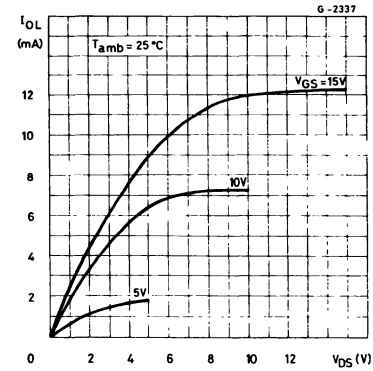
**DYNAMIC ELECTRICAL CHARACTERISTICS** (continued)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLZ}$, $t_{PZL}$ | Propagation Delay Time | | 5 | | 90 | 180 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 35 | 70 | |
| $t_{TLH}$, $t_{THL}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_W$ | Pulse Width (SET or RESET) | | 5 | 160 | 80 | | ns |
| | | | 10 | 80 | 40 | | |
| | | | 15 | 40 | 20 | | |

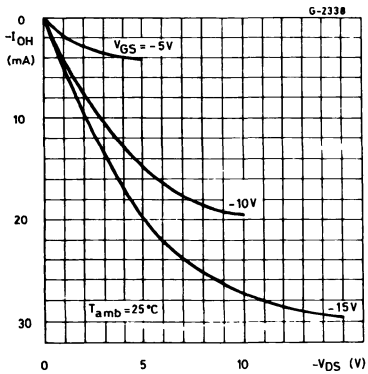
Typical Output Low (sink) Current.



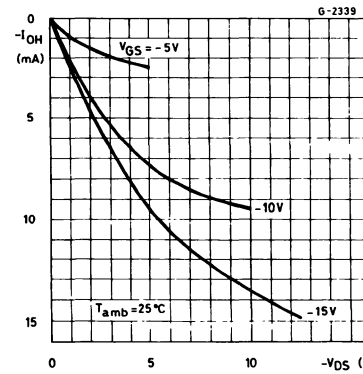

Minimum Output Low (sink) Current Characteristics.



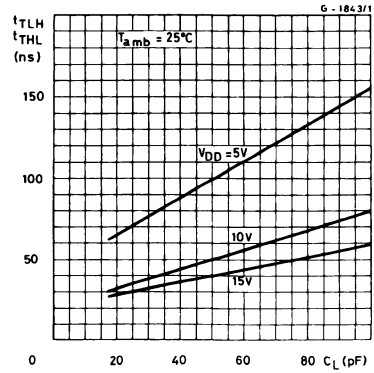

Typical Output High (source) Current Characteristics.



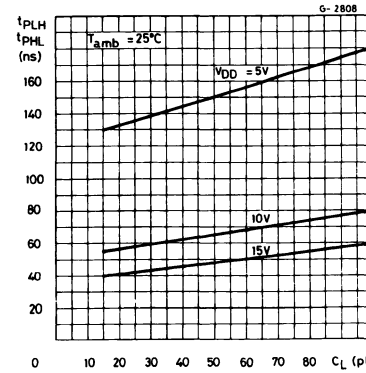

Minimum Output High (source) Current Characteristics.



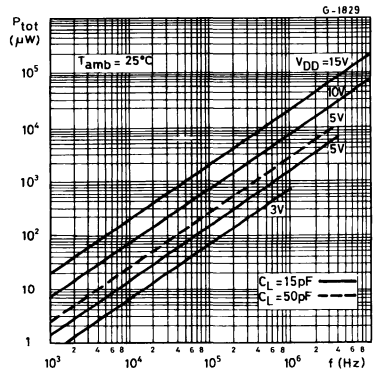
Typical Transition Time vs. Load Capacitance.



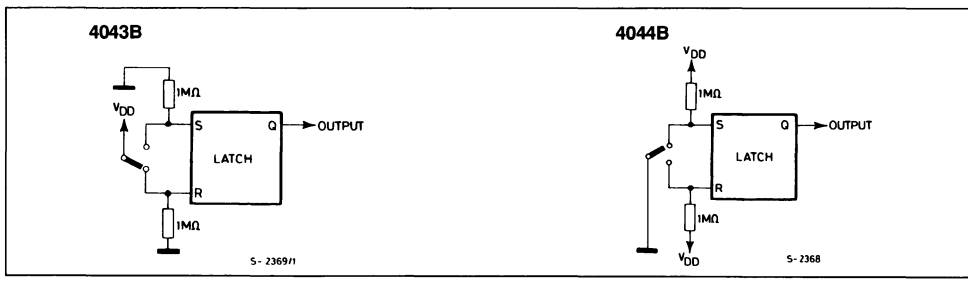

Typical Propagation Delay Time vs. Load Capacitance (SET, RESET to Q, $\overline{Q}$).




Typical Power Dissipation/device vs. Frequency.

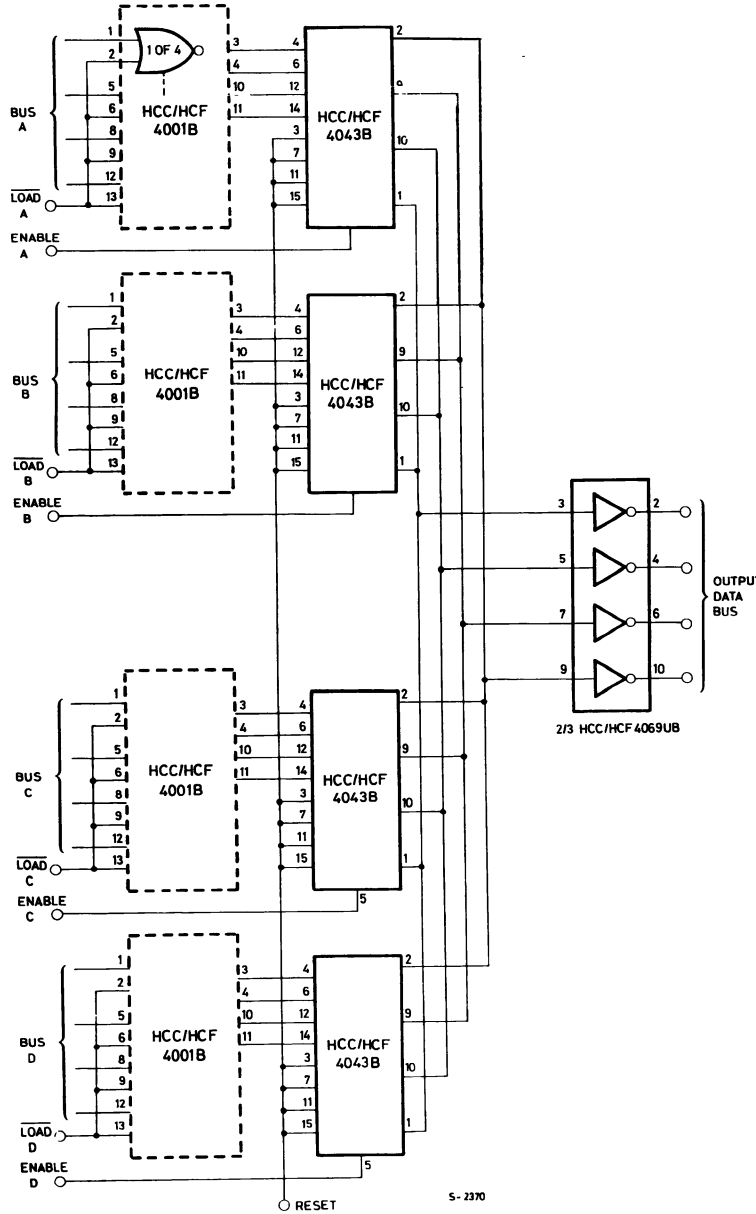



Switch Bounce Eliminator.



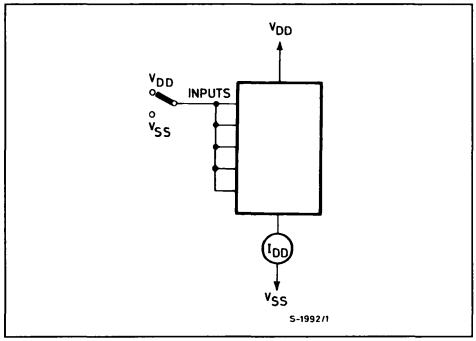
## APPLICATIONS

MULTIPLE BUS STORAGE.

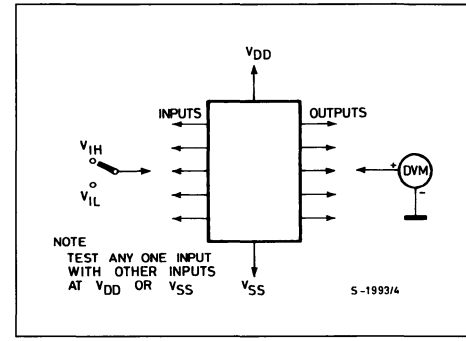


## TEST CIRCUITS

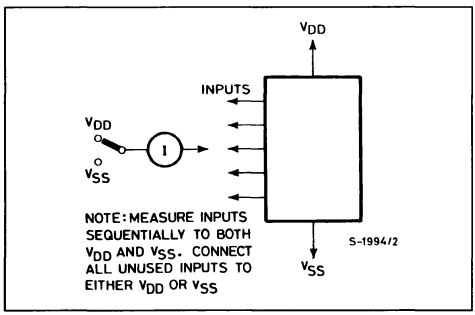
Quiescent Device Current.



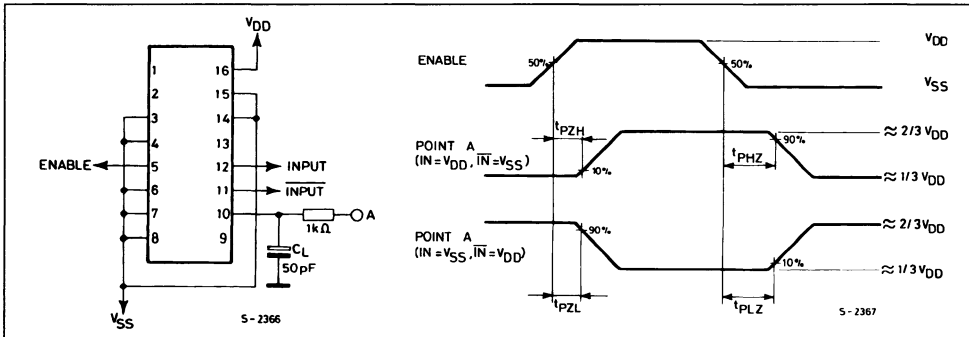

Input Voltage.




Input Current.




Enable Propagation Delay Time and Waveforms.




| Test | IN | $\overline{IN}$ | A |
|---|---|---|---|
| $t_{PHZ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ |
| $t_{PLZ}$ | $V_{SS}$ | $V_{DD}$ | $V_{DD}$ |
| $t_{PZH}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ |
| $t_{PZL}$ | $V_{SS}$ | $V_{DD}$ | $V_{DD}$ |

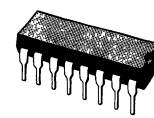
Z = High impedance

SGS-THOMSON MICROELECTRONICS

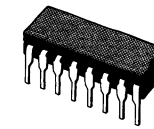
# HCC/HCF4045B

## 21-STAGE COUNTER

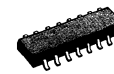
- VERY LOW OPERATING DISSIPATION.... 1mW (typ.) ; @ $V_{DD}$ = 5V, $f_\phi$ = 1MHz
- OUTPUT DRIVERS WITH SINCK OR SOURCE CAPABILITY....7mA (typ.) @ $V_{DD}$ = 5V
- MEDIUM SPEED (typ.)....$f_\phi$, = 16MHz, @ $V_{DD}$ = 10V
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)



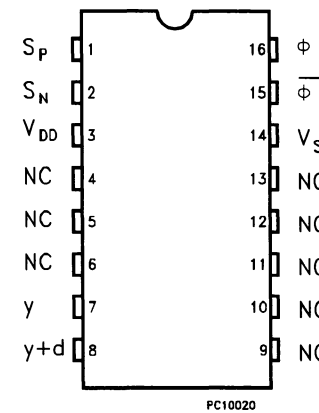
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4045BF HCF4045BM1
HCF4045BEY HCF4045BC1

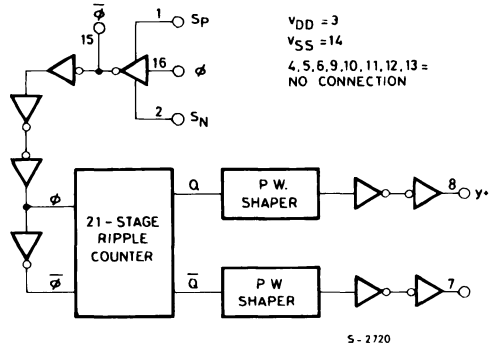
**PIN CONNECTIONS**




### DESCRIPTION

The **HCC4045B** (extended temperature range) and **HCF4045B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF4045B** is a timing circuit consisting of 21 counter stages, two output-shaping flip-flops, two inverter output drivers, and input inverters for use in a crystal oscillator. The **HCC/HCF4045B** configuration provides 21 flip-flop counting stages, and two flip-flops for shaping the output waveform for a 3.125% duty cycle. Push-pull operation is provided by the inverter output drivers. The first inverter is intended for use as a crystal oscillator-amplifier. However, it may be used as a normal logic inverter if desired. A crystal oscillator circuit can be made less sensitive to voltage-supply variations by the use of source resistors. In this device, the sources of the p and n transistors have been brought out to package terminals. If external resistors are not required, the sources must be shorted to their respective substrates ($S_p$ to $V_{DD}$, $S_n$ to $V_{SS}$).

## LOGIC DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

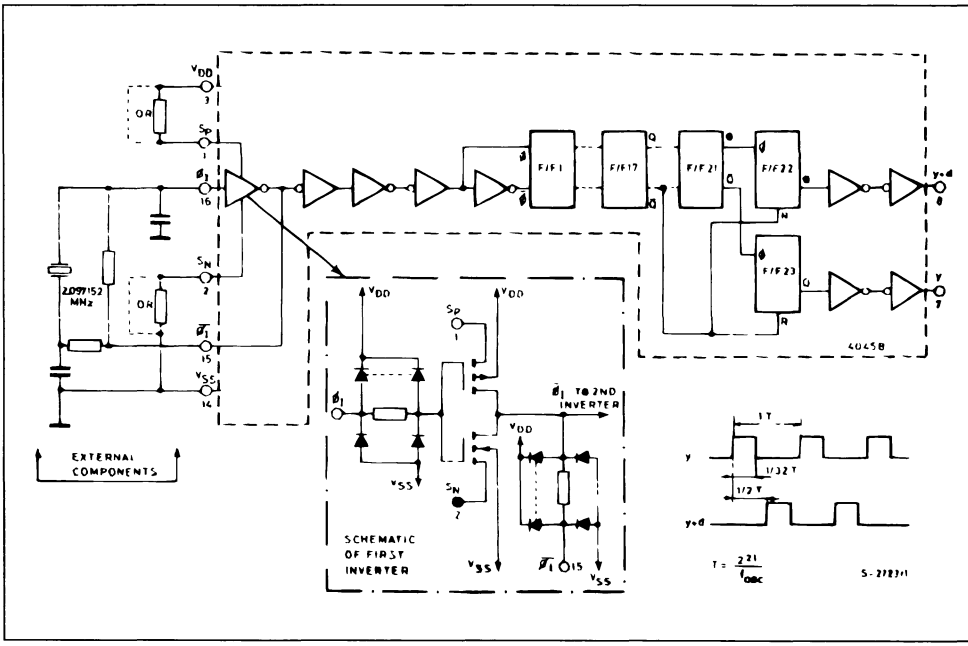
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltage values are referred to $V_{SS}$ pin voltage

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAM

4045B and Outboard Components in a Typical 21-stage Counter Application.




## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{Low}$* | | 25°C | | | $T_{High}$* | | |
| | | | | | | | Min. | Max. | Min. | Typ. | Max. | Min. | Max. | |
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |

* $T_{Low}$ = – 55°C for **HCC** device – 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.

## STATIC ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/5 | 4.6 | | 5 | − 4.5 | | − 3.6 | − 7 | | − 2.5 | | mA |
| | | | 0/10 | 9.5 | | 10 | − 11.2 | | − 9.1 | − 18 | | − 6.3 | | |
| | | | 0/15 | 13.5 | | 15 | − 29.4 | | − 23.8 | − 47 | | − 16.8 | | |
| | | HCF Types | 0/5 | 4.6 | | 5 | − 3.6 | | − 3 | − 7 | | − 2.46 | | |
| | | | 0/10 | 9.5 | | 10 | − 8.9 | | − 7.7 | − 18 | | − 6.54 | | |
| | | | 0/15 | 13.5 | | 15 | − 23.8 | | − 20 | − 47 | | − 16.6 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/5 | 0.4 | | 5 | 4.5 | | 3.6 | 7 | | 2.5 | | mA |
| | | | 0/10 | 0.5 | | 10 | 11.2 | | 9.1 | 18 | | 6.3 | | |
| | | | 0/15 | 1.5 | | 15 | 29.4 | | 23.8 | 47 | | 16.8 | | |
| | | HCF Types | 0/5 | 0.4 | | 5 | 3.6 | | 3 | 7 | | 2.46 | | |
| | | | 0/10 | 0.5 | | 10 | 8.9 | | 7.7 | 18 | | 6.54 | | |
| | | | 0/15 | 1.5 | | 15 | 23.8 | | 20 | 47 | | 16.6 | | |
| $I_{IH}$, $I_{IL}$ | Input Laekage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.

## DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ = 0.3%/°C values, all input rise and fall times = 20ns)

| Symbol | Parameter | Test Conditions | $V_{DD}$ (V) | Value Min. | Value Typ. | Value Max. | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time ø to y or y + d Out | | 5 | | 2.2 | 5.5 | μs |
| | | | 10 | | 0.9 | 2.7 | |
| | | | 15 | | 0.65 | 2 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | 5 | | 25 | 50 | ns |
| | | | 10 | | 13 | 25 | |
| | | | 15 | | 10 | 20 | |
| $f_{max}$ | Maximum Input Pulse Frequency External Pulse Source | | 5 | 5 | 10 | | MHz |
| | | | 10 | 12 | 25 | | |
| | | | 15 | 15 | 30 | | |

## DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_W$ | Input Pulse Width | | 5 | | 50 | 100 | ns |
| | | | 10 | | 25 | 50 | |
| | | | 15 | | 20 | 40 | |
| $t_r$, $t_f$ | Clock Input Rise or Fall Time | | 5 | | | 500 | µs |
| | | | 10 | | | 500 | |
| | | | 15 | | | 500 | |
| | Variation of Output Frequency (unit to unit) | f = 5MHz | 5 | | 0.05 | | % |
| | | | 10 | | 0.03 | | |
| | | | 15 | | 0.1 | | |
| **RC OSCILLATOR OPERATION** | | | | | | | |
| $f_{osc}$ | Maximum Oscillator Frequency (see fig. belove left) | $R_X$ = 50KΩ<br>$R_S$ = 560KΩ<br>$C_X$ = 50pF | 5 | 45 | 60 | 75 | KHz |
| | | | 10 | 45 | 60 | 75 | |
| | | | 15 | 45 | 60 | 75 | |

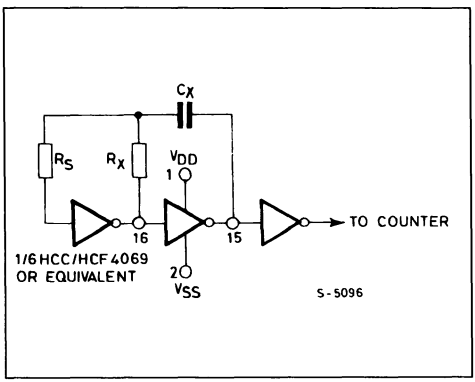
## TYPICAL APPLICATIONS

Digital equipment in which ultra-low dissipation and/or operation using a battery source are primary design requirements.

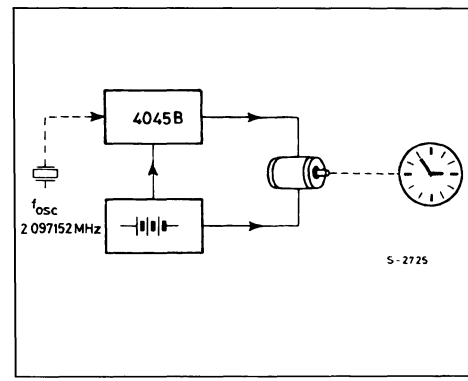
Accurate timing from a crystal oscillator for timing applications such as wall clocks, table clocks, automobile clocks, and digital timing references in any circuit requiring accurately timed outputs at various intervals in the counting sequence.

Driving miniature synchronous motors, stepping motors, or external bipolar transistors in push-pull fashion.

Typical RC Circuit.

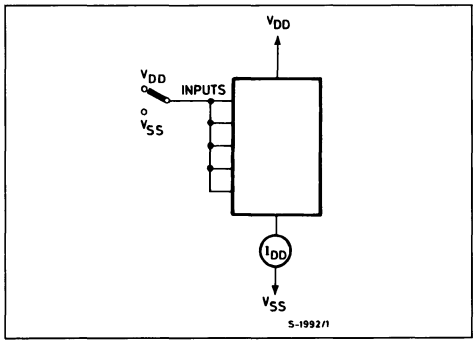



Electronic Watch Application Circuit.

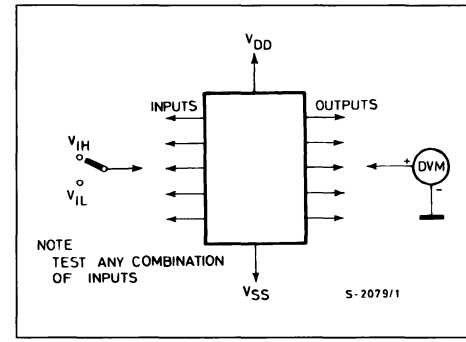


## TEST CIRCUITS

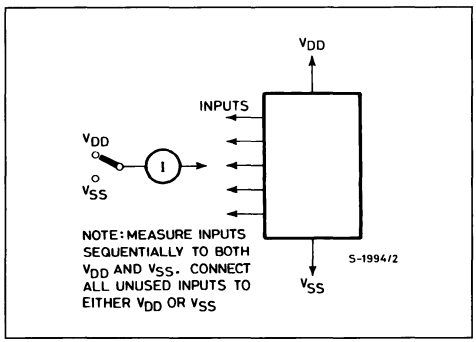
Quiescent Device Current.




Noise Immunity.




Input Leakage Current.

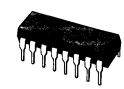


SGS-THOMSON MICROELECTRONICS

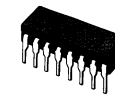
# HCC/HCF4046B

## MICROPOWER PHASE-LOCKED LOOP

- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- VERY LOW POWER CONSUMPTION : 100µW (TYP.) AT VCO $f_o$ = 10kHz, $V_{DD}$ = 5V
- OPERATING FREQUENCY RANGE : UP TO 1.4MHz (TYP.) AT $V_{DD}$ = 10V
- LOW FREQUENCY DRIFT : 0.06%/°C (typ.) AT $V_{DD}$ = 10V
- CHOICE OF TWO PHASE COMPARATORS : 1) EXCLUSIVE - OR NETWORK 2) EDGE-CONTROLLED MEMORY NETWORK WITH PHASE-PULSE OUTPUT FOR LOCK IN-DICATION
- HIGH VCO LINEARITY : 1% (TYP.)
- VCO INHIBIT CONTROL FOR ON-OFF KEYING AND ULTRA-LOW STANDBY POWER CONSUMPTION
- SOURCE-FOLLOWER OUTPUT OF VCO CONTROL INPUT (demod. output)
- ZENER DIODE TO ASSIST SUPPLY REGULA-TION
- 5V, 10V AND 15V PARAMETRIC RATING
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TEN-TATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)

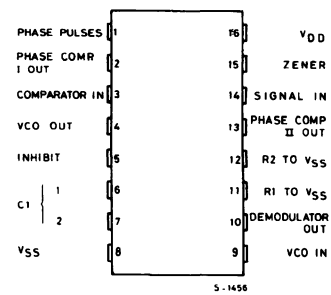


**F**
(Ceramic Package)

**C1**
(Chip Carrier)

**ORDER CODES :**
HCC4046BF HCF4046BEY
HCF4043BC1

**PIN CONNECTIONS**




### DESCRIPTION

The **HCC4046B** (extended temperature range) and **HCF4046B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package. The **HCC/HCF4046B** COS/MOS Micropower Phase-Locked Loop (PLL) consists of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2V zener diode is provided for supply regulation if necessary.

### VCO Section

The VCO requires one external capacitor C1 and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ($10^{12\Omega}$) of the VCO simplifiers the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor ($R_S$) of 10 kΩ or more should be connected from this terminal to $V_{SS}$. If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full COS/MOS logic swing is available at the output of the VCO and allows direct coupling to COS/MOS frequency dividers such as the **HCC/HCF4024B**, **HCC/HCF4018B**, **HCC/HCF4020B**, **HCC/HCF4022B**, **HCC/HCF4029B**,and **HBC/HBF4059A**. One or more **HCC/HCF4018B** (Presettable Divide-by-N Counter) or **HCC/HCF4029B** (Presettable Up/Down Counter), or **HBC/HBF4059A** (Programmable Divide-by-"N" Counter), together with the **HCC/HCF4046B** (Phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

### Phase Comparators

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within COS/MOS logic levels [logic "0" ≤ 30 % ($V_{DD}$ – $V_{SS}$), logic "1" ≥ 70 % ($V_{DD}$ - $V_{SS}$)]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input. Phase comparator I is an exclusive-OR network ; it operates analagously to an over-driven balanced mixer. To maximize the lock range, the signal-and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency ($f_o$). The frequency range of input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range ($2 f_c$). The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range ($2 f_L$). The capture range is ≤ the lock range. With phase comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal. One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Fig. (a) shows the typical, triangular, phase-to-output response characteristic of phase-comparator I. Typical waveforms for a COS/MOS phase-locked-loop employing phase comparator I in locked condition of $f_o$ is shown in fig. (b). Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-stage output-circuit comprising p- and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to $V_{DD}$ or down to $V_{SS}$, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON most of the time, and both the n- and p-drivers OFF (3 state) the remainder of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON most of the time, and both the n- and p-drivers OFF (3 state) the remainder of the time. If the signal and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal and comparator-input frequencies are the same, but the comparator input lags the signal in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p- and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists be-

tween signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig. (c) shows typical waveforms for a COS/MOS PLL employing phase comparator II in

**Figure a** : Phase-Comparator I Characteristics at Low-Pass Filter Output.

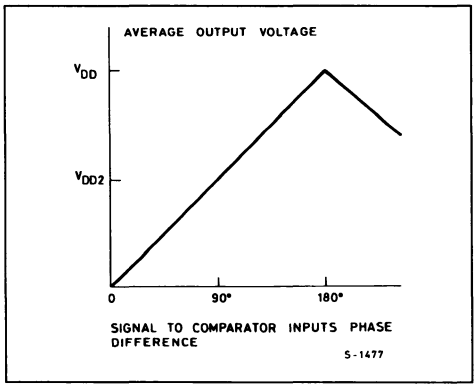



**Figure b** : Typical Waveforms for COS/MOS Phase Locked-Loop Employing Phase Comparator I in Locked Condition of $f_o$.

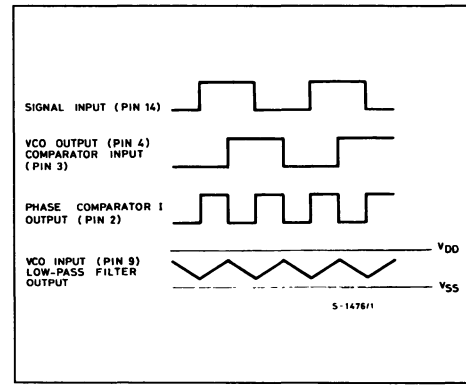
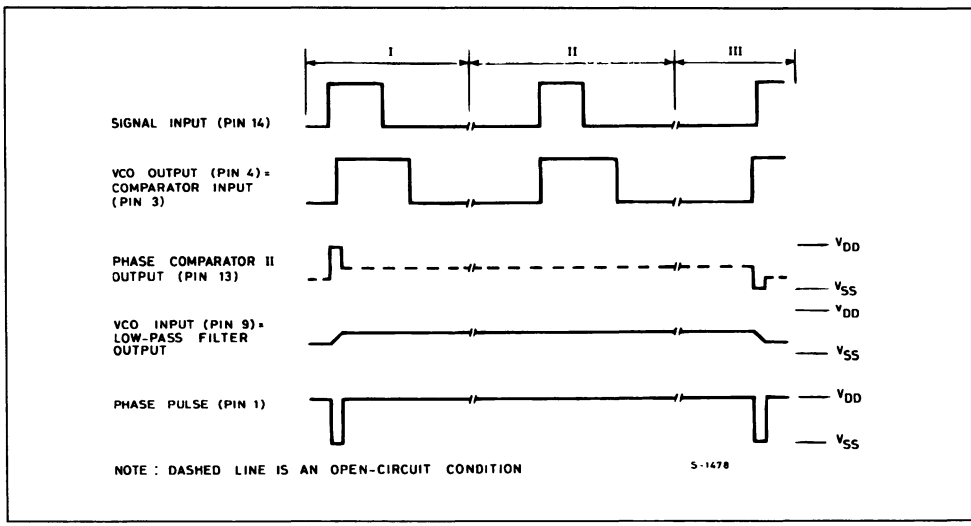
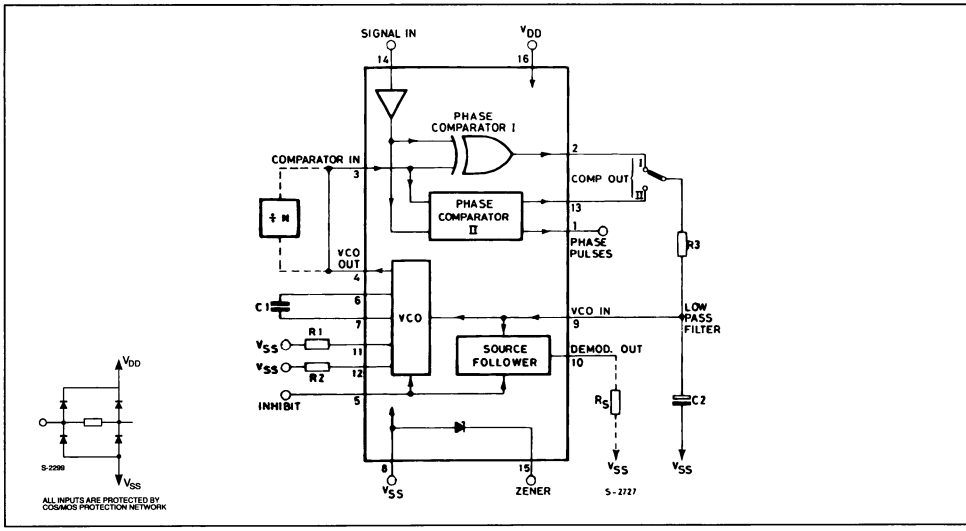



**Figure C** : Typical Waveforms For COS/MOS Phase-locked Loop Employing Phase Comparator II In Locked Condition.



## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **VCO SECTION** | | | | | | | | | | | | | | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | 5 | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | 10 | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | 15 | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $± 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $± 10^{-5}$ | ± 0.3 | | ± 1 | |
| **PHASE COMPARATOR SECTION** | | | | | | | | | | | | | | |
| $I_{DD}$ | Total Device Current Pin 14 = Open Pin 5 = $V_{DD}$ | | 0/ 5 | | | 5 | | 0.1 | | 0.05 | 0.1 | | 0.1 | mA |
| | | | 0/10 | | | 10 | | 0.5 | | 0.25 | 0.5 | | 0.5 | |
| | | | 0/15 | | | 15 | | 1.5 | | 0.75 | 1.5 | | 1.5 | |
| | | | 0/20 | | | 20 | | 4 | | 2 | 4 | | 4 | |
| | Pin 14 = $V_{SS}$ or $V_{DD}$ Pin 5 = $V_{DD}$ | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.

## STATIC ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | | Test Conditions | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current (except. pin 14) | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | ± $10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | ± $10^{-5}$ | ± 0.3 | | ± 1 | |
| $I_{OUT}$ | 3-state Leakage Current | HCC Types | 0/18 | 0/18 | | 18 | | ± 0.4 | | ± $10^{-4}$ | ± 0.4 | | ± 12 | μA |
| | | HCF Types | 0/15 | 0/15 | | 15 | | ± 1.0 | | ± $10^{-4}$ | ± 1.0 | | ± 7.5 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.

## ELECTRICAL CARACTERISTICS ($T_{amb}$ = 25 °C)

| Symbol | Parameter | Test Conditions | $V_{DD}$ (V) | Value Min. | Value Typ. | Value Max. | Unit |
|---|---|---|---|---|---|---|---|
| **VCO SECTION** | | | | | | | |
| $P_D$ | Operating Power Dissipation | fo = 10 KHz R1 = 10 MΩ R2 = ∞ $V_{COIN} = \frac{V_{DD}}{2}$ | 5 | | 70 | 140 | μW |
| | | | 10 | | 800 | 1600 | |
| | | | 15 | | 3000 | 6000 | |
| $f_{max}$ | Maximum Frequency | R1 = 10 KΩ C1 = 50 pF R2 = ∞ $V_{COIN} = V_{DD}$ | 5 | 0.3 | 0.6 | | MHz |
| | | | 10 | 0.6 | 1.2 | | |
| | | | 15 | 0.8 | 1.6 | | |
| | | R1 = 5 KΩ n C1 = 50 pF R2 = ∞ $V_{COIN} = V_{DD}$ | 5 | 0.5 | 0.8 | | |
| | | | 10 | 1 | 1.4 | | |
| | | | 15 | 1.4 | 2.4 | | |
| | Center Frequency ($f_o$) and Frequency Range $f_{max}$ - $f_{min}$ | Programmable with external components R1, R2 and C1 | | | | | |
| | Linearity | $V_{COIN}$=2.5V $^{\pm 0.3}$ R1=10 KΩ | 5 | | 1.7 | | % |
| | | $V_{COIN}$=5V $^{\pm 1}$ R1=100 KΩ | 10 | | 0.5 | | |
| | | $V_{COIN}$=5V $^{\pm 2.5}$ R1=400 KΩ | 10 | | 4 | | |
| | | $V_{COIN}$=7.5V $^{\pm 1.5}$ R1=100 KΩ | 15 | | 0.5 | | |
| | | $V_{COIN}$=7.5V $^{\pm 5}$ R1=1 MΩ | 15 | | 7 | | |
| | Temperature Frequency Stability (no frequency offset) $f_{min}$ = 0 | | 5 | | ±0.12 | | %/°C |
| | | | 10 | | ±0.04 | | |
| | | | 15 | | ±0.015 | | |
| | Temperature Frequency Stability (frequency offset) $f_{min} \neq 0$ | | 5 | | ±0.09 | | |
| | | | 10 | | ±0.07 | | |
| | | | 15 | | ±0.03 | | |
| $V_{CO}$ | Output Duty Cycle | | 5, 10, 15 | | 50 | | % |
| $t_{THL}$ $t_{TLH}$ | VCO Output Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| | Source Follower Output (demodulated Output): Offset Voltage $V_{COIN}$ - $V_{DEM}$ | $R_S$ > 10 KΩ | 5, 10, 15 | | 1.8 | 2.5 | V |
| | Source Follower Output (demodulated Output): Linearity | $R_S$=100 KΩ $V_{COIN}$=2.5 $^{\pm 0.3}$V | 5 | | 0.3 | | % |
| | | $R_S$=300 KΩ $V_{COIN}$=5 $^{\pm 2.5}$V | 10 | | 0.7 | | |
| | | $R_S$=500 KΩ $V_{COIN}$=7.5 $^{\pm 5}$V | 15 | | 0.9 | | |
| $V_Z$ | Zener Diode Voltage | $I_Z$ = 50 μA | | 4.45 | 5.5 | 7.5 | V |
| $R_Z$ | Zener Dynamic Resistance | $I_Z$ = 1 mA | | | 40 | | Ω |
| **PHASE COMPARATOR SECTION** | | | | | | | |
| R14 | Pin 14 (signal in) Input Resistance | | 5 | 1 | 2 | | MΩ |
| | | | 10 | 0.2 | 0.4 | | |
| | | | 15 | 0.1 | 0.2 | | |
| | A.C. Coupled Signal Input Voltage Sensitivity * (peak to paek) | $f_{in}$ = 100 KHz sine wave | 5 | 180 | 360 | | mV |
| | | | 10 | 330 | 660 | | |
| | | | 15 | 900 | 1800 | | |

## ELECTRICAL CHARACTERISTICS (continued)

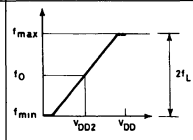
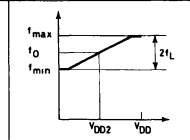
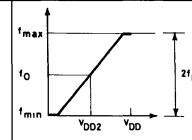
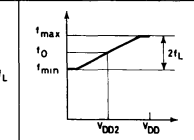
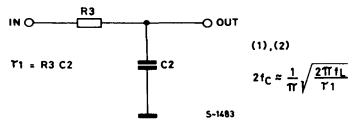
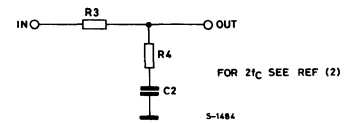
| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| **PHASE COMPARATOR SECTION** (cont'd) | | | | | | | |
| $T_{PHL}$ | Propagation Delay Time High to Low Level Pins 14 to 13 | | 5 | 225 | 450 | | ns |
| | | | 10 | 100 | 200 | | |
| | | | 15 | 65 | 130 | | |
| $T_{PLH}$ | Propagation Delay Time Low to High, Level | | 5 | | 350 | 700 | ns |
| | | | 10 | | 150 | 300 | |
| | | | 15 | | 100 | 200 | |
| $T_{PHZ}$ | Propagation Delay Time 3-state High Level to High Impedance Pins 14 to 13 | | 5 | | 225 | 450 | ns |
| | | | 10 | | 100 | 200 | |
| | | | 15 | | 65 | 130 | |
| $T_{PLZ}$ | Low Level to High Impedance | | 5 | | 285 | 570 | ns |
| | | | 10 | | 130 | 260 | |
| | | | 15 | | 95 | 190 | |
| $t_r$, $t_f$ | Input Rise or Fall Time Comparator Pin 3 | | 5 | | | 50 | µs |
| | | | 10 | | | 1 | |
| | | | 15 | | | 0.3 | |
| | Signal Pin 14 | | 5 | | | 500 | µs |
| | | | 10 | | | 20 | |
| | | | 15 | | | 2.5 | |
| $T_{THL}$, $T_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

* For sine wave the frequency must be greater than 10KHz for Phase Comparator II.

## DESIGN INFORMATION

This information is a guide for approximating the values of external components for the **HCC/HCF 4046B** in a Phase-Locked-Loop system. The selected external components must be within the following ranges :

$5k\Omega \leq R1, R2, R_S \leq 1M\Omega$ $\quad C1 \geq 100pF$ at $V_{DD} \geq 5V$ $\quad C1 \geq 50pF$ at $V_{DD} \geq 10V$

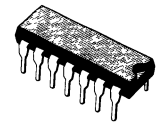
| CHARACTERISTICS | USING PHASE COMPARATOR I | | USING PHASE COMPARATOR II | |
|---|---|---|---|---|
| | VCO WITHOUT OFFSET R2 = ∞ | VCO WITH OFFSET | VCO WITHOUT OFFSET R2 = ∞ | VCO WITH OFFSET |
| VCO Frequency |  |  |  |  |
| For No Signal Input | VCO in PLL System will Adjust to centre frequency $f_o$ | | VCO in PLL System will Adjust to Lowest Operating Frequency $f_{min}$ | |
| Frequency Lock Range, $2f_L$ | $2f_L$ = full VCO frequency range<br>$2f_L = f_{max} - f_{min}$ | | | |
| Frequency Capture Range, $2f_C$ |  | | $f_C = f_L$ | |
| Loop Filter Component Selection |  | | | |
| Phase Angle Between Signal and Comparator | 90° at Centre Frequency ($f_o$), approximating 0° and 180° at ends of lock range ($2f_L$) | | Always 0° in lock | |
| Locks on Harmonics of Centre Frequency | Yes | | No | |
| Signal Input Noise Rejection | High | | Low | |

* G.S. Mosckytz "miniaturized RC filters using phase Lockedloop" BSTJ, may 1965

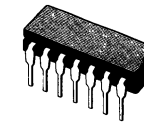
# HCC/HCF4047B

## LOW-POWER MONOSTABLE/ASTABLE MULTIVIBRATOR

- LOW POWER CONSUMPTION : SPECIAL COS/MOS OSCILLATOR CONFIGURATION
- MONOSTABLE (one-shot) OR ASTABLE (free-running) OPERATION
- TRUE AND COMPLEMENTED BUFFERED OUTPUTS
- ONLY ONE EXTERNAL R AND C REQUIRED
- BUFFERED INPUTS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

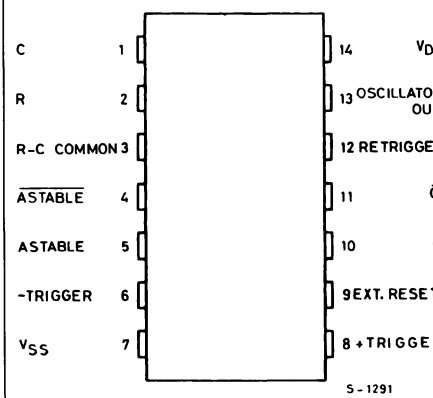
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4047BF HCF4047BM1
HCF4047BEY HCF4047BC1

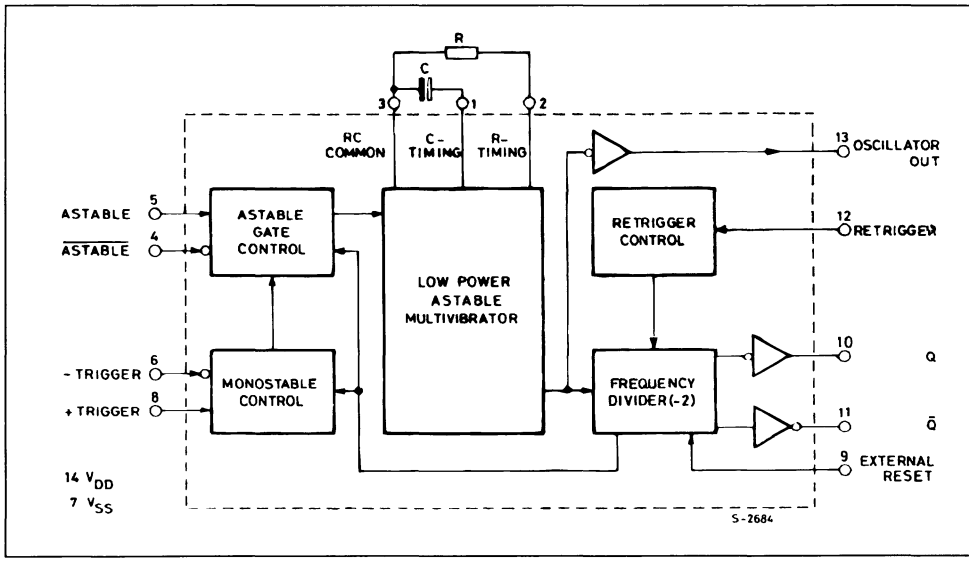
**PIN CONNECTIONS**




### DESCRIPTION

The **HCC4047B** (extended temperature range) and **HCF4047B** (intermediate temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and plastic micropackage. The **HCC/HCF4047B** consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options. Inputs include +TRIGGER -TRIGGER, ASTABLE, ASTABLE, RETRIGGER, and EXTERNAL RESET. Buffered outputs are Q, Q̄, and OSCILLATOR. In all modes of operation, an external capacitor must be connected between C-Timing and RC-Common terminals, and an external resistor must be connected between the R-Timing and RC-Common terminals. For operating modes see functional terminal connections and application notes.

## BLOCK DIAGRAM




## FUNCTIONAL TERMINAL CONNECTIONS

| Function* | Terminal Connections | | | Output Pulse From | Output Period or Pulse Width |
|---|---|---|---|---|---|
| | to $V_{DD}$ | to $V_{SS}$ | Input Pulse to | | |
| Astable Multivibrator : | | | | | |
| Free Running | 4, 5, 6, 14 | 7, 8, 9, 12 | – | 10, 11, 13 | $t_A$ (10, 11) = 4.40RC |
| True Gating | 4, 6, 14 | 7, 8, 9, 12 | 5 | 10, 11, 13 | |
| Complement Gating | 6, 14 | 5, 7, 8, 9 ,12 | 4 | 10, 11, 13 | $t_A$ (13) = 2.20RC |
| Monostable Multivibrator : | | | | | |
| Positive–Edge Trigger | 4, 14 | 5, 6, 7, 9, 12 | 8 | 10, 11 | |
| Negative–Edge Trigger | 4, 8, 14 | 5, 7, 9, 12 | 6 | 10, 11 | |
| Retriggerable | 4, 14 | 5, 6, 7, 9 | 8, 12 | 10, 11 | $t_M$ (10, 11) = 2.48RC |
| External Countdown** | 14 | 5, 6, 7, 8, 9, 12 | – | 10, 11 | |

* In all cases external capacitor and resistor between pins, 1, 2 and 3 (see logic diagrams).
** Input pulse to Reset of External Counting Chip.
External Counting Chip Output to pin 4

## ABSOLUTE MAXIMUM RATINGS

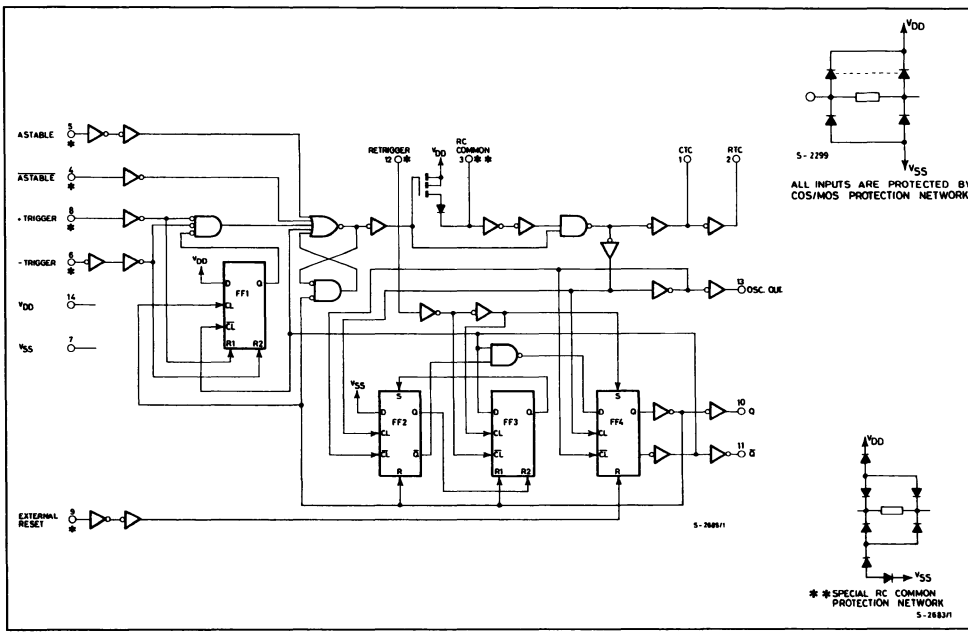
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltage values are referred to $V_{SS}$ pin voltage.

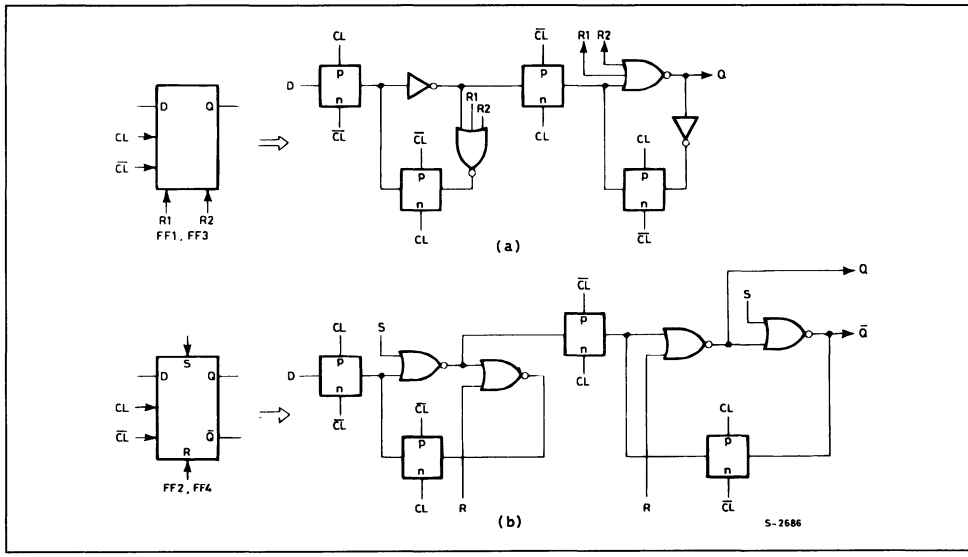
## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAM



Detail for Flip-flops FF1 and FF3 (a) and for Flip-flops FF2 and FF4 (b).




**STATIC ELECTRICAL CHARACTERISTICS** (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | |
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 1 | | 0.02 | 1 | | 30 | μA |
| | | | 0/10 | | | 10 | | 2 | | 0.02 | 2 | | 60 | |
| | | | 0/15 | | | 15 | | 4 | | 0.02 | 4 | | 120 | |
| | | | 0/20 | | | 20 | | 20 | | 0.04 | 20 | | 600 | |
| | | HCF Types | 0/ 5 | | | 5 | | 4 | | 0.02 | 4 | | 30 | |
| | | | 0/10 | | | 10 | | 8 | | 0.02 | 8 | | 60 | |
| | | | 0/15 | | | 15 | | 16 | | 0.02 | 16 | | 120 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device · + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.

## STATIC ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input leakage Curent | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.

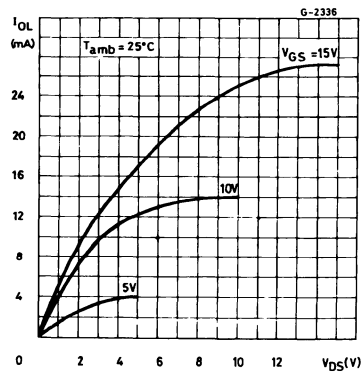
## DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall times = 20ns)

| Symbol | Parameter | | Test Conditions | $V_{DD}$ (V) | Value Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time | Astable, $\overline{\text{Astable}}$ to osc. out | | 5 | | 200 | 400 | ns |
| | | | | 10 | | 100 | 200 | |
| | | | | 15 | | 80 | 160 | |
| | | Astable, $\overline{\text{Astable}}$ to Q, $\overline{Q}$ | | 5 | | 350 | 700 | |
| | | | | 10 | | 175 | 350 | |
| | | | | 15 | | 125 | 250 | |
| | | + or − Trigger to Q, $\overline{Q}$ | | 5 | | 500 | 1000 | |
| | | | | 10 | | 225 | 450 | |
| | | | | 15 | | 150 | 300 | |

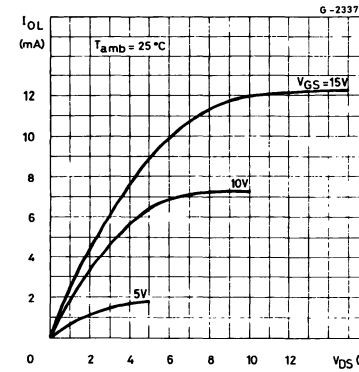
## DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | | Test Conditions | Value | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time | Retrigger to Q, $\overline{Q}$ | | 5 | | 300 | 600 | ns |
| | | | | 10 | | 150 | 300 | |
| | | | | 15 | | 100 | 200 | |
| | | External Reset to Q, $\overline{Q}$ | | 5 | | 250 | 500 | |
| | | | | 10 | | 100 | 200 | |
| | | | | 15 | | 70 | 140 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time Osc. Out Q, $\overline{Q}$ | | | 5 | | 100 | 200 | |
| | | | | 10 | | 50 | 100 | |
| | | | | 15 | | 40 | 80 | |
| $t_w$ | Input Pulse Width : | + Trigger, – Trigger | | 5 | | 200 | 400 | |
| | | | | 10 | | 80 | 160 | |
| | | | | 15 | | 50 | 100 | |
| | | Reset | | 5 | | 100 | 200 | |
| | | | | 10 | | 50 | 100 | |
| | | | | 15 | | 30 | 60 | |
| | | Retrigger | | 5 | | 300 | 600 | |
| | | | | 10 | | 115 | 230 | |
| | | | | 15 | | 75 | 150 | |
| $t_r$, $t_f$ | Input Rise and Fall Time All Inputs | | | 5 | Unlimited | | | µs |
| | | | | 10 | | | | |
| | | | | 15 | | | | |
| | Q or $\overline{Q}$ Deviation from 50% Duty Factor | | | 5 | | ± 0.5 | ± 1 | % |
| | | | | 10 | | ± 0.5 | ± 1 | |
| | | | | 15 | | ± 0.1 | ± 0.5 | |

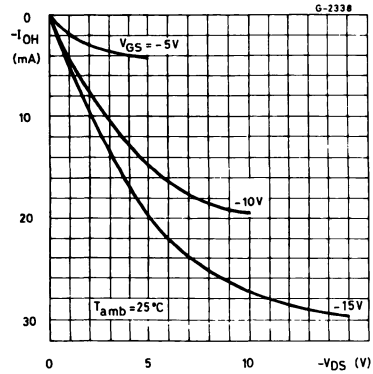
Typical Output Low (sink) Current Characteristics.



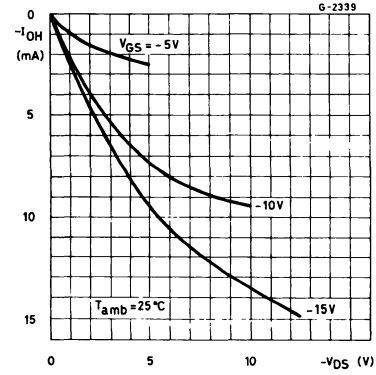

Minimum Output Low (sink) Current Characteristics.



Typical Output High (source) Current Characteristics.




Minimum Output High (source) Current Characteristics.




## APPLICATION INFORMATION

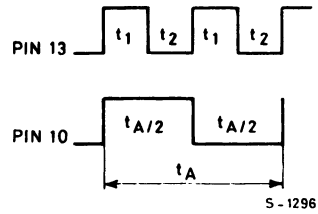
### 1 - CIRCUIT DESCRIPTION

Astable operation is enabled by a high level on the ASTABLE input. The period of the square wave at the Q and Q Outputs in this mode of operation is a function of the external components employed. "True" input pulses on the ASTABLE input or "Complement" pulses on the ASTABLE input allow the circuit to be used as a gatable multivibrator. The OSCILLATOR output period will be half of the Q terminal output in the astable mode. However, a 50% duty cycle is not guaranteed at this output. In the monostable mode, positive-edge triggering is accomplished by application of a leading-edge pulse to the +TRIGGER input and a low level to the –TRIGGER input. For negative-edge triggering, a trailing-edge pulse is applied to the –TRIGGER and a high level is applied to the +TRIGGER. Input pulses may be of any duration relative to the output pulse. The multivibrator can be retriggered (on the leading edge only) by applying a common pulse to both the RETRIGGER and +TRIGGER inputs. In this mode the output pulse remains high as long as the input pulse period is shorter than the period determined by the RC components. An external countdown option can be implemented by coupling "Q" to an external "N" counter and resetting the counter with the trigger pulse. The counter output pulse is fed back to the ASTABLE input and has a duration equal to N times the period of the multivibrator. A high level on the EXTERNAL RESET input assures no output pulse during an "ON" power condition. This input can also be activated to terminate the output pulse at any time. In the monostable mode, a high-level or power-on reset pulse, must be applied to the EXTERNAL RESET whenever $V_{DD}$ is applied.

### 2 - ASTABLE MODE

The following analysis presents worst-case variations from unit-to-unit as a function of transfer-voltage ($V_{TR}$) shift (33% – 67% $V_{DD}$) for free-running (astable) operation.

ASTABLE MODE WAVEFORMS.




$$t_1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_{TR}}$$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}}$$

$$t_A = 2(t_1 + t_2) = -2RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2V_{DD} - V_{TR})}$$

Typ : $V_{TR} = 0.5\ V_{DD}$ $t_A = 4.40\ RC$

Min : $V_{TR} = 0.33\ V_{DD}$ $t_A = 4.62\ RC$

Max : $V_{TR} = 0.67\ V_{DD}$ $t_A = 4.62\ RC$

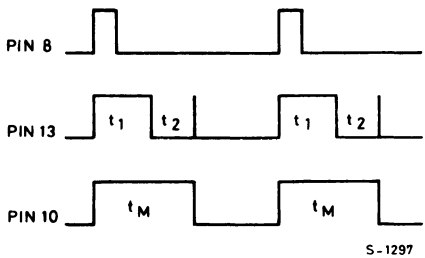
thus if $t_A = 4.40\ RC$ is used, the maximum variation will be (+ 5.0%, – 0.0%)

In addition to variations from unit-to-unit, the astable period may vary as a function of frequency with respect to $V_{DD}$ and temperature.

3 - MONOSTABLE MODE

The following analysis presents worst-case variations from unit-to-unit as a function of transfer-voltage ($V_{TR}$) shift (33% – 67% $V_{DD}$) for one-shot (monostable) operation.

MONOSTABLE WAVEFORMS.




$$t_1 = -RC \ln \frac{V_{TR}}{2V_{DD}}$$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}}$$

$$t_M = (t_1 + t_2) = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(2V_{DD} - V_{TR})(2V_{DD})}$$

Where $t_M$ = monostable mode pulse width. Values for $t_M$ are as follows :

Typ : $V_{TR} = 0.5\ V_{DD}$ $t_M = 2.48\ RC$

Min : $V_{TR} = 0.33\ V_{DD}$ $t_M = 2.71\ RC$

Max : $V_{TR} = 0.67\ V_{DD}$ $t_M = 2.48\ RC$

Thus if $t_M = 2.48\ RC$ is used, the maximum variation will be (+ 9.3%, – 0.0%).

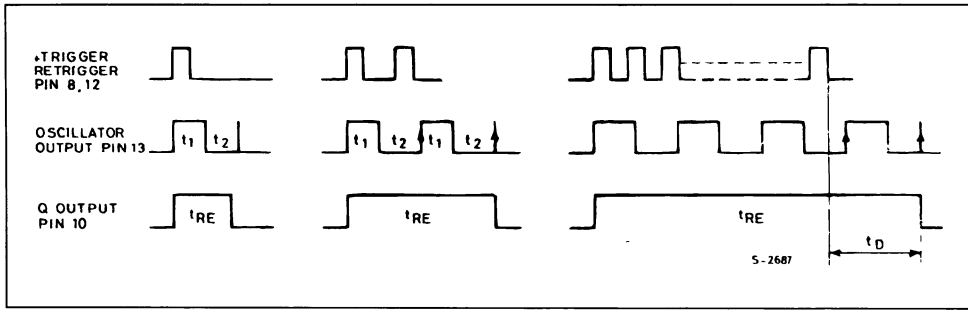
Note : In the astable mode, the first positive half cycle has a duration of $T_M$ ; succeeding durations are $t_A/2$.

In addition to variations from unit to unit, the monostable pulse width may vary as a function of frequency with respect to $V_{DD}$ and temperature.

4 - RETRIGGER MODE

The **HCC/HCF4047B** can be used in the retrigger mode to extend the output-pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to terminals 8 and 12, and the output is taken from terminal 10 or 11. As shown in fig. A normal monostable action is obtained when one retrigger pulse is applied. Extended pulse duration is obtained when more than one pulse is applied. For two input pulses, $t_{RE} = t_1' + t_1 + 2t_2$. For more than two pulses, $t_{RE}$ (Q OUTPUT) terminates at some variable time $t_D$ after the termination of the last retrigger pulse. $t_D$ is variable because $t_{RE}$ (Q OUTPUT) terminates after the second positive edge of the oscillator output appears at flip-flop 4 (see logic diagram).

**Figure A** : Retrigger-mode Waveforms.




5 - EXTERNAL COUNTER OPTION

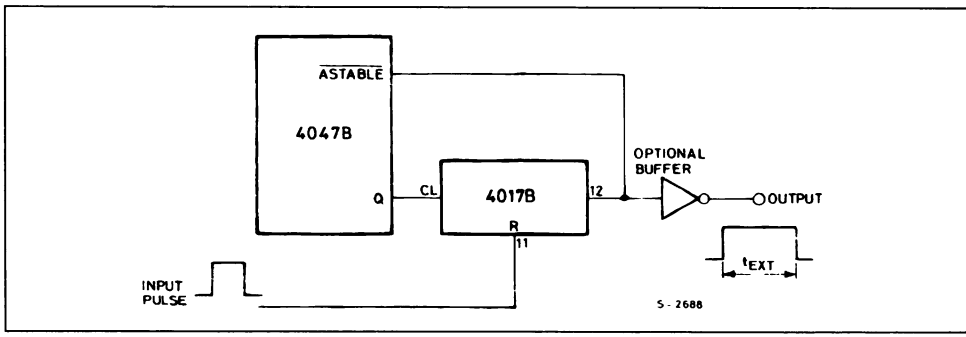
Time $t_M$ can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time.

A typical implementation is shown in fig. B. The pulse duration at the output is

$$t_{ext} = (N - 1)\ (t_A) + (t_M + t_A/2)$$

Where $t_{ext}$ = pulse duration of the circuitry, and N is the number of counts used.

**Figure B** : Implementation of External Counter Option.




6 - POWER CONSUMPTION

In the standby mode (Monostable or Astable), power dissipation will be a function of leakage current in the circuit, as shown in the static electrical characteristics. For dynamic operation, the power needed to charge the external timing capacitor C is given by the following formula :

Astable Mode : $P = 2CV^2f$. (Output at Pin 13)

$P = 4CV^2f$. (Output at Pin 10 and 11)

Monostable Mode : $P = \dfrac{(2.9CV^2)\ (\text{Duty Cycle})}{T}$

(Output at Pin 10 and 11)

The circuit is designed so that most of the total power is consumed in the external components. In practice, the lower the values of frequency and voltage used, the closer the actual power dissipation will be to the calculated value.

Because the power dissipation does not depend on R, a design for minimum power dissipation would be a small value of C. The value of R would depend on the desired period (within the limitations discussed above).

7 - TIMING-COMPONENT LIMITATIONS

The capacitor used in the circuit should be non-polarized and have low leakage (i.e. the parallel resistance of the capacitor should be an order of magnitude greater than the external resistor used). Three is no upper or lower limit for either R or C value to maintain oscillation.

However, in consideration of accuracy, C must be much larger than the inherent stray capacitance in

the system (unless this capacitance can be measured and taken into account). R must be much larger than the COS/MOS "ON" resistance in series with it, which typically is hundreds of ohms. In addition, with very large values of R, some short-term instability with respect to time may be noted.

The recommended values for these components to maintain agreement with previously calculated formulas without trimming should be :

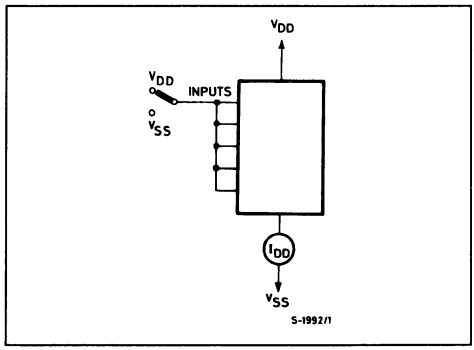
$C \geq 100pF$, up to any practical value, for astable modes ;

$C \geq 1000pF$, up to any practical value, for monostable modes.

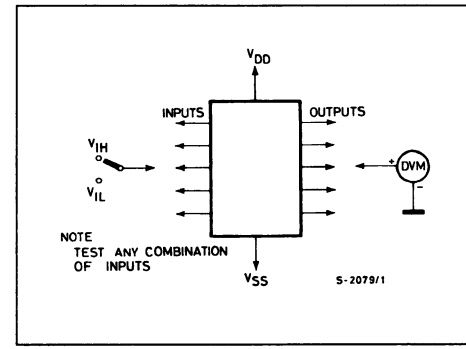
$10K\Omega \leq R \leq 1M\Omega$.

## TEST CIRCUITS

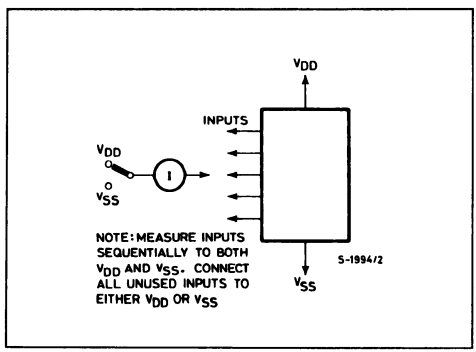
Quiescent Device Current.




Input Voltage.

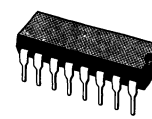



Input Current.

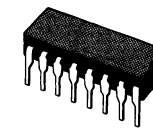


# MULTIFUNCTION EXPANDABLE 8-INPUT GATE

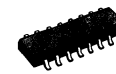
- THREE-STATE OUTPUT
- MANY LOGIC FUNCTIONS AVAILABLE IN ONE PACKAGE
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
Plastic Package



**F**
Ceramic Frit Seal Package



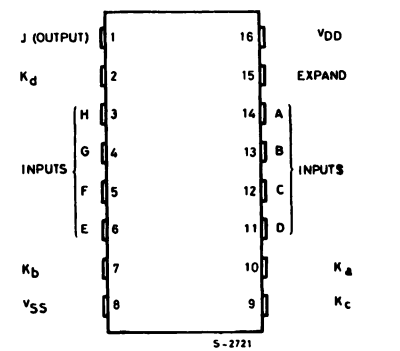
**M1**
Micro Package

**C1**
Plastic Chip Carrier

**ORDER CODES :**

HCC4048BF HCF4048BM1
HCF4048BEY HCF4048BC1

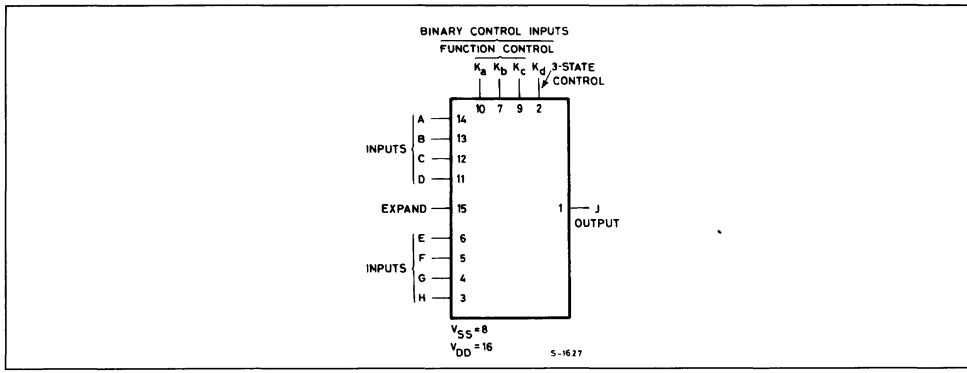
**PIN CONNECTIONS**




## DESCRIPTION

The **HCC4048B** (extended temperature range) and **HCF4048B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF4048B** is an 8-input gate having four control inputs. Three binary control inputs - Ka, Kb, and Kc - provide the implementation of eight different logic functions. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR and AND/NOR. A fourth control input-Kd-provides the user with a 3-state output. When control input Kd is high the output is either a logic 1 or a logic 0 depending on the inner states. When control input Kd is low, the output is an open circuit. This feature enables the user to connect this device to a common bus line. In addition to the eight input lines, an EXPAND input is provided that permits the user to increase the number of inputs to one **HCC/HCF4048B**. For example, two **HCC/HCF4048B**'s can be cascaded to provide a 16-input multifunction gate. When the EXPAND input is not used, it should be connected to $V_{SS}$.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

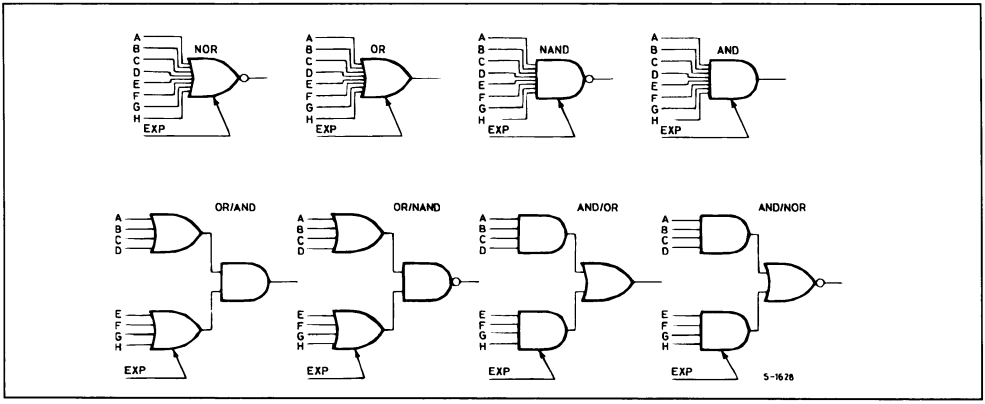
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for external periods may affect device reliability

* All voltages values are referred to $V_{SS}$ pin voltage.

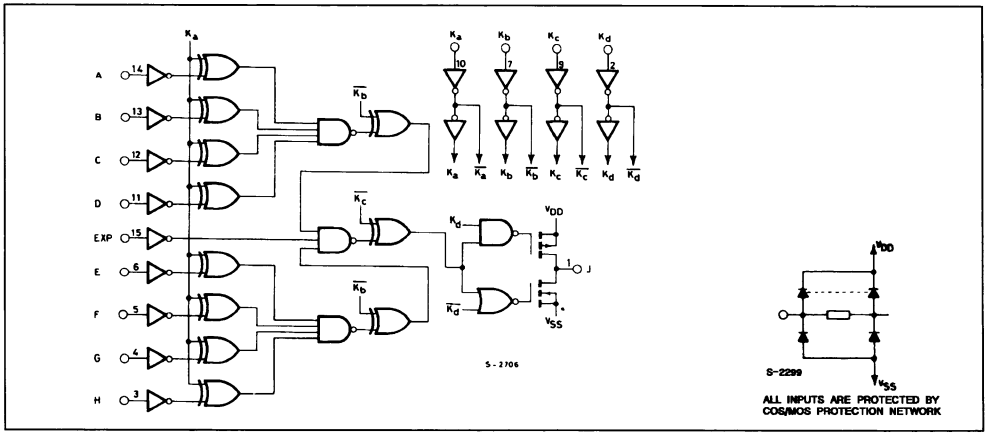
## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## BASIC LOGIC CONFIGURATIONS




## LOGIC DIAGRAM




## FUNCTION TRUTH TABLE

| Output Function | Boolean Expression | $K_a$ | $K_b$ | $K_c$ | Unused Input |
|---|---|---|---|---|---|
| NOR | $J = \overline{A+B+C+D+E+F+G+H}$ | 0 | 0 | 0 | $V_{SS}$ |
| OR | $J = A+B+C+D+E+F+G+H$ | 0 | 0 | 1 | $V_{SS}$ |
| OR/AND | $J = (A+B+C+D)\cdot(E+F+G+H)$ | 0 | 1 | 0 | $V_{SS}$ |
| OR/NAND | $J = \overline{(A+B+C+D)\cdot(E+F+G+H)}$ | 0 | 1 | 1 | $V_{SS}$ |
| AND | $J = ABCDEFGH$ | 1 | 0 | 0 | $V_{DD}$ |
| NAND | $J = \overline{ABCDEFGH}$ | 1 | 0 | 1 | $V_{DD}$ |
| AND/NOR | $J = \overline{ABCD + EFGH}$ | 1 | 1 | 0 | $V_{DD}$ |
| AND/OR | $J = ABCD + EFGH$ | 1 | 1 | 1 | $V_{DD}$ |

$K_d = 1$ Normal Inverter Action
$K_d = 0$ High Impedance Output

EXPAND Input = 0

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

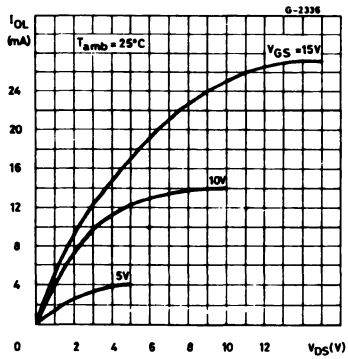
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 0.25 | | 0.01 | 0.25 | | 7.5 | μA |
| | | | 0/10 | | | 10 | | 0.5 | | 0.01 | 0.5 | | 15 | |
| | | | 0/15 | | | 15 | | 1 | | 0.01 | 1 | | 30 | |
| | | | 0/20 | | | 20 | | 5 | | 0.02 | 5 | | 150 | |
| | | HCF Types | 0/ 5 | | | 5 | | 1 | | 0.01 | 1 | | 7.5 | |
| | | | 0/10 | | | 10 | | 2 | | 0.01 | 2 | | 15 | |
| | | | 0/15 | | | 15 | | 4 | | 0.01 | 4 | | 30 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | ± $10^{-5}$ | ± 0.01 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | ± $10^{-5}$ | ± 0.3 | | ± 1 | |
| $I_{OH}$ | 3-state Output Current | HCC Types | 0/18 | 0/18 | | 18 | | ± 0.4 | | ± $10^{-4}$ | ± 0.4 | | ± 12 | μA |
| | | HCF Types | 0/15 | 0/15 | | 15 | | ± 1.0 | | ± $10^{-4}$ | ± 1.0 | | ± 7.5 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$ = − 125°C for **HCC** device : − 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V,

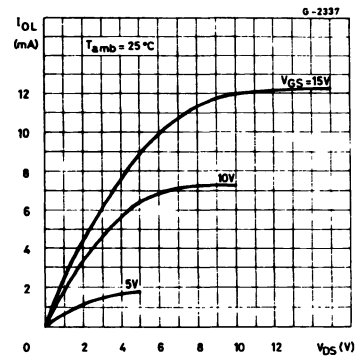
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ = 0.3%/°C values, all input rise and fall time = 20ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time Inputs to Output and Ka to Output | | 5 | | 300 | 600 | ns |
| | | | 10 | | 150 | 300 | |
| | | | 15 | | 120 | 240 | |
| | Kb to Output | | 5 | | 225 | 450 | |
| | | | 10 | | 85 | 170 | |
| | | | 15 | | 55 | 110 | |
| | Kc to Output | | 5 | | 140 | 280 | |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| | Expand Input to Output | | 5 | | 190 | 380 | |
| | | | 10 | | 90 | 180 | |
| | | | 15 | | 65 | 130 | |
| $t_{PHZ}$, $t_{PLZ}$ $t_{PZH}$, $t_{PZL}$ | 3–state Propagation Delay Time Kd to Output | $R_L$ = 1kΩ | 5 | | 80 | 160 | |
| | | | 10 | | 35 | 70 | |
| | | | 15 | | 25 | 50 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| 3-state Output Capacitance | | | | | 5 | 10 | pF |

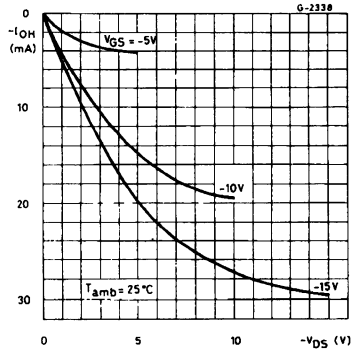
Typical Output Low (sink) Current Characteristics.



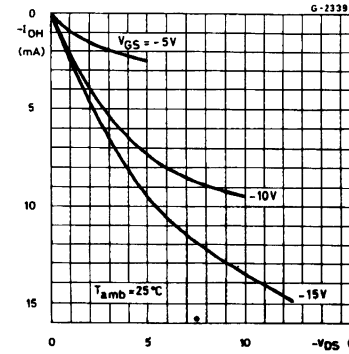

Minimum Output Low (sink) Current Characteristics.



Typical Output High (source) Current Characteristics.

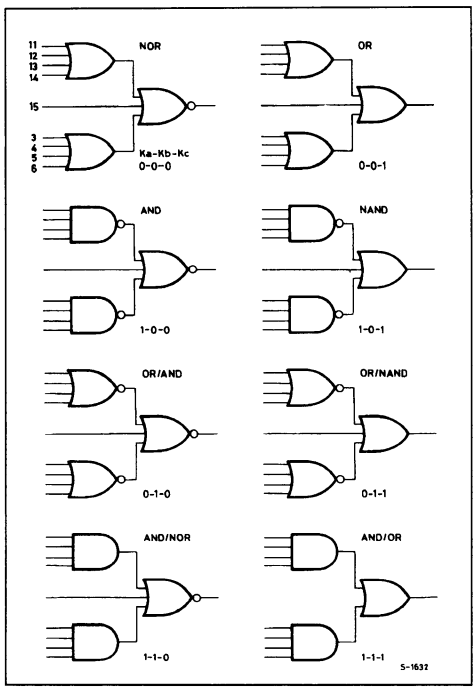



Minimum Output high (source) Current Characteristics.




## APPLICATIONS OF EXPAND INPUT

ACTUAL-CIRCUIT LOGIC CONFIGURATIONS




EXPANSION LOGIC AND TRUTH TABLE

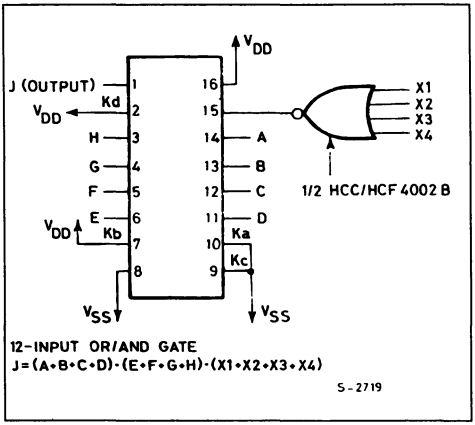
IMPLEMENTATION OF EXPAND INPUT FOR 9 OR MORE INPUTS

| OUTPUT FUNCTION | FUNCTION NEEDED AT EXPAND INPUT | OUTPUT BOOLEAN EXPRESSION |
|---|---|---|
| NOR | OR | $J = \overline{(A+B+C+D+E+F+G+H) + (EXP)}$ |
| OR | OR | $J = (A+B+C+D+E+F+G+H) + (EXP)$ |
| AND | NAND | $J = (ABCDEFGH)\ (EXP)$ |
| NAND | NAND | $J = \overline{(ABCDEFGH)\ (EXP)}$ |
| OR/AND | NOR | $J = (A+B+C+D)\ (E+F+G+H)\ (EXP)$ |
| OR/NAND | NOR | $J = \overline{(A+B+C+D) \cdot (E+F+G+H)\ (EXP)}$ |
| AND/NOR | AND | $J = \overline{(ABCD) + (EFGH) + (EXP)}$ |
| AND/OR | AND | $J = (ABCD) + (EFGH) + (EXP)$ |

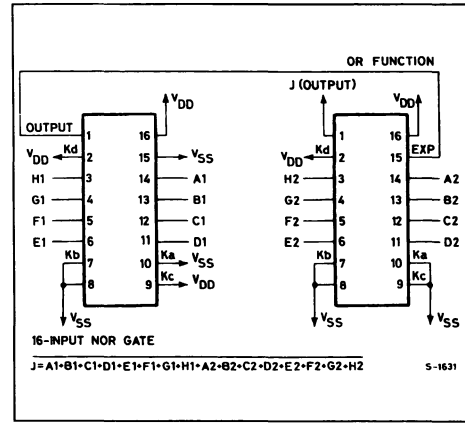
**Note :** (EXP) designates the EXPAND function (i.e., $X_1 + X_2 + .. X_N$).

## APPLICATIONS OF EXPAND INPUT (continued)

12-Input or/and Gate.

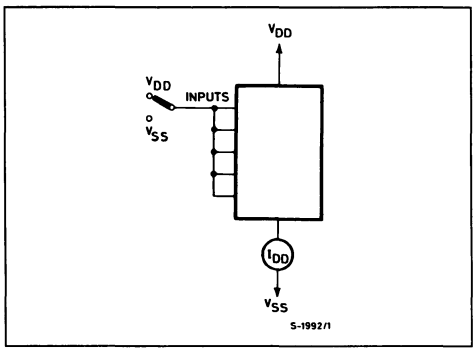



16-Input Nor Gate.

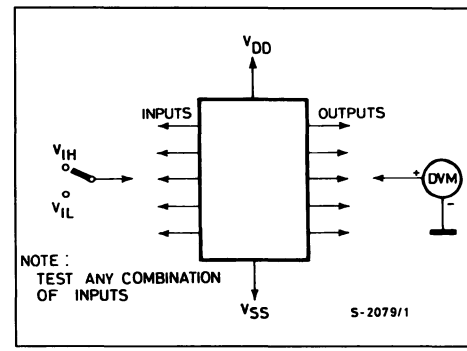



## TEST CIRCUITS

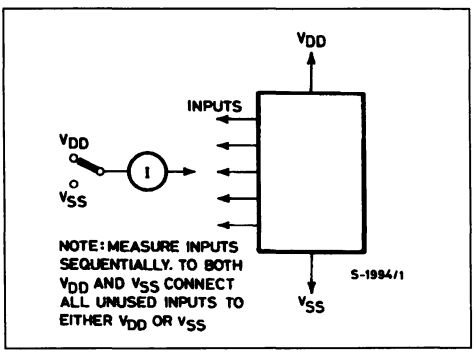
Quiescent Device Current.




Input Voltage.




Input Current.



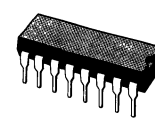
SGS-THOMSON MICROELECTRONICS

# HCC/HCF4049UB
# HCC/HCF4050B

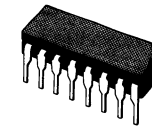
## HEX BUFFER/CONVERTERS

**4049UB INVERTING TYPE**
**4050B NON-INVERTING TYPE**

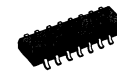
- HIGH SINK CURRENT FOR DRIVING 2 TTL LOADS
- HIGH-TO-LOW LEVEL LOGIC CONVERSION
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- HIGH "SINK" AND "SOURCE" CURRENT CAPABILITY
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)



**M1**
(Micro Package)

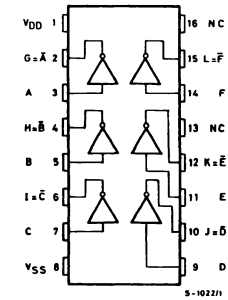
**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

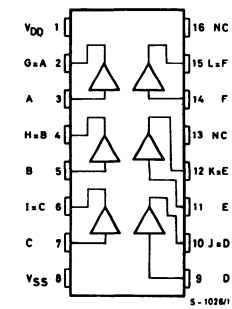
HCC40XXBF HCF40XXBM1
HCF40XXBEY HCF40XXBC1

**PIN CONNECTIONS**

**4049UB**




**4050B**

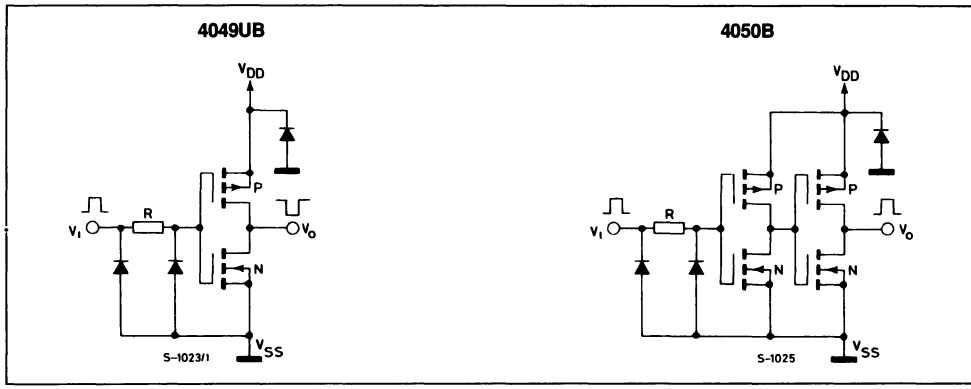



### DESCRIPTION

The **HCC4049UB/4050B** (extended temperature range) and the **HCF4049UB/4050B** (intermediate temperature range) are monolithic integrated circuits available in 16-lead dual in-line plastic or ceramic package and plastic micro package.

The **HCC/HCF4049UB/4050B** are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage ($V_{DD}$). The input-signal high level ($V_{IH}$) can exceed the $V_{DD}$ supply voltage when these devices are used for logic level conversions. These devices are intended for use as COS/MOS to DTL/TTL converters and can drive directly two DTL/TTL loads ($V_{DD} = 5V$, $V_{OL} \leq 0.4V$, and $I_{OL} \geq 3.2mA$).

## SCHEMATIC DIAGRAMS (1 of 6 identical units)




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

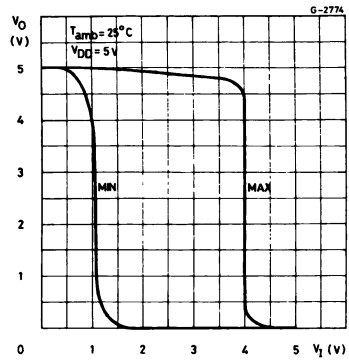
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Supply Current | HCC Types | 0/ 5 | | 5 | | 1 | | 0.02 | 1 | | 30 | µA |
| | | | 0/10 | | 10 | | 2 | | 0.02 | 2 | | 60 | |
| | | | 0/15 | | 15 | | 4 | | 0.02 | 4 | | 120 | |
| | | | 0/20 | | 20 | | 20 | | 0.04 | 20 | | 600 | |
| | | HCF Types | 0/ 5 | | 5 | | 4 | | 0.02 | 4 | | 30 | |
| | | | 0/10 | | 10 | | 8 | | 0.02 | 8 | | 60 | |
| | | | 0/15 | | 15 | | 16 | | 0.02 | 16 | | 120 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage (4049UB) | | | 0.5 | 5 | 4 | | 4 | | | 4 | | V |
| | | | | 1 | 10 | 8 | | 8 | | | 8 | | |
| | | | | 2 | 15 | 12 | | 12 | | | 12 | | |
| $V_{IH}$ | Input High Voltage (4050B) | | | 4.5 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 9 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 13.5 | 16 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage (4049UB) | | | 4.5 | 5 | | 1 | | | 1 | | 1 | V |
| | | | | 9 | 10 | | 2 | | | 2 | | 2 | |
| | | | | 13 | 15 | | 3 | | | 3 | | 3 | |
| $V_{IL}$ | Input Low Voltage (4050B) | | | 0.5 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 1.5 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | 5 | 1.6 | | –1.25 | – 6.4 | | – 0.9 | | mA |
| | | | 0/ 5 | 4.6 | 5 | 0.64 | | –0.51 | – 1.6 | | –0.36 | | |
| | | | 0/10 | 9.5 | 10 | 1.6 | | –1.30 | – 3.6 | | – 0.9 | | |
| | | | 0/15 | 13.5 | 15 | 4.7 | | –3.75 | – 12 | | – 2.7 | | |
| | | HCF Types | 0/ 5 | 2.5 | 5 | 1.5 | | –1.25 | – 6.4 | | – 1 | | |
| | | | 0/ 5 | 4.6 | 5 | 0.61 | | –0.51 | – 1.6 | | –0.42 | | |
| | | | 0/10 | 9.5 | 10 | 1.5 | | –1.25 | – 3.6 | | – 1 | | |
| | | | 0/15 | 13.5 | 15 | 4.5 | | –3.75 | – 12 | | – 3 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | 5 | 3.75 | | 3.2 | 6.4 | | 2.2 | | mA |
| | | | 0/10 | 0.5 | 10 | 10 | | 8 | 16 | | 5.6 | | |
| | | | 0/15 | 1.5 | 15 | 30 | | 24 | 48 | | 17 | | |
| | | HCF Types | 0/ 5 | 0.4 | 5 | 3.6 | | 3.2 | 6.4 | | 2.6 | | |
| | | | 0/10 | 0.5 | 10 | 9.6 | | 8 | 16 | | 6.6 | | |
| | | | 0/15 | 1.5 | 15 | 28 | | 24 | 48 | | 19 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | µA |
| | | HCF Types | 0/15 | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | 4049UB | Any Input | | | | | | 15 | 22.5 | | | pF |
| | | 4050B | | | | | | | 5 | 7.5 | | | |

(*) $T_{Low}$ = – 55°C for **HCC** device : – 40°C for **HCF** device.
$T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin (only **HCC/HCF4050B** type) for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.

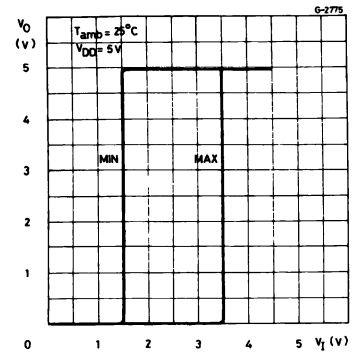
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall times = 20ns)

| Symbol | Parameter | Test Conditions | | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$ | Propagation Delay Time (4049UB) | | 5 | 5 | | 60 | 120 | ns |
| | | | 10 | 10 | | 32 | 65 | |
| | | | 10 | 5 | | 45 | 90 | |
| | | | 15 | 15 | | 25 | 50 | |
| | | | 15 | 5 | | 45 | 90 | |
| $t_{PLH}$ | Propagation Delay Time (4050B) | | 5 | 5 | | 70 | 140 | ns |
| | | | 10 | 10 | | 40 | 80 | |
| | | | 10 | 5 | | 45 | 90 | |
| | | | 15 | 15 | | 30 | 60 | |
| | | | 15 | 5 | | 40 | 80 | |
| $t_{PHL}$ | Propagation delay Time (4049UB) | | 5 | 5 | | 32 | 65 | |
| | | | 10 | 10 | | 20 | 40 | |
| | | | 10 | 5 | | 15 | 30 | |
| | | | 15 | 15 | | 15 | 30 | |
| | | | 15 | 5 | | 10 | 20 | |
| $t_{PHL}$ | Propagation Delay Time (4050B) | | 5 | 5 | | 55 | 110 | ns |
| | | | 10 | 10 | | 22 | 55 | |
| | | | 10 | 5 | | 50 | 100 | |
| | | | 15 | 15 | | 15 | 30 | |
| | | | 15 | 5 | | 50 | 100 | |
| $t_{TLH}$ | Transition Time | | 5 | 5 | | 80 | 160 | ns |
| | | | 10 | 10 | | 40 | 80 | |
| | | | 15 | 15 | | 30 | 60 | |
| $t_{THL}$ | Transition Time | | 5 | 5 | | 30 | 60 | |
| | | | 10 | 10 | | 20 | 40 | |
| | | | 15 | 15 | | 15 | 30 | |

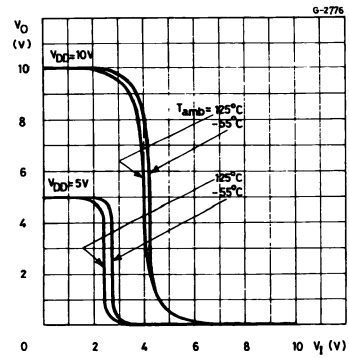
Minimum and Maximum Voltage Transfer Characteristics for 4049UB.



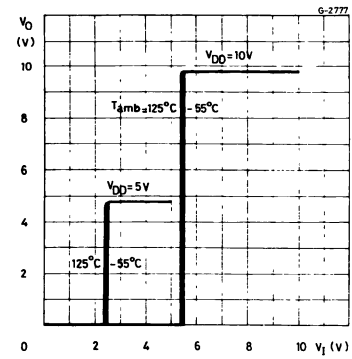

Minimum and Maximum Voltage Transfer Characteristics for 4050B.



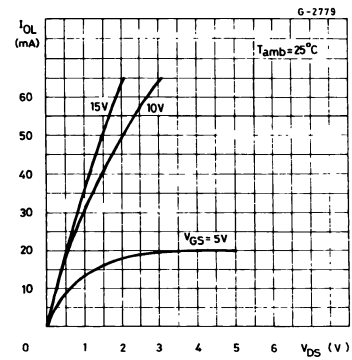

Typical Voltage Transfer Characteristics as a Function of Temperature for 4049UB.



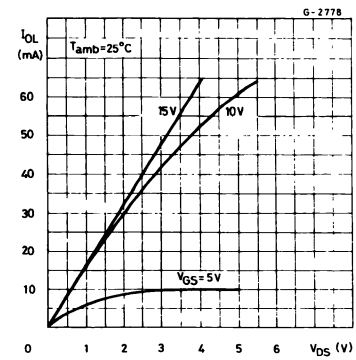

Typical Voltage Transfer Characteristics as a Function of Temperature for 4050B.



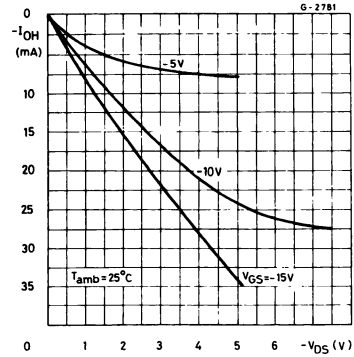

Typical Output Low (sink) Current Characteristics.



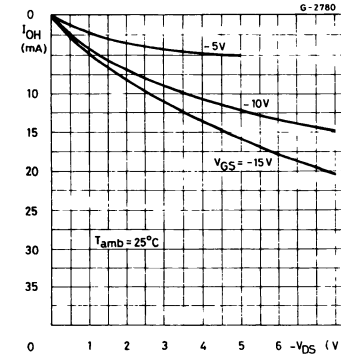

Minimum Output Low (sink) Current Characteristics.



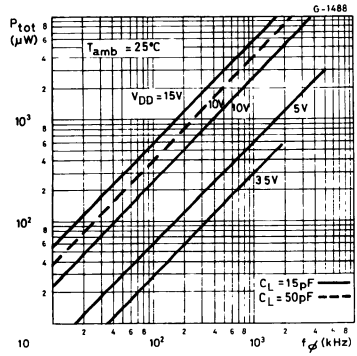
Typical Output High (source) Current Characteristics.



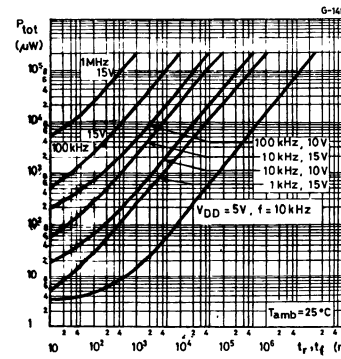

Minimum Output High (source) Current Characteristics.



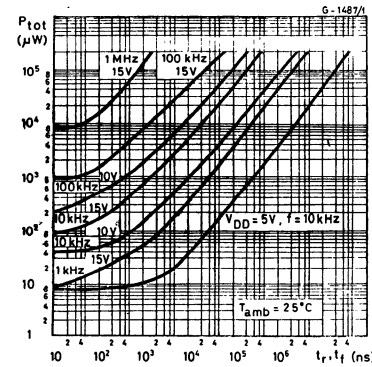

Typical Power Dissipation per Buffer/Inverter vs. Frequency.



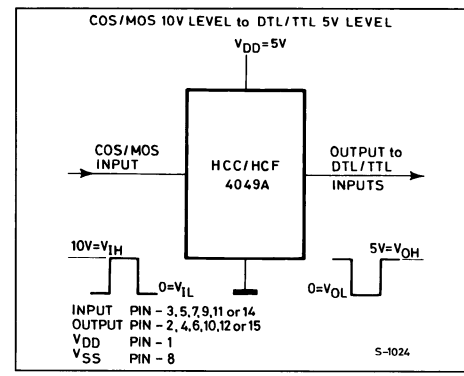

Typical Power Dissipation vs. Input Transition Time per Inverter for 4049UB.




Typical Power Dissipation vs. Input Transition Time per Inverter for 4050B.

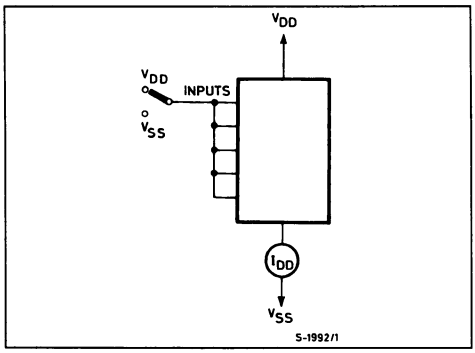



Logic-Level Conversion Application.

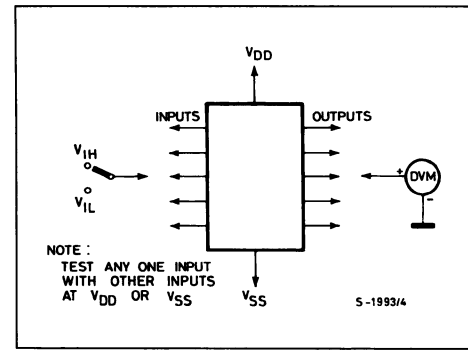


## TEST CIRCUITS

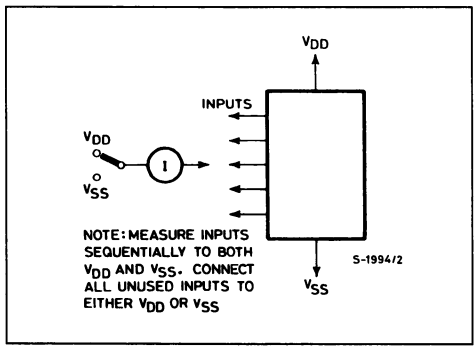
Quiescent Device Current.




Input Voltage.




Input Current.



# HCC4051B/52B/53B
# HCF4051B/52B/53B

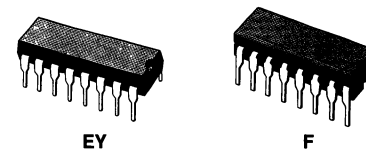
## ANALOG MULTIPLEXERS-DEMULTIPLEXERS

**4051B - SINGLE 8-CHANNEL**

**4052B - DIFFERENTIAL 4-CHANNEL**

**4053B - TRIPLE 2-CHANNEL**

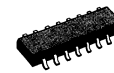
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- LOW "ON" RESISTANCE : 125Ω (typ.) OVER 15V p.p. SIGNAL-INPUT RANGE FOR $V_{DD}$-$V_{EE}$ = 15V
- HIGH "OFF" RESISTANCE : CHANNEL LEAKAGE ± 100pA (typ.) $V_{DD} - V_{EE}$ = 18V
- BINARY ADDRESS DECODING ON CHIP
- VERY LOW QUIESCENT POWER DISSIPATION UNDER ALL DIGITAL CONTROL INPUT AND SUPPLY CONDITIONS : 0.2 µW (typ.), $V_{DD} - V_{SS} = V_{DD} - V_{EE}$ = 10V
- MATCHED SWITCH CHARACTERISTICS : $R_{ON}$ = 5Ω (typ.) for $V_{DD} - V_{EE}$ = 15V
- WIDE RANGE OF DIGITAL AND ANALOG SIGNAL LEVELS : DIGITAL 3 TO 20V, ANALOG TO 20V p.p.
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100mA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY** (Plastic Package)



**F** (Ceramic Frit Seal Package)



**M1** (Micro Package)

**C1** (Plastic Chip Carrier)

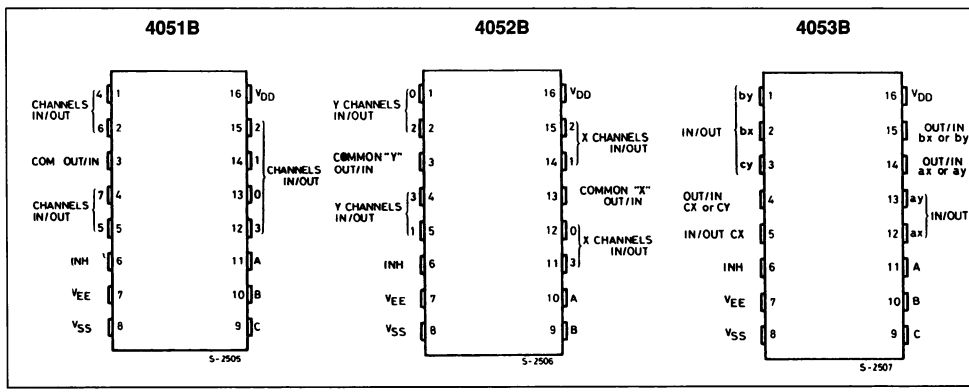
**ORDER CODES :**

HCC40XXBF HCF40XXBM1
HCF40XXBEY HCF40XXBC1

### DESCRIPTION

The **HCC 4051B, 4052B** and **4053B** (extended temperature range) and **HCF4051B, 4052B** and **4053B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and plastic micropackage. **HCC/HCF4051B, HCC/HCF4052B**, and **HCC/HCF4053B** analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedance and very low OFF

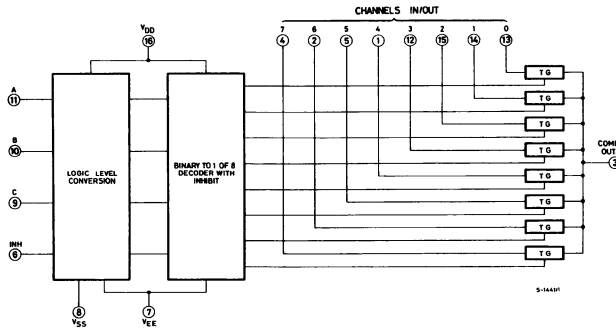
### PIN CONNECTIONS



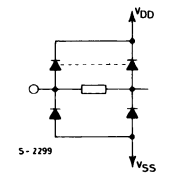
leakage current. These multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD}$ – $V_{SS}$ and $V_{DD}$ – $V_{EE}$ supply-voltage ranges, independent of the logic state of the control signals. When a-logic "1" is present at the inhibit input terminal all channel are off. The **HCC/HCF4051B** is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output. The **HCC/HCF4052B** is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs. The **HCC/HCF4053B** is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a singlepole double-throw configuration.

## FUNCTIONAL DIAGRAMS AND TRUTH TABLES

**4051B**

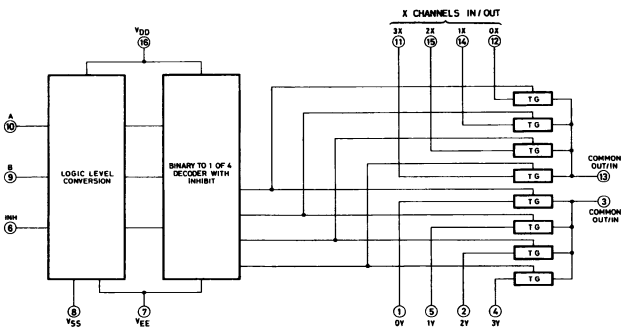



| Input States | | | | "On" Channel (S) |
|---|---|---|---|---|
| Inhibit | C | B | A | |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | X | X | X | None |

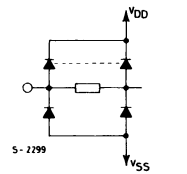



ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

**4052B**




| Inhibit | B | A | |
|---|---|---|---|
| 0 | 0 | 0 | 0x, 0y |
| 0 | 0 | 1 | 1x, 1y |
| 0 | 1 | 0 | 2x, 2y |
| 0 | 1 | 1 | 3x, 3y |
| 1 | X | X | None |



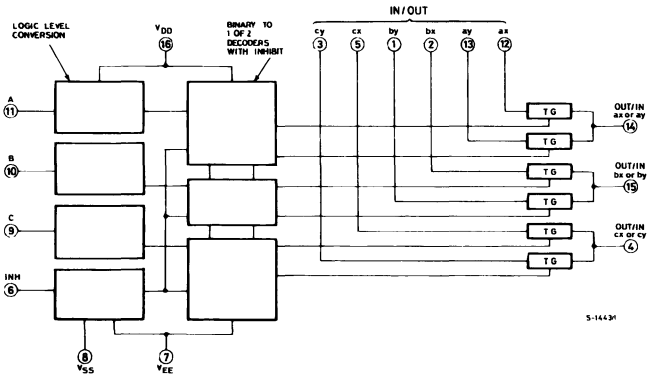

ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

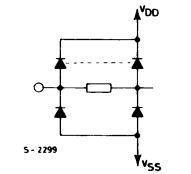
## FUNCTIONAL DIAGRAMS AND TRUTH TABLES (continued)

**4053**

| Inhibit | A or B or C | |
|---|---|---|
| 0 | 0 | ax or bx or cx |
| 0 | 1 | ay or by or cy |
| 1 | X | None |

X = Don't care




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability

* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_{IS}$ (V) | $V_{EE}$ (V) | $V_{SS}$ (V) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25 °C Min. | 25 °C Typ. | 25 °C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Device Current | HCC Types | | | | 5 | | 5 | | 0.04 | 5 | | 150 | µA |
| | | | | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| **SWITCH** | | | | | | | | | | | | | | |
| ON | Resistance | HCC Types | $0 \le V_I \le V_{DD}$ | 0 | 0 | 5 | | 880 | | 470 | 1050 | | 1200 | Ω |
| | | | | | | 10 | | 310 | | 180 | 400 | | 580 | |
| | | | | | | 15 | | 220 | | 125 | 280 | | 400 | |
| | | HCF Types | $0 \le V_I \le V_{DD}$ | 0 | 0 | 5 | | 880 | | 470 | 1050 | | 1200 | |
| | | | | | | 10 | | 330 | | 180 | 400 | | 520 | |
| | | | | | | 15 | | 230 | | 125 | 280 | | 360 | |
| ΔON | Resistance $\Delta R_{ON}$ (between any 2 channels) | | | 0 | 0 | 5 | | | | 10 | | | | Ω |
| | | | | | | 10 | | | | 10 | | | | |
| | | | | | | 15 | | | | 5 | | | | |
| OFF (•) Channel Leakage Current | Any Channel OFF | HCC Types | | 0 | 0 | 18 | | 100 | | ± 0.1 | 100 | | 1000 | nA |
| | All Channels OFF (common OUT/IN) | HCC Types | | 0 | 0 | 18 | | 100 | | ± 0.1 | 100 | | 1000 | nA |
| | Any Channel OFF | HCF Types | | 0 | 0 | 15 | | 300 | | ± 0.1 | 300 | | 1000 | nA |
| | All Channels OFF (common OUT/IN) | HCF Types | | 0 | 0 | 15 | | 300 | | ± 0.1 | 300 | | 1000 | nA |
| C Capacitance | Input | | | | | | | | | 5 | | | | pF |
| | Output 4051 | | | − 5 | − 5 | 5 | | | | 30 | | | | |
| | Output 4052 | | | | | | | | | 18 | | | | |
| | Output 4053 | | | | | | | | | 9 | | | | |
| | Feedthrough | | | | | | | | | 0.2 | | | | |
| **CONTROL** (Address or Inhibit) | | | | | | | | | | | | | | |
| $V_{IL}$ | Input Low Voltage | | = $V_{DD}$ Thru 1KΩ | $V_{EE}$ = $V_{SS}$ $R_L$ = 1KΩ to $V_{SS}$ $I_{IS}$ < 2µA (on all off channels) | | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | | | 10 | | 3 | | | 3 | | 3 | |
| | | | | | | 15 | | 4 | | | 4 | | 4 | |
| $V_{IH}$ | Input High Voltage | | | | | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | | | 10 | 7 | | 7 | | | 7 | | |
| | | | | | | 15 | 11 | | 11 | | | 11 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | $V_I$ = 0/18V | | | 18 | | ± 0.1 | | $\pm 10^{-3}$ | ± 0.1 | | ± 1 | µA |
| | | HCF Types | $V_I$ = 0/15V | | | 15 | | ± 0.3 | | $\pm 10^{-3}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | Any Address or Inhibit Input | | | | | | | 5 | 7.5 | | | pF |

(•) Determined by minimum feasible leakage measurement for automatic testing
(*) $T_{Low}$ = − 55°C for **HCC** device · − 40°C for **HCF** device
(*) $T_{High}$ = + 125°C for **HCC** device . + 85°C for **HCF** device

## DYNAMIC ELECTRICAL CHARACTERISTICS

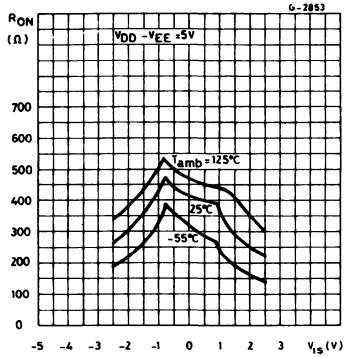
($T_{amb}$ = 25°C, $C_L$ = 50pF all input square wave rise and fall time = 20ns)

| Parameter | Test Conditions | | | | | | | | Value | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $V_{EE}$ (V) | $R_L$ (kΩ) | $f_i$ (kHz) | $V_{IS}$ (V) | $V_{SS}$ (V) | $V_{DD}$ (V) | | | Typ. | Max. | |
| **SWITCH** | | | | | | | | | | | |
| $t_{pd}$ Propagation Delay Time (signal input to output) | | 200 | | 10 V | | 5 | | | 30 | 30 | ns |
| | | | | | | 10 | | | 15 | 60 | |
| | | | | | | 15 | | | 11 | 20 | |
| Frequency Response Channel "ON" (sine wave input) at 20 Log $\frac{V_o}{V_i}$ = – 3dB | = $V_{SS}$ | 1 | | 5 (•) | | 10 | $V_o$ at Common OUT/IN | 4053B | 30 | | MHz |
| | | | | | | | | 4052B | 25 | | |
| | | | | | | | | 4051B | 20 | | |
| | | | | | | | $V_o$ at any Channel | | 60 | | |
| Feedthrough (all channels OFF) at 20 Log $\frac{V_o}{V_i}$ = – 40dB | = $V_{SS}$ | 1 | | 5 (•) | | 10 | $V_o$ at Common OUT/IN | 4053 | 8 | | MHz |
| | | | | | | | | 4052 | 10 | | |
| | | | | | | | | 4051 | 12 | | |
| | | | | | | | $V_o$ at any Channel | | 8 | | |
| Frequency Signal Crosstalk at 20 Log $\frac{V_o}{V_i}$ = – 40dB | = $V_{SS}$ | 1 | | 5 (•) | | 10 | Between any 2 Channels | | 3 | | MHz |
| | | | | | | | Between Sections 4052B only | measured on common | 6 | | |
| | | | | | | | | measured on any channel | 10 | | |
| | | | | | | | Between any 2 Sections 4053B only | in Pin 2 out Pin 14 | 2.5 | | MHz |
| | | | | | | | | in Pin 15 out Pin 14 | 6 | | |
| Sine Wave Distortion $f_{is}$ = 1kHz Sine Wave | = $V_{SS}$ | 10 | 1 | 2 (•) | | 5 | | | 0.3 | | % |
| | | 10 | 1 | 3 (•) | | 10 | | | 0.2 | | |
| | | 10 | 1 | 5 (•) | | 15 | | | 0.12 | | |
| **CONTROL** (Address or Inhibit) | | | | | | | | | | | |
| Progation Delay Time : Address-to Signal OUT Channels ON or OFF | 0 | | | | 0 | 5 | | | 360 | 720 | ns |
| | 0 | | | | 0 | 10 | | | 160 | 320 | |
| | 0 | | | | 0 | 15 | | | 120 | 240 | |
| | – 5 | | | | 0 | 5 | | | 225 | 450 | |
| Propagation Delay Time : Inhibit to Signal OUT (channel turning ON) | 0 | 10 | | | 0 | 5 | | | 360 | 720 | ns |
| | 0 | | | | 0 | 10 | | | 160 | 320 | |
| | 0 | | | | 0 | 15 | | | 120 | 240 | |
| | – 10 | | | | 0 | 5 | | | 200 | 400 | |
| Propagation Delay Time : Inhibit to Signal OUT (channel turning OFF) | 0 | 0.3 | | | | 5 | | | 200 | 450 | ns |
| | 0 | | | | | 10 | | | 90 | 210 | |
| | 0 | | | | | 15 | | | 70 | 160 | |
| | – 10 | | | | | 5 | | | 130 | 300 | |
| Address or Inhibit to Signal Crosstalk | 0 | 10* | | | 0 | 10 | $V_C$ = $V_{DD}$–$V_{SS}$ (square wave) | | 65 | | mV peak |

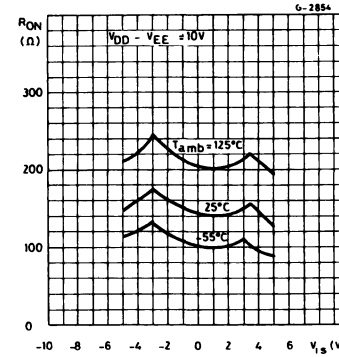
(•) Peak to peak voltage symmetrical about $\frac{V_{DD}-V_{EE}}{2}$

(*) Both ends of channel

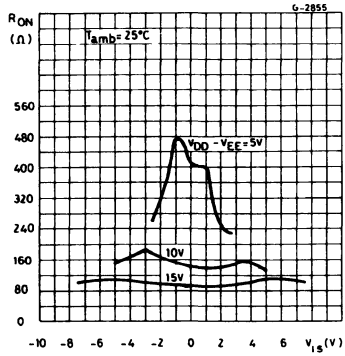
Typical Channel ON Resistance vs. Input Signal Voltage (all types).



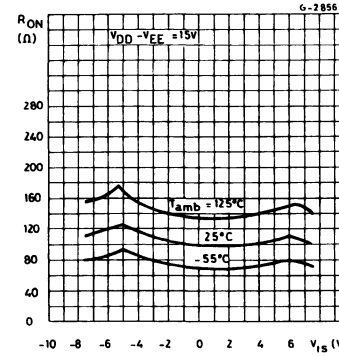

Typical Channel ON Resistance vs. Input Signal Voltage (all types).



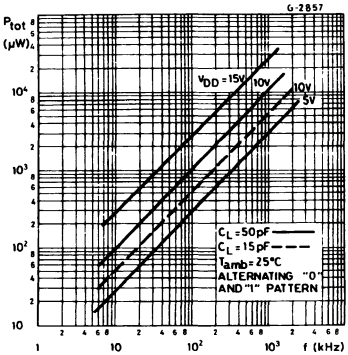

Typical Channel ON Resistance vs. Input Signal Voltage (all types).



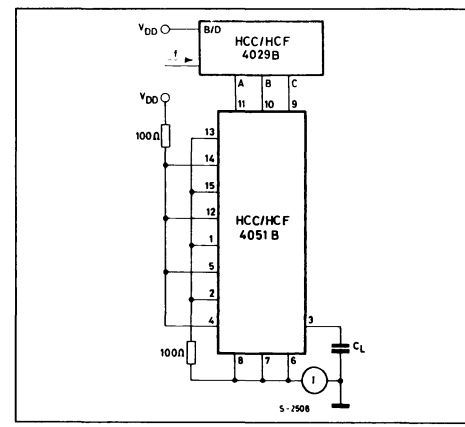

Typical Channel ON Resistance vs. Input Signal Voltage (all types).



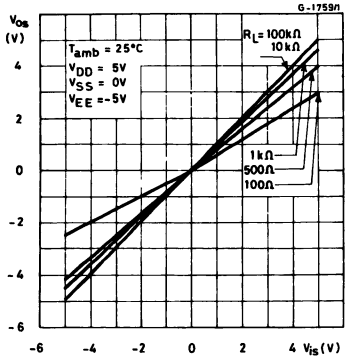

Typical Dynamic Power Dissipation/Package vs.



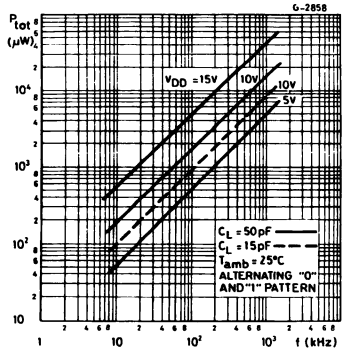

Switching Frequency and Test Circuit (4051B).



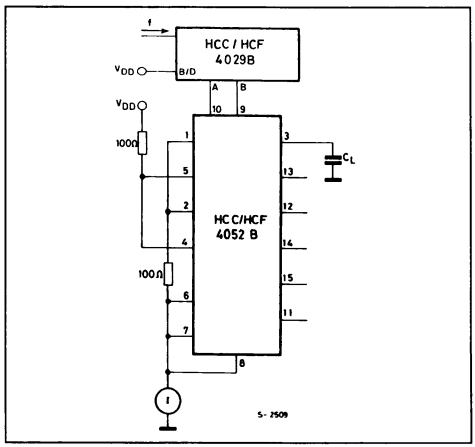
Typical ON Characteristics for 1 of 8 Channels (4051B).



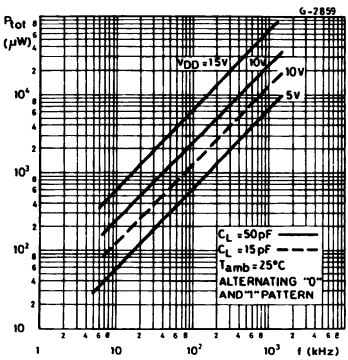

Typical Dynamic Power Dissipation/Package vs.



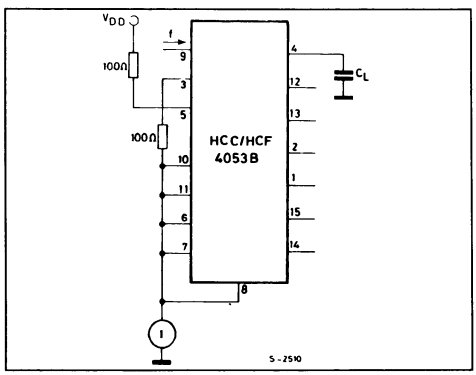

Switching Frequency and Test Circuit (4052B).




Typical Dynamic Power Dissipation/Package vs.

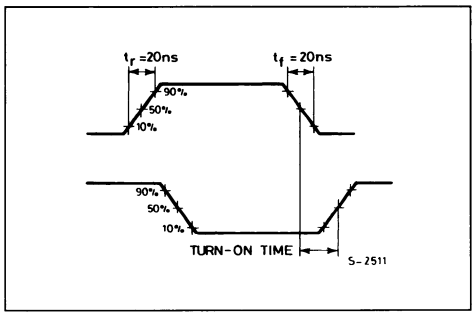



Switching Frequency and Test Circuit (4053B).

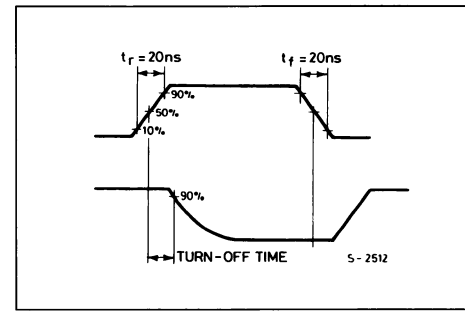


## WAVEFORMS

Channel Being Turned ON ($R_L$ = 10KΩ).




Channel Being Turned OFF ($R_L$ = 300KΩ).




## TYPICAL BIAS VOLTAGES

Fig. (a)

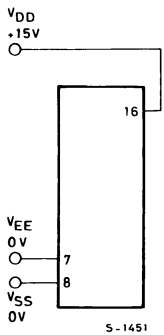



Fig. (b)

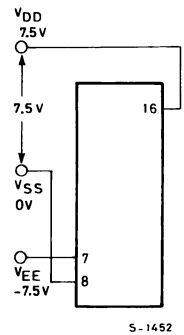



Fig. (c)

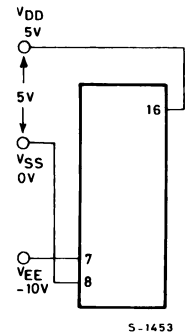
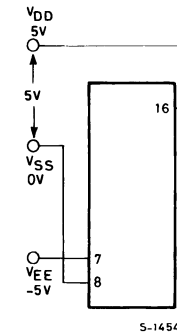


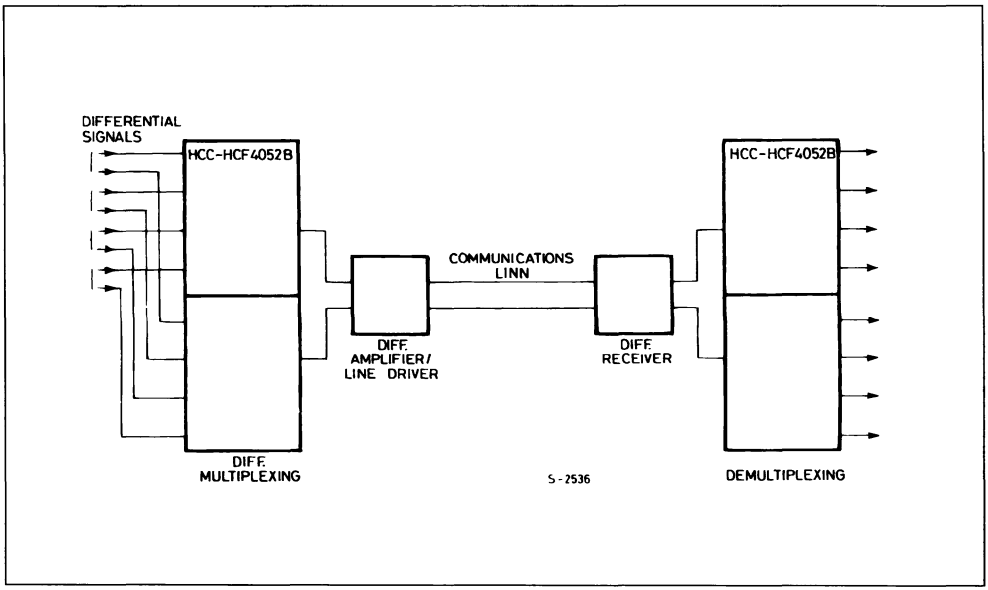

Fig. (d)




The ADDRESS (digital-control inputs) and INHIBIT logic levels are "0"=$V_{SS}$ and "1"=$V_{DD}$. The analog signal (trough the TG) may swing from $V_{EE}$ to $V_{DD}$

## TYPICAL APPLICATIONS

TYPICAL TIME-DIVISION APPLICATION OF THE 4052B

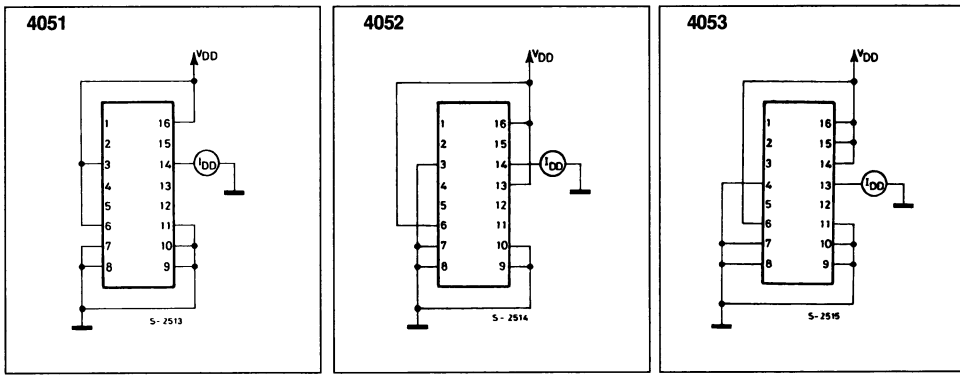



## SPECIAL CONSIDERATIONS

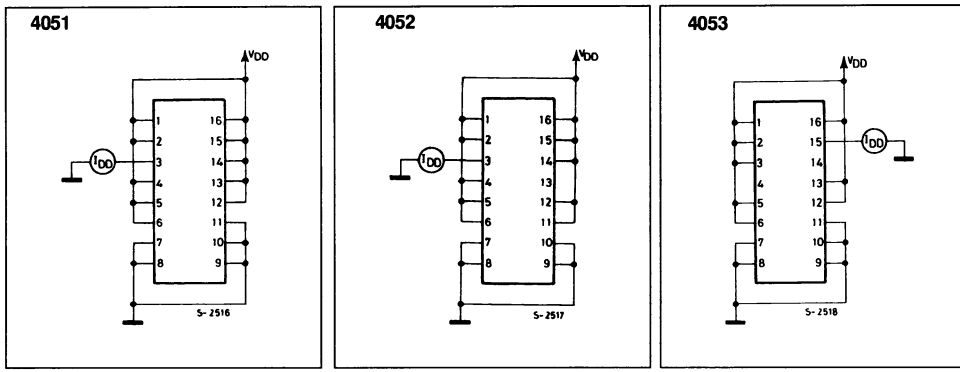
Control of analog signals up to 20V peak-to-peak can be achieved by digital signal amplitudes of 4.5 to 20V (if $V_{DD} - V_{SS} = 3V$, a $V_{DD} - V_{EE}$ of up to 13V can be controlled ; for $V_{DD} - V_{EE}$ level differences above 13V, a $V_{DD} - V_{SS}$ of at least 4.5V is required). For example, if $V_{DD} = +5V$, $V_{SS} = 0$, and $V_{EE} = -13.5V$, analog signals from – 13.5V to + 4.5V can be controlled by digital inputs of 0 to 4.5V. In certain applications, the externa! load-resistor current may include both $V_{DD}$ and signal-line components. To avoid drawing $V_{DD}$ current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0,8 volt (valvulated from $R_{ON}$ values shown in ELECTRICAL CHARACTERISTICS CHART). No $V_{DD}$ current will flow through $R_L$ if the switch current flows into lead 3 on the **HCC/HCF4051** ; leads 3 and 13 on the **HCC/HCF4052** ; leads 4, 14, and 15 on the **HCC/HCF4053**.

## TEST CIRCUITS

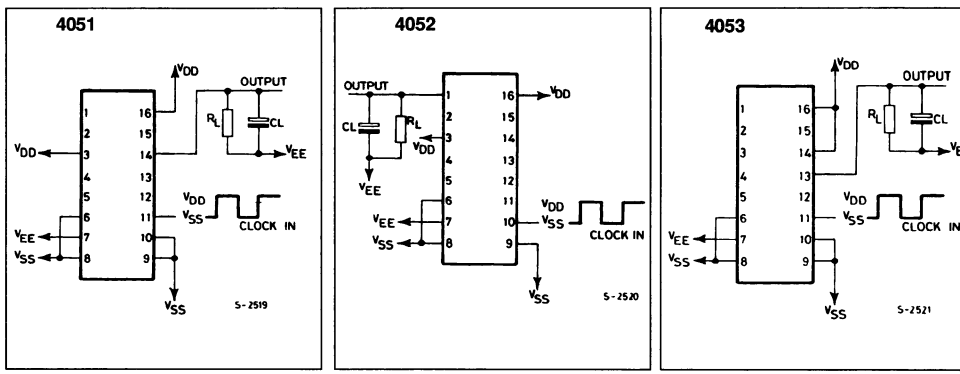
Off Channel Leakage Current-any Channel OFF.




Off Channel Leakage Current-all Channel OFF.

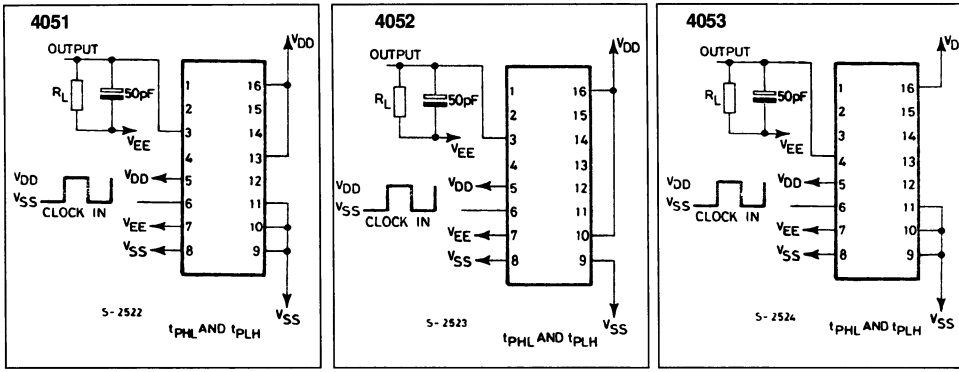



Propagation Delay-adress Input to Signal Output.

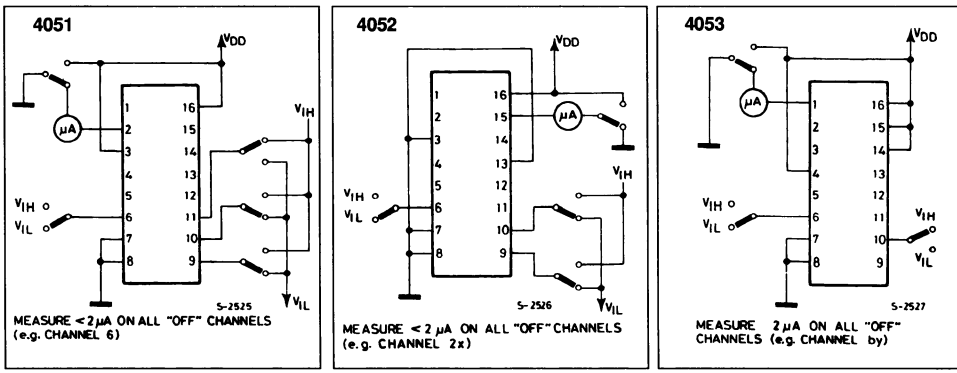


**TEST CIRCUITS** (continued)

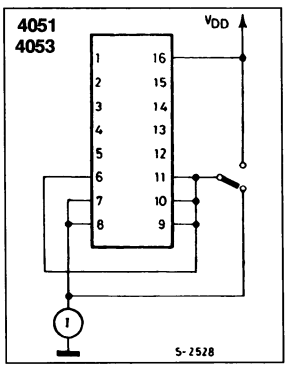
Propagation Delay-Inhibit Input to Signal Output.



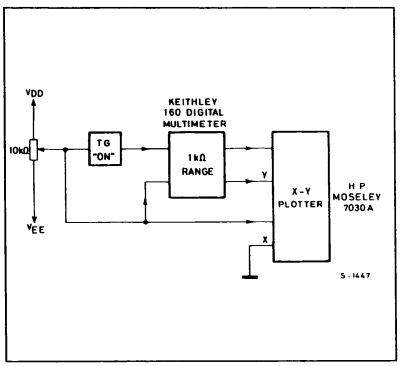

Input Voltage.




Quiescent Device Current.

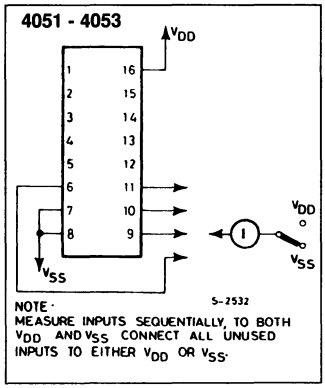


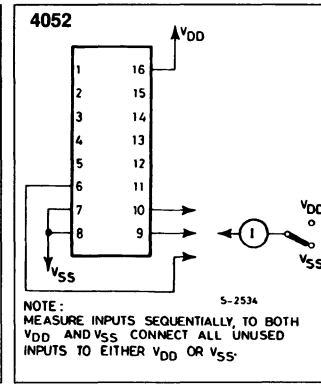

Channel ON Resistance
Meaurement Circuit.



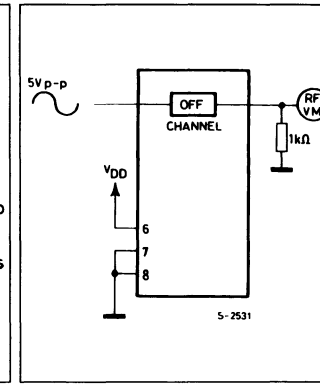
**TEST CIRCUITS** (continued)

Input Current.

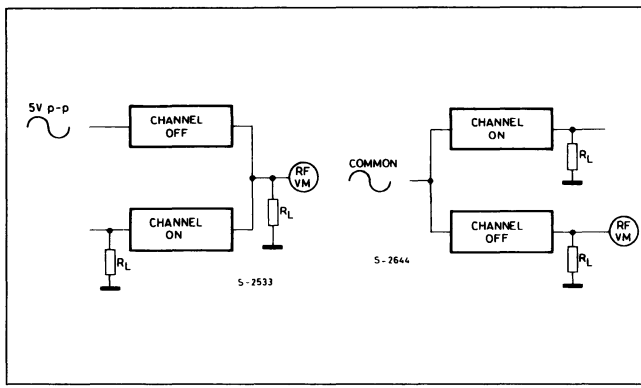


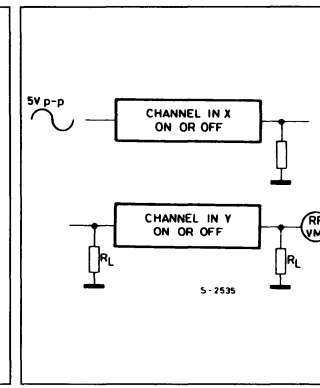

Feedthrough (All Types).




Crosstalk Betwen any two Channels (All Types).




Crosstalk Betweenn Duals or Triplets (4052-4053).



# HCC4054B/55B/56B
# HCF4054B/55B/56B

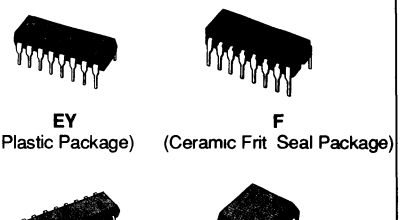
## LIQUID-CRYSTAL DISPLAY DRIVERS

**4054B 4-SEGMENT DISPLAY DRIVER - STROBED LATCH FUNCTION**

**4055B BCD TO 7-SEGMENT DECODER/DRIVER, WITH "DISPLAY-FREQUENCY" OUTPUT**

**4056B BCD TO 7-SEGMENT DECODER/DRIVER WITH STROBED LATCH FUNCTION**

- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- OPERATION OF LIQUID CRYSTALS WITH COS/MOS CIRCUITS PROVIDES ULTRA-LOW-POWER DISPLAYS
- EQUIVALENT AC OUTPUT DRIVE FOR LIQUID-CRYSTAL DISPLAYS-NO EXTERNAL CAPACITOR REQUIRED
- VOLTAGE DOUBLING ACROSS DISPLAY [($V_{DD} - V_{EE}$) = 18V)] RESULTS IN EFFECTIVE 36V (p-p) DRIVE ACROSS SELECTED DISPLAY SEGMENTS
- LOW-OR HIGH-OUTPUT LEVEL DC DRIVE FOR OTHER TYPES OF DISPLAYS
- ON-CHIP LOGIC-LEVEL CONVERSION FOR DIFFERENT INPUT AND OUTPUT-LEVEL SWINGS
- FULL DECODING OF ALL INPUT COMBINATIONS : "0 – 9, L, H, P, A– " AND BLANK POSITIONS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY** (Plastic Package)

**F** (Ceramic Frit Seal Package)

**M1** (Micro Package)

**C1** (Plastic Chip Carrier)

**ORDER CODES :**

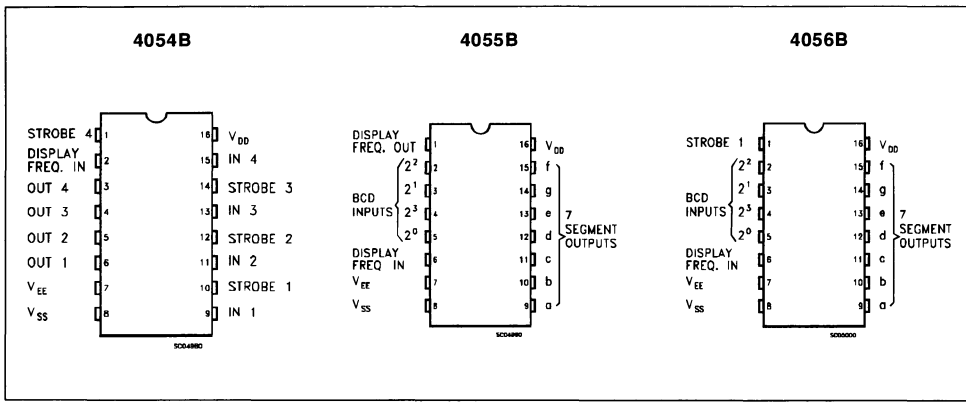
HCC40XXBF HCF40XXBM1
HCF40XXBEY HCF40XXBC1

### DESCRIPTION

The **HCC4054B**, **HCC4055B** and **HCC4056B** (extended temperature range) and the **HCF4054B, HCF4055B** and **HCF4056B** (intermediate temperature range) are monolithic integrated circuits available in 16-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF4055B** and **HCC/HCF4056B** types are single-digit BCD-to-7-segment decoder/driver circuits that provide level-shifting functions on the chip. This feature permits the BCD input-signal swings ($V_{DD}$ to $V_{SS}$) to be the same as or different from the 7-segment output-signal swings ($V_{DD}$ to $V_{EE}$). For example, the BCD input-signal swings ($V_{DD}$ to $V_{SS}$) may be as low as 0 to – 3V, whereas the output-display drive-signal swing ($V_{DD}$ to $V_{EE}$) may be from 0 to – 5V. If $V_{DD}$ to $V_{EE}$ exceeds 15V, $V_{DD}$ to $V_{SS}$ should be at least 4V. The 7-segment outputs are controlled by the DISPLAY-FREQUENCY (DF) input which causes the selected segment outputs to be low, high, or a square-wave output (for liquid-crystal displays). When the DF input is low the output segments will be high when selected by the BCD inputs. When the DF input is high, the output segments will be low when selected by the BCD inputs. When a square-wave is present at the DF input, the selected segments will have a square-wave output that is 180° out of phase with the DF input. Those segments which are not selected will have a square-wave output that is in phase with the input. DF square-wave repetition rates for liquid-crystal displays usually range from 30Hz (well above flicker rate) to 200Hz (well below the upper limit of the liquid-crystal frequency response). The **HCC/HCF4055B** provides a level-shifted high-amplitude DF output which is required for driving the common electrode in liquid-crystal displays. The **HCC/HCF4056B** provides a strobed-latch function at the BCD inputs. Decoding of all input combinations on the **HCC/HCF4055B** and **HCC/HCF4056B** provides displays of 0 to 9 as well

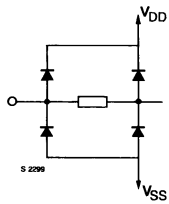
as L, P, H, A,– , and a blank position. (see typical application for other letters). The **HCC/HCF4054B** provides level shifting similar to the **HCC/HCF4055B** and **HCC/HCF4056B** independently strobed latches, and common DF control on 4 signal lines. The **HCC/HCF4054B** is intended to provide drive-signal compatibility with the **HCC/HCF4055B** and **HCC/HCF4056B** 7-segment decoder types for the decimal point, colon, polarity, and similar display lines. A level-shifted high-amplitude DF output can be obtained from any **HCC/HCF4054B** output line by connecting the corresponding input and strobe lines to a low and high level, respectively. The **HCC/HCF4054B** may also be utilized for logic-level "up conversion" or "down conversion". For example, input-signal swings ($V_{DD}$ to $V_{SS}$) from + 5 to 0V can be converted to output-signal swings ($V_{DD}$ to $V_{EE}$) of + 5 to – 5V. The level-shifted function on all three types permits the use of different input-and output-signal swings. The input swings from a low level of $V_{SS}$ to a high level of $V_{DD}$ while the output swings from a low level of $V_{EE}$ to the same high level of $V_{DD}$. Thus, the input and output swings can be selected independently of each other over a 3-to-18V range. $V_{SS}$ may be connected to $V_{EE}$ when no level-shift function is required. For the **HCC/HCF 4054B** and **HCC/HCF 4056B**, data are transferred from input to output by placing a high voltage level at the strobe input. A low voltage level at the strobe input latches the data input and the corresponding output segments remain selected (or non-selected) while the strobe is low. Whenever the level-shifting function is required, the **HCC/HCF4055B** can be used by itself to drive a liquid-crystal display (fig. 10 and fig. 12). The **HCC/HCF4056B**, however, must be used together with a **HCC/HCF4054B** to provide the common DF output (fig. 14). The capability of extending the voltage swing on the negative end (this voltage cannot be extended on the positive end) can be used to advantage in the set-up of fig. 11. Fig. 9 is common to all three types.

## PIN CONNECTIONS

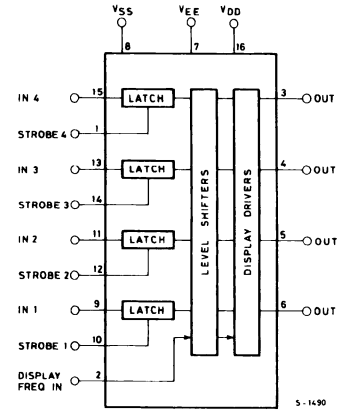


## FUNCTIONAL DIAGRAMS

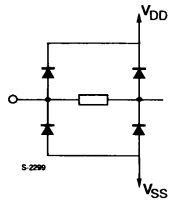
### 4054B



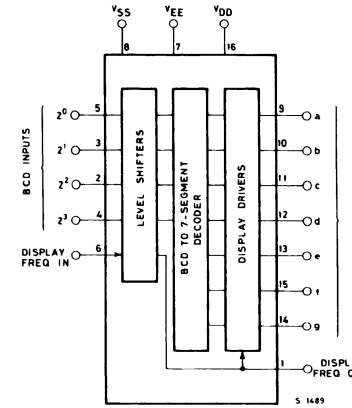

ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK



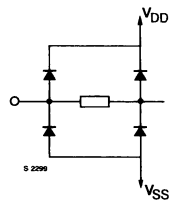

### 4055B



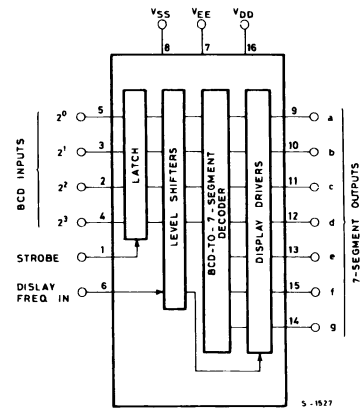

ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK




### 4056B




ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK



## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for external periods may affect device reliability

* All voltage values are referred to $V_{SS}$ pin voltage

## RECOMMENDED OPERATING CONDITIONS

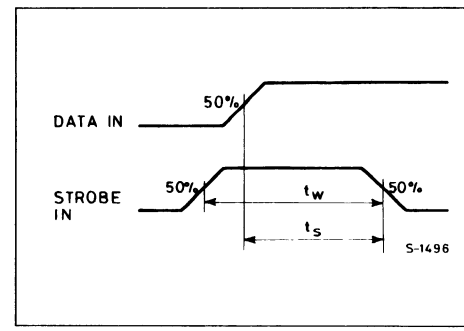
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to 125<br>− 40 to 85 | °C<br>°C |

## TRUTH TABLE

**4055 B** and **4056 B**

| Input Code | | | | Output State | | | | | | | Display Character |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $2^3$ | $2^2$ | $2^1$ | $2^0$ | a | b | c | d | e | f | g | |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 2 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 3 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 4 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 5 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 6 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 7 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 9 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | L |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | H |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | P |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | A |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | – |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BLANK |

Data Setup Time and Strobe Pulse Duration.



**STATIC ELECTRICAL CHARACTERISTICS** (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions | | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{EE}$ (V) | $V_I$ (V) | $V_O$ (V) | $V_{SS}$ (V) | $V_{DD}$ (V) | $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | |
| $I_L$ | Quiescent Supply Current | HCC Types | – 5 | 0/5 | | 0 | 5 | | 5 | | 0.04 | 5 | | 150 | µA |
| | | | 0 | 0/10 | | 0 | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0 | 0/15 | | 0 | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0 | 0/20 | | 0 | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | – 5 | 0/5 | | 0 | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0 | 0/10 | | 0 | 10 | | 40 | | 0 04 | 40 | | 300 | |
| | | | 0 | 0/15 | | 0 | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0 | 0/5 | | 0 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0 | 0/10 | | 0 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0 | 0/15 | | 0 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 0 | 5/0 | | 0 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 0 | 10/0 | | 0 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 0 | 15/0 | | 0 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | – 5 | | 0 5/4 5 | 0 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | 0 | | 1/9 | 0 | 10 | 7 | | 7 | | | 7 | | |
| | | | 0 | | 1 5/18 5 | 0 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | 5 | | 0 5/4 5 | 0 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | 0 | | 9/1 | 0 | 10 | | 3 | | | 3 | | 3 | |
| | | | 0 | | 1 5/18 5 | 0 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output High Current | HCC Types | – 5 | 0/5 | 4.5 | 0 | 5 | – 0.6 | | – 0.45 | – 0.9 | | – 0.3 | | mA |
| | | | 0 | 0/10 | 9.5 | 0 | 10 | – 0.6 | | – 0.45 | – 0.9 | | – 0.3 | | |
| | | | 0 | 0/15 | 13.5 | 0 | 15 | – 1.9 | | – 1.5 | – 3 | | – 1.1 | | |
| | | HCF Types | – 5 | 0/5 | 4.5 | 0 | 5 | – 0.47 | | – 0.38 | – 0.9 | | – 0.28 | | |
| | | | 0 | 0/10 | 9.5 | 0 | 10 | – 0.47 | | – 0.38 | – 0.9 | | – 0.28 | | |
| | | | 0 | 0/15 | 13.5 | 0 | 15 | – 1.58 | | – 1.27 | – 3 | | – 0.95 | | |
| $I_{OL}$ | Output Low Current | HCC Types | – 5 | 0/5 | 0.4 | 0 | 5 | 1.6 | | 1.3 | 2.6 | | 0.9 | | mA |
| | | | 0 | 0/10 | 0.5 | 0 | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0 | 0/15 | 1.5 | 0 | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | – 5 | 0/5 | 0.4 | 0 | 5 | 1.37 | | 1.1 | 2.6 | | 0.82 | | |
| | | | 0 | 0/10 | 0.5 | 0 | 10 | 1.37 | | 1.1 | 2.6 | | 0.82 | | |
| | | | 0 | 0/15 | 1.5 | 0 | 15 | 3.62 | | 2.9 | 6.8 | | 2.17 | | |
| $I_{IH}$, $I_{IL}$** | Input Leakage Current | HCC Types | 0 | 0/18 | | 0 | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | µA |
| | | HCF Types | 0 | 0/15 | | 0 | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | µA |
| $C_I$** | Input Capacitance | | | | | | | | | | 5 | 7.5 | | | pF |

*$T_{Low}$ = – 55°C for **HCC** device : – 40°C for **HCF** device.
*$T_{High}$ = 125°C fr **HCC** device · + 85°C for **HCF** device
The Noise Margin for both "1" and "0" level is 1V min with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2.5 V min. with $V_{DD}$ = 15V.
** Any input

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall times = 20ns)

| Symbol | Parameter | Test Conditions | | | | Types | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | 4054B | | | 4055B, 4056B | | | |
| | | | $V_{EE}$ (V) | $V_{SS}$ (V) | $V_{DD}$ (V) | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time (any input to any output) | | – 5 | 0 | 5 | | 400 | 800 | | 650 | 1300 | ns |
| | | | 0 | 0 | 10 | | 340 | 680 | | 575 | 1150 | |
| | | | 0 | 0 | 15 | | 250 | 500 | | 375 | 750 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time (any output) | | – 5 | 0 | 5 | | 100 | 200 | | 100 | 200 | ns |
| | | | 0 | 0 | 10 | | 100 | 200 | | 100 | 200 | |
| | | | 0 | 0 | 15 | | 75 | 150 | | 75 | 150 | |
| $t_{setup}$ * | Data Setup Time | | – 5 | 0 | 5 | 220 | 110 | | 220 | 110 | | ns |
| | | | 0 | 0 | 10 | 100 | 50 | | 100 | 50 | | |
| | | | 0 | 0 | 15 | 70 | 35 | | 70 | 35 | | |
| $t_W$ * | Strobe Pulse Width | | – 5 | 0 | 5 | 220 | 110 | | 220 | 110 | | ns |
| | | | 0 | 0 | 10 | 100 | 50 | | 100 | 50 | | |
| | | | 0 | 0 | 15 | 70 | 35 | | 70 | 35 | | |

* HCC/HCF4054B and HCC/HCF4056B only.

**Figure 1 :** Typical Output Low (sink) Current Characteristics.

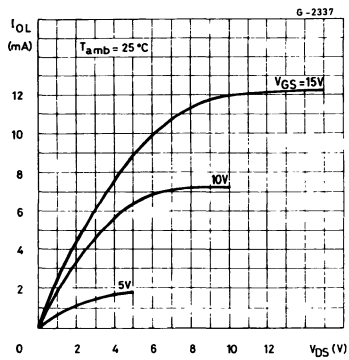



**Figure 2 :** Minimum Output High (source) Current Characteristics.

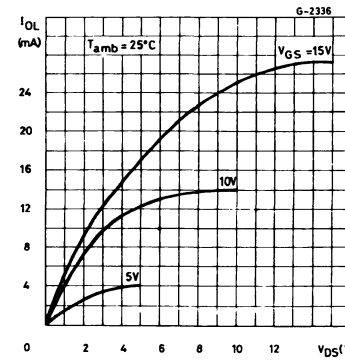


**Figure 3 :** Typical Output High (source) Current Characteristics.

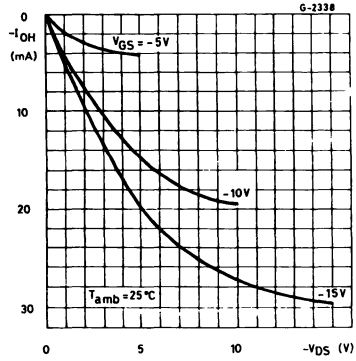



**Figure 4 :** Minimum Output (source) Current Characteristics.

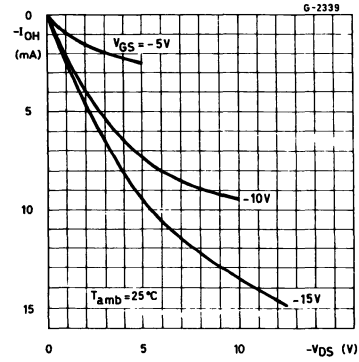



**Figure 5 :** Typical Propagation Delay Time vs. Load Capacitance (for 4054B).

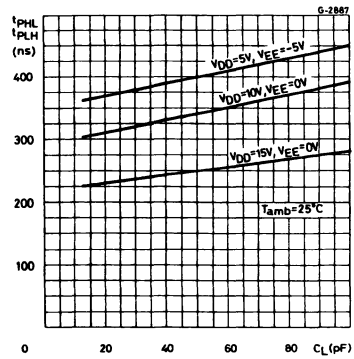



**Figure 6 :** Typical Propagation Delay Time vs. Load Capacitance (for 4055B and 4056B).

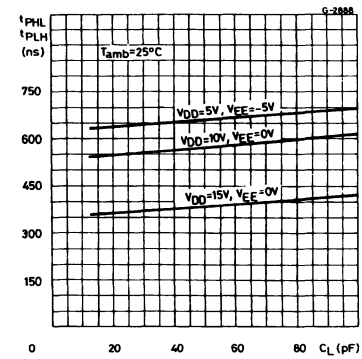



**Figure 7 :** Typical Transition Time vs. Load Capacitance.

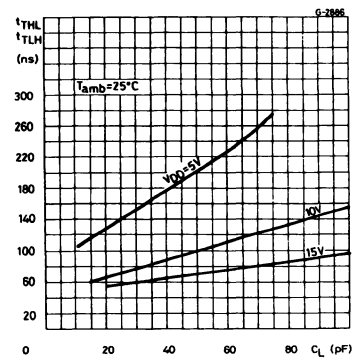
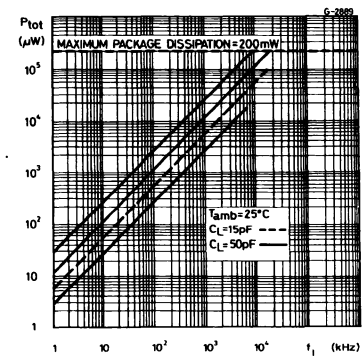



**Figure 8 :** Typical Dynamic Power Dissipation vs. Frequency.



## TYPICAL APPLICATIONS

**Figure 9 :** Display-driver Circuit for one Segment Line and Waveforms.

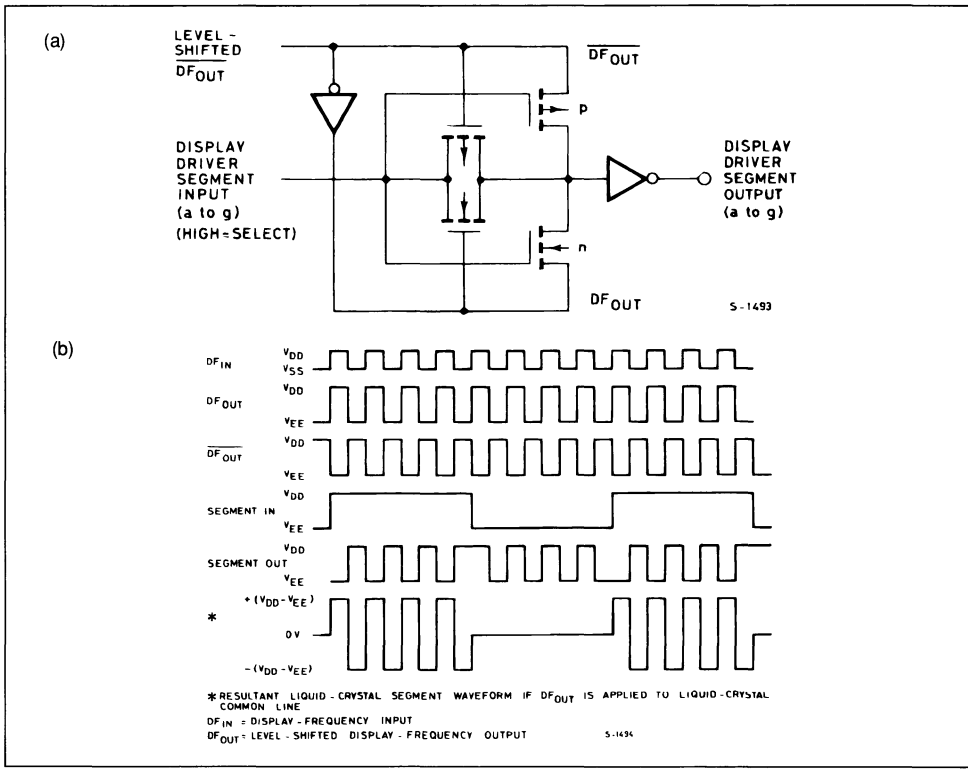
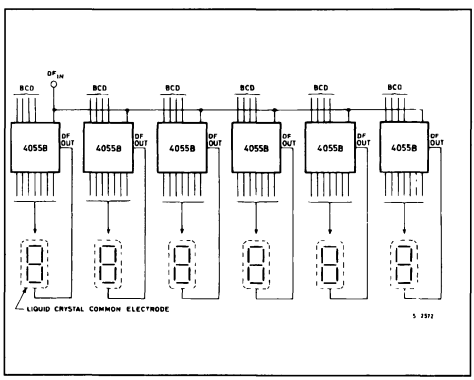
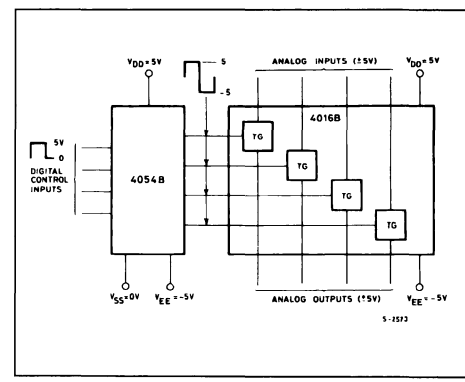



**Figure 10 :** Clock Display.




$V_{DD}$ = 0V, $V_{SS}$ = – 5V, $V_{EE}$ = – 15V, $F_{IN}$ = 30 Hz square wave

**Figure 11 :** Digital (0 to + 5V) to bidirectional Analog Control (+ 5 to – 5V) Level Shifter.



**TYPICAL APLLICATIONS** (continued)

**Figure 12 :** Single-digit Liquid Crystal Display.

**BCD IN FROM DTL, TTL, OR COS/MOS LOGIC**

| OPTION 1 | OPTION 2 |
|---|---|
| $V_{DD}$ 0V | $V_{DD}$ + 5V |
| $V_{SS}$ −5V | $V_{SS}$ 0V |
| $V_{EE}$ −15V | $V_{EE}$ − 10V |

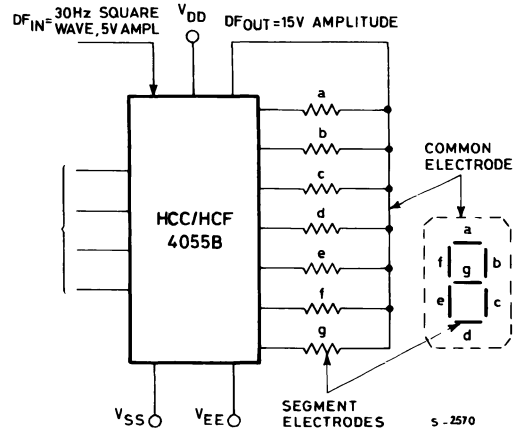
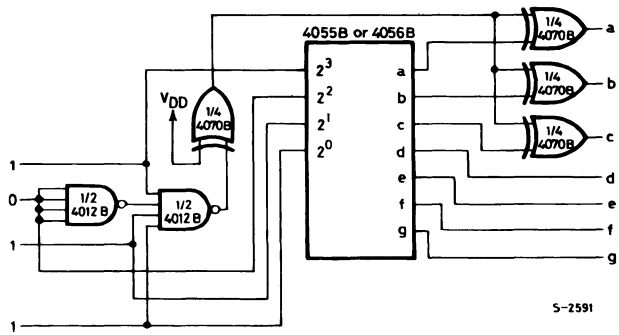
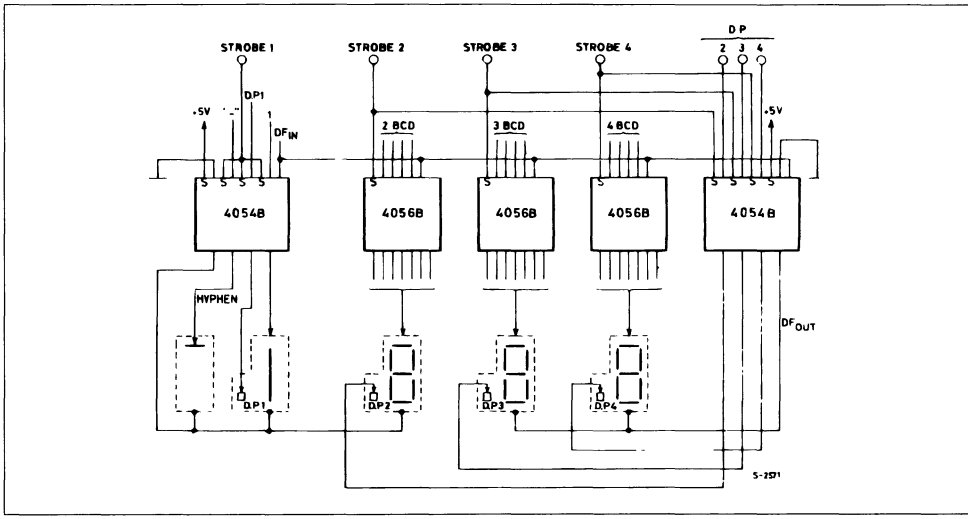



**Figure 13 :** Conversion of "H" Display to "F" Display.



**TYPICAL APLLICATIONS** (continued)

**Figure 14 :** Typical 3 1/2 – Digit–crystal Display : ($V_{DD}$ = + 5V, $V_{SS}$ = 0V, $V_{EE}$ = – 10V, $DF_N$ = 30 Hz square).



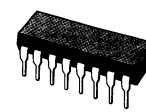

In addition to the letters L, H, P, and A, five other letters can be displayed through the use of simple logic circuits preceding and following the **HCC/HCF4055B** or **HCC/HCF4056B** devices. Fig. 13 is an example of a circuit that converts an "H" display, (code 1011) to an "F" display. One condition that must be met is that $V_{EE} = V_{SS}$. If $V_{EE} \neq V_{SS}$, the **HCC/HCF4054B** must be used to level shift in the appropriate places. In a similar manner the letters C, E, J, and U can be displayed. These circuits can also be used to drive LED displays provided the exclusive-OR gates have sufficient output-current drive. The letters B, D, G, I, O, and S may be represented by the codes for numbers 8, 0, 6, 1, 0, and 5, respectively, when there is preknowledge that only letters are to be displayed.

SGS-THOMSON
MICROELECTRONICS

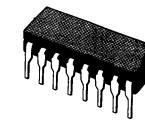
# HCC4060B
# HCF4060B

## 14-STAGE RIPPLE CARRY BINARY COUNTER/DIVIDER AND OSCILLATOR

- MEDIUM-SPEED OPERATION
- COMMON RESET
- FULLY STATIC OPERATION
- BUFFERED INPUTS AND OUTPUTS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 1005 TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N. 13A, " STANDARD SPECIFICATIONS FOR DESCRIPTION OF ' B ' SERIES CMOS DEVICES "



**EY**
(Plastic Package)



**F**
(Ceramic Package)

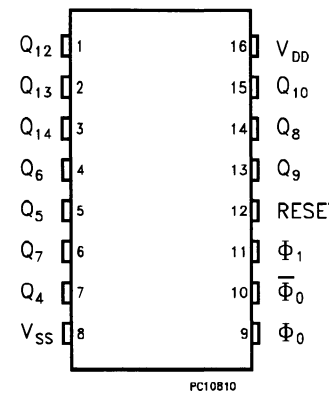
**M1**
(Micro Package)

**C1**
(Chip Carrier)

**ORDER CODES :**

| | |
|---|---|
| HCC4060BF | HCF4060BM1 |
| HCF4060BEY | HCF4060BC1 |

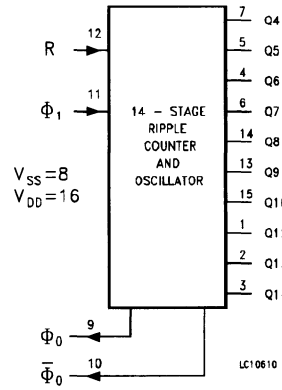
**PIN CONNECTIONS**




### DESCRIPTION

The **HCC4060B** (extended temperature range) and **HCF4060B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in line plastic or ceramic package and plastic micropackage. The **HCC/HCF4060B** consist of an oscillator section and 14 ripple carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A RESET input is provided which reset the counter to the all 0's state and disables oscillator. A high level on the RESET line accmplishes the reset function. All counter stages are master slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of $\phi_1$ (and $\phi_0$). All inputs and outputs are fully buffered. Schmitt trigger action on the clock lin permits unlimited clock rise and fall time.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ * | Supply Voltage: **HCC** Types<br>**HCF** Types | -0.5 to +20<br>-0 5 to +18 | V<br>V |
| $V_I$ | Input Voltage | -0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for Top = Full Package Temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |

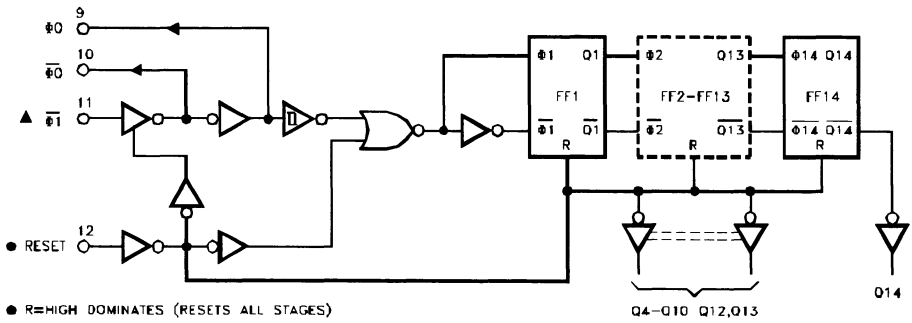
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability

* All voltage values are referred to $V_{SS}$ pin voltage

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage. **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |

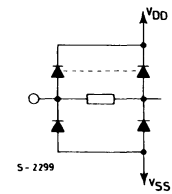
## LOGIC DIAGRAM




● R=HIGH DOMINATES (RESETS ALL STAGES)

▲ COUNTER ADVANCES ONE BINARY COUNT ON EACH NEGATIVE GOING TRANSITION OF Φ1 (AND Φ0)

LC10620




ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditios | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{LOW}$ * Min. | $T_{LOW}$ * Max. | 25 °C Min. | 25 °C Typ. | 25 °C Max. | $T_{HIGH}$ * Min. | $T_{HIGH}$ * Max. | |
| $I_L$ | Quiescent Current | HCC Types | 0/5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/5 | | < 1 | 5 | 4 95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0 05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/5 | 2.5 | | 5 | -2 | | -1.6 | -3.2 | | -1.15 | | mA |
| | | | 0/5 | 4.6 | | 5 | -0.64 | | -0.51 | -1 | | -0.36 | | |
| | | | 0/10 | 9.5 | | 10 | -1.6 | | -1.3 | -2.6 | | -0.9 | | |
| | | | 0/15 | 13.5 | | 15 | -4.2 | | -3 4 | -6.8 | | -2.4 | | |
| | | HCF Types | 0/5 | 2.5 | | 5 | -1.53 | | -1.36 | -3 2 | | -1.1 | | |
| | | | 0/5 | 4.6 | | 5 | -0.52 | | -0.44 | -1 | | -0.36 | | |
| | | | 0/10 | 9.5 | | 10 | -1 3 | | -1.1 | -2 6 | | -0.9 | | |
| | | | 0/15 | 13.5 | | 15 | -3.6 | | -3.0 | -6.8 | | -2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/5 | 0.4 | | 5 | 0 64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1 1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | | 0/18 | Any Input | | 18 | | ±0.1 | | $±10^{-5}$ | ±0.1 | | ±1 | μA |
| | | | 0/15 | | | 15 | | ±0.3 | | $±10^{-5}$ | ±0.3 | | ±1 | μA |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{LOW}$ = -55 °C for **HCC** device -40 °C for **HCF** device

* $T_{HIGH}$ = +125 °C for **HCC** device +85 °C for **HCF** device

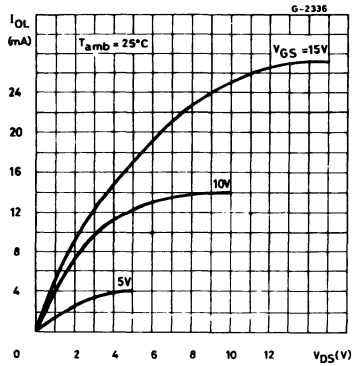
The Noise Margin for both "1" and "0" level is 1V min with $V_{DD}$ = 5 V, 2 V min. with $V_{DD}$ = 10 V, 2 5 V min with $V_{DD}$ = 15 V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 KΩ, typical temperature coefficent for all $V_{DD}$ values is 03 %/°C, all input rise and fall times= 20 ns)

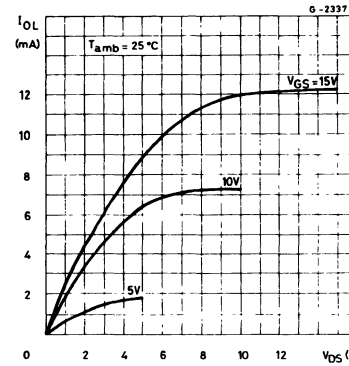
| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time ($\phi$ to Q4 out) | | 5 | | 370 | 740 | ns |
| | | | 10 | | 150 | 300 | |
| | | | 15 | | 100 | 200 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (Qn to $Q_{n+1}$) | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_{TLH}$ $t_{THL}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_W$ | Input Pulse Width | f = 100KHz | 5 | | 50 | 100 | ns |
| | | | 10 | | 20 | 40 | |
| | | | 15 | | 15 | 30 | |
| $t_r$, $t_f$ | Input Pulse Rise and Fall Time | | 5 | Unlimited | | | µs |
| | | | 10 | | | | |
| | | | 15 | | | | |
| $f_{max}$ | Maximum Clock Input Frequency | | 5 | 3.5 | 7 | | MHz |
| | | | 10 | 8 | 16 | | |
| | | | 15 | 12 | 24 | | |
| **RESET OPERATION** | | | | | | | |
| $t_{PHL}$ | Propagation Delay Time | | 5 | | 180 | 360 | ns |
| | | | 10 | | 80 | 160 | |
| | | | 15 | | 50 | 100 | |
| $t_W$ | Reset Pulse Width | | 5 | | 60 | 120 | ns |
| | | | 10 | | 30 | 60 | |
| | | | 15 | | 20 | 40 | |
| **RC OPERATION** | | | | | | | |
| | Variation of Frequency (Unit-to-Unit) | $C_X$ = 200pF $R_S$ = 560KΩ $R_X$ = 50 KΩ | 5 | 18 | 21.5 | 25 | KHz |
| | | | 10 | 20 | 23 | 26 | |
| | | | 15 | 21.1 | 24 | 27 | |
| | Variation of Frequency With Voltage Change (Same Unit) | $C_X$ = 200pF $R_S$ = 560KΩ $R_X$ = 50 KΩ | 5 to 10 | | | 2 | |
| | | | 10 to 15 | | | 1 | |
| $R_X$ | | $C_X$ = 10µF | 5 | | | 20 | MΩ |
| | | $C_X$ = 50µF | 10 | | | 20 | |
| | | $C_X$ = 10µF | 15 | | | 10 | |
| $C_X$ | | $R_X$ = 500 KΩ | 5 | | | 1000 | mF |
| | | $R_X$ = 300 KΩ | 10 | | | 50 | |
| | | $R_X$ = 300 KΩ | 15 | | | 50 | |
| | Maximum Oscillator Frequency * | $R_X$ = 5KΩ $C_X$ = 15pF | 10 | 530 | 650 | 810 | pF |
| | | | 15 | 690 | 800 | 94 | |

* RC oscillator applications are not recommended at supply voltages below 7V for $R_X$ = 50KΩ

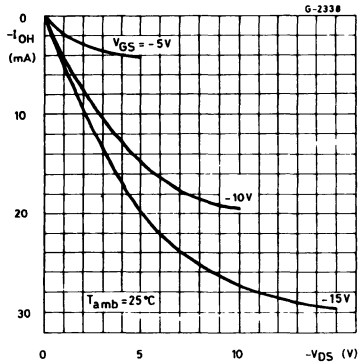
Typical Output Low (sink) Current Characteristics



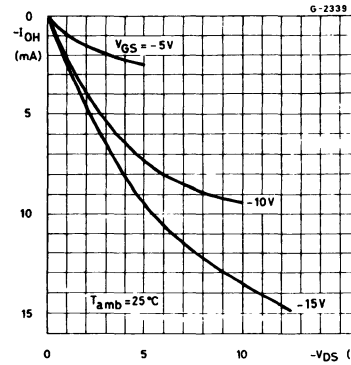

Minimum Output Low (sink) Current Characteristics



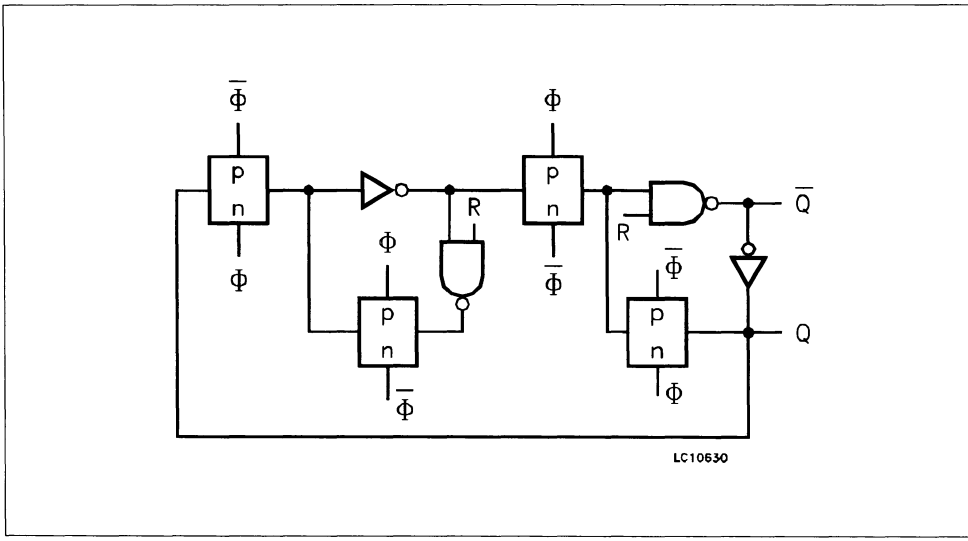

Typical Output High (source) Current Characteristics



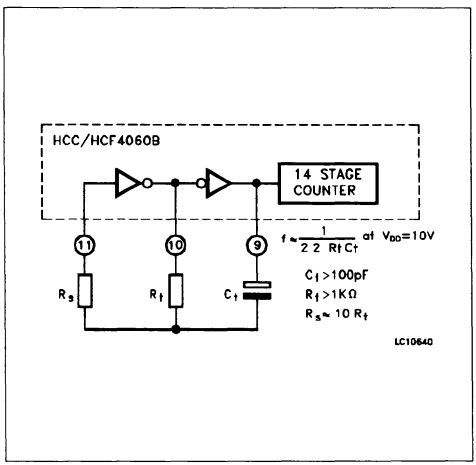

Minimum Output High (source) Current Characteristics



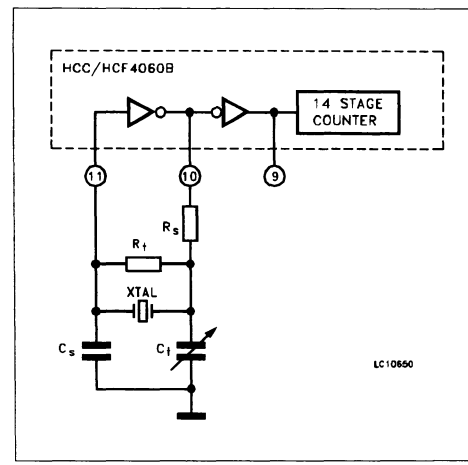
## DETAIL OF TYPICAL FILP-FLOP STAGE




## TYPICAL RC OSILLATOR CIRCUIT

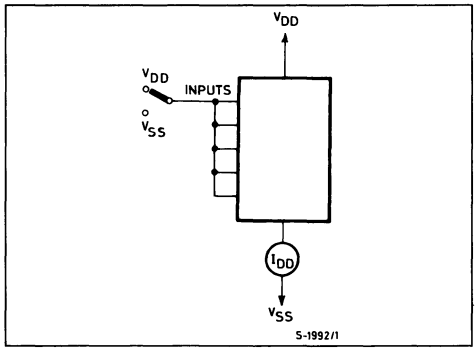



## TYPICAL CRYSTAL OSCILLATOR CIRCUIT

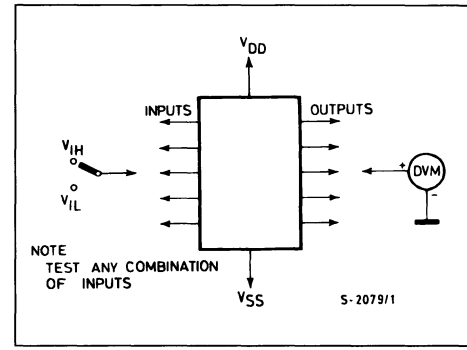


## TEST CIRCUITS

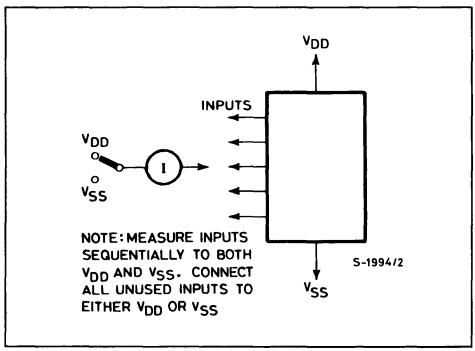
Quiescent Device Current.




Noise Immunity.




Input Leakage Current.

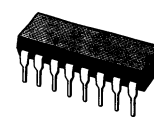


SGS-THOMSON MICROELECTRONICS

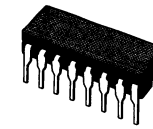
# HCC/HCF4063B

## 4-BIT MAGNITUDE COMPARATOR

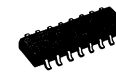
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARD B-SERIES OUTPUT DRIVE
- EXPANSION TO 8-16V...4 N BITS BY CASCADING UNITS
- MEDIUM SPEED OPERATION : COMPARES TWO 4-BIT WORDS IN 250ns (typ.) AT 10V
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)



**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

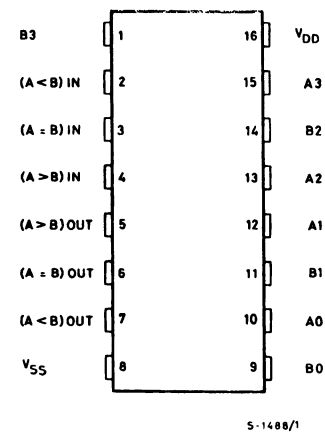
HCC4063BF HCF4063BM1
HCF4063BEY HCF4063BC1

### DESCRIPTION

The **HCC4063B** (extended temperature range) and **HCF4063B** (intermediate temperature range) are available in 16-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF4063B** is a low-power 4-bit magnitude comparator designed for use in computer and logic applications that require the comparison of two 4-bit words. This logic circuit determines whether one 4-bit word (Binary or BCD) is "less than", "equal to" or "greater than" a second 4-bit word. The **HCC/HCF4063B** has eight comparing inputs (A3, B3, through A0, B0), three outputs (A < B, A = B, A > B) and three cascading inputs (A < B, A = B, A > B) that permit systems designers to expand the comparator function to 8, 12, 16...4 N bits. When a single **HCC/HCF4063B** is used, the cascading inputs are connected as follows :
(A < B) = low, (A = B) = high, (A > B) = low.

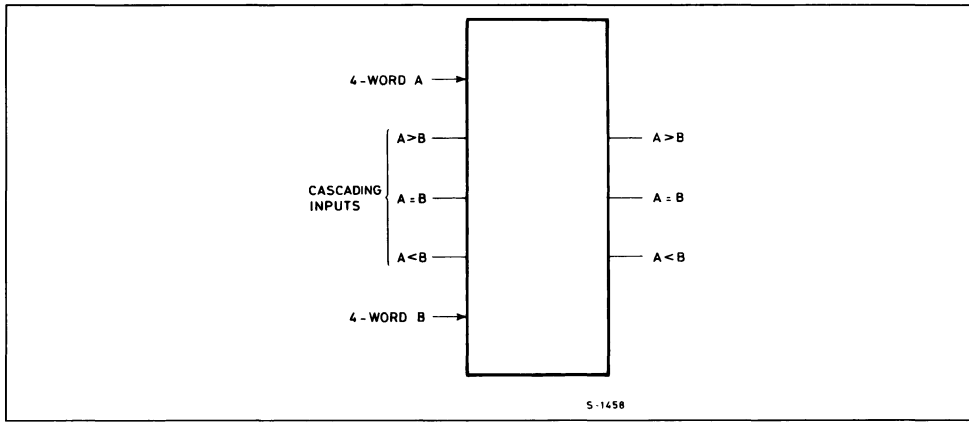
For words longer than 4 bits, **HCC/HCF4063B** devices may be cascaded by connecting the outputs of the less-significant comparator to the corresponding cascading inputs of the more-significant comparator. Cascading inputs (A < B, A = B, and A > B) on the least significant comparator are connected to a low, a high, and a low level, respectively.

### PIN CONNECTIONS




S-1488/1

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

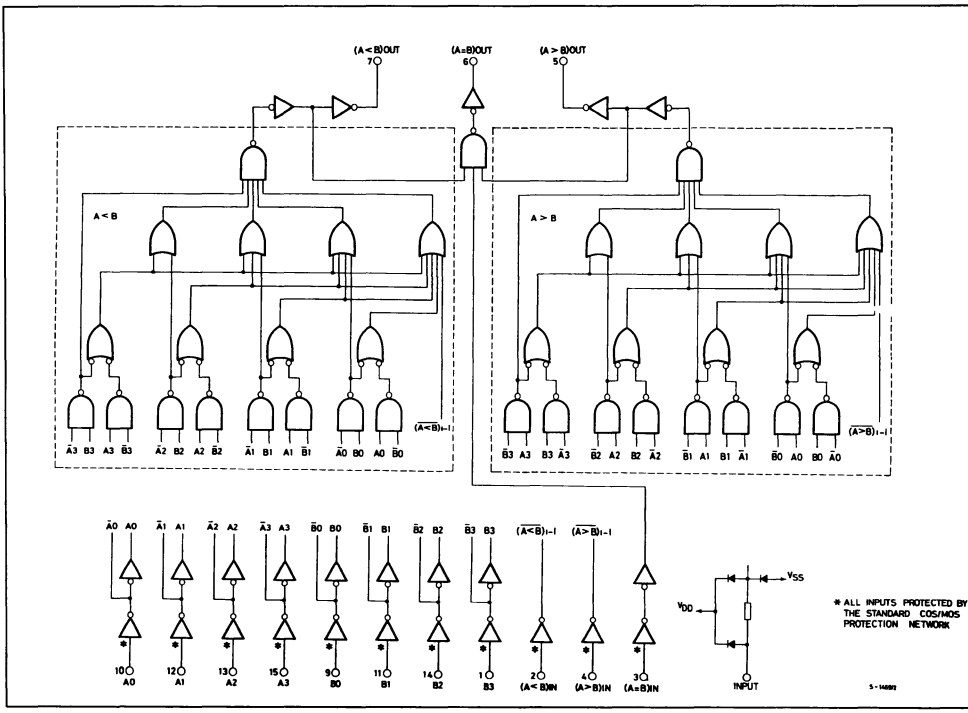
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAM




## TRUTH TABLE

| Inputs | | | | | | | Outputs | | |
|---|---|---|---|---|---|---|---|---|---|
| Comparing | | | | Cascading | | | | | |
| A3, B3 | A2, B2 | A1, B1 | A0, B0 | A < B | A = B | A > B | A < B | A = B | A > B |
| A3 > B3 | X | X | X | X | X | X | 0 | 0 | 1 |
| A3 = B3 | A2 > B2 | X | X | X | X | X | 0 | 0 | 1 |
| A3 = B3 | A2 = B2 | A1 > B1 | X | X | X | X | 0 | 0 | 1 |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 > B0 | X | X | X | 0 | 0 | 1 |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | 0 | 0 | 1 | 0 | 0 | 1 |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | 0 | 1 | 0 | 0 | 1 | 0 |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | 1 | 0 | 0 | 1 | 0 | 0 |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 < B0 | X | X | X | 1 | 0 | 0 |
| A3 = B3 | A2 = B2 | A1 < B1 | X | X | X | X | 1 | 0 | 0 |
| A3 = B3 | A2 < B2 | X | X | X | X | X | 1 | 0 | 0 |
| A3 < B3 | X | X | X | X | X | X | 1 | 0 | 0 |

X = Don't care  1 ≡ High state  0 ≡ Low state

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

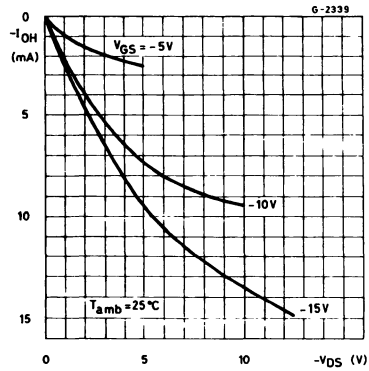
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device . − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device . + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is 1V min. with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.

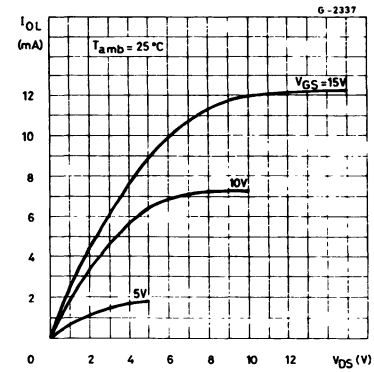
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall times = 20ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time | Comparing Inputs to Outputs | 5 | | 625 | 1250 | ns |
| | | | 10 | | 250 | 500 | |
| | | | 15 | | 175 | 350 | |
| | | Cascading Inputs to Outputs | 5 | | 500 | 1000 | |
| | | | 10 | | 200 | 400 | |
| | | | 15 | | 140 | 280 | |
| $t_{TLH}$, $t_{THL}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

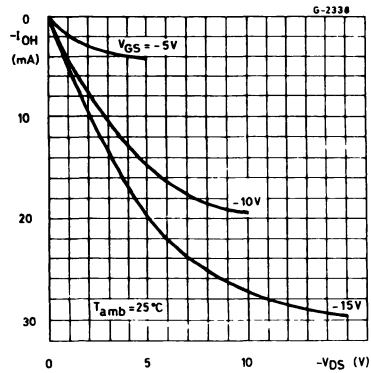
Minimum Output High (source) Current Characteristics.



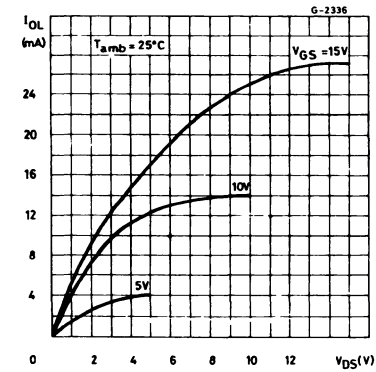

Minimum Output Low (sink) Current Characteristics.



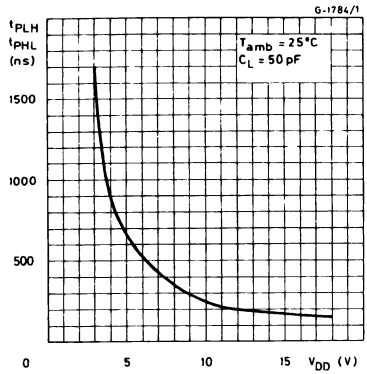

Typical Output High (source) Current Characteristics.



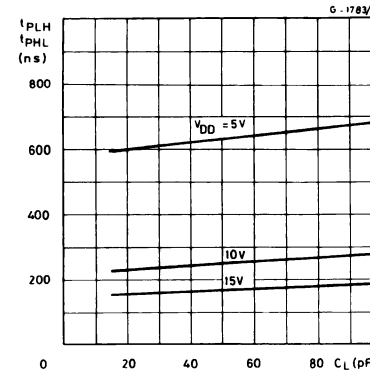

Typical Output Low (sink) Current Characteristics.



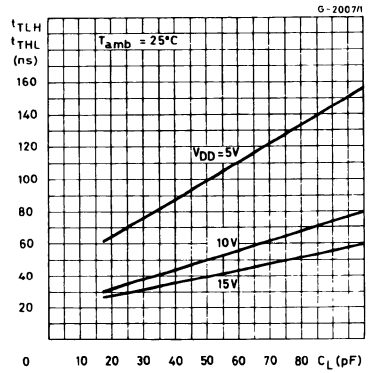
Typical Propagation Delay Time vs. $V_{DD}$.



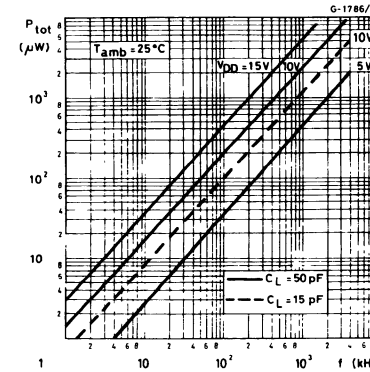

Typical Propagation Delay Time vs. $C_L$.



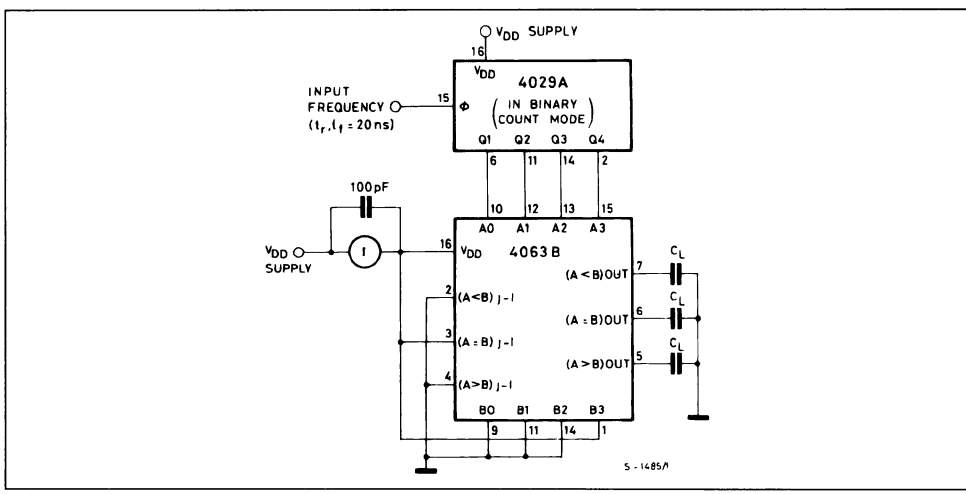

Typical Transition Time vs. Load Capacitance.




Typical Power Dissipation Characteristics.

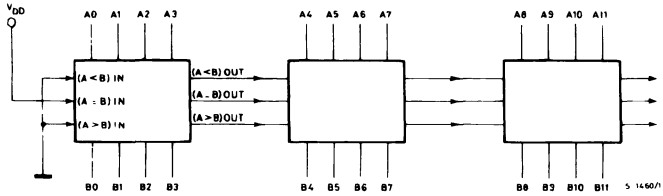



Dynamic Power Dissipation.



## TYPICAL APPLICATION

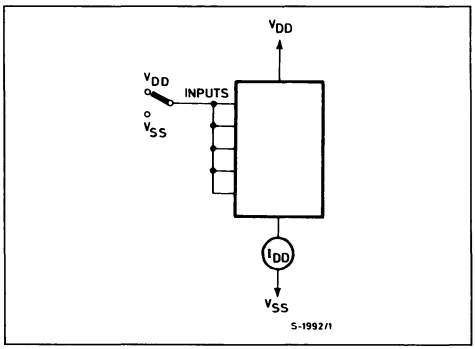
TYPICAL SPEED CHARACTERISTICS OF A 12-BIT COMPARATOR



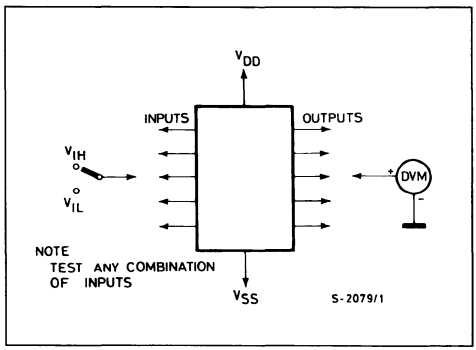

$t_{p\ (TOT)} = t_p$ (COMPARE INPUTS) + 2 x $t_p$ (CASCADE INPUTS) at $C_L$ = 50pF (each output),
$V_{DD}$ = 10V (3 stages) = 250 + 2 x (200) = 650ns (typ ).

## TEST CIRCUITS

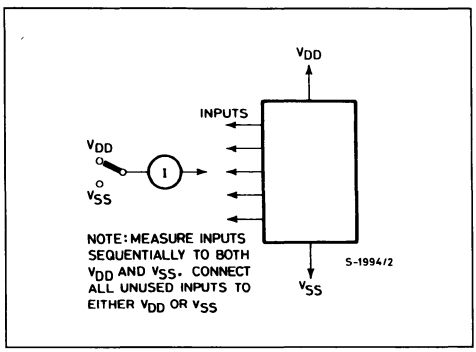
Quiescent Device Current.




Noise Immunity.




Input Leakage Current.

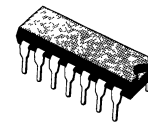


SGS-THOMSON MICROELECTRONICS

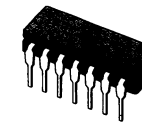
# HCC/HCF4066B

## QUAD BILATERAL SWITCH FOR TRANSMISSION OR MULTIPLEXING OF ANALOG OR DIGITAL SIGNALS

- 15V DIGITAL OR ± 7.5V PEAK-TO-PEAK SWITCHING
- 80Ω TYPICAL ON RESISTANCE FOR 15V OPERATION
- SWITCH ON RESISTANCE MATCHED TO WITHIN 5Ω OVER 15V SIGNAL-INPUT RANGE
- ON RESISTANCE FLAT OVER FULL PEAK-TO-PEAK SIGNAL RANGE
- HIGH ON/OFF OUTPUT-VOLTAGE RATIO : 65dB TYP. @ $f_{is}$ = 10kHz, $R_L$ = 10kΩ
- HIGH DEGREE OF LINEARITY : < 0.5% DISTORTION TYP. @ $f_{is}$ = 1kHz, $V_{is}$ = 5 Vp-p, $V_{DD} - V_{SS} \geq 10V$, $R_L$ = 10kΩ
- EXTREMELY LOW OFF SWITCH LEAKAGE RESULTING IN VERY LOW OFFSET CURRENT AND HIGH EFFECTIVE OFF RESISTANCE ; 10pA TYP. @ $V_{DD} - V_{SS}$ = 10V, $T_A$ = 25°C
- EXTREMELY HIGH CONTROL INPUT IMPEDANCE (control circuit isolated from signal circuit) : $10^{12}$ Ω TYP.
- LOW CROSSTALK BETWEEN SWITCHES : – 50dB TYP. @ $f_{is}$ = 0.9MHz, $R_L$ = 1kΩ
- MATCHED CONTROL-INPUT TO SIGNAL-OUTPUT CAPACITANCE : REDUCES OUTPUT SIGNAL TRANSIENTS
- FREQUENCY RESPONSE, SWITCH ON = 40MHz (typ.)
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

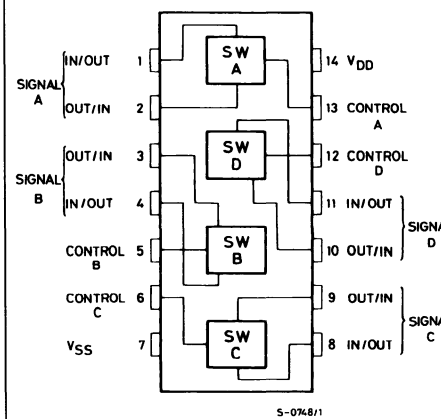
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

| | |
|---|---|
| HCC4066BF | HCF4066BM1 |
| HCF4066BEY | HCF4066BC1 |

**PIN CONNECTIONS**



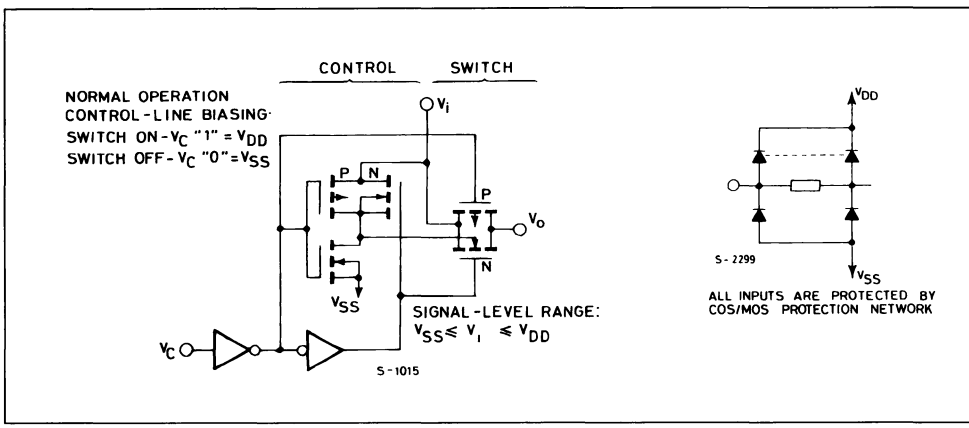

### DESCRIPTION

The **HCC4066B** (extended temperature range) and **HCF4066B** (intermediate temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and plastic micropackage. The **HCC/HCF4066B** is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin

compatible with **HCC/HCF4016B**, but exhibits a much lower ON resistance. In addition, the ON resistance is relatively constant over the full input-signal range. The **HCC/HCF4066B** consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased ON or OFF simultaneously by the control signal. As shown in schematic diagram, the well of the n-channel device on each switch is either tied to the input when the switch is ON or to $V_{SS}$ when the switch is OFF. This configuration eliminates the variation of the switch-transistor threshold voltage with input signal, and thus keeps the ON resistance low over the full operating-signal range. The advantages over single-channel switches include peak input signal voltage swings equal to the full supply voltage, and more constant ON impedance over the input-signal range. For sample-and-hold applications, however, the **HCC/HCF4016B** is recommended.

## SCHEMATIC DIAGRAM

1 OF 4 IDENTICAL SWITCHES AND ITS ASSOCIATED CONTROL CIRCUITRY.




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltage values are referred to $V_{SS}$ pin voltage

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## ELECTRICAL CHARACTERISTICS

($T_{amb}$ = 25°C, typical temperature coefficient for all $V_{DD}$ values is 0,3%/°C)

| Symbol | Parameter | | Test Conditions | $V_I$ (V) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Device Current (all switches ON or all switches OFF) | HCC Types | | 0/ 5 | 5 | | 0.25 | | 0.01 | 0.25 | | 7.5 | µA |
| | | | | 0/10 | 10 | | 0.5 | | 0.01 | 0.5 | | 15 | |
| | | | | 0/15 | 15 | | 1 | | 0.01 | 1 | | 30 | |
| | | | | 0/20 | 20 | | 5 | | 0.02 | 5 | | 150 | |
| | | HCF Types | | 0/ 5 | 5 | | 1 | | 0.01 | 1 | | 7.5 | |
| | | | | 0/10 | 10 | | 2 | | 0.01 | 2 | | 15 | |
| | | | | 0/15 | 15 | | 4 | | 0.01 | 4 | | 30 | |
| **SIGNAL INPUTS** ($V_{is}$) and Outputs ($V_{os}$) | | | | | | | | | | | | | |
| $R_{ON}$ | On Resistance | HCC Types | $V_C = V_{DD}$<br>$R_L$ = 10KΩ Return to $\frac{V_{DD} - V_{SS}}{2}$<br>$V_{is} = V_{SS}$ to $V_{DD}$ | | 5 | | 800 | | 470 | 1050 | | 1300 | Ω |
| | | | | | 10 | | 310 | | 180 | 400 | | 550 | |
| | | | | | 15 | | 200 | | 125 | 240 | | 320 | |
| | | HCF Types | | | 5 | | 850 | | 470 | 1050 | | 1200 | |
| | | | | | 10 | | 330 | | 180 | 400 | | 500 | |
| | | | | | 15 | | 210 | | 125 | 240 | | 300 | |
| ΔON | Resistance between any 2 Switches, $\Delta R_{ON}$ | | $R_L$ 10kΩ, $V_C = V_{DD}$ | | 5 | | | | 15 | | | | Ω |
| | | | | | 10 | | | | 10 | | | | |
| | | | | | 15 | | | | 5 | | | | |
| TDH | Total Harmonic Distorsion | | $V_C = V_{DD}$ = 5V,<br>$V_{SS}$ = − 5V,<br>$V_{is}$ (p-p) = 5V<br>(sine wave centered in 0V)<br>$R_L$ = 10kΩ,<br>$f_{is}$ = 1kHz sine wave | | | | | | 0.4 | | | | % |
| | - 3 dB Cutoff Frequency (switch on) | | $V_C = V_{DD}$ = 5V,<br>$V_{SS}$ = − 5V,<br>$V_{is}$ (p-p) = 5V<br>(sine wave centured on 0V)<br>$R_L$ = 1kΩ | | | | | | 40 | | | | MHz |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.

**ELECTRICAL CHARACTERISTICS** (continued)

| Symbol | Parameter | | Test Conditions | $V_{DD}$ (V) | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | $T_{Low}$* | | 25°C | | | $T_{High}$* | | |
| | | | | | Min. | Max. | Min. | Typ. | Max. | Min. | Max. | |
| | - 50 dB Feedthrough Frequency (switch off) | | $V_C$ = $V_{SS}$ = − 5V, $V_{is}$ (p-p) = 5V (sine wave centured on 0V) $R_L$ = 1kΩ | | | | | 1 | | | | MHz |
| | - 50 dB Crosstalk Frequency | | $V_C$ (A) = $V_{DD}$ = + 5V $V_C$ (B) = $V_{SS}$ = − 5V $V_{is}$ (A) = 5Vp-p, 50Ω source $R_L$ = 1kΩ | | | | | 8 | | | | MHz |
| $t_{pd}$ | Propagation Delay (signal input to signal output) | | $R_L$ = 200kΩ $V_C$ = $V_{DD}$, $V_{SS}$ = GND, $C_L$ = 50pF, $V_{is}$ = 10V (square wave centured on 5V) $t_r$, $t_f$ = 20ns | 5 | | | | 20 | 40 | | | ns |
| | | | | 10 | | | | 10 | 20 | | | |
| | | | | 15 | | | | 7 | 15 | | | |
| $C_{is}$ | Input Capacitance | | $V_{DD}$ = + 5V $V_C$ = $V_{SS}$ = − 5V | | | | | 8 | | | | pF |
| $C_{os}$ | Output Capacitance | | | | | | | 8 | | | | |
| $C_{ios}$ | Feedthrough | | | | | | | 0.5 | | | | |
| | Input/Output Leakage Current Switch OFF | HCC Types | $V_C$ = 0V $V_{is}$ = 18V , $V_{os}$ = 0V $V_{is}$ = 0V ; $V_{os}$ = 18V | 18 | | ± 0.1 | | $\pm 10^{-3}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | $V_C$ = 0V $V_{is}$ = 15V , $V_{os}$ = 0V $V_{is}$ = 0V , $V_{os}$ = 15V | 15 | | ± 0.3 | | $\pm 10^{-3}$ | ± 0.3 | | ± 1 | |
| **CONTROL** ($V_C$) | | | | | | | | | | | | |
| $V_{ILC}$ | Control Input Low Voltage | | $\|I_{is}\|$ < 10μA $V_{is}$ = $V_{SS}$, $V_{os}$ = $V_{DD}$ and $V_{is}$ = $V_{DD}$, $V_{os}$ = $V_{SS}$ | 5 | | 1 | | | 1 | | 1 | V |
| | | | | 10 | | 2 | | | 2 | | 2 | |
| | | | | 15 | | 2 | | | 2 | | 2 | |
| $V_{IHC}$ | Control Input High Voltage | | | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 10 | 7 | | 7 | | | 7 | | |
| | | | | 15 | 11 | | 11 | | | 11 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | $V_{is}$ ≤ $V_{DD}$ $V_{DD}$ − $V_{SS}$ = 18V | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | $V_{DD}$ − $V_{SS}$ = 15V $V_{CC}$ ≤ $V_{DD}$ − $V_{SS}$ | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |

* $T_{Low}$ = − 55°C for **HCC** device − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device · + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is · 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.

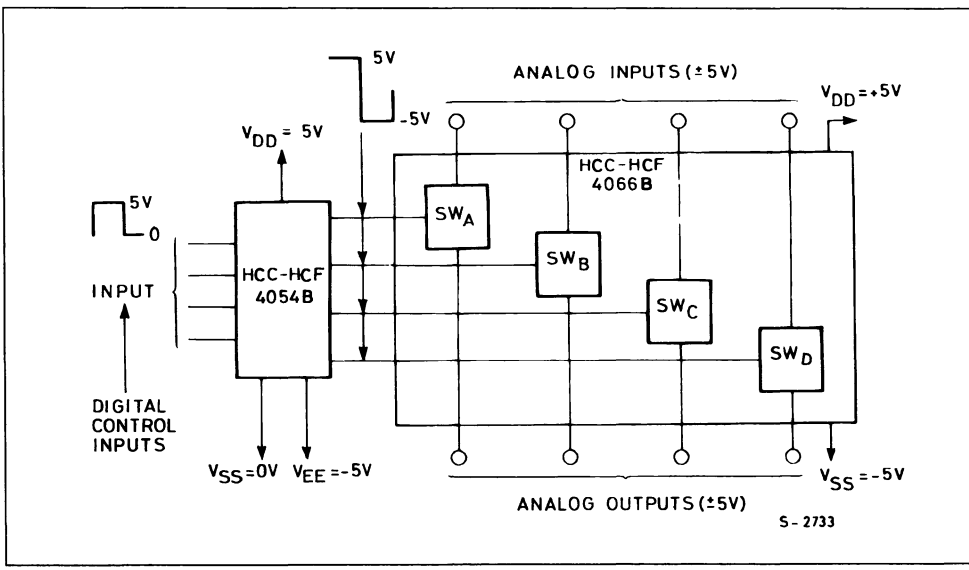
## ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | Test Conditions | $V_{DD}$ (V) | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_{Low}$* | | 25°C | | | $T_{High}$* | | |
| | | | | Min. | Max. | Min. | Typ. | Max. | Min. | Max. | |
| | Crosstalk (control input to signal output) | $V_C$ = 10V (sq. wave)<br>$t_r$, $t_f$ = 20ns<br>$R_L$ = 10kΩ | 10 | | | | 50 | | | | mV |
| | Turn-on Propagation Delay | $V_{IN}$ = $V_{DD}$<br>$t_r$, $t_f$ = 20ns<br>$C_L$ = 50pF<br>$R_L$ = 1kΩ | 5 | | | | 35 | 70 | | | ns |
| | | | 10 | | | | 20 | 40 | | | |
| | | | 15 | | | | 15 | 30 | | | |
| | Control Input Repetition Rate | $V_{is}$ = $V_{DD}$,$V_{SS}$ = GND<br>$R_L$ = 1kΩ to gnd<br>$C_L$ = 50pF<br>$V_C$ = 10V (square wave centured on 5V)<br>$t_r$, $t_f$ = 20ns<br>$V_{os}$ = 1/2$V_{os}$ @ 1kHz | 5 | | | | 6 | | | | MHz |
| | | | 10 | | | | 9 | | | | |
| | | | 15 | | | | 9.5 | | | | |
| $C_I$ | Input Capacitance | Any Input | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device − 40°C for **HCF** device
* $T_{High}$ = + 125°C for **HCC** device + 85°C for **HCF** device
The Noise Margin for both "1" and "0" level is 1V min with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min with $V_{DD}$ = 15V.

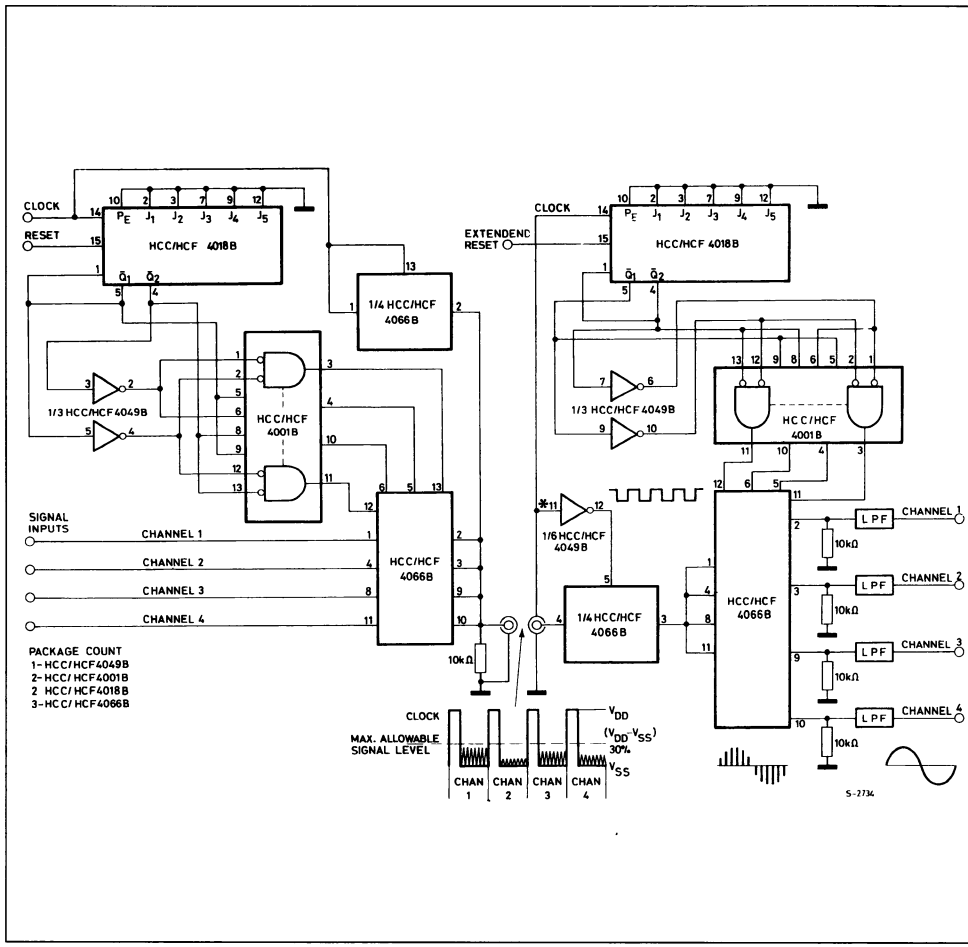
## TYPICAL APPLICATIONS

BIDIRECTIONAL SIGNAL TRANSMISSION VIA DIGITAL CONTROL LOGIC



## TYPICAL APPLICATIONS (continued)

4-CHANNEL PAM MULTIPLEX SYSTEM DIAGRAM.

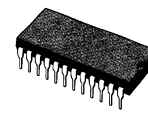


# HCC/HCF4067B
# HCC/HCF4097B

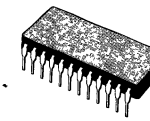
## ANALOG MULTIPLEXER/DEMULTIPLEXER

**4067B–SINGLE 16-CHANNEL**
**4097B–DIFFERENTIAL 8-CHANNEL**

- LOW ON RESISTANCE: 125Ω (typ.) OVER 15 Vp-p SIGNAL INPUT RANGE FOR $V_{DD}$ - $V_{SS}$ = 15V
- HIGH OFF RESISTANCE: CHANNEL LEAKAGE OF ±10pA (typ.) @ $V_{DD}$ - $V_{SS}$ = 10V
- MATCHED SWITCH CHARACTERISTICS: $\Delta R_{ON}$ = 5Ω (typ.) FOR $V_{DD}$ - $V_{SS}$ = 15V
- VERY LOW QUIESCENT POWER DISSIPATION UNDER A DIGITAL CONTROL INPUT AND SUPPLY CONDITIONS: 0.2μW (typ.) @ $V_{DD}$ -$V_{SS}$ = 10V
- BINARY ADDRESS DECODING ON CHIP
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIE CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Package)

**M1**
(Micro Package)

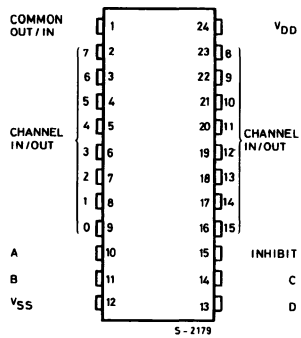
**C1**
(Chip Carrier)

**ORDER CODES :**

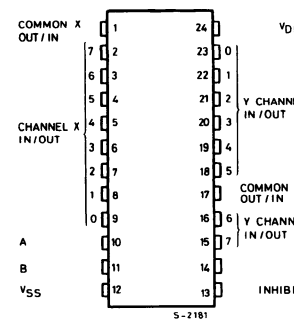
HCC40XXBF HCF40XXBM1
HCF40XXBEY HCF40XXBC1

### PIN CONNECTIONS

**4067B**




**4097B**



## DESCRIPTION

The **HCC4067B, HCC4097B** (extended temperature range) and **HCF4067B, HCF4097B** (intermediate temperature range) are monolithic integrated circuits available in 24-lead dual in line plastic or ceramic package.

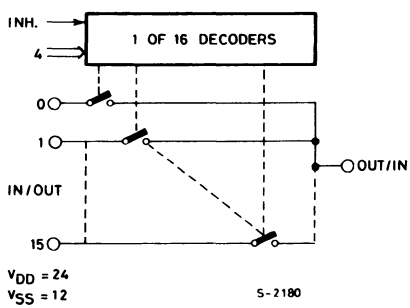
The **HCC/HCF4067B** and **HCC/HCF4097B** COS/MOS analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedance, low OFF leakage current and internal address decoding. in addition, the ON resistance is relatively constant over the full input-signal range.

The **HCC/HCF4067B** ia a 16-channel multiplexer with four binary control inputs A, B, C, D, and an inhibit input, arranged so that any combination of the inputs selects one switch.

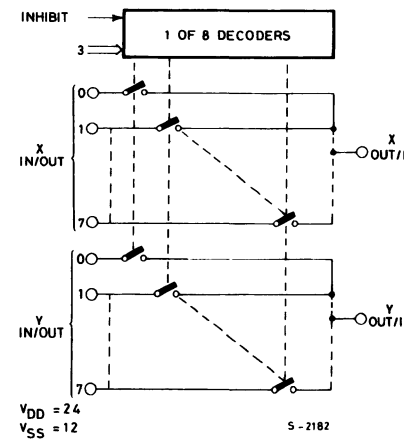
The **HCC/HCF4097** is a differential 8-channel multiplexer having three binary control inputs A, B, C, and an inhibit input. The inputs permit selection of one of eight pairs of switches. A logic "1" present at the inhibit input turn all channels off.

## FUNCTIONAL DIAGRAM

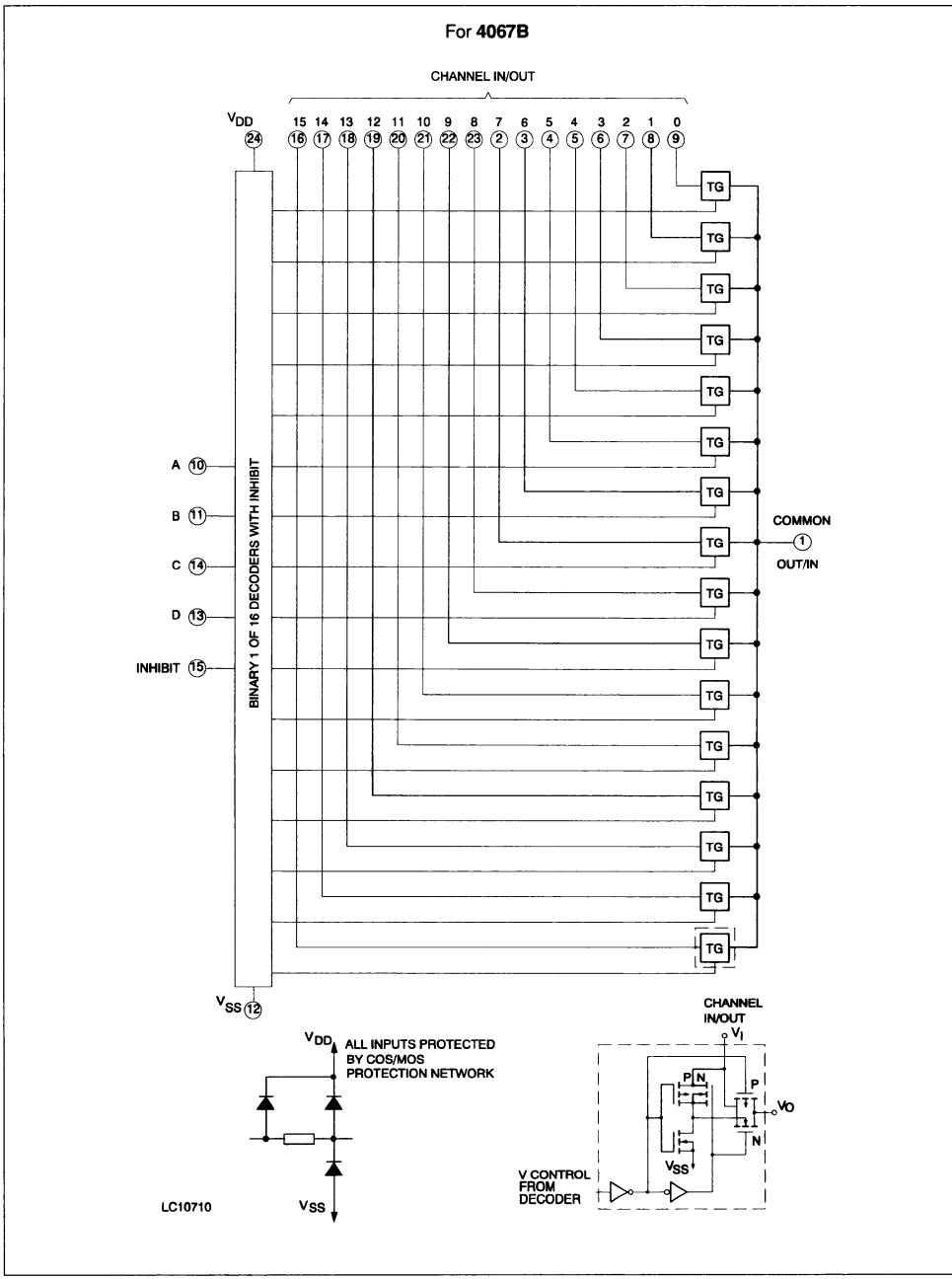
For **4067B**




For **4097B**

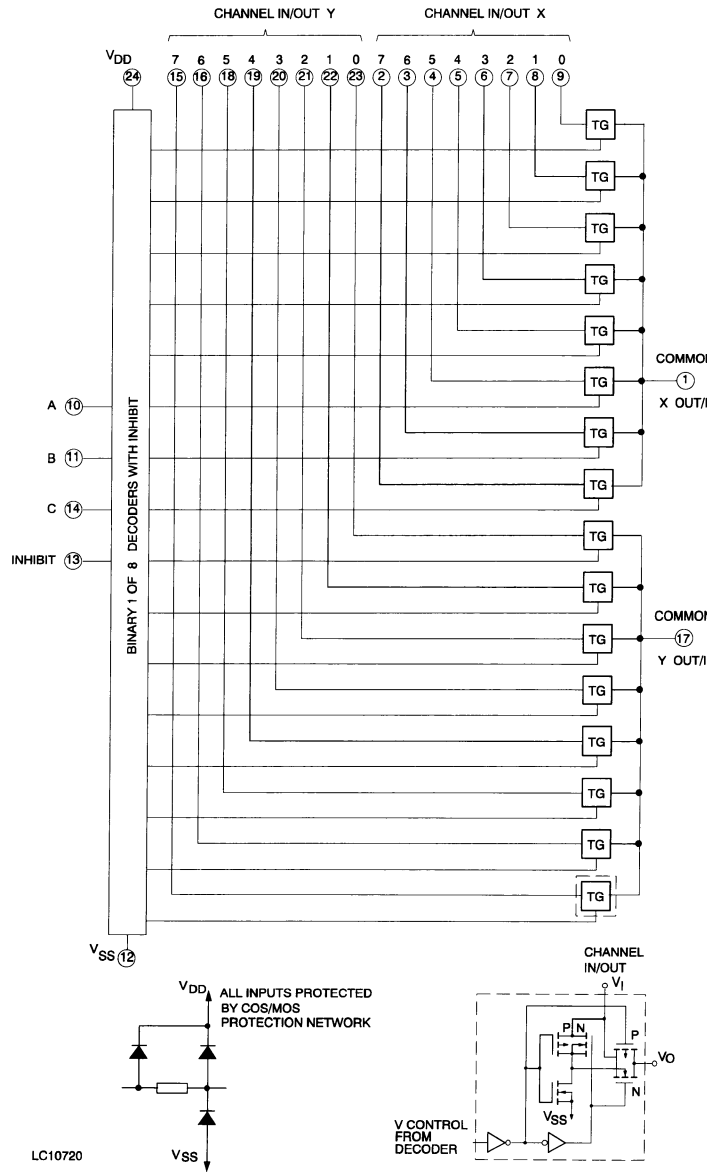


## LOGIC DIAGRAM



## LOGIC DIAGRAM

For **4097B**



## TRUTH TABLES FOR HCC/HCF4067B

| A | B | C | D | INH | SELECTED CHANNEL |
|---|---|---|---|---|---|
| X | X | X | X | 1 | None |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 2 |
| 1 | 1 | 0 | 0 | 0 | 3 |
| 0 | 0 | 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 0 | 0 | 5 |
| 0 | 1 | 1 | 0 | 0 | 6 |
| 1 | 1 | 1 | 0 | 0 | 7 |
| 0 | 0 | 0 | 1 | 0 | 8 |
| 1 | 0 | 0 | 1 | 0 | 9 |
| 0 | 1 | 0 | 1 | 0 | 10 |
| 1 | 1 | 0 | 1 | 0 | 11 |
| 0 | 0 | 1 | 1 | 0 | 12 |
| 1 | 0 | 1 | 1 | 0 | 13 |
| 0 | 1 | 1 | 1 | 0 | 14 |
| 1 | 1 | 1 | 1 | 0 | 15 |

## TRUTH TABLE FOR HCC/HCF4097B

| A | B | C | INH | SELECTED CHANNEL |
|---|---|---|---|---|
| X | X | X | 1 | None |
| 0 | 0 | 0 | 0 | 0X 0Y |
| 1 | 0 | 0 | 0 | 1X 1Y |
| 0 | 1 | 0 | 0 | 2X 2Y |
| 1 | 1 | 0 | 0 | 3X 3Y |
| 0 | 0 | 1 | 0 | 4X 4Y |
| 1 | 0 | 1 | 0 | 5X 5Y |
| 0 | 1 | 1 | 0 | 6X 6Y |
| 1 | 1 | 1 | 0 | 7X 7Y |

## ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ * | Supply Voltage: **HCC** Types<br>**HCF** Types | -0.5 to +20<br>-0.5 to +18 | V<br>V |
| $V_I$ | Input Voltage | -0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for Top = Full Package Temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage: **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditios $V_{IS}$ (V) | $V_{EE}$ (V) | $V_{SS}$ (V) | $V_{DD}$ (V) | Value $T_{LOW}$ * Min. | $T_{LOW}$ * Max. | 25 °C Min. | 25 °C Typ. | 25 °C Max. | $T_{HIGH}$ * Min. | $T_{HIGH}$ * Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Supply Current | HCC types | | | | 5 | | 5 | | 0.04 | 5 | | 150 | µA |
| | | | | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF types | | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| **SWITCH** | | | | | | | | | | | | | | |
| $R_{ON}$ | On Resistance | HCC types | $0 \le V_I \le V_{DD}$ | 0 | 0 | 5 | | 800 | | 470 | 1050 | | 1300 | Ω |
| | | | | | | 10 | | 310 | | 180 | 400 | | 580 | |
| | | | | | | 15 | | 200 | | 125 | 240 | | 320 | |
| | | HCF types | $0 \le V_I \le V_{DD}$ | 0 | 0 | 5 | | 850 | | 470 | 1050 | | 1200 | |
| | | | | | | 10 | | 330 | | 180 | 400 | | 520 | |
| | | | | | | 15 | | 210 | | 125 | 240 | | 300 | |
| ΔON | Resistance $\Delta R_{ON}$ (Between any two channels) | | | 0 | 0 | 5 | | | | 10 | | | | Ω |
| | | | | | | 10 | | | | 10 | | | | |
| | | | | | | 15 | | | | 5 | | | | |
| OFF (•) Channel Leakage Current | Any Channel OFF | HCC types | | 0 | 0 | 18 | | 100 | | ±0.1 | 100 | | 1000 | µA |
| | All Channel OFF (common OUT/IN) | HCC types | | 0 | 0 | 18 | | 100 | | ±0.1 | 100 | | 1000 | |
| | Any Channel OFF | HCF types | | 0 | 0 | 15 | | 300 | | ±0.1 | 300 | | 1000 | |
| | All Channel OFF (common OUT/IN) | HCF types | | 0 | 0 | 15 | | 300 | | ±0.1 | 300 | | 1000 | |
| C | Capacitance Input<br>Output for 4067<br>Output for 4097<br>Feedthrough | | | | -5 | 5 | | | | 5<br>55<br>35<br>0.2 | | | | pF |
| **CONTROL** | | | | | | | | | | | | | | |
| $V_{IL}$ | Input Low Voltage | | = $V_{DD}$ thru 1KΩ | $V_{EE}=V_{SS}$ $R_L$ =1KΩ to $V_{SS}$ $I_{IS}$ < 2µA (on all OFF channels) | | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | | | 10 | | 3 | | | 3 | | 3 | |
| | | | | | | 15 | | 4 | | | 4 | | 4 | |
| $V_{IH}$ | Input High Voltage | | | | | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | | | 10 | 7 | | 7 | | | 7 | | |
| | | | | | | 15 | 11 | | 11 | | | 11 | | |
| $I_{IH}$ $I_{IL}$ | Input Leakage Current | HCC types | $V_I$ = 0/18V | | | 18 | | ±0.1 | | $\pm 10^{-3}$ | ±0.1 | | ±1 | µA |
| | | HCF types | $V_I$ = 0/15V | | | 15 | | ±0.3 | | $\pm 10^{-3}$ | ±0.3 | | ±1 | |
| $C_I$ | Input Capacitance | | Any Address or Inhibit Input | | | | | | | 5 | 7.5 | | | pF |

• Determined by minimum feasible leakage measurement for automatic testing
* $T_{LOW}$ = -55 °C for **HCC** device: -40 °C for **HCF** device.
* $T_{HIGH}$ = +125 °C for **HCC** device: +85 °C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with $V_{DD}$ = 5 V, 2 V min. with $V_{DD}$ = 10 V, 2.5 V min. with $V_{DD}$ = 15 V

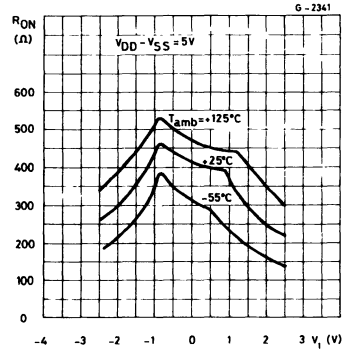
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 KΩ, typical temperature coefficent for all $V_{DD}$ values is 03 %/°C, all input rise and fall times= 20 ns)

| Symbol | Parameter | Test Conditions | | | | | | | | Value | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_C$ (V) | $R_L$ (KΩ) | $f_i$ (KHz) | $V_I$ (V) | $V_{SS}$ (V) | $V_{DD}$ (V) | | | Typ. | Max. | |
| **SWITCH** | | | | | | | | | | | | |
| $t_{pd}$ | Propagation Delay Time (Signal Input to Output) | = $V_{DD}$ | 200 | | ⎍ | 0 | 5 | | | 30 | 60 | ns |
| | | | | | | | 10 | | | 15 | 30 | |
| | | | | | | | 15 | | | 11 | 20 | |
| | Frequency Response Channel "ON" (Sine Wave Input) at $20\ Log \frac{V_O}{V_I} = -3\ dB$ | = $V_{DD}$ | 1 | | 5 (•) | 0 | 10 | $V_O$ at Common OUT/IN | 4067B | 14 | | ns |
| | | | | | | | | | 4097B | 20 | | |
| | | | | | | | | $V_O$ at Any Channel | | 60 | | |
| | Feedthrough (All Channels OFF) at $20\ Log \frac{V_O}{V_I} = -40\ dB$ | = $V_{SS}$ | 1 | | 5 (•) | 0 | 10 | $V_O$ at Common OUT/IN | 4067B | 20 | | MHz |
| | | | | | | | | | 4097B | 12 | | |
| | | | | | | | | $V_O$ at Any Channel | | 8 | | |
| | Frequency Signal Crosstalk at $20Log \frac{V_{O(B)}}{V_{I(A)}} = -40dB$ | $V_{C(A)}$=$V_{DD}$ $V_{C(B)}$=$V_{SS}$ | 1 | | 5 (•) | 0 | 10 | Between Any two (A and B) Channels | | 1 | | MHz |
| | | | | | | | | Between Sections (A and B) 4097B only | Measured on common | 10 | | |
| | | | | | | | | | Measured on Any Channel | 18 | | |
| tw | Sine Wave Distortion ($f_{is}$ = 1KHz sine wave) | 5 | 10 | 1 | 2 (•) | 0 | 5 | | | 0.3 | | % |
| | | 10 | 10 | 1 | 3 (•) | 0 | 10 | | | 0.2 | | |
| | | 15 | 10 | 1 | 5 (•) | 0 | 15 | | | 0.12 | | |
| **CONTROL** (address or Inhibit) | | | | | | | | | | | | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time: Address or Inhibit to Signal OUT (Channel Turning ON) | $V_{DD}$ 0 ⎍ | 1 | | | 0 | 5 | | | 325 | 650 | ns |
| | | | | | | 0 | 10 | | | 135 | 270 | |
| | | | | | | 0 | 15 | | | 95 | 190 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time: Address or Inhibit to Signal OUT (Channel Turning OFF) | $V_{DD}$ 0 ⎍ | 0.3 | | | 0 | 5 | | | 220 | 440 | ns |
| | | | | | | 0 | 10 | | | 90 | 180 | |
| | | | | | | 0 | 15 | | | 65 | 130 | |
| | Address or Inhibit to Signal Crosstalk | $V_{DD}$ 0 ⎍ | 10* | | | 0 | 10 | | | 75 | | mV peak |

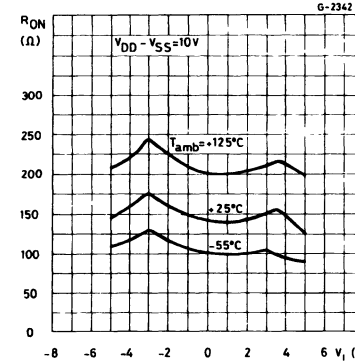
(•) Peak to peak voltage symmetrical about $\frac{V_{DD} - V_{SS}}{2}$

(*) Both ends of channel

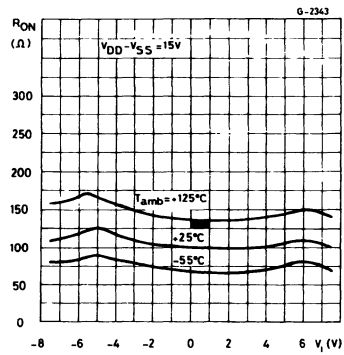
Typical ON Resistance vs Input Signal Voltage (All Types)



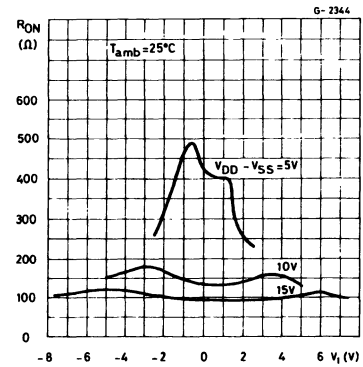

Typical ON Resistance vs Input Signal Voltage (All Types)




Typical ON Resistance vs Input Signal Voltage (All Types)

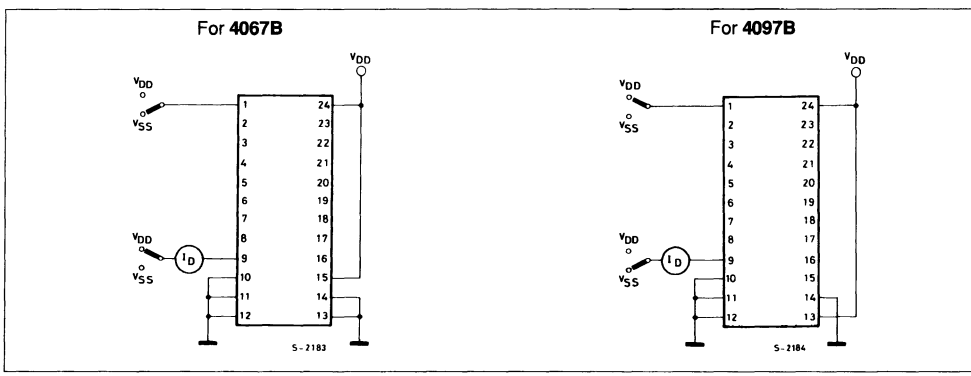



Typical ON Resistance vs Input Signal Voltage (All Types)



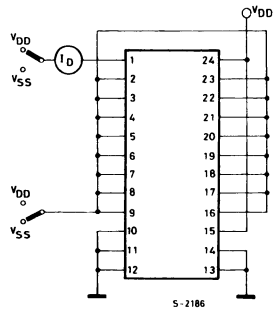

## TEST CIRCUITS

OFF Channel Leakage Current Any Channel OFF

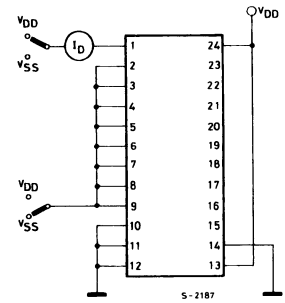


OFF Channel Leakage Current All Channels OFF

For **4067B**

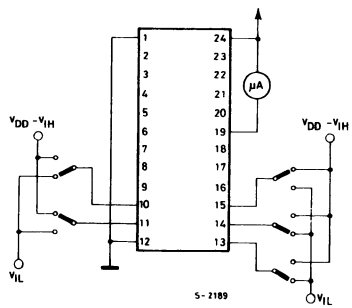



For **4097B**

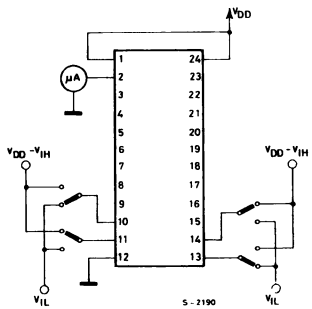



Input Voltage Measure < 2 μA an All OFF Channels (e.g. Channel 12)

For **4067B**

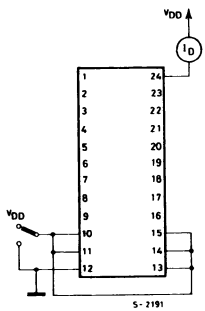



For **4097B**

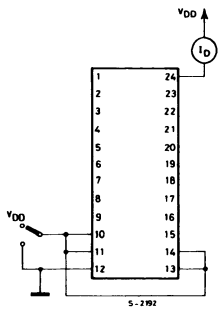



Quiescent Device Current

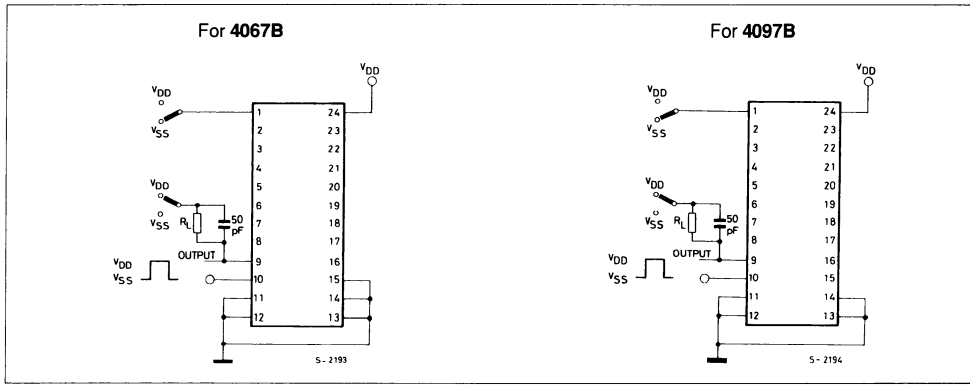
For **4067B**



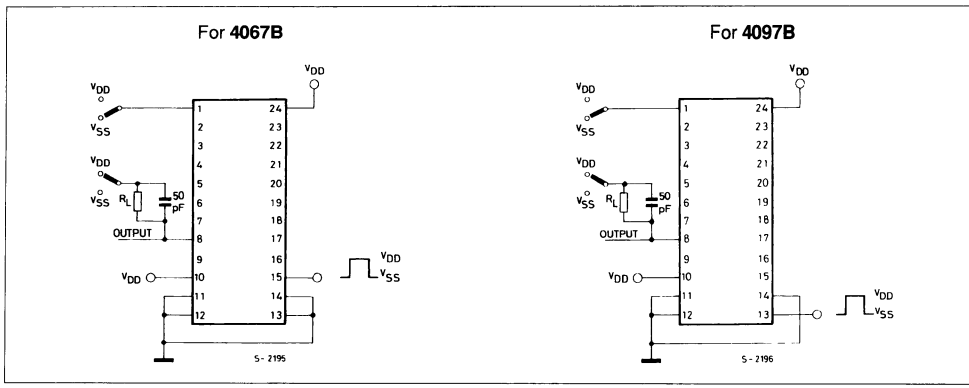

For **4097B**



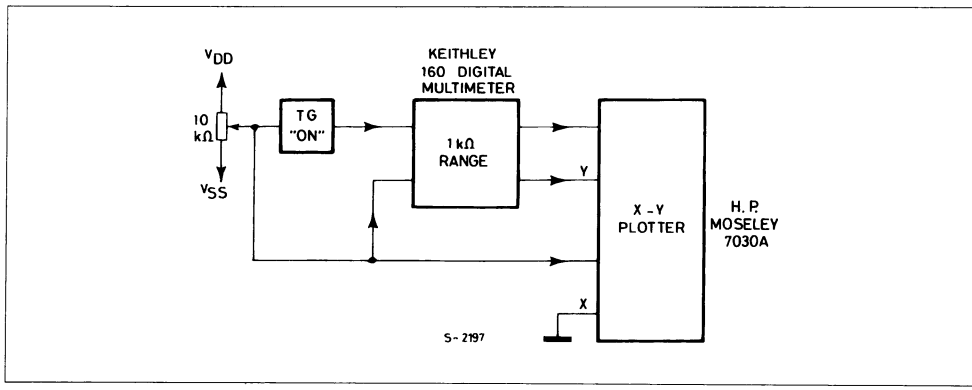
Turn-on and Turn-off Propagation Delay Address Select Input to Signal Output (e. g. Channel 0)



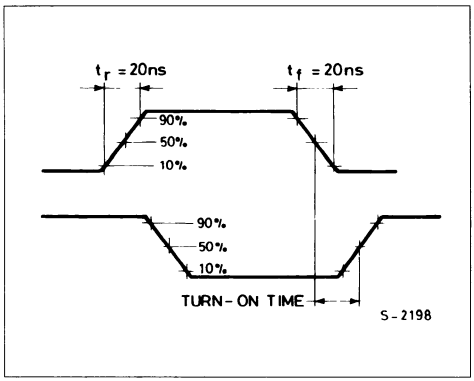

Turn-on and Turn-off Propagation Delay-Inhibit Input to Signal Output (e. g. Channel 1)



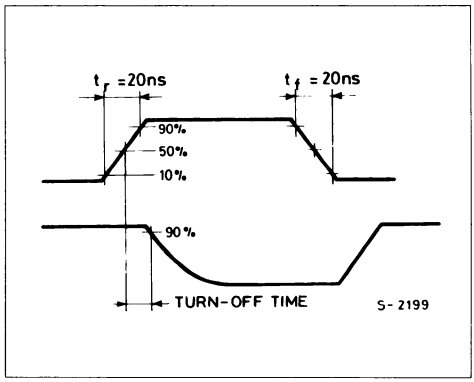

Channel ON Resistance Measurement Circuit



Propagation Delay Waveform Channel Being Turned ON ($R_L$ = 10 KΩ, $C_L$ = 50 pF)




Propagation Delay Waveform Channel Being Turned OFF ($R_L$ = 300 Ω, $C_L$ = 50 pF)




## APPLICATIONS INFORMATION

In applications where separate power sources are used to drive $V_{DD}$ and the signal inputs, the $V_{DD}$ current capability should exceed $V_{DD}/R_L$ ($R_L$ = effective external load). This provision avoids permanent current flow or clamp action on the $V_{DD}$ supply when power is applied or removed from the **HCC/HCF4067B** or **HCC/HCF4097B.**

When switching from one address to another, some of the ON periods of the channels of the multiplexers will overlap momentarily, which may be objectionable in certain applications. Also when a channel is turned ON or OFF by an address input, there is a momentary conductive path from the channel to VSS, which will drump some charge from any capacitor connected to the input or output of the channel. The inhibit input turning on a channel will similarly drump some charge to $V_{SS}$.

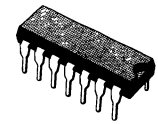
The amount of charge dumped is mostly a function of the signal level above $V_{SS}$.
Typically, ay $V_{DD}$ - $V_{SS}$ = 10V, a 100 pF capacitor connected to the input or output of the channel will lose 3-4% of its voltage at the moment the channel turns ON or OFF. This loss of voltage is essentially independent of the address or inhibit signal trnasition time, if the transition time is less than 1- 2 μs. When the inhibit signal turns a channel off, there is no change dumping of $V_{SS}$. Rather, there is a slight rise in the channel voltage level (65 mV typ.) due to the capacitance coupling from inhibit input to channel input or output. Address input also couple some voltage steps onto the channel signal levels.

In certain applications, the external load-resistor current may include both $V_{DD}$ and signal line components. To avoid drawing $V_{DD}$ current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 V (calculated from $R_{ON}$ values shown in ELECTRICAL CHARACTERISTICS CHART). No VDD current will flow through $R_L$ if the switch current flows into terminal 1 on the **HCC/HCF4067B**, terminals 1 and 17 on the **HCC/HCF4097B.**

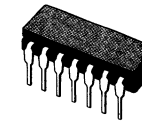
# HCC/HCF4068B

## 8-INPUT NAND/AND GATE

- MEDIUM-SPEED OPERATION – $t_{PHL}$, $t_{PLH}$ = 75ns (typ.) AT 10V
- BUFFERED OUTPUT
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

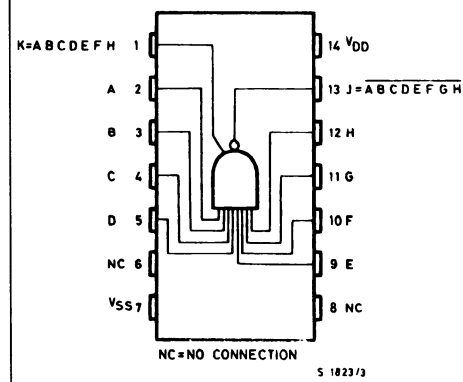
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

| | |
|---|---|
| HCC4068BF | HCF4068BM1 |
| HCF4068BEY | HCF4068BC1 |

**PIN CONNECTIONS**




### DESCRIPTION

The **HCC4068B** (extended temperature range) and **HCF4068B** (intermediate temperature range) are monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF4068B** NAND/AND gate provides the system designer with direct implementation of the positive-logic 8-input NAND and AND functions and supplements the existing family of COS/MOS gates.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to 125<br>− 40 to 85 | °C<br>°C |

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{Low}$* | | 25°C | | | $T_{High}$* | | |
| | | | | | | | Min. | Max. | Min. | Typ. | Max. | Min. | Max. | |
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 0.25 | | 0.01 | 0.25 | | 7.5 | μA |
| | | | 0/10 | | | 10 | | 0.5 | | 0.01 | 0.5 | | 15 | |
| | | | 0/15 | | | 15 | | 1 | | 0.01 | 1 | | 30 | |
| | | | 0/20 | | | 20 | | 5 | | 0.02 | 5 | | 150 | |
| | | HCF Types | 0/ 5 | | | 5 | | 1 | | 0.01 | 1 | | 7.5 | |
| | | | 0/10 | | | 10 | | 2 | | 0.01 | 2 | | 15 | |
| | | | 0/15 | | | 15 | | 4 | | 0.01 | 4 | | 30 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.

## STATIC ELECTRICAL CHARACTERISTICS (continued)

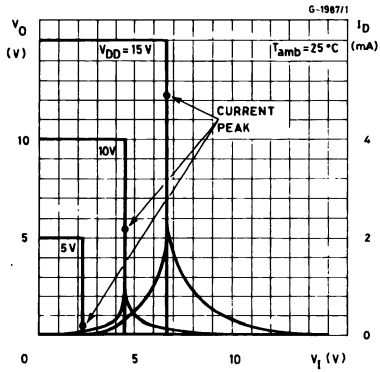
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | – 2 | | – 1.6 | – 3.2 | | – 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | – 0.64 | | – 0.51 | – 1 | | – 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | – 1.6 | | – 1.3 | – 2.6 | | – 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | – 4.2 | | – 3.4 | – 6.8 | | – 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | – 1.53 | | – 1.36 | – 3.2 | | – 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | – 0.52 | | – 0.44 | – 1 | | – 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | – 1.3 | | – 1.1 | – 2.6 | | – 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | – 3.6 | | – 3.0 | – 6.8 | | – 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input leakage Curent | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = – 55°C for **HCC** device : – 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device · + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.

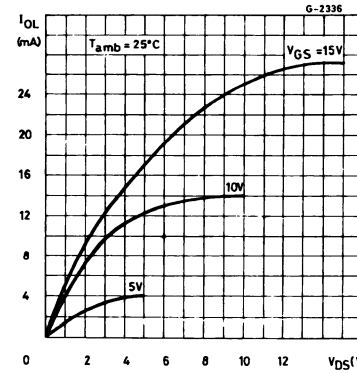
## DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall times = 20ns)

| Symbol | Parameter | Test Conditions | $V_{DD}$ (V) | Value Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time | | 5 | | 150 | 300 | ns |
| | | | 10 | | 75 | 150 | |
| | | | 15 | | 55 | 110 | |
| $t_{TLH}$, $t_{THL}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

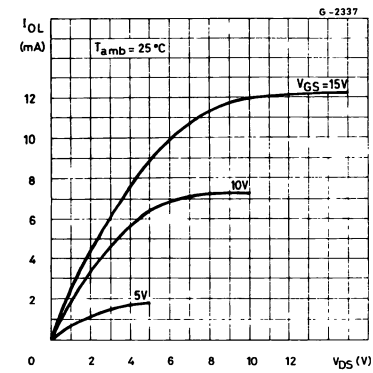
Typical Voltage and Current Transfer Characteristics.



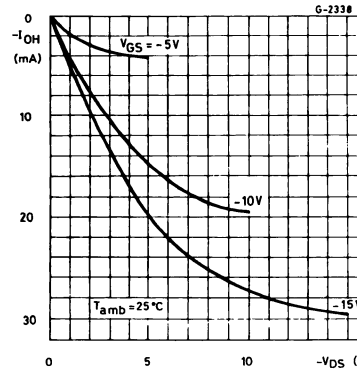

Typical Output Low (sink) Current Characteristics.



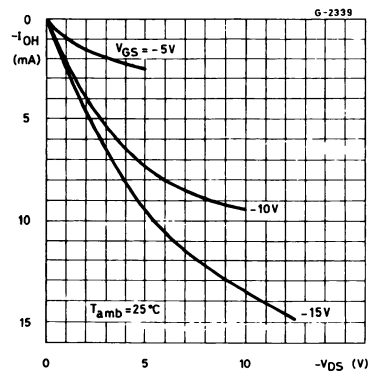

Minimum Output Low (sink) Current Characteristics.



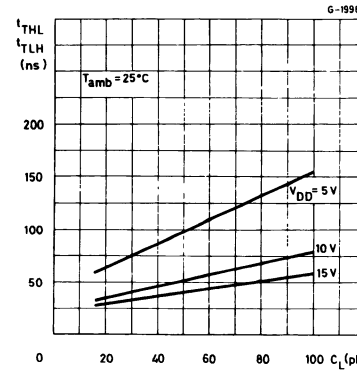

Typical Output High (source) Current Characteristics.




Minimum Output-p-channel Drain Characteristics.

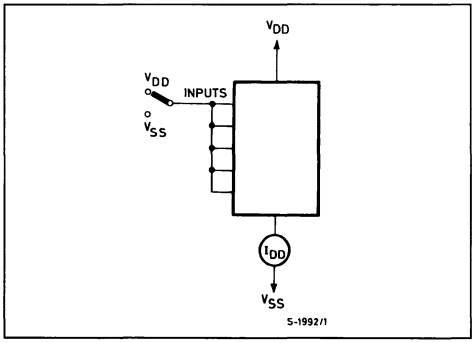



Typical Transition Time vs. $C_L$.

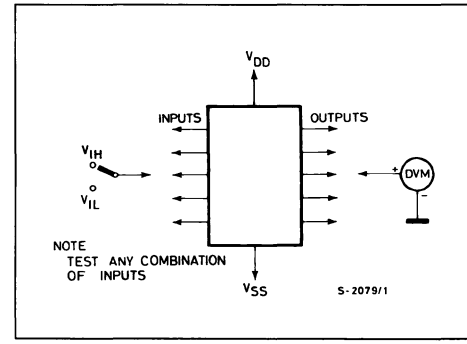


## TEST CIRCUITS

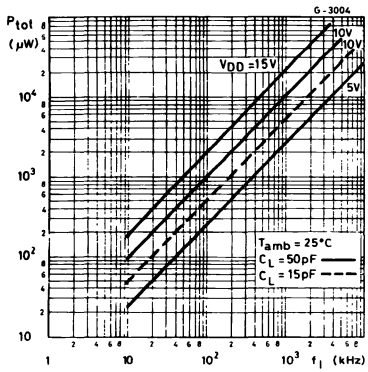
Quiescent Device Current.



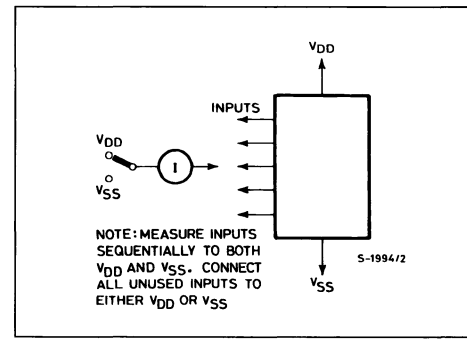

Input Voltage.




Typical Dynamic Power Dissipation vs. Frequency.



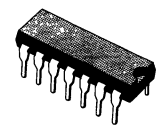

Input Current.



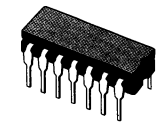
# HCC/HCF4069UB

## HEX INVERTER

- MEDIUM-SPEED OPERATION
  – $t_{PHL}$, $t_{PLH}$ = 30ns (typ.) AT 10V
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

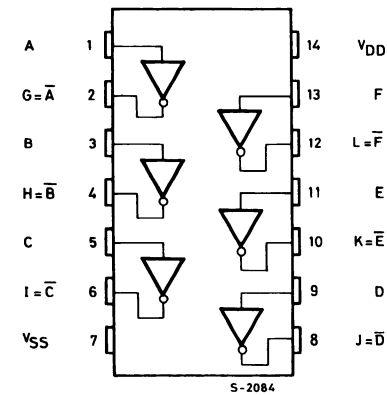
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

| | |
|---|---|
| HCC4069UBF | HCF4069UBM1 |
| HCF4069UBEY | HCF4069UBC1 |

**PIN CONNECTIONS**

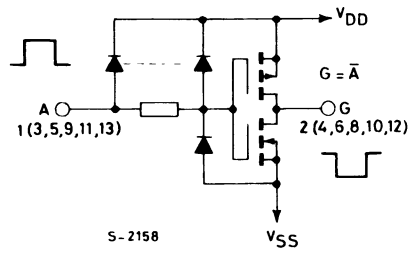



### DESCRIPTION

The **HCC4069UB** (extended temperature range) and **HCF4069UB** (intermediate temperature range) are monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package and plastic micro package.

The **HCC/HCF4069UB** consists of six COS/MOS inverter circuits. This device is intended for all general-purpose inverter applications where the medium-power TTL-drive and logic-level-conversion capabilities of circuits such as **HCC/HCF4049B** Hex Inverter/Buffers are not required.

## SCHEMATIC DIAGRAM OF ONE OF SIX IDENTICAL INVERTERS.




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for Top = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to $V_{SS}$ pin voltage

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

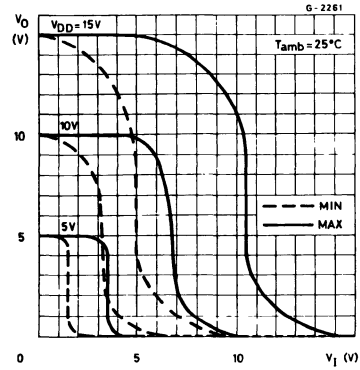
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 0.25 | | 0.01 | 0.25 | | 7.5 | μA |
| | | | 0/10 | | | 10 | | 0 5 | | 0.01 | 0.5 | | 15 | |
| | | | 0/15 | | | 15 | | 1 | | 0.01 | 1 | | 30 | |
| | | | 0/20 | | | 20 | | 5 | | 0.02 | 5 | | 150 | |
| | | HCF Types | 0/ 5 | | | 5 | | 1 | | 0.01 | 1 | | 7.5 | |
| | | | 0/10 | | | 10 | | 2 | | 0.01 | 2 | | 15 | |
| | | | 0/15 | | | 15 | | 4 | | 0.01 | 4 | | 30 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 4 | | 4 | | | 4 | | V |
| | | | | 1/9 | < 1 | 10 | 8 | | 8 | | | 8 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 12.5 | | 12.5 | | | 12.5 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1 | | | 1 | | 1 | V |
| | | | | 9/1 | < 1 | 10 | | 2 | | | 2 | | 2 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 2.5 | | | 2.5 | | 2.5 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2 6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V

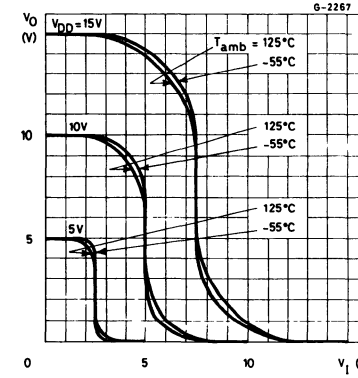
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ = 0.3%/°C values, all input rise and fall time = 20ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time | | 5 | | 55 | 110 | ns |
| | | | 10 | | 30 | 60 | |
| | | | 15 | | 25 | 50 | |
| $t_{TLH}$, $t_{THL}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

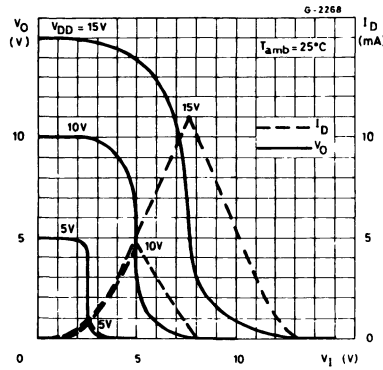
Minimum and Maximum Voltage Transfer Characteristics.



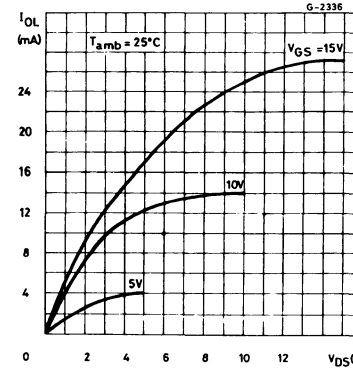

Typical Voltage Transfer Characteristics as a Function of Temperature.



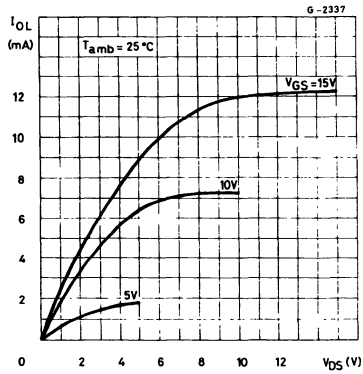

Typical Current and Voltage Transfer Characteristics.



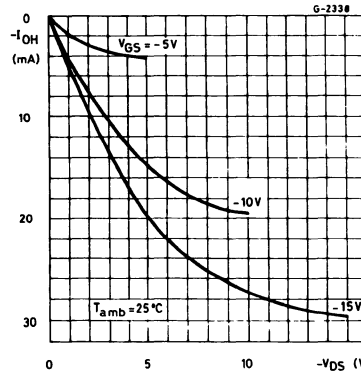

Typical Output Low (sink) Current Characteristics.



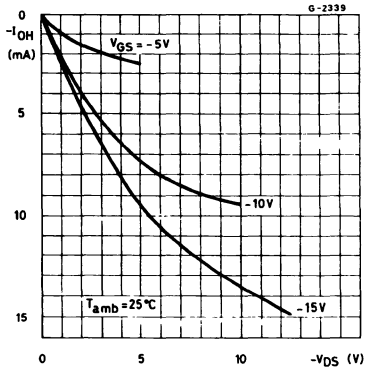
Minimum Output Low (sink) Current Characteristics.



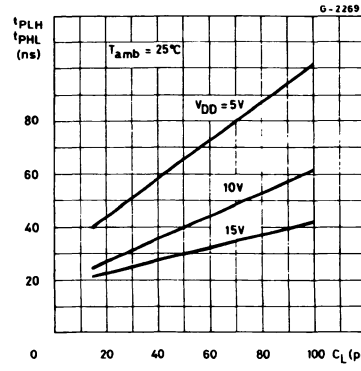

Typical Output High (source) Current Characteristics.



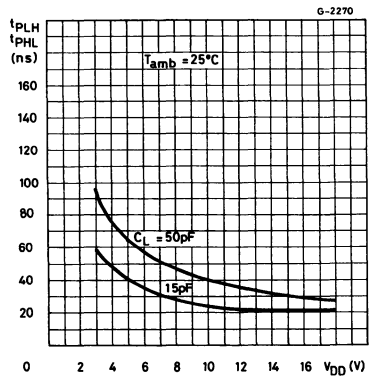

Minimum Output High (source) Current Characteristics.



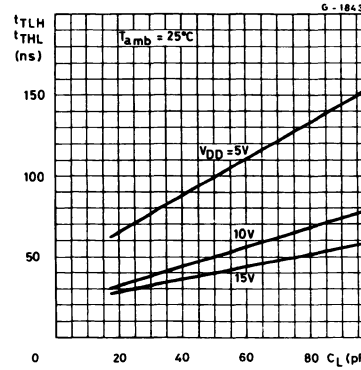

Typical Propagation Delay Time vs. Load Capacitance.



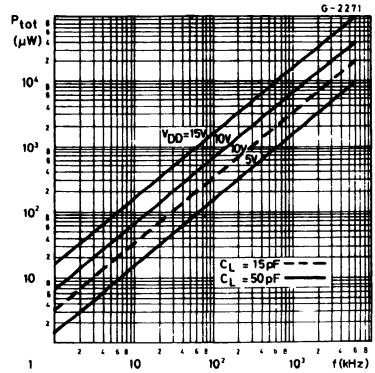

Typical Propagation Delay Time vs. Load Capacitance.



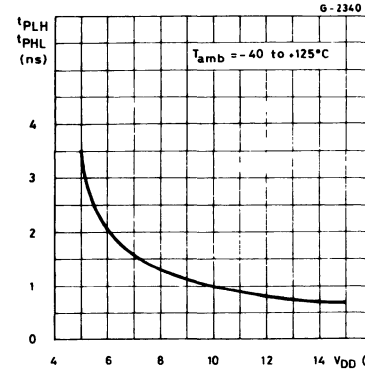

Typical Transition Time vs. Load Capacitance.



Typical Dynamic Power Dissipation/per Inverter vs. Frequency.

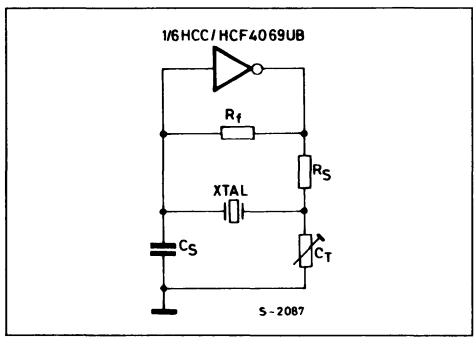



Variation of Normalized Propagation Delay Time ($t_{PHL}$ and $t_{PLH}$) with Supply Voltage.

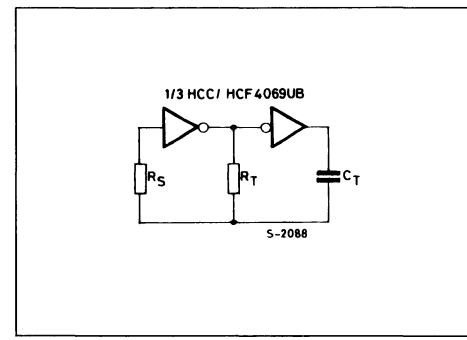



## APPLICATIONS

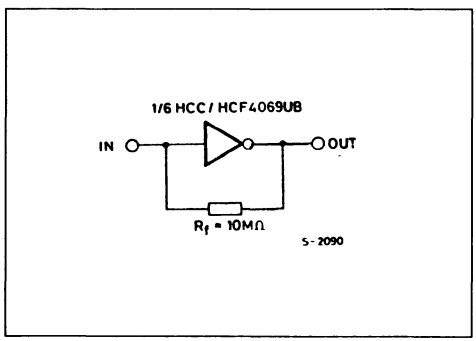
Typical Crystal Oscillator Circuit.



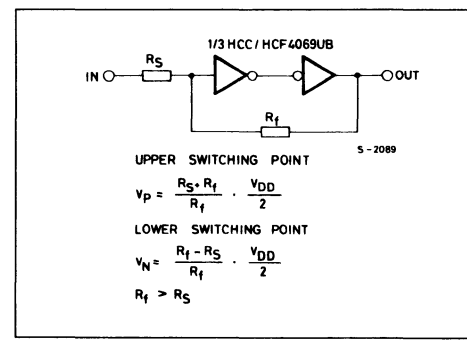

Typical RC Oscillator Circuit.



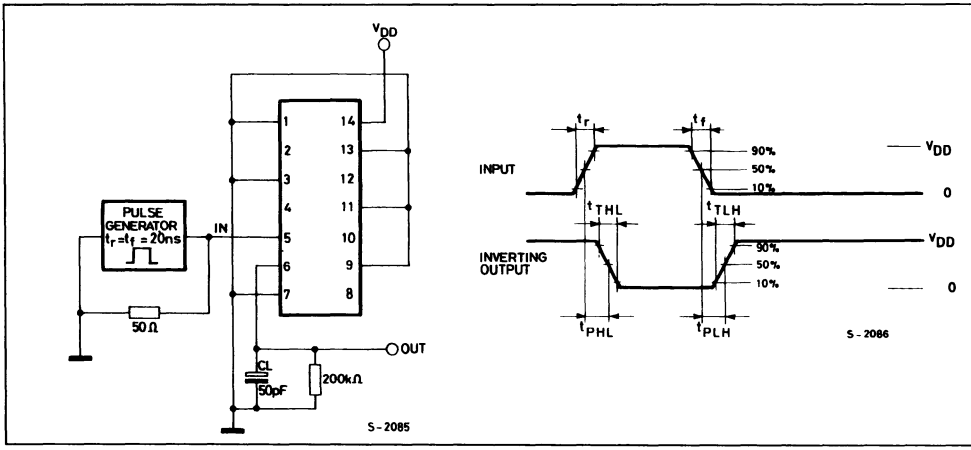

High Input Impedance Amplifier.




Input Pulse Shaping Circuit (schmitt trigger).

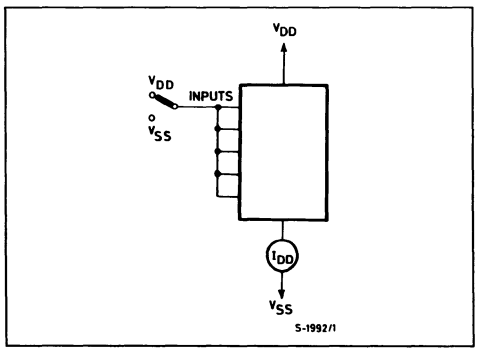


## DYNAMIC ELECTRICAL CHARACTERISTICS AND WAVEFORMS

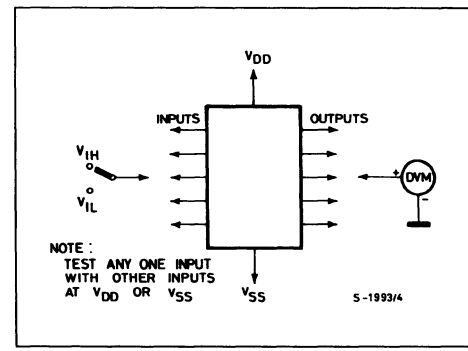



## TEST CIRCUITS

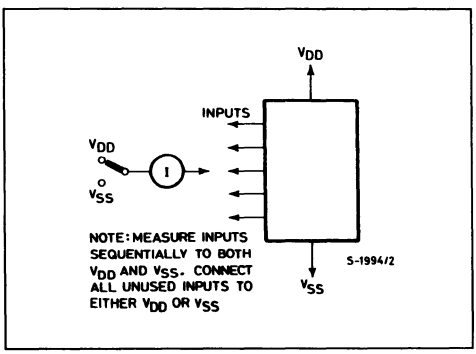
Quiescent Device Current.




Noise Immunity.

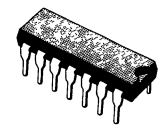



Input Leakage Current.

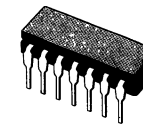


**4070B–QUAD EXCLUSIVE–OR GATE**
**4037B–QUAD EXCLUSIVE–NOR GATE**

- MEDIUM-SPEED OPERATION $t_{PHL}$ = $t_{PLH}$ = 70ns (typ.) AT $V_{CC}$ = 10V, $C_L$ = 50pF
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V AND 15V PARAMETRIC RATING
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Package)

**M1**
(Micro Package)

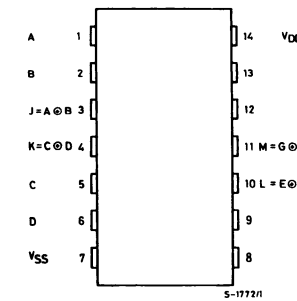
**C1**
(Chip Carrier)

**ORDER CODES :**

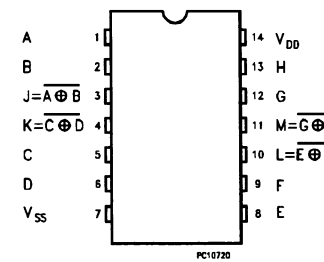
HCC40XXBF HCF40XXBM1
HCF40XXBEY HCF40XXBC1

**PIN CONNECTIONS**

**4070B**




**4077B**




## DESCRIPTION

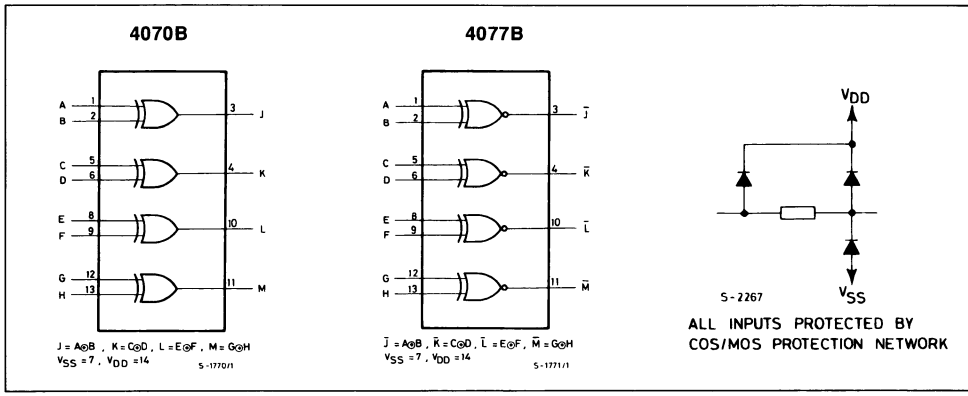
The **HCC4070B/4077B** (extended temperature range) and **HCF4070B/4077B** (intermediate temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and plastic micropackage.

The **HCC/HCF4070B** contains four independent exclusive-OR gates.

The **HCC/HCF4077B** contains four independent exclusive-NOR gates.

The **HCC/HCF4070B** and **HCC/HCF4077B** provide the system designer with a means for direct implementation of the exclusive-OR and exclusive-NOR function, respectively. For applications as Logical comparators, Adders/subtractors, Parity generators and checkers.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ * | Supply Voltage: **HCC** Types<br>**HCF** Types | -0.5 to +20<br>-0.5 to +18 | V<br>V |
| $V_I$ | Input Voltage | -0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for Top = Full Package Temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to $V_{SS}$ pin voltage

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage: **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |

## TRUTH TABLES (1 of 4 gates)

| HCC4070B | | |
|---|---|---|
| **A** | **B** | **J** |
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

| HCC4077B | | |
|---|---|---|
| **A** | **B** | **J** |
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditios $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{LOW}$ * Min. | $T_{LOW}$ * Max. | 25 °C Min. | 25 °C Typ. | 25 °C Max. | $T_{HIGH}$ * Min. | $T_{HIGH}$ * Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/5 | | | 5 | | 1 | | 0.02 | 1 | | 30 | μA |
| | | | 0/10 | | | 10 | | 2 | | 0.02 | 2 | | 60 | |
| | | | 0/15 | | | 15 | | 4 | | 0.02 | 4 | | 120 | |
| | | | 0/20 | | | 20 | | 20 | | 0.04 | 20 | | 600 | |
| | | HCF Types | 0/5 | | | 5 | | 4 | | 0.02 | 4 | | 30 | |
| | | | 0/10 | | | 10 | | 8 | | 0.02 | 8 | | 60 | |
| | | | 0/15 | | | 15 | | 16 | | 0.02 | 16 | | 120 | |
| $V_{OH}$ | Output High Voltage | | 0/5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OL}$ | Output Drive Current | HCC Types | 0/5 | 2.5 | | 5 | -2 | | -1.6 | -3.2 | | -1.15 | | mA |
| | | | 0/5 | 4.6 | | 5 | -0.64 | | -0.51 | -1 | | -0.36 | | |
| | | | 0/10 | 9.5 | | 10 | -1.6 | | -1.3 | -2.6 | | -0.9 | | |
| | | | 0/15 | 13.5 | | 15 | -4.2 | | -3.4 | -6.8 | | -2.4 | | |
| | | HCF Types | 0/5 | 2.5 | | 5 | -1.53 | | -1.36 | -3.2 | | -1.1 | | |
| | | | 0/5 | 4.6 | | 5 | -0.52 | | -0.44 | -1 | | -0.36 | | |
| | | | 0/10 | 9.5 | | 10 | -1.3 | | -1.1 | -2.6 | | -0.9 | | |
| | | | 0/15 | 13.5 | | 15 | -3.6 | | -3.0 | -6.8 | | -2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ±0.1 | | $±10^{-5}$ | ±0.1 | | ±1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ±0.3 | | $±10^{-5}$ | ±0.3 | | ±1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{LOW}$ = -55 °C for **HCC** device: -40 °C for **HCF** device.

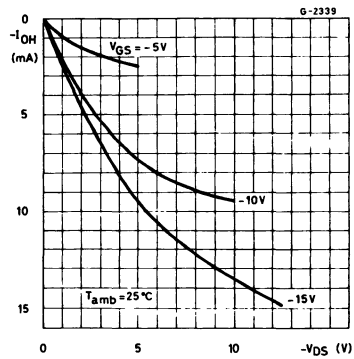
* $T_{HIGH}$ = +125 °C for **HCC** device: +85 °C for **HCF** device.

The Noise Margin for both "1" and "0" level is: 1V min. with $V_{DD}$ = 5 V, 2 V min. with $V_{DD}$ = 10 V, 2.5 V min. with $V_{DD}$ = 15 V

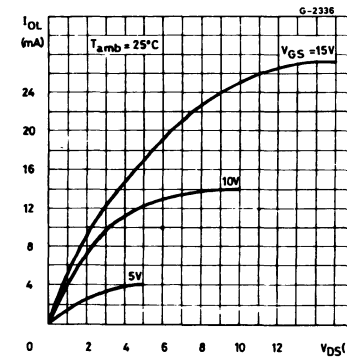
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 KΩ, typical temperature coefficent for all $V_{DD}$ values is 03 %/°C, all input rise and fall times= 20 ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time | | 5 | | 140 | 280 | ns |
| | | | 10 | | 65 | 130 | |
| | | | 15 | | 50 | 100 | |
| $t_{TLH}$ $t_{THL}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

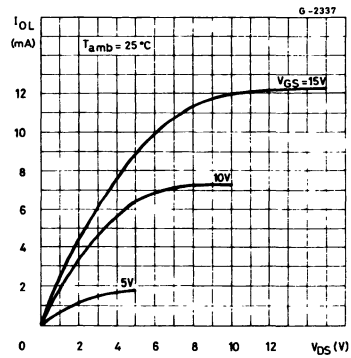
Minimum Output High (source) Current Characteristics.



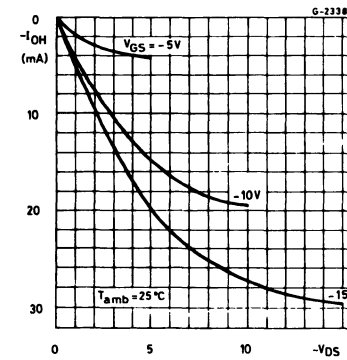

Typical Output Low (sink) Current.



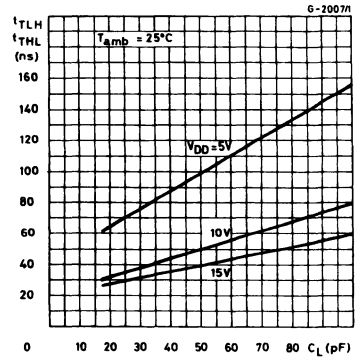

Minimum Output Low (sink) Current Characteristics.



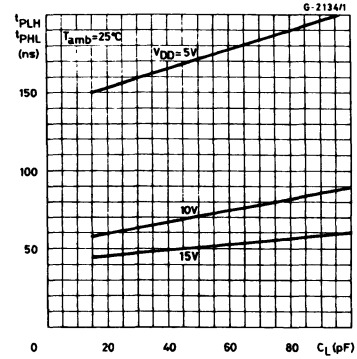

Typical Output High (source) Current Characteristics.



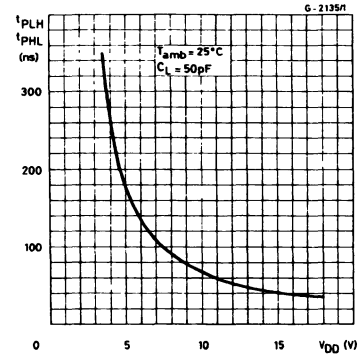
Typical Transition Time vs. Load Capacitance.



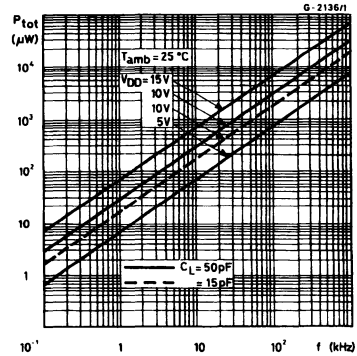

Typical Proagation Delay Time vs. Load Capacitance.




Typical Propagation Delay Time vs. Supply Voltage.

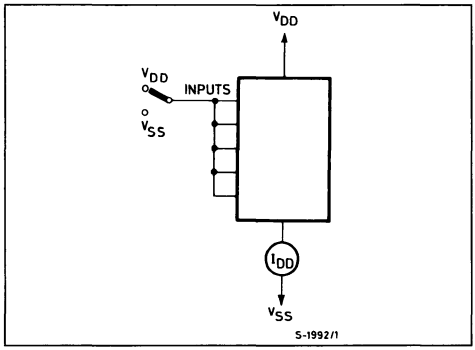



Typical Dynamic Power Dissipation vs. Input Frequency.

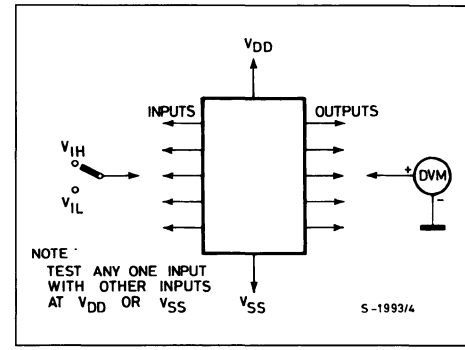


## TEST CIRCUIT

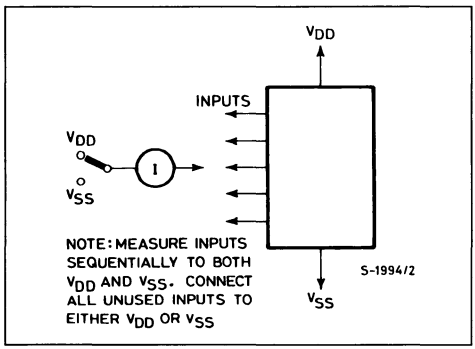
Quiescent Device Current.




Input Voltage.




Input Leakage Current.

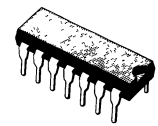


# HCC4071B/72B/75B
# HCF4071B/72B/75B

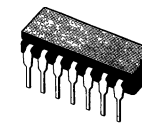
## OR GATE

**4071B - QUAD 2–INPUT OR GATE**
**4072B - QUAD 4–INPUT OR GATE**
**4075B - TRIPLE 3–INPUT OR GATE**

- MEDIUM-SPEED OPERATION $t_{PLH}$, $t_{PHL}$ = 60ns. (typ.) AT $V_{DD}$ = 10V
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC40XXBF HCF40XXBM1
HCF40XXBEY HCF40XXBC1

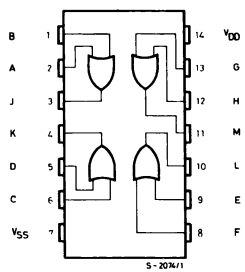
### DESCRIPTION

The **HCC4071B/4072B** and **4075B** (extended temperature range) and **HCF4071B/4072B** and **4075B** (intermediate temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and plastic micropackage.

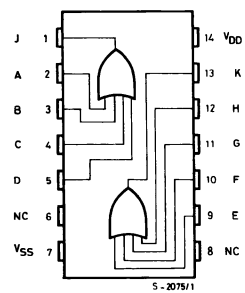
The **HCC/HCF4071B, 4072B** and **4075B** OR gates provide the system designer with direct implementation of the positive-logic OR function and supplement the existing family of COS/MOS gates.

### PIN CONNECTIONS

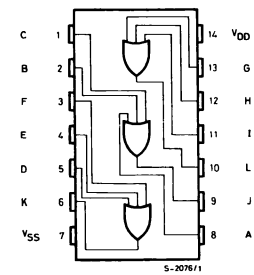
**4071B**




**4072B**




**4075B**



## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for Top = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

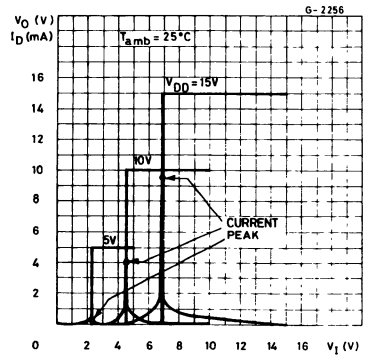
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability

* All voltage values are referred to $V_{SS}$ pin voltage.

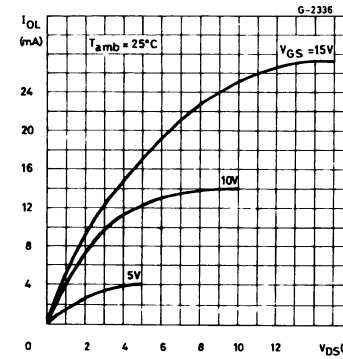
## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

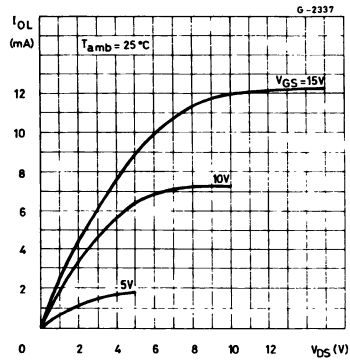
Typical Voltage and Current Transfer Characteristics.



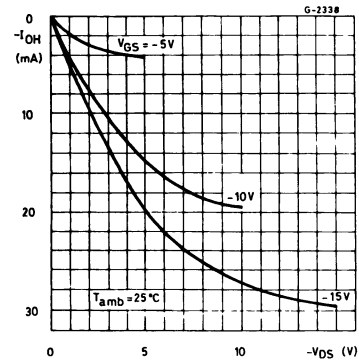

Typical Output Low (sink) Current Characterisitcs.



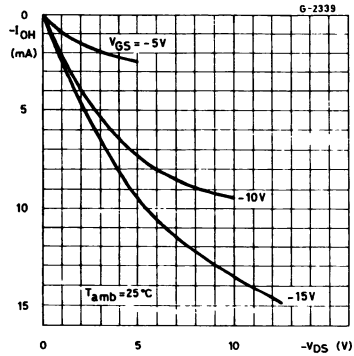
Minimum Output Low (sink) Current Characteristics.



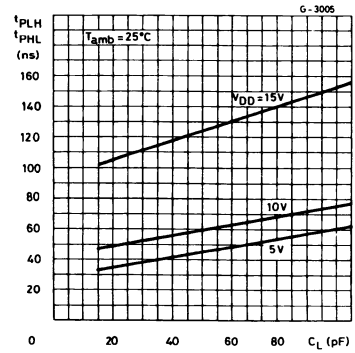

Typical Output High (source) Current Characteristics.



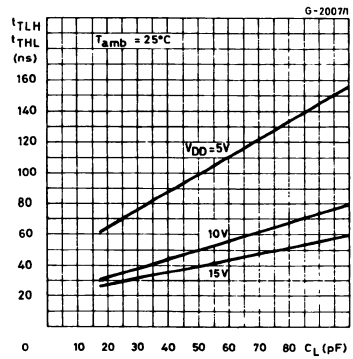

Minimum Output High (source) Current Characterisitcs.



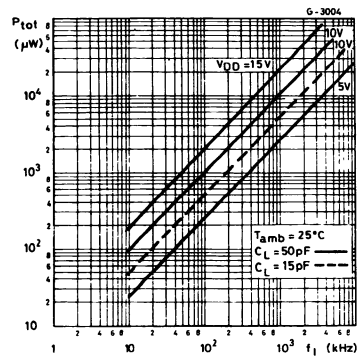

Typical Propagation Delay Time vs. Load Capacitance.




Typical Transition Time vs. Load Capacitance.

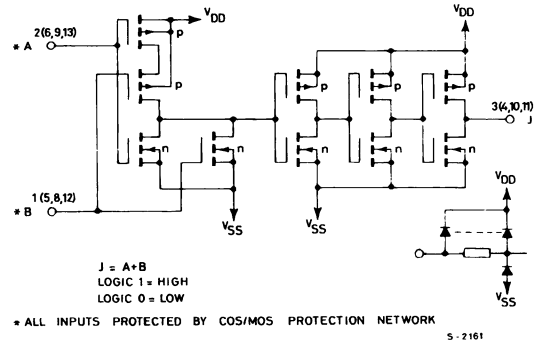



Typical Dynamic Power Dissipation vs. Frequency.

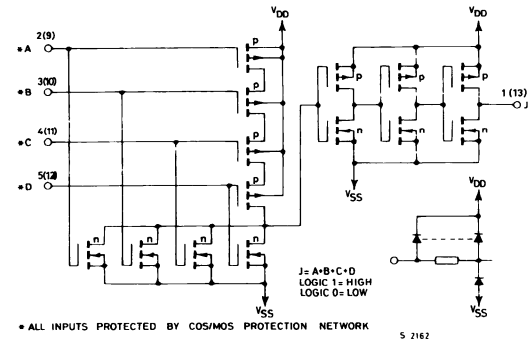


## SCHEMATIC DIAGRAMS

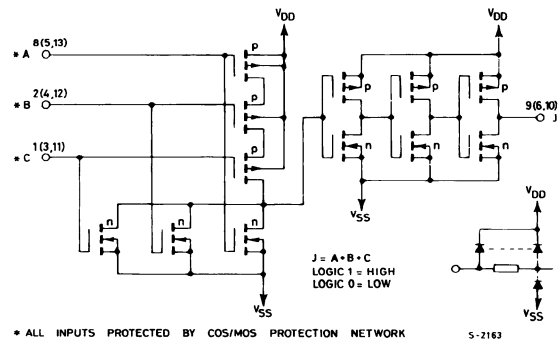
**4071B** – 1 of 4 identical OR gates




**4072B** – 1 of 2 identical OR gates




**4075B** – 1 of 3 identical OR gates



## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 0.25 | | 0.01 | 0.25 | | 7.5 | μA |
| | | | 0/10 | | | 10 | | 0.5 | | 0.01 | 0.5 | | 15 | |
| | | | 0/15 | | | 15 | | 1 | | 0.01 | 1 | | 30 | |
| | | | 0/20 | | | 20 | | 5 | | 0.02 | 5 | | 150 | |
| | | HCF Types | 0/ 5 | | | 5 | | 1 | | 0.01 | 1 | | 7.5 | |
| | | | 0/10 | | | 10 | | 2 | | 0.01 | 2 | | 15 | |
| | | | 0/15 | | | 15 | | 4 | | 0.01 | 4 | | 30 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9 95 | | |
| | | | 0/15 | | < 1 | 15 | 14 95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1 5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13 5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2 6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2 6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device

* $T_{High}$ = + 125°C for **HCC** device · + 85°C for **HCF** device

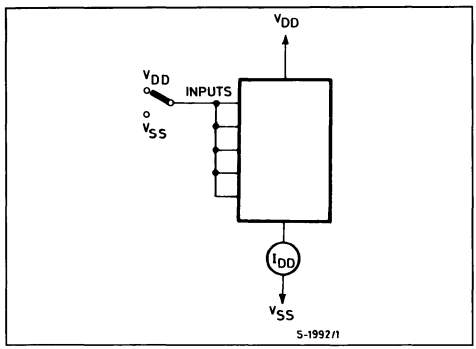
The Noise Margin for both "1" and "0" level is 1V min. with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2.5 V min with $V_{DD}$ = 15V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ = 0.3%/°C values , all input rise and fall time = 20ns)

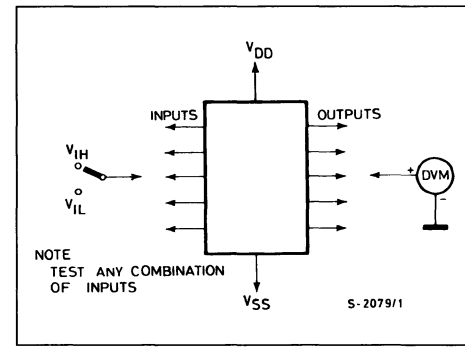
| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$ | Propagation Delay Time | | 5 | | 125 | 250 | ns |
| | | | 10 | | 60 | 120 | |
| | | | 15 | | 45 | 90 | |
| $t_{PLH}$ | Propagation Delay Time | | 5 | | 175 | 350 | ns |
| | | | 70 | | 50 | 140 | |
| | | | 15 | | 50 | 140 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

## TEST CIRCUITS

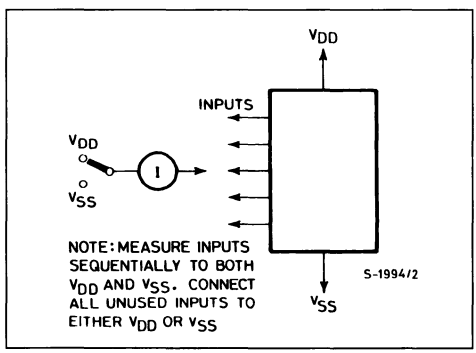
Quiescent Device Current.




Input Voltage.




Input Leakage Current.

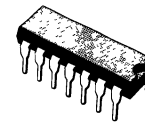


# HCC4073B/81B/82B
# HCF4073B/81B/82B

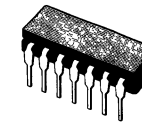
## AND GATES

**4073B TRIPLE 3–INPUT AND GATE**
**4081B QUAD 2–INPUT AND GATE**
**4082B DUAL 4–INPUT AND GATE**

- MEDIUM SPEED OPERATION – $t_{PLH}$ = 85ns (typ.) ; $t_{PHL}$ = 65ns (typ.) AT 10V
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

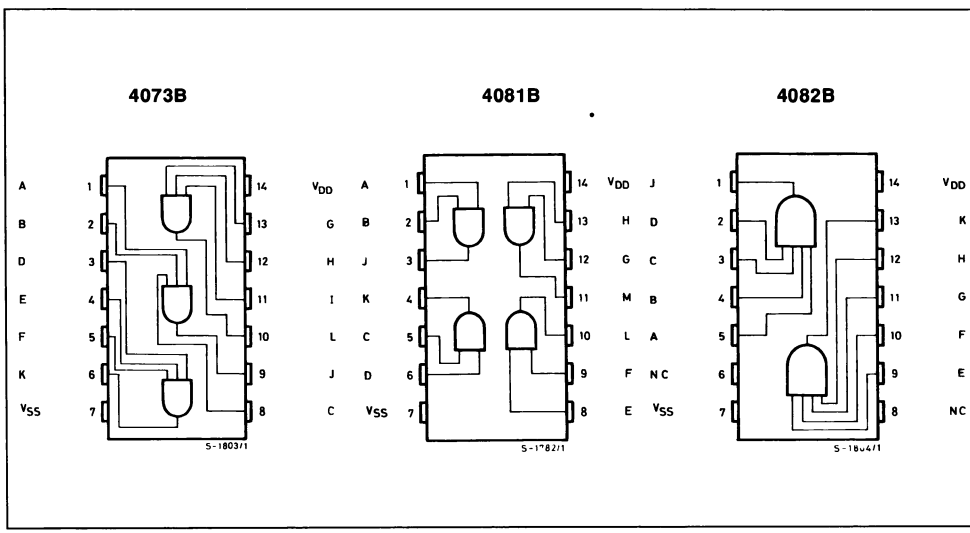
HCC40XXBF HCF40XXBM1
HCF40XXBEY HCF40XXBC1

### DESCRIPTION

The **HCC4073B**, **HCC4081B** and **HCC4082B** (extended temperature range) and the **HCF4073B**, **HCF4081B** and **HCF4082B** (intermediate temperature range) are monolithic integrated circuits available in 14-lead dual in-line plastic or ceramic package and plastic micro package.

The **HCC/HCF4073B**, **4081B** and **4082B** AND gates provide the system designer with direct implementation of the AND function and supplement the existing family of COS/MOS gates.

### CONNECTION DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{Low}$* | | 25 °C | | | $T_{High}$* | | |
| | | | | | | | Min. | Max. | Min. | Typ. | Max. | Min. | Max. | |
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 0.25 | | 0.01 | 0.25 | | 7.5 | μA |
| | | | 0/10 | | | 10 | | 0.5 | | 0.01 | 0.5 | | 15 | |
| | | | 0/15 | | | 15 | | 1 | | 0.01 | 1 | | 30 | |
| | | | 0/20 | | | 20 | | 5 | | 0 02 | 5 | | 150 | |
| | | HCF Types | 0/ 5 | | | 5 | | 1 | | 0.01 | 1 | | 7.5 | |
| | | | 0/10 | | | 10 | | 2 | | 0.01 | 2 | | 15 | |
| | | | 0/15 | | | 15 | | 4 | | 0.01 | 4 | | 30 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |

* $T_{Low}$ = − 55°C for **HCC** device − 40°C for **HCF** device

* $T_{High}$ = + 125°C for **HCC** device + 85°C for **HCF** device

The Noise Margin for both "1" and "0" level is . 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2 5V min. with $V_{DD}$ = 15V

## STATIC ELECTRICAL CHARACTERISTICS (continued)

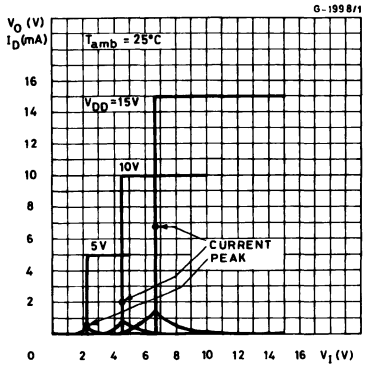
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25 °C Min. | 25 °C Typ. | 25 °C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is 1V min with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V

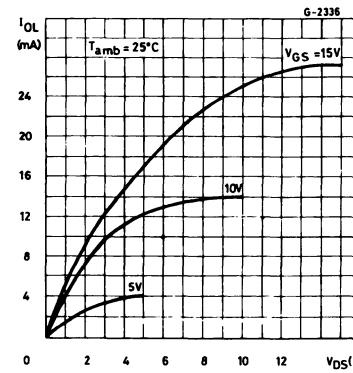
## DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb}$ = 25°C, $C_L$ = 50pF, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall times = 20ns, $R_L$ = 200kΩ)

| Symbol | Parameter | Test Conditions | $V_{DD}$ (V) | Value Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time | | 5 | | 125 | 250 | ns |
| | | | 10 | | 60 | 125 | |
| | | | 15 | | 45 | 90 | |
| $t_{TLH}$, $t_{THL}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

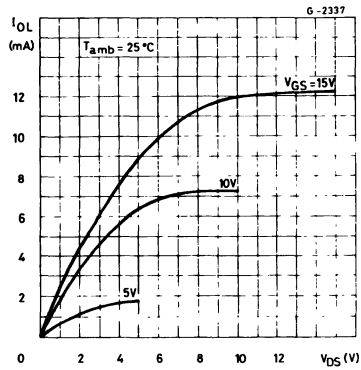
Typical Voltage and Current Transfer Characteristics.



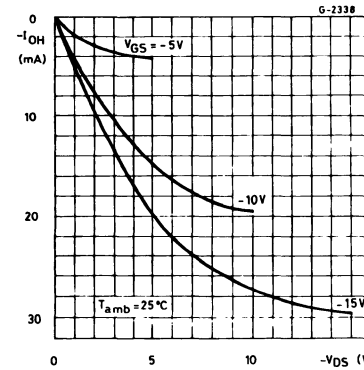

Typical Output Low (sink) Current .



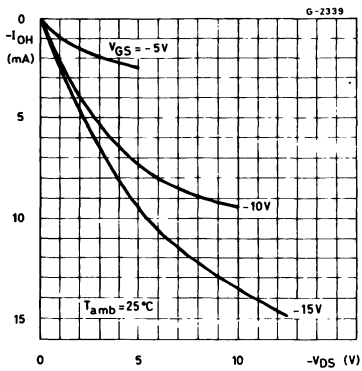

Minimum Output Low (sink) Current Characteristics.



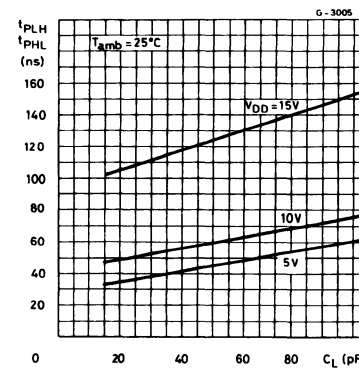

Typical Output High (source) Current Characteristics.



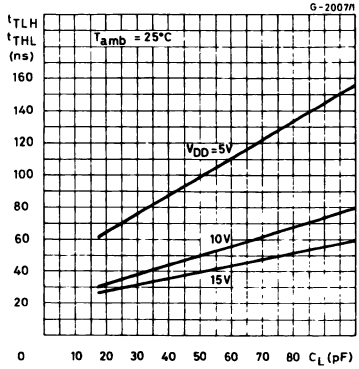

Minimum Output High (source) Current Characteristics.



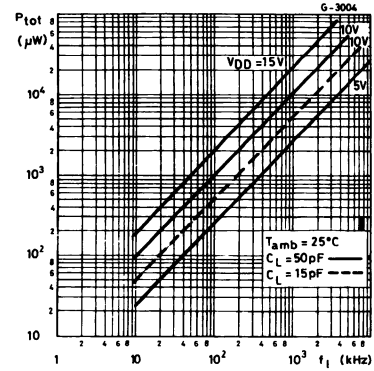

Typical Propagation Delay Time vs. Load Capacitance.



Typical Transition Time vs. Load Capacitance.

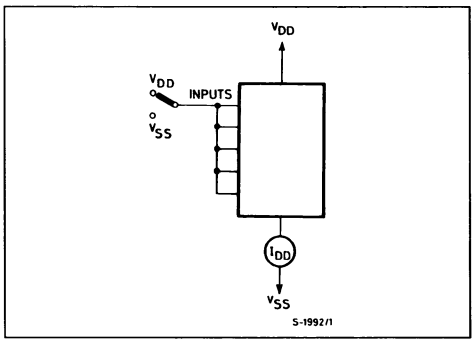



Typical Dynamic Power Dissipation per Gate vs. Frequency.

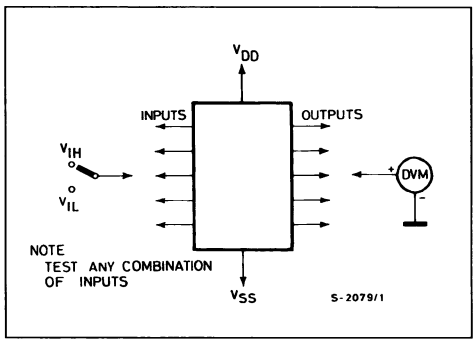



## TEST CIRCUITS

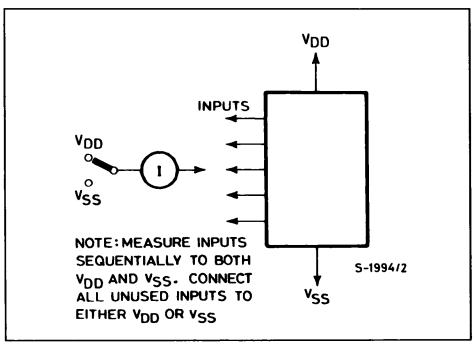
Quiescent Device Current.




Input Voltage.




Input Leakage Current.

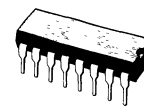


SGS-THOMSON MICROELECTRONICS

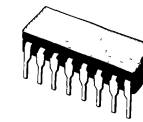
# HCC4076B
# HCF4076B

## 4 BIT D TYPE REGISTERS

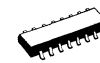
- THREE STATE OUTPUTS
- INPUT DISABLE WITHOUT GATING THE CLOCK
- GATED OUTPUT CONTROL LINES FOR ENABLING OR DISABLING THE OUTPUTS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N. 13A, " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES "



**EY**
(Plastic Package)



**F**
(Ceramic Package)



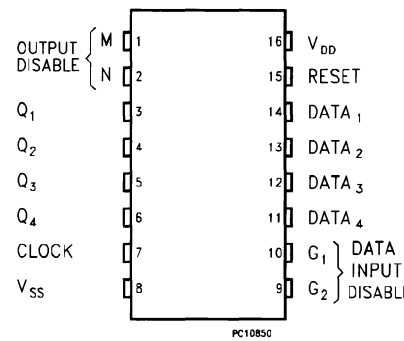
**M1**
(Micro Package)

**C1**
(Chip Carrier)

**ORDER CODES :**

| | |
|---|---|
| HCC4076BF | HCF4076BM1 |
| HCF4076BEY | HCF4076BC1 |

**PIN CONNECTIONS**

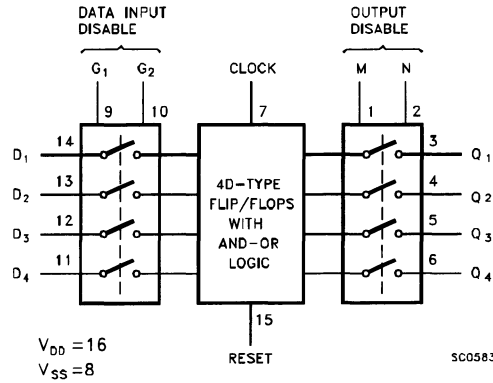



### DESCRIPTION

The **HCC4076B** (extended temperature range) and **HCC4076B** (intermediate temperature range) are monolithic integrated circuit, available in 16 lead dual in line plastic or ceramic package and plastic micropackage.

The **HCC/HCF4076B** types are four-bit registers consisting of D-type flip-flops that feature three-state outputs. Data Disable inputs are provided to control the entry of data into the flip-flops. When both Data Disable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the click input. Output Disable inputs are also provided. When the Output Disable inputs are both low, the normal logic states of the four outputs are available to the load. The outputs are disabled independently of the clock by a high logic level at either Output Disable input, and present a high impedance.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ * | Supply Voltage: **HCC** Types<br>**HCF** Types | -0.5 to +20<br>-0.5 to +18 | V<br>V |
| $V_I$ | Input Voltage | -0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for Top = Full Package Temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |

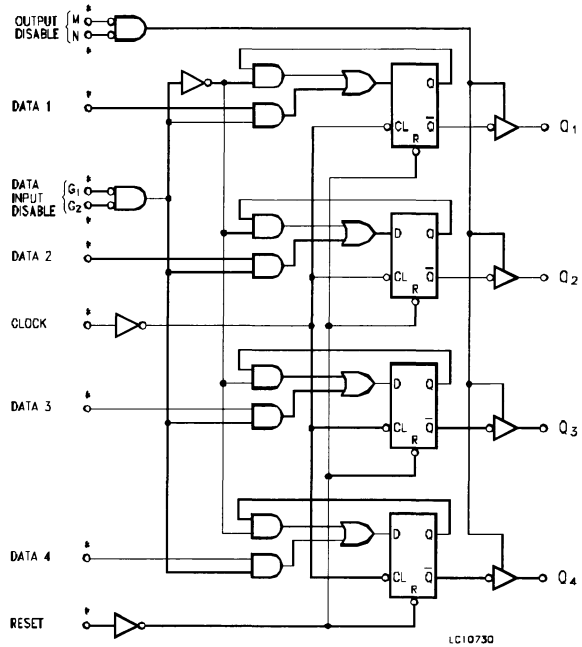
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage: **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |

## LOGIC DIAGRAM




* ALL INPUTS PROTECTED BY COS/MOS PROTECTION NETWORK

## TRUTH TABLE

| RESET | CLOCK | DATA INPUT DISABLE | | DATA D | NEXT STATE OUTPUT G | |
|---|---|---|---|---|---|---|
| | | G1 | G2 | | | |
| 1 | X | X | X | X | 0 | |
| 0 | 0 | X | X | X | Q | NC |
| 0 | ⎍ | 1 | X | X | Q | NC |
| 0 | ⎍ | X | 1 | X | Q | NC |
| 0 | ⎍ | 0 | 0 | 1 | 1 | |
| 0 | ⎍ | 0 | 0 | 0 | 0 | |
| 0 | 1 | X | X | X | Q | NC |
| 0 | ⎎ | X | X | X | Q | NC |

When either Output Disable M or N is high, the outputs are disablesd (high impedance state). however sequential operation of the flip-flop is not affected.
1 = High Level, 0 = Low Level, X = Don't Care, NC = No Change

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditios $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{LOW}$ * Min. | $T_{LOW}$ * Max. | 25 °C Min. | 25 °C Typ. | 25 °C Max. | $T_{HIGH}$ * Min. | $T_{HIGH}$ * Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9 95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14 95 | | | 14 95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0 05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0 05 | | | 0 05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0 05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0 5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13 5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4 5/0 5 | < 1 | 5 | | 1 5 | | | 1 5 | | 1 5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/5 | 2.5 | | 5 | -2 | | -1 6 | -3.2 | | -1 15 | | mA |
| | | | 0/5 | 4.6 | | 5 | -0.64 | | -0.51 | -1 | | -0.36 | | |
| | | | 0/10 | 9 5 | | 10 | -1 6 | | -1.3 | -2 6 | | -0 9 | | |
| | | | 0/15 | 13 5 | | 15 | -4 2 | | -3 4 | -6 8 | | -2.4 | | |
| | | HCF Types | 0/5 | 2 5 | | 5 | -1.53 | | -1 36 | -3 2 | | -1.1 | | |
| | | | 0/5 | 4.6 | | 5 | -0 52 | | -0.44 | -1 | | -0 36 | | |
| | | | 0/10 | 9 5 | | 10 | -1.3 | | -1.1 | -2 6 | | -0 9 | | |
| | | | 0/15 | 13.5 | | 15 | -3 6 | | -3 0 | -6 8 | | -2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/5 | 0.4 | | 5 | 0 64 | | 0 51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0 5 | | 10 | 1 6 | | 1 3 | 2 6 | | 0 9 | | |
| | | | 0/15 | 1 5 | | 15 | 4 2 | | 3.4 | 6.8 | | 2 4 | | |
| | | HCF Types | 0/5 | 0 4 | | 5 | 0.61 | | 0 44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1 | | 1 1 | 2 6 | | 0.9 | | |
| | | | 0/15 | 1 5 | | 15 | 3 6 | | 3 0 | 6 8 | | 2 4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | | 0/18 | Any Input | | 18 | | ±0.1 | | $±10^{-5}$ | ±0.1 | | ±1 | μA |
| | | | 0/15 | | | 15 | | ±0 3 | | $±10^{-5}$ | ±0 3 | | ±1 | μA |
| $I_{OH}$, $I_{OL}$ | Input Leakage Current | HCC Types | 0/18 | 0/18 | | 18 | | ±0.4 | | $±10^{-4}$ | ±0.4 | | ±12 | μA |
| | | HCF Types | 0/15 | 0/15 | | 15 | | ±1.0 | | $±10^{-4}$ | ±1.0 | | ±7.5 | μA |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{LOW}$ = -55 °C for **HCC** device -40 °C for **HCF** device

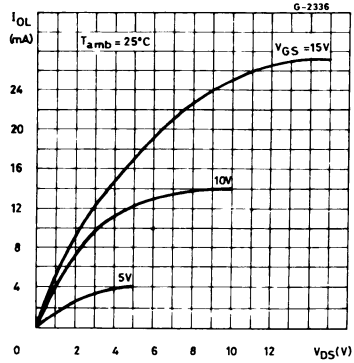
* $T_{HIGH}$ = +125 °C for **HCC** device +85 °C for **HCF** device

The Noise Margin for both "1" and "0" level is. 1V min with $V_{DD}$ = 5 V, 2 V min with $V_{DD}$ = 10 V, 2 5 V min. with $V_{DD}$ = 15 V

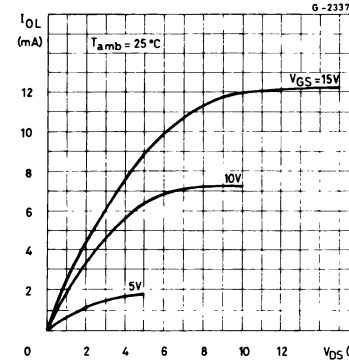
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 KΩ, typical temperature coefficent for all $V_{DD}$ values is 03 %/°C, all input rise and fall times= 20 ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (Clock to Q Output) | | 5 | | 300 | 600 | ns |
| | | | 10 | | 125 | 250 | |
| | | | 15 | | 90 | 180 | |
| $t_{PHL}$(R) | Propagation Delay Time (Reset) | | 5 | | 230 | 460 | ns |
| | | | 10 | | 100 | 200 | |
| | | | 15 | | 75 | 150 | |
| $t_{P(1-H)}$ $t_{P(0-H)}$ | 3-State Output 1 or 0 to High Impedance | $R_L$ = 1KΩ | 5 | | 150 | 300 | ns |
| | | | 10 | | 75 | 150 | |
| | | | 15 | | 60 | 120 | |
| $t_{P(H-1)}$ $t_{P(L-1)}$ | 3-State High Impedance to 1 or 0 Output | $R_L$ = 1KΩ | 5 | | 150 | 300 | ns |
| | | | 10 | | 75 | 150 | |
| | | | 15 | | 60 | 120 | |
| $t_W$ | Clock Pulse Width | | 5 | 200 | 100 | | ns |
| | | | 10 | 100 | 50 | | |
| | | | 15 | 80 | 40 | | |
| $t_W$ | Reset Pulse Width | | 5 | 120 | 60 | | ns |
| | | | 10 | 50 | 25 | | |
| | | | 15 | 40 | 20 | | |
| $t_{setup}$ | Data Setup Time | | 5 | 200 | 100 | | ns |
| | | | 10 | 80 | 40 | | |
| | | | 15 | 60 | 30 | | |
| $t_{setup}$ | Data Input Disable Setup Time | | 5 | 180 | 90 | | ns |
| | | | 10 | 100 | 50 | | |
| | | | 15 | 70 | 35 | | |
| $f_{max}$ | Maximum Clock Frequency | | 5 | 3 | 6 | | MHz |
| | | | 10 | 6 | 12 | | |
| | | | 15 | 8 | 16 | | |
| $t_r$, $t_f$ | Clock Input Rise or Fall Time | | 5 | 15 | | | µs |
| | | | 10 | 5 | | | |
| | | | 15 | 5 | | | |

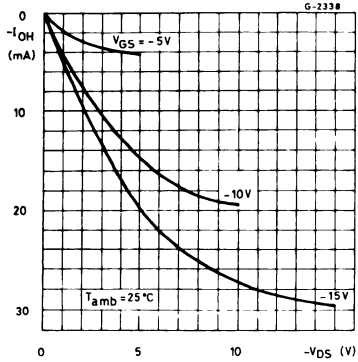
Typical Output Low (sink) Current Characteristics



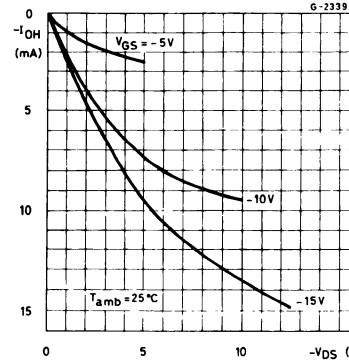

Minimum Output Low (sink) Current Characteristics



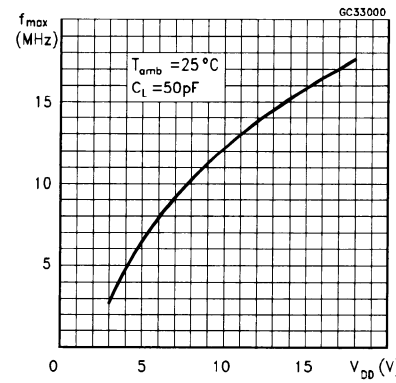

Typical Output High (source) Current Characteristics



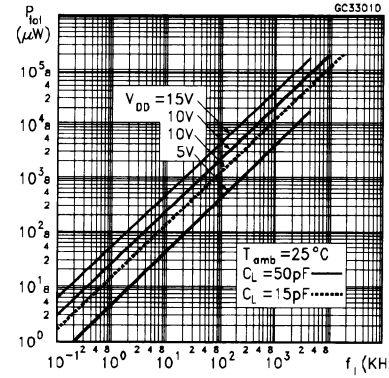

Minimum Output High (source) Current Characteristics



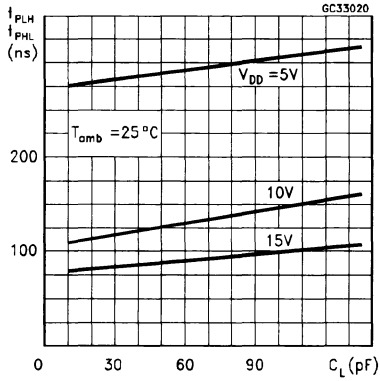

Typical Maximum Clock Input Frequency vs Supply Voltage



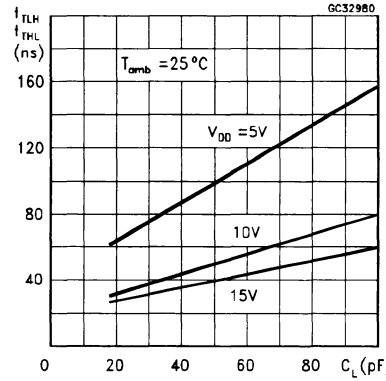

Typical Dynamic Power Dissipation vs Frequency



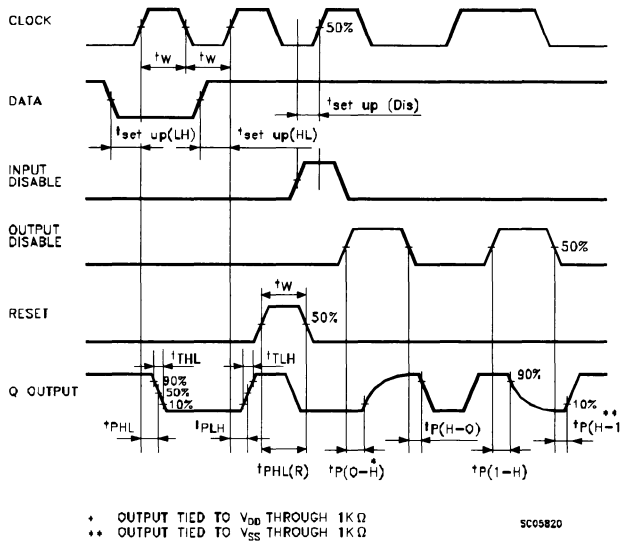
Typical Propagation Delay Time vs Capacitance




Typical Transition Time vs Load Capacitance

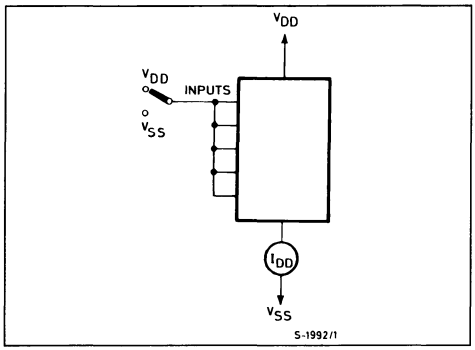



## WAVEFORMS

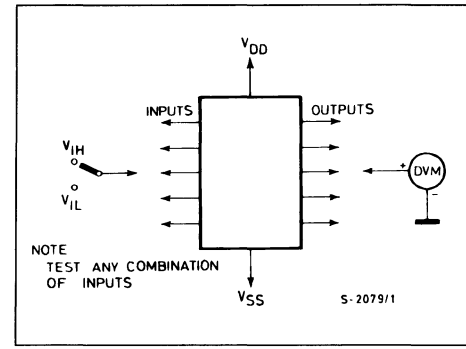


## TEST CIRCUITS

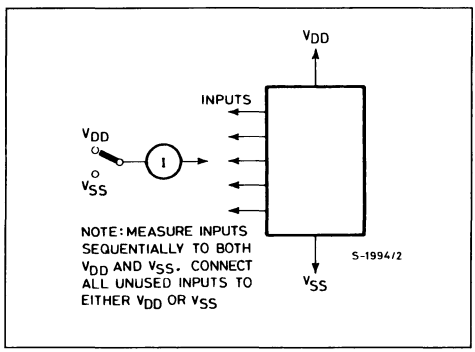
Quiescent Device Current.




Noise Immunity.



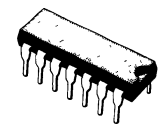

Input Leakage Current.



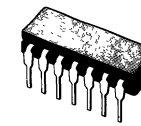
# HCC/HCF4078B

## 8-INPUT NOR/OR GATE

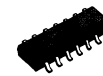
- MEDIUM-SPEED OPERATION $t_{PHL}$, $t_{PLH}$ = 75ns (TYP.) AT $V_{DD}$ = 10V
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)



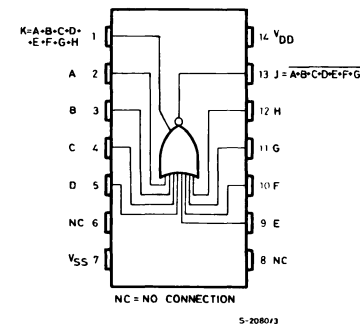
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4078BF HCF4078BM1
HCF4078BEY HCF4078BC1

**PIN CONNECTIONS**




### DESCRIPTION

The **HCC4078B** (extended temperature range) and **HCF4078B** (intermediate temperature range) are monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package, plastic micropackage.

The **HCC/HCF4078B** NOR/OR Gate provides the system designer with direct implementation of the positive-logic-8-input NOR and OR function and supplements the existing family of COS/MOS gates.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

**STATIC ELECTRICAL CHARACTERISTICS** (over recommended operating conditions)

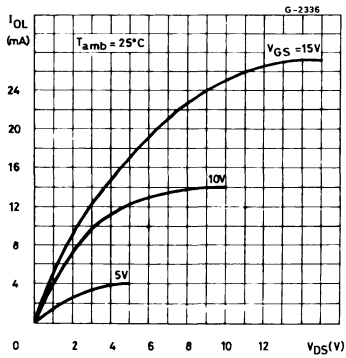
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 0.25 | | 0.01 | 0.25 | | 7.5 | μA |
| | | | 0/10 | | | 10 | | 0.5 | | 0.01 | 0.5 | | 15 | |
| | | | 0/15 | | | 15 | | 1 | | 0.01 | 1 | | 30 | |
| | | | 0/20 | | | 20 | | 5 | | 0.02 | 5 | | 150 | |
| | | HCF Types | 0/ 5 | | | 5 | | 1 | | 0.01 | 1 | | 7.5 | |
| | | | 0/10 | | | 10 | | 2 | | 0.01 | 2 | | 15 | |
| | | | 0/15 | | | 15 | | 4 | | 0.01 | 4 | | 30 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5 V min. with $V_{DD}$ = 15V.

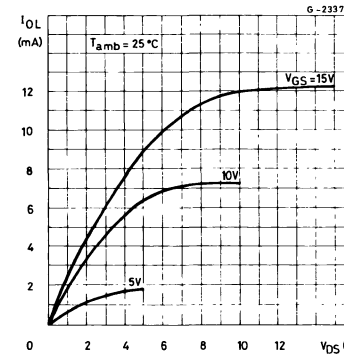
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall time = 20ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time | | 5 | | 150 | 300 | ns |
| | | | 10 | | 75 | 150 | |
| | | | 15 | | 55 | 110 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

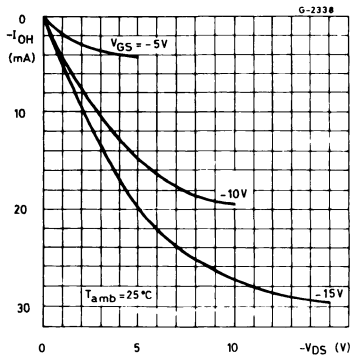
Typical Output Low (sink) Current Characteristics.



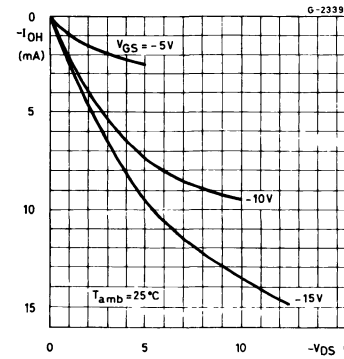

Minimum Output Low (sink) Current Characteristics.



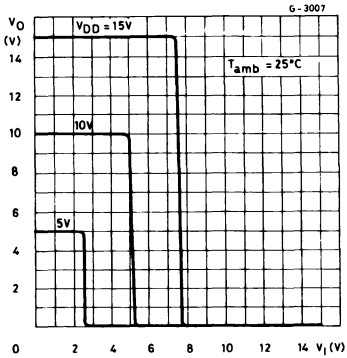

Typical Output High (source) Current Characteristics.



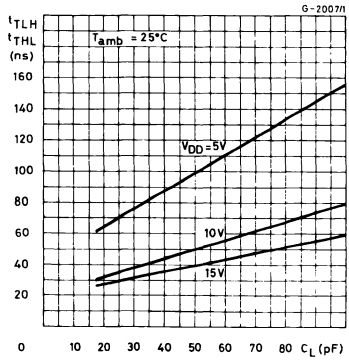

Minimum Output High (source) Current Characteristics.



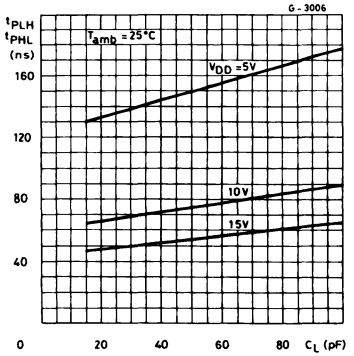
Typical Voltage Transfer Characteristics (NOR output).



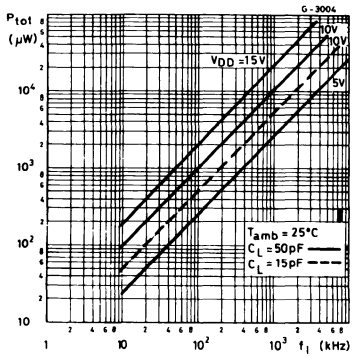

Typical Transition Time vs. Load Capacitance.




Typical Propagation Delay Time vs. Load Capacitance.

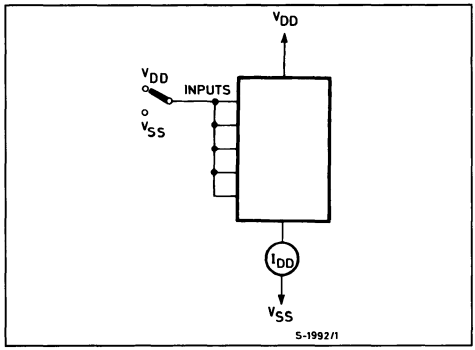



Typical Power Dissipation vs. Frequency.

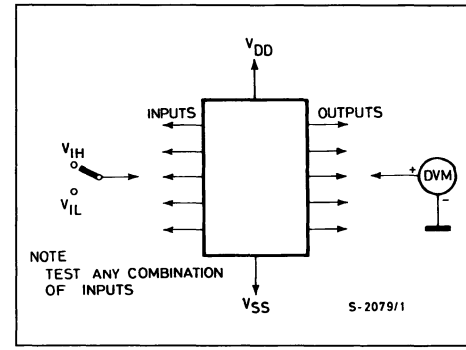


## TEST CIRCUITS

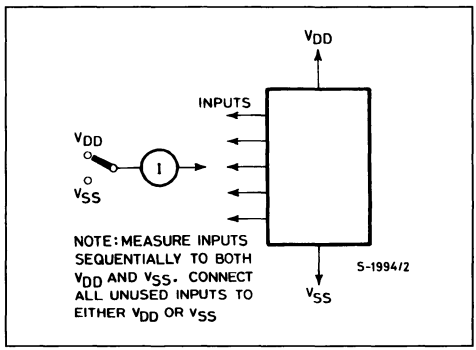
Quiescent Device Current.



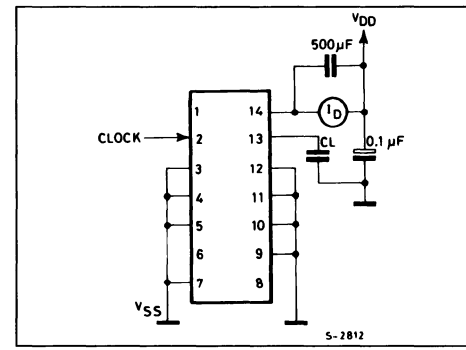

Input Voltage.




Input Current.

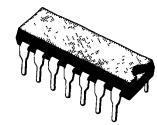



Dynamic Power Dissipation.

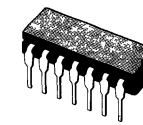


# DUAL 2-WIDE 2-INPUT AND-OR-INVERTER GATE

- MEDIUM-SPEED OPERATION – $t_{PHL}$ = 90ns ; $t_{PLH}$ = 125ns (TYP.) AT 10V
- INDIVIDUAL INHIBIT CONTROLS
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

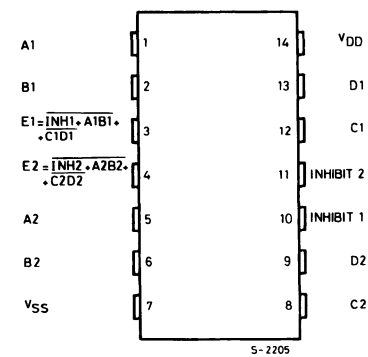
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES** :

HCC4085BF HCF4085BM1
HCF4085BEY HCF4085BC1

**PIN CONNECTIONS**

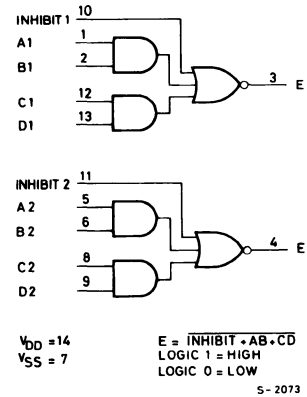



## DESCRIPTION

The **HCC4085B** (extended temperature range) and **HCF4085B** (intermediate temperature range) are monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package and plastic micropackage.

The **HCC/HCF4085B** contains a pair of AND-OR-INVERT gates, each consisting of two 2-input AND gates driving a 3-input NOR gate. Individual inhibit controls are provided for both A-O-I gates.

## LOGIC DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

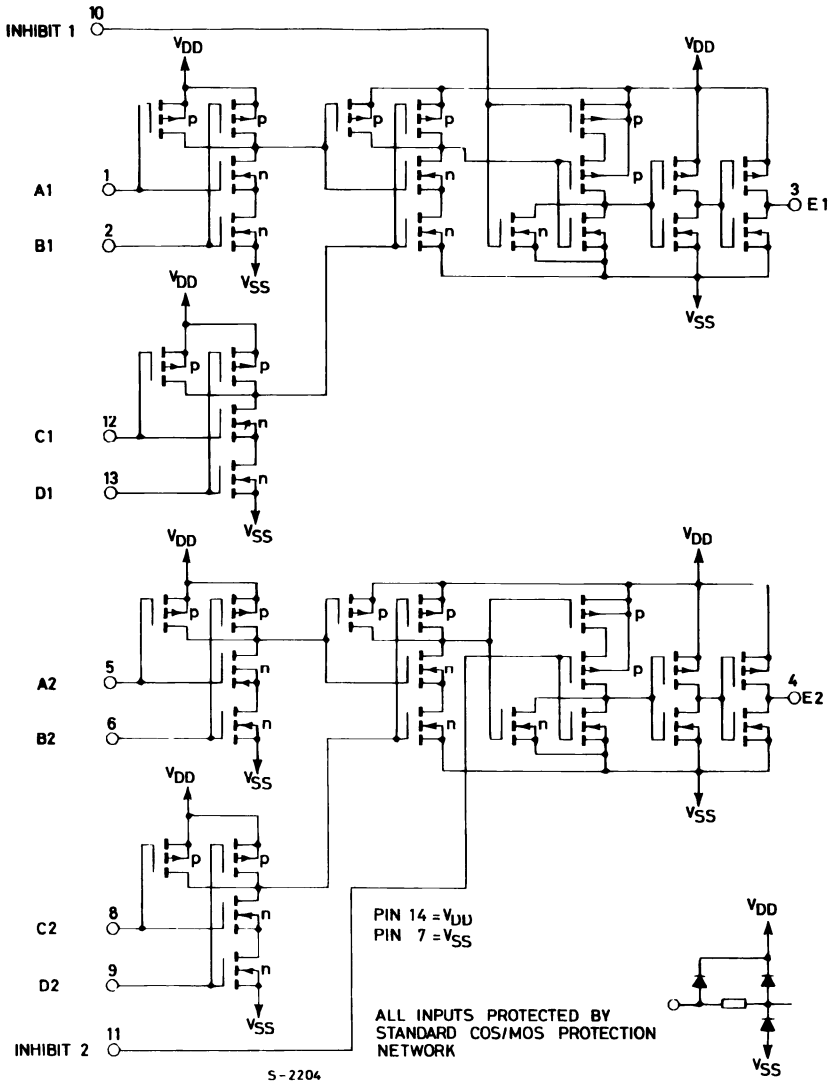
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at those or any other conditions aboves those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability

* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## SCHEMATIC DIAGRAM



## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

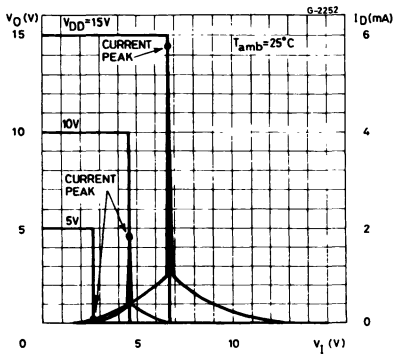
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 1 | | 0.02 | 1 | | 30 | μA |
| | | | 0/10 | | | 10 | | 2 | | 0.02 | 2 | | 60 | |
| | | | 0/15 | | | 15 | | 4 | | 0.02 | 4 | | 120 | |
| | | | 0/20 | | | 20 | | 20 | | 0.04 | 20 | | 600 | |
| | | HCF Types | 0/ 5 | | | 5 | | 4 | | 0.02 | 4 | | 30 | |
| | | | 0/10 | | | 10 | | 8 | | 0.02 | 8 | | 60 | |
| | | | 0/15 | | | 15 | | 16 | | 0.02 | 16 | | 120 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0 05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3 5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0 51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

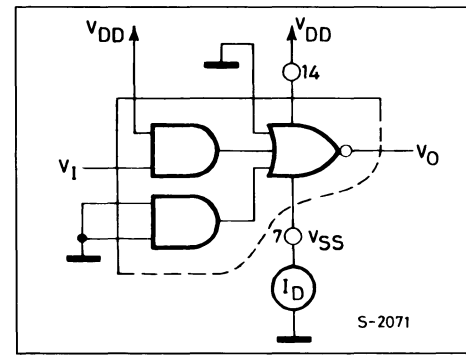
* $T_{Low}$ = − 55°C for **HCC** device · − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device . + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is 1V min with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2.5min with $V_{DD}$ = 15V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ = 0.3%/°C values, all input rise and fall time = 20ns)

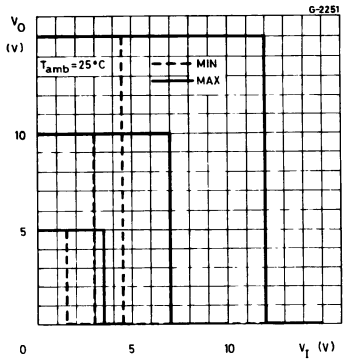
| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$ | Propagation Delay Time (data) | | 5 | | 225 | 450 | ns |
| | | | 10 | | 90 | 180 | |
| | | | 15 | | 65 | 130 | |
| $t_{PLH}$ | Propagation Delay Time (data) | | 5 | | 310 | 620 | |
| | | | 10 | | 125 | 250 | |
| | | | 15 | | 90 | 180 | |
| $t_{PHL}$ | Propagation Delay Time (inhibit) | | 5 | | 150 | 300 | ns |
| | | | 10 | | 60 | 120 | |
| | | | 15 | | 40 | 80 | |
| $t_{PLH}$ | Propagation Delay Time (inhibit) | | 5 | | 250 | 500 | |
| | | | 10 | | 100 | 200 | |
| | | | 15 | | 70 | 140 | |
| $t_{TLH}$, $t_{THL}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

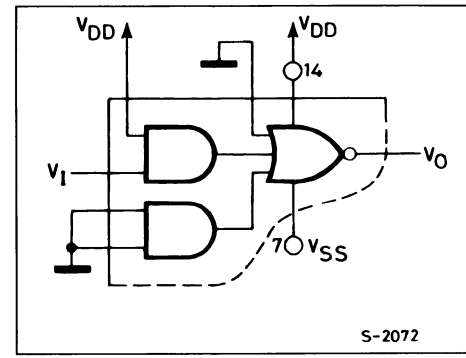
Typical Voltage and Current Transfer Characteristics with Test Circuit.



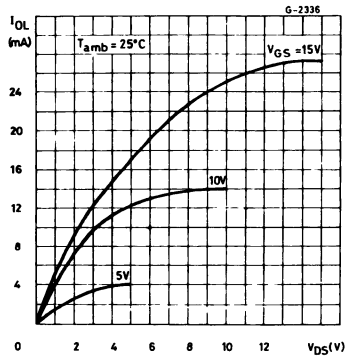



Minimum and Maximum Voltage Transfer Characteristics with Test Circuit.

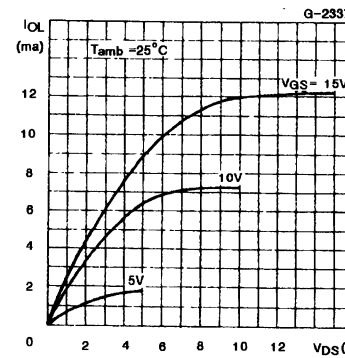


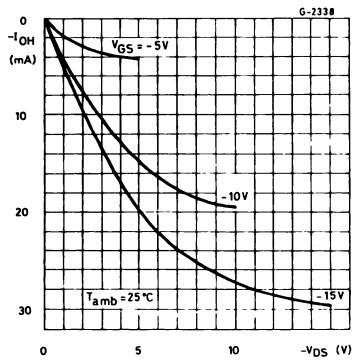

Typical Output Low (sink) Current Characteristics.



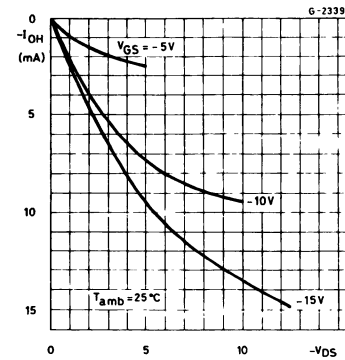

Minimum Output Low (sink) Current Characteristics.



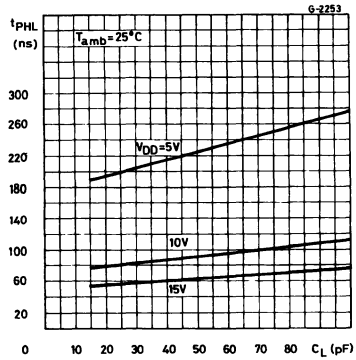

Typical Ouput High (source) Current Characteristics.



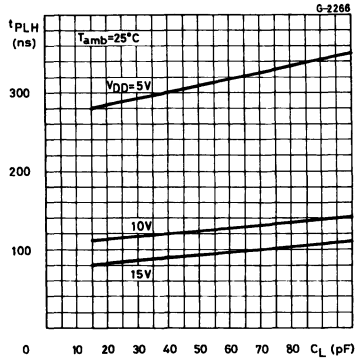

Minimum Output High (source) Current Characteristics.



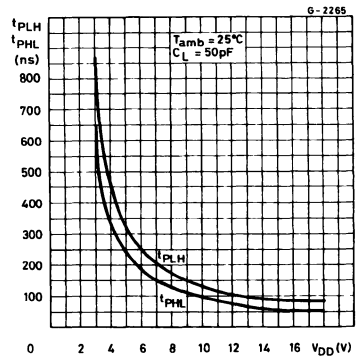
Typical Data High-to-low Level Propagation Delay Time vs. Load Capacitance.



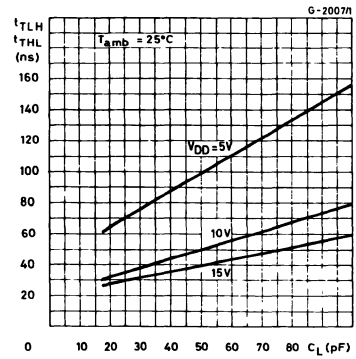

Typical Data Low-to-high Level Propagation Delay Time vs. Load Capacitance.



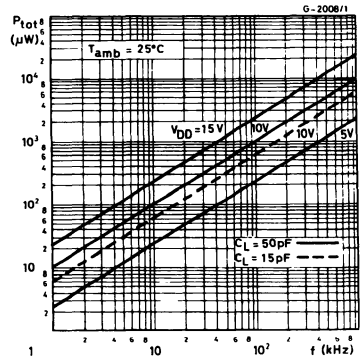

Typical Data Propagation Delay Time vs. Supply Voltage.




Typical Transition Time vs. Load Capacitance.

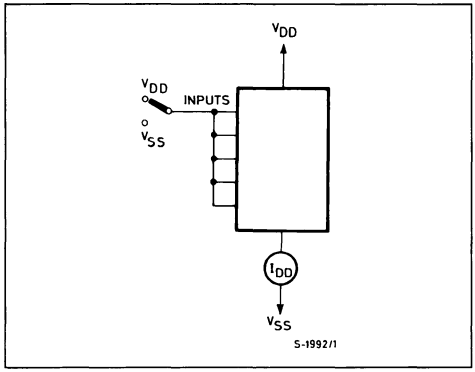



Typical Power Dissipation vs. Frequency.

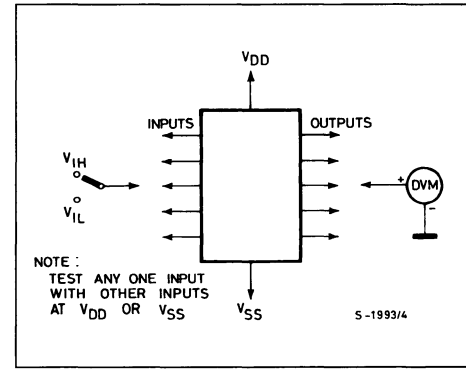


## TEST CIRCUITS

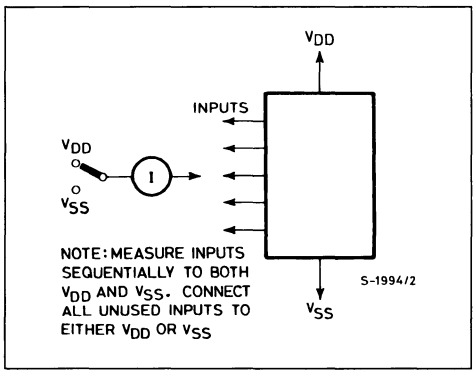
Quiescent Device Current.




Input Voltage.




Input Current.

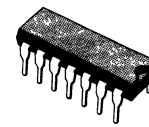


SGS-THOMSON MICROELECTRONICS

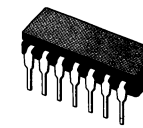
# HCC4086B
# HCF4086B

## EXPANDABLE 4 WIDE 2 INPUT AND OR INVERT GATE

- MEDIUM SPEED OPERATION: $t_{PHL}$ = 90ns; $t_{PLH}$ = 140ns (TYP.) AT 10V
- INHIBIT AND ENABLE INPUTS
- BUFFERED OUTPUTS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHACACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25oC FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N. 13A, " STANDARD SPECIFICATIONS FOR DESCRIPTION OF ' B ' SERIES CMOS DEVICES "



**EY**
(Plastic Package)



**F**
(Ceramic Package)

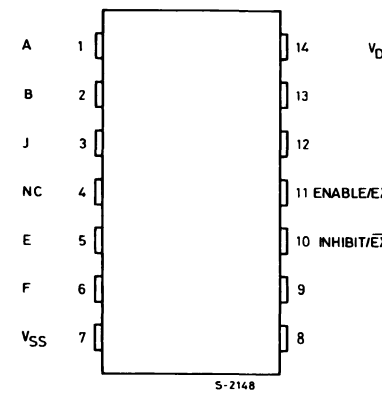
**M1**
(Micro Package)

**C1**
(Chip Carrier)

**ORDER CODES :**

| | |
|---|---|
| HCC4086BF | HCF4086BM1 |
| HCF4086BEY | HCF4086BC1 |

**PIN CONNECTIONS**

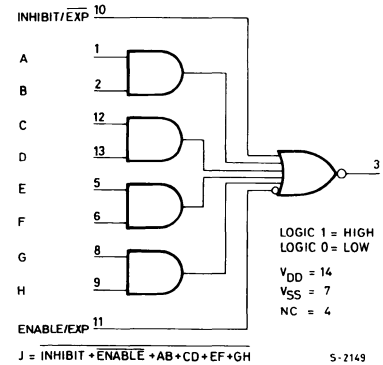



### DESCRIPTION

The **HCC4086B** (extended temperature range) and **HCF4086B** (intermediate temperature range) are monolithic integrated circuit, available in 14 lead dual in line plastic or ceramic package and plastic micropackage.

The **HCC/HCF4086B** contains one 4 wide 2 input AND OR INVERT gate with an INHIBIT/EXP input and an ENABLE/EXP input. For a 4 wide A-O-I function INHIBIT/EXP is tied to VSS and ENABLE/EXP to VDD. See application and its associated explanation for applications where a capability greater than 4 wide is required.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ * | Supply Voltage: **HCC** Types<br>**HCF** Types | -0.5 to +20<br>-0.5 to +18 | V<br>V |
| $V_I$ | Input Voltage | -0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for Top = Full Package Temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |

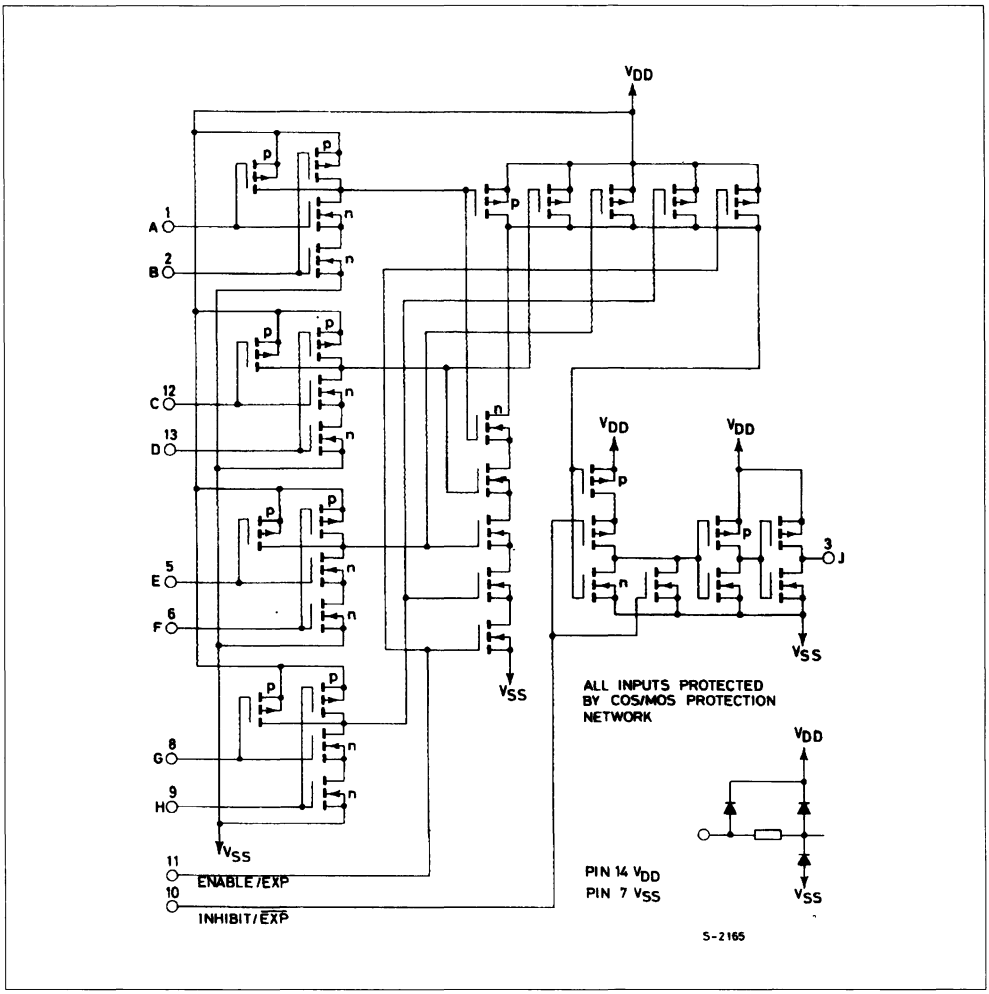
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to $V_{SS}$ pin voltage

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage: **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |

## SCHEMATIC DIAGRAM



## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditios | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{LOW}$ * Min. | $T_{LOW}$ * Max. | 25 °C Min. | 25 °C Typ. | 25 °C Max. | $T_{HIGH}$ * Min. | $T_{HIGH}$ * Max. | |
| $I_L$ | Quiescent Current | HCC Types | 0/5 | | | 5 | | 1 | | 0.02 | 1 | | 30 | μA |
| | | | 0/10 | | | 10 | | 2 | | 0.02 | 2 | | 60 | |
| | | | 0/15 | | | 15 | | 4 | | 0.02 | 4 | | 120 | |
| | | | 0/20 | | | 20 | | 20 | | 0.04 | 20 | | 600 | |
| | | HCF Types | 0/5 | | | 5 | | 4 | | 0.02 | 4 | | 30 | |
| | | | 0/10 | | | 10 | | 8 | | 0.02 | 8 | | 60 | |
| | | | 0/15 | | | 15 | | 16 | | 0.02 | 16 | | 120 | |
| $V_{OH}$ | Output High Voltage | | 0/5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9 95 | | | 9 95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0 05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0 05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3 5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/5 | 2.5 | | 5 | -2 | | -1.6 | -3 2 | | -1.15 | | mA |
| | | | 0/5 | 4.6 | | 5 | -0.64 | | -0.51 | -1 | | -0.36 | | |
| | | | 0/10 | 9 5 | | 10 | -1.6 | | -1 3 | -2.6 | | -0.9 | | |
| | | | 0/15 | 13.5 | | 15 | -4.2 | | -3.4 | -6.8 | | -2 4 | | |
| | | HCF Types | 0/5 | 2.5 | | 5 | -1 53 | | -1.36 | -3.2 | | -1.1 | | |
| | | | 0/5 | 4.6 | | 5 | -0 52 | | -0.44 | -1 | | -0 36 | | |
| | | | 0/10 | 9.5 | | 10 | -1.3 | | -1.1 | -2 6 | | -0 9 | | |
| | | | 0/15 | 13.5 | | 15 | -3.6 | | -3.0 | -6.8 | | -2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/5 | 0.4 | | 5 | 0 52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1 5 | | 15 | 3.6 | | 3 0 | 6 8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | | 0/18 | Any Input | | 18 | | ±0.1 | | $\pm 10^{-5}$ | ±0.1 | | ±1 | μA |
| | | | 0/15 | | | 15 | | ±0.3 | | $\pm 10^{-5}$ | ±0.3 | | ±1 | μA |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{LOW}$ = -55 °C for **HCC** device: -40 °C for **HCF** device.

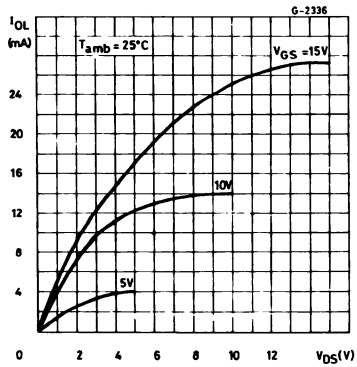
* $T_{HIGH}$ = +125 °C for **HCC** device +85 °C for **HCF** device

The Noise Margin for both "1" and "0" level is 1V min. with $V_{DD}$ = 5 V, 2 V min with $V_{DD}$ = 10 V, 2.5 V min. with $V_{DD}$ = 15 V

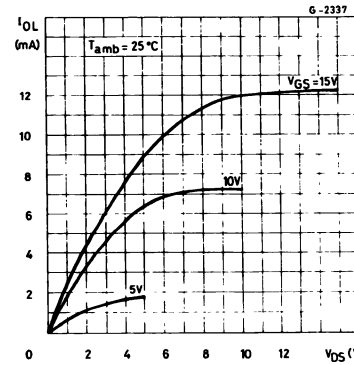
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 KΩ, typical temperature coefficent for all $V_{DD}$ values is 03 %/°C, all input rise and fall times= 20 ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$ | Propagation Delay Time (Data) | | 5 | | 225 | 450 | ns |
| | | | 10 | | 90 | 180 | |
| | | | 15 | | 60 | 120 | |
| $t_{PLH}$ | Propagation Delay Time (Data) | | 5 | | 310 | 620 | ns |
| | | | 10 | | 125 | 250 | |
| | | | 15 | | 90 | 180 | |
| $t_{PHL}$ | Propagation Delay Time (Inhibit) | | 5 | | 150 | 300 | ns |
| | | | 10 | | 60 | 120 | |
| | | | 15 | | 40 | 80 | |
| $t_{PLH}$ | Propagation Delay Time (Inhibit) | | 5 | | 250 | 500 | ns |
| | | | 10 | | 100 | 200 | |
| | | | 15 | | 70 | 140 | |
| $t_{TLH}$ $t_{THL}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

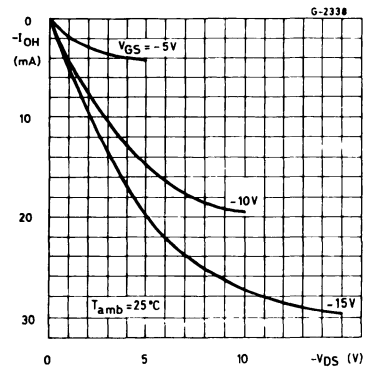
Typical Output Low (sink) Current Characteristics



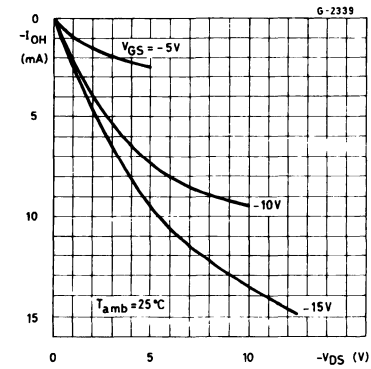

Minimum Output Low (sink) Current Characteristics



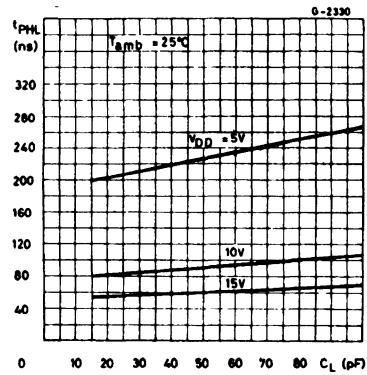
Typical Output High (source) Current Characteristics



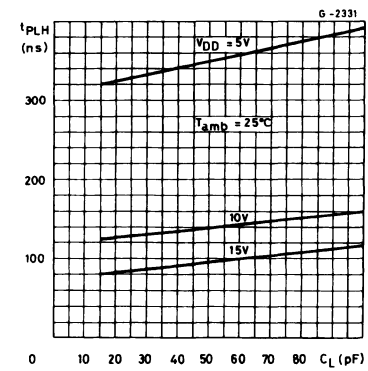

Minimum Output High (source) Current Characteristics



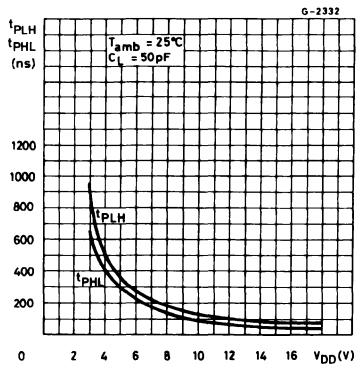

Typical DATA Or ENABLE High to Low Level Propagation Delay Time vs Load Capacitance



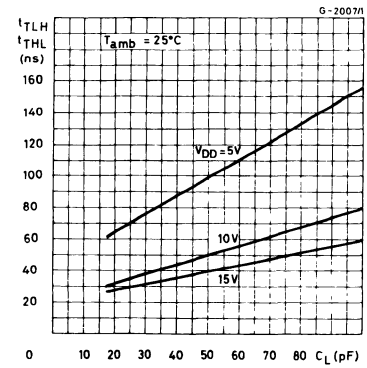

Typical DATA Or ENABLE Low to High Level Propagation Delay Time vs Load Capacitance



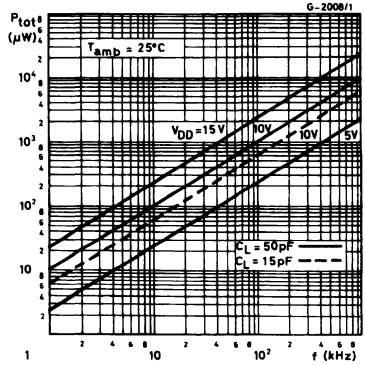

Typical DATA Or ENABLE Propagation Delay Time vs Supply Voltage



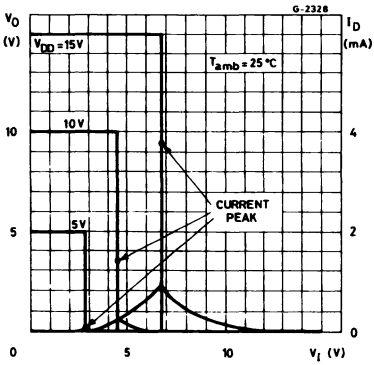

Typical Transition Time vs Load Capacitance

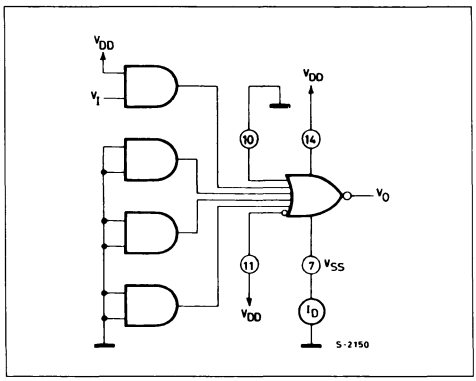


Typical Powwer Dissipation vs Frequency

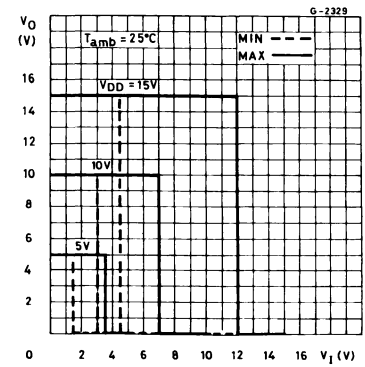


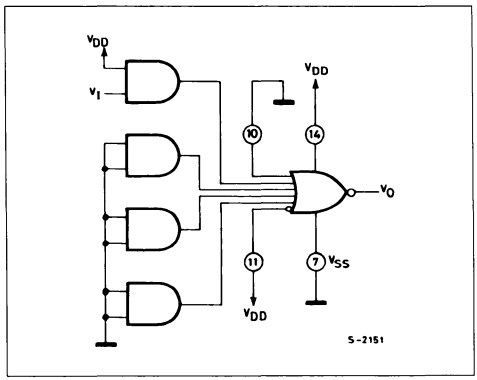

Typical Voltage and Current Transfer Characteristics and Tast Circuit



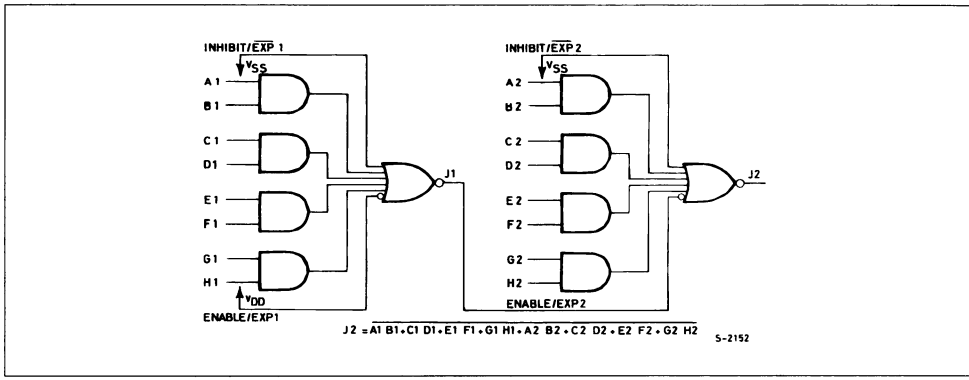

Minimum and Maximum Voltage Transfer Characteristics and Test Circuit



## APPLICATION

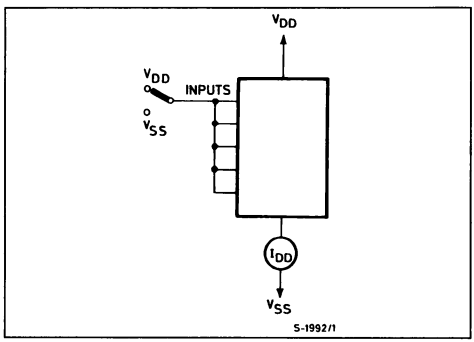
Two 4086B Connected as an 8 Wide 2 Input A-O-I Gate



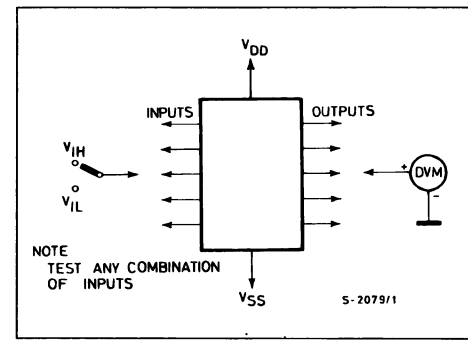

This application shows two HCC/HCF4086B utilized to obtain an 8-widee 2 input A-O-I function. The output (J1) of one HCC/HCF4086B is fed directly to the ENABLE/EXP 2 line of the second HCC/HCF4086B. In a similar fashion, any NAND gate output can be fed directly into the ENABLE/EXP input to obtain a 5 wide A-O-I function. In addition, any AND gate output can be fed directly into the INIBIT/EXP input with the same result.

## TEST CIRCUITS

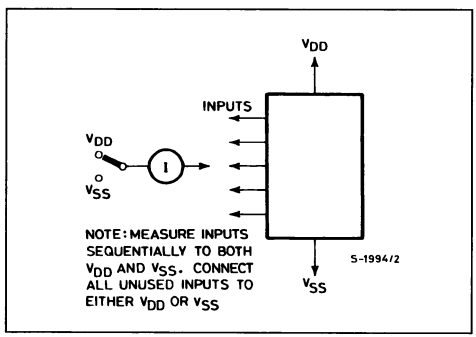
Quiescent Device Current.




Noise Immunity.




Input Leakage Current.



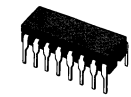
SGS-THOMSON MICROELECTRONICS

# HCC/HCF4089B

## BINARY RATE MULTIPLIER

- CASCADABLE IN MULTIPLES OF 4-BITS
- SET TO "15" INPUT AND "15" DETECT OUTPUT
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

**EY**
(Plastic Package)

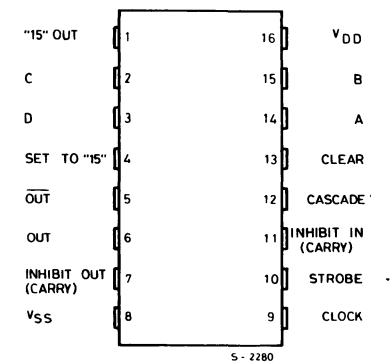


**F**
(Ceramic Package)

**C1**
(Chip Carrier)

**ORDER CODES :**
HCC4089BF HCF4089BEY
HCF4089BC1

**PIN CONNECTIONS**




### DESCRIPTION

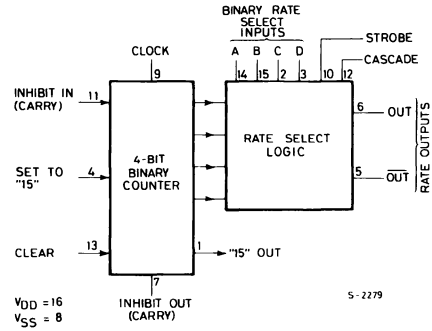
The **HCC4089B** (extended temperature range) and **HCF4089B** (intermediate temperature range) are monolithic integrated circuit available in 16-lead dual in-line plastic or ceramic package.

The **HCC/HCF4089B** is a low-power 4-bit digital rate multiplier that provides an output pulse rate that is the clock-input-pulse rate multiplied by 1/16 times the binary input. For example, when the binary input number is 13, there will be 13 output pulses for every 16 input pulses.

The **HCC/HCF4089B** has an internal synchronous 4-bit counter which, together with one of the four binary input bits, produces pulse trains as shown in timing diagram.

If more than one binary input bit is high, the resulting pulse train is a combination of the above separate pulse trains. This device may be used to perform arithmetic operations (add, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigonometric functions, A/D and D/A conversions, and frequency division.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage . **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

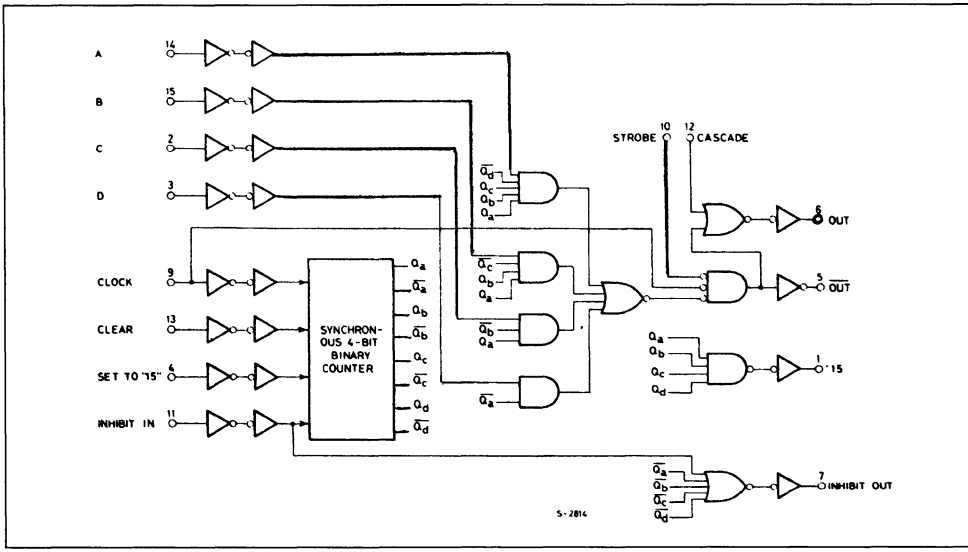
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability

* All voltage values are referred to $V_{SS}$ pin voltage

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAM



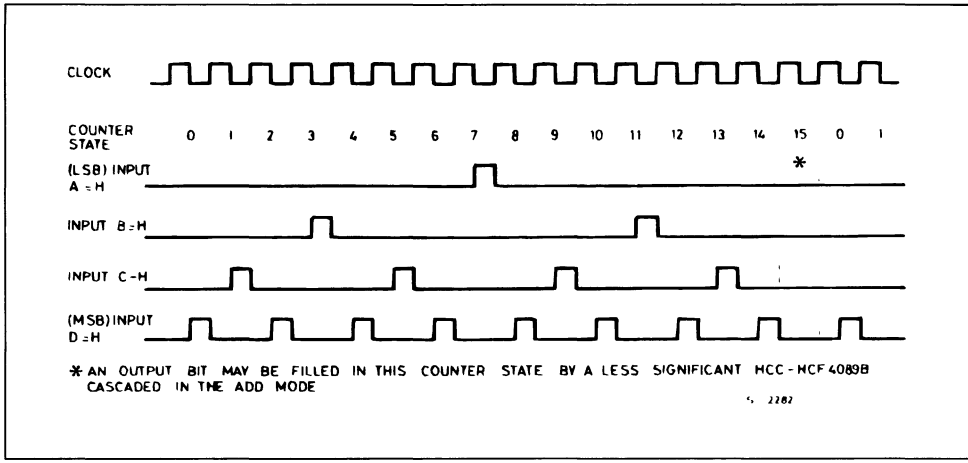

## TRUTH TABLE

| Inputs | | | | | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Number of Pulses or Input Logic Level (0 = low ; 1 = high ; X = don't care) | | | | | | | | | | Number of Pulses or Output Logic Level (L = low ; H = high) | | | |
| D | C | B | A | CLK | INH IN | STR | CAS | CLR | SET | OUT | $\overline{OUT}$ | INH OUT | "15" OUT |
| 0 | 0 | 0 | 0 | 16 | 0 | 0 | 0 | 0 | 0 | L | H | 1 | 1 |
| 0 | 0 | 0 | 1 | 16 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 16 | 0 | 0 | 0 | 0 | 0 | 2 | 2 | 1 | 1 |
| 0 | 0 | 1 | 1 | 16 | 0 | 0 | 0 | 0 | 0 | 3 | 3 | 1 | 1 |
| 0 | 1 | 0 | 0 | 16 | 0 | 0 | 0 | 0 | 0 | 4 | 4 | 1 | 1 |
| 0 | 1 | 0 | 1 | 16 | 0 | 0 | 0 | 0 | 0 | 5 | 5 | 1 | 1 |
| 0 | 1 | 1 | 0 | 16 | 0 | 0 | 0 | 0 | 0 | 6 | 6 | 1 | 1 |
| 0 | 1 | 1 | 1 | 16 | 0 | 0 | 0 | 0 | 0 | 7 | 7 | 1 | 1 |
| 1 | 0 | 0 | 0 | 16 | 0 | 0 | 0 | 0 | 0 | 8 | 8 | 1 | 1 |
| 1 | 0 | 0 | 1 | 16 | 0 | 0 | 0 | 0 | 0 | 9 | 9 | 1 | 1 |
| 1 | 0 | 1 | 0 | 16 | 0 | 0 | 0 | 0 | 0 | 10 | 10 | 1 | 1 |
| 1 | 0 | 1 | 1 | 16 | 0 | 0 | 0 | 0 | 0 | 11 | 11 | 1 | 1 |
| 1 | 1 | 0 | 0 | 16 | 0 | 0 | 0 | 0 | 0 | 12 | 12 | 1 | 1 |
| 1 | 1 | 0 | 1 | 16 | 0 | 0 | 0 | 0 | 0 | 13 | 13 | 1 | 1 |
| 1 | 1 | 1 | 0 | 16 | 0 | 0 | 0 | 0 | 0 | 14 | 14 | 1 | 1 |
| 1 | 1 | 1 | 1 | 16 | 0 | 0 | 0 | 0 | 0 | 15 | 15 | 1 | 1 |
| X | X | X | X | 16 | 1 | 0 | 0 | 0 | 0 | • | • | H | • |
| X | X | X | X | 16 | 0 | 1 | 0 | 0 | 0 | L | H | 1 | 1 |
| X | X | X | X | 16 | 0 | 0 | 1 | 0 | 0 | H | * | 1 | 1 |
| 1 | X | X | X | 16 | 0 | 0 | 0 | 1 | 0 | 16 | 16 | H | L |
| 0 | X | X | X | 16 | 0 | 0 | 0 | 1 | 0 | L | H | H | L |
| X | X | X | X | 16 | 0 | 0 | 0 | 0 | 1 | L | H | L | H |

* Output same as the first 16 lines of this truth table (depending on values of A, B, C, D).

• Depends on internal state of counter.

## TIMING DIAGRAM




## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | | |

* $T_{Low}$ = – 55°C for **HCC** device : – 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device · + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.

## STATIC ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | | Test Conditions | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | – 2 | | – 1.6 | – 3.2 | | – 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | – 0.64 | | – 0.51 | – 1 | | – 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | – 1.6 | | – 1.3 | – 2.6 | | – 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | – 4.2 | | – 3.4 | – 6.8 | | – 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | – 1.53 | | – 1.36 | – 3.2 | | – 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | – 0.52 | | – 0.44 | – 1 | | – 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | – 1.3 | | – 1.1 | – 2.6 | | – 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | – 3.6 | | – 3.0 | – 6.8 | | – 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = – 55°C for **HCC** device : – 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device . + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall times = 20ns)

| Symbol | Parameter | | Test Conditions | Value | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time | Clock to $\overline{out}$ | | 5 | | 110 | 220 | ns |
| | | | | 10 | | 55 | 110 | |
| | | | | 15 | | 45 | 90 | |
| | | Clock or Strobe to out | | 5 | | 150 | 300 | ns |
| | | | | 10 | | 75 | 150 | |
| | | | | 15 | | 60 | 120 | |
| | | Clock to Inhibit High Level to Low Level | | 5 | | 360 | 720 | ns |
| | | | | 10 | | 160 | 320 | |
| | | | | 15 | | 110 | 220 | |
| | | Low Level to High Level | | 5 | | 250 | 500 | ns |
| | | | | 10 | | 100 | 200 | |
| | | | | 15 | | 75 | 150 | |
| | | Clear to out | | 5 | | 380 | 760 | ns |
| | | | | 10 | | 175 | 350 | |
| | | | | 15 | | 130 | 260 | |
| | | Clock to "9" or "15" out | | 5 | | 300 | 600 | ns |
| | | | | 10 | | 125 | 250 | |
| | | | | 15 | | 90 | 180 | |
| | | Cascade to out | | 5 | | 90 | 180 | ns |
| | | | | 10 | | 45 | 90 | |
| | | | | 15 | | 35 | 70 | |
| | | Inhibit in to Inhibit out | | 5 | | 160 | 320 | ns |
| | | | | 10 | | 75 | 150 | |
| | | | | 15 | | 55 | 110 | |
| | | Set to out | | 5 | | 330 | 660 | ns |
| | | | | 10 | | 150 | 300 | |
| | | | | 15 | | 110 | 220 | |

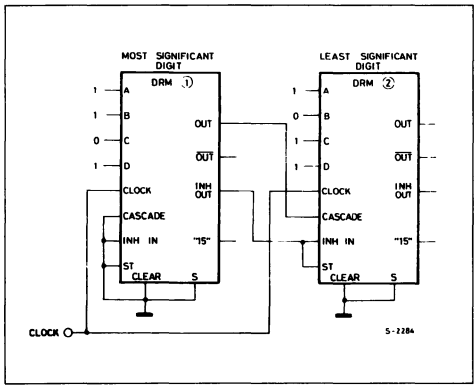
**DYNAMIC ELECTRICAL CHARACTERISTICS** (continued )

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | 5 | | 100 | 200 | ns |
| | | 10 | | 50 | 100 | |
| | | 15 | | 40 | 80 | |
| $f_{CL}$ | Maximum Clock Frequency | 5 | 1.2 | 2.4 | | MHz |
| | | 10 | 2.5 | 5 | | |
| | | 15 | 3.5 | 7 | | |
| $t_W$ | Clock Pulse Width | 5 | 330 | 165 | | ns |
| | | 10 | 170 | 85 | | |
| | | 15 | 100 | 50 | | |
| $t_r$, $t_f$ | Clock Rise or Fall Time | 5 | | | 15 | µs |
| | | 10 | | | 15 | |
| | | 15 | | | 15 | |
| $t_W$ | Set or Clear Pulse Width | 5 | 160 | 80 | | ns |
| | | 10 | 90 | 45 | | |
| | | 15 | 60 | 30 | | |
| $t_{setup}$ | Inhibit Input Setup Time, High Level to Low Level | 5 | 100 | 50 | | ns |
| | | 10 | 40 | 20 | | |
| | | 15 | 20 | 10 | | |
| $t_R$ | Inhibit, Input Removal Time | 5 | 240 | 120 | | ns |
| | | 10 | 130 | 65 | | |
| | | 15 | 110 | 55 | | |
| $t_R$ | Minimum Set Removal Time | 5 | 150 | 75 | | ns |
| | | 10 | 80 | 40 | | |
| | | 15 | 50 | 25 | | |
| $t_R$ | Clear Removal Time | 5 | 60 | 30 | | ns |
| | | 10 | 40 | 20 | | |
| | | 15 | 30 | 15 | | |

## APPLICATION NOTES

For words of more than 4 bits, **HCC/HCF4089B** devices may be cascaded in two different modes : an Add mode and a Multiply mode.

Two **HCC/HCF4089B's** cascaded in the "Add" mode with a preset number of 189.

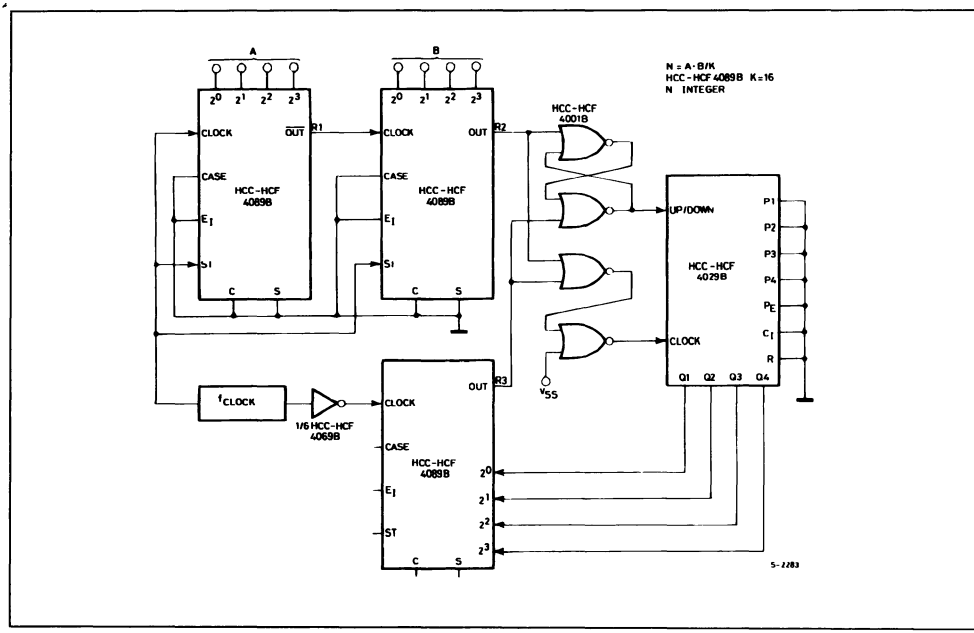



**Nota :**

In the Add mode some of the gaps left by the more significant unit at the count of 15 are filled in by the less significant units. For example, when two units are cascaded in the Add mode and programmed to 11 and 13, respectively, the more significant unit will have 11 output pulses for every 16 input pulses and the other unit will have 13 output pulses for every 256 input pulses for a total of

$$\frac{11}{16} + \frac{13}{256} = \frac{189}{256}$$

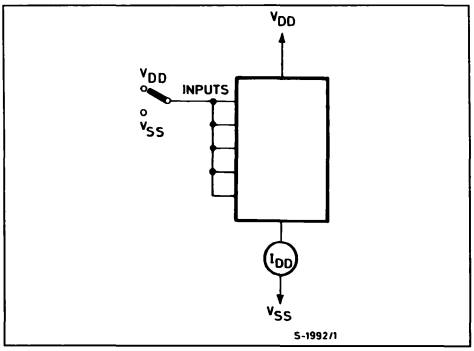
Two **HCC/HCF4089B's** cascaded in the Multiply mode for Multiplication of two variables A and B with loop circuit control.



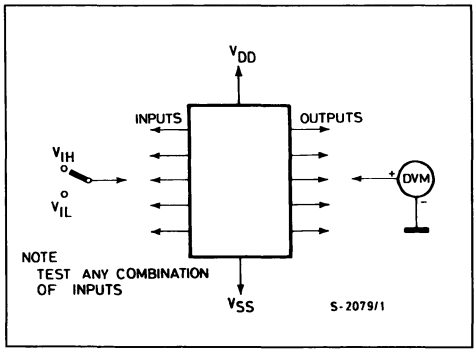

When the loop stabilies rate R2 = rate R3, thus fclock $\left(\frac{A}{16}\cdot\frac{B}{16}\right)$ = fclock $\left(\frac{1}{16}\cdot\frac{N}{16}\right)$ therefore N = A.B.

## TEST CIRCUITS

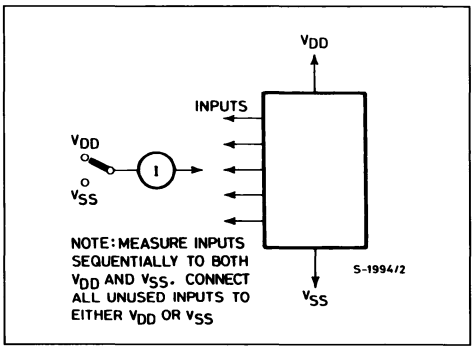
Quiescent Device Current.




Noise Immunity.




Input Leakage Current.



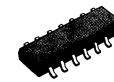
# HCC/HCF4093B

## QUAD 2-INPUT NAND SCHMIDT TRIGGERS

- SCHMITT-TRIGGER ACTION ON EACH INPUT WITH NO EXTERNAL COMPONENTS
- HYSTERESIS VOLTAGE TYPICALLY 0.9V AT $V_{DD}$ = 5V AND 2.3V AT $V_{DD}$ = 10V
- NOISE IMMUNITY GREATER THAN 50% OF $V_{DD}$ (typ.)
- NO LIMIT ON INPUT RISE AND FALL TIMES
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

**EY**
(Plastic Package)

**F**
(Ceramic Frit Seal Package)



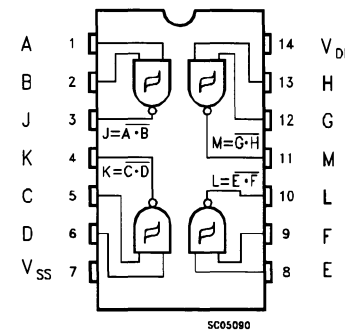
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4093BF HCF4093BM1
HCF4093BEY HCF4093BC1

**PIN CONNECTIONS**



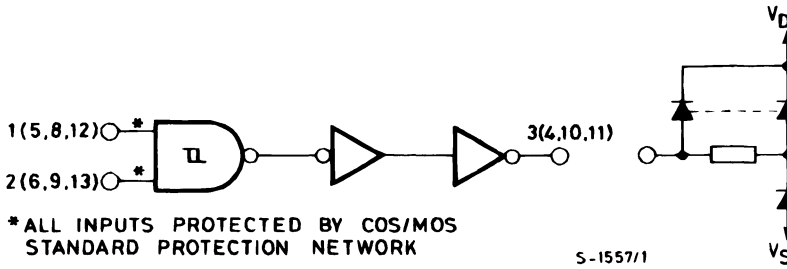

### DESCRIPTION

The **HCC4093B** (extended temperature range) and **HCF4093B** (intermediate temperature range) are available in 14-lead dual in-line plastic or ceramic package and plastic micropackage. The **HCC/HCF4093B** consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive and negative-going signals.

The difference between the positive voltage ($V_P$) and the negative voltage ($V_N$) is defined as hysteresis voltage ($V_H$) (see fig. 1).

## FUNCTIONAL DIAGRAM

1 of 4 Schmitt triggers




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings "may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 1 | | 0.02 | 1 | | 30 | μA |
| | | | 0/10 | | | 10 | | 2 | | 0.02 | 2 | | 60 | |
| | | | 0/15 | | | 15 | | 4 | | 0.02 | 4 | | 120 | |
| | | | 0/20 | | | 20 | | 20 | | 0.04 | 20 | | 600 | |
| | | HCF Types | 0/ 5 | | | 5 | | 4 | | 0.02 | 4 | | 30 | |
| | | | 0/10 | | | 10 | | 8 | | 0.02 | 8 | | 60 | |
| | | | 0/15 | | | 15 | | 16 | | 0.02 | 16 | | 120 | |
| $V_P$ | Positive Trigger Threshold Voltage | | a | | | 5 | 2.2 | 3.6 | 2.2 | 2.9 | 3.6 | 2.2 | 3.6 | V |
| | | | a | | | 10 | 4.6 | 7.1 | 4.6 | 5.9 | 7.1 | 4.6 | 7.1 | |
| | | | a | | | 15 | 6.8 | 10.8 | 6.8 | 8.8 | 10.8 | 6.8 | 10.8 | |
| | | | b | | | 5 | 2.6 | 4 | 2.6 | 3.3 | 4 | 2.6 | 4 | |
| | | | b | | | 10 | 5.6 | 8.2 | 5.6 | 7 | 8.2 | 5.6 | 8.2 | |
| | | | b | | | 15 | 6.3 | 12.7 | 6.3 | 9.4 | 12.7 | 6.3 | 12.7 | |
| $V_N$ | Negative Trigger Threshold Voltage | | a | | | 5 | 0.9 | 2.8 | 0.9 | 1.9 | 2.8 | 0.9 | 2.8 | V |
| | | | a | | | 10 | 2.5 | 5.2 | 2.5 | 3.9 | 5.2 | 2.5 | 5.2 | |
| | | | a | | | 15 | 4 | 7.4 | 4 | 5.8 | 7.4 | 4 | 7.4 | |
| | | | b | | | 5 | 1.4 | 3.2 | 1.4 | 2.3 | 3.2 | 1.4 | 3.2 | |
| | | | b | | | 10 | 3.4 | 6.6 | 3.4 | 5.1 | 6.6 | 3.4 | 6.6 | |
| | | | b | | | 15 | 4.8 | 9.6 | 4.8 | 7.3 | 9.6 | 4.8 | 9.6 | |
| $V_H$ | Hysteresis Voltage | | a | | | 5 | 0.3 | 1.6 | 0.3 | 0.9 | 1.6 | 0.3 | 1.6 | V |
| | | | a | | | 10 | 1.2 | 3.4 | 1.2 | 2.3 | 3.4 | 1.2 | 3.4 | |
| | | | a | | | 15 | 1.6 | 5 | 1.6 | 3.5 | 5 | 1.6 | 5 | |
| | | | b | | | 5 | 0.3 | 1.6 | 0.3 | 0.9 | 1.6 | 0.3 | 1.6 | |
| | | | b | | | 10 | 1.2 | 3.4 | 1.2 | 2.3 | 3.4 | 1.2 | 3.4 | |
| | | | b | | | 15 | 1.6 | 5 | 1.6 | 3.5 | 5 | 1.6 | 5 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |

a : input on terminals 1, 5, 8, 12 or 2, 6, 9, 13 ; other inputs to $V_{DD}$.
b : input on terminals 1 and 2, 5 and 6, 8 and 9, or 12 and 13 ; other inputs to $V_{DD}$.
* $T_{Low}$ = −55°C for **HCC** device : -40°C for **HCF** device.
* $T_{High}$ = +125°C for **HCC** device : +85°C for **HCF** device.

## STATIC ELECTRICAL CHARACTERISTICS ( continued)

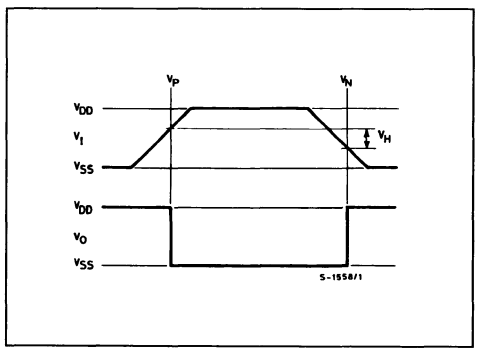
| Symbol | Parameter | | Test Conditions | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{Low}$* | | 25°C | | | $T_{High}$* | | |
| | | | | | | | Min. | Max. | Min. | Typ. | Max. | Min. | Max. | |
| $I_{OL}$ | Output Sink Current | | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | ± $10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | ± $10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

## DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ = 0.3%/°C values , all input rise and fall time = 20ns)

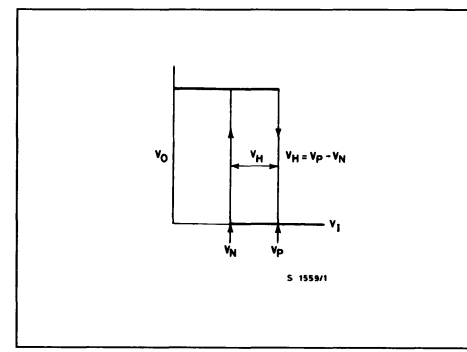
| Symbol | Parameter | Test Conditions | Value | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time | | 5 | | 190 | 380 | ns |
| | | | 10 | | 90 | 180 | |
| | | | 15 | | 65 | 130 | |
| $t_{TLH}$, $t_{THL}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

**Figure1** : Hysteresis Definition, Characteristics and Test Setup.

(a) Definition of $V_P$, $V_N$ and $V_H$




(b) Transfer characteristics of 1 of 4 gates



(c) Test setup

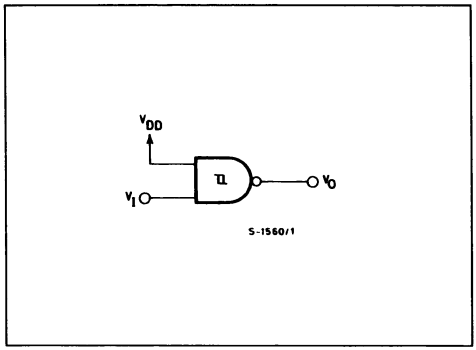



**Figure 2** : Input and Output Characteristics.

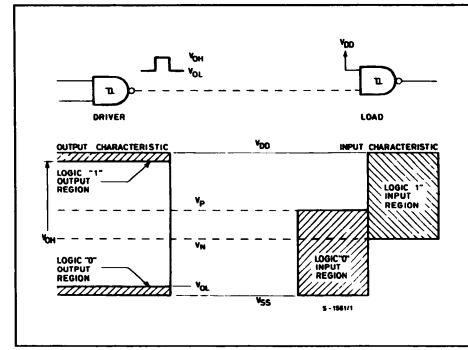
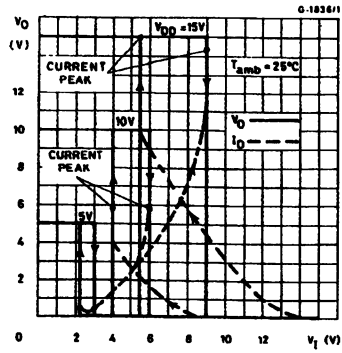



**Figure 3** : Typical Current and Voltage Transfer Characteristics.



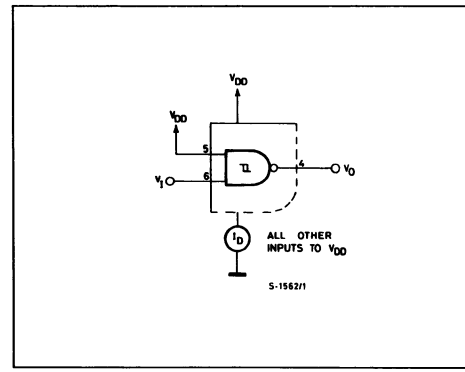
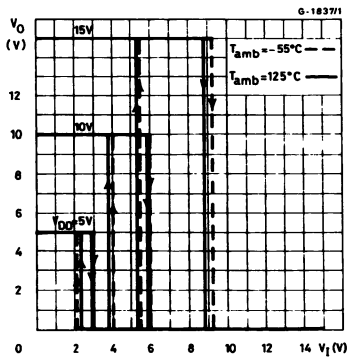




**Figure 4** : Typical Voltage Transfer Characteristics as a Function of Temperature, and Test Circuit.



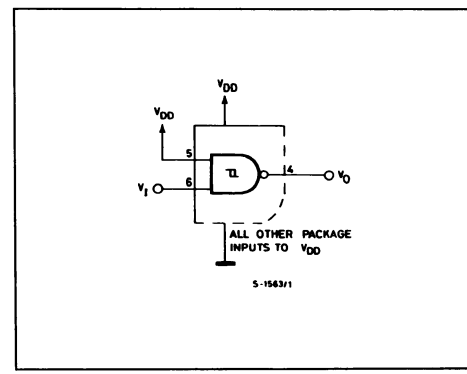



**Figure 5** : Typical Output Low (sink) Current Characteristics.

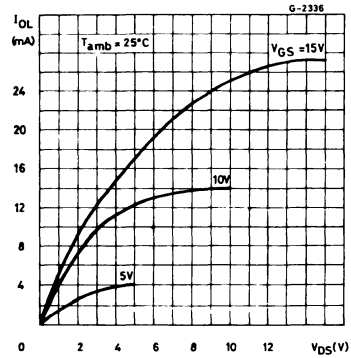



**Figure 6** : Minimum Output Low (sink) Current Characteristics.

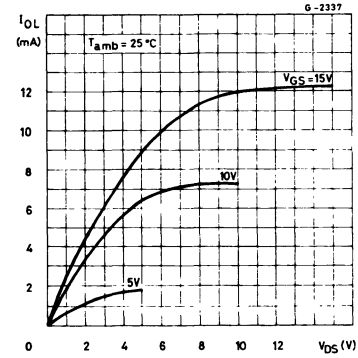



**Figure 7** : Typical Output High (source) Current Characteristic.

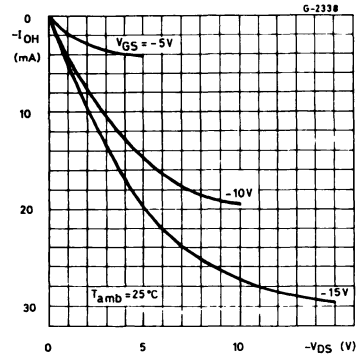



**Figure 8** : Minimum Output High Current Characteristics.

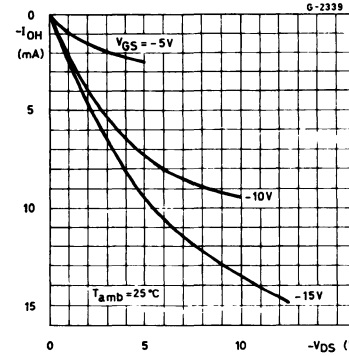



**Figure 9** : Typical Propagation Delay Time vs. Supply Voltage.

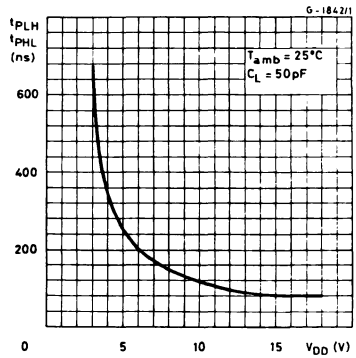



**Figure 10** : Typical Transition Time vs. Load Capacitance.

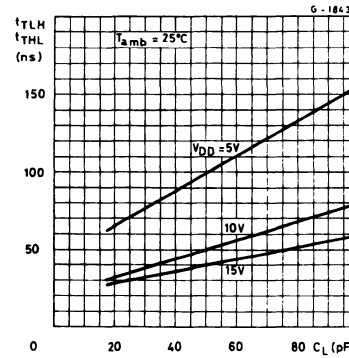


**Figure 11** : Typical Trigger Threshold Voltage vs. $V_{DD}$

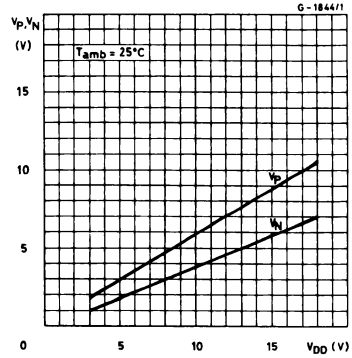



**Figure 12** : Typical per cent Hysteresis vs. Supply Voltage.

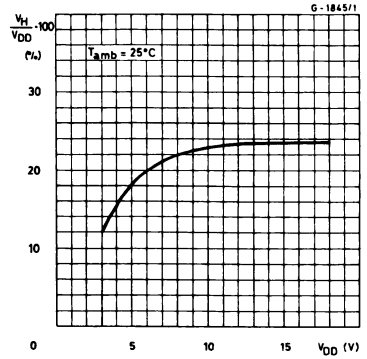



**Figure 13** : Typical Dissipation Characteristics.

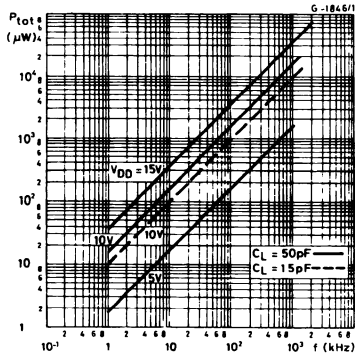
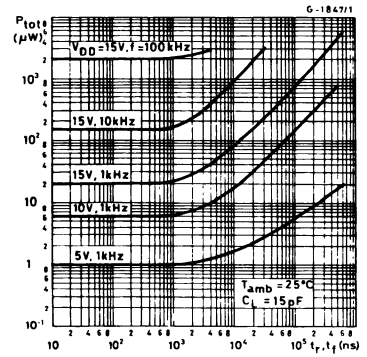



**Figure 14** : Power Dissipation vs. Rise and Fall Times.



## APPLICATIONS

**Figure 15** : Wave Shaper.

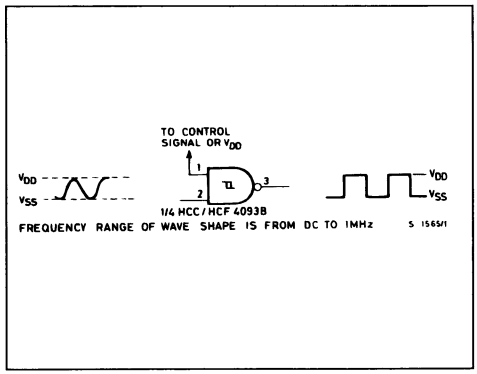



**Figure 16** : Monostable Multivibrator.

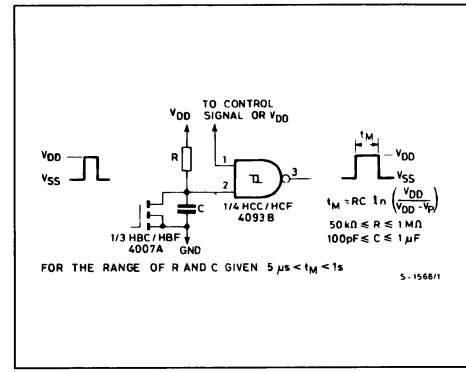
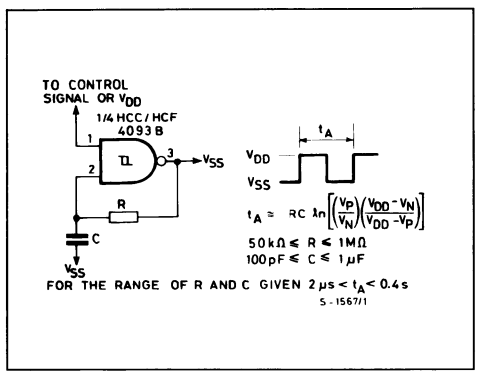



**Figure17** : Astable Multivibrator.




## TEST CIRCUITS

**Figure18** : Quiescent Device Current.

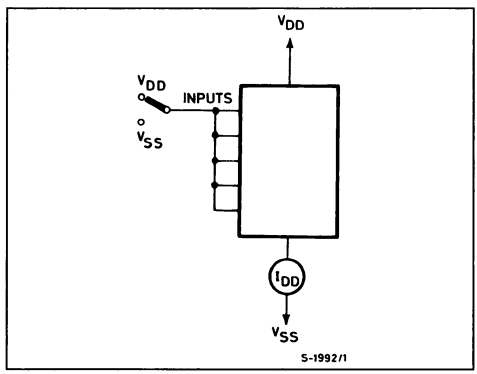
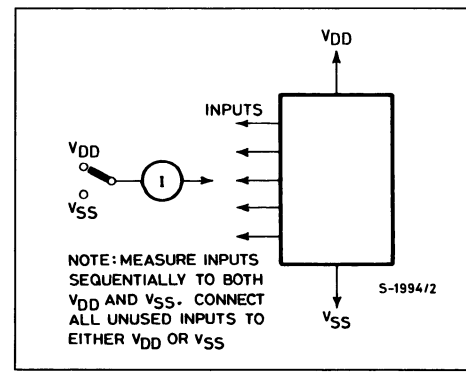



**Figure 19** : Input Leakage Current.

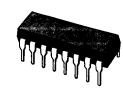


SGS-THOMSON MICROELECTRONICS

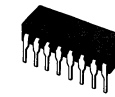
# HCC/HCF4094B

## 8–STAGE SHIFT-AND-STORE BUS REGISTER

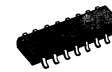
- 3-STATE PARALLEL OUTPUTS FOR CONNECTION TO COMMON BUS
- SEPARATE SERIAL OUTPUTS SYNCHRONOUS TO BOTH POSITIVE AND NEGATIVE CLOCK EDGES FOR CASCADING
- MEDIUM SPEED OPERATION 5MHz AT 10V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)



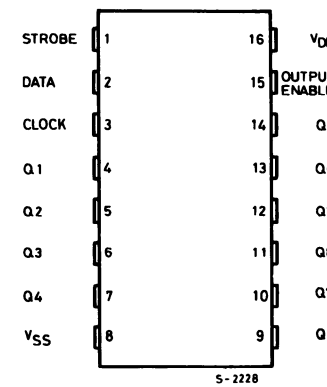
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4094BF HCF4094BM1
HCF4094BEY HCF4094BC1

### PIN CONNECTIONS

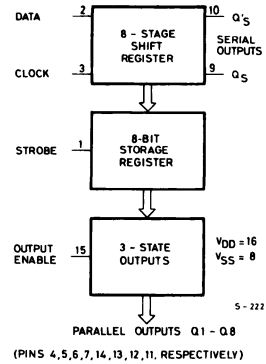



### DESCRIPTION

The **HCC4094B** (extended temperature range) and **HCF4094B** (intermediate temperature range) are monolithic integrated circuits available in 16-lead dual in-line plastic or ceramic packageand plastic micropackage.

The **HCC/HCF4094B** is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the STROBE input is high. Data in the storage register appears at the outputs whenever the OUTPUT-ENABLE signal is high. Two serial outputs are available for cascading a number of **HCC/HCF4094B** devices. Data is available at the $Q_S$ serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the Q's terminal on the next negative clock edge, provides a means for cascading **HCC/HCF4094B** devices when the clock rise time is slow.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

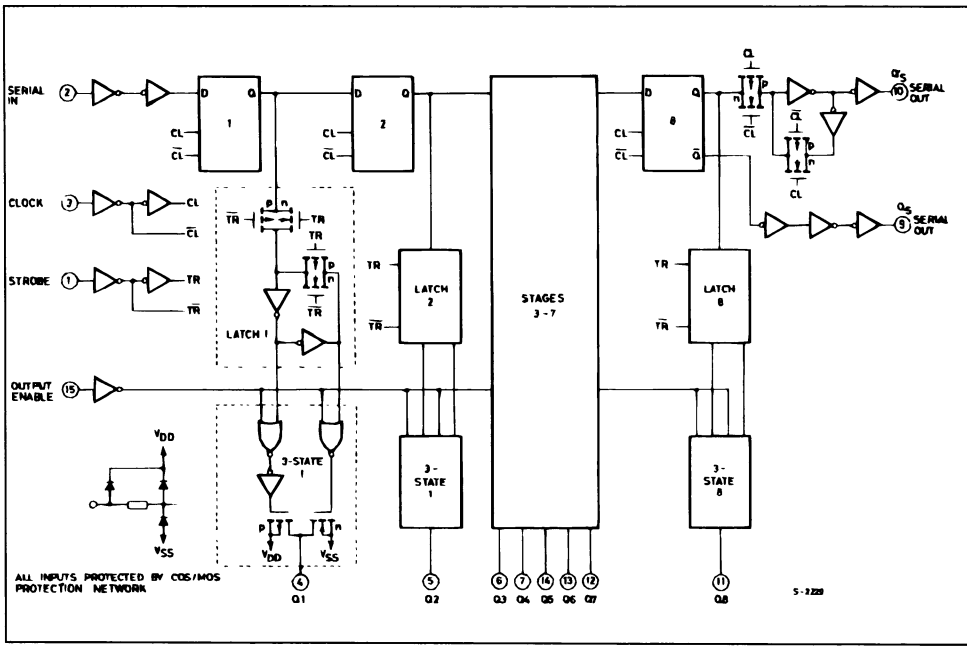
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to $V_{SS}$ pin voltage.

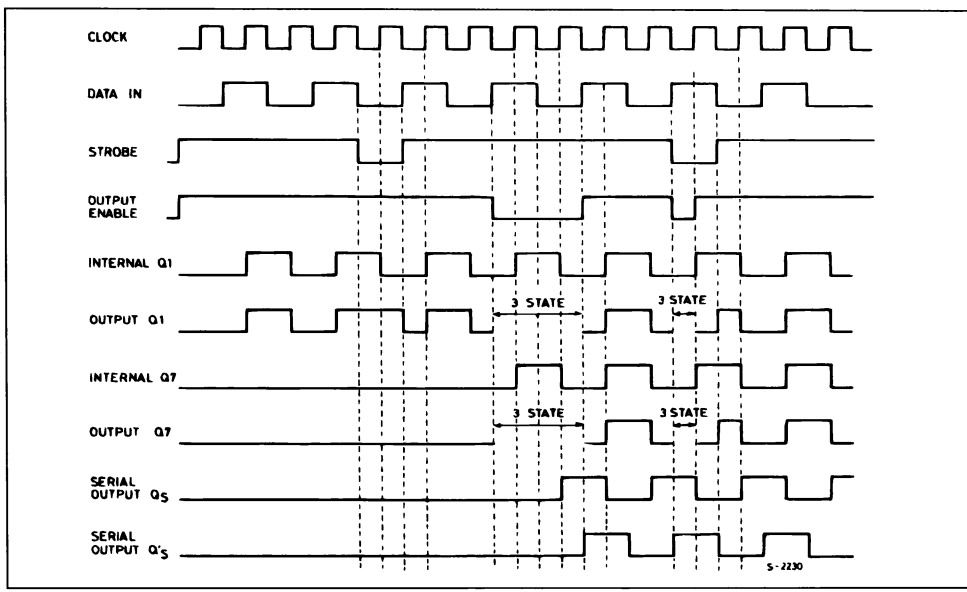
## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAMS




## TIMING DIAGRAM



## TRUTH TABLE

TRUTH TABLE

| CL$^{\Delta}$ | Outputs Enable | Strobe | Data | Parallel Outputs | | Serial Outputs | |
|---|---|---|---|---|---|---|---|
| | | | | Q1 | QN | QS* | Q'S |
| ⎍ | 0 | X | X | OC | OC | Q7 | NC |
| ⎏ | 0 | X | X | OC | OC | NC | Q7 |
| ⎍ | 1 | 0 | X | NC | NC | Q7 | NC |
| ⎍ | 1 | 1 | 0 | 0 | $Q_N$-1 | Q7 | NC |
| ⎍ | 1 | 1 | 1 | 1 | $Q_N$-1 | Q7 | NC |
| ⎏ | 1 | 1 | 1 | NC | NC | NC | Q7 |

▲ = Level Change
X = Don't Care
NC = No Change
OC = Open Circuit
Logic 1 ≡ High
Logic 0 ≡ Low

* At the positive clock edge information in the 7th shift register stage is transferred to the 8th register stage and the $Q_S$ output

**STATIC ELECTRICAL CHARACTERISTICS** (over recommended operating conditions)

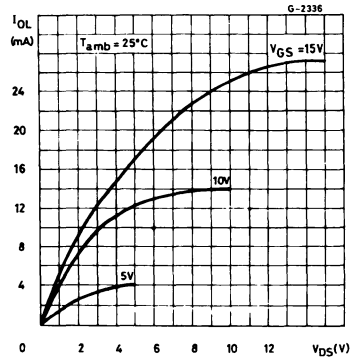
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1 5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $I_{OH}$, $I_{OL}$ | 3-state Output Leakage Current | HCC Types | 0/18 | 0/18 | | 18 | | ± 0.4 | | $± 10^{-4}$ | ± 0.4 | | ± 12 | μA |
| | | HCF Types | 0/15 | 0/15 | | 15 | | ± 1.0 | | $± 10^{-4}$ | ± 1.0 | | ± 7.5 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device
The Noise Margin for both "1" and "0" level is . 1V min with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V

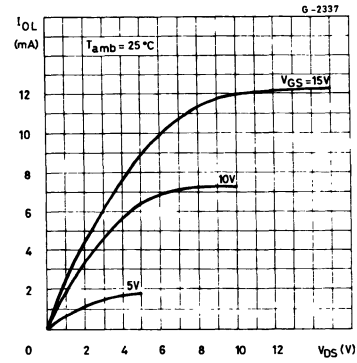
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ = 0.3%/°C values , all input rise and fall time = 20ns)

| Symbol | Parameter | Test Conditions | Value | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time Clock to Serial Output $Q_S$ | | 5 | | 300 | 600 | ns |
| | | | 10 | | 125 | 250 | |
| | | | 15 | | 95 | 190 | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time Clock to Serial Output $Q'_S$ | | 5 | | 230 | 460 | ns |
| | | | 10 | | 110 | 220 | |
| | | | 15 | | 75 | 150 | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time Clock to Parallel Output | | 5 | | 420 | 840 | ns |
| | | | 10 | | 195 | 390 | |
| | | | 15 | | 135 | 270 | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time Strobe to Parallel Output | | 5 | | 290 | 580 | ns |
| | | | 10 | | 145 | 290 | |
| | | | 15 | | 100 | 200 | |
| $t_{PHZ}$ | Propagation Delay Time Output Enable to Parallel Output : Output High to High Impedance | | 5 | | 140 | 280 | ns |
| | | | 10 | | 75 | 150 | |
| | | | 15 | | 55 | 110 | |
| $t_{PLZ}$ | Out Low to High Impedance | | 5 | | 225 | 450 | ns |
| | | | 10 | | 95 | 190 | |
| | | | 15 | | 70 | 140 | |
| $t_W$ | Strobe Pulse Width | | 5 | 200 | 100 | | ns |
| | | | 10 | 80 | 40 | | |
| | | | 15 | 70 | 35 | | |
| $t_W$ | Clock Pulse Width | | 5 | 200 | 100 | | ns |
| | | | 10 | 100 | 50 | | |
| | | | 15 | 83 | 40 | | |
| $t_{setup}$ | Data Setup Time | | 5 | 125 | 60 | | ns |
| | | | 10 | 55 | 30 | | |
| | | | 15 | 35 | 20 | | |
| $t_{TLH}$, $t_{THL}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_r$, $t_f$ | Clock Input Rise or Fall Time | | 5 | 15 | | | µs |
| | | | 10 | 5 | | | |
| | | | 15 | 5 | | | |
| $f_{max}$ | Maximum Clock Input Frequency | | 5 | 1.25 | 2.5 | | MHz |
| | | | 10 | 2.5 | 5 | | |
| | | | 15 | 3 | 6 | | |

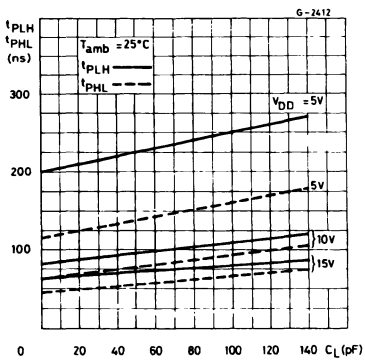
Typical Output Low (sink) Current Characteristics.



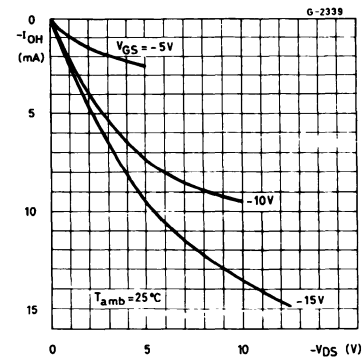

Minimum Output Low (sink) Current Characteristics.



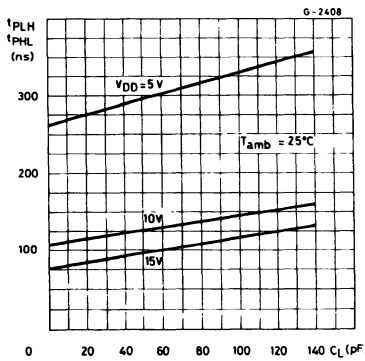

Typical Output High (source) Current Charateristics.



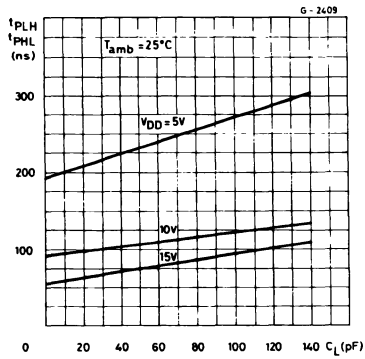

Minimum Output High (source) Current Characteristics.



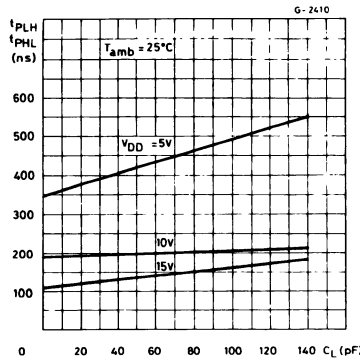

Clock-to-serial Output $Q_S$ Propagation Delay vs. $C_L$.



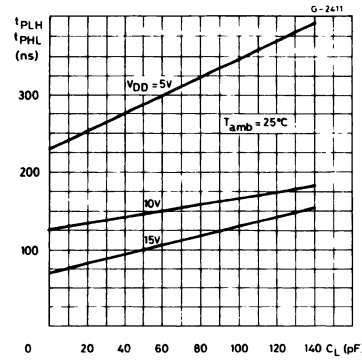

Clock-to-serial Output $Q'_S$ Propagation Delay vs. $C_L$.



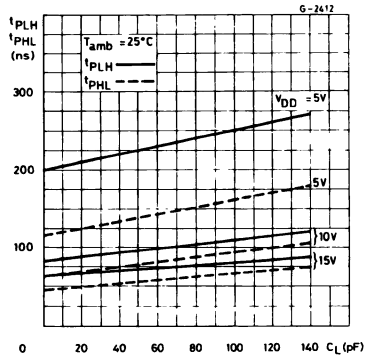
Clock-to-parallel Output Propagation Delay vs. $C_L$.



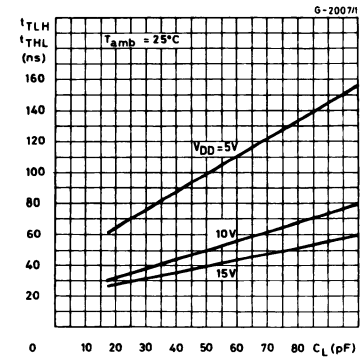

Strobe-to-parallel Output Propagation Delay vs. $C_L$.



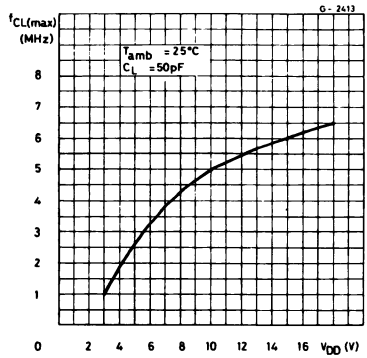

Output Enable-to-parallel Output Propagation Delay vs.



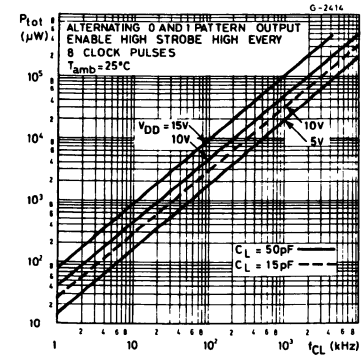

Typical Transition Time vs. Load Capacitance.




Typical Maximum-clock Frequency vs. Supply Voltage.

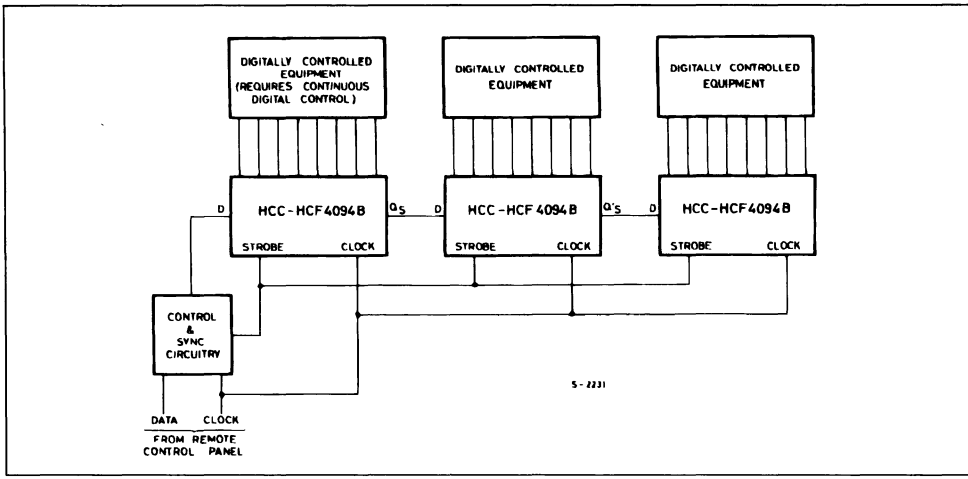



Dynamic Power Dissipation vs. Input Clock Frequency.



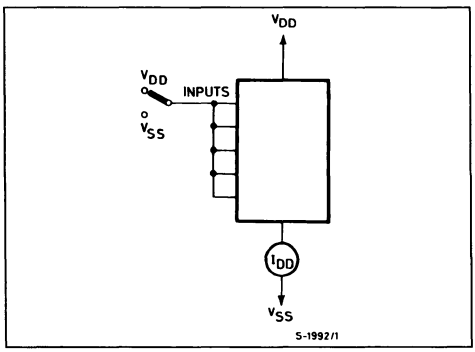
## TYPICAL APPLICATION

REMOTE CONTROL HOLDING REGISTER

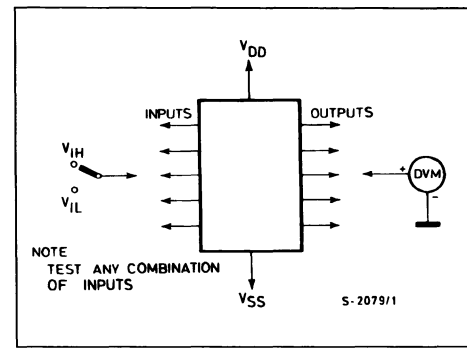



## TEST CIRCUITS

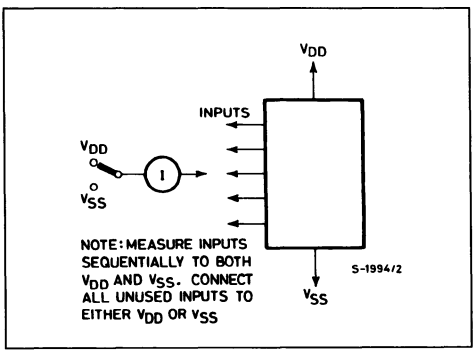
Quiescent Device Current.




Noise Immunity.




Input Leakage Current.



SGS-THOMSON MICROELECTRONICS

# HCC/HCF4095B
# HCC/HCF4096B

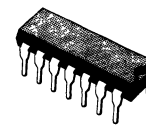
## GATE J-K MASTER-SLAVE FLIP-FLOPS

- 16 MHz TOGGLE RATE (typ.) AT $V_{DD}$ - $V_{SS}$ = 10V
- GATED INPUTS
- QUIESCENT CURRENT SPECIFIED TO 20v FOR HCC DEVICE
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25oC FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No 13 A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"

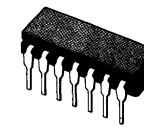
### DESCRIPTION

The **HCC4095B/4096B** (extended temperature range) and **HCF4095B/4096B** (intermediate temperature range) are monolithic integrated circuits, available in 14 lead dual in-line plastic or ceramic package and plastic micropackage.

The **HCC/HCF4095B** and **HCC/HCF4096B** are J-K Master-Slave Flip-Flops featuring separate AND gating of multiple J and K inputs. The gated J-K input control transfer of information into the master section during clocked operation. Information on the J-K inputs is transferred to the Q and $\overline{Q}$ outputs on the positive edge of the clock pulse. SET and RESET inputs (active high) are provided for asynchronous operation.



**EY**
(Plastic Package)



**F**
(Ceramic Package)

**M1**
(Micro Package)

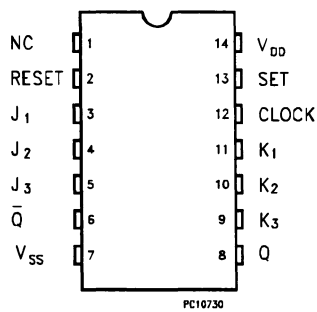
**C1**
(Chip Carrier)

**ORDER CODES :**

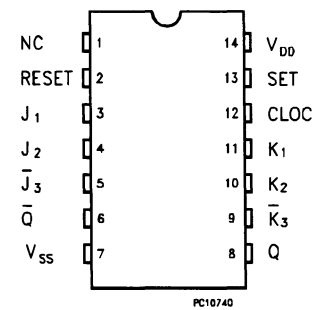
| | |
|---|---|
| HCC40XXBF | HCF40XXBM1 |
| HCF40XXBEY | HCF40XXBC1 |

### PIN CONNECTIONS

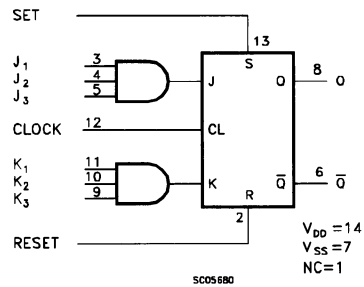
**4095B**

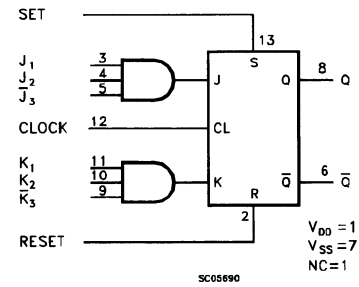



**4096B**

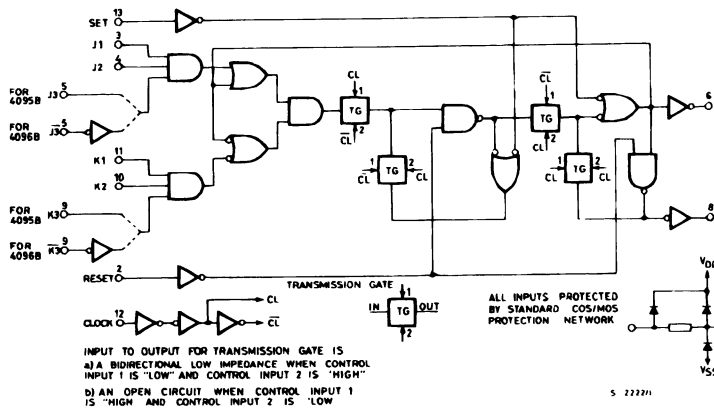


## FUNCTIONAL DIAGRAMS




## LOGIC DIAGRAM




## TRUTH TABLES

### SYNCHRONOUS OPERATION (S=0 R=0)

| Inputs Before Positive Clock Transition | | Outputs After Positive Clock Transition | |
|---|---|---|---|
| J * | K * | Q | $\overline{Q}$ |
| 0 | 0 | No Change | |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | Toggles | |

* For 4095B J = J1 • J2 • $\overline{J3}$, K = K1 • K2 • $\overline{K3}$
* For 4095B J = J1 • J2 • J3, K = K1 • K2 • $\overline{K3}$

### ASYNCHRONOUS OPERATION (J and K DON'T CARE)

| S | R | Q | $\overline{Q}$ |
|---|---|---|---|
| 0 | 0 | No Change | |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

0 = $V_{SS}$, 1 = $V_{DD}$

## ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ * | Supply Voltage: **HCC** Types<br>**HCF** Types | -0.5 to +20<br>-0.5 to +18 | V<br>V |
| $V_I$ | Input Voltage | -0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for Top = Full Package Temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage: **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditios | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{LOW}$ * Min. | $T_{LOW}$ * Max. | 25 °C Min. | 25 °C Typ. | 25 °C Max. | $T_{HIGH}$ * Min. | $T_{HIGH}$ * Max. | |
| $I_L$ | Quiescent Current | HCC Types | 0/5 | | | 5 | | 1 | | 0.02 | 1 | | 30 | μA |
| | | | 0/10 | | | 10 | | 2 | | 0.02 | 2 | | 60 | |
| | | | 0/15 | | | 15 | | 4 | | 0.02 | 4 | | 120 | |
| | | | 0/20 | | | 20 | | 20 | | 0.04 | 20 | | 600 | |
| | | HCF Types | 0/5 | | | 5 | | 4 | | 0.02 | 4 | | 30 | |
| | | | 0/10 | | | 10 | | 8 | | 0.02 | 8 | | 60 | |
| | | | 0/15 | | | 15 | | 16 | | 0.02 | 16 | | 120 | |
| $V_{OH}$ | Output High Voltage | | 0/5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/5 | 2.5 | | 5 | -2 | | -1.6 | -3.2 | | -1.15 | | mA |
| | | | 0/5 | 4.6 | | 5 | -0.64 | | -0.51 | -1 | | -0.36 | | |
| | | | 0/10 | 9.5 | | 10 | -1 6 | | -1.3 | -2.6 | | -0.9 | | |
| | | | 0/15 | 13.5 | | 15 | -4.2 | | -3.4 | -6.8 | | -2.4 | | |
| | | HCF Types | 0/5 | 2.5 | | 5 | -1.53 | | -1.36 | -3.2 | | -1.1 | | |
| | | | 0/5 | 4.6 | | 5 | -0.52 | | -0.44 | -1 | | -0.36 | | |
| | | | 0/10 | 9.5 | | 10 | -1.3 | | -1.1 | -2.6 | | -0.9 | | |
| | | | 0/15 | 13.5 | | 15 | -3.6 | | -3.0 | -6.8 | | -2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | | 0/18 | Any Input | | 18 | | ±0.1 | | $±10^{-5}$ | ±0.1 | | ±1 | μA |
| | | | 0/15 | | | 15 | | ±0.3 | | $±10^{-5}$ | ±0.3 | | ±1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{LOW}$ = -55 °C for **HCC** device: -40 °C for **HCF** device.

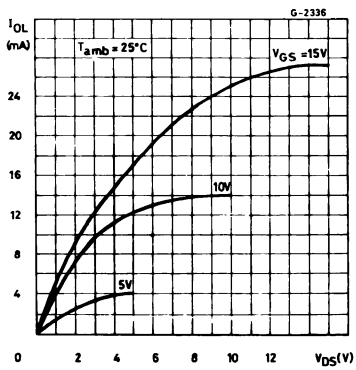
* $T_{HIGH}$ = +125 °C for **HCC** device: +85 °C for **HCF** device.

The Noise Margin for both "1" and "0" level is: 1V min. with $V_{DD}$ = 5 V, 2 V min. with $V_{DD}$ = 10 V, 2.5 V min. with $V_{DD}$ = 15 V

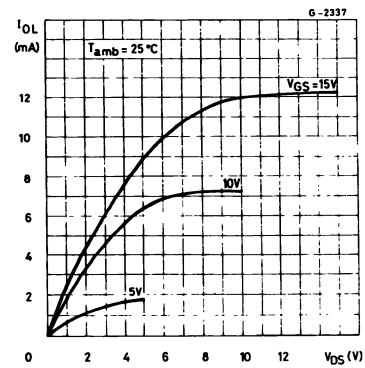
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 KΩ, typical temperature coefficent for all $V_{DD}$ values is 03 %/°C, all input rise and fall times= 20 ns)

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time | | 5 | | 250 | 500 | ns |
| | | | 10 | | 100 | 200 | |
| | | | 15 | | 75 | 150 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (Set or Reset) | | 5 | | 150 | 300 | ns |
| | | | 10 | | 75 | 150 | |
| | | | 15 | | 50 | 100 | |
| $t_{THL}$ $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $f_{CL}$ | Maximum Clock Input Frequency | | 5 | 3.5 | 7 | | MHz |
| | | | 10 | 8 | 16 | | |
| | | | 15 | 12 | 24 | | |
| $t_W$ | Clock Pulse Width | | 5 | 140 | 70 | | ns |
| | | | 10 | 60 | 30 | | |
| | | | 15 | 40 | 20 | | |
| $t_r$ $t_f$ | Clock Input Rise or Fall Time | | 5 | | | 15 | µs |
| | | | 10 | | | 5 | |
| | | | 15 | | | 5 | |
| $t_W$ | Set or Reset Pulse Width | | 5 | 200 | 100 | | ns |
| | | | 10 | 100 | 50 | | |
| | | | 15 | 50 | 25 | | |
| $t_{setup}$ | Data Setup Time | | 5 | 400 | 200 | | ns |
| | | | 10 | 160 | 80 | | |
| | | | 15 | 100 | 50 | | |

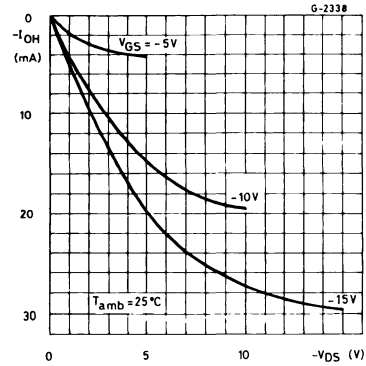
Typical Output Low (sink) Current Characteristics



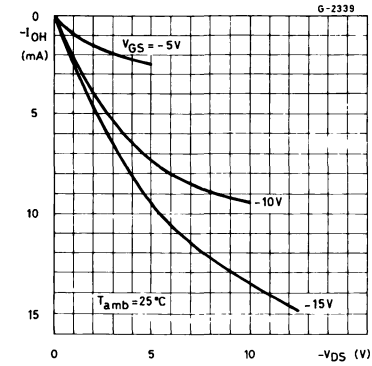

Minimum Output low (sink) Current Characteristics



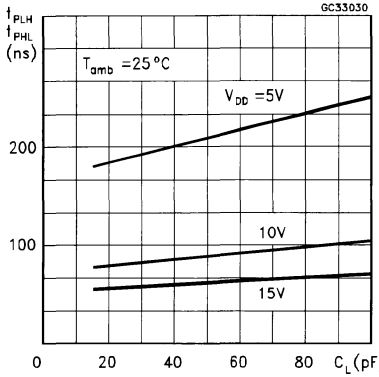
Typical Output High (source) Current Characteristics



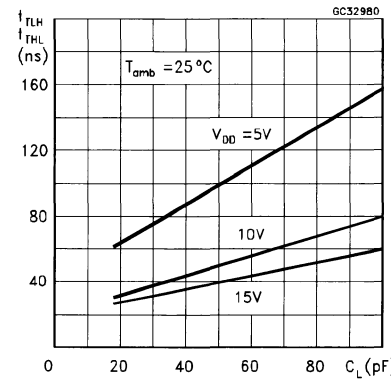

Minimum Output High (source) Current Characteristics



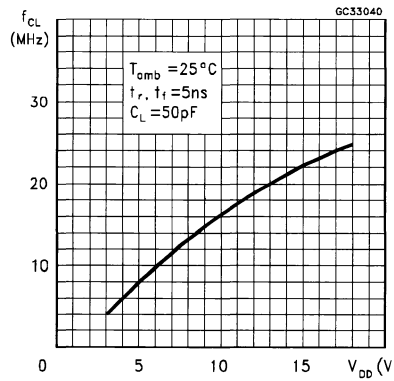

Typical Propagation Delay Time vs Load Capacitance



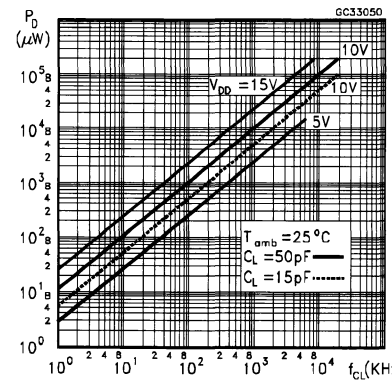

Typical Transition Time vs Load Capacitance




Typical Clock Frequency vs Supply Voltage (Toggle Mode)

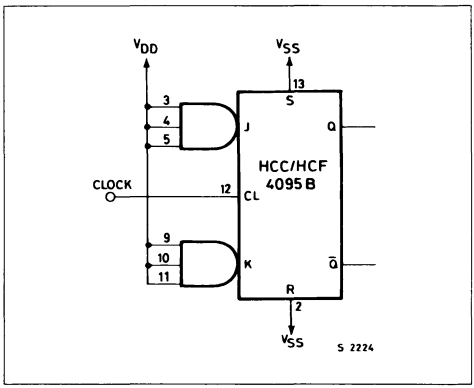



Typical Power Power Dissipation Vs. Input Clock Frequency

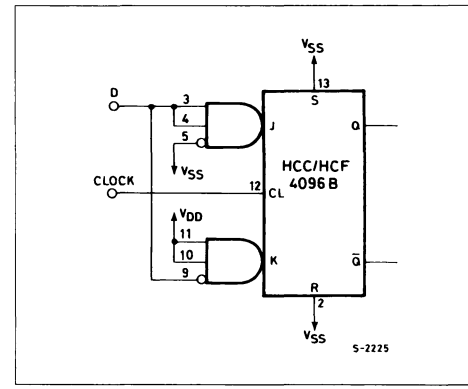


## TYPICAL APPLICATIONS

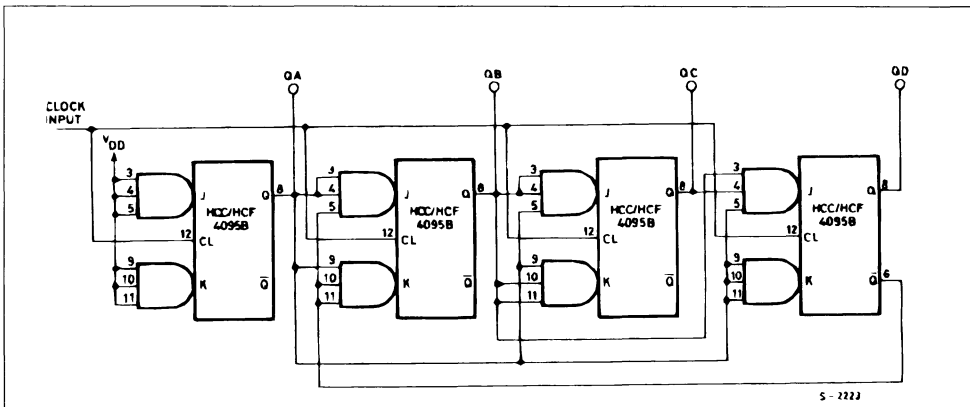
T-type Flip-Flop

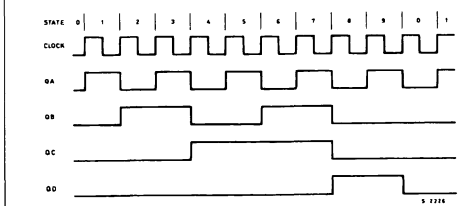



D-type Flip-Flop




Synchronous Binary Divide by Ten Counter



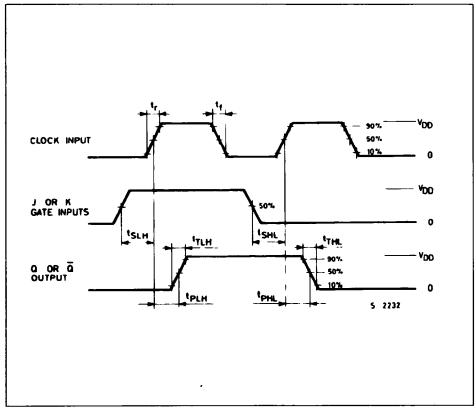




| STATE | QA | QB | QC | QD |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 1 | 1 | 0 | 0 |
| 4 | 0 | 0 | 1 | 0 |
| 5 | 1 | 0 | 1 | 0 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 | 0 |
| 8 | 0 | 0 | 0 | 1 |
| 9 | 1 | 0 | 0 | 1 |

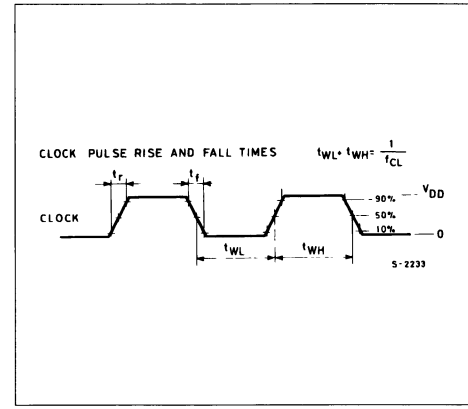
NOTE: In all 4095B units the Set and Reset are Connected to $V_{SS}$

## WAVEFORMS

Propagation Delay, Transition and Setup Time

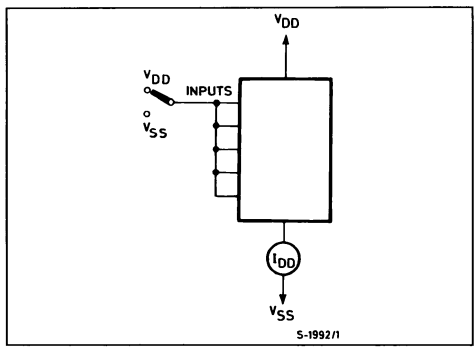



Clock Pulse Rise and Fall Time

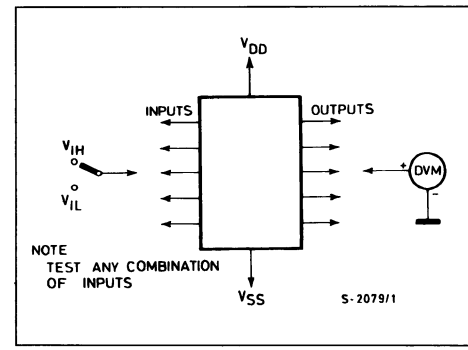



## TEST CIRCUITS

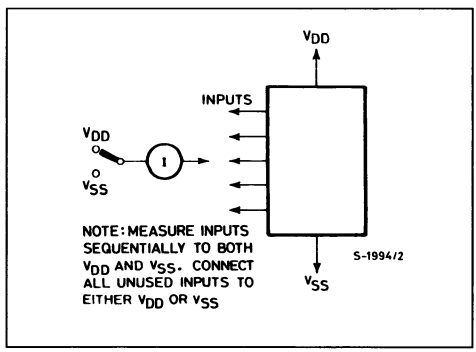
Quiescent Device Current.




Noise Immunity.



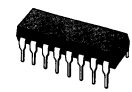

Input Leakage Current.



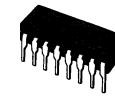
# HCC/HCF4098B

## DUAL MONOSTABLE MULTIVIBRATOR

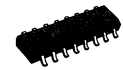
- RETRIGGERABLE/RESETTABLE CAPABILITY
- TRIGGER AND RESET PROPAGATION DELAYS INDEPENDENT OF $R_X$, $C_X$
- TRIGGERING FROM LEADING OR TRAILING EDGE
- Q AND $\overline{Q}$ BUFFERED OUTPUTS AVAILABLE
- SEPARATE RESETS
- WIDE RANGE OF OUTPUT-PULSE WIDTHS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)



**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

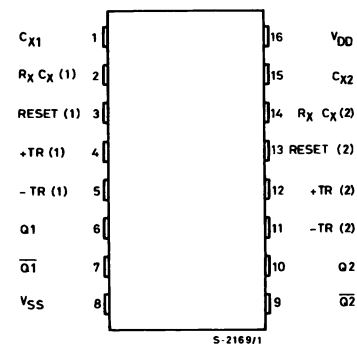
**ORDER CODES :**

| | |
|---|---|
| HCC4098BF | HCF4098BM1 |
| HCF4098BEY | HCF4098BC1 |

### DESCRIPTION

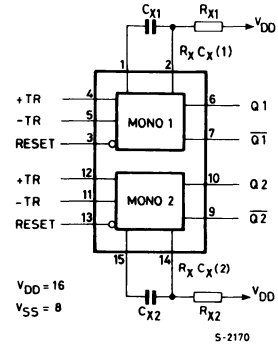
The **HCC4098B** (extended temperature range) and **HCF4098B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and plastic micropackage. The **HCC/HCF4098B** dual monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application. An external resistor ($R_X$) and an external capacitor ($C_X$) control the timing for the circuit. Adjustment of $R_X$ and $C_X$ provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of $R_X$ and $C_X$. Leading-edge-triggering (+ TR) and trailing-edge-triggering (– TR) inputs are provided for triggering from either edge of an input pulse. An unused + TR input should be tied to $V_{SS}$. An unused – TR input should be tied to $V_{DD}$. A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to $V_{DD}$. However, if an entire section of the **4098B** is not used, its RESET should be tied to $V_{SS}$. See table I. In normal operation the circuit triggers (ex-

**PIN CONNECTIONS**



tends the output pulse one period) on the application of each new trigger pulse. For operation in the non-triggerable mode, Q is connected to –TR when leading-edge triggering (+ TR) is used or Q is connected to + TR when trailing-edge triggering (– TR) is used. The time period (T) for this multivibrator can be approximated by $T_X = 1/2\ R_X C_X$ for $C_X \geq 0.01\ \mu F$. Time periods as a function of $R_X$ for values of $C_X$ and $V_{DD}$ are given in fig. 8. Values of T vary from unit to unit and as a function of voltage, temperature, and $R_X C_X$. The minimum value of external resistance, $R_X$, is 5 kΩ. The maximum value of external capacitance, $C_X$, is 100μF. Fig.9 shows time periods as a function of $C_X$ for values of $R_X$ and $V_{DD}$. The output pulse width has variations of ± 2.5 % typically, over the temperature range of – 55°C to 125° C for $C_X$ = 1000pF and $R_X$ = 100 kΩ. For power supply variations of ± 5%, the output pulse width has variations of ± 0.5% typically, for $V_{DD}$ = 10V and 15V and ± 1% typically, for $V_{DD}$ = 5 V at $C_X$ = 1000 pF and $R_X$ = 5kΩ.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | – 0.5 to + 20<br>– 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | – 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | – 55 to + 125<br>– 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | – 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability

* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | – 55 to + 125<br>– 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAMS

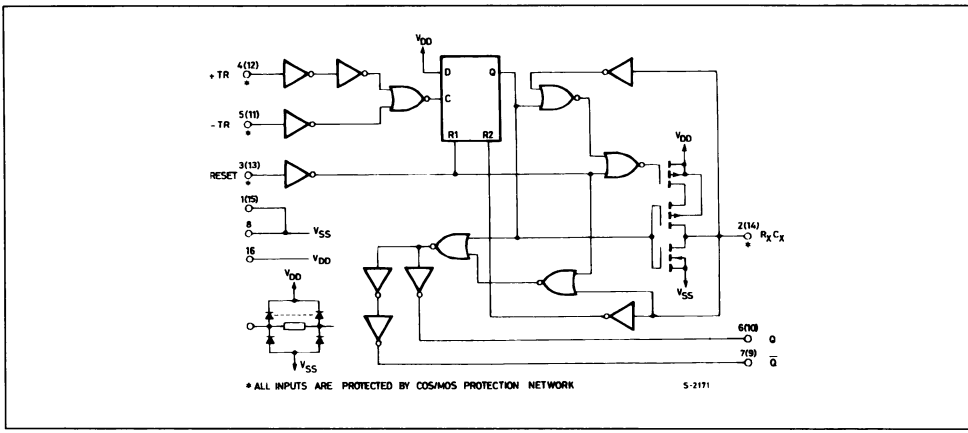
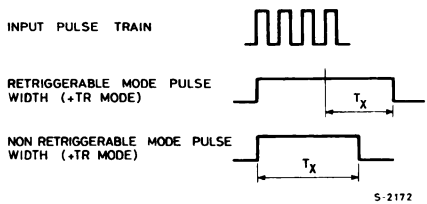



**Table 1 :** Functional Terminal Connections.

| Function | Terminal Connections | | | | | | Other Connections | |
|---|---|---|---|---|---|---|---|---|
| | to $V_{DD}$ | | to $V_{SS}$ | | Input Pulse to | | | |
| | Mono (1) | Mono (2) | Mono (1) | Mono (2) | Mono (1) | Mono (2) | Mono (1) | Mono (2) |
| Leading - Edge Trigger/Retriggerable | 3,5 | 11,13 | | | 4 | 12 | | |
| Leading - Edge Trigger/Non - retriggerable | 3 | 13 | | | 4 | 12 | 5,7 | 11,9 |
| Trailing - Edge Trigger/Retriggerable | 3 | 13 | 4 | 12 | 5 | 11 | | |
| Trailing - Edge Trigger/Non - retriggerable | 3 | 13 | | | 5 | 11 | 4,6 | 12,10 |
| Unused Section | 5 | 11 | 3,4 | 12,13 | | | | |

**Notes** : 1. A Refriggerable one-shot multivibrator has an output pulse width which is extended one full time period ($T_X$) after application of the last trigger pulse.
2 A non-refriggerable one-shot multivibrator has a time period $T_X$ referenced from the application of the first trigger pulse.



## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 1 | | 0.02 | 1 | | 30 | μA |
| | | | 0/10 | | | 10 | | 2 | | 0.02 | 2 | | 60 | |
| | | | 0/15 | | | 15 | | 4 | | 0.02 | 4 | | 120 | |
| | | | 0/20 | | | 20 | | 20 | | 0.04 | 20 | | 600 | |
| | | HCF Types | 0/ 5 | | | 5 | | 4 | | 0.02 | 4 | | 30 | |
| | | | 0/10 | | | 10 | | 8 | | 0.02 | 8 | | 60 | |
| | | | 0/15 | | | 15 | | 16 | | 0.02 | 16 | | 120 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device · + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5 V min. with $V_{DD}$ = 15V.

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall times = 20ns)

| Symbol | Parameter | Test Conditions | | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | $R_X$ (kΩ) | $C_X$ (pF) | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Trigger Propagation Delay Time (+ TR, – TR to Q, $\overline{Q}$) | 5 to 10.000 | ≥ 15 | 5 | | 250 | 500 | ns |
| | | | | 10 | | 125 | 250 | |
| | | | | 15 | | 100 | 200 | |
| $t_{WH}$, $t_{WL}$ | Trigger Pulse Width | 5 to 10.000 | ≥ 15 | 5 | 140 | 70 | | ns |
| | | | | 10 | 60 | 30 | | |
| | | | | 15 | 40 | 20 | | |
| $t_{TLH}$ | Transition Time | 5 to 10.000 | ≥ 15 | 5 | | 100 | 200 | ns |
| | | | | 10 | | 50 | 100 | |
| | | | | 15 | | 40 | 80 | |
| $t_{THL}$ | Transition Time | 5 to 10.000 | 15 to 10.000 | 5 | | 100 | 200 | |
| | | | | 10 | | 50 | 100 | |
| | | | | 15 | | 40 | 80 | |
| | | 5 to 10.000 | 0.01µF to 0.1µF | 5 | | 150 | 300 | |
| | | | | 10 | | 75 | 150 | |
| | | | | 15 | | 65 | 130 | |
| | | 5 to 10.000 | 0.1µF to 1µF | 5 | | 250 | 500 | |
| | | | | 10 | | 150 | 300 | |
| | | | | 15 | | 80 | 160 | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time (reset) | 5 to 10.000 | ≥ 15 | 5 | | 225 | 450 | ns |
| | | | | 10 | | 125 | 250 | |
| | | | | 15 | | 75 | 150 | |
| $t_WR$ | Pulse Width (reset) | 100 | 15 | 5 | 200 | 100 | | ns |
| | | | | 10 | 80 | 40 | | |
| | | | | 15 | 60 | 30 | | |
| | | | 1000 | 5 | 1200 | 600 | | |
| | | | | 10 | 600 | 300 | | |
| | | | | 15 | 500 | 250 | | |
| | | | 0.1µF | 5 | 50 | 250 | | µs |
| | | | | 10 | 30 | 15 | | |
| | | | | 15 | 20 | 10 | | |
| $t_r$, $t_f$ (TR) | Rise or Fall Time (trigger) | | 5 to 15 | | | | 100 | µs |
| | Pulse Width Match Between Circuits in Same Package | 10 | 10.000 | 5 | | 5 | 10 | % |
| | | | | 10 | | 7.5 | 15 | |
| | | | | 15 | | 7.5 | 15 | |

**Figure 2** : Typical Output Low (sink) Current Characteristics.

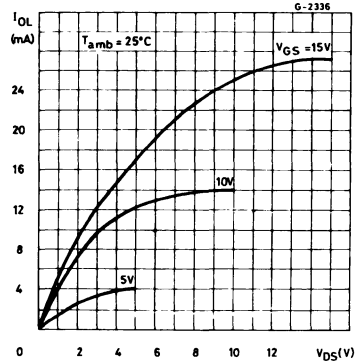



**Figure 3** : Minimum Output Low (sink) Current Characteristics.

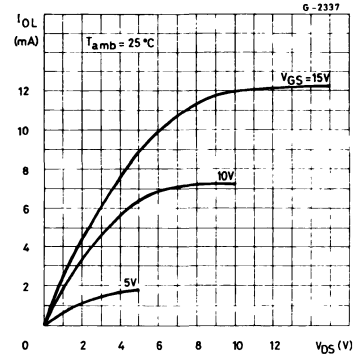



**Figure 4** : Typical Output High (source) Current Characteristics.

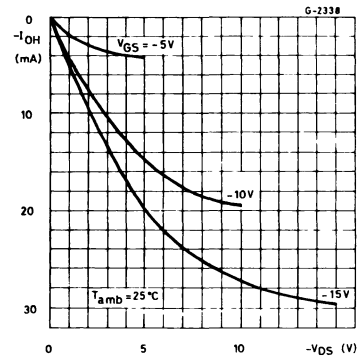



**Figure 5** : Minimum Output High (source) Current Characteristics.

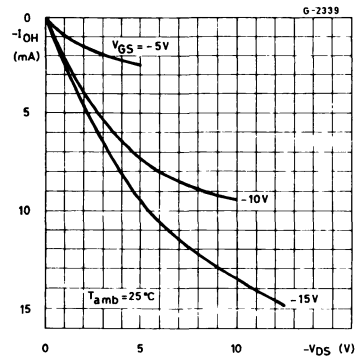



**Figure 6** : Typical Propagation Delay Times vs. Load Capacitance, Trigger in to Q out. (All values of $C_X$ and $R_X$).

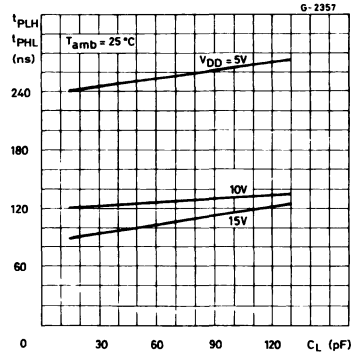



**Figure 7** : Transition Time vs. Load Capacitance for $R_X$ = 5kΩ, 10000 kΩ and $C_X$ = 15pF, 10000pF.

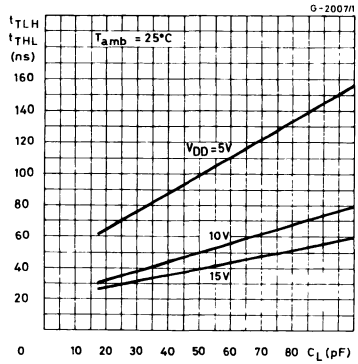


**Figure 8** : Typical External Resistance vs. Pulse Width at Various $V_{DD}$ and $C_X$.

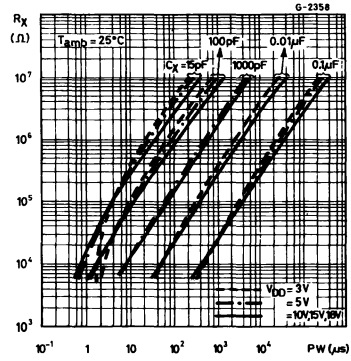



**Figure 9** : Typical External Capacitance vs.Pulse Width at Various $V_{DD}$ and $R_X$.

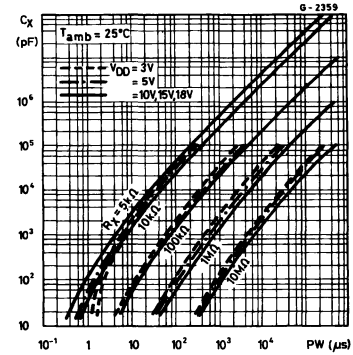



**Figure 10** : Typical Minimum Reset Pulse Width vs. External Capacitance.

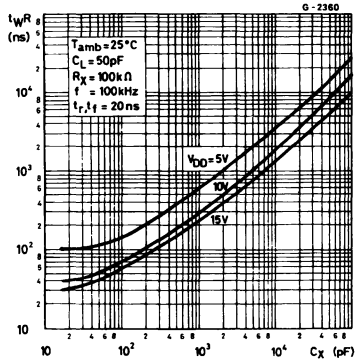
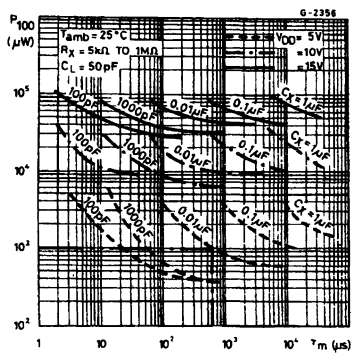



**Figure 11** : Average Power Dissipation for 100% Duty Cycle vs. One-shot Pulse width.




To calculate average power dissipation (P) for less than 100% duty cycle :

$P_{100}$ = average power for 100% duty cycle

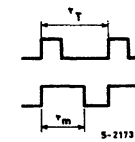
$$P = \left(\frac{\tau_m}{\tau_T}\right) P_{100}$$ where $\tau_m$ = one-shot pulse width

$\tau_T$ = trigger pulse period

e.g. : For tm = 600ms tT = 1000ms,
CX = 0.01μF, $V_{DD}$ = 5V

$$P = \left(\frac{600}{1000}\right) 103\mu W = 600\mu W$$

(see dotted line on graph)



## TEST CIRCUITS

**Figure 12** : Quiescent -Device Current.

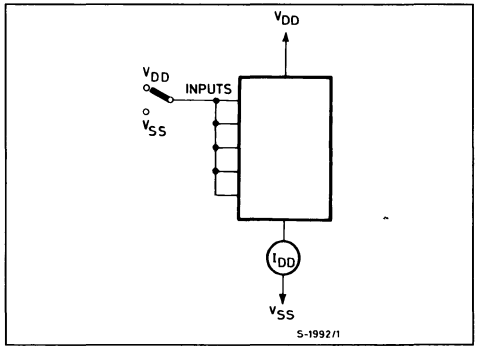



**Figure 13** : Input-Voltage.

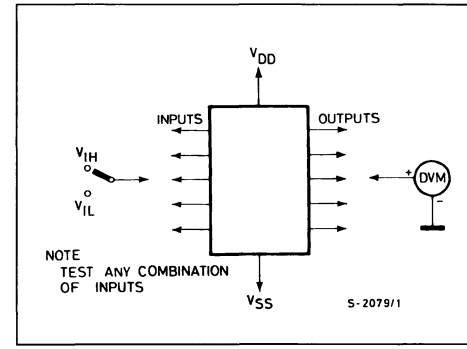
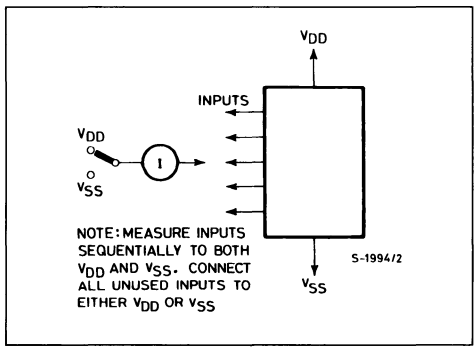
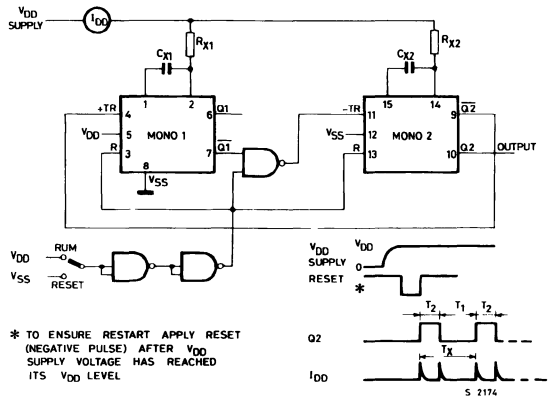



**Figure 14** : Input Leakage.



## TYPICAL APPLICATIONS

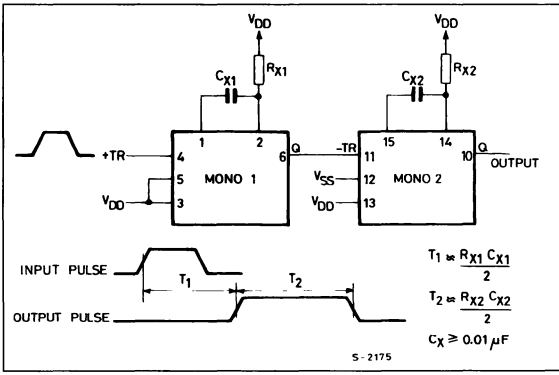
**Figure 15** : Astable Multivibrator with Restart after Reset Capability.




| $R_X$ | $I_{DD}$(Avg) | $T_X$ ($T_1 + T_2$) | $V_{DD}$ |
|---|---|---|---|
| 10kΩ | 1mA ↓ 0.05mA | 3.8µs ↓ 0.5s | 5V |
| | 2.5mA ↓ 0.5mA | 3.2µs ↓ 0.5s | 10V |
| 10MΩ | 5mA ↓ 1mA | 3µs ↓ 0.5s | 15V |

**Notes** All values are typical
$C_X$ range 0.0001µF to 0.1µF.

**Figure 16** : Pulse Delay.

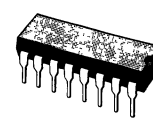


SGS-THOMSON MICROELECTRONICS

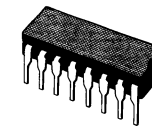
# HCC/HCF4099B

## 8-BIT ADDRESSABLE LATCH

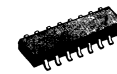
- SERIAL DATA INPUT - ACTIVE PARALLEL OUTPUT
- STORAGE REGISTER CAPABILITY - MASTER CLEAR
- CAN FUNCTION AS DEMULTIPLEXER
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
Plastic Package



**F**
Ceramic Frit Seal Package



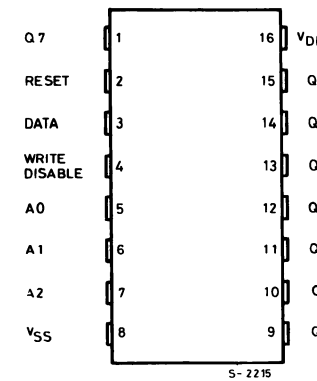
**M1**
Micro Package

**C1**
Plastic Chip Carrier

**ORDER CODES** :

| | |
|---|---|
| HCC4099BF | HCF4099BM1 |
| HCF4099BEY | HCF4099BC1 |

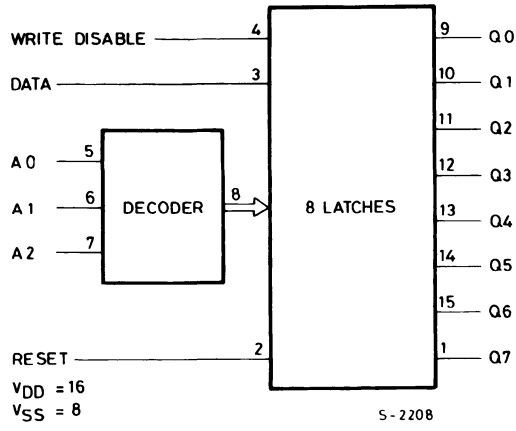
**PIN CONNECTIONS**




### DESCRIPTION

The **HCC4099B** (extended temperature range) and **HCF4099B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and plastic micro package. The HCC/HCF4099B 8-bit addressable latch is a serial-input, parallel-output storage register that can perform a variety of functions. Data are inputted to a particular bit in the latch when that bit is addressed (by means of inputs A0, A1, A2) and when WRITE DISABLE is at a low level. When WRITE DISABLE is high, data entry is inhibited ; however, all 8 outputs can be continuously read independent of WRITE DISABLE and address inputs. A master RESET input is available, which resets all bits to a logic "0" level when RESET and WRITE DISABLE are at a high level. When RESET is at a high level, and WRITE DISABLE is at a low level, the latch acts as a 1-of-8 demultiplexer ; the bit that is addressed has an active output which follows the data input, while all unaddressed bits are held to a logic "0" level.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage . **HCC** Types<br>**HCF** Types | − 0 5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0 5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature · **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

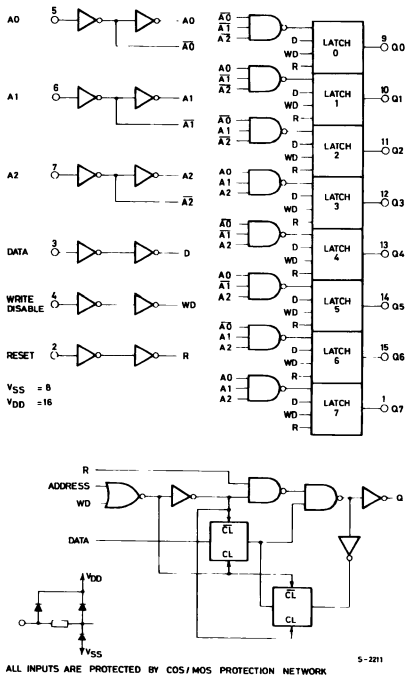
Stresses above listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage · **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAM

1 of 8 latches

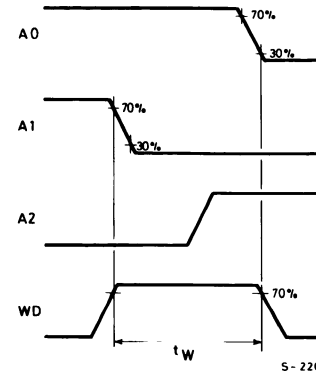






ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

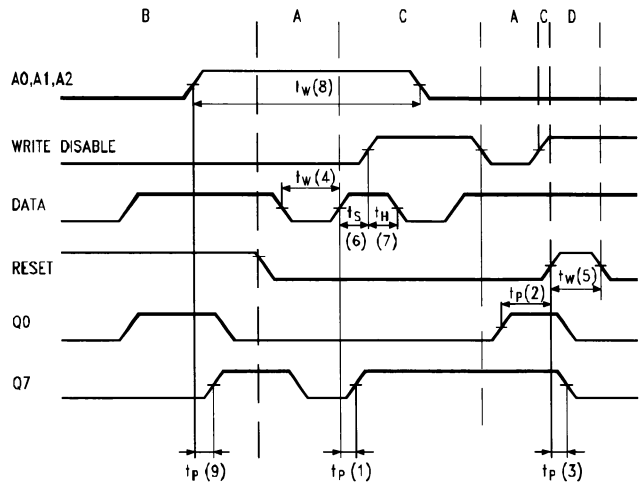
Definition of WRITE DIABLE ON Time




| Types | Mode Selection | | | |
|---|---|---|---|---|
| | WD | R | Addressed Latch | Unaddressed Latch |
| A | 0 | 0 | Follows Data | Holds Previous State |
| B | 0 | 1 | Follows Data (active high 8-channel demultiplexer) | Reset to "0" |
| C | 1 | 0 | Holds Previous State | |
| D | 1 | 1 | Reset to "0" | Reset to "0" |

WD = WRITE DISABLE R = RESET

Master Timing Diagram



## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

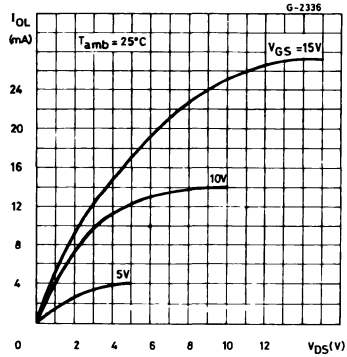
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0 05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0 44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0 3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for HCC device − 40°C for HCF device
* $T_{HIGH}$ = + 125°C for HCC device + 85°C for HCF device.
The Noise Margin for both "1" and "0" level is 1V min with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2 5V min with $V_{DD}$ = 15V,

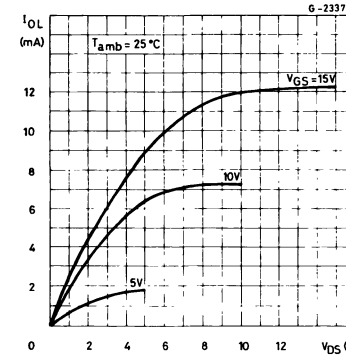
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall times = 20ns)

| Symbol | Parameter | | Test Conditions (see master timing diagram) | $V_{DD}$ (V) | Value Min. | Value Typ. | Value Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time | Data to Output | (1) | 5 | | 200 | 400 | ns |
| | | | | 10 | | 75 | 150 | |
| | | | | 15 | | 50 | 100 | |
| | | Write Disable to Output | (2) | 5 | | 200 | 400 | |
| | | | | 10 | | 80 | 160 | |
| | | | | 15 | | 60 | 120 | |
| | | Address to Output | (9) | 5 | | 225 | 450 | |
| | | | | 10 | | 100 | 200 | |
| | | | | 15 | | 75 | 150 | |
| $t_{PHL}$ | Propagation Delay Time | Reset to Output | (3) | 5 | | 175 | 350 | |
| | | | | 10 | | 80 | 160 | |
| | | | | 15 | | 65 | 130 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | Any Output | | 5 | | 100 | 200 | ns |
| | | | | 10 | | 50 | 100 | |
| | | | | 15 | | 40 | 80 | |
| $t_W$ | Pulse Width | Data | (4) | 5 | 200 | 100 | | ns |
| | | | | 10 | 100 | 50 | | |
| | | | | 15 | 80 | 40 | | |
| | | Address | (8) | 5 | 400 | 200 | | |
| | | | | 10 | 200 | 100 | | |
| | | | | 15 | 125 | 65 | | |
| | | Reset | (5) | 5 | 150 | 75 | | |
| | | | | 10 | 75 | 40 | | |
| | | | | 15 | 50 | 25 | | |
| $t_{setup}$ | Setup Time | Data to Write Disable | (6) | 5 | 100 | 50 | | ns |
| | | | | 10 | 50 | 25 | | |
| | | | | 15 | 35 | 20 | | |
| $t_{hold}$ | Hold Time | Data to Write Disable | (7) | 5 | 150 | 75 | | ns |
| | | | | 10 | 75 | 40 | | |
| | | | | 15 | 50 | 25 | | |

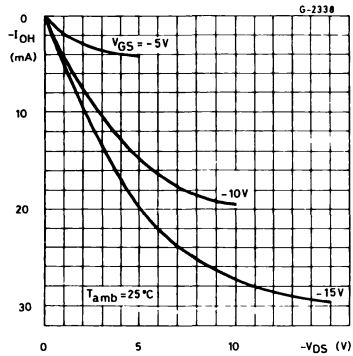
Typical Output Low (sink) Current Characteristics.



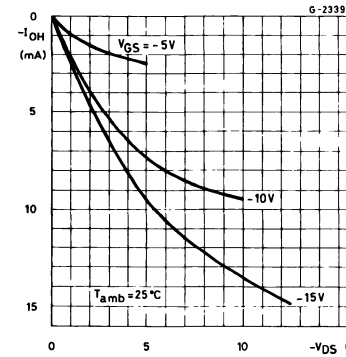

Minimum Output Low (sink) Current Characteristics.



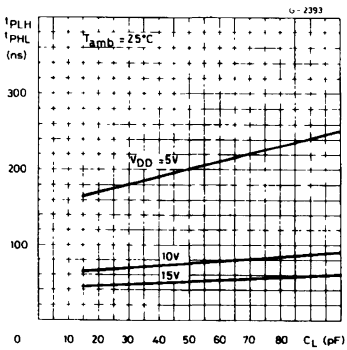

Typical Output High (source) Current Characteristics.



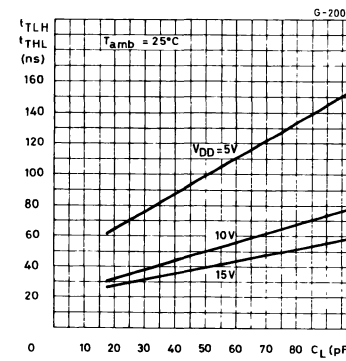

Minimum Output High (source) Current Characteristics.



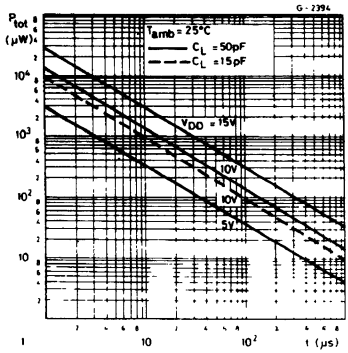

Typical Propagation Delay Time (data to Qn) vs. Load Capacitance.




Typical Transition Time vs. Load Capacitance.

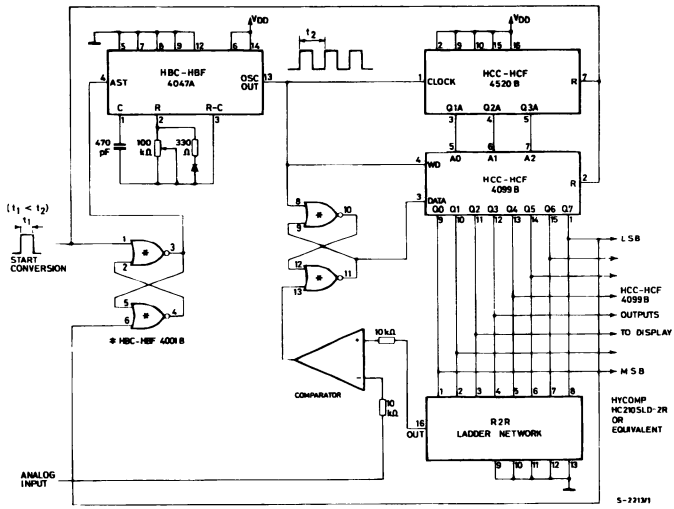


Typical Dynamic power Dissipation vs. Address Cycle Time.



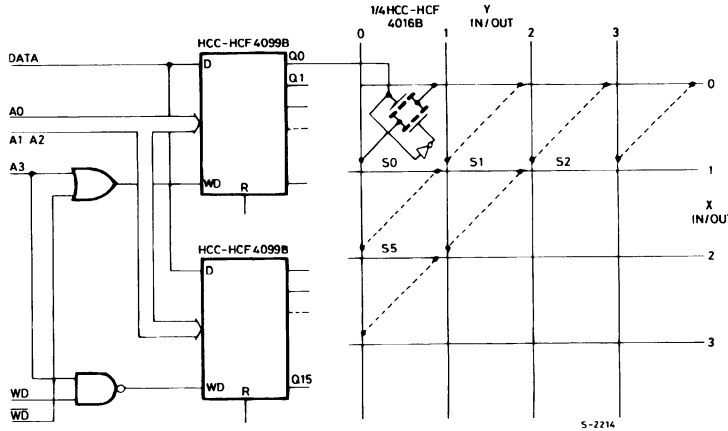

## TYPICAL APPLICATIONS

A/D Converter

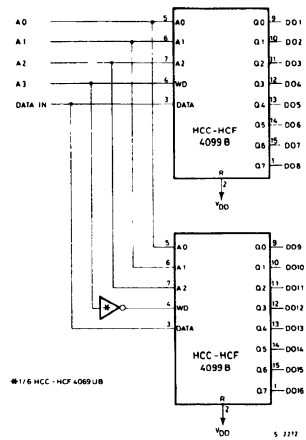


## TYPICAL APPLICATIONS

Multiple Selection Decoding – 4x4 Crosspoint Switch

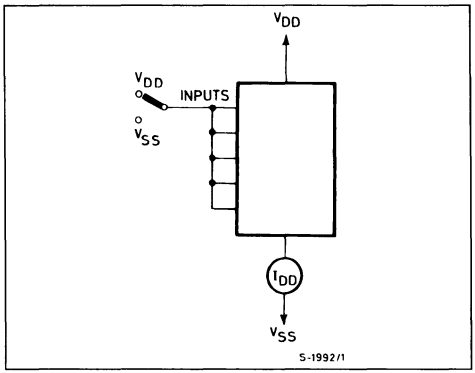



1 of 16 Decoder/demultiplexer

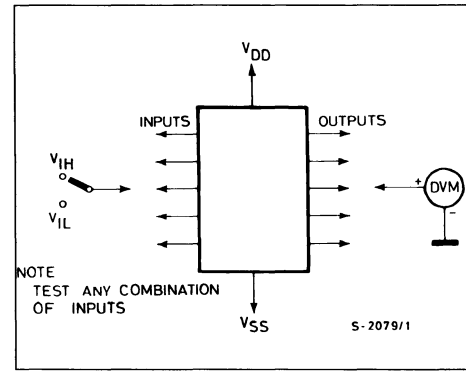


## TEST CIRCUITS

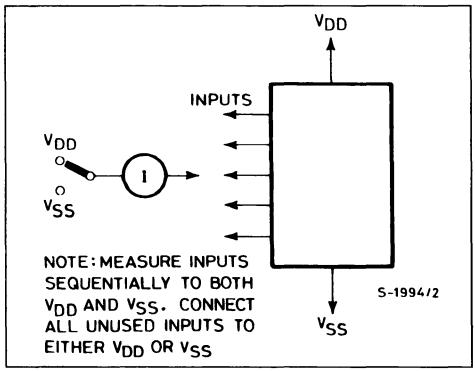
Quiescent Device Current.




Input Voltage.



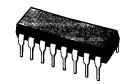

Input Current.



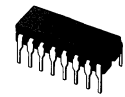
# HCC/HCF4502B

## STROBED HEX INVERTER/BUFFER

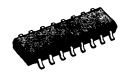
- 2 TTL-LOAD OUTPUT DRIVE CAPABILITY
- 3-STATE OUTPUTS
- COMMON OUTPUT-DISABLE CONTROL
- INHIBIT CONTROL
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)



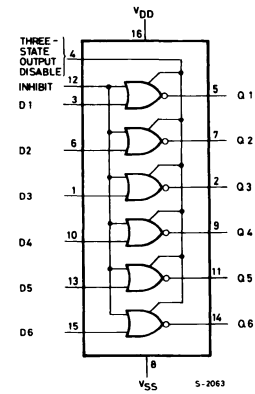
**M1**
Micro Package

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4502BF HCF4502BM1
HCF4502BEY HCF4502BC1

### PIN CONNECTIONS




### DESCRIPTION

The **HCC4502B** (extended temperature range) and **HCF4502B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF 4502B** consists of six inverter-buffers with 3-state outputs. A logic "1" on the OUTPUT DISABLE input produces a high-impedance state in all six outputs. This feature permits common busing of the outputs, thus simplifying system design. A logic "1" on the INHIBIT input switches all six outputs to logic "0" if the OUTPUT DISABLE input is a logic "0". This device is capable of driving two standard TTL loads, which is equivalent to six times the JEDEC "B" series $I_{OL}$ standard.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage . **HCC** Types<br>**HCF** Types | − 0 5 to + 20<br>− 0 5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0 5 to $V_{DD}$ + 0 5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for external periods may affect device reliability

* All voltage values are referred to $V_{SS}$ pin voltage

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to + 18<br>3 to + 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature · **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## TRUTH TABLE

| Disable | Inhibit | Dn | Qn |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | I | 0 |
| 0 | I | X | 0 |
| I | X | X | Z |

X = don't care
Z = high impedance
Logic 1 = high
Logic 0 = low

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

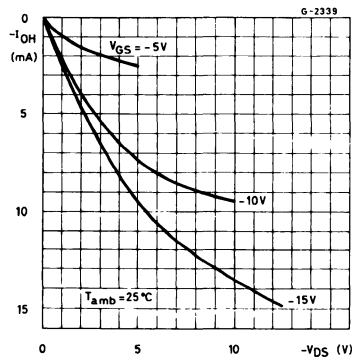
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 1 | | 0.02 | 1 | | 30 | μA |
| | | | 0/10 | | | 10 | | 2 | | 0.02 | 2 | | 60 | |
| | | | 0/15 | | | 15 | | 4 | | 0.02 | 4 | | 120 | |
| | | | 0/20 | | | 20 | | 20 | | 0.04 | 20 | | 600 | |
| | | HCF Types | 0/ 5 | | | 5 | | 4 | | 0.02 | 4 | | 30 | |
| | | | 0/10 | | | 10 | | 8 | | 0.02 | 8 | | 60 | |
| | | | 0/15 | | | 15 | | 16 | | 0.02 | 16 | | 120 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14 95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3 2 | | −1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | −0.64 | | −0.51 | − 1 | | −0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13 5 | | 15 | − 4.2 | | − 3 4 | − 6 8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | −1.53 | | −1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | −0.52 | | −0.44 | − 1 | | −0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1 3 | | − 1 1 | − 2 6 | | − 0 9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 3.84 | | 3.06 | 6 | | 2.10 | | mA |
| | | | 0/10 | 0.5 | | 10 | 9.6 | | 7.8 | 15.6 | | 5.4 | | |
| | | | 0/15 | 1.5 | | 15 | 25.2 | | 20.4 | 40.8 | | 14.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 3.11 | | 2.6 | 6 | | 2.10 | | |
| | | | 0/10 | 0.5 | | 10 | 7 05 | | 6 63 | 15 6 | | 5.61 | | |
| | | | 0/15 | 1.5 | | 15 | 20.4 | | 17.3 | 40.8 | | 14.2 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0 1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0 3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $I_{OH}$, $I_{OL}$ | 3-state Output | HCC Types | 0/18 | | | 18 | | ± 0.4 | | $\pm 10^{-4}$ | ± 0 4 | | ± 12 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 1.0 | | $\pm 10^{-4}$ | ± 1.0 | | ± 7.5 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$= − 55°C for **HCC** device − 40°C for **HCF** device
* $T_{High}$= + 125°C for **HCC** device + 85°C for **HCF** device
The Noise Margin for both "1" and "0" level is 1V min with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2 5 V min with $V_{DD}$ = 15V

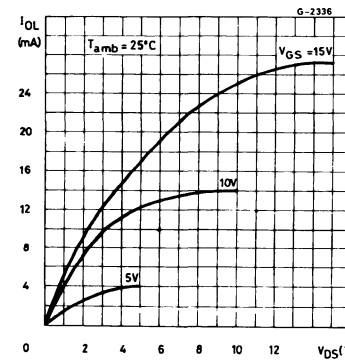
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 kΩ typical temperature coefficient for all $V_{DD}$ values is 0.3 %/°C, all input rise and fall times = 20 ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$ | Data or Inhibit Delay Time | | 5 | | 135 | 270 | ns |
| | | | 10 | | 60 | 120 | |
| | | | 15 | | 40 | 80 | |
| $t_{PLH}$ | Data or Inhibit Delay Time | | 5 | | 190 | 380 | ns |
| | | | 10 | | 90 | 180 | |
| | | | 15 | | 65 | 30 | |
| $t_{PHZ}$ | Disable Delay Time (output high to high impedance) | | 5 | | 60 | 120 | ns |
| | | | 10 | | 40 | 80 | |
| | | | 15 | | 30 | 60 | |
| $t_{PZH}$ | Disable Delay Time (high impedance to output high) | | 5 | | 110 | 220 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_{PLZ}$ | Disable Delay Time (output low to high impedance) | | 5 | | 125 | 250 | ns |
| | | | 10 | | 65 | 130 | |
| | | | 15 | | 55 | 110 | |
| $t_{PZL}$ | Disable Delay Time (high impedance to output low) | | 5 | | 125 | 250 | ns |
| | | | 10 | | 55 | 110 | |
| | | | 15 | | 40 | 80 | |
| $t_{TLH}$ | Tansition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_{THL}$ | Transition Time | | 5 | | 60 | 120 | ns |
| | | | 10 | | 30 | 60 | |
| | | | 15 | | 20 | 40 | |

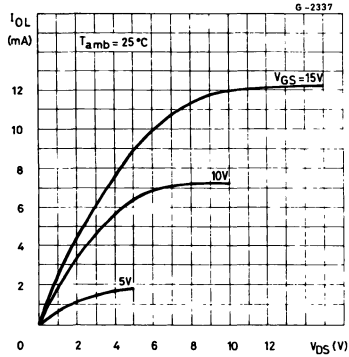
Minimum Output High (source) Current Characteristics.



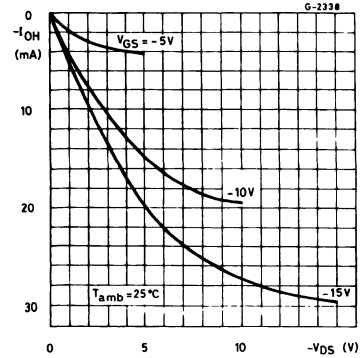

Typical Output Low (sink) Current.



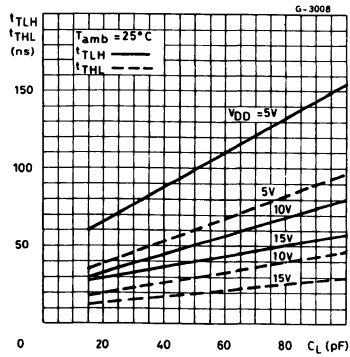
Minimum Output Low (sink) Current Characteristics.



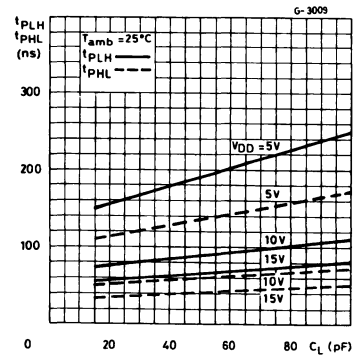

Typical Output High (source) Current Characteristics.




Typical Transition Time vs. Load Capacitance.

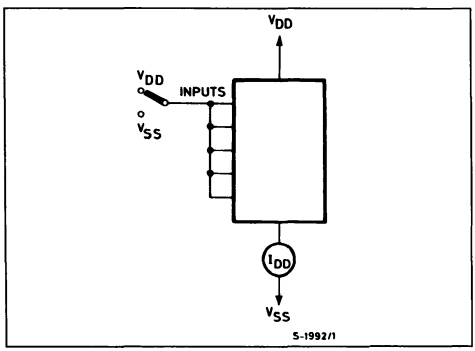



Typical Propagation Delay Time vs. Load Capacitance.

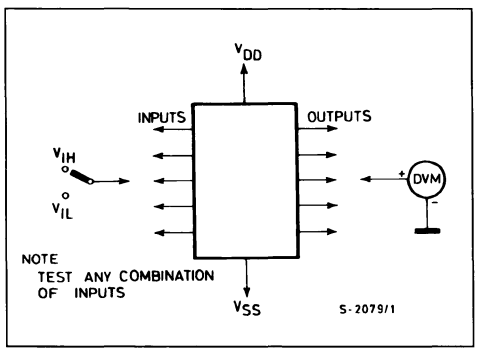



## TEST CIRCUIT

Quiescent Device Current.

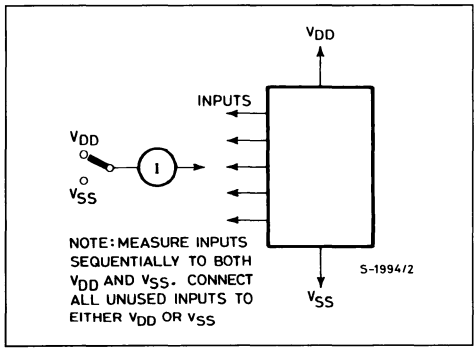



Input Voltage.



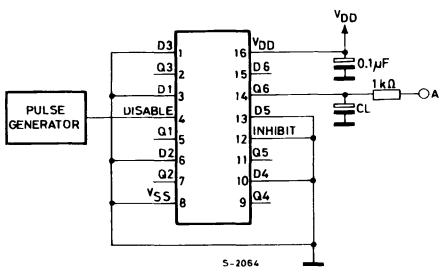
## TEST CIRCUIT (continued)

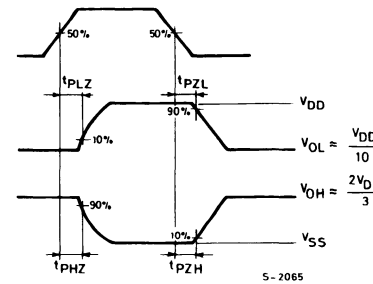
Input Leakage Current.




## TEST CIRCUIT AND WAVEFORMS

Disable Delay Time.



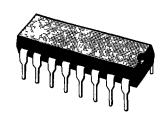

| Test Conditions | | |
|---|---|---|
| **Test** | **Pin 15** | **Point A** |
| $t_{PHZ}$ | $V_{SS}$ | $V_{SS}$ |
| $t_{PLZ}$ | $V_{DD}$ | $V_{DD}$ |
| $t_{PZL}$ | $V_{DD}$ | $V_{DD}$ |
| $t_{PZH}$ | $V_{SS}$ | $V_{SS}$ |

SGS-THOMSON
MICROELECTRONICS

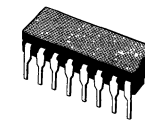
# HCC4503B
# HCF4503B

## HEX BUFFER

- 1 TTL-LOAD OUTPUT DRIVE CAPABILITY
- 2 OUTPUT-DISABLE CONTROLS
- 3 STATE OUTPUTS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Package)

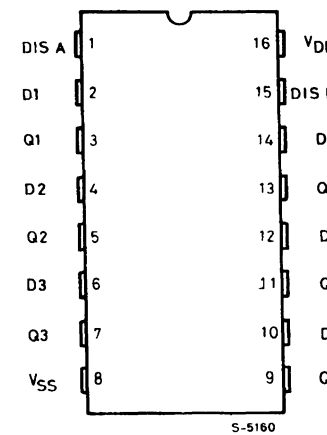
**M1**
(Micro Package)

**C1**
(Chip Carrier)

**ORDER CODES :**

HCC4503BF HCF4503BM1
HCF4503BEY HCF4503BC1

**PIN CONNECTIONS**

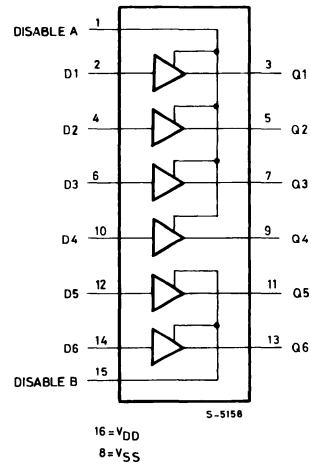



### DESCRIPTION

The **HCC4503B** (extended temperature range) and **HCF4503B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package, and plastic micro package.

The **HCC/HCF4503B** is a hex noninverting buffer with 3-state outputs having high sink and source-current capability. Two disable controls are provided, one of which controls four buffers and the other controls the remaining two buffers.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ * | Supply Voltage. **HCC** Types<br>**HCF** Types | -0.5 to +20<br>-0 5 to +18 | V<br>V |
| $V_I$ | Input Voltage | -0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for Top = Full Package Temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |

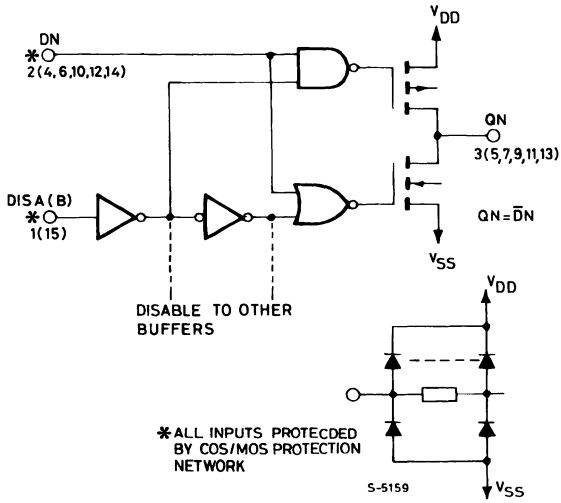
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for external periods may affect device reliability

* All voltage values are referred to $V_{SS}$ pin voltage

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage· **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature· **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |

## LOGIC DIAGRAM AND TRUTH TABLE




| DN | DIS A (B) | QN |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| X | 1 | High Z |

X = Don't care

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditios $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{LOW}$ * Min. | $T_{LOW}$ * Max. | 25 °C Min. | 25 °C Typ. | 25 °C Max. | $T_{HIGH}$ * Min. | $T_{HIGH}$ * Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/5 | | | 5 | | 1 | | 0 02 | 1 | | 30 | μA |
| | | | 0/10 | | | 10 | | 2 | | 0 02 | 2 | | 60 | |
| | | | 0/15 | | | 15 | | 4 | | 0 02 | 4 | | 120 | |
| | | | 0/20 | | | 20 | | 20 | | 0 04 | 20 | | 600 | |
| | | HCF Types | 0/5 | | | 5 | | 4 | | 0.02 | 4 | | 30 | |
| | | | 0/10 | | | 10 | | 8 | | 0 02 | 8 | | 60 | |
| | | | 0/15 | | | 15 | | 16 | | 0.02 | 16 | | 120 | |
| $V_{OH}$ | Output High Voltage | | 0/5 | | < 1 | 5 | 4 95 | | 4 95 | | | 4 95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14 95 | | 14 95 | | | 14 95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0 05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0 05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0 5/4 5 | < 1 | 5 | 3.5 | | 3 5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1 5 | | 1 5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/5 | 2.5 | | 5 | -5 8 | | -4.8 | -6 1 | | -3 | | mA |
| | | | 0/5 | 4.6 | | 5 | -1 2 | | -1 02 | -1 9 | | -0 7 | | |
| | | | 0/10 | 9.5 | | 10 | -3.1 | | -2.6 | -3.7 | | -1.8 | | |
| | | | 0/15 | 13 5 | | 15 | -8.2 | | -6 8 | -14.1 | | -4 8 | | |
| | | HCF Types | 0/5 | 2.5 | | 5 | -4.8 | | -4.1 | -5.2 | | -2 9 | | |
| | | | 0/5 | 4 6 | | 5 | -1 | | -0 8 | -1.6 | | -0 6 | | |
| | | | 0/10 | 9 5 | | 10 | -2.5 | | -2.2 | -3.1 | | -1 6 | | |
| | | | 0/15 | 13 5 | | 15 | -6 8 | | -5 8 | -11 9 | | -4.2 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/5 | 0.4 | | 5 | 2.6 | | 2.1 | 2 3 | | 1 3 | | mA |
| | | | 0/10 | 0 5 | | 10 | 6 5 | | 5 5 | 2 6 | | 3.8 | | |
| | | | 0/15 | 1 5 | | 15 | 19 2 | | 16 1 | 23 | | 11 2 | | |
| | | HCF Types | 0/5 | 0 4 | | 5 | 2 1 | | 1.8 | 1 9 | | 1 2 | | |
| | | | 0/10 | 0 5 | | 10 | 5 4 | | 4.7 | 5 3 | | 3 3 | | |
| | | | 0/15 | 1 5 | | 15 | 16 | | 13.7 | 19 5 | | 9 7 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | | 0/18 | Any Input | | 18 | | ±0.1 | | $±10^{-5}$ | ±0 1 | | ±1 | μA |
| | | | 0/15 | | | 15 | | ±0.3 | | $±10^{-5}$ | ±0 3 | | ±1 | |
| $I_{OH}$ | Input Leakage Current | | 0/18 | Any Input | | 18 | | ±0 4 | | $±10^{-4}$ | ±0 4 | | ±12 | μA |
| | | | 0/15 | | | 15 | | ±1.0 | | $±10^{-4}$ | ±1 0 | | ±7.5 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7 5 | | | pF |

* $T_{LOW}$ = -55 °C for **HCC** device -40 °C for **HCF** device

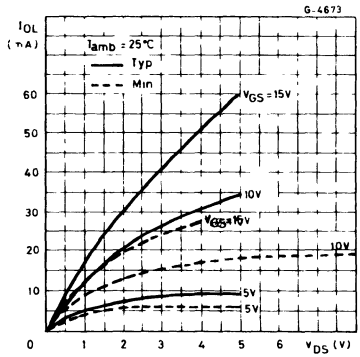
* $T_{HIGH}$ = +125 °C for **HCC** device +85 °C for **HCF** device

The Noise Margin for both "1" and "0" level is 1V min with $V_{DD}$ = 5 V, 2 V min. with $V_{DD}$ = 10 V, 2 5 V min with $V_{DD}$ = 15 V

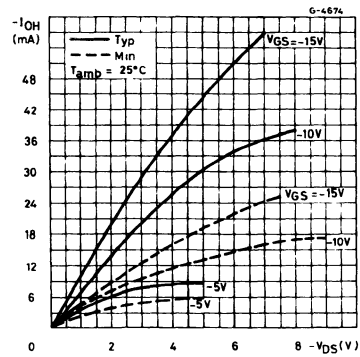
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 KΩ, typical temperature coefficent for all $V_{DD}$ values is 03 %/°C, all input rise and fall times= 20 ns)

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$ | Propagation Delay Time | 5 | | 75 | 150 | ns |
| | | 10 | | 35 | 70 | |
| | | 15 | | 25 | 50 | |
| $t_{PHL}$ | Propagation Delay Time | 5 | | 55 | 110 | ns |
| | | 10 | | 25 | 50 | |
| | | 15 | | 17 | 35 | |
| $t_{PHZ}$ $t_{PZH}$ | 3-State Propagation Delay Time | 5 | | 70 | 140 | ns |
| | | 10 | | 30 | 60 | |
| | | 15 | | 25 | 50 | |
| $t_{PZL}$ $t_{PLZ}$ | 3-State Propagation Delay Time | 5 | | 90 | 180 | ns |
| | | 10 | | 40 | 80 | |
| | | 15 | | 35 | 70 | |
| $t_{TLH}$ | Transition Time | 5 | | 50 | 90 | ns |
| | | 10 | | 30 | 45 | |
| | | 15 | | 25 | 35 | |
| $t_{THL}$ | Transition Time | 5 | | 35 | 70 | ns |
| | | 10 | | 20 | 40 | |
| | | 15 | | 13 | 25 | |

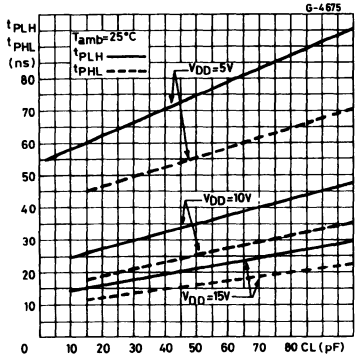
N-Channel Output Low (sink) Current Characteristics.



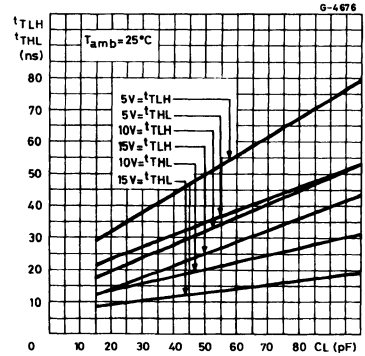

P-Channel Output High (source) Current Characteristics.



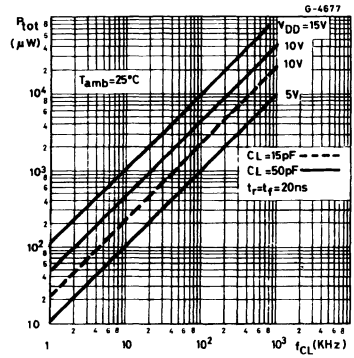
Typical Propagation Delay Time vs. Load Capacitance.




Typical Transition Time vs. Load Capacitance.

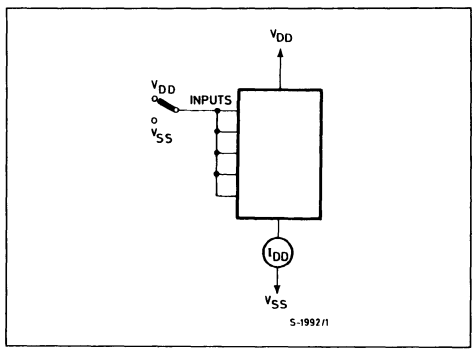



Typical Dynamic Power Dissipation vs. Frequency.

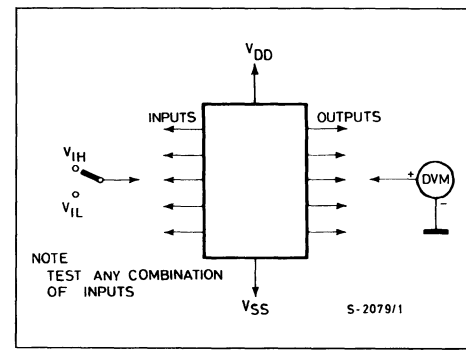



## TEST CIRCUITS

Quiescent Device Current.

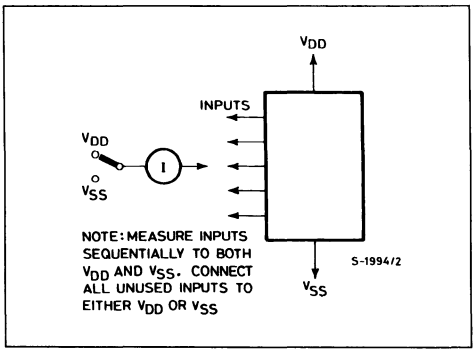



Input Voltage.

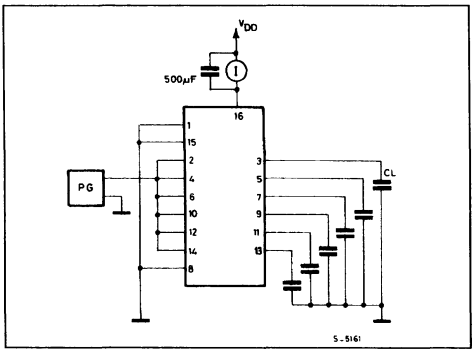


**TEST CIRCUIT** (continued)

Input Leakage Current.




Dynamic Power Dissipation.

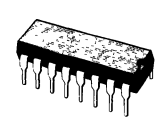


# HCC4504B
# HCF4504B

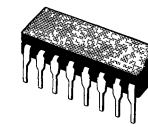
## HEX TTL OR CMOS TO CMOS LEVEL SHIFTER

**PRODUCT PREVIEW**

- VERY LOW QUIESCENT CURRENT
- HIGH NOISE IMMUNITY
- SUPPLY VOLTAGE RANGE 3V TO 18V FOR $V_{DD}$ AND $V_{CC}$
- UP TRANSLATES FROM A LOW TO A HIGH VOLTAGE OR DOWN TRANSLATES FROM A HIGH TO A LOW VOLTAGE
- INPUT THRESHOLD CAN BE SHIFTED FOR TTL COMPATIBILITY



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

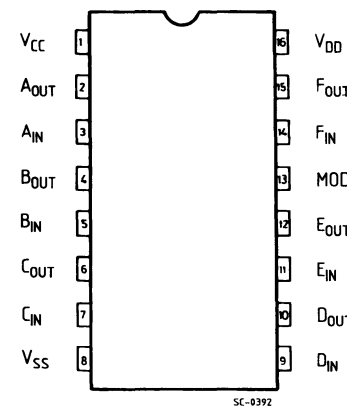
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4504 BF HCF4504 BM1
HCF4504 BEY HCF4504 BC1

**PIN CONNECTION** (top view)




### DESCRIPTION

The HCC4504B and HCF4504B are monolithic integrated circuits, available in 16-lead dual-in-line plastic or ceramic packages or in 16-pin SO micropackages.

The HCC4504B and HCF4504B are hex non-inverting level shifters. They will shift a TTL signal to CMOS logic levels for any CMOS supply voltage between 5V and 15V. A control input also allows interface from CMOS to CMOS at one logic level to another logic level. Either up or down level translating is accomplished by selection of power supply levels $V_{DD}$ and $V_{CC}$. The $V_{CC}$ level sets the input signal levels ; $V_{DD}$ selects the output voltage levels.

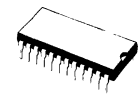
The supply current is typically 1nA at $V_{DD}$ = 10V for CMOS to CMOS operation. For TTL to CMOS translation the supply current is typically 2.5mA taken from $V_{CC}$.

SGS-THOMSON MICROELECTRONICS

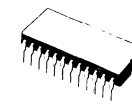
# HCC/HCF4508B

## DUAL 4-BIT LATCH

- TWO INDIPENDENT 4-BIT LATCHES
- INDIVIDUAL MASTER RESET FOR EACH 4-BIT-LATCH
- 3-STATE OUTPUTS WITH HIGH-IMPEDANCE STATE FOR BUS LINE APPLICATION
- MEDIUM-SPEED OPERATION $t_{PHL} = t_{PLH} =$ 70ns (TYP.) AT $V_{DD} = 10V$ AND $C_L = 50pF$
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**BEY**
(Plastic Package)

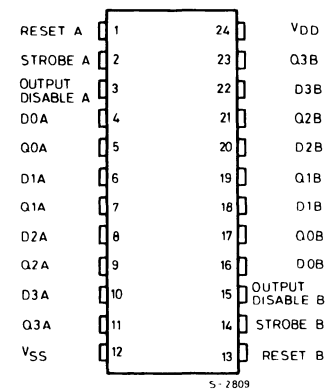


**BF**
(Ceramic Frit Seal Package)

**BM1**
(Micro Package)

**ORDER CODES :**
HCC4508BF HCF4508BEY
HCF4508BM1

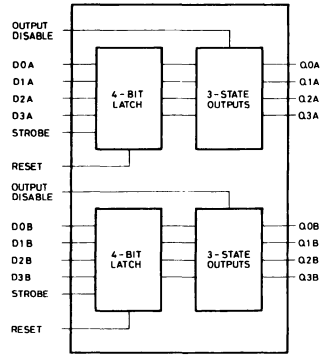
**PIN CONNECTIONS**




### DESCRIPTION

The **HCC4508B** (extended temperature range) and the **HCF4508B** (intermediate temperature range) are monolithic integrated circuits available in 24-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF4508B** dual 4-bit latch contains two identical 4-bit latches with separate STROBE, RESET, and OUTPUT DISABLE controls. With the STROBE line in the high state, the data on the "D" inputs appear at the corresponding "Q" outputs provided the DISABLE line is in the low state. Changing the STROBE line to the low state locks the data into the latch. A high on the reset line forces the outputs to a low level regardless of the state of the STROBE input. The outputs are forced to the high-impedance state for bus line applications by a high level on the DISABLE input

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

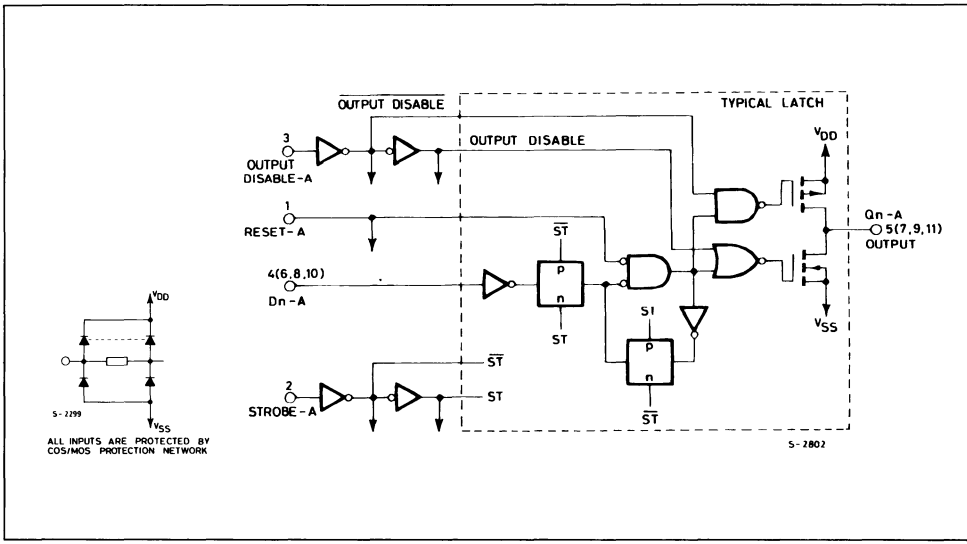
Stresses above those listed under "Absolute Maximum Ratings "may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltage values are referred to $V_{SS}$ pin voltage

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to + 18<br>3 to + 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

**LOGIC DIAGRAM** (A section)

1 OF 4 IDENTICAL LATCHES WITH COMMON OUTPUT DISABLE, RESET AND STROBE




## TRUTH TABLE

| Reset | Disab. | Strobe | D Input | Q Input |
|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | X | Latched |
| 1 | 0 | X | X | 0 |
| X | 1 | X | X | Z |

1 = High level
0 = Low level

X = Don't care
Z = High impedance

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0 04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4 95 | | V |
| | | | 0/10 | | < 1 | 10 | 9 95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14 95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0 05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4 5 | < 1 | 5 | 3.5 | | 3 5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4 5/0 5 | < 1 | 5 | | 1 5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13 5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | – 2 | | – 1.6 | – 3.2 | | – 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | – 0.64 | | – 0.51 | – 1 | | – 0.36 | | |
| | | | 0/10 | 9 5 | | 10 | – 1 6 | | – 1.3 | – 2.6 | | – 0.9 | | |
| | | | 0/15 | 13 5 | | 15 | – 4.2 | | – 3.4 | – 6.8 | | – 2 4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | – 1.53 | | – 1.36 | – 3 2 | | – 1.1 | | |
| | | | 0/ 5 | 4 6 | | 5 | – 0 52 | | – 0.44 | – 1 | | – 0.36 | | |
| | | | 0/10 | 9 5 | | 10 | – 1.3 | | – 1.1 | – 2.6 | | – 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | – 3.6 | | – 3.0 | – 6.8 | | – 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0 4 | | 5 | 0.64 | | 0.51 | 1 | | 0 36 | | mA |
| | | | 0/10 | 0 5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1 5 | | 15 | 4.2 | | 3 4 | 6 8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0 4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1 5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $I_O$ | 3-state Output | HCC Types | 0/18 | | | 18 | | ± 0.4 | | $\pm 10^{-4}$ | ± 0.4 | | ± 12 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 1.0 | | $\pm 10^{-4}$ | ± 1.0 | | ± 7.5 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

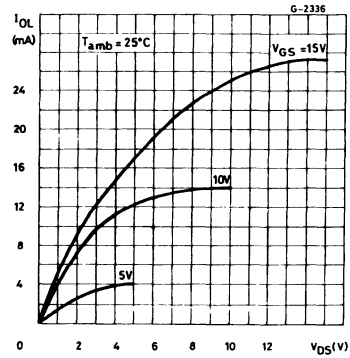
* $T_{Low}$ = – 55°C for **HCC** device – 40°C for **HCF** device
* $T_{High}$ = + 125°C for **HCC** device + 85°C for **HCF** device
The Noise Margin for both "1" and "0" level is 1V min with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2 5 V min with $V_{DD}$ = 15V

## DYNAMIC ELECTRICAL CHARACTERISTICS

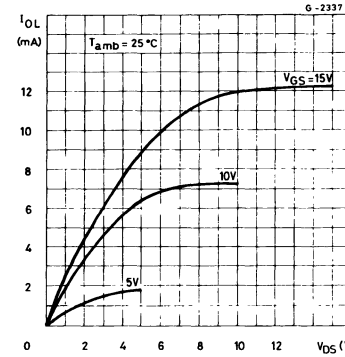
($T_{amb}$ = 25°C, input $t_r$, $t_f$ = 20ns, $C_L$ = 50pF, $R_L$ = 200kΩ, unless otherwise specified)

| Symbol | Parameter | | Test Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min | Typ. | Max. | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_{W(R)}$ | Reset Pulse Width | | 5 | 200 | 100 | | ns |
| | | | 10 | 140 | 70 | | |
| | | | 15 | 100 | 50 | | |
| $t_{W(st)}$ | Strobe Pulse Width | | 5 | 140 | 70 | | ns |
| | | | 10 | 80 | 40 | | |
| | | | 15 | 70 | 35 | | |
| $t_{setup}$ | Setup Time | | 5 | 50 | 25 | | ns |
| | | | 10 | 30 | 15 | | |
| | | | 15 | 20 | 10 | | |
| $t_H$ | Hold Time | | 5 | 0 | 0 | | ns |
| | | | 10 | 0 | 0 | | |
| | | | 15 | 0 | 0 | | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time: | Strobe to Data Out | 5 | | 130 | 260 | ns |
| | | | 10 | | 70 | 140 | |
| | | | 15 | | 50 | 100 | |
| | | Data in to Data Out | 5 | | 105 | 210 | ns |
| | | | 10 | | 60 | 120 | |
| | | | 15 | | 45 | 90 | |
| | | Reset to Data Out | 5 | | 90 | 180 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_{PHZ}$ | 3-State Propagation Delay Time: Output High to High impedance | | 5 | | 90 | 180 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 35 | 70 | |
| $t_{PZH}$ | High Impedance to Output High | | 5 | | 90 | 180 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 35 | 70 | |
| $t_{PLZ}$ | Output Low to High Impedance | | 5 | | 90 | 180 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 35 | 70 | |
| $t_{PZL}$ | High Impedance to Output Low | | 5 | | 90 | 180 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 35 | 70 | |

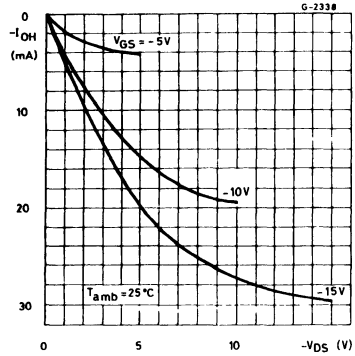
Typical Output Low (sink) Current Characteristics.



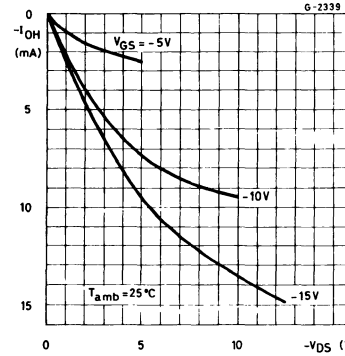

Minimum Output Low (sink) Current Characteristics.



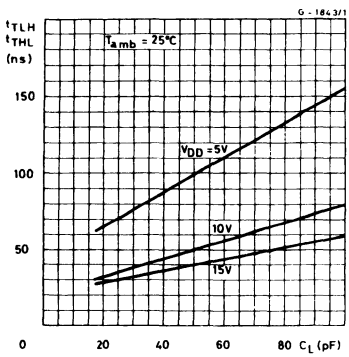

Typical Output High (source) Current Characteristics.



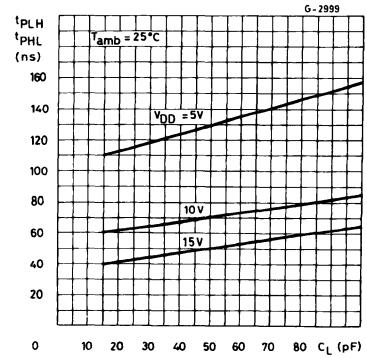

Minimum Output High (source) Current Characteristics.



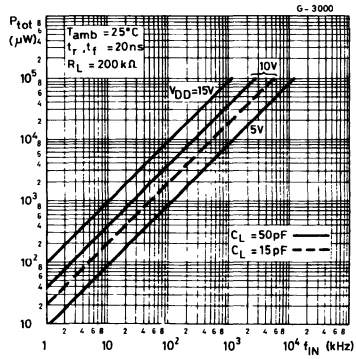

Typical Transition Time vs. Load Capacitance.



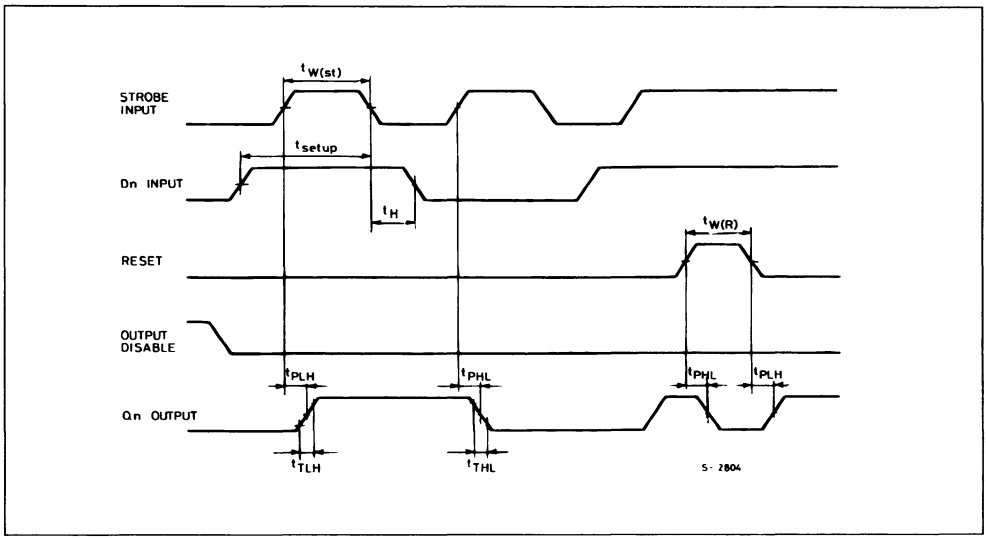

Typical Propagation Delay Time vs. Load Capacitance (strobe to dataout).



Typical Power Dissipation vs. Frequency .

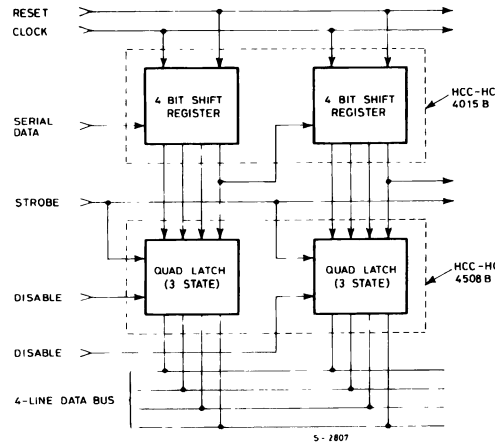



## TEST WAVEFORM

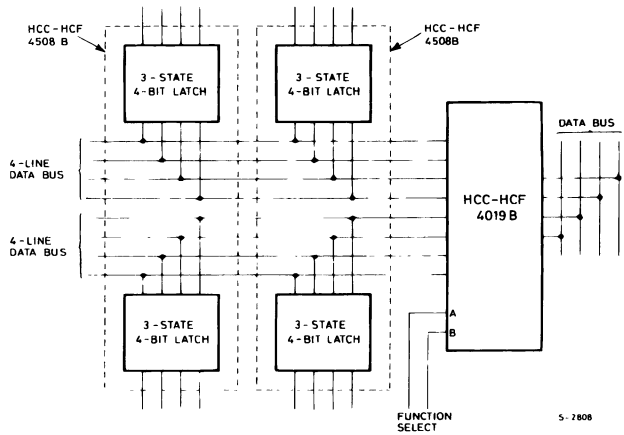


## TYPICAL APPLICATIONS

A) **Figure 15** : Bus register.



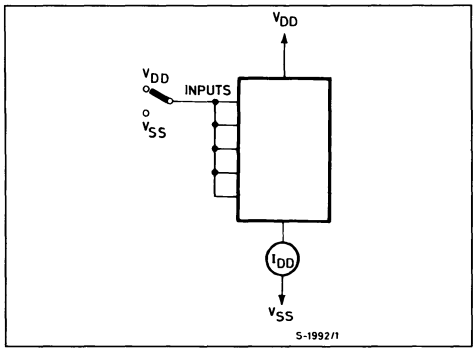

B) **Figure 16** : Dual multiplexed bus register with function select.



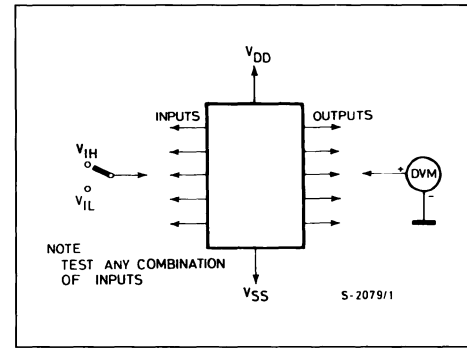

| A | B | Function |
|---|---|---|
| 0 | 0 | Inhibit (all 0) |
| 1 | 0 | Select A Bus |
| 0 | 1 | Select B Bus |
| 1 | 1 | $A_1 + B_1$ |

## TEST CIRCUITS

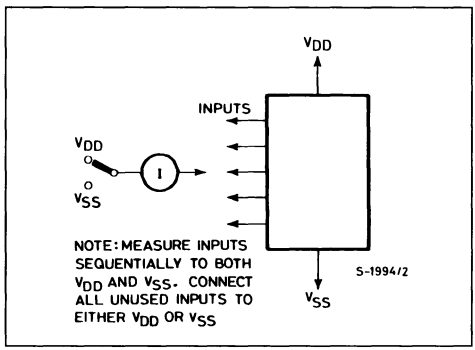
Quiescent Device Current Test Circuit.



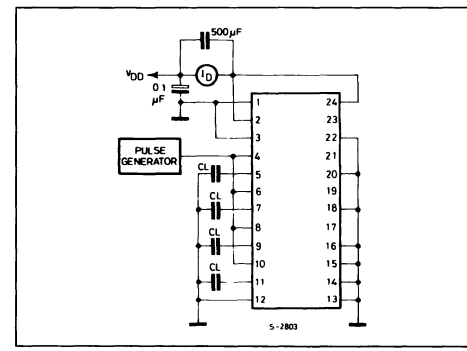

Input Voltage Test Circuit.



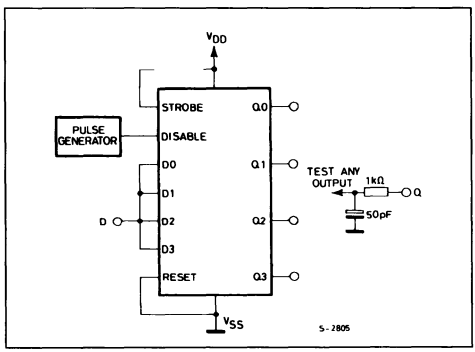

Input Current Test Circuit.



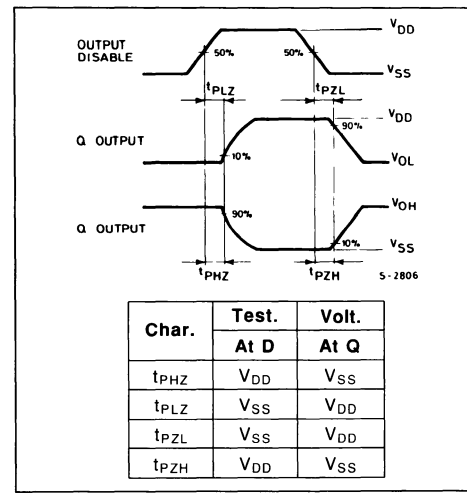

Power Dissipation Test Circuit.




Output Disable.




Waveform.



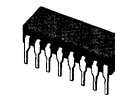

| Char. | Test. | Volt. |
|---|---|---|
| | At D | At Q |
| $t_{PHZ}$ | $V_{DD}$ | $V_{SS}$ |
| $t_{PLZ}$ | $V_{SS}$ | $V_{DD}$ |
| $t_{PZL}$ | $V_{SS}$ | $V_{DD}$ |
| $t_{PZH}$ | $V_{DD}$ | $V_{SS}$ |

# HCC/HCF4510B
# HCC/HCF4516B

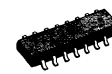
## PRESETTABLE UP/DOWN CUNTERS

- MEDIUM SPEED OPERATION $f_{CL}$ = 8MHz TYP. AT 10V
- SYNCHRONOUS INTERNAL CARRY PROPAGATION
- RESET AND PRESET CAPABILITY
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

**EY**
(Plastic Package)



**F**
(Ceramic Package)



**M1**
(Micro Package)

**C1**
(Chip Carrier)

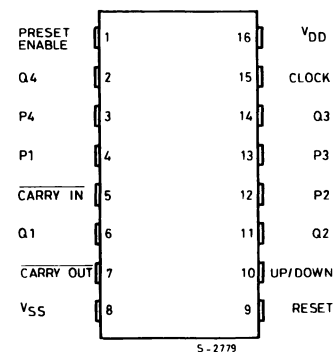
**ORDER CODES :**

HCC45XXBF HCF4516BM1
HCF45XXBEY HCF45XXBC1

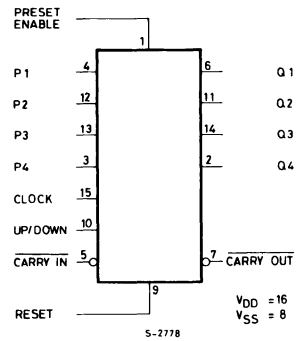
### DESCRIPTION

The **HCC4510B, HCC4516B** (extended temperature range) and the **HCF4510B, HCF4516B** (intermediate temperature range) are monolithic integrated circuits available in 16-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF4510B** Presettable BCD Up/Down Counter and the **HCC/HCF4516B** Presettable Binary Up/Down Counter consist of four synchronously clocked D-type flip-flops (with a gating structure to provide T-type flip-flop capability) connected as counters. These counters can be cleared by a high level on the RESET line, and can be preset to any binary number present on the jam inputs by a high level on the PRESET ENABLE line. The **HCC/HCF4510B** will count out of non-BCD counter states in a maximum of two clock pulses in the up mode, and a maximum of four clock pulses in the down mode. If the CARRY-IN input is held low, the counter advances up or down on each positive-going clock transition. Synchronous cascading is accomplished by connecting all clock inputs in parallel and connecting the CARRY-OUT of a less significant stage to the CARRY-IN of a more significant stage. The **HCC/HCF4510B** and **HCC/HCF4516B** can be cascaded in the ripple mode by connecting the CARRY-OUT to the clock of the next stage. If the UP/DOWN input changes during a terminal count, the CARRY-OUT must be gated with the clock, and the UP/DOWN input must change while the clock is high. This method provides a clean clock signal to the subsequent counting stage.

### PIN CONNECTIONS



## FUNCTIONAL DIAGRAM




| CL | $\overline{CI}$ | U/D | PE | R | Action |
|---|---|---|---|---|---|
| X | 1 | X | 0 | 0 | No Count |
| ⎍⎾ | 0 | 1 | 0 | 0 | Count Up |
| ⎍⎾ | 0 | 0 | 0 | 0 | Count Down |
| X | X | X | 1 | 0 | Preset |
| X | X | X | X | 1 | Reset |

X = Don't care

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functionnal operation of the device at these or any other conditions above those indicated in the operationale sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability

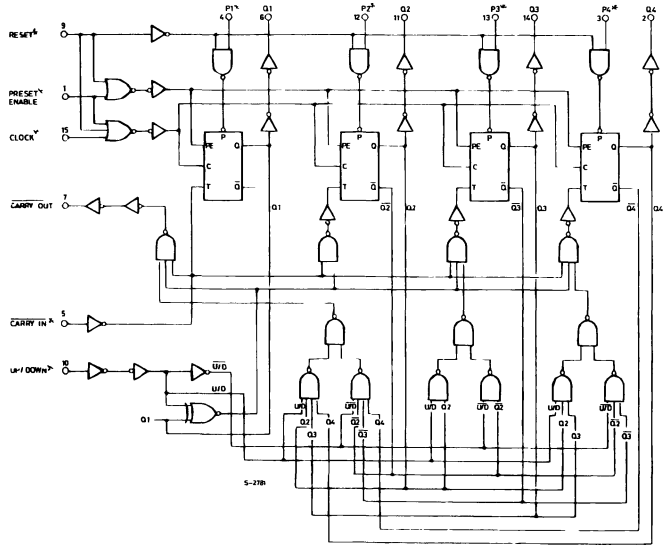
* All voltage values are referred to $V_{SS}$ pin voltage

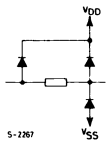
## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage · **HCC** Types<br>**HCF** Types | 3 to + 18<br>3 to + 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAMS

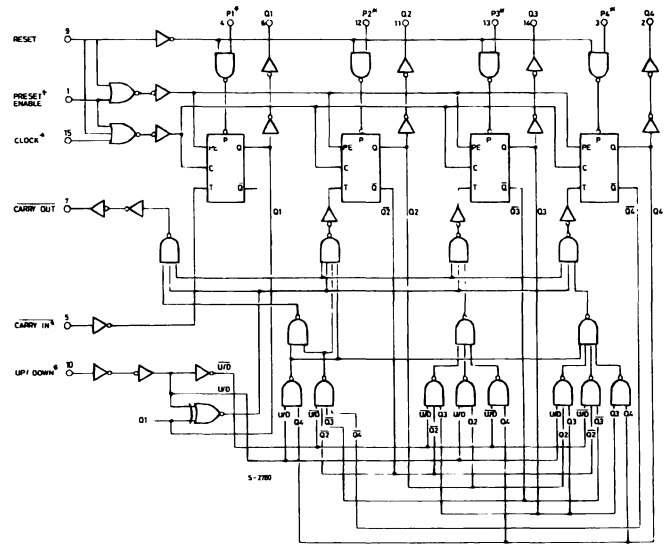
### 4510B

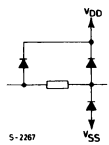



ALL INPUTS PROTECTED BY COS/MOS PROTECTION NETWORK

### 4516B

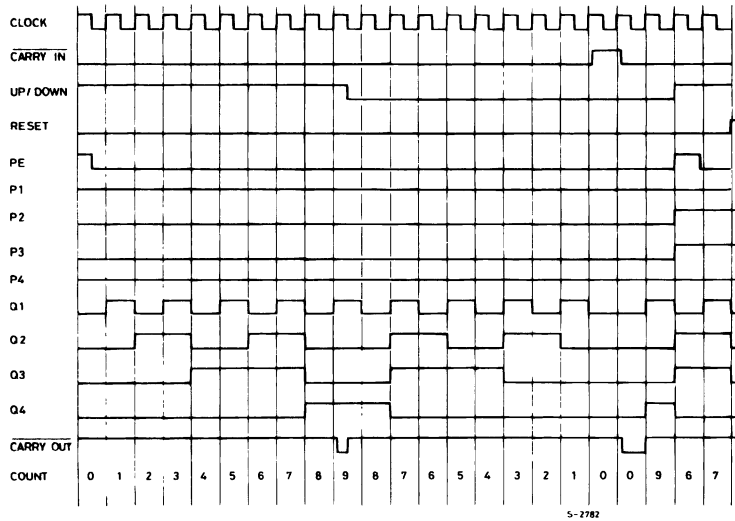


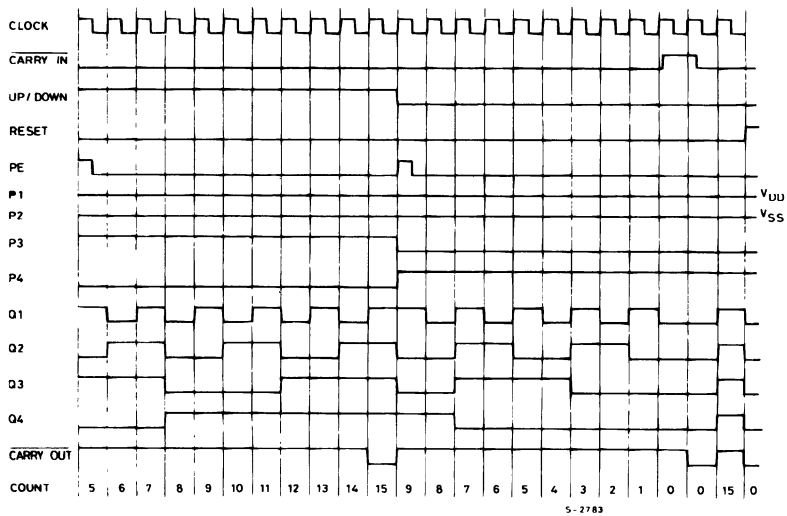

ALL INPUTS PROTECTED BY COS/MOS PROTECTION NETWORK

## TIMING DIAGRAMS

**4510B**




**4516B**



## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$= − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$= + 125°C for **HCC** device . + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5 V min. with $V_{DD}$ = 15V.

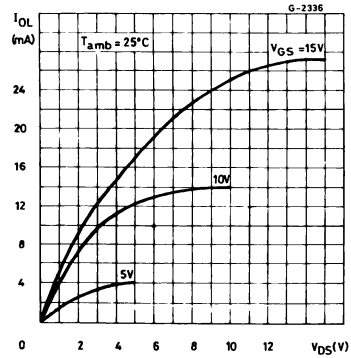
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall times = 20ns)

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time Clock to Q Output | 5 | | 200 | 400 | ns |
| | | 10 | | 100 | 200 | |
| | | 15 | | 75 | 150 | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time Preset or Reset to Q Output | 5 | | 210 | 420 | ns |
| | | 10 | | 105 | 210 | |
| | | 15 | | 80 | 160 | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time Clock to Carry Out | 5 | | 240 | 480 | ns |
| | | 10 | | 120 | 240 | |
| | | 15 | | 90 | 180 | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time Carry in to Carry Out | 5 | | 125 | 250 | ns |
| | | 10 | | 60 | 120 | |
| | | 15 | | 50 | 100 | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time Preset or Reset to Carry Out | 5 | | 320 | 640 | ns |
| | | 10 | | 160 | 320 | |
| | | 15 | | 125 | 250 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | 5 | | 100 | 200 | ns |
| | | 10 | | 50 | 100 | |
| | | 15 | | 40 | 80 | |
| $f_{max}$ | Max. Clock Frequency | 5 | 2 | 4 | | MHz |
| | | 10 | 4 | 8 | | |
| | | 15 | 5.5 | 11 | | |
| $t_W$ | Clock Pulse Width | 5 | 150 | | | ns |
| | | 10 | 75 | | | |
| | | 15 | 60 | | | |
| | •Preset Enable or Reset Removal Time | 5 | 150 | | | ns |
| | | 10 | 80 | | | |
| | | 15 | 60 | | | |
| $t_r$, $t_f$ | *Clock Rise and Fall Time | 5 | | | 15 | µs |
| | | 10 | | | 5 | |
| | | 15 | | | 5 | |
| $t_{setup}$ | Carry in Setup Time | 5 | 130 | | | ns |
| | | 10 | 60 | | | |
| | | 15 | 45 | | | |
| $t_{setup}$ | Up-down Setup Time | 5 | 360 | | | ns |
| | | 10 | 160 | | | |
| | | 15 | 110 | | | |
| $t_W$ | Preset Enable or Reset Pulse Width | 5 | 220 | | | ns |
| | | 10 | 100 | | | |
| | | 15 | 75 | | | |

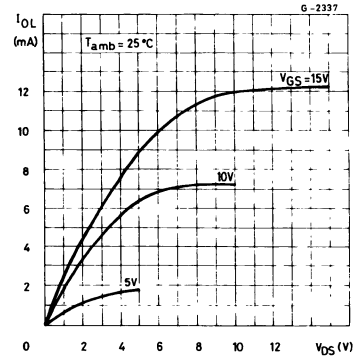
• Time required after the falling edge of the reset or preset enable inputs before the rising edge of the clock will trigger the counter (similar to setup time)

* If more than unit is cascaded in the parallel clocked application, $t_rCL$ should be made less than or equal to the sum of the fixed propagation delay at 15pF and the transition time of the carry output driving stage for the estimated capacitive load

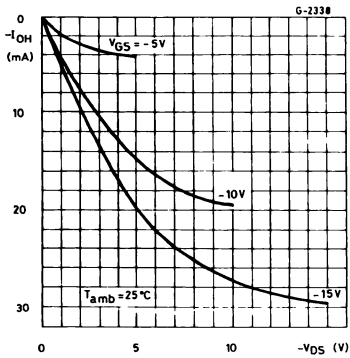
Typical Output Low (sink) Current Characteristics.



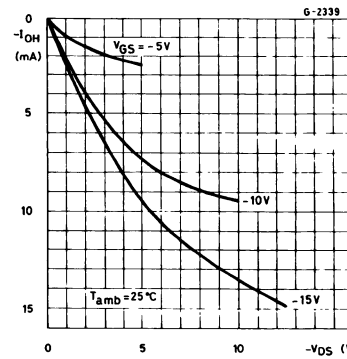

Minimum Output Low (sink) Current Characteristics.



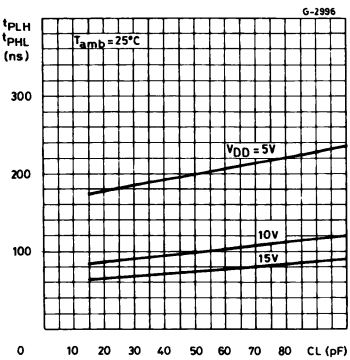

Typical Output High (source) Current Characteristics.



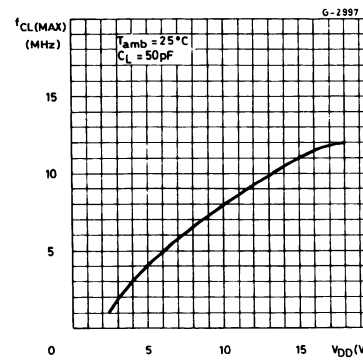

Minimum Output High (source) Current Characteristics.



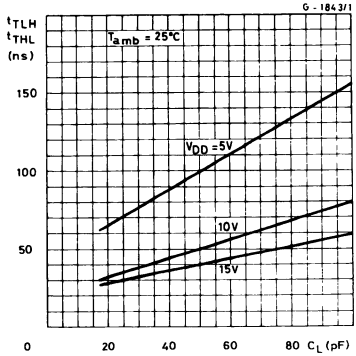

Typical Propagation Delay Time vs. Load Capacitance for Clock to Q Output.



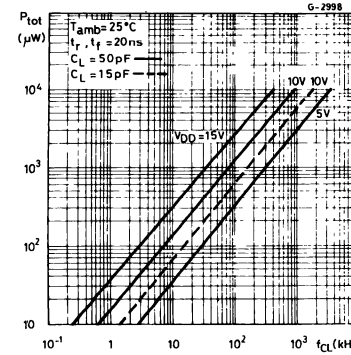

Typical Maximum Clock Input Frequency vs. Supply Voltage.



Typical Transition Time vs. Load Capacitance.

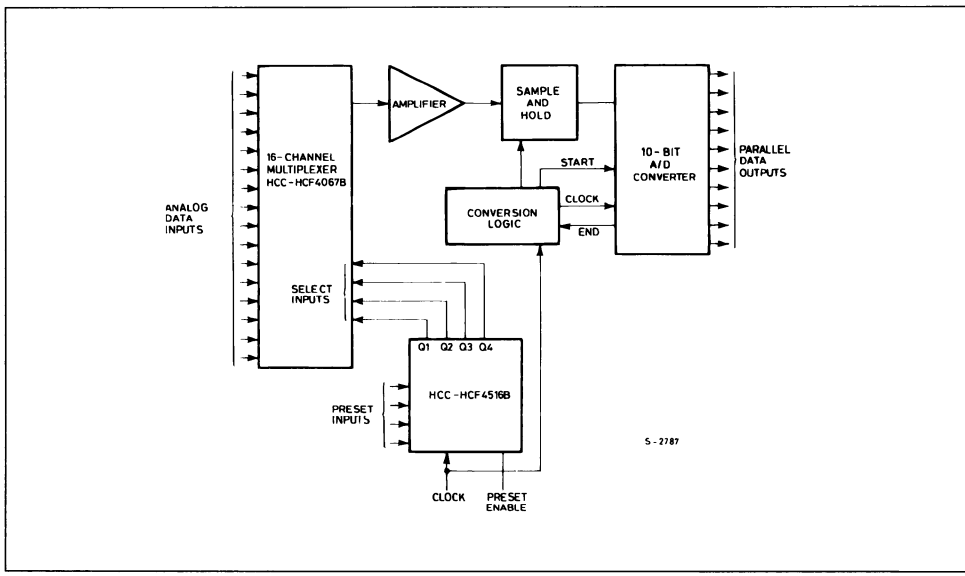



Typical Dynamic Power Dissipation vs. Frequency.



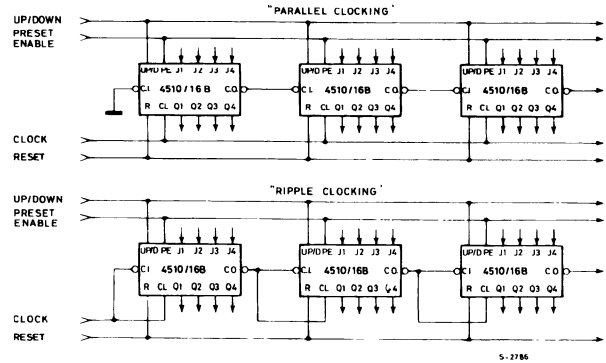

## TYPICAL APPLICATIONS

TYPICAL 16-CHANNEL, 10 BIT DATA ACQUISITION SYSTEM



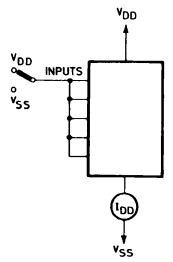

This acquisition system can be operated in the random access mode by jamming in the channel number at the present inputs, or in the sequential mode by clocking the HCC/HCF4516B

## CASCADING COUNTER PACKAGES

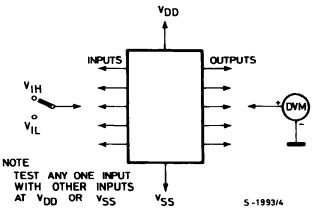



## TEST CIRCUITS

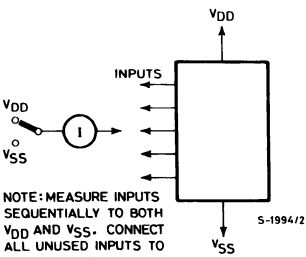
Quiescent Device Current.



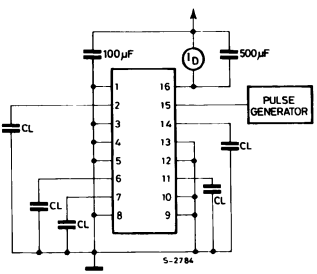

Noise Immunity.




Input Leakage Current.

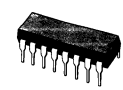



Power Dissipation and Input Waveform.

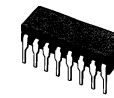


# BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

- HIGH-OUTPUT-SOURCING CAPABILITY (up to 25 mA)
- INPUT LATCHES FOR BCD CODE STORAGE
- LAMP TEST AND BLANKING CAPABILITY
- 7-SEGMENT OUTPUTS BLANKED FOR BCD INPUT CODES > 1001
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100mA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

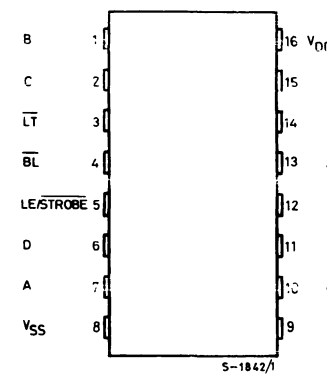
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4511BF HCF4511BM1
HCF4511BEY HCF4511BC1

**PIN CONNECTIONS**



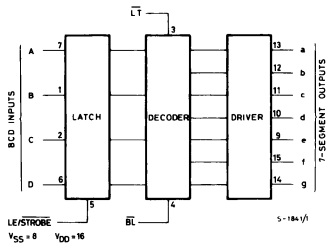

## DESCRIPTION

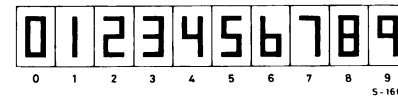
The **HCC 4511B** (extended temperature range) and the **HCF 4511B** (intermediate temperature range) are monolithic integrated circuits available in 16-lead dual in-line plastic or ceramic package and plastic micro package.

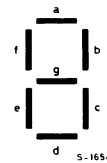
The **HCC/HCF 4511B** types are BCD-to-7-segment latch decoder drivers constructed with COS/MOS logic and n-p-n bipolar transistor output devices on a single monolithic structure. These devices combine the low quiescent power dissipation and high noise immunity features of COS/MOS with n-p-n bipolar output transistors capable of sourcing up to 25 mA. This capability allows the **HCC/HCF 4511B** types to drive LED's and other displays directly.

Lamp Test ($\overline{LT}$), Blanking ($\overline{BL}$), and Latch Enable or Strobe inputs are provided to test the display, shut off or intensity-modulate it, and store or strobe a BCD code, respectively. Several different signal may be multiplexed and displayed when external multiplexing circuitry is used.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

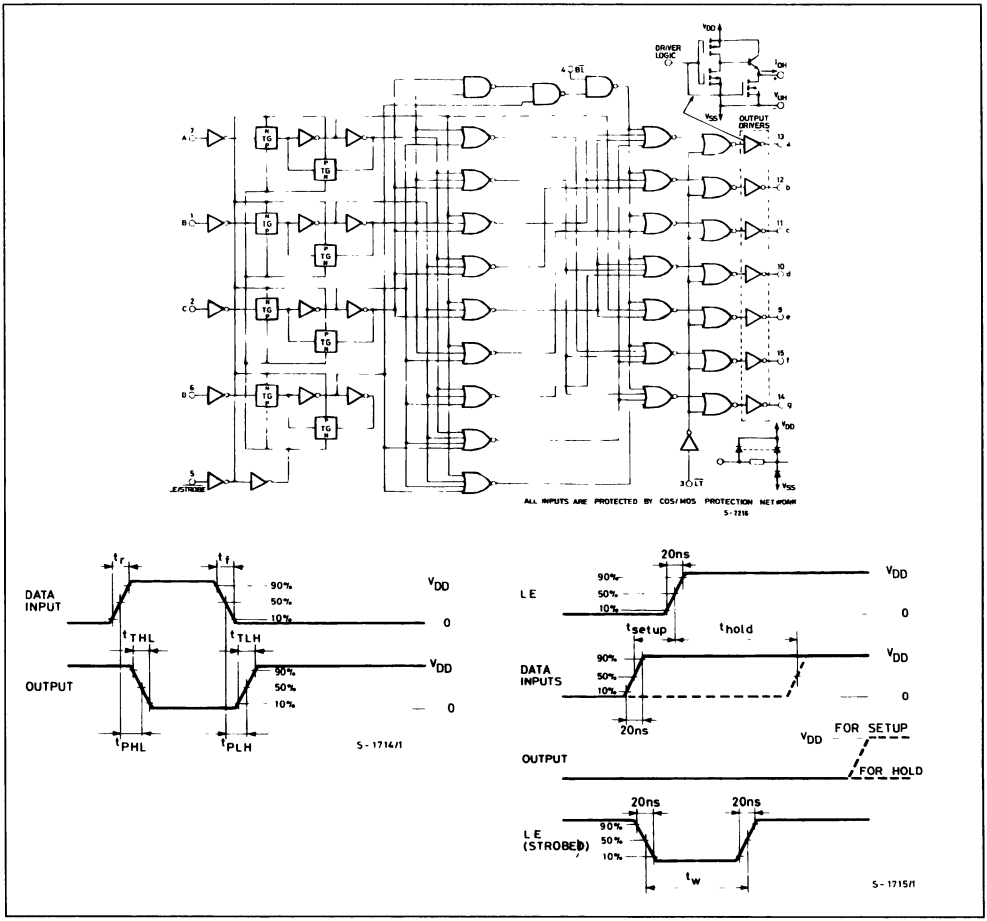
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functionnal operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAMS



## TRUTH TABLE

| LE | $\overline{BI}$ | $\overline{LT}$ | D | C | B | A | a | b | c | d | e | f | g | Display |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| X | X | 0 | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8 |
| X | 0 | 1 | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 2 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 3 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 4 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 5 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 6 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 7 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 9 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 1 | 1 | 1 | X | X | X | X | | | | * | | | | * |

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | | 5 | 4 | | 4.1 | 4.55 | | 4.2 | | V |
| | | | 0/10 | | | 10 | 9 | | 9.1 | 9.55 | | 9.2 | | |
| | | | 0/15 | | | 15 | 14 | | 14.1 | 14.55 | | 14.2 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/3.8 | | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/8.8 | | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.8 | | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 3.8/0.5 | | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 8.8/1 | | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.8/1.5 | | 15 | | 4 | | | 4 | | 4 | |
| $V_{OH}$ | Output Drive Voltage | HCC Types | | | 0 | 5 | 4.1 | | 4.10 | 4.55 | | 4.20 | | V |
| | | | | | 5 | | | | | 4.25 | | | | |
| | | | | | 10 | | 3.80 | | 3.90 | 4.10 | | 3.90 | | |
| | | | | | 15 | | | | | 3.95 | | | | |
| | | | | | 20 | | 3.55 | | 3.40 | 3.75 | | | | |
| | | | | | 25 | | 3.40 | | 3.10 | 3.55 | | | | |
| | | | | | 0 | 10 | 9 | | 9.10 | 9.55 | | 9.20 | | V |
| | | | | | 5 | | | | | 9.25 | | | | |
| | | | | | 10 | | 8.85 | | 9 | 9.15 | | | | |
| | | | | | 15 | | | | | 9.05 | | | | |
| | | | | | 20 | | 8.70 | | 8.60 | 8.90 | | 8.40 | | |
| | | | | | 25 | | 8.60 | | 8.30 | 8.75 | | | | |
| | | | | | 0 | 15 | 14 | | 14.10 | 14.55 | | 14.20 | | V |
| | | | | | 5 | | | | | 14.30 | | | | |
| | | | | | 10 | | 13.90 | | 14 | 14.20 | | 14 | | |
| | | | | | 15 | | | | | 14.10 | | | | |
| | | | | | 20 | | 13.75 | | 13.70 | 13.95 | | 13.50 | | |
| | | | | | 25 | | 13.65 | | 13.50 | 13.80 | | 13.10 | | |

* $T_{Low}$= − 55°C for **HCC** device . − 40°C for **HCF** device.
* $T_{High}$= + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5 V min. with $V_{DD}$ = 15V.

## STATIC ELECTRICAL CHARACTERISTICS (continued)

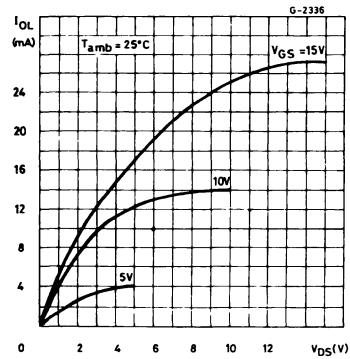
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output Drive Voltage | HCF Types | | | 0 | 5 | 4 1 | | 4 1 | 4 57 | | 4.1 | | V |
| | | | | | 5 | | | | | 4 24 | | | | |
| | | | | | 10 | | 3 6 | | 3 6 | 4.12 | | 3 3 | | |
| | | | | | 15 | | | | | 3.94 | | | | |
| | | | | | 20 | | 2 8 | | 2 8 | 3 75 | | 2 5 | | |
| | | | | | 25 | | | | | 3.54 | | | | |
| | | | | | 0 | 10 | 9 1 | | 9 1 | 9 58 | | 9 1 | | V |
| | | | | | 5 | | | | | 9 26 | | | | |
| | | | | | 10 | | 8 75 | | 8 75 | 9 17 | | 8 45 | | |
| | | | | | 15 | | | | | 9.04 | | | | |
| | | | | | 20 | | 8.1 | | 8 1 | 8.90 | | 7 8 | | |
| | | | | | 25 | | | | | 8.75 | | | | |
| | | | | | 0 | 15 | 14 1 | | 14.1 | 14.59 | | 14 1 | | V |
| | | | | | 5 | | | | | 14 27 | | | | |
| | | | | | 10 | | 13 75 | | 13 75 | 14 18 | | 13.45 | | |
| | | | | | 15 | | | | | 14.07 | | | | |
| | | | | | 20 | | 13 1 | | 13 1 | 13 95 | | 12 8 | | |
| | | | | | 25 | | | | | 13.80 | | | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0 4 | | 5 | 0 64 | | 0.51 | 1 | | 0 36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1 3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1 5 | | 15 | 4 2 | | 3.4 | 6 8 | | 2 4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0 44 | 1 | | 0.36 | | |
| | | | 0/10 | 0 5 | | 10 | 1.3 | | 1.1 | 2 6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3 6 | | 3 | 6 8 | | 2 4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0 1 | | $\pm 10^{-5}$ | ± 0.1 | | ±1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ±0 3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7 5 | | | pF |

* $T_{Low}$= − 55°C for **HCC** device . − 40°C for **HCF** device.
* $T_{High}$= + 125°C for **HCC** device + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is . 1V min with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2 5 V min with $V_{DD}$ = 15V

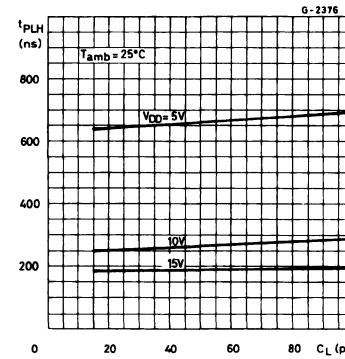
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ = 0.3% /°C values, all input rise and fall time = 20ns)

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$ | Propagation Delay Time (data) | 5 | | 520 | 1040 | ns |
| | | 10 | | 210 | 420 | |
| | | 15 | | 150 | 300 | |
| $t_{PLH}$ | Propagation Delay Time (data) | 5 | | 660 | 1320 | ns |
| | | 10 | | 260 | 520 | |
| | | 15 | | 180 | 360 | |
| $t_{PHL}$ | Propagation Delay Time ($\overline{BL}$) | 5 | | 350 | 700 | ns |
| | | 10 | | 175 | 350 | |
| | | 15 | | 125 | 250 | |
| $t_{PLH}$ | Propagation Delay Time ($\overline{BL}$) | 5 | | 400 | 800 | ns |
| | | 10 | | 175 | 350 | |
| | | 15 | | 150 | 300 | |
| $t_{PHL}$ | Propagation Delay Time ($\overline{LT}$) | 5 | | 250 | 500 | ns |
| | | 10 | | 125 | 250 | |
| | | 15 | | 85 | 170 | |
| $t_{PLH}$ | Propagation Delay Time ($\overline{LT}$) | 5 | | 150 | 300 | ns |
| | | 10 | | 75 | 150 | |
| | | 15 | | 50 | 100 | |
| $t_{TLH}$ | Transition Time | 5 | | 40 | 80 | ns |
| | | 10 | | 30 | 60 | |
| | | 15 | | 20 | 50 | |
| $t_{THL}$ | Transition Time | 5 | | 125 | 310 | ns |
| | | 10 | | 75 | 185 | |
| | | 15 | | 65 | 160 | |
| $t_{setup}$ | Setup Time | 5 | 150 | 75 | | ns |
| | | 10 | 70 | 35 | | |
| | | 15 | 40 | 20 | | |
| $t_{hold}$ | Hold Time | 5 | 0 | − 75 | | ns |
| | | 10 | 0 | − 35 | | |
| | | 15 | 0 | − 20 | | |
| $t_W$ | Strobe Pulse Widht | 5 | 400 | 200 | | ns |
| | | 10 | 160 | 80 | | |
| | | 15 | 100 | 50 | | |

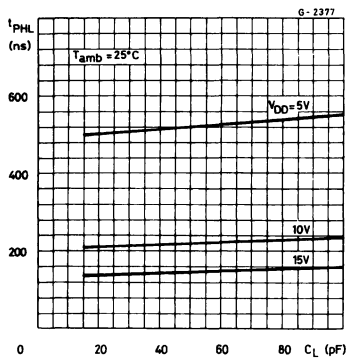
Typical Output Low (sink) Current Characteristics.



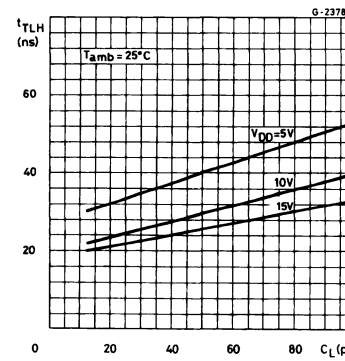

Typical data-to-output, low-to-high-level propagation delay time as a function of load capacitance.



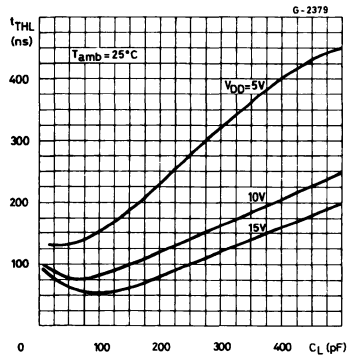

Typical data-to-output, high-to-low-level propagation delay time as a function of load capacitance.



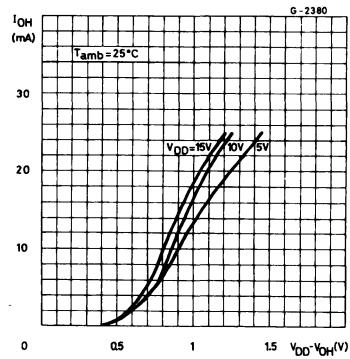

Typical low-to-high level transition ime as a function of load capacitance.



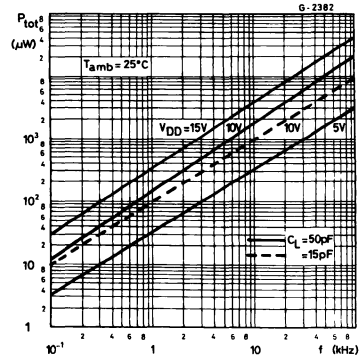

Typical high-to-low level transition ime as a function of load capacitance.



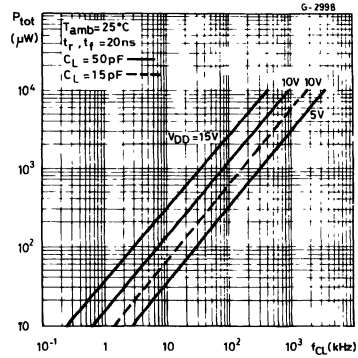

Typical Voltage drop ($V_{DD}$ to output) vs. Output source Current as a Function of Supply.



Typical Dynamic Power Dissipation Characteristics.



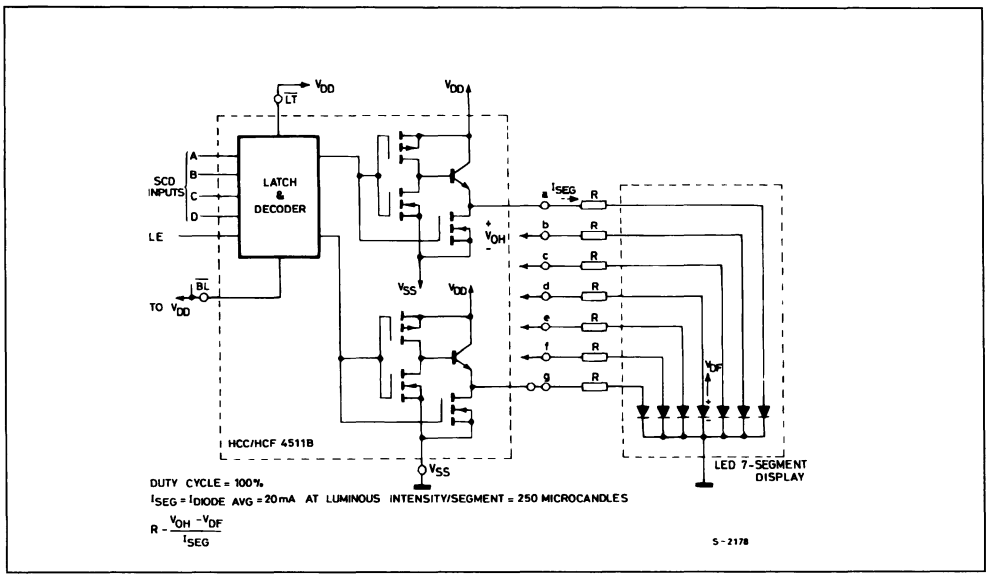

Derated Static Output Current Per Output.




Maximum continuous derated output current IOH applies to a single output with all other outputs sourcing an equal amount of current at the supply voltages shown Operation above the derating curve is not recommenced

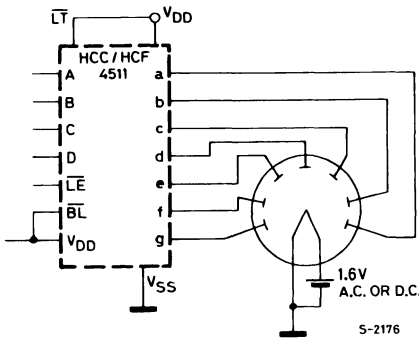
**TYPICAL APPLICATIONS** (interfacing with various displays)

DRIVING COMMON-CATHODE 7-SEGMENT LED DISPLAYS



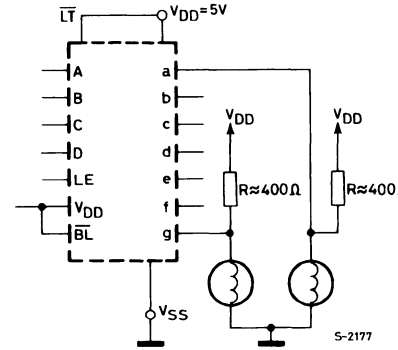
## TYPICAL APPLICATIONS (continued)

Driving Low-voltage Fluorescent Displays.




A medium-brightness intensity display can be obtained with low-voltage fluorescent displays such as the Tung-Sot Digivac S/G series.

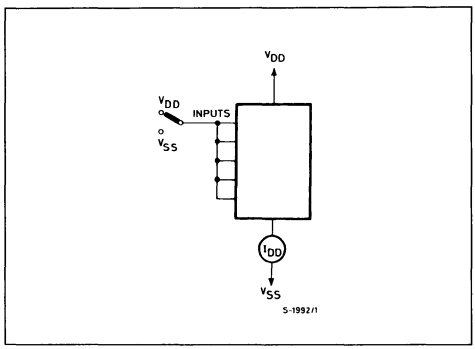
Driving Incandescent Displays.



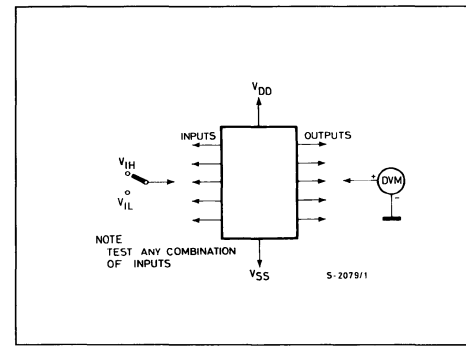

**2 of 7 Segments Shown Connected**
Resistors R from VDD VDD to each 7-segment driver output are choosen to keep all Numitron segments slightly on and warm.

## TEST CIRCUITS

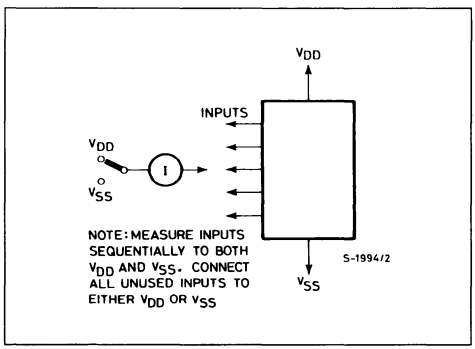
Quiescent Device Current.



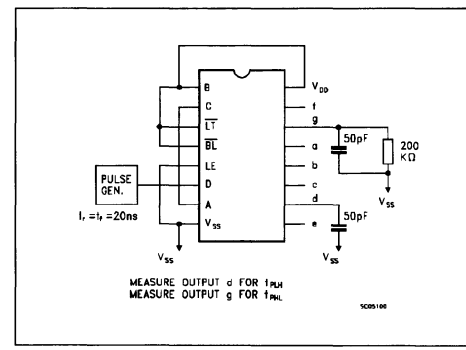

Noise Immunity.




Input Leakage Current.

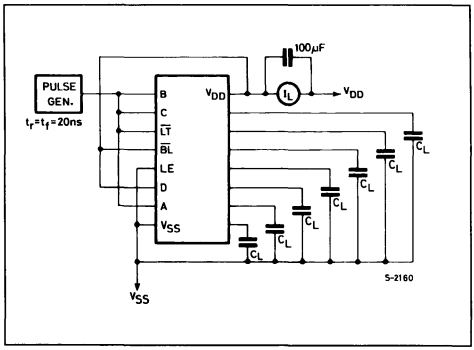



Data Propagation Delay.



**TEST CIRCUITS** (continued)

Dynamic Power dissipation.



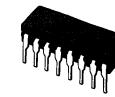
SGS-THOMSON MICROELECTRONICS

# HCC4512B
# HCF4512B

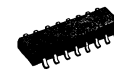
## 8–CHANNEL DATA SELECTOR

- 3-STATE OUTPUT
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

**EY**
(Plastic Package)



**F**
(Ceramic Package)



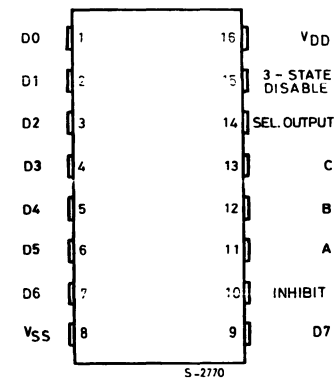
**M1**
(Micro Package)

**C1**
(Chip Carrier)

**ORDER CODES :**

HCC4512BF HCF4512BM1
HCF4512BEY HCF4512BC1

**PIN CONNECTIONS**

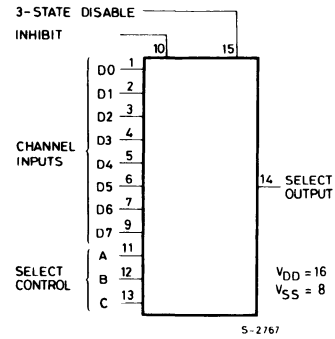



### DESCRIPTION

The **HCC4512B** (extended temperature range) and **HCF4512B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and plastic micro package.

The **HCC/HCF4512B** is an 8-channel data selector featuring a three-state output that can interface directly with, and drive, data lines of bus-oriented systems.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0 5 to $V_{DD}$ + 0 5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature . **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings may cause permanent ddamage to the device This is a stress rating only and functionnal operation of the device at these or any other conditions above those indicated in the operationale sections of this specification is not implied Exposure to absolute maximum rating conditions for external periods may affect device reliability
* All voltage values are refered to $V_{SS}$ pin voltage

## RECOMMENDED OPERATING CONDITIONS

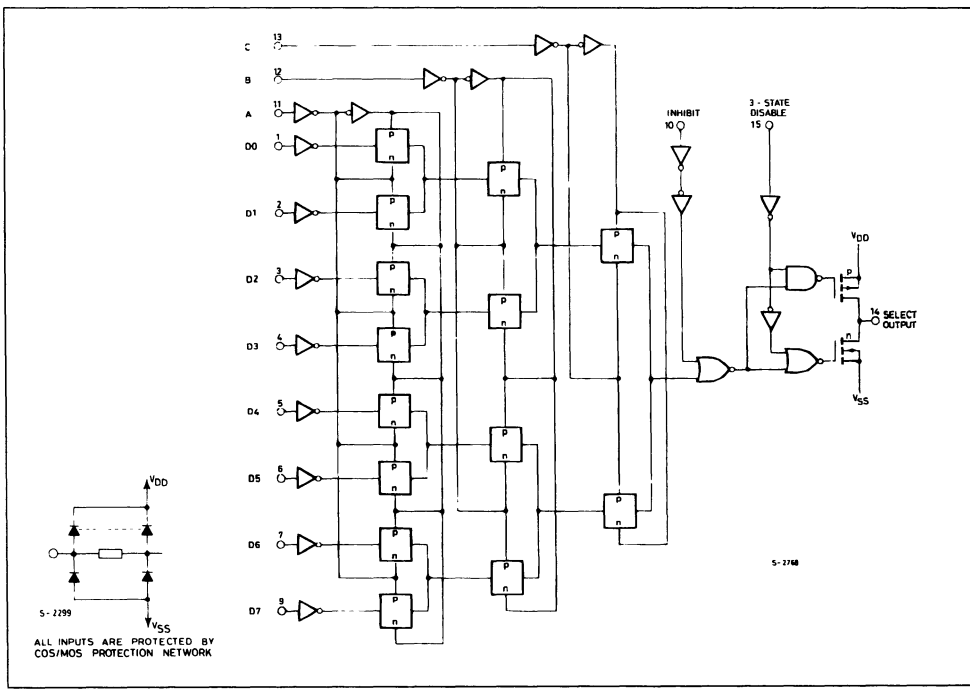
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to + 18<br>3 to + 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature . **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## TRUTH TABLE

| Sel. Cont. | | | Inh. | 3-State Disable | Sel. Output |
|---|---|---|---|---|---|
| A | B | C | | | |
| 0 | 0 | 0 | 0 | 0 | D0 |
| 1 | 0 | 0 | 0 | 0 | D1 |
| 0 | 1 | 0 | 0 | 0 | D2 |
| 1 | 1 | 0 | 0 | 0 | D3 |
| 0 | 0 | 1 | 0 | 0 | D4 |
| 1 | 0 | 1 | 0 | 0 | D5 |
| 0 | 1 | 1 | 0 | 0 | D6 |
| 1 | 1 | 1 | 0 | 0 | D7 |
| X | X | X | 1 | 0 | 0 |
| X | X | X | X | 1 | High Z |

1 = High Level  0 = Low Level  X = Don't Care

## LOGIC DIAGRAMS



## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

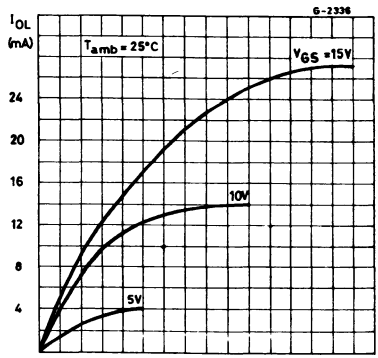
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1 1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1 1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0 5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $I_{O\ max}$ | 3-State Output Leakage Current | HCC Types | 0/18 | 0/18 | | 18 | | ± 0.4 | | $\pm 10^{-4}$ | ± 0.4 | | ± 12 | μA |
| | | HCF Types | 0/18 | 0/18 | | 18 | | ± 1.0 | | $\pm 10^{-4}$ | ± 1.0 | | 7.5 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$= − 55°C for **HCC** device : − 40°C for **HCF** device
* $T_{High}$= + 125°C for **HCC** device + 85°C for **HCF** device
The Noise Margin for both "1" and "0" level is · 1V min. with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2 5 V min with $V_{DD}$ = 15V

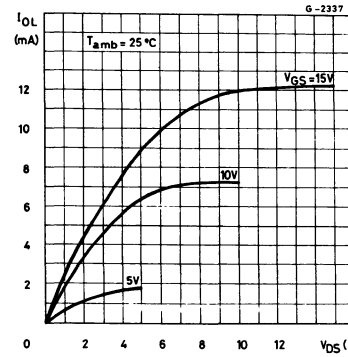
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall time = 20ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time Inhibit to Output | | 5 | | 140 | 280 | ns |
| | | | 10 | | 70 | 140 | |
| | | | 15 | | 50 | 100 | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time "A" Select to Output | | 5 | | 200 | 400 | ns |
| | | | 10 | | 85 | 170 | |
| | | | 15 | | 60 | 120 | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time Data to Output | | 5 | | 180 | 360 | ns |
| | | | 10 | | 75 | 150 | |
| | | | 15 | | 55 | 110 | |
| $t_{PZL}$, $t_{PLZ}$ $t_{PHZ}$, $t_{PZH}$ | 3-state Disable Delay Time | | 5 | | 60 | 120 | ns |
| | | | 10 | | 30 | 60 | |
| | | | 15 | | 20 | 40 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

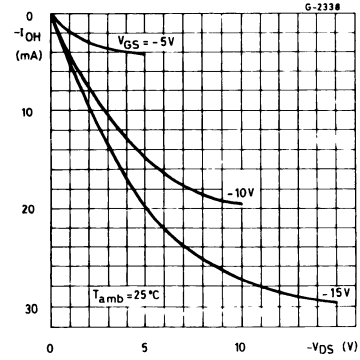
Typical Output Low (sink) Current Characteristics.



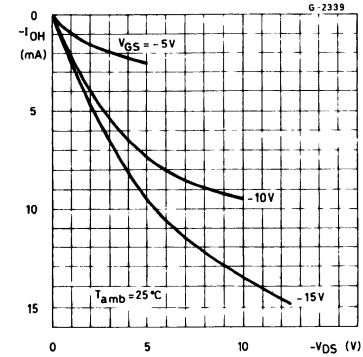

Minimum Output Low (sink) Current Characteristics.



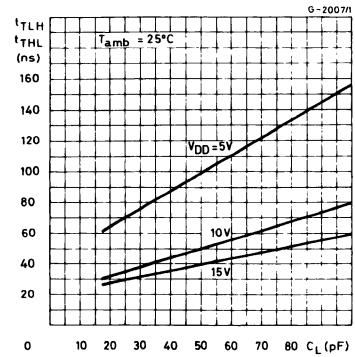
Typical Output High (source) Current Characteristics.



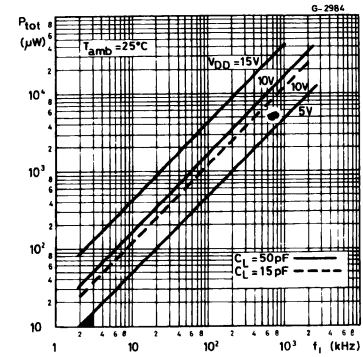

Minimum Output High (source) Current Characteristics.



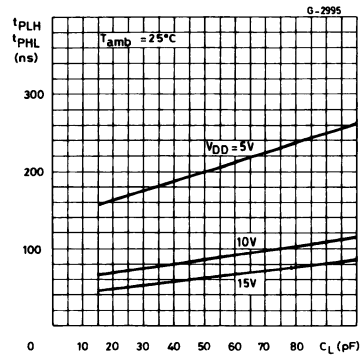

Typical Transition Time vs. Load Capacitance.




Typical Dynamic Power Dissipation vs. Input Frequency.

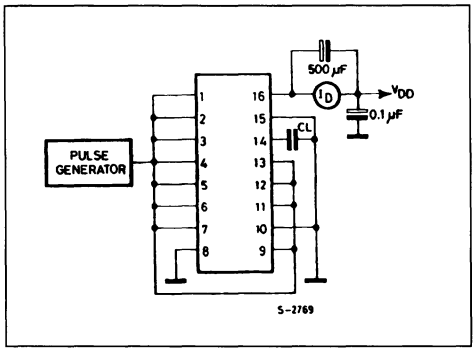



Typical Propagation Delay Time as a Function of Load Capacitance ("A" select to output).

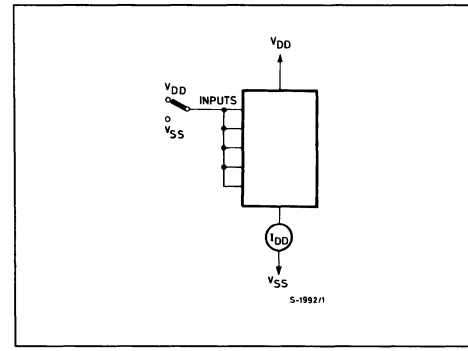


## TEST CIRCUITS

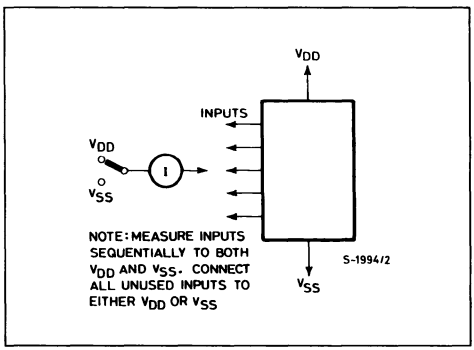
Dynamic Power Dissipation Test Circuit.



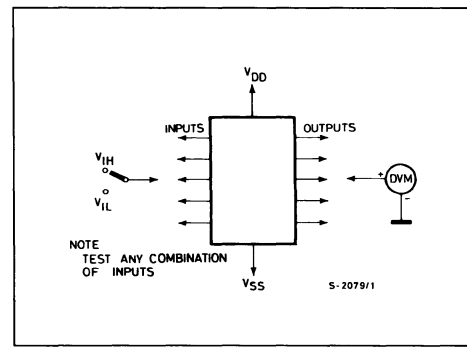

Quiescent Device Current Test Circuit.




Input Current Test Circuit.




Input Voltage Test Circuit.



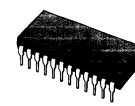
SGS-THOMSON MICROELECTRONICS

# HCC/HCF4514B
# HCC/HCF4515B

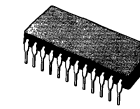
## 4-BIT LATCH/4-TO-16 LINE DECODER

**HCC/HCF4514B OUTPUT "HIGH" ON SELECT**
**HCC/HCF4515B OUTPUT "LOW" ON SELECT**

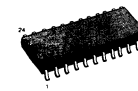
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STROBED INPUT LATCH
- INHIBIT CONTROL
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

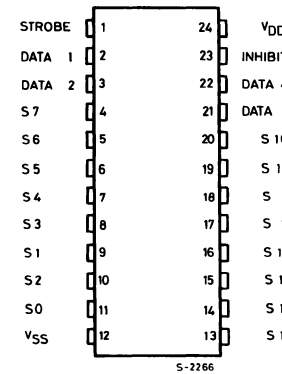


**M1**
(Micro Package)

**ORDER CODES :**

HCC45XXBF HCF45XXBEY
HCF45XXBM1

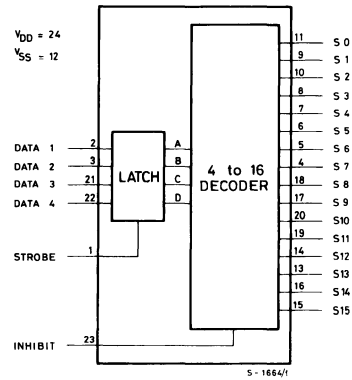
**PIN CONNECTIONS**




### DESCRIPTION

The **HCC 4514B/HCC4515B** (extended temperature range) and the **HCF 4514B/HCF4515B** (intermediate temperature range) are monolithic integrated circuits available in 24-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF4514B/4515B** consisting of a 4-bit strobed latch and a 4 to 16 line decoder. The latches hold the last input data presented prior to the strobe transition from 1 to 0. Inhibit control allows all outputs to be placed at 0 (**HCC/HCF4514B**) or 1 (**HCC/HCF4515B**) regardless of the state of the data or strobe inputs. The decode truth table indicates all combinations of data inputs and appropriate selected outputs.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

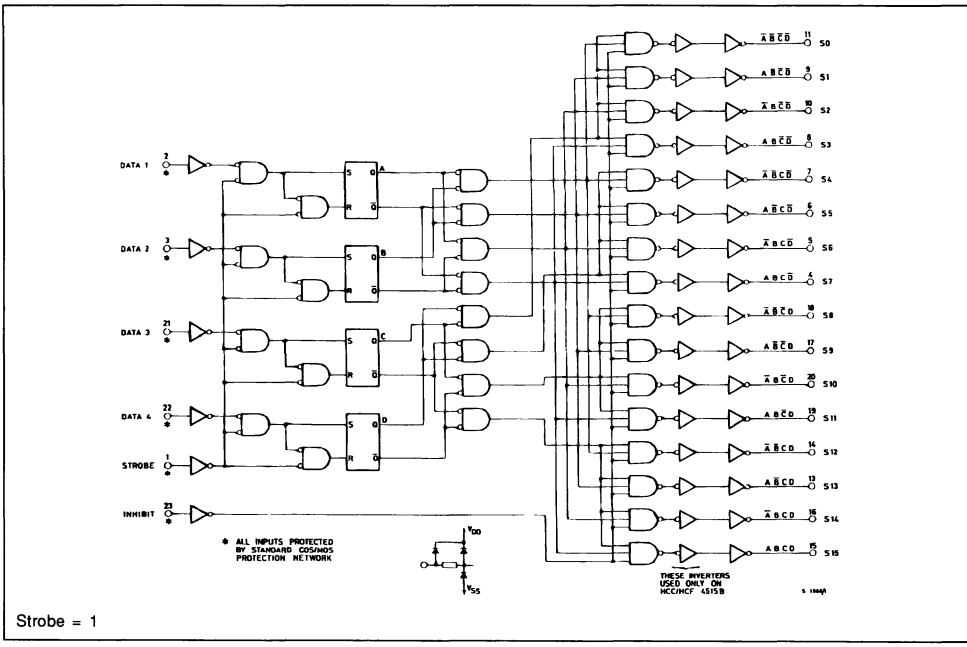
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0 5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAM AND TRUTH TABLE



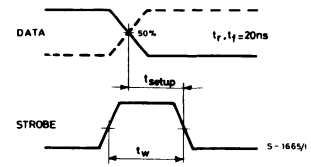

Strobe = 1

| Inhibit | Data Inputs | | | | Selected Output HCC/HCF 4514B = Logic 1 (High) HCC/HCF 4515B = Logic 0 (Low) |
|---|---|---|---|---|---|
| | D | C | B | A | |
| 0 | 0 | 0 | 0 | 0 | S0 |
| 0 | 0 | 0 | 0 | 1 | S1 |
| 0 | 0 | 0 | 1 | 0 | S2 |
| 0 | 0 | 0 | 1 | 1 | S3 |
| 0 | 0 | 1 | 0 | 0 | S4 |
| 0 | 0 | 1 | 0 | 1 | S5 |
| 0 | 0 | 1 | 1 | 0 | S6 |
| 0 | 0 | 1 | 1 | 1 | S7 |
| 0 | 1 | 0 | 0 | 0 | S8 |
| 0 | 1 | 0 | 0 | 1 | S9 |
| 0 | 1 | 0 | 1 | 0 | S10 |
| 0 | 1 | 0 | 1 | 1 | S11 |
| 0 | 1 | 1 | 0 | 0 | S12 |
| 0 | 1 | 1 | 0 | 1 | S13 |
| 0 | 1 | 1 | 1 | 0 | S14 |
| 0 | 1 | 1 | 1 | 1 | S15 |
| 1 | X | X | X | X | All Outputs = 0, HCC/HCF 4514B<br>All Outputs = 1, HCC/HCF 4515B |

X = Don't Care
1 = high

## WAVEFORMS

Setup Time and Strobe Pulse Width.



## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

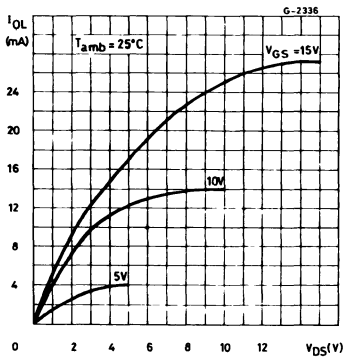
* $T_{Low}$= − 55°C for **HCC** device − 40°C for **HCF** device.
* $T_{High}$= + 125°C for **HCC** device + 85°C for **HCF** device
The Noise Margin for both "1" and "0" level is 1V min. with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2.5 V min. with $V_{DD}$ = 15V.

## DYNAMIC ELECTRICAL CHARACTERISTICS

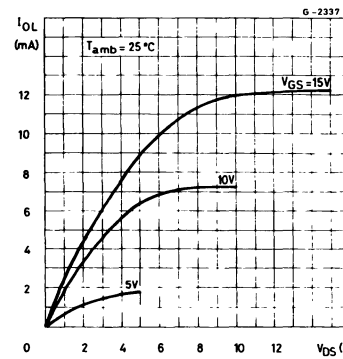
($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, all input rise and fall time = 20ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time | Strobe or Data | 5 | | 485 | 970 | ns |
| | | | 10 | | 185 | 370 | |
| | | | 15 | | 135 | 270 | |
| | | Inhibit | 5 | | 250 | 500 | ns |
| | | | 10 | | 110 | 220 | |
| | | | 15 | | 85 | 170 | |
| $t_{THL}$, $t_{THL}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_W$ | Strobe Pulse Width | | 5 | 250 | 125 | | ns |
| | | | 10 | 100 | 50 | | |
| | | | 15 | 75 | 40 | | |
| $t_{setup}$ | Setup Time | | 5 | 150 | 75 | | ns |
| | | | 10 | 70 | 35 | | |
| | | | 15 | 40 | 20 | | |

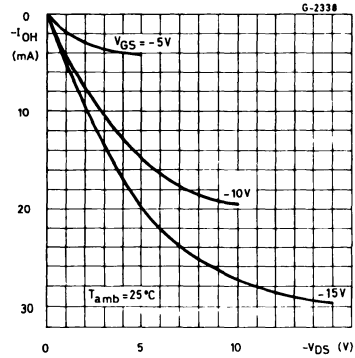
Typical Output Low (sink) Current Characteristics.



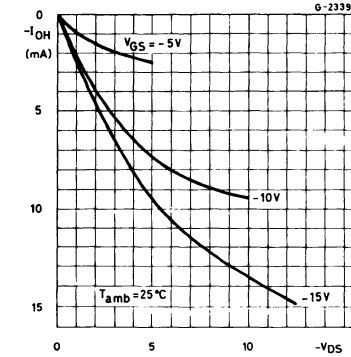

Minimum Output Low (sink) Current Characteristics.



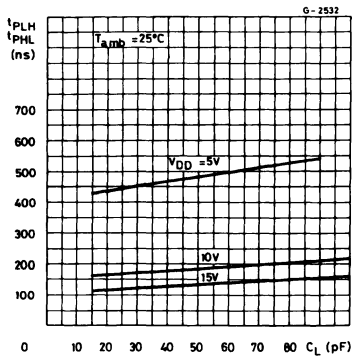
Typical Output High (source) Current Characteristics.



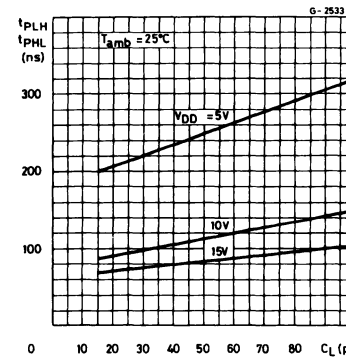

Minimum Output High (source) Current Characteristics.



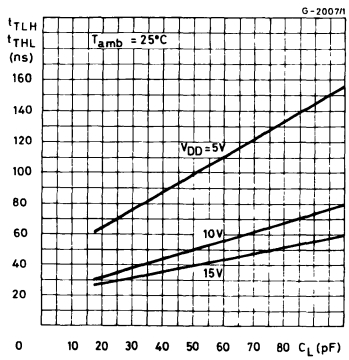

Typical Strobe or Data Propagation Delay Time vs. Load Capacitance.



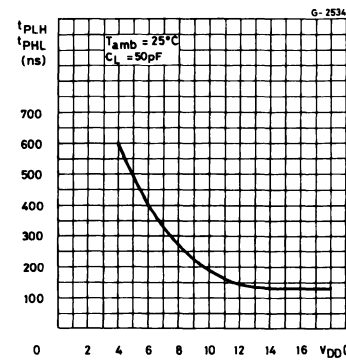

Typical Inhibit Propagation Delay Time vs. Load Capacitance.



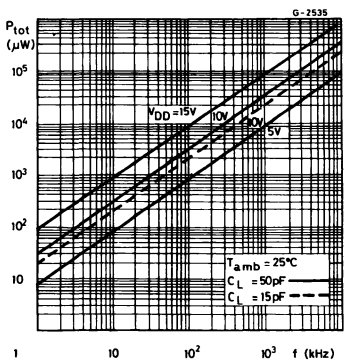

Typical Transition Time vs. Load Capacitance.




Typical Strobe or Data Propagation Delay Time vs. Supply Voltage.

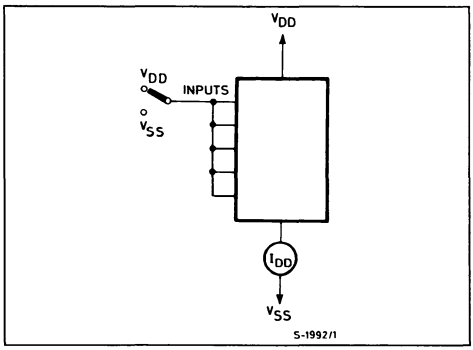


Typical Power Dissipation vs. Frequency.

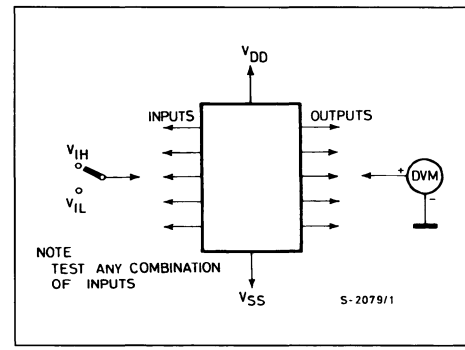



## TEST CIRCUITS

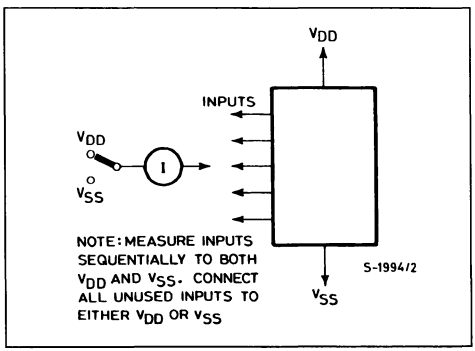
Quiescent Device Current.




Noise Immunity.




Input Leakage Current.

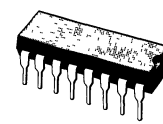


SGS-THOMSON MICROELECTRONICS

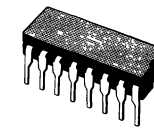
# HCC/HCF4517B

## DUAL 64-STAGE STATIC SHIFT REGISTER

- CLOCK FREQUENCY 12MHz (TYP.) AT $V_{DD}$ = 10V
- SCHMITT TRIGGER CLOCK INPUTS ALLOW OPERATION WITH VERY SLOW CLOCK RISE AND FALL TIMES
- THREE-STATE OUTPUTS
- QUIESCENT CURRENT SPECIFIED AT 20V FOR HCC DEVICE
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURREN OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)

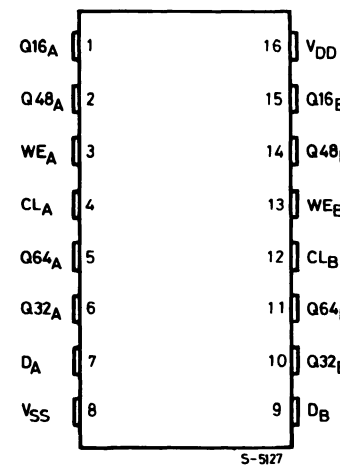


**F**
(Ceramic Package)

**C1**
(Chip Carrier)

**ORDER CODES :**
HCC4517BF HCF4517BM1
HCF4517BC1

**PIN CONNECTIONS**

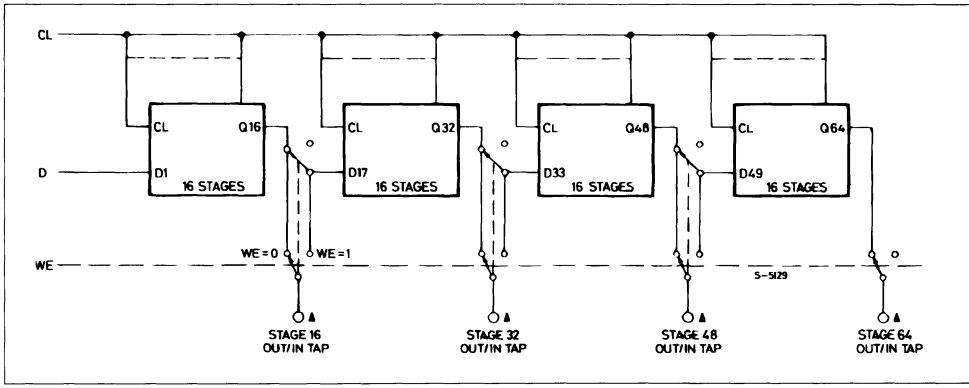



### DESCRIPTION

The **HCC4517B** (extended temperature range) and **HCF4517B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package.

The **HCC/HCF4517B** dual 64-stage static shift register consists of two independent registers each having a clock, data, and write enable input and outputs accessible at taps following the 16th, 32nd, 48th, and 64th stages. These taps also serve as input points allowing data to be inputted at the 17th, 33rd, and 49th stages when the write enable input is a logic 1 and the clock goes through a low-to-high transition. The truth table indicates how the clock and write enable inputs control the operation of the **HCC/HCF4517B**. Inputs at the intermediate taps allow entry of 64 bits into the register with 16 clock pulses. The 3-state outputs permit connection of this device to an external bus.

## FUNCTIONAL DIAGRAM (one half)




## ABSOLUTE MAXIMUM RATINGS

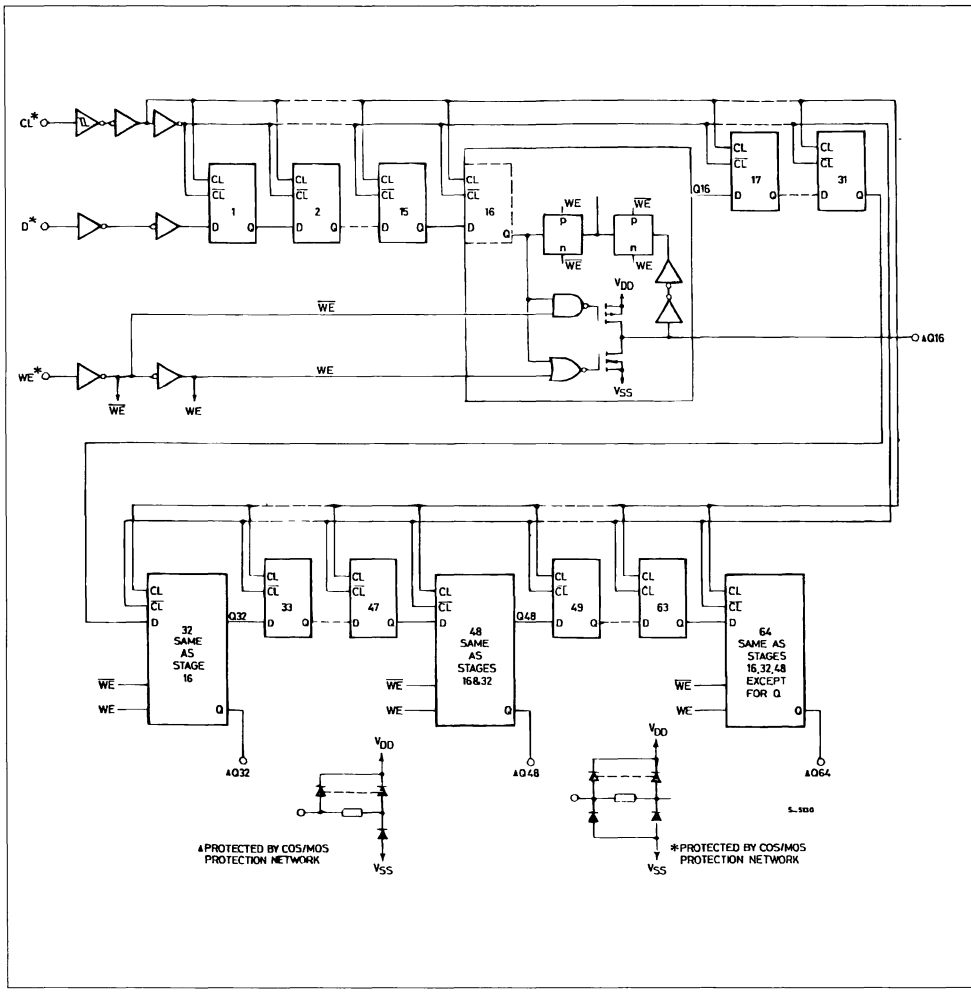
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
* All voltages are with respect to $V_{SS}$ (GND)

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAM AND TRUTH TABLE




| Clock | Write Enable | Data | Stage 16 Tap | Stage 32 Tap | Stage 48 Tap | Stage 64 Tap |
|---|---|---|---|---|---|---|
| 0 | 0 | X | Q16 | Q32 | Q48 | Q64 |
| 0 | 1 | X | Z | Z | Z | Z |
| 1 | 0 | X | Q16 | Q32 | Q48 | Q64 |
| 1 | 1 | X | Z | Z | Z | Z |
| ⎍ | 0 | DI In | Q16 | Q32 | Q48 | Q64 |
| ⎍ | 1 | DI In | D17 In | D33 In | D49 In | Z |
| ⎎ | 0 | X | Q16 | Q32 | Q48 | Q64 |
| ⎎ | 1 | X | Z | Z | Z | Z |

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3 4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $I_{OH}$, $I_{OL}$ | 3-State Output Leakage Current | HCC Types | 0/18 | | | 18 | | ± 0.4 | | $\pm 10^{-4}$ | ± 0.4 | | ± 12 | μA |
| | | HCF Types | 0/18 | | | 15 | | ± 1.0 | | $\pm 10^{-4}$ | ± 1.0 | | ± 7.5 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

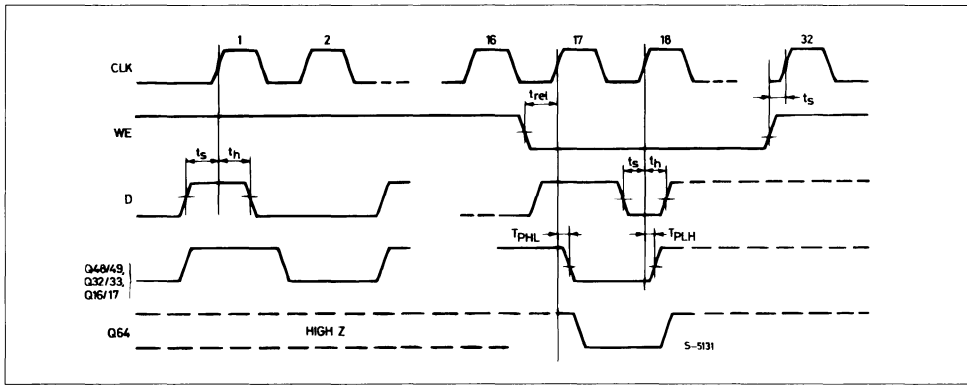
* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device . + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min with $V_{DD}$ = 15V,

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, Input $t_r$, $t_f$ = 20ns, $C_L$ = 50pF, $R_L$ = 200kΩ)

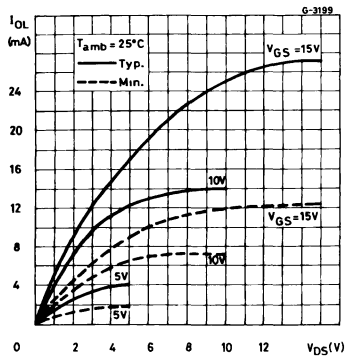
| Symbol | Parameter | Test Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time : CL to Bit 16 Tap | 5 | | 200 | 400 | ns |
| | | 10 | | 110 | 220 | |
| | | 15 | | 90 | 180 | |
| $t_{PLZ}$, $t_{PHZ}$ $t_{PZL}$, $t_{PZH}$ | 3-State Output WE to Bit 16 Tap (see note) | 5 | | 75 | 150 | ns |
| | | 10 | | 40 | 80 | |
| | | 15 | | 30 | 60 | |
| $t_{THL}$, $t_{TLH}$ | Output Transition Time | 5 | | 100 | 200 | ns |
| | | 10 | | 50 | 100 | |
| | | 15 | | 40 | 80 | |
| $t_{setup}$ | Write Enable to Clock | 5 | − 100 | − 50 | | ns |
| | | 10 | − 50 | − 25 | | |
| | | 15 | − 30 | − 15 | | |
| $t_{setup}$ | Data to Clock | 5 | − 100 | − 50 | | ns |
| | | 10 | − 60 | − 30 | | |
| | | 15 | − 30 | − 15 | | |
| | Write Enable to Clock Release Time | 5 | | 50 | 100 | ns |
| | | 10 | | 25 | 50 | |
| | | 15 | | 20 | 40 | |
| $t_{hold}$ | Data to Clock | 5 | | 100 | 200 | ns |
| | | 10 | | 50 | 100 | |
| | | 15 | | 25 | 50 | |
| $t_W$ | Minimum Clock Pulse Width | 5 | | 90 | 180 | ns |
| | | 10 | | 40 | 80 | |
| | | 15 | | 25 | 50 | |
| $f_{CL}$ | Maximum Clock Input Frequency | 5 | 3 | 6 | | MHz |
| | | 10 | 6 | 12 | | |
| | | 15 | 8 | 15 | | |
| $t_f$, $t_r$ | Maximum Clock Input Rise or Fall Time | 5 | UNLIMITED | | | µs |
| | | 10 | | | | |
| | | 15 | | | | |

**Note** Measured at the point of 10% change in output load of 50pF, $R_L$ = 1kΩ to $V_{DD}$ for $t_{PZL}$, $t_{PLZ}$ and $R_L$ = 1kΩ to $V_{SS}$ for $t_{PHZ}$

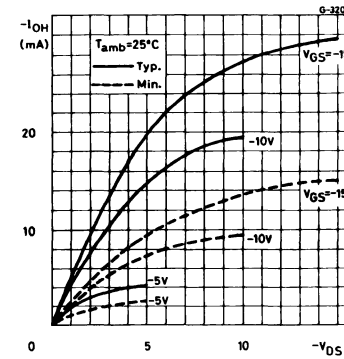
## WAVEFORMS



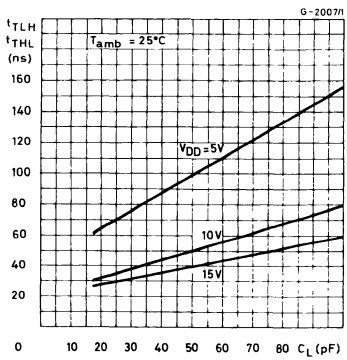

Output Low (sink) Current Characteristics.



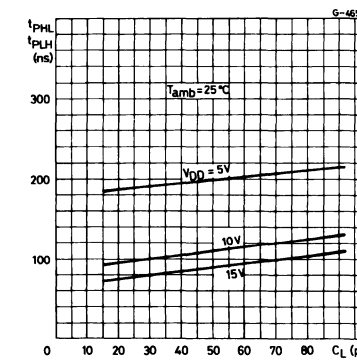

Output High (source) Current Characteristics.



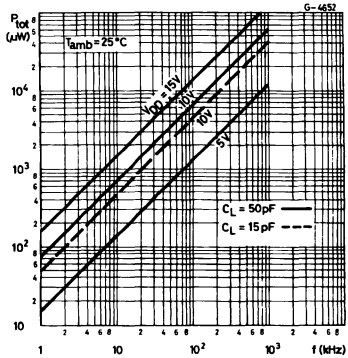

Typical Transition Time vs. Load Capacitance.



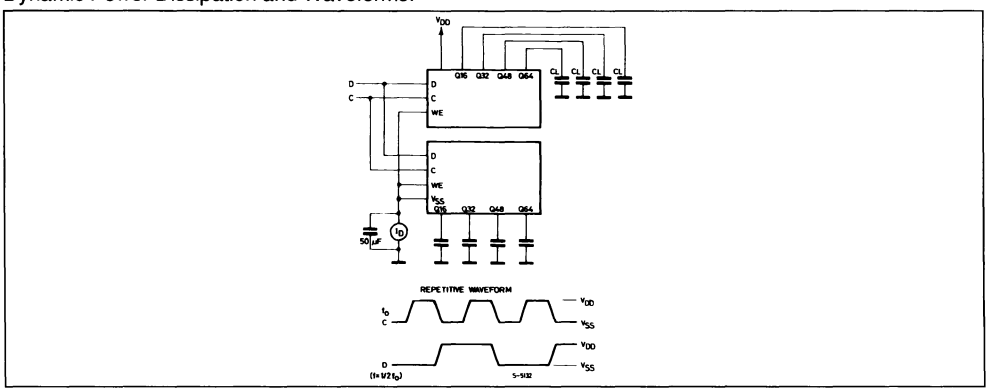

Typical Propagation Delay Time vs. Load Capacitance.



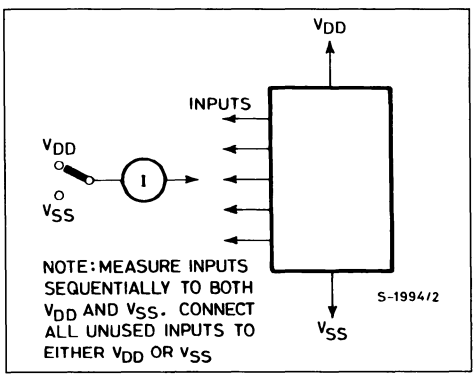
Typical Dynamic Power Dissipation vs. Frequency.

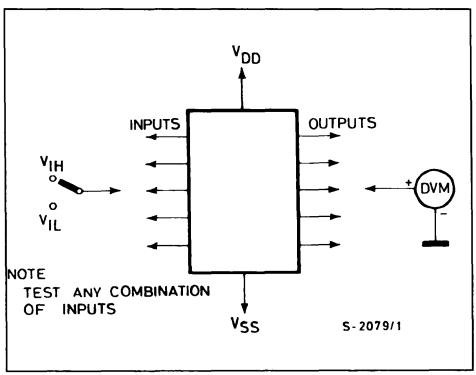



Dynamic Power Dissipation and Waveforms.

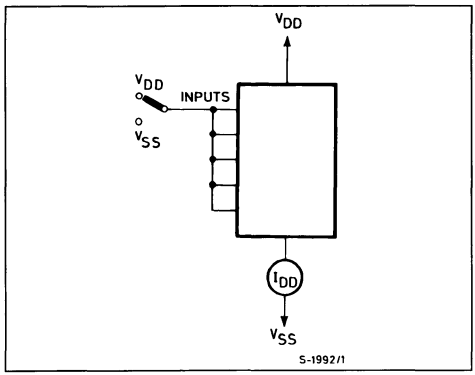



## TEST CIRCUITS



**TEST CIRCUITS** (continued)



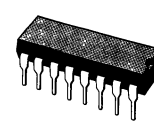
SGS-THOMSON MICROELECTRONICS

# HCC/HCF4518B HCC/HCF4520B

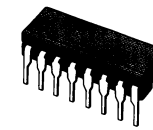
## DUAL UP-COUNTERS

**HCC/HCF4518B DUAL BCD UP-COUNTER**
**HCC/HCF4520B DUAL BINARY UP-COUNTER**

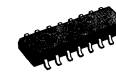
- MEDIUM-SPEED OPERATION – 6MHz TYP. CLOCK FREQUENCY AT 10V
- POSITIVE - OR NEGATIVE - EDGE TRIGGERING
- SYNCHRONOUS INTERNAL CARRY PROPAGATION
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)



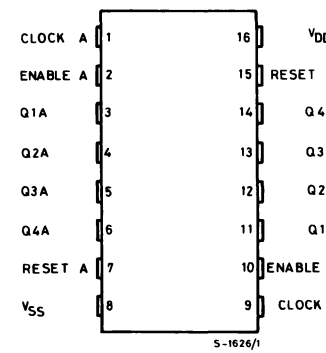
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC45XXBF HCF45XXBM1
HCF45XXBEY HCF45XXBC1

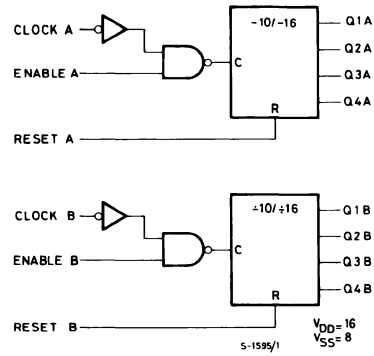
### PIN CONNECTIONS




### DESCRIPTION

The **HCC4518B/4520B** (extended temperature range) and **HCF4518B/4520B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF4518B** Dual BCD Up Counter and **HCC/HCF4520B** Dual Binary Up Counter each consist of two identical, internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition. For single-unit operation the Enable input is maintained "high" and the counter advances on each positive-going transition of the Clock. The counters are cleared by high levels on their Reset lines. The counter can be cascaded in the ripple mode by connecting Q4 to the enable input of the subsequent counter while the clock input of the latter is held low.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

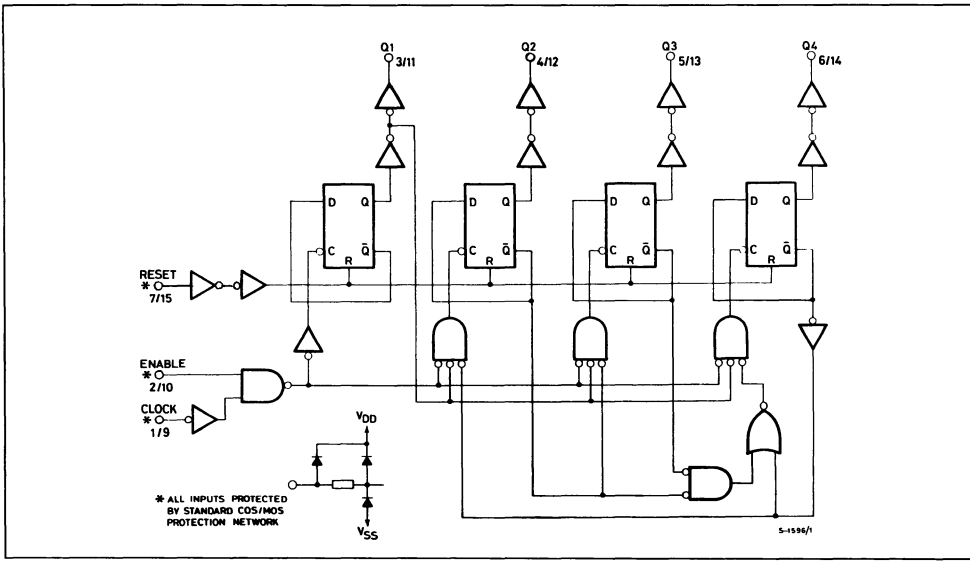
* All voltage values are referred to $V_{SS}$ pin voltage

## RECOMMENDED OPERATING CONDITIONS

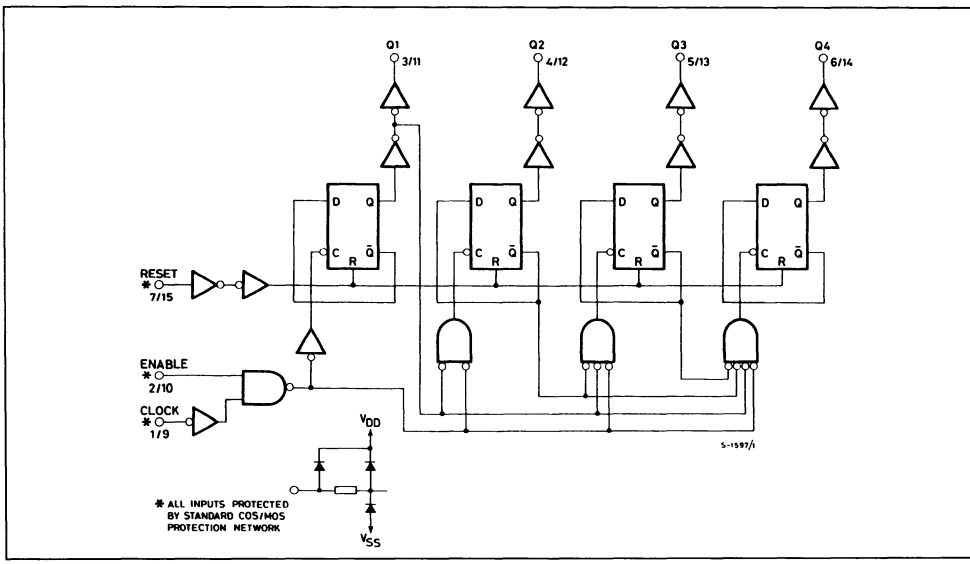
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

**LOGIC DIAGRAMS** (for one of two identical counter)

Decade Counter for 4518B.




Binary Counter for 4520B.

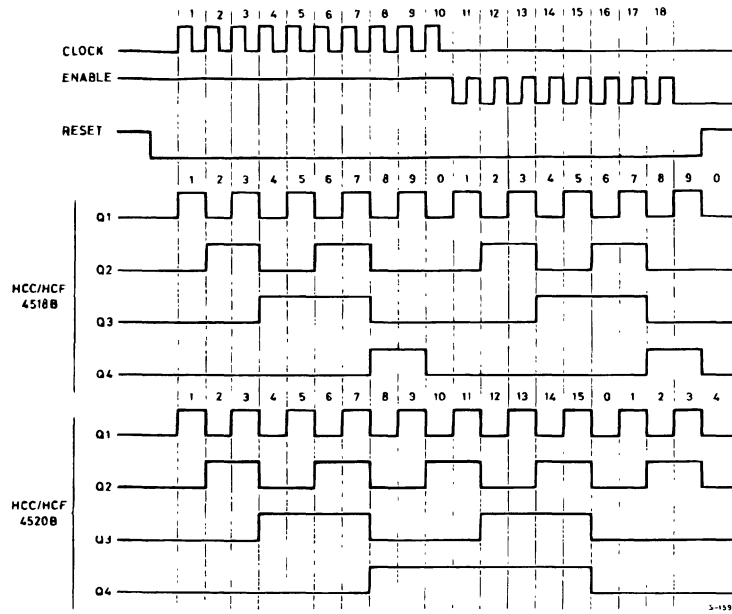


## TRUTH TABLE

| Clock | Enable | Reset | Action |
|---|---|---|---|
| _/‾ | 1 | 0 | Increment Counter |
| 0 | ‾_ | 0 | Increment Counter |
| ‾_ | X | 0 | No Change |
| X | _/‾ | 0 | No Change |
| _/‾ | 0 | 0 | No Change |
| 1 | ‾_ | 0 | No Change |
| X | X | 1 | Q1 Thru Q4 = 0 |

X = Don't Care  Logic 1 = High State  Logic 0 = Low

## TIMING DIAGRAM



**STATIC ELECTRICAL CHARACTERISTICS** (over recommended operating conditions)

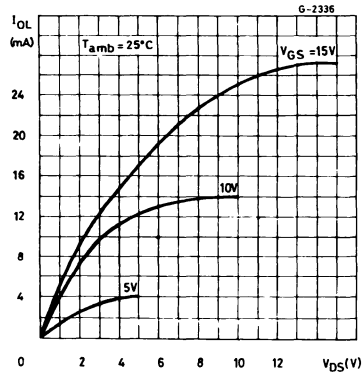
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device . − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.

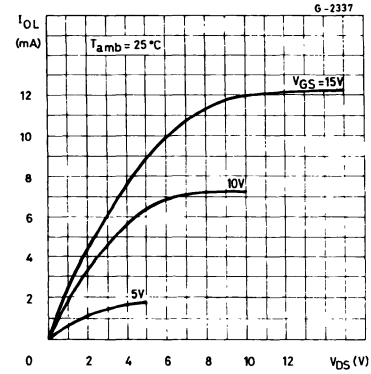
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ = 0.3%/°C values, all input rise and fall time = 20ns)

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time (clock or enable to output) | 5 | | 280 | 560 | ns |
| | | 10 | | 115 | 230 | |
| | | 15 | | 80 | 160 | |
| $t_{PLH}$, $t_{PHL}$, | Propagation Delay Time (reset to output) | 5 | | 330 | 650 | ns |
| | | 10 | | 130 | 225 | |
| | | 15 | | 90 | 170 | |
| $t_{TLH}$ ,$t_{THL}$ | Transition Time | 5 | | 100 | 200 | ns |
| | | 10 | | 50 | 100 | |
| | | 15 | | 40 | 80 | |
| $t_W$ | Clock Pulse Width | 5 | 200 | 100 | | ns |
| | | 10 | 100 | 50 | | |
| | | 15 | 70 | 35 | | |
| $t_W$ | Reset Pulse Width | 5 | 250 | 125 | | ns |
| | | 10 | 110 | 55 | | |
| | | 15 | 80 | 40 | | |
| $t_W$ | Enable Pulse Width | 5 | 400 | 200 | | ns |
| | | 10 | 200 | 100 | | |
| | | 15 | 140 | 70 | | |
| $t_r$, $t_f$ | Clock or Enable Rise and Fall Time | 5 | | | 15 | µs |
| | | 10 | | | 15 | |
| | | 15 | | | 5 | |
| $f_{max}$ | Maximum Clock Frequency | 5 | 1.5 | 3 | | MHz |
| | | 10 | 3 | 6 | | |
| | | 15 | 4 | 8 | | |
| $t_r$, $t_f$ | Clock Input Rise or Fall Time | 5 | | | 15 | µs |
| | | 10 | | | 5 | |
| | | 15 | | | 5 | |

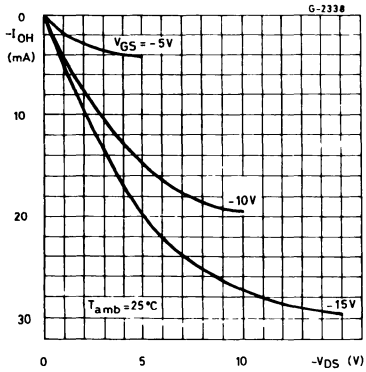
Typical Output Low (sink) Current Characteristics.



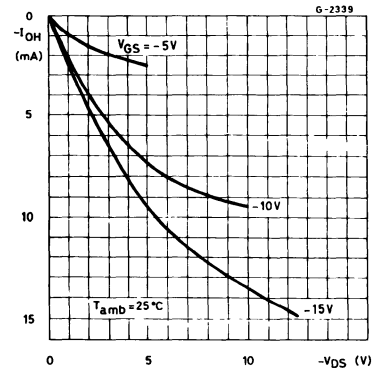

Minimum Output Low (sink) Current Characteristics.



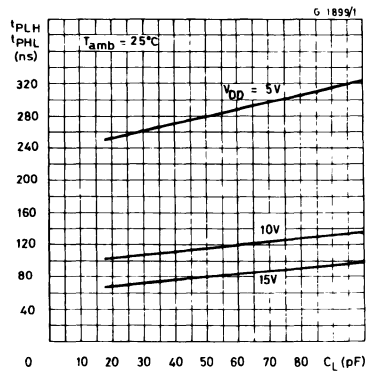

Typical Output High (source) Current Characteristics.



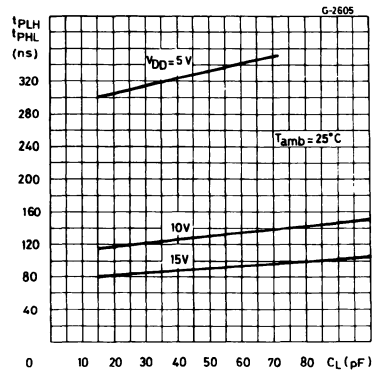

Minimum output High (source) Current Characteristics.



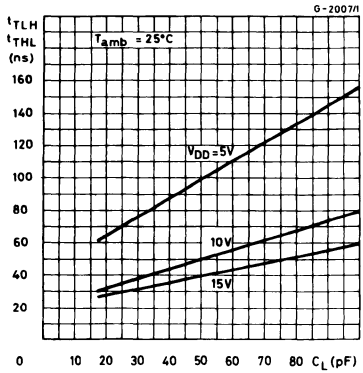

Typical Propagation Delay vs. Load Capacitance, Reset to output.



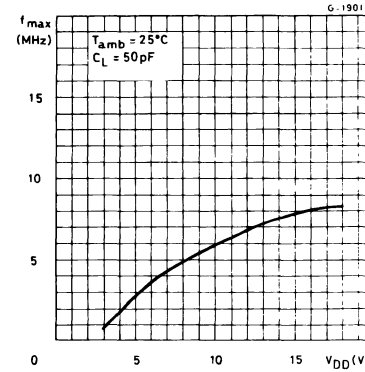

Typical Propagation Delay Time vs. Load Capacitance, Clock or Enable to Output.



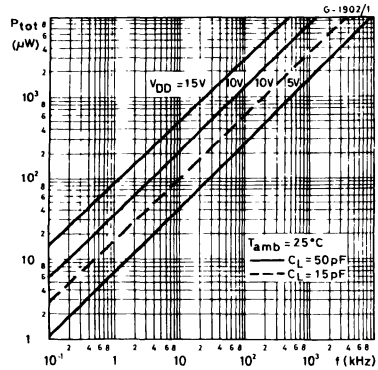
Typical Transition Time vs. load Capacitance.




Typical Maximum-clock Frequency vs, Supply Voltage.

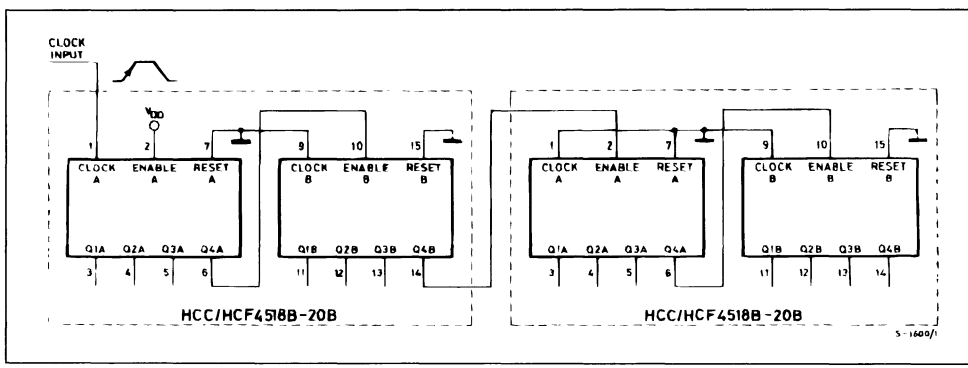



Typical Power Dissipation/Counter vs. Frequency.

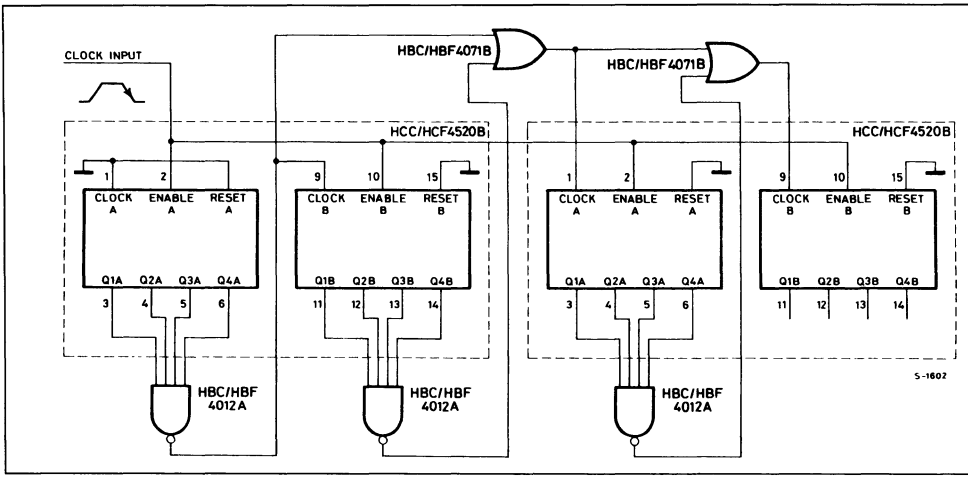



## TYPICAL APPLICATIONS

RIPPLE CASCADING OF FOUR COUNTERS WITH POSITIVE-EDGE TRIGGERING.

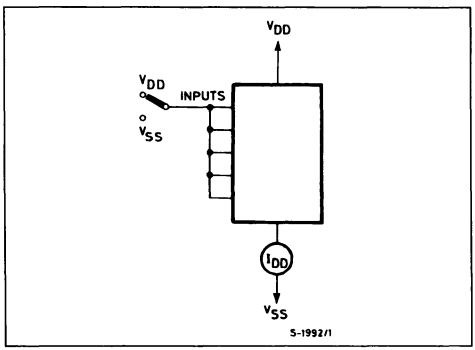


SYNCHRONOUS CASCADING OF FOUR BINARY COUNTERS WITH NEGATIVE-EDGE TRIGGERING.

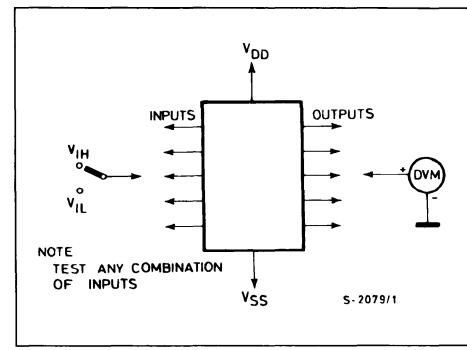



## TEST CIRCUITS

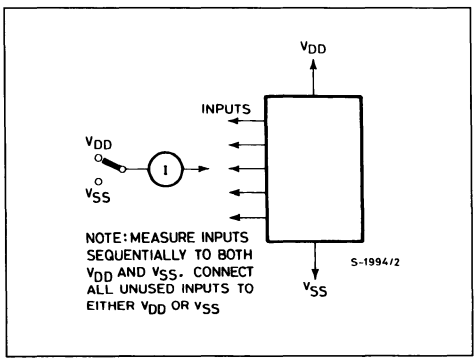
Quiescent Device Current.



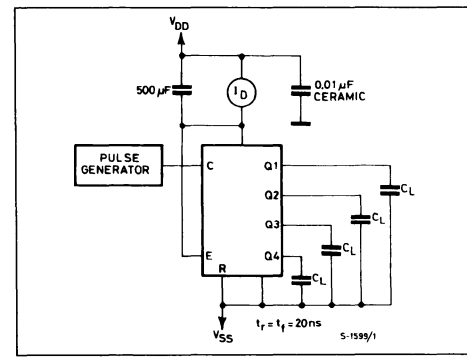

Noise Immunity.




Input Leakage Current.




Dynamic Power Dissipation.

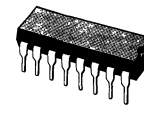


# HCC4519B
# HCF4519B

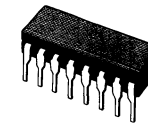
## 4 - BIT AND/OR SELECTOR

**PRODUCT PREVIEW**

- VERY LOW QUIESCENT CURRENT
- HIGH NOISE IMMUNITY
- SUPPLY VOLTAGE RANGE 3V TO 18V
- SINGLE SUPPLY VOLTAGE - POSITIVE OR NEGATIVE
- LOGIC SWING INDEPENDENT OF FANOUT



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

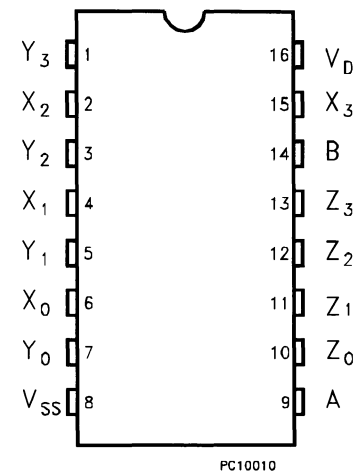
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4519 BF
HCF4519 BEY
HCF4519 BM1
HCF4519 BC1

**PIN CONNECTION** (top view)




### DESCRIPTION

The **HCC4519B** and **HCF4519B** are monolithic integrated circuits, available in 16-lead dual-in-line plastic or ceramic packages or in 16-pin SO micro-packages.

The **HCC4519B** and **HCF4519B** can be used for three different functions. They are :

1) a 4-bit and/or selector,

2) a quad 2-channel data selector,

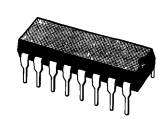
3) a quad exclusive "NOR" gate.

# HCC4521B
# HCF4521B

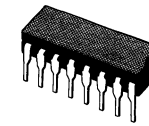
## 24 - STAGE FREQUENCY DIVIDER

**PRODUCT PREVIEW**

- VERY LOW QUIESCENT CURRENT
- HIGH NOISE IMMUNITY
- VOLTAGE SUPPLY RANGE 3V TO 18V
- ALL STAGES ARE RESETTABLE
- RESET DISABLES THE RC OSCILLATOR FOR LOW STANDBY POWER DRAIN
- RC AND CRYSTAL OSCILLATOR OUTPUT ARE CAPABLE OF DRIVING EXTERNAL LOADS



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

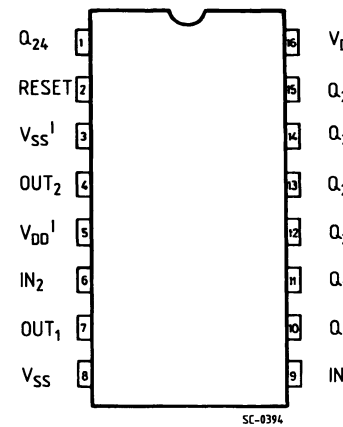
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4521 BF
HCF4521 BEY
HCF4521 BM1
HCF4521 BC1

**PIN CONNECTION** (top view)




### DESCRIPTION

The HCC4521B and HCF4521B are monolithic integrated circuits, available in 16-lead dual-in-line plastic or ceramic packages and plastic micro packages.

The HCC4521B and HCF4521B have a chain of 24 flip-flops with an input circuit that allows three modes of operation. The input circuit functions as a crystal or an RC oscillator or as an input buffer for an external oscillator. Each flip-flop preforms a divide-by-two function giving a total count of $2^{24}$ = 16, 777, 216. The count advances on the negative going edge of the clock. Access is available to the final seven stages giving the device added flexibility.

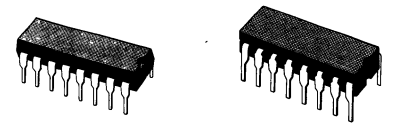
SGS-THOMSON MICROELECTRONICS

# HCC4522B
# HCF4522B

## PROGRAMMABLE BCD DIVIDER-BY-N COUNTER

**PRODUCT PREVIEW**

- VERY LOW QUIESCENT CURRENT
- HIGH NOISE IMMUNITY
- SUPPLY VOLTAGE RANGE 3V TO 18V
- INTERNALLY SYNCHRONOUS FOR HIGH INTERNAL AND EXTERNAL SPEEDS
- 5.0MHz COUNTING RATE
- INCREMENTED ON POSITIVE TRANSITION OF CLOCK OR NEGATIVE TRANSITION OF CLOCK INHIBIT
- ASYNCHRONOUS PRESET ENABLE



**EY** (Plastic Package)



**F** (Ceramic Frit Seal Package)

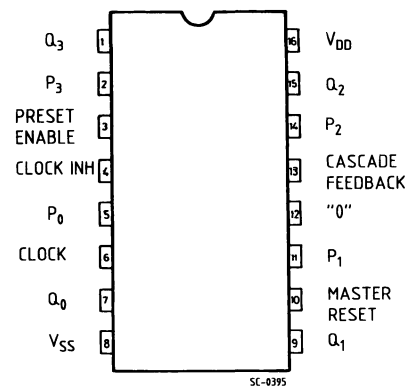
**M1** (Micro Package)

**C1** (Plastic Chip Carrier)

**ORDER CODES :**

HCC4522 BF
HCF4522 BEY
HCF4522 BM1
HCF4522 BC1

**PIN CONNECTION** (top view)




### DESCRIPTION

The HCC4522B and HCF4522B are monolithic integrated circuits, available in 16-lead dual-in-line plastic or ceramic packages and plastic micro packages.

The HCC4522B and HCF4522B are programmable, BCD down counters with a decoded "0" state output for divide-by-N applications. The counters are cascadable. In single stage applications the "0" output is applied to the Preset Enable input. The cascade feedback input allows cascade divide-by-N operation with no additional gates required. The clock Inhibit input allows disabling of the pulse counting function.

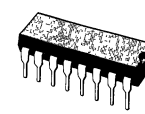
Applications for these programmable divide-by-N counters include frequency synthesizers, phase-locked loops and other frequency dividing circuits where low power and/or high noise immunity is required.

SGS-THOMSON MICROELECTRONICS

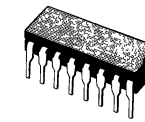
# HCC4527B
# HCF4527B

## BCD RATE MULTIPLEXER

- CASCADABLE IN MULTIPLES OF 4-BITS
- SET TO 9 INPUT AND 9 DETECT OUTPUT
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N. 13A, " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES "



**EY**
(Plastic Package)



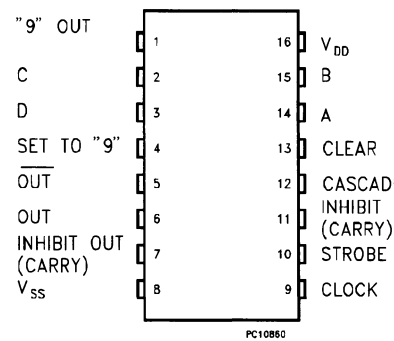
**F**
(Ceramic Package)

**C1**
(Chip Carrier)

**ORDER CODES :**

HCC4076BF
HCF4076BEY
HCF4076BC1

**PIN CONNECTIONS**

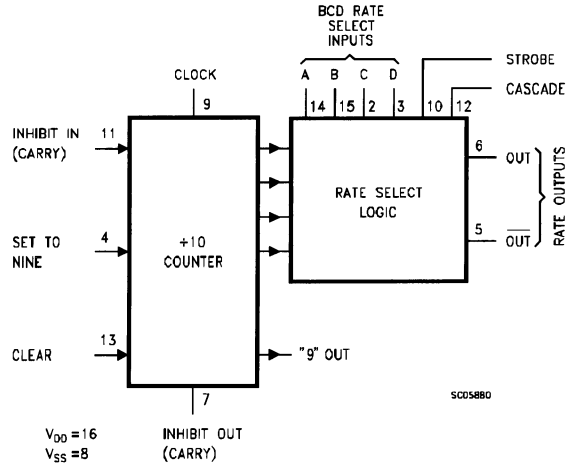



### DESCRIPTION

The **HCC4527B** (extended temperature range) and **HCF4527B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in line plastic or ceramic package.

The **HCC/HCF4527B** is a low power 4 bit digital rate multiplier that provides an output pulse rate which is the clock input pulse rate multiplied by 1/10 times the BCD input. For example, when the BCD input is 8, there will be 8 output pulses for every 10 input pulses. This device may be used to preform arithmetic operations (add, subtract, divide, raise to a power), solve algebraic and differential equations, generate naturel logarithms and trigonometric functions, A/D and D/A conversion, and frequency division.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ * | Supply Voltage: **HCC** Types<br>**HCF** Types | -0.5 to +20<br>-0.5 to +18 | V<br>V |
| $V_I$ | Input Voltage | -0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for Top = Full Package Temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |

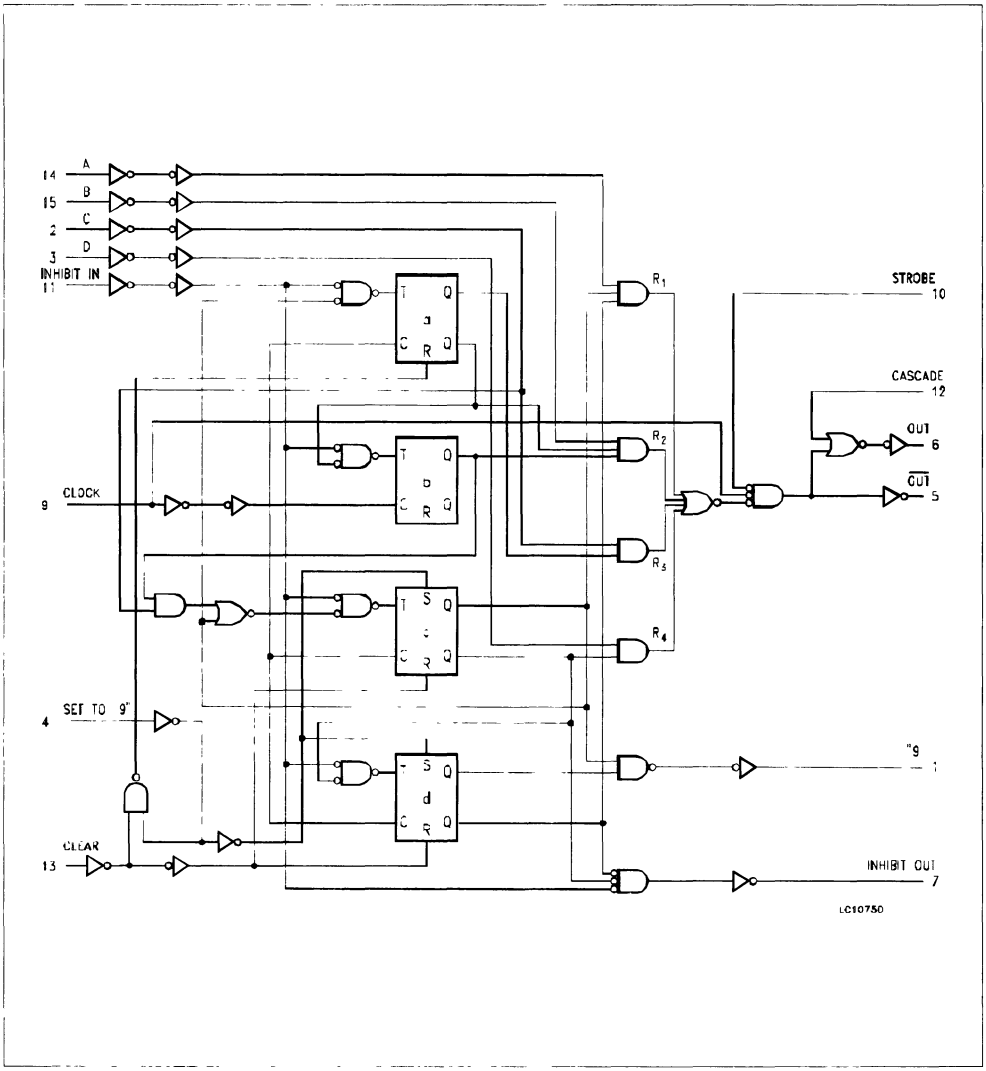
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage: **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |

## LOGIC DIAGRAM



## TRUTH TABLE

| Inputs | | | | | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Number of Pulsed or Logic Level (0 = Low; 1 = High; X = Don't Care) | | | | | | | | | | Number of Pulses or Output Logic Level (L = LOW, H = High) | | | |
| D | C | B | A | CLK | INH IN | STR | CAS | CLR | SET | OUT | $\overline{OUT}$ | INH OUT | "9" OUT |
| 0 | 0 | 0 | 0 | 10 | 0 | 0 | 0 | 0 | 0 | L | H | 1 | 1 |
| 0 | 0 | 0 | 1 | 10 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 10 | 0 | 0 | 0 | 0 | 0 | 2 | 2 | 1 | 1 |
| 0 | 0 | 1 | 1 | 10 | 0 | 0 | 0 | 0 | 0 | 3 | 3 | 1 | 1 |
| 0 | 1 | 0 | 0 | 10 | 0 | 0 | 0 | 0 | 0 | 4 | 4 | 1 | 1 |
| 0 | 1 | 0 | 1 | 10 | 0 | 0 | 0 | 0 | 0 | 5 | 5 | 1 | 1 |
| 0 | 1 | 1 | 0 | 10 | 0 | 0 | 0 | 0 | 0 | 6 | 6 | 1 | 1 |
| 0 | 1 | 1 | 1 | 10 | 0 | 0 | 0 | 0 | 0 | 7 | 7 | 1 | 1 |
| 1 | 0 | 0 | 0 | 10 | 0 | 0 | 0 | 0 | 0 | 8 | 8 | 1 | 1 |
| 1 | 0 | 0 | 1 | 10 | 0 | 0 | 0 | 0 | 0 | 9 | 9 | 1 | 1 |
| 1 | 0 | 1 | 0 | 10 | 0 | 0 | 0 | 0 | 0 | 8 | 8 | 1 | 1 |
| 1 | 0 | 1 | 1 | 10 | 0 | 0 | 0 | 0 | 0 | 9 | 9 | 1 | 1 |
| 1 | 1 | 0 | 0 | 10 | 0 | 0 | 0 | 0 | 0 | 8 | 8 | 1 | 1 |
| 1 | 1 | 0 | 1 | 10 | 0 | 0 | 0 | 0 | 0 | 9 | 9 | 1 | 1 |
| 1 | 1 | 1 | 0 | 10 | 0 | 0 | 0 | 0 | 0 | 8 | 8 | 1 | 1 |
| 1 | 1 | 1 | 1 | 10 | 0 | 0 | 0 | 0 | 0 | 9 | 9 | 1 | 1 |
| X | X | X | X | 10 | 1 | 0 | 0 | 0 | 0 | ■ | ■ | H | ■ |
| X | X | X | X | 10 | 0 | 1 | 0 | 0 | 0 | L | H | 1 | 1 |
| X | X | X | X | 10 | 0 | 0 | 1 | 0 | 0 | H | ● | 1 | 1 |
| 1 | X | X | X | 10 | 0 | 0 | 0 | 1 | 0 | 10 | 10 | H | L |
| 0 | X | X | X | 10 | 0 | 0 | 0 | 1 | 0 | L | H | H | L |
| X | X | X | X | 10 | 0 | 0 | 0 | 0 | 1 | L | H | L | H |

● Output same as the first 16 lines of this truth table (depending on value of A, B, C, D)

■ Depends on internal state of counter

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditios | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{LOW}$ * Min. | $T_{LOW}$ * Max. | 25 °C Min. | 25 °C Typ. | 25 °C Max. | $T_{HIGH}$ * Min. | $T_{HIGH}$ * Max. | |
| $I_L$ | Quiescent Current | HCC Types | 0/5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0 04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4 95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/5 | 2.5 | | 5 | -2 | | -1.6 | -3 2 | | -1.15 | | mA |
| | | | 0/5 | 4.6 | | 5 | -0.64 | | -0.51 | -1 | | -0.36 | | |
| | | | 0/10 | 9.5 | | 10 | -1.6 | | -1.3 | -2.6 | | -0.9 | | |
| | | | 0/15 | 13.5 | | 15 | -4 2 | | -3.4 | -6.8 | | -2.4 | | |
| | | HCF Types | 0/5 | 2.5 | | 5 | -1.53 | | -1.36 | -3.2 | | -1.1 | | |
| | | | 0/5 | 4.6 | | 5 | -0.52 | | -0.44 | -1 | | -0.36 | | |
| | | | 0/10 | 9.5 | | 10 | -1.3 | | -1.1 | -2.6 | | -0.9 | | |
| | | | 0/15 | 13.5 | | 15 | -3.6 | | -3.0 | -6.8 | | -2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2 4 | | |
| | | HCF Types | 0/5 | 0.4 | | 5 | 0.53 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | | 0/18 | Any Input | | 18 | | ±0.1 | | $±10^{-5}$ | ±0.1 | | ±1 | μA |
| | | | 0/15 | | | 15 | | ±0.3 | | $±10^{-5}$ | ±0.3 | | ±1 | μA |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{LOW}$ = -55 °C for **HCC** device: -40 °C for **HCF** device

* $T_{HIGH}$ = +125 °C for **HCC** device: +85 °C for **HCF** device

The Noise Margin for both "1" and "0" level is: 1V min. with $V_{DD}$ = 5 V, 2 V min. with $V_{DD}$ = 10 V, 2.5 V min with $V_{DD}$ = 15 V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 KΩ, typical temperature coefficent for all $V_{DD}$ values is 03 %/°C, all input rise and fall times= 20 ns)

| Symbol | Parameter | Test Conditions | Value | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time Clock to Output) | | 5 | | 110 | 220 | ns |
| | | | 10 | | 55 | 110 | |
| | | | 15 | | 45 | 90 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time Clock or Strobe to Output | | 5 | | 150 | 300 | ns |
| | | | 10 | | 75 | 150 | |
| | | | 15 | | 60 | 120 | |
| $t_{PLH}$ | Propagation Delay Time Clock to Inhibit Output | | 5 | | 320 | 640 | ns |
| | | | 10 | | 145 | 290 | |
| | | | 15 | | 100 | 200 | |
| $t_{PHL}$ | Propagation Delay Time Clock to Inhibit Output | | 5 | | 250 | 500 | ns |
| | | | 10 | | 100 | 200 | |
| | | | 15 | | 75 | 150 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time Clear to Output | | 5 | | 380 | 760 | ns |
| | | | 10 | | 175 | 550 | |
| | | | 15 | | 130 | 260 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time Clock to "9" or "1" Q Output | | 5 | | 300 | 600 | ns |
| | | | 10 | | 125 | 250 | |
| | | | 15 | | 90 | 180 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time Cascade to Output | | 5 | | 90 | 180 | ns |
| | | | 10 | | 45 | 90 | |
| | | | 15 | | 35 | 70 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time Inhibit Input to Inhibit Output | | 5 | | 130 | 260 | ns |
| | | | 10 | | 60 | 120 | |
| | | | 15 | | 45 | 90 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time Set to Output | | 5 | | 330 | 660 | ns |
| | | | 10 | | 150 | 300 | |
| | | | 15 | | 110 | 220 | |
| $t_{THL}$ $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $f_{CL}$ | Maximum Clock Frequency | | 5 | 1 2 | 2.4 | | MHz |
| | | | 10 | 2.5 | 5 | | |
| | | | 15 | 3.5 | 7 | | |
| $t_W$ | Clock Pulse Width | | 5 | 330 | 165 | | ns |
| | | | 10 | 170 | 85 | | |
| | | | 15 | 100 | 50 | | |
| $t_r$, $t_f$ | Clock Rise or Fall Time | | 5 | | | 15 | µs |
| | | | 10 | | | 15 | |
| | | | 15 | | | 15 | |
| $t_W$ | Set or Clear Pulse Width | | 5 | 160 | 80 | | ns |
| | | | 10 | 90 | 45 | | |
| | | | 15 | 60 | 30 | | |
| $t_{setup}$ | Inhibit Input Setup Time | | 5 | 100 | 50 | | ns |
| | | | 10 | 40 | 20 | | |
| | | | 15 | 20 | 10 | | |

## DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_R$ | Inhibit Input Removal Time | | 5 | 240 | 120 | | ns |
| | | | 10 | 130 | 65 | | |
| | | | 15 | 110 | 55 | | |
| $t_R$ | Set Remova Time | | 5 | 150 | 75 | | ns |
| | | | 10 | 80 | 40 | | |
| | | | 15 | 50 | 25 | | |
| $t_R$ | Clear Removal Time | | 5 | 60 | 30 | | ns |
| | | | 10 | 40 | 20 | | |
| | | | 15 | 30 | 15 | | |

## APPLICATION NOTE

For fractional multipliers with more than one digit, HCC/HCF4527B devices may be cascated in two different modes: the Add mode and the MItiply mode (see figures 1 and 2).

When two units are cascated in Add mode and programmed to 9 and 4 respectively, the more significant unit will have 9 output pulses for every 10 input pulses and the other unit will have 4 output pulses for every 100 input pulses for a total of:

$$\frac{9}{10}+\frac{4}{100}=\frac{94}{100}$$

In the multiply mode, the fraction programmed into the first rate multiplier is multiplied by the fraction programmed into the second one:

If $N_1 = 9$ and $N_2 = 4$

$$f_{out2}=\frac{4}{10}\,f_{out1}$$

$$f_{out1}=\frac{9}{10}\,f_{clock}$$

$$f_{out2}=\frac{4}{10}\times\left(\frac{9}{10}\,f_{clock}\right)=\frac{36}{100}\,f_{clock}$$

Therefore 36 output pulses for every 100 clock input pulses.

Fig. 1: Two **HCC/HCF4527B** Cascaded in The "Add" Mode With a Preset Number

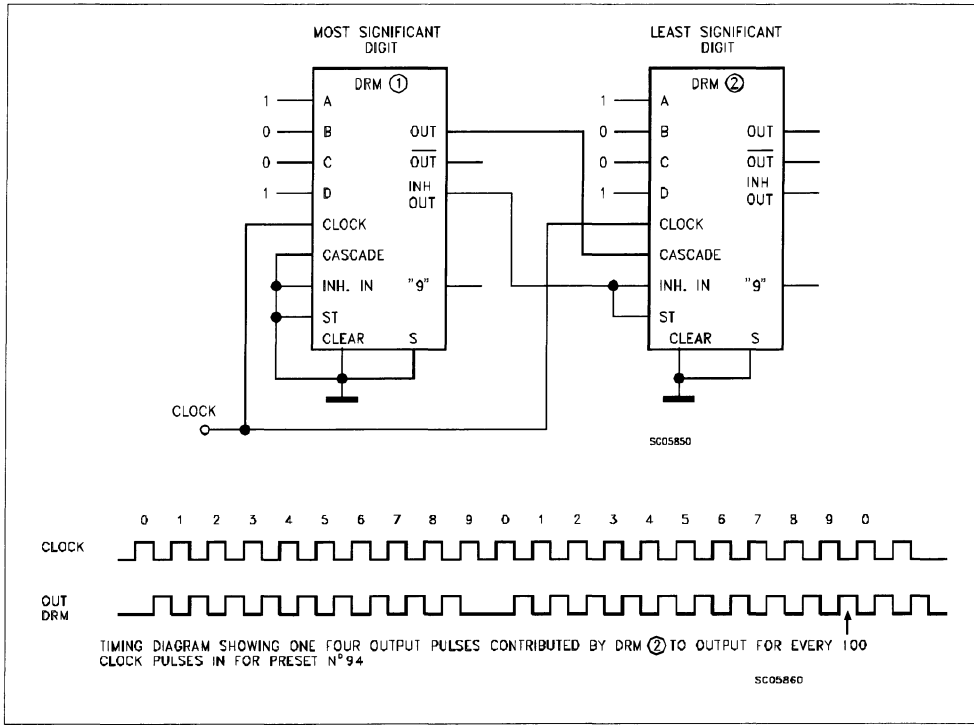



Fig. 2: Two **HCC/HCF4527B** Cascaded in The "Multiply" Mode With a Preset Number

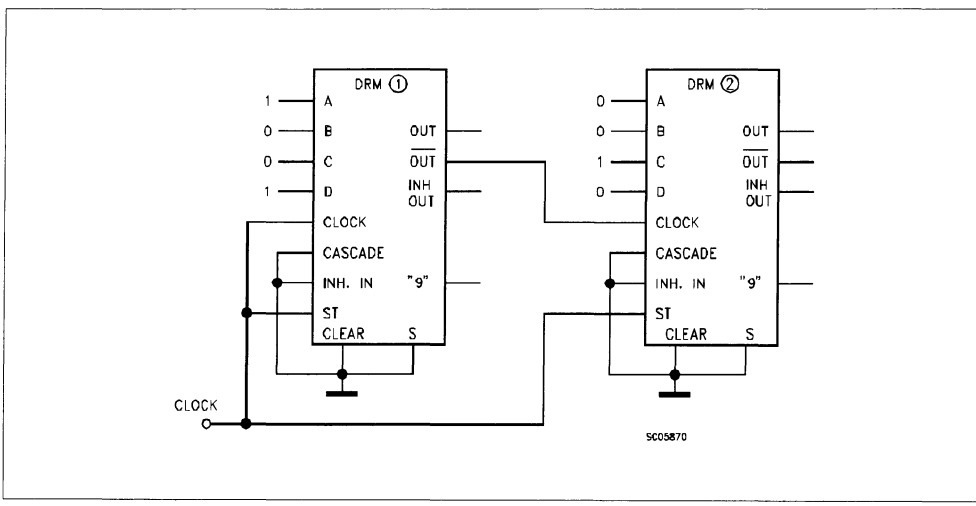
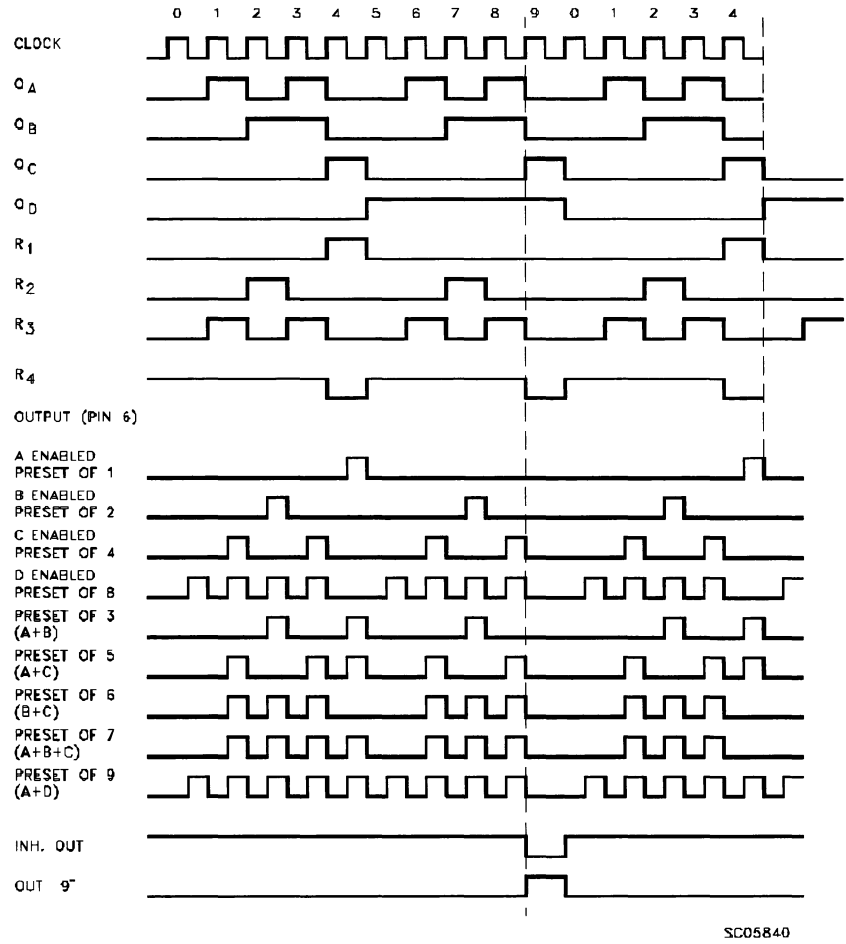


Fig. 3: Timing Diagram (see Logic Diagram)

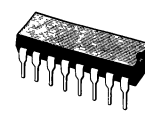


SGS-THOMSON MICROELECTRONICS

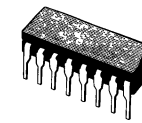
# HCC4529B
# HCF4529B

## DUAL 4-CHANNEL OR SINGLE 8-CHANNEL ANALOG DATA SELECTOR

- DATA PATHS ARE BIDIRECTIONAL
- 10 MHz OPERATION (typical)
- 3-STATE OUTPUTS
- "ON" RESISTANCE 125 W TYPICAL @ 15V
- SUPPLY VOLTAGE RANGE = 3Vdc TO 18Vdc



**EY**
(Plastic Package)



**F**
(Ceramic Package)

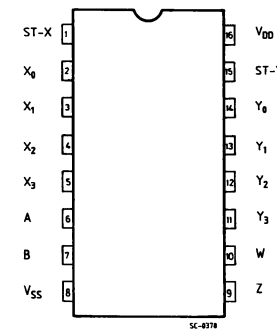
**M1**
(Micro Package)

**C1**
(Chip Carrier)

**ORDER CODES :**

| | |
|---|---|
| HCC4529BF | HCF4529BM1 |
| HCF4529BEY | HCF4529BC1 |

**PIN CONNECTIONS**




### DESCRIPTION

The HCC4529B (extended temperataure range) and HCF4529b (intermediate temperature range) are monolithic integrated circuits available in 16-lead dual in line plastic or ceramic package and plastic micropackage.

The HCC/HCF4529b is a DUAL 4-CHANNEL or 8-CHANNEL device. One of the two possible functions can be selected by a proper input coding. For the single 8-bit mode Z and W output must be tied together.

HCC/HCF4529B is suitable for digital as well as analogue applications, including 1 of 4 and 1 of 8 data selector functions. Dual binary to 1 of 4 or single binary to 1 of 8 decoder applications can be implemented because the device allow analogue and bidirectional operation.

## ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ * | Supply Voltage: **HCC** Types<br>**HCF** Types | -0.5 to +20<br>-0.5 to +18 | V<br>V |
| $V_I$ | Input Voltage | -0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for Top = Full Package Temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

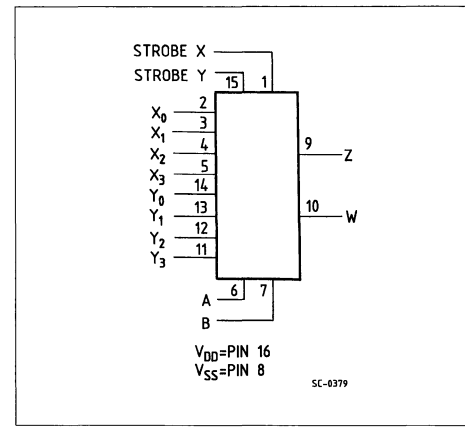
* All voltage values are referred to $V_{SS}$ pin voltage

## TRUTH TABLE

| $ST_X$ | $ST_Y$ | B | A | Z | W | MODE |
|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | X0 | Y0 | Dual 4-Channel Mode 2 Outputs |
| 1 | 1 | 0 | 1 | X1 | Y1 | |
| 1 | 1 | 1 | 0 | X2 | Y2 | |
| 1 | 1 | 1 | 1 | X3 | Y3 | |
| 1 | 0 | 0 | 0 | X0 | | Single 8-Channel Mode 1 Output (Z and W tied together) |
| 1 | 0 | 0 | 1 | X1 | | |
| 1 | 0 | 1 | 0 | X2 | | |
| 1 | 0 | 1 | 1 | X3 | | |
| 0 | 1 | 0 | 0 | Y0 | | |
| 0 | 1 | 0 | 1 | Y1 | | |
| 0 | 1 | 1 | 0 | Y2 | | |
| 0 | 1 | 1 | 1 | Y3 | | |
| 0 | 0 | X | X | High Impedance | | |

X = Don't care

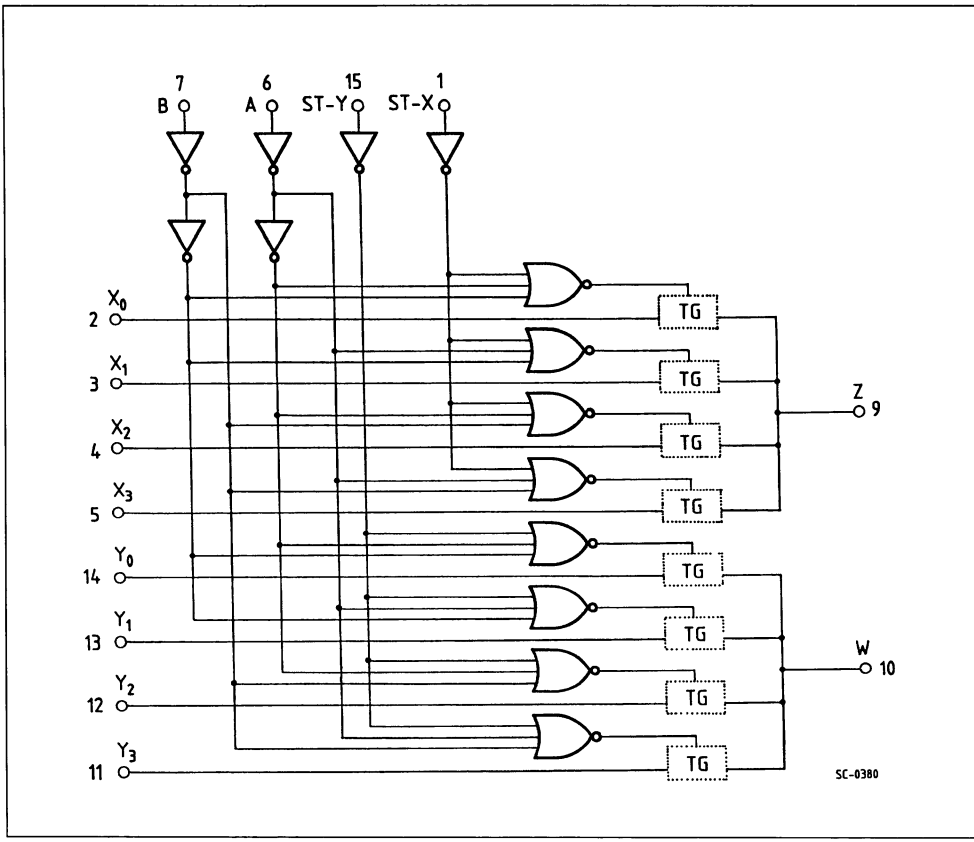
## FUNCTIONAL DIAGRAM




## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage: **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |

## BLOCK DIAGRAM



## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditios $V_{IS}$ (V) | $V_{SS}$ (V) | $V_{DD}$ (V) | Value $T_{LOW}$ * Min. | $T_{LOW}$ * Max. | 25 °C Min. | 25 °C Typ. | 25 °C Max. | $T_{HIGH}$ * Min. | $T_{HIGH}$ * Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | | | 5 | | 5 | | 0.04 | 5 | | 150 | µA |
| | | | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | | | 20 | | 100 | | 0 08 | 100 | | 3000 | |
| | | HCF Types | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| **SWITCH** | | | | | | | | | | | | | |
| ON | Resistance | HCC Types | $0 \le V_I \le V_{DD}$ | 0 | 5 | | 880 | | 470 | 1050 | | 1200 | Ω |
| | | | | | 10 | | 310 | | 180 | 400 | | 580 | |
| | | | | | 15 | | 220 | | 125 | 280 | | 400 | |
| | | HCC Types | $0 \le V_I \le V_{DD}$ | 0 | 5 | | 880 | | 470 | 1050 | | 1200 | |
| | | | | | 10 | | 330 | | 180 | 400 | | 520 | |
| | | | | | 15 | | 230 | | 125 | 280 | | 360 | |
| ΔON | Resistance $\Delta R_{ON}$ (Between any 2 channels) | | | 0 | 5 | | | | 10 | | | | Ω |
| | | | | | 10 | | | | 10 | | | | |
| | | | | | 15 | | | | 5 | | | | |
| OFF Channel Leakage Current | Any Channel OFF | HCC Types | | 0 | 18 | | 100 | | ±0 1 | 100 | | 1000 | nA |
| | All Channel OFF (common OUT/IN) | HCC Types | | 0 | 18 | | 100 | | ±0 1 | 100 | | 1000 | nA |
| | Any Channel OFF | HCC Types | | 0 | 15 | | 300 | | ±0 1 | 300 | | 1000 | nA |
| | All Channel OFF (common OUT/IN) | HCC Types | | 0 | 15 | | 300 | | ±0.1 | 300 | | 1000 | nA |
| **CONTROL** (Address or Inhibit) | | | | | | | | | | | | | |
| $V_{IL}$ | Input Low Voltage | | = $V_{DD}$ thru 1KΩ | $R_L$=1KΩ to $V_{SS}$ $I_{IS}$ < 2µA (On All OFF Channels) | 5 | | 1 5 | | | 1.5 | | 1.5 | V |
| | | | | | 10 | | 3 | | | 3 | | 3 | |
| | | | | | 15 | | 4 | | | 4 | | 4 | |
| $V_{IH}$ | Input High Voltage | | | | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | | 10 | 7 | | 7 | | | 7 | | |
| | | | | | 15 | 11 | | 11 | | | 11 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | $V_I$ = 0/18V | | 18 | | ±0 1 | | $±10^{-3}$ | ±0.1 | | ±1 | µA |
| | | HCF Types | $V_I$ = 0/15V | | 15 | | ±0.3 | | $±10^{-3}$ | ±0 3 | | ±1 | |
| $C_I$ | Input Capacitance | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{LOW}$ = -55 °C for **HCC** device -40 °C for **HCF** device

* $T_{HIGH}$ = +125 °C for **HCC** device +85 °C for **HCF** device

The Noise Margin for both "1" and "0" level is 1V min with $V_{DD}$ = 5 V, 2 V min with $V_{DD}$ = 10 V, 2 5 V min with $V_{DD}$ = 15 V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 KΩ, typical temperature coefficent for all $V_{DD}$ values is 03 %/°C, all input rise and fall times= 20 ns)

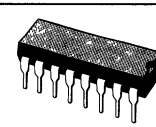
| Symbol | Parameter | Test Conditions | | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{SS}$ (V) | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$<br>$t_{PHL}$ | $V_{in}$ to $V_{out}$ Propagation Delay Time<br>($C_L$ = 50pF, $R_L$ = 1KΩ) | | 0 | 5 | | 20 | 40 | ns |
| | | | | 10 | | 10 | 20 | |
| | | | | 15 | | 8 | 15 | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay Time, Control to Output,<br>Vin = $V_{DD}$ or $V_{SS}$<br>($V_{in}$ ≤ 10 Vdc, $C_L$ = 50pF, $R_L$ = 1 KΩ) | | 0 | 5 | | 200 | 400 | ns |
| | | | | 10 | | 80 | 160 | |
| | | | | 15 | | 50 | 120 | |
| | Crosstalk, Control to Output<br>($C_L$ = 50pF, $R_L$ = 1 KΩ, $R_{out}$ = 10 KΩ) | | 0 | 5 | | 5 | | mV |
| | | | | 10 | | 5 | | |
| | | | | 15 | | 5 | | |
| | Maximum Control Input Pulse Frequency<br>($C_L$ = 50pF, $R_L$ = 1 KΩ) | | 0 | 5 | | 5 | | MHz |
| | | | | 10 | | 10 | | |
| | | | | 15 | | 12 | | |
| | Sine Wave (Distortion) ($V_{in}$ = 1.77 Vdc RMS<br>Centred @ 0.0 Vdc, $R_L$ = 10 KΩ, f = 1 KHz) | | -5 | 5 | | 0.36 | | % |
| BW | Bandwidth (-3 dB) ($V_{in}$ = 1.77 Vdc RMS<br>Centred @ 0 0 Vdc) | | -5 | 5 | | | | MHz |
| | ($R_L$ = 1KΩ) | | | | | 35 | | |
| | ($R_L$ = 10KΩ) | | | | | 28 | | |
| | ($R_L$ = 100KΩ) | | | | | 27 | | |
| | ($R_L$ = 1MΩ) | | | | | 26 | | |
| | Feedthrough and Crosstalk<br>$\left(20\ Log_{10}\frac{V_{out}}{V_{in}} = -50\ dB\right)$ | | -5 | 5 | | | | KHz |
| | ($R_L$ = 1KΩ) | | | | | 850 | | |
| | ($R_L$ = 10KΩ) | | | | | 100 | | |
| | ($R_L$ = 100KΩ) | | | | | 12 | | |
| | ($R_L$ = 1MΩ) | | | | | 1.5 | | |

SGS-THOMSON MICROELECTRONICS

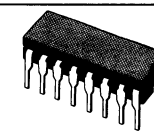
# HCC/HCF4532B

## 8–BIT PRIORITY ENCODER

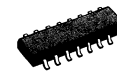
- CONVERTS FROM 1 OF 8 TO BINARY
- PROVIDES CASCADING FEATURE TO HANDLE ANY NUMBER OF INPUTS
- GROUP SELECT INDICATES ONE OR MORE PRIORITY INPUTS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)



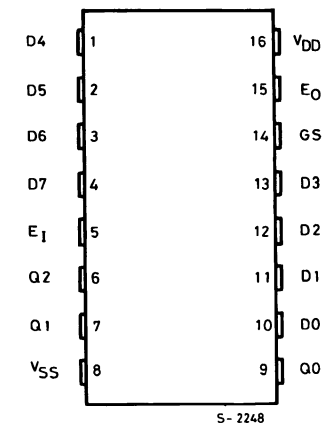
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4532BF HCF4532BM1
HCF4532BEY HCF4532BC1

**PIN CONNECTIONS**

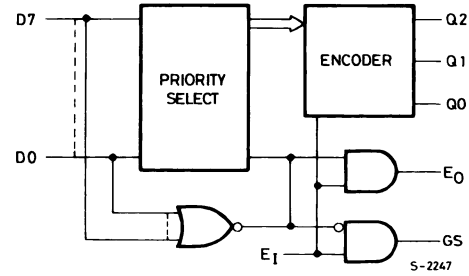



### DESCRIPTION

The **HCC4532B** (extended temperature range) and **HCF4532B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and plastic micro package.

The **HCC/HCF4532** consists of combinational logic that encodes the highest priority input (D7-D0) to a 3-bit binary code. The eight inputs, D7 through D0, each have an assigned priority. D7 is the highest priority and D0 is the lowest. The priority encoder is inhibited when the chip-enable input $E_I$ is low. When $E_I$ is high, the binary representation of the highest-priority input appears on output lines Q2-Q0, and the group select line GS is high to indicate that priority inputs are present. The enable-out ($E_O$) is high when no priority inputs are present. If any one input is high, $E_O$ is low and all cascaded lower-order stages are disabled.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

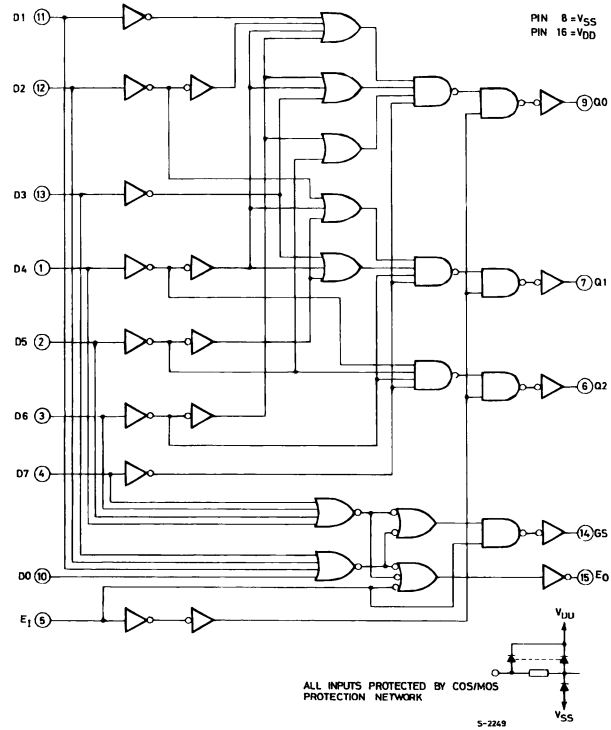
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for external periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAM




## TRUTH TABLE

| Input | | | | | | | | | Output | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $E_I$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | GS | Q2 | Q1 | Q0 | $E_O$ |
| 0 | X | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | X | X | X | X | X | X | X | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | X | X | X | X | X | X | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | X | X | X | X | X | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | X | X | X | X | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | X | X | X | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

X ≡ Don't Care  Logic 1 ≡ High  Logic 0 ≡ Low

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

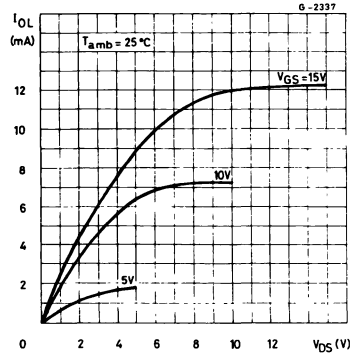
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device · + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is · 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5 V min. with $V_{DD}$ = 15V.

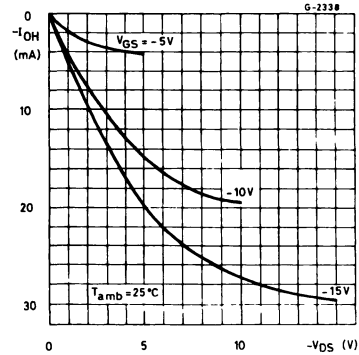
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall times = 20ns)

| Symbol | Parameter | Test Conditions | Value | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time ($E_I$ to $E_O$, $E_I$ to GS) | | 5 | | 110 | 220 | ns |
| | | | 10 | | 55 | 110 | |
| | | | 15 | | 45 | 85 | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time ($E_I$ to Qm, Dn to GS) | | 5 | | 170 | 340 | ns |
| | | | 10 | | 85 | 170 | |
| | | | 15 | | 65 | 125 | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time (Dn to $Q_M$) | | 5 | | 220 | 440 | ns |
| | | | 10 | | 110 | 220 | |
| | | | 15 | | 85 | 160 | |
| $t_{TLH}$, $t_{THL}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

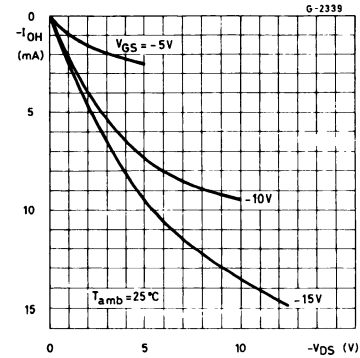
Minimum Output Low (sink) Current Characteristics.



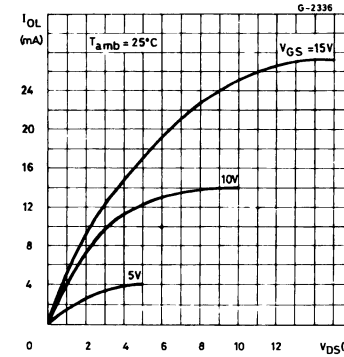

Typical Output High (source) Current Characteristics.



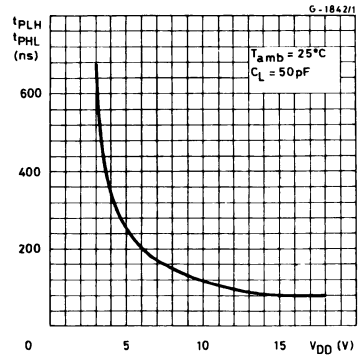
Minimum Output High (source) Current Characteristics.



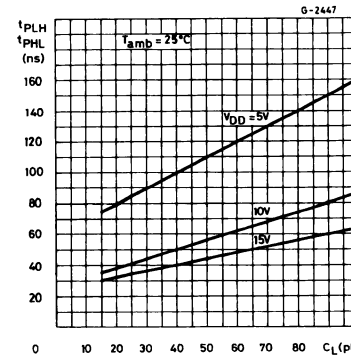

Typical Output Low (sink) Current Characteristics.



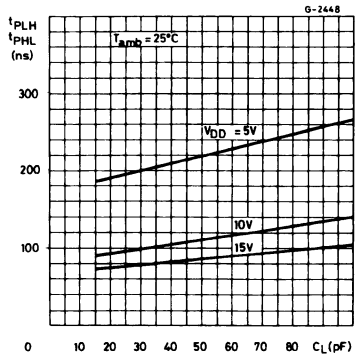

Typical Propagation Delay (Dn to Qm) vs. Supply Voltage.



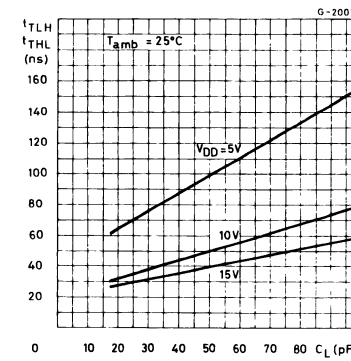

Typical Propagation Delay ($E_I$ to GS, $E_I$ to $E_O$) vs. Load Capacitance.



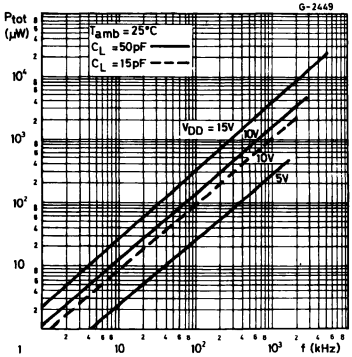

Typical Propagation Delay (Dn to Qm) vs. Load Capacitance.




Typical Transition Time vs. Load Capacitance.

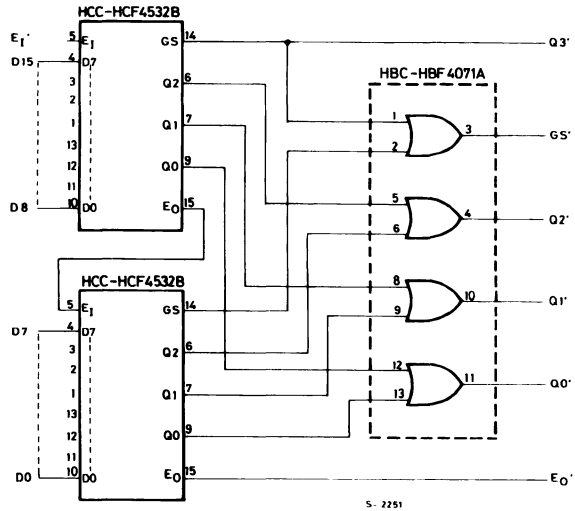


Typical Dynamic Power Dissipation vs. Frequency.



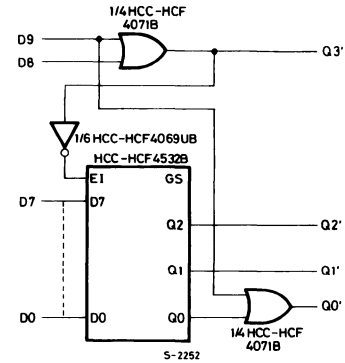

## APPLICATIONS

16-LEVEL PRIORITY ENCODER



**APPLICATIONS** (continued)

0-TO-9 KEYBOARD ENCODER



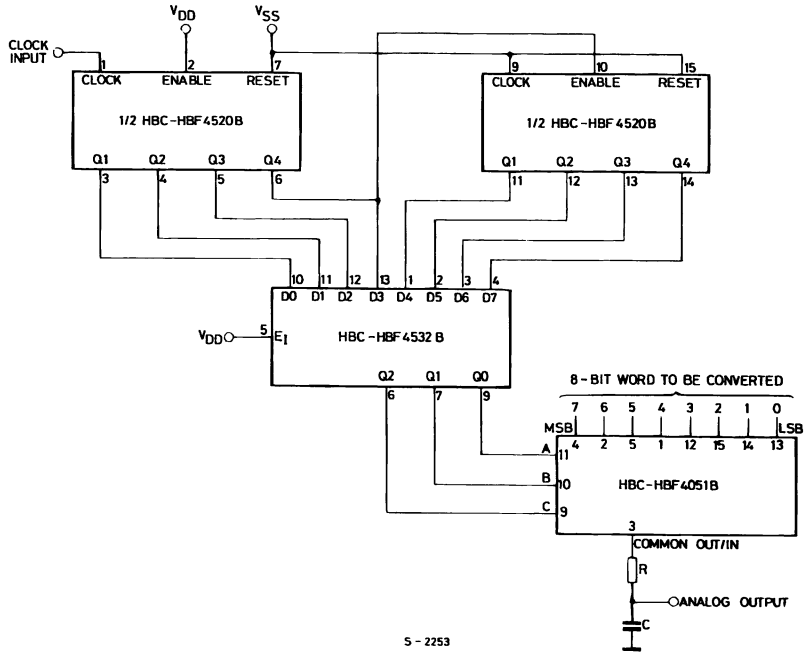

**TRUTH TABLE**

| Input | | | | | | | | | | Output | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **GS** | **Q3'** | **Q2'** | **Q1'** | **Q0** |
| 1 | X | X | X | X | X | X | X | X | X | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | X | X | X | X | X | X | X | X | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | X | X | X | X | X | X | X | 1 | 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | X | X | X | X | X | X | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | X | X | X | X | X | 1 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | X | X | X | X | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | X | 1 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

X = Don't Care  Logic 1 ≡ High  Logic 0 ≡ Low

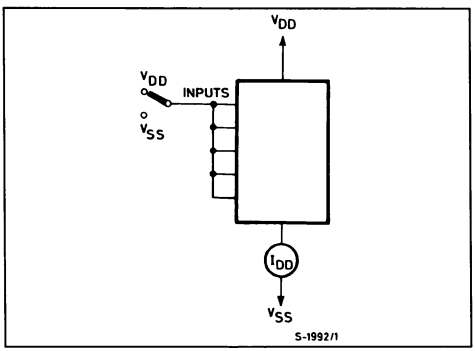
**APPLICATIONS** (continued)

DIGITAL TO ANALOG CONVERSION

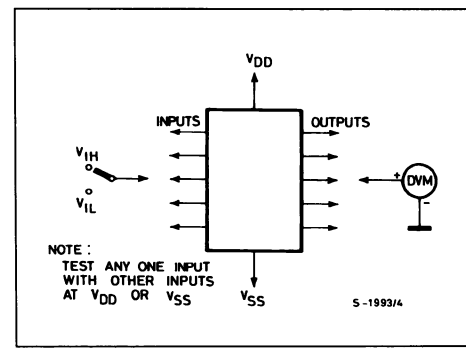



## TEST CIRCUITS

Input Leakage Current.

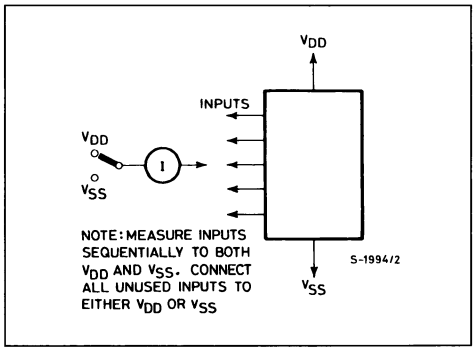



Noise Immunity.

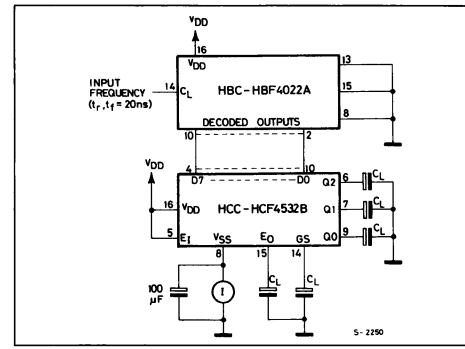


**TEST CIRCUITS** (continued)

Quiescent Device Current.



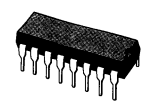

Dynamic Power Dissipation.



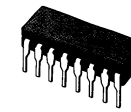
# HCC/HCF4536B

## PROGRAMMABLE TIMER

- 24 FLIP-FLOP STAGES - COUNTS FROM $2^0$ TO $2^{24}$
- LAST 16 STAGES SELECTABLE BY BCD SELECT CODE
- BYPASS INPUT ALLOWS BYPASSING FIRST 8 STAGES
- ON-CHIP RC OSCILLATOR PROVISION
- CLOCK INHIBIT INPUT
- SCHMITT-TRIGGER IN CLOCK LINE PERMITS OPERATION WITH VERY LONG RISE AND FALL TIMES
- ON-CHIP MONOSTABLE OUTPUT PROVISION
- TYPICAL $f_{CL}$ = 3MHz AT $V_{DD}$ = 10V
- TEST MODE ALLOWS FAST TEST SEQUENCE
- SET AND RESET INPUTS
- CAPABLE OF DRIVING TWO LOW POWER TTL LOADS, ONE LOWER-POWER SCHOTTKY LOAD, OR TWO HTL LOADS OVER THE RATED TEMPERATURE RANGE
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT AT 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



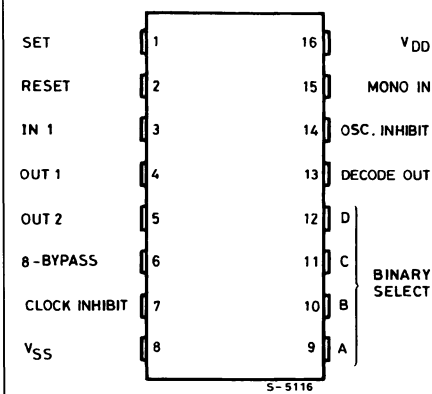
**F**
(Ceramic Package)

**C1**
(Chip Carrier)

**ORDER CODES :**

HCC4536BF HCF4536BEY
HCF4536BC1

**PIN CONNECTIONS**

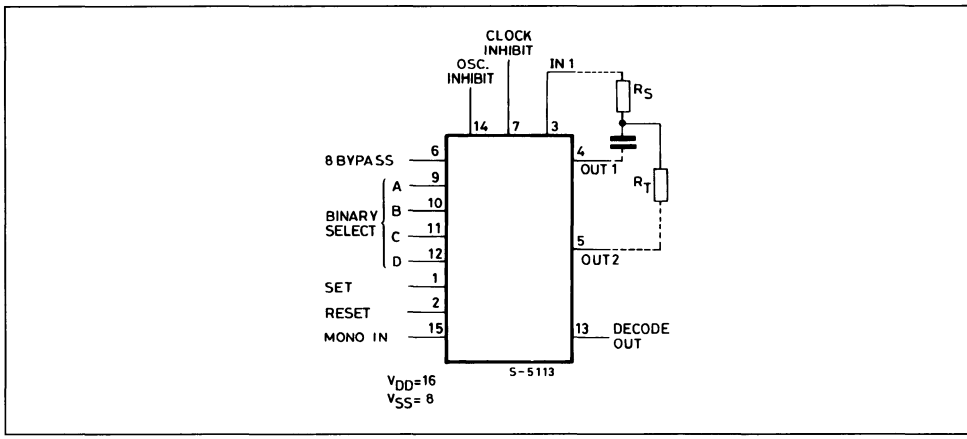



### DESCRIPTION

The **HCC4536B** (extended temperature range) and **HCF4536B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package. The **HCC/HCF4536B** is a programmable timer consisting of 24 ripple-binary counter stages. The salient feature of this device is its flexibility. The device can count from 1 to $2^{24}$ or the first 8 stages can be bypassed to allow an output, selectable by a 4-bit code, from any one of the remaining 16 stages. It can be driven by an external clock or an RC oscillator that can be constructed using on-chip components. Input IN1 serves as either

the external clock input or the input to the on-chip RC oscillator. OUT1 and OUT2 are connection terminals for the external RC components. In addition, an on-chip monostable circuit is provided to allow a variable pulse width output. Various timing functions can be achieved using combinations of these capabilities. A logic 1 on the 8-BYPASS input enables a bypass of the first 8 stages and makes stage 9 the first counter stage of the last 16 stages. Selection of 1 of 16 outputs is accomplished by the decoder and the BCD inputs A, B, C and D. MONO IN is the timing input for the on-chip monostable oscillator. Grounding of the MONO IN terminal through a resistor of 10KΩ or higher, disables the one-shot circuit and connects the decoder directly to the DECODE OUT terminal. A resistor to $V_{DD}$ and a capacitor to ground from the MONO IN terminal enables the one-shot circuit and controls its pulse width. A fast test mode is enabled by a logic 1 on 8-BYPASS, SET, and RESET. This mode divides the 24-stage counter into three 8-stage sections to facilitate a fast test sequence.

## FUNCTIONAL DIAGRAM



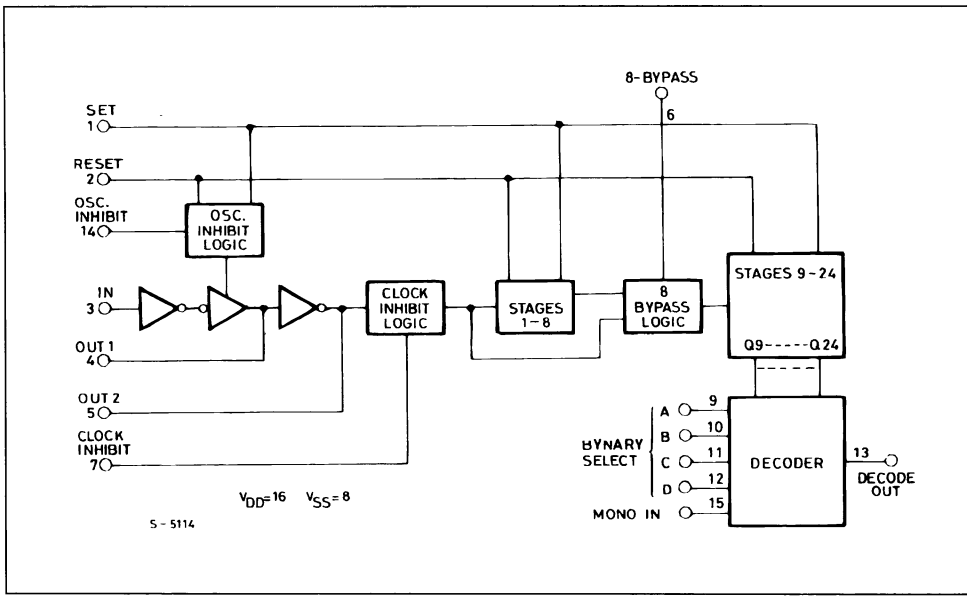

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltages are with respect to $V_{SS}$ (GND).

## BLOCK DIAGRAM




## TRUTH TABLE

| In1 | Set | Reset | Clock Inh | Osc Inh | Out1 | Out2 | Decode Out |
|---|---|---|---|---|---|---|---|
| ⎍ | 0 | 0 | 0 | 0 | ⎍ | ⎎ | No Change |
| ⎎ | 0 | 0 | 0 | 0 | ⎎ | ⎍ | Advance to Next State |
| X | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| X | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| X | 0 | 0 | 1 | 0 | | | No Change |
| 0 | 0 | 0 | 0 | X | 0 | 1 | No Change |
| 1 | 0 | 0 | 0 | ⎍ | ⎎ | ⎍ | Advance to Next State |

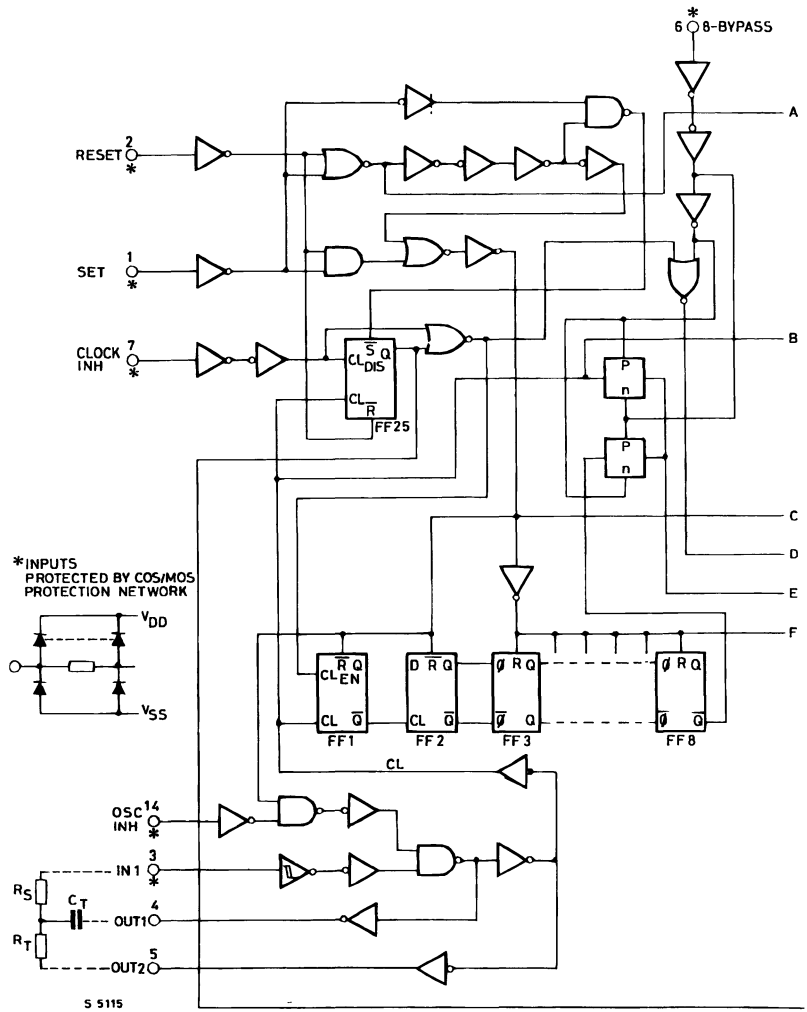
0 = Low Level 1 = High Level X = Don't Care

## DECODE OUT SELECTION TABLE

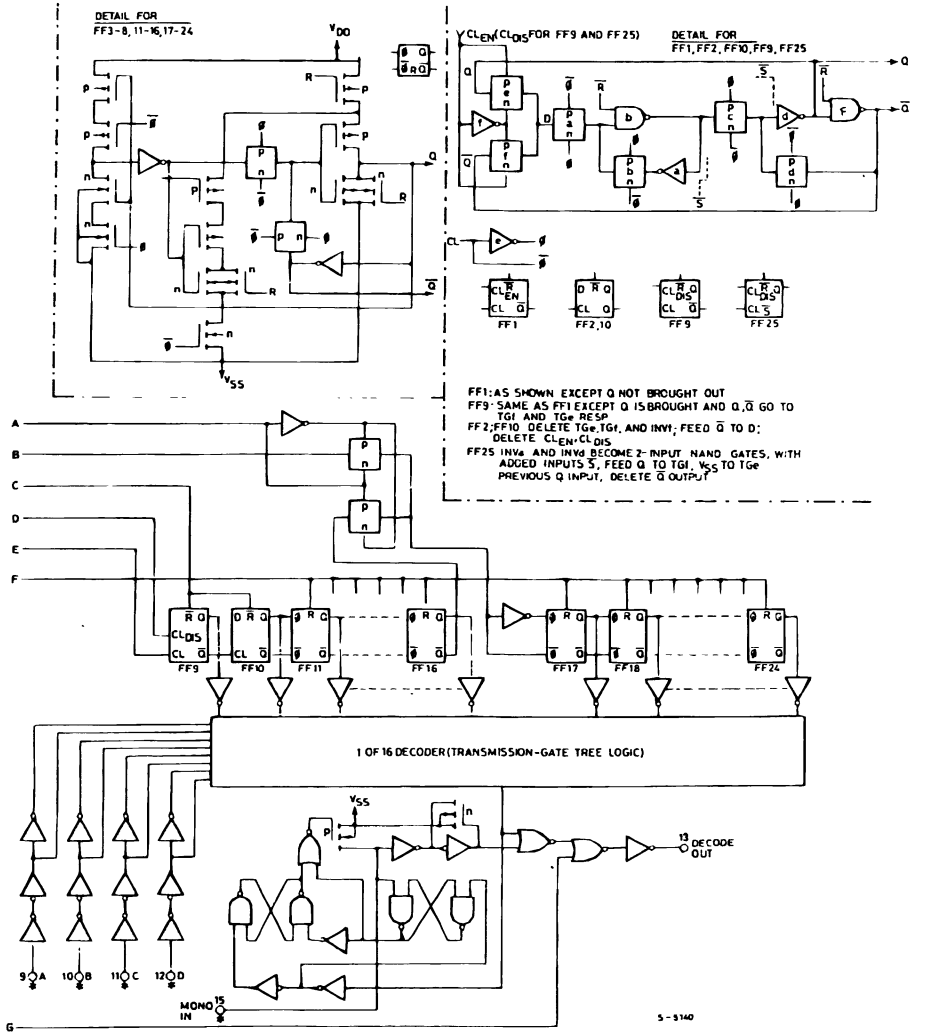
| D | C | B | A | Number or Stages In Divider Chain | |
|---|---|---|---|---|---|
| | | | | 8-BYPASS = 0 | 8-BYPASS = 1 |
| 0 | 0 | 0 | 0 | 9 | 1 |
| 0 | 0 | 0 | 1 | 10 | 2 |
| 0 | 0 | 1 | 0 | 11 | 3 |
| 0 | 0 | 1 | 1 | 12 | 4 |
| 0 | 1 | 0 | 0 | 13 | 5 |
| 0 | 1 | 0 | 1 | 14 | 6 |
| 0 | 1 | 1 | 0 | 15 | 7 |
| 0 | 1 | 1 | 1 | 16 | 8 |
| 1 | 0 | 0 | 0 | 17 | 9 |
| 1 | 0 | 0 | 1 | 18 | 10 |
| 1 | 0 | 1 | 0 | 19 | 11 |
| 1 | 0 | 1 | 1 | 20 | 12 |
| 1 | 1 | 0 | 0 | 21 | 13 |
| 1 | 1 | 0 | 1 | 22 | 14 |
| 1 | 1 | 1 | 0 | 23 | 15 |
| 1 | 1 | 1 | 1 | 24 | 16 |

0 = Low Level 1 = High Level

**LOGIC DIAGRAMS** (continued on next page)



## LOGIC DIAGRAMS (continued)



## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

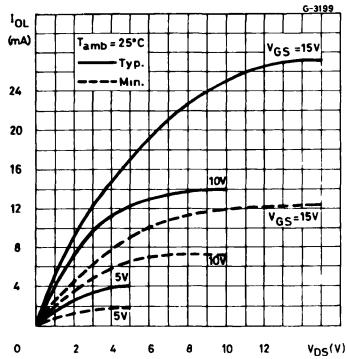
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0 05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3 5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device . − 40°C for **HCF** device
* $T_{High}$= + 125°C for **HCC** device . + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is · 1V min with $V_{DD}$ = 5V , 2V min with $V_{DD}$ = 10V, 2 5 V min with $V_{DD}$ = 15V

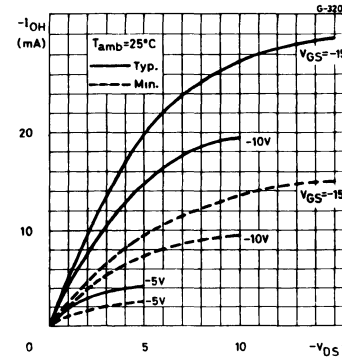
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$, 50pF, $R_L$ = 200kΩ, typical temperature coefficent for all $V_{DD}$ values is 0.3% /°C all input rise and fall time = 20ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time Clock to Q1, 8-bypass High | | 5 | | 1 | 2 | µs |
| | | | 10 | | 0.5 | 1 | |
| | | | 15 | | 0.35 | 0.7 | |
| | Clock to Q1, 8-bypass Low | | 5 | | 2.5 | 5 | µs |
| | | | 10 | | 0.8 | 0.6 | |
| | | | 15 | | 0.6 | 1.2 | |
| | Clock to Q16 | | 5 | | 4 | 8 | µs |
| | | | 10 | | 1 5 | 3 | |
| | | | 15 | | 1 | 2 | |
| | $Q_n$ to $Q_{n+1}$ | | 5 | | 150 | 300 | ns |
| | | | 10 | | 75 | 150 | |
| | | | 15 | | 50 | 100 | |
| $t_{PLH}$ | Propagation Delay Time | | 5 | | 300 | 600 | ns |
| | | | 10 | | 125 | 250 | |
| | | | 15 | | 80 | 160 | |
| $t_{PHL}$ | Reset to $Q_n$ | | 5 | | 3 | 6 | µs |
| | | | 10 | | 1 | 2 | |
| | | | 15 | | 0.75 | 1 5 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_W$ | Pulse Widht Clock | | 5 | | 200 | 400 | ns |
| | | | 10 | | 75 | 150 | |
| | | | 15 | | 50 | 100 | |
| | Set | | 5 | | 200 | 400 | ns |
| | | | 10 | | 100 | 200 | |
| | | | 15 | | 60 | 120 | |
| | Reset | | 5 | | 3 | 6 | µs |
| | | | 10 | | 1 | 2 | |
| | | | 15 | | 0.75 | 1.5 | |
| | Recovery Tıme Set | | 5 | | 2.5 | 5 | µs |
| | | | 10 | | 1 | 2 | |
| | | | 15 | | 0.6 | 1.6 | |
| | Reset | | 5 | | 3.5 | 7 | µs |
| | | | 10 | | 1.5 | 3 | |
| | | | 15 | | 1 | 2 | |
| $t_r$, $t_f$ | Clock Input Rise or Fall Time | | 5 | Unlimited | | | µs |
| | | | 10 | | | | |
| | | | 15 | | | | |
| $f_{CL}$ | Maximum Clock Input Frequency | | 5 | 0.5 | 1 | | MHz |
| | | | 10 | 1.5 | 3 | | |
| | | | 15 | 2.5 | 5 | | |

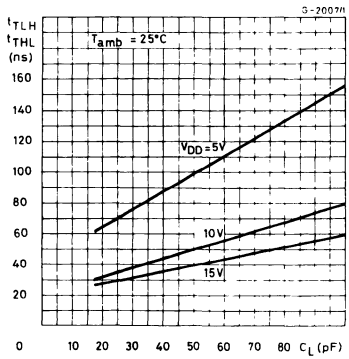
Output Low (sink) Current Characteristics.



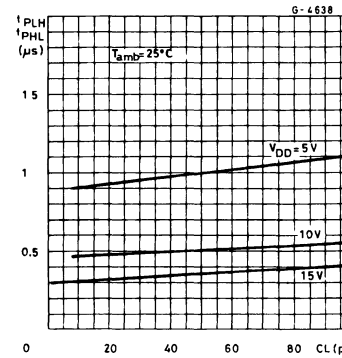

Output High (source) Current Characteristics.



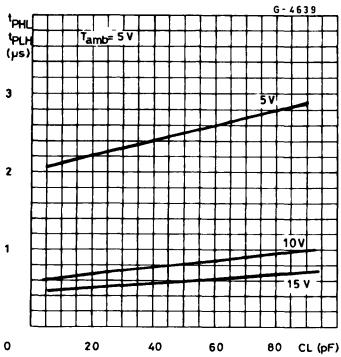

Typical Transition Time vs. Load Capacitance.



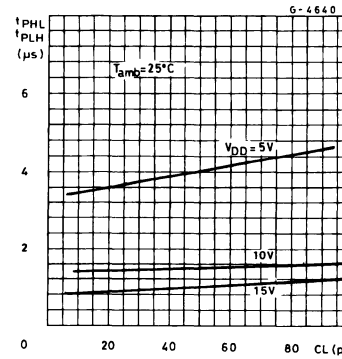

Typical Propagation Delay Time vs. Load Capacitance (clock to Q1, 8 Bypass high).



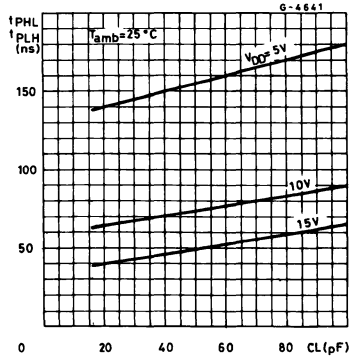

Typical Propagation Delay Time vs. Load Capacitance (Clock to Q1, 8 Bypass low).



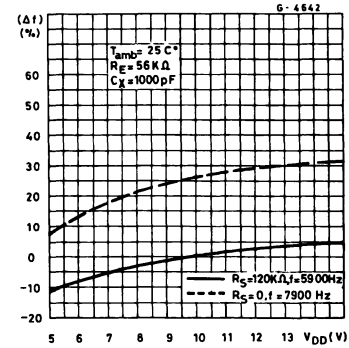

Typical Propagation Delay Time vs. Load Capacitance (Clock to Q16, 8 Bypass high).



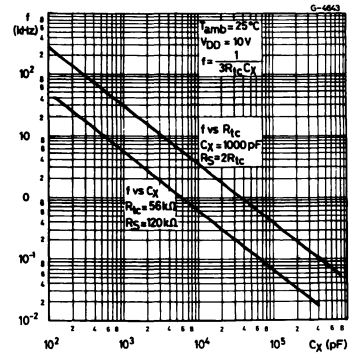
Typical Propagation Delay Time vs. Load Capacitance ($Q_N$ to $Q_{N+1}$).



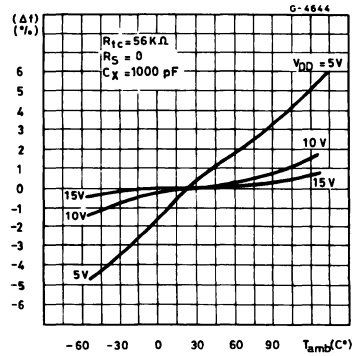

Typical RC Oscillator Frequency Deviation vs. Supply Voltage.



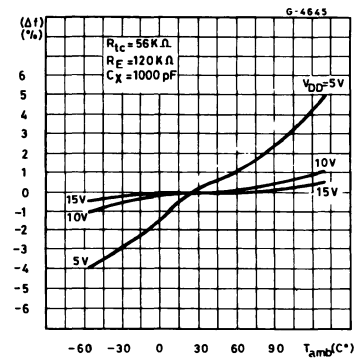

Typical RC Oscillator Frequency Deviation vs. Time Constant Resistance and Capacitance.



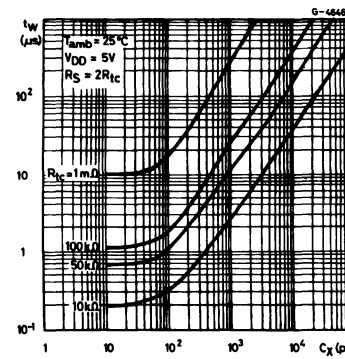

Typical RC Oscillator Frequency Deviation vs. Ambient Temperature ($R_S$ = 0).



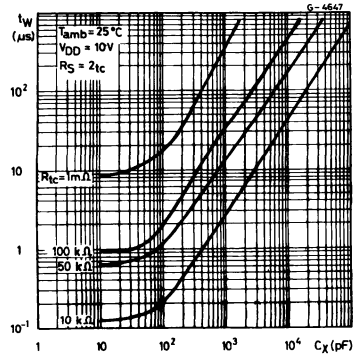

Typical RC Oscillator Frequency Deviation vs. Ambient Temperature ($R_S$ = 120KΩ).



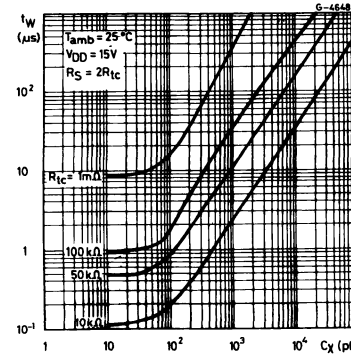

Typical Pulse Width vs. External Capacitance ($V_{DD}$ = 5V).



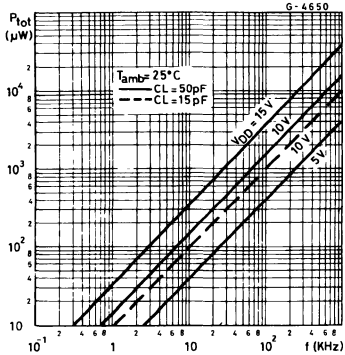
Typical Pulse Width vs. External Capacitance ($V_{DD}$ = 10V).




Typical Pulse Width vs. External Capacitance ($V_{DD}$ = 15V).

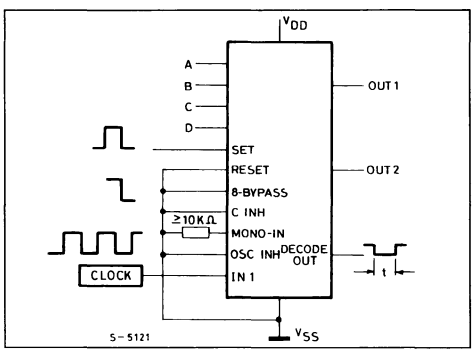



Typical Dynamic Power Dissipation vs. Input Pulse Frequency.

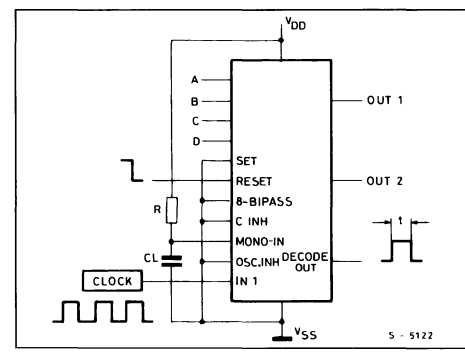



## TYPICAL APPLICATIONS

Time Internal Configuration Using External Clock ; Set and Clock Inhibit Functions.

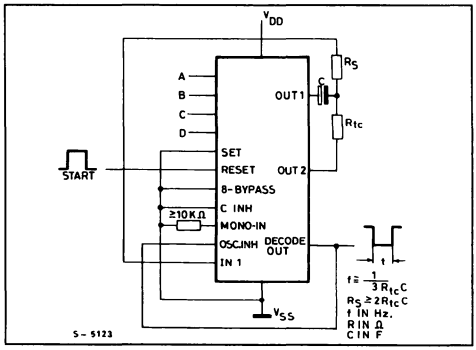



Time Internal Configuration Using External Clock ; Reset and Output Monostable to Achieve a Pulse Output.

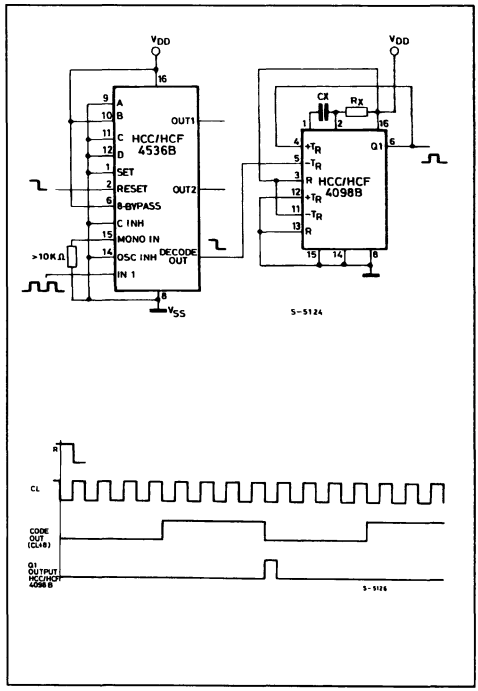


## TYPICAL APPLICATIONS (Continued)

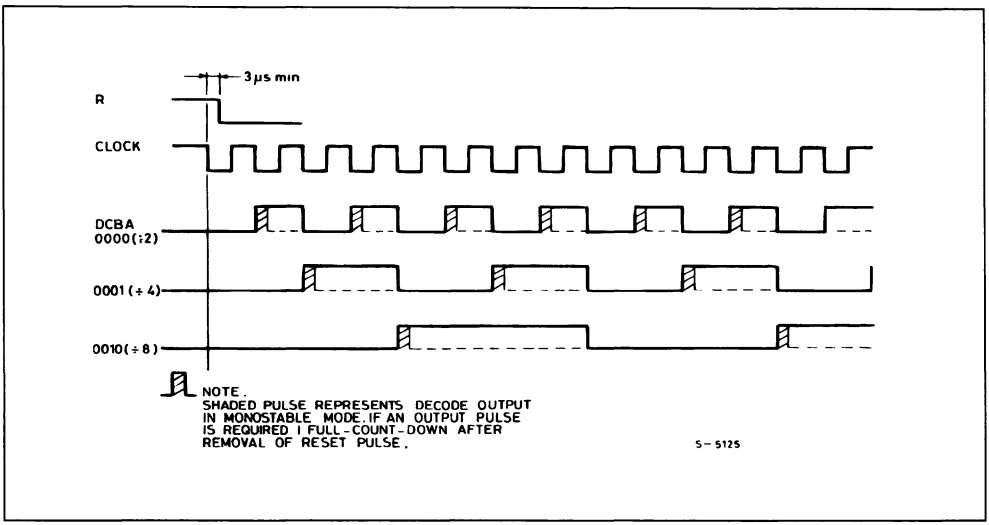
Time Internal Configuration Using Onchip RC Oscillator and Reset Input to Initiate Time Interval.




Application Showing Use of 4098B and 4536B to get Decode Pulse 8 Clock Pulses after Reset Pulse.




## TIMING DIAGRAM



| Functional Test Sequence | | | | | |
|---|---|---|---|---|---|
| Inputs | | | | Outputs | Comments |
| In1 | Set | Reset | 8-Bypass | Decade Out Q1 Thru Q24 | All 24 steps are in reset mode. |
| 1 | 0 | 1 | 1 | 0 | |
| 1 | 1 | 1 | 1 | 0 | Counter is in three 8-stage section in parallel mode. |
| 0 | 1 | 1 | 1 | 0 | First "1" to "0" Transition of Clock |
| 1<br>0<br>–<br>– | 1 | 1 | 1 | | 255 "1" to "0" transitions are clocked in the counter. |
| 0 | 1 | 1 | 1 | 1 | The 255 "1" to "0" Transition |
| 0 | 0 | 0 | 0 | 1 | Counter converted back to 24 stages in series mode.<br>Set and Reset must be connected together and simultaneoulsy go from "1" to "0". |
| 1 | 0 | 0 | 0 | 1 | $In_1$ switches to a "1". |
| 0 | 0 | 0 | 0 | 0 | Counter Ripples from an all "1" state to an all "0" state. |

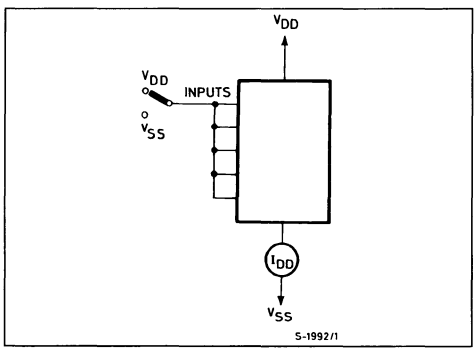
## FUNCTIONAL TEST SEQUENCE

Test Function has been included for the reduction of test time required to exercise all 24 counter stages.

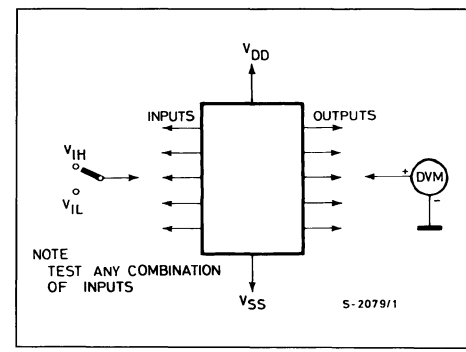
This test function divides the counter into three 8-stage section and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a "1". The counter is now returned to the normal 24-steps in series configuration. One more pulse is entered into $In_1$ which will cause the counter to ripple from an all "1" state to an all "0" state.

## TEST CIRCUITS

Quiescent Device Current.

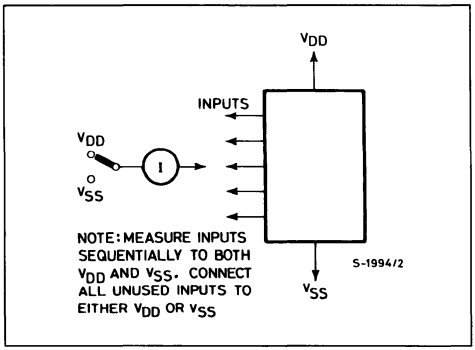



Input Voltage.

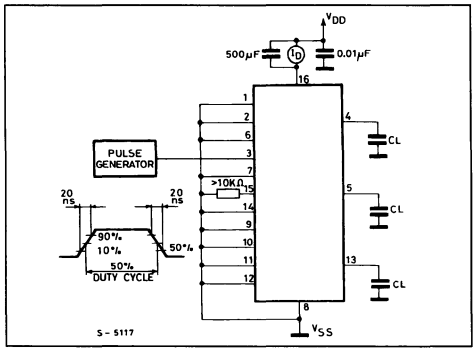


**TEST CIRCUITS** (continued)

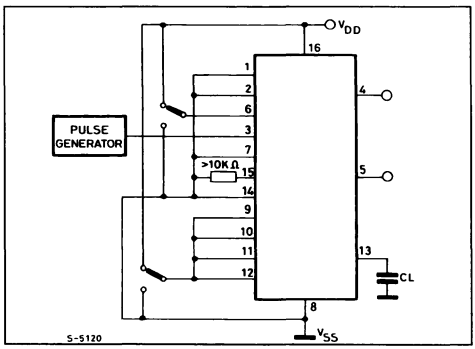
Input Leakage Current.



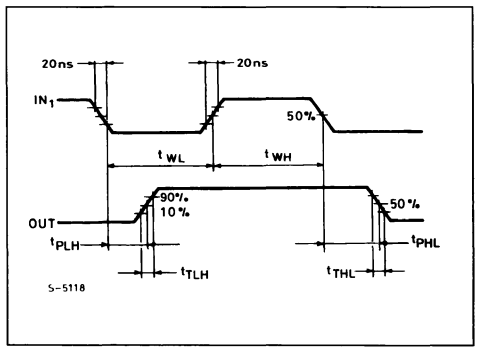

Dynamic Power Dissipation.



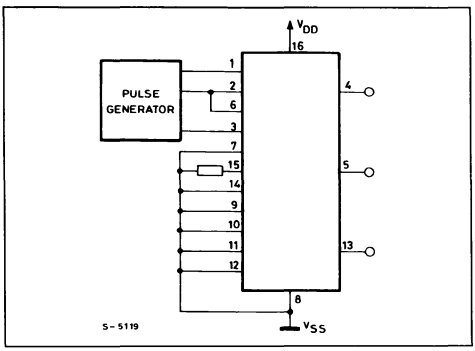

Switching Time.




Input Waveforms for Switching-Time.




Functional.

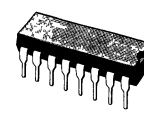


SGS-THOMSON MICROELECTRONICS

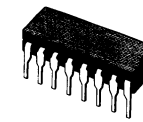
# HCC4538B
# HCF4538B

## DUAL MONOSTABLE MULTIVIBRATOR

- RETRIGGERABLE/RESETTABLE CAPABILITY
- TRIGGER AND RESET PROPAGATION DELAYS INDEPENDENT OF $R_X$, $C_X$
- TRIGGERING FROM LEADING OR TRAILING EDGE
- Q AND $\overline{Q}$ BUFFERED OUTPUTS AVAILABLE
- SEPARATE RESETS
- WIDE RANGE OF OUTPUT-PULSE WIDTHS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- SCHMITT TRIGGER INPUT ALLOWS UNLIMITER RISE AND FALL TIMES ON + TR AND – TR INPUTS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Package)

**M1**
(Micro Package)

**C1**
(Chip Carrier)

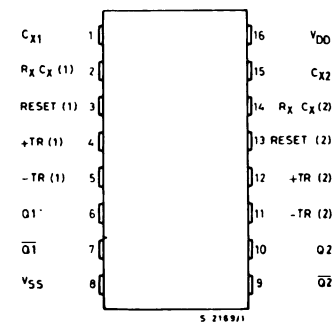
**ORDER CODES :**

HCC4538BF HCF4538BM1
HCF4538BEY HCF4538BC1

### DESCRIPTION

The **HCC4538B** (extended temperature range) and **HCF4538B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or-ceramic package and plastic micro package. The **HCC/HCF4538B** dual precision monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application. An external resistor ($R_X$) and an external capacitor ($C_X$) control the timing and accuracy for the circuit. Adjustment of $R_X$ and $C_X$ provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of $R_X$ and $C_X$. Precision control of output pulse widths is achieved through linear CMOS techniques. Leading-edge-triggering (+ TR) and trailing-edge-triggering (– TR) inputs are provided for triggering from either edge of an input pulse. An unused + TR input should be tied to $V_{SS}$. An unused – TR input should be tied to $V_{DD}$. A RESET (on low level) is provided for immediate termination of the output pulse or to

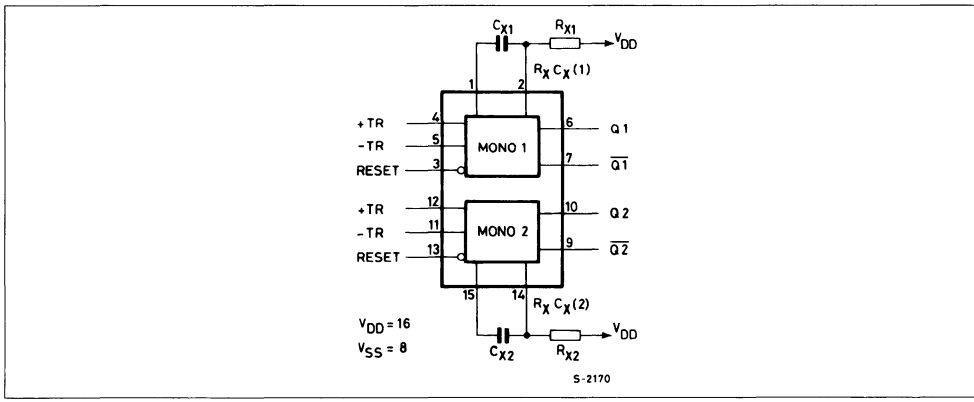
**PIN CONNECTIONS**




TERMINALS 1 8,15 ARE ELECTRICALLY CONNECTED INTERNALLY

prevent output pulses when power is turned on. An unused RESET input should be tied to $V_{DD}$. However, if an entire section of the **HCC/HCF4538B** is not used, its inputs must be tied to either $V_{DD}$ or $V_{SS}$ (see table 1). In normal operation the circuit triggers (extends the output pulse one period) on the application of each new trigger pulse. For operation in the non-retriggerable mode, $\overline{Q}$ is connected to – TR when leading-edge triggering (+ TR) is used or Q is connected to + TR when trailingedge triggering (– TR) is used. The time period (T) for this multivibrator can be calculated by : $T = R_X C_X$. The min. value of external resistance, $R_X$, is 4KΩ. The max. and min. values of external capacitance, $C_X$, are 100μF and 5nF, respectively.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ * | Supply Voltage: **HCC** Types<br>**HCF** Types | -0.5 to +20<br>-0.5 to +18 | V<br>V |
| $V_I$ | Input Voltage | -0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for Top = Full Package Temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |

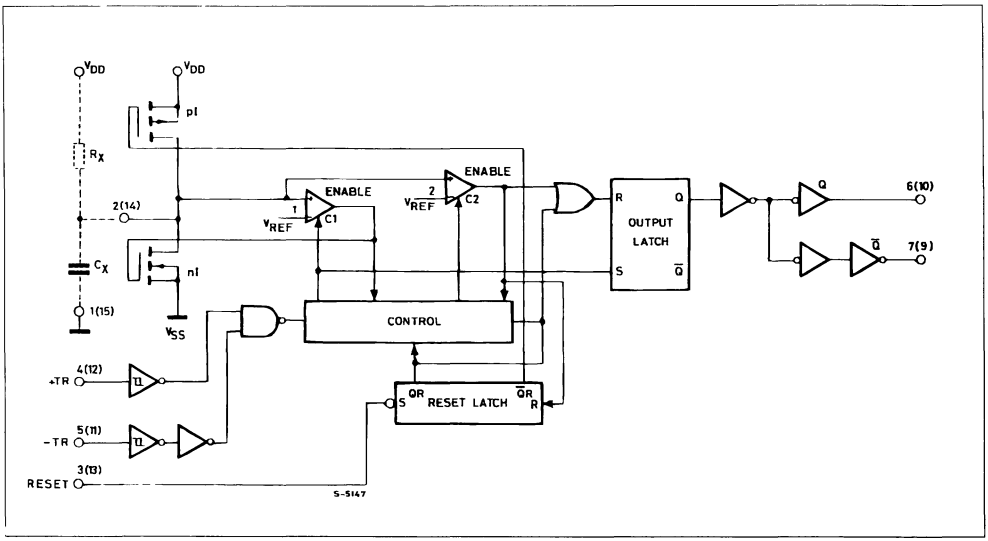
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to $V_{SS}$ pin voltage

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage: **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |

## LOGIC DIAGRAM (1/2 of device shown)

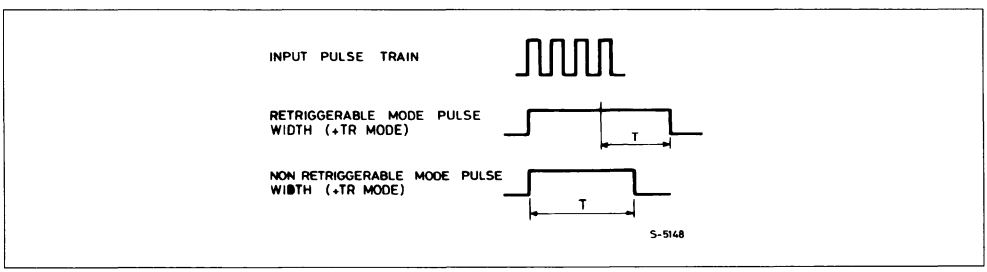



## TABLE 1: Functional Terminal Connections

| Function | $V_{DD}$ to Term. NO | | $V_{SS}$ to Term. NO | | Input Pulse to Term. No | | Other Connections | |
|---|---|---|---|---|---|---|---|---|
| | Mono (1) | Mono (2) | Mono (1) | Mono (2) | Mono (1) | Mono (2) | Mono (1) | Mono (2) |
| Leading-Edge Trigger/Retriggerable | 3, 5 | 11, 13 | | | 4 | 12 | | |
| Leading-Edge Trigger/Non-retriggerable | 3 | 13 | | | 4 | 12 | 5, 7 | 11, 9 |
| Trailing-Edge Trigger/Retriggerable | 3 | 13 | 4 | 12 | 5 | 11 | | |
| Trailing-Edge Trigger/Non-retriggerable | 3 | 13 | | | 5 | 11 | 4, 6 | 12, 10 |

**Notes :** 1 A Retriggerable one-shot multivibrator has an output pulse width which is extended on full time period (T) after application of the last trigger pulse
2 A Non-retriggerable one-shot multivibrator has a time period (T) referenced from the application of the first trigger pulse

### Pulse Width



## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditios | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{LOW}$ * Min. | $T_{LOW}$ * Max. | 25 °C Min. | 25 °C Typ. | 25 °C Max. | $T_{HIGH}$ * Min. | $T_{HIGH}$ * Max. | |
| $I_L$ | Quiescent Current | HCC Types | 0/5 | | | 5 | | 5 | | 0 04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/5 | | < 1 | 5 | 4.95 | | 4.95 | 5 | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | 10 | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | 15 | | 14 95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0 05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0 05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4 5/0.5 | < 1 | 5 | | 1.5 | | | 1 5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/5 | 2 5 | | 5 | -2 | | -1.6 | -3 2 | | -1.15 | | mA |
| | | | 0/5 | 4.6 | | 5 | -0.64 | | -0.51 | -1 | | -0.36 | | |
| | | | 0/10 | 9 5 | | 10 | -1.6 | | -1 3 | -2.6 | | -0.9 | | |
| | | | 0/15 | 13.5 | | 15 | -4.2 | | -3 4 | -6.8 | | -2.4 | | |
| | | HCF Types | 0/5 | 2 5 | | 5 | -1 8 | | -1 6 | -3.2 | | -1.3 | | |
| | | | 0/5 | 4.6 | | 5 | -0.61 | | -0.51 | -1 | | -0.42 | | |
| | | | 0/10 | 9 5 | | 10 | -1 5 | | -1 3 | -2 6 | | -1 1 | | |
| | | | 0/15 | 13.5 | | 15 | -4 | | -3 4 | -6.8 | | -2.8 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0 9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6 8 | | 2 4 | | |
| | | HCF Types | 0/5 | 0.4 | | 5 | 0.61 | | 0 51 | 1 | | 0.42 | | |
| | | | 0/10 | 0.5 | | 10 | 1.5 | | 1.3 | 2.6 | | 1.1 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.4 | 6 8 | | 2 8 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | | 0/18 | Any Input | | 18 | | ±0 1 | | ±$10^{-5}$ | ±0.1 | | ±1 | μA |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{LOW}$ = -55 °C for **HCC** device -40 °C for **HCF** device

* $T_{HIGH}$ = +125 °C for **HCC** device +85 °C for **HCF** device

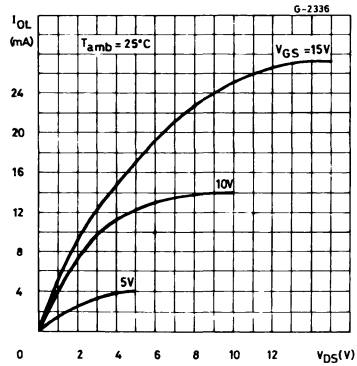
The Noise Margin for both "1" and "0" level is 1V min with $V_{DD}$ = 5 V, 2 V min with $V_{DD}$ = 10 V, 2 5 V min with $V_{DD}$ = 15 V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 KΩ, typical temperature coefficent for all $V_{DD}$ values is 03 %/°C, all input rise and fall times= 20 ns)

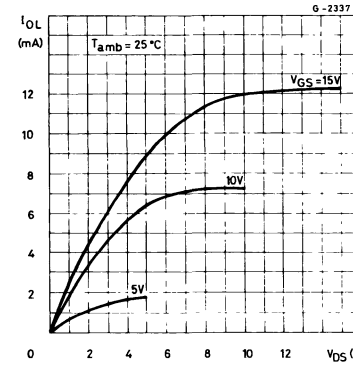
| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{TLH}$ $t_{THL}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time +TR or -TR to Q or $\overline{Q}$ | | 5 | | 300 | 600 | ns |
| | | | 10 | | 150 | 300 | |
| | | | 15 | | 100 | 220 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time Reset to Q or $\overline{Q}$ | $R_L$ = 1KΩ | 5 | | 250 | 500 | ns |
| | | | 10 | | 125 | 250 | |
| | | | 15 | | 95 | 190 | |
| $t_{WH}$ $t_{WL}$ | Minimum Input Pulse Width +TR, -TR or Reset | $R_L$ = 1KΩ | 5 | | 80 | 140 | ns |
| | | | 10 | | 40 | 80 | |
| | | | 15 | | 30 | 60 | |
| $t_{WT}$ | Output Pulse Width - Q or $\overline{Q}$ ($C_X$ = 0.005 µF, $R_X$ = 10 KΩ *) | | 5 | 57 | 60.6 | 64.5 | µs |
| | | | 10 | 55 | 58.9 | 63.0 | |
| | | | 15 | 55 | 59.1 | 63.5 | |
| $t_{WT}$ | Output Pulse Width - Q or $\overline{Q}$ ($C_X$ = 0.1 µF, $R_X$ = 100 KΩ) | | 5 | 9.4 | 9.97 | 10.5 | ms |
| | | | 10 | 9.4 | 9.95 | 10.6 | |
| | | | 15 | 9.5 | 10.00 | 10.6 | |
| $t_{WT}$ | Output Pulse Width - Q or $\overline{Q}$ ($C_X$ = 10 µF, $R_X$ = 100 KΩ) | | 5 | 0.95 | 1.00 | 1.06 | s |
| | | | 10 | 0.95 | 1.00 | 1.06 | |
| | | | 15 | 0.96 | 1.00 | 1.07 | |
| $t_W$ | Pulse Width Match Between Circuits in Same Package: $\frac{100\,(T_1 - T_2)}{T_1}$ ($C_X$ = 0.1 µF, $R_X$ = 100 KΩ) | | 5 | | ±1 | | % |
| | | | 10 | | ±1 | | |
| | | | 15 | | ±1 | | |
| $t_{rr}$ | Minimum Retrigger Time | | 5 | 0 | | | ns |
| | | | 10 | 0 | | | |
| | | | 15 | 0 | | | |
| $C_{IN}$ | Input Capacitance | | Any Input | | 5 | 7.5 | pF |

* Minimum $R_X$ value = 4 KΩ, minimum $C_X$ value = 500 pF

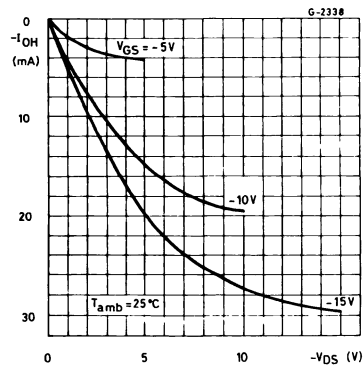
Typical Output Low (sink) Current Characteristics



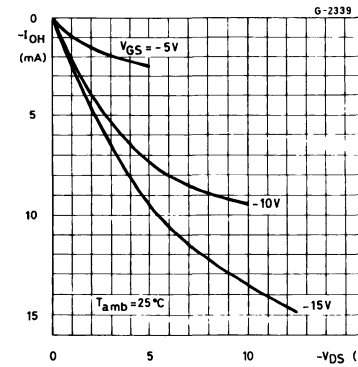

Minimum Output Low (sink) Current Characteristics



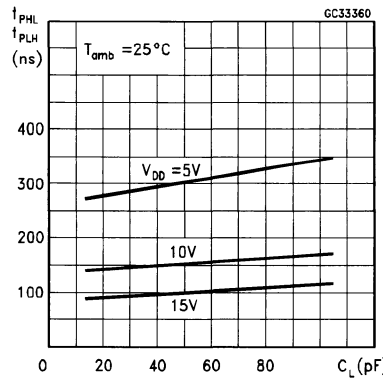

Typical Output High (source) Current Characteristics



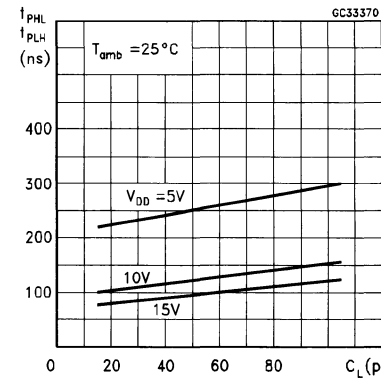

Minimum Output High (source) Current Characteristics



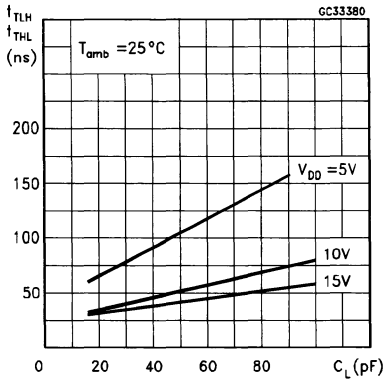

Typical Propagation Delay Time as a Function of Load Capacitance (+TR or -TR to Q or $\overline{Q}$)



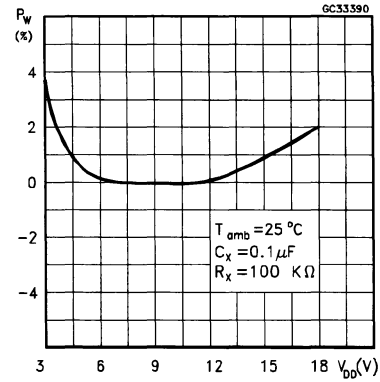

Typical Propagation Delay TIme as a Function of Load Capacitance (RESET to Q or $\overline{Q}$)



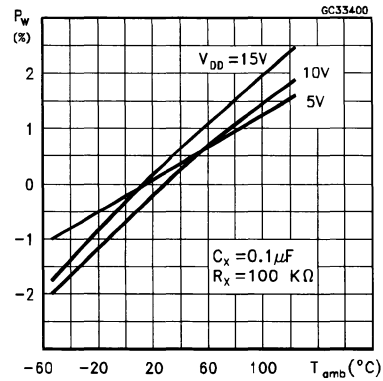
Typical Transition Time as a Function of Load Capacitance



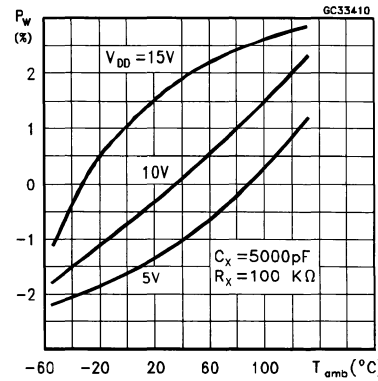

Typical Pulse Width Variation as a Function of Supply Voltage



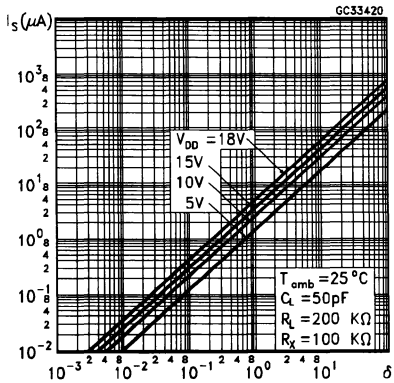

Typical Pulse Width Variation as a Function of Temperature




Typical Pulse Width Variation as a Function of Temeprature




Typical Total Supply Current as a Function of Output Duty Cycle



## Power Down Mode

During a rapid power-down conditiona, as would occur with a power supply short circuit or with a poorly filtered power supply, the energy stored in $C_X$ could discharge into Pin 2 or 14. To Avoid possible device damage in this mode, when $C_X$ is ≤0.5 microfarad, a aprotection diode with a 1 Ampere or higher rating (1N5395 or equivalent) and a separate ground return for $C_X$ should be provided as shown in Fig. 1

An alternate protection method is shown in Fig. 2, where a 51 Ω current limit resistor is inserted in series with CX. Note that a small pulse width decrease will occour however, and RX must be appropriately increased to obtain the originally desired pulse width.

Figure 1: rapid Power Down Protection Circuit

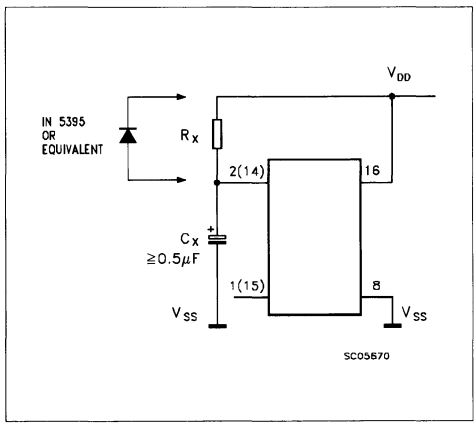
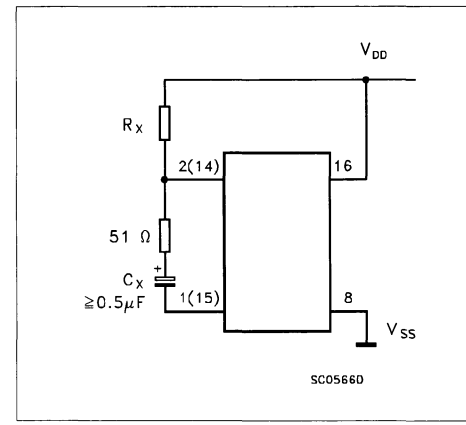
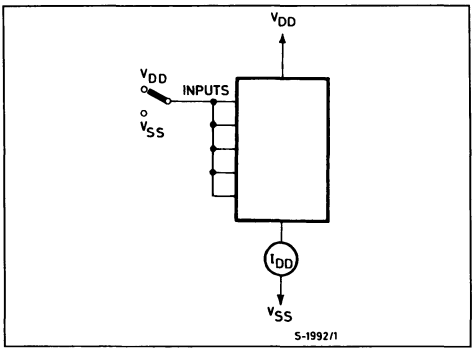



Figure 2: Alternate rapid Power Down Protection Circuit

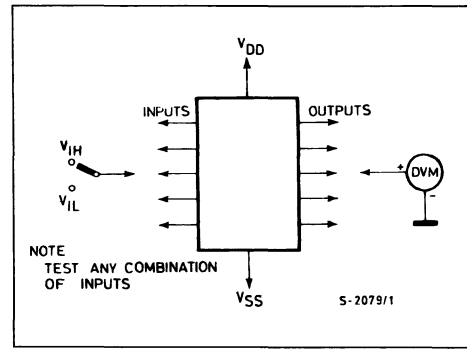


## TEST CIRCUITS

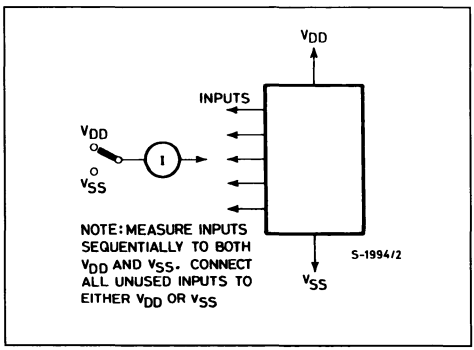
Quiescent Device Current.




Noise Immunity.




Input Leakage Current.

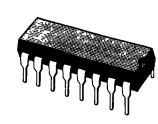


SGS-THOMSON MICROELECTRONICS

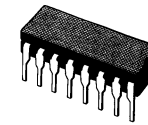
# HCC4541B
# HCF4541B

## PROGRAMMABLE TIMER

- 16 STAGE BINARI COUNTER
- LOW SYMMETRICAL OUTPUT RESISTANCE, TYPICALLY 100 OHM AT $V_{DD}$ = 15V
- OSCILLATOR FREQUENCY RANGE : DC TO 100kHz
- AUTO OR MASTER RESET DISABLES OSCILLATOR DURING RESET TO REDUCE POWER DISSIPATION
- OPERATES WITH VERY SLOW CLOCK RISE AND FALL TIMES
- BUILT-IN LOW-POWER RC OSCILLATOR
- EXTERNAL CLOCK (applied to pin 3) CAN BE USED INSTEAD OF OSCILLATOR
- OPERATES AS $2^N$ FREQUENCY DIVIDER OR AS A SINGLE-TRANSITION TIMER
- Q/$\overline{Q}$ SELECT PROVIDES OUTPUT LOGIC LEVEL FLEXIBILITY
- CAPABLE OF DRIVING SIX LOW POWER TTL LOADS, THREE LOW-POWER SCHOTTKY LOADS, PR SIX HTL LOADS OVER THE RATED TEMPERATURE RANGE
- SYMMETRICAL OUTPUT CHARACTERISTICS
- 100% TESTED FOR QUIESCENT CURRENT AT 20V
- 5-10-15V PARAMETRIC RATINGS
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF 'B' SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

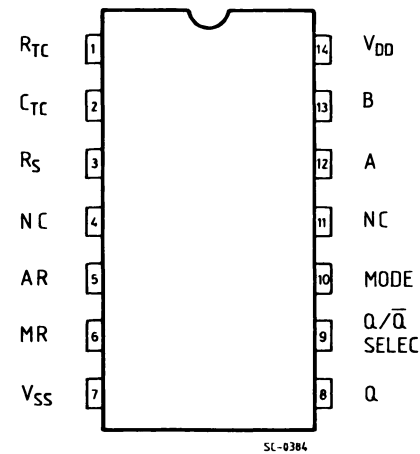
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4541 BF HCF4541 BM1
HCF4541 BEY HCF4541 BC1

**PIN CONNECTION** (top view)




### DESCRIPTION

The **HCC/HCF4541B** Programmable Timer is composed of a 16-stage binary counter, an oscillator controlled by 2 external resistors and a capacitor, an output control logic and an automatic power-on reset circuit. The counter varies on positive-edge clock transation and it can be cleared by the MASTER RESET input. The output from this timer is the Q or $\overline{Q}$ output from the 8th, 13th, or 16th counter stage. The choice of the stage depends on the time-select inputs A or B (see frequency selection table). The output is available in one of the two modes that can be selected via the MODE input, pin 10 (see truth table). The output turns out as a continuous square wave, with a frequency equal to the oscillator frequency divided by $2^N$. When this MODE

input is a logic " 1 ", when it is a logic " 0 " and after a MASTER RESET is started, and Q output has been selected, the output goes up to a high state after $2^{N-1}$ counts. It remains in that state till another MASTER RESET pulse is apply or the mode input is a logic " 1 ". The process starts by setting the AUTO RESET input (pin 5) to logic " 0 " and switching power on. If pin 5 is set to logic " 1 ", the AUTO RESET circuit is not enabled and counting cannot start till a positive MASTER RESET pulse is applied, returning to a low level. The AUTO RESET consumes a remarkable amount of power and should not be used if low-power operation is wanted.

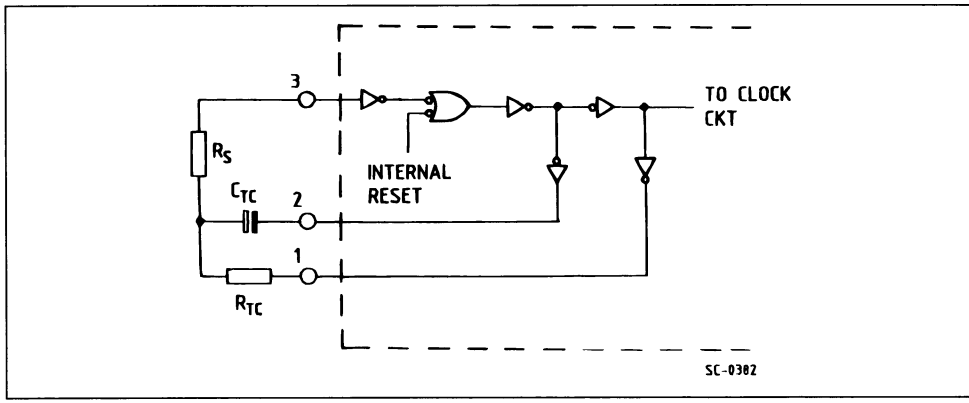
The frequency of the oscillator depends on the RC network. It can be calculated using the following formula:

$$f = \frac{1}{2.3\ R_{TC}\ C_{TC}}$$

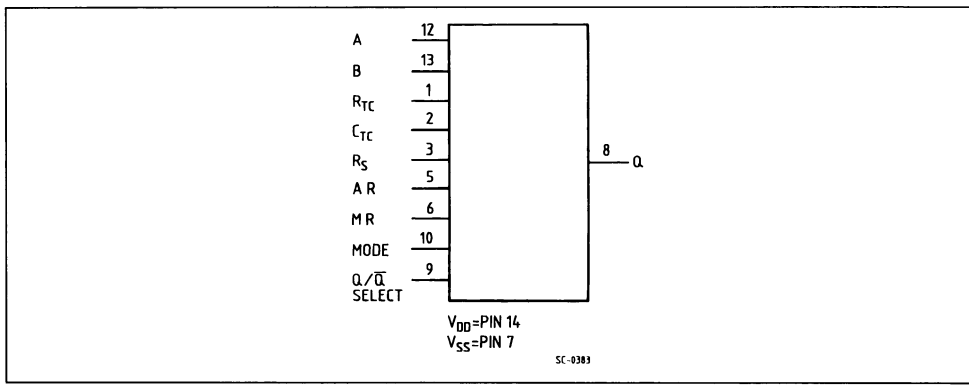
where f is between 1 kHz and 100 kHz

and RS $\geq$ 10 k$\Omega$ and $\approx$ 2 $R_{TC}$

RC Oscillator Circuit.




## FUNCTIONAL DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

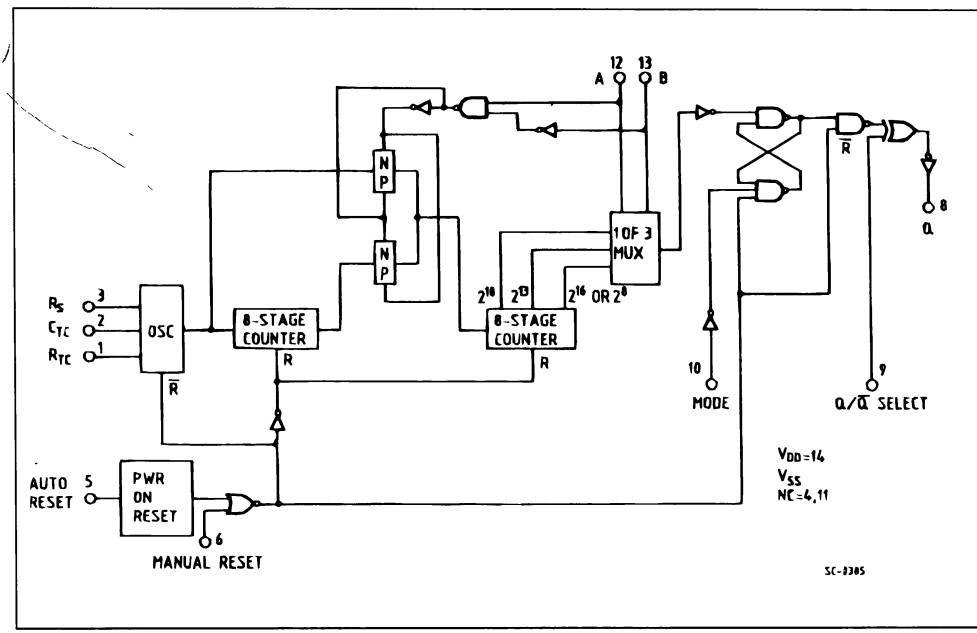
Stresses above those listed under " Absolute Maximum Ratings " may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

* All voltages are with respect to $V_{SS}$ (GND).

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to 125<br>− 40 to 85 | °C<br>°C |

## LOGIC DIAGRAM



## STATIC ELECTRICAL

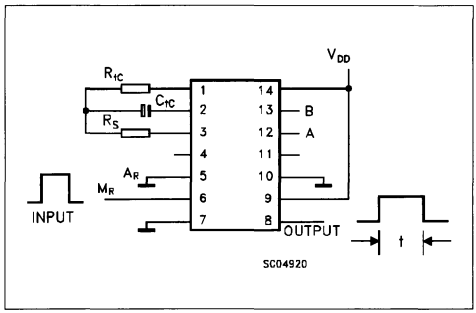
| Symbol | Parameter | | Test Conditions | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $I_O$ (uA) | $V_{DD}$ (V) | $T_{Low}$ | | 25°C | | | $T_{High}$ | | |
| | | | | | | | Min. | Max. | Min. | Typ. | Max. | Min. | Max. | |
| $I_L$ | Quiescent Current | HCC Types | 0/5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | µA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9 95 | | 9 95 | | | 9 95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/5 | 4.6 | | 5 | − 1.9 | | − 1.55 | − 3.1 | | − 1.08 | | mA |
| | | | 0/5 | 2.5 | | 5 | − 6.2 | | − 5 | − 10 | | − 3 | | |
| | | | 0/10 | 9.5 | | 10 | − 5.0 | | − 4 | − 8 | | − 2.8 | | |
| | | | 0/15 | 13.5 | | 15 | − 12.6 | | − 10 | − 20 | | − 7.2 | | |
| | | HCF Types | 0/5 | 4.6 | | 5 | − 1.85 | | − 1.55 | − 3.1 | | − 1.26 | | |
| | | | 0/5 | 2.5 | | 5 | − 6.0 | | − 5 | − 10 | | − 4 1 | | |
| | | | 0/10 | 9.5 | | 10 | − 4 8 | | − 4 | − 8 | | − 3.3 | | |
| | | | 0/15 | 13.5 | | 15 | − 12 | | − 10 | − 20 | | − 8.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/5 | 0.4 | | 5 | 1 9 | | 1.55 | 3.1 | | 1.08 | | mA |
| | | | 0/10 | 0.5 | | 10 | 5.0 | | 4 | 8 | | 2.8 | | |
| | | | 0/15 | 1.5 | | 15 | 12.6 | | 10 | 20 | | 7.2 | | |
| | | HCF Types | 0/5 | 0.4 | | 5 | 1.85 | | 1.55 | 3.1 | | 1.26 | | |
| | | | 0/10 | 0.5 | | 10 | 4.8 | | 4 | 8 | | 3.3 | | |
| | | | 0/15 | 1.5 | | 15 | 12 | | 10 | 20 | | 8.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm \frac{0.1}{5}$ | ± 0.1 | | ± 1 | µA |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = - 55C for HCC device - 40C for HCF device
* $T_{High}$ = + 125C for HCC device + 85C for HCF device
The Noise Margin for both " 1 " and " 0 " level is 1V min with $V_{DD}$ = 5V 2V min with $V_{DD}$ = 10V 2 5V min with $V_{DD}$ = 15V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall time = 20ns)

| Symbol | Parameter | VDD (V) | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| ($2^8$) $t_{PHL}$ $t_{PLH}$ | Propagation Delay Time Clock to Q | 5 | | 3.5 | 10.5 | µs |
| | | 10 | | 1.25 | 3.8 | |
| | | 15 | | 0.9 | 2.9 | |
| ($2^{16}$) $t_{PHL}$ $t_{PLH}$ | | 5 | | 6 | 18 | µs |
| | | 10 | | 3.5 | 10 | |
| | | 15 | | 2.5 | 7.5 | |
| $t_{THL}$ | Transition Time | 5 | | 100 | 200 | ns |
| | | 10 | | 50 | 100 | |
| | | 15 | | 40 | 80 | |
| $t_{TLH}$ | | 5 | | 180 | 360 | |
| | | 10 | | 90 | 180 | |
| | | 15 | | 65 | 130 | |
| | Master Reset, Clock Pulse Width | 5 | 900 | 300 | | ns |
| | | 10 | 300 | 100 | | |
| | | 15 | 225 | 85 | | |
| $f_{CL}$ | Maximum Clock Pulse Input Frequency | 5 | | 1.5 | | MHz |
| | | 10 | | 4 | | |
| | | 15 | | 6 | | |
| tr, tf | Maximum Clock Pulse Input Rise or Fall Time | 5 | Unlimited | | | µs |
| | | 10 | | | | |
| | | 15 | | | | |

## DIGITAL TIMER APPLICATION




A positive MASTER RESET pulse clears the counters and latch. The output goes high and keeps up till the number of pulses, selected by A and B, are counted. This circuit is retriggerable and is as accurate as the input frequency. If a more accurate circuit is desired, an external clock can be used on pin 3. A set-up time equal to the width of the one shot output is required immediately following initial power up, during which time the output will be high.

## FREQUENCY SELECTION TABLE

| A | B | N° of Stages N | Count $2^N$ |
|---|---|---|---|
| 0 | 0 | 13 | 8192 |
| 0 | 1 | 10 | 1024 |
| 1 | 0 | 18 | 256 |
| 1 | 1 | 16 | 65536 |

## TRUTH TABLE

| Pin | State | |
|---|---|---|
| | 0 | 1 |
| 5 | Auto Reset On | Auto Reset Disable |
| 6 | Master Reset Off | Master Reset On |
| 9 | Output Initially Low After Reset (Q) | Output Initially High After Reset ($\overline{Q}$) |
| 10 | Single Transition Mode | Recycle Mode |

# BCD-TO-7 SEGMENT LATCH/DECODER/LCD DRIVER

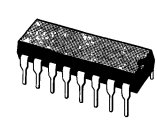
- DISPLAY BLANKING OF ALL ILLEGAL INPUT COMBINATIONS
- LATCH STORAGE OF CODE
- CAPABILITY OF DRIVING TWO LOW POWER TTL LOADS, TWO HTL LOADS, OR ONE LOW POWER SCHOTTKY LOAD OVER THE FULL RATED-TEMPERATURE RANGE
- PIN-FOR-PIN REPLACEMENT FOR THE HCF4056B (with pin 7 tied to $V_{SS}$)
- DIRECT LED DRIVING CAPABILITY
- 100% TESTED FOR QUIESCENT CURRENT AT 20V
- MAXIMUM INPUT CURRENT OF 1A AT 18V OVER FULL PACKAGE-TEMPERATURE RANGE ; 100nA AT 18V AND 25°C
- NOISE MARGIN (full package-temperature range) = 1V AT $V_{DD}$ = 5V
  2V AT $V_{DD}$ = 10V
  2.5V AT $V_{DD}$ = 15V
- 5-V, 10-V, AND 15-V PARAMETRIC RATINGS

**Applications :**

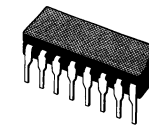
- INSTRUMENT DISPLAY DRIVER
- DASHBOARD DISPLAY DRIVER
- COMPUTER/CALCULATOR DISPLAY DRIVER
- TIMING DEVICE DRIVER (clocks, watches, timers)

## DESCRIPTION

The HCC/HCF4543B is a BCD-to-seven segment latch/decoder/driver designed primarily for liquid-crystal display (LCD) applications. It is also capable of driving light emitting diode (LED), incandescent, gas-discharge, and fluorescent displays. This device is functionally similar to and serves as direct replacement for the HCF4056B when pin 7 is connected to $V_{SS}$. It differs from the HCF4056B in that it has a display blanking capability instead of a level-shifting function and requires only one power supply. When the HCF4056B is used in the level shifting mode, two power supplies are required. When the HCF4543B is used for LCD applications, a square wave must be applied to the PHASE input and the backplane of the LCD device. For LED applications a logic 1 is required at the PHASE input for common-cathode devices ; a logic 0 is required for common-anode devices (see truth table).



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

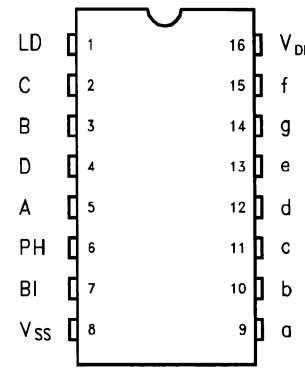
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4543 BF
HCF4543 BEY
HCF4543 BM1
HCF4543 BC1

**PIN CONNECTION** (top view)

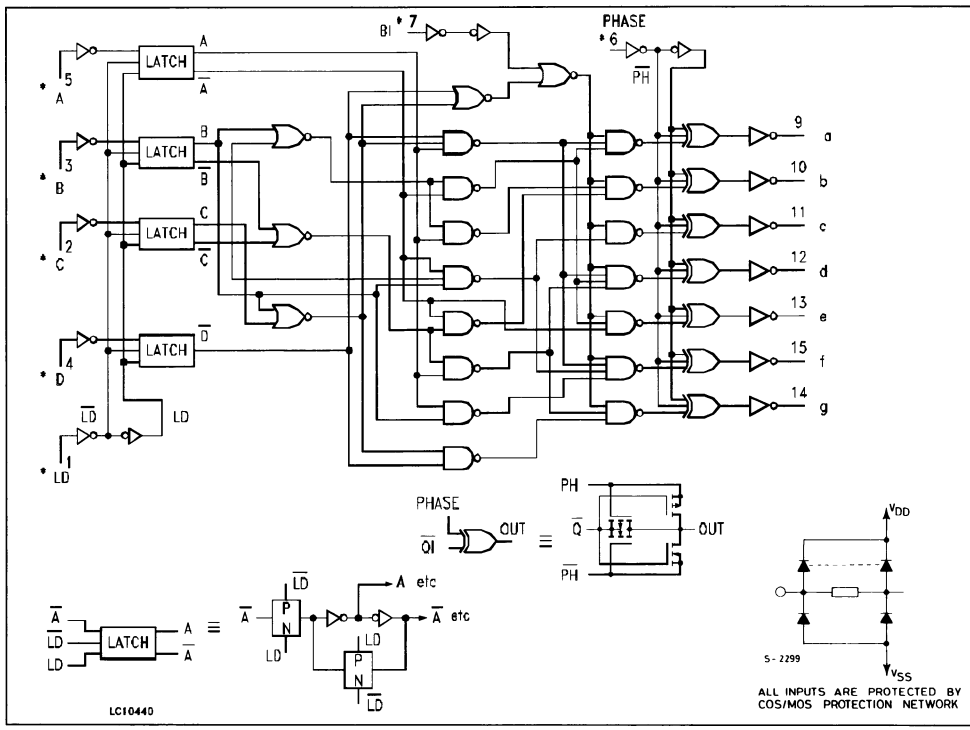


## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

* All Voltage Values are referred to $V_{SS}$ pin voltage

## LOGIC DIAGRAM (1/2 of device shown)




## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| VDD | Supply Voltage : **HCC** types<br>**HCF** types | 3 to 18<br>3 to 15 | V |
| VI | Input Voltage | 0 to VDD | V |
| Top | Operating Temperature : **HCC** types<br>**HCF** types | − 55 to + 125<br>− 40 to + 85 | °C |

## TRUTH TABLE

| INPUT CODE | | | | | | | OUTPUT STATE | | | | | | | DISPLAY CHARACTER |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LD | BI | Ph* | D | C | B | A | a | b | c | d | e | f | g | |
| X | 1 | 0 | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 2 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 3 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 5 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 6 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 7 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 9 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 0 | 0 | X | X | X | X | ** | | | | | | | ** |
| • | • | • | • | | | | Inverse of Output Combinations Above | | | | | | | Display as above |

X = Don't care.
• = Above combinations
* = For liquid-crystal readouts, apply a square wave to Ph.
For common cathode LED readouts, select Ph = 0.
For common anode LED readouts, select Ph = 1.
** = Depends upon the BCD code previously applied when LD = 1.

## STATIC ELECTRICAL CHARACTERISTICS

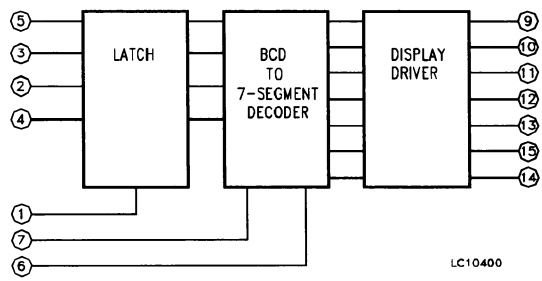
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $I_O$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$ Min. | $T_{Low}$ Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$ Min. | $T_{High}$ Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/5 | 2.5 | | 5 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | mA |
| | | | 0/5 | 4.6 | | 5 | − 0.46 | | − 0.37 | − 0.75 | | − 0.26 | | |
| | | | 0/10 | 9.5 | | 10 | − 0.98 | | − 0.8 | − 1.6 | | − 0.55 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.33 | | − 2.7 | − 5.4 | | − 1.9 | | |
| | | HCF Types | 0/5 | 2.5 | | 5 | 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/5 | 4.6 | | 5 | 0.36 | | − 0.31 | − 0.75 | | − 0.25 | | |
| | | | 0/10 | 9.5 | | 10 | 0.81 | | − 0.68 | − 1.6 | | − 0.54 | | |
| | | | 0/15 | 13.5 | | 15 | 2.7 | | − 2.3 | − 5.4 | | − 1.84 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC types | 0/18 | Any Input | | 18 | | ± 0.1 | | $± 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF types | 0/15 | | | 15 | | ± 0.3 | | $± 10^{-5}$ | ± 0.3 | | ± 1 | |

* $T_{Low}$ = − 55°C for HCC device : − 40°C for HCF device.
* $T_{High}$ = + 125°C for HCC device + 85°C for HCF device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2 5V min. with $V_{DD}$ = 15V

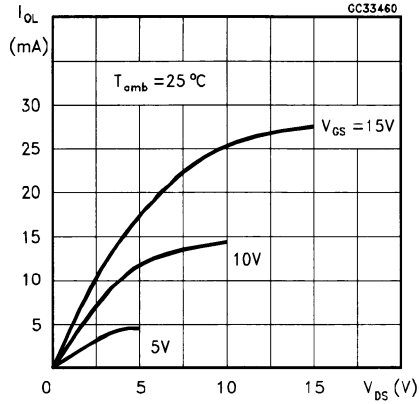
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall time = 20ns)

| Symbol | Parameter | Test Conditions $V_{DD}$ (V) | Limits All packages | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{PHL}$ | Propagation Delay Time | 5 | | 600 | 1200 | ns |
| | | 10 | | 200 | 400 | |
| | | 15 | | 150 | 300 | |
| $t_{PLH}$ | | 5 | | 500 | 1000 | |
| | | 10 | | 200 | 400 | |
| | | 15 | | 150 | 300 | |
| $t_{THL}$ | Transition Time | 5 | | 180 | 360 | |
| | | 10 | | 90 | 180 | |
| | | 15 | | 65 | 130 | |
| $t_{TLH}$ | | 5 | | 180 | 360 | |
| | | 10 | | 90 | 180 | |
| | | 15 | | 65 | 130 | |
| $t_{WH}$ | Latch Disable Pulse Width | 5 | 250 | 125 | | |
| | | 10 | 100 | 50 | | |
| | | 15 | 80 | 40 | | |
| $t_{SU}$ | Address Setup Time | 5 | 60 | 15 | | |
| | | 10 | 20 | −5 | | |
| | | 15 | 10 | −5 | | |
| $t_H$ | Address Hold Time | 5 | 25 | -5 | | |
| | | 10 | 20 | 10 | | |
| | | 15 | 20 | 0 | | |
| $C_{IN}$ | Input Capacitance | Any Input | | 5 | 7.5 | pF |

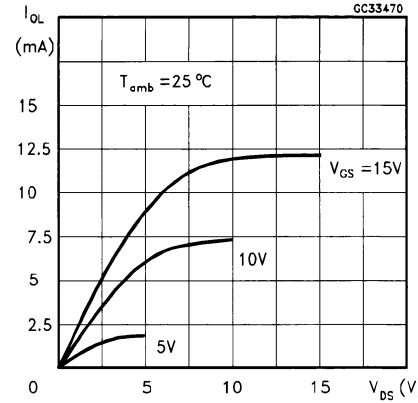
BCD-to-seven-segment latch/decoder/driver functional diagram



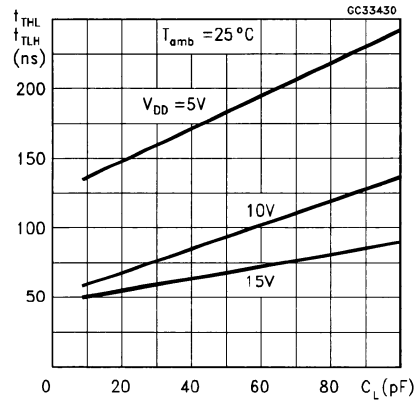
Typical Output Low (sink) Current Characteristics.



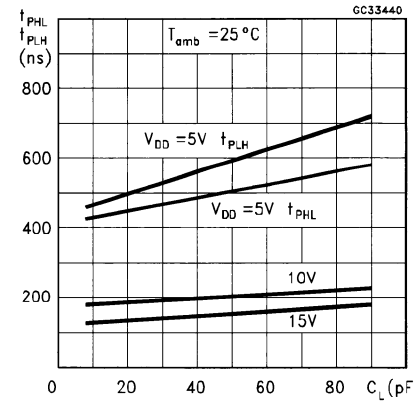

Minimum Output Low (sink) Current Characteristics.



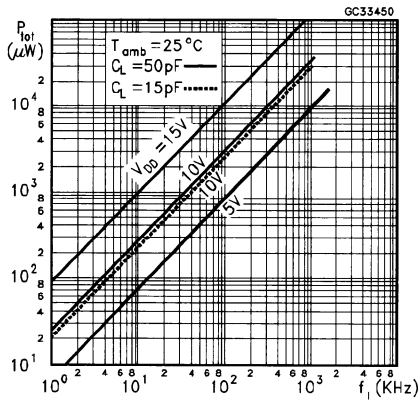

Typical Transition Time as a Function of Load Capacitance



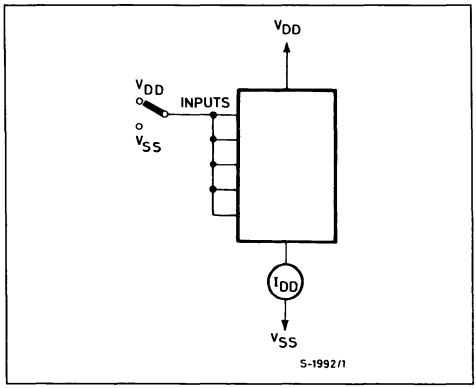

Typical Propagation Delay Time as a Function of Load Capacitance



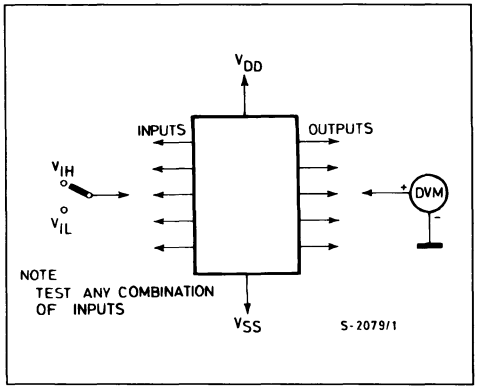

Typical Dinamic Power Dissipation as a Function of Frequency



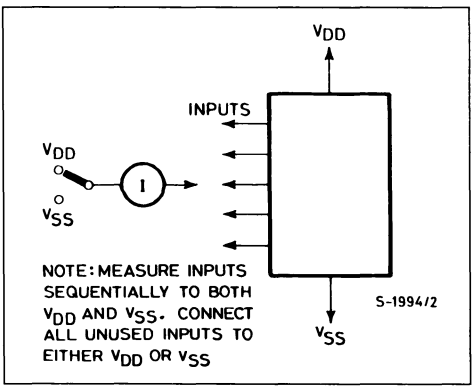
Input Voltage Test Circuit.




Quiescent Device Current Test Circuit.




Input-leakage -current Test Circuit.

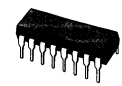


# HCC/HCF4555B
# HCC/HCF4556B

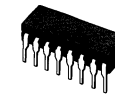
## DUAL BINARY TO 1 OF 4 DECODER/DEMULTIPLEXERS

**4555B OUTPUTS HIGH ON SELECT**
**4556B OUTPUTS LOW ON SELECT**

- EXPANDABLE WITH MULTIPLE PACKAGES
- STANDARD, SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

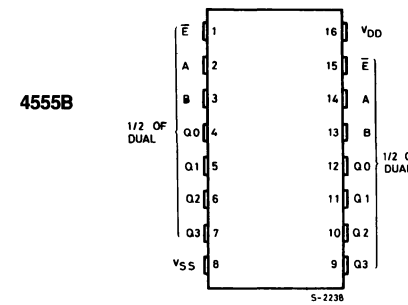
**M1**
(Micro Package)

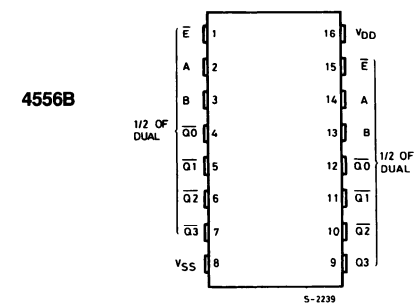
**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC45XXBF HCF45XXBM1
HCF45XXBEY HCF45XXBC1

**PIN CONNECTIONS**



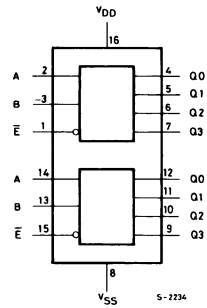

### DESCRIPTION

The **HCC4555B, HCC4556B** (extended temperature range) and the **HCF4555B, HCF4556B** (intermediate temperature range) are monolithic integrated circuits available in 16-lead dual in-line plastic or ceramic package and plastic micropackage.

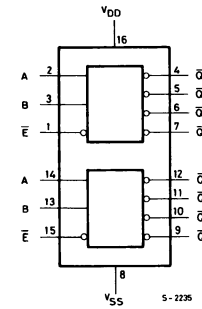
The **HCC/HCF4555B** and **HCC/HCF4556B** are dual one-of-four decoders/demultiplexers. Each decoder has two select inputs (A and B), an Enable input (E), and four mutually exclusive outputs. On the **HCC/HCF4555B** the outputs are high on select; on the **HCC/HCF4556B** the outputs are low on select. When the Enable input is high, the outputs of the **HCC/HCF4555B** remain low and the outputs of the **HCC/HCF4556B** remain high regardless of the state of the select inputs A and B.

## FUNCTIONAL DIAGRAMS

**4555B**




**4556B**




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

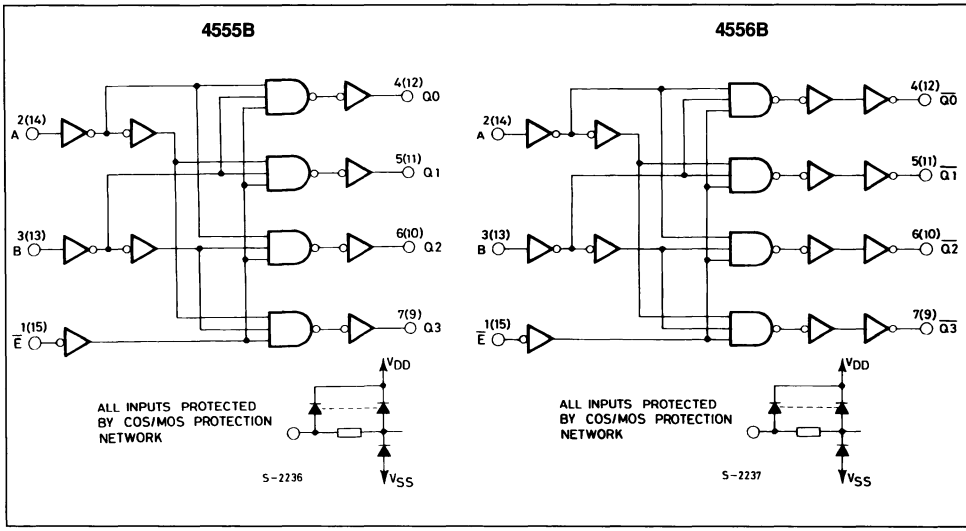
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltages values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAMS




## TRUTH TABLE

| Inputs Enable Select | | | Outputs 4555B | | | | Outputs 4556B | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{E}$ | B | A | Q3 | Q2 | Q1 | Q0 | $\overline{Q3}$ | $\overline{Q2}$ | $\overline{Q1}$ | $\overline{Q0}$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1 | X | X | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

X = DON'T CARE, LOGIC 1 = HIGH, LOGIC 0 = LOW

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

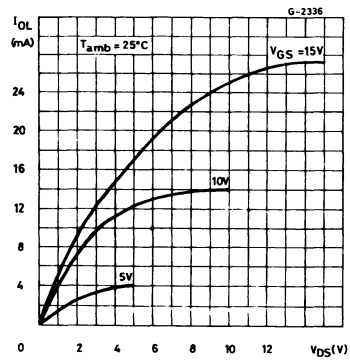
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0 05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

(*) $T_{LOW}$ = − 55°C for **HCC** device : − 40°C for **HCF** device
(*) $T_{HIGH}$ = + 125°C for **HCC** device . + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is 1V min with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V

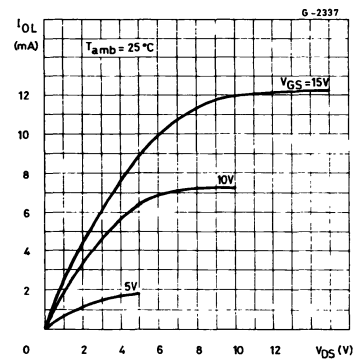
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall times = 20ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time (A or B input to any output) | | 5 | | 220 | 440 | ns |
| | | | 10 | | 95 | 190 | |
| | | | 15 | | 70 | 140 | |
| | Propagation Delay Time ($\overline{E}$ input to any output) | | 5 | | 200 | 400 | ns |
| | | | 10 | | 85 | 170 | |
| | | | 15 | | 65 | 130 | |
| $t_{TLH}$, $t_{THL}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

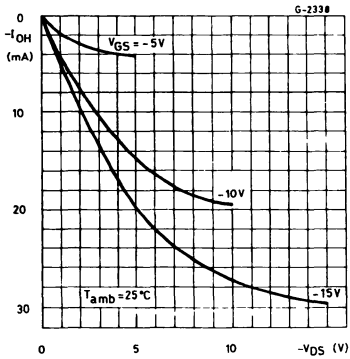
Typical Output Low (sink) Current Characteristics.



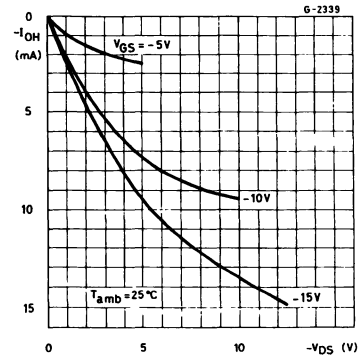

Minimum Output Low (sink) Current Characteristics.



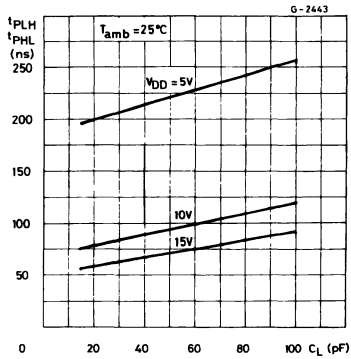

Typical Output High (source) Current Characteristics.



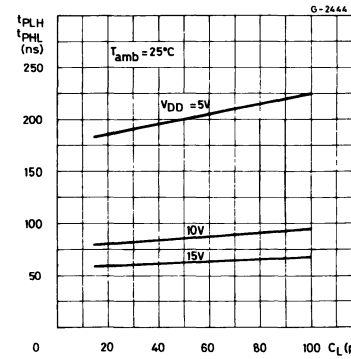

Minimum Output High (source) Current Characteristics.



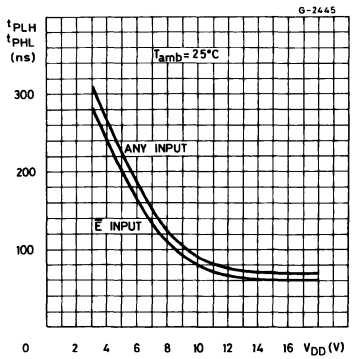
Typical Propagation Delay Time vs. Load Capacitance (A or B input to any output).



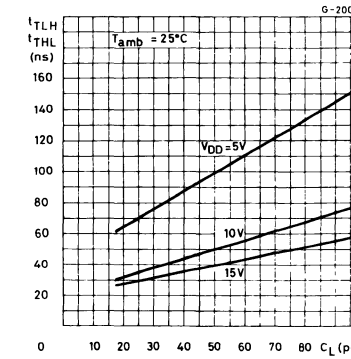

Typical Propagation Delay Time vs. Load Capacitance ($\overline{E}$ input to any input ).



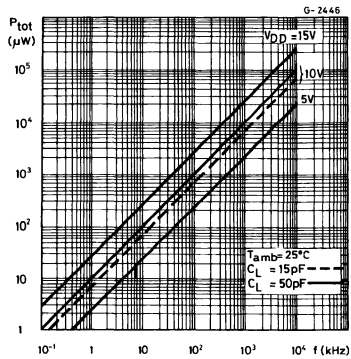

Typical Propagation Delay Time vs. Supply Voltage.




Typical Transition Time vs. Load Capacitance.

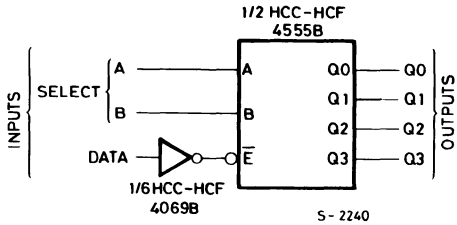



Typical Dynamic Power Dissipation/per Device vs. Frequency.



## APPLICATIONS

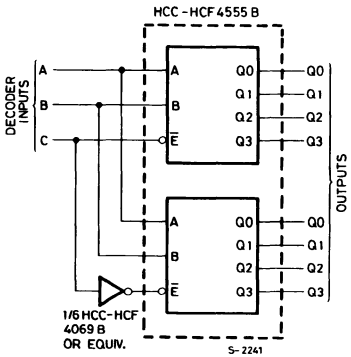
1 of 4 Line Data Demultiplexer using HCC/HCF4555B




**TRUTH TABLE**

| Select Inputs | | Outputs | | | |
|---|---|---|---|---|---|
| B | A | Q0 | Q1 | Q2 | Q3 |
| 0 | 0 | DATA | 0 | 0 | 0 |
| 0 | 1 | 0 | DATA | 0 | 0 |
| 1 | 0 | 0 | 0 | DATA | 0 |
| 1 | 1 | 0 | 0 | 0 | DATA |

1 of 8 Decoder using HCC/HCF 4555B

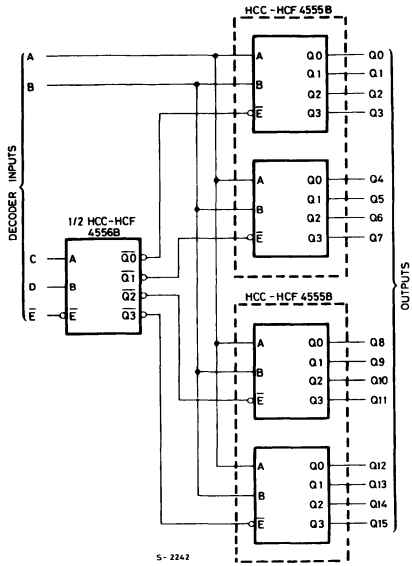



**TRUTH TABLE**

| Inputs | | | Q Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

## APPLICATIONS (continued)

1 of 16 Decoder using HCC/HCF4555B and HCC/HCF4556B

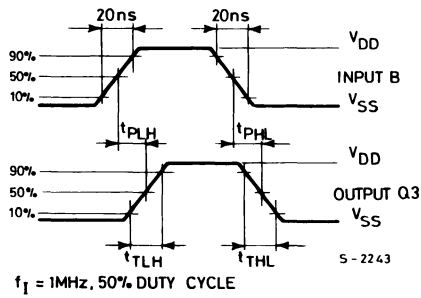



**TRUTH TABLE**

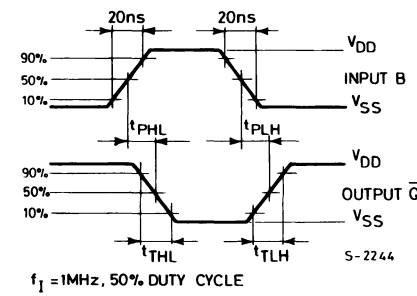
| Inputs | | | | | Q Outputs | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

X = Don't care.

HCC/HCF4555B Input to Q3 Output Dynamic Signal Waveforms

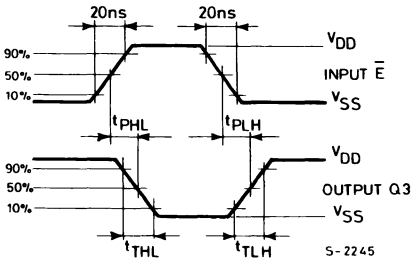



HCC/HCF4556B Input to $\overline{Q3}$ Output Dynamic Signal Waveforms



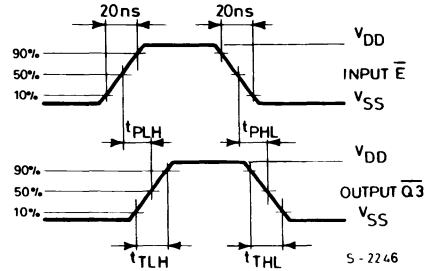
## APPLICATIONS (continued)

HCC/HCF4555B $\overline{E}$ Input to Q3 Output Dynamic Signal Waveforms




$f_I$ = 1MHz, 50% DUTY CYCLE

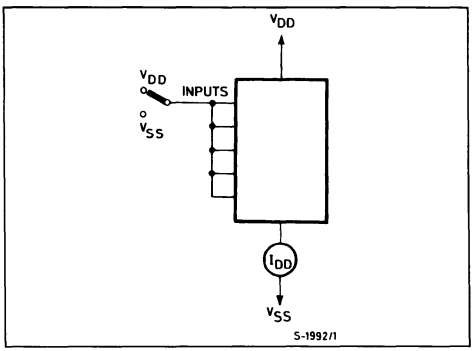
HCC/HCF4556B $\overline{E}$ Input to $\overline{Q3}$ Output Dynamic Signal Waveforms



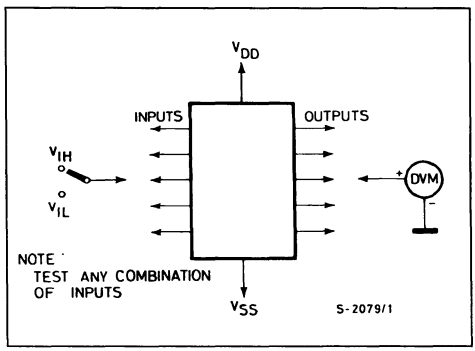

$f_I$ = 1MHz, 50% DUTY CYCLE

## TEST CIRCUITS

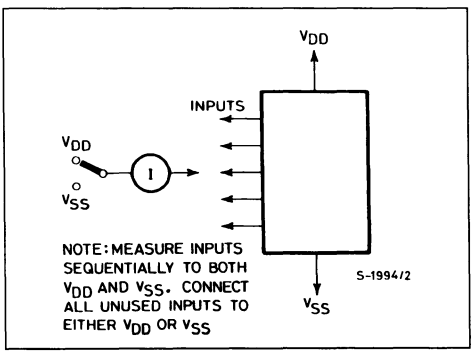
Quiescien tDevice Current.




Noise Immunity.




Input Leakage Current.



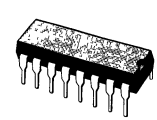
SGS-THOMSON MICROELECTRONICS

# HCC4560B
# HCF4560B

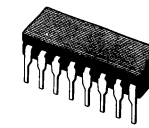
## NBCD ADDER

**PRODUCT PREVIEW**

- VERY LOW QUIESCENT CURRENT
- HIGH NOISE IMMUNITY
- SINGLE SUPPLY OPERATION - POSITIVE OR NEGATIVE
- SUPPLY VOLTAGE RANGE 3V TO 18V
- DIODE PROTECTION ON ALL INPUTS



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

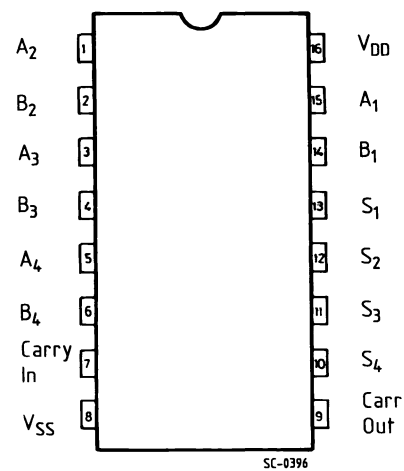
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4560 BF
HCF4560 BEY
HCF4560 BM1
HCF4560 BC1

**PIN CONNECTION** (top view)




### DESCRIPTION

The HCC4560B and HCF4560B are monolithic integrated circuits, available in 16-lead dual-in-line plastic or ceramic packages and plastic micro packages.

The HCC4560B and HCF4560B add two 4-bit numbers in NBCD (natural binary coded decimal) format, resulting in sum and carry outputs in NBCD code.

All inputs and outputs are active high. The carry input for the least significant digit is connected to $V_{SS}$ for no carry in.

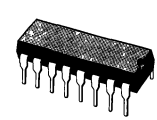
SGS-THOMSON MICROELECTRONICS

# HCC4566B
# HCF4566B

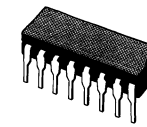
## INDUSTRIAL TIME-BASE GENERATOR

**PRODUCT PREVIEW**

- VERY LOW QUIESCENT CURRENT
- HIGH NOISE IMMUNITY
- SUPPLY VOLTAGE RANGE 3V TO 18V
- NEGATIVE EDGE TRIGGERED COUNTERS FOR EASY CASCADING
- PULSE SHAPING ON COUNTER INPUTS ACCEPTS SLOW INPUT RISE TIMES
- MONOSTABLE MULTIVIBRATOR POSITIVE OR NEGATIVE EDGE TRIGGERED



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

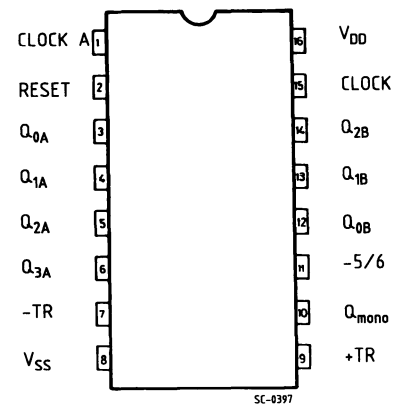
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4566 BF
HCF4566 BEY
HCF4566 BM1
HCF4566 BC1

**PIN CONNECTION** (top view)




### DESCRIPTION

The HCC4566B and HCF4566B are monolithic integrated circuits, available in 16-lead dual-in-line plastic or ceramic packages and plastic micro packages.

The HCC4566B and HCF4566B are industrial time base generators. They consist of a divide-by-10 ripple counter and a divide-by-5 or divide-by-6 ripple counter to permit stable time generation from a 50 or 60Hz line.

Cascading these devices as divide by 60 counters provides a seconds and minutes counter with an output in BCD format. An internal monostable multivibrator is included whose output can be used as a reset or clock pulse providing additional frequency flexibility. A divide-by-5 facility allows the generation of a 1Hz signal from the European 50Hz-line.

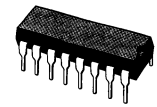
SGS-THOMSON
MICROELECTRONICS

# HCC4572B
# HCF4572B

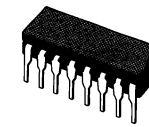
## HEX GATE

**PRODUCT PREVIEW**

- VERY LOW QUIESCENT CURRENT
- HIGH NOISE IMMUNITY
- SINGLE SUPPLY OPERATION
- SUPPLY VOLTAGE RANGE 3V TO 18V
- HIGH INPUT IMPEDANCE
- PIN LAYOUT OPTIMISED FOR MAXIMUM FLEXIBILITY



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

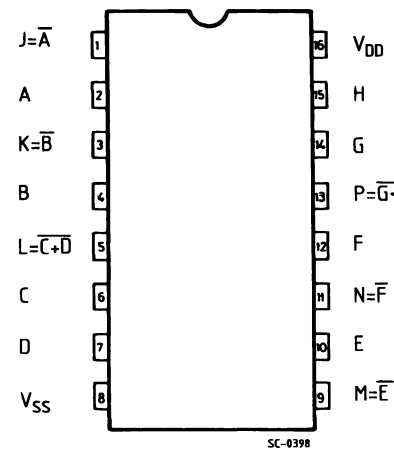
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC4572 BF
HCF4572 BEY
HCF4572 BM1
HCF4572 BC1

**PIN CONNECTION** (top view)



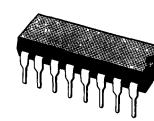

### DESCRIPTION

The HCC4572B and HCF4572B are a monolithic integrated circuits, available in 16-lead dual-in-line plastic and ceramic packages and plastic micro packages.

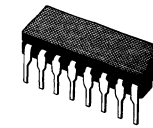
The HCC4572B and HCF4572B are hex functional gates containing one NOR gate, one NAND gate and four inverters. These devices are intended for application where low power dissipation and/or high noise immunity is required.

# 4-BIT MAGNITUDE COMPARATOR

- EXPANSION TO 8, 12, 16 ... 4 N BITS BY CASCADING UNITS
- MEDIUM-SPEED OPERATION : COMPARES TWO 4-BIT WORDS IN 180ns (typ.) AT 10V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

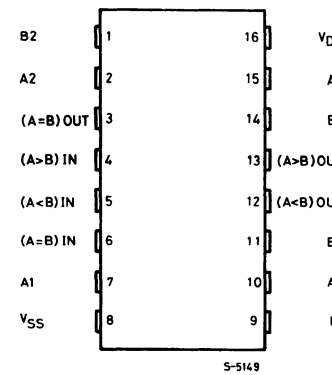
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

| | |
|---|---|
| HCC4585BF | HCF4585BM1 |
| HCF4585BEY | HCF4585BC1 |

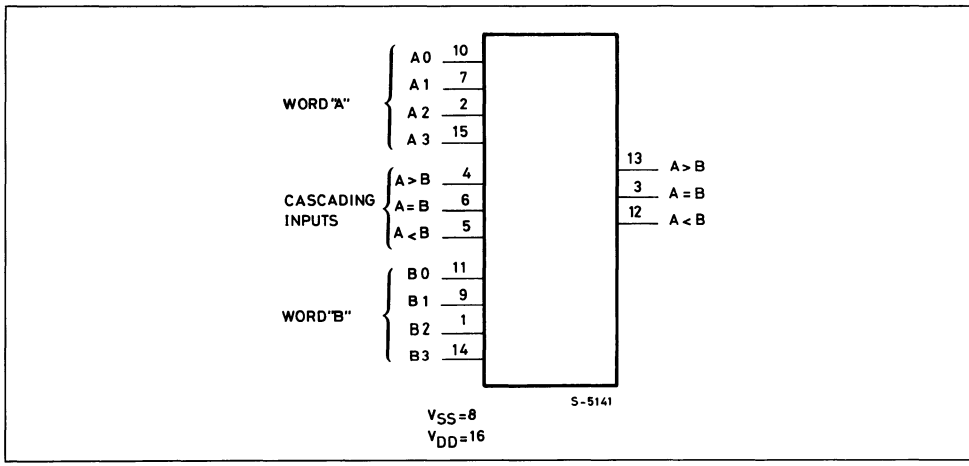
## PIN CONNECTIONS




## DESCRIPTION

The **HCC4585B** (extended temperature range) and **HCF4585B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package, and plastic micro package. The **HCC/HCF4585B** is a 4-bit magnitude comparator designed for use in computer and logic applications that require the comparison of two 4-bit words. This logic circuit determines whether one 4-bit word (Binary or BCD) is "less than", "equal to", or "greater than" a second 4-bit word. The **HCC/HCF4585B** has eight comparing inputs (A3, B3, through A0, B0), three outputs (A < B, A = B, A > B) and three cascading inputs (A < B, A = B, A > B) that permit systems designers to expand the comparator function to 8, 12, 16 ... 4 N bits. When a single **HCC/HCF4585B** is used, the cascading inputs are connected as follows : (A < B) = low, (A = B) = high, (A > B) = high. Cascading these units for comparison of more than 4 bits is accomplished as shown in typical application.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

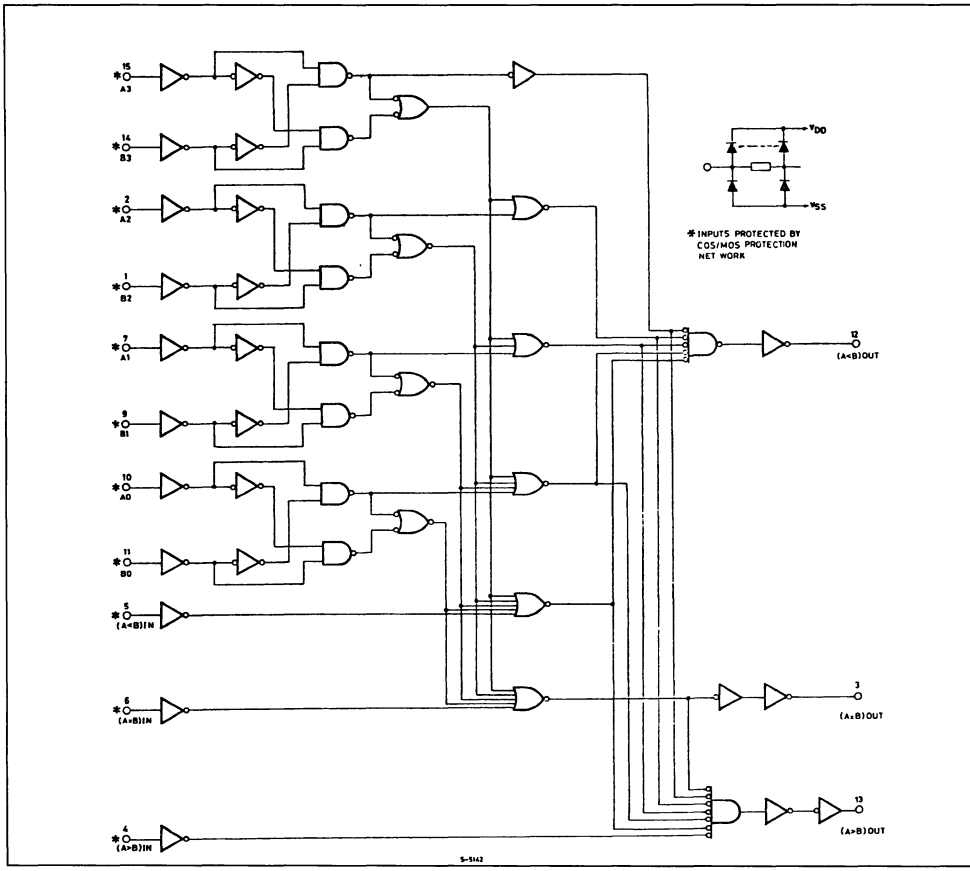
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage · **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltages are with respect to $V_{SS}$ (GND)

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAM




## TRUTH TABLE

| Inputs | | | | | | | Outputs | | |
|---|---|---|---|---|---|---|---|---|---|
| Comparing | | | | Cascading | | | | | |
| A3, B3 | A2, B2 | A1, B1 | A0, B0 | A < B | A = B | A > B | A < B | A = B | A > B |
| A3 > B3 | X | X | X | X | X | 1 | 0 | 0 | 1 |
| A3 = B3 | A2 > B2 | X | X | X | X | 1 | 0 | 0 | 1 |
| A3 = B3 | A2 = B2 | A1 > B1 | X | X | X | 1 | 0 | 0 | 1 |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 > B0 | X | X | 1 | 0 | 0 | 1 |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | 0 | 0 | 1 | 0 | 0 | 1 |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | 0 | 1 | X | 0 | 1 | 0 |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | 1 | 0 | X | 1 | 0 | 0 |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 < B0 | X | X | X | 1 | 0 | 0 |
| A3 = B3 | A2 = B2 | A1 < B1 | X | X | X | X | 1 | 0 | 0 |
| A3 = B3 | A2 < B2 | X | X | X | X | X | 1 | 0 | 0 |
| A3 < B3 | X | X | X | X | X | X | 1 | 0 | 0 |

X = Don't Care

Logic 1 = High Level

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

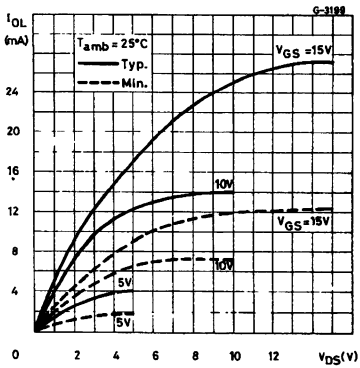
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1 5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1 1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1 3 | 2 6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device − 40°C for **HCF** device
* $T_{High}$ = + 125°C for **HCC** device + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is 1V min with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2 5V min with $V_{DD}$ = 15V.

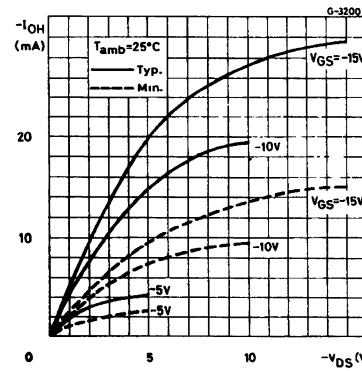
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall time = 20ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time Comparing Inputs to Outputs | | 5 | | 300 | 600 | ns |
| | | | 10 | | 125 | 250 | |
| | | | 15 | | 80 | 160 | |
| | Cascading Input to Outputs | | 5 | | 200 | 400 | ns |
| | | | 10 | | 80 | 160 | |
| | | | 15 | | 60 | 120 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

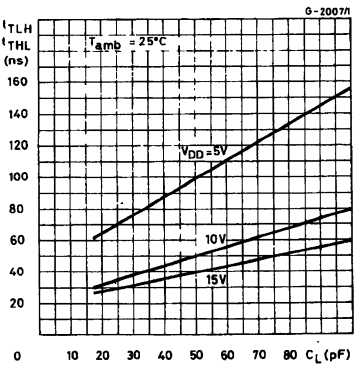
Output Low (sink) Current Characteristics.



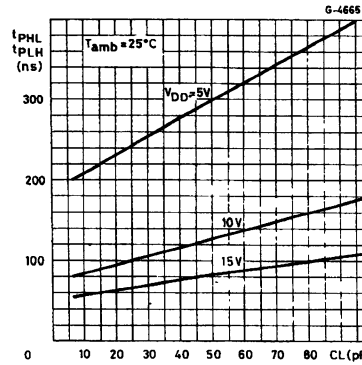

Output High (source) Current Characteristics.



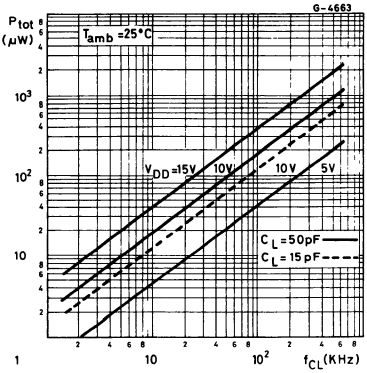

Typical Transition Time vs. Load Capacitance.




Typical Propagation Delay Time (comparing inputs to outputs) vs. Load Capacitance.

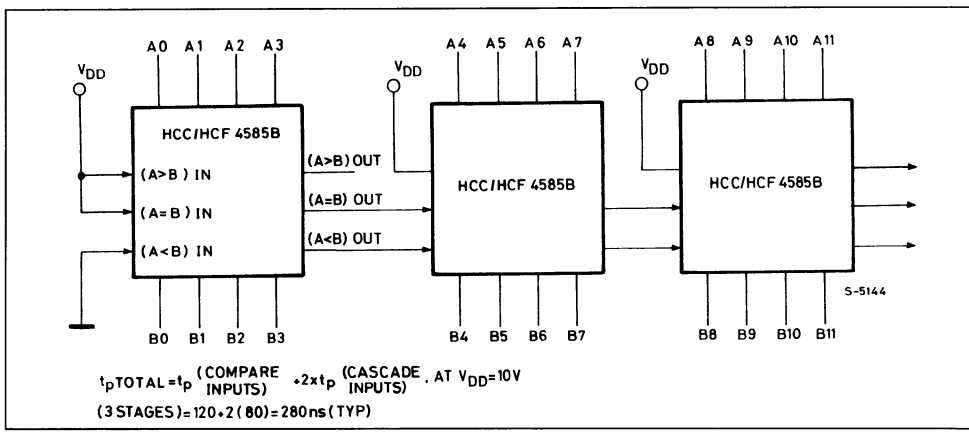


Typical Dynamic Power Dissipation vs. Clock Input Frequency.



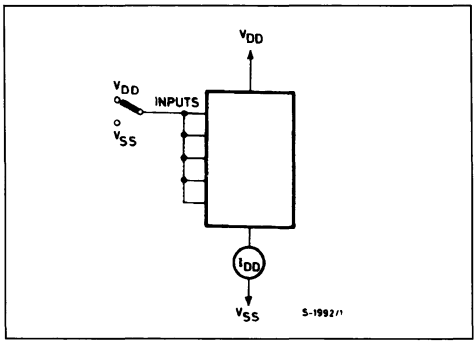

## TYPICAL APPLICATION

TYPICAL SPEED CHARACTERISTICS OF A 12-BIT COMPARATOR

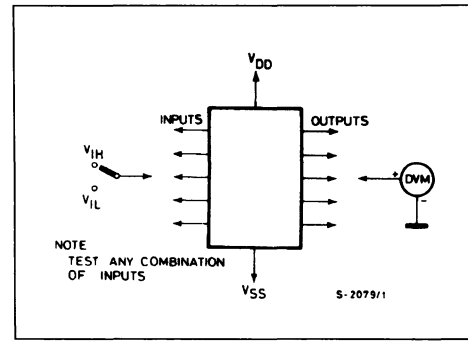


## TEST CIRCUITS

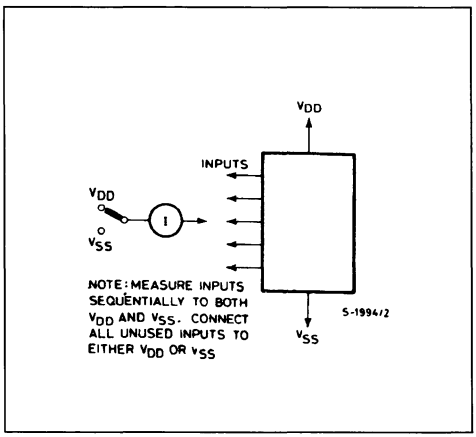
Quiescent Device Current.



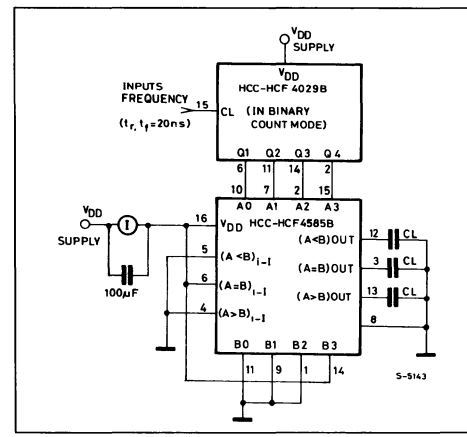

Input Voltage.




Input Leakage Current.



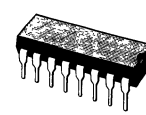

Dynamic Power Dissipation.



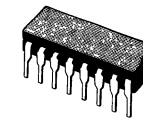
# HCC4724B
# HCF4724B

## 8 BIT ADDRESSABLE LATCH

- SERIAL DATA INPUT - ACTIVE PARALLEL OUTPUT
- STORAGE REGISTER CAPABILITY - MASTER CLEAR
- CAN FUNCTION AS DEMULTIPLEXER
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTER
- 100% TESTED FOR QUIESCENT CURRENT AT 20V
- MAXIMUM INPUT CURRENT OF 1μA AT 18V (full package-temperature range), 100nA AT 18V AND 25°C
- NOISE MARGIN (full package-temperature range) = 1V AT $V_{DD}$ = 5V, 2V AT $V_{DD}$ = 10V, 2.5V AT $V_{DD}$ = 15V
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N. 13A, " STANDARD SPECIFICATIONS FOR DESCRIPTION OF ' B ' SERIES CMOS DEVICES "



**EY**
(Plastic Package)



**F**
(Ceramic Package)

**M1**
(Micro Package)

**C1**
(Chip Carrier)

**ORDER CODES :**

HCC4724BF HCF4724BM1
HCF4724BEY HCF4724BC1

### APPLICATION

- MULTI-LINE DECODERS
- A/D CONVERTERS

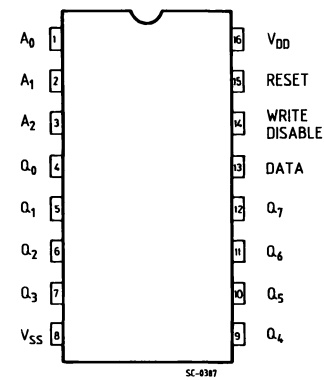
### DESCRIPTION

The **HCC/HCF4724B** 8-bit addressable latch is a serial-input, parallel-output storage register that can perform a variety of functions.

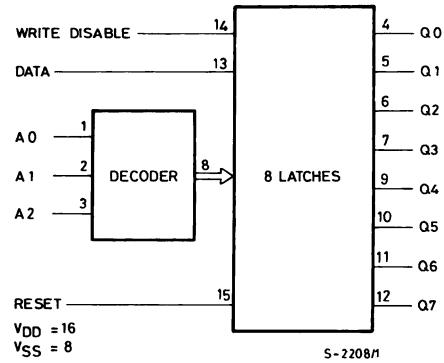
Data are inputted to a particular bit in the latch when that bit is addressed (by means of inputs A0, A1, A2) and when WRITE DISABLE is at low level. When WRITE DISABLE is high, data entry is inhibited however, all 8 outputs can be continuously read independent of WRITE DISABLE and address inputs.

A master RESET input is available, which resets all bits to a logic " 0 " level when RESET and WRITE DISABLE are at a high level. When RESET is at a high level, and WRITE DISABLE is at a low level, the latch acts as a 1-of-8 demultiplexer ; the bit that is addressed has an active output which follows the data input, while all unaddressed bits are held to a logic " 0 " level.

### PIN CONNECTIONS



## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ * | Supply Voltage: **HCC** Types<br>**HCF** Types | -0.5 to +20<br>-0.5 to +18 | V<br>V |
| $V_I$ | Input Voltage | -0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for Top = Full Package Temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |

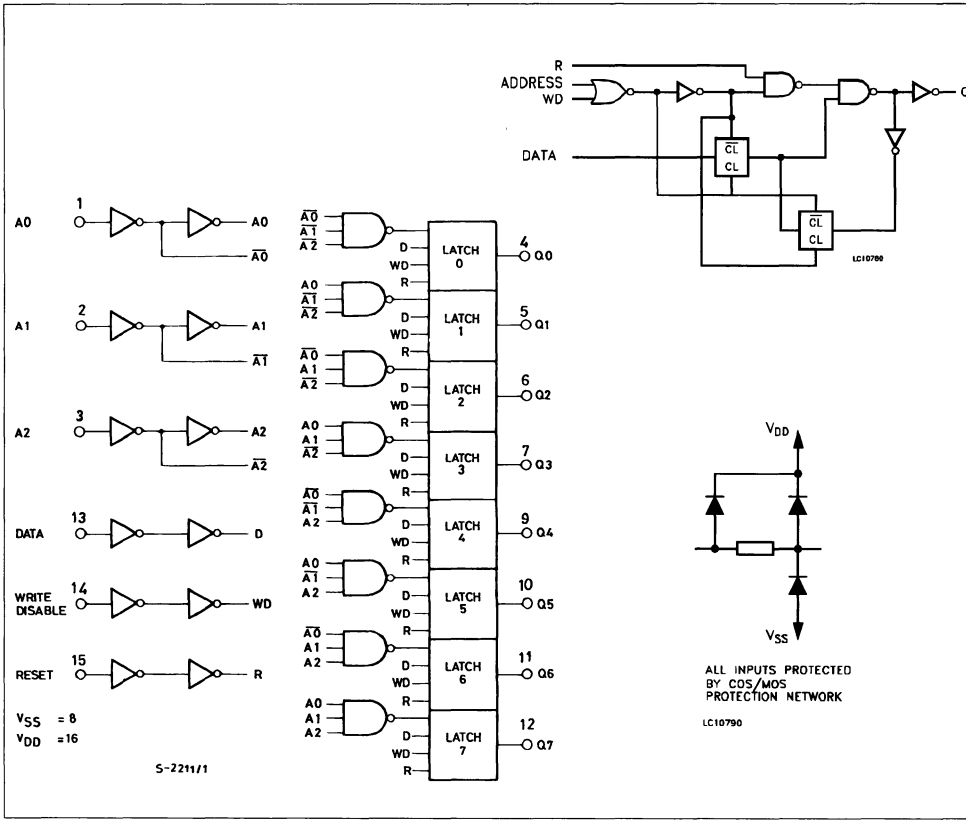
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability

* All voltage values are referred to $V_{SS}$ pin voltage

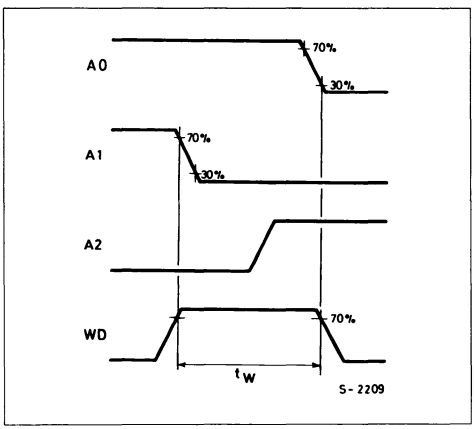
## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage: **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |

## LOGIC DIAGRAM




## Definition of WRITE DISABLE ON Time




## MODE SELECTION

| TYPE | WD | R | Addressed Latch | Unaddressed Latch |
|---|---|---|---|---|
| A | 0 | 0 | Follows Data | Hold Previous State |
| B | 0 | 1 | Follows Data (Active High 8-Channel De-multiplexer) | Reset to "0" |
| C | 1 | 0 | Hold Previous State | |
| D | 1 | 1 | Reset to "0" | Reset to "0" |

WD = WRITE DISABLE R= RESET

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditios | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{LOW}$ * Min. | $T_{LOW}$ * Max. | 25 °C Min. | 25 °C Typ. | 25 °C Max. | $T_{HIGH}$ * Min. | $T_{HIGH}$ * Max. | |
| $I_L$ | Quiescent Current | HCC Types | 0/5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/5 | 2.5 | | 5 | -2 | | -1.6 | -3.2 | | -1.15 | | mA |
| | | | 0/5 | 4 6 | | 5 | -0.64 | | -0.51 | -1 | | -0.36 | | |
| | | | 0/10 | 9.5 | | 10 | -1.6 | | -1.3 | -2.6 | | -0.9 | | |
| | | | 0/15 | 13.5 | | 15 | -4.2 | | -3.4 | -6.8 | | -2.4 | | |
| | | HCF Types | 0/5 | 2.5 | | 5 | -1.8 | | -1.6 | -3.2 | | -1.3 | | |
| | | | 0/5 | 4.6 | | 5 | -0.61 | | -0.51 | -1 | | -0.42 | | |
| | | | 0/10 | 9.5 | | 10 | -1.5 | | -1.3 | -2.6 | | -1.1 | | |
| | | | 0/15 | 13.5 | | 15 | -4 | | -3.4 | -6.8 | | -2.8 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/5 | 0.4 | | 5 | 0.61 | | 0.51 | 1 | | 0.42 | | |
| | | | 0/10 | 0.5 | | 10 | 1.5 | | 1.3 | 2.6 | | 1.1 | | |
| | | | 0/15 | 1.5 | | 15 | 4 | | 3.4 | 6.8 | | 2.8 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | | 0/18 | Any Input | | 18 | | ±0.1 | | $±10^{-5}$ | ±0.1 | | ±1 | μA |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{LOW}$ = -55 °C for **HCC** device. -40 °C for **HCF** device

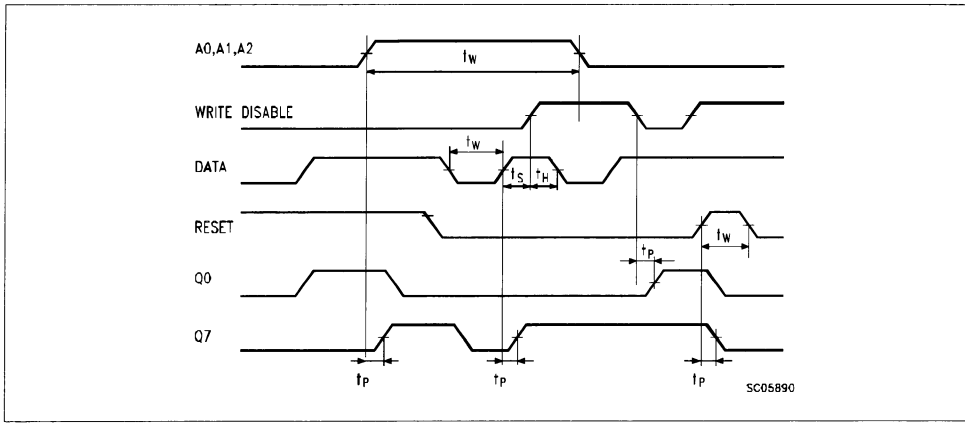
* $T_{HIGH}$ = +125 °C for **HCC** device +85 °C for **HCF** device

The Noise Margin for both "1" and "0" level is. 1V min with $V_{DD}$ = 5 V, 2 V min with $V_{DD}$ = 10 V, 2 5 V min. with $V_{DD}$ = 15 V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 KΩ, typical temperature coefficent for all $V_{DD}$ values is 03 %/°C, all input rise and fall times= 20 ns)

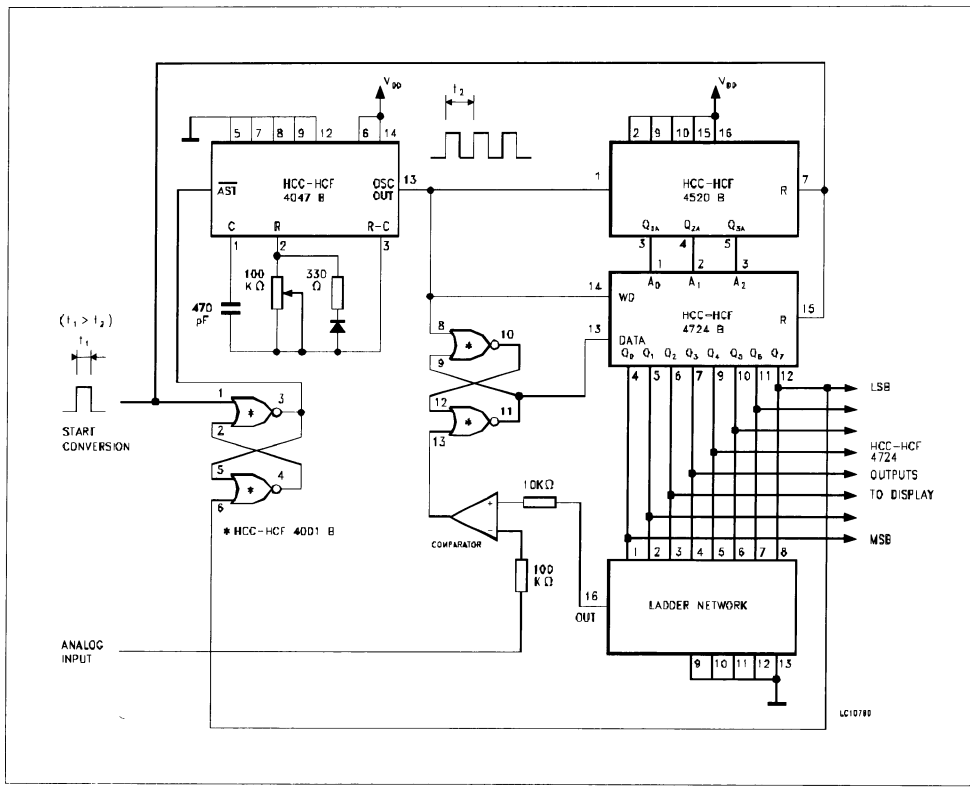
| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time Data to Output | (See Figure 1) | 5 | | 200 | 400 | ns |
| | | | 10 | | 75 | 150 | |
| | | | 15 | | 50 | 100 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time Write Disable to Output | (See Figure 1) | 5 | | 200 | 400 | ns |
| | | | 10 | | 80 | 160 | |
| | | | 15 | | 60 | 120 | |
| $t_{PHL}$ | Propagation Delay Time Reset to Output | (See Figure 1) | 5 | | 175 | 350 | ns |
| | | | 10 | | 80 | 160 | |
| | | | 15 | | 65 | 130 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time Address to Output | (See Figure 1) | 5 | | 225 | 450 | ns |
| | | | 10 | | 100 | 200 | |
| | | | 15 | | 75 | 150 | |
| $t_{TLH}$ $t_{THL}$ | Transition Time Any Output | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_W$ | Minimum Pulse Width Data | (See Figure 1) | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| | Minimum Pulse Width Address | (See Figure 1) | 5 | | 200 | 400 | ns |
| | | | 10 | | 100 | 200 | |
| | | | 15 | | 65 | 125 | |
| | Minimum Pulse Width Reset | (See Figure 1) | 5 | | 75 | 150 | ns |
| | | | 10 | | 40 | 75 | |
| | | | 15 | | 25 | 50 | |
| $t_S$ | Minimum Setup Time Data to Write Disable | (See Figure 1) | 5 | | 50 | 100 | ns |
| | | | 10 | | 25 | 50 | |
| | | | 15 | | 20 | 35 | |
| $t_H$ | Minimum Holf Time Data to Write Disable | (See Figure 1) | 5 | | 75 | 150 | ns |
| | | | 10 | | 40 | 75 | |
| | | | 15 | | 25 | 50 | |
| $C_{IN}$ | Input Capacitance | | Any Input | | 5 | 7.5 | pF |

**Figure 1**: Master Timing Diagram

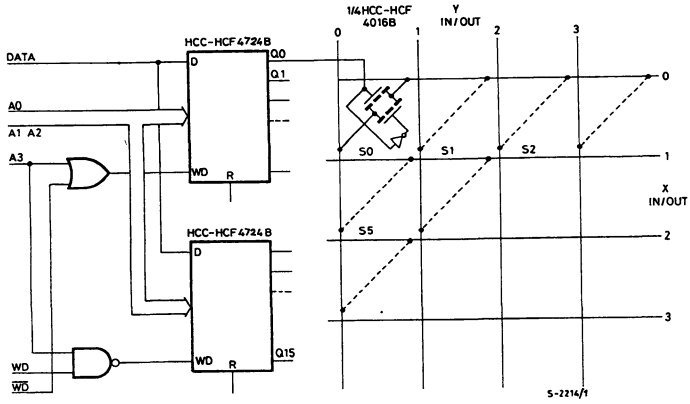



## TYPICAL APPLICATIONS

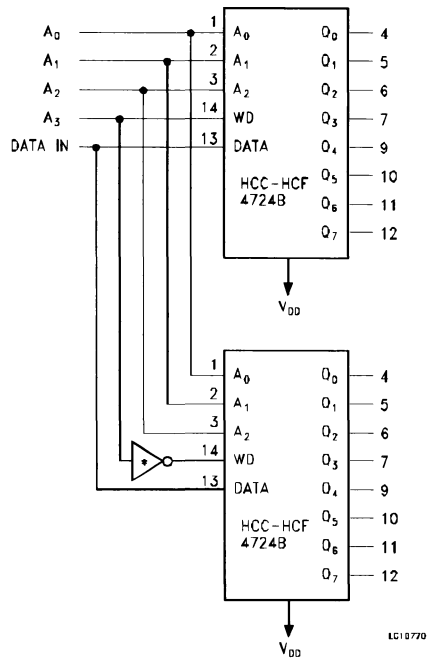
A/D Converter



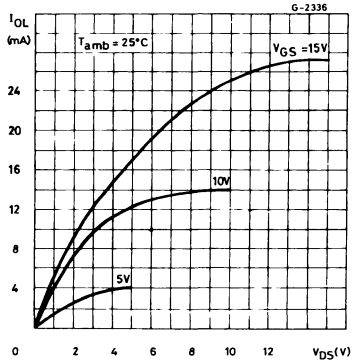
Multiple Selection Decoding - 4 x 4 Crosspoint Switch



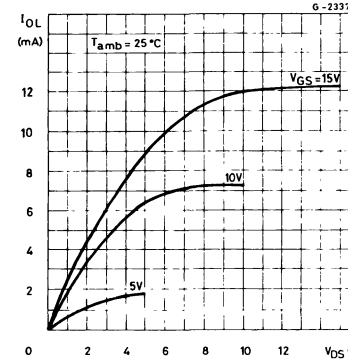

1 of 6 Decoder/Demultiplexer



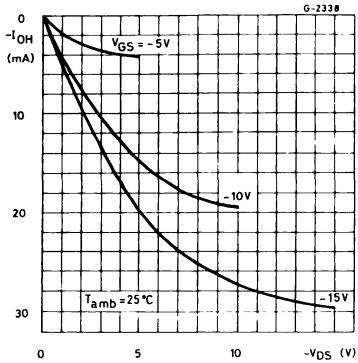
Typical Output Low (sink) Current Characteristics



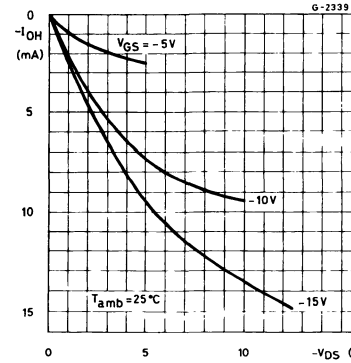

Minimum Output Low (sink) Current Characteristics



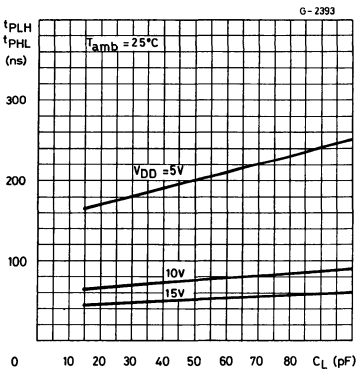

Typical Output High (source) Current Characteristics



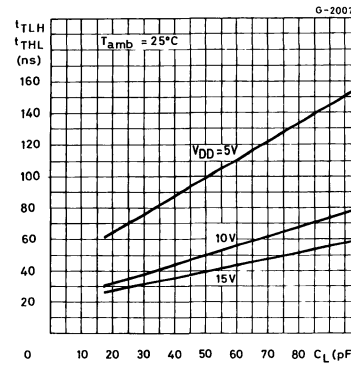

Minimum Output High (source) Current Characteristics



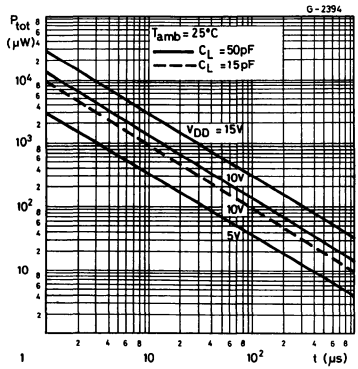

Typical Propagation Delay Time (data to Qn) vs Load Capacitance




Typical Transition Time vs Load Capacitance

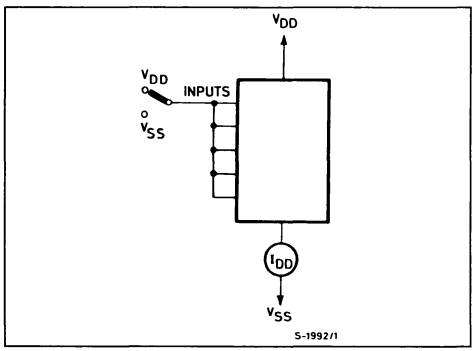


Typical Dynamic Power Dissipation vs Address Cycle Time

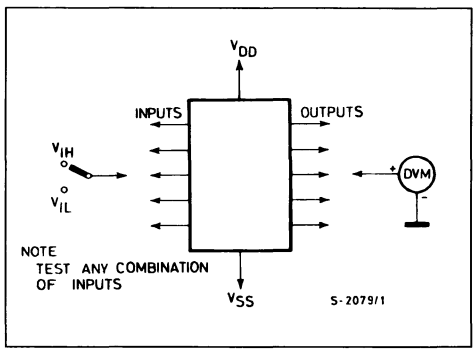



## TEST CIRCUITS

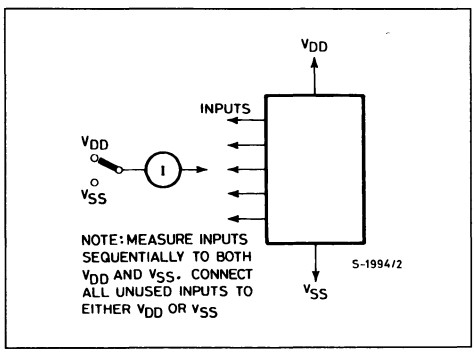
Quiescent Device Current.




Noise Immunity.




Input Leakage Current.



SGS-THOMSON MICROELECTRONICS

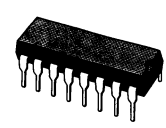
# HCC/HCF40100B

## 32-STAGE STATIC LEFT/RIGHT SHIFT REGISTER

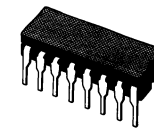
- FULLY STATIC OPERATION
- SHIFT LEFT/SHIFT RIGHT CAPABILITY
- MULTIPLE PACKAGE CASCADING
- RECIRCULATE CAPABILITY
- LIFO OR FIFO CAPABILITY
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED AT 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

### DESCRIPTION

The **HCC40100B** (extended temperature range) and **HCF40100B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF40100B** is a 32-stage shift register containing 32 D-type master-slave flip-flops. The data present at the SHIFT-RIGHT INPUT is transferred into the first register stage synchronously with the positive CLOCK edge, provided the LEFT/RIGHT CONTROL is at a low level, the RECIRCULATE CONTROL is at a high level, and the CLOCK INHIBIT is low. If the LEFT/RIGHT CONTROL is at a high level and the RECIRCULATE CONTROL is also high, data at the SHIFT-LEFT INPUT is transferred into the 32nd register stage synchronously with the positive CLOCK transition, provided the CLOCK INHIBIT is low. The state of the LEFT/RIGHT CONTROL, RECIRCULATE CONTROL, and CLOCK INHIBIT should not be changed when the CLOCK is high. Data is shifted one stage left or one stage right depending on the state of the LEFT/RIGHT CONTROL, synchronously with the positive CLOCK edge. Data clocked into the first or 32nd register states is available at the SHIFT-LEFT or SHIFT-RIGHT OUTPUT respectively, on the next negative CLOCK transition (see Data Transfer Table). No shifting occurs on the positive CLOCK edge if the CLOCK INHIBIT line is at a high level. With the RECIRCULATE CONTROL low, data in the 32nd stage is shifted into the first stage when the LEFT/RIGHT CONTROL is low and from the 1st stage to the 32nd stage when the LEFT/RIGHT CONTROL is high.



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

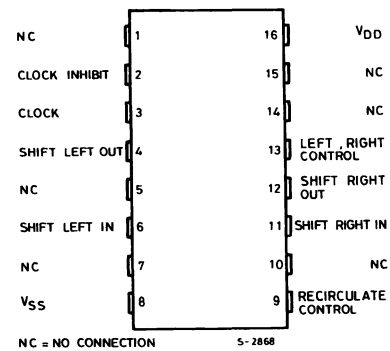
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

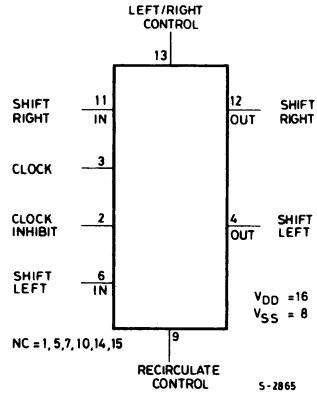
**ORDER CODES :**

HCC40100BF HCF40100BM1
HCF40100BEY HCF40100BC1

**PIN CONNECTIONS**



## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

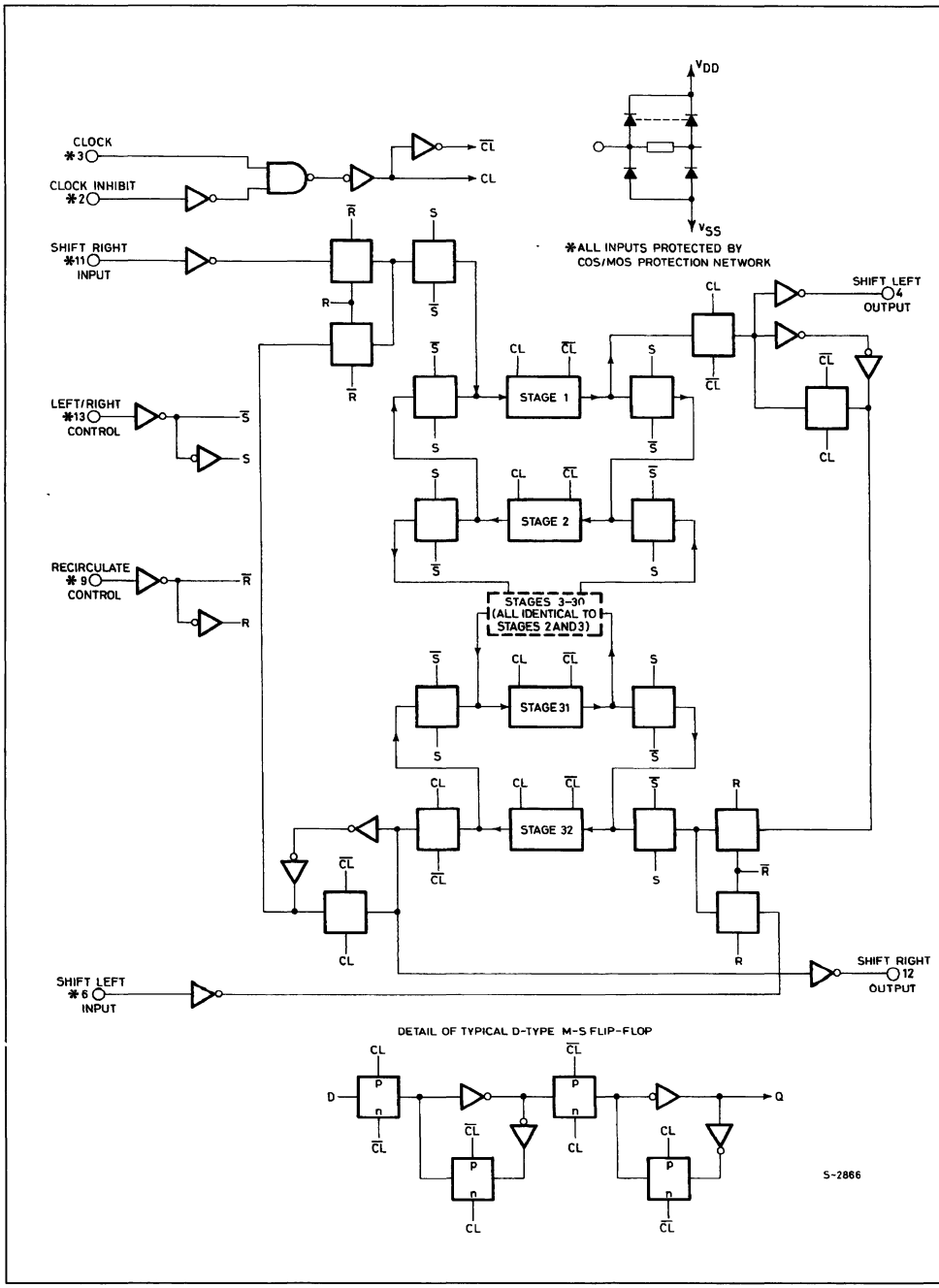
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to + 18<br>3 to + 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAM



## TRUTH TABLES

CONTROL

| Left/Right Control | Clock · Inhibit | Recirculate Control | Action | Input Bit Origin |
|---|---|---|---|---|
| 1 | 0 | 1 | Shift Left | Shift Left Input |
| 1 | 0 | 0 | Shift Left | Stage 1 |
| 0 | 0 | 1 | Shift Right | Shift Right Input |
| 0 | 0 | 0 | Shift Right | Stage 32 |
| X | 1 | X | No Shift | – |

DATA TRANSFER

| Initial State | | | Clock | Resulting State | |
|---|---|---|---|---|---|
| Data Input | Clock Inhibit | Internal Stage | Level Change | Internal Stage Q | Output |
| 0 | 0 | X | ⎍ | 0 | NC |
| X | 0 | 0 | ⎏ | NC | 0 |
| 1 | 0 | X | ⎍ | 1 | NC |
| X | 0 | 1 | ⎏ | NC | 1 |
| X | 1 | 1 | X | NC | NC |

0 = Low level  1 = High level  X= Don't Care  NC = No change.

* For Shift-Right Mode
Data Input = SHIFT-RIGHT INPUT (Pin 11)
Internal Stage = Stage 1 (Q1)
Output = SHIFT-LEFT OUTPUT (Pin 4).

For Shift-left Mode
Data input = SHIFT LEFT INPUT (Pin 6)
Internal Stage = Stage 32 (Q32)
Output = SHIFT-RIGHT OUTPUT (Pin 12)

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | Max. | 25°C Min. | Typ. | Max. | $T_{High}$* Min. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4 95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9 95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0 05 | | 0.05 | |

* $T_{Low}$ = – 55°C for **HCC** device : – 40°C for **HCF** device
* $T_{High}$ = + 125°C for **HCC** device + 85°C for **HCF** device
The Noise Margin for both "1" and "0" level is 1V min with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2.5 V min. with $V_{DD}$ = 15V.

## STATIC ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | | Test Conditions | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5 V min with $V_{DD}$ = 15V

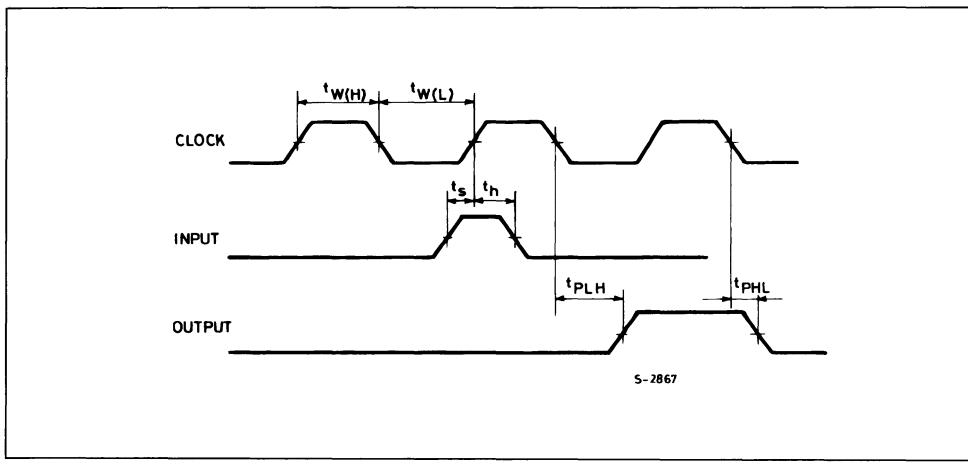
## DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall time = 20ns)

| Symbol | Parameter | Test Conditions | Value | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time Clock to Shift Left/Right Output | | 5 | | 360 | 720 | ns |
| | | | 10 | | 165 | 330 | |
| | | | 15 | | 115 | 230 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

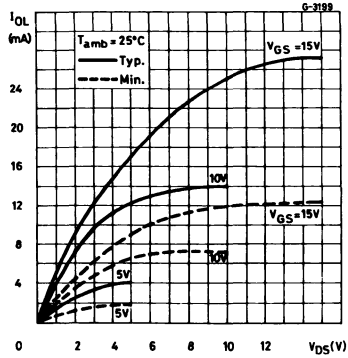
## DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{setup}$ | Data Setup Time | | 5 | 100 | 50 | | ns |
| | | | 10 | 20 | 10 | | |
| | | | 15 | 10 | 5 | | |
| $t_{hold}$ | Data Hold Time | | 5 | 275 | 170 | | ns |
| | | | 10 | 100 | 75 | | |
| | | | 15 | 75 | 50 | | |
| $t_W$ | Clock Input Pulse Width Low Level | | 5 | 450 | 225 | | ns |
| | | | 10 | 230 | 115 | | |
| | | | 15 | 190 | 95 | | |
| $t_W$ | Clock Input Pulse Width High Level | | 5 | 280 | 140 | | ns |
| | | | 10 | 150 | 75 | | |
| | | | 15 | 140 | 70 | | |
| $f_{CL}$ | Maximum Clock Input Frequency | | 5 | 1 | 2 | | MHz |
| | | | 10 | 2.5 | 5 | | |
| | | | 15 | 3 | 6 | | |

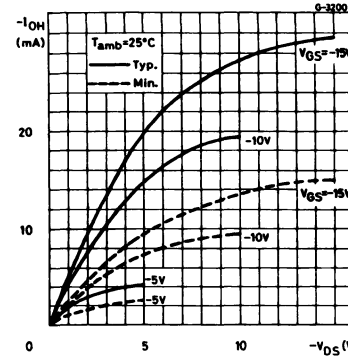
## WAVEFORMS



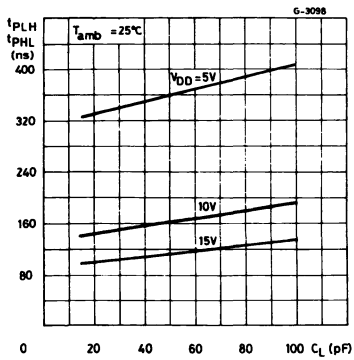
Output Low (sink) Current Characteristics.



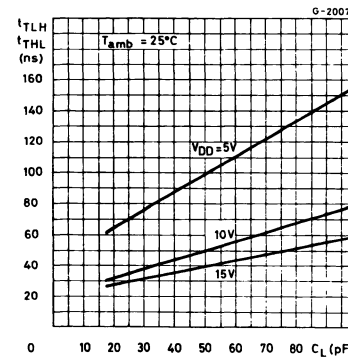

Output High (source) Current Characteristics.



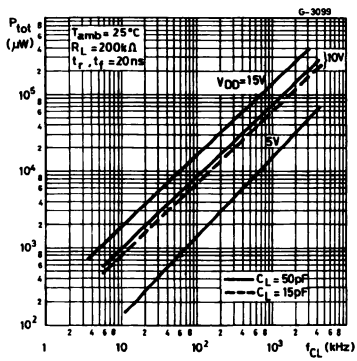

Typical Propagation Delay Time (clock to shift left right) vs. Load Capacitance.




Typical Transition Time vs. Load Capacitance.

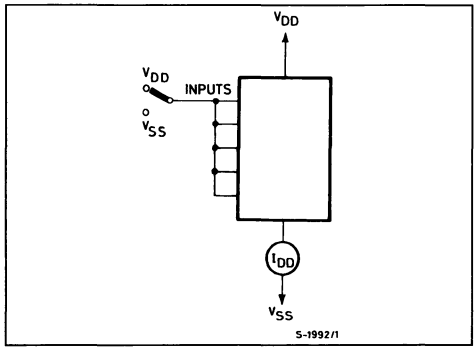



Typical Dynamic Power Dissipation vs. Clock Frequency .

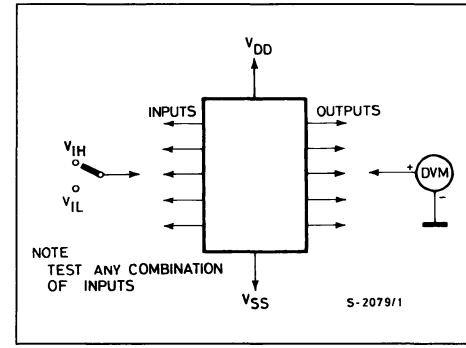


## TEST CIRCUITS

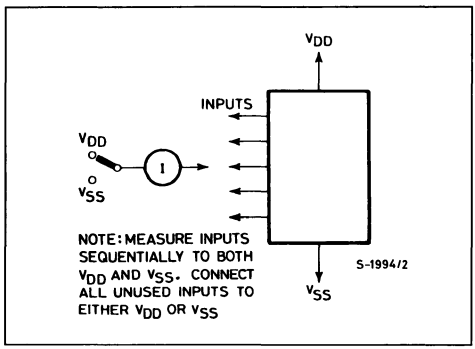
Quiescent Device Current.




Input Voltage.




Input Leakage Current.

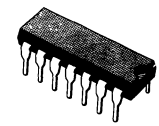


SGS-THOMSON MICROELECTRONICS

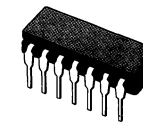
# HCC/HCF40101B

## 9-BIT PARITY GENERATOR/CHECKER

- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED AT 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

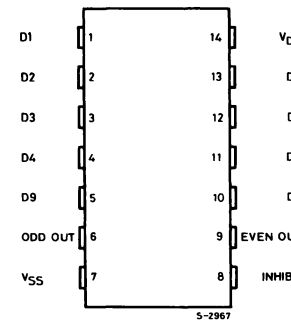
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC40101BF HCF40101BM1
HCF40101BEY HCF40101BC1

**PIN CONNECTIONS**

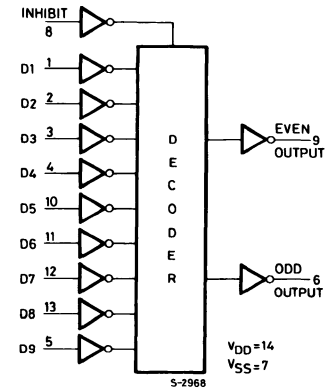



### DESCRIPTION

The **HCC40101B** (extended temperature range) and **HCF40101B** (intermediate temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and plastic micro package.

The **HCC/HCF40101B** is a 9-bit (8 data bits plus 1 parity bit) parity generator/checker. It may be used to detect errors in data transmission or data retrieval. Odd and even outputs facilitate odd or even parity generation and checking. When used as a parity generator, a parity bit is supplied along with the data to generate an even or odd parity output. When used a parity checker, the received data bits and parity bits are compared for correct parity. The even or odd outputs are used to indicate an error in the received data. Word-length capability is expandable by cascading. The **HCC/HCF40101B** is also provided with an inhibit control. If the inhibit control is set at logical "1", the even and odd outputs go to a logical "0".

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

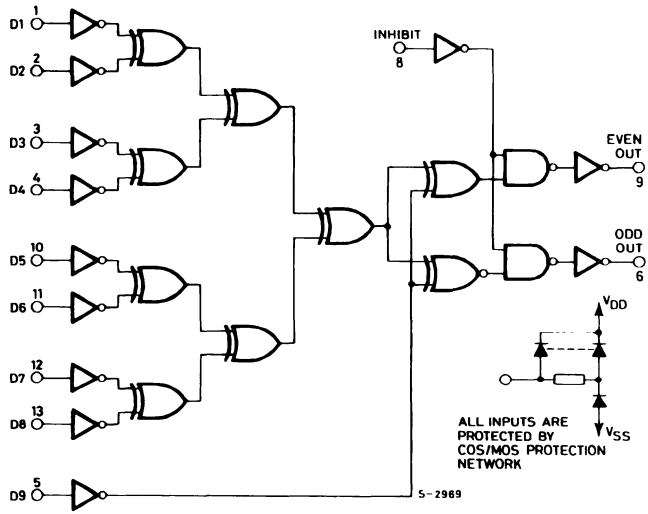
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltages are with respect to $V_{SS}$ (GND).

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAM




## TRUTH TABLE

| Inputs | | Outputs | |
|---|---|---|---|
| D1-D9 | Inhibit | Even | Odd |
| $\Sigma$ 1's = Even | 0 | 1 | 0 |
| $\Sigma$ 1's = Odd | 0 | 0 | 1 |
| X | 1 | 0 | 0 |

X = Don't Care
Logic 1 = High
Logic 0 = Low.

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

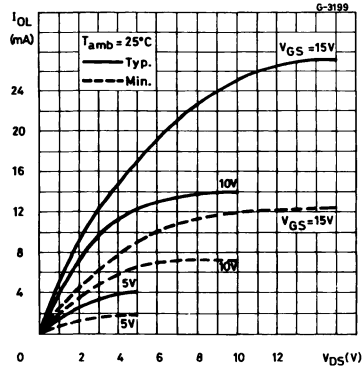
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0 04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3 2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device
* $T_{High}$ = + 125°C for **HCC** device + 85°C for **HCF** device
The Noise Margin for both "1" and "0" level is . 1V min. with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2.5V min with $V_{DD}$ = 15V.

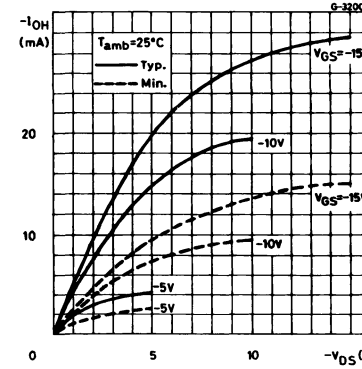
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall time = 20ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time | | 5 | | 350 | 700 | ns |
| | | | 10 | | 150 | 300 | |
| | | | 15 | | 100 | 200 | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time Inhibit to Output | | 5 | | 140 | 280 | ns |
| | | | 10 | | 70 | 140 | |
| | | | 15 | | 50 | 100 | |
| $t_{TLH}$, $t_{THL}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

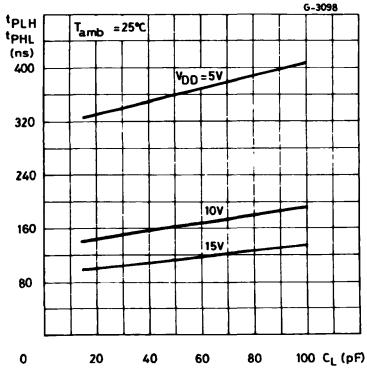
Output Low (sink) Current Characteristics.



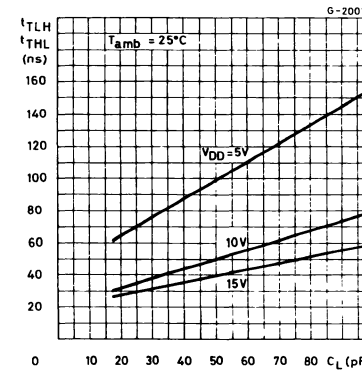

Output High (source) Current Characteristics.



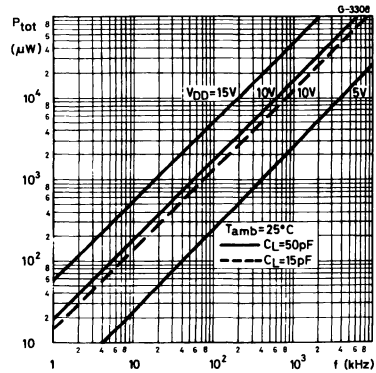

Typical Propagation Delay Time vs. Load Capacitance.




Typical Transition Time vs. Load Capacitance.

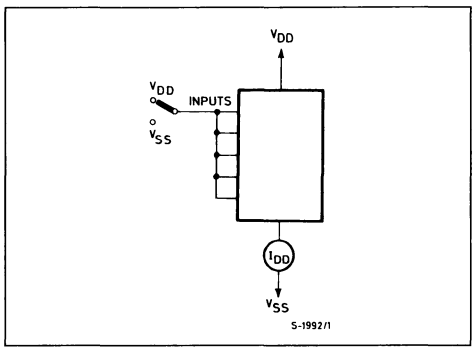


Typical Dynamic power Dissipation vs. Input Frequency.

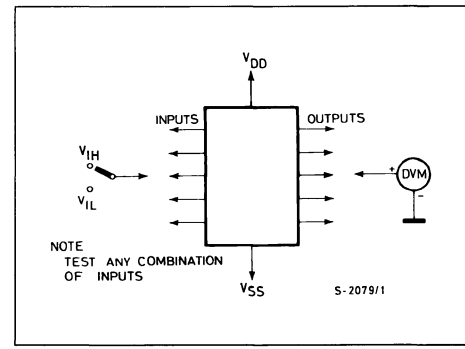



## TEST CIRCUITS

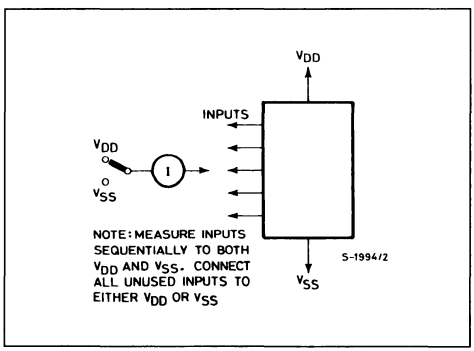
Quiescent Device Current.



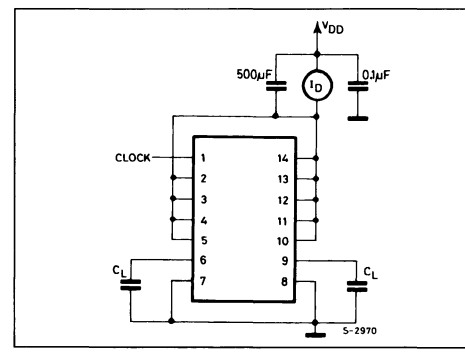

Input Voltage.




Input Leakage Current.




Dynamic Power Dissipation.

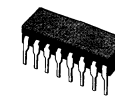


# 8-STAGE PRESETTABLE SYNCHRONOUS DOWN COUNTERS

**40102B 2-DECADE BCD TYPE**
**40103B 8-BIT BINARY TYPE**

- SYNCHRONOUS OR ASYNCHRONOUS PRESET
- MEDIUM-SPEED OPERATION : $f_{CL}$ = 3.6MHz (TYP.) @ $V_{DD}$ = 10V
- CASCADABLE
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13 A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

**EY**
(Plastic Package)



**F**
(Ceramic Package)

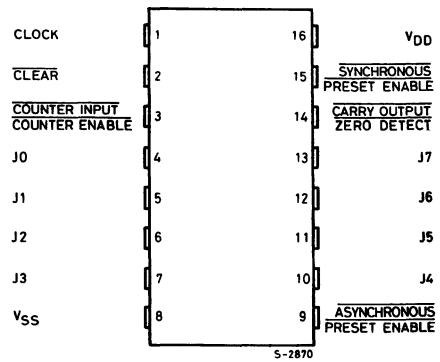
**C1**
(Chip Carrier)

**ORDER CODES :**
HCC401XXBF HCF401XXBEY
HCF401XXBC1

## DESCRIPTION

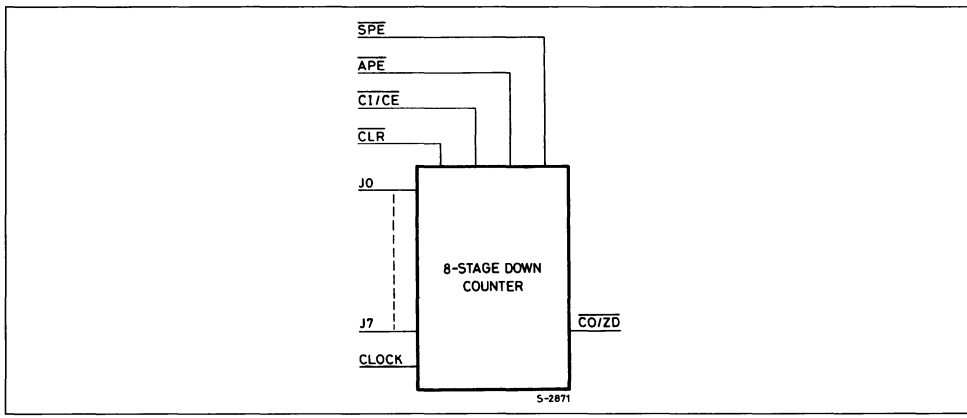
The **HCC40102B**, **HCC40103B**, (extended temperature range) and the **HCF40102B**, **HCF40103B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package. The **HCC/HCF40102B**, and **HCC/HCF40103B** consist of an 8-stage synchronous down counter with a single output which is active when the internal count is zero. The **HCC/HCF40102B** is configured as two cascaded 4-bit BCD counters, and the **HCC/HCF40103B** contains a single 8-bit binary counter. Each type has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the CARRY-OUT/ZERO-DETECT output are active-low logic. In normal operation, the counter is decremented by one count on each positive transition of the CLOCK. Counting is inhibited when the CARRY-IN/COUNTER ENABLE (CI/CE) input is high. The CARRY-OUT/ZERO-DETEC (CO/ZD) output goes low when the count reaches zero if the CI/CE input is low, and remains low for one full clock period. When the SYNCHRONOUS PRESET-ENABLE (SPE) input is low, data at the JAM input is clocked into the counter on the next positive clock transition regardless of the state of the CI/CE input. When the ASYNCHRONOUS PRESET-ENABLE (APE) input is low, data at the

**PIN CONNECTIONS**



JAM inputs is asynchronously forced into the counter regardless of the state of the SPE, CI/CE, or CLOCK inputs. JAM inputs JO-J7 represent two 4-bit BCD words for the **HCC/HCF40102B** and a single 8-bit binary word for the **HCC/HCF40103B**. When the CLEAR (CLR) input is low, the counter is asynchronously cleared to its maximum count ($99_{10}$ for the **HCC/HCF40102B** and $255_{10}$ for the**HCC/HCF40103B)** regardless of the state of any other input. The precedence relationship between control input is indicated in the truth table. If all control inputs are high at the tieme of zero count, the counters will jump to the maximum count, giving a counting sequence of 100 or 256 clock pulses long. The **HCC/HCF40102B** and **HCC/HCF40103B** may be cascaded using the CI/CE input and the

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

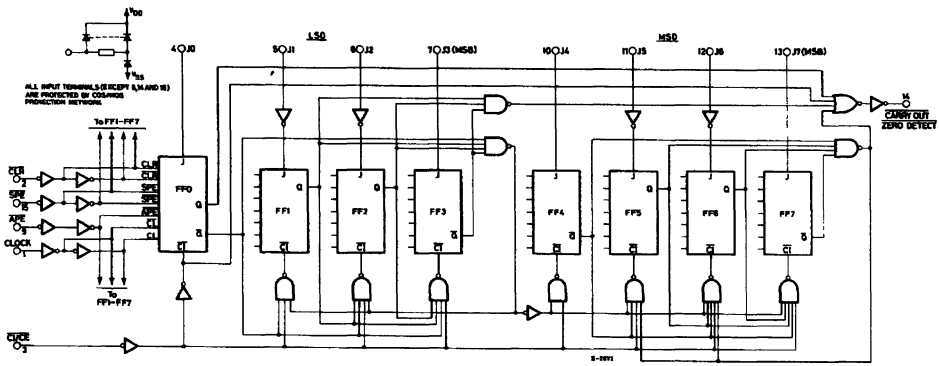
* All voltages are with respect to $V_{SS}$ (GND)

## RECOMMENDED OPERATING CONDITIONS

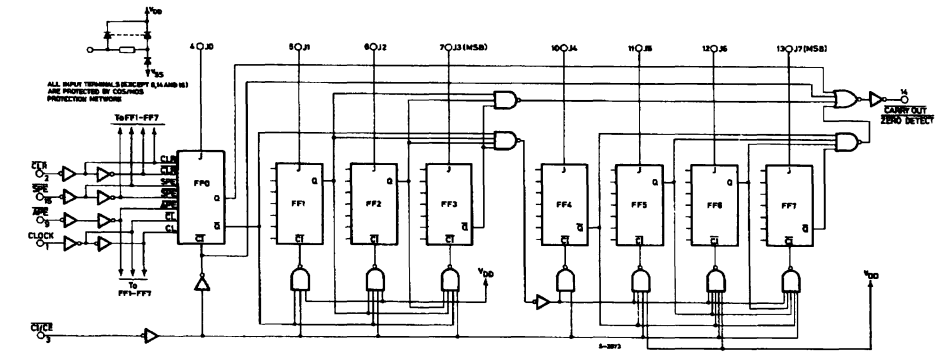
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAMS

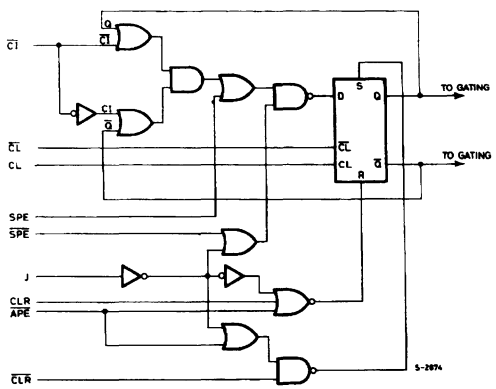
**40102B**




**40103B**



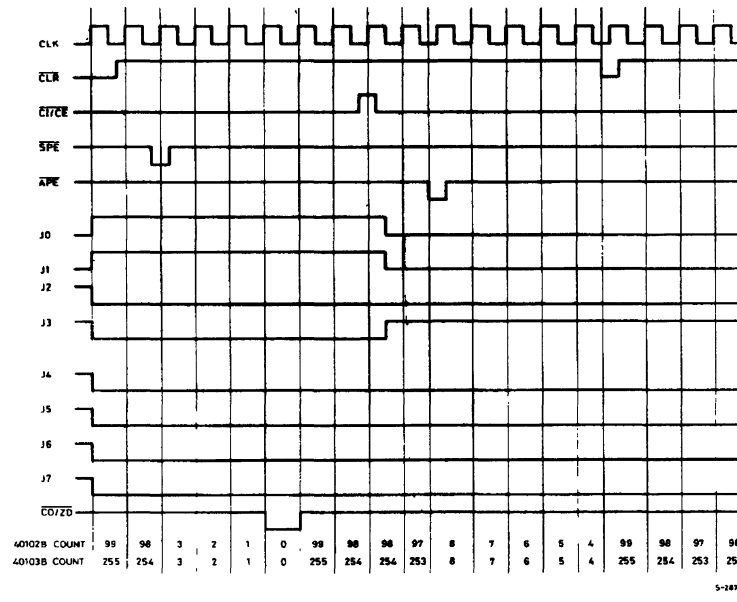

Detail logic diagram for flip-flops, FF0-FF7 used in logic diagrams for **40102B** and **40103B**.



## LOGIC DIAGRAMS (continued)

Timing Diagram for 40102B and 40103B

**40102B**




## TRUTH TABLE

| Control Inputs | | | | Preset Mode | Action |
|---|---|---|---|---|---|
| $\overline{CLR}$ | $\overline{APE}$ | $\overline{SPE}$ | $\overline{CI/CE}$ | | |
| 1 | 1 | 1 | 1 | Synchronous | Inhibit Counter |
| 1 | 1 | 1 | 0 | | Count Down |
| 1 | 1 | 0 | X | | Preset on Next Positive Clock Transition |
| 1 | 0 | X | X | Asynchronous | Preset Asynchrounously |
| 0 | X | X | X | | Clear to Maximum Count |

**Notes** : 1. 0 = Low level
1 = High level
X = Don't care
2. Clock connected to clock input.
3. Synchronous operation changes occur on negative-to-positive clock transitions.
JAM inputs . HCC/HCF010B ; MSD = J7, J6, J5, J4 (J7 is MSB)
LSD = J3, J2, J1, J0 (J3 is MSB)
HCC/HCF40103B Binary ; MSB = J7, LSB = J0

**STATIC ELECTRICAL CHARACTERISTICS** (over recommended operating conditions)

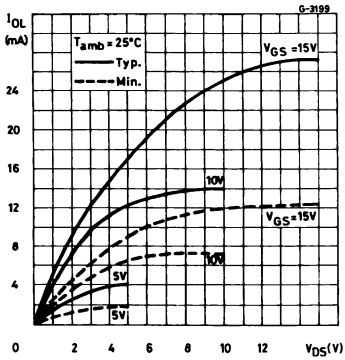
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5 V min. with $V_{DD}$ = 15V.

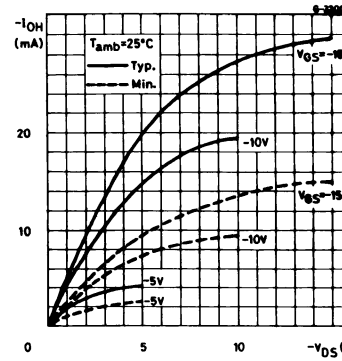
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall time = 20ns)

| Symbol | Parameter | | Test Conditions | Value | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time | Clock to-out | | 5 | | 300 | 600 | ns |
| | | | | 10 | | 130 | 260 | |
| | | | | 15 | | 95 | 190 | |
| | | Carry In/Counter Enable-to-output | | 5 | | 200 | 400 | ns |
| | | | | 10 | | 90 | 180 | |
| | | | | 15 | | 65 | 130 | |
| | | Asynchronous Preset Enable-to-output | | 5 | | 650 | 1300 | |
| | | | | 10 | | 300 | 600 | |
| | | | | 15 | | 200 | 400 | |
| | | $\overline{\text{Clear}}$-to-output | | 5 | | 375 | 750 | ns |
| | | | | 10 | | 180 | 360 | |
| | | | | 15 | | 100 | 200 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | | 5 | | 100 | 200 | ns |
| | | | | 10 | | 50 | 100 | |
| | | | | 15 | | 40 | 80 | |
| $t_W$ | Pulse Width | Clock Pulse Width | | 5 | 300 | 150 | | ns |
| | | | | 10 | 180 | 90 | | |
| | | | | 15 | 80 | 40 | | |
| | | $\overline{\text{CLR}}$ Pulse Width | | 5 | 320 | 160 | | ns |
| | | | | 10 | 160 | 80 | | |
| | | | | 15 | 100 | 50 | | |
| | | $\overline{\text{APE}}$ Pulse Width | | 5 | 360 | 180 | | ns |
| | | | | 10 | 160 | 80 | | |
| | | | | 15 | 120 | 60 | | |
| $t_{setup}$ | Setup Time | $\overline{\text{SPE}}$ Setup Time | | 5 | 280 | 140 | | ns |
| | | | | 10 | 140 | 70 | | |
| | | | | 15 | 100 | 50 | | |
| | | JAM Setup Time | | 5 | 200 | 100 | | ns |
| | | | | 10 | 80 | 40 | | |
| | | | | 15 | 60 | 30 | | |
| $f_{CL}$ | Maximum Clock Input Frequency | | | 5 | 0.7 | 1.4 | | MHz |
| | | | | 10 | 1.8 | 3.6 | | |
| | | | | 15 | 2.4 | 4.8 | | |

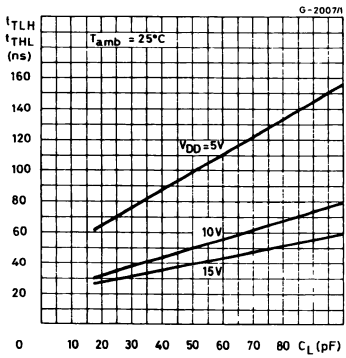
Output Low (sink) Current Characteristics.



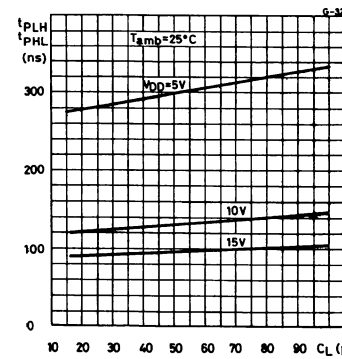

Output High (source) Current Characteristics.



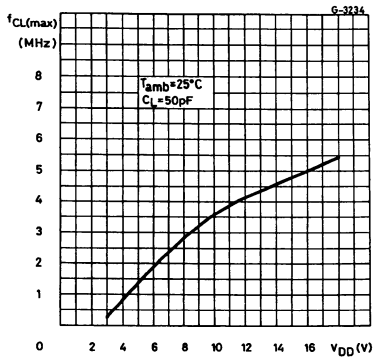

Typical Transition Time vs. Load Capacitance.



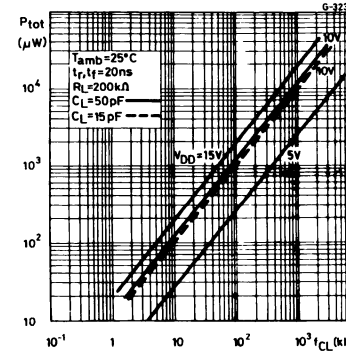

Typical Propagation Delay Time vs. Load Capacitance (clock to $\overline{CO}$/ZD).




Typical Maximum Clock Input Frequency vs. Supply Voltage.

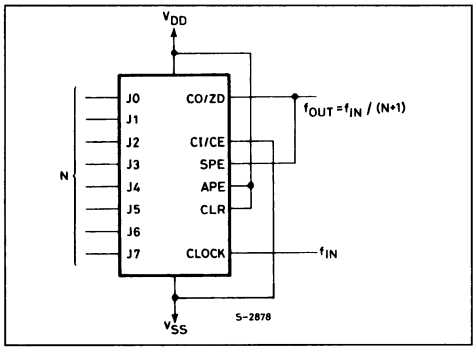



Typical Dynamic Power Dissipation vs. Frequency.

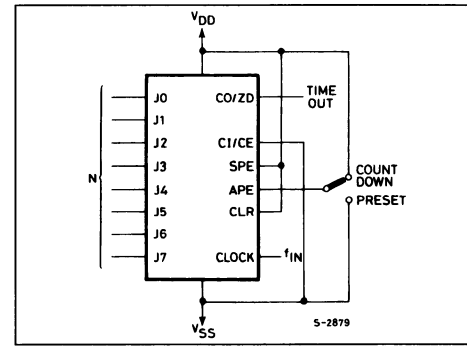


## TYPICAL APPLICATIONS

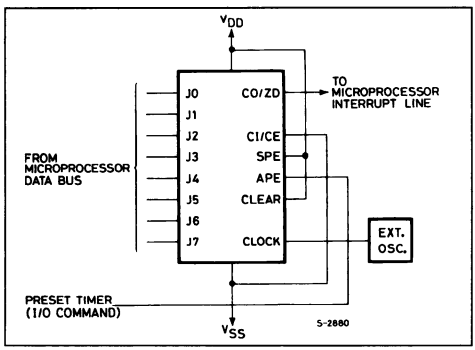
Divide-by-"N" Counter.



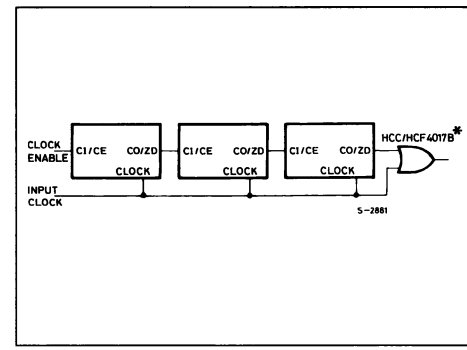

Programmable Timer.




Microprocessor Interrupt Timer.

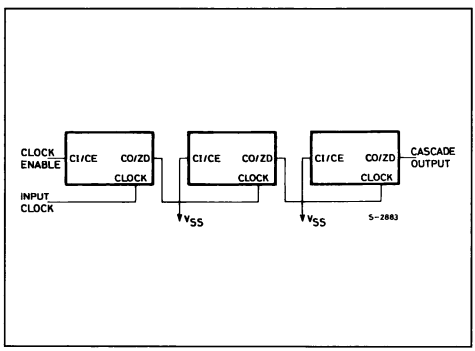



Synchronous Cascading.



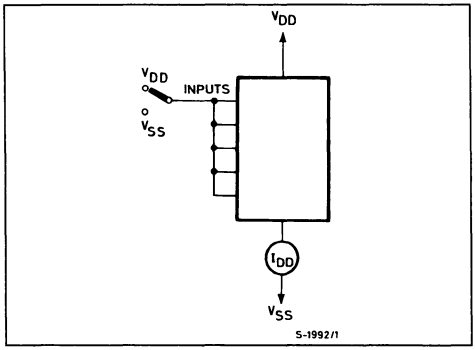

* An output spike (160ns @ $V_{DD}$ = 5V) occurs whenever two or more devices are cascaded in the parallel-clocked mode because the clock-to-carry out delay is greater than the carry-in-to-carry out delay. This spike is eliminated by gating the out put of the last device with the clock as shown.

Microprocessor Interrupt Timer.

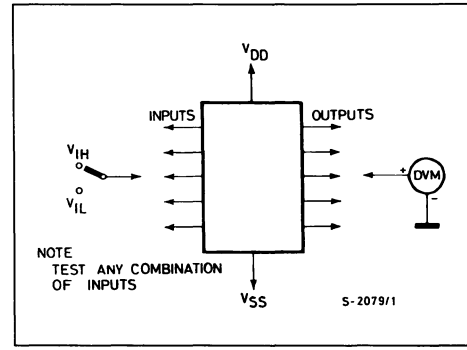


## TEST CIRCUITS

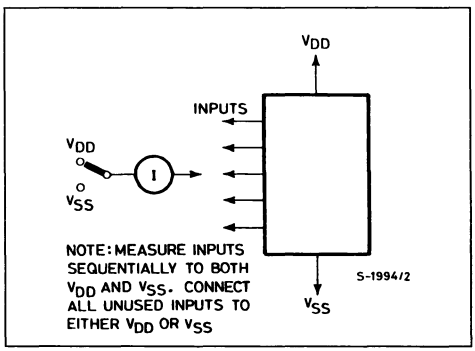
Quiescent Device Current.



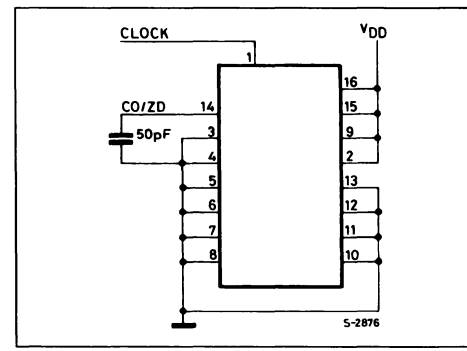

Input Voltage.



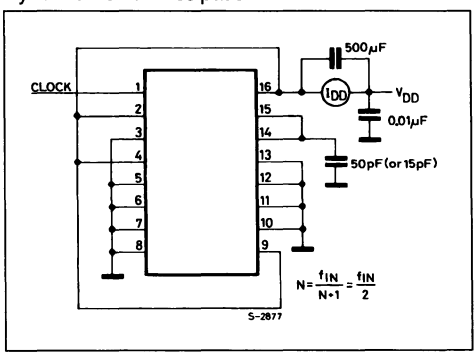

Input Current.




Maximum Clock Frequency.




Dynamic Power Dissipation.



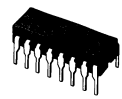
SGS-THOMSON MICROELECTRONICS

# HCC/HCF40104B
# HCC/HCF40194B

## 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

- MEDIUM-SPEED OPERATION : $f_{CL}$ = 9MHz (typ.) @ $V_{DD}$ = 10V
- FULLY STATIC OPERATION
- SYNCHRONOUS PARALLEL OR SERIAL OPERATION
- THREE-STATE OUTPUTS (**HCC/HCF40104B**)
- ASYNCHRONOUS MASTER RESET (**HCC/HCF40194B**)
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT AT 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

**EY**
(Plastic Package)



**F**
(Ceramic Package)

**C1**
(Plastic Chip Carrier)

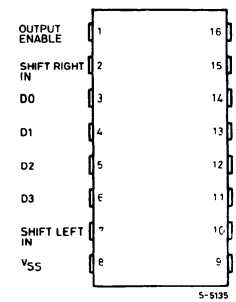
**ORDER CODES :**
HCC401XXBF HCF401XXBEY
HCF401XXBC1

### DESCRIPTION

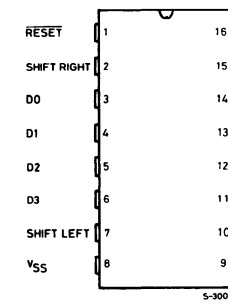
The **HCC40104B, HCC40194B**, (extended temperature range) and the **HCC40104B, HCF40194B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF 40104B** is a universal shift register featuring parallel inputs, parallel outputs, SHIFT RIGHT and SHIFT LEFT serial inputs, and a high-impedance third output state allowing the device to be used in bus-organized systems. In the parallel-load mode (S0 and S1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift-right and shift-left are accomplished synchronously on the positive clock edge with serial data entered at the SHIFT RIGHT and SHIFT LEFT serial inputs, respectively. Clearing the register is accomplished by setting both mode controls low and clocking the register. When the output enable input is low, all outputs assume the high impedance state. The **HCC/HCF40194B** is a universal shift register featuring parallel inputs, parallel outputs SHIFT RIGHT and SHIFT LEFT serial inputs, and a direct overriding clear input. In the parallel-load mode (S0 and S1 are high), data is loaded into the associated

### PIN CONNECTIONS

**40104B**

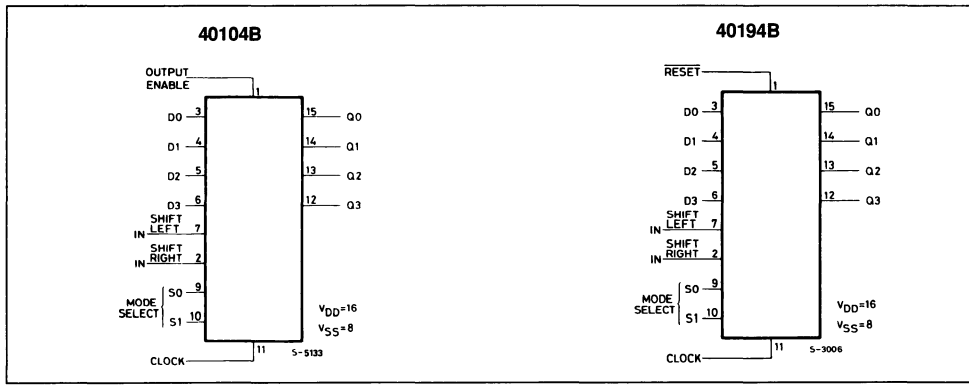



**40194B**



flip-flop and appears at the output after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift right and shift left are accomplished synchronously on the positive clock edge with data entered at the SHIFT RIGHT and SHIFT LEFT serial inputs, respectively. Clocking of the register is inhibited when both mode control inputs are low. When low, the RESET input resets all stages and forces all outputs low. The **HCC/HCF40194B** is similar to industry types 340194 and MC40194.

## FUNCTIONAL DIAGRAMS




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

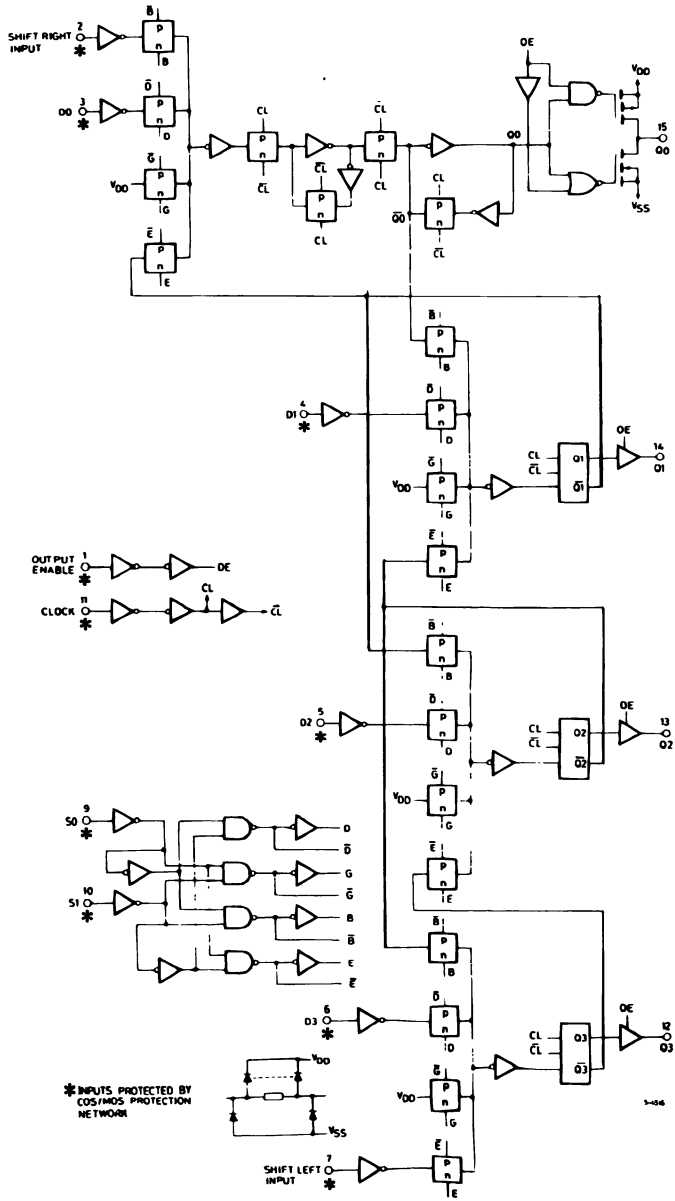
* All voltages values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

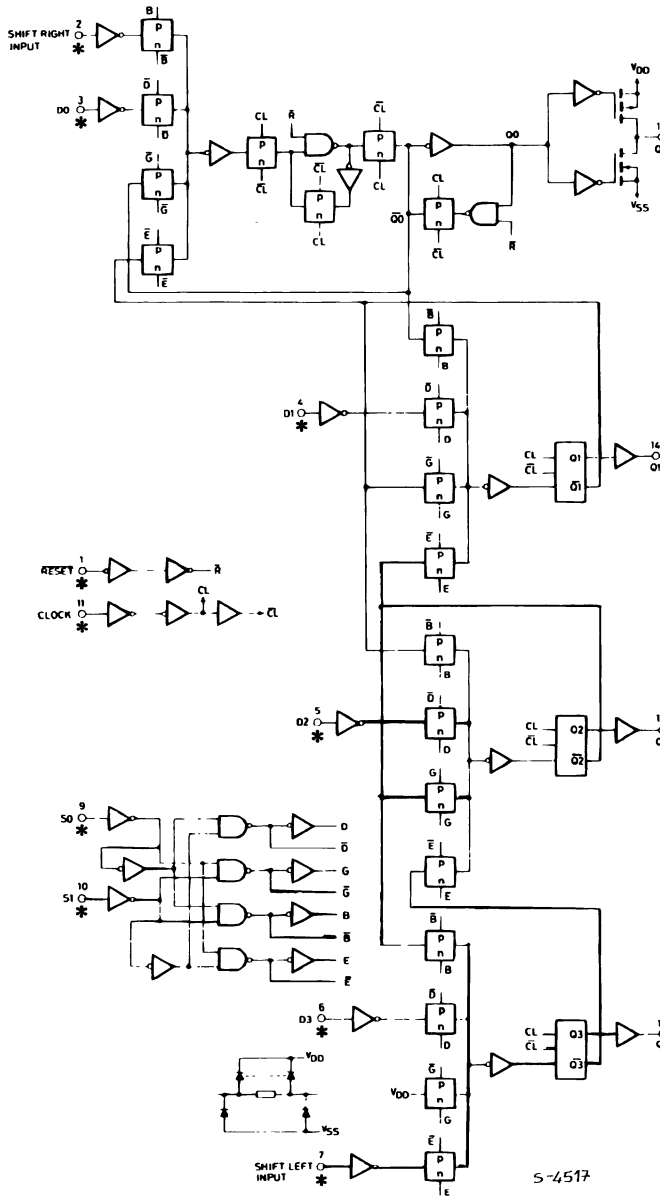
## LOGIC DIAGRAMS

40104B



## LOGIC DIAGRAMS

**40194B**



**STATIC ELECTRICAL CHARACTERISTICS** (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{LOW}$= − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{HIGH}$= + 125°C for **HCC** device : + 85°C for **HCF** device.
The noise Margin for both "1" and "0" level is · 1V min with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5 min. with $V_{DD}$ = 15V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall time = 20ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$,$t_{PHL}$ | Propagation Delay Time Clock to Q | | 5 | | 220 | 440 | ns |
| | | | 10 | | 100 | 200 | |
| | | | 15 | | 70 | 140 | |
| $t_{PZH}$,$t_{PZL}$, $t_{PLZ}$ | 3-state Outputs ■ High Impedance | | 5 | | 80 | 160 | ns |
| | | | 10 | | 35 | 70 | |
| | | | 15 | | 25 | 50 | |
| $t_{PHZ}$ | | | 5 | | 45 | 90 | ns |
| | | | 10 | | 25 | 50 | |
| | | | 15 | | 20 | 40 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_{setup}$ | Setup Time D0,D3,SR, SL to Clock | | 5 | | 80 | 100 | ns |
| | | | 10 | | 35 | 70 | |
| | | | 15 | | 20 | 50 | |
| | S0, S1 to Clock | | 5 | | 200 | 400 | ns |
| | | | 10 | | 110 | 220 | |
| | | | 15 | | 65 | 130 | |
| $t_{hold}$ | Hold Time D0,D3,SR, SL to Clock | | 5 | | – 65 | 0 | ns |
| | | | 10 | | – 25 | 0 | |
| | | | 15 | | – 15 | 0 | |
| | S0, S1 to Clock | | 5 | | – 170 | 0 | ns |
| | | | 10 | | – 95 | 0 | |
| | | | 15 | | – 55 | 0 | |
| $t_W$ | Clock Pulse Width | | 5 | | 90 | 180 | ns |
| | | | 10 | | 40 | 180 | |
| | | | 15 | | 25 | 50 | |
| $f_{CL}$ | Clock Input Frequency | | 5 | 3 | 6 | | MHz |
| | | | 10 | 6 | 12 | | |
| | | | 15 | 8 | 15 | | |
| $t_r$, $t_f$ | Clock Input Rise or Fall Time | | 5 | | | 1000 | µs |
| | | | 10 | | | 100 | |
| | | | 15 | | | 100 | |
| $t_W$ | Reset Pulse Width* | | 5 | | 150 | 300 | ns |
| | | | 10 | | 100 | 200 | |
| | | | 15 | | 70 | 140 | |
| $t_{PRHL}$ | Propagation Delay Reset* | | 5 | | 230 | 460 | ns |
| | | | 10 | | 90 | 180 | |
| | | | 15 | | 65 | 130 | |

■ For 40104B series only  * For 40194B series only.

## TRUTH TABLES

40104B

| Clock▲ | Mode Select | | Output Enable | Action |
|---|---|---|---|---|
| | S0 | S1 | | |
| _/‾ | 0 | 0 | 1 | Reset |
| _/‾ | 1 | 0 | 1 | Shift Right (Q0 toward Q3) |
| _/‾ | 0 | 1 | 1 | Shift Left (Q3 toward Q0) |
| _/‾ | 1 | 1 | 1 | Parallel Load |
| X | X | X | 0 | Operations occur as shown above, but outputs assume high impedance |

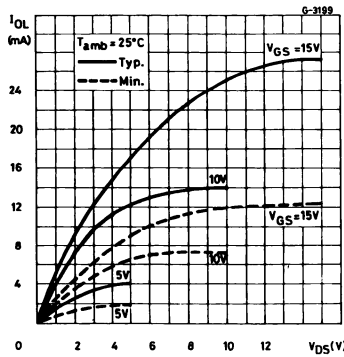
40194B

| Clock | Mode Select | | $\overline{\text{Reset}}$ | Action |
|---|---|---|---|---|
| | S0 | S1 | | |
| X | 0 | ∪ | 1 | No Change |
| _/‾ | 1 | 0 | 1 | Shift Right (Q0 toward Q3) |
| _/‾ | 0 | 1 | 1 | Shift Left (Q3 toward Q0) |
| _/‾ | 1 | 1 | 1 | Parallel Load |
| X | X | X | 0 | Reset |

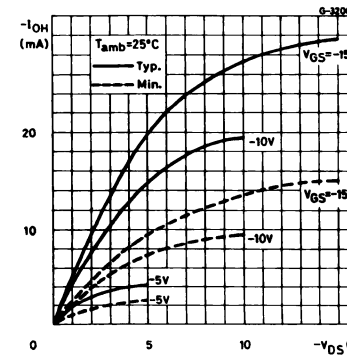
1=High level
0=Low level

X= Don't care
Δ = Level change

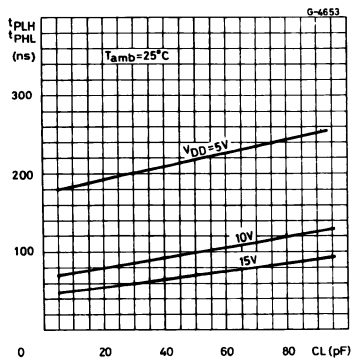
Output Low (sink) Current Characteristics.



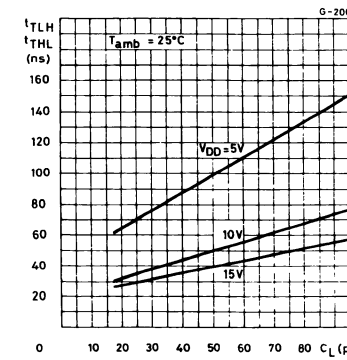

Output High (source) Current Characteristics.



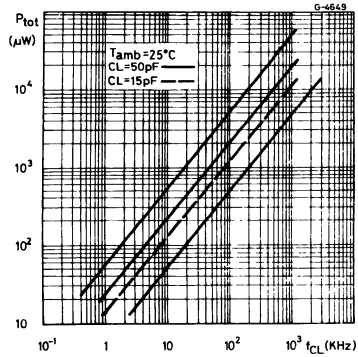

Typical Propagation Delay Time vs. Load Capacitance.




Typical Transition Time vs. Load Capacitance.

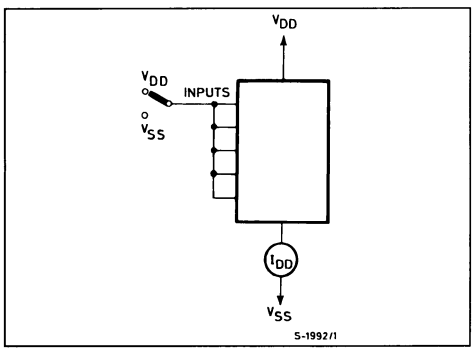


Typical Dynamic Power Dissipation vs. Frequency.

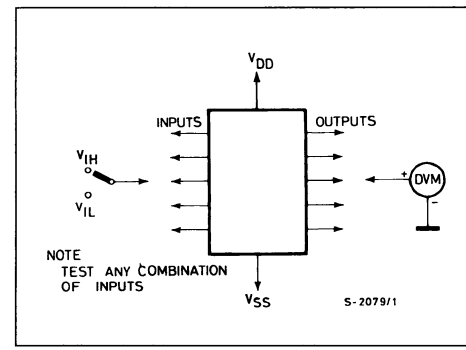



## TEST CIRCUITS

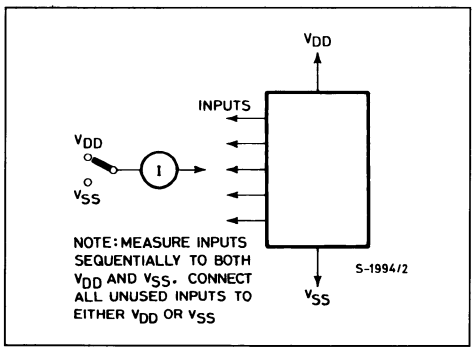
Quiescent Device Current.



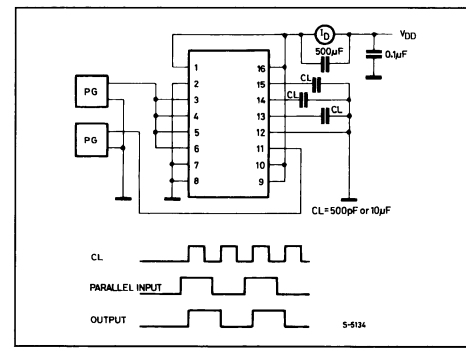

Input Voltage.




Input Leakage Current.




Dynamic Power Dissipation.



SGS-THOMSON MICROELECTRONICS

# HCC40105B
# HCF40105B

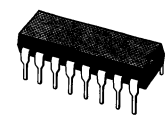
## FIFO REGISTER

- INDEPENDENT ASYNCHRONOUS INPUTS AND OUTPUTS
- 3-STATE OUTPUTS
- EXPANDABLE IN EITHER DIRECTION
- STATUS INDICATORS ON INPUT AND OUTPUT
- RESET CAPABILITY
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED AT 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

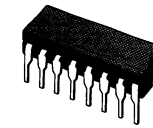
### DESCRIPTION

The **HCC40105B** (extended temperature range) and **HCF40105B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package.

The **HCC/HCF40105B** is a low-power first-in-first-out (FIFO) "elastic" storage register that can store 16 4-bit words. It is capable of handling input and output data at different shifting rates. This feature makes it particularly useful as a buffer between asynchronous systems. Each word position in the register is clocked by a control flip-flop, which stores a marker bit. A "1" signifies that the position's data is filled and a "0" denotes a vacancy in that position. The control flip-flop detects the state of the preceding flip-flop and communicates its own status to the succeeding flip-flop. When a control flip-flop is in the "0" state and sees a "1" in the preceding flip-flop, it generates a clock pulse that transfers data from the preceding four data latches into its own four data latches and resets the preceding flip-flop to "0". The first and last control flip-flops have buffered outputs. Since all empty locations "bubble" automatically to the input end, and all valid data ripple through to the output end, the status of the first control flip-flop (DATA-IN READY) indicates if the FIFO is full, and the status of the last flip-flop (DATA-OUT READY) indicates if the FIFO contains data. As the earliest data are removed from the bottom of the data stack (the output end), all data entered later will automatically propagate (ripple) toward the output.



**EY**
(Plastic Package)

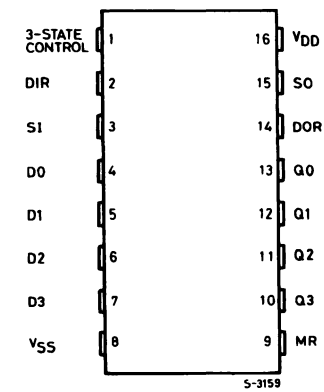


**F**
(Ceramic Package)

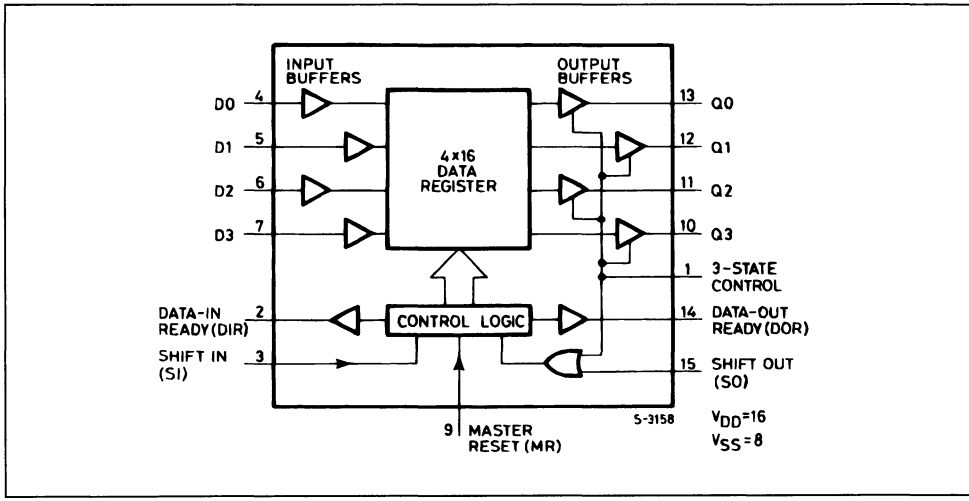
**C1**
(Chip Carrier)

**ORDER CODES :**
HCC40105BF HCF40105BEY
HCF40105BC1

**PIN CONNECTIONS**



## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

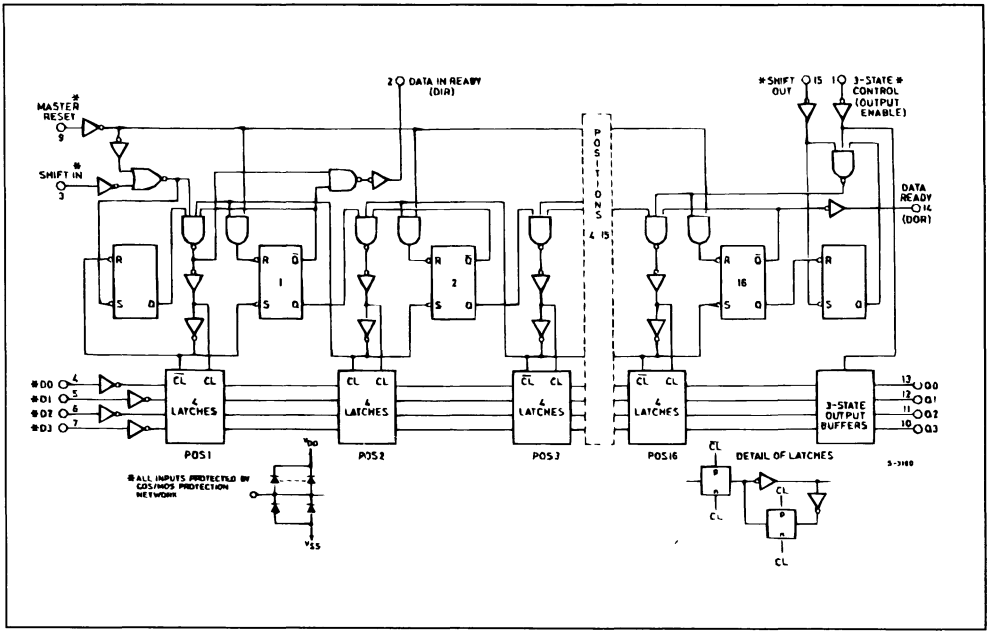
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltage values are referred to $V_{SS}$ pin voltage.

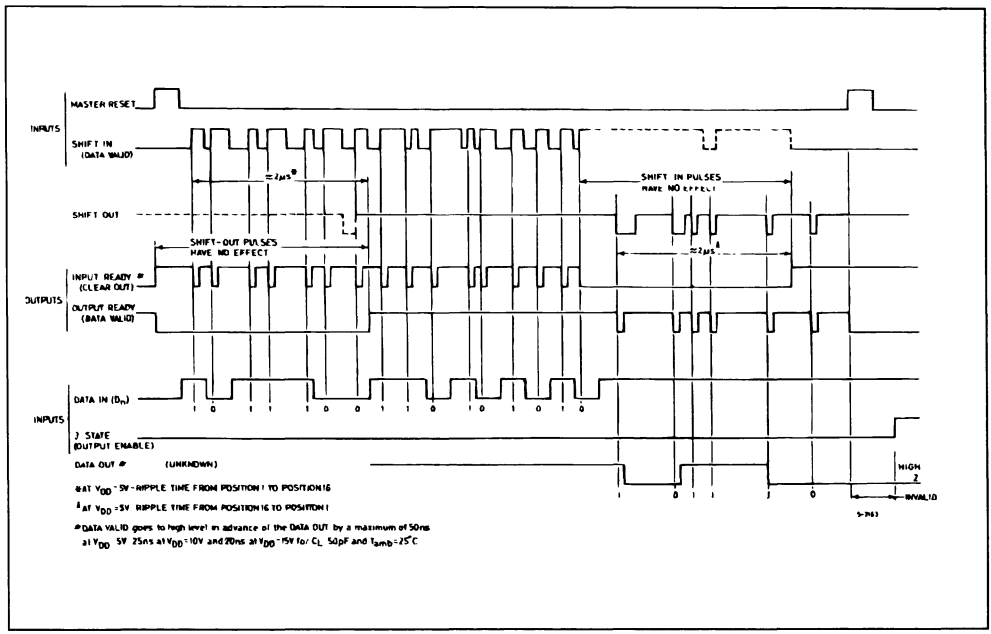
## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAM




## TIMING DIAGRAM



## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $I_{OH}$,$I_{OL}$** | 3-State Output Leakage Current | HCC Types | 0/18 | 0/18 | | 18 | | ± 0.4 | | $±10^{-4}$ | ± 0.4 | | ± 12 | μA |
| | | HCF Types | 0/15 | 0/15 | | 15 | | ± 1.0 | | $±10^{-4}$ | ± 1.0 | | ± 7.5 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

*$T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device
*$T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5 V min. with $V_{DD}$ = 15V.
* * Forced output disable.

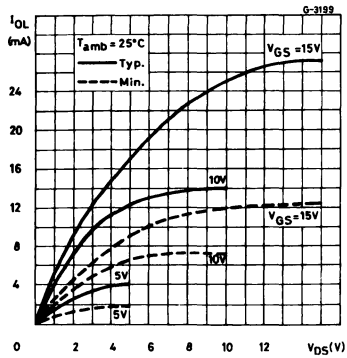
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3 %/°C, all input rise and fall time = 20 ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$ | Propagation Delay Time Shift-out or Reset to Data-out Ready | | 5 | | 185 | 370 | ns |
| | | | 10 | | 90 | 180 | |
| | | | 15 | | 65 | 130 | |
| $t_{PHL}$ | Propagation Delay Time Shift-in to Data-in Ready | | 5 | | 160 | 320 | ns |
| | | | 10 | | 65 | 130 | |
| | | | 15 | | 45 | 90 | |
| $t_{PZH}$, $t_{PZL}$ | Propagation Delay Time 3-state Control to Data-out | | 5 | | 140 | 280 | ns |
| | | | 10 | | 60 | 120 | |
| | | | 15 | | 40 | 80 | |
| $t_{PHZ}$, $t_{PLZ}$ | Propagation Delay Time 3-State Control to Data-out | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_{PLH}$ | Ripple-through Delay Input to Output | | 5 | | 2 | 4 | µs |
| | | | 10 | | 1 | 2 | |
| | | | 15 | | 0.7 | 1.4 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $f_I$ | Shift-in or Shift-out Rate | | 5 | | 1.5 | 3 | MHz |
| | | | 10 | | 3 | 6 | |
| | | | 15 | | 4 | 8 | |
| $t_{WH}$ | Shift-in Pulse Width | | 5 | 200 | 100 | | ns |
| | | | 10 | 80 | 40 | | |
| | | | 15 | 60 | 30 | | |
| $t_{WL}$ | Shift-out Pulse Width | | 5 | 360 | 180 | | ns |
| | | | 10 | 160 | 80 | | |
| | | | 15 | 100 | 50 | | |
| $t_r$ | Shift-in or Shift-out Rise Time | | 5 | | | 15 | µs |
| | | | 10 | | | 15 | |
| | | | 15 | | | 15 | |
| $t_f$ | Shift-in Fall Time | | 5 | | | 15 | µs |
| | | | 10 | | | 15 | |
| | | | 15 | | | 15 | |
| $t_f$ | Shift-out Fall Time | | 5 | | | 15 | µs |
| | | | 10 | | | 5 | |
| | | | 15 | | | 5 | |
| $t_{setup}$ | Data Setup Time | | 5 | 0 | | | ns |
| | | | 10 | 0 | | | |
| | | | 15 | 0 | | | |

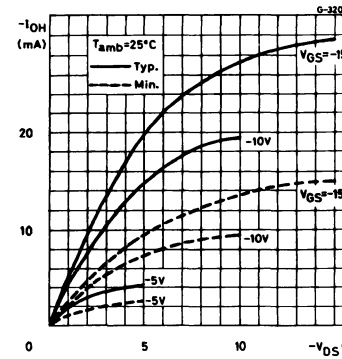
## DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{hold}$ | Data Hold Time | | 5 | 350 | 175 | | ns |
| | | | 10 | 150 | 75 | | |
| | | | 15 | 120 | 60 | | |
| $t_{WL}$ | Data–in Ready Pulse Width | | 5 | | 260 | 520 | ns |
| | | | 10 | | 100 | 120 | |
| | | | 15 | | 70 | 140 | |
| $t_{WL}$ | Data–out Ready Pulse Width | | 5 | | 220 | 440 | ns |
| | | | 10 | | 90 | 180 | |
| | | | 15 | | 665 | 130 | |
| $t_{WH}$ | Master Reset Pulse Width | | 5 | 200 | 100 | | ns |
| | | | 10 | 90 | 45 | | |
| | | | 15 | 60 | 30 | | |

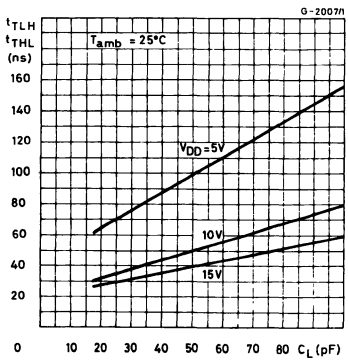
Output Low (sink) Current Characteristics.



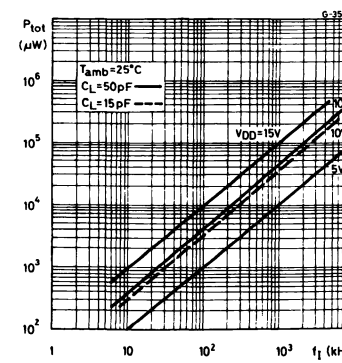

Output High (source) Current Characteristics.




Typical Transition Time vs. Load Capacitance.

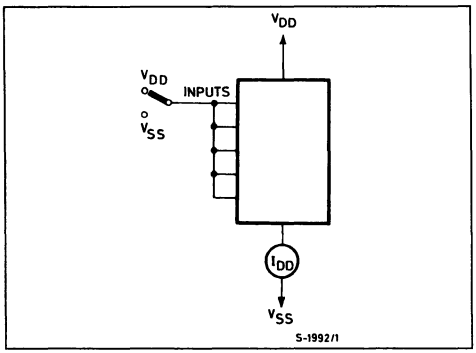



Typical Dynamic Power Dissipation vs. Frequency.

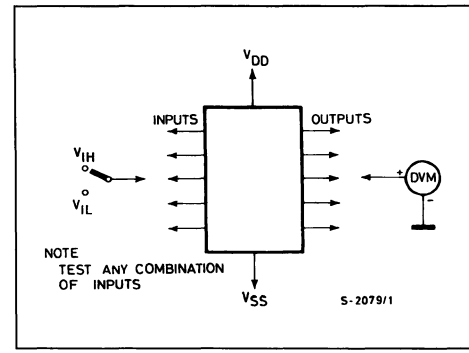


## TEST CIRCUITS

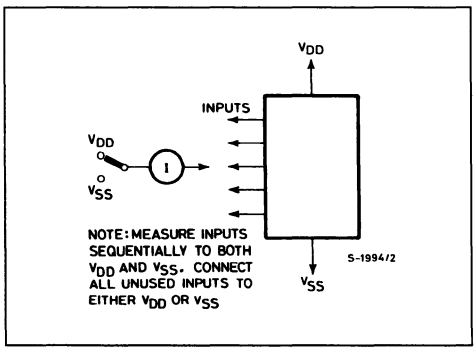
Quiescent Device Current.



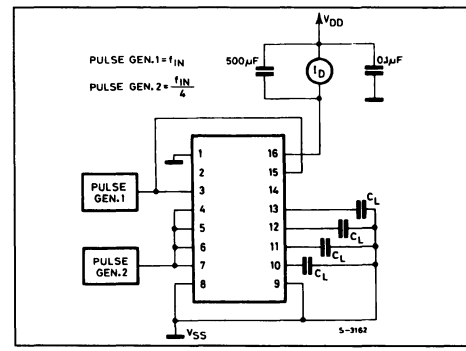

Input Voltage.




Input Leakage Current.

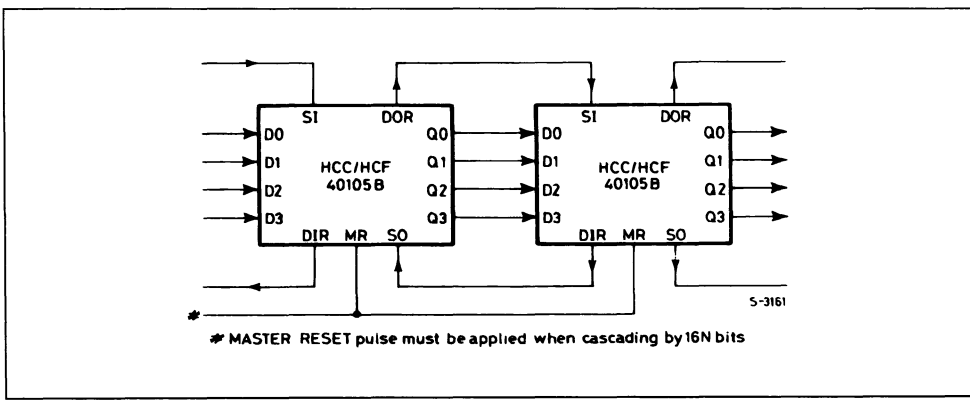



Dynamic Power Dissipation.

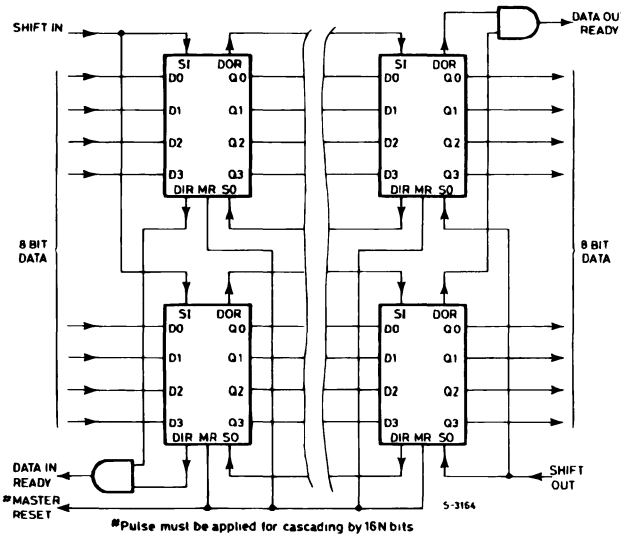



## TYPICAL APPLICATIONS

EXPANSION, 4 BITS–WIDE–BY–16 N–BITS LONG.



EXPANSION, 8 BITS–WIDE–BY–16 N–BITS LONG.




## APPLICATIONS INFORMATION

### LOADING DATA

Data can be entered whenever the DATA-IN READY (DIR) flag is high, by a low to high transition on the SHIFT-IN (SI) input. This input must go low momentarily before the next word is accepted by the FIFO. The DIR flag will go low momentarily, until the data have been transferred to the second location. The flag will remain low when all 16-word locations are filled with valid data, and further pulses on the SI input will be ignored until DIR goes high.

### UNLOADING DATA

As soon as the first word has rippled to the output, DATA-OUT READY (DOR) goes high, and data can be removed by a falling edge on the SO input. This falling edge causes the DOR signal to go low while the word on the output is dumped and the next word moves to the output. As long as valid data are available in the FIFO, the DOR signal will go high again signifying that the next word is ready at the output. When the FIFO is empty, DOR will remain low, and any further commands will be ignored until a "1" marker ripples down to the last control register, when DOR goes high. Unloading of data is inhibited while the 3-state control input is high. The 3-state control signal should not be shifted from high to low (data outputs turned on) while the SHIFT-OUT is at logic 0. This level change would cause the first word to be shifted out (unloaded) immediately and the data to be lost.

### CASCADING

The **HCC/HCF40105B** can be cascaded to form longer registers simply by connecting the DIR to SO and DOR to SI. In the cascaded mode, a MASTER RESET pulse must be applied after the supply voltage is turned on. For words wider than 4 bits, the DIR and the DOR outputs must be gated together with AND gates. Their outputs drive the SI and SO inputs in parallel, if expanding is done in both directions.

### 3-STATE OUTPUTS

In order to facilitate data busing, 3-state outputs are provided on the data output lines, while the load condition of the register can be detected by the state of the DOR output.

### MASTER RESET

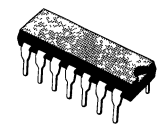
A high on the MASTER RESET (MR) sets all the control logic marker bits to "0". DOR goes low and DIR goes high. The contents of the data register are not changed, only declared invalid, and will be superseded when the first word is loaded.

SGS-THOMSON
MICROELECTRONICS

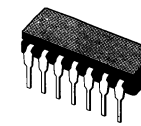
# HCC40106B
# HCF40106B

## HEX SCHMITT TRIGGERS

- SCHMITT-TRIGGER ACTION WITH NO EXTERNAL COMPONENTS
- HYSTERESIS VOLTAGE (TYP.) 0.9V AT $V_{DD}$ = 5V, 2.3V AT $V_{DD}$ = 10V AND 3.5V AT $V_{DD}$ = 15V
- NOISE IMMUNITY GREATER THAN 50%
- NO LIMIT ON INPUT RISE AND FALL TIME
- LOW $V_{DD}$ TO $V_{SS}$ CURRENT DURING SLOW INPUT RAMP
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED AT 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

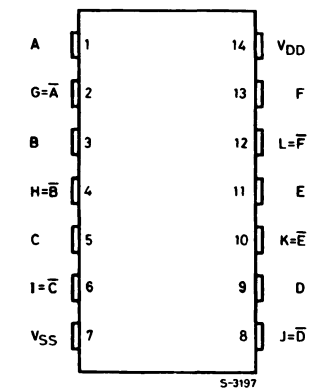
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC40106BF HCF40106BM1
HCF40106BEY HCF40106BC1

**PIN CONNECTIONS**

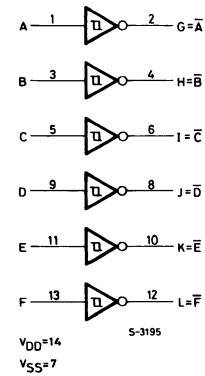



### DESCRIPTION

The **HCC40106B** (extended temperature range) and **HCF40106B** (intermediate temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and plastic micropackage.

The **HCC/HCF40106B** consists of six Schmitt-trigger circuits. Each circuit functions as an inverter with Schmitt-trigger action on the input. The trigger switches at different points for positive and negative-going signals. The difference between the positive-going voltage ($V_P$) and the negative-going voltage ($V_N$) is defined as hysteresis voltage ($V_H$).

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

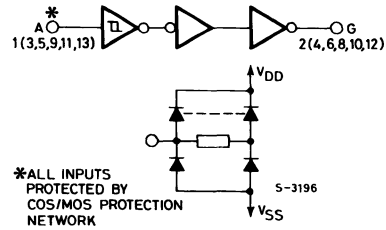
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAM




## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 1 | | 0.02 | 1 | | 30 | μA |
| | | | 0/10 | | | 10 | | 2 | | 0.02 | 2 | | 60 | |
| | | | 0/15 | | | 15 | | 4 | | 0.02 | 4 | | 120 | |
| | | | 0/20 | | | 20 | | 20 | | 0.04 | 20 | | 600 | |
| | | HCF Types | 0/ 5 | | | 5 | | 4 | | 0.02 | 4 | | 30 | |
| | | | 0/10 | | | 10 | | 8 | | 0.02 | 8 | | 60 | |
| | | | 0/15 | | | 15 | | 16 | | 0.02 | 16 | | 120 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/10 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_P$ | Positive Trigger Threshold Voltage | | | | | 5 | 2.2 | 3.6 | 2.2 | 2.9 | 3.6 | 2.2 | 3.6 | V |
| | | | | | | 10 | 4.6 | 7.1 | 4.6 | 5.9 | 7.1 | 4.6 | 7.1 | |
| | | | | | | 15 | 6.8 | 10.8 | 6.8 | 8.8 | 10.8 | 6.8 | 10.8 | |
| $V_N$ | Negative Trigger Threshold Voltage | | | | | 5 | 0.9 | 2.8 | 0.9 | 1.9 | 2.8 | 0.9 | 2.8 | V |
| | | | | | | 10 | 2.5 | 5.2 | 2.5 | 3.9 | 5.2 | 2.5 | 5.2 | |
| | | | | | | 15 | 4 | 7.4 | 4 | 5.8 | 7.4 | 4 | 7.4 | |
| $V_H$ | Hysteresis Voltage | | | | | 5 | 0.3 | 1.6 | 0.3 | 0.9 | 1.6 | 0.3 | 1.6 | V |
| | | | | | | 10 | 1.2 | 3.4 | 1.2 | 2.3 | 3.4 | 1.2 | 3.4 | |
| | | | | | | 15 | 1.6 | 5 | 1.6 | 3.5 | 5 | 1.6 | | |

* $T_{Low}$= – 55°C for **HCC** device : – 40°C for **HCF** device
* $T_{High}$= + 125°C for **HCC** device : + 85°C for **HCF** device.

## STATIC ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | – 2 | | – 1.6 | – 3.2 | | – 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | – 0.64 | | – 0.51 | – 1 | | – 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | – 1.6 | | – 1.3 | – 2.6 | | – 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | – 4.2 | | – 3.4 | – 6.8 | | – 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | – 1.53 | | – 1.36 | – 3.2 | | – 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | – 0.52 | | – 0.44 | – 1 | | – 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | – 1.3 | | – 1.1 | – 2.6 | | – 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | – 3.6 | | – 3.0 | – 6.8 | | – 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.6 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.9 | | |
| $I_{IH}$, $I_{IL}$** | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | p |

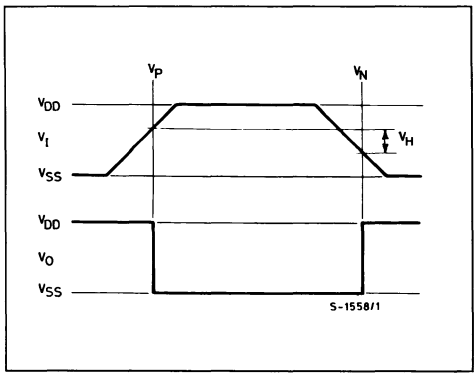
* $T_{Low}$= – 55°C for **HCC** device · – 40°C for **HCF** device.
* $T_{High}$= + 125°C for **HCC** device : + 85°C for **HCF** device.

## DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall time = 20ns)

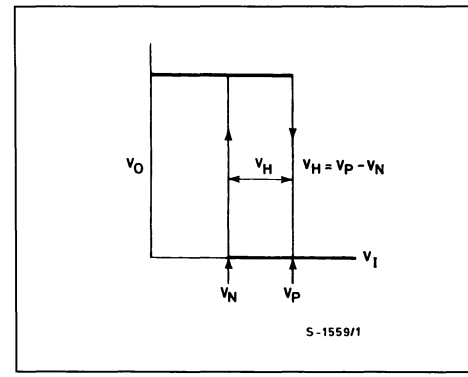
| Symbol | Parameter | Test Conditions | $V_{DD}$ (V) | Value Min. | Value Typ. | Value Max. | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time | | 5 | | 140 | 280 | ns |
| | | | 10 | | 70 | 140 | |
| | | | 15 | | 60 | 120 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

## HYSTERESIS DEFINITION, CHARACTERISTICS AND TEST SETUP

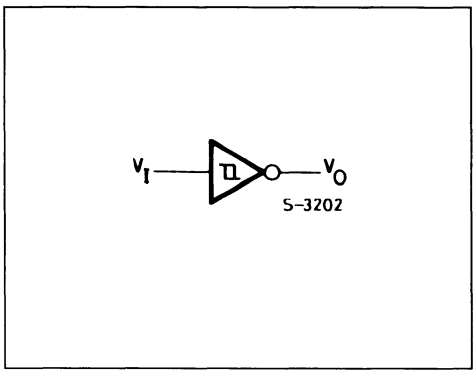
(a) Definition of $V_P$, $V_N$ and $V_H$.



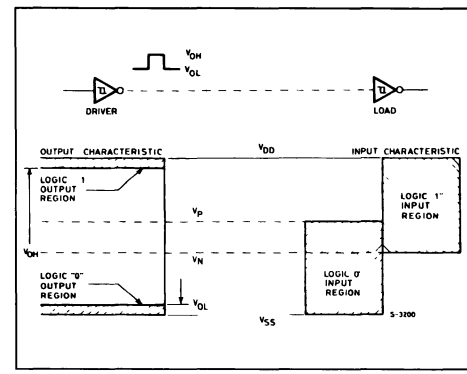

(b) Transfer Characteristic of 1 of 6 gates.



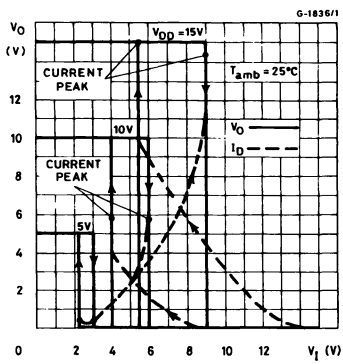

(c) Test Setup.

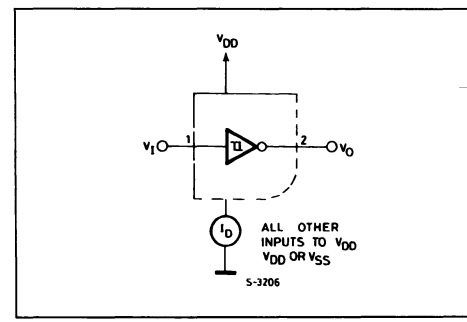



Input and Output Characteristics.



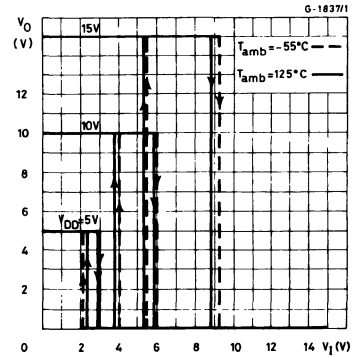

Typical Current Voltage Transfer Characteristics, and Test Circuit.

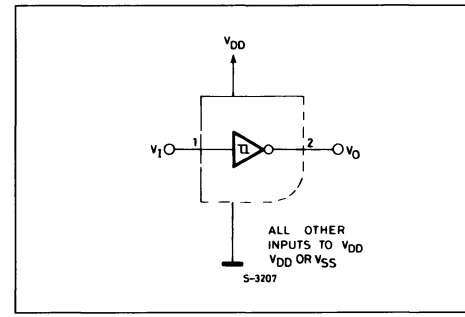


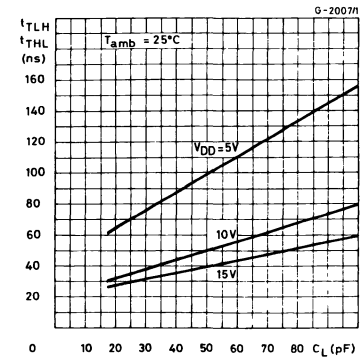
## HYSTERESIS DEFINITION, CHARACTERISTICS AND TEST SETUP

Typical Voltage Transfer Characteristics vs. Temperature, and Test Circuit.

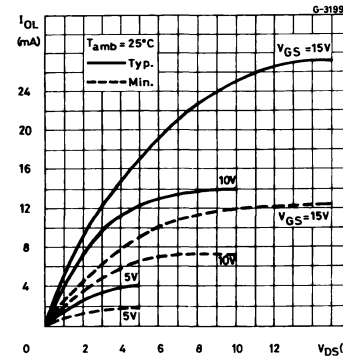


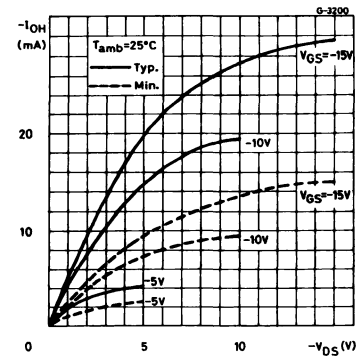

Typical Transition Time vs. Load Capacitance.



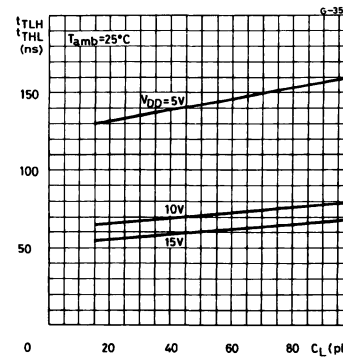

Output Low (sink) Current Characteristics.



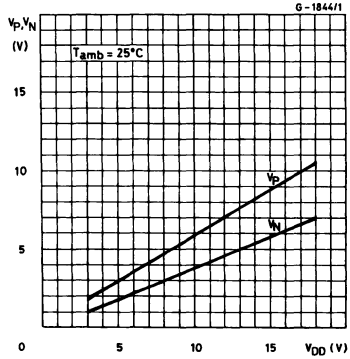

Output High (source) Current Characteristics.



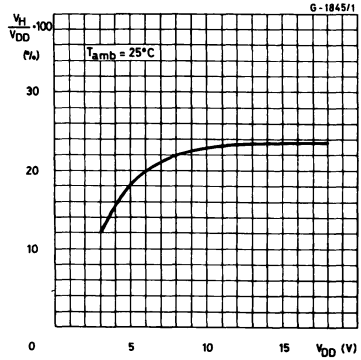

Typical Propagation Delay Time vs. Load Capacitance.



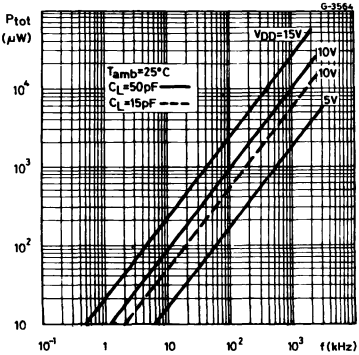
Typical Trigger Threshold Voltage vs. Supply Voltage .



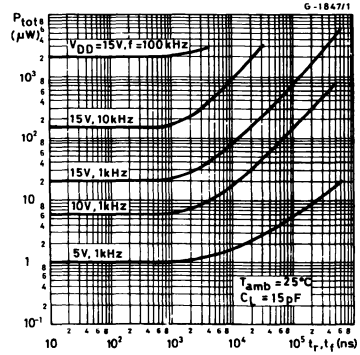

Typical per Cent Hysteresis vs. Supply Voltage.




Typical Power Dissipation per Trigger vs. Input Frequency.

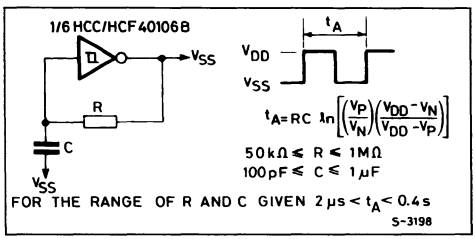



Typical Power Dissipation per Trigger vs. Input Frequency.

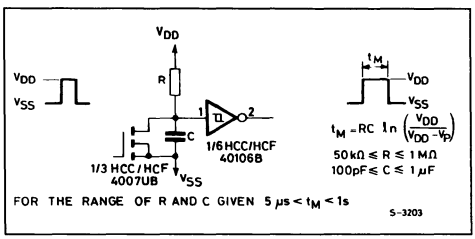



## TYPICAL APPLICATIONS

ASTABLE MULTIVIBRATOR.

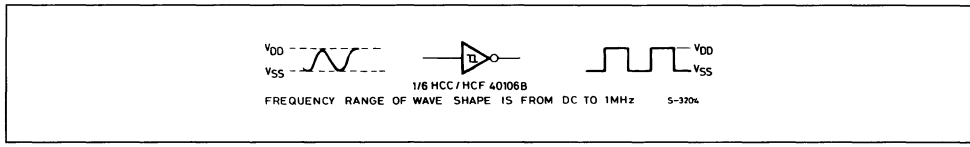



MONOSTABLE MULTIVIBRATOR.



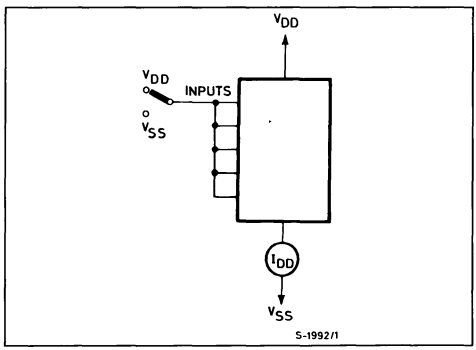
## TYPICAL APPLICATIONS (continued)

WAVE SHAPER.

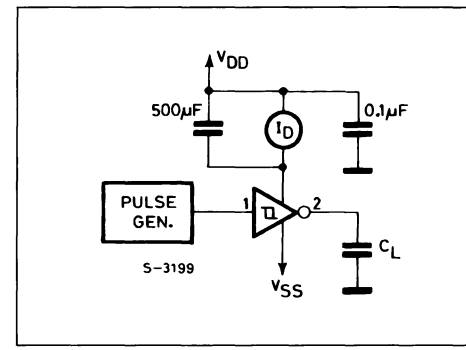



## TEST CIRCUITS

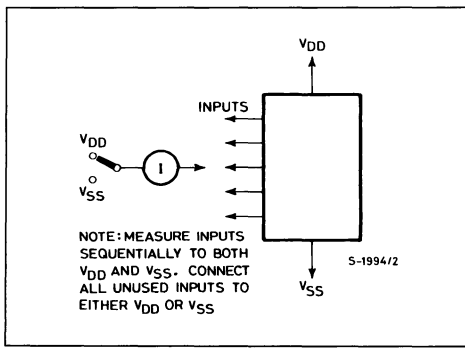
Quiescent Device Current.




Dynamic Power Dissipation.




Input Current .

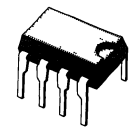


SGS-THOMSON MICROELECTRONICS

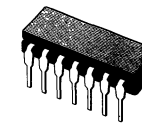
# HCC/HCF40107B

## DUAL 2-INPUT NAND BUFFER/DRIVER

- 32 TIMES STANDARD B-SERIES OUTPUT CURRENT DRIVE SINKING CAPABILITY – 136mA TYP. @ $V_{DD}$ = 10V, $V_{DS}$ = 1V
- QUIESCENT CURRENT SPECIFIED AT 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

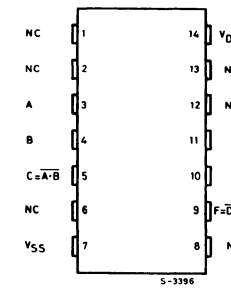
**M1**
(Micro Package)

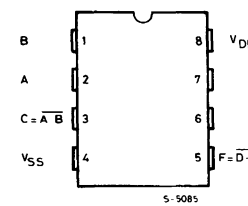
**C1**
(Plastic Chip Carrier)

**ORDER CODES**

HCC40107BF HCF40107BM1
HCF40107BEY HCF40107BC1

**PIN CONNECTIONS**



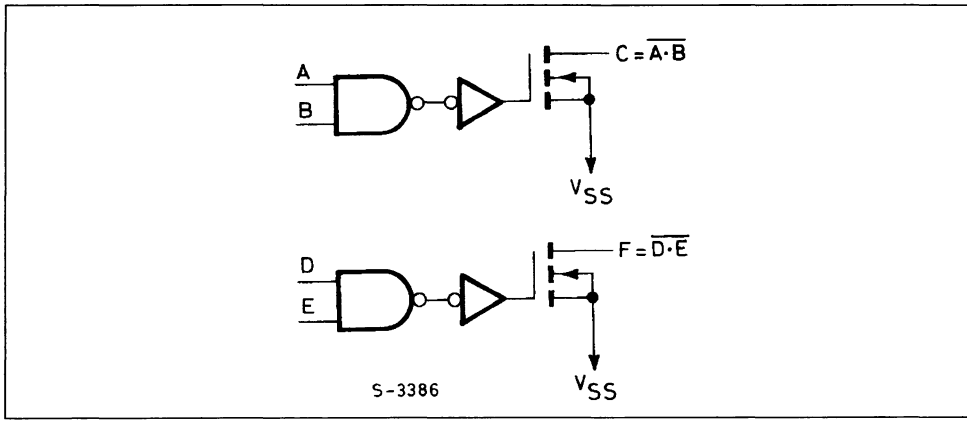




### DESCRIPTION

The **HCC40107B** (extended temperature range) and **HCF40107B** (intermediate temperature range) are monolithic integrated circuits, available in 14-lead dual in-line ceramic package 8-lead minidip plastic package and 8-lead plastic micropackage.

The **HCC/HCF40107B** is a dual 2-input NAND buffer/driver containing two independent 2-input NAND buffers with open-drain single n-channel transistor outputs. This device features a wired-OR capability and high output sink current capability (136mA typ. at $V_{DD}$ = 10V, $V_{DS}$ = 1V).

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** types<br>**HCF** types | − 0.5 to + 20<br>− 0.5 to + 18 | V |
| $V_I$ | Input Voltage | − 0.5 to VDD + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = full package-temperature Range | 200<br><br>100 | mW |
| $T_{op}$ | Operating Temperature : **HCC** types<br>**HCF** types | − 55 to + 125<br>− 40 to + 85 | °C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

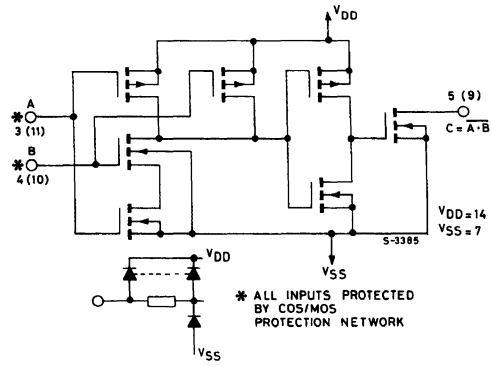
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltages values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## SCHEMATIC DIAGRAM AND TRUTH TABLE




| A | B | C | |
|---|---|---|---|
| 0 | 0 | 1* | Z# |
| 1 | 0 | 1* | Z# |
| 0 | 1 | 1* | Z# |
| 1 | 1 | 0 | |

* Requires external and pull-up resistor ($R_L$) to $V_{DD}$.
\# Without pull-up resistor (3-state).

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 1 | | 0.02 | 1 | | 30 | μA |
| | | | 0/10 | | | 10 | | 2 | | 0.02 | 2 | | 60 | |
| | | | 0/15 | | | 15 | | 4 | | 0.02 | 4 | | 120 | |
| | | | 0/20 | | | 20 | | 20 | | 0.04 | 20 | | 600 | |
| | | HCF Types | 0/ 5 | | | 5 | | 4 | | 0.02 | 4 | | 30 | |
| | | | 0/10 | | | 10 | | 8 | | 0.02 | 8 | | 60 | |
| | | | 0/15 | | | 15 | | 16 | | 0.02 | 16 | | 120 | |
| $V_{IH}$** | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$** | Input Low Voltage | | | 4.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |

* $T_{Low}$ = − 55°C for HCC device ; − 40°C for HCF device.
* $T_{High}$ = + 125°C for HCC device ; + 85°C for HCF device.
The Noise Margin, full package temperature range, $R_L$ to $V_{DD}$ = 10kΩ · 1V min with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2.5V min with VDD = 15V.
** Measured with external pull-up resistor, $R_L$ = 10kΩ to $V_{DD}$.
*** Forced output disabled.

## STATIC ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_{OL}$ | Output Sink Current | HCC Types | 5 | 0.4 | | 5 | 21 | | 16 | 32 | | 12 | | mA |
| | | | 5 | 1 | | 5 | 44 | | 30 | 68 | | 25 | | |
| | | | 10 | 0.5 | | 10 | 49 | | 37 | 74 | | 28 | | |
| | | | 10 | 1 | | 10 | 89 | | 68 | 136 | | 51 | | |
| | | | 15 | 0.5 | | 15 | 66 | | 50 | 100 | | 38 | | |
| | | HCF Types | 5 | 0.4 | | 5 | 17 | | 13.6 | 32 | | 12 | | |
| | | | 5 | 1 | | 5 | 35.7 | | 25.5 | 68 | | 22 | | |
| | | | 10 | 0.5 | | 10 | 39.1 | | 31.4 | 74 | | 27 | | |
| | | | 10 | 1 | | 10 | 72.2 | | 57.8 | 136 | | 51 | | |
| | | | 15 | 0.5 | | 15 | 53.5 | | 42.5 | 100 | | 37 | | |
| $I_{OH}$ | Output Drive Current | | No Internal Pull-up Device | | | | | | | | | | | mA |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $I_{OH}$,$I_{OL}$ *** | 3-State Output Leakage Current | HCC Types | 0/18 | 18 | | 18 | | 2 | | $\pm 10^{-4}$ | 2 | | 20 | μA |
| | | HCF Types | 0/15 | 15 | | 15 | | 2 | | $\pm 10^{-4}$ | 2 | | 20 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |
| $C_O$ | Output Capacitance | | | Any Output | | | | | | 30 | | | | pF |

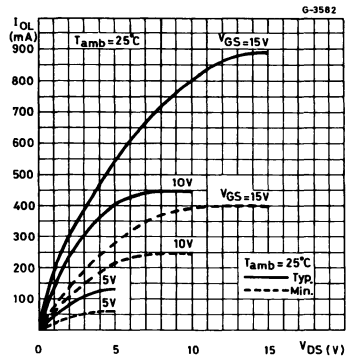
* $T_{Low}$ = – 55°C for HCC device ; – 40°C for HCF device.
* $T_{High}$ = + 125°C for HCC device ; + 85°C for HCF device
The Noise Margin, full package temperature range, $R_L$ to $V_{DD}$ = 10kΩ 1V min with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2.5V min with VDD = 15V
** Measured with external pull-up resistor, $R_L$ = 10kΩ to $V_{DD}$
*** Forced output disabled

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall time = 20ns)

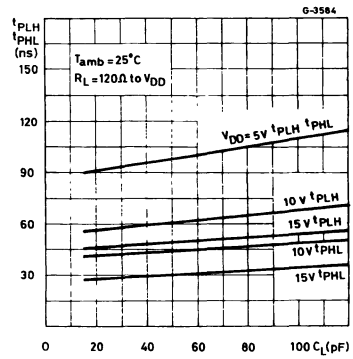
| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time High to Low | $R_L$* = 120Ω | 5 | | 100 | 200 | ns |
| | | | 10 | | 45 | 90 | |
| | | | 15 | | 30 | 60 | |
| | Low to High | $R_L$* = 120Ω | 5 | | 100 | 200 | ns |
| | | | 10 | | 60 | 120 | |
| | | | 15 | | 50 | 100 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time High to Low | $R_L$* = 120Ω | 5 | | 50 | 100 | ns |
| | | | 10 | | 20 | 40 | |
| | | | 15 | | 10 | 20 | |
| | Low to High | $R_L$* = 120Ω | 5 | | 50 | 100 | ns |
| | | | 10 | | 35 | 70 | |
| | | | 15 | | 25 | 50 | |

* $R_L$ is external pull-up resistor to $V_{DD}$.

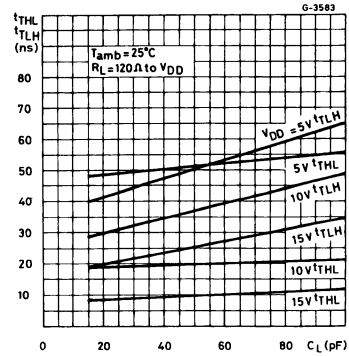
Output Low (sink) Current Characteristics.



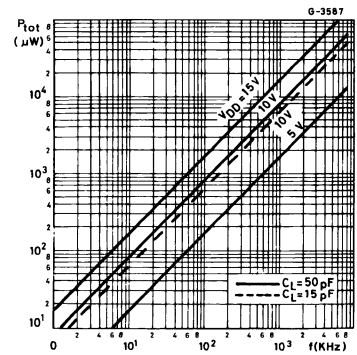

Typical Propagation Delay Time vs. Load Capacitance.



Typical Transition Time vs. Load Capacitance.



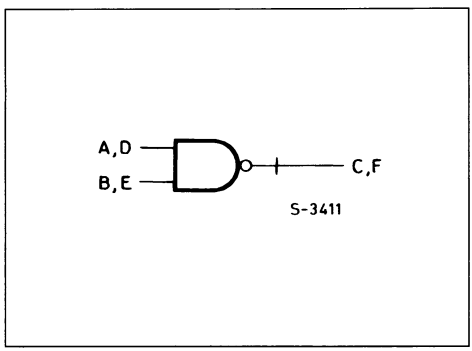

Typical Dynamic Power Dissipation vs. Input Frequency.



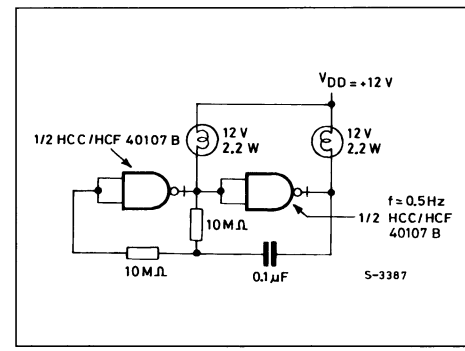

## TYPICAL APPLICATIONS

The bar on the output line of this logic diagram indicates that the output is open drain as is shown in the previous schematic diagram and truth table.

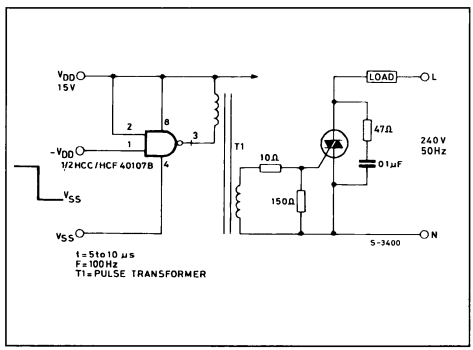
Logic Diagram of The **HCC/HCF40107B** nand Buffer.



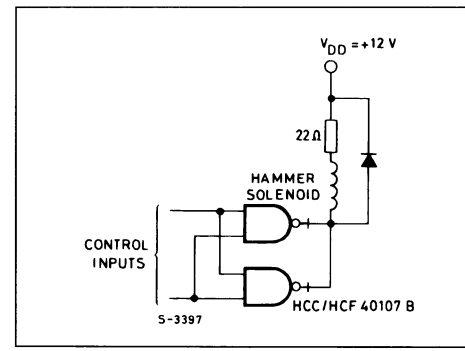

A 2.2-watt Incandescent Lamp-driver Circuit.




Interface of **40107B** with Triac, with COS/MOS Component and Triac isolated.

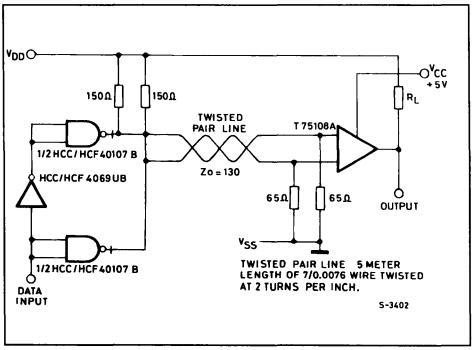



Solenoid Driver Circuit.

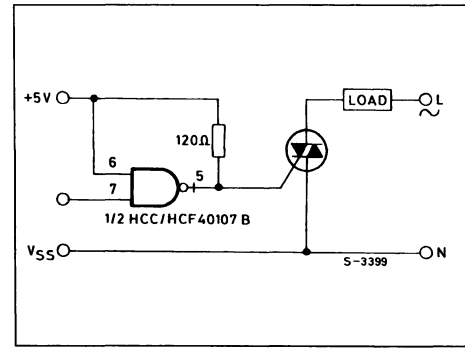


## TYPICAL APPLICATIONS (continued)

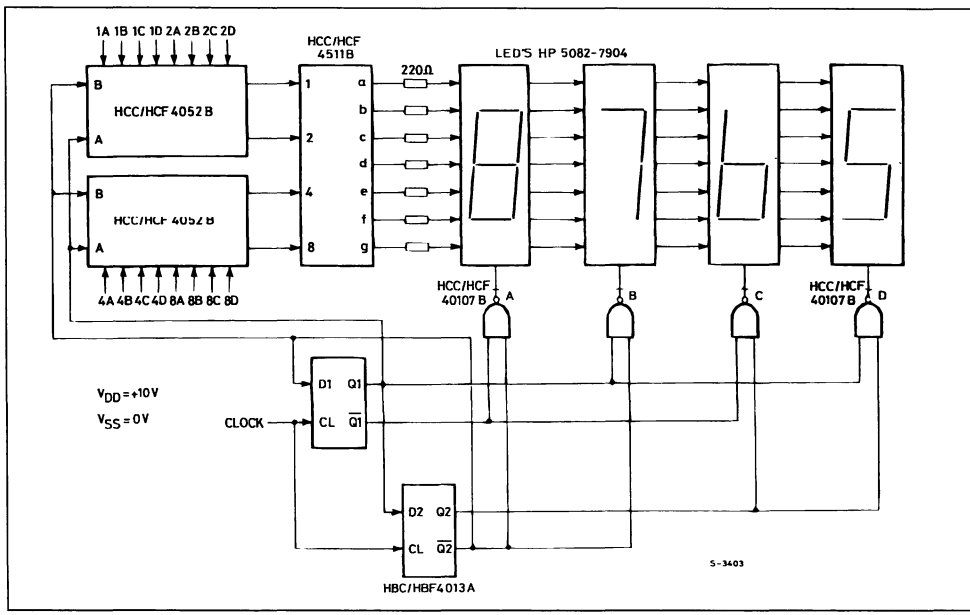
Line-driver Circuit.




Direct Dc Driver Interface of **40107B** with a Triac.

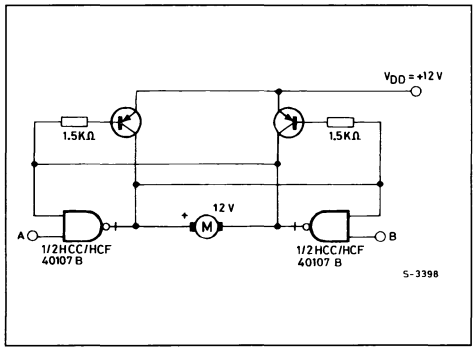



Multiplexed Led Circuit.



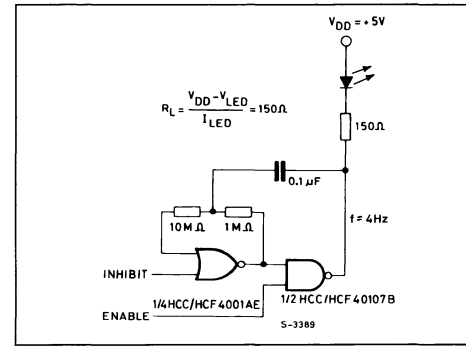
## TYPICAL APPLICATIONS (continued)

Motor-controller Circuit.




| A | B | Motor Function |
|---|---|---|
| O | O | OFF |
| I | O | COUNTER CLOCKWISE |
| I | I | AS PREVIOUS STATE |
| O | I | CLOCKWISE |
| I | I | AS PREVIOUS STATE |

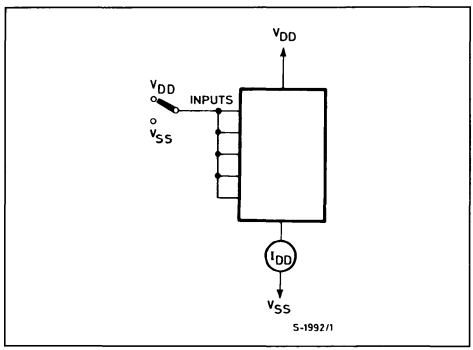
Led Driver Circuit.



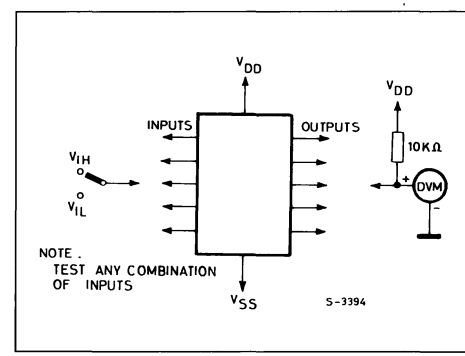

| INHIBIT | ENABLE | OUTPUT |
|---|---|---|
| 0 | 0 | OFF |
| 1 | 0 | OFF |
| 0 | 1 | OFF |
| 0 | 1 | ON |

## TEST CIRCUITS

Quiescent Device Current.

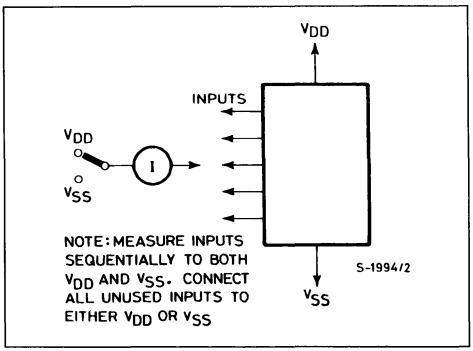



Input Voltage.

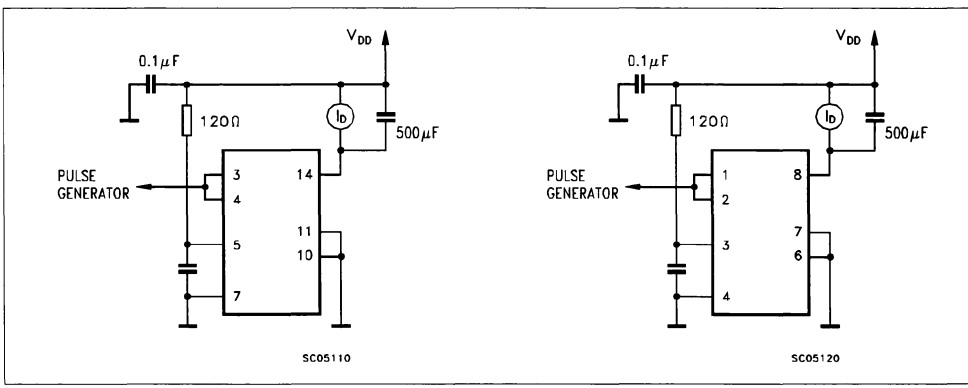


**TEST CIRCUITS** (continued)

Dynamic Power Dissipation.




Dynamic Power Dissipation.

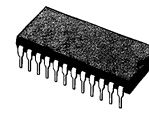


# 4 x 4 MULTIPORT REGISTER

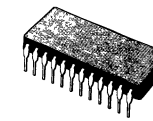
- FOUR 4-BIT REGISTERS
- ONE INPUT AND TWO OUTPUT BUSES
- UNLIMITED EXPANSION IN BIT AND WORD DIRECTION
- DATA LINES HAVE LATCHED INPUTS
- 3-STATE OUTPUTS
- SEPARATE CONTROL OF EACH BUS, ALLOWING SIMULTANEOUS INDEPENDET READING AND ANY OF FOUR REGISTERS ON BUS A AND BUS B AND INDEPENDENT WRITING INTO ANY ANY OF THE FOUR REGISTERS
- 40108B IS PIN COMPATIBLE WITH INDUSTRY TYPE MC14580
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED AT 20V FOR HCC DEVICE
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25oC FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No 13a, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"

## DESCRIPTION

The HCC40108B (extended temperature range) and HCF40108B (intermediate temperature range) are monolithic integrated circuits, available in 24 lead dual in line plastic or ceramic packageand plastic micropackage. The HCC/HCF40108B is a 4 X 4 multiport register containing four 4-bit register, write address decoder, two separate read address decoders, and two 3-state output buses. When the ENABLE input is low, the corresponding output bus is switched, independently of the clock, to a high impedance state. The high impedance third state provides the outputs with the capability of being connected to the bus lines in a bus organized system without the need for interface or pull-up components. When the WRITE ENABLE input is high, all data input lines are latched on the positive transition of the CLOCK and the data is entered into the word selected by the write address lines. When WRITE ENABLE is low, the CLOCK is inhibited and no new data is netered. In either case, the contents of any word may be accessed via the read address lines independent of the state of the CLOCK input.



**EY**
(Plastic Package)



**F**
(Ceramic Package)

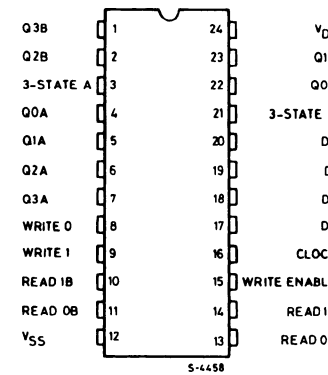
**M1**
(Micro Package)

**C1**
(Chip Carrier)

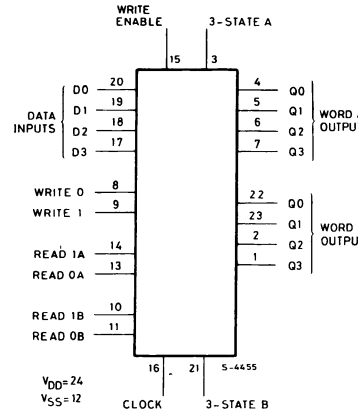
**ORDER CODES :**

| | |
|---|---|
| HCC40108BF | HCF40108BM1 |
| HCF40108BEY | HCF40108BC1 |

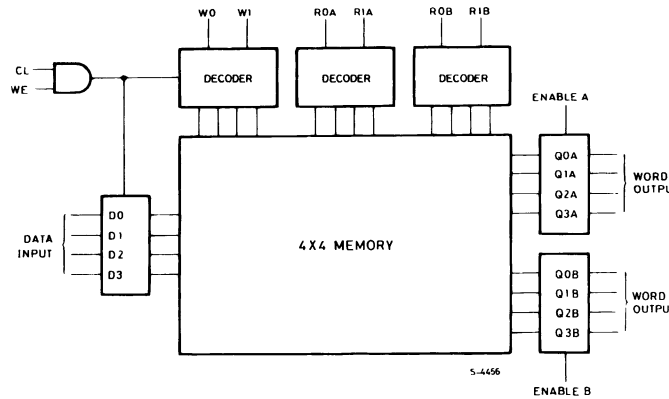
**PIN CONNECTIONS**



## FUNCTIONAL DIAGRAM




## LOGIC DIAGRAM



## ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ * | Supply Voltage: **HCC** Types<br>**HCF** Types | -0.5 to +20<br>-0.5 to +18 | V<br>V |
| $V_I$ | Input Voltage | -0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for Top = Full Package Temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for external periods may affect device reliability

* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage: **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |

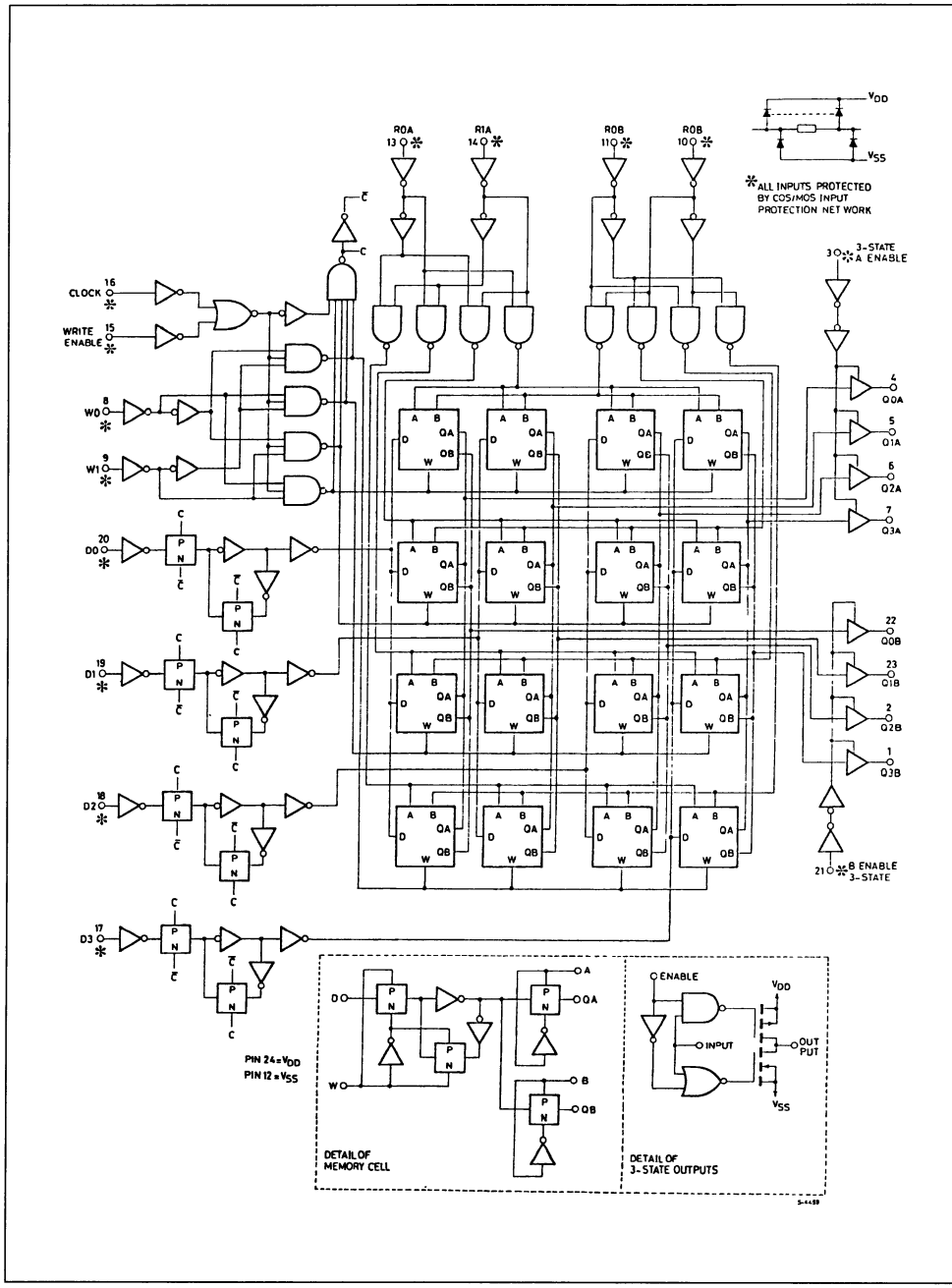
## TRUTH TABLE

| CLOCK | Write Enable | Write 1 | Write 2 | Read 1A | Read 0A | Read 1B | Read 0B | En-able A | En-able B | $D_n$ | $Q_{nA}$ | $Q_{nB}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ⎍ | 1 | S1 | S2 | S1 | S2 | S1 | S2 | 1 | 1 | 1 | 1 | 1 |
| ⎍ | 1 | S1 | S2 | S1 | S2 | S1 | S2 | 1 | 0 | 0 | 0 | 0 |
| X | X | X | X | X | X | X | X | 0 | X | Z | Z | Z |
| ⎍ | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | $D_n$ to word 0 | Word 1 Out | Word 2 Out |
| ⎍ | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | Word 0 not altered | Word 1 Out | Word 2 Out |
| X | X | X | X | 1 | 0 | 0 | 1 | 1 | X | X | Word 2 Out | Word 1 Out |
| ⎎ | X | X | X | X | X | X | X | 1 | 1 | X | NC | NC |

1 = HIGH LEVEL, 0 = LOW LEVEL, X = DON'T CARE, Z = HIGH IMPEDANCE

S1 and S2 refer to input strates of either 1 or 0

## SCHEMATIC DIAGRAM



## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditios | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{LOW}$ * Min. | $T_{LOW}$ * Max. | 25 °C Min. | 25 °C Typ. | 25 °C Max. | $T_{HIGH}$ * Min. | $T_{HIGH}$ * Max. | |
| $I_L$ | Quiescent Current | HCC Types | 0/5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/5 | 2.5 | | 5 | -2 | | -1.6 | -3.2 | | -1.15 | | mA |
| | | | 0/5 | 4.6 | | 5 | -0.64 | | -0.51 | -1 | | -0.36 | | |
| | | | 0/10 | 9.5 | | 10 | -1.6 | | -1.3 | -2.6 | | -0.9 | | |
| | | | 0/15 | 13.5 | | 15 | -4.2 | | -3.4 | -6.8 | | -2.4 | | |
| | | HCF Types | 0/5 | 2.5 | | 5 | -1.53 | | -1.36 | -3.2 | | -1.1 | | |
| | | | 0/5 | 4.6 | | 5 | -0.52 | | -0.44 | -1 | | -0.36 | | |
| | | | 0/10 | 9.5 | | 10 | -1.3 | | -1 1 | -2.6 | | -0.9 | | |
| | | | 0/15 | 13.5 | | 15 | -3.6 | | -3.0 | -6.8 | | -2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1 5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ±0.1 | | $±10^{-5}$ | ±0.1 | | ±1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ±0.3 | | $±10^{-5}$ | ±0.3 | | ±1 | |
| $I_{OH}$, $I_{OL}$ ** | 3-Sate Output Leakage Current | HCC Types | 0/18 | 0/18 | | 18 | | ±0.4 | | $±10^{-4}$ | ±0.4 | | ±12 | μA |
| | | HCF Types | 0/15 | 0/15 | | 15 | | ±1.0 | | $±10^{-4}$ | ±1.0 | | ±7.5 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{LOW}$ = -55 °C for **HCC** device: -40 °C for **HCF** device.

* $T_{HIGH}$ = +125 °C for **HCC** device: +85 °C for **HCF** device

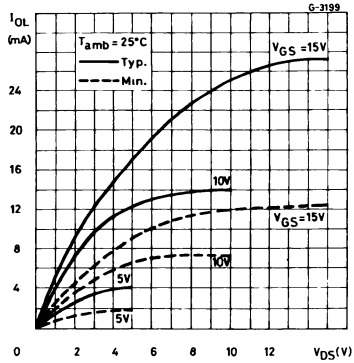
The Noise Margin for both "1" and "0" level is: 1V min. with $V_{DD}$ = 5 V, 2 V min. with $V_{DD}$ = 10 V, 2.5 V min. with $V_{DD}$ = 15 V

** Forced output disable

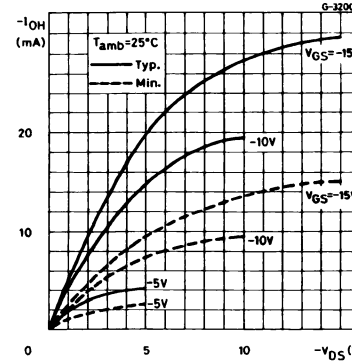
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 KΩ, typical temperature coefficent for all $V_{DD}$ values is 03 %/°C, all input rise and fall times= 20 ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time Clock or Write Enable to Q | | 5 | | 360 | 720 | ns |
| | | | 10 | | 140 | 280 | |
| | | | 15 | | 100 | 200 | |
| | Propagation Delay Time Read or Write Address to Q | | 5 | | 300 | 600 | |
| | | | 10 | | 120 | 240 | |
| | | | 15 | | 85 | 170 | |
| $t_{PZH}$ $t_{PHZ}$ | 3-State Disable Delay Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_{PZL}$ $t_{PLZ}$ | 3-State Display Delay Time | | 5 | | 130 | 260 | ns |
| | | | 10 | | 60 | 120 | |
| | | | 15 | | 50 | 100 | |
| $t_{TLH}$ $t_{THL}$ | Output Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_{setup}$ | Setup Time Data to Clock $t_{s(D)}$ | | 5 | 0 | -95 | | ns |
| | | | 10 | 0 | -35 | | |
| | | | 15 | 0 | -20 | | |
| | Setup Time Write Enable to Clock $t_{s(WE)}$ | | 5 | 250 | 125 | | |
| | | | 10 | 100 | 50 | | |
| | | | 15 | 70 | 35 | | |
| | Setup Time Write Address to Clock $t_{s(WA)}$ | | 5 | 250 | 125 | | |
| | | | 10 | 100 | 50 | | |
| | | | 15 | 70 | 35 | | |
| $t_r$, $t_s$ | Clock Rise and Fall Time | | 5 | | | 15 | µs |
| | | | 10 | | | 5 | |
| | | | 15 | | | 5 | |
| $t_{hold}$ | Hold Time Data to Clock $t_{s(D)}$ | | 5 | 220 | 110 | | ns |
| | | | 10 | 100 | 50 | | |
| | | | 15 | 80 | 40 | | |
| | Hold Time Write Enable to Clock $t_{s(WE)}$ | | 5 | 270 | 135 | | |
| | | | 10 | 130 | 65 | | |
| | | | 15 | 80 | 40 | | |
| | Hold Time Write Address to Clock $t_{s(WA)}$ | | 5 | 330 | 165 | | |
| | | | 10 | 140 | 70 | | |
| | | | 15 | 90 | 45 | | |
| $t_W$ | Clock Pulse Width Clock or Write Enable $t_{W(CL)}$ | | 5 | 350 | 175 | | ns |
| | | | 10 | 130 | 65 | | |
| | | | 15 | 90 | 45 | | |
| | Clock Pulse Width Write Address $t_{W(WA)}$ | | 5 | 300 | 150 | | |
| | | | 10 | 150 | 75 | | |
| | | | 15 | 90 | 45 | | |
| $f_{CL}$ | Maximum Clock Input Frequency | | 5 | 1.5 | 3 | | MHz |
| | | | 10 | 3.5 | 7 | | |
| | | | 15 | 4.5 | 9 | | |

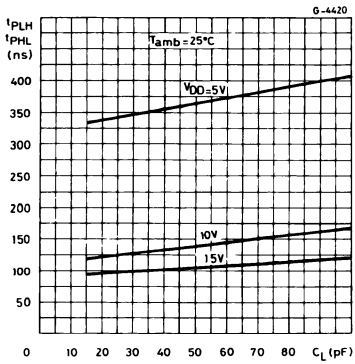
Output Low (sink) Current Characteristics



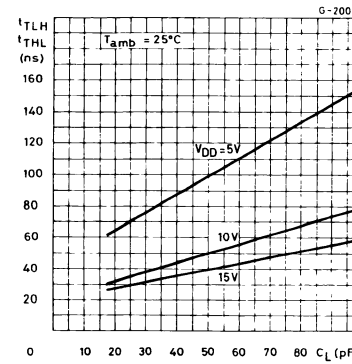

Output High (source) Current Characteristics



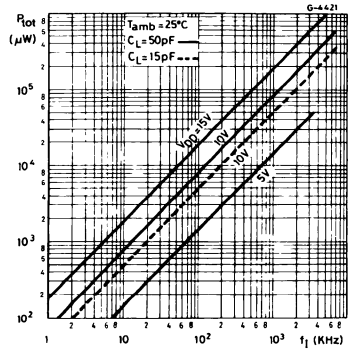

Typical Propagation Delay Time vs Load Capacitance (CL or WE to Q)



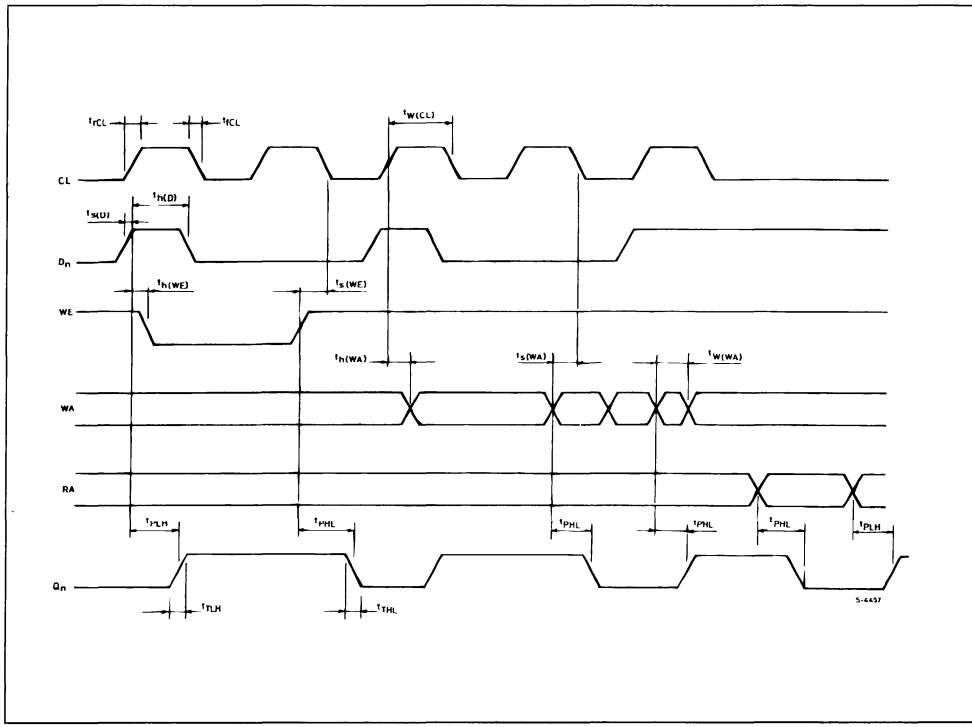

Typical Transition Time vs Load Capacitance




Typical Dynamic Power Dissipation vs Input Frequency

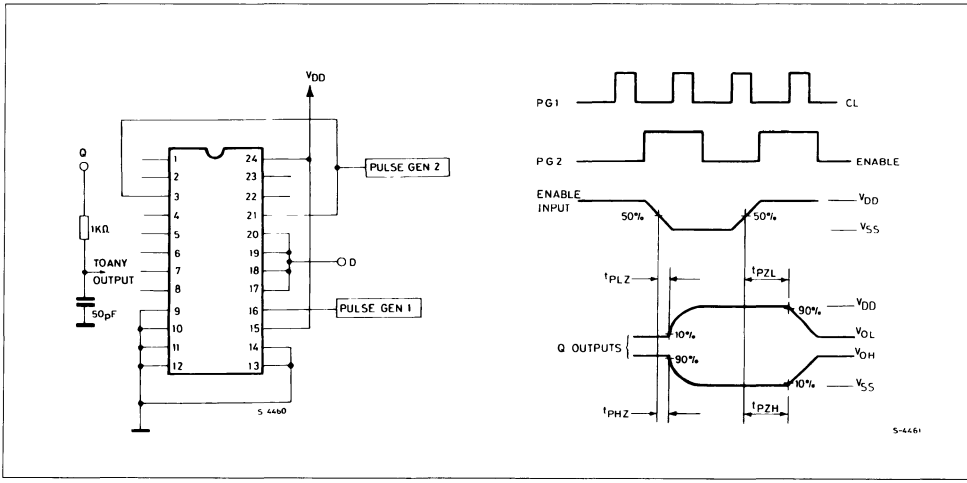


## TIMING DIAGRAM

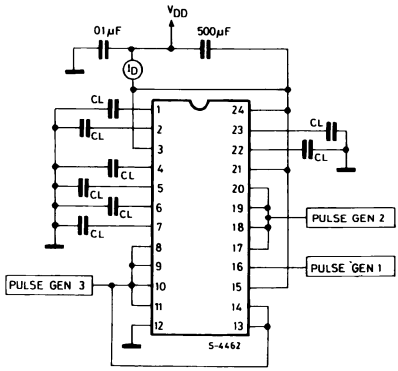


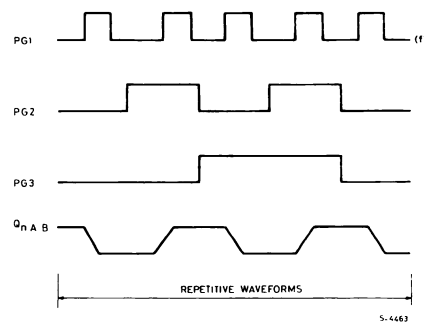

## TEST CIRCUITS

Output Enable Delay Times and Waveforms

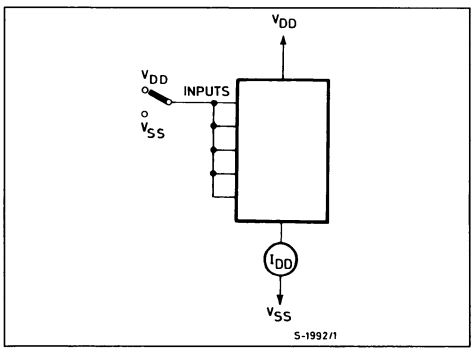


## Power Dissipation and Waveforms

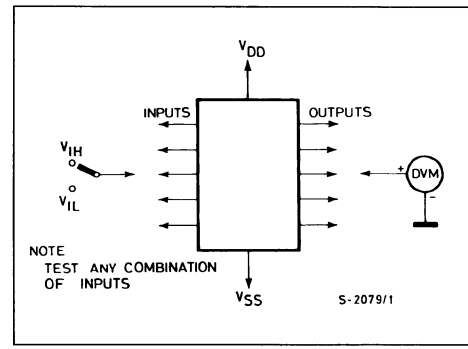


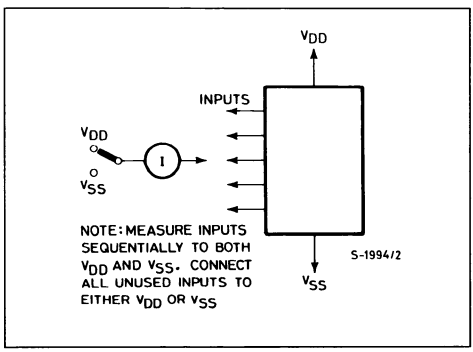

## Quiescent Device Current.




## Noise Immunity.




## Input Leakage Current.



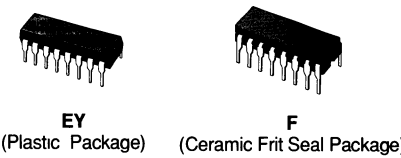
# HCC/HCF40109B

## QUAD LOW-TO-HIGH VOLTAGE LEVEL SHIFTER

- INDEPENDENCE OF POWER SUPPLY SEQUENCE CONSIDERATIONS – $V_{CC}$ CAN EXCEED $V_{DD}$, INPUT SIGNALS CAN EXCEED BOTH $V_{CC}$ AND $V_{DD}$
- UP AND DOWN LEVEL-SHIFTING CAPABILITY
- THREE-STATE OUTPUTS WITH SEPARATE ENABLE CONTROLS
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED AT 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

### DESCRIPTION

The **HCC40109B** (extended temperature range) and **HCF40109B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and plastic micropackage. The **HCC/HCF40109B** contains four low-to-high-voltage level-shifting circuits. Each circuit will shift a low-voltage digital-logic input signal (A, B, C, D) with logical 1 = $V_{CC}$ and logical 0 = $V_{SS}$ to a higher-voltage output signal (E, F, G, H) with logical 1 = $V_{DD}$ and logical 0 = $V_{SS}$. The **HCC/HCF40109B**, unlike other low-to-high level-shifting circuits, does not require the presence of the high-voltage supply ($V_{DD}$) before the application of either the low-voltage supply ($V_{CC}$) or the input signals. There are no restrictions on the sequence of application of $V_{DD}$, $V_{CC}$, or the input signals. In addition, there are no restrictions on the relative magnitudes od the supply voltages or input signals within the device maximum ratings ; $V_{CC}$ may exceed $V_{DD}$, and input signals may exceed $V_{CC}$, and $V_{DD}$. When operated in the mode $V_{CC}$ $V_{DD}$, the **HCC/HCF40109B**, will operate as a high-to-low level-shifter. The **HCC/HCF 40109B** also features individual three-state output capability. A low level on any of the separately enabled three-state output controls produces a high-impedance state in the corresponding output.



**EY**
(Plastic Package)

**F**
(Ceramic Frit Seal Package)

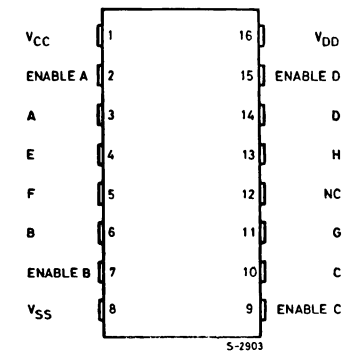
**C1**
(Micro package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

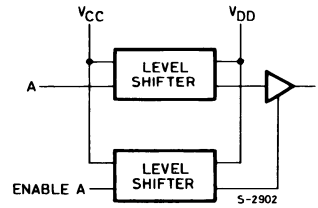
HCC40109BF HCF40109BM1
HCF40109BEY HCF40109BC1

**PIN CONNECTIONS**



## FUNCTIONAL DIAGRAM

1 of 4 units




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

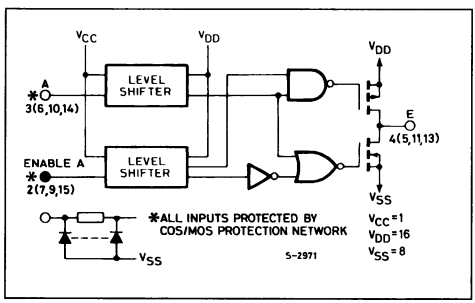
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage are with respect to $V_{SS}$ (GND)

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAM




## TRUTH TABLE

| Mode | Inputs | | Outputs |
|---|---|---|---|
| | A, B, C, D | Enable A, B, C, D | E, F, G, H |
| Low to High Level Shift | 0 | 1 | 0 |
| | 1 | 1 | 1 |
| | X | 0 | Z |

LOGIC 0 = LOW ($V_{SS}$) X = Don't Care. Z = High Impedance.

LOGIC 1 = $V_{CC}$ at INPUTS and $V_{DD}$ at OUTPUTS.

**STATIC ELECTRICAL CHARACTERISTICS** (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions | | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{CC}$ (V) | $V_{DD}$ (V) | $T_{Low}$* Min | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | |
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | | 5 | | 1 | | 0.02 | 1 | | 30 | μA |
| | | | 0/10 | | | | 10 | | 2 | | 0.02 | 2 | | 60 | |
| | | | 0/15 | | | | 15 | | 4 | | 0.02 | 4 | | 120 | |
| | | | 0/20 | | | | 20 | | 20 | | 0.04 | 20 | | 600 | |
| | | HCF Types | 0/ 5 | | | | 5 | | 4 | | 0.02 | 4 | | 30 | |
| | | | 0/10 | | | | 10 | | 8 | | 0.02 | 8 | | 60 | |
| | | | 0/15 | | | | 15 | | 16 | | 0.02 | 16 | | 120 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 1/9 | < 1 | 5 | 10 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1.5/13.5 | < 1 | 10 | 15 | 7 | | 7 | | | 7 | | |
| $V_{IL}$ | Input Low Voltage | | | 1/9 | < 1 | 5 | 10 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 1.5/13.5 | < 1 | 10 | 15 | | 3 | | | 3 | | 3 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | | 18 | | ± 0.1 | | ± $10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | | 15 | | ± 0.3 | | ± $10^{-5}$ | ± 0.3 | | ± 1 | |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.
** Forced output disabled.

## STATIC ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | | Test Conditions | | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (V) | $V_{CC}$ (V) | $V_{DD}$ (V) | $T_{Low}$* Min. | $T_{Low}$* Max. | 25 °C Min. | 25 °C Typ. | 25 °C Max. | $T_{High}$* Min. | $T_{High}$* Max. | |
| $I_{OH}$, $I_{OL}$** | 3-State Output Leakage Current | HCC Types | 0/18 | 0/18 | | | 18 | | ± 0.4 | | $\pm 10^{-4}$ | ± 0.4 | | ± 12 | µA |
| | | HCF Types | 0/15 | 0/15 | | | 15 | | ± 1.0 | | $\pm 10^{-4}$ | ± 1.0 | | ± 7.5 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device . − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device ..+ 85°C for **HCF** device
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2 5V min. with $V_{DD}$ = 15V.
** Forced output disabled.

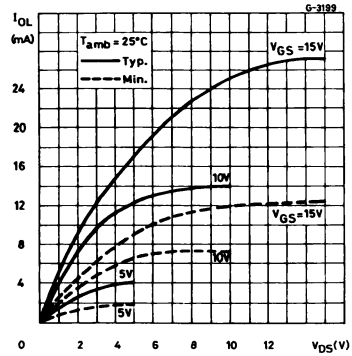
## DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall time = 20ns)

| Symbol | Parameter | Shifting Mode | Test Conditions $V_{CC}$ (V) | Test Conditions $V_{DD}$ (V) | Value Min. | Value Typ. | Value Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time (data input to output) High to Low Level | L - H | 5 | 10 | | 300 | 600 | ns |
| | | | 5 | 15 | | 220 | 440 | |
| | | | 10 | 15 | | 180 | 360 | |
| | | H - L | 10 | 5 | | 850 | 1600 | |
| | | | 15 | 5 | | 850 | 1600 | |
| | | | 15 | 10 | | 290 | 580 | |
| | Low to High Level | L - H | 5 | 10 | | 130 | 260 | ns |
| | | | 5 | 15 | | 120 | 240 | |
| | | | 10 | 15 | | 70 | 140 | |
| | | H - L | 10 | 5 | | 230 | 460 | |
| | | | 15 | 5 | | 230 | 460 | |
| | | | 15 | 10 | | 80 | 160 | |
| $t_{PHZ}$ | 3-State Disable Delay Time Output High to High Impedance | L - H | 5 | 10 | | 60 | 120 | ns |
| | | | 5 | 15 | | 50 | 100 | |
| | | | 10 | 15 | | 35 | 70 | |
| | | H - L | 10 | 5 | | 120 | 240 | |
| | | | 15 | 5 | | 120 | 240 | |
| | | | 15 | 10 | | 40 | 80 | |
| $t_{PZH}$ | High Impedance to Output High | L - H | 5 | 10 | | 320 | 640 | ns |
| | | | 5 | 15 | | 230 | 460 | |
| | | | 10 | 15 | | 180 | 360 | |
| | | H - L | 10 | 5 | | 800 | 1500 | |
| | | | 15 | 5 | | 800 | 1500 | |
| | | | 15 | 10 | | 280 | 560 | |
| $t_{PLZ}$ | Output Low to High Impedance | L - H | 5 | 10 | | 370 | 740 | ns |
| | | | 5 | 15 | | 300 | 600 | |
| | | | 10 | 15 | | 250 | 500 | |
| | | H - L | 10 | 5 | | 850 | 1600 | |
| | | | 15 | 5 | | 850 | 1600 | |
| | | | 15 | 10 | | 350 | 700 | |

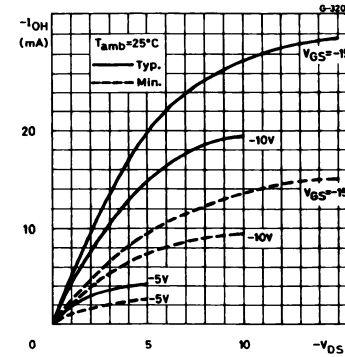
**DYNAMIC ELECTRICAL CHARACTERISTICS** (continued)

| Symbol | Parameter | Shifting Mode | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ (V) | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PZL}$ | High Impedance to Output Low | L - H | 5 | 10 | | 100 | 200 | ns |
| | | | 5 | 15 | | 80 | 160 | |
| | | | 10 | 15 | | 40 | 80 | |
| | | H - L | 10 | 5 | | 120 | 240 | |
| | | | 15 | 5 | | 120 | 240 | |
| | | | 15 | 10 | | 40 | 80 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | L - H | 5 | 10 | | 50 | 100 | ns |
| | | | 5 | 15 | | 40 | 80 | |
| | | | 10 | 15 | | 40 | 80 | |
| | | H - L | 10 | 5 | | 100 | 200 | |
| | | | 15 | 5 | | 100 | 200 | |
| | | | 15 | 10 | | 50 | 100 | |

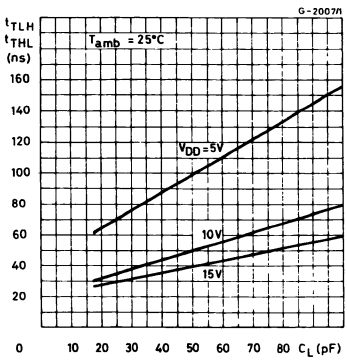
Output Low (sink) Current Characteristics.



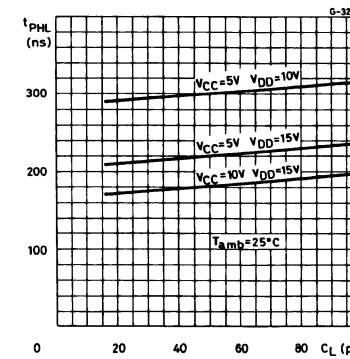

Output High (source) Current Characteristics.



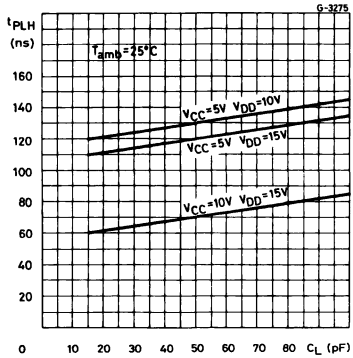

Typical Transition Timevs. Load Capacitance.



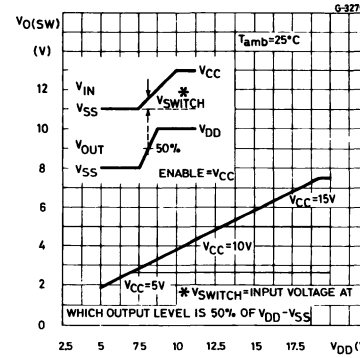

Typical High-to-low Propagation Delay Time vs. Load Capacitance.



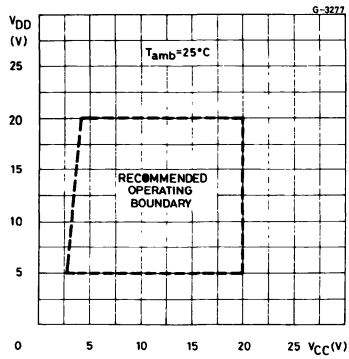
Typical Low-to-high Propagation Delay Time vs. Load Capacitance.



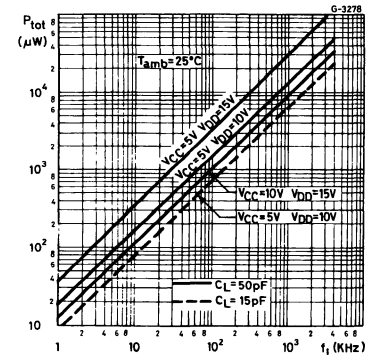

Typical Input Switching vs. High-level Supply Voltage.




High-level Supply Voltage vs. Low-level Supply Voltage.

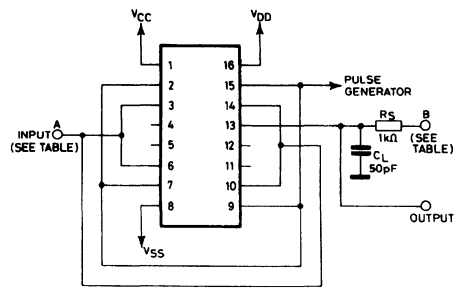


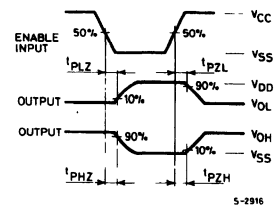

Typical Dynamic Power Dissipation vs. Input Frequency.




## TEST CIRCUITS

Output Enable Delay Times Test Circuit and Waveforms.

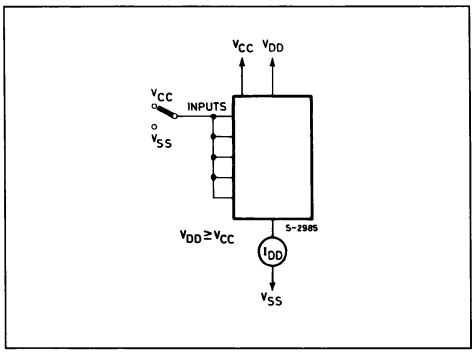


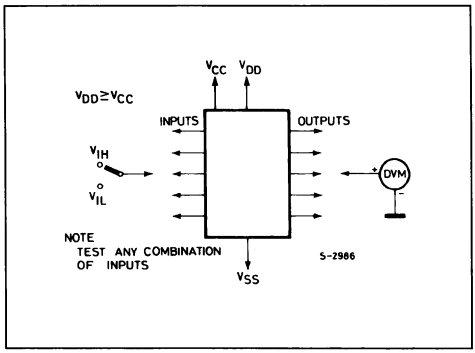

| CHAR. | TEST VOLTAGE | |
|---|---|---|
| | AT A | AT B |
| $t_{PHZ}$ | $V_{CC}$ | $V_{SS}$ |
| $t_{PLZ}$ | $V_{SS}$ | $V_{DD}$ |
| $t_{PZL}$ | $V_{SS}$ | $V_{DD}$ |
| $t_{PZH}$ | $V_{CC}$ | $V_{SS}$ |

**TEST CIRCUITS** (continued)

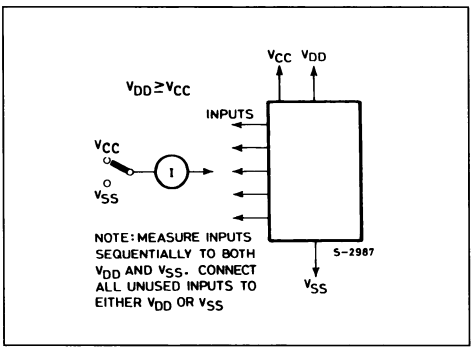
Quiescent Device Current.



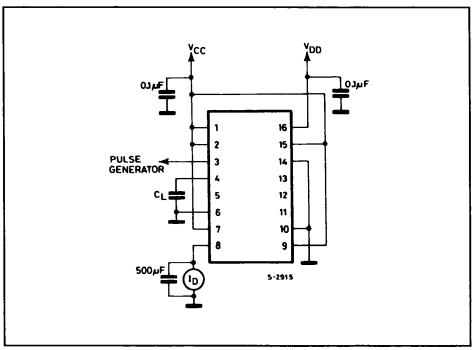

Input Voltage.




Input Leakage Current.




Dynamic Power Dissipation.

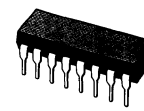


SGS-THOMSON MICROELECTRONICS

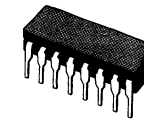
# HCC40110B
# HCF40110B

## DECADE UP-DOWN COUNTER/DECODER/LATCH/DRIVER

- SEPARATE CLOCK-UP AND CLOCK-DOWN LINES
- CAPABLE OF DRIVING COMMON CATHODE LEDS AND OTHER DISPLAYS DIRECTLY
- ALLOWS CASCADING WITHOUT ANY EXTERNAL CIRCUITRY
- MAXIMUM INPUT CURRENT OF 1 μA AT 18 V (full package-temperature range)
- QUIESCENT CURRENT AT 20 V FOR HCC DEVICE
- 5 V, 10 V AND 15 V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18 V AND 25 °C FOR HCC DEVICE
- 100 % TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13 A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Package)

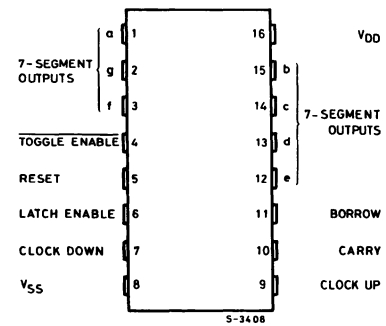
**C1**
(Chip Carrier)

**ORDER CODES :**
HCC40110BF HCF40110BEY
HCF40110BC1

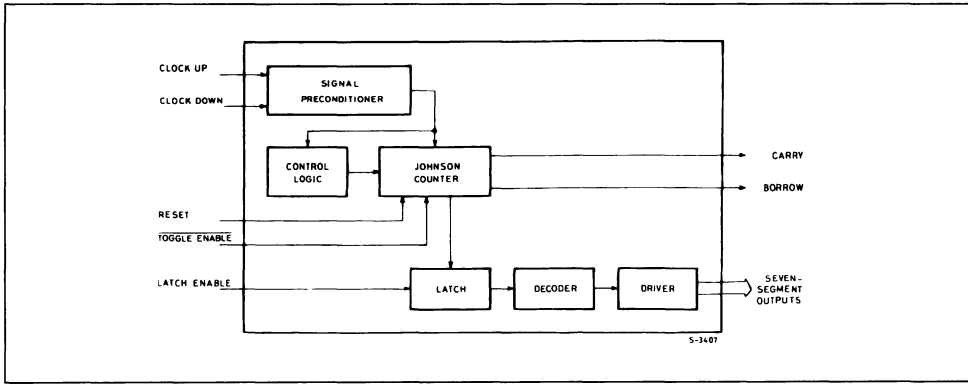
### DESCRIPTION

The **HCC 40110B** (extended temperature range) and **HCF 40110B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package. The **HCC/HCF 40110B** is a dual-clocked up/down counter with a special preconditioning circuit that allows the counter to be clocked, via positive going inputs, up or down regardless of that state or timing (within 100 ns typ.) of the other clock line. The clock signal is fed into the control logic and Johnson counter after is preconditioned. The outputs of the Johnson counter (which include antilock gating to avoid being locked at an illegal state) are fed into a latch. This data can be fed directly to the decoder through the latch or can be strobed to hold a particular count while the Johnson counter continues to be clocked. The decoder feeds a seven-segment bipolar output driver which can source up to 25 mA to drive LEDs and other displays such as low-voltage fluorescent and incandescent lamps. A short duration negative-going pulse appears on the BORROW output when the count changes from 0 to 9 or the CARRY output when the count changes from 9 to 0. At the other times the BORROW and CARRY output are a logic 1. The CARRY and BORROW outputs can be tied directly to the clock-up and clock-down lines respectively of another HCC/HCF 40110B for easy cascading of several counters.

### PIN CONNECTIONS



## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ * | Supply Voltage: **HCC** Types<br>**HCF** Types | -0.5 to +20<br>-0.5 to +18 | V<br>V |
| $V_I$ | Input Voltage | -0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for Top = Full Package Temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |

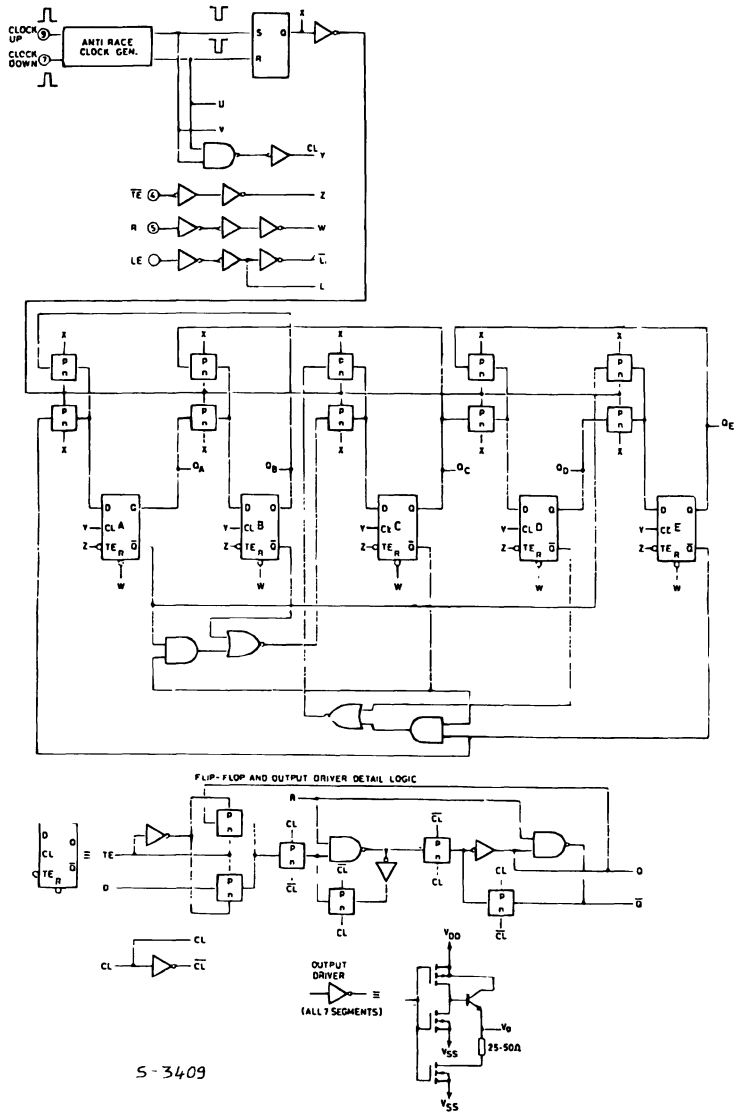
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability

* All voltage values are referred to $V_{SS}$ pin voltage.

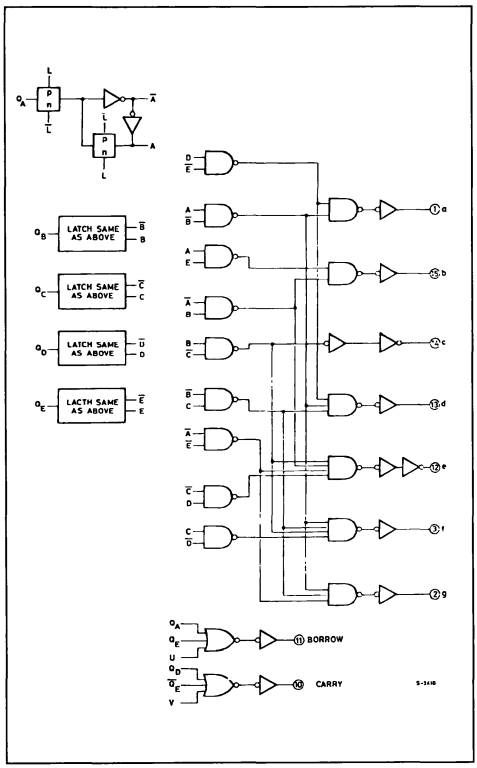
## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage: **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |

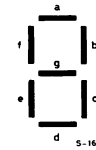
## LOGIC DIAGRAMS



## LOGIC DIAGRAM (continued)

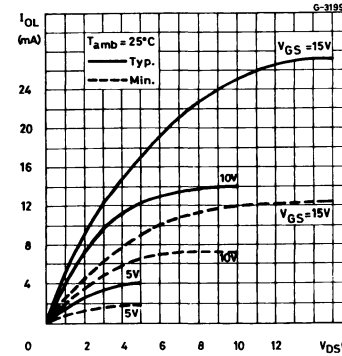



## DISPLAY SEGMENTS





Ouptut Low (sink) Current Characterisitcs.




## TRUTH TABLE

| CLOCK UP* | CLOCK DOWN* | LATCH ENABLE | $\overline{\text{TOGGLE ENABLE}}$ | RESET | COUNTER | DISPLAY |
|---|---|---|---|---|---|---|
| ⎍ | X | 0 | 0 | 0 | Increments by 1 | Follows Counter |
| X | ⎍ | 0 | 0 | 0 | Decrement by 1 | Follows Counter |
| ⎎ | ⎎ | X | X | 0 | No Change | No Change |
| X | X | X | X | 1 | Goes to 00000 | Follows Counter (Display = 0 ) |
| X | X | X | 1 | 0 | Inhibited | Remains Fixed |
| ⎍ | X | 1 | 0 | 0 | Increments by 1 | Remains Fixed |
| X | ⎍ | 1 | 0 | 0 | Decrement by 1 | Remains Fixed |

x = Don't care 1 = High State 2 = Low State

* Typically 100 ns between clock-up and clock-down positive transitions are required to ensure proper counting

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditios | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{LOW}$ * Min. | $T_{LOW}$ * Max. | 25 °C Min. | 25 °C Typ. | 25 °C Max. | $T_{HIGH}$ * Min. | $T_{HIGH}$ * Max. | |
| $I_L$ | Quiescent Current | HCC Types | 0/5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 15 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 20 | | 0.48 | 100 | | 3000 | |
| | | HCF Types | 0/5 | | | 5 | | 5 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 15 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/5 | | | 5 | | | | 4.95 | | | | V |
| | | | 0/10 | | | 10 | | | | 9.55 | | | | |
| | | | 0/15 | | | 15 | | | | 14.55 | | | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | | 5 | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| | | | 10/0 | | | 10 | | 0.05 | | 0 | 0.05 | | 0.05 | |
| | | | 15/0 | | | 15 | | 0.05 | | 0 | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/3.8 | | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/8.8 | | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/3.8 | | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 0.5/3.8 | | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 1/8.8 | | 10 | | 3 | | | 3 | | 3 | |
| | | | | 1.5/3.8 | | 15 | | 4 | | | 4 | | 4 | |
| $V_{OL}$ | Output Drive Voltage (for **HCC/HCF**) | | | | 0 | 5 | | | | 4.55 | | | | V |
| | | | | | 10 | 5 | | | | 4.13 | | | | |
| | | | | | 25 | 5 | | | | 3.64 | | | | |
| | | | | | 0 | 10 | | | | 9.55 | | | | |
| | | | | | 10 | 10 | | | | 9.25 | | | | |
| | | | | | 25 | 10 | | | | 8.85 | | | | |
| | | | | | 0 | 15 | | | | 14.55 | | | | |
| | | | | | 10 | 15 | | | | 14.21 | | | | |
| | | | | | 25 | 15 | | | | 13.9 | | | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ±0.1 | | $±10^{-5}$ | ±0.1 | | ±1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ±0.3 | | $±10^{-5}$ | ±0.3 | | ±1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{LOW}$ = -55 °C for **HCC** device: -40 °C for **HCF** device.

* $T_{HIGH}$ = +125 °C for **HCC** device: +85 °C for **HCF** device.

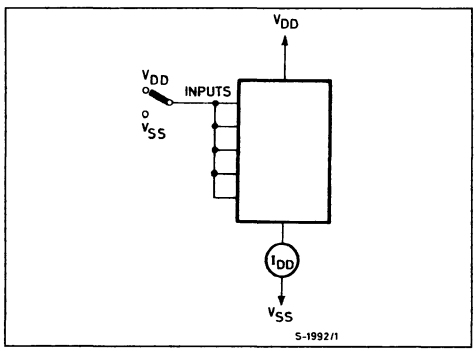
The Noise Margin for both "1" and "0" level is: 1V min. with $V_{DD}$ = 5 V, 2 V min. with $V_{DD}$ = 10 V, 2.5 V min. with $V_{DD}$ = 15 V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 KΩ, typical temperature coefficent for all $V_{DD}$ values is 03 %/°C, all input rise and fall times= 20 ns)

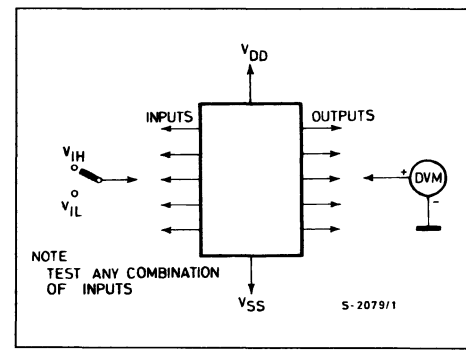
| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| **CLOCK UP/CLOCK DOWN** | | | | | | | |
| $t_W$ | Pulse Width | | 5 | | 85 | | ns |
| | | | 10 | | 35 | | |
| | | | 15 | | 15 | | |
| $f_{CL}$ | Maximum Frequency | | 5 | | 2.5 | | MHz |
| | | | 10 | | 5 | | |
| | | | 15 | | 8 | | |
| $t_{WC}$ | Carry Pulse Width | | 5 | | 225 | | ns |
| | | | 10 | | 100 | | |
| | | | 15 | | 70 | | |
| $t_{WB}$ | Borrow Pulse Width | | 5 | | 260 | | |
| | | | 10 | | 110 | | |
| | | | 15 | | 80 | | |
| **RESET** | | | | | | | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time Reset to Clock | | 5 | | 750 | | ns |
| | | | 10 | | 285 | | |
| | | | 15 | | 200 | | |
| | Delay from Reset to First Allowable Clock | | 5 | | 300 | | |
| | | | 10 | | 125 | | |
| | | | 15 | | 75 | | |
| $t_W$ | Pulse Width | | 5 | | 150 | | |
| | | | 10 | | 60 | | |
| | | | 15 | | 40 | | |

## TEST CIRCUITS

Quiescent Device Current.

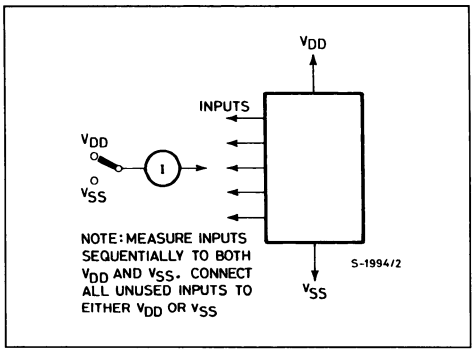



Noise Immunity.



## TEST CIRCUITS

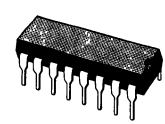
Input Leakage Current.



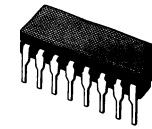
# HCC/HCF40174B

## HEX "D" – TYPE FLIP–FLOP

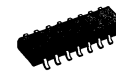
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED AT 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18 V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)



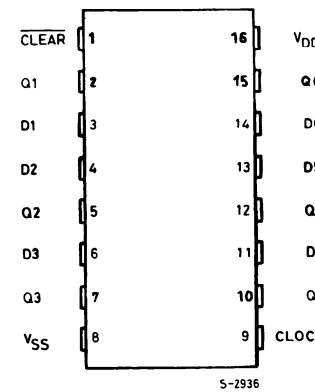
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC40174BF HCF40174BM1
HCF40174BEY HCF40174BC1

**PIN CONNECTIONS**

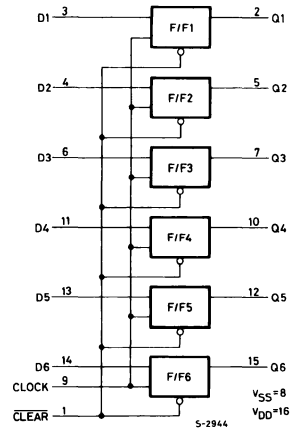



### DESCRIPTION

The **HCC40174B** (extended temperature range) and **HCF40174B** (intermediate temperature range) are monolithic integrated circuits available in 16-lead dual in-line plastic or ceramic package and plastic micro package.

The **HCC/HCF40174B** consists of six identical 'D' - type flip-flops having independent DATA inputs. The CLOCK and CLEAR inputs are common to all six units. Data is transferred to the Q outputs on the positive-going transition of the clock pulse. All six flip-flops are simultaneously reset by a low level on the CLEAR input.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

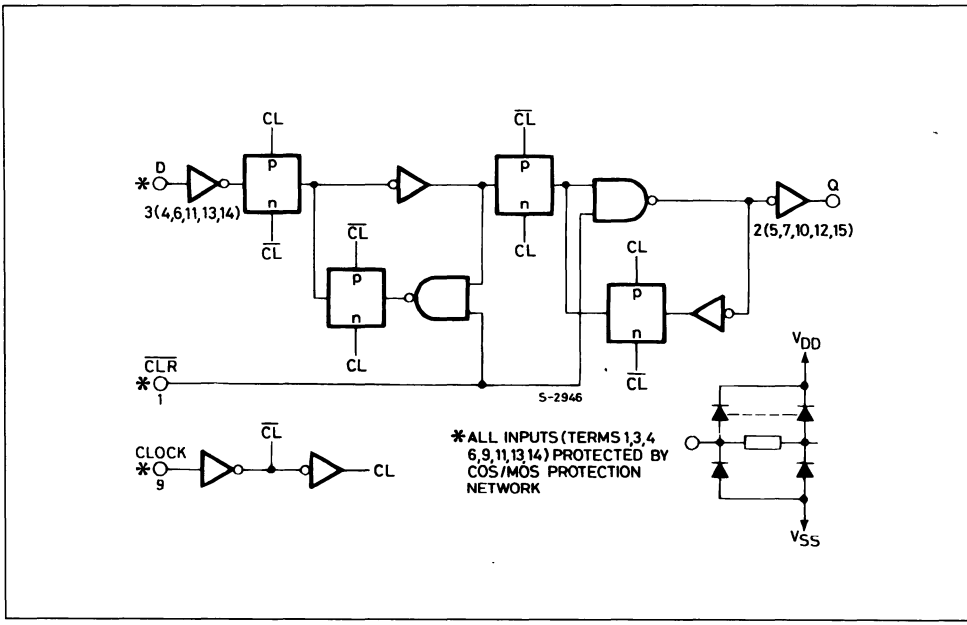
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0 5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

**LOGIC DIAGRAM** (1 of 6 Flip-Flops)




**TRUTH TABLE**

| Inputs | | | Output |
|---|---|---|---|
| Clock | Data | $\overline{\text{Clear}}$ | Q |
| ⎍ | 0 | 1 | 0 |
| ⎍ | 1 | 1 | 1 |
| ⎎ | X | 1 | NC |
| X | X | 0 | 0 |

1 = High Level X = Don't Care
0 = Low Level NC = No Change

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

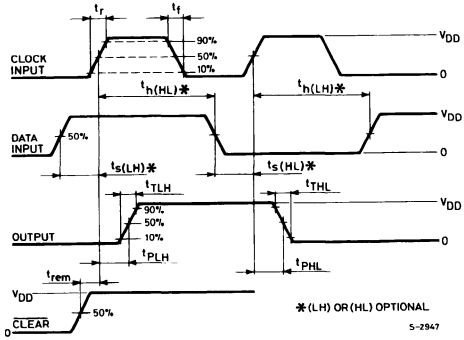
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 1 | | 0.02 | 1 | | 30 | μA |
| | | | 0/10 | | | 10 | | 2 | | 0.02 | 2 | | 60 | |
| | | | 0/15 | | | 15 | | 4 | | 0.02 | 4 | | 120 | |
| | | | 0/20 | | | 20 | | 20 | | 0.04 | 20 | | 600 | |
| | | HCF Types | 0/ 5 | | | 5 | | 4 | | 0.02 | 4 | | 30 | |
| | | | 0/10 | | | 10 | | 8 | | 0.02 | 8 | | 60 | |
| | | | 0/15 | | | 15 | | 16 | | 0.02 | 16 | | 120 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4 2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0 44 | − 1 | | − 0 36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1 1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device . − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is · 1V min with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2 5 V min. with $V_{DD}$ = 15V

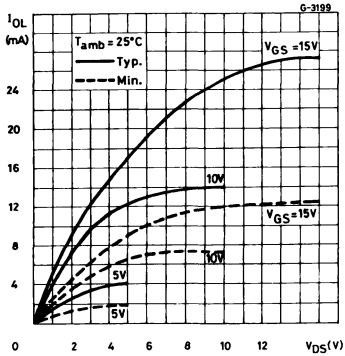
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall time = 20ns)

| Symbol | Parameter | Test Conditions | Value | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time Clock to Output | | 5 | | 150 | 300 | ns |
| | | | 10 | | 70 | 140 | |
| | | | 15 | | 50 | 100 | |
| $t_{PHL}$ | Propagation Delay Time $\overline{\text{Clear}}$ to Output | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_{setup}$ | Data Setup Time | | 5 | 40 | 20 | | ns |
| | | | 10 | 20 | 10 | | |
| | | | 15 | 10 | 0 | | |
| $t_{hold}$ | Data Hold Time | | 5 | 80 | 40 | | ns |
| | | | 10 | 40 | 20 | | |
| | | | 15 | 30 | 15 | | |
| $t_W$ | Clock Input Pulse Width Low Level | | 5 | 130 | 65 | | ns |
| | | | 10 | 60 | 30 | | |
| | | | 15 | 40 | 20 | | |
| $t_W$ | Clock Input Pulse Width High Level | | 5 | 130 | 65 | | ns |
| | | | 10 | 60 | 30 | | |
| | | | 15 | 40 | 20 | | |
| $t_W$ | $\overline{\text{Clear}}$ Input Pulse Width Low Level | | 5 | 100 | 50 | | ns |
| | | | 10 | 50 | 25 | | |
| | | | 15 | 40 | 20 | | |
| $t_r$, $t_f$ | Clock Input Rise or Fall Time | | 5 | | | 15 | μs |
| | | | 10 | | | 15 | |
| | | | 15 | | | 15 | |
| $t_{rem}$ | $\overline{\text{Clear}}$ Removal Time | | 5 | 0 | − 40 | | ns |
| | | | 10 | 0 | − 15 | | |
| | | | 15 | 0 | − 10 | | |
| $f_{CL}$ | Maximum Clock Input Frequency | | 5 | 3.5 | 7 | | MHz |
| | | | 10 | 6 | 12 | | |
| | | | 15 | 8 | 16 | | |

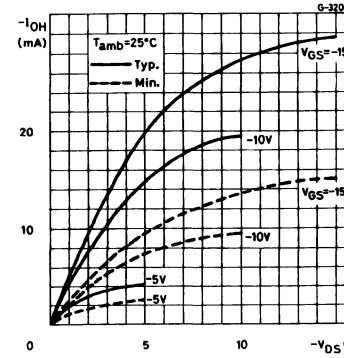
## WAVEFORMS



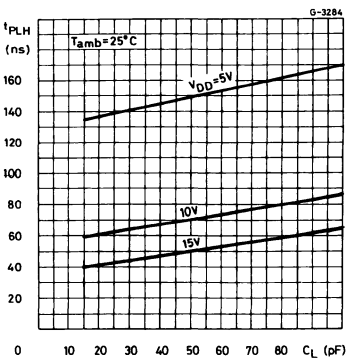

Output Low (sink) Current Characteristics.



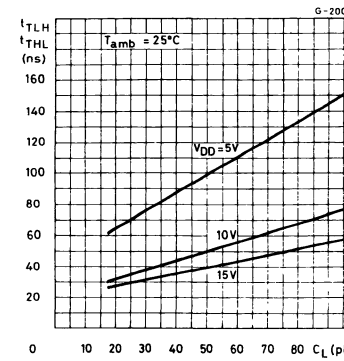

Output High (source) Current Characteristics.



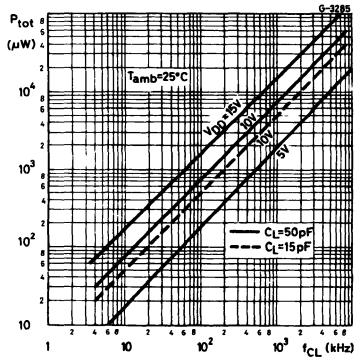

Typical Propagation Delay Time (clock to output) vs. Load Capacitance.




Typical Transition Time vs. Load Capacitance.

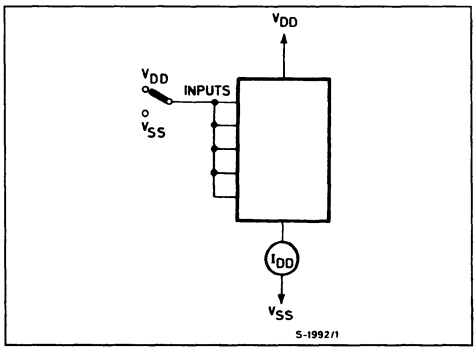


Typical Dynamical Power Dissipation vs. Clock Frequency.

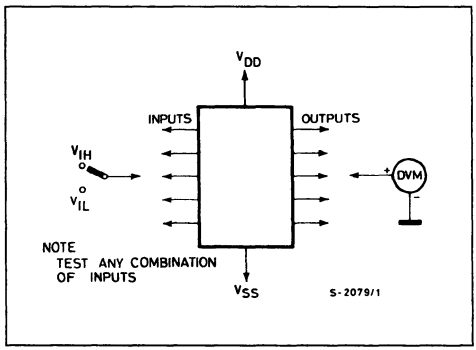



## TEST CIRCUITS

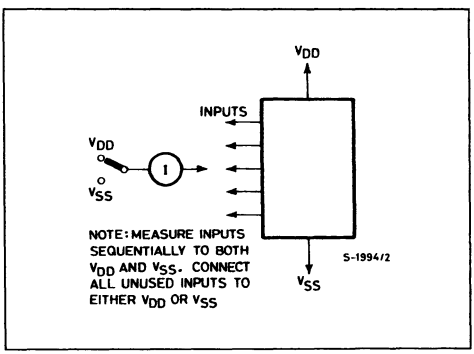
Quiescent Device Current.



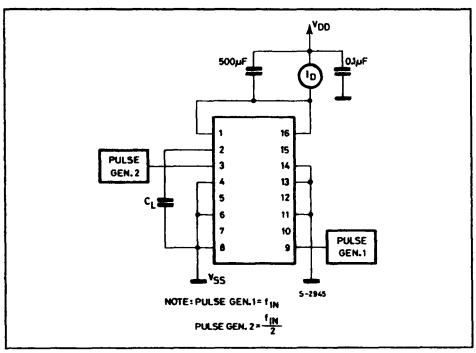

Input Voltage.




Input Leakage Current.




Dynamic Power Dissipation.

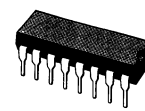


# HCC/HCF40160B-40161B HCC/HCF40162B-40163B

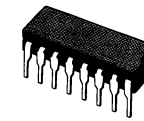
## SYNCHRONOUS PROGRAMMABLE 4-BIT COUNTERS

**40160B - DECADE WITH ASYNCHRONOUS CLEAR**
**40161B - BINARY WITH ASYNCHRONOUS CLEAR**
**40162B - DECADE WITH SYNCHRONOUS CLEAR**
**40163B - BINARY WITH SYNCHRONOUS CLEAR**

- INTERNAL LOOK-AHEAD FOR FAST COUNTING
- CARRY OUTPUT FOR CASCADING
- SYNCHRONOUSLY PROGRAMMABLE
- LOW-POWER TTL COMPATIBILITY
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED AT 20V FOR HCC DEVICE
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25oC FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N. 13A, " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES "



**EY**
(Plastic Package)



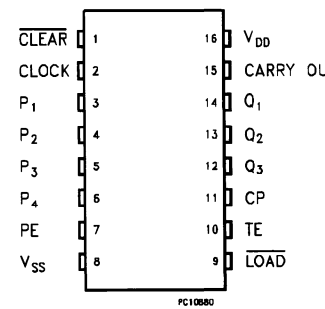
**F**
(Ceramic Package)

**M1**
(Micro Package)

**C1**
(Chip Carrier)

**ORDER CODES :**
HCC40XXXBF HCF40XXXBEY
HCF40XXXBC1

**PIN CONNECTIONS**




### DESCRIPTION

The **HCC40160B, 40161B, 40162B, 40163B** (extended temperature range) and **HCF40160B, 40161B, 40162B, 40163B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in line plastic or ceramic package and plastic micropackage.
**HCC/HCF40160B, 40161B, 40162B** and **40163B** are 4-bit synchronous programmable counters. The $\overline{\text{CLEAR}}$ function of the **HCC/HCF40162B** and **40163B** is synchronous and a low on the at the clear $\overline{\text{CLEAR}}$ input sets all four outputs low on the next positive CLOCK edge. The $\overline{\text{CLEAR}}$ function of the **HCC/HCF40160B** and **40161B** is asynchronous and a low level at the $\overline{\text{CLEAR}}$ input sets all four outputs low regardless of the state of the CLOCK, $\overline{\text{LOAD}}$ or ENABLE inputs. A low level at the $\overline{\text{LOAD}}$ input disables the counter and causes the output to agree with the set-up data after the next CLOCK pulse regardless of the conditions of the ENABLE inputs. The carry look-ahead circuitry provides for

cascading counter for n-bit synchronour application without additional gating. Instrumental in accomplishing this function are two count-enable input and a carry output (COUT). Counting is enable when both PE and TE inputs are high. The TE input is fed forward to enable COUT. This enable output produces a positive output pulse with a duration approximately equal to the positive portion of the Q1 output. This positive overflow carry pulse can be used to enable successive cascaded stages. Logic transitions at the PE or TE inputs may occur when the clock is either high or low.

## ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ * | Supply Voltage: **HCC** Types<br>**HCF** Types | -0.5 to +20<br>-0.5 to +18 | V<br>V |
| $V_I$ | Input Voltage | -0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for Top = Full Package Temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to $V_{SS}$ pin voltage

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage: **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |

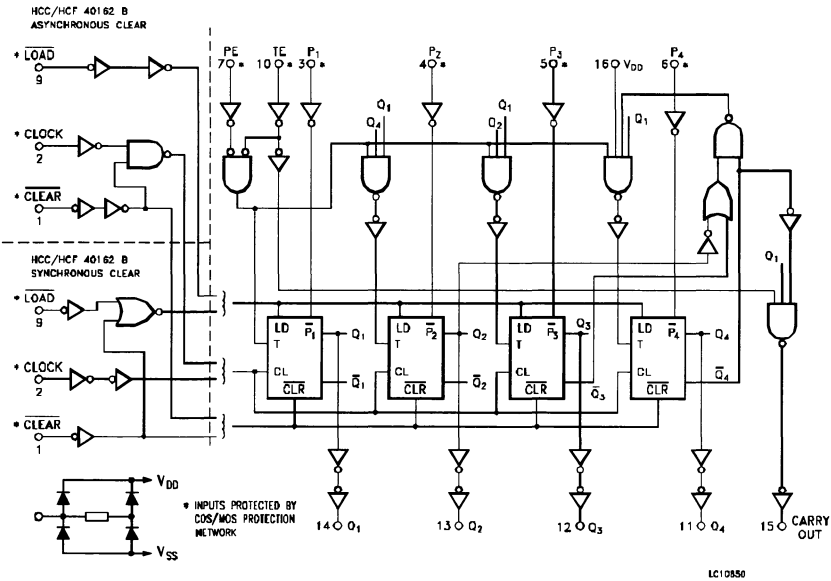
## TRUTH TABLE

| Clock | $\overline{CLR}$ | $\overline{LOAD}$ | PE | TE | Operation |
|---|---|---|---|---|---|
| ⎍ | 1 | 0 | X | X | Preset |
| ⎍ | 1 | 1 | 0 | X | NC |
| ⎍ | 1 | 1 | X | 0 | NC |
| ⎍ | 1 | 1 | 1 | 1 | Count |
| X | 0 | X | X | X | Reset (HCC/HCF40160B, HCC/HCF40161B) |
| ⎍ | 0 | X | X | X | Reset (HCC/HCF40162B, HCC/HCF40163B) |
| ⎌ | 1 | X | X | X | NC (HCC/HCF40162B, HCC/HCF40163B) |

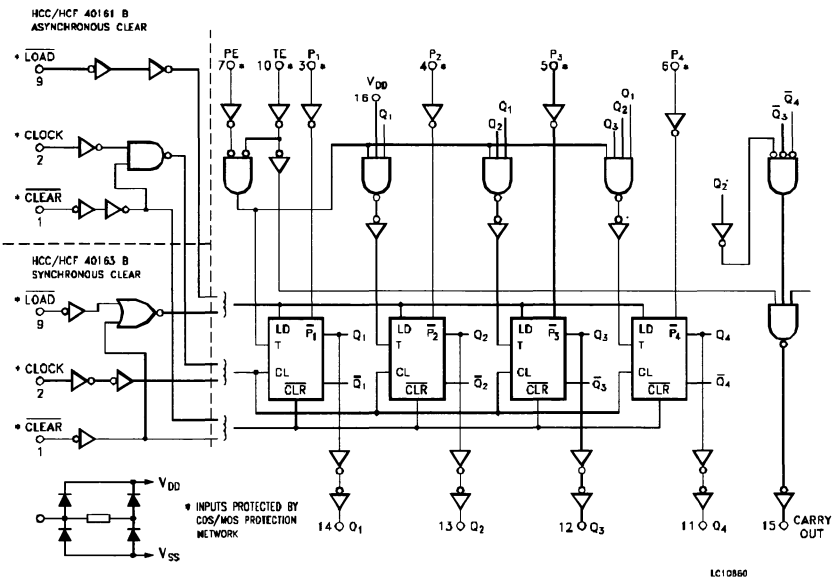
1 = HIGH LEVEL, 0 = LOW LEVEL, X = DON'T CARE, NC = NO CHANGE

## LOGIC DIAGRAMS

### HCC40160B/HCC40162B

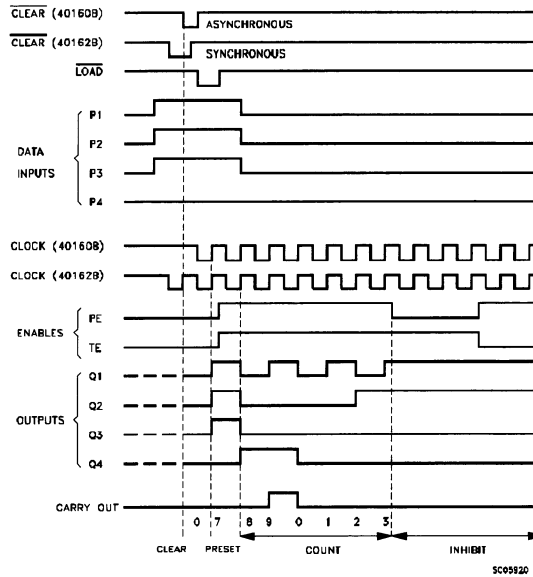



### HCC40161B/HCC40163B

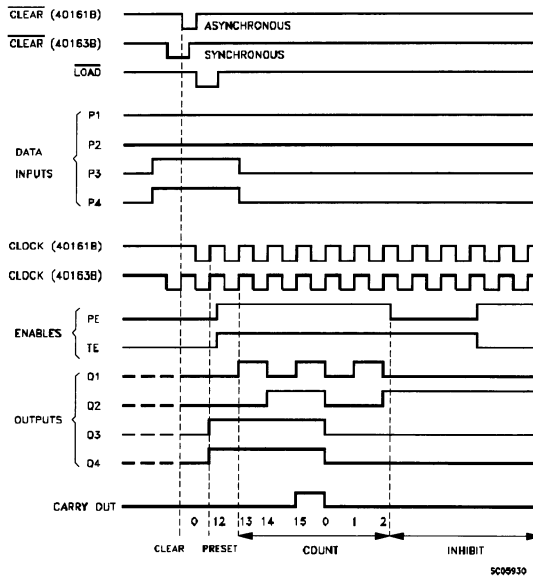


## TIMING DIAGRAMS

### HCC40160B/HCC40162B




### HCC40161B/HCC40163B



## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditios | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{LOW}$ * Min. | $T_{LOW}$ * Max. | 25 °C Min. | 25 °C Typ. | 25 °C Max. | $T_{HIGH}$ * Min. | $T_{HIGH}$ * Max. | |
| $I_L$ | Quiescent Current | HCC Types | 0/5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/5 | 2.5 | | 5 | -2 | | -1.6 | -3.2 | | -1.15 | | mA |
| | | | 0/5 | 4.6 | | 5 | -0.64 | | -0.51 | -1 | | -0.36 | | |
| | | | 0/10 | 9.5 | | 10 | -1.6 | | -1.3 | -2.6 | | -0.9 | | |
| | | | 0/15 | 13.5 | | 15 | -4.2 | | -3.4 | -6.8 | | -2.4 | | |
| | | HCF Types | 0/5 | 2.5 | | 5 | -1.53 | | -1.36 | -3.2 | | -1.1 | | |
| | | | 0/5 | 4.6 | | 5 | -0.52 | | -0.44 | -1 | | -0.36 | | |
| | | | 0/10 | 9.5 | | 10 | -1.3 | | -1.1 | -2.6 | | -0.9 | | |
| | | | 0/15 | 13.5 | | 15 | -3.6 | | -3.0 | -6.8 | | -2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/5 | 0.4 | | 5 | 0.53 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ±0.1 | | $±10^{-5}$ | ±0.1 | | ±1 | μA |
| | | HCC Types | 0/15 | | | 15 | | ±0.3 | | $±10^{-5}$ | ±0.3 | | ±1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{LOW}$ = -55 °C for **HCC** device: -40 °C for **HCF** device.

* $T_{HIGH}$ = +125 °C for **HCC** device. +85 °C for **HCF** device.

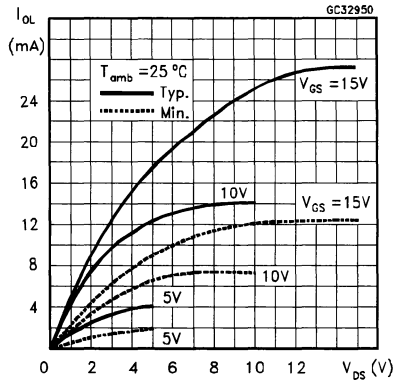
The Noise Margin for both "1" and "0" level is. 1V min. with $V_{DD}$ = 5 V, 2 V min. with $V_{DD}$ = 10 V, 2.5 V min. with $V_{DD}$ = 15 V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 KΩ, typical temperature coefficent for all $V_{DD}$ values is 03 %/°C, all input rise and fall times= 20 ns)

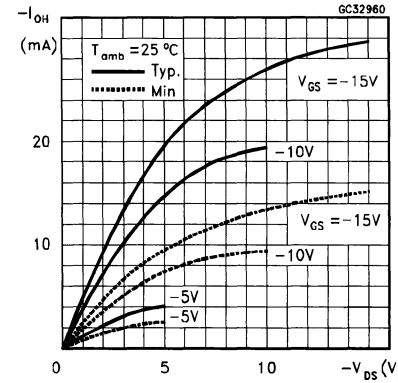
| Symbol | Parameter | Test Conditions | Value | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time Clock to Q | | 5 | | 200 | 400 | ns |
| | | | 10 | | 80 | 160 | |
| | | | 15 | | 60 | 120 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time Clock to $C_{OUT}$ | | 5 | | 225 | 450 | ns |
| | | | 10 | | 95 | 190 | |
| | | | 15 | | 70 | 140 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time TE to $C_{OUT}$ | | 5 | | 125 | 250 | ns |
| | | | 10 | | 55 | 110 | |
| | | | 15 | | 40 | 80 | |
| $t_{setup}$ | Setup Time Data to Clock | | 5 | 240 | 120 | | ns |
| | | | 10 | 90 | 45 | | |
| | | | 15 | 60 | 30 | | |
| $t_{setup}$ | Setup Time Load to Clock | | 5 | 240 | 120 | | ns |
| | | | 10 | 90 | 45 | | |
| | | | 15 | 60 | 30 | | |
| $t_{setup}$ | Setup Time PE or TE to Clock | | 5 | 340 | 170 | | ns |
| | | | 10 | 140 | 70 | | |
| | | | 15 | 100 | 50 | | |
| $t_{hold}$ | Hold Time | | 5 | 0 | | | ns |
| | | | 10 | 0 | | | |
| | | | 15 | 0 | | | |
| $t_{THL}$ $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_W$ | CLock Input Pulse Width | | 5 | 170 | 85 | | ns |
| | | | 10 | 70 | 35 | | |
| | | | 15 | 50 | 25 | | |
| $f_{CL}$ | Maximum Clock Input Frequency | | 5 | 2 | 3 | | MHz |
| | | | 10 | 5.5 | 8.5 | | |
| | | | 15 | 8 | 12 | | |
| $t_r$ $t_f$ | Clock Input Rise or Fall Time * | | | | | 200 | ns |
| | | | | | | 70 | |
| | | | | | | 15 | |
| $t_{PHL}$ | Propagation Delay Time (40160B, 40161B) Clear to Q | | 5 | | 250 | 500 | ns |
| | | | 10 | | 110 | 220 | |
| | | | 15 | | 80 | 160 | |
| $t_{setup}$ | Setup Time (40162B, 40163B) Clear to Clock | | 5 | 340 | 170 | | ns |
| | | | 10 | 140 | 70 | | |
| | | | 15 | 100 | 50 | | |
| $t_{hold}$ | Hold Time (40162B, 40163B) Clear to Clock | | 5 | 0 | | | ns |
| | | | 10 | 0 | | | |
| | | | 15 | 0 | | | |
| $t_{rem}$ | $\overline{\text{Clear}}$ Removal Time (40162B, 40163B) | | 5 | 200 | 100 | | ns |
| | | | 10 | 100 | 50 | | |
| | | | 15 | 70 | 35 | | |
| $t_W$ | $\overline{\text{Clear}}$ Input Pulse Width Low Level (40160B, 40161B) | | 5 | 170 | 85 | | ns |
| | | | 10 | 70 | 35 | | |
| | | | 15 | 50 | 25 | | |

* If more than one unit is cascated in the parallel clocked application, tr should be made less than or equal to the sum of the fixed propagation delay at 50 pF and the transition time of the carry output driving stage for the estimated capacitance

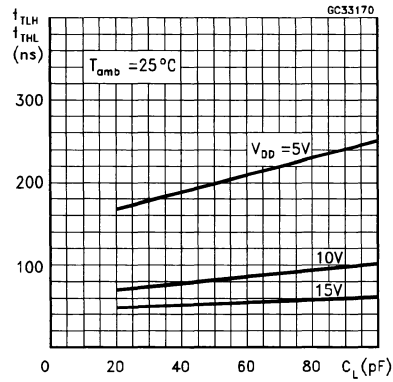
Output Low (sink) Current Characteristics



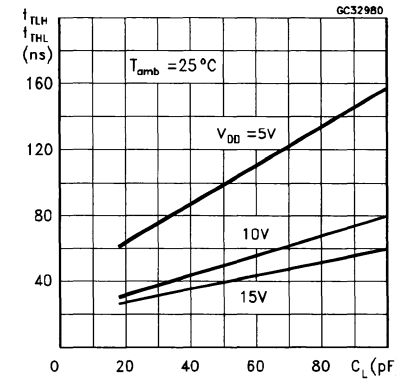

Output High (source) Current Characteristics



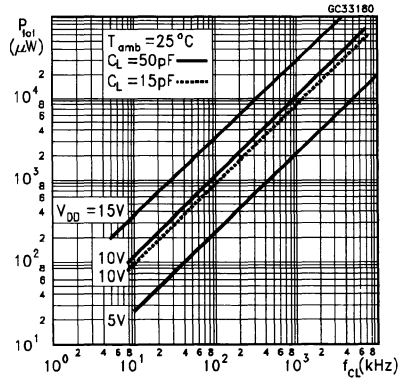

Typical Propagation Delay Time vs Load Capacitance




Typical Transition Time vs Load Capacitance

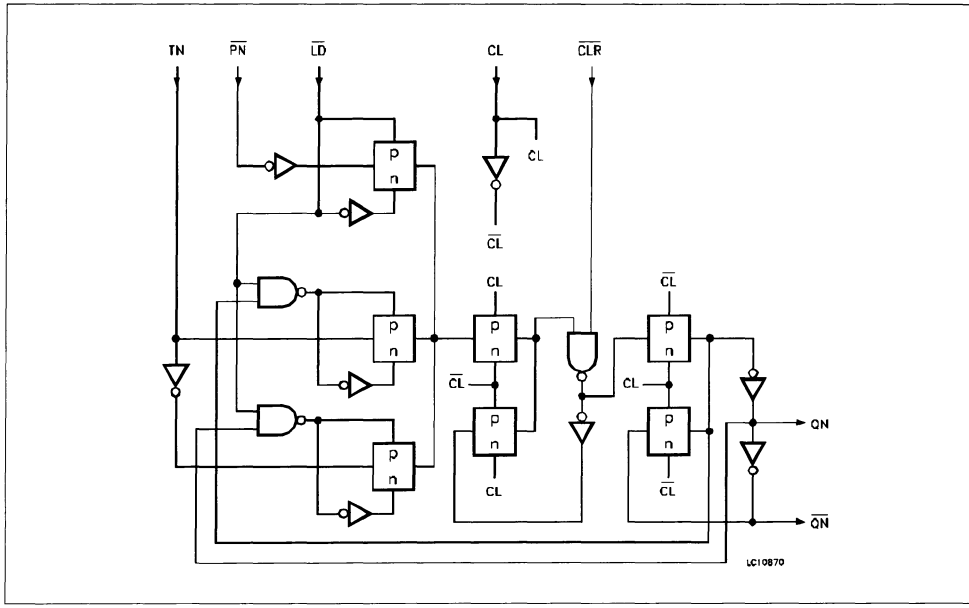



Typical Dynamic Power Dissipation vs Input Frequency

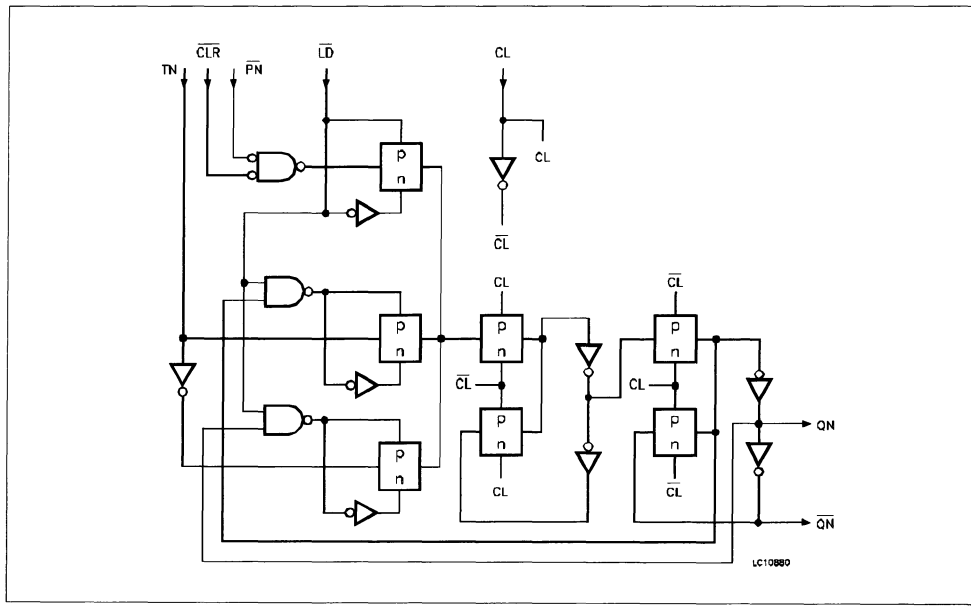


## TYPICAL APPLICATIONS

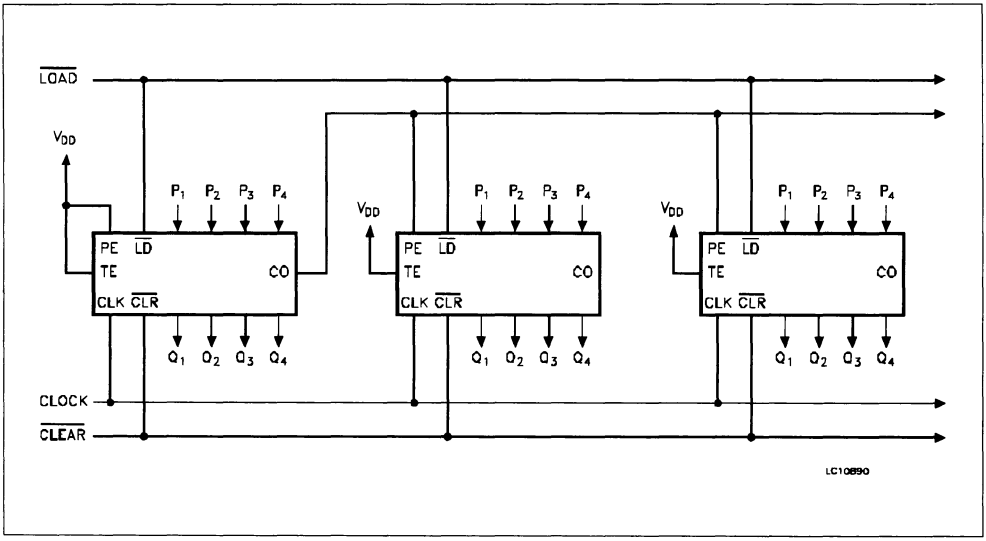
Detail of Flip-flops For 40160B And 40161B (Asynchronous Clear)



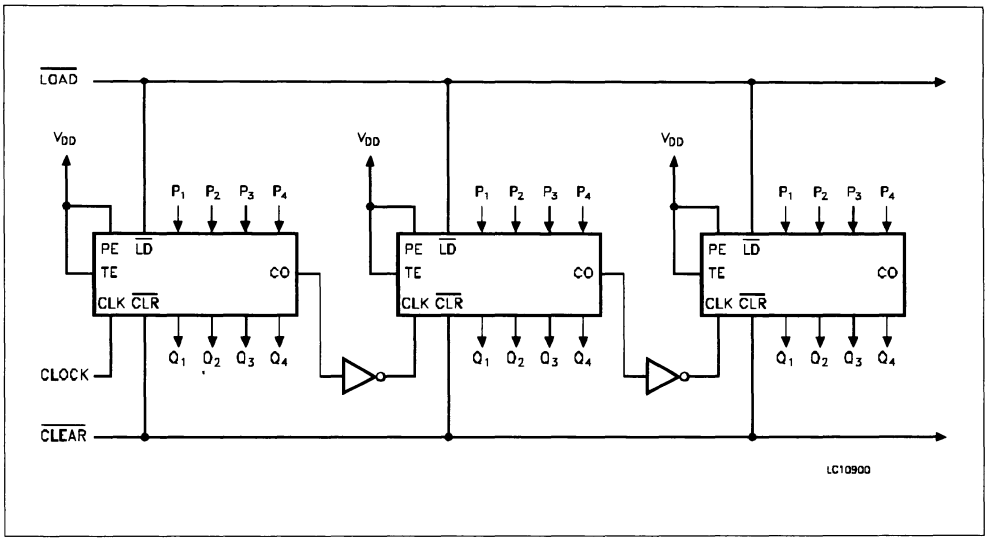

Detail of Flip-flops For 40162B And 40163B (Synchronous Clear)



Cascading Counter Packages In The Parallel-Clocked Mode

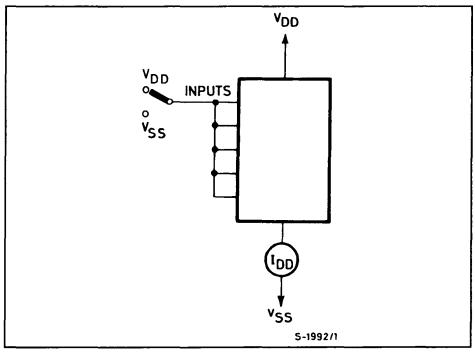



Cascading Counter Packages In The Ripple-Clocked Mode

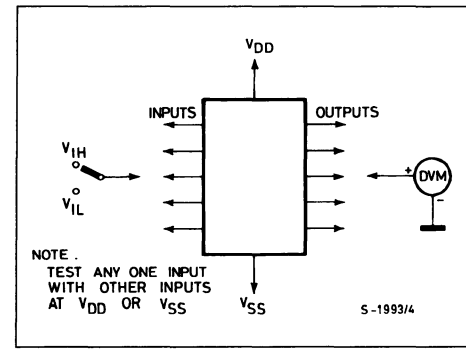


## TEST CIRCUIT

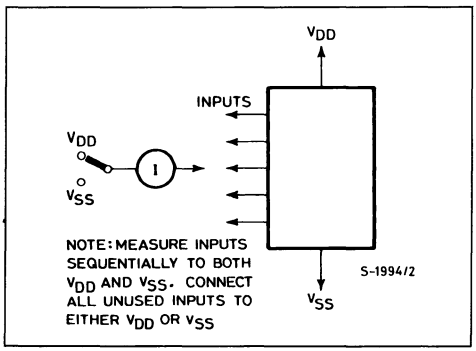
Quiescent Device Current.



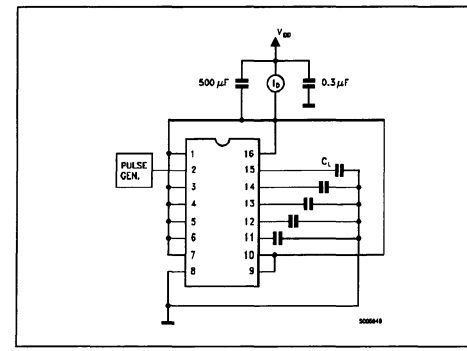

Input Voltage.




Input Leakage Current.




Dinamic Power Dissipation



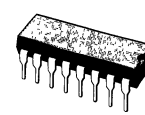
# HCC40147B
# HCF40147B

## 10 TO 4 LINE BCD PRIORITY ENCODER

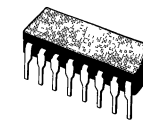
- ENCODES 10 LINE TO 4 LINE BCD
- ACTIVE LOW INPUTS AND OUTPUTS
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERIZATION
- 100 % TESTED FOR QUIESCENT CURRENT AT 20 V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- MAXIMUM INPUT CURREENT OF 1 μA AT 18V OVER FULL PACKAGE TEMPERATURE RANGE; 100 nA AT 18 V AND 25 °C
- NOISE MARGIN (FULL PACKAGE TEMPERATURE RANGE): 1V AT $V_{DD}$ = 5V, 2V AT $V_{DD}$ = 10V, 2.5V AT $V_{DD}$ = 15V

**APPLICATIONS:**

- KEYBOARD ENCODING
- 10 LINE TO BCD ENCODING
- RANGE SELECTION



**EY**
(Plastic Package)



**F**
(Ceramic Package)

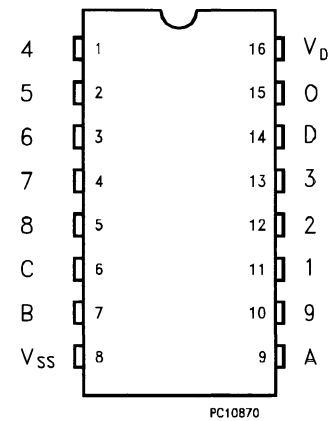
**M1**
(Micro Package)

**C1**
(Chip Carrier)

**ORDER CODES :**

HCC40147BF HCF40147BM1
HCF40147BEY HCF40147BC1

**PIN CONNECTIONS**




### DESCRIPTION

The **HCC/HCF40147B** CMOS encoder features priority encoding of the inputs to ensure that only the highest order data line is encoded. Ten data input lines (0-9) are encoded to four line (8, 4, 2, 1) BCD. The highest priority line is line 9. All four output lines are logic 1 (VSS) when all input lines are logic 0. All inputs and outputs are buffered, and each output can drive one TTL Low Power Schottky load. The **HCC/HCFF40147** is functionally similar to the T54/T74LS147 if pin 15 is tied low.

The **HCC/HCF40147B** types are supplied in 16 lead plastic or ceramic and plastic micropackage.

## ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ * | Supply Voltage: **HCC** Types<br>**HCF** Types | -0.5 to +20<br>-0.5 to +18 | V<br>V |
| $V_I$ | Input Voltage | -0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for Top = Full Package Temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to $V_{SS}$ pin voltage

## RECOMMENDED OPERATING CONDITIONS

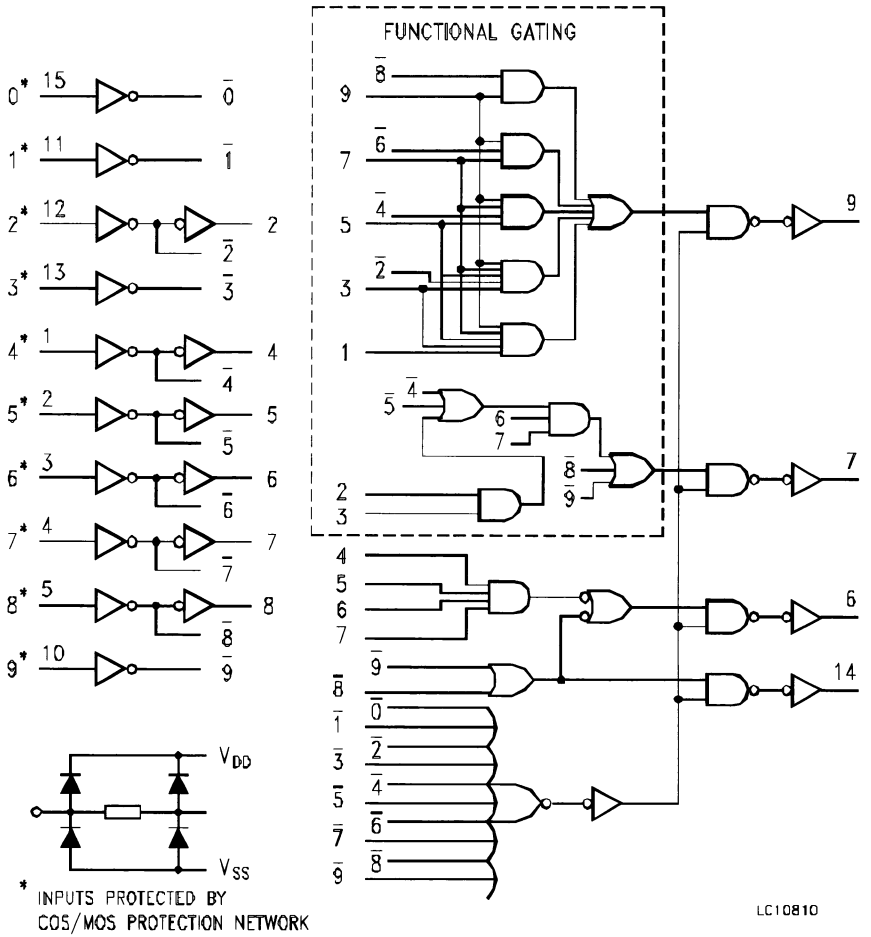
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage: **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature: **HCC** Types<br>**HCF** Types | -55 to +125<br>-40 to +85 | °C<br>°C |

## TRUTH TABLE

| INPUT | | | | | | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **D** | **C** | **B** | **A** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| X | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| X | X | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| X | X | X | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| X | X | X | X | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| X | X | X | X | X | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| X | X | X | X | X | X | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| X | X | X | X | X | X | X | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| X | X | X | X | X | X | X | X | 1 | 0 | 1 | 0 | 0 | 0 |
| X | X | X | X | X | X | X | X | X | 1 | 1 | 0 | 0 | 1 |

0 = High Level, 1 = Low Level, X = Don't Care

## LOGIC DIAGRAM



## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{LOW}$ * Min. | $T_{LOW}$ * Max. | 25 °C Min. | 25 °C Typ. | 25 °C Max. | $T_{HIGH}$ * Min. | $T_{HIGH}$ * Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/5 | | | 5 | | 1 | | 0.02 | 1 | | 30 | μA |
| | | | 0/10 | | | 10 | | 2 | | 0.02 | 2 | | 60 | |
| | | | 0/15 | | | 15 | | 4 | | 0.02 | 4 | | 120 | |
| | | | 0/20 | | | 20 | | 20 | | 0.04 | 20 | | 600 | |
| | | HCF Types | 0/5 | | | 5 | | 4 | | 0.02 | 4 | | 30 | |
| | | | 0/10 | | | 10 | | 8 | | 0.02 | 8 | | 60 | |
| | | | 0/15 | | | 15 | | 16 | | 0.02 | 16 | | 120 | |
| $V_{OH}$ | Output High Voltage | | 0/5 | | < 1 | 5 | 4 95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14 95 | | 14 95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0 5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13 5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/5 | 2.5 | | 5 | -2 | | -1.6 | -3 2 | | -1 15 | | mA |
| | | | 0/5 | 4.6 | | 5 | -0.64 | | -0.51 | -1 | | -0.36 | | |
| | | | 0/10 | 9.5 | | 10 | -1.6 | | -1.3 | -2.6 | | -0.9 | | |
| | | | 0/15 | 13.5 | | 15 | -4 2 | | -3.4 | -6 8 | | -2.4 | | |
| | | HCF Types | 0/5 | 2.5 | | 5 | -1.53 | | -1.36 | -3.2 | | -1.1 | | |
| | | | 0/5 | 4.6 | | 5 | -0.52 | | -0.44 | -1 | | -0.36 | | |
| | | | 0/10 | 9.5 | | 10 | -1.3 | | -1.1 | -2.6 | | -0.9 | | |
| | | | 0/15 | 13 5 | | 15 | -3 6 | | -3.0 | -6.8 | | -2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0 36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4 2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1 3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | | 0/18 | Any Input | | 18 | | ±0 1 | | $\pm10^{-5}$ | ±0.1 | | ±1 | μA |
| | | | 0/15 | | | 15 | | ±0.3 | | $\pm10^{-5}$ | ±0.3 | | ±1 | μA |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{LOW}$ = -55 °C for **HCC** device -40 °C for **HCF** device

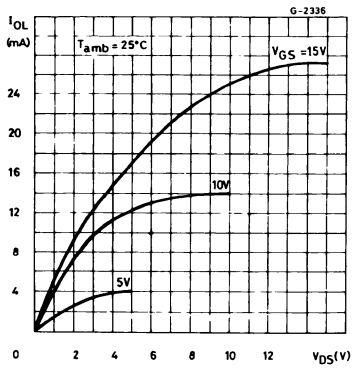
* $T_{HIGH}$ = +125 °C for **HCC** device +85 °C for **HCF** device

The Noise Margin for both "1" and "0" level is 1V min with $V_{DD}$ = 5 V, 2 V min with $V_{DD}$ = 10 V, 2.5 V min with $V_{DD}$ = 15 V

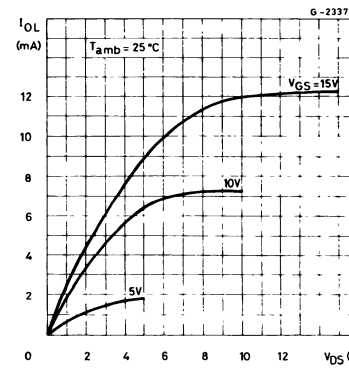
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 KΩ, typical temperature coefficent for all $V_{DD}$ values is 03 %/°C, all input rise and fall times= 20 ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time In Phase Output | | 5 | | 450 | 900 | ns |
| | | | 10 | | 200 | 400 | |
| | | | 15 | | 150 | 300 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time Out of Phase Output | | 5 | | 425 | 850 | ns |
| | | | 10 | | 175 | 350 | |
| | | | 15 | | 125 | 250 | |
| $t_{TLH}$ $t_{THL}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $C_I$ | Input Capacitance | | | | 5 | 7.5 | pF |

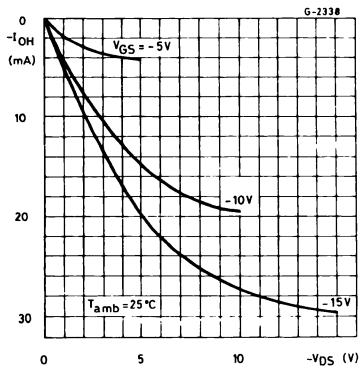
Typical Output Low (source) Current Characteristics



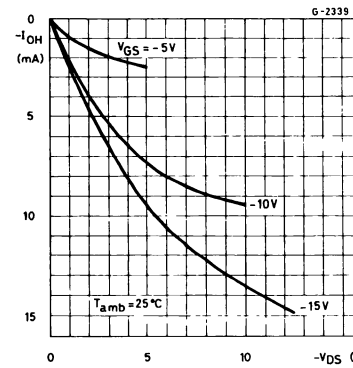

Minimum Output Low (source) Current Characteristics



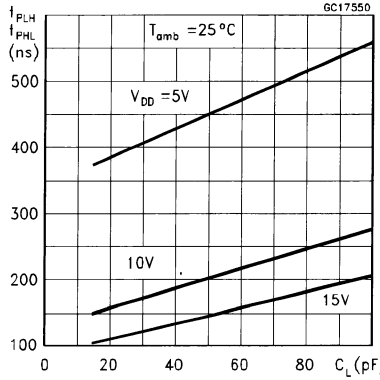

Typical Output High (source) Current Characteristics



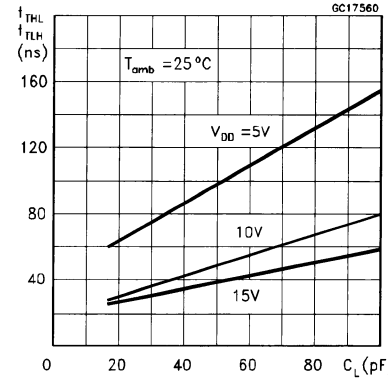

Minimum Output High (source) Current Characteristics



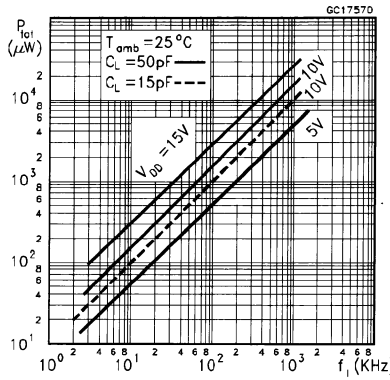
Propagation Delay Time vs Load Capacitance




Tipical Transition Time vs Load Capacitance

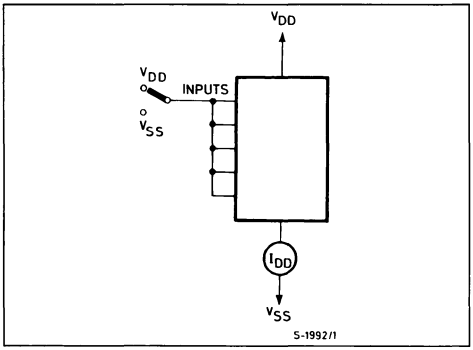



Typical Dynamic Power Dissipation vs Input Frequency

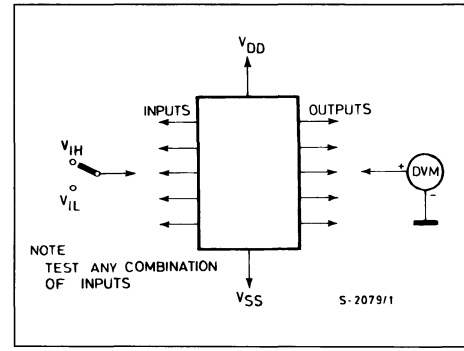


## TEST CIRCUITS

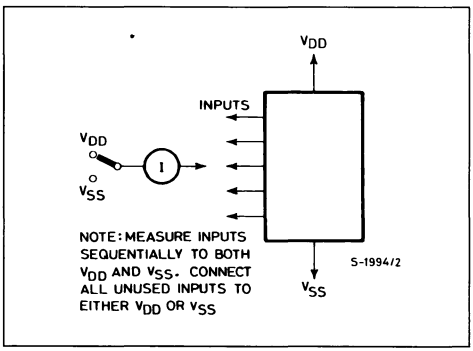
Quiescent Device Current.



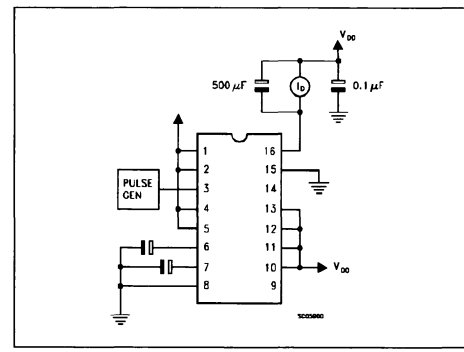

Noise Immunity.




Input Leakage Current.




Dynamic Power DIssipation Test Circuit

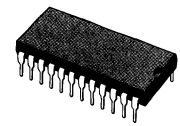


SGS-THOMSON MICROELECTRONICS

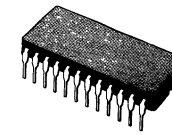
# HCC/HCF40181B

## 4-BIT ARITHMETIC LOGIC UNIT

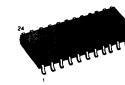
- FULL LOOK-AHEAD CARRY FOR SPEED OPERATIONS ON LONG WORDS
- GENERATES 16 LOGIC FUNCTIONS OF TWO BOOLEAN VARIABLES
- GENERATES 16 ARITHMETIC FUNCTIONS OF TWO 4-BIT BINARY WORDS
- A = B COMPARATOR OUTPUT AVAILABLE
- RIPPLE-CARRY INPUT AND OUTPUT AVAILABLE
- TYPICAL ADDITION TIME 200ns @ $V_{DD}$ = 10V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT AT 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

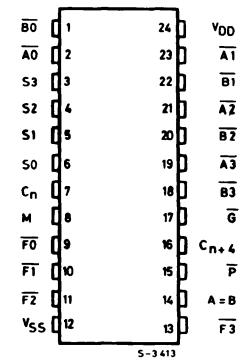


**M1**
(Micro Package)

**ORDER CODES :**

HCC40181BF
HCF40181BEY
HCF40181BM1

**PIN CONNECTIONS**



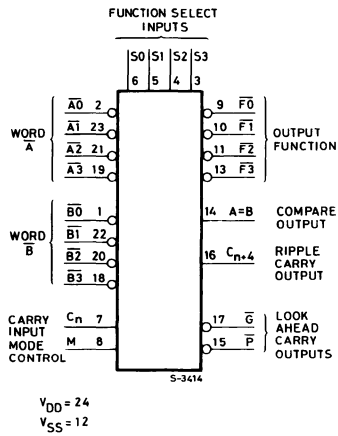

### DESCRIPTION

The **HCC40181B** (extended temperature range) and **HCF40181B** (intermediate temperature range) are monolithic integrated circuits, available in 24-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF40181B** is a low-power four-bit parallel arithmetic logic unit (ALU) capable of providing 16 binary arithmetic operations on two four-bit words and 16 logical functions of two Boolean variables. The mode control input M selects logical (M = High) or arithmetic (M = Low) operation. The four select inputs (S0, S1, S2, and S3) select the desired logical or arithmetic functions, which include AND, OR, NAND, NOR, and exclusive-OR and-NOR in the logical mode, and addition, subtraction, decrement, left-shift and straight transfer in the arithmetic mode, according to the truth table. The **HCC/HCF40181B** operation may be interpreted with either active-low or active-high data at the A and B word inputs and the function outputs F, by using the appropriate truth table. The **HCC/HCF40181B** contains logic for full look-ahead carry operation for fast carry generation using the carry-generate and carry-propagate outputs $\overline{G}$ and

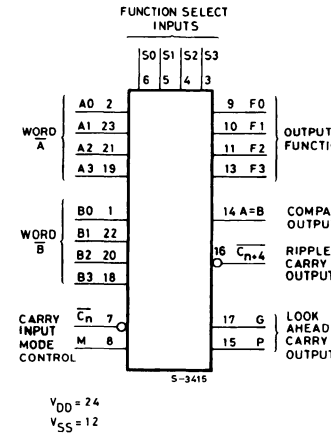
$\overline{P}$ for the four bits of the **HCC/HCF40181B**. Use of the **HCC/HCF40182B** look-ahead carry generator in conjunction with multiple **HCC/HCF40181B**'s permits high-speed arithmetic operations on long words. A ripple carry output $C_{n+4}$ is available for use in systems where speed is not of primary importance. Also included in the **HCC/HCF40181B** is a comparator output A = B, which assumes a high level whenever the two four-bit input words A and B are equal and the device is in the subtract mode. In addition, relative magnitude information may be derived from the carry-in input $C_n$ and ripple carry-out output $C_{n+4}$ by placing the unit in the subtract mode and externally decoding using the information in table II. The **HCC/HCF40181B** is similar to industry types MC 14581 and 74181.

## FUNCTIONAL DIAGRAM

Active-low Data.




Active-high Data.




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltages are with respect to $V_{SS}$ (GND)

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | – 55 to + 125<br>– 40 to + 85 | °C<br>°C |

## TRUTH TABLES

**Table 1.**

| Function Select | | | | Inputs/Outputs Active Low | | Inputs/Outputs Active High | |
|---|---|---|---|---|---|---|---|
| | | | | Logic Function (M = H) | Arithmetic* Function (M = L, $C_n$ = L) | Logic Function (M = H) | Arithmetic* Function (M = L, $\overline{C_n}$ = H) |
| S3 | S2 | S1 | S0 | | | | |
| 0 | 0 | 0 | 0 | $\overline{A}$ | A minus 1 | $\overline{A}$ | A |
| 0 | 0 | 0 | 1 | $\overline{AB}$ | AB minus 1 | $\overline{A+B}$ | A + B |
| 0 | 0 | 1 | 0 | $\overline{A}$ + B | $A\overline{B}$ minus 1 | $\overline{AB}$ | A + $\overline{B}$ |
| 0 | 0 | 1 | 1 | Logic 1 | minus 1 | Logic 0 | minus 1 |
| 0 | 1 | 0 | 0 | $\overline{A+B}$ | A plus (A + $\overline{B}$) | $\overline{AB}$ | A plus $A\overline{B}$ |
| 0 | 1 | 0 | 1 | $\overline{B}$ | AB plus (A + $\overline{B}$) | $\overline{B}$ | (A + B) plus $A\overline{B}$ |
| 0 | 1 | 1 | 0 | $\overline{A \oplus B}$ | A minus B minus 1 | A ⊕ B | A minus B minus 1 |
| 0 | 1 | 1 | 1 | A + $\overline{B}$ | A + $\overline{B}$ | $A\overline{B}$ | $A\overline{B}$ minus 1 |
| 1 | 0 | 0 | 0 | $\overline{AB}$ | A plus (A + B) | $\overline{A}$ + B | A plus AB |
| 1 | 0 | 0 | 1 | A ⊕ B | A plus B | $\overline{A \oplus B}$ | A plus B |
| 1 | 0 | 1 | 0 | B | $A\overline{B}$ plus (A + B) | B | (A + $\overline{B}$) plus AB |
| 1 | 0 | 1 | 1 | A + B | A + B | AB | AB minus 1 |
| 1 | 1 | 0 | 0 | Logic 0 | A plus A | Logic 1 | A plus A |
| 1 | 1 | 0 | 1 | $A\overline{B}$ | AB plus A | A + $\overline{B}$ | (A + B) plus A |
| 1 | 1 | 1 | 0 | AB | $A\overline{B}$ plus A | A + B | (A + $\overline{B}$) plus A |
| 1 | 1 | 1 | 1 | A | A | A | A minus 1 |

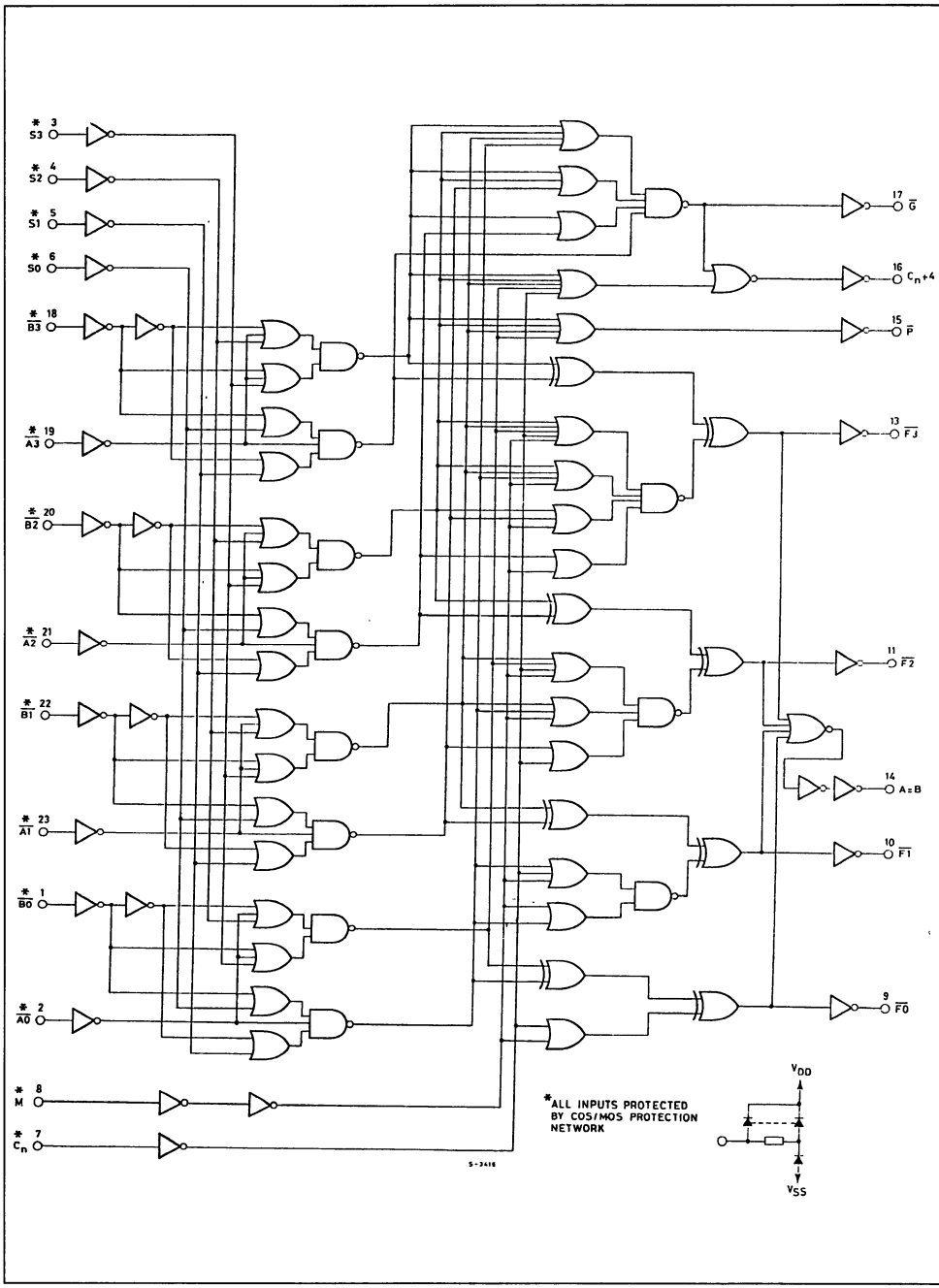
* Expressed as two's complement. For arithmetic function with $C_n$ in the opposite state, the resulting function is as show plus 1.
1 = HIGH LEVEL.
0 = LOW LEVEL.

**Table 2 :** Magnitude Comparison.

| Active-high Data | | | Active-low Data | | |
|---|---|---|---|---|---|
| Input $C_n$ | Output $C_{n+4}$ | Magnitude | Input $C_n$ | Output $C_{n+4}$ | Magnitude |
| 1 | 1 | A ≤ B | 0 | 0 | A ≤ B |
| 0 | 1 | A < B | 1 | 0 | A < B |
| 1 | 0 | A > B | 0 | 1 | A > B |
| 0 | 0 | A ≥ B | 1 | 1 | A ≥ B |

1 = HIGH LEVEL
0 = LOW LEVEL

## LOGIC DIAGRAM Active-low Data



## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2.5V min with $V_{DD}$ = 15V.

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall time = 20ns)

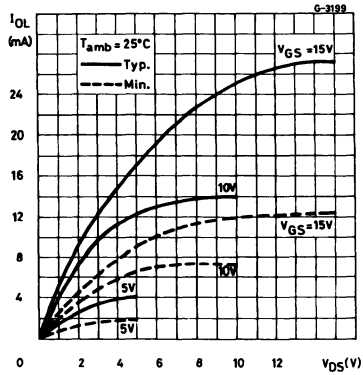
| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time A or B to F (logic mode) A or B to G or P | | 5 | | 400 | 800 | ns |
| | | | 10 | | 160 | 320 | |
| | | | 15 | | 120 | 240 | |
| | A or B to F, $C_{n+4}$, or A = B | | 5 | | 300 | 1000 | ns |
| | | | 10 | | 200 | 400 | |
| | | | 15 | | 140 | 280 | |
| | $C_n$ to F | | 5 | | 320 | 640 | ns |
| | | | 10 | | 135 | 270 | |
| | | | 15 | | 100 | 200 | |
| | $C_n$ to $C_{n+4}$ | | 5 | | 200 | 400 | ns |
| | | | 10 | | 100 | 200 | |
| | | | 15 | | 70 | 140 | |
| $t_{TLH}$, $t_{THL}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

**Table 3 :** AC Test Setup Reference (active-low data).

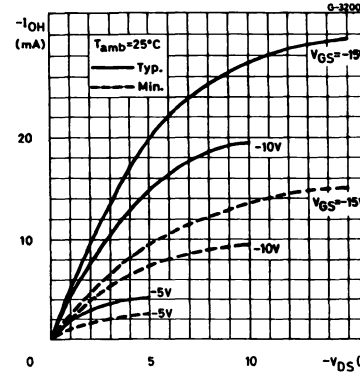
| Test Delay Times | AC Paths | | DC Data Inputs | | Mode* |
|---|---|---|---|---|---|
| | Inputs | Outputs | to $V_{SS}$ | to $V_{DD}$ | |
| $SUM_{IN}$ to $SUM_{OUT}$ | $\overline{BO}$ | Any $\overline{F}$ | $\overline{B1}$, $\overline{B2}$, $\overline{B3}$, M, $C_n$ | All $\overline{A}$'s | ADD |
| $SUM_{IN}$ to P | $\overline{AO}$ | $\overline{P}$ | $\overline{A1}$, $\overline{A2}$, $\overline{A3}$, M, $C_n$ | All $\overline{B}$'s | ADD |
| $SUM_{IN}$ to $\overline{G}$ | $\overline{BO}$ | $\overline{G}$ | All $\overline{A}$'s M, $C_n$ | $\overline{B1}$, $\overline{B2}$, $\overline{B3}$ | ADD |
| $SUM_{IN}$ to $C_{n+4}$ | $\overline{BO}$ | $C_{n+4}$ | All $\overline{A}$'s, M, $C_n$ | $\overline{B1}$, $\overline{B2}$, $\overline{B3}$ | ADD |
| $C_n$ to $SUM_{OUT}$ | $C_n$ | Any $\overline{F}$ | All $\overline{A}$'s, M | All $\overline{B}$'s | ADD |
| $C_n$ to $C_{n+4}$ | $C_n$ | $C_{n+4}$ | All $\overline{A}$'s, M | All $\overline{B}$'s | ADD |
| $SUM_{IN}$ to A = B | $\overline{BO}$ | A = B | All A's B1, B2, B3, M | $C_n$ | SUBTRACT |
| $SUM_{IN}$ to $SUM_{OUT}$ (logic mode) | All $\overline{B}$'s | Any $\overline{F}$ | All $\overline{A}$'s, $C_n$ | M | EXCLUSIVE OR |

* ADD Mode . S0, S3 = $V_{DD}$ ; S1, S2 = $V_{SS}$ SUBTRACT Mode · S0, S3 = $V_{SS}$ , S1, S2 = $V_{DD}$.

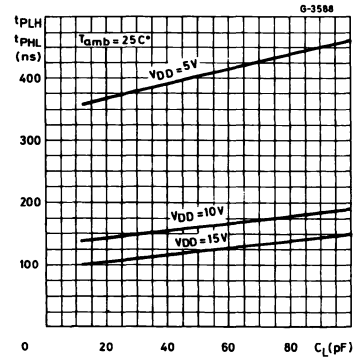
Output Low (sink) Current Characteristics.



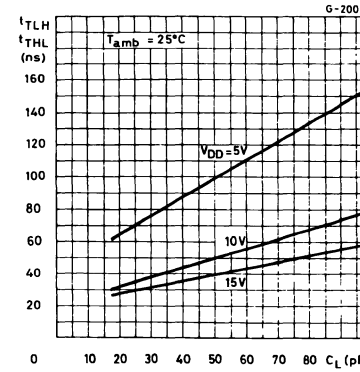

Output High (source) Current Characteristics.



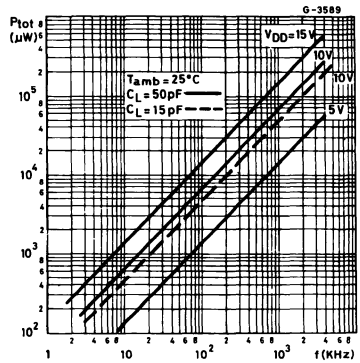

Typical Propagation Delay Time vs. Load Capacitance (for A or B to F, logic mode).




Typical Transition Time vs. Load Capacitance.

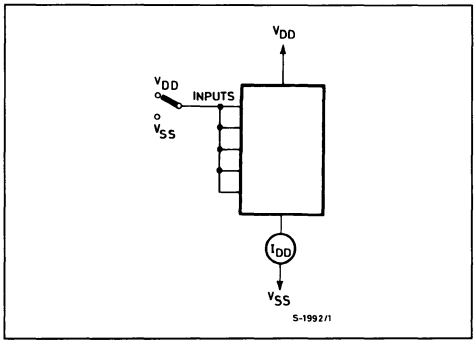



Typical Dynamic Power Dissipation vs. Input Frequency.

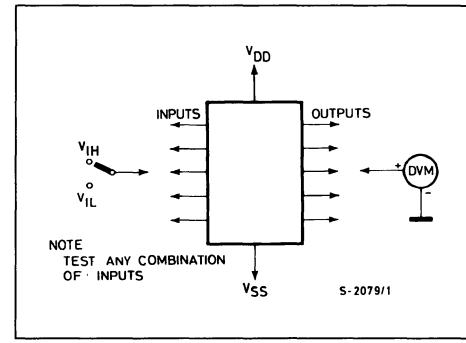


## TEST CIRCUITS

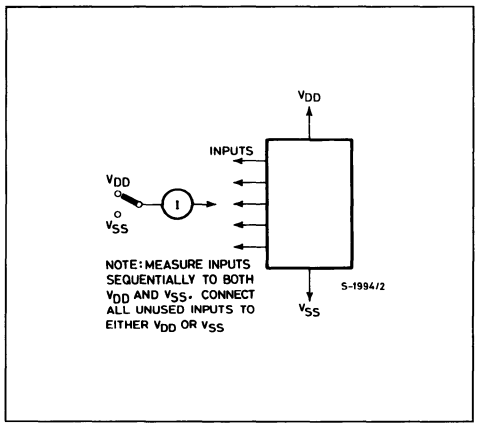
Quiescent Device Current.



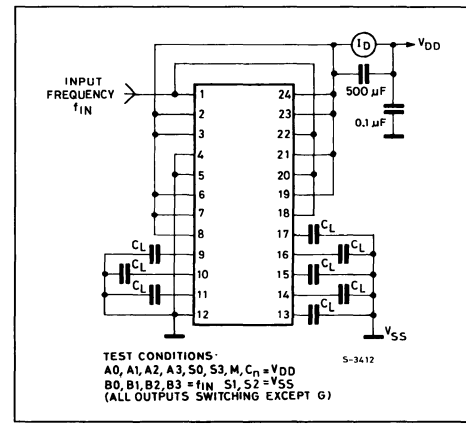

Input Voltage.




Input Leakage Current.



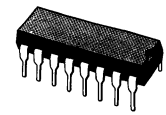

Dynamic Power Dissipation.



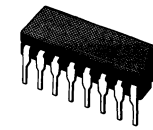
# HCC/HCF40182B

## LOOK-AHEAD CARRY GENERATOR

- GENERATES HIGH-SPEED CARRY ACROSS FOUR ADDERS OF ADDER GROUPS
- HIGH-SPEED OPERATIONAL : $t_{PHL} = t_{PLH} =$ 100ns (typ.) @ $V_{DD} = 10V$
- CASCADABLE FOR FAST CARRIES OVER N BITS
- DESIGNED FOR USE WITH **HCC/HCF40181B** ALU
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED AT 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

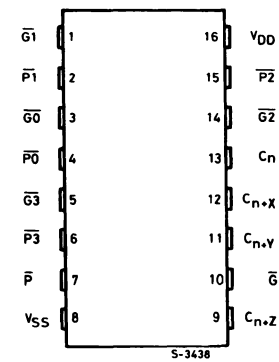
**ORDER CODES :**

| | |
|---|---|
| HCC40182BF | HCF40182BM1 |
| HCF40182BEY | HCF40182BC1 |

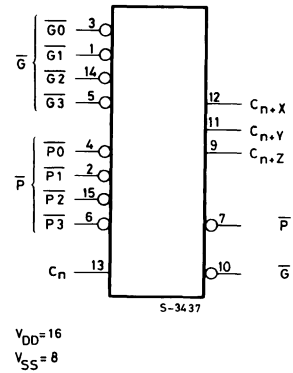
### DESCRIPTION

The **HCC40182B** (extended temperature range) and **HCF40182B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF40182B** is a high-speed look-ahead carry generator capable of anticipating a carry across four binary adders or groups of adders. The **HCC/HCF40182B** is cascadable to perform full look-ahead across n-bit adders. Carry, propagate-carry, and generate-carry functions are provided as enumerated in the terminal designation below. The **HCC/HCF40182B**, when used in conjunction with the **HCC/HCF40181B** arithmetic logic unit (ALU), provides full high-speed look-ahead carry capability for up to n-bit words. Each **HCC/HCF40182B** generates the look-ahead (anticipated carry) across a group of four ALU's. In addition, other **HCC/HCF40182B**'s may be employed to anticipate the carry across sections of four look-ahead blocks up to n-bits. Carry inputs and outputs of the **HCC/HCF40181B** are active-high logic, and carry-generate (G) and carry-propagate (P) outputs are active low. Therefore the inputs and outputs of the **HCC/HCF40182B** are compatible. The **HCC/HCF40182B** is similar to industry type MC14582.

### PIN CONNECTIONS



## FUNCTIONAL DIAGRAM




## TERMINAL DESIGNATIONS TABLE

| Pin Name | Pin | Function |
|---|---|---|
| $\overline{G0}$, $\overline{G1}$, $\overline{G2}$, $\overline{G3}$ | 3, 1, 14, 5 | Active-low Carry-generate Inputs |
| $\overline{P0}$, $\overline{P1}$, $\overline{P2}$, $\overline{P3}$ | 4, 2, 15, 6 | Active-low Carry-propagate Inputs |
| $C_n$ | 13 | Active-high Carry Input |
| $C_{n+X}$, $C_{n+Y}$, $C_{n+Z}$ | 12, 11, 9 | Active-high Carry Outputs |
| $\overline{G}$ | 10 | Active-low Group Carry-generate Output |
| $\overline{P}$ | 7 | Active-low Group Carry-propagate Output |

## ABSOLUTE MAXIMUM RATINGS

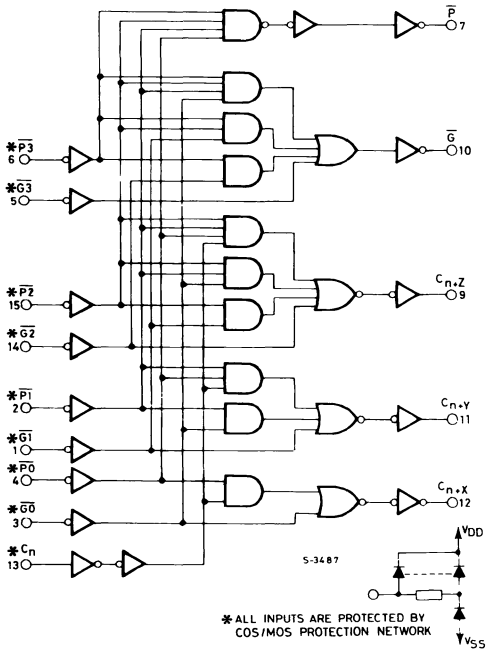
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltages are with respect to $V_{SS}$ (GND).

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAM




**Logic Equations :**

$Cn + X = G0 + P0 \cdot Cn$

$C_{n+Y} = G1 + P1 \cdot G0 + P1 \cdot P0 \cdot C_n$

$C_{n+Z} = G2 + P2 \cdot G1 + P2 \cdot P1 \cdot G0 + P2 \cdot P1 \cdot P0 \cdot C_n$

$\overline{G} = \overline{G3 + P3 \cdot G2 + P3 \cdot P2 \cdot G1 + P3 \cdot P2 \cdot P1 \cdot G0}$

$\overline{P} = \overline{P3 \cdot P2 \cdot P1 \cdot P0}$

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

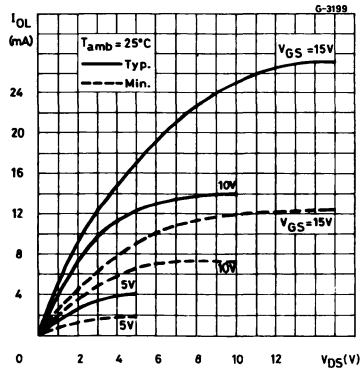
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | 5 | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | 10 | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | 15 | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $±10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $±10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.

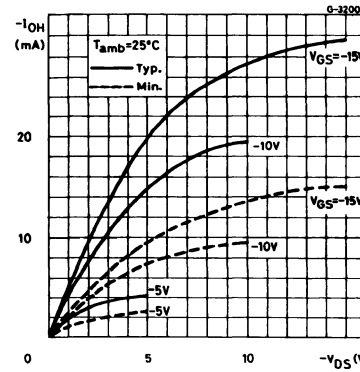
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall time = 20ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$ $t_{PLH}$, | Propagation Delay Time P, G, in to P G Out and Carry Outs | | 5 | | 200 | 400 | ns |
| | | | 10 | | 100 | 200 | |
| | | | 15 | | 75 | 150 | |
| | $C_n$ to Carry Outs | | 5 | | 240 | 480 | ns |
| | | | 10 | | 120 | 240 | |
| | | | 15 | | 90 | 180 | |
| $t_{THL}$ $t_{TLH}$, | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

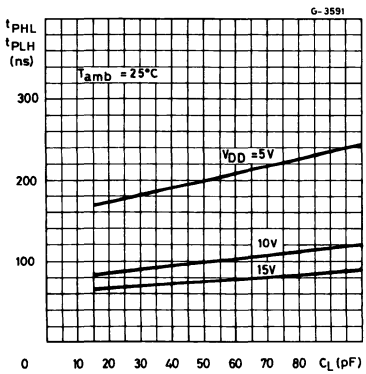
Output Low (sink) Current Characteristics.



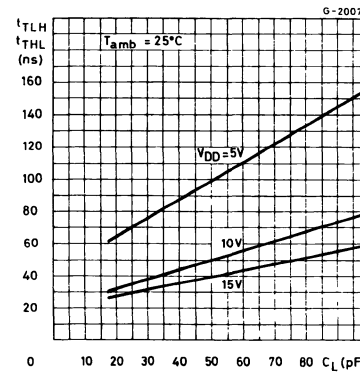

Output High (source) Current Characteristics.



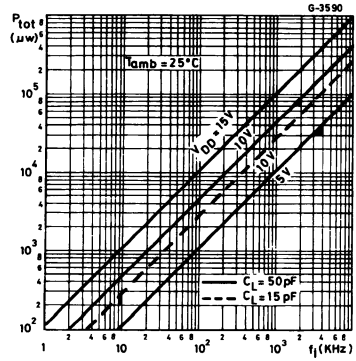

Typical Propagation Delay Time (P, G In to P, G Out and Carry-outs) vs. Load Capacitance.




Typical Transition Time vs. Load Capacitance.

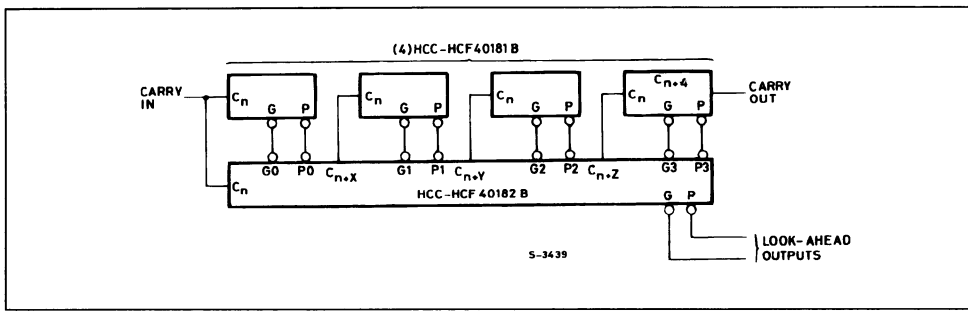


Typical Dynamic Power Dissipation vs. Input Frequency.

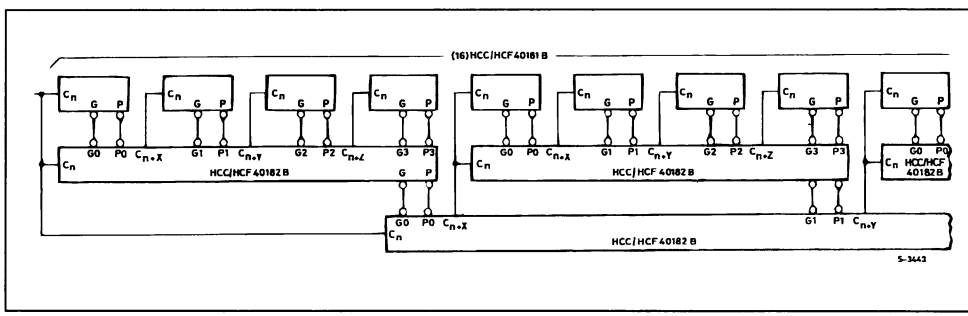



## TYPICAL APPLICATIONS

16-BIT TWO-LEVEL LOOK-AHEAD ALU

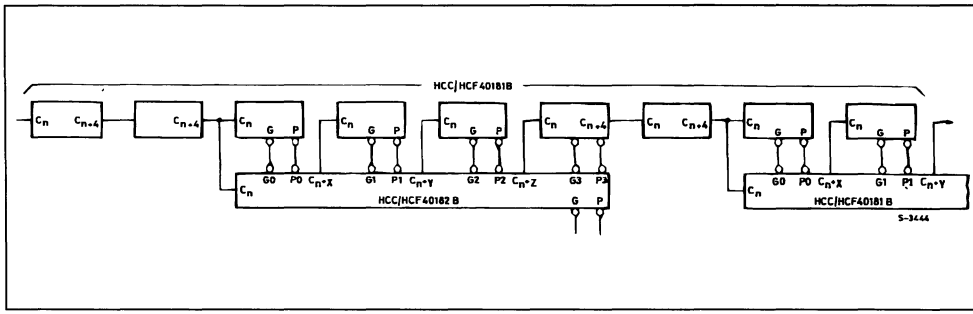



64-BIT FULL CARRY LOOK-AHEAD ALU IN 3 LEVELS



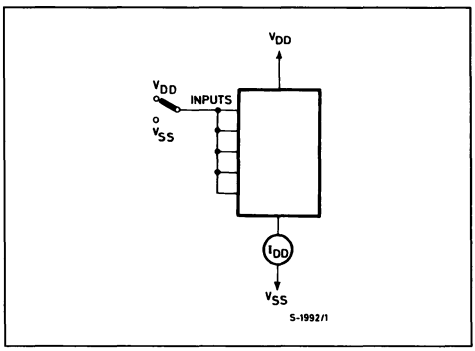
## TYPICAL APPLICATIONS (continued)

COMBINED TWO-LEVEL LOOK-AHEAD AND RIPPLE-CARRY ALU

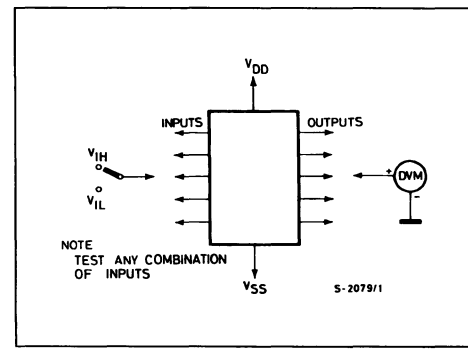



## TEST CIRCUITS

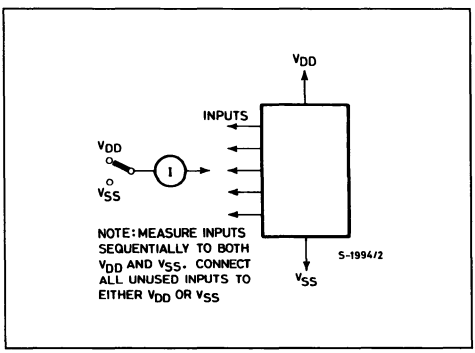
Quiescent Device Current.



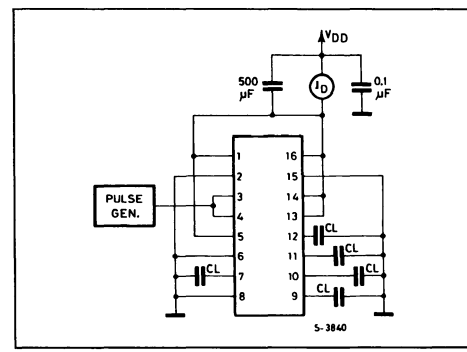

Input Voltage.




Input Leakage Current.



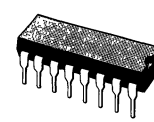

Dynamic Power Dissipation.



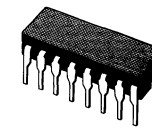
# HCC/HCF40192B
# HCC/HCF40193B

## PRESETTABLE UP/DOWN COUNTERS (DUAL CLOCK WITH RESET) 40192B – BCD TYPE 40193B – BINARY TYPE

- INDIVIDUAL CLOCK LINES FOR COUNTING UP OR COUNTING DOWN
- SYNCHRONOUS HIGH-SPEED CARRY AND BORROW PROPAGATION DELAYS FOR CASCADING
- ASYNCHRONOUS RESET AND PRESET CAPABILITY
- MEDIUM-SPEED OPERATION - $f_{CL}$ = 8MHz (typ.) @ 10V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)

**M1**
(Chip Carrier)

**C1**
(Plastic Chip Carrier)

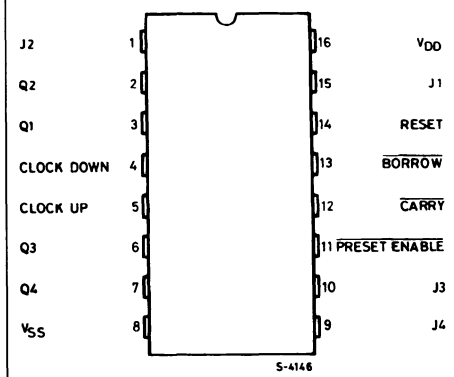
**ORDER CODES :**

HCC401XXBF HCF401XXBM1
HCF401XXBEY HCF401XXBC1

### DESCRIPTION

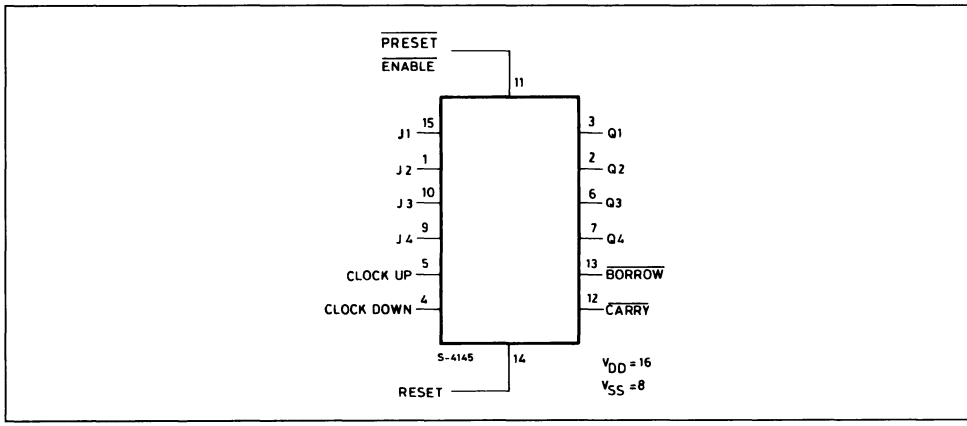
The **HCC40192B, HCC40193B**, (extended temperature range) and the **HCF40192B, HCF40193B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and platic micro package. The **HCC/HCF40192B** Presettable BCD Up/Down Counter and the **HCC/HCF40193B** Presettable Binary Up/Down Counter each consist of 4 synchronously clocked, gated "D" type flip-flops connected as a counter. The inputs consist of 4 individual jam lines, a PRESET ENABLE control, individual CLOCK UP and CLOCK DOWN signals and a master RESET. Four buffered Q signal outputs as well as CARRY and BORROW outputs for multiple-stage counting schemes are provided. The counter is cleared so that all outputs are in a low state by a high on the RESET line. A RESET is accomplished asynchronously with the clock. Each output is individually programmable asynchronously with the clock to the level on the corresponding jam input when the PRESET ENABLE control is low. The counter counts up one count on the positive clock edge of the CLOCK UP signal provided the CLOCK DOWN line is high. The counter counts down one count on the positive clock edge of the CLOCK DOWN signal provided the CLOCK UP line

### PIN CONNECTIONS



is high. The $\overline{\text{CARRY}}$ and $\overline{\text{BORROW}}$ signals are high when the counter is counting up or down. The CARRY signal goes low one-half clock cycle after the counter reaches its maximum count in the count-up mode. The $\overline{\text{BORROW}}$ signal goes low one-half clock cycle after the counter reaches its minimum count in the count-down mode. Cascading of multiple packages is easily accomplished without the need for additional external circuitry by tying the $\overline{\text{BORROW}}$ and $\overline{\text{CARRY}}$ outputs to the CLOCK DOWN and CLOCK UP inputs, respectively, of the succeeding package.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

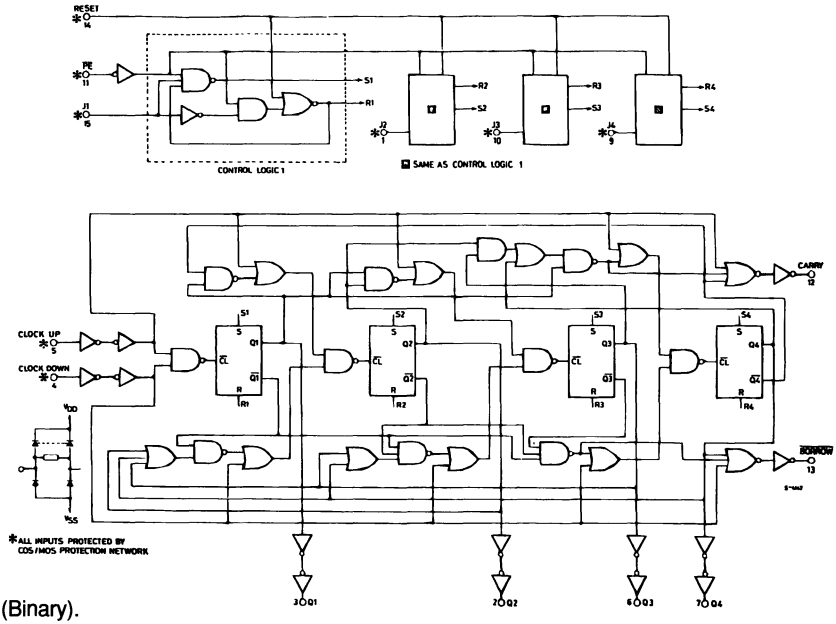
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltages are with respect to $V_{SS}$ (GND).

## RECOMMENDED OPERATING CONDITIONS

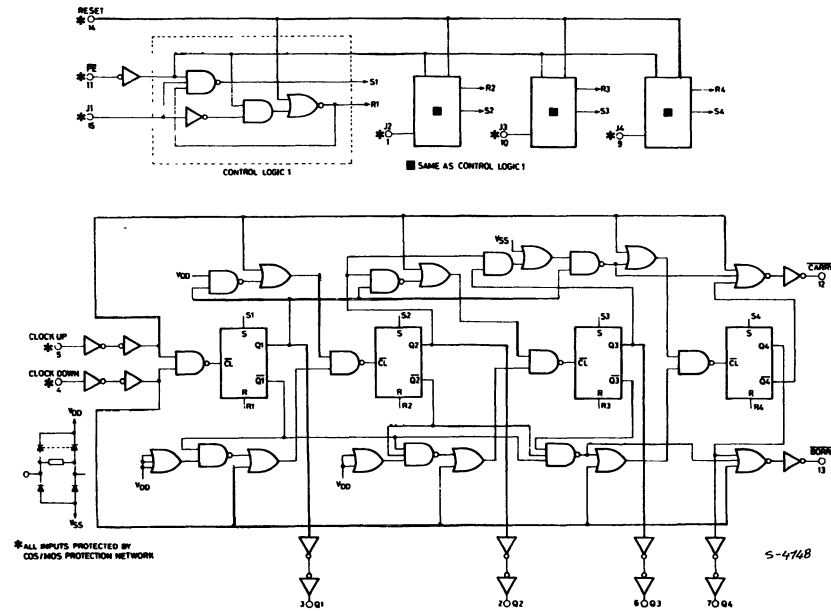
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAMS

**40192B** (BCD).

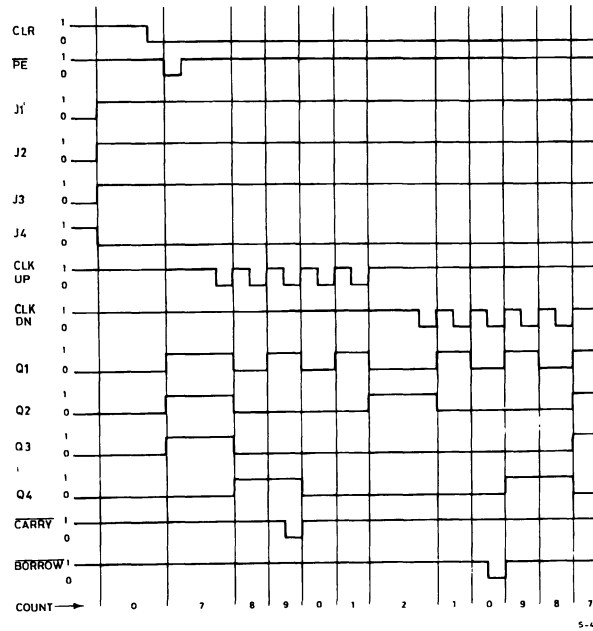



**40193B** (Binary).

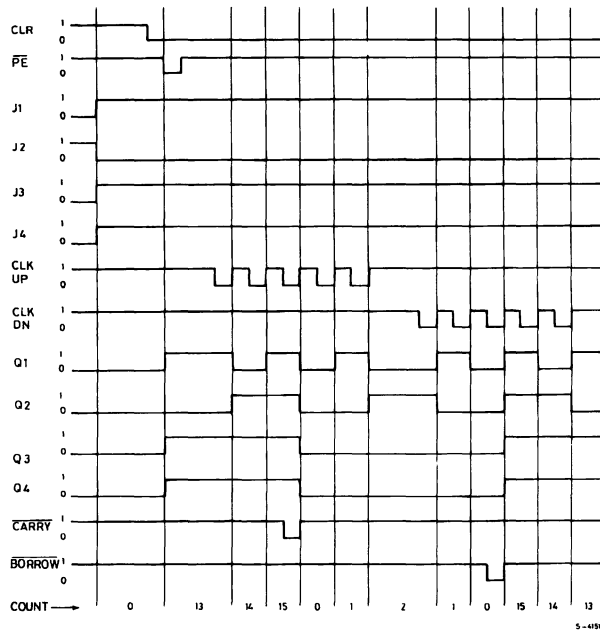


## TIMING DIAGRAMS

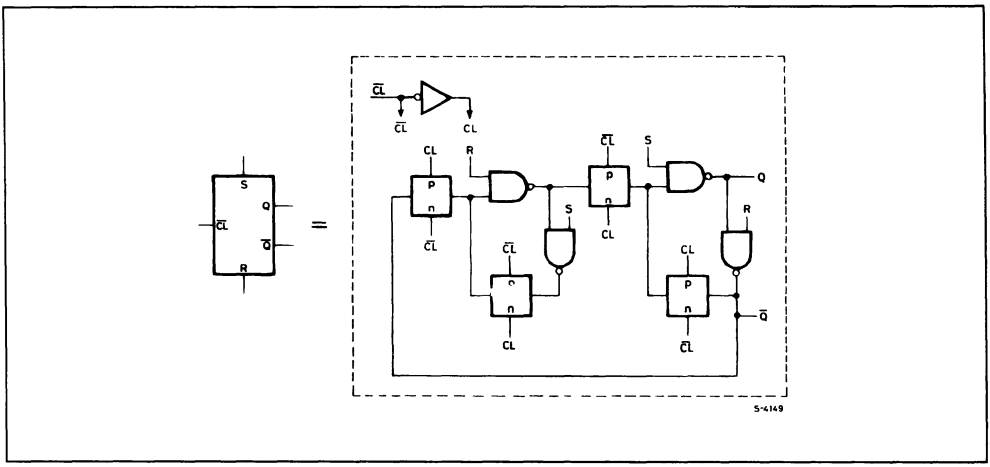
**40192B** (BCD).




**40193B** (Binary).



Internal Logic of Flip-flop.




## TRUTH TABLE

| Clock Up | Clock Down | Preset Enable | Reset | Action |
|---|---|---|---|---|
| _/‾ | 1 | 1 | 0 | Count Up |
| ‾_ | 1 | 1 | 0 | No Count |
| 1 | _/‾ | 1 | 0 | Count Down |
| 1 | ‾_ | 1 | 0 | No Count |
| X | X | 0 | 0 | Preset |
| X | X | X | 1 | Reset |

1 = High Level 0 = Low Level X = Don't Care.

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | |
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9 95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0 05 | | | 0 05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1 5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2 5 | | 5 | – 2 | | – 1.6 | – 3.2 | | – 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | – 0.64 | | – 0.51 | – 1 | | – 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | – 1.6 | | – 1.3 | – 2.6 | | – 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | – 4.2 | | – 3.4 | – 6.8 | | – 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | – 1.53 | | – 1.36 | – 3.2 | | – 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | – 0.52 | | – 0.44 | – 1 | | – 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | – 1.3 | | – 1.1 | – 2.6 | | – 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | – 3.6 | | – 3.0 | – 6.8 | | – 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0 3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

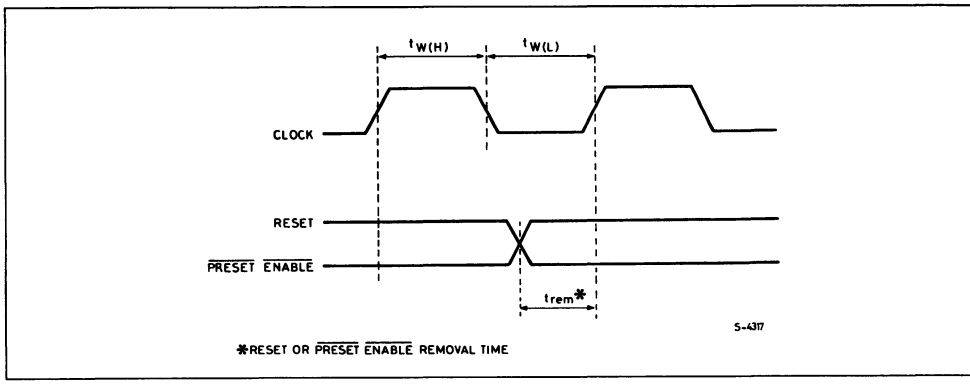
* $T_{Low}$ = – 55°C for **HCC** device – 40°C for **HCF** device
* $T_{High}$ = + 125°C for **HCC** device + 85°C for **HCF** device
The Noise Margin for both "1" and "0" level is 1V min with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2.5V min with $V_{DD}$ = 15V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall time = 20ns)

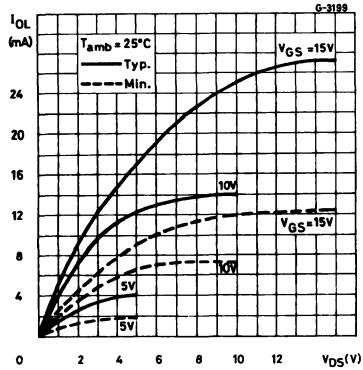
| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time<br>Clock Up or Clock Down to Q<br>Reset to Q | | 5 | | 250 | 500 | ns |
| | | | 10 | | 120 | 240 | |
| | | | 15 | | 90 | 180 | |
| | $\overline{PE}$ to Q | | 5 | | 200 | 400 | ns |
| | | | 10 | | 100 | 200 | |
| | | | 15 | | 70 | 140 | |
| | Clock Up to $\overline{Carry}$<br>Clock Down to $\overline{Borrow}$ | | 5 | | 160 | 320 | ns |
| | | | 10 | | 80 | 160 | |
| | | | 15 | | 60 | 120 | |
| | $\overline{Reset}$ or $\overline{PR}$ to $\overline{Borrow}$ or $\overline{Carry}$ | | 5 | | 300 | 600 | ns |
| | | | 10 | | 150 | 300 | |
| | | | 15 | | 110 | 220 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_{rem}$* | Removal Time<br>Reset or $\overline{PE}$ | | 5 | 80 | 40 | | ns |
| | | | 10 | 40 | 20 | | |
| | | | 15 | 30 | 15 | | |
| $t_W$ | Clock Input Pulse Width<br>Reset | | 5 | 480 | 240 | | ns |
| | | | 10 | 300 | 150 | | |
| | | | 15 | 260 | 130 | | |
| | $\overline{PE}$ | | 5 | | 120 | 240 | ns |
| | | | 10 | | 85 | 170 | |
| | | | 15 | | 70 | 140 | |
| | Clock | | 5 | | 90 | 180 | ns |
| | | | 10 | | 45 | 90 | |
| | | | 15 | | 30 | 60 | |
| $t_r$, $t_f$ | Clock Input Rise or Fall Time | | 5 | | | 15 | µs |
| | | | 10 | | | 15 | |
| | | | 15 | | | 5 | |
| $f_{CL}$ | Maximum Clock Input Frequency | | 5 | 2 | 4 | | MHz |
| | | | 10 | 5 | 8 | | |
| | | | 15 | 5.5 | 11 | | |

* The time required for Reset or Preset Enable control to be removed before clocking (see timing diagram).

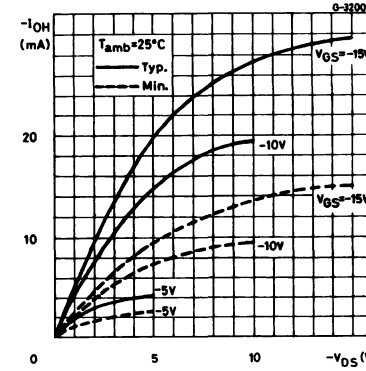
Timing Diagram Defining $t_{rem}$.



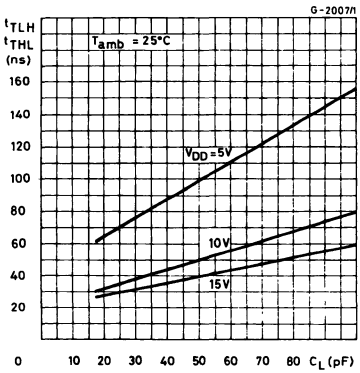

Output Low (sink) Current Characteristics.



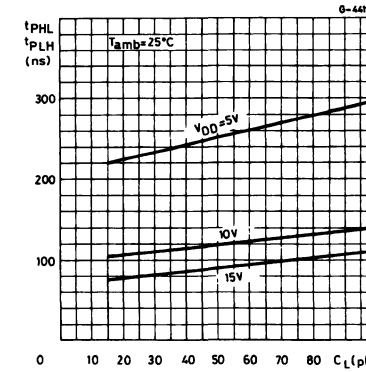

Output high (source) Current Characteristics.



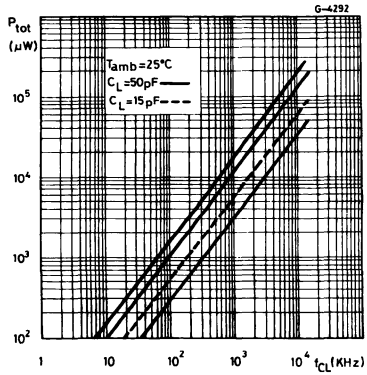

Typical Transition Time vs. Load Capacitance.




Typical Propagation Delay Time vs. Load Capacitance.

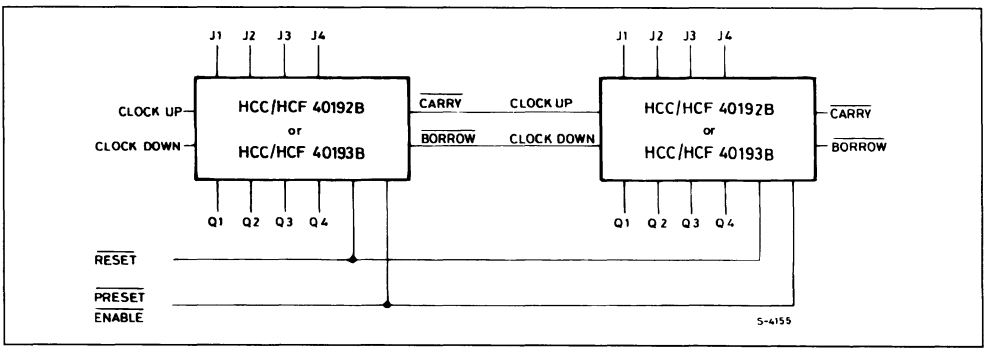


Typical Dynamic Power Dissipation.



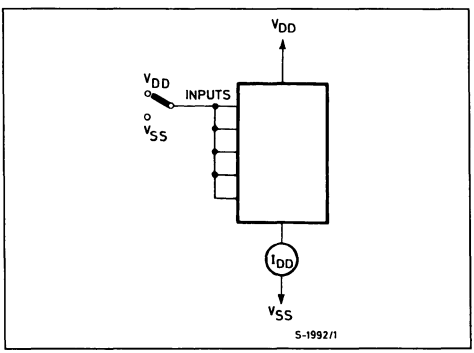

## TYPICAL APPLICATION

CASCADED COUNTER PACKAGES

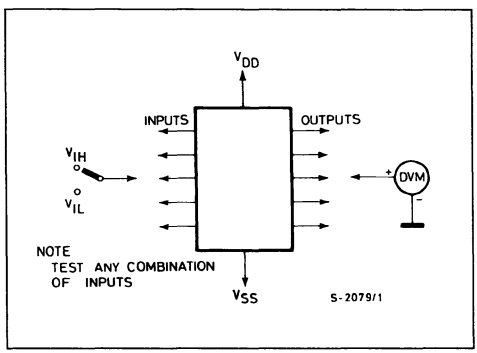



## TEST CIRCUITS

Quiescent Device Current.

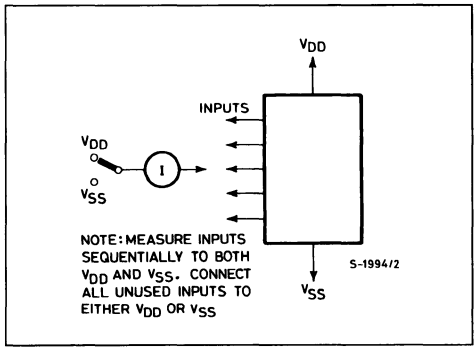



Input Voltage.

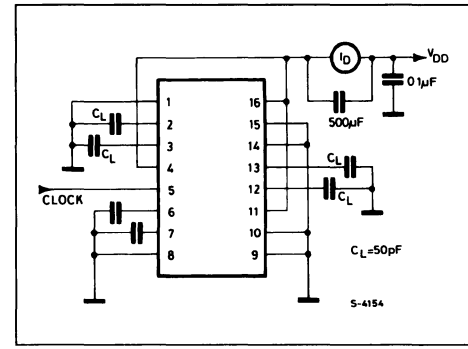


**TEST CIRCUITS** (continued)

Input Leakage Current.




Dynamic Power Dissipation.

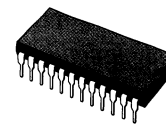


SGS-THOMSON MICROELECTRONICS

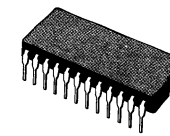
# HCC/HCF40208B

## 4 x 4 MULTIPORT REGISTER

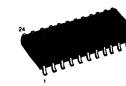
- FOUR 4-BIT REGISTERS
- ONE INPUT AND TWO OUTPUT BUSES
- UNLIMITED EXPANSION IN BIT AND WORD DIRECTIONS
- DATA LINES HAVE LATCHED INPUTS
- 3-STATE OUTPUTS
- SEPARATE CONTROL OF EACH BUS, ALLOWING SIMULTANEOUS INDEPENDENT READING OF ANY OF FOUR REGISTERS ON BUS A AND BUS B AND INDEPENDENT WRITING INTO ANY OF THE FOUR REGISTERS
- 40108B IS PIN-COMPATIBLE WITH INDUSTRY TYPE MC14580
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED AT 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**BEY**
(Plastic Package)



**BF**
(Ceramic Frit Seal Package)



**BM1**
(Micro Package)

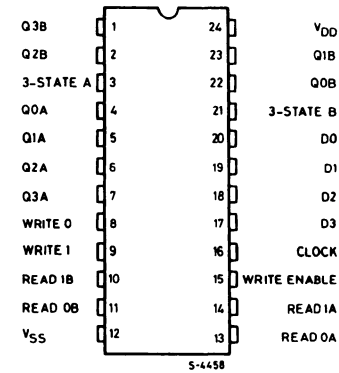
**ORDER CODES :**

HCC40208BF HCF40208BEY
HCF40208BM1

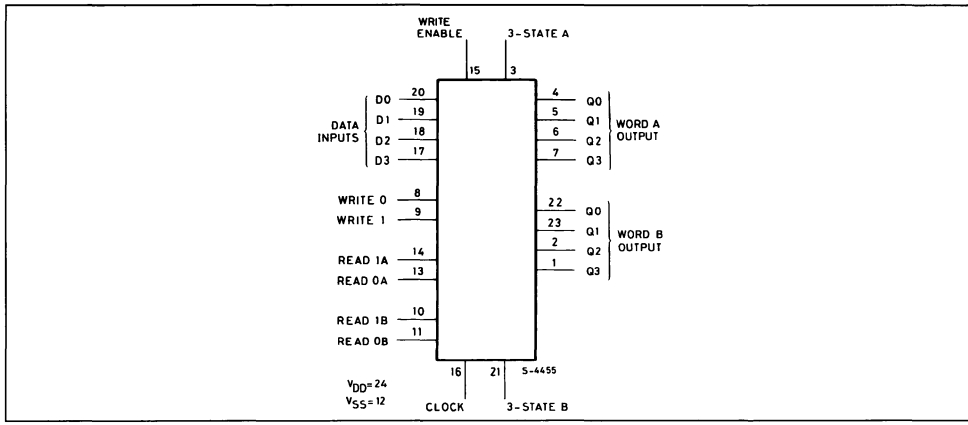
### DESCRIPTION

The HCC40208B (extended temperature range) and HCF40208B (intermediate temperature range) are monolithic integrated circuits, available in 24-lead dual in-line plastic or ceramic package and plastic micro package. The HCC/HCF40208B is a 4 x 4 multiport register containing four 4-bit registers, write address decoder, two separate read address decoders, and two 3-state output buses. When the ENABLE input is low, the corresponding output bus is switched, independently of the clock to a high-impedance state. The high-impedance third state provides the outputs with the capability of being connected to the bus lines in a bus-organized system without the need for interface or pull-up components. When the WRITE ENABLE input is high, all data input lines are latched on the positive transition of the CLOCK and the data is entered into the word selected by the write address lines. When WRITE ENABLE is low, the CLOCK is inhibited and no new data is entered. In either case, the contents of any word may be accessed via the read address lines independent of the state of the CLOCK input.

### PIN CONNECTIONS



## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

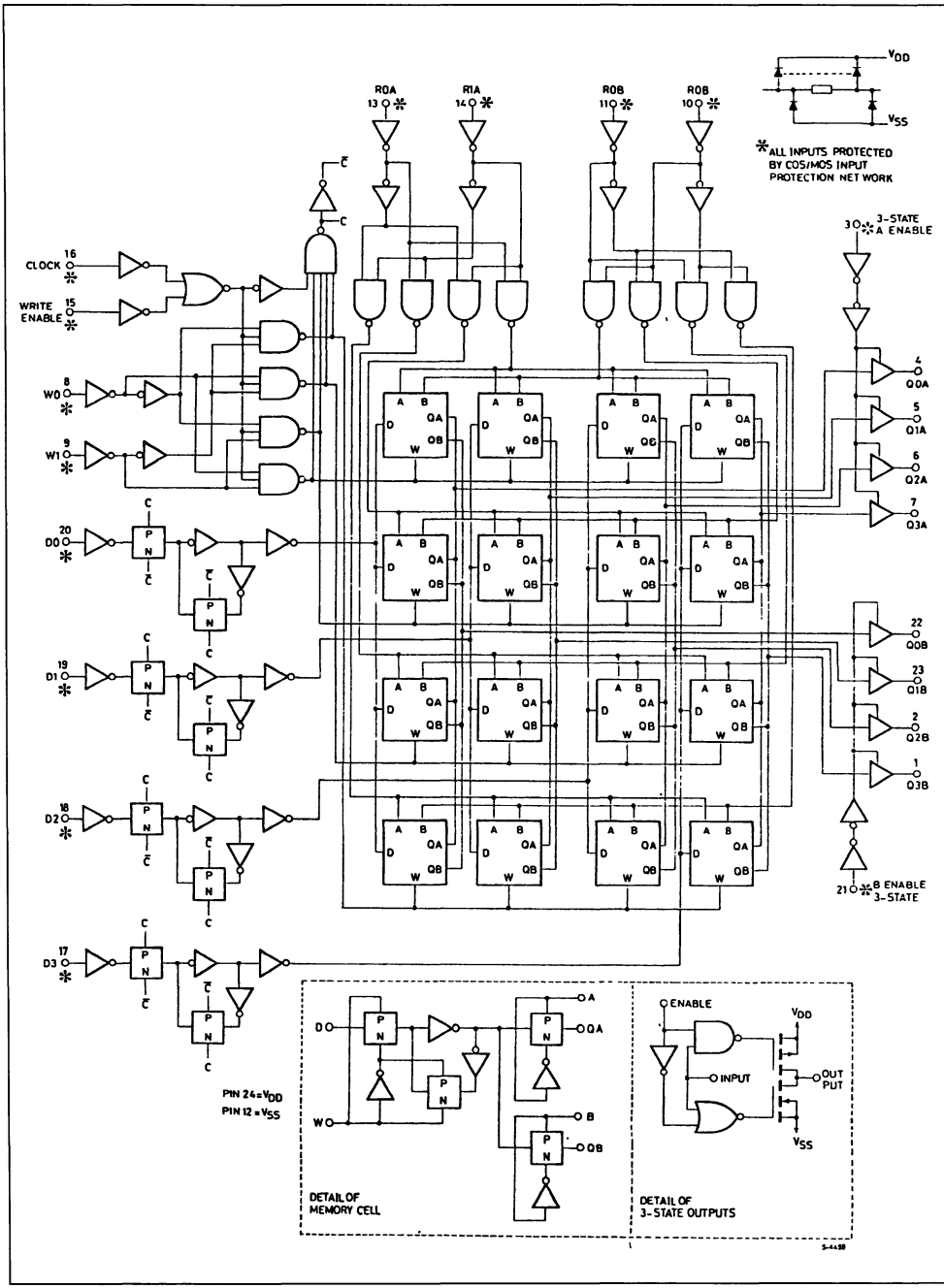
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltages are with respect to $V_{SS}$ (GND)

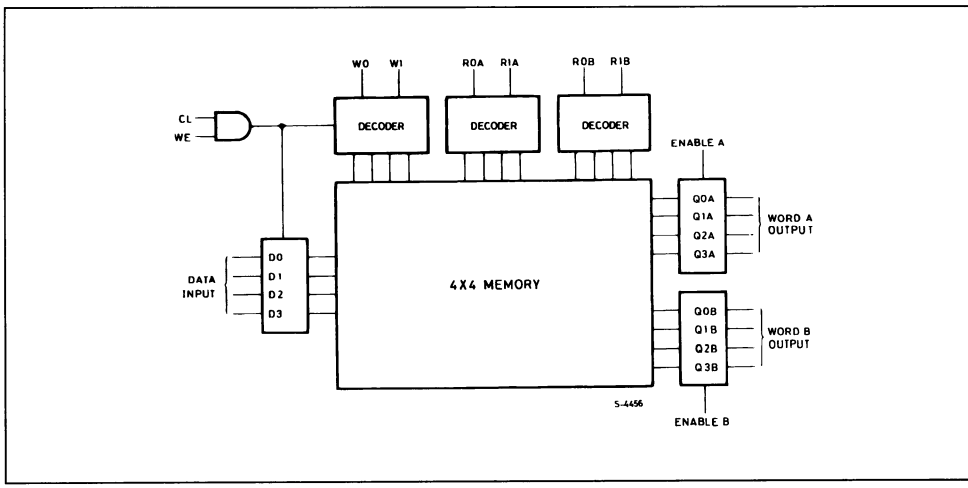
## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

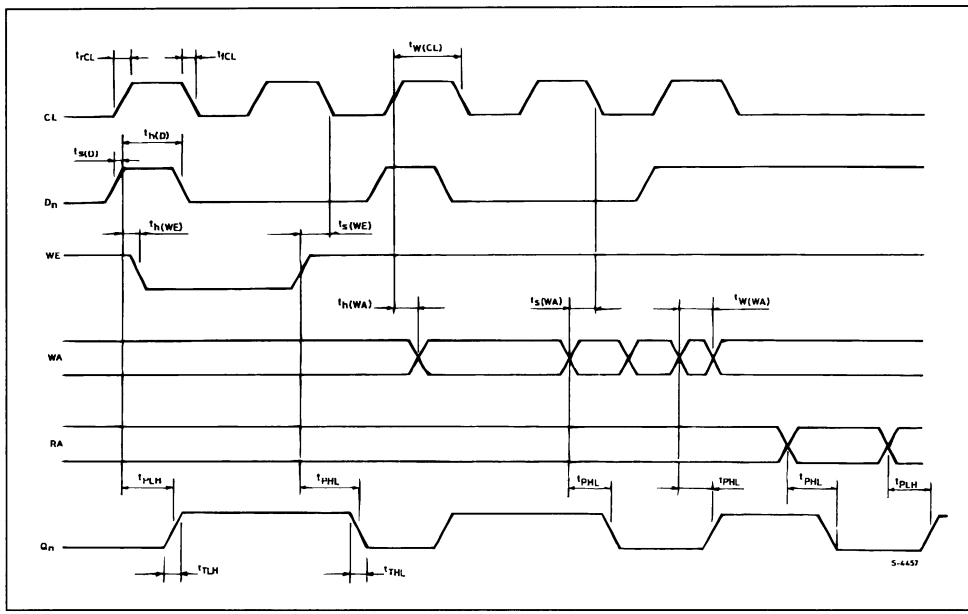
## SCHEMATIC DIAGRAM



## LOGIC DIAGRAM




## TIMING DIAGRAM



## TRUTH TABLE

| Clock | Write Enable | Write 1 | Write 0 | Read 1A | Read 0A | Read 1B | Read 0B | Enable A | Enable B | $D_n$ | $Q_{nA}$ | $Q_{nB}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ⎍ | 1 | S1 | S2 | S1 | S2 | S1 | S2 | 1 | 1 | 1 | 1 | 1 |
| ⎍ | 1 | S1 | S2 | S1 | S2 | S1 | S2 | 1 | 1 | 0 | 0 | 0 |
| X | X | X | X | X | X | X | X | 0 | 0 | X | Z | Z |
| ⎍ | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | $D_n$ to Word 0 | Word 1 Out | Word 2 Out |
| ⎍ | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | Word 0 Not Altered | Word 1 Out | Word 2 Out |
| X | X | X | X | 1 | 0 | 0 | 1 | 1 | 1 | X | Word 2 Out | Word 1 Out |
| ⎍ | X | X | X | X | X | X | X | 1 | 1 | X | NC | NC |

1 = HIGH LEVEL, 0 = LOW LEVEL, X = DON'T CARE, Z = HIGH IMPEDANCE.
S1 and S2 refer to input strates of either 1 or 0.

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions• $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | − 2 | | − 1.6 | − 3.2 | | − 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | − 0.64 | | − 0.51 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.6 | | − 1.3 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 4.2 | | − 3.4 | − 6.8 | | − 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | − 1.53 | | − 1.36 | − 3.2 | | − 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | − 0.52 | | − 0.44 | − 1 | | − 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | − 1.3 | | − 1.1 | − 2.6 | | − 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | − 3.6 | | − 3.0 | − 6.8 | | − 2.4 | | |

* $T_{Low}$ = − 55°C for **HCC** device : − 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.
** Forced output disable.

## STATIC ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $I_{OH}$,$I_{OL}$** | 3-State Output Leakage Current | HCC Types | 0/18 | 0/18 | | 18 | | ± 0.4 | | $\pm 10^{-4}$ | ± 0.4 | | ± 12 | μA |
| | | HCF Types | 0/15 | 0/15 | | 15 | | ± 1.0 | | $\pm 10^{-4}$ | ± 1.0 | | ± 7.5 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = – 55°C for **HCC** device : – 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is . 1V min. with $V_{DD}$ = 5V, 2V min with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.
** Forced output disable.

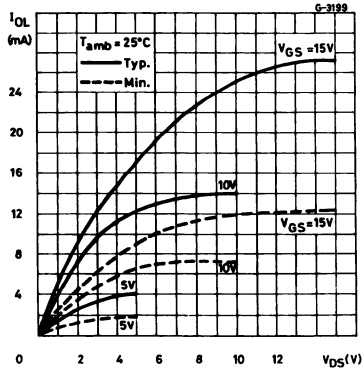
## DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall time = 20ns)

| Symbol | Parameter | Test Conditions | $V_{DD}$ (V) | Value Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time : Clock to Write Enable to Q | | 5 | | 360 | 720 | ns |
| | | | 10 | | 140 | 280 | |
| | | | 15 | | 100 | 200 | |
| | Read or Write Address to Q | | 5 | | 300 | 600 | ns |
| | | | 10 | | 120 | 240 | |
| | | | 15 | | 85 | 170 | |
| $t_{PZH}$, $t_{PHZ}$ | 3-state Disable Delay Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_{PZL}$, $t_{PLZ}$ | 3-State Disable Delay time | | 5 | | 130 | 260 | ns |
| | | | 10 | | 60 | 120 | |
| | | | 15 | | 50 | 100 | |
| $t_{THL}$, $t_{TLH}$ | Output Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_{setup}$ | Setup Time Data to Clock $t_{s\,(D)}$ | | 5 | 0 | – 95 | | ns |
| | | | 10 | 0 | – 35 | | |
| | | | 15 | 0 | – 20 | | |
| | Write Enable to $\overline{Clock}$ $t_{s(WE)}$ | | 5 | 250 | 125 | | ns |
| | | | 10 | 100 | 50 | | |
| | | | 15 | 70 | 35 | | |
| | Write Address to $\overline{Clock}$ $t_{s\,(WA)}$ | | 5 | 250 | 125 | | ns |
| | | | 10 | 100 | 50 | | |
| | | | 15 | 70 | 35 | | |

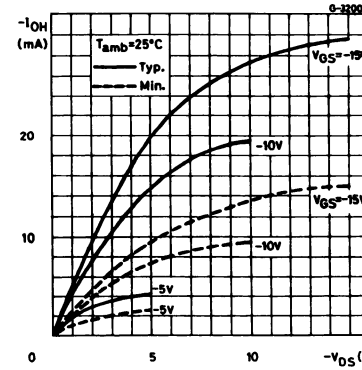
## DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_r$, $t_f$ | Clock Rise and Fall Time | | 5 | | | 15 | µs |
| | | | 10 | | | 5 | |
| | | | 15 | | | 5 | |
| $t_{hold}$ | Hold Time<br>Data to Clock $t_{h(D)}$ | | 5 | 220 | 110 | | ns |
| | | | 10 | 100 | 50 | | |
| | | | 15 | 80 | 40 | | |
| | Write Enable to Clock $t_{h(WE)}$ | | 5 | 270 | 135 | | ns |
| | | | 10 | 130 | 65 | | |
| | | | 15 | 80 | 40 | | |
| | Write Address to $\overline{Clock}$ $t_{s(WA)}$ | | 5 | 330 | 165 | | |
| | | | 10 | 140 | 70 | | |
| | | | 15 | 90 | 45 | | |
| $t_W$ | Clock Pulse Width<br>Clock or Write Enable $t_{W(CL)}$ | | 5 | 350 | 175 | | ns |
| | | | 10 | 130 | 65 | | |
| | | | 15 | 90 | 45 | | |
| | Write Address $t_{W(WA)}$ | | 5 | 300 | 150 | | ns |
| | | | 10 | 150 | 75 | | |
| | | | 15 | 90 | 45 | | |
| $f_{CL}$ | Maximum Clock Input Frequency | | 5 | 1.5 | 3 | | MHz |
| | | | 10 | 3.5 | 7 | | |
| | | | 15 | 4.5 | 9 | | |

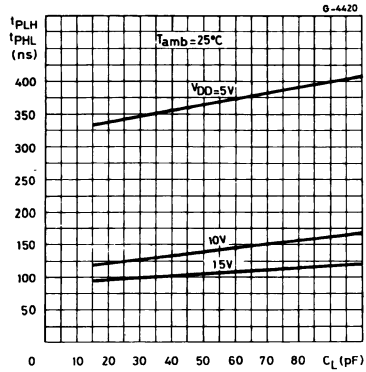
Output Low (sink) Current Characteristics.



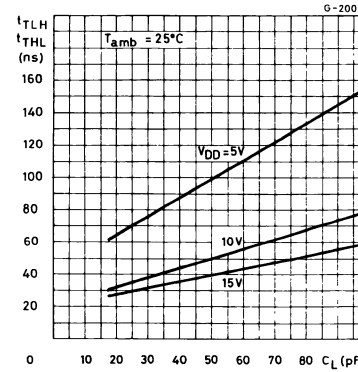

Output High (source) Current Characteristics.



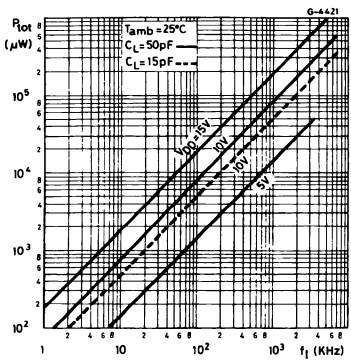
Typical Propagation Delay Time vs. Load Capacitance (CL or WE to Q).




Typical Transition Time vs. Load Capacitance.

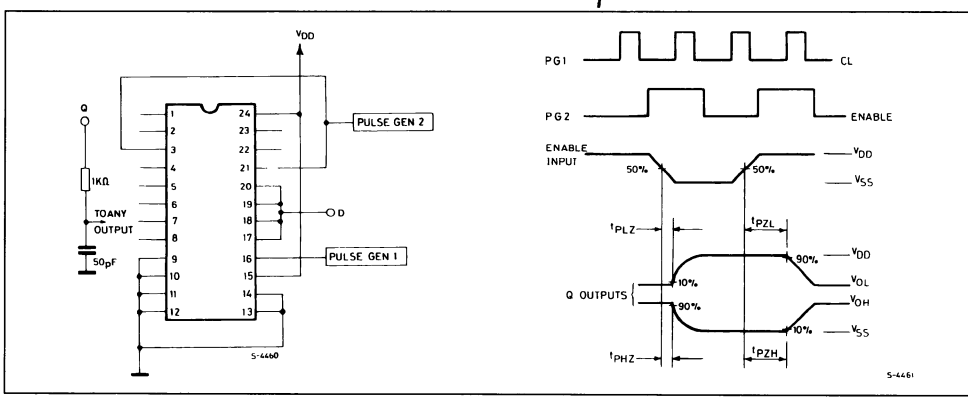



Typical Dynamic Power Dissipation vs. Input Frequency.

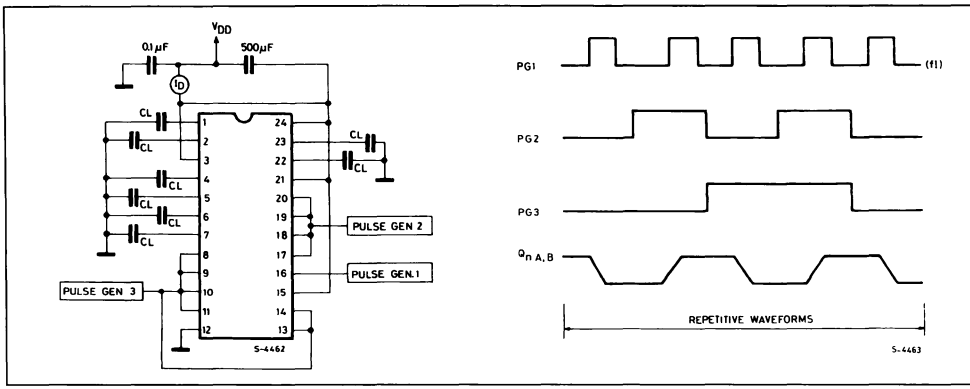



## TEST CIRCUITS

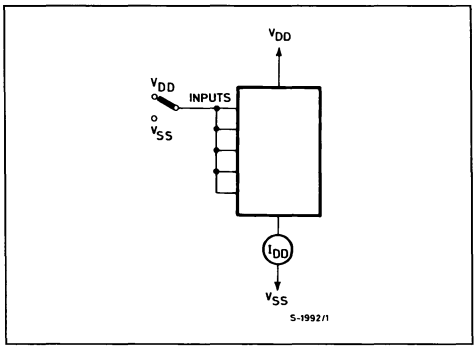
Output-enable-delay-times and Waveforms.



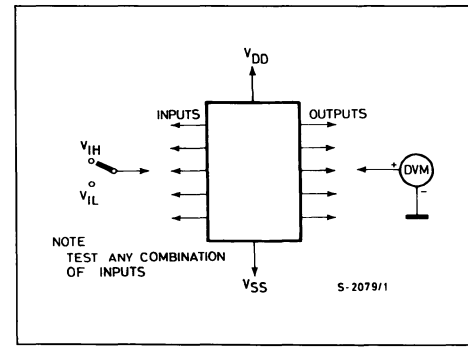
Power-dissipation and Waveforms.



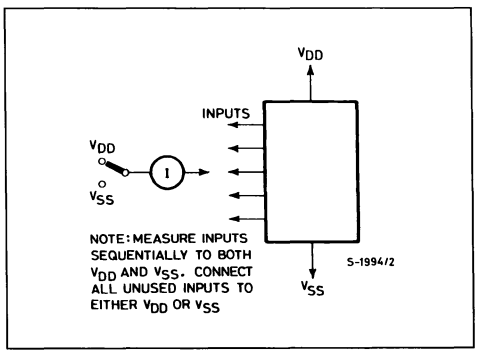

Quiescent Device Current.




Input Voltage.

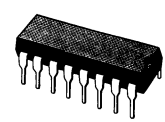



Input Current.

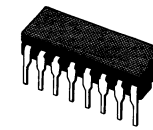


# QUAD 2-LINE-TO-1-LINE DATA SELECTOR/MULTIPLEXER

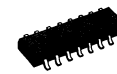
- 3-STATE OUTPUTS
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Frit Seal Package)



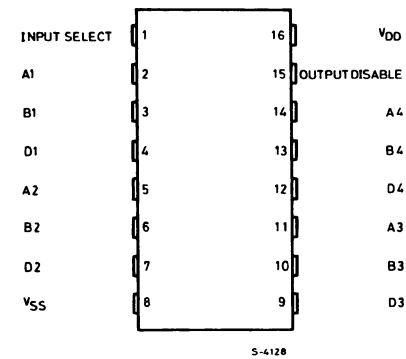
**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

HCC40257BF HCF40257BM1
HCF40257BEY HCF40257BC1

**PIN CONNECTIONS**

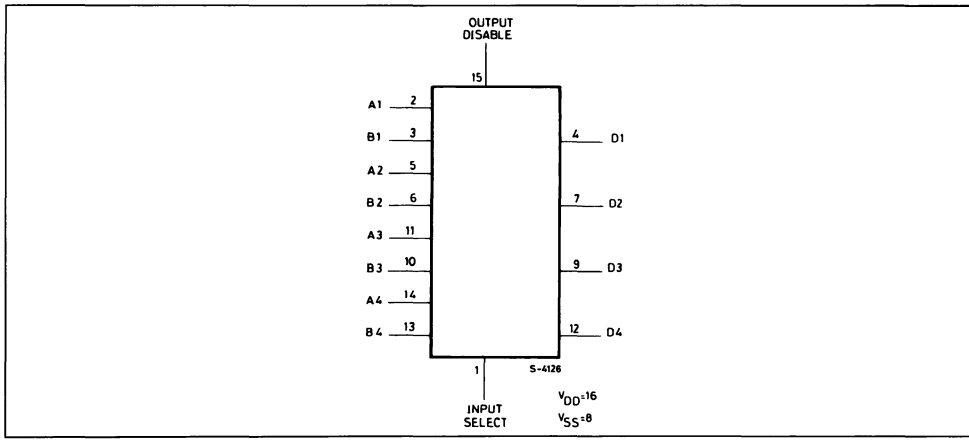



## DESCRIPTION

The **HCC40257B** (extended temperature range) and **HCF40257B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and plastic micro package.

The **HCC/HCF40257B** is a Data Selector/Multiplexer featuring three-state outputs which can interface directly with and drive data lines of bus-oriented systems.

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

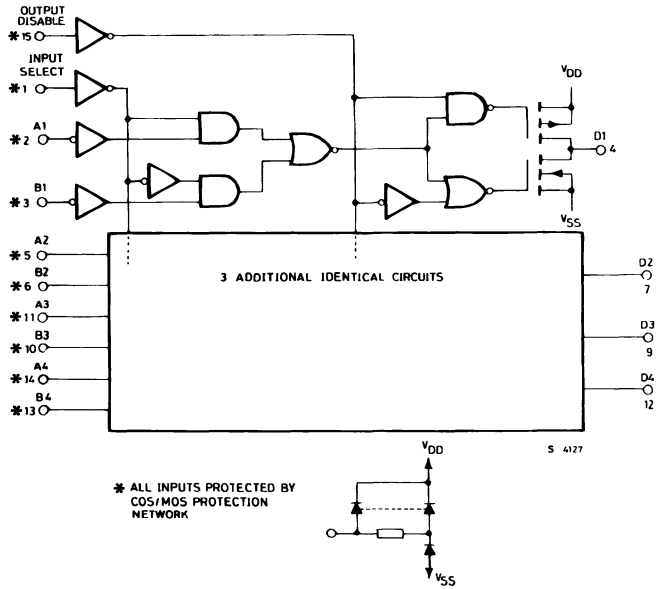
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | − 0.5 to + 20<br>− 0.5 to + 18 | V<br>V |
| $V_I$ | Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
* All voltages are with respect to $V_{SS}$ (GND).

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | − 55 to + 125<br>− 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAM




## TRUTH TABLE

| Inputs | | | | Output |
|---|---|---|---|---|
| 3-State Output Disable | Select | A | B | D |
| 1 | X | X | X | Z |
| 0 | 0 | 0 | X | 0 |
| 0 | 0 | 1 | X | 1 |
| 0 | 1 | X | 0 | 0 |
| 0 | 1 | X | 1 | 1 |

X = Don't Care
Logic 1 = High
Logic 0 = Low
Z = High impedance.

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

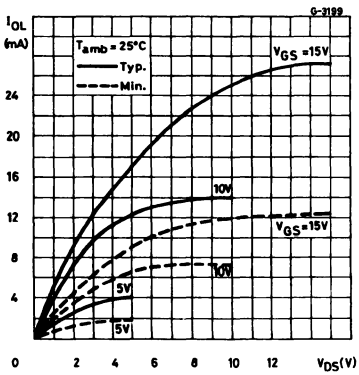
| Symbol | Parameter | | Test Conditions $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (μA) | $V_{DD}$ (V) | Value $T_{Low}$* Min. | $T_{Low}$* Max. | 25°C Min. | 25°C Typ. | 25°C Max. | $T_{High}$* Min. | $T_{High}$* Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 1 | | 0.02 | 1 | | 30 | μA |
| | | | 0/10 | | | 10 | | 2 | | 0.02 | 2 | | 60 | |
| | | | 0/15 | | | 15 | | 4 | | 0.02 | 4 | | 120 | |
| | | | 0/20 | | | 20 | | 20 | | 0.04 | 20 | | 600 | |
| | | HCF Types | 0/ 5 | | | 5 | | 4 | | 0.02 | 4 | | 30 | |
| | | | 0/10 | | | 10 | | 8 | | 0.02 | 8 | | 60 | |
| | | | 0/15 | | | 15 | | 16 | | 0.02 | 16 | | 120 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/10 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | | 0/ 5 | 2.5 | | 5 | – 2 | | – 1.6 | – 3.2 | | – 1.15 | | mA |
| | | HCC Types | 0/ 5 | 4.6 | | 5 | – 0.64 | | – 0.51 | – 1 | | – 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | – 1.6 | | – 1.3 | – 2.6 | | – 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | – 4.2 | | – 3.4 | – 6.8 | | – 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | – 1.53 | | – 1.36 | – 3.2 | | – 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | – 0.52 | | – 0.44 | – 1 | | – 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | – 1.3 | | – 1.1 | – 2.6 | | – 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | – 3.6 | | – 3.0 | – 6.8 | | – 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $I_{OH}$, $I_{OL}$** | 3-State Output Leakage Current | HCC Types | 0/18 | 0/18 | | 18 | | ± 0.4 | | $\pm 10^{-4}$ | ± 0.4 | | ± 12 | μA |
| | | HCF Types | 0/18 | 0/18 | | 18 | | ± 1.0 | | $\pm 10^{-4}$ | ± 1.0 | | 7.5 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = – 55°C for **HCC** device . – 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5V min. with $V_{DD}$ = 15V.
** Forced output disable.

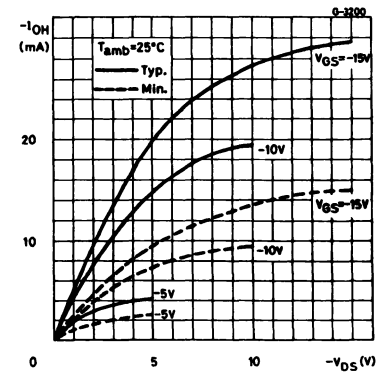
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3%/°C, all input rise and fall time = 20ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time Data Input to Output | | 5 | | 150 | 300 | ns |
| | | | 10 | | 70 | 140 | |
| | | | 15 | | 50 | 100 | |
| | Select to Output | | 5 | | 190 | 380 | ns |
| | | | 10 | | 85 | 170 | |
| | | | 15 | | 65 | 130 | |
| | Output Disable to Output | | 5 | | 95 | 190 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_{THL}$ $t_{TLH}$, | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |

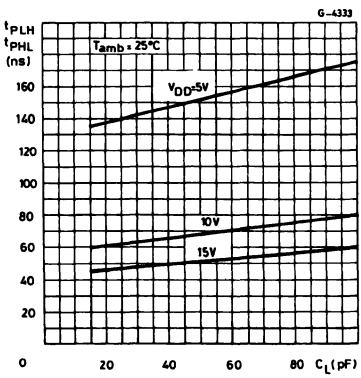
Output Low (sink) Current Characteristics.



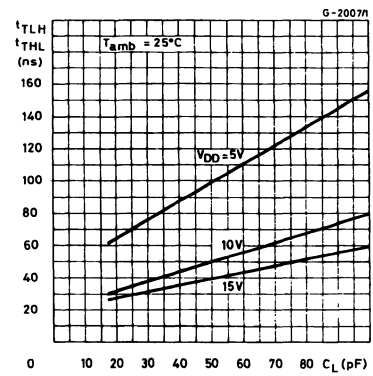

Output High (source) Current Characteristics.



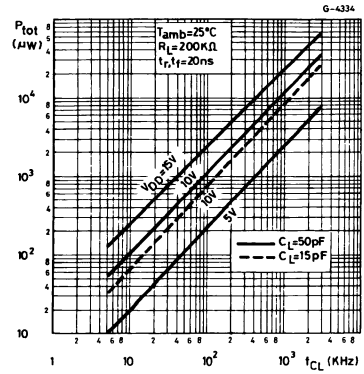

Typical Propagation Delay Time vs. Load Capacitance (Data Input to Output).




Typical Transition Time vs. Load Capacitance.

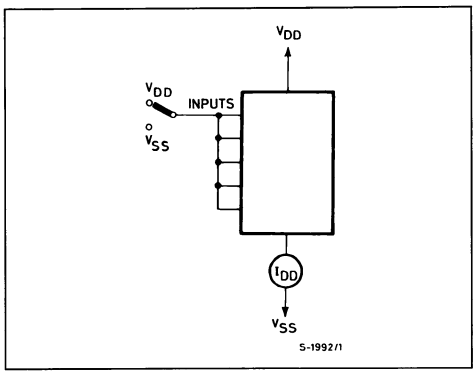


Typical Dynamic Power Dissipation vs. Input Frequency (one input to one output).

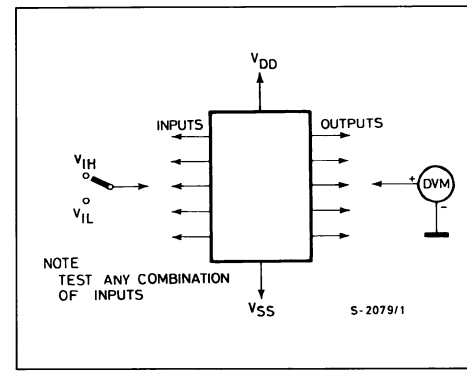



## TEST CIRCUITS

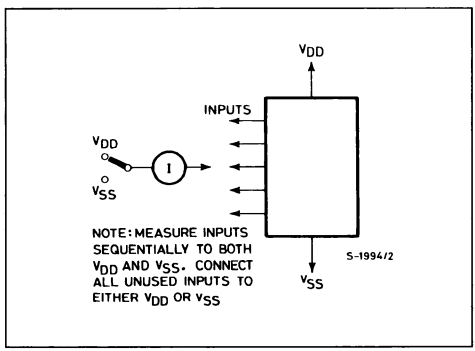
Quiescent Device Current.




Input Voltage.




Input Leakage Current.



# 4 X 4 CROSSPOINT SWITCH WITH CONTROL MEMORY

- LOW ON RESISTANCE – 75 Ω TYP. AT $V_{DD}$ = 12 V
- "BUILT-IN" CONTROL LATCHES
- LARGE ANALOG SIGNAL CAPABILITY ± $V_{DD}$/2
- TRANSMITS SIGNALS UP TO 10 MHz
- MATCHED SWITCH CHARACTERISTICS $\Delta R_{ON}$ = 18 Ω TYP. AT $V_{DD}$ – $V_{SS}$ = 12 V.
- HIGH LINEARITY : – 0.5 % DISTORTION (typ.) AT f = 1 KHz, $V_{IN}$ = 5 V PEAK TO PEAK, $V_{DD}$ - $V_{SS}$ = 10 V, $R_L$ = 10 KΩ
- STANDARD COS/MOS NOISE IMMUNITY
- 100 % TESTED FOR QUIESCENT CURRENT

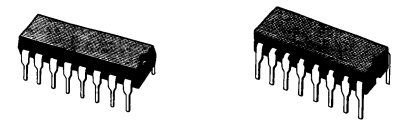
## DESCRIPTION

The M22100 combines a 4 x 4 array of crosspoints (transmission gates) with a 4-line-to-16-line decoder and 16 latch circuits. Any one of the sixteen transmission gates (crosspoints) can be selected by applying the appropriate four line address. The selected transmission gate can be turned on or off by applying a logical one or zero, respectively, to the data input and strobing the strobe input to a logical one. Any number of the transmission gates can be ON simultaneously.

When the required operating power is applied to the 22100, the states of the 16 switches are indeterminate.

Therefore, all switches must be turned off by putting the strobe high and data-in-low, and then addressing all switches in succession.

The device is available in 16 lead dual in-line plastic or ceramic package.

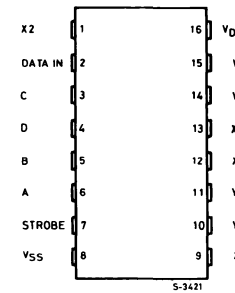


**EY** (Plastic Package) **F** (Ceramic Package)

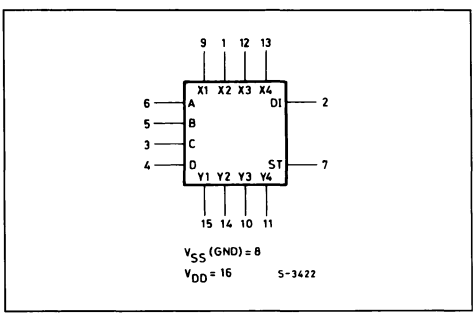
**ORDER CODES :**

M22100 B1 M22100 F1

## PIN CONNECTIONS




## FUNCTIONAL DIAGRAM




## TRUTH TABLE

| Address | | | | Select | | Address | | | | Select | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | B | C | D | | | A | B | C | D | | |
| 0 | 0 | 0 | 0 | X1 | Y1 | 0 | 0 | 0 | 1 | X1 | Y3 |
| 1 | 0 | 0 | 0 | X2 | Y1 | 1 | 0 | 0 | 1 | X2 | Y3 |
| 0 | 1 | 0 | 0 | X3 | Y1 | 0 | 1 | 0 | 1 | X3 | Y3 |
| 1 | 1 | 0 | 0 | X4 | Y1 | 1 | 1 | 0 | 1 | X4 | Y3 |
| 0 | 0 | 1 | 0 | X1 | Y2 | 0 | 0 | 1 | 1 | X1 | Y4 |
| 1 | 0 | 1 | 0 | X2 | Y2 | 1 | 0 | 1 | 1 | X2 | Y4 |
| 0 | 1 | 1 | 0 | X3 | Y2 | 0 | 1 | 1 | 1 | X3 | Y4 |
| 1 | 1 | 1 | 0 | X4 | Y2 | 1 | 1 | 1 | 1 | X4 | Y4 |

## ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ * | Supply Voltage: Ceramic Types<br>Plastic Types | -0.5 to +20<br>-0.5 to +18 | V<br>V |
| $V_I$ | Input Voltage | -0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for Top = Full Package Temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature: Ceramic Types<br>Plastic Types | -55 to +125<br>-40 to +85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |

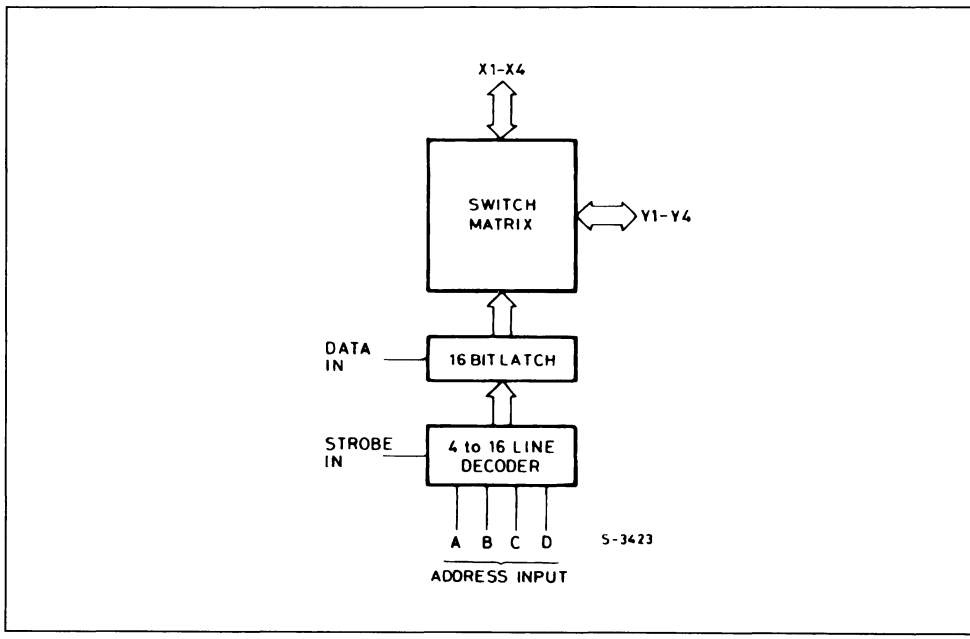
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability

* All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage: Ceramic Types<br>Plastic Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature: Ceramic Types<br>Plastic Types | -55 to +125<br>-40 to +85 | °C<br>°C |

## LOGIC DIAGRAM



## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditios | $V_I$ (V) | $V_{DD}$ (V) | Value $T_{LOW}$ * Min. | $T_{LOW}$ * Max. | 25 °C Min. | 25 °C Typ. | 25 °C Max. | $T_{HIGH}$ * Min. | $T_{HIGH}$ * Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CROSSPOINT** | | | | | | | | | | | | | |
| $I_L$ | Quiescent Supply Current | F1 | | | 5 | | | | 0.04 | 5 | | 150 | µA |
| | | | | | 10 | | | | 0.04 | 10 | | 300 | |
| | | | | | 15 | | | | 0.04 | 20 | | 600 | |
| | | | | | 20 | | | | 0.08 | 100 | | 3000 | |
| | | B1 | | | 5 | | | | 0.04 | 20 | | 150 | |
| | | | | | 10 | | | | 0.04 | 40 | | 300 | |
| | | | | | 15 | | | | 0.04 | 80 | | 600 | |
| $R_{ON}$ | On Resistance | F1 | Any Switch | | 5 | | 450 | | 225 | 1250 | | 1625 | Ω |
| | | | | | 10 | | 135 | | 85 | 180 | | 230 | |
| | | | | | 12 | | 100 | | 75 | 135 | | 175 | |
| | | | | | 15 | | 70 | | 65 | 95 | | 125 | |
| | | B1 | $V_{IS}$ = 0 to $V_{DD}$ | | 5 | | 1000 | | 225 | 1250 | | 1440 | |
| | | | | | 10 | | 145 | | 85 | 180 | | 205 | |
| | | | | | 12 | | 110 | | 75 | 135 | | 155 | |
| | | | | | 15 | | 75 | | 65 | 95 | | 110 | |
| ΔON | Resistance $\Delta R_{ON}$ (Between any two channels) | | | | 5 | | | | 35 | | | | Ω |
| | | | | | 10 | | | | 20 | | | | |
| | | | | | 12 | | | | 18 | | | | |
| | | | | | 15 | | | | 15 | | | | |
| OFF Channel Leakage Current | | F1 | All Switch OFF | 0/18 | 18 | | ±0.1 | | $±10^{-3}$ | ±0.1• | | ±1 | µA |
| | | B1 | | 0/15 | 15 | | ±0.3 | | $±10^{-3}$ | ±0.3 | | ±1 | |
| **CONTROL** | | | | | | | | | | | | | |
| $V_{IL}$ | Input Low Voltage | | OFF Switch $I_L$ < 0.2 µA | | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | | 10 | | 3 | | | 3 | | 3 | |
| | | | | | 15 | | 4 | | | 4 | | 4 | |
| $V_{IH}$ | Input High Voltage | | ON Switch see $R_{ON}$ Characteristics | | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | | 10 | 7 | | 7 | | | 7 | | |
| | | | | | 15 | 11 | | 11 | | | 11 | | |
| $I_I$ | Input Current | F1 | Any Control Input | 0/18 | 18 | | ±0.1 | | $±10^{-5}$ | ±0.1• | | ±1 | µA |
| | | B1 | | 0/15 | 15 | | ±0.3 | | $±10^{-5}$ | ±0.3 | | ±1 | |
| $C_I$ | Input Capacitance | | Any Input | | | | | | 5 | 7.5 | | | pF |

• Determined by minimum feasible leakage measurement for automatic testing

* $T_{LOW}$ = -55 °C for **HCC** device: -40 °C for **HCF** device.

* $T_{HIGH}$ = +125 °C for **HCC** device: +85 °C for **HCF** device.

The Noise Margin for both "1" and "0" level is: 1V min. with $V_{DD}$ = 5 V, 2 V min. with $V_{DD}$ = 10 V, 2.5 V min. with $V_{DD}$ = 15 V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, all input rise and fall times= 20 ns)

| Symbol | Parameter | Test Conditions | | | | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | $f_i$ (KHz) | $R_L$ (KW) | $V_{IS}$ • (V) | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| **CROSSPOINT** | | | | | | | | | | |
| $t_{PHL}$ $t_{PLH}$ | Propagation Delay Time Address or Strobe Inputs to Output | | | 10 | 5 | 5 | | 30 | 60 | ns |
| | | | | | 10 | 10 | | 15 | 30 | |
| | | | | | 15 | 15 | | 10 | 20 | |
| | Frequency Response (Any Switch ON) | | 1 | 1 | 5 | 10 | | 40 | | MHz |
| | | | Sine Wave Input $20\ Log \frac{V_{OS}}{V_{IS}} = -3\ dB$ | | | | | | | |
| | Sine Wave Distortion | | 1 | 1 | 5 | 10 | | 0.5 | | % |
| | Feedthrough (All Switches OFF) | | 1.6 | 1 | 5 | 10 | | 80 | | dB |
| | | | Sine Wave Input | | | | | | | |
| | Frequency for Signal Crosstalk Attenuation of 40 dB | | | 1 | 10 | 10 | | 1.5 | | MHz |
| | | | Sine Wave Input | | | | | | | |
| | Frequency for Signal Crosstalk Attenuation of 110 dB | | | 1 | 10 | 10 | | 0.1 | | KHz |
| | | | Sine Wave Input | | | | | | | |
| C | Capacitance Xn to Ground Yn to Ground Feedthrough | | | | | 5-15 | | 18 30 0.4 | | pF |
| **CONTROLS** | | | | | | | | | | |
| $t_{PHZ}$ | Propagation Delay Time Strobe to Output (Switch Turn-ON to High Level) | $R_L$ = 1 KΩ $C_L$ = 50 pF $t_r$, $t_f$ = 20 ns | | See Figure 1 | | 5 | | 500 | 1000 | ns |
| | | | | | | 10 | | 230 | 460 | |
| | | | | | | 15 | | 145 | 290 | |
| $t_{PZH}$ | Propagation Delay Time Data-In to Output (Switch Turn-ON to High Level) | | | See Figure 2 | | 5 | | 500 | 1000 | ns |
| | | | | | | 10 | | 220 | 440 | |
| | | | | | | 15 | | 135 | 270 | |
| $t_{PZH}$ | Propagation Delay Time Address to Output (Switch Turn-ON to High Level) | | | See Figure 3 | | 5 | | 480 | 960 | ns |
| | | | | | | 10 | | 225 | 450 | |
| | | | | | | 15 | | 150 | 300 | |
| $t_{PHZ}$ | Propagation Delay Time Strobe to Output (Switch Turn-OFF) | | | See Figure 1 | | 5 | | 450 | 900 | ns |
| | | | | | | 10 | | 200 | 400 | |
| | | | | | | 15 | | 165 | 330 | |
| $t_{PZL}$ | Propagation Delay Time Data-In to Output (Switch Turn-ON to Low Level) | | | See Figure 2 | | 5 | | 500 | 1000 | ns |
| | | | | | | 10 | | 220 | 440 | |
| | | | | | | 15 | | 135 | 270 | |
| $t_{PHZ}$ | Propagation Delay Time Address to Output (Switch Turn-OFF) | | | See Figure 3 | | 5 | | 425 | 850 | ns |
| | | | | | | 10 | | 190 | 380 | |
| | | | | | | 15 | | 145 | 290 | |
| $t_{setup}$ | Setup Time Data-In to Strobe, Address | | | | | 5 | | 200 | 400 | ns |
| | | | | | | 10 | | 80 | 160 | |
| | | | | | | 15 | | 50 | 100 | |

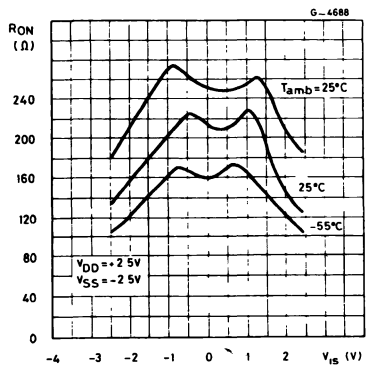
• Peak to peak voltage symmetrical about $V_{DD}/2$

## DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

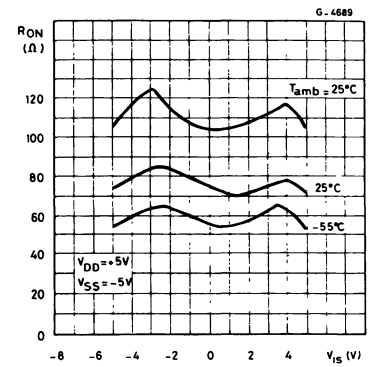
| Symbol | Parameter | Test Conditions | | | | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | $f_i$ (KHz) | $R_L$ (KW) | $V_{IS}$ • (V) | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| **CONTROLS** (continued) | | | | | | | | | | |
| $t_{hold}$ | Hold Time Data-In to Strobe, Address | $R_L$ = 1 KΩ<br>$C_L$ = 50 pF<br>$t_r$, $t_f$ = 20 ns | | | | 5 | | 180 | | ns |
| | | | | | | 10 | | 110 | | |
| | | | | | | 15 | | 35 | | |
| $f\phi$ | Switching Frequency | | | | | 5 | 0.6 | 1.2 | | MHz |
| | | | | | | 10 | 1.6 | 3.2 | | |
| | | | | | | 15 | 2.5 | 5 | | |
| $t_W$ | Strobe Pulse Width | | | | | 5 | | 300 | 600 | ns |
| | | | | | | 10 | | 120 | 240 | |
| | | | | | | 15 | | 90 | 180 | |
| | Control Crosstalk Data-In, Address, or Storbe to Output | | | 10 | 10 | 10 | | 75 | | mV (peak) |

• Peak to peak volatge symmetrical about $V_{DD}/2$

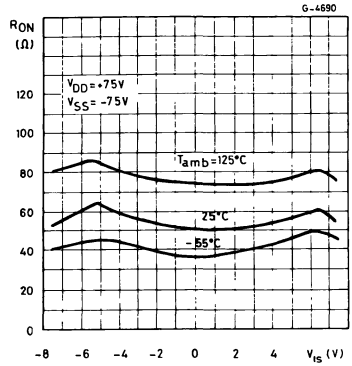
Typical ON Resistance vs. Input Signal Voltage at $V_{DD} = -V_{SS} = 2.5$ V.



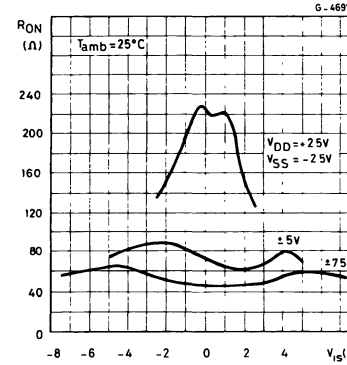

Typical ON Resistance vs. Input Signal Voltage at $V_{DD} = -V_{SS} = 5$ V.



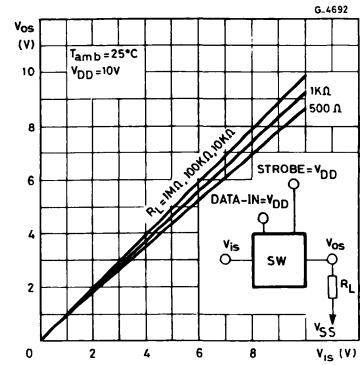
Typical ON Resistance vs. Input Signal Voltage at $V_{DD} = -V_{SS} = 7.5$ V.



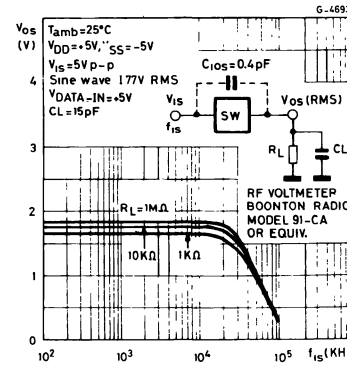

Typical ON Resistance vs.. Input Signal Voltage at $T_{amb} = 25$ °C.



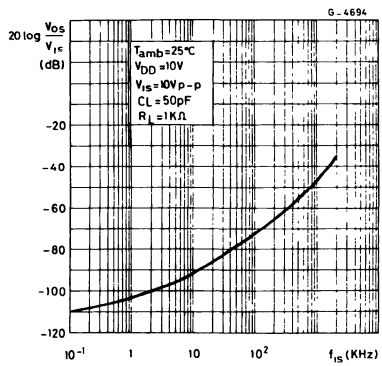

Typical Swich ON Transfert Characteristics (1 of 16 switches).



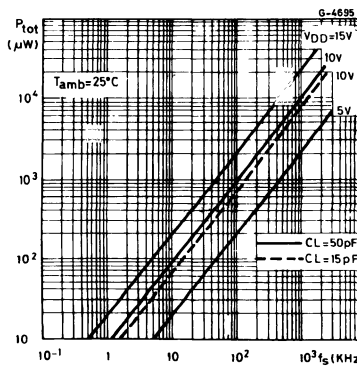

Typical Swich ON Frequency Response Characteristics.




Typical Crosstalk Between switches vs. Signal Frequency.

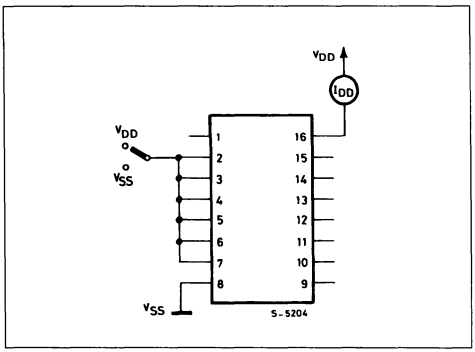



Typical Dynamic Power Dissipation vs. Switching Frequency..

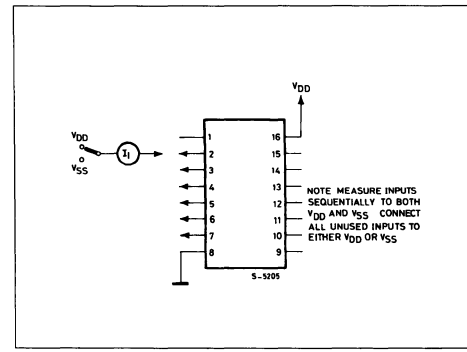


## TEST CIRCUITS

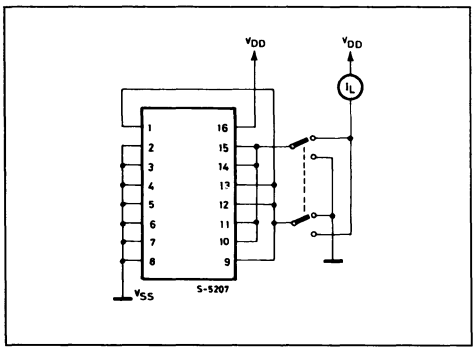
Quiescent Current.



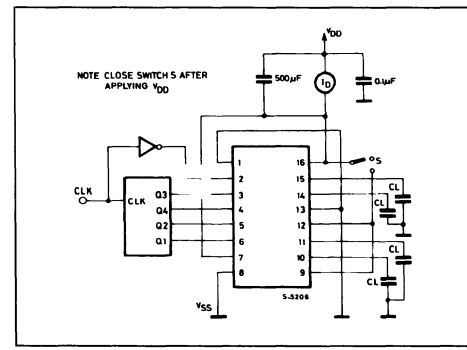

Input Current.



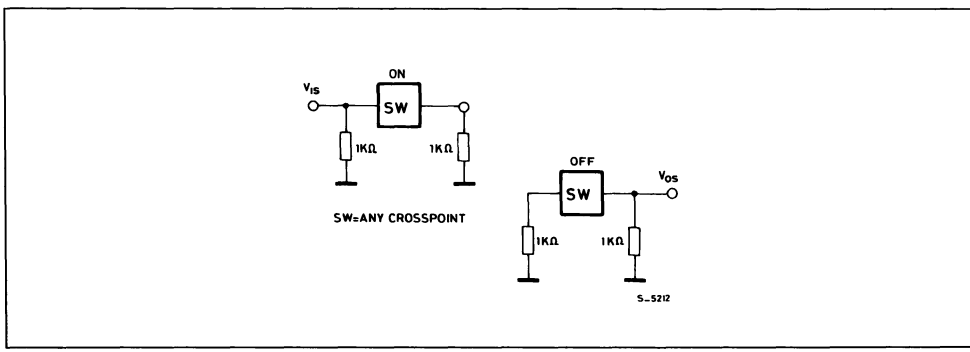

Off Switch Input or Output Leakage Current.



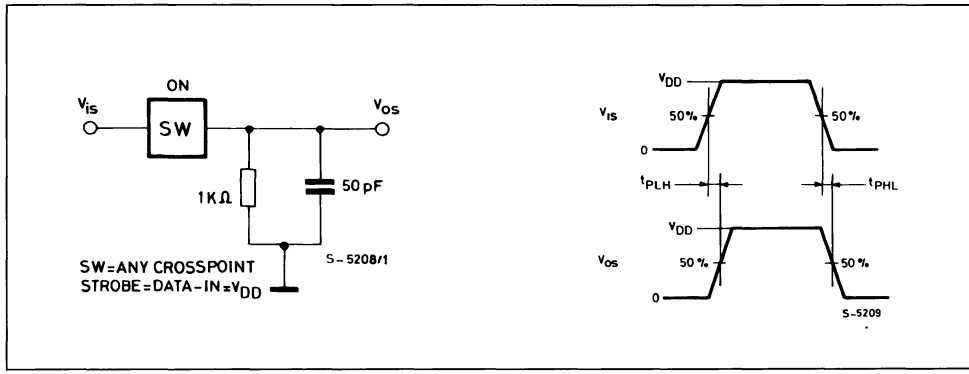

Dynamic Power Dissipation.




Croostalk Between Switch Circuits in the Same Package.



Propagation Delay Time and Waveforms (signal input to signal output, switch ON).




Waveforms for Crosstalk (control input to signal output).

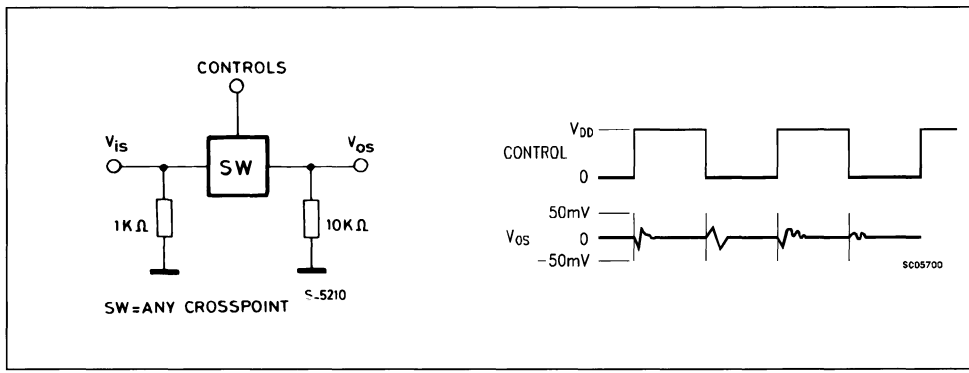



**Figure 1 :** Propagation Delay Time and Waveforms (strobe to signal output, switch Turn-ON or Turn-OFF).

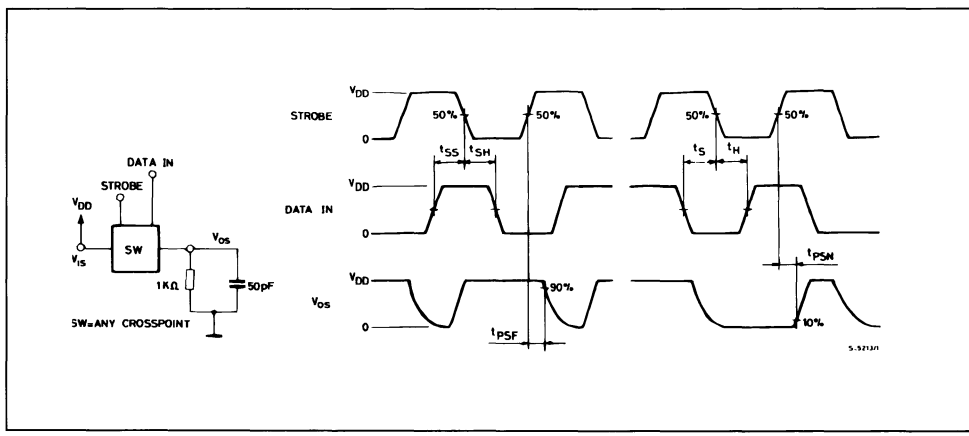


**Figure 2 :** Propagation Delay Time and Waveforms (data-in to signal output, switch Turn-ON to high or low level).

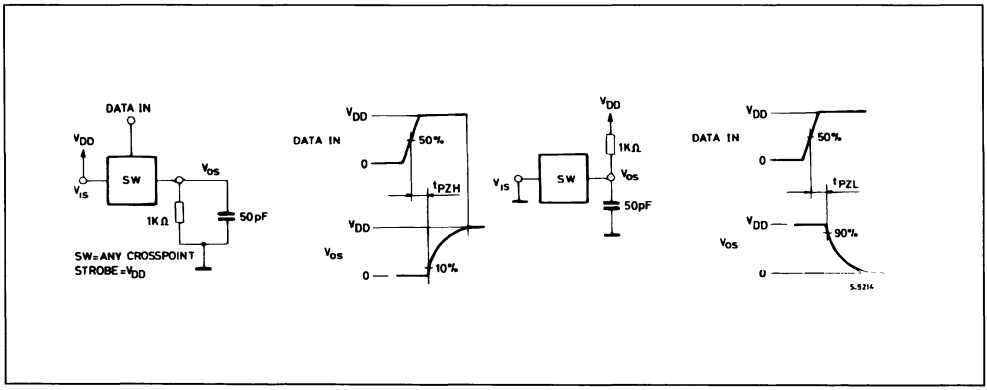
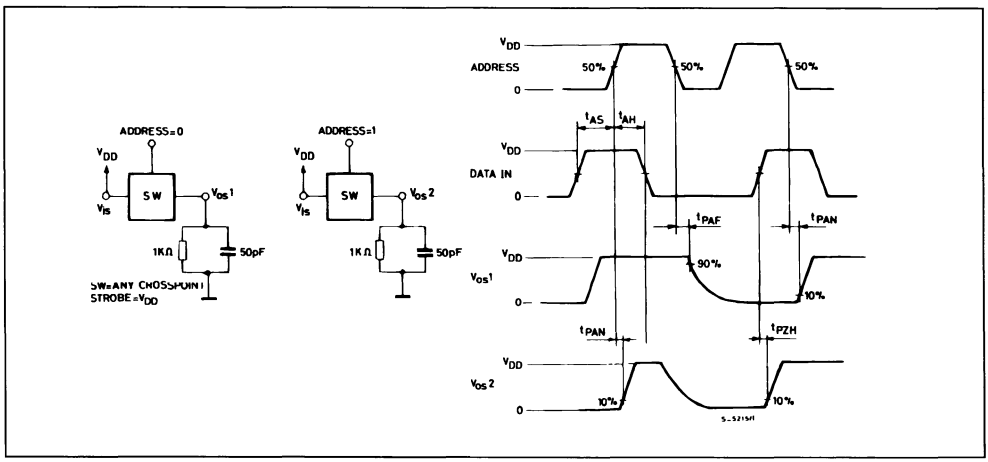



**Figure 3 :** Propagation Delay Time and Waveforms (address to signal output switch Turn-ON or Turn-OFF).



SGS-THOMSON MICROELECTRONICS

# M22101
# M22102

## 4 X 4 X 2 CROSSPOINT SWITCHES WITH CONTROL MEMORY

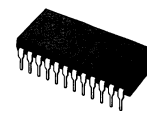
- LOW ON RESISTANCE – 75 Ω TYP AT $V_{DD}$ = 12 V
- "BUILT-IN" LATCHED INPUTS
- LARGE ANALOG SIGNAL CAPACITY ± $V_{DD}/2$
- 10 MHz SWITCH BANDWITH
- MATCHED SWITCH CHARACTERISTICS
- Δ RON = 8 Ω TYP, AT $V_{DD}$ = 12 V
- HIGH LINEARITY – 0.25 % DISTORTION TYP, AT f = 1 kHz, $V_{IN}$ = 5 V, $V_{DD}$ - $V_{SS}$ = 10 V AND RI = 1 Ω
- STANDARD CMOS NOISE IMMUNITY

### DESCRIPTION

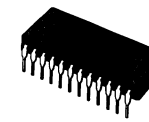
The **M22101** and **M22102** crosspoint switches consist of 4 x 4 x 2 arrays of crosspoints (transmission gates), 4-line to 16-line decoders, and 16 latch circuits. Any one of the sixteen crosspoint pairs can be selected by applying the appropriate four-line address and any number of crosspoint pairs can be ON simultaneously. Corresponding crosspoints in each array are turned on and OFF simultaneously, also.

In the **M22101**, the selected crosspoint pair can be turned on or off by applying a logical ONE or ZERO, respectively, to the data input, and applying a ONE to the strobe input. When the device is "power-up", the state of the 16 switches is indeterminate. Therefore all switches must be turned off by putting the strobe hight, data-in-low, and the addressing all switches in succession.

The selected pair of crosspoints in the **M22102** is turned on by applying a logical ONE to the $K_a$ (set) input while a logical ZERO is on the $K_b$ (reset) input, and turned off by applying a logical ONE to the $K_b$ input while a logical ZERO is on the $K_a$ input. In this respect the control latches of the **M22102** are similar to SET/RESET flip-flops. They differ, however, in that the simultaneous application of ONEs to the $K_a$ and $K_b$ inputs turns off (resets) all crosspoints. All crosspoints in both devices must be turned off as $V_{DD}$ is applied.



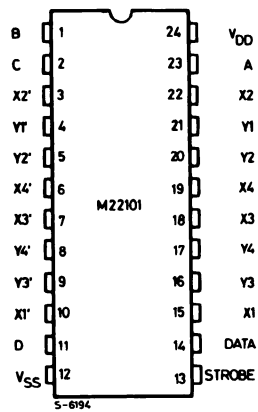
**B1**
(Plastic Package)

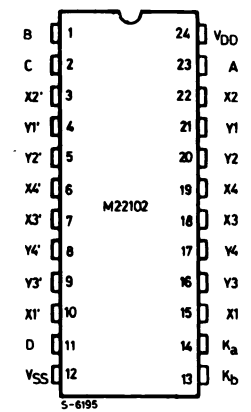


**F1**
(Ceramic Package)

**ORDER CODES :**
M22XXX B1 M22XXX F1

### PIN CONNECTIONS



## ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage: Ceramic Type<br>Plastic Type | -0.5 to +20<br>-0.5 to +18 | V<br>V |
| $V_I$ | Input Voltage | -0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for Top = Full Package Temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature: Ceramic Type<br>Plastic Type | -55 to +125<br>-40 to +85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage: Ceramic Type<br>Plastic Type | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature: Ceramic Type<br>Plastic Type | -55 to +125<br>-40 to +85 | °C<br>°C |

## CONTROL TRUTH TABLE FOR M22101

| Function | Address | | | | Strobe | Data | Select |
|---|---|---|---|---|---|---|---|
| | A | B | C | D | | | |
| Switch-on | 1 | 1 | 1 | 1 | 1 | 1 | (X4 Y4) & (X4' Y4') |
| Switch-off | 1 | 1 | 1 | 1 | 1 | 0 | (X4 Y4) & (X4' Y4') |
| No CHange | X | X | X | X | 0 | X | X X X X |

Note: 1 = High, 0 = Low, X = Don't Care

## CONTROL TRUTH TABLE FOR M22102

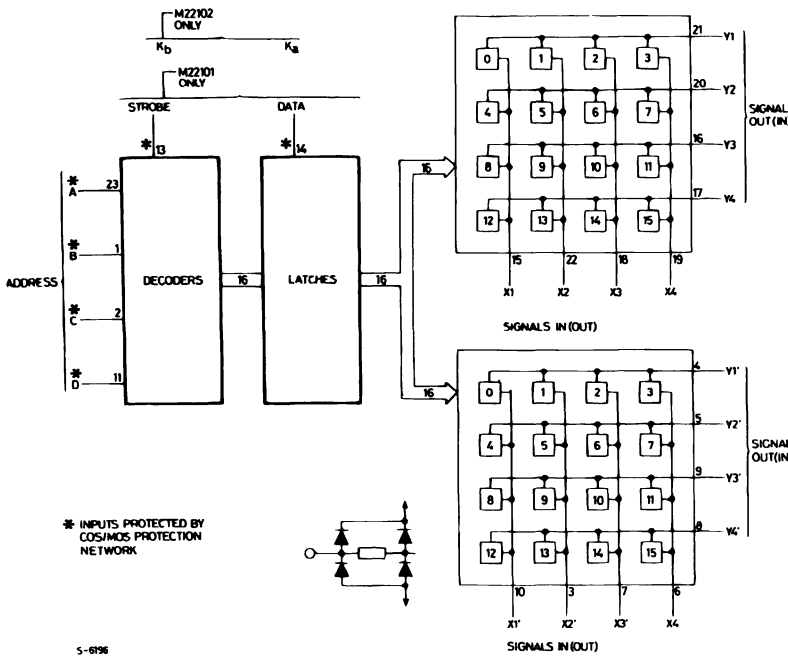
| Function | Address | | | | Strobe | Data | Select |
|---|---|---|---|---|---|---|---|
| | A | B | C | D | | | |
| Switch-on | 1 | 1 | 1 | 1 | 1 | 0 | (X4 Y4) & (X4' Y4') |
| Switch-off | 1 | 1 | 1 | 1 | 0 | 1 | (X4 Y4) & (X4' Y4') |
| All Switch-off | X | X | X | X | 1 | 1 | All |
| No CHange | X | X | X | X | 0 | 0 | X X X X |

Note: 1 = High, 0 = Low, X = Don't Care

## DECODER TRUTH TABLE

| Address | | | | Select | | Address | | | | Select | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | B | C | D | | | A | B | C | D | | |
| 0 | 0 | 0 | 0 | X1 Y1 | X1' Y1' | 0 | 0 | 0 | 1 | X1 Y3 | X1' Y3' |
| 1 | 0 | 0 | 0 | X2 Y1 | X2' Y1' | 1 | 0 | 0 | 1 | X2 Y3 | X2' Y3' |
| 0 | 1 | 0 | 0 | X3 Y1 | X3' Y1' | 0 | 1 | 0 | 1 | X3 Y3 | X3' Y3' |
| 1 | 1 | 0 | 0 | X4 Y1 | X4' Y1' | 1 | 1 | 0 | 1 | X4 Y3 | X4' Y3' |
| 0 | 0 | 1 | 0 | X1 Y2 | X1' Y2' | 0 | 0 | 1 | 1 | X1 Y4 | X1' Y4' |
| 1 | 0 | 1 | 0 | X2 Y2 | X2' Y2' | 1 | 0 | 1 | 1 | X2 Y4 | X2' Y4' |
| 0 | 1 | 1 | 0 | X3 Y2 | X3' Y2' | 0 | 1 | 1 | 1 | X3 Y4 | X3' Y4' |
| 1 | 1 | 1 | 0 | X4 Y2 | X4' Y2' | 1 | 1 | 1 | 1 | X4 Y4 | X4' Y4' |

## FUNCTIONAL AND BLOCK DIAGRAM



## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter | | Test Conditios | $V_I$ (V) | $V_{DD}$ (V) | Value $T_{LOW}$ * Min. | $T_{LOW}$ * Max. | 25 °C Min. | 25 °C Typ. | 25 °C Max. | $T_{HIGH}$ * Min. | $T_{HIGH}$ * Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CROSSPOINT** | | | | | | | | | | | | | |
| $I_L$ | Quiescent Supply Current | F1 | | | 5 | | | | 0.04 | 5 | | 150 | µA |
| | | | | | 10 | | | | 0.04 | 10 | | 300 | |
| | | | | | 15 | | | | 0.04 | 20 | | 600 | |
| | | | | | 20 | | | | 0.08 | 100 | | 3000 | |
| | | B1 | | | 5 | | | | 0.04 | 20 | | 150 | |
| | | | | | 10 | | | | 0.04 | 40 | | 300 | |
| | | | | | 15 | | | | 0.04 | 80 | | 600 | |
| $R_{ON}$ | On Resistance | F1 | Any Switch | | 5 | | 450 | | 225 | 1250 | | 1625 | Ω |
| | | | | | 10 | | 135 | | 85 | 180 | | 230 | |
| | | | | | 12 | | 100 | | 75 | 135 | | 175 | |
| | | | | | 15 | | 70 | | 65 | 95 | | 125 | |
| | | B1 | $V_{IS}$ = 0 to $V_{DD}$ | | 5 | | 1000 | | 225 | 1250 | | 1440 | |
| | | | | | 10 | | 145 | | 85 | 180 | | 205 | |
| | | | | | 12 | | 110 | | 75 | 135 | | 155 | |
| | | | | | 15 | | 75 | | 65 | 95 | | 110 | |
| ΔON | Resistance $\Delta R_{ON}$ (Between any two channels) | | | | 5 | | | | 35 | | | | Ω |
| | | | | | 10 | | | | 20 | | | | |
| | | | | | 12 | | | | 18 | | | | |
| | | | | | 15 | | | | 15 | | | | |
| OFF Channel Leakage Current | | F1 | All Switch OFF | 0/18 | 18 | | ±0.1 | | $\pm10^{-3}$ | ±0.1• | | ±1 | µA |
| | | B1 | | 0/15 | 15 | | ±0.3 | | $\pm10^{-3}$ | ±0.3 | | ±1 | |
| **CONTROL** | | | | | | | | | | | | | |
| $V_{IL}$ | Input Low Voltage | | OFF Switch $I_L$ < 0.2 µA | | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | | 10 | | 3 | | | 3 | | 3 | |
| | | | | | 15 | | 4 | | | 4 | | 4 | |
| $V_{IH}$ | Input High Voltage | | ON Switch see $R_{ON}$ Characteristics | | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | | 10 | 7 | | 7 | | | 7 | | |
| | | | | | 15 | 11 | | 11 | | | 11 | | |
| $I_I$ | Input Current | F1 | Any Control Input | 0/18 | 18 | | ±0.1 | | $\pm10^{-5}$ | ±0.1 | | ±1 | µA |
| | | B1 | | 0/15 | 15 | | ±0.3 | | $\pm10^{-5}$ | ±0.3 | | ±1 | |
| $C_I$ | Input Capacitance | | Any Input | | | | | | 5 | 7.5 | | | pF |

• Determined by minimum feasible leakage measurement for automatic testing

* $T_{LOW}$ = -55 °C for **HCC** device: -40 °C for **HCF** device.

* $T_{HIGH}$ = +125 °C for **HCC** device: +85 °C for **HCF** device

The Noise Margin for both "1" and "0" level is 1V min. with $V_{DD}$ = 5 V, 2 V min. with $V_{DD}$ = 10 V, 2.5 V min with $V_{DD}$ = 15 V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 KΩ, typical temperature coefficent for all $V_{DD}$ values is 03 %/°C, all input rise and fall times= 20 ns)

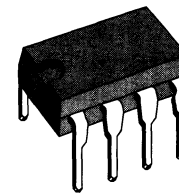
| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$ $t_{PLH}$ | Propagation Delay Time Address or Strobe Inputs to Output | $R_L$ = 10 KΩ $C_L$ = 50 pF | 12 | | 200 | | ns |
| $t_{PHL}$ $t_{PLH}$ | Propagation Delay Time Across Crosspoint | | | | 20 | | ns |
| | Minimum Strobe Pulse Width | | | | 80 | | ns |

# PACKAGES

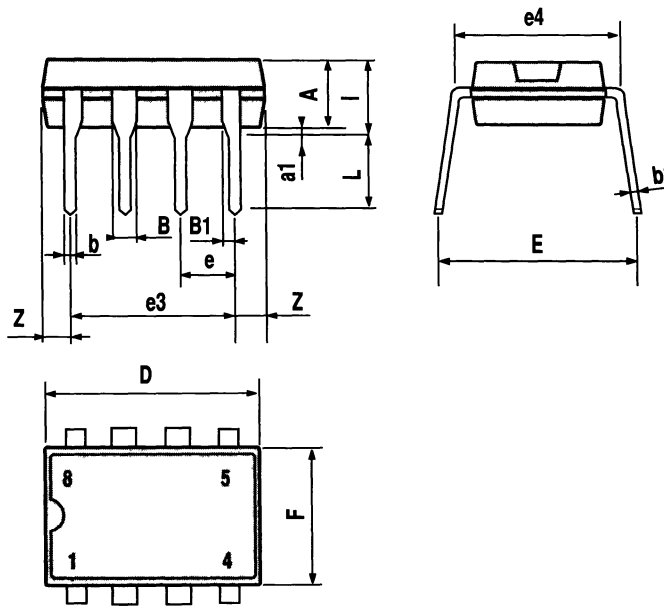
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | 3.3 | | | 0.130 | |
| a1 | 0.7 | | | 0.028 | | |
| B | 1.39 | | 1.65 | 0.055 | | 0.065 |
| B1 | 0.91 | | 1.04 | 0.036 | | 0.041 |
| b | | 0.5 | | | 0.020 | |
| b1 | 0.38 | | 0.5 | 0.015 | | 0.020 |
| D | | | 9.8 | | | 0.386 |
| E | | 8.8 | | | 0.346 | |
| e | | 2.54 | | | 0.100 | |
| e3 | | 7.62 | | | 0.300 | |
| e4 | | 7.62 | | | 0.300 | |
| F | | | 7.1 | | | 0.280 |
| I | | | 4.8 | | | 0.189 |
| L | | 3.3 | | | 0.130 | |
| Z | 0.44 | | 1.6 | 0.017 | | 0.063 |

SGS-THOMSON MICROELECTRONICS

## OUTLINE AND MECHANICAL DATA



## Minidip (0.4)

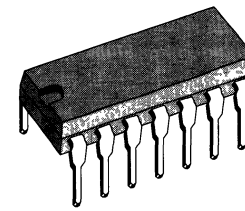



P001F

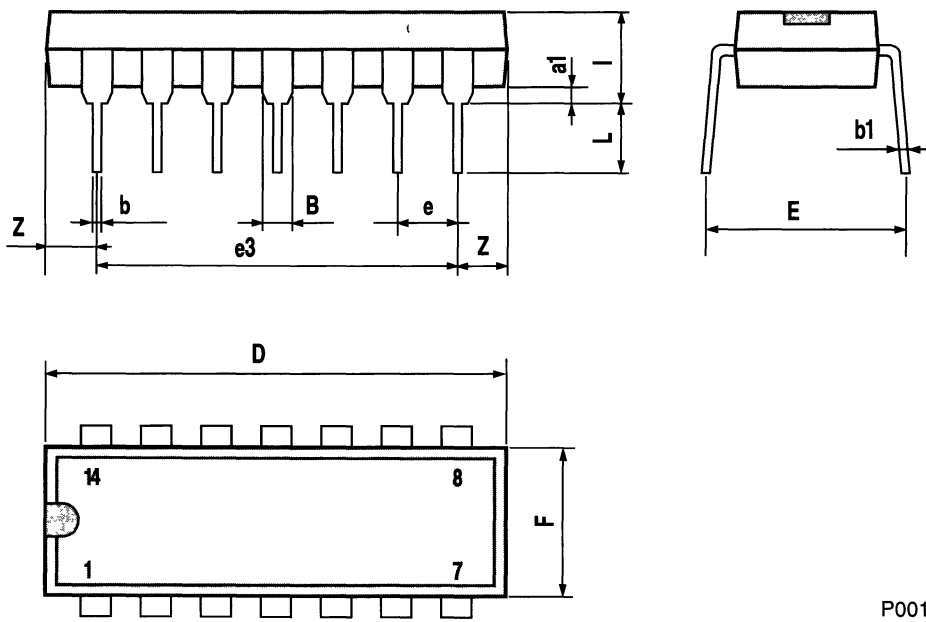
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| a1 | 0.51 | | | 0.020 | | |
| B | 1.39 | | 1.65 | 0.055 | | 0.065 |
| b | | 0.5 | | | 0.020 | |
| b1 | | 0.25 | | | 0.010 | |
| D | | | 20 | | | 0.787 |
| E | | 8.5 | | | 0.335 | |
| e | | 2.54 | | | 0.100 | |
| e3 | | 15.24 | | | 0.600 | |
| F | | | 7.1 | | | 0.280 |
| I | | | 5.1 | | | 0.201 |
| L | | 3.3 | | | 0.130 | |
| Z | 1.27 | | 2.54 | 0.050 | | 0.100 |

SGS-THOMSON MICROELECTRONICS

## OUTLINE AND MECHANICAL DATA



## Plastic DIP14

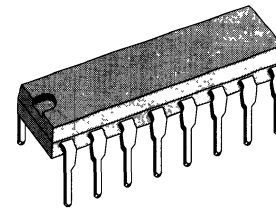



P001A

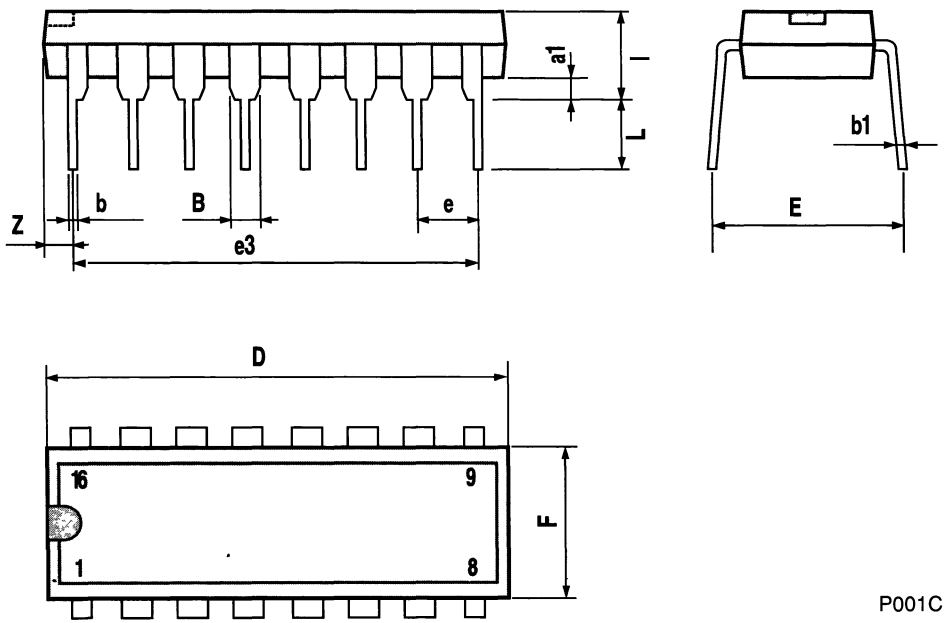
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| a1 | 0.51 | | | 0.020 | | |
| B | 0.77 | | 1.65 | 0.030 | | 0.065 |
| b | | 0.5 | | | 0.020 | |
| b1 | | 0.25 | | | 0.010 | |
| D | | | 20 | | | 0.787 |
| E | | 8.5 | | | 0.335 | |
| e | | 2.54 | | | 0.100 | |
| e3 | | 17.78 | | | 0.700 | |
| F | | | 7.1 | | | 0.280 |
| I | | | 5.1 | | | 0 201 |
| L | | 3.3 | | | 0.130 | |
| Z | | | 1.27 | | | 0.050 |

SGS-THOMSON MICROELECTRONICS

## OUTLINE AND MECHANICAL DATA



## Plastic DIP16 (0.25)

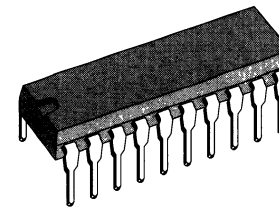



P001C

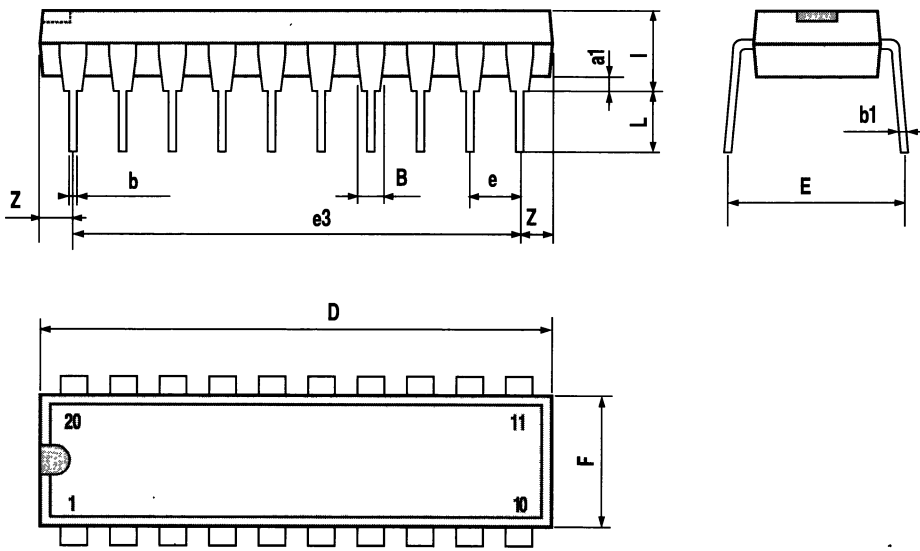
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| a1 | 0.254 | | | 0.010 | | |
| B | 1.39 | | 1.65 | 0.055 | | 0.065 |
| b | | 0.45 | | | 0.018 | |
| b1 | | 0.25 | | | 0.010 | |
| D | | | 25.4 | | | 1.000 |
| E | | 8.5 | | | 0.335 | |
| e | | 2.54 | | | 0.100 | |
| e3 | | 22.86 | | | 0.900 | |
| F | | | 7.1 | | | 0.280 |
| I | | | 3.93 | | | 0.155 |
| L | | 3.3 | | | 0.130 | |
| Z | | | 1.34 | | | 0.053 |

SGS-THOMSON MICROELECTRONICS

## OUTLINE AND MECHANICAL DATA



## Plastic DIP20 (0.25)

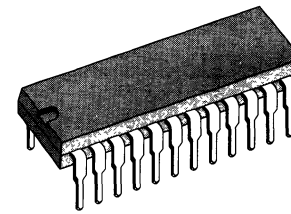



P001J

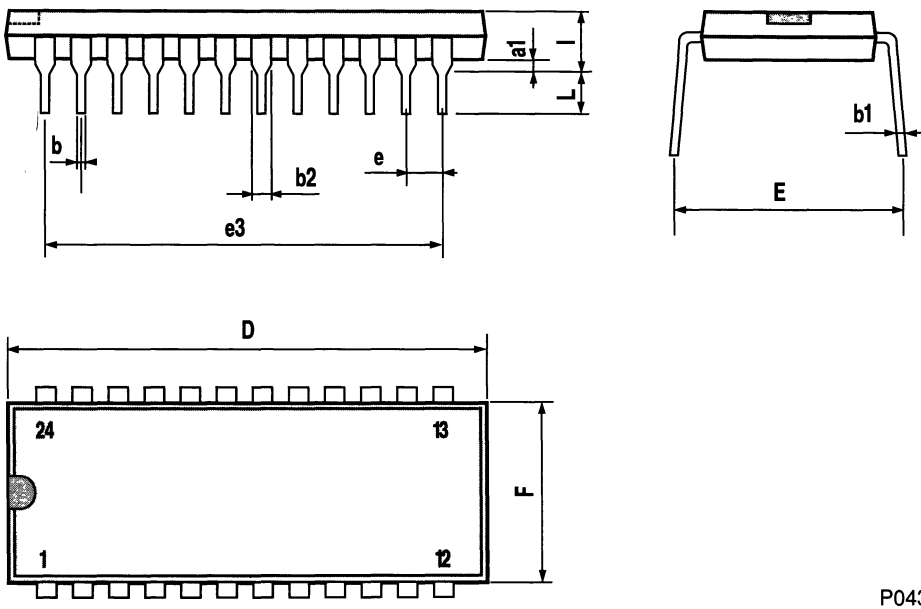
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| a1 | | 0.63 | | | 0.025 | |
| b | | 0.45 | | | 0.018 | |
| b1 | 0.23 | | 0.31 | 0.009 | | 0.012 |
| b2 | | 1.27 | | | 0.050 | |
| D | | | 32.2 | | | 1.268 |
| E | 15.2 | | 16.68 | 0.598 | | 0.657 |
| e | | 2.54 | | | 0.100 | |
| e3 | | 27.94 | | | 1.100 | |
| F | | | 14.1 | | | 0.555 |
| I | | 4.445 | | | 0.175 | |
| L | | 3.3 | | | 0.130 | |

SGS-THOMSON MICROELECTRONICS

## OUTLINE AND MECHANICAL DATA



## Plastic DIP24 (0.25)

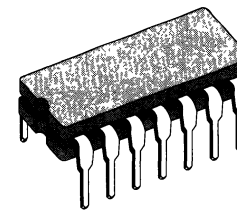



P043A

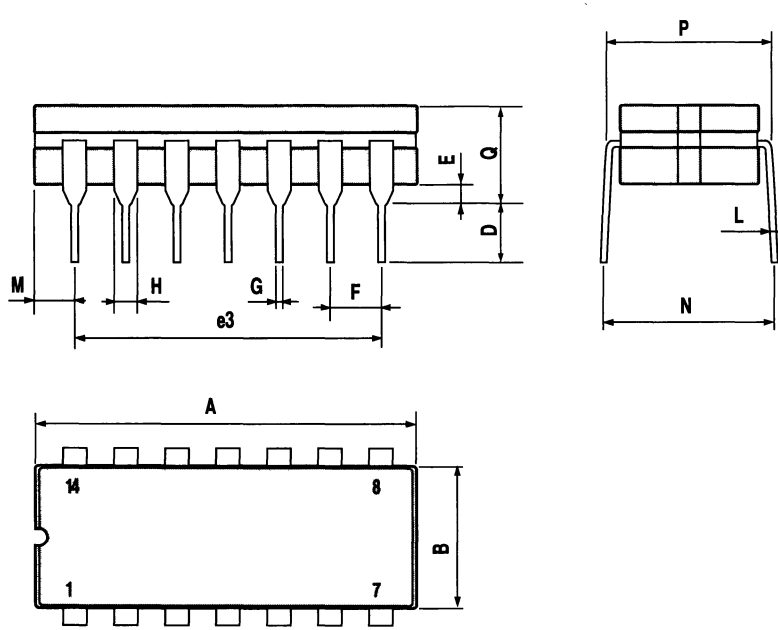
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 20 | | | 0.787 |
| B | | | 7.0 | | | 0.276 |
| D | | 3.3 | | | 0.130 | |
| E | 0.38 | | | 0.015 | | |
| e3 | | 15.24 | | | 0.600 | |
| F | 2.29 | | 2.79 | 0.090 | | 0.110 |
| G | 0.4 | | 0.55 | 0.016 | | 0.022 |
| H | 1.17 | | 1.52 | 0.046 | | 0.060 |
| L | 0.22 | | 0.31 | 0.009 | | 0.012 |
| M | 1.52 | | 2.54 | 0.060 | | 0.100 |
| N | | | 10.3 | | | 0.406 |
| P | 7.8 | | 8.05 | 0.307 | | 0.317 |
| Q | | | 5.08 | | | 0.200 |

SGS-THOMSON MICROELECTRONICS

## OUTLINE AND MECHANICAL DATA



## Ceramic DIP14/1

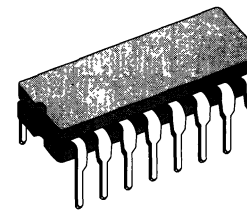



P053C

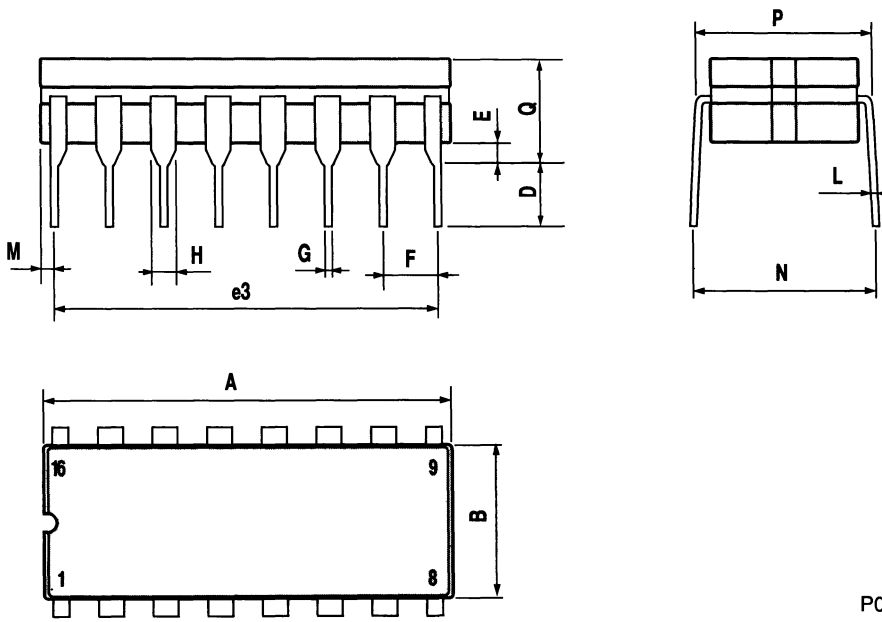
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 20 | | | 0.787 |
| B | | | 7 | | | 0.276 |
| D | | 3.3 | | | 0.130 | |
| E | 0.38 | | | 0.015 | | |
| e3 | | 17.78 | | | 0.700 | |
| F | 2.29 | | 2.79 | 0.090 | | 0.110 |
| G | 0.4 | | 0.55 | 0.016 | | 0.022 |
| H | 1.17 | | 1.52 | 0.046 | | 0.060 |
| L | 0.22 | | 0.31 | 0.009 | | 0.012 |
| M | 0.51 | | 1.27 | 0.020 | | 0.050 |
| N | | | 10.3 | | | 0.406 |
| P | 7.8 | | 8.05 | 0.307 | | 0.317 |
| Q | | | 5.08 | | | 0.200 |

SGS-THOMSON MICROELECTRONICS

## OUTLINE AND MECHANICAL DATA



## Ceramic DIP16/1

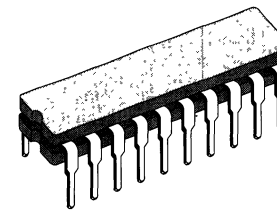



P053D

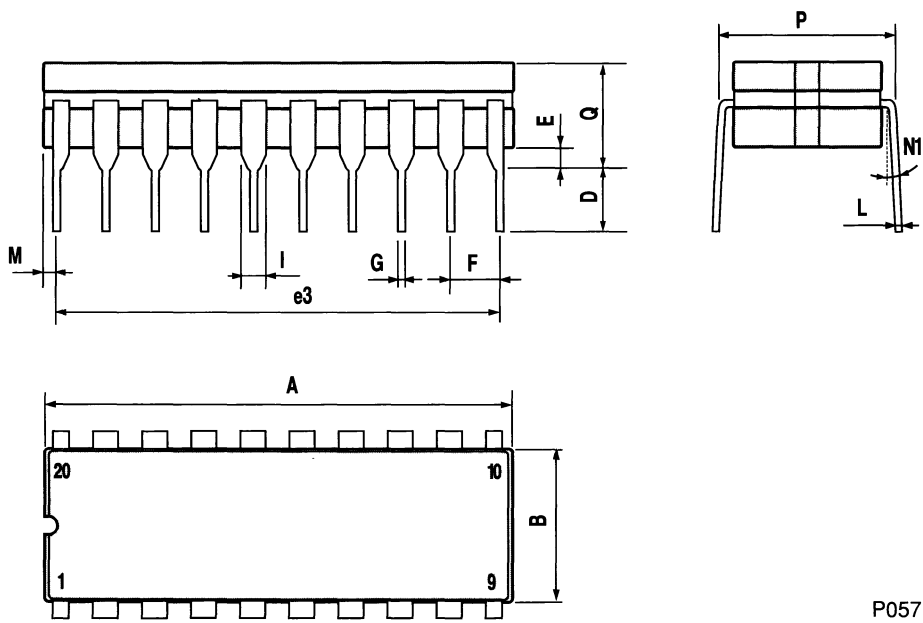
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 25 | | | 0.984 |
| B | | | 7.8 | | | 0.307 |
| D | | 3.3 | | | 0.130 | |
| E | 0.5 | | 1.78 | 0.020 | | 0.070 |
| e3 | | 22.86 | | | 0.900 | |
| F | 2.29 | | 2.79 | 0.090 | | 0.110 |
| G | 0.4 | | 0.55 | 0.016 | | 0.022 |
| I | 1.27 | | 1.52 | 0.050 | | 0.060 |
| L | 0.22 | | 0.31 | 0.009 | | 0.012 |
| M | 0.51 | | 1.27 | 0.020 | | 0.050 |
| N1 | 4° (min.), 15° (max.) | | | | | |
| P | 7.9 | | 8.13 | 0.311 | | 0.320 |
| Q | | | 5.71 | | | 0.225 |

SGS-THOMSON MICROELECTRONICS

## OUTLINE AND MECHANICAL DATA



## Ceramic DIP20

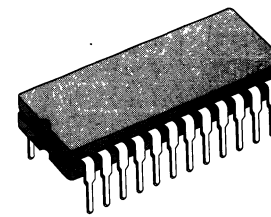



P057H

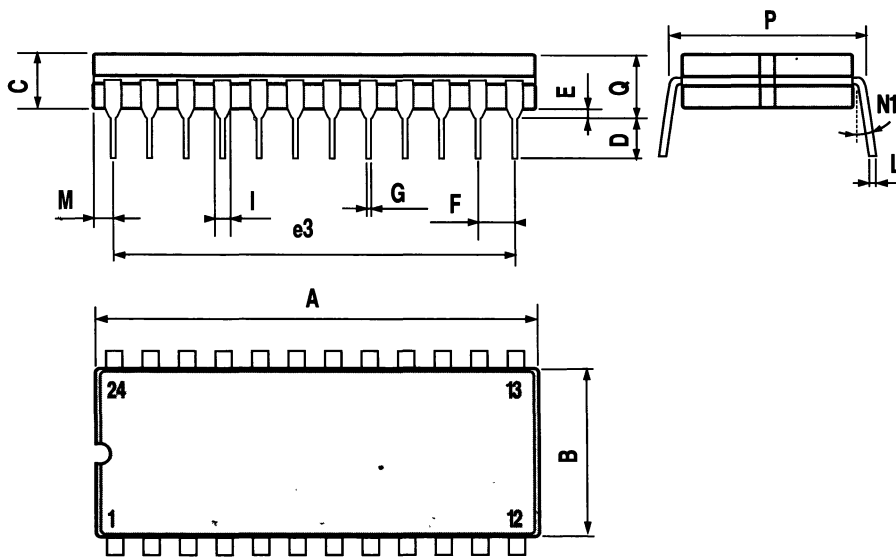
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 32.3 | | | 1.272 |
| B | 13.05 | | 13.36 | 0.514 | | 0.526 |
| C | 3.9 | | 5.08 | 0.154 | | 0.200 |
| D | 3 | | | 0.118 | | |
| E | 0.5 | | 1.78 | 0.020 | | 0.070 |
| e3 | | 27.94 | | | 1.100 | |
| F | 2.29 | | 2.79 | 0.090 | | 0.110 |
| G | 0.4 | | 0.55 | 0.016 | | 0.022 |
| I | 1.17 | | 1.52 | 0.046 | | 0.060 |
| L | 0.22 | | 0.31 | 0.009 | | 0.012 |
| M | 1.52 | | 2.49 | 0.060 | | 0.098 |
| N1 | 4° (min.), 15° (max.) | | | | | |
| P | 15.4 | | 15.8 | 0.606 | | 0.622 |
| Q | | | 5.71 | | | 0.225 |

SGS-THOMSON MICROELECTRONICS

## OUTLINE AND MECHANICAL DATA



## Ceramic DIP24

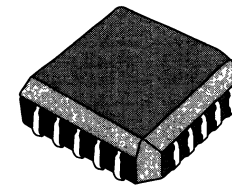



P058C

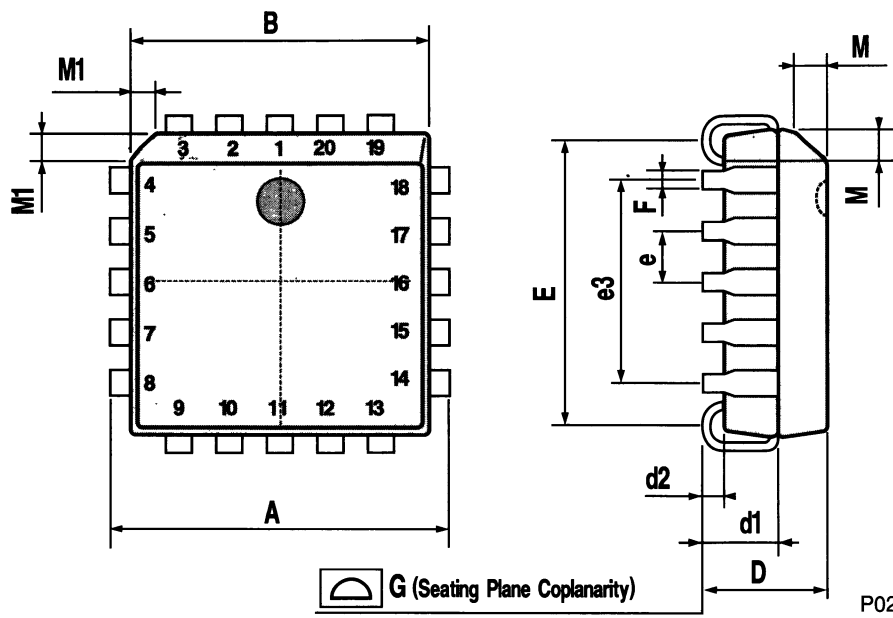
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 9.78 | | 10.03 | 0.385 | | 0.395 |
| B | 8.89 | | 9.04 | 0.350 | | 0.356 |
| D | 4.2 | | 4.57 | 0.165 | | 0.180 |
| d1 | | 2.54 | | | 0.100 | |
| d2 | | 0.56 | | | 0.022 | |
| E | 7.37 | | 8.38 | 0.290 | | 0.330 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 5.08 | | | 0.200 | |
| F | | 0.38 | | | 0.015 | |
| G | | | 0.101 | | | 0.004 |
| M | | 1.27 | | | 0.050 | |
| M1 | | 1.14 | | | 0.045 | |

SGS-THOMSON MICROELECTRONICS

## OUTLINE AND MECHANICAL DATA



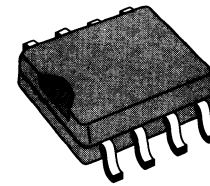
## PLCC20



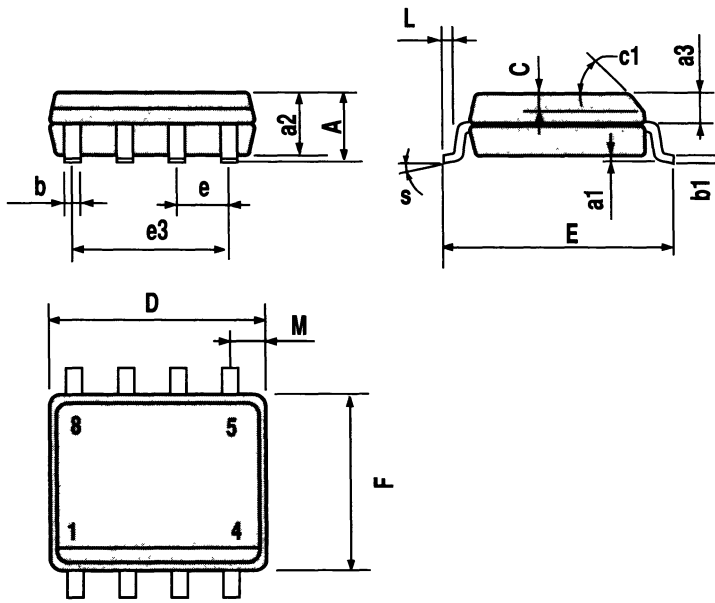
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.75 | | | 0.069 |
| a1 | 0.1 | | 0.25 | 0.004 | | 0.010 |
| a2 | | | 1.65 | | | 0.065 |
| a3 | 0.65 | | 0.85 | 0.026 | | 0.033 |
| b | 0.35 | | 0.48 | 0.014 | | 0.019 |
| b1 | 0.19 | | 0.25 | 0.007 | | 0.010 |
| C | 0.25 | | 0.5 | 0.010 | | 0.020 |
| c1 | 45° (typ.) | | | | | |
| D | 4.8 | | 5.0 | 0.189 | | 0.197 |
| E | 5.8 | | 6.2 | 0.228 | | 0.244 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 3.81 | | | 0.150 | |
| F | 3.8 | | 4.0 | 0.15 | | 0.157 |
| L | 0.4 | | 1.27 | 0.016 | | 0.050 |
| M | | | 0.6 | | | 0.024 |
| S | 8° (max.) | | | | | |

SGS-THOMSON MICROELECTRONICS

## OUTLINE AND MECHANICAL DATA



## SO8

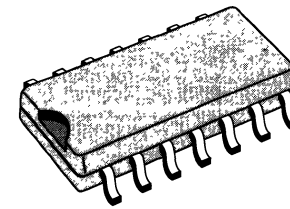



P013M

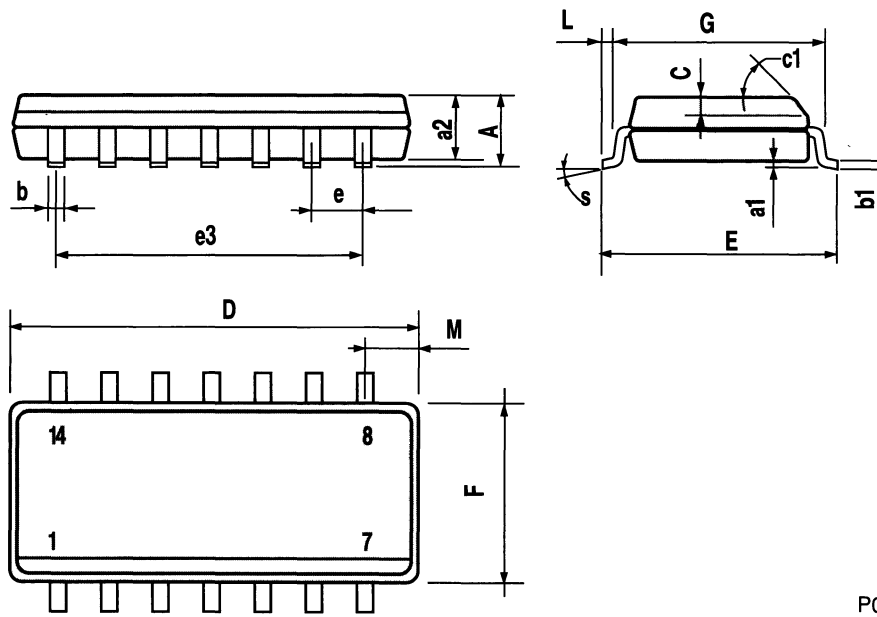
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.75 | | | 0.069 |
| a1 | 0.1 | | 0.2 | 0.004 | | 0 008 |
| a2 | | | 1.6 | | | 0.063 |
| b | 0.35 | | 0.46 | 0.014 | | 0.018 |
| b1 | 0.19 | | 0.25 | 0.007 | | 0.010 |
| C | | 0.5 | | | 0.020 | |
| c1 | 45° (typ.) | | | | | |
| D | 8.55 | | 8.75 | 0.336 | | 0.344 |
| E | 5.8 | | 6.2 | 0.228 | | 0.244 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 7.62 | | | 0.300 | |
| F | 3.8 | | 4.0 | 0.15 | | 0.157 |
| G | 4.6 | | 5.3 | 0.181 | | 0.208 |
| L | 0.5 | | 1.27 | 0.020 | | 0.050 |
| M | | | 0.68 | | | 0.027 |
| S | 8° (max.) | | | | | |

SGS-THOMSON MICROELECTRONICS

## OUTLINE AND MECHANICAL DATA



## SO14

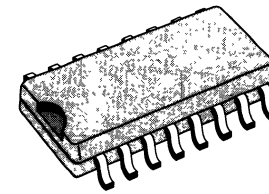



P013G

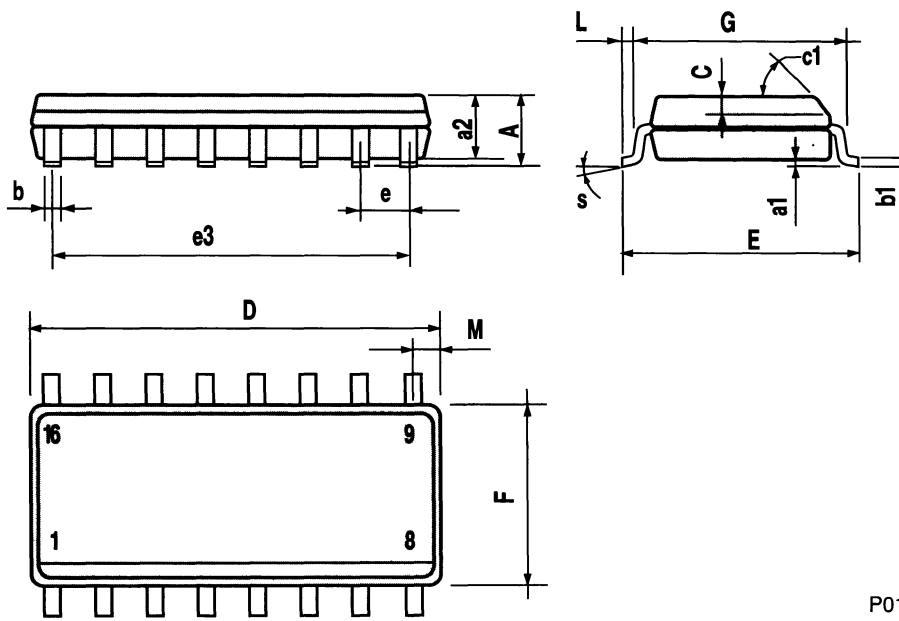
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.75 | | | 0.069 |
| a1 | 0.1 | | 0.2 | 0.004 | | 0.008 |
| a2 | | | 1.6 | | | 0.063 |
| b | 0.35 | | 0.46 | 0.014 | | 0.018 |
| b1 | 0.19 | | 0.25 | 0.007 | | 0.010 |
| C | | 0.5 | | | 0.020 | |
| c1 | 45° (typ.) | | | | | |
| D | 9.8 | | 10 | 0.386 | | 0.394 |
| E | 5.8 | | 6.2 | 0.228 | | 0.244 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 8.89 | | | 0.350 | |
| F | 3.8 | | 4.0 | 0.150 | | 0.157 |
| G | 4.6 | | 5.3 | 0.181 | | 0.209 |
| L | 0.5 | | 1.27 | 0.020 | | 0.050 |
| M | | | 0.62 | | | 0.024 |
| S | 8° (max.) | | | | | |

SGS-THOMSON MICROELECTRONICS

## OUTLINE AND MECHANICAL DATA



## SO16

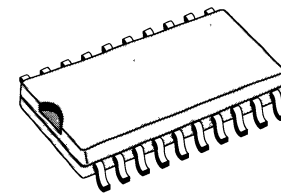



P013H

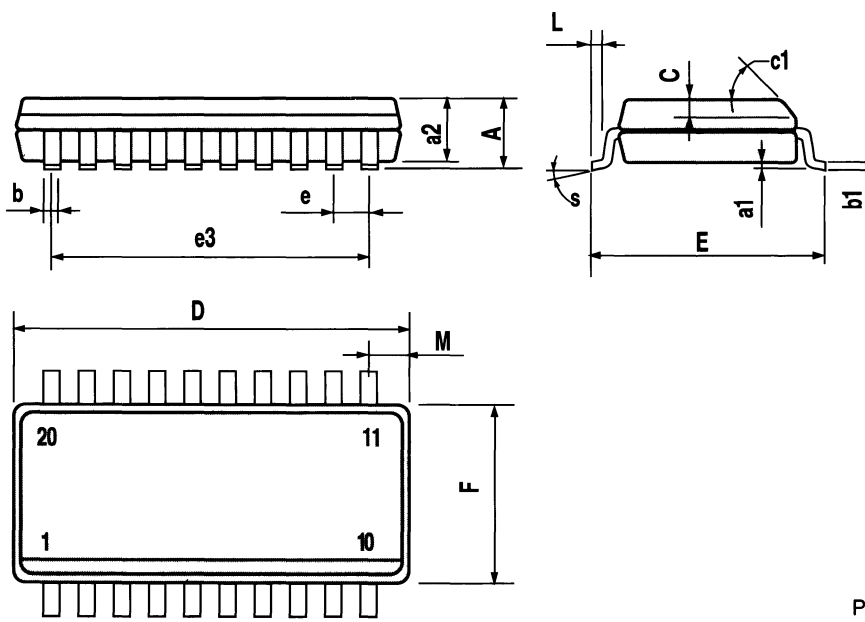
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 2.65 | | | 0.104 |
| a1 | 0.1 | | 0.2 | 0.004 | | 0.008 |
| a2 | | | 2.45 | | | 0.096 |
| b | 0.35 | | 0.49 | 0.014 | | 0 019 |
| b1 | 0.23 | | 0 32 | 0.009 | | 0.013 |
| C | | 0.5 | | | 0.020 | |
| c1 | 45° (typ.) | | | | | |
| D | 12.6 | | 13.0 | 0.496 | | 0.510 |
| E | 10 | | 10.65 | 0.394 | | 0.419 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 11.43 | | | 0.450 | |
| F | 7.4 | | 7.6 | 0.291 | | 0.300 |
| L | 0.5 | | 1 27 | 0 020 | | 0 050 |
| M | | | 0.75 | | | 0.030 |
| S | 8° (max.) | | | | | |

SGS-THOMSON MICROELECTRONICS

## OUTLINE AND MECHANICAL DATA



## SO20

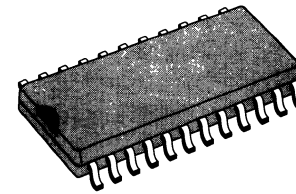



P013L

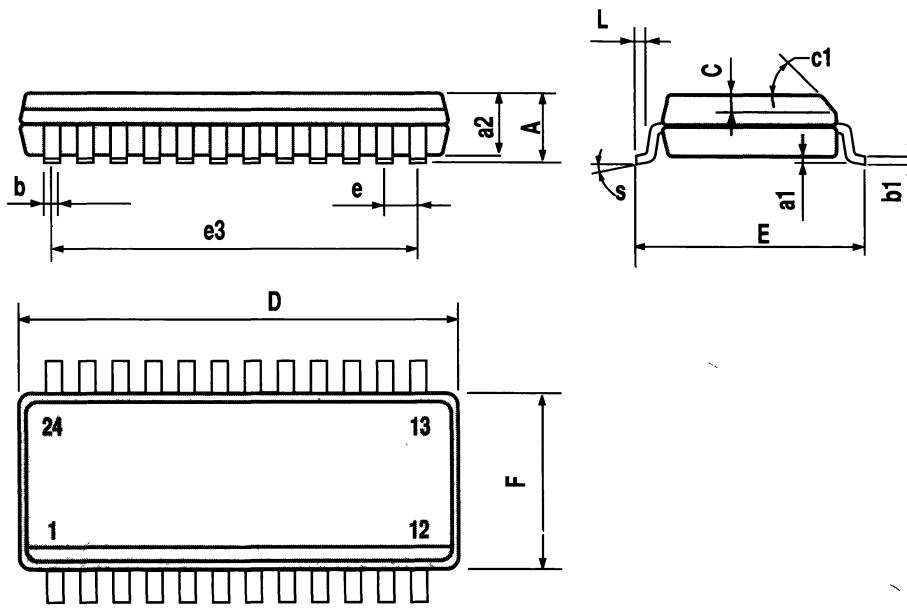
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 2.65 | | | 0.104 |
| a1 | 0.1 | | 0.2 | 0.004 | | 0.008 |
| a2 | | | 2.45 | | | 0.096 |
| b | 0.35 | | 0.49 | 0.014 | | 0.019 |
| b1 | 0.23 | | 0.32 | 0.009 | | 0.013 |
| C | | 0.5 | | | 0.020 | |
| c1 | 45° (typ.) | | | | | |
| D | 15.2 | | 15.6 | 0.598 | | 0.614 |
| E | 10 | | 10.65 | 0.394 | | 0.419 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 13.97 | | | 0.550 | |
| F | 7.4 | | 7.6 | 0.291 | | 0.300 |
| L | 0.5 | | 1.27 | 0.020 | | 0.050 |
| M | | | 0.75 | | | 0.030 |
| S | 8° (max.) | | | | | |

SGS-THOMSON MICROELECTRONICS

## OUTLINE AND MECHANICAL DATA



**SO24**



**NOTES**

# SALES OFFICES

## EUROPE

### DENMARK

**2730 HERLEV**
Herlev Torv, 4
Tel (45-42) 94.85 33
Telex 35411
Telefax (45-42) 948694

### FINLAND

**LOHJA SF-08150**
Karjalankatu, 2
Tel (358-12) 155 11
Telefax (358-12) 155 66

### FRANCE

**94253 GENTILLY Cedex**
7 - avenue Gallieni - BP 93
Tel (33-1) 47 40 75 75
Telex 632570 STMHQ
Telefax (33-1) 47 40 79 10

**67000 STRASBOURG**
20, Place des Halles
Tel (33) 88 75 50 66
Telex 870001F
Telefax (33) 88 22 29 32

### GERMANY

**6000 FRANKFURT**
Gutleutstrasse 322
Tel (49-69) 237492-3
Telex 176997 689
Telefax (49-69) 231957
Teletex. 6997689=STVBP

**8011 GRASBRUNN**
Bretonischer Ring 4
Neukeferloh Technopark
Tel (49-89) 46006-0
Telex 528211
Telefax (49-89) 4605454
Teletex 897107=STDISTR

**3000 HANNOVER 51**
Rotenburger Strasse 28A
Tel (49-511) 615960
Telex 175118418
Teletex 5118418 CSFBEH
Telefax (49-511) 6151243

**5202 HENNEF**
Reuther Strasse 1A-C
Tel (49-2242) 6088
(49-2242) 4019/4010
Telefax (49-2242) 84181

**8500 NÜRNBERG 20**
Erlenstegenstrasse, 72
Tel (49-911) 59893-0
Telex 626243
Telefax (49-911) 5980701

**7000 STUTTGART 31**
Mittlerer Pfad 2-4
Tel (49-711) 13968-0
Telex 721718
Telefax (49-711) 8661427

### ITALY

**20090 ASSAGO (MI)**
Vle Milanofiori - Strada 4 - Palazzo A/4/A
Tel (39-2) 89213 1 (10 linee)
Telex 330131 - 330141 SGSAGR
Telefax (39-2) 8250449

**40033 CASALECCHIO DI RENO (BO)**
Via R Fucini, 12
Tel (39-51) 591914
Telex 512442
Telefax (39-51) 591305

**00161 ROMA**
Via A Torlonia, 15
Tel (39-6) 8443341
Telex 620653 SGSATE I
Telefax (39-6) 8444474

### NETHERLANDS

**5652 AR EINDHOVEN**
Meerenakkerweg 1
Tel (31-40) 550015
Telex 51186
Telefax (31-40) 528835

### SPAIN

**08021 BARCELONA**
Calle Platon, 6 4$^{th}$ Floor, 5$^{th}$ Door
Tel (34-3) 4143300-4143361
Telefax (34-3) 2021461

**28027 MADRID**
Calle Albacete, 5
Tel (34-1) 4051615
Telex 46033 TCCEE
Telefax (34-1) 4031134

### SWEDEN

**S-16421 KISTA**
Borgarfjordsgatan, 13 - Box 1094
Tel (46-8) 7939220
Telex 12078 THSWS
Telefax (46-8) 7504950

### SWITZERLAND

**1218 GRAND-SACONNEX (GENEVA)**
Chemin Francois-Lehmann, 18/A
Tel (41-22) 7986462
Telex 415493 STM CH
Telefax (41-22) 7984869

### UNITED KINGDOM and EIRE

**MARLOW, BUCKS**
Planar House, Parkway
Globe Park
Tel (44-628) 890800
Telex 847458
Telefax (44-628) 890391

# AMERICAS

## BRAZIL

**05413 SÃO PAULO**
R Henrique Schaumann 286-CJ33
Tel (55-11) 883-5455
Telex (391)11-37988 "UMBR BR"
Telefax (55-11) 282-2367

## U.S.A.

NORTH & SOUTH AMERICAN
MARKETING HEADQUARTERS
1000 East Bell Road
Phoenix, AZ 85022
(1-602) 867-6100

SALES COVERAGE BY STATE

**ALABAMA**
Huntsville - (205) 533-5995

**ARIZONA**
Phoenix - (602) 867-6217

**CALIFORNIA**
Santa Ana - (714) 957-6018
San Jose - (408) 452-8585

**COLORADO**
Boulder (303) 449-9000

**ILLINOIS**
Schaumburg - (708) 517-1890

**INDIANA**
Kokomo - (317) 459-4700

**MASSACHUSETTS**
Lincoln - (617) 259-0300

**MICHIGAN**
Livonia - (313) 462-4030

**NEW JERSEY**
Voorhees - (609) 772-6222

**NEW YORK**
Poughkeepsie - (914) 454-8813

**NORTH CAROLINA**
Raleigh - (919) 787-6555

**TEXAS**
Carrollton - (214) 466-8844

FOR RF AND MICROWAVE POWER TRANSISTORS CONTACT THE FOLLOWING REGIONAL OFFICE IN THE U S.A.

**PENNSYLVANIA**
Montgomeryville - (215) 361-6400

# ASIA / PACIFIC

## AUSTRALIA

**NSW 2027 EDGECLIFF**
Suite 211, Edgecliff centre
203-233, New South Head Road
Tel (61-2) 327 39 22
Telex 071 126911 TCAUS
Telefax (61-2) 327 61 76

## HONG KONG

**WANCHAI**
22nd Floor - Hopewell centre
183 Queen's Road East
Tel (852-5) 8615788
Telex 60955 ESGIES HX
Telefax (852-5) 8656589

## INDIA

**NEW DELHI 110001**
LiasonOffice
62, Upper Ground Floor
World Trade Centre
Barakhamba Lane
Tel (91-11) 3715191
Telex 031-66816 STMI IN
Telefax (91-11) 3715192

## MALAYSIA

**PULAU PINANG 10400**
4th Floor - Suite 4-03
Bangunan FOP-123D Jalan Anson
Tel (04) 379735
Telefax (04) 379816

## KOREA

**SEOUL 121**
8th floor Shinwon Building
823-14, Yuksam-Dong
Kang-Nam-Gu
Tel (82-2) 553-0399
Telex SGSKOR K29998
Telefax (82-2) 552-1051

## SINGAPORE

**SINGAPORE 2056**
28 Ang Mo Kio - Industrial Park 2
Tel (65) 4821411
Telex RS 55201 ESGIES
Telefax (65) 4820240

## TAIWAN

**TAIPEI**
12th Floor
325 Section 1, Tun Hua South Road
Tel (886-2) 755-4111
Telex 10310 ESGIE TW
Telefax (886-2) 755-4008

# JAPAN

**TOKYO 108**
Nisseki - Takanawa Bld 4F
2-18-10 Takanawa
Minato-Ku
Tel (81-3) 3280-4121
Telefax (81-3) 3280-4131


ORDER CODE: DBCMOSBST/1