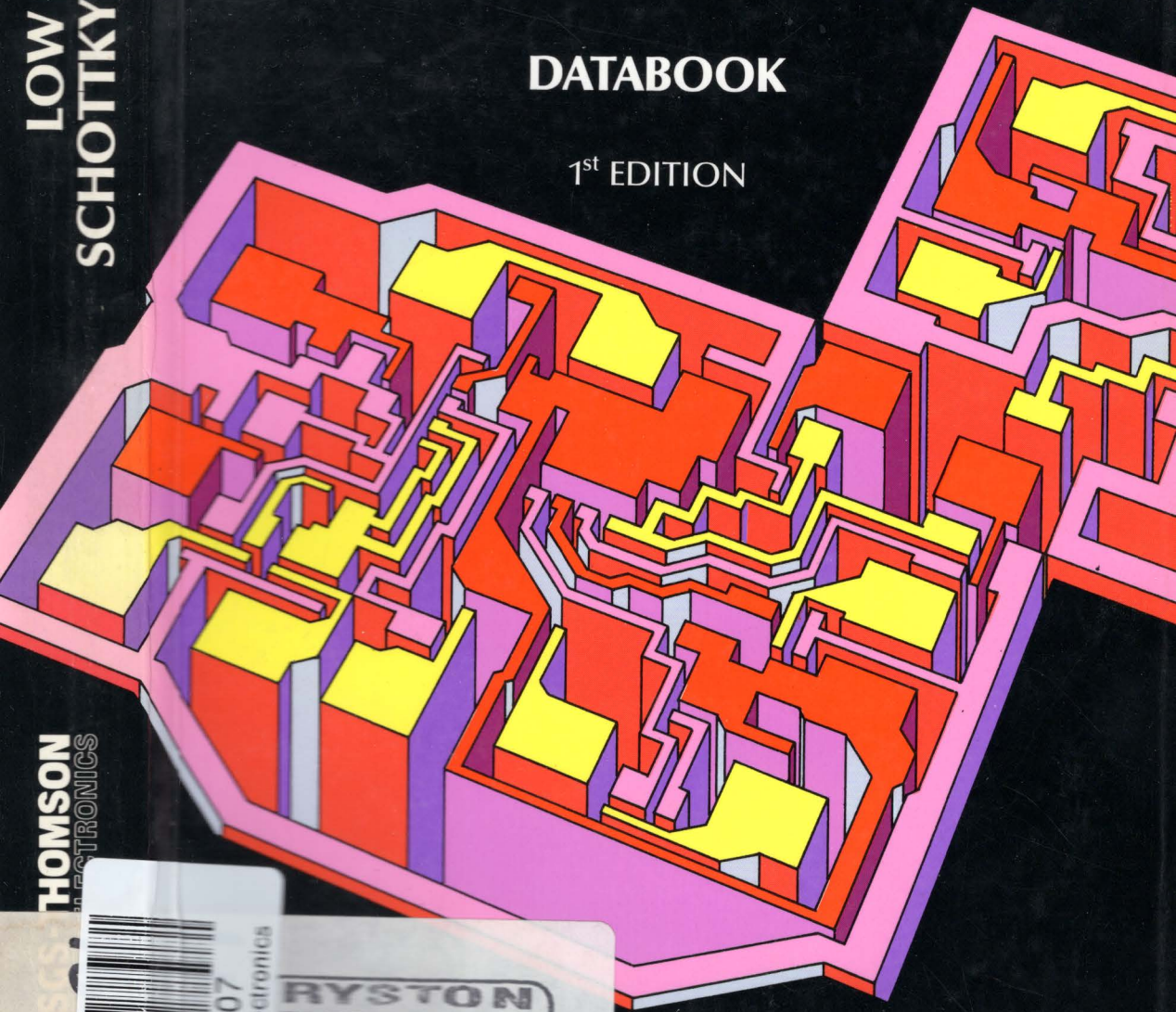
LOW POWER SCHOTTKY TTL ICs

DATABOOK

1st EDITION



SGS-THOMSON MICROELECTRONICS

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JUNE 1991

USE IN LIFE SUPPORT DEVICES OR SYSTEMS MUST BE EXPRESSLY AUTHORIZED

SGS-THOMSON PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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INTRODUCTION

Low Power Schottky integrated circuits are one of the three major logic families supplied in high volume by SGS-THOMSON. This databook contains datasheets on the companys range of Low Power Schottky ICs.

The information for each product, given in accordance with EIA/JEDEC specifications, has been specially presented in order that the performance of the product can be readily evaluated within any required equipment design.

The SGS-THOMSON range of packages includes all of the most commonly used plastic and ceramic dual-in-line as well as surface mounting packages. New developments in packaging include the PLCC package. As with all DIL packages all the surface out-line packages (SO) are made to JEDEC standards.

Additionally, general considerations that should be taken into account in the operation and application of Low Power Schottky integrated circuits are described.
Selection guides are included to simplify the task of choosing the best combination of circuits for a system.

The databook also contains the results of the reliability studies made by SGS-THOMSON of its Low Power Schottky devices.

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THE PRODUCT FEATURES

In the world of semiconductors, the TTL family has been for several years, one of the most diffused technologies in the field of integrated circuits. The Low Power Schottky technology represents the most successful evolution of the basic TTL. Its main advantages are:

– reduced chip size

– lower power dissipation
higher switching speed

Nowadays the LPS Family has substantially replaced the TTL Family, and it is the most diffused among bipolar digital ones. SGS-THOMSON is present in this field with a wide range of highly reliable TTL-LS products.
The TTL-LS devices are typically used in computer mainframes and peripherals, telecom equipment, industrial control systems, etc.

THE PRODUCT TECHNOLOGY

SGS-THOMSON has improved the already well known Schottky technology using the latest available facilities in design and in manufacturing. Our design "philosophy" is "quality oriented". This means that the lay-out rules give absolute priority to device quality, reliability and life-time.

The performance, the repeatability and the low leakage level of the principal parameters are fundamental principles in the philosophy of SGS-THOMSON. They are guaranteed by the use of advanced, fully automated equipment such as:

– ion implanters for all doping processes

– computer control and furnaces

– high precision projection mask aligners

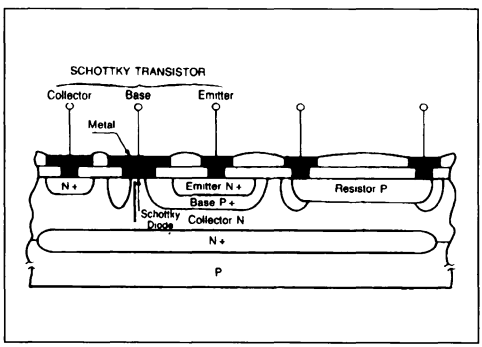
– wafer by wafer sputtering equipment
For the TTL-LS Family SGS-THOMSON is the first semiconductor manufacturer to use only 5" wafers with fully implanted doping processes. In this way, wafer handling is greatly reduced leading to a much higher level of quality and productivity.

The Low Power Schottky TTL family combines a current and power reduction by a factor 5, compared to 7400 TTL.

This is compled with anti-saturation Schottky diode clamping and advanced processing, using shallower diffusions and higher sheet resistivity to obtain circuit performances better than conventional TTL.

To the system designer the advantages of the TTL-LS family are many:

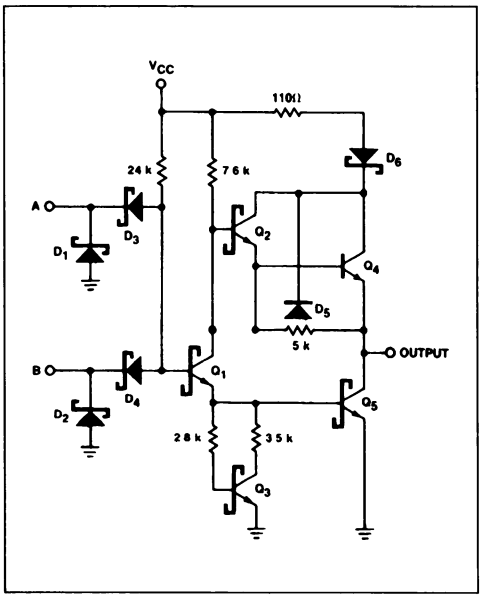
- Lower supply current allows smaller, cheaper power supplies, reducing equipment cost, size and weight.
- Lower power consumption means less heat is generated, which simplifies thermal design. Packing density can be increased or cooling requirements reduced, or perhaps both. The number of cooling fans can be reduced, or slower, quieter ones substituted.
- Reliability is enhanced, since lower dissipation causes less chip temperature rise above ambient; lower junction temperature increases MTBF. Also, lower chip current densities minimizes metal related failure mechanisms.
- Less noise is generated, since the improved transistors and lower operating currents lead to much smaller current spikes than standard TTL, which in turn means that fewer or smaller power supply decoupling capacitors are needed.
  In addition, load currents are only 25% of standard TTL and 20% of HTTL, which means that when a logic transition occurs, current changes along signal lines are proportionately smaller, as are the changes in ground current.
  Rise and fall times and thus wiring rules, are the same as for standard TTL and more relaxed than for HTTL or STTL.
- Simplified MOS to TTL interfacing is provided, since the input load current of LSTTL is only 25% of a standard TTL load.
- Ideally suited for CMOS to TTL interfacing. CMOS and most other 4000 or 74C CMOS are designed to drive one LS input load at 5.0V. The LS can also interface directly with CMOS operating up to 15V due to high voltage Schottky input diodes.
- Best TTL to MOS or CMOS driver. With the modest input current of MOS or CMOS as a load, any LS output will rise up to within 1V of V_{CC}, and can be pulled up to 10V with an external resistor.
- Interfaces directly with other TTL types, as indicated in the input and output loading tables.



Circuit Characteristics

The LS circuit features are most easily explained by using the 74LS00 2-input NAND gate as an example of the input/output circuits of all LS TTL. While the logic function and the basic structure of LS circuis are the same as conventional TTL, there are also significant differences, as we can see in Figure 1.

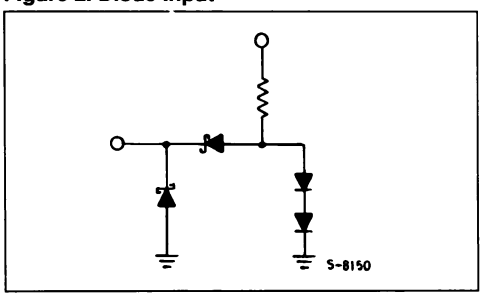
Figure 1.



Input Configuration

The various input configurations which SGS-THOMSON uses are described below.
The most common input configuration used by SGS-THOMSON in the LS family includes a Schottky Diode (see Fig. 2).

Figure 2. Diode Input



With respect to the standard multi-emitter this layout is much faster and has a high input breakdown voltage.
The circuits including an input diode have been tested for leakage with

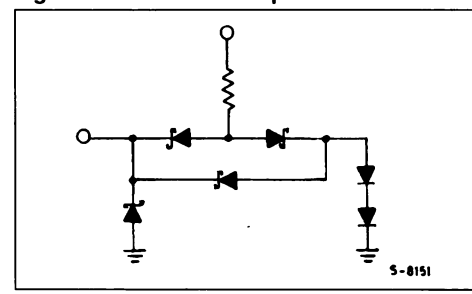
$$V_{IN}=7V$$

The voltage breakdown is typically 15V.
Fig. 7 shows the transfer characteristic of a gate with the structure of fig. 2.

The thereshold voltage is:

$$V_{TH} = 2V_{BE}-V_F \cong 1.05V$$
at: $T \cong 25°$

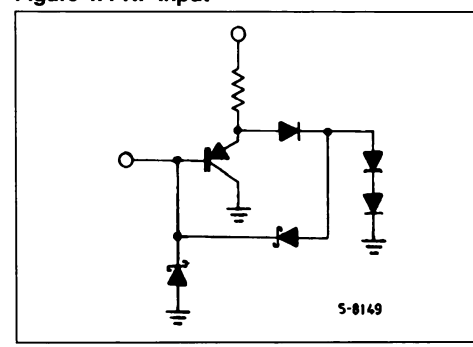
Figure 3. Diode Cluster Input



This configuration (see fig. 3) is incorporated in some circuits to slightly improve the V_{TH} with respect to the input diode configuration.
In this case the threshold voltage becomes.

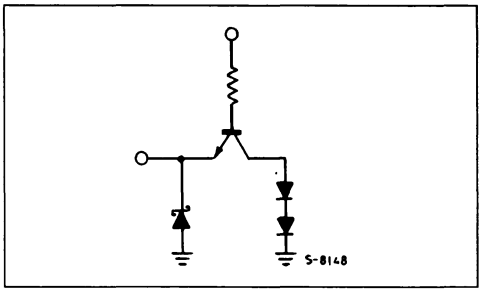
$$V_{TH} = 2V_{BE}.$$

Figure 4. PNP Input



This configuration (see fig. 4) is an improvement of the diode cluster. Besides $V_{TH} = 2V_{BE}$ there is also a reduction of the current supplied by the input. Here the equivalent input resistance is amplified by the gain of the transistor with respect to the input diode configuration.Therefore: $R_{IN(PNP)}=\beta mb_{(PNP)}xR_{IN}$

Figure 5. Emitter Inputs

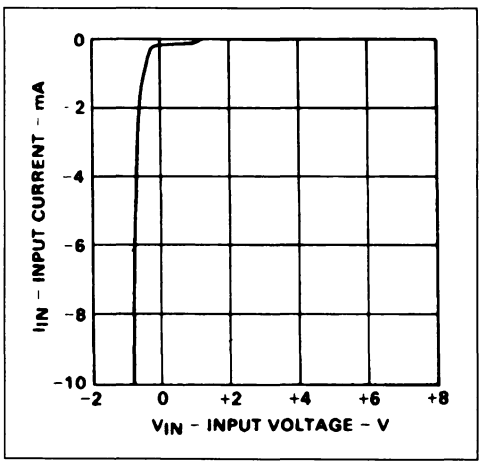


This is the standard layout (see fig. 5) used by the old TTL family this has both a breakdown voltage greater than 5.5V and a threshold voltage:

$$V_{TH}=2V_{BE}-V_{CESAT}$$

which is slightly higher than that of the input diode configuration. All the inputs described have a Schottky clamping diode which conducts when the input signal becomes negative. (Fig. 6)
This limits the undershoot and minimizes the ringing in long interconnections which work as transmission lines. This ringing could become significant when the delay along an interconnection is greater than a quarter of the fall time of the driving signal.
The clamping diode must be used only to sink the transient current and not for "steady state clamping". The effective input capacitance of an LS-TTL is 3.3 pF.
For each internal function driven by the input, 1.5pF is added.

Figure 6. Typical Input Current Voltage Characteristics

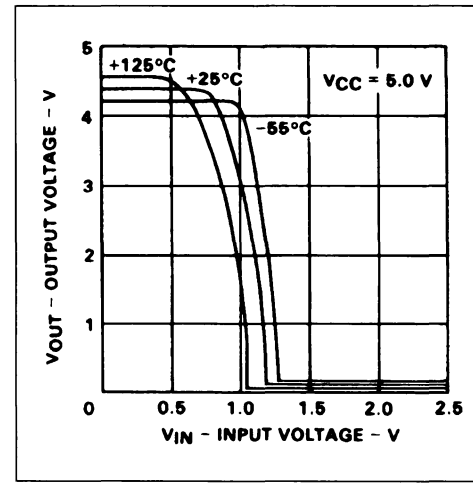


Output Configuration

The base of the pull-down output transistor is returned to ground through a resistor-transistor network instead of through a simple resistor. This squares up the transfer characteristics (see fig. 7) since it prevents conduction in the phase splitter until base current is supplied to the pull-down output transistor.

The "squaring network" improves the propagation delay be creating a path of low resistence to discharge the base capacitance of Q5 during turn-off. The output pull-up circuit is a 2-transistor Darlington circuit with the base of the output transistor returned through a 5kΩ resistor to the output terminal. This configuration allows the output to pull-up to one V_{BE} below V_{CC} for low values of output current.

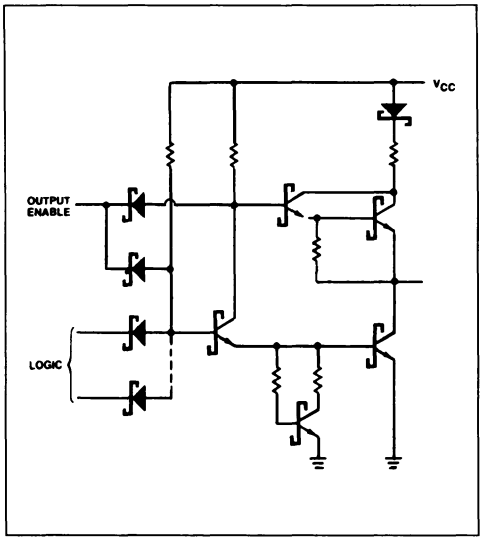
Figure 7. Typical Output Versus Input Voltage Characteristics



The LS outputs use a Schottky diode in series with the Darlington collector resistor. This diode allows the output to be pulled substantially higher than V_{CC} (e.g., to + 10V, convenient for interfacing with CMOS). For the same reason the parasitic diode of the base return resistor is connected to the Darlington common collector, not to V_{CC}.

Figure 8 shows the extra circuitry used to obtain the "high Z" condition in 3-state outputs. When the Output Enable signal is LOW, both the phase splitter and the Darlington pull-up are turned off. In this condition the output of 2 or more such circuits to be connected together in a bus application where only one output is enabled at any particular time.

Figure 8. Typical 3-State Output Control



Output Charateristics

Figure 9 shows the Low state output characteristics. For Low I_{OL} values, the pull-down transistor is clamped Out of deep saturation which contributes to speed. The curves also show the clamping effect when I_{OL} tends to go negative, as it often does due to reflections on a long interconnection after a negative-going transition.
This clamping effect helps to minimize ringing.

The waveform of a rising output signal resembles an exponential, except that the signal is slightly rounded at the beginning of the rise. Once past this initial rounded portion, the starting leading edge rate of rise is approximately 0.5 V/ns with a 15 pF load and 0.25V/ns with a 50pF load. For analytical purposes, the rising waveform can be approximated by the following expression.

$$v(t) = V_{OL} + 3.7\,[1 - \text{esp}\,(-t/T)]$$

where

$$T = 8 \text{ ns for } C_L = 15\text{pF}$$
$$= 16 \text{ ns for } C_L = 50\text{pF}$$

The waveform of a falling output signal resembles that part of a cosine wave between the angles o 0° and 180°.
Fall times from 90% to 10% are approximately 4.5 ns with a 15pF load and 8.5ns with a 50pF load. Equivalent edge rates are approximately 0.8 V/ns and 0.4 V/ns, respectively. For analytical purposes, the falling waveform can be approximated by the following expression.

$$v(t) = V_{OL} + 1.9\mu(t)[1 + \cos\omega t] - 1.9\,\mu\,(t-a)[1 + \cos\omega(t-a)]$$

where	For t in nanoseconds
$\mu(t)= 0$ for $t < 0$	and C_L = 15 pF
$= 1$ for $t > 0$	a = 7.5ns, ω = 0.42
and	For C_L = 50 pF
$\mu(t-a)= 0$ for $t < a$	a = 14ns, ω = 0.23
$= 1$ for $t > a$	

Figure 9. Typical Output Current - Voltage Characteristics

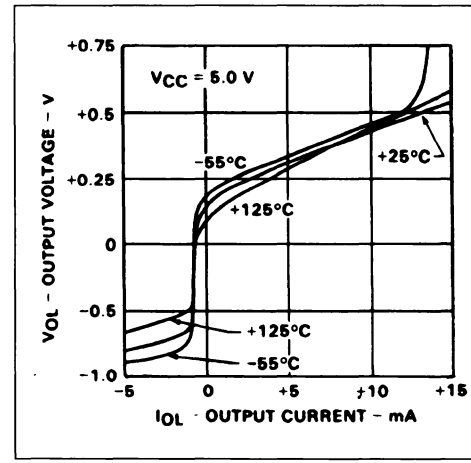
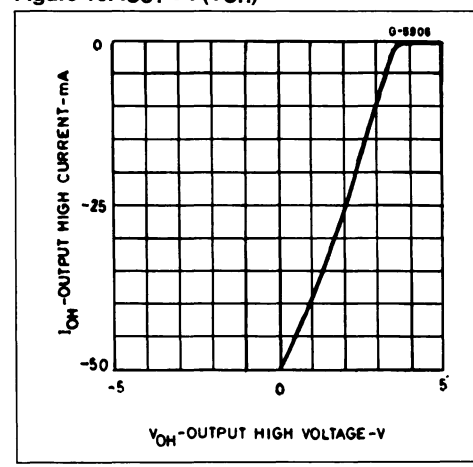


Figure 10. $I_{OUT} = F(V_{OH})$



AC Switching Characteristics

The average propagation delay of a Low Power Schottky gate is 5 ns at a load of 15 pF as shown in Figure 11. The delay times increase at an average of 0.08 ns/pF for larger values of capacitive load. These delay times are relatively insensitive to variations in power supply and temperature. The average propagation delay time changes less than 1.0ns over temperature range and less than 0.5 ns with V_{CC} for the military temperature and voltage ranges. (See Figures 12 and 13).

Figure 11. Typical Propagation Delay Versus Load Capacitance

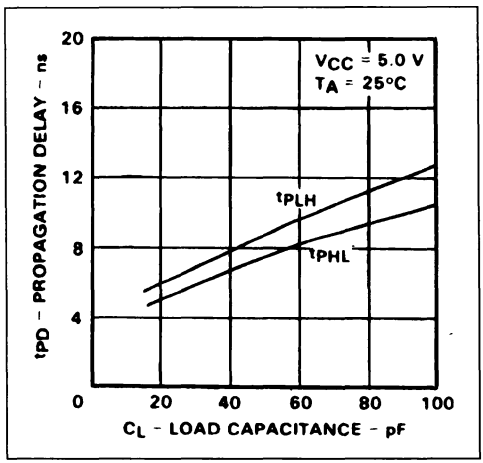


Figure 12. Propagation Delay Change with Temperature

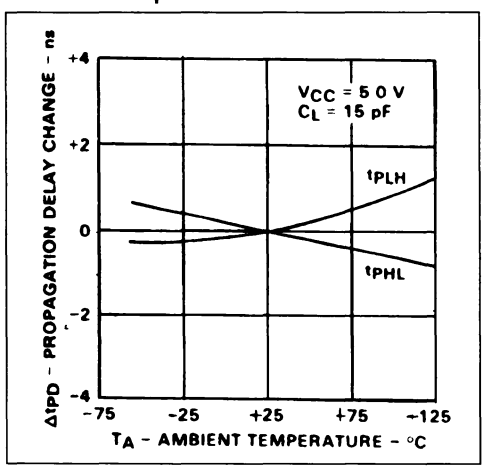
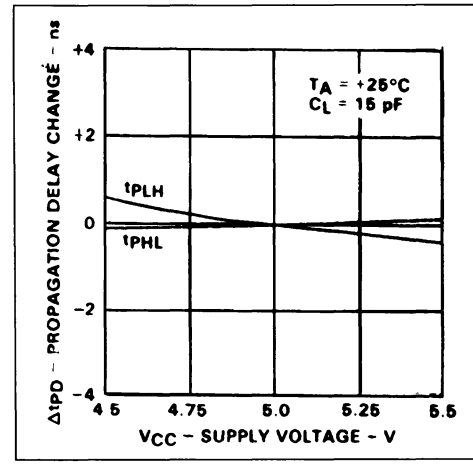


Figure 13. Propagation Delay Change Supply Voltage



DC SYMBOLS AND DEFINITIONS

VOLTAGES - All voltages are referenced to ground. Negative voltage limits are specified as absolute values (i,e, – 10 V is greater thant – 1.0 V).

CURRENTS - Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified absolute values.

V_{CC}	**Supply voltage** - The range of power supply voltage over which the device is guaranteed to operate within the specified limits.
$V_{CD(MAX)}$	**Input clamp diode voltage** - The most negative voltage at an input when 18 mA is forced out of that input terminal. This parameter guarantees the integrity of the input diode which is intended to clamp negative ringing at the input terminal.
V_{IH}	**Input HIGH voltage** - The range of input voltages that represents a logic HIGH in the system.
$V_{IH(MIN)}$	**Minimum input HIGH voltage** - The minimum allowed input HIGH in a logic system. This value represents the guaranteed input HIGH threshold for the device.
V_{IL}	**Input LOW voltage** - The range of input voltages that represents a logic LOW in the system.
$V_{IL(MAX)}$	**Maximum input LOW voltage** - The maximum allowed input LOW in a system. This value represents the guaranteed input LOW threshold for the device.
$V_{OH(MIN)}$	**Output HIGH voltage** - The minimum voltage at an output terminal for the specified output current I_{OH} and the minimum value of V_{CC}.
$V_{OL(MAX)}$	**Output LOW voltage** - The maximum voltage at an output terminal sinking the maximum specified load current I_{OL}.
V_{T+}	**Positive-going threshold voltage** The input voltage of a variable threshold device (i.e., Schmitt Trigger) that is interpreted as a V_{IH} as the input transition rises from below $V_{T-(MIN)}$.
V_{T-}	**Negative-going threshold voltage** The input voltage of a variable threshold device (i.e. Schmitt Trigger) that is interpreted as a V_{IL} as the input transition falls from above $V_{T+(MAX)}$.
I_{CC}	**Supply current** - The current flowing into the V_{CC} supply terminal of a circuit with the specified input conditions and the outputs open. When not specified, input conditions are chosen to guarantee worst case operation.
I_{IH}	**Input HIGH current** - The current flowing into an input when a specified HIGH voltage is applied.
I_{IL}	**Input LOW current** - The current flowing out of an input when a specified LOW voltage is applied.
I_{OH}	**Output HIGH current** - The leakage current flowing into a turned off open collector output with a specified HIGH output voltage applied. For devices with a pull-up circuit, the I_{OH} is the current flowing out of an output which is in the HIGH state.
I_{OL}	**Output LOW current** - The current flowing into an output which is in the LOW state.
I_{OS}	**Output short circuit current** The current flowing out of an output which is in the HIGH state when that output is short circuit to ground (or other specified potential).
I_{OZH}	**Output off current HIGH** - The current flowing into a disabled 3-state output with a specified HIGH output voltage applied.
I_{OZL}	**Output off current LOW** - The current flowing out of a disabled 3-state output with a specified LOW output voltage applied.

AC SWITCHING PARAMETERS

f_{MAX}	**Troggle frequency/operating frequency** - The maximum rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.
t_{PLH}	**Propagation delay time** - The time between the specified reference points, normally 1.3V on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level.
t_{PHL}	**Propagation delay time** - The time between the specified reference points, normally 1.3V on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level.
t_W	**Pulse width** - The time between 1.3 V amplitude points on the leading and trailing edges of a pulse.
t_h	**Hold time** - The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.
t_S	**Set-up time** - The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{PHZ}	**Output disable time (of a 3-state output) from LOW level** - The time between the 1.3 V on the input and a voltage 0.5 V below the steady state output HIGH level with the 3-state output changing from the defined HIGH level to a high-impedance (off) state.
t_{PLZ}	**Output disable time (of a 3-state output) from LOW level** - The time between the 1.3 V level on the input and a voltage 0.5 V above the steady state output LOW level with the 3-state output changing from the defined LOW level to a high-impedance (off) state.
t_{PZH}	**Output enable time (of a 3-state output) to a HIGH level** - The time between the 1.3 V levels of the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to a HIGH level.
t_{PZL}	**Output enable time (of a 3-state output) to a LOW level** - The time between the 1.3 V levels of the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to a LOW level.
t_{rec}	**Recovery time** - The time between the 1.3 V level on the trailing edge of an asynchronous input control pulse and the 1.3 V level on a synchronous input (clock) pulse such that the device will respond to the synchronous input.

SUPPLY VOLTAGE AND TEMPERATURE RANGE

The nominal supply voltage (V_{CC}) for all TTL circuits is +5.0V. Commercial grade parts are guaranteed to perform with a ±5% supply tolerance (±250 mV) over an ambient temperature range of 0°C to 75°C.

MIL-grade parts are guaranteed to perform with a ±10% supply tolerance (±500 mV) over an ambient temperature range –55°C to +125°C.

TTL families may be mixed for optimum system design. The following table specify the worst case noise immunity in mixed systems.

WORST CASE TTL DC NOISE IMMUNITY/NOISE MARGINS

Electrical Characteristics											
Item	Symbol	SGS-THOMSON TTL Families	Military (– 55 to +125°C)				Commercial (0 to 75°C)				Units
			V_{IL}	V_{IH}	V_{OL}	V_{OH}	V_{IL}	V_{IH}	V_{OL}	V_{OH}	
6	TTL	Standard TTL (54/74)	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
7	HTTL	High Speed TTL (54H/74H)	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
10	LSTTL	Low Power Schottky TTL (54LS/74LS)	0.7	2.0	0.4	2.5	0.8	2.0	0.5	2.7	V

V_{OL} and V_{OH} are the voltages generated at the output. V_{IL} and V_{IH} are the voltage required at the input to generate the appropriate output levels. The numbers given above are guaranteed worst-case values.

LOW Level Noise Margins (Military)				
From \ To	TTL	HTTL	LSTTL	Units
TTL	400	400	300	mV
HTTL	400	400	300	mV
LSTTL	400	400	300	mV

From "V_{OL}" to "V_{IL}"

LOW Level Noise Margins (Commercial)				
From \ To	TTL	HTTL	LSTTL	Units
TTL	400	400	400	mV
HTTL	400	400	400	mV
LSTTL	300	300	300	mV

From "V_{OL}" to "V_{IL}"

HIGH Level Noise Margins (Military)				
From \ To	TTL	HTTL	LSTTL	Units
TTL	400	400	400	mV
HTTL	400	400	400	mV
LSTTL	500	500	500	mV

From "V_{OH}" to "V_{IH}"

LOW Level Noise Margins (Commercial)				
From \ To	TTL	HTTL	LSTTL	Units
TTL	400	400	400	mV
HTTL	400	400	400	mV
LSTTL	700	700	700	mV

From "V_{OH}" to "V_{IH}"

FAN-IN AND FAN-OUT

In order to simplify designing with SGS-THOMSON LSTTL devices, the input and output loading parameters of all families are normalized to the following values:

1 TTL Unit Load (U.L.) = 40µA in the HIGH state (Logic "1")

1 TTL Unit Load (U.L.) = 1.6 mA in the LOW state (logic "0")

Input loading and output drive factors of all products described in this handbook are related to these definitions.

Examples-Input Load

1. A 7400 gate, wich has a maximum I_{IL} of 1.6 mA and I_{IH} of 40 µA is specified as having an input load factor of 1 U.L. (Also called a fan-in of 1 load).
2. The 74LS95 which has a value of I_{IL} = 0.8 mA and I_{IH} of 40 µA on the CP terminal, is specified as having an input LOW load factor of

$$\frac{0.8mA}{1.6mA} \text{ or } 0.5 \text{ U.L.}$$

and an input HIGH load factor of

$$\frac{40\mu A}{40\mu A} \text{ or } 1 \text{U.L.}$$

3. The 74LS00 gate which has an I_{IL} of 0.36 mA and an I_{IH} of 20 µA, has input LOW load factor of

$$\frac{0.36mA}{1.6mA} \text{ or } 0.225 \text{U.L.}$$

(normally rounded to 0.25 U.L.) and an input HIGH load factor of

$$\frac{20\mu A}{40\mu A} \text{ or } 0.5 \text{ U.L.}$$

Examples-Output Drive

1. The output of the 7400 will sink 16 mA in the LOW (logic "0") state and source 800µA in the HIGH (logic "1") state. The normalized output LOW drive factor is therefore

$$\frac{16mA}{1.6mA} = 10 \text{U.L.}$$

and the output HIGH drive factor is

$$\frac{800\mu A}{40\mu A} \text{ or } 20 \text{ U.L.}$$

2. The output of the 74LS00 (Commercial Grade) will sink 8.0 mA in the LOW state and source 400 µA in the HIGH state. The normalized output LOW drive factor is

$$\frac{80mA}{1.6mA} \text{ or } 5 \text{ U.L.}$$

and the output HIGH drive factor is

$$\frac{400\mu A}{40\mu A} \text{ or } 10 \text{ U.L.}$$

Relative load and drive factors for the basic TTL families are given in Table 1.

Table 1

Family	Input Load		Output Drive	
	High	Low	High	Low
74LS00	0.5 U.L.	0.25 U.L.	10 U.L.	5 U.L.
7400	1 U.L.	1 U.L.	20 U.L.	10 U.L.
9000	1 U.L.	1 U.L.	20 U.L.	10 U.L.
74H00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.
74S00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.

Values for MSI devices vary significant from one element to another Consult the appropriate data sheet for actual characteristics.

WIRED-OR APPLICATIONS

Certain TTL devices are provided with an "open" collector output to permit the Wired-OR (actually Wired-AND) function. This is achieved by connecting open collector outputs together and adding an external pull-up resistor.

The value of the pull-up resistor is determined by considering the fan-out of the OR tie and the number of devices in the OR tie.
The pull-up resistor value is chosen from a range between a maximum value (established to maintain the required V_{OH} with all the OR tied outputs HIGH) and a minimum value (established so that the OR tie fanout is not exceeded when only one output is LOW).

Minimum and Maximum Pull-Up Resistor Values

$$R_{X(MIN)} = \frac{V_{CC(MAX)} - V_{OL}}{I_{OL} - N_{2(LOW)} \cdot 1.6mA}$$

$$R_{X(MAX)} = \frac{V_{CC(MIN)} - V_{OH}}{N_1 \cdot I_{OH} + N_{2(HIGH)} \cdot 40\mu A}$$

where

R_X = External Pull-up Resistor

N_1 = Number of Wired-OR Outputs

N_2 = Number of Input Unit Loads being Driven

$I_{OH}=I_{CEX}$ = Output HIGH Leakage Current

I_{OL} = LOW Level Fan-out Current of Driving Element

V_{OL} = Output LOW Voltage Level (0.5V)

V_{OH} = Output HIGH Voltage Level (2.4V)

V_{CC} = Power Supply Current

Example: Four 74LS03 gate outputs driving four other 74LS gates or MSI inputs.

$$R_{X(MIN)} = \frac{5.25V - 0.5V}{8mA - 1.6mA} = \frac{4.75V}{6.4mA} = 742\ \Omega$$

$$R_{X(MIN)} = \frac{4.75V - 2.4V}{4 \cdot 100\mu A + 2 \cdot 40\mu A} = \frac{2.35V}{0.48mA} = 4.9K\Omega$$

where

$N_1 = 4$

$N_{2(HIGH)} = 4 \cdot 0.5$ U.L. $= 2$ U.L.

$N_{2(LOW)} = 4 \cdot 0.25$ U.L. $= 1$ U.L.

$I_{OH} = 100\ \mu A$

$I_{OL} = 8$ mA

$V_{OL} = 0.5V$

$V_{OH} = 2.4V$

Any value of pull-up resistor between 742 Ω and 4.9 kΩ can be used. The lower values yield the fastest speeds while the higher values yield the lowest power dissipation.

UNUSED INPUTS

For best noise immunity and switching speed, unused TTL inputs should not be left floating, but should be held between 2.4V and the absolute maximum input voltage.

Two possible ways of handing unused inputs are:

1. Connect unused input to V_{CC}. Most 74LS inputs have a breakdown voltage >15V and require, therefore, no series resistor. For all multi-emitter conventional TTL inputs, a 1 to 10kΩ current limiting series resistor is recommended, to protect against V_{CC} transients that exceed 5.5V.

2. Connect the unused input to the output of an unused gate that is forced HIGH.

CAUTION: *Do not connect an unused LSTTL input to another input of the same NAND or AND function. This method, recommended for normal TTL, increases the input coupling capacitance and thus reduces the ac noise immunity.*

INTERCONNECTION DELAYS

For those parts of a system in which timing is critical, designers should take into account the finite delay along the interconnections. These range from about 0.12 to 0.15 ns/inch for the type of interconnections normally used in TTL systems. Exceptions occur in system using ground planes with STTL to reduce ground noise during a logic transition; ground planes give higher distributed capacitance and delays of about 0.15 to 0.22 ns/inch.

Most interconnections on a logic board are short enough that the wiring and load capacitance can be treated as a lumped capacitance for purposes of estimating their effect on the propagation delay of the driving circuit.

When an interconnection is long enough that its delay is one-fourth to one-half of the signal transition time, the driver output waveform exhibits noticeable slope changes during a transition. This is evidence that during the initial portion of the output voltage transition the driver sees the characteristic impedance of the interconnection (normally 150Ω to 200Ω), which for transient conditions appears as a resistor returned to the quiescent voltage existing just before the beginning of the transition. This characteristic impedance forms a voltage divider with the driver output impedance, tending to produce a signal transition having the same rise or fall time as in the no-load condition but with a reduced amplitude. This attenuated signal travels to the far end of the interconnection, which is essentially an unterminated transmission line, whereupon the signal starts doubling. Simultaneously, a reflection voltage is generated which has the same amplitude and polarity as the original signal, e.g., if the driver output signal is positive-going the reflection will be positive-going, and as it travels back toward the driver it adds to the line voltage. At the instant the reflection arrives at the driver it adds algebraically to the still-rising driver output, accelerating the transition rate and producing the noticeable change in slope.

If an interconnection is of such length that its delay is longer than half the signal transition time, the attenuated output of the driver has time to reach substantial completion before the reflection arrives. In the limit, the waveform observed at the driver output is a 2-step signal with a pedestal. In this circumstance the first load circuit to receive a full signal is the one at the far end, because of the doubling effect, while the last one to receive a full signal is the one nearest the driver since it must wait for the reflection to complete the transition. Thus, in a worst-case situation, the net contribution to the overall delay is twice the delay of the interconnection because the initial part of the signal must travel to the far end of the line and the reflection must return.

When load circuits are distributed along an interconnection, the input capacitance of each will cause a small reflection having a polarity opposite that of the signal transition, and each capacitance also slows the transition rate of the signal as it passes by. The series of small reflections, arriving back at the driver, is subtractive and has the effect of reducing the apparent amplitude of the signal. The successive slowing of the transition rate of the transmitted signal means that it takes longer for the signal to rise or fall to the threshold level of any particular load circuit. A rough but workable approach is to treal the load capacitances as an increase in the intrinsic distributed capacitance of the interconnection. Increasing the distributed capacitance of a transmission line reduces its impedance and increases its delay. A good approximation for ordinary TTL interconnections is that distributed load capacitance decreases the characteristic impedance by about one-third and increases the delay by one-half.

Another advantage of LSTTL has to do with its output impedance during a positive-going transition. Whereas the low output impedance of STTL and HTTL allows these circuits to force a larger initial swing into a low impedance interconnection, the low output impedance also has a disadvantage. It makes the reflection coefficient negative at the driven end of the interconnection, a situation that exists any time a transmission line is terminated by an impedance lower than its characteristics impedance. This means that when the reflection from the (essentially) open end of the interconnection arrives back at the driver it will be re-reflected with the opposite polarity. The result is a sequence of reflected signal which alternate in sign and decrease in magnitude, commonly known as ringing. The lower the driver output impedance, the greater the amplitude of the ringing and the longer it takes to damp out.

The output impedance of LSTTL, on the other hand, is closer to the characteristic impedance of the interconnections commonly used with TTL, and ringing is practically non existent. Thus no special packaging is required. This advantage, combined with excellent speed, modest edge rates and very low transient currents, are some of the reasons that designers have found LSTTL extremely easy to work with and very cost effective.

METASTABLE CHARACTERISTIC

When a setup, hold or recovery time is violated, the response of a flip-flop is uncertain. Reliable operation under this condition cannot be guaranteed, since there is the probability that the output locks in the metastable region for a certain period.
The metastable state is defined as that time period in which the output level is not at logic "0" nor at logic "1", but stays in the region between 0.8 and 2V.

The following test circuits and conditions represent SGS's-THOMSON typical AC test procedures. The output loading for standard Low Power Schottky devices is a 15 pF capacitor. Experimental evidence shows that test results using the additional diode-resistor load are within 0.2 ns of the capacitor only load.

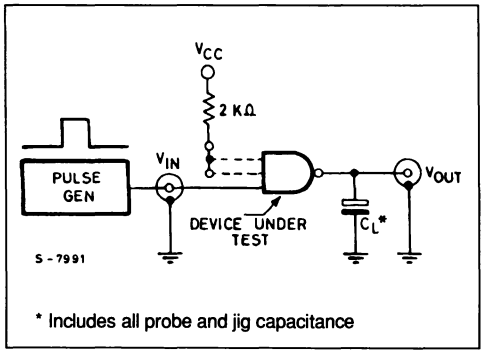
The capacitor only load also has the advantage of repeatable, easily correlated test results. The input pulse rise and fall times are specified at 6 ns to closely approximate the Low Power Schottky output transitions through the active threshold region.

The specified propagation delay limits can be guaranteed with a 15 ns input rise time on all parameters except those requiring narrow pulse widths. Any frequency measurement over 15MHz or pulse width less than 30 ns must be performed with a 6 ns input rise time.

Pulse Generator Settings (unless otherwise specified)

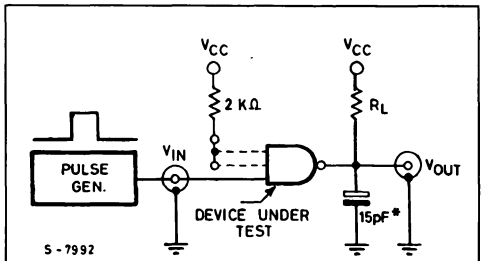
Frequency = 1MHz
Duty Cycle = 50%
t_{TLH}(t_{rise}) = 6ns
t_{THL}(t_{fall}) = 6ns
Amplitude = 0 to 3V

Test Circuit for Standard Output Devices



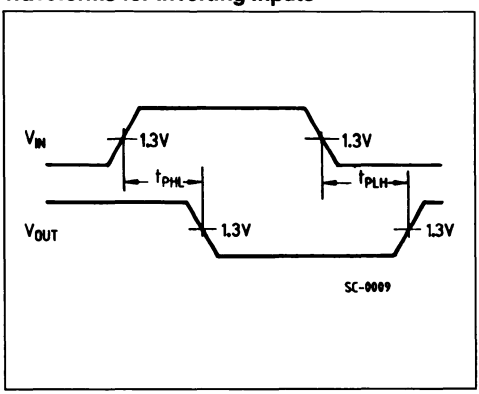
* Includes all probe and jig capacitance

Test Circuit for Open Collector Output Devices

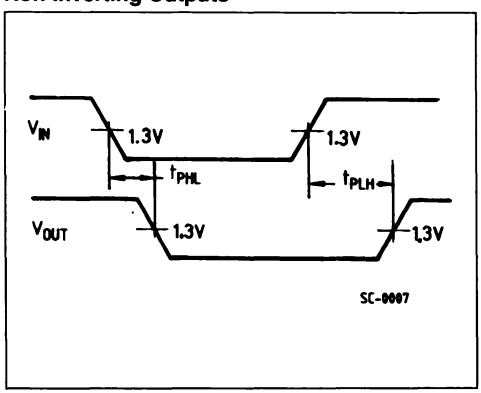


* Includes all probe and jig capacitance

Waveforms for Inverting Inputs



Non-Inverting Outputs



3-STATE

Fig. 1

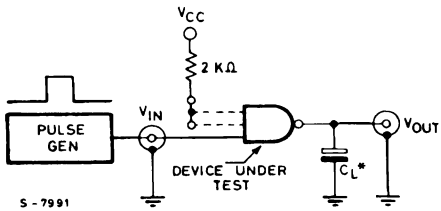


Fig. 2

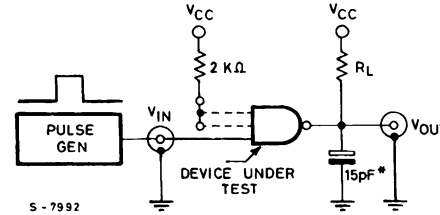


Fig. 3

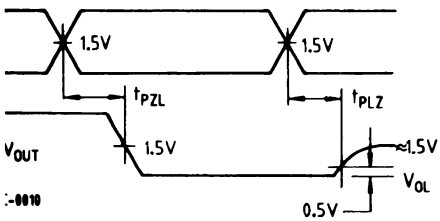


Fig. 4

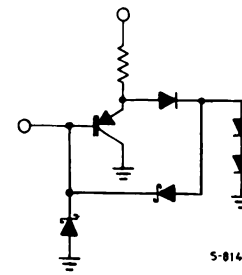
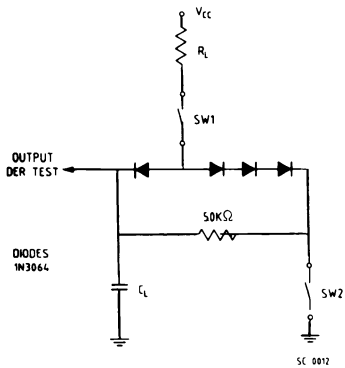


Fig. 5



SWITCHING POSITIONS

Symbol	SW1	SW2
tPZH	Open	Closed
tPZL	Closed	Open
tPLZ	Closed	Closed
tPHZ	Closed	Closed

RELIABILITY REPORT

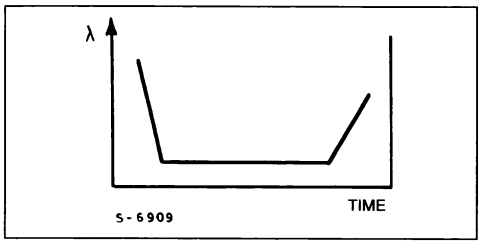
RELIABILITY AND FAILURE MECHANISMS

FUNDAMENTALS

-Through accelerated stresses we ascertain the value of the components failure rates, in terms of how many devices (in percent) are expected to fail every 1000 hours of operation (λ or F.R.)

-Failure rate versus time of activity shows the well-known trend.

-Failure rate



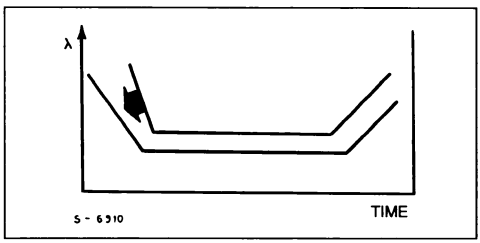
During the first time period the products are affected by the so-called "infant mortality" intrinsic to all semiconductor technologies. End users are very sensitive to this parameter which causes early operational failures in their equipment.

TARGETS

SGS-THOMSON periodically reviews and publishes lifetime results; at this time a new set of failure rate targets are being defined. These targets are translated into actual required test hours.

The goal is a steady shift of the limits.

Failure rate λ



TESTS

With accelerated tests we define the failure rate of the products, then, derating the data for different conditions, we know the life expectancy under the actual operating conditions.

In its simplest form the failure rate (at a given temperature) is:

$$F.R. = \frac{N}{D \cdot H} \qquad (1)$$

Where N = Number of failures
D = Number of components
H = Number of testing hours

If we intend to determine the failure rate at other temperatures an acceleration factor must be considered.
Some tests are accelerated by means of increased temperature, based on the assumption of the Arrhenius law:

$$F.R. = Ae^{-Ea/KTj} \qquad (2)$$

A = Constant

Ea = Activation energy

K = Boltzman's constant

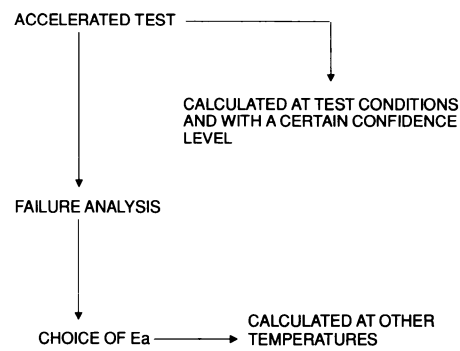
Tj = Junction Absolute temperature

For two different temp. $F.R.(T_1)=F(T_1, T_2)F.R.(T_2)$

from (2) it is: $$F(T_1,T_2) \equiv EXP\left[\frac{-Ea}{K}\left(\frac{1}{T_1}-\frac{1}{T_2}\right)\right] \quad (3)$$

Clearly the choice of an appropriate activation energy, Ea is of paramount importance.
The different mechanisms which could lead to circuit failure are characterized by specific activation energies whose values are published in the relevant literature.

THUS THE CORRECT PROCEDURE IS



Arrhenius equation (2) describes the rate of many processes responsible for degradation and failure of electronic components; it follows that if the transition of an item from an initial stable condition to a defined degraded state occurs by a thermally activated mechanism, then the time for the transition is given by an equation of the form:

MTBF = B EXP (Ea/Kt)

MTBF = Mean time between failure

B = Temperature-independent constant

MTBF can be defined as the time to suffer a device degradation. The dramatic effect of the choice of the Ea value can be seen by plotting equation (2).

The acceleration effect of a 125°C device junction test with respect to 70°C actual device junction operation is equal to a factor of 100 for Ea = 1eV and respectively 4 for Ea = 0.3eV.

Some words of caution are needed about published values of Ea:

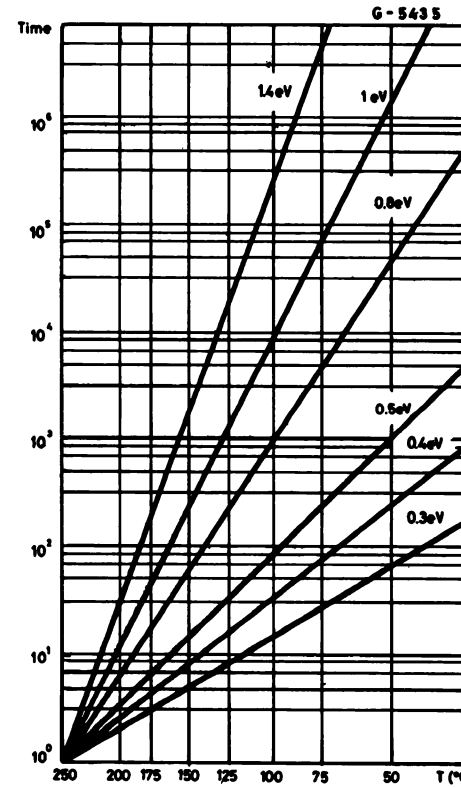
A)They are often related to high temperature test where a single Ea (with high value) mechanism has become significant.

B)They are specifically related to the devices produced by that supplier (and to its technology) and in that period of time.

C)They could be modified by the mutual action of other stresses (voltage, mechanical)

D)Field device-application conditions should be considered.

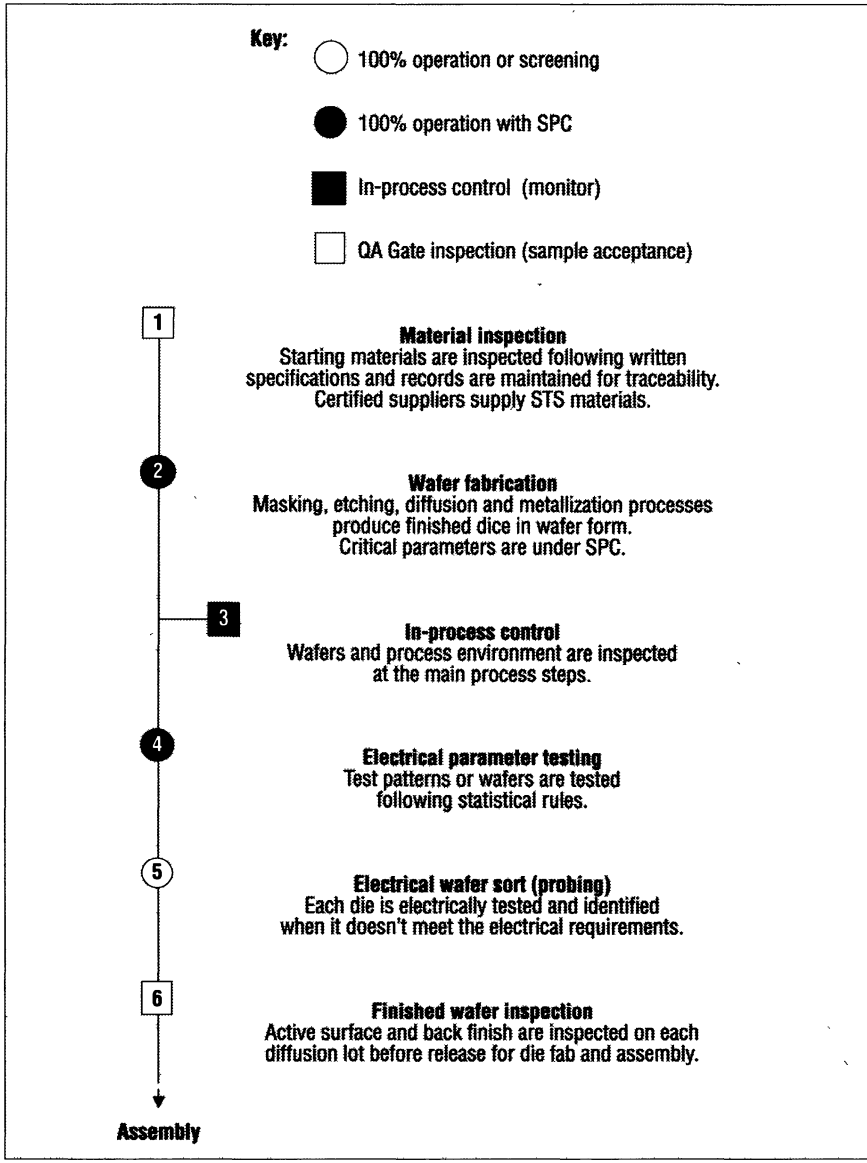
Life-Hours



Main Failure modes and relevant activation energies

Failure Mode	Activation Energy (eV)	Accelerating
SURFACE CHARGE	1.0 - 1.05	HIGH TEMPERATURE BIAS
IONIC CONTAMINATION	1.0 - 1.4	HIGH TEMPERATURE BIAS
DIELECTRIC DEFECTS	0.3 - 0.6	HIGH TEMPERATURE BIAS
ELECTROMIGRATION	0.5 - 1.2	HIGH TEMPERATURE BIAS
INTERMETALLIC GROWTH	1.0 - 1.05	HIGH TEMPERATURE BIAS, STORAGE
METAL CORROSION	0.3 - 0.8	HIGH HUMIDITY BIAS

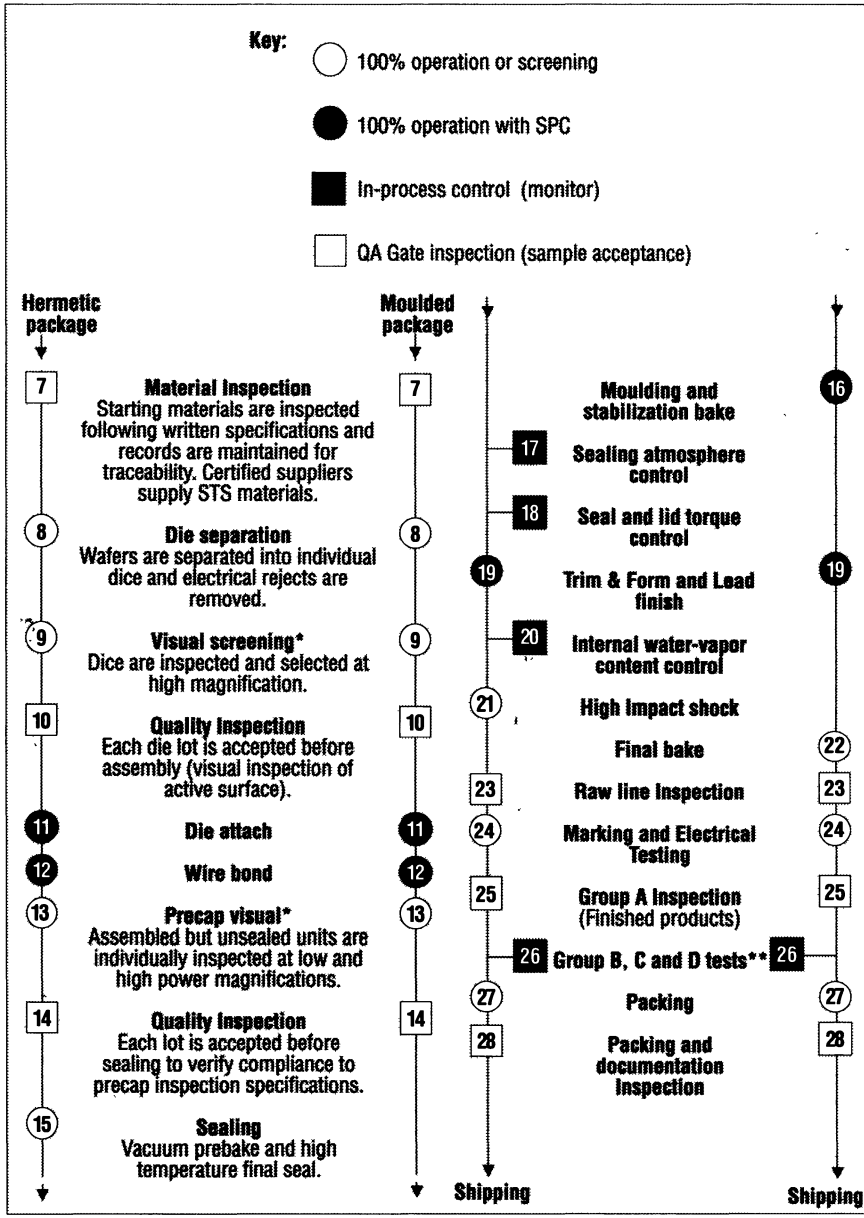
WAFER FAB TYPICAL PRODUCTION PROCESS FLOW CHART



In-process control during wafer fabrication
The table emphasizes the most important fabrication steps with the relevant SPC measures and/or monitors performed.

PROCESS STEPS	IN-PROCESS INSPECTIONS/MONITORS
OXIDATION	– Visual – Thickness – Refractive Index – CV plot (stability of ionic concentration and contamination control)
DEPOSITION: Nitride, Poly Si	– Visual – Thickness – Refractive index – Doping content
PHOTOLITHOGRAPHY	– Mask and wafer cleanliness – Alignment and focusing accuracy – Critical dimensions
ETCHING	– Quality of etching and wafer cleanliness – Critical dimensions
DOPING BY IMPLANT (P, As, B)	– Sheet resistance (dose and implant uniformity)
DOPING BY DIFFUSION ($POCl_3$, As)	– Sheet resistance – Thickness – CV plot (stability of ionic concentration and contamination control)
EPITAXIAL GROWTH	– Thickness – Resistivity – Crystal quality (stacking faults, bumps and others)
METALLIZATION	– Wafer cleanliness – Visual – SEM (step coverage and film quality) – Thickness – CV plot (stability of ionic concentration and contamination control)
INTERMEDIATE AND FINAL PASSIVATION	– Thickness – Doping content – Passivation integrity (density of pinholes and cracks) – Visual
BACK FINISHING	– Wafer thickness – Back metal thickness – Metal adherence
ELECTRICAL CHARACTERIZATION	– Main parameters for active and parasitic structures (e. g. threshold voltage, saturation current, h_{FE}, resistances, capacitances ...)
WAFER INSPECTION	– Visual (microscope and/or laser surface inspection system)
ALL DEPOSITIONS AND PHOTOLITHOGRAPHY	– Surface Scan (to detect and to measure foreign particles)

ASSEMBLY TYPICAL PRODUCTION PROCESS FLOW CHART



* Omitted when the intrinsic quality meets the specified quality level
** For non military products, these reliability tests can be performed after step 23 on 100% electrically tested samples (when requested)

In-process control during assembly process

The table emphasizes the most important fabrication steps with the relevant SPC measures and/or monitors performed.

PROCESS STEPS	TESTS	DESCRIPTION
11	DIE ATTACH	–Integrated Circuits MIL-STD-883 Method 2010 cond B (internal visual) and Method 2019 (die shear strength); CECC 90000 –Discrete Devices MIL-STD-750 Method 2072 (internal visual) and Method 2017 (die shear strength); CECC 50000
12	WIRE BOND	– Integrated Circuits MIL-STD-883 Method 2010 cond. B (internal visual) and Method 2011 cond. D (bond strength); CECC 90000 – Discrete Devices MIL-STD-750 Method 2072 (internal visual) and Method 2037 (bond strength); CECC 50000
14	QUALITY INSPECTION	– Integrated Circuits MIL-STD-883 Methods 2010 cond. B (internal visual); CECC 90000 –Discrete Devices MIL-STD-750 Method 2072 (internal visual); CECC 50000
16	MOULDING AND STABILIZATION BAKE	– Visual and temperature process control
17	SEALING ATMOSPHERE CONTROL	Moisture content: < 200 ppm for Ceramic packages < 100 ppm for Metal Can packages
18	SEAL CONTROL	Fine Leak – Integrated Circuits MIL-STD-883 Method 1014 cond. A1 Helium leak detector after pressurization in He for: 2h at 5.1 atm Limit: 5×10^{-8} cc/s for ICV < 0.05 cc 4h at 5.1 atm Limit: 5×10^{-8} cc/s for ICV ≥ 0.05 < 0.5 cc 2h at 3.0 atm Limit: 1×10^{-7} cc/s for ICV ≥ 0.5 < 1cc 5h at 3.0 atm Limit: 5×10^{-8} cc/s for ICV ≥ 1 < 10cc ICV = Internal Cavity Volume – Discrete Devices MIL-STD-750 Method 1071 cond. H1 Helium leak detector after pressurization in He for: 2h at 4.1 atm Limit: 5×10^{-8} cc/s for ICV < 0.4 cc 2h at 4.1 atm Limit: 2×10^{-7} cc/s for ICV ≥ 0.4 cc 4h at 2.0 atm Limit: 1×10^{-7} cc/s for ICV ≥ 0.4 cc Gross Leak – Integrated Circuits MIL-STD-883 Method 1014 cond. C1 (fluorocarbon gross leak) 5 Torr vacuum for 30 minutes minimum followed by pressurization of the devices immersed in mineral oil and subsequent immersion in another mineral oil at Ta = 125°C – Discrete Devices MIL-STD-750 Method 1071 cond. C (fluorocarbon gross leak) 0.5 Torr vacuum for 1h, except for ICV ≥ 0.1 cc, followed by pressurization of the devices immersed in mineral oil at: 4.1 atm for 2h ICV ≤ 0.1 cc or 5.1 atm for 2h ICV ≥ 0.1 cc and subsequent immersion in mineral oil at Ta = 125°C

In-process control during assembly process (cont'd)

PROCESS STEPS	TESTS	DESCRIPTION
18 (cont.d)	LID TORQUE CONTROL	Ceramic packages only MIL-STD-883 Method 2024 (e.g. ≥ 60 Kg x cm for seal area values between 1.41 and 1.73 cm^2)
19	TRIM & FORM AND LEAD FINISH	– Trim & Form not for Metal Can packages – Dimensions, thickness and contamination control – Solderability control: Aging as per page 51 215 ± 5°C for 3 ± 0.5 sec. (SMD only) 235 ± 5°C for 2 ± 0.5 sec. 245 ± 5°C for 5 ± 0.5 sec.
20	INTERNAL WATER VAPOR CONTENT CONTROL	Dew Point method MIL-STD-883 Method 1018 procedure 3 5000 ppm max (dew point temperature less than - 15°C) Ceramic packages only
21	HIGH IMPACT SHOCK	Metal Can packages only (except TO3) 20000 g minimum; t = 25μ sec. minimum; Y1 axis only
22	FINAL BAKE	For SMD only (according to internal specifications)
23	RAW LINE INSPECTION	External Visual – Integrated Circuits MIL-STD-883 Method 2009; CECC 90000 – Discrete Devices MIL-STD-750 Method 2071; CECC 50000 Note: at this step some reliability tests (pressure pot, temperature cycling, life test etc.) are performed as a monitor, generally on a weekly basis, to have fast feedback on process behaviour (Real Time Control Tests)
25	GROUP A INSPECTION	See page 40
26	GROUPS B, C AND D TESTS	Performed on the product family representative types (by rotation); the results are extended to all the other devices of the same family according to the structure similarity concept
28	PACKING AND DOCUMENTATION INSPECTION	Inspection for: – right quantity – right type – right boxing – right labelling – right documentation – various

GROUP A INSPECTION - FINISHED PRODUCT ACCEPTANCE

ICs and Discrete devices

SUBGROUP	PARAMETERS	MINIMUM SAMPLE SIZE	ACCEPTANCE NUMBER
A1	Visual and mechanical inspection	315	0
A2+A3+A4	Cumulative electrical and inoperative mechanical failures	315	0

Notes
- This product acceptance is valid for standard production, for agreed customer programs other sampling plans can be applied
- Specified temperature ranges according to SGS-THOMSON databooks

PPM (RESULTS AND TARGETS)

As a consequence of its quality improvement programmes SGS-THOMSON has continually improved outgoing quality and is pursuing ambitious quality targets.

PPM values and targets for cumulative electrical failures* (inoperative mechanical included)

LPS	1988	1989	1990	1991
	20	20	15	10

* Values referred to the end of each year.

GROUPS B, C AND D TESTS

Integrated circuits - Groups B, C and D tests

Every week or every three months on raw line and/or finished products

SUBGROUP	TEST PROCEDURE	MIL-STD-883 METHOD	CECC 90000 METHOD	SGS-THOMSON TEST CONDITIONS	PACKAGE			MINIMUM SAMPLE SIZE	ACCEPTANCE NUMBER (C)	NOTES
					METAL	CERAMIC	PLASTIC			(1)
1	Physical dimension	2016	4.3	Data Sheet Drawing	x	x	x	2	0	
2	Resistance to solvents	2015	4 4	1 minute immersion in solvent solution followed by 10 strokes with a hard brush as per MIL-STD method (the procedure shall be repeated 3 times)	x	x	x	4	0	
3	Solderability	2003	4.6.10 Cond 1	215 ±5°C 3 ±0 5sec. 235 ±5°C 2 ±0.5sec 245 ±5°C 5 ±0 5sec	– x x	– x x	x x x	22	0	2
4	Operating Life Test or Intermittent Life Test (for Power devices) end point electrical parameters	1005 – 	4 8 – 	1000 h according to detail spec 5000 Cycles as per device spec.	x – x	x – x	x x x	45	0	3
5	Temperature cycling Constant acceleration Seal - fine - gross	1010 2001 1014	4.6 8 4 6 7 4 6 9	10 cycles Ta = -65°C to + 150°C 30000 g see page 38	x x x	x x x x	– – – x	22 –	0	 4
6	Pressure pot end point electrical parameters	–	–	Ta = 121°C, 2 atm, 240 h min as per device spec.	– –	– –	x x	22	0	
7	HAST (Highly Accelerated Stress Test) end point electrical parameters	–	4.6 3 Cond2	130°C/85%RH with bias t=150h according to detail specification as per device spec	– –	– –	x x	22	0	

Notes
1) Sample can be increased according to LTPD table, till c=2
2) Aging of 8h in steam vapor or 16h at 155°C Soldering temperature of 215°C for SMD only
3) Ta such to have $T_j = T_j$ max
4) 20000g for packages with cavity perimeter of 5cm or more and/or with a mass of 5 grams or more

Integrated circuits - Groups B, C and D tests

Every six months on raw line and/or finished products

SUBGROUP	TEST PROCEDURE	MIL-STD-883 METHOD	CECC 90000 METHOD	SGS-THOMSON TEST CONDITIONS	PACKAGE: METAL	PACKAGE: CERAMIC	PACKAGE: PLASTIC	MINIMUM SAMPLE SIZE	ACCEPTANCE NUMBER (C)	NOTES (1)
1	Lead integrity	2004	4 6 12 /1	Tensile test (as per CECC 90000)	x	–	–	22	0	
			4 6 12 /2	Lead Fatigue Cond. B2 - Wire leads, a force of 0.229 ±0.014 Kg for three 90° ± 5° arcs on each lead bending cycle 2 to 5 sec. For flat package and power dissipation packages the leads shall be bent 3 times simultaneously for at least 5 sec. permanent deformation during the 3rd cycle in opposite direction	x	x	x			2
				Solder pad adhesion Cond. D a force of 2.98 Kg min to each solder pad for 30 sec minimum	-	x	-			3
	Seal - fine - gross	1014	4 6 9	see page 38	x x	x x	- -			
2	Thermal shock	1011	4 6 8	Cond. B 15 shocks Ta = -55 to +125°C	x	x	-	22	0	
	Temperature cycling	1010	4 6 8	Cond. C, 100 cycles Ta = -65 to +150°C	x	x	x			4
	Moisture resistance	1004	4 6 3	Lead bend conditioning followed by 10 cycles of 24h Ta = 25°C to 65°C RH = 80% to 100% one 3rd cycle at Ta = -10°C	x	x	-			
	Seal - fine - gross	1014	4 6 9	see page 38	x x	x x	- -			
	Visual examination	1004 1010	–	without appraisal of marking	x	x	-			
	end point electrical parameters			as per device spec	x	x	x			
3	Mechanical shock	2002	4 6 4	Cond. B 1500g 0.5msec 5 blows in each of the 6 orientations not operating	x	x	–	22	0	
	Vibration, variable frequency	2007	4 6 5	Cond. A 20g 3 orientations f = 20 to 2000 cps four 4 minutes cycles 48 minutes total not operating	x	x	–			
	Constant accelerations	2001	4 6 7	Cond. E 30000 g Y1 orientation	x	x	–			5
	Seal - fine - gross	1014	4 6 9	see page 38	x x	x x	– –			
	Visual examination	1010 1011	–		x	x				
	end point electrical parameters			as per device spec	x	x	–			
4	Salt atmosphere	1009	4 6 14	Cond. A 10 to 50 gr of NaCl per m³ for 24 hr at Ta= 35°C min	x	x	x	22	0	
	Seal - fine - gross	1014	4 6 9	see page 38	x x	x x	– –			
	Visual examination	1009	4 6 14		x	x	x			
5	Humidity test	–	4 6 3 Cond 1	85°C/85% RH with biast = 100Vdc according to detail specification	–	–	x	45	0	
	end point electrical parameters			as per device spec	–	–	x			
6	Internal water-vapor content	1018	–	Dew point method procedure 3 (5000 ppm max)	x	x	–	3 5	0 1	6
7	Lid Torque	2024	–	see page 39	–	x	–	22	0	7

Notes
1) Sample can be increased according to LTPD table. till c=2
2) Not for SMD
3) Leadless chip carrier only
4) For plastic packages Ta= -65/-40°C according to device type
5) 20000g for packages with cavity perimeter of 5cm or more and/or with a mass of 5 grams or more
6) Test three devices If one fails test two additional devices with no failure
7) Applied only to packages which use glass-frit seal to lead the frame lead or package body (i.e. wherever frit seal establishes hermeticity or package integrity)

LPS - RESULTS SUMMARY

Test	Condition	Plastic				Ceramic				S.O. Package			
		1989		1990		1989		1990		1989		1990	
		SS	REJ	SS	REJ	SS	REJ	SS	REJ	SS	REJ	SS	REJ
HIGH TEMPERATURE BIAS	1000 hrs	1971	0	1809	0	620	0	675	0	738	0	756	0
	2000 hrs	540	0	513	0	135	0			198	0	216	0
TEMPERATURE HUMIDITY BIAS	1000 hrs	1951	0	1890	0	–	–	–	–	738	0	918	0
	2000 hrs	513	0	378	0					180	0	216	0
PRESSURE COOKER	168 hrs	2125	0	1830	0	–	–	–	–	795	0	810	0
	336 hrs	675	0	630	0					275	0	270	0
THERMAL SHOCKS	200 cyc	1425	0	1950	0	450	0	375	0	150	0	125	0
THERMAL CYCLES	200 cyc												
	1000 cyc	1070	0	1110	0	570	0	540	0	580	0	630	0
ENVIRONMENTAL SEQUENCE		–	–	–	–	1325	0	1275	0	–	–	–	–
MECHANICAL SEQUENCE		–	–	–	–	1325	0	1275	0	–	–	–	–
RESISTANCE TO SOLVENT		475	1	425	1	350	0	325	0	425	1	375	0
SOLDERABILITY		475	0	425	0	350	0	325	0	425	2	375	1
LEAD INTEGRITY		475	0	425	0	350	0	325	0				
HAST	96 hrs	175	0	225	0	–	–	–	–	100	0	125	0
	240 hrs	100	0	100	0					50	0	75	0

FAILURE RATE EVALUATION (AT 60% CONFIDENCE LEVEL)

Package	Device x Hours	Fail	Failure Rate FIT *	
			125°C	55°C
PLASTIC	3.78×10^6	0	242	0.5
CERAMIC	1.32×10^6	0	693	1.4
S.O. PACKAGE	1.49×10^6	0	613	1.3

* FIT = Failure in Time. Number of failures/10^9 Hours of operation (or 10^{-9}). The activation energy, from analysis, was chosen as 0.7 eV based on our tests results: the failure rate at lower operating temperature can be extrapolated from the Arrhenius plot.

The actual junction temperature should be used; it can be computed using the relationship

$$Tj = T_A + (P \times \theta_{JA})$$

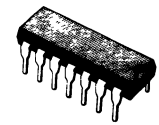
Where Tj = Junction temperature
T_A = Ambient temperature
θ_{JA} = Junction to ambient thermal resistance (typically 100°C/watt for a 16 pin DIP)
P = Power actual consumption

DATASHEETS

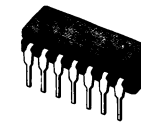
QUAD 2-INPUT NAND GATE

DESCRIPTION

The T74LS00 is a high speed QUAD 2-INPUT NAND GATE fabricated in LOW POWER SCHOTTKY technology.



B1
(Plastic Package)



D1
(Ceramic Package)

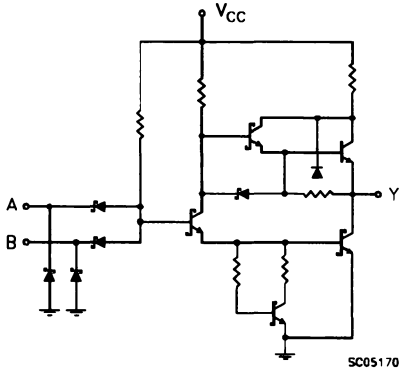
M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

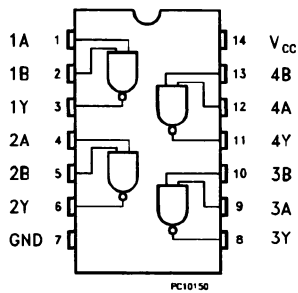
T74LS00 D1	T74LS00 C1
T74LS00 B1	T74LS00 M1

SCHEMATIC

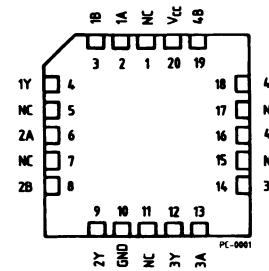


PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE

A	B	Y
L	X	H
X	L	H
H	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to + 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS00XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = -400 µA, V_{IN} = V_{IL}		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = 2.0 V	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CCH}	Supply Current HIGH		0.8	1.6	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CCL}	Supply Current LOW		2.4	4.4	V_{CC} = MAX, Inputs Open		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

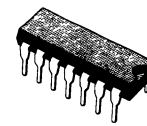
AC CHARACTERISTICS: $T_A = 25^oC$ (for AC test circuits and waveforms see databook introduction)

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		9	15	V_{CC} = 5.0 V	ns
t_{PHL}	Turn On Delay, Input to Output		10	15	C_L = 15 pF	ns

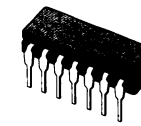
QUAD 2-INPUT NAND GATE

DESCRIPTION

The T74LS01 is a high speed QUAD 2-INPUT NAND GATE (with open collector output) fabricated in LOW POWER SCHOTTKY technology.



B1
(Plastic Package)



D1
(Ceramic Package)

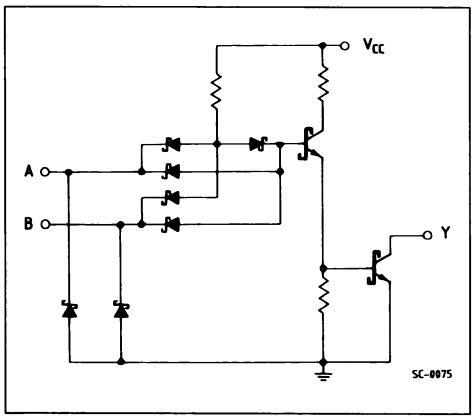
M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

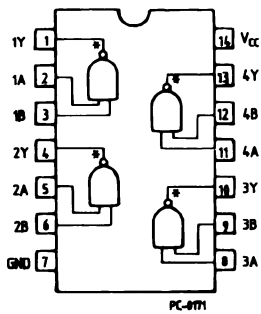
T74LS01 D1
T74LS01 B1
T74LS01 C1
T74LS01 M1

SCHEMATIC



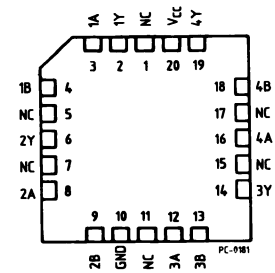
PIN CONNECTION (top view)

DUAL IN LINE



* With Open Collector Output

CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE

A	B	Y
L	X	H
X	L	H
H	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	0 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS01XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for all Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for all Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
I_{OH}	Output HIGH Current			100	V_{CC} = MIN, V_{OH} = 5.5 V		µA
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN	V
			0.35	0.5	I_{OL} = 8.0 mA	V_{IN} = V_{IH} or V_{IL} per Truth Table	V
I_{IH}	Input HIGH Current			20 0 1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			 1 6 4.4	V_{CC} = MAX,		 mA mA

Notes : 1 For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C

AC CHARACTERISTICS: $T_A = 25^oC$ (for AC test circuits and waveforms see databook introduction)

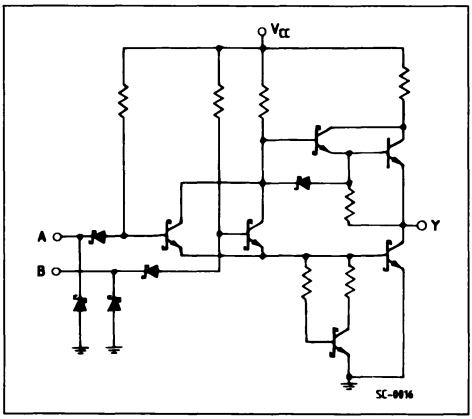
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		17	32	V_{CC} = 5.0 V C_L = 15 pF, R_L = 2.0 kΩ	ns
t_{PHL}	Turn On Delay, Input to Output		15	28		ns

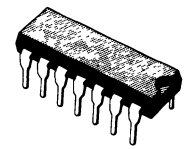
QUAD 2-INPUT NOR GATE

DESCRIPTION

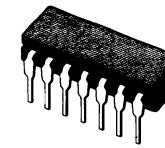
The T74LS02 is a high speed QUAD 2-INPUT NOR GATE fabricated in LOW POWER SCHOTTKY technology.

SCHEMATIC

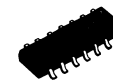




B1
(Plastic Package)



D1
(Ceramic Package)



M1
(Micro Package)

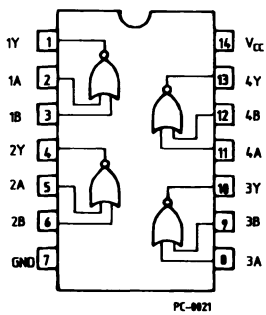
C1
(Plastic Chip Carrier)

ORDER CODES :

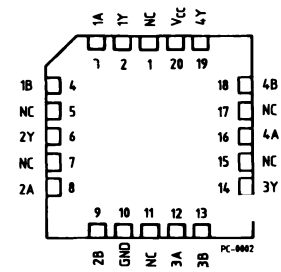
T74LS02 D1	T74LS02 C1
T74LS02 B1	T74LS02 M1

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE

A	B	Y
H	X	L
X	H	L
L	L	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0 5 to 7	V
V_I	Input Voltage, Applied to Input	– 0 5 to 15	V
V_O	Output Voltage, Applied to Output	– 0 5 to 5 5	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS02XX	4.75 V	5 0 V	5 25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)	Unit
		Min.	Typ. (*)	Max.		
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage	V
V_{IL}	Input LOW Voltage			0 8	Guaranteed Input LOW Voltage	V
V_{CD}	Input Clamp Diode Voltage		- 0 65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA	V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = -400 µA, V_{IN} = V_{IL}	V
V_{OL}	Output LOW Voltage		0 25	0 4	I_{OL} = 4 0 mA; V_{CC} = MIN, V_{IN} = 2.0 V	V
			0 35	0.5	I_{OL} = 8 0 mA; V_{CC} = MIN, V_{IN} = 2.0 V	V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7 0 V	µA mA
I_{IL}	Input LOW Current			- 0 4	V_{CC} = MAX, V_{IN} = 0.4 V	mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V	mA
I_{CCH}	Supply Current HIGH		1.6	3.2	V_{CC} = MAX, V_{IN} = 0 V	mA
I_{CCL}	Supply Current LOW		2.4	5 4	V_{CC} = MAX, Inputs Open	mA

Notes : 1 For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2 Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: $T_A = 25^{\circ}C$ (for AC test circuits and waveforms see databook introduction)

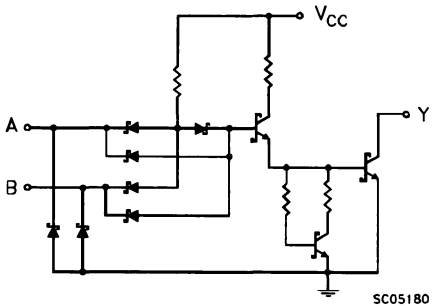
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		10	15	$V_{CC} = 5.0$ V $C_L = 15$ pF	ns
t_{PHL}	Turn On Delay, Input to Output		10	15		ns

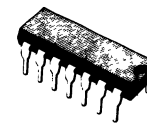
QUAD 2-INPUT NAND GATE

DESCRIPTION

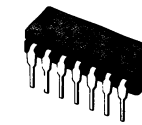
The T74LS03 is a high speed QUAD 2-INPUT NAND GATE fabricated in LOW POWER SCHOTTKY technology.

SCHEMATIC





B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

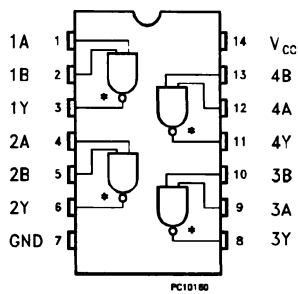
C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS03 D1	T74LS03 C1
T74LS03 B1	T74LS03 M1

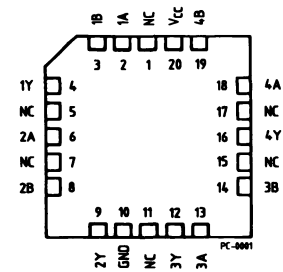
PIN CONNECTION (top view)

DUAL IN LINE



* Open Collector Outputs

CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE

A	B	Y
L	X	H
X	L	H
H	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to + 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS03XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
I_{OH}	Output HIGH Current			100	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IL}		µA
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN	V
			0.35	0.5	I_{OL} = 8.0 mA	V_{IN} = 2.0 V	V
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{CCH}	Supply Current HIGH			1.6	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CCL}	Supply Current LOW			4.4	V_{CC} = MAX, Inputs Open		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges
2. Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

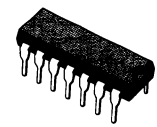
AC CHARACTERISTICS: $T_A = 25^oC$ (for AC test circuits and waveforms see databook introduction)

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		17	32	V_{CC} = 5.0 V	ns
t_{PHL}	Turn On Delay, Input to Output		15	28	C_L = 15 pF, R_L = 2.0 KΩ	ns

HEX INVERTER

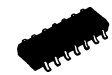
DESCRIPTION

The T74LS04 is a high speed HEX INVERTER fabricated in LOW POWER SCHOTTKY technology.



B1
(Plastic Package)

D1
(Ceramic Package)



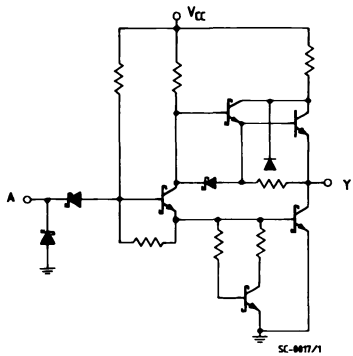
M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

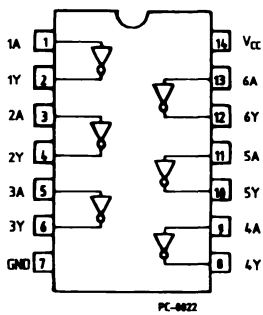
T74LS04 D1	T74LS04 C1
T74LS04 B1	T74LS04 M1

SCHEMATIC

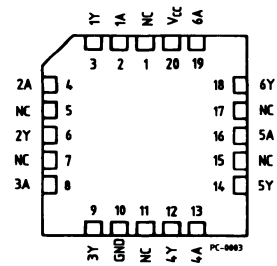


PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE

A	Y
L	H
H	L

L = LOW Voltage Level
H = HIGH Voltage Level

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage Applied to Input	– 0.5 to 15	V
V_O	Output Voltage Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS04XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)	Unit
		Min.	Typ. (*)	Max.		
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage	V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage	V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA	V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = -400 µA, V_{IN} = V_{IL}	V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = 2.0 V	V
			0.35	0.5	I_{OL} = 8.0 mA; V_{CC} = MIN, V_{IN} = 2.0 V	V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V	µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V	mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V	mA
I_{CCH}	Supply Current HIGH		1.2	2.4	V_{CC} = MAX, V_{IN} = 0 V	mA
I_{CCL}	Supply Current LOW		3.6	6.6	V_{CC} = MAX, Inputs Open	mA

Notes : 1 For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges
2 Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C

AC CHARACTERISTICS: $T_A = 25^\circ C$ (for AC test circuits and waveforms see databook introduction)

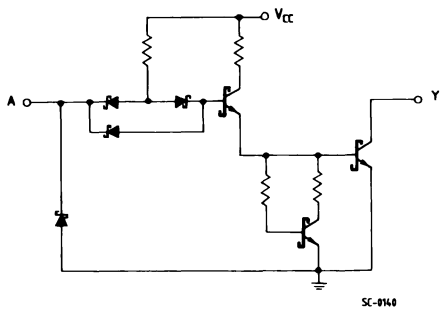
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		9	15	$V_{CC} = 5.0$ V $C_L = 15$ pF	ns
t_{PHL}	Turn On Delay, Input to Output		10	15		ns

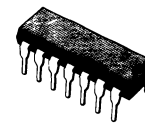
HEX INVERTER

DESCRIPTION

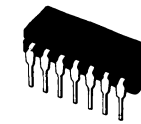
The T74LS05 is a high speed HEX INVERTER fabricated in LOW POWER SCHOTTKY technology.

SCHEMATIC





B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

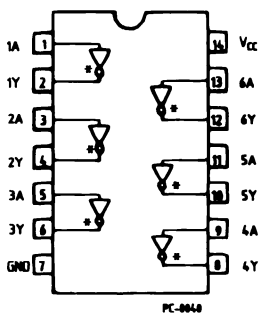
C1
(Plastic Chip Carrier)

ORDER CODES :

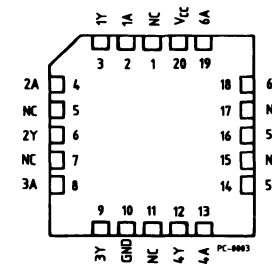
T74LS05 D1	T74LS05 C1
T74LS05 B1	T74LS05 M1

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE

A	Y
L	H
H	L

L = LOW Voltage Level
H = HIGH Voltage Level

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 5.5	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS05XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
I_{OH}	Output HIGH Current			100	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IL}		µA
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = 2.0 V	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0 4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{CCH}	Supply Current HIGH			2.4	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CCL}	Supply Current LOW			6.6	V_{CC} = MAX, Inputs Open		mA

Notes : 1 For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C

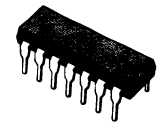
AC CHARACTERISTICS: $T_A = 25^oC$ (for AC test circuits and waveforms see databook introduction)

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		17	32	V_{CC} = 5.0 V C_L = 15 pF, R_L = 2.0 kΩ	ns
t_{PHL}	Turn On Delay, Input to Output		15	28		ns

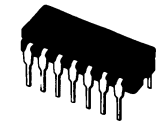
QUAD 2-INPUT AND GATE

DESCRIPTION

The T74LS08 is a high speed QUAD 2-INPUT AND GATE fabricated in LOW POWER SCHOTTKY technology.



B1
(Plastic Package)



D1
(Ceramic Package)

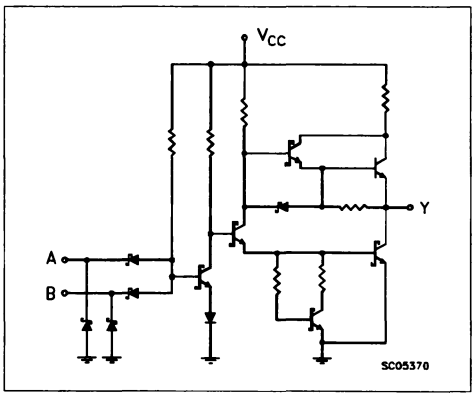
M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

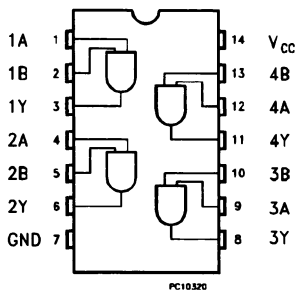
T74LS08 D1	T74LS08 C1
T74LS08 B1	T74LS08 M1

SCHEMATIC



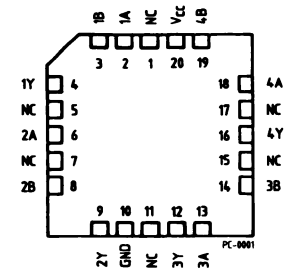
PIN CONNECTION (top view)

DUAL IN LINE



* Open Collector Outputs

CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE

A	B	Y
L	X	L
X	L	L
H	H	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to + 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS08XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3 4		V_{CC} = MIN, I_{OH} = -400 µA, V_{IN} = V_{IH}		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN	V
			0.35	0.5	I_{OL} = 8.0 mA	V_{IN} = V_{IL}	V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.36	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CCH}	Supply Current HIGH		2.4	4.8	V_{CC} = MAX, Inputs Open		mA
I_{CCL}	Supply Current LOW		4.4	8.8	V_{CC} = MAX, V_{IN} = 0 V		mA

Notes : 1 For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges
2 Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C.

AC CHARACTERISTICS: $T_A = 25^oC$ (for AC test circuits and waveforms see databook introduction)

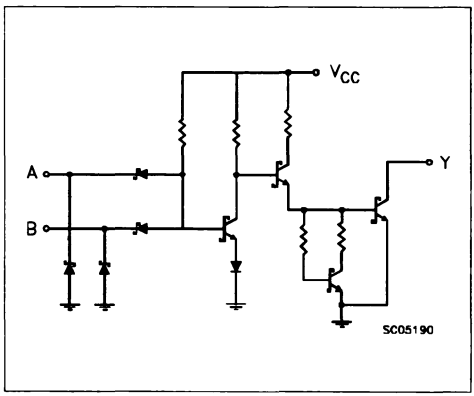
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		9	15	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PHL}	Turn On Delay, Input to Output		10	15		ns

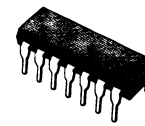
QUAD 2-INPUT AND GATE

DESCRIPTION

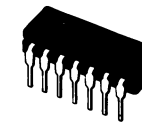
The T74LS09 is a high speed QUAD 2-INPUT AND GATE (WITH OPEN COLLECTOR OUTPUT) fabricated in LOW POWER SCHOTTKY technology.

SCHEMATIC





B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

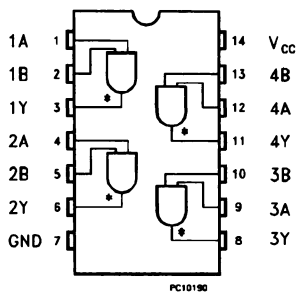
C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS09 D1	T74LS09 C1
T74LS09 B1	T74LS09 M1

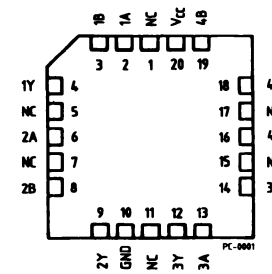
PIN CONNECTION (top view)

DUAL IN LINE



* Open Collector Outputs

CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE

A	B	Y
L	X	L
X	L	L
H	H	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	− 0.5 to + 7	V
V_I	Input Voltage, Applied to Input	− 0.5 to 15	V
V_O	Output Voltage, Applied to Output	− 0.5 to 10	V
I_I	Input Current, Into Inputs	− 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS09XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
I_{OH}	Output HIGH Current			100	V_{CC} = MIN, V_{OH} = - 5.5 V, V_{IN} = V_{IH}		µA
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN	V
			0.35	0.5	I_{OL} = 8.0 mA	V_{IN} = V_{IL}	V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0 4 V		mA
I_{CCH}	Supply Current HIGH		2.4	4.8	V_{CC} = MAX, Inputs Open		mA
I_{CCL}	Supply Current LOW		4.4	8.8	V_{CC} = MAX, V_{IN} = 0 V		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C

AC CHARACTERISTICS: $T_A = 25^oC$ (for AC test circuits and waveforms see databook introduction)

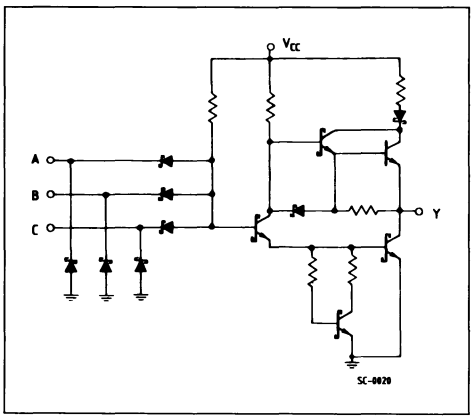
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		20	35	V_{CC} = 5.0 V	ns
t_{PHL}	Turn On Delay, Input to Output		17	35	C_L = 15 pF, R_L = 2.0 KΩ	ns

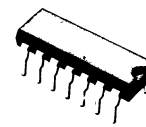
TRIPLE 3-INPUT NAND GATE

DESCRIPTION

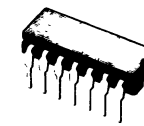
The T74LS10 is a high speed TRIPLE 3-INPUT NAND GATE fabricated in LOW POWER SCHOTTKY technology.

SCHEMATIC DIAGRAM





B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

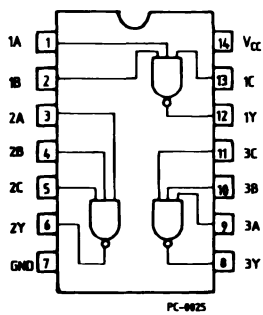
C1
(Plastic Chip Carrier)

ORDER CODES :

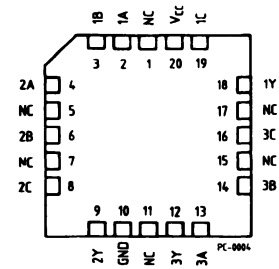
T74LS10 D1	T74LS10 C1
T74LS10 B1	T74LS10 M1

PIN CONNECTION (top view)

DUAL IN LINE

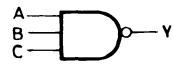


CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE



A	B	C	Y
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 5.5	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS10XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)	Unit
		Min.	Typ. (*)	Max.		
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage	V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage	V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA	V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = -400 µA, V_{IN} = V_{IL}	V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = 2 0 V	V
			0.35	0.5	I_{OL} = 8.0 mA; V_{CC} = MIN, V_{IN} = 2 0 V	V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V	µA mA
I_{IL}	Input LOW Current			- 0.36	V_{CC} = MAX, V_{IN} = 0.4 V	mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V	mA
I_{CCH}	Supply Current HIGH		0.6	1.2	V_{CC} = MAX, V_{IN} = 0 V	mA
I_{CCL}	Supply Current LOW		1.8	3.3	V_{CC} = MAX, Inputs Open	mA

Notes : 1 For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges
2. Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C

AC CHARACTERISTICS: $T_A = 25^oC$ (for AC test circuits and waveforms see databook introduction)

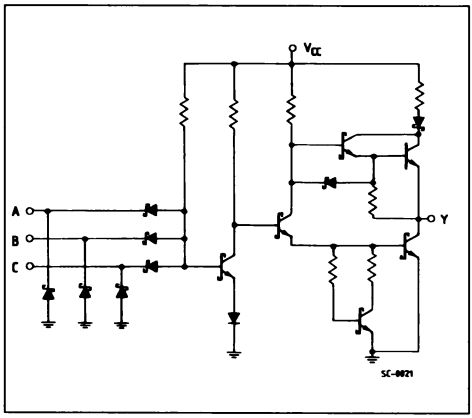
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		9	15	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PHL}	Turn On Delay, Input to Output		10	15		ns

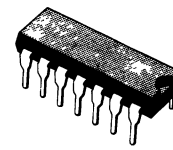
TRIPLE 3-INPUT AND GATE

DESCRIPTION

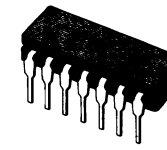
The T74LS11 is a high speed TRIPLE 3-INPUT AND GATE fabricated in LOW POWER SCHOTTKY technology.

SCHEMATIC

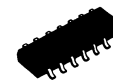




B1
(Plastic Package)



D1
(Ceramic Package)



M1
(Micro Package)

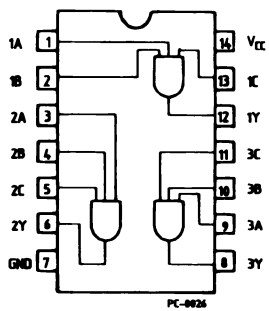
C1
(Plastic Chip Carrier)

ORDER CODES :

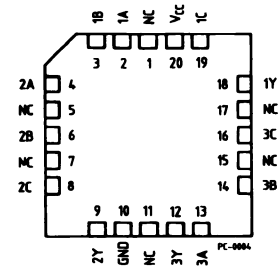
T74LS11 D1	T74LS11 C1
T74LS11 B1	T74LS11 M1

PIN CONNECTION (top view)

DUAL IN LINE

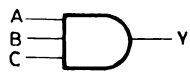


CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE



A	B	C	Y
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0 5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS11XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage			0 8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = -400 µA, V_{IN} = V_{IH}		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN	V
			0.35	0.5	I_{OL} = 8.0 mA	V_{IN} = V_{IL}	V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CCH}	Supply Current HIGH		1.8	3 6	V_{CC} = MAX, Inputs Open		mA
I_{CCL}	Supply Current LOW		3.3	6.6	V_{CC} = MAX, V_{IN} = 0 V		mA

Notes : 1 For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges
2 Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C

AC CHARACTERISTICS: $T_A = 25^oC$ (for AC test circuits and waveforms see databook introduction)

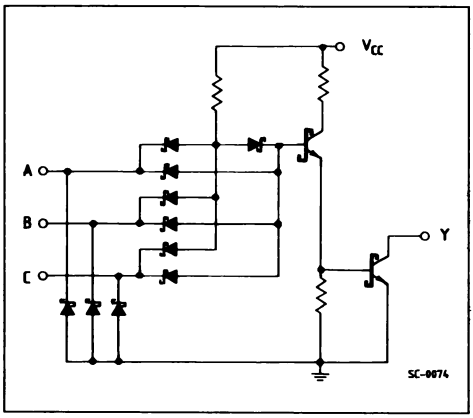
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		8	15	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PHL}	Turn On Delay, Input to Output		10	20		ns

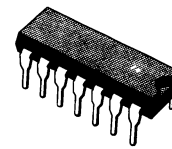
TRIPLE 3-INPUT NAND GATE

DESCRIPTION

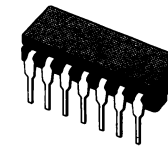
The T74LS12 is a high speed TRIPLE 3-INPUT NAND GATE (with open collector output) fabricated in LOW POWER SCHOTTKY technology.

SCHEMATIC





B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

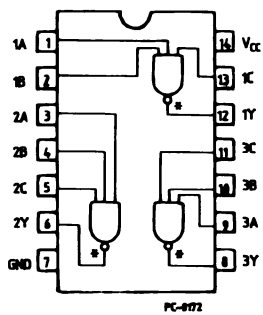
C1
(Plastic Chip Carrier)

ORDER CODES :

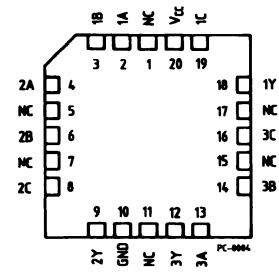
T74LS12 D1	T74LS12 C1
T74LS12 B1	T74LS12 M1

PIN CONNECTION (top view)

DUAL IN LINE



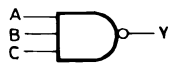
CHIP CARRIER



* With Open Collector Output

NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE



A	B	C	Y
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	0 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS12XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
I_{OH}	Output HIGH Current			100	V_{CC} = MIN, V_{OH} = 5.5 V		µA
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN	V
			0.35	0.5	I_{OL} = 8.0 mA	V_{IN} = V_{IH} or V_{IL} per Truth Table	V
I_{IH}	Input HIGH Current			20	V_{CC} = MAX, V_{IN} = 2.7 V		µA
				0.1	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{CC}	Power Supply Current				V_{CC} = MAX		
	Total, Output HIGH			1.4			mA
	Total, Output LOW			3.3			mA

Notes : 1 For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C

AC CHARACTERISTICS: $T_A = 25^oC$ (for AC test circuits and waveforms see databook introduction)

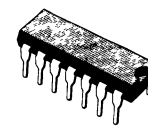
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		17	32	V_{CC} = 5.0 V C_L = 15 pF, R_L = 2.0 KΩ	ns
t_{PHL}	Turn On Delay, Input to Output		15	28		ns

DUAL 4-INPUT SCHMITT TRIGGER

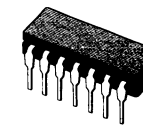
DESCRIPTION

The T74LS13 contains two-4 Input NAND Gates that accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have a greater noise margin than conventional NAND gates.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter that drives a TTL totem-pole output. The Schmitt trigger uses positive feedbak to effectively speed-up slow input transitions and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

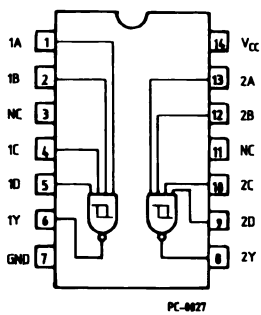
C1
(Plastic Chip Carrier)

ORDER CODES :

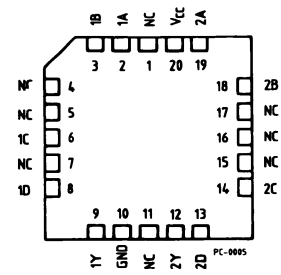
T74LS13 D1	T74LS13 C1
T74LS13 B1	T74LS13 M1

PIN CONNECTION (top view)

DUAL IN LINE

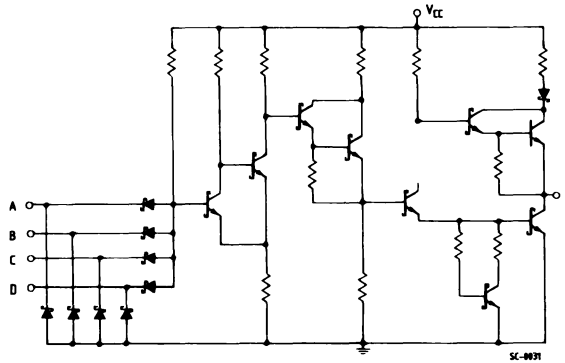


CHIP CARRIER

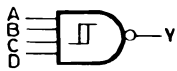


NC = No Internal Connection

SCHEMATIC



LOGIC DIAGRAM AND TRUTH TABLE



A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.6 to 5.5	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS13XX	4.75 V	5 0 V	5.25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)	Unit
		Min.	Typ. (*)	Max.		
V_{T+}	Positive-going Threshold Voltage	1.5	1.8	2.0	V_{CC} = 5.0 V	V
V_{T-}	Negative-going Threshold Voltage	0.6	0.95	1.1	V_{CC} = 5.0 V	V
$V_{T+} - V_{T-}$	Hysteresis	0.4	0.8		V_{CC} = 5.0 V	V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA	V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = 0.5 V	V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = 1.9 V	V
			0.35	0.5	I_{OL} = 8.0 mA; V_{CC} = MIN, V_{IN} = 1.9 V	V
I_{T+}	Input Current at Positive-going Threshold		- 0.14		V_{CC} = 5.0 V, V_{IN} = V_{T+}	mA
I_{T-}	Input Current at Negative-going Threshold		- 0.18		V_{CC} = 5.0 V, V_{IN} = V_{T-}	mA
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V	µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V	mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V	mA
I_{CCH}	Supply Current HIGH		3	6	V_{CC} = MAX, V_{IN} = 0 V	mA
I_{CCL}	Supply Current LOW		4	7	V_{CC} = MAX, V_{IN} = 4.5 V	mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		15	22	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PHL}	Turn On Delay, Input to Output		18	27		ns

Figure 1 : V_{IN} Versus V_{OUT} Transfer Function.

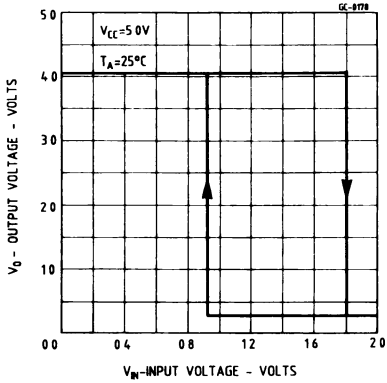


Figure 2 : Threshold Voltage and Hysteresis Versus Power Supply Voltage.

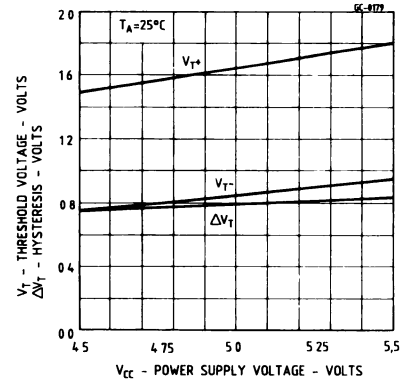


Figure 3 : Threshold Voltage and Hysteresis Versus Temperature.

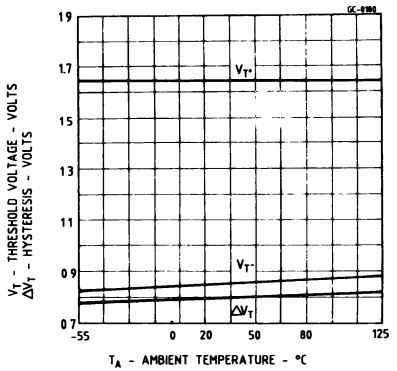
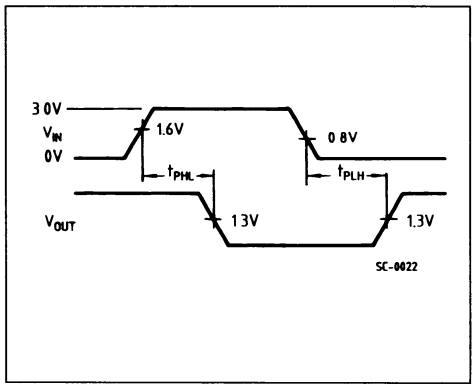


Figure 4.



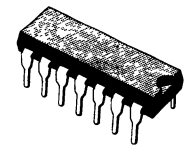
T74LS14

HEX SCHMITT TRIGGER INVERTER

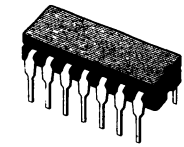
DESCRIPTION

The T74LS14 contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater a noise margin than conventional inverters.

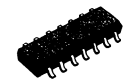
Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter that drives a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going tran-sitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.



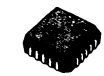
B1
(Plastic Package)



D1
(Ceramic Package)



M1
(Micro Package)



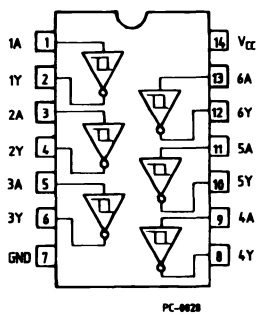
C1
(Plastic Chip Carrier)

ORDER CODES :

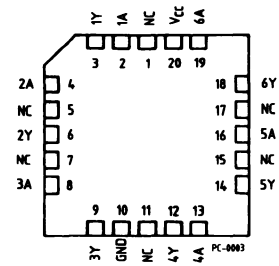
T74LS14 D1	T74LS14 C1
T74LS14 B1	T74LS14 M1

PIN CONNECTION (top view)

DUAL IN LINE

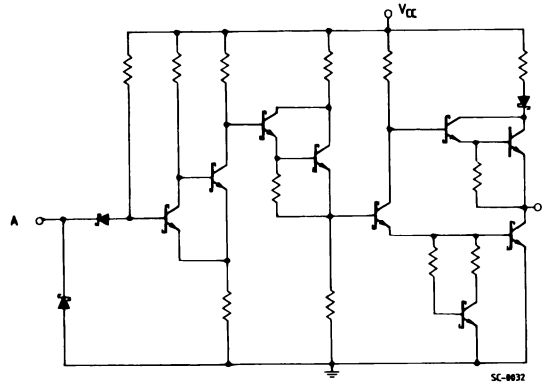


CHIP CARRIER

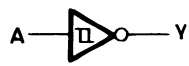


NC = No Internal Connection

SCHEMATIC DIAGRAM



LOGIC DIAGRAM AND TRUTH TABLE



A	Y
L	H
H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS14XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{T+}	Positive-going Threshold Voltage	1.4	1.6	1.9	V_{CC} = 5.0 V		V
V_{T-}	Negative-going Threshold Voltage	0.5	0.8	1.0	V_{CC} = 5.0 V		V
$V_{T+} - V_{T-}$	Hysteresis	0.4	0 8		V_{CC} = 5 0 V		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = 0.5 V		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = 1.9 V	V
			0.35	0.5	I_{OL} = 8 0 mA		V
I_{T+}	Input Current at Positive-going Threshold		- 0.14		V_{CC} = 5.0 V, V_{IN} = V_{T+}		mA
I_{T-}	Input Current at Negative-going Threshold		- 0.18		V_{CC} = 5.0 V, V_{IN} = V_{T-}		mA
I_{IH}	Input HIGH Current		1.0	20 0 1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7 0 V		µA mA
I_{IL}	Input LOW Current			- 0 4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CCH}	Supply Current HIGH		8 6	16	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CCL}	Supply Current LOW		12	21	V_{CC} = MAX, V_{IN} = 4.5 V		mA

Notes : 1 For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		15	22	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PHL}	Turn On Delay, Input to Output		15	22		ns

Figure 1 : V_{IN} Versus V_{OUT} Transfer Function.

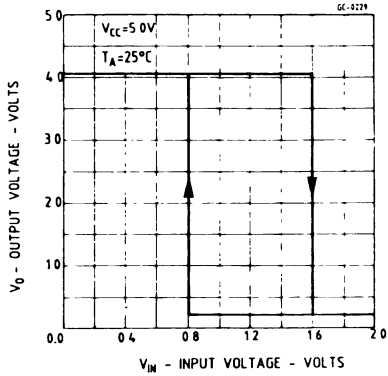


Figure 2: Threshold Voltage and Hysteresis Versus Power Supply Voltage.

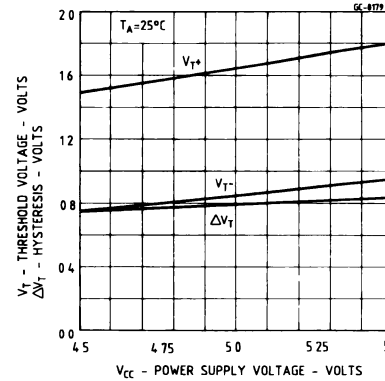


Figure 3 : Threshold Voltage and Hysteresis Versus Temperature.

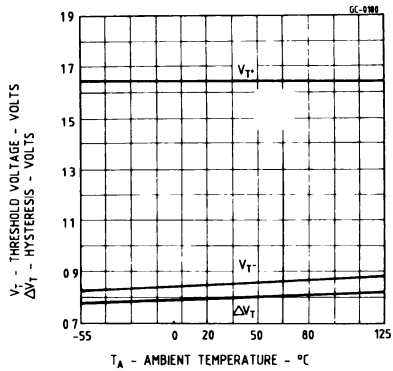
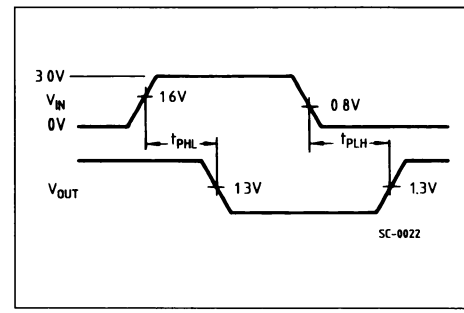


Figure 4.

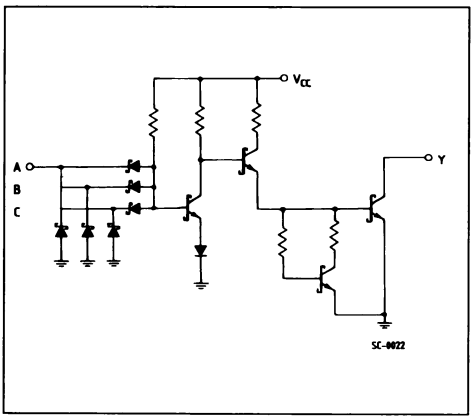


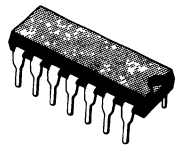
TRIPLE 3-INPUT AND GATE

DESCRIPTION

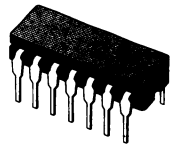
The T74LS15 is a high speed TRIPLE 3-INPUT AND GATE (with open collector output) fabricated in LOW POWER SCHOTTKY technology.

SCHEMATIC

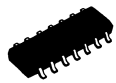




B1
(Plastic Package)



D1
(Ceramic Package)



M1
(Micro Package)

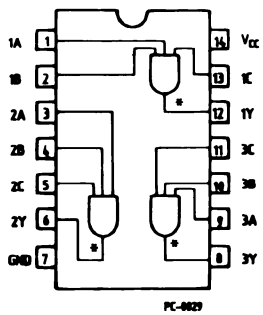
C1
(Plastic Chip Carrier)

ORDER CODES :

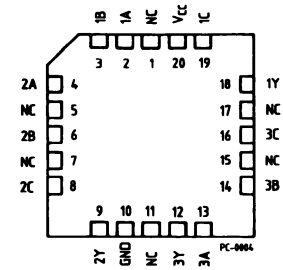
T74LS15 D1	T74LS15 C1
T74LS15 B1	T74LS15 M1

PIN CONNECTION (top view)

DUAL IN LINE



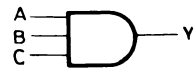
CHIP CARRIER



* Open Collector Outputs

NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE



A	B	C	Y
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS15XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
I_{OH}	Output HIGH Current			100	V_{CC} = MIN, V_{OH} = 5.5 V V_{IN} = V_{IH}		µA
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN	V
			0.35	0.5	I_{OL} = 8.0 mA	V_{IN} = V_{IL}	V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{CCH}	Supply Current HIGH		1.8	3.6	V_{CC} = MAX, Inputs Open		mA
I_{CCL}	Supply Current LOW		3.3	6.6	V_{CC} = MAX, V_{IN} = 0 V		mA

Notes : 1 For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C.

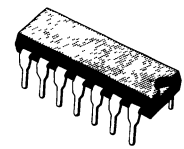
AC CHARACTERISTICS: $T_A = 25^oC$ (for AC test circuits and waveforms see databook introduction)

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		20	35	V_{CC} = 5.0 V C_L = 15 pF, R_L = 2.0 KΩ	ns
t_{PHL}	Turn On Delay, Input to Output		17	35		ns

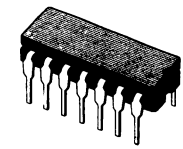
DUAL 4-INPUT NAND GATE

DESCRIPTION

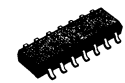
The T74LS20 is a high speed DUAL 4-INPUT NAND GATE fabricated in LOW POWER SCHOTTKY technology.



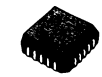
B1
(Plastic Package)



D1
(Ceramic Package)



M1
(Micro Package)

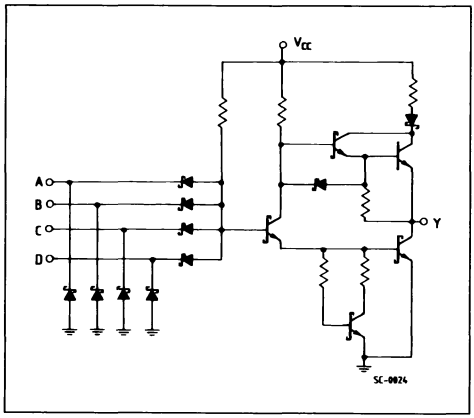


C1
(Plastic Chip Carrier)

ORDER CODES :

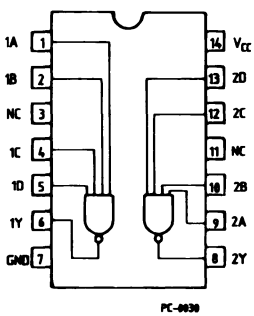
T74LS20 D1	T74LS20 C1
T74LS20 B1	T74LS20 M1

SCHEMATIC

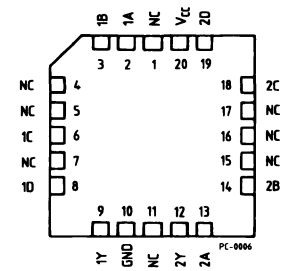


PIN CONNECTION (top view)

DUAL IN LINE

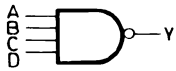


CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE



A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 5.5	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS20XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)	Unit
		Min.	Typ. (*)	Max.		
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage	V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage	V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1 5	V_{CC} = MIN, I_{IN} = -18 mA	V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IL}	V
V_{OL}	Output LOW Voltage		0 25	0.4	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = 2.0 V	V
			0.35	0.5	I_{OL} = 8.0 mA; V_{CC} = MIN, V_{IN} = 2.0 V	V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V	µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V	mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V	mA
I_{CCH}	Supply Current HIGH		0.4	0.8	V_{CC} = MAX, V_{IN} = 0 V	mA
I_{CCL}	Supply Current LOW		1.2	2.2	V_{CC} = MAX, Inputs Open	mA

Notes : 1 For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2 Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: $T_A = 25^oC$ (for AC test circuits and waveforms see databook introduction)

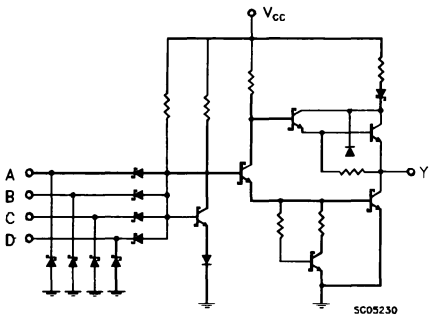
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		9	15	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PHL}	Turn On Delay, Input to Output		10	15		ns

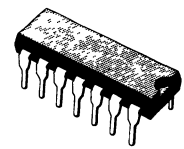
DUAL 4-INPUT AND GATE

DESCRIPTION

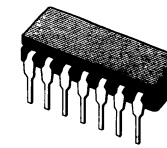
The T74LS21 is a high speed DUAL 4-INPUT AND GATE fabricated in LOW POWER SCHOTTKY technology.

SCHEMATIC

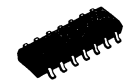




B1
(Plastic Package)



D1
(Ceramic Package)



M1
(Micro Package)

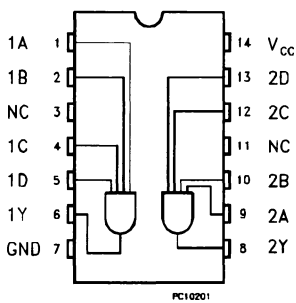
C1
(Plastic CHip Carrier)

ORDER CODES :

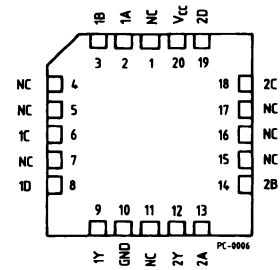
T74LS21 D1	T74LS21 C1
T74LS21 B1	T74LS21 M1

PIN CONNECTION (top view)

DUAL IN LINE

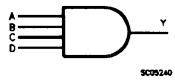


CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE



A	B	C	D	Y
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	- 0.5 to 7	V
V_I	Input Volatge, Applied to Input	- 0.5 to 15	V
V_O	Output Voltage, Applied to Output	- 0.5 to 5.5	V
I_I	Input Current, Into Inputs	- 30 to 5	mA
I_O	Output Current, Into Outputs	60	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS21XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH}		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN	V
			0.35	0.5	I_{OL} = 8.0 mA	V_{IN} = V_{IL}	V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CCH}	Supply Current HIGH		1.2	2.4	V_{CC} = MAX, Inputs Open		mA
I_{CCL}	Supply Current LOW		2.2	4.4	V_{CC} = MAX, V_{IN} = 0 V		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2 Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: $T_A = 25^oC$ (for AC test circuits and waveforms see databook introduction)

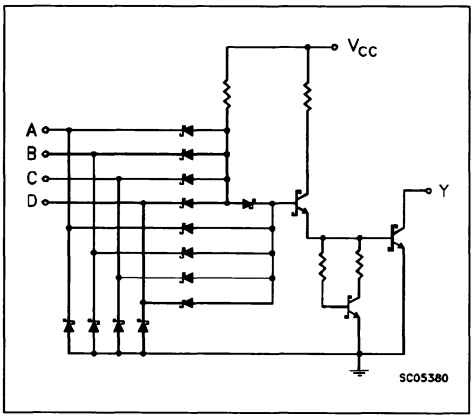
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		8	15	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PHL}	Turn On Delay, Input to Output		10	20		ns

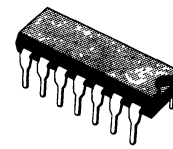
DUAL 4-INPUT NAND GATE

DESCRIPTION

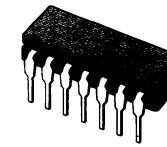
The T74LS22 is a high speed DUAL 4-INPUT NAND GATE fabricated in LOW POWER SCHOTTKY technology.

SCHEMATIC

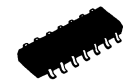




B1
(Plastic Package)



D1
(Ceramic Package)



M1
(Micro Package)

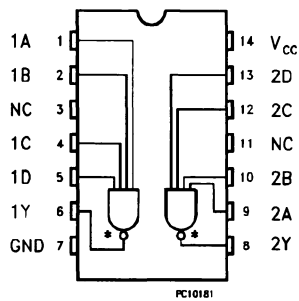
C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS22 D1	T74LS22 C1
T74LS22 B1	T74LS22 M1

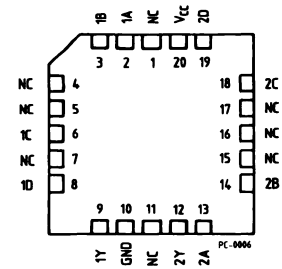
PIN CONNECTION (top view)

DUAL IN LINE



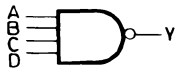
* Open Collector Outputs

CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE



A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 5.5	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS22XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
I_{OH}	Output HIGH Current			100	V_{CC} = MIN, V_{OH} = 5.5 V V_{IN} = V_{IL}		µA
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = 2.0 V	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{CCH}	Supply Current HIGH		0.4	0.8	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CCL}	Supply Current LOW		1.2	2.2	V_{CC} = MAX, Inputs Open		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: $T_A = 25^oC$ (for AC test circuits and waveforms see databook introduction)

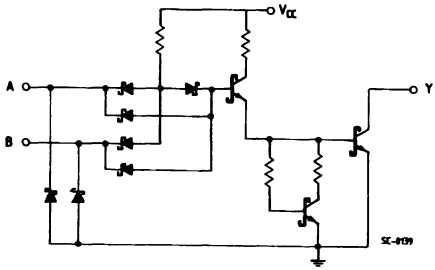
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		17	32	V_{CC} = 5.0 V C_L = 15 pF, R_L = 2.0 KΩ	ns
t_{PHL}	Turn On Delay, Input to Output		15	28		ns

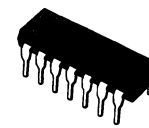
QUAD 2-INPUT NAND BUFFER

DESCRIPTION

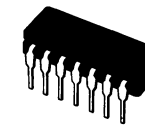
The T74LS26 is a high speed QUAD 2-INPUT NAND BUFFER (with open collector output) fabricated in LOW POWER SCHOTTKY technology.

SCHEMATIC





B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

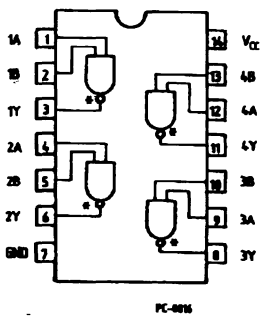
C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS26 D1	T74LS26 C1
T74LS26 B1	T74LS26 M1

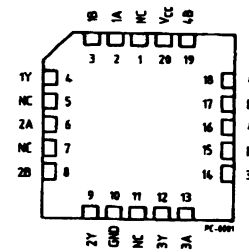
PIN CONNECTION (top view)

DUAL IN LINE



* Open Collector Outputs

CHIP CARRIER



NC = No Internal Connection

SCHEMATIC DIAGRAM

A	B	Y
L	X	H
X	L	H
H	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 15	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	60	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS26XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Input		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Input		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
I_{OH}	Output HIGH Current			1000 50	V_{CC} = MIN, V_{OH} = 15 V V_{CC} = MIN, V_{OH} = 12 V		µA
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = 2.0 V	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current		0.1	2.0 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{CCH}	Supply Current HIGH		0.8	1.6	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CCL}	Supply Current LOW		2.4	4.4	V_{CC} = MAX, Input Open		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

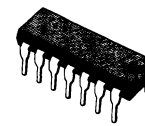
AC CHARACTERISTICS: $T_A = 25^oC$ (for AC test circuits and waveforms see databook introduction)

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		17	32	VCC = 5.0 V C_L = 15 pF, R_L = 2.0 kΩ	ns
t_{PHL}	Turn On Delay, Input to Output		15	28		ns

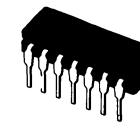
TRIPLE 3-INPUT NOR GATE

DESCRIPTION

The T74LS27 is a high speed TRIPLE 3-INPUT NOR GATE fabricated in LOW POWER SCHOTTKY technology.



B1
(Plastic Package)



D1
(Ceramic Package)

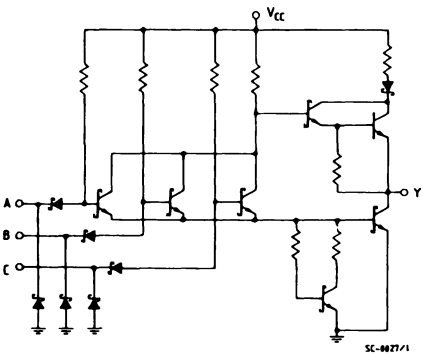
M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

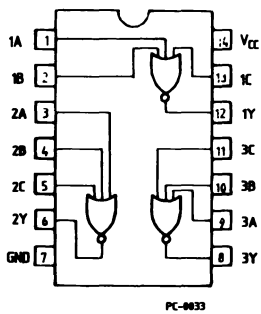
T74LS27 D1	T74LS27 C1
T74LS27 B1	T74LS27 M1

SCHEMATIC

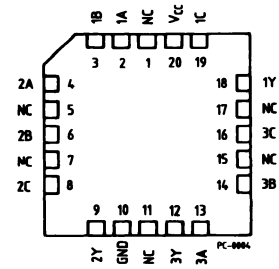


PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE

A	B	C	Y
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	60	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS27X	4.75 V	5 0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IL}		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN	V
			0.35	0.5	I_{OL} = 8.0 mA	V_{IN} = 2.0 V	V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CCH}	Supply Current HIGH		2.0	4.0	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CCL}	Supply Current LOW		3.4	6.8	V_{CC} = MAX, Inputs Open		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C.

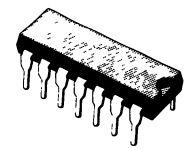
AC CHARACTERISTICS: $T_A = 25^oC$ (for AC test circuits and waveforms see databook introduction)

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		10	15	V_{CC} = 5.0 V C_L = 15 pF,	ns
t_{PHL}	Turn On Delay, Input to Output		10	15		ns

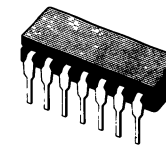
QUAD 2-INPUT NOR BUFFER

DESCRIPTION

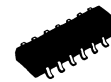
The T74LS28 is a high speed QUAD 2-INPUT NOR BUFFER fabricated in LOW POWER SCHOTTKY technology.



B1
(Plastic Package)



D1
(Ceramic Package)



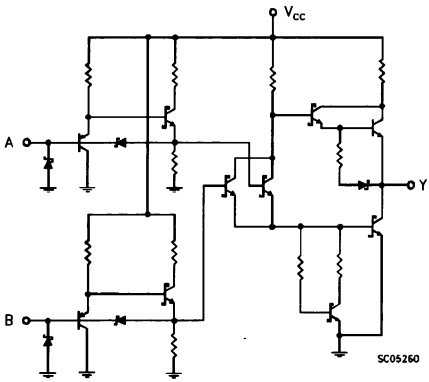
M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

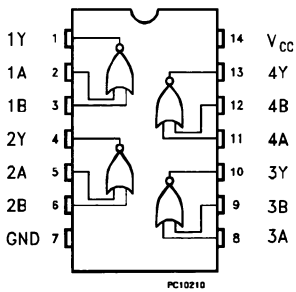
T74LS28 D1	T74LS28 C1
T74LS28 B1	T74LS28 M1

SCHEMATIC

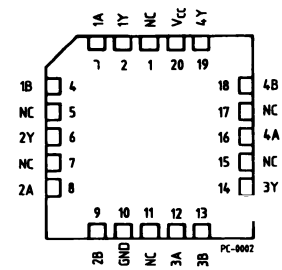


PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE

A	B	Y
H	X	L
X	H	L
L	L	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_o	Ouptut Voltage, Applied to Output	– 0.5 to 5.5	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_o	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS28XX	4.75 V	5 0 V	5.25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)	Unit
		Min.	Typ. (*)	Max.		
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage	V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage	V
V_{CD}	Input Clamp Diode Voltage		- 0.85	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA	V
V_{OH}	Output HIGH Voltage	2.7			V_{CC} = MIN, I_{OH} = - 1.2 mA, V_{IN} = V_{IL}	V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 12 mA; V_{CC} = MIN, V_{IN} = V_{IH}	V
			0.35	0 5	I_{OL} = 24 mA; V_{CC} = MIN, V_{IN} = V_{IH}	V
I_{IH}	Input HIGH Current		1.0	20	V_{CC} = MAX, V_{IN} = 2.7 V	µA
			1.0	100	V_{CC} = MAX, V_{IN} = 7 0 V	µA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V	mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V	mA
I_{CCH}	Supply Current HIGH		2.1	3.6	V_{CC} = MAX	mA
I_{CCL}	Supply Current LOW		11	13.8	V_{CC} = MAX	mA

Notes : 1 For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges
2 Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C

AC CHARACTERISTICS: $T_A = 25^oC$ (for AC test circuits and waveforms see databook introduction)

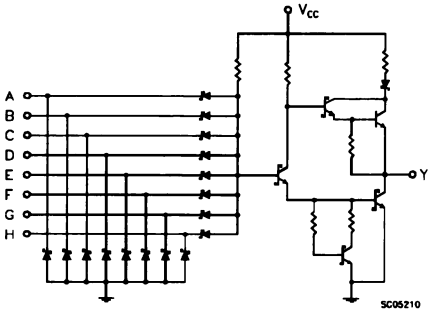
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		12	24	V_{CC} = 5.0 V C_L = 45 pF, R_L = 667 Ω	ns
t_{PHL}	Turn On Delay, Input to Output		12	24		ns

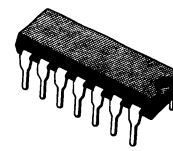
8-INPUT NAND GATE

DESCRIPTION

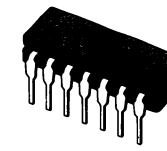
The T74LS30 is a high speed 8-INPUT NAND GATE fabricated in LOW POWER SCHOTTKY technology.

SCHEMATIC

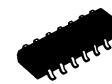




B1
(Plastic Package)



D1
(Ceramic Package)



M1
(Micro Package)

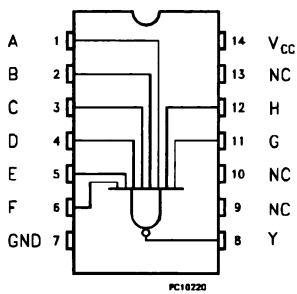
C1
(Plastic Chip Carrier)

ORDER CODES :

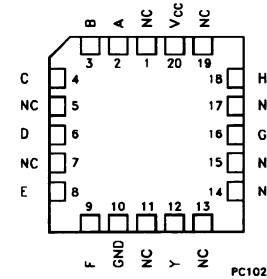
T74LS30 D1	T74LS30 C1
T74LS30 B1	T74LS30 M1

PIN CONNECTION (top view)

DUAL IN LINE

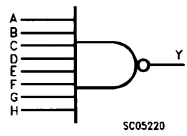


CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE



A	B	C	D	E	F	G	H	Y
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	- 0.5 to 7	V
V_I	Input Volatge, Applied to Input	- 0.5 to 15	V
V_O	Output Voltage, Applied to Output	- 0.5 to 5.5	V
I_I	Input Current, Into Inputs	- 30 to 5	mA
I_O	Output Current, Into Outputs	60	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS30XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IL}		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = 2.0 V	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CCH}	Supply Current HIGH		0.35	0.5	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CCL}	Supply Current LOW		0.6	1.1	V_{CC} = MAX, Inputs Open		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C

AC CHARACTERISTICS: T_A = 25°C (for AC test circuits and waveforms see databook introduction)

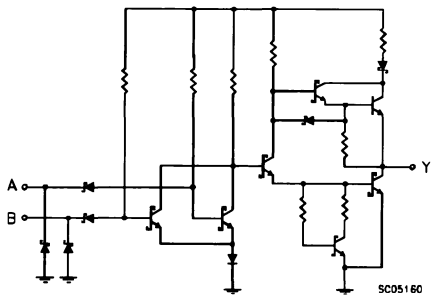
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		8	15	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PHL}	Turn On Delay, Input to Output		13	20		ns

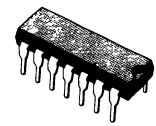
QUAD 2-INPUT OR GATE

DESCRIPTION

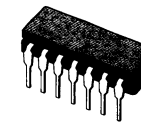
The T74LS32 is a high speed QUAD 2-INPUT OR GATE fabricated in LOW POWER SCHOTTKY technology.

SCHEMATIC





B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

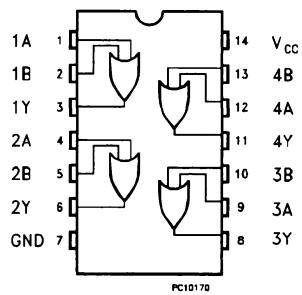
C1
(Plastic Chip Carrier)

ORDER CODES :

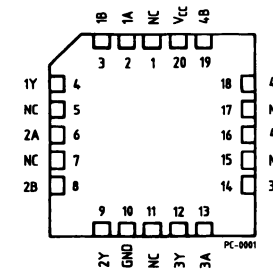
T74LS32 D1	T74LS32 C1
T74LS32 B1	T74LS32 M1

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE

A	B	Y
L	L	L
X	H	H
H	X	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to + 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS32XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = -400 µA, V_{IN} = V_{IL}		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IL}	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CCH}	Supply Current HIGH		3.1	6.2	V_{CC} = MAX, Inputs Open		mA
I_{CCL}	Supply Current LOW		4.9	9.8	V_{CC} = MAX, V_{IN} = 0 V		mA

Notes : 1 For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2 Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C

AC CHARACTERISTICS: $T_A = 25^oC$ (for AC test circuits and waveforms see databook introduction)

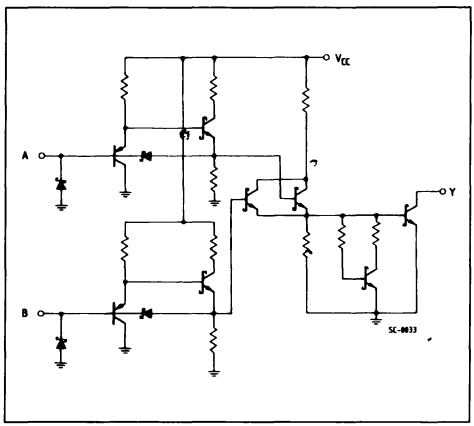
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		14	22	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PHL}	Turn On Delay, Input to Output		14	22		ns

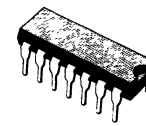
QUAD 2-INPUT NOR BUFFER

DESCRIPTION

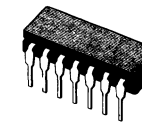
The T74LS33 is a high speed QUAD 2-INPUT NOR BUFFER fabricated in LOW POWER SCHOTTKY technology.

SCHEMATIC





B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

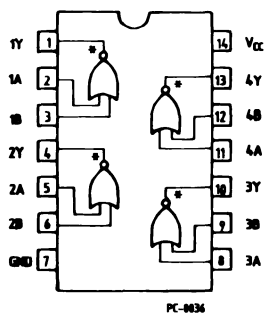
C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS33 D1	T74LS33 C1
T74LS33 B1	T74LS33 M1

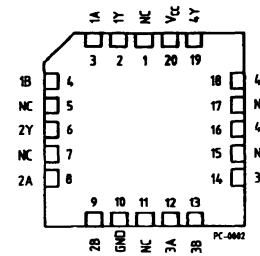
PIN CONNECTION (top view)

DUAL IN LINE



* Open Collector Outputs

CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE

A	B	Y
H	X	L
X	H	L
L	L	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0 5 to 7	V
V_I	Input Voltage, Applied to Input	– 0 5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	60	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS33XX	4 75 V	5 0 V	5 25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2 0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage		- 0 65	- 1 5	V_{CC} = MIN, I_{IN} = -18 mA		V
I_{OH}	Output HIGH Current			100	V_{CC} = MIN, V_{OH} = 5.5 V V_{IN} = V_{IL}		µA
V_{OL}	Output LOW Voltage		0 25	0.4	I_{OL} = 12 mA	V_{CC} = MIN	V
			0.35	0 5	I_{OL} = 24 mA	V_{IN} = 2.0 V	V
I_{IH}	Input HIGH Current		0.1	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{CCH}	Supply Current HIGH		2 0	3.6	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CCL}	Supply Current LOW		10	13.8	V_{CC} = MAX, Inputs Open		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges
2. Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: $T_A = 25^oC$ (for AC test circuits and waveforms see databook introduction)

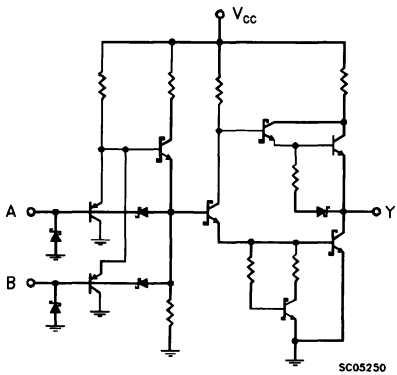
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		20	32	V_{CC} = 5.0 V C_L = 45 pF, R_L = 667 Ω	ns
t_{PHL}	Turn On Delay, Input to Output		18	28		ns

QUAD 2-INPUT NAND BUFFER

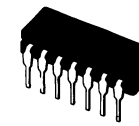
DESCRIPTION

The T74LS37 is a high speed QUAD 2-INPUT NAND BUFFER fabricated in LOW POWER SCHOTTKY technology.

SCHEMATIC



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

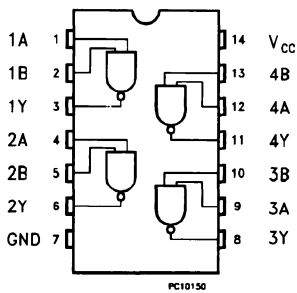
C1
(Plastic Chip Carrier)

ORDER CODES :

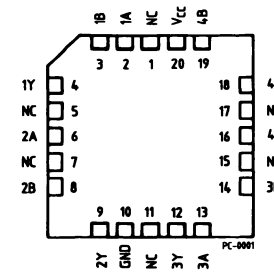
T74LS37 D1	T74LS37 C1
T74LS37 B1	T74LS37 M1

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE

A	B	Y
L	X	H
X	L	H
H	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	- 0.5 to 7	V
V_I	Input Volatge, Applied to Input	- 0.5 to 15	V
V_O	Output Voltage, Applied to Output	- 0.5 to 5.5	V
I_I	Input Current, Into Inputs	- 30 to 5	mA
I_O	Output Current, Into Outputs	60	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS37XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 1.2 mA, V_{IN} = V_{IL}		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 12 mA	V_{CC} = MIN, V_{IN} = 2.0 V	V
			0.35	0.5	I_{OL} = 24 mA		V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 30		- 130	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CCH}	Supply Current HIGH		0.9	2.0	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CCL}	Supply Current LOW		6.0	12	V_{CC} = MAX, Inputs Open		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges
2. Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: $T_A = 25^oC$ (for AC test circuits and waveforms see databook introduction)

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		12	24	V_{CC} = 5.0 V C_L = 45 pF, R_L = 667 Ω	ns
t_{PHL}	Turn On Delay, Input to Output		12	24		ns

SGS-THOMSON MICROELECTRONICS

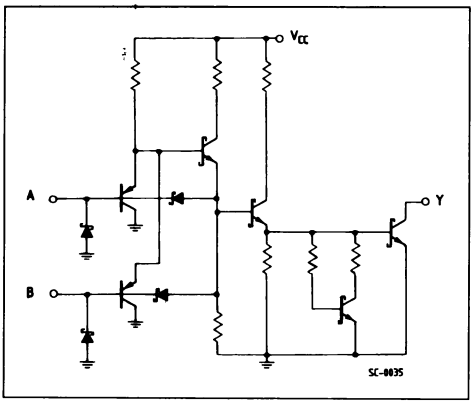
T74LS38

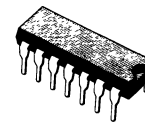
QUAD 2-INPUT NAND BUFFER

DESCRIPTION

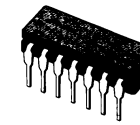
The T74LS38 is a high speed QUAD 2-INPUT NAND BUFFER (open collector outputs) fabricated in LOW POWER SCHOTTKY technology.

SCHEMATIC





B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

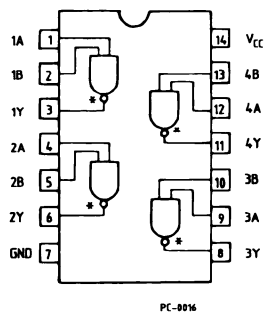
C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS38 D1	T74LS38 C1
T74LS38 B1	T74LS38 M1

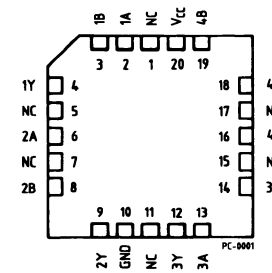
PIN CONNECTION (top view)

DUAL IN LINE



* Open Collector Outputs

CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE

A	B	Y
L	X	H
X	L	H
H	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0 5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0 5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	60	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS38XX	4 75 V	5 0 V	5 25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
I_{OH}	Output HIGH Current			250	V_{CC} = MIN, V_{OH} = 5.5 V V_{IN} = V_{IL}		µA
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 12 mA	V_{CC} = MIN	V
			0 35	0 5	I_{OL} = 24 mA	V_{IN} = 2.0 V	V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{CCH}	Supply Current HIGH		0.9	2.0	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CCL}	Supply Current LOW		6.0	12	V_{CC} = MAX, Inputs Open		mA

Notes : 1 For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C

AC CHARACTERISTICS: $T_A = 25^oC$ (for AC test circuits and waveforms see databook introduction)

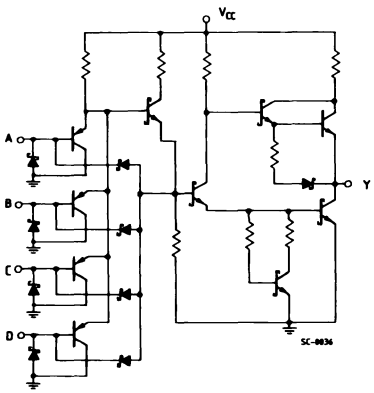
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		20	32	V_{CC} = 5 0 V C_L = 45 pF, R_L = 667 Ω	ns
t_{PHL}	Turn On Delay, Input to Output		18	28		ns

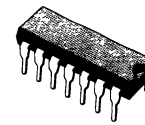
DUAL 4-INPUT NAND BUFFER

DESCRIPTION

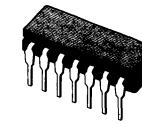
The T74LS40 is a high speed DUAL 4-INPUT NAND BUFFER fabricated in LOW POWER SCHOTTKY technology.

SCHEMATIC





B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

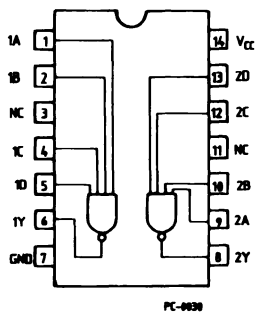
C1
(Plastic Chip Carrier)

ORDER CODES :

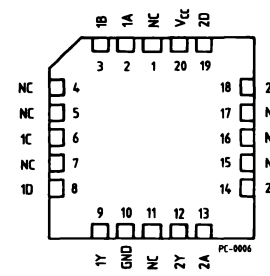
T74LS40 D1	T74LS40 C1
T74LS40 B1	T74LS40 M1

PIN CONNECTION (top view)

DUAL IN LINE

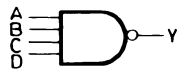


CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE



A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	60	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS40XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 1.2 mA V_{IN} = V_{IL}		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 12 mA	V_{CC} = MIN	V
			0.35	0.5	I_{OL} = 24 mA	V_{IN} = 2.0 V	V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 30		- 130	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CCH}	Supply Current HIGH		0 45	1.0	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CCL}	Supply Current LOW		3.0	6.0	V_{CC} = MAX, Inputs Open		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2 Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: $T_A = 25^oC$ (for AC test circuits and waveforms see databook introduction)

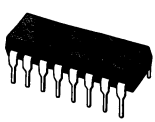
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		12	24	V_{CC} = 5.0 V C_L = 45 pF, R_L = 667 Ω	ns
t_{PHL}	Turn On Delay, Input to Output		12	24		ns

ONE-OF-TEN DECODER

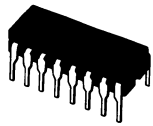
- MULTI-FUNCTION CAPABILITY
- MUTUALLY EXCLUSIVE OUTPUTS
- DEMULTIPLEXING CAPABILITY
- INPUT CLAMP DIODES LIMIT HIGH SPEED
- TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

DESCRIPTION

The LSTTL/MSI T74LS42 is a Multipurpose Decoder designed to accept four BCD inputs and provide ten mutually exclusive outputs. The LS42 is fabricated with the Schottky barrier diode proces for high speed and is completely compatible with all TTL families.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

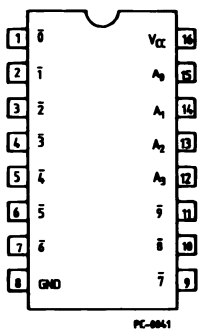
T74LS42 D1 T74LS42 C1
T74LS42 B1 T74LS42 M1

PIN NAMES

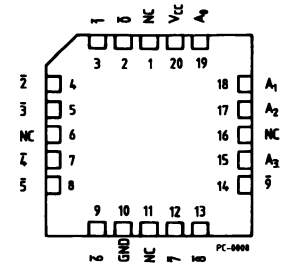
$\underline{A}_0$ to $\underline{A}_3$	ADDRESS INPUTS
0 to 9	OUTPUTS, ACTIVE LOW

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



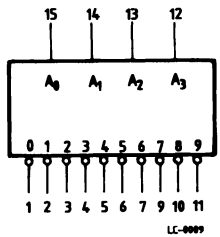
NC = No Internal Connection

TRUTH TABLE

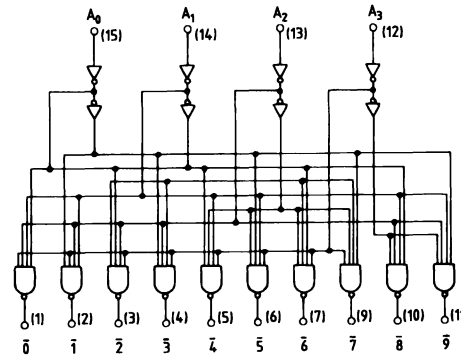
A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC SYMBOL AND LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS42X	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

FUNCTIONAL DESCRIPTION

The LS42 decoder accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs, as shown by logic symbol or diagram. The active LOW outputs facilitate addressing other MSI units with active LOW input enables.

The logic design of the LS42 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant input A_3 produces a useful inhibit function when the LS42 is used as a one-of-eight decoder. The A_3 input can also be used as the Data input in an 8-output demultiplexer application.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Threshold Voltage for all Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Threshold Voltage for all Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		7.0	13	V_{CC} = MAX,		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges
2. Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: T_A = 25°C (for AC test circuits and waveforms see databook introduction)

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Propagation Delay (2 levels)		15	25		ns
t_{PHL}	Fig. 2		15	25	VCC = 5.0 V	ns
t_{PLH}	Propagation Delay (3 levels)		20	30	C_L = 15 pF	ns
t_{PHL}	Fig. 1		20	30		ns

AC WAVEFORMS

Figure 1.

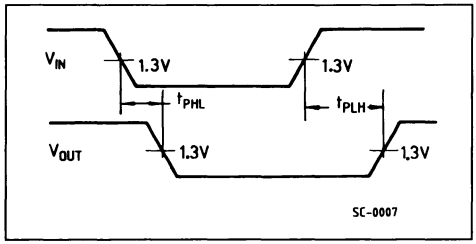
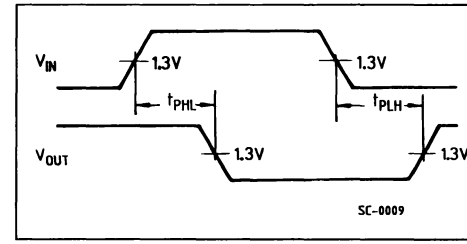


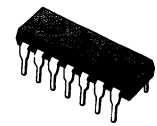
Figure 2.



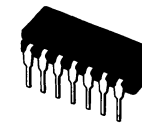
DUAL 2-WIDE 2-INPUT / 3-INPUT AND-OR-INVERT GATE

DESCRIPTION

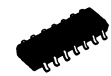
The T74LS51 is a high speed DUAL 2-WIDE 2-INPUT / 3-INPUT AND-OR-INVERT GATE fabricated in LOW POWER SCHOTTKY technology.



B1
(Plastic Package)



D1
(Ceramic Package)



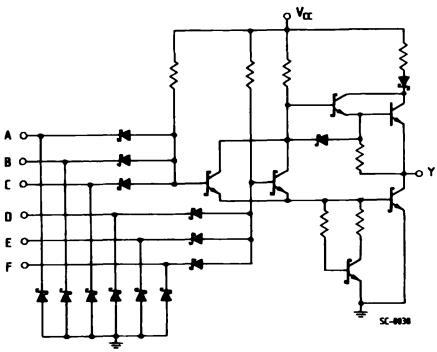
M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

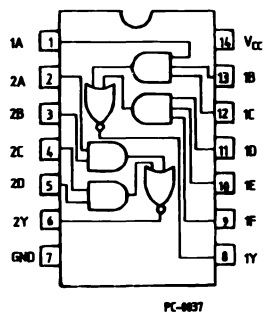
T74LS51 D1	T74LS51 C1
T74LS51 B1	T74LS51 M1

SCHEMATIC

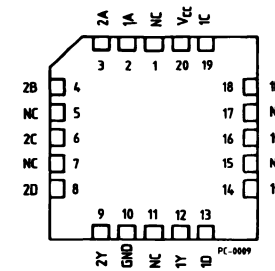


PIN CONNECTION (top view)

DUAL IN LINE

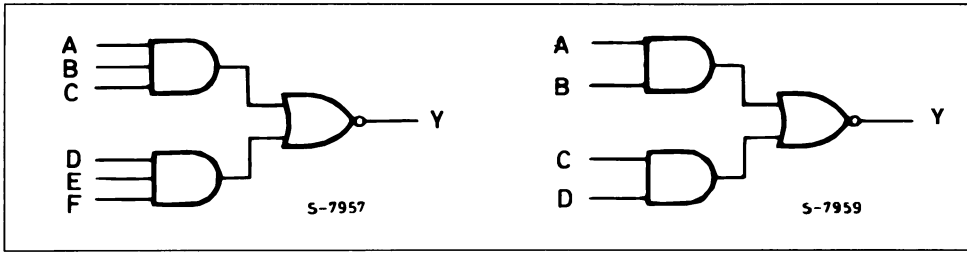


CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 5.5	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS38XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)	Unit
		Min.	Typ. (*)	Max.		
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage	V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage	V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA	V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IL}	V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA, V_{CC} = MIN	V
			0.35	0.5	I_{OL} = 8.0 mA, V_{IN} = 2.0 V	V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V	µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V	mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V	mA
I_{CCH}	Supply Current HIGH		0.8	1.6	V_{CC} = MAX, V_{IN} = 0 V	mA
I_{CCL}	Supply Current LOW		1.4	2.8	V_{CC} = MAX, Inputs Open	mA

Notes : 1 For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2 Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: $T_A = 25^oC$ (for AC test circuits and waveforms see databook introduction)

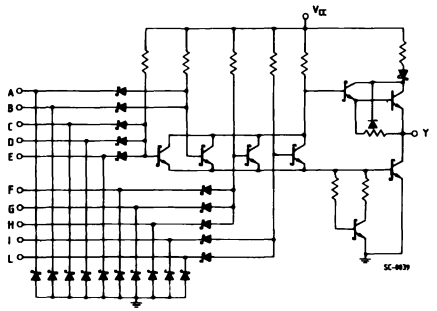
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		12	20	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PHL}	Turn On Delay, Input to Output		12.5	20		ns

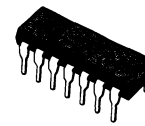
3-2-2-3-INPUT AND-OR-INVERT GATE

DESCRIPTION

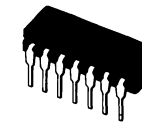
The T74LS54 is a high speed 3-2-2-3-INPUT AND-OR-INVERT GATE fabricated in LOW POWER SCHOTTKY technology.

SCHEMATIC





B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

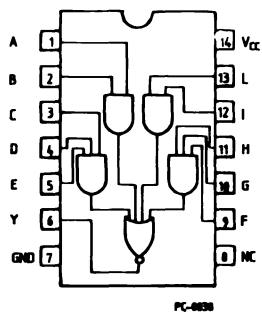
C1
(Plastic Chip Carrier)

ORDER CODES :

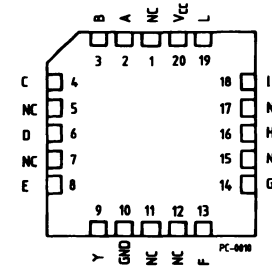
T74LS54 D1	T74LS54 C1
T74LS54 B1	T74LS54 M1

PIN CONNECTION (top view)

DUAL IN LINE

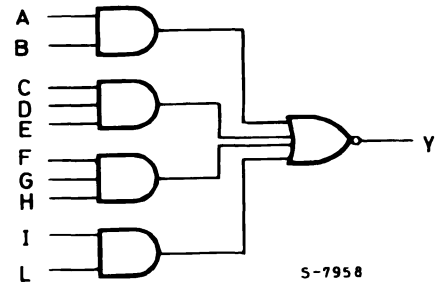


CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	60	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS54XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IL}		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = 2.0 V	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CCH}	Supply Current HIGH		0.8	1.6	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CCL}	Supply Current LOW		1.0	2.0	V_{CC} = MAX, Inputs Open		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2 Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: T_A = 25°C (for AC test circuits and waveforms see databook introduction)

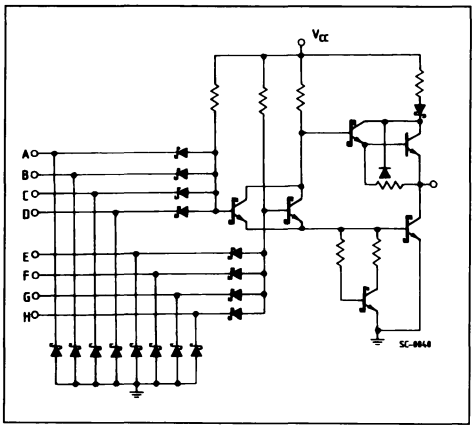
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		12	20	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PHL}	Turn On Delay, Input to Output		12.5	20		ns

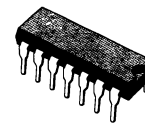
2-WIDE 4-INPUT AND-OR-INVERT GATE

DESCRIPTION

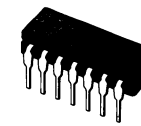
The T74LS55 is a high speed 2-WIDE 4-INPUT AND-OR-INVERT GATE fabricated in LOW POWER SCHOTTKY technology.

SCHEMATIC

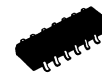




B1
(Plastic Package)



D1
(Ceramic Package)



M1
(Micro Package)

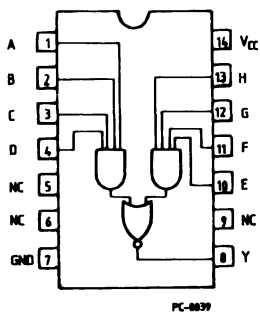
C1
(Plastic Chip Carrier)

ORDER CODES :

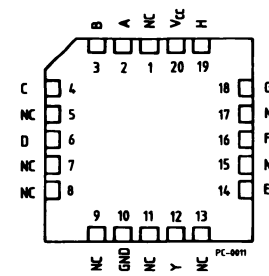
T74LS55 D1
T74LS55 B1
T74LS55 C1
T74LS55 M1

PIN CONNECTION (top view)

DUAL IN LINE

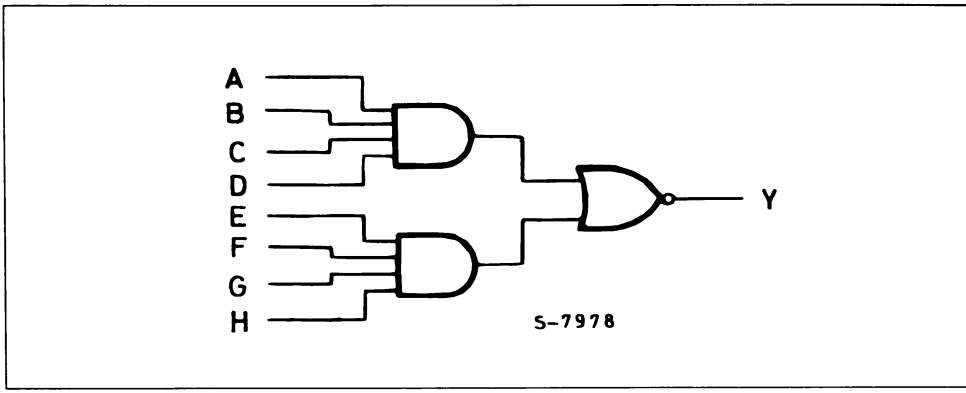


CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	60	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS55XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)	Unit
		Min.	Typ. (*)	Max.		
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage	V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage	V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA	V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IL}	V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA; V_{CC} = MIN	V
			0.35	0.5	I_{OL} = 8.0 mA; V_{IN} = 2.0 V	V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V	µA mA
I_{IL}	Input LOW Current			- 0.36	V_{CC} = MAX, V_{IN} = 0.4 V	mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{IN} = 0 V	mA
I_{CCH}	Supply Current HIGH		0.4	0.8	V_{CC} = MAX, V_{IN} = 0 V	mA
I_{CCL}	Supply Current LOW		0.7	1.3	V_{CC} = MAX, Inputs Open	mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges
2. Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: T_A = 25°C (for AC test circuits and waveforms see databook introduction)

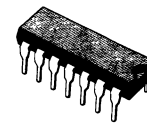
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		12	20	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PHL}	Turn On Delay, Input to Output		12.5	20		ns

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

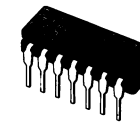
DESCRIPTION

The T74LS74A dual edge-triggered flip-flop utilizes Schottky TTL circuitry to produce high speed D-type flip-flops. Each flip-flop has individual clear and set inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or the LOW level, the D input signal has no effect.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

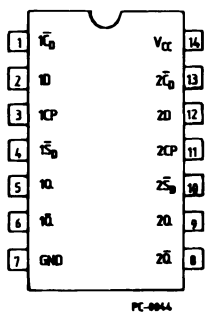
C1
(Plastic Chip Carrier)

ORDER CODES :

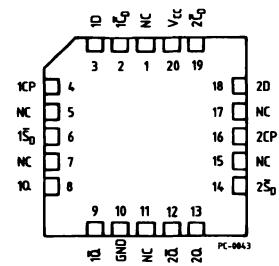
T74LS74A D1	T74LS74A C1
T74LS74A B1	T74LS74A M1

PIN CONNECTION (top view)

DUAL IN LINE

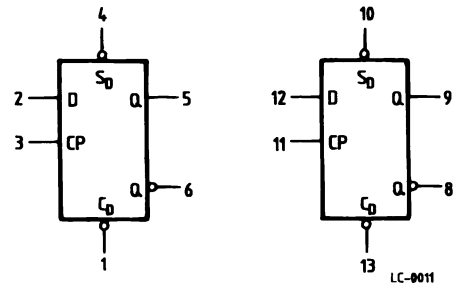


CHIP CARRIER

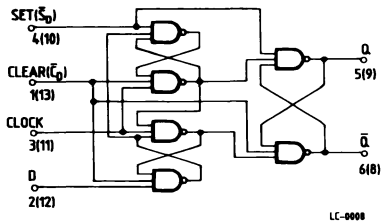


NC = No Internal Connection

LOGIC SYMBOL



LOGIC DIAGRAM AND TRUTH TABLE



V_{CC} = Pin 11
GND = Pin 4
( ) = Pin numbers

Operating Mode	Inputs			Outputs	
	$\overline{S}_D$	$\overline{C}_D$	D	Q	$\overline{Q}$
Set	L	H	X	H	L
Reset (clear)	H	L	X	L	H
* Undetermined	L	L	X	H	H
Load "1" (set)	H	H	h	H	L
Load "0" (reset)	H	H	l	L	H

* Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.
The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable ; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h, (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS74AXX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Condition (note 1)		Unit
			Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage		2.0			Guaranteed Input HIGH Voltage for All Input		V
V_{IL}	Input LOW Voltage				0.8	Guaranteed Input LOW Voltage for All Input		V
V_{CD}	Input Clamp Diode Voltage			- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage		2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage			0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
				0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current	Data, Clock Set, Clear			20 40	V_{CC} = MAX, V_{IN} = 2.7 V		µA
		Data, Clock Set, Clear			0.1 0.2	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current	Data, Clock Set, Clear			- 0.4 - 0.8	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)		- 20		- 100	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CC}	Power Supply Current				8.0	V_{CC} = MAX		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under garanteed operating ranges .
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

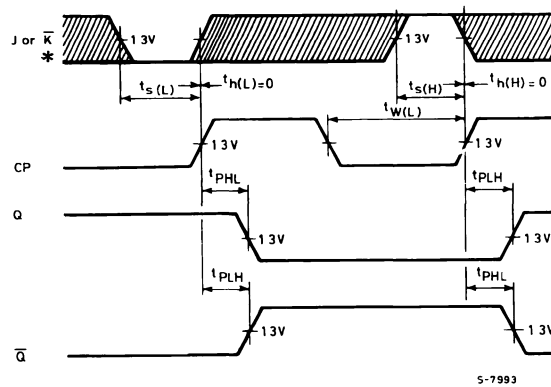
Symbol	Parameter	Limits			Tests Conditions		Unit
		Min.	Typ.	Max.			
f_{MAX}	Maximum Clock Frequency	25	33		Fig. 1	V_{CC} = 5.0 V C_L = 15 pF	MHz
t_{PLH} t_{PHL}	Clock, Clear, Set to Output		13 25	25 40	Fig. 1		ns

AC SET-UP REQUIREMENTS : T_A = 25 °C

Symbol	Parameter		Limits			Test Conditions		Unit
			Min.	Typ.	Max.			
t_W	Clock, Clear, Set Pulse Width		25			Fig. 3	V_{CC} = 5.0 V	ns
t_s	Data Set-up Time	HIGH	25			Fig. 3		ns
		LOW	20					ns
t_h	Hold Time		5			Fig 3		ns

AC WAVEFORMS

Figure 1 : Clock to Output Delays, Data Set-up and Hold Times, Clock Pulse Width.



* The shaded areas indicate when the input is permitted to change for predictable output performance

Figure 2 : Set and Clear to Output Delays, Set and Clear Pulse Widths.

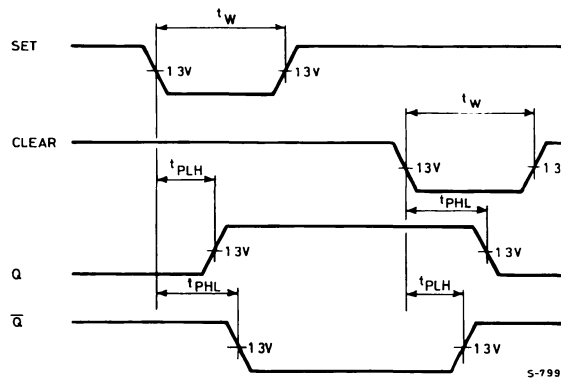
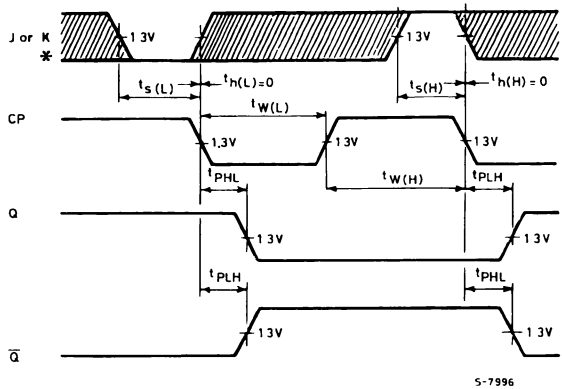


Figure 3 : Clock to Output Delays, Data Set-up and Hold Times, Clock Pulse Width.

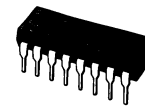


* The shaded areas indicate when the input is permitted to change for predictable output performance.

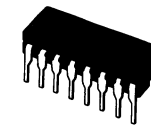
DUAL 4-INPUT MULTIPLEXER

DESCRIPTION

The T74LS75 is a 4-bit D latch; it is applied as temporary storage for binary information between processing units and input/output or indicator units. When the Enable is HIGH, the information present at data (D) input shifts to the Q output, wich follows the data input on conditio that the Enable remains HIGH. If the Enable goes LOW, the information is kept at the Q output until the Enable is allowed to go HIGH.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

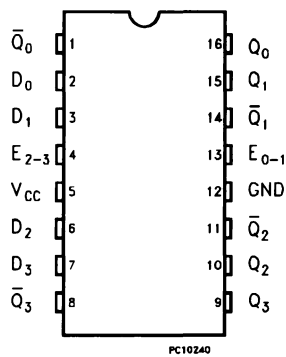
T74LS75 D1 T74LS75 C1
T74LS75 B1 T74LS75 M1

PIN NAMES

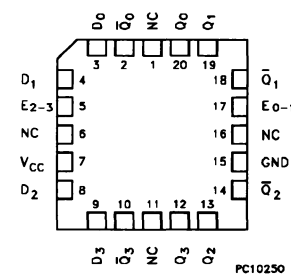
D_1-D_4	Data Inputs
E_{0-1}	Enable Input Latches 0, 1
E_{2-3}	Enable Input Latches 2, 3
Q_1-Q_4	Latch Outputs
$\overline{Q}_1$-$\overline{Q}_4$	Compementary Latch Outputs

PIN CONNECTION (top view)

DUAL IN LINE

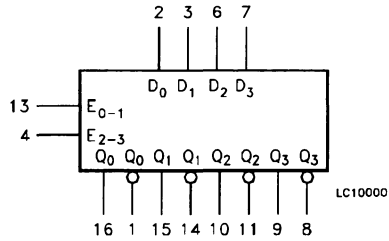


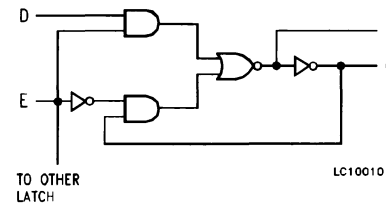
CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM AND TRUTH TABLE





(Each Latch)

t_n	t_{n+1}
D	Q
H	H
L	L

Notes: t_n = bit time before clock negative-going transition
t_{n+1} = bit time after clock negative-going transition

V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS75XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Condition (note 1)		Unit
			Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage		2.0			Guaranteed Input HIGH Voltage for All Input		V
V_{IL}	Input LOW Voltage				0.8	Guaranteed Input LOW Voltage for All Input		V
V_{CD}	Input Clamp Diode Voltage			- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage		2.7	3.5		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage			0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
				0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current	D Input E Input			20 80	V_{CC} = MAX, V_{IN} = 2.7 V		µA
		D Input E Input			0.1 0.4	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current	D Input E Input			- 0.4 - 1.6	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)		- 20		- 100	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CC}	Power Supply Current				12	V_{CC} = MAX		mA

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: T_A = 25 °C

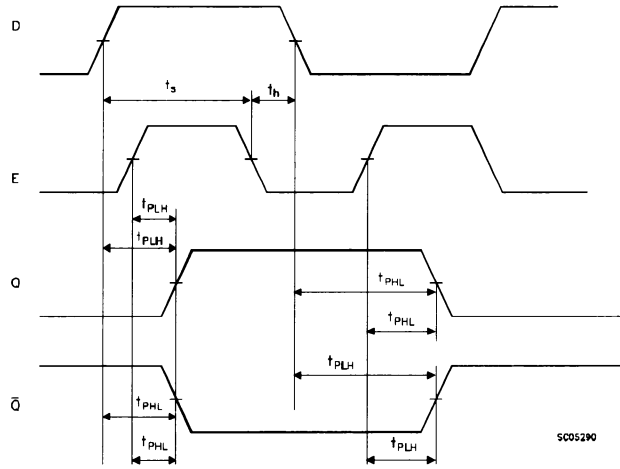
Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay, Data to Q		15 9.0	27 17	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PLH} t_{PHL}	Propagation Delay, Data to $\overline{Q}$		12 7.0	20 15		ns
t_{PLH} t_{PHL}	Propagation Delay, Enable to Q		15 14	27 25		ns
t_{PLH} t_{PHL}	Propagation Delay, Enable to $\overline{Q}$		16 7.0	30 15		ns
t_W	Enable Pulse Width	20			V_{CC} = 5.0 V	ns
t_s	Set-up Time	20				ns
t_h	Hold Time	5				ns

DEFINITION OF TERMS:

SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) - is defined as the maximum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

AC WAVEFORMS



SGS-THOMSON MICROELECTRONICS

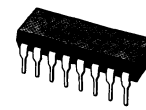
T74LS83A

4-BIT BINARY FULL ADDER WITH FAST CARRY

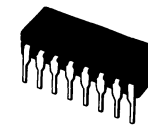
DESCRIPTION

The T74LS83A is a high-speed 4-Bit Binary Full Adder with internal carry lookahead.

It accepts two 4-bit binary words (A_1-A_4, B_1-B_4) and a Carry (C_{IN}). It ganerates the binary Sum outputs (Σ_1-Σ_4) and the Carry Output (C_{OUT}) from the most significant bit. The LS83A operates with either active HIGH or LOW operand (positive or negative logic). The T74LS83A is recommented for new designs since it is identical in function with this device and features standard corner power pins.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

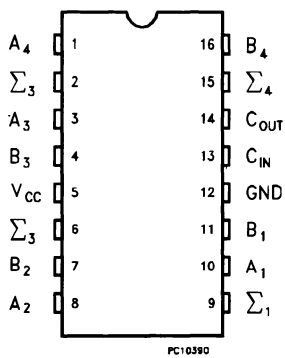
T74LS83A D1
T74LS83A B1
T74LS83A C1
T74LS83A M1

PIN NAMES

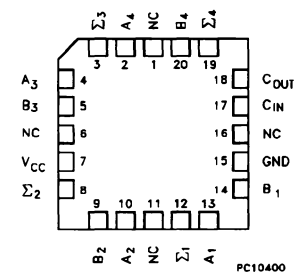
A_1-A_4	Operand A Inputs
B_1-B_4	Operand B Inputs
C_{IN}	Carry Inputs
S_1-S_4	Sum Outputs
C_{OUT}	Carry Outputs

PIN CONNECTION (top view)

DUAL IN LINE

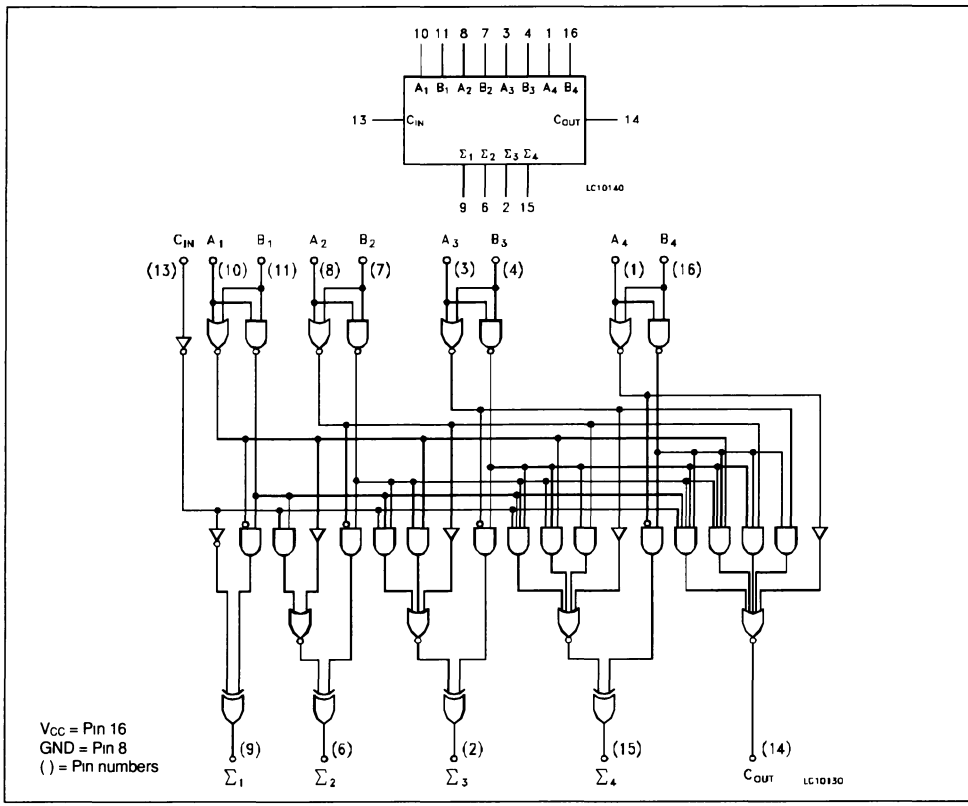


CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS83AXX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

FUNCTIONAL DESCRIPTION

The LS83A adds to 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs (Σ_1-Σ_4) and outgoing carry (C_{OUT}) outputs.

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{OUT}$$

Where : (+) = plus

Due to the symmetry of the binary add function the LS83A can be used with either all input and otput active HIGH (positive logic) or with all inputs and output active LOW (negative logic).

Note that with active HIGH inputs Carry In can not be left open, but must be held LOW when no carry in is intended.

Example:

	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}	
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	10 + 9 = 19
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	Carry + 5 + 6 = 12

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Input		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Input		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.5		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current CIN Any A or B			 20 40	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	CIN Any A or B			0.1 0.2	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current CIN Any A or B			 - 0.4 - 0.8	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CC}	Power Supply Current		22 19	39 34	V_{CC} = MAX, All Inputs 0 V V_{CC} = MAX, A Inputs = 4.5 V		mA

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay, C_{IN} Input to Any Σ Output		16 15	24 24	V_{CC} = 5.0 V C_L = 15 pF Figures 1 and 2	ns
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to Σ Output		15 15	24 24		ns
t_{PLH} t_{PHL}	Propagation Delay, CIN Input to C_{OUT} Output		11 15	17 22		ns
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to COUT Output		11 12	17 17		ns

AC WAVEFORMS

Figure 1

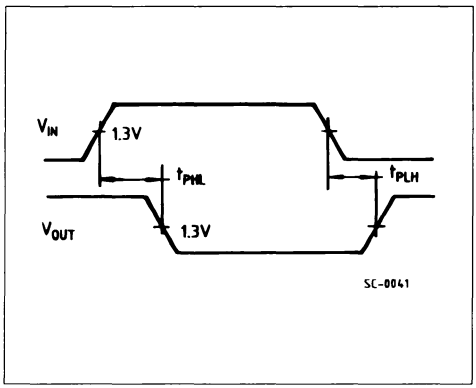
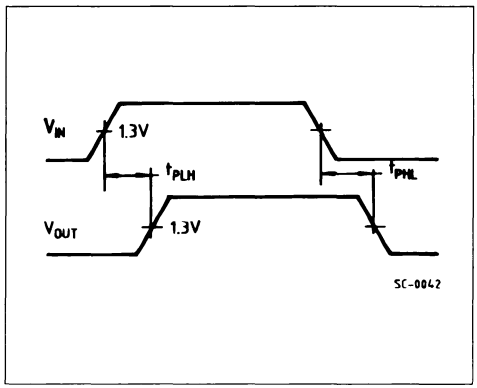


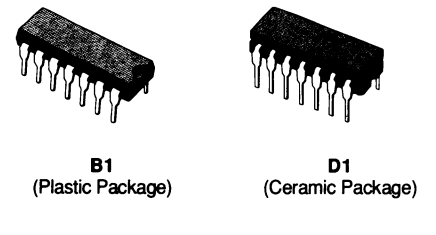
Figure 2



QUAD 2-INPUT EXCLUSIVE OR GATE

DESCRIPTION

The T74LS86 is a high speed QUAD 2-INPUT EXCLUSIVE OR GATE fabricated in LOW POWER SHOTTKY technology.



B1
(Plastic Package)

D1
(Ceramic Package)

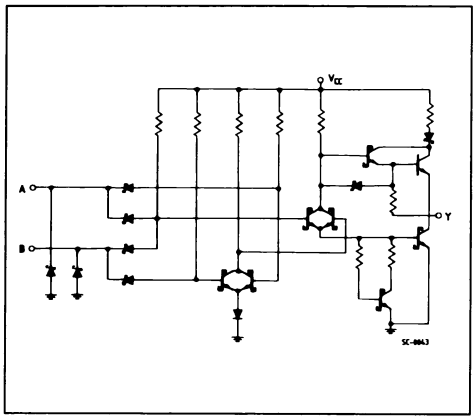
M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

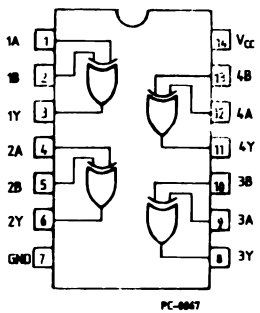
T74LS86 D1	T74LS86 C1
T74LS86 B1	T74LS86 M1

SCHEMATIC

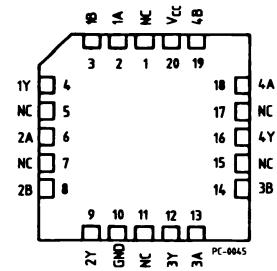


PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE

In		Out
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	60	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS86XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current			40 0.2	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.6	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CCH}	Supply Current HIGH		6.0	10	V_{CC} = MAX		mA

Notes : 1 For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: $T_A = 25^oC$ (for AC test circuits and waveforms see databook introduction)

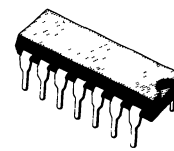
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Propagation Delay Other		12	23	VCC = 5.0 V C_L = 15 pF	ns
t_{PHL}	Input LOW		10	17		ns
t_{PLH}	Propagation Delay Other		10	30		ns
t_{PHL}	Input HIGH		13	22		ns

SGS-THOMSON MICROELECTRONICS

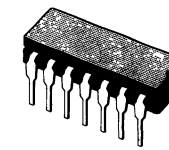
T74LS90
T74LS92/93

COUNTERS: LS90 DECADE LS92 DIVIDE BY TWELVE LS93 4-BIT BINARY

- LOW POWER CONSUMPTION TYPICALLY 45 mW
- HIGH COUNT RATES TYP 50 MHz
- CHOICE OF COUNTING MODES BCD, BI-QUINARY, DIVIDE-BY-TWELVE BINARY
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND MOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LSXX D1	T74LSXX C1
T74LSXX B1	T74LSXX M1

PIN NAMES

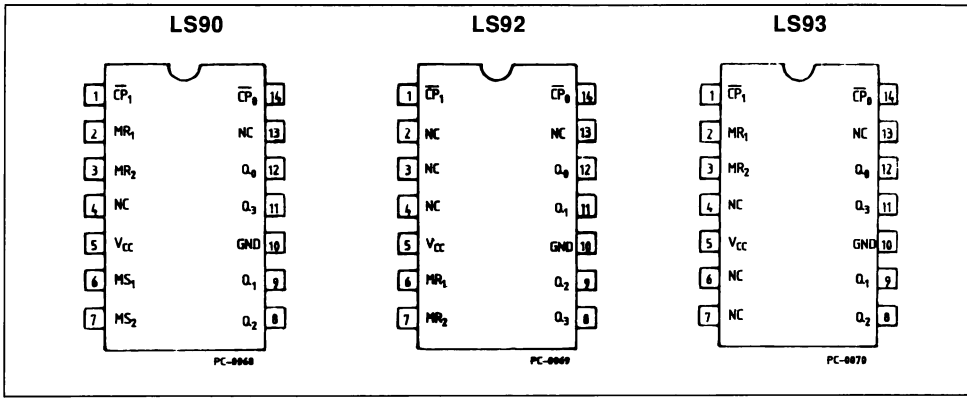
$\overline{CP}_0$	Clock (Active LOW Going Edge) Input to ÷ 2 Section
$\overline{CP}_1$	Clock (Active LOW Going Edge) Input to ÷ 5 Section (LS90), ÷ 6 Section (LS92)
$\overline{CP}_1$	Clock (Active LOW Going Edge) Input to ÷ 8 Section (LS93)
MR_1, MR_2	Master Reset (Clear) Inputs
MS_1, MS_2	Master Set (Preset-9, LS90) Inputs
Q_0	Output from ÷ 2 Section
Q_1, Q_2, Q_3	Outputs from ÷ 6 (LS90), ÷ 6 (LS92), ÷ 8 (LS93) Section

Note : The Q_0 Outputs are guaranteed to drive the full fan out plus the $\overline{CP}_1$ input of the device.

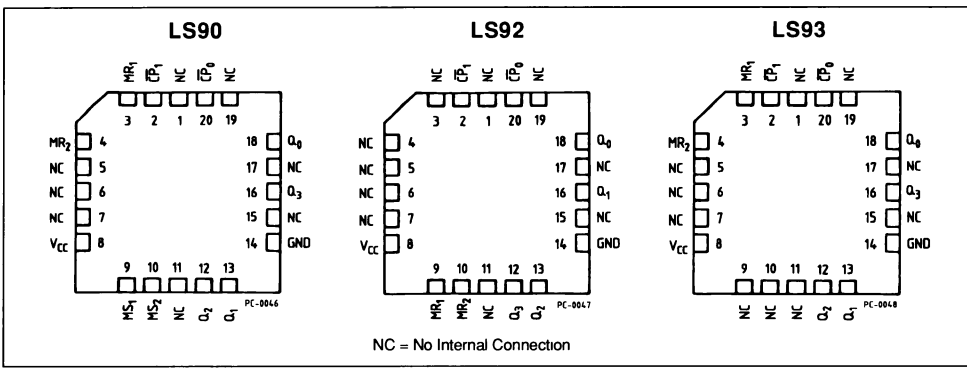
DESCRIPTION

The T74LS90 T74LS92 and T74LS93 are high speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS90), or divide-by-eight (LS93) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to $\overline{CP}$) to from BCD, bi-quinary, modulo-12, or modulo-16 counters. All of the counters have a 2-input gated Master Reset (Clear), and the LS90 also has a 2-input gated Master Set (Preset 9).

PIN CONNECTION (top view)



CHIP CARRIER



NC = No Internal Connection

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

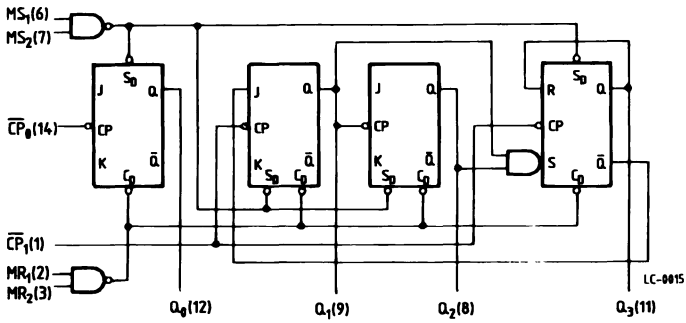
GUARANTEED OPERATING RANGE

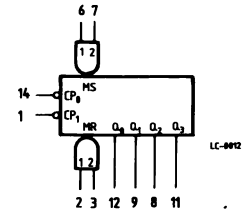
Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS90/92/93XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

LOGIC DIAGRAM AND LOGIC SYMBOL

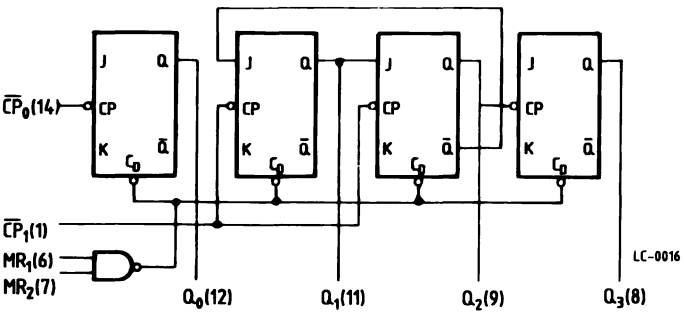
LS90

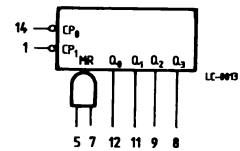




NC = Pins 4, 13

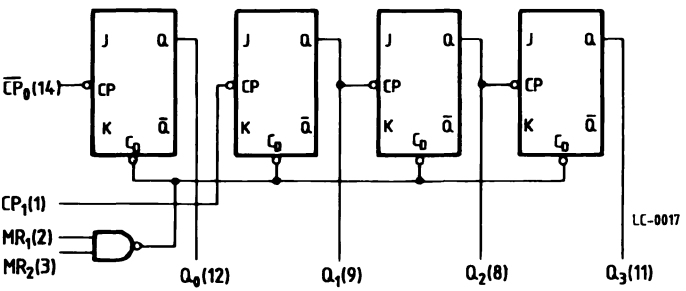
LS92

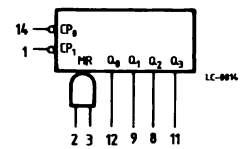




NC = Pins 2, 3, 4, 13

LS93





NC = Pins 4, 6, 7, 13

V_{CC} = Pin 5
GND = Pin 10
( ) = Pin numbers.

FUNCTIONAL DESCRIPTION

The LS90 LS92 and LS93 are 4-bit ripple type Decade, Divide-By-Twelve and Binary Counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS90), divide by six (LS92) or divide-by-eigh (LS93) section. Each section has a separate clock input which initiates state change of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input of the device.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided on all counters which overrides and clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set ($MS_1 \cdot MS_2$) is provided on the LS90 which overrrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.

LS90

A. BCD Decade (8421) Counter - The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Bi-quinary Divide-By-Ten counter. The Q_3 output must be externally connected to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at outpt Q_0.

C. Divide-By-Two and Divide-By-Five counter - No external interconections are required. The first flip-flop is used as a binary element for the divide-by-two ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain binary divide-by-five operation at the Q_3 output.

LS92

A. Modulo12, Divide By Twelve Counter - The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receivers the incoming count and Q_3 produces a symmetrical divide by twelve square wave output.

B. Divide By Two and Divide By Six Counter - External interconnections are required. The first flip-flop is used as a binary element for the divide by two function. The $\overline{CP}_1$ input is used to obtain divide by three operation at the Q_1 and Q_2 outputs and divide by six at the Q_3 output.

LS93

A. 4-bit Ripple Counter - The output Q_0 must be externally connected to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2 and Q_3 outputs as shown in the truth table.

B. 3-Bit Ripple Counter - the input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions fo 2, 4, and 8 are available at the Q_1, Q_2 and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple through counter.

MODE SELECTION LS90

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care.

MODE SELECTION LS92 AND LS93

RESET/INPUTS		OUTPUT			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

BCD COUNT SEQUENCE LS90

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

Note : Output Q_0 connected to input $\overline{CP_1}$ for BCD count.

TRUTH TABLE LS92

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H

Note : Output Q_0 connected to input $\overline{CP_1}$

TRUTH TABLE LS93

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Note : Output Q_0 connected to input $\overline{CP_1}$

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Threshold Voltage for All Input		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Threshold Voltage for All Input		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4 0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current MS, MR $\overline{CP_0}$ $\overline{CP_1}$ (LS93) $\overline{CP_1}$ (LS90, LS92)			 2.0 120 40 80	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	MS, MR			0.1	V_{CC} = MAX, V_{IN} = 7.0 V		mA
	$\overline{CP_0}$, $\overline{CP_1}$ (LS93) $\overline{CP_1}$ (LS90, LS92)			0.4 0.8	V_{CC} = MAX, V_{IN} = 5.5 V		mA
I_{IL}	Input LOW Current MS, MR $\overline{CP_0}$ $\overline{CP_1}$ (LS93) $\overline{CP_1}$ (LS90, LS92)			 - 0.4 - 2.4 - 1.6 - 3.2	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CC}	Power Supply Current		9	15	V_{CC} = MAX		mA

Notes : 1 Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2 Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C

AC SET-UP REQUIREMENTS: T_A = 25 °C, V_{CC} = 5.0 V

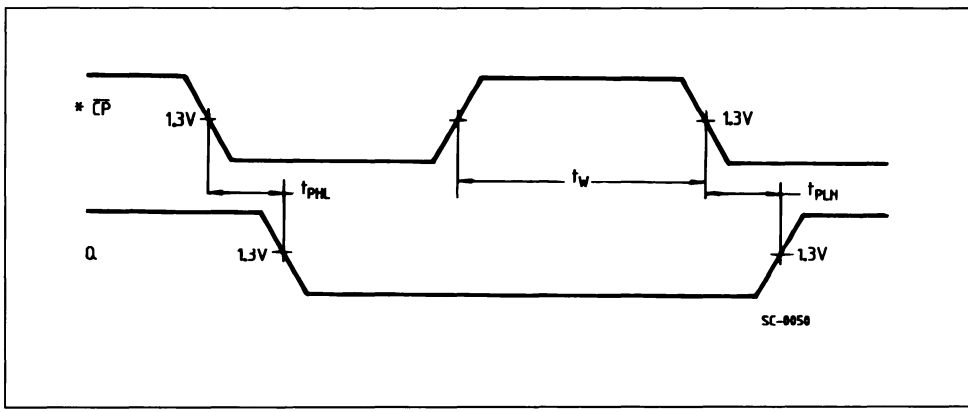
Symbol	Parameter	Limits						Note	Units
		LS90		LS92		LS93			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_W	$\overline{CP_0}$ Pulse Width	15		15		15		Fig. 1	ns
t_W	CP_1 Pulse Width	30		30		30		Fig. 1	
t_W	MR Pulse Width	30		30		30		Fig. 2	
t_W	MS Pulse Width	30						Fig. 2, 3	
t_{rec}	Recovery Time MR to $\overline{CP}$	25		25		25		Fig. 2	
t_{rec}	Recovery Time MS to $\overline{CP}$	25						Fig. 2, 3	

RECOVERY TIME (trec) - is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH to LOW in order to recognize and transfer HIGH data to Q output

AC CHARACTERISTICS T_A = 25 °C, V_{CC} = 5.0 V, C_L = 15 pF

Symbol	Parameter	Limits						Note	Unit
		LS90		LS92		LS93			
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{MAX}	$\overline{CP}_0$ Input Count Frequency	32		32		32		Fig. 1	MHz
f_{MAX}	$\overline{CP}_1$ Input Count Frequency	16		16		16		Fig. 1	MHz
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_0$ Input to Q_0 Output		16 18		16 18		16 18	Fig. 1	ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_1$ Input to Q_1 Output		16 21		16 21		16 21	Fig. 1	ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_1$ Input to Q_2 Output		32 35		16 21		32 35	Fig. 1	ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_1$ Input to Q_3 Output		32 35		32 35		51 51	Fig. 1	ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_0$ Input to Q_3 Output		48 50		48 50		70 70	Fig. 1	ns
t_{PHL}	MS Input to Q_0 and Q_3 Outputs		30					Fig. 3	ns
t_{PHL}	MS Input to Q_1 and Q_2 Outputs		40					Fig. 2	ns
t_{PHL}	MR Input to any Output		40		40		40	Fig. 2	ns

Figure1.



* The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Tables.

Figure 2.

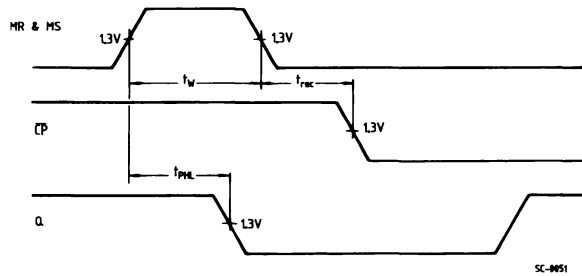
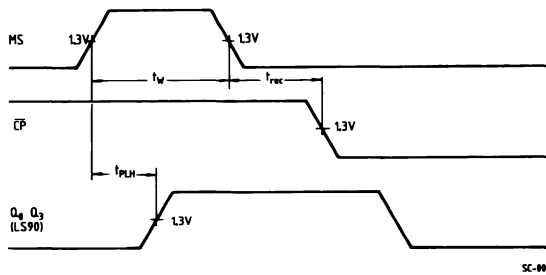


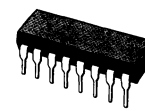
Figure 3.



8-BIT SHIFT REGISTER

DESCRIPTION

The T74LS91 is an 8 Bit Serial-In/Serial-Out Shift Register. This device is composed of eight RS master slave flip-flops, input gating and a clock driver. Single-rail data and input control are gated through inputs A, B and an internal inverter, in order to form the complementary inputs to the first bit of the shift register. Drive for internal common clock line is obtained by means of an inverter. The clock signal inverter driver causes this circuitry to shift information one-bit on the positive edge of the input clock pulse.



B1
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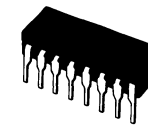


D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS91 D1 T74LS91 C1
T74LS91 B1 T74LS91 M1

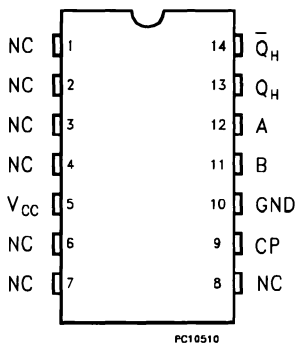
TRUTH TABLE

INPUTS AT t_n		OUTPUTS AT t_{n+8}	
A	B	O_H	$\overline{O}_H$
H	H	H	L
L	X	L	H
X	L	L	H

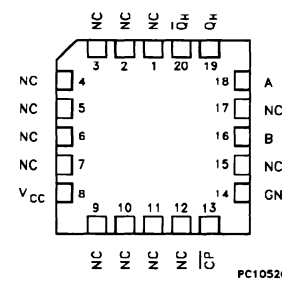
H = HIGH, L = LOW, X = Don't Care
t_n = Reference bit time
t_{n+8} = Bit time after LOW to High Clock Transition

PIN CONNECTION (top view)

DUAL IN LINE

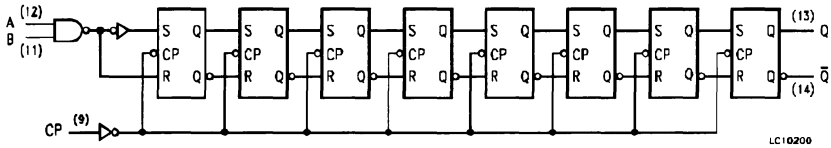


CHIP CARRIER



NC = No Internal Connection

FUNCTIONAL BLOCK DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	- 0.5 to 7	V
V_I	Input Voltage, Applied to Input	- 0.5 to 15	V
V_O	Output Voltage, Applied to Output	- 0.5 to 10	V
I_I	Input Current, Into Inputs	- 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS91XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Input		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Input		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.5		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current			20	V_{CC} = MAX		mA

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
f_{MAX}	Maximum Clock Frequency	10	18		V_{CC} = 5.0 V C_L = 15 pF	MHz
t_{PLH} t_{PHL}	Propagation Delay		24 27	40 40		ns

AC SET-UP REQUIREMENTS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
t_W	Clear Pulse Width	25			V_{CC} = 5.0 V	ns
t_s	Set-Up Time	25				ns
t_h	Hold Time	0				ns

SGS-THOMSON MICROELECTRONICS

T74LS95B

4-BIT SHIFT REGISTER

- SYNCHRONOUS, EXPANDABLE SHIFT RIGHT
- SYNCHRONOUS, SHIFT LEFT CAPABILITY
- SYNCHRONOUS, PARALLEL LOAD
- SEPARATE SHIFT AND LOAD CLOCK INPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

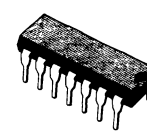
DESCRIPTION

The T74LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel D inputs to the Q outputs synchronous with the HIGH to LOW transition of the appropriate clock input.

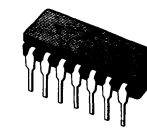
PIN NAMES

S	MODE CONTROL INPUT
D_S	SERIAL DATA INPUT
$\underline{P_0}$-P_3	PARALLEL DATA INPUTS
CP_1	SERIAL CLOCK (active LOW going edge) INPUT
$\overline{CP_2}$	PARALLEL CLOCK (active LOW going edge) INPUT
Q_0-Q_3	PARALLEL OUTPUTS

The LS95B is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all TTL families.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

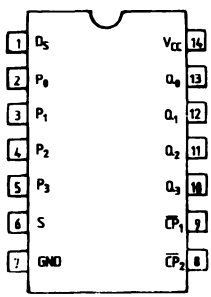
C1
(Plastic Chip Carrier)

ORDER CODES :

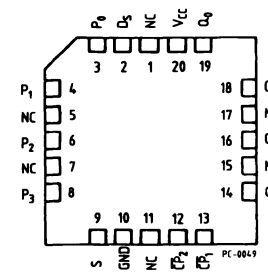
T74LS95B D1 T74LS95B C1
T74LS95B B1 T74LS95B M1

PIN CONNECTION (top view)

DUAL IN LINE

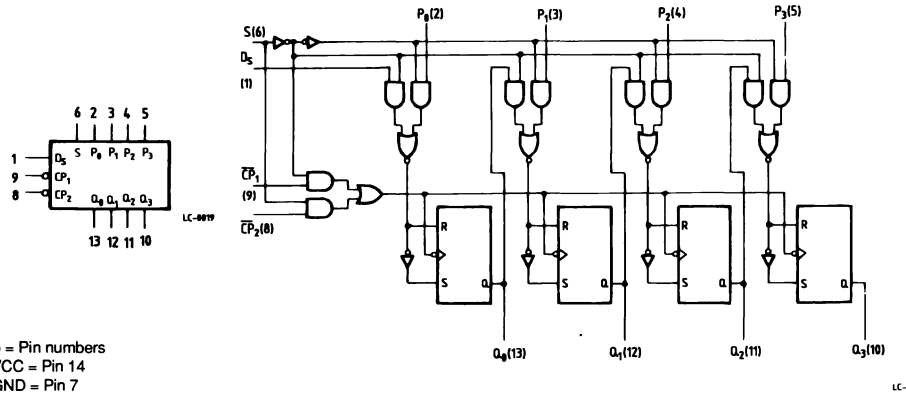


CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND LOGIC SYMBOL



() = Pin numbers
VCC = Pin 14
GND = Pin 7

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	60	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS95BXX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

TRUTH TABLE

Operating Mode	Inputs					Outputs			
	S	$\overline{CP}_1$	$\overline{CP}_2$	D_S	P_n	Q_0	Q_1	Q_2	Q_3
Shift	L	⊓	X	l	X	L	q_0	q_1	q_2
	L	⊓	X	h	X	H	q_0	q_1	q_2
Parallel Load	H	X	⊓	X	p_n	p_0	p_1	p_2	p_3
Mode Change	⊓	L	L	X	X	No Change			
	⊔	L	L	X	X	No Change			
	⊓	H	L	X	X	No Change			
	⊔	H	L	X	X	Undetermined			
	⊓	L	H	X	X	Undetermined			
	⊔	L	H	X	X	No Change			
	⊓	H	H	X	X	Undetermined			
	⊔	H	H	X	X	No Change			

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
l = LOW Voltage Level one set-up time prior to the High to LOW clock transition.
h = HIGH Voltage Level one set-up time prior to the HIGH to LOW clock transition.
Pn = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock Transition.

FUNCTIONAL DESCRIPTION

The LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a Serial (D_S) and four Parallel (P_0-P_3) Data inputs and four Parallel Data outputs (Q_0-Q_3). The serial or parallel mode of operation is controlled by a Mode Control input (S) and two Clock inputs ($\overline{CP}_1$) and ($\overline{CP}_2$). The serial (right-shift) or parallel data transfers occur synchronous with the HIGH to LOW transition of the selected clock input.

When the Mode Control input (S) is HIGH, $\overline{CP}_2$ is enabled. A HIGH to LOW transition on enabled $\overline{CP}$ 2 transfers parallel data from the P_0-P_3 inputs to the Q_0-Q_3 outputs.

When the Mode Control input (S) is LOW, $\overline{CP}_1$ is enable. A HIGH to LOW transition on enabled $\overline{CP}_1$ transfers the data from serial input (D_S) to Q_0 and shifts the data in Q_0 to Q_1, Q_1 to Q_2, and Q_2 to Q_3 respectively (right-shift). A left-shift is accomplished by externally connecting Q_3 to P_2, Q_2 to P_1, and Q_1 to P_0, and operating the LS95B in the parallel mode (S = HIGH).

For normal operation, S should only change states when both Clock inputs are LOW. However, changing S from LOW to HIGH while $\overline{CP}_2$ is HIGH, or changing S from HIGH to LOW while $\overline{CP}_1$ is HIGH and $\overline{CP}_2$ is LOW will not cause any changes on the register outputs.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current D_S, P_0, P_1, P_2, P_3, $\overline{CP_1}$, $\overline{CP_2}$, S			20 40	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	D_S, P_0, P_1, P_2, P_3, $\overline{CP_1}$, $\overline{CP_2}$, S			0.1 0.2	V_{CC} = MAX, V_{IN} = 7 0 V		mA
I_{IL}	Input LOW Current D_S, P_0, P_1, P_2, P_3, $\overline{CP_1}$, $\overline{CP_2}$, S			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		13	21	V_{CC} = MAX		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C

AC SET-UP REQUIREMENTS : T_A = 25 °C

Symbol	Parameter	Limits			Tests Conditions		Unit
		Min.	Typ.	Max.			
t_W(CP)	Clock Pulse Width	25			Fig. 1	V_{CC} = 5.0 V C_L = 15 pF	ns
t_s(data)	Set-up Time, Data to Clock	20			Fig. 1		ns
t_h(data)	Hold Time, Data to Clock	20					ns
t_{sL}	Set-up Time LOW Mode Control to Clock	20			Fig. 1		ns
t_{hL}	Hold Time, LOW Mode Control to Clock	0					ns
t_{sH}	Set-up Time, HIGH Mode Control to Clock	20			Fig. 1		ns
t_{hH}	Hold Time, HOGH Mode Control to Clock	0					ns

SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transfered to the output.
HOLD TIME (t_h) - is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be mantained at the input in order to ensure continued recognition A negative HOLD TIME indicates that the correct logic level may be relased prior to the clock transition from HIGH to LOW and still be recognized

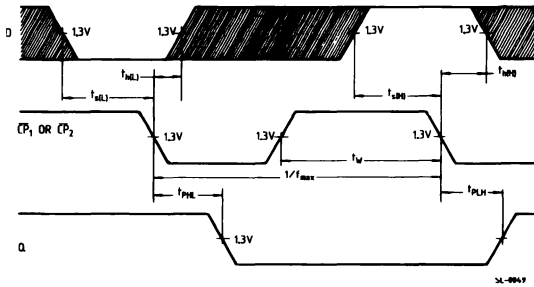
AC CHARACTERISTICS : (T_A = 25 °C)

Symbol	Parameter	Limits			Tests Conditions		Unit
		Min.	Typ.	Max.			
f_{MAX}	Shift Frequency	25	36		Fig. 1	V_{CC} = 5.0 V C_L = 15 pF	MHz
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		18 21	27 32	Fig. 2		ns

AC WAVEFORMS

Figure 1.

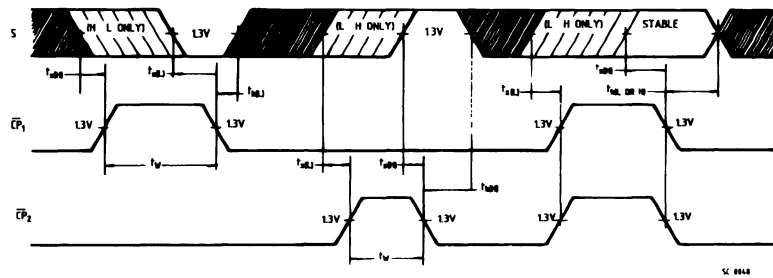
The shaded areas indicate when the input is permitted to change for predictable output performance



* The Data Input is (D_S for $\overline{CP_1}$) or (P_n for $\overline{CP_2}$)

Figure 2.

The shaded areas indicate when the input is permitted to change for predictable output performance



* The Data Input is (D_S for $\overline{CP_1}$) or (P_n for $\overline{CP_2}$)

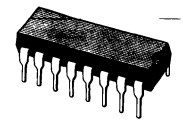
SGS-THOMSON MICROELECTRONICS

T74LS109A

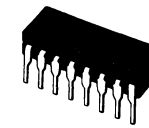
DUAL JK POSITIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION

The T74LS109A consist of two high speed completely independent transition clocked $J\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The $J\overline{K}$ design allows operation as a D flip-flop by simply connecting the J and K pins together.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

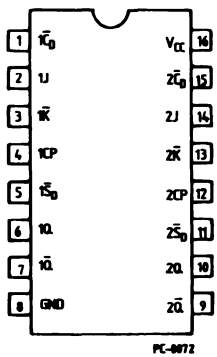
C1
(Plastic Chip Carrier)

ORDER CODES :

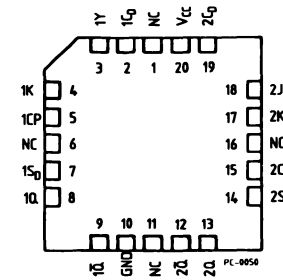
T74LS109A D1	T74LS109A C1
T74LS109A B1	T74LS109A M1

PIN CONNECTION (top view)

DUAL IN LINE

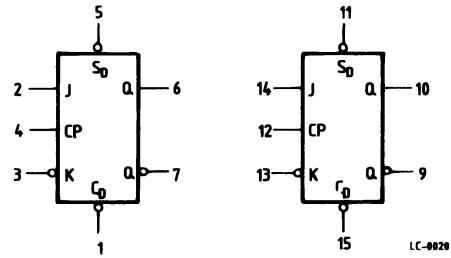


CHIP CARRIER

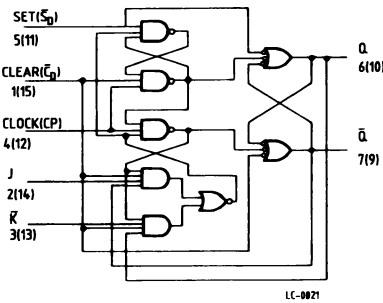


NC = No Internal Connection

LOGIC SYMBOL



LOGIC DIAGRAM AND TRUTH TABLE



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

Operating Mode	Input				Output	
	$\overline{S}_D$	$\overline{C}_D$	J	$\overline{K}$	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (clear)	H	L	X	X	L	H
* Undetermined	L	L	X	X	H	H
Load "1" (set)	H	H	h	h	H	L
Hold	H	H	l	h	q	$\overline{q}$
Toggle	H	H	h	l	$\overline{q}$	q
Load "0" (reset)	H	H	l	l	L	H

* Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously
The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable, that is, it will not persist when either Preset or Clear returns to its inactive (high) level

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Don't Care
l, h, (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS109AXX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Condition (note 1)		Unit
			Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage		2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage				0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage			- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage		2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage			0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IL} or V_{IH} per Truth Table	V
				0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current	J, K, Clock Set, Clear			20 40	V_{CC} = MAX, V_{IN} = 2.7 V		µA
		J, K, Clock Set, Clear			0.1 0.2	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current	J, K, Clock Set, Clear			- 0.4 - 0.8	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)		- 20		- 100	V_{CC} = MAX		mA
I_{CC}	Power Supply Current				8.0	V_{CC} = MAX		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

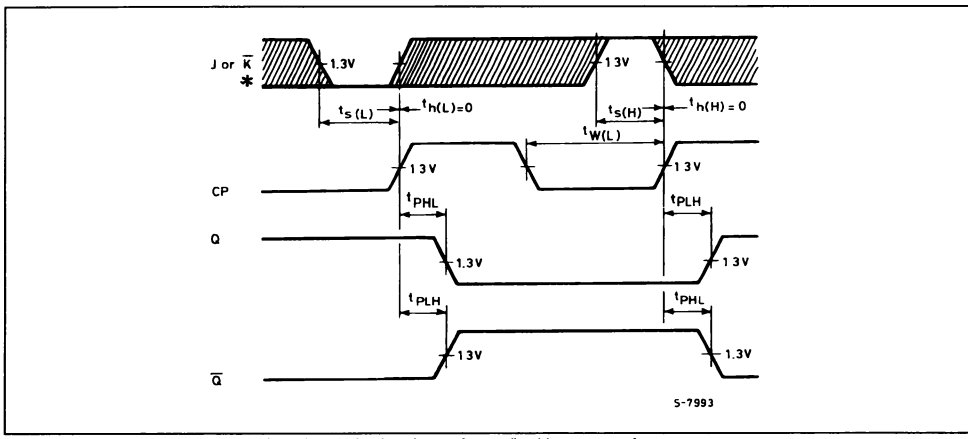
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
f_{MAX}	Maximum Clock Frequency	25	33		V_{CC} = 5.0 V C_L = 15 pF	MHz
t_{PLH} t_{PHL}	Clock, Clear Set to Output		13 25	25 40		ns

AC SET-UP REQUIREMENTS : T_A = 25 °C

Symbol	Parameter		Limits			Test Conditions	Unit
			Min.	Typ.	Max.		
t_W	Clock, Clear, Set Pulse Width		25			V_{CC} = 5.0 V	ns
t_s	Data Set-up Time	HIGH	35				ns
		LOW	25				ns
t_h	Hold Time		5.0				ns

AC WAVEFORMS

Figure 1 :Clock to Output Delays, Data Set-up and Hold Times, Clock Pulse Width.



* The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 2 :Set and Clear to Output Delays, Set and Clear Pulse Widths.

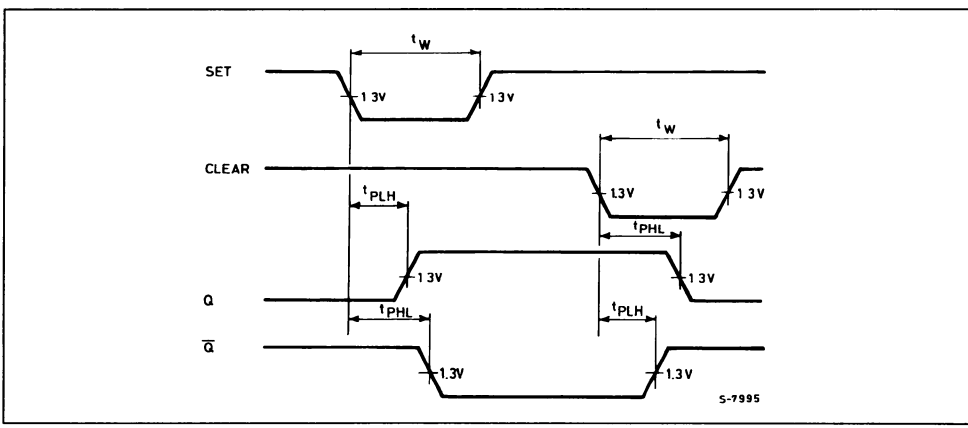
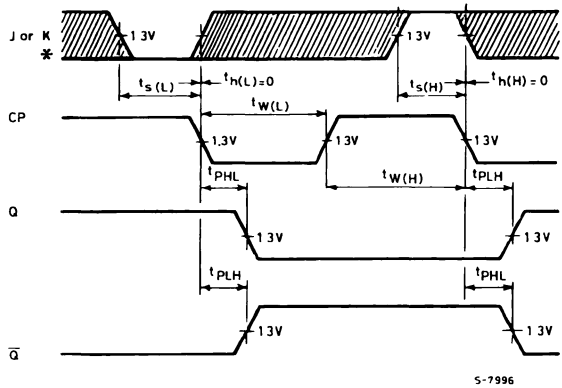


Figure 3 :Clock to Output Delays, Data Set-up and Hold Times, Clock Pulse Width.

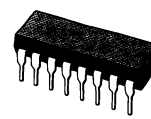


* The shaded areas indicate when the input is permitted to change for predictable output performance.

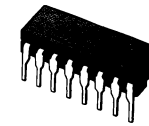
DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION

The T74LS112A is a dual JK flip-flop featuring individual J, K, clock, and asynchronous set and clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up and hold time are observed. Input data is transferred to the outputs on the negative-going clock pulse edge.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

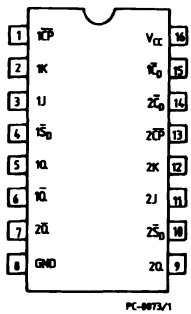
C1
(Plastic Chip Carrier)

ORDER CODES :

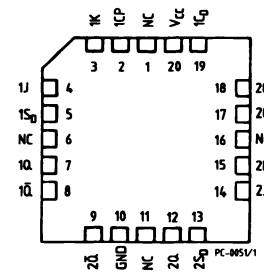
T74LS112A D1 T74LS112A C1
T74LS112A B1 T74LS112A M1

PIN CONNECTION (top view)

DUAL IN LINE

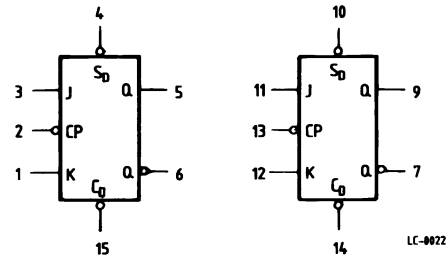


CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL

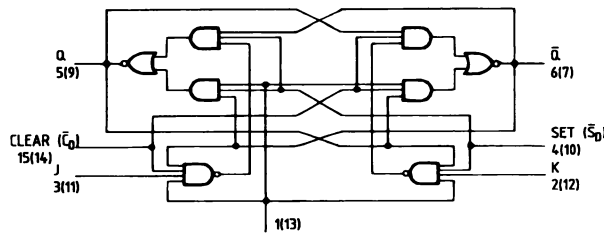


LOGIC DIAGRAM AND TRUTH TABLE

Operating Mode	Inputs				Outputs	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (clear)	H	L	X	X	L	H
* Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (reset)	H	H	l	h	L	H
Load "1" (set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\overline{q}$

* Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.
The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable ; that is, it will not persist when either Preset or Clear returns to its inactive (high) level

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h, (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS112AXX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Condition (note 1)		Unit
			Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage		2.0			Guaranteed Input HIGH Voltage for all Inputs		V
V_{IL}	Input LOW Voltage				0.8	Guaranteed Input LOW Voltage for all Inputs		V
V_{CD}	Input Clamp Diode Voltage			- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage		2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage			0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IL} or V_{IH} per Truth Table	V
				0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current	J, K Set, Clear Clock			20 60 80	V_{CC} = MAX, V_{IN} = 2.7 V		µA
		J, K Set, Clear Clock			0.1 0.3 0.4	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current	J, K Set, Clear Clock			- 0.4 - 0.8 - 0.8	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)		- 20		- 100	V_{CC} = MAX		mA
I_{CC}	Power Supply Current				8.0	V_{CC} = MAX		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

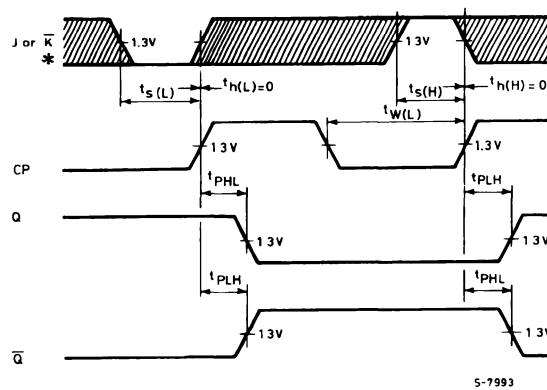
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
f_{MAX}	Maximum Clock Frequency	30	45		V_{CC} = 5.0 V C_L = 15 pF	MHz
t_{PLH} t_{PHL}	Clock, Clear Set to Output		15 15	20 20		ns

AC SET-UP REQUIREMENTS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_W	Clock, Set Pulse Width	20			V_{CC} = 5.0 V	ns
t_W	Clear, Set Pulse Width	25				ns
t_s	Set-up Time	20				ns
t_h	Hold Time	0				ns

AC WAVEFORMS

Figure 1 :Clock to Output Delays, Data Set-up and Hold Times, Clock Pulse Width.



* The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 2 :Set and Clear to Output Delays, Set and Clear Pulse Widths.

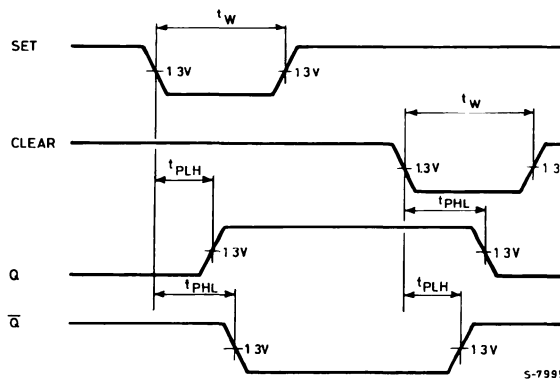
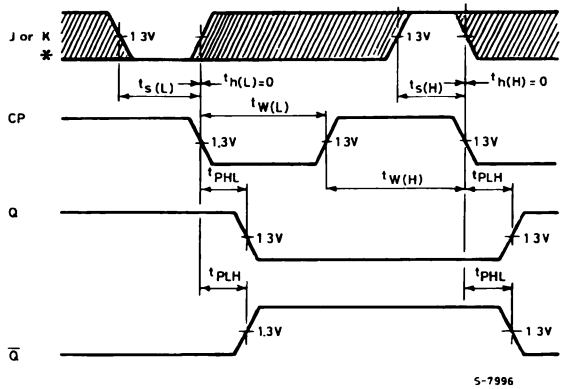


Figure 3 : Clock to Output Delays, Data Set-up and Hold Times, Clock Pulse Width.

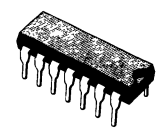


* The shaded areas indicate when the input is permitted to change for predictable output performance.

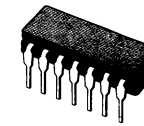
DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION

The T74LS113A offers individual J, K, set and clock inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

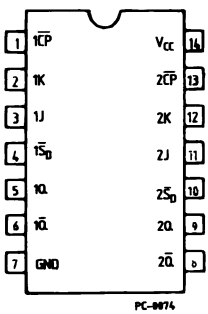
C1
(Plastic Chip Carrier)

ORDER CODES :

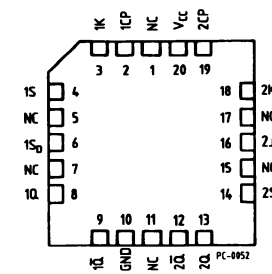
T74LS113A D1	T74LS113A C1
T74LS113A B1	T74LS113A M1

PIN CONNECTION (top view)

DUAL IN LINE

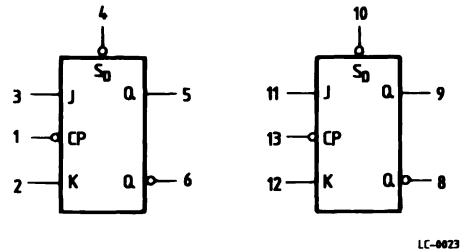


CHIP CARRIER



NC = No Internal Connection

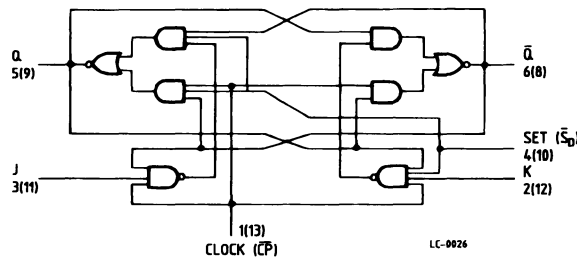
LOGIC SYMBOL



LOGIC DIAGRAM AND TRUTH TABLE

Operating Mode	Inputs			Outputs	
	$\overline{S}_D$	J	K	Q	$\overline{Q}$
Set	L	X	X	H	L
Toggle	H	h	h	$\overline{q}$	q
Load "0" (reset)	H	l	h	L	H
Load "1" (set)	H	h	l	H	L
Hold	H	l	l	q	$\overline{q}$

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h, (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.



V_{CC} = Pin 14
GND = Pin 7
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS113AXX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Condition (note 1)		Unit
			Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage		2.0			Guaranteed Input HIGH Voltage for all Inputs		V
V_{IL}	Input LOW Voltage				0.8	Guaranteed Input LOW Voltage for all Inputs		V
V_{CD}	Input Clamp Diode Voltage			- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage		2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage			0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IL} or V_{IH} per Truth Table	V
				0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current	J, K Set Clock			20 60 80	V_{CC} = MAX, V_{IN} = 2.7 V		µA
		J, K Set Clock			0.1 0.3 0.4	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current	J, K Set.Clock			- 0.4 - 0.8	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)		- 20		- 100	V_{CC} = MAX		mA
I_{CC}	Power Supply Current				8.0	V_{CC} = MAX		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

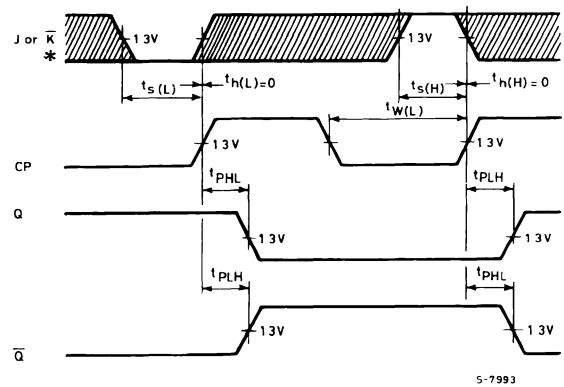
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
f_{MAX}	Maximum Clock Frequency	30	45		V_{CC} = 5.0 V C_L = 15 pF	MHz
t_{PLH} t_{PHL}	Propagation Delay, Clock Set to Output		15 15	20 20		ns

AC SET-UP REQUIREMENTS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_W	Clock Pulse Width	20			V_{CC} = 5.0 V	ns
t_W	Set Pulse Width	25				ns
t_s	Set-up Time	20				ns
t_h	Hold Time	0				ns

AC WAVEFORMS

Figure 1 : Clock to Output Delays, Data Set-up and Hold Times, Clock Pulse Width.



* The shaded areas indicate when the input is permitted is change to predictable output performance.

Figure 2 : Set and Clear to Output Delays, Set and Clear Pulse Widths.

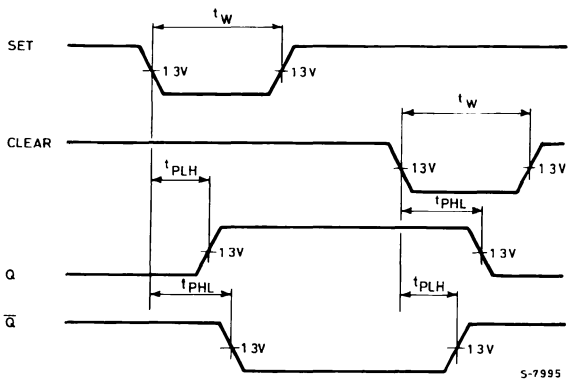
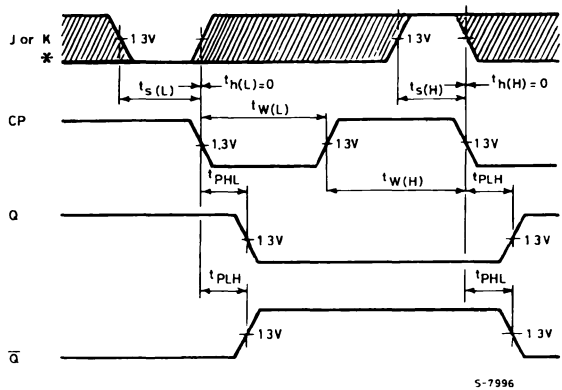


Figure 3 : Clock to Output Delays, Data Set-up and Hold Times, Clock Pulse Width.



* The shaded areas indicate when the input is permitted is change to predictable output performance.

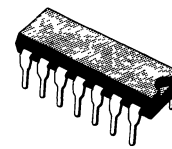
SGS-THOMSON MICROELECTRONICS

T74LS114A

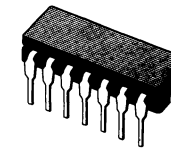
DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION

The T74LS114A offer common clock and common clear inputs and individual J, K, and set inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

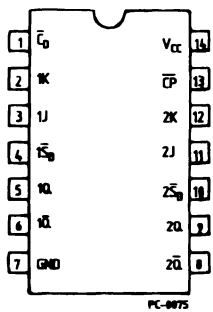
C1
(Plastic Chip Carrier)

ORDER CODES :

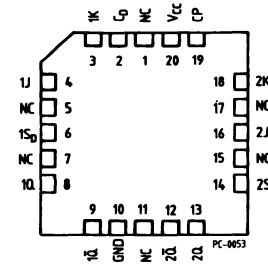
T74LS114A D1	T74LS114A C1
T74LS114A B1	T74LS114A M1

PIN CONNECTION (top view)

DUAL IN LINE

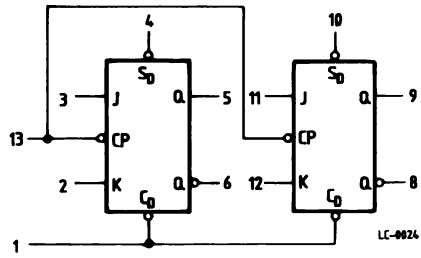


CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL

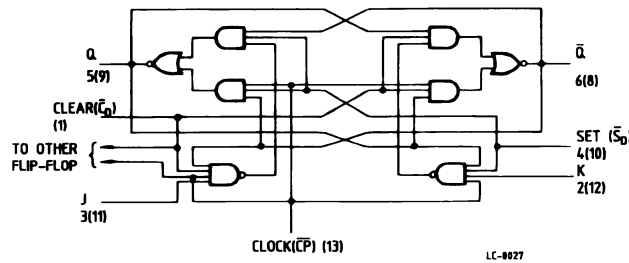


LOGIC DIAGRAM AND TRUTH TABLE

Operating Mode	Inputs				Outputs	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (clear)	H	L	X	X	L	H
* Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (reset)	H	H	l	h	L	H
Load "1" (set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\overline{q}$

* Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.
The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable ; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h, (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.



V_{CC} = Pin 14
GND = Pin 7
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS114AXX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Condition (note 1)		Unit
			Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage		2.0			Guaranteed Input HIGH Voltage for all Inputs		V
V_{IL}	Input LOW Voltage				0.8	Guaranteed Input LOW Voltage for all Inputs		V
V_{CD}	Input Clamp Diode Voltage			- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage		2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage			0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IL} or V_{IH} per Truth Table	V
				0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current	J, K Set Clear Clock			20 60 120 160	V_{CC} = MAX, V_{IN} = 2.7 V		µA
		J, K Set Clear Clock			0.1 0.3 0.6 0.8	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current	J, K Set Clear,Clock			- 0.4 - 0.8 - 1.6	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)		- 20		- 100	V_{CC} = MAX		mA
I_{CC}	Power Supply Current				6.0	V_{CC} = MAX		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2 Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

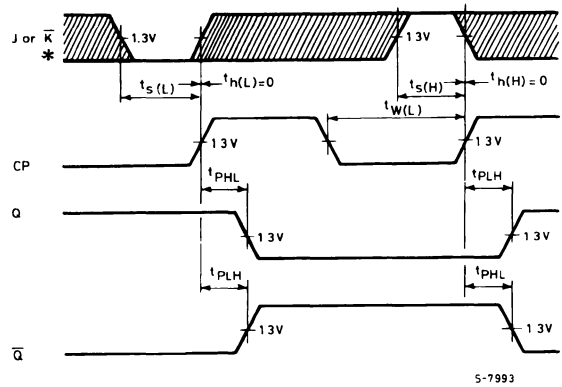
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
f_{MAX}	Maximum Clock Frequency	30	45		V_{CC} = 5.0 V C_L = 15 pF	MHz
t_{PLH} t_{PHL}	Propagation Delay, Clock Clear Set to Output		15 15	20 20		ns

AC SET-UP REQUIREMENTS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_W	Clock Pulse Width	20			V_{CC} = 5.0 V	ns
t_W	Clear, Set Pulse Width	25				ns
t_s	Set-up Time	20				ns
t_h	Hold Time	0				ns

AC WAVEFORMS

Figure 1 : Clock to Output Delays, Data Set-up and Hold Times, Clock Pulse Width.



* The shaded areas indicate when the input is permitted to change for predictable output performance

Figure 2 : Set and Clear to Output Delays, Set and Clear Pulse Widths.

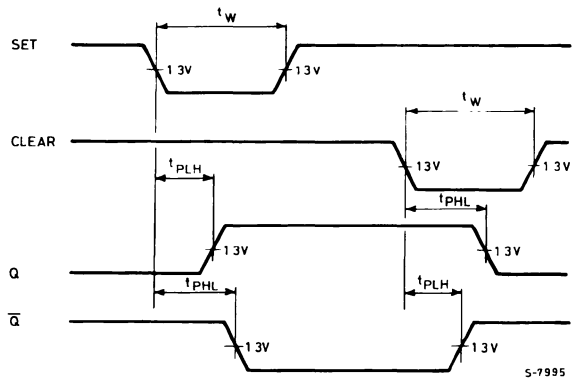
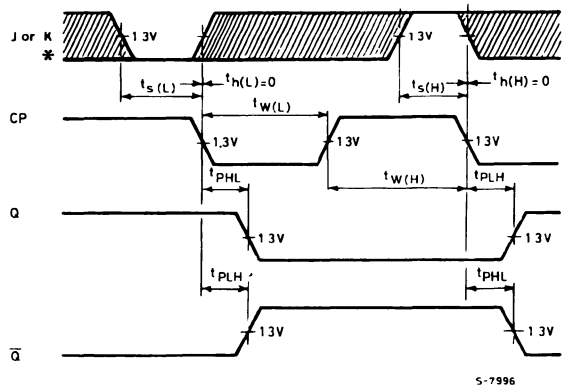


Figure 3 : Clock to Output Delays, Data Set-up and Hold Times, Clock Pulse Width.



* The shaded areas indicate when the input is permitted to change for predictable output performance.

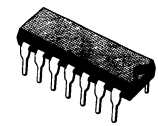
SGS-THOMSON
MICROELECTRONICS

T74LS125A
T74LS126A

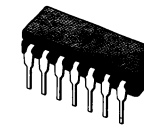
LS125A-QUAD 3-STATE BUFFER (LOW ENABLE)
LS126A-QUAD 3-STATE BUFFER (HIGH ENABLE)

DESCRIPTION

The T74LS125A/126A are high speed QUAD 3-STATE BUFFERS WITH ACTIVE HIGH ENABLES fabricated in LOW POWER SCHOTTKY technology.



B1
(Plastic Package)



D1
(Ceramic Package)

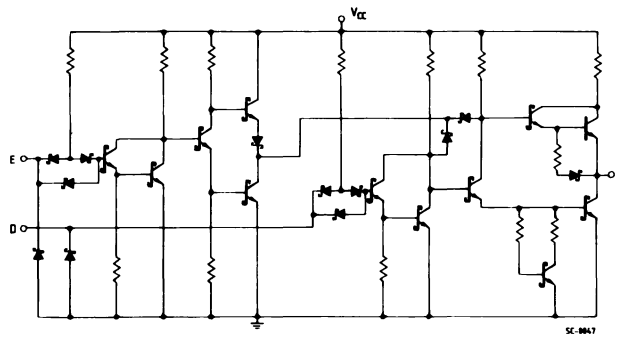
M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

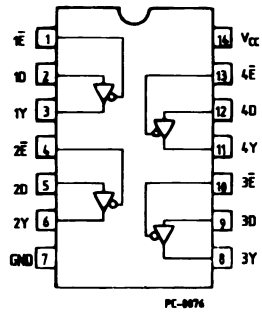
T74LSXXXX D1	T74LSXXXX C1
T74LSXXXX B1	T74LSXXXX M1

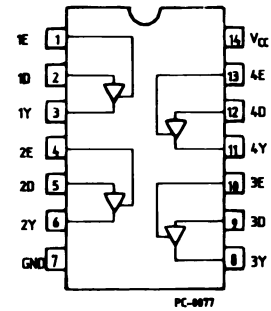
SCHEMATIC



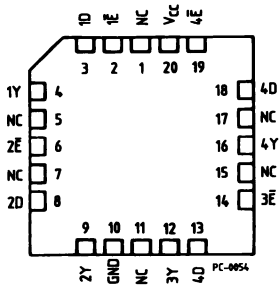
PIN CONNECTION (top view)

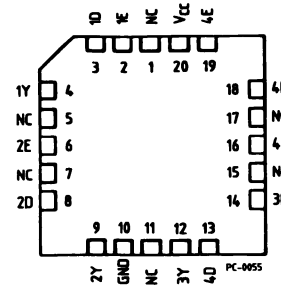
DUAL IN LINE





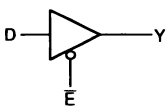
CHIP CARRIER





NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE



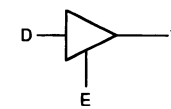
LS125A

Inputs		Output
$\overline{E}$	D	
L	L	L
L	H	H
H	X	Z

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
Z = High Impedance (off)

LS126A

Inputs		Output
$\overline{E}$	D	
H	L	L
H	H	H
L	X	Z



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I 125A 126A	Input Voltage, Applied to Input	0.5 to 10 – 0.5 to 15	V
V_O 125A 126A	Output Voltage, Applied to Output	0 to 15 0 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS125A/126A XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

AC CHARACTERISTICS: T_A = 25°C

Symbol	Parameter	Limits						Test Conditions		Unit
		LS125A			LS126A					
		Min.	Typ.	Max.	Min.	Typ.	Max.			
T_{PLH} T_{PHL}	Propagation Delay Data to Output		9 7	15 18		9 7	15 18	Figs 1, 2	V_{CC} = 5.0 V C_L = 45 pF R_L =667 Ω	ns
T_{PZH}	Output Enable Time to HIGH Level		12	20		16	25	Figs. 4, 5		ns
T_{PZL}	Output Enable Time to LOW Level		15	25		21	35	Figs. 3, 5		ns
T_{PLZ}	Output Enable Time from LOW Level			20			25	Figs. 3, 5	V_{CC} = 5.0 V C_L = 5 pF R_L =667 Ω	ns
T_{PHZ}	Output Disable Time from HIGH Level			20			25	Figs. 4, 5		ns

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Condition (note 1)		Unit
			Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage		2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage				0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage			- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage		2.4	3.1		V_{CC} = MIN, I_{OH} = - 2.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage			0.25	0.4	I_{OL} = 12 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
				0.35	0.5	I_{OL} = 24 mA		V
I_{OZH}	Output Off Current-HIGH	125A			20	V_{CC} = MAX, V_{OUT} = 2.7 V, V_E = V_{IH}		µA
I_{OZL}	Output Off Current-LOW	125A			- 20	V_{CC} = MAX, V_{OUT} = 0.4 V, V_E = V_{IH}		µA
I_{OZH}	Output Off Current-HIGH	126A			20	V_{CC} = MAX, V_{OUT} = 2.7 V, V_E = V_{IL}		µA
I_{OZL}	Output Off Current-LOW	126A			- 20	V_{CC} = MAX, V_{OUT} = 0.4 V, V_E = V_{IL}		µA
I_{IH}	Input HIGH Current				20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current				- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)		- 40		- 225	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current Outputs LOW	125A			16	$\overline{V_E}$ = 0 V V_E = 4.5 V	V_{CC} = MAX, V_{IN} = 0 V	mA
		126A			20			
	Power Supply Current Outputs HIGH	125A			20	$\overline{V_E}$ = 4.5 V V_E = 0 V		mA
		126A			24			

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges
2. Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C

AC WAVEFORMS

Figure 1.

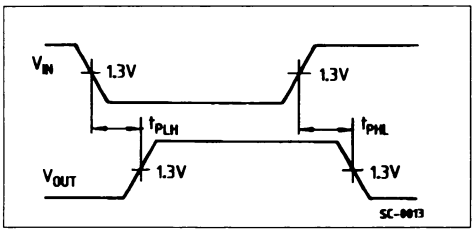


Figure 2.

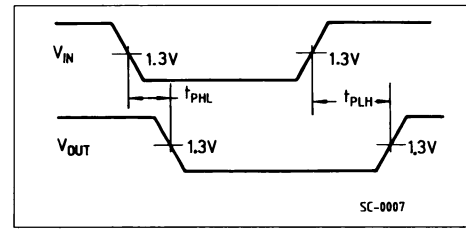


Figure 3.

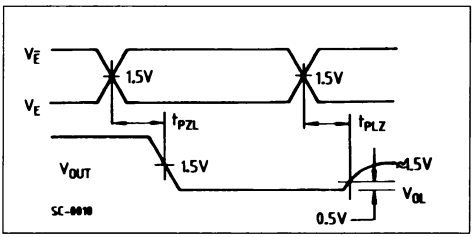
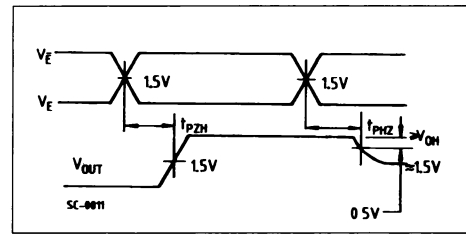
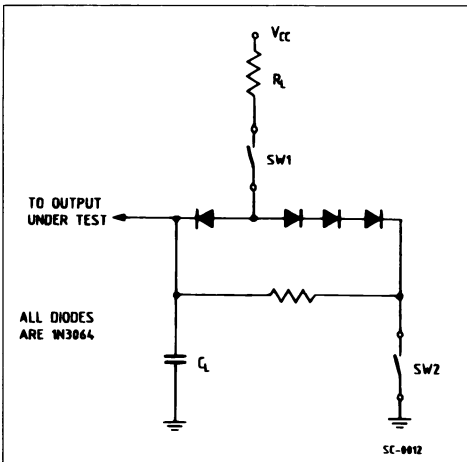


Figure 4.



AC LOAD CIRCUIT

Figure 5.



SWITCH POSITION

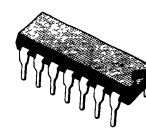
Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

QUAD 2-INPUT SCHMITT TRIGGER NAND GATE

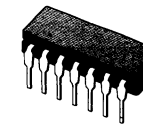
DESCRIPTION

The T74LS132 contains four 2-input NAND Gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater noise margin than conventional NAND Gates.

Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter that drive a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as one input remains at a more positive voltage than V_{T+} (MAX), the gare will respond to the transition of the other input as shown in figure 1.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

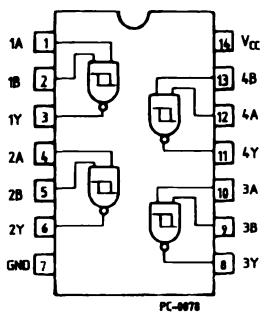
C1
(Plastic Chip Carrier)

ORDER CODES :

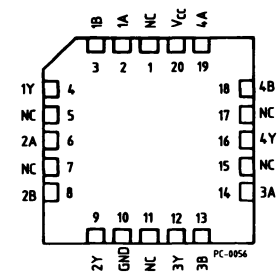
T74LS132 D1	T74LS132 C1
T74LS132 B1	T74LS132 M1

PIN CONNECTION (top view)

DUAL IN LINE

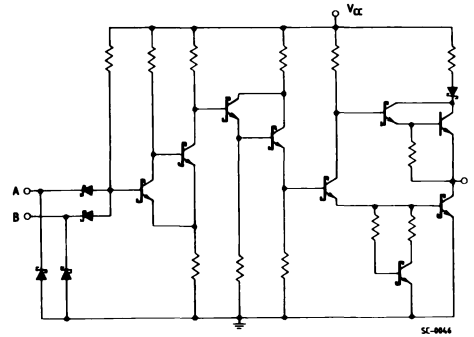


CHIP CARRIER



NC = No Internal Connection

SCHEMATIC DIAGRAM



LOGIC DIAGRAM AND TRUTH TABLE

IN		OUT
A	B	Y
L	X	H
X	L	H
H	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.6 to 5.5	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS132XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)	Unit
		Min.	Typ. (*)	Max.		
V_{T+}	Positive-going Threshold Voltage	1.4	1.6	1.9	V_{CC} = 5.0 V	V
V_{T-}	Negative-going Threshold Voltage	0.5	0.8	1.0	V_{CC} = 5.0 V	V
$V_{T+} - V_{T-}$	Hysteresis	0.4	0.8		V_{CC} = 5.0 V	V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA	V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = 0.5 V	V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA; V_{CC} = MIN	V
			0.35	0.5	I_{OL} = 8.0 mA; V_{IN} = 1.9 V	V
I_{T+}	Input Current at Positive-going Threshold		- 0.14		V_{CC} = 5.0 V, V_{IN} = V_{T+}	mA
I_{T-}	Input Current at Negative-going Threshold		- 0.18		V_{CC} = 5.0 V, V_{IN} = V_{T-}	mA
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V	µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V	mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V	mA
I_{CCH}	Supply Current HIGH		6.0	11	V_{CC} = MAX, V_{IN} = 0 V	mA
I_{CCL}	Supply Current LOW		8.0	14	V_{CC} = MAX, V_{IN} = 4.5 V	mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		15	22	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PHL}	Turn On Dealy, Input to Output		15	22		ns

Figure 1.

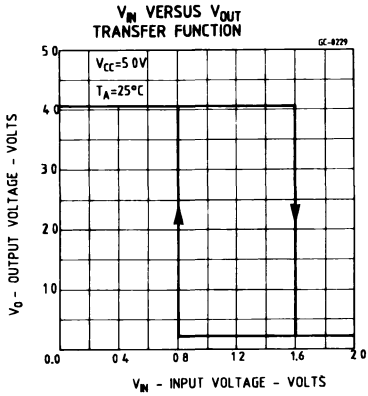


Figure 2.

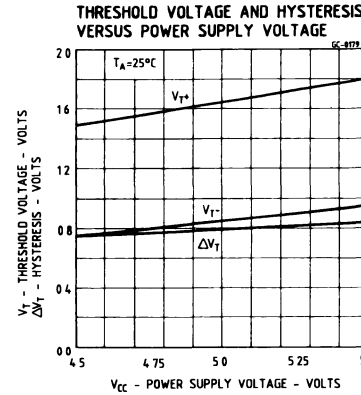


Figure 3.

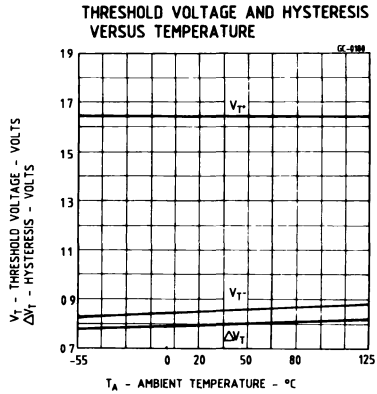
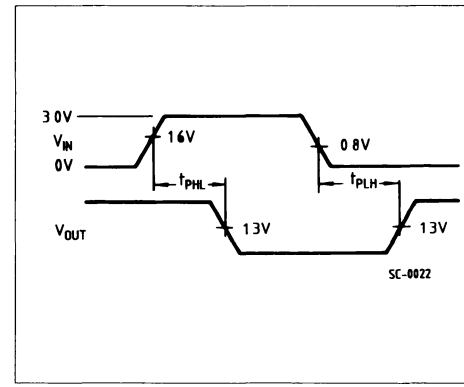


Figure 4.



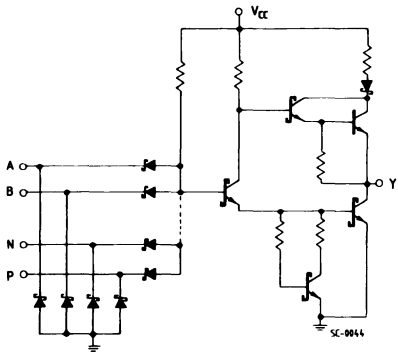
T74LS133

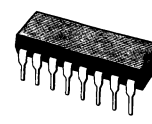
13-INPUT NAND GATE

DESCRIPTION

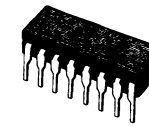
The T74LS133 is a high speed 13-INPUT NAND GATE fabricated in silicon LOW POWER SCHOTTKY technology.

SCHEMATIC





B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

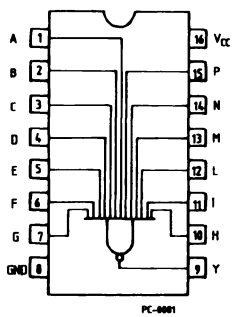
C1
(Plastic Chip Carrier)

ORDER CODES :

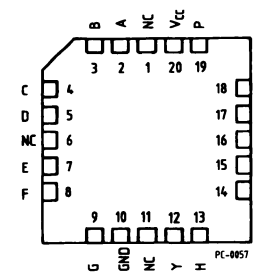
T74LS133 D1	T74LS133 C1
T74LS133 B1	T74LS133 M1

PIN CONNECTION (top view)

DUAL IN LINE

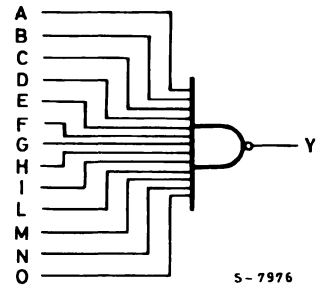


CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	60	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS133XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IL}		µA
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = 2.0 V	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CCH}	Supply Current HIGH		0.35	0.5	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CCL}	Supply Current LOW		0.6	1.1	V_{CC} = MAX, Inputs Open		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C.

AC CHARACTERISTICS: T_A = 25°C (for AC test circuits and waveforms see databook introduction)

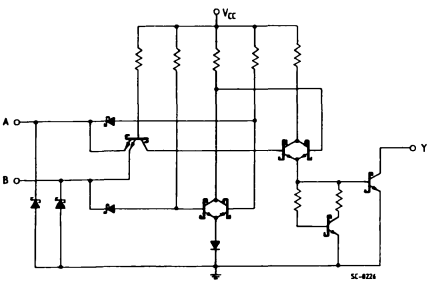
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		10	15	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PHL}	Turn On Delay, Input to Output		25	38		ns

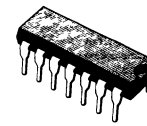
QUAD 2-INPUT EXCLUSIVE OR GATE

DESCRIPTION

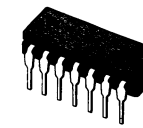
The T74LS136 is a high speed QUAD 2-INPUT EXCLUSIVE OR GATE (with open collector output) fabricated in LOW POWER SCHOTTKY technology.

SCHEMATIC DIAGRAM





B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

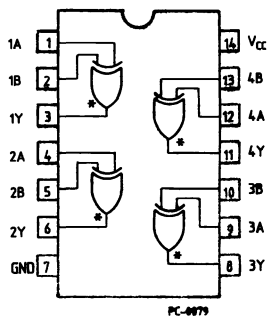
C1
(Plastic Chip Carrier)

ORDER CODES

T74LS136 D1	T74LS136 C1
T74LS136 B1	T74LS136 M1

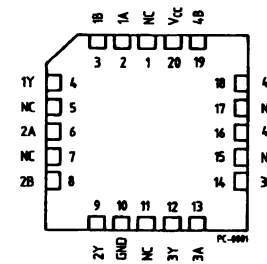
PIN CONNECTION (top view)

DUAL IN LINE



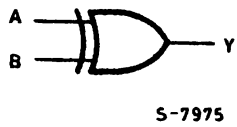
* Open Collector Outputs

CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE



A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

L = LOW Voltage level
H = HIGH Voltage level

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS136XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
I_{OH}	Output HIGH Voltage			100	V_{CC} = MIN, V_{OH} = - 5.5 V V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current			40 0 2	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 5.5 V		µA mA
I_{IL}	Input LOW Current			- 0.6	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{CC}	Supply Current LOW		6.0	10	V_{CC} = MAX		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C

AC CHARACTERISTICS: $T_A = 25^oC$ (for AC test circuits and waveforms see databook introduction)

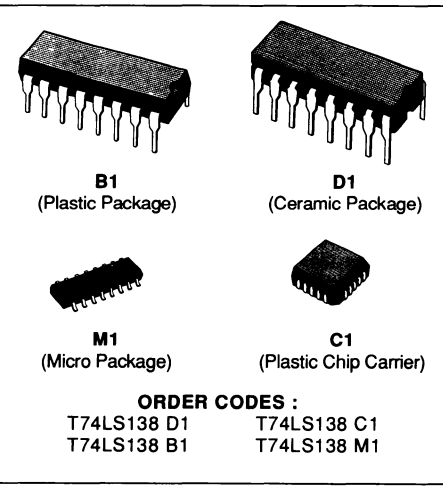
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Other Input LOW		18 18	30 30	VCC = 5.0 V C_L = 15 pF, R_L = 2.0 KΩ	ns
t_{PLH} t_{PHL}	Propagation Delay Other Input HIGH		18 18	30 30		ns

1-OF-8 DECODER/DEMULTIPLEXER

- DEMULTIPLEXING CAPABILITY
- MULTIPLE INPUT ENABLE FOR EASY EXPANSION
- TYPICAL POWER DISSIPATION OF 32 mW
- ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

DESCRIPTION

The T74LS138 is a high speed 1-of-8 Decoder/Demultiplexer. This device is ideally suited for high speed bipolar memory chip select address decoding. The multiple input enables allowparallel expansion to a 1-of-24 decoder using just three LS138 devices or to a 1-of-32 decoder using four LS138 and one inverter. The LS138 is fabricated with the Schottky barrier diode process for high speed and is compatible with all TTL families.



B1 (Plastic Package)

D1 (Ceramic Package)

M1 (Micro Package)

C1 (Plastic Chip Carrier)

ORDER CODES :

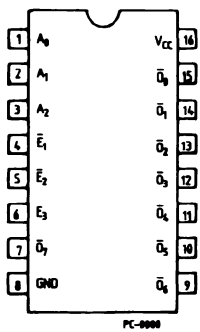
T74LS138 D1 T74LS138 C1
T74LS138 B1 T74LS138 M1

PIN NAMES

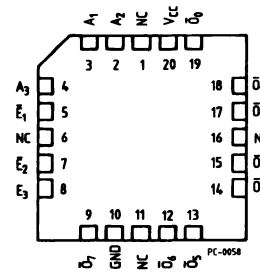
$\underline{A}_0 - \underline{A}_3$	ADDRESS INPUTS
$E_1 - E_2$	ENABLE (active LOW) INPUTS
$\underline{E}_3$	ENABLE (active HIGH) INPUT
$\overline{O}_0 - \overline{O}_7$	ACTIVE LOW OUTPUTS

PIN CONNECTION (top view)

DUAL IN LINE

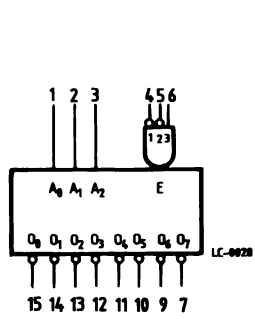


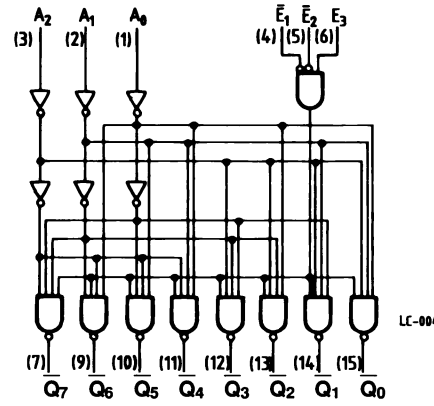
CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM





V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 5.5	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS138XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

FUNCTIONAL DESCRIPTION

The LS138 is a high speed 1-of-8 Decoder/Demultiplexer fabricated with the low power Schottky barrier diode process. The decoder accepts three binary weigthed inputs (A_0, A_1, A_2) and when enable provides eight mutually exclusive active LOW outputs (O_0-O_7). The LS138 features three Enable inputs two active LOW (E_1, E_2) and one active HIGH (E_3). All outputs will be HIGH uneless E_1 and E_2 are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device of a 1-of-32 (5 lines to 32) decoded with just four LS138s and one inverter. (see figure 1).

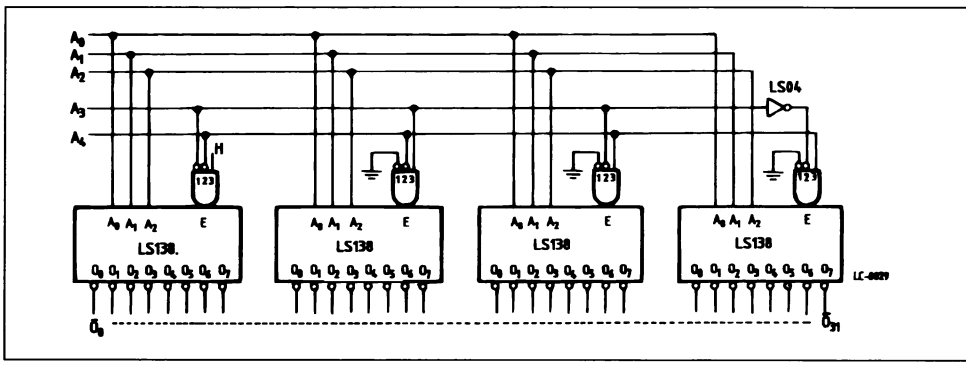
The LS138 can be used as an 8-output demultiplexer by using one of the active LOW Enable Inputs as the data input and the other Enable Inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

TRUTH TABLE

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	$\overline{E}_3$	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Figure 1.



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)	Unit
		Min.	Typ. (*)	Max.		
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Treshold Voltage for All Inputs	V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Treshold Voltage for All Inputs	V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA	V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table	V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V	µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V	mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V	mA
I_{CC}	Power Supply Current		6.0	10	V_{CC} = MAX	mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges
2. Not more than one output should be shorted at a time.
3. Typical values are at V_{CC} = 5 0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Level of Delay	Limits			Test Conditions	Unit
			Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay, Address to Output	2 2		13 27	20 41	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PLH} t_{PHL}	Propagation Delay, Address to Output	3 3		18 26	27 39		ns
t_{PLH} t_{PHL}	Propagation Delay, E to any Output	2 2		12 21	18 32		ns
t_{PLH} t_{PHL}	Propagation Delay, E to any Output	3 3		17 25	26 38		ns

AC WAVEFORMS

Figure 2.

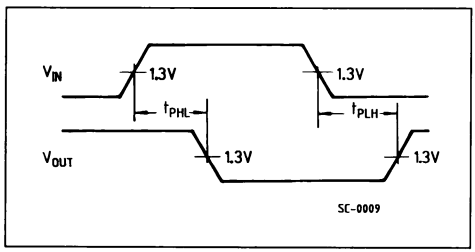
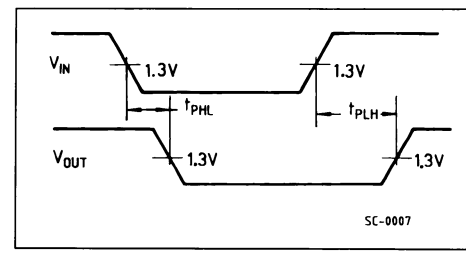


Figure 3.

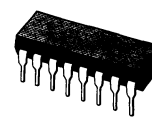


DUAL 1-OF-4 DECODER

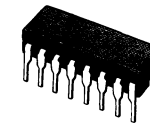
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- TWO COMPLETELY INDEPENDENT 1-OF-4 DECODERS
- ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

DESCRIPTION

The T74LS139 is a high speed Dual 1-of-4 Decoder/Demultiplexer. This device has two independent decoders, each accepting two inputs and providing four mutually exclusive active LOW outputs. Each decoder has an active LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the LS139 can be used as a function generator providing all four minterms of two variables. The LS139 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all TTL families.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

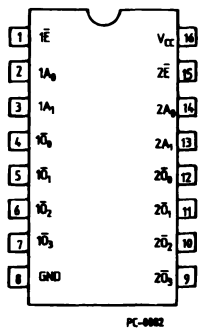
T74LS139 D1 T74LS139 C1
T74LS139 B1 T74LS139 M1

PIN NAMES

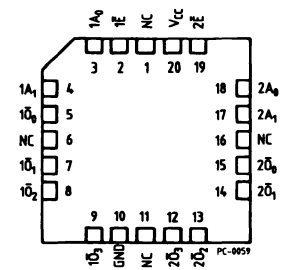
$\underline{A_0} - A_1$	ADDRESS INPUTS
$\underline{\overline{E}}$	ENABLE (active LOW) INPUT
$\overline{O_0} - \overline{O_3}$	ACTIVE LOW OUTPUTS

PIN CONNECTION (top view)

DUAL IN LINE

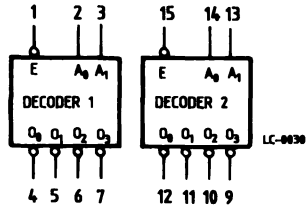


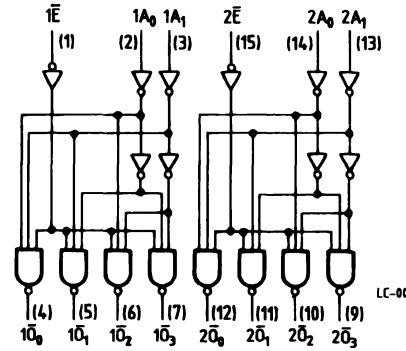
CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM





V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.6 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS139XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

FUNCTIONAL DESCRIPTION

The LS139 is a high speed dual 1-of-4 Decoder/Demultiplexer fabricated with the Schottky barrier diode process. The device has two independent decoders, each of which accept two binary weighted inputs (A_0-A_1) and provide four mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_3$). Each decoder has an active LOW Enable ($\overline{E}$). When $\overline{E}$ is HIGH all output are forced HIGH.

The enable can be used as the data input for a 4-output demultiplexer application.

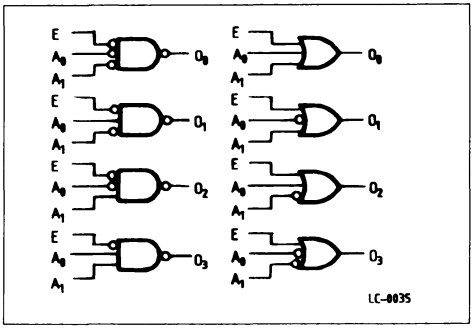
Each half of the LS139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in fig. 1, and thereby reducing the number of packages required in a logic network.

TRUTH TABLE

Inputs			Outputs			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Figure 1.



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN	V
			0.35	0.5	I_{OL} = 8.0 mA	V_{IN} = V_{IH} or V_{IL} per Truth Table	V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.36	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		7.0	11	V_{CC} = MAX		mA

Notes : 1. Conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Level of Delay	Limits			Test Conditions	Unit
			Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay, Address to Output	2 2		13 22	20 33		ns
t_{PLH} t_{PHL}	Propagation Delay, Enable to Output	3 3		18 25	29 38	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PLH} t_{PHL}	Propagation Delay, Enable to Output	2 2		16 21	24 32		ns

AC WAVEFORMS

Figure 2.

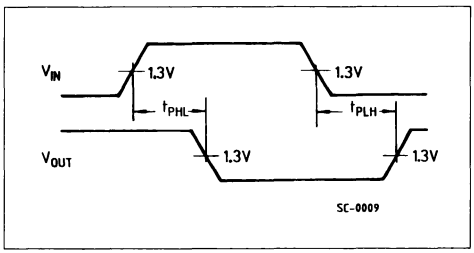
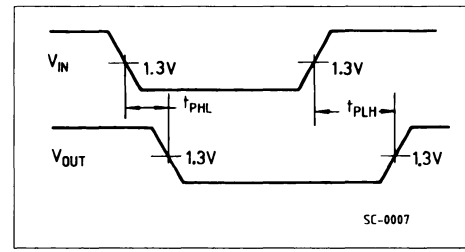


Figure 3.

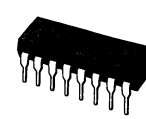


8-LINE TO 3-LINE PRIORITY ENCODERS

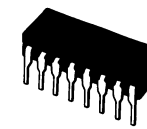
DESCRIPTION

This priority Encoder decodes the inputs to ensure that only the highest order data line is encoded. All inputs and outputs data are active at the low logic level.

The LS148 encloses eigt data lines to three line (4-2-1) binary (octal). Cascading circuitry (Enable Input EI and Enable Output EO) has been provided to allow octal expansion without needing external circuitry.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

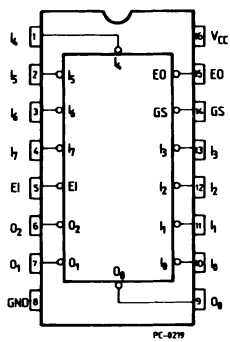
C1
(Plastic Chip Carrier)

ORDER CODES :

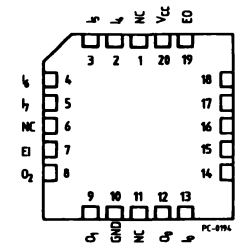
T74LS148 D1 T74LS148 C1
T74LS148 B1 T74LS148 M1

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



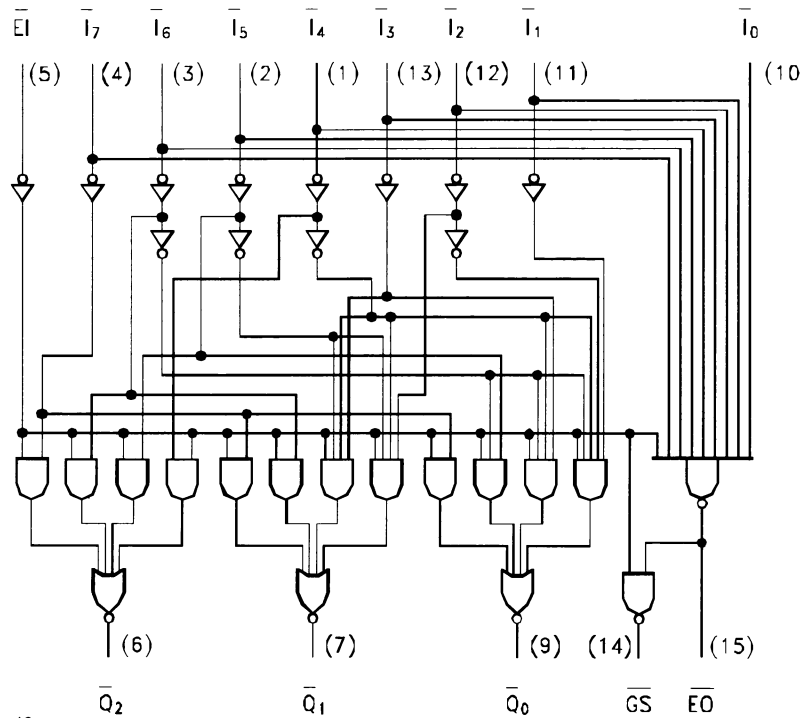
NC = No Internal Connection

TRUTH TABLE

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A_2	A_1	A_0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

L = LOW Voltage Level H = HIGH Voltage Level X = Don't Care

FUNCTIONAL BLOCK DIAGRAM



VCC = Pin 16
GND = Pin 8
( ) = Pin Number

LC10210

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS148XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Input		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Input		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.5		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current All Others Inputs 1-7			 20 40	V_{CC} = MAX, V_{IN} = 2.7 V		µA mA
	All Others Inputs 1-7			0.1 0.2	V_{CC} = MAX, V_{IN} = 7.0 V		
I_{IL}	Input LOW Current All Others Inputs 1-7			 - 0.4 - 0.8	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 120	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CC}	Power Supply Current			20	V_{CC} = MAX, Inputs 7 and EI Grounded, Others Open		mA
				17	V_{CC} = MAX, All Inputs and Outputs Open		mA

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
2. Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: T_A = 25 °C

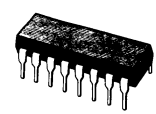
Symbol	From (Input)	To (Output)	Waveforms	Limits			Test Conditions	Units
				Min.	Typ.	Max.		
t_{PLH} t_{PHL}	1 thru 7	A0, A1 or A2	In-Phase Output		14 15	18 25	C_L = 15 pF R_L = 2 KΩ	ns
t_{PLH} t_{PHL}	1 thru 7	A0, A1 or A2	Out-of-Phase Output		20 16	36 29		ns
t_{PLH} t_{PHL}	0 thru 7	EO	Out-of-Phase Output		7.0 25	18 40		ns
t_{PLH} t_{PHL}	0 thru 7	GS	In-Phase Output		35 9.0	55 21		ns
t_{PLH} t_{PHL}	EI	A0, A1 or A2	In-Phase Output		16 12	25 25		ns
t_{PLH} t_{PHL}	EI	GS	In-Phase Output		12 14	17 36		ns
t_{PLH} t_{PHL}	EI	EO	In-Phase Output		12 23	21 35		ns

SGS-THOMSON MICROELECTRONICS

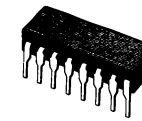
T74LS151

8-INPUT MULTIPLEXER

- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- ON-CHIP SELECT LOGIC DECODING
- FULLY BUFFERED COMPLEMENTARY OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

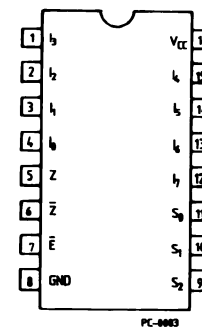
T74LS151 D1
T74LS151 B1
T74LS151 C1
T74LS151 M1

DESCRIPTION

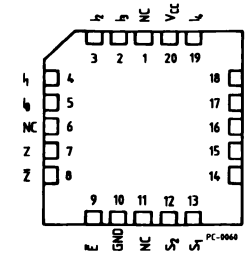
The T74LS151 is a high speed 8-input Digital Multiplexer. It provides in one package, the ability to select one bit of data from up to eight sources. The LS151 can be a universal function generator to generete any logic function of four variables. Both assertion and negation outputs are provided.

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER

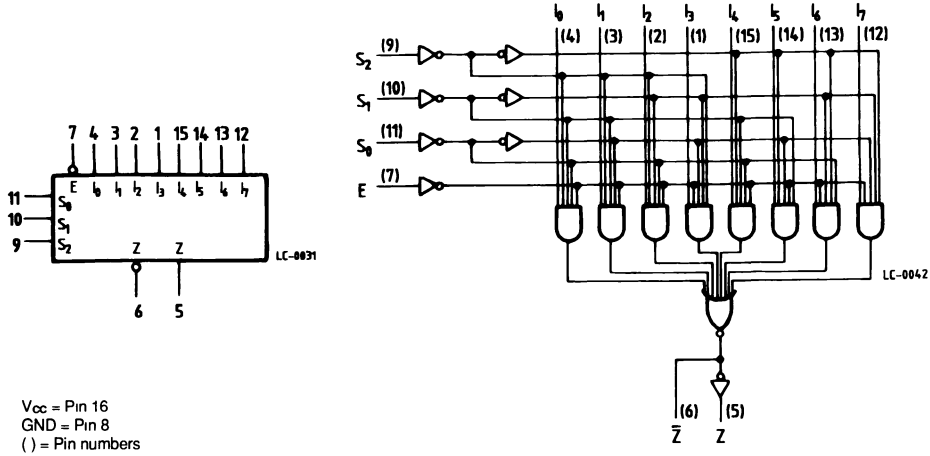


NC = No Internal Connection

PIN NAMES

$\overline{S}_0 - S_2$	SELECT INPUT
$\overline{E}$	ENABLE (active LOW) INPUT
$I_0 - I_7$	MULTIPLEXER INPUTS
$\underline{Z}$	MULTIPLEXER OUTPUT
$\overline{Z}$	COMPLEMENTARY MULTIPLEXER OUTPUT

LOGIC SYMBOL AND LOGIC DIAGRAM



Vcc = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.6 to 5.5	V
I_I	Input Current, into Inputs	– 0.5 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS151XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

FUNCTIONAL DESCRIPTION

The LS151 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs S_0, S_1, S_2. Both assertion and negation outputs are provide.

The Enable input (E) is active LOW. When it is not activated, the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic functions provides at the output is:

$$Z = \overline{E} \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

The LS151 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the LS51 can provide any logic function of four variables and its negation.

TRUTH TABLE

$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Treshold Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Treshold Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN,	V
			0.35	0.5	I_{OL} = 8.0 mA	V_{IN} = V_{IH} or V_{IL} per Truth Table	V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		6.0	10	V_{CC} = MAX		mA

Notes : 1. Conditions for testing, not shown in the table, are chosen to guarantee under "worst case" conditions.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Tests Conditions		Unit
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Select to $\overline{Z}$ Output		14 20	33 32	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PLH} t_{PHL}	Propagation Delay, Select to Z Output		27 18	43 30	Fig. 2		ns
t_{PLH} t_{PHL}	Propagation Delay, Enable to $\overline{Z}$ Output		15 18	24 30	Fig. 2		ns
t_{PLH} t_{PHL}	Propagation Delay, Enable to Z Output		26 20	42 32	Fig. 1		ns
t_{PLH} t_{PHL}	Propagation Delay, Data to $\overline{Z}$ Output		13 12	21 20	Fig. 1		ns
t_{PLH} t_{PHL}	Propagation Delay, Data to Z Output		20 16	32 26	Fig. 2		ns

AC WAVEFORMS

Figure 1.

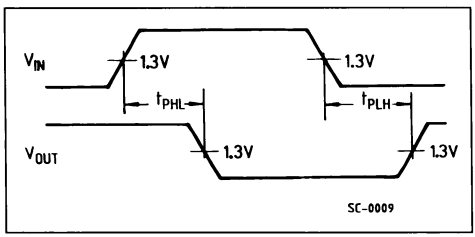
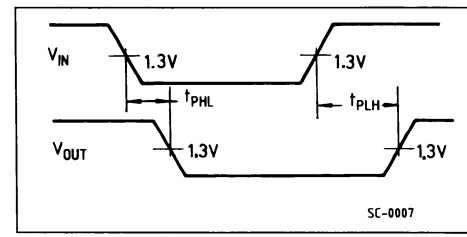


Figure 2.

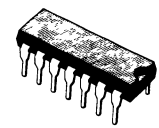


SGS-THOMSON MICROELECTRONICS

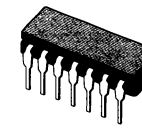
T74LS152

8-INPUT MULTIPLEXER

- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- ON-CHIP SELECT LOGIC DECODING
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

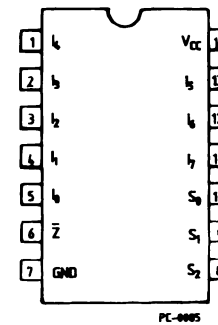
T74LS152 D1 T74LS152 C1
T74LS152 B1 T74LS152 M1

DESCRIPTION

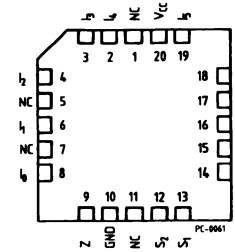
The T74LS152 is a MSI high speed 8-input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as a universal function generator to generate any logic function of four variables.

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



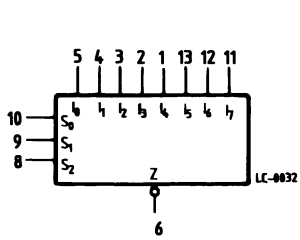
NC = No Internal Connection

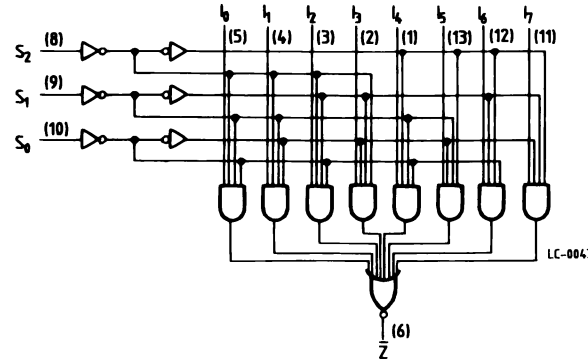
PIN NAMES

$S_0 - S_2$	SELECT INPUT
$\overline{I_0} - \overline{I_7}$	MULTIPLEXER INPUTS
$\overline{Z}$	COMPLEMENTARY MULTIPLEXER

September 1988

LOGIC SYMBOL AND LOGIC DIAGRAM





V_{CC} = Pin 14
GND = Pin 7
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 1.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 5.5	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	60	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS152XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

FUNCTIONAL DESCRIPTION

This device is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. The logic function provided at the output is :

This device provides the ability, in one package, to select from eight sources of data or control information.

$$\overline{Z} = (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

TRUTH TABLE

S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$
L	L	L	L	X	X	X	X	X	X	X	H
L	L	L	H	X	X	X	X	X	X	X	L
L	L	H	X	L	X	X	X	X	X	X	H
L	L	H	X	H	X	X	X	X	X	X	L
L	H	L	X	X	L	X	X	X	X	X	H
L	H	L	X	X	H	X	X	X	X	X	L
L	H	H	X	X	X	L	X	X	X	X	H
L	H	H	X	X	X	H	X	X	X	X	L
H	L	L	X	X	X	X	L	X	X	X	H
H	L	L	X	X	X	X	H	X	X	X	L
H	L	H	X	X	X	X	X	L	X	X	H
H	L	H	X	X	X	X	X	H	X	X	L
H	H	L	X	X	X	X	X	X	L	X	H
H	H	L	X	X	X	X	X	X	H	X	L
H	H	H	X	X	X	X	X	X	X	L	H
H	H	H	X	X	X	X	X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Treshold Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Treshold Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		6.0	9.0	V_{CC} = MAX		mA

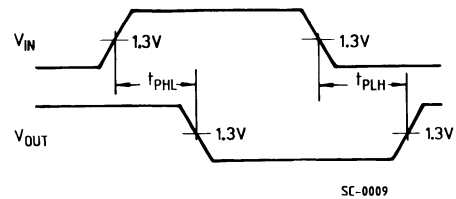
Notes : 1 Conditions for testing, not shown in the table, are chosen to guarantee under "worst case" conditions.
2 Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Tests Conditions		Unit
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Select to $\overline{Z}$ Output		14 20	23 32	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PLH} t_{PHL}	Propagation Delay, Select to $\overline{Z}$ Output		13 12	21 20	Fig. 1		ns

AC WAVEFORMS

Figure 1.

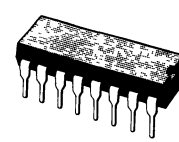


DUAL 4-INPUT MULTIPLEXER

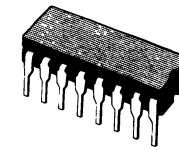
- MULTIFUNCTION CAPABILITY
- NON-INVERTING OUTPUTS
- SEPARATE ENABLE FOR EACH MULTIPLEXER
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

DESCRIPTION

The T74LS153 is a high speed Dual 4-input Multiplexer with common select inputs and individual enable inputs for each section. It can select two bits data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the LS153 can generate any two functions of three variables. The LS153 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all TTL families.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

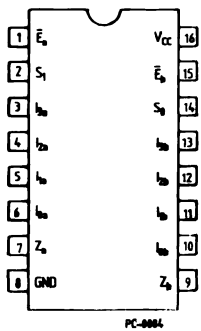
T74LS153 D1 T74LS153 C1
T74LS153 B1 T74LS153 M1

PIN NAMES

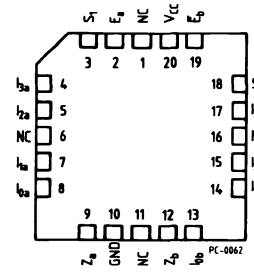
$\overline{S}_0$	COMMON SELECT INPUT
$\overline{E}$	ENABLE (active LOW) INPUT
I_0, I_1	MULTIPLEXER INPUTS
Z	MULTIPLEXER OUTPUT

PIN CONNECTION (top view)

DUAL IN LINE

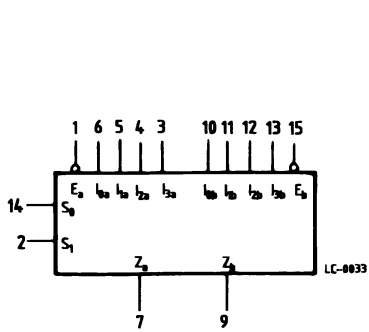


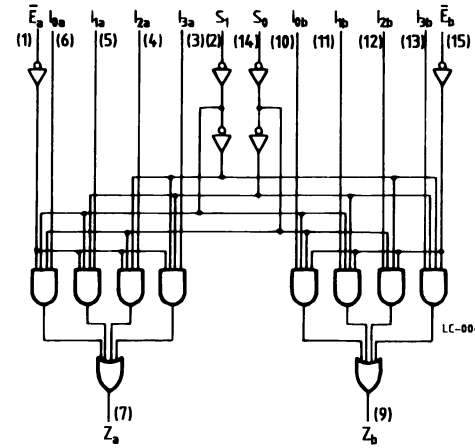
CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM





V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.6 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS153XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

FUNCTIONAL DESCRIPTION

The LS153 is a Dual 4-Input Multiplexer fabricated with Low Power Schottky barrier diode process for high speed. It can select two bits of data from up to four sources under the control of the common Select Inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs (Z_a, Z_b) are forced LOW.

The LS153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select Inputs. The logic equations for the outputs are shown below.

$$Z_a = \overline{E}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$
$$Z_b = \overline{E}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

The LS153 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select Inputs. A less obvious application is a function generator. The LS153 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

Select Inputs		Input (a or b)					Output
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Treshold Voltage for all Input		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Treshold Voltage for all Input		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.36	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		6.0	10	V_{CC} = MAX		mA

Notes : 1. Conditions for testing, not shown in the table, are chosen to guarantee under "worst case" conditions.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Tests Conditions		Unit
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		19 25	25 38	Fig. 2		ns
t_{PLH} t_{PHL}	Propagation Delay, Enable to Output		16 21	24 32	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		10 17	15 26	Fig. 2		ns

AC WAVEFORMS

Figure 1.

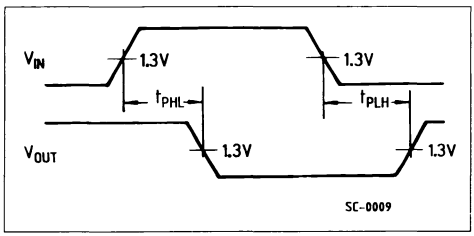
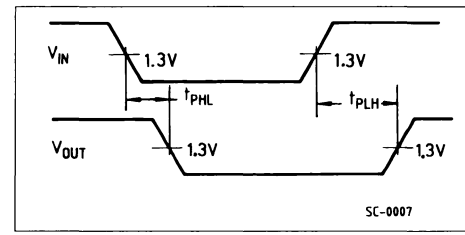


Figure 2.



SGS-THOMSON
MICROELECTRONICS

T74LS155
T74LS156

DUAL 1-OF-4 DECODER/DEMULTIPLEXER

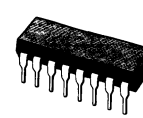
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- COMMON ADDRESS INPUTS
- TRUE OR COMPLEMENT DATA DEMULTIPLEXING
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

DESCRIPTION

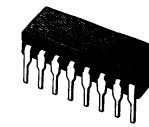
The TTL/MSI T74LS155 and T74LS156 are high speed Dual 1-of-4 Decoder/Demultiplexers. These devices have two decoders with common 2-bit Address inputs and separate gated Enable inputs.

Decoder "a" has an Enable gate with one active HIGH and one active LOW input. Decoder "b" has two active LOW Enable inputs.If the Enable functions are satisfied, one input of each decoder will be LOW as selected by the address inputs. The LS156 has open collector outputs for wired-OR (DOT-AND) decoding and function generator applications.

The LS155 and LS156 are fabricated with the Schottky barrier diode process for high speed and are completely compatible with all TTL families.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

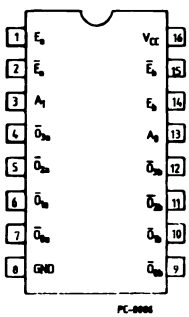
T74LSXXX D1 T74LSXXX C1
T74LSXXX B1 T74LSXXX M1

PIN NAMES

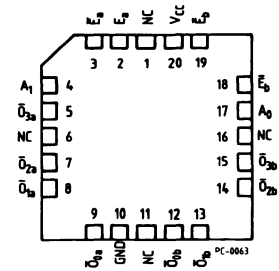
$\underline{A}_0 - \underline{A}_1$	ADDRESS INPUTS
$\underline{E}_a - \underline{E}_b$	ENABLE (active LOW) INPUTS
$\underline{E}_a$	ENABLE (active HIGH) INPUT
$\overline{O}_0 - \overline{O}_3$	ACTIVE LOW OUTPUTS

PIN CONNECTION (top view)

DUAL IN LINE

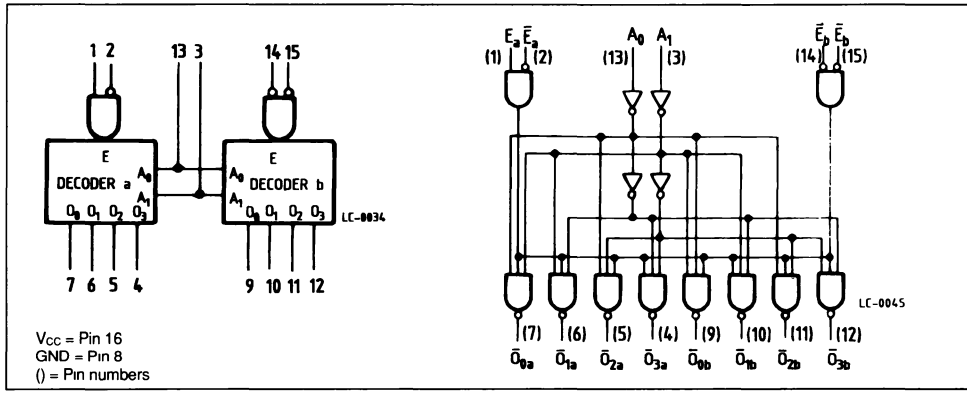


CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
() = Pin numbers

ABSOLUTE MAXIMUM RATING

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		- 0.5 to 7	V
V_I	Input Voltage, Applied to Input	LS155	- 0.5 to 15	V
		LS156	- 1.5 to 5.5	V
V_O	Output Voltage, Applied to Output		- 0.5 to 10	V
I_I	Input Current, into Inputs		- 30 to 5	mA
I_O	Output Current, into Outputs		50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS155/156XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

FUNCTIONAL DESCRIPTION

The LS155 and LS156 are Dual 1-of-4 Decoder/demultiplexer with common Address inputs and separate gated Enable inputs. When enabled, each decoder section accepts the binary weighted Address inputs (A_0-A_1) and provides four mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_3$). If the Enable requirements of each decoder are not met, all ouputs of that decoder are HIGH.

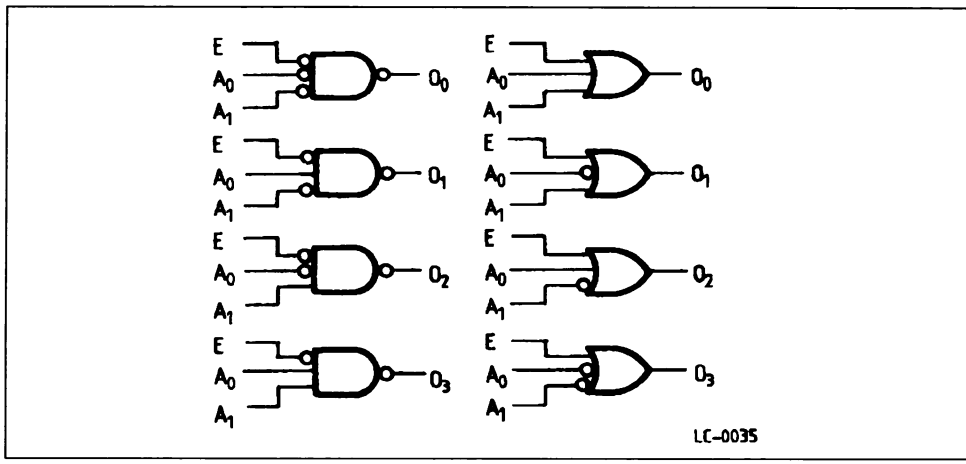
Each decoder section has a 2-input enable gate. The enable gate for Decoder "a" requires one active HIGH input and one active LOW input ($E_a \bullet \overline{E}_a$). In demultiplexing applications, Decoder "a" can accepts either true or complemented data by using the $\overline{E}_a$ or $\overline{E}_a$ inputs respectively. The enable gate for Decoder "b" requires two active LOW inputs ($\overline{E}_b \bullet \overline{E}_b$). The LS155 or LS156 can be used as a 1-of-8 Decoder/Demultiplexer by tying $\overline{E}_a$ to $\overline{E}_b$ and relabeling the common connection as (A2). The other $\overline{E}_b$ to $\overline{E}_a$ are connected together to form the common enable.

The LS155 and LS156 can be used to generate all four minterms of two variables. These four minterms are used in some applications replacing multiple gate functions as shown in Fig. 1. The LS156 has the further advantage of being able to AND the minterm functions by tying outputs together. Any number of terms can be wired-AND as shown below.

$$f = (E + A_0 + A_1) \bullet (E + \overline{A_0} + A_1) \bullet (E + A_0 + \overline{A_1}) \bullet (E + \overline{A_0} + \overline{A_1})$$

where $E = E_a + \overline{E_a}$; $E = E_b + \overline{E_b}$

Figure 1.



TRUTH TABLE

Address		Enable "a"		Output "a"				Enable "b"		Output "b"			
A_0	A_1	E_a	$\overline{E}_a$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{E}_b$	$\overline{E}_b$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Treshold Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Treshold Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage for LS155 Only	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
I_{OH}	Output HIGH Current for LS156 Only			100	V_{CC} = MIN, V_{OH} = - 5.5 V V_{IN} = V_{IH} or V_{IL} per Truth Table		µA
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		6.0	10	V_{CC} = MAX		mA

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits				Test Conditions		Unit
		LS155		LS156				
		Typ.	Max.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Address to Output	17 19	26 30	31 34	46 51	Fig. 2	V_{CC} = 5.0 V C_L = 15 pF R_L = 2 kΩ (only LS156)	ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{E}_a$ or $\overline{E}_b$ to Output	10 19	15 30	25 34	40 51	Fig. 3		ns
t_{PLH} t_{PHL}	Propagation Delay, E_a to Output	18 18	27 27	32 32	48 48	Fig. 2		ns

AC WAVEFORMS

Figure 2 .

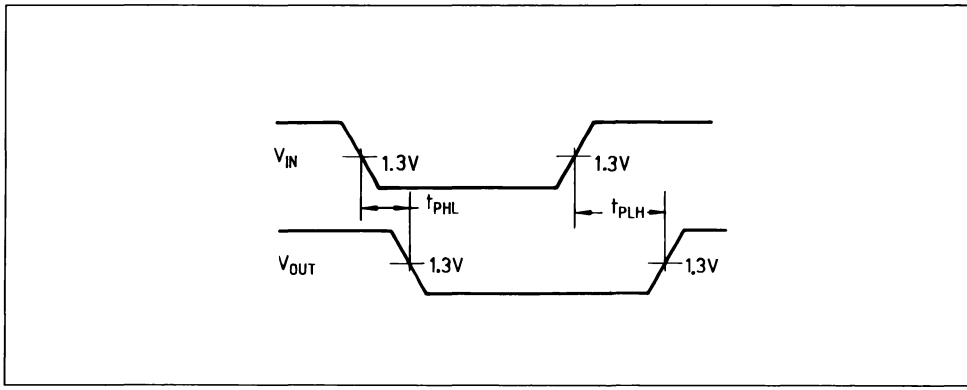
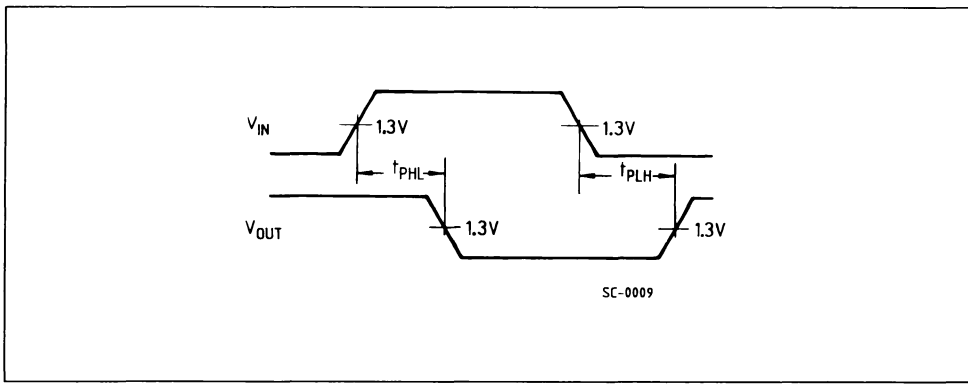


Figure 3.

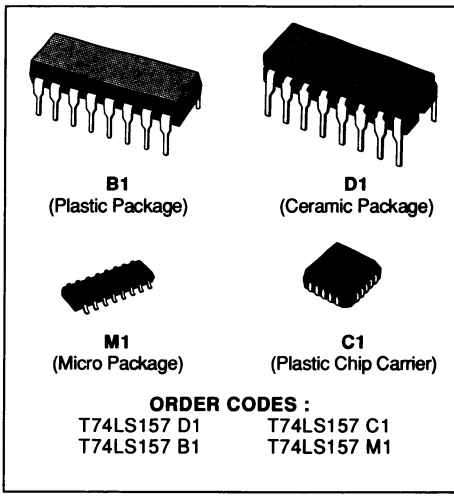


QUAD 2-INPUT MULTIPLEXER

- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- NON-INVERTING OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

DESCRIPTION

The TTL/MSI T74LS157 is a very high speed Quad 2-input Multiplexer, Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) from. The LS157 can also be used to generate any four of the 16 different functions of two variables. The LS157 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all TTL families.



B1 (Plastic Package)

D1 (Ceramic Package)

M1 (Micro Package)

C1 (Plastic Chip Carrier)

ORDER CODES :

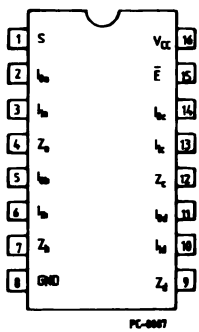
T74LS157 D1 T74LS157 C1
T74LS157 B1 T74LS157 M1

PIN NAMES

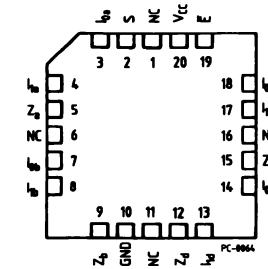
$\overline{S}$	COMMON SELECT INPUT
$\overline{E}$	ENABLE (active LOW) INPUT
$I_{0a} - I_{0b}$	DATA INPUTS FROM SOURCE 0
$I_{1a} - I_{1b}$	DATA INPUTS FROM SOURCE 1
$Z_a - Z_b$	MULTIPLEXER OUTPUTS

PIN CONNECTION (top view)

DUAL IN LINE

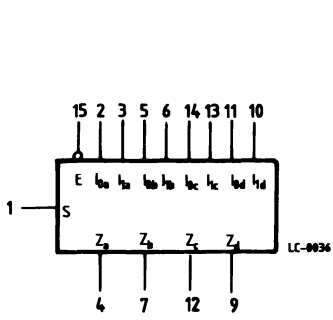


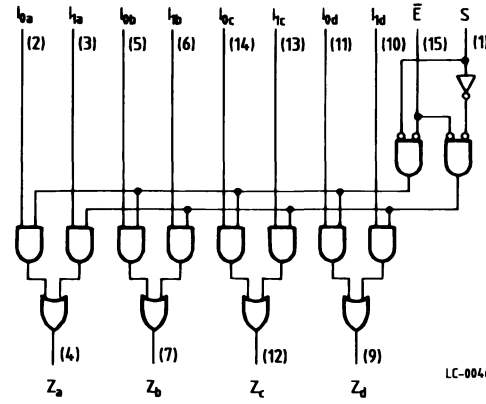
CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM





V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.6 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	

XX = package type.

FUNCTIONAL DESCRIPTION

The LS157 is a Quad 2-Input Multiplexer fabricated with the Schottky barrier diode process for high speed. It selects four bits of data from two sources under the control or the common Select Input (S). The Enable Input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs.

The LS157 is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels supplied to the Select Inputs. The logic equation for the outputs are shown below.

$$Z_a = \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$
$$Z_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$Z_c = \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$
$$Z_d = E \cdot (I_{1d} \cdot S + I_{0d} \cdot S)$$

A common use of the LS157 is the moving of data from two groups of registers to four common output buses. The particular register from which the data comes is determined by the state of the Select Input. A less obvious use is as a function generator. The LS157 can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.

TRUTH TABLE

Enable	Select Input	Inputs		Output
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Treshold Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Treshold Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN,	V
			0.35	0.5	I_{OL} = 8.0 mA	V_{IN} = V_{IH} or V_{IL} per Truth Table	V
I_{IH}	Input HIGH Current I_0, I_1 $\overline{E}$, S			 20 40	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	Input HIGH Current at Max Input Voltage I_0, I_1 $\overline{E}$, S			 0.1 0.2	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current I_0, I_1 $\overline{E}$, S			 - 0.4 - 0.8	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		10	16	V_{CC} = MAX		mA

Notes : 1 Conditions for testing, not shown in the table, are chosen to guarantee under "worst case" conditions.
2. Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Tests Conditions		Unit
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		15 18	23 27	Fig. 2	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PLH} t_{PHL}	Propagation Delay, Enable to Output		13 14	20 21	Fig. 1		ns
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		9 9	14 14	Fig. 2		ns

AC WAVEFORMS

Figure 1.

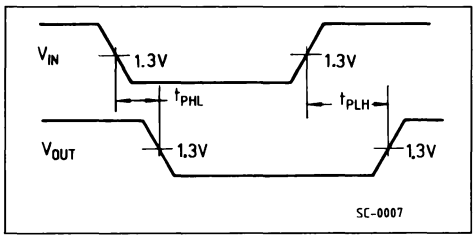
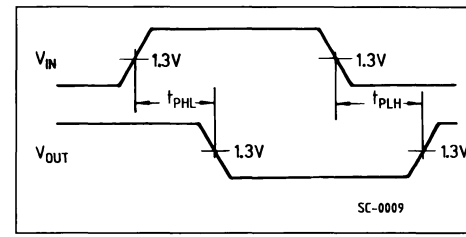


Figure 2.



SGS-THOMSON MICROELECTRONICS

T74LS158

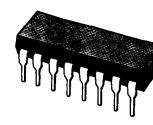
QUAD 2-INPUT MULTIPLEXER

- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- INVERTING OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

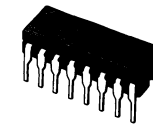
DESCRIPTION

The T74LS158 is a high speed Quad 2-input Multiplexer. It selects four bits of data from two sources using common Select and Enable inputs. The four buffered outputs present the selected data in the true inverted from. The LS158 can also generate any four of the 16 different functions of two variables.

The LS158 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all TTL families.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

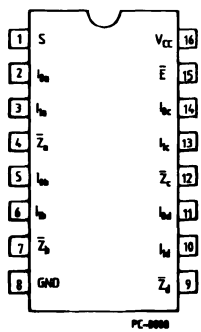
T74LS158 D1
T74LS158 B1
T74LS158 C1
T74LS158 M1

PIN NAMES

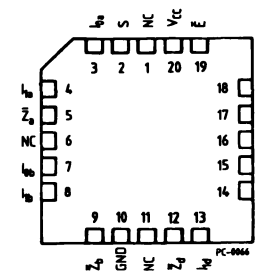
$\overline{S}$	COMMON SELECT INPUT
$\overline{E}$	ENABLE (active LOW) INPUT
$I_{0a} - I_{0d}$	DATA INPUTS FROM SOURCE 0
$I_{1a} - I_{1d}$	DATA INPUTS FROM SOURCE 1
$Z_a - Z_d$	INVERTED OUTPUTS

PIN CONNECTION (top view)

DUAL IN LINE

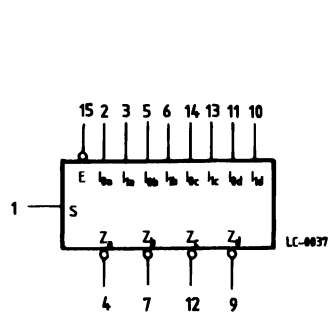


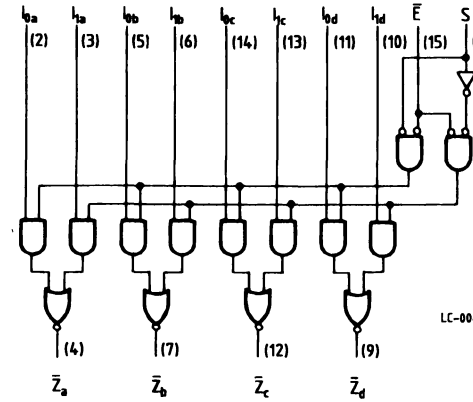
CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM





V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.6 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS158XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

FUNCTIONAL DESCRIPTION

The LS158 is a Quad 2-Input Multiplexer fabricated with the Schottky barrier diode process for high speed. It selects four bits of data from two sources under the control or the common Select Input (S) and present the data in inverted form at the four outputs. The Enable Input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs ($\overline{Z}$) are forced HIGH regardless of all other inputs.

The LS158 is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels supplied to the Select Inputs.

A common use of the LS158 is the moving of data from two groups of registers to four common output buses. The particular register from which the data comes is determined by the state of the Select Input. A less obvious use is as a function generator. The LS158 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

TRUTH TABLE

Enable	Select Input	Inputs		Output
$\overline{E}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Treshold Voltage for all Input		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Treshold Voltage for all Input		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN	V
			0.35	0.5	I_{OL} = 8.0 mA	V_{IN} = V_{IH} or V_{IL} per Truth Table	V
I_{IH}	Input HIGH Current I_0, I_1 E, S			 20 40	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	Input HIGH Current at Max Input Voltage I_0, I_1 E, S			 0.1 0.2	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current I_0, I_1 E, S			 - 0.4 - 0.8	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		5.0	8.0	V_{CC} = MAX		mA

Notes : 1. Conditions for testing, not shown in the table, are chosen to guarantee under "worst case" conditions.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Tests Conditions		Unit
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		13 16	20 24	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PLH} t_{PHL}	Propagation Delay, Enable to Output		11 18	17 24	Fig. 2		ns
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		7 10	12 15	Fig. 1		ns

AC WAVEFORMS

Figure 1.

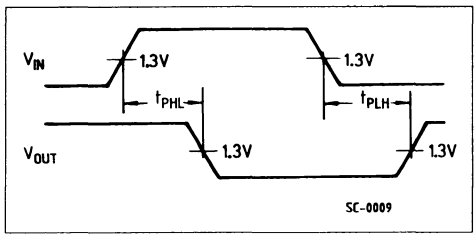
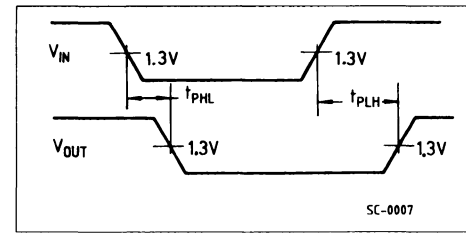


Figure 2.



T74LS160A/161A T74LS162A/163A

LS160A/162A : BCD DECADE COUNTERS
LS161A/163A : 4-BIT BINARY COUNTERS

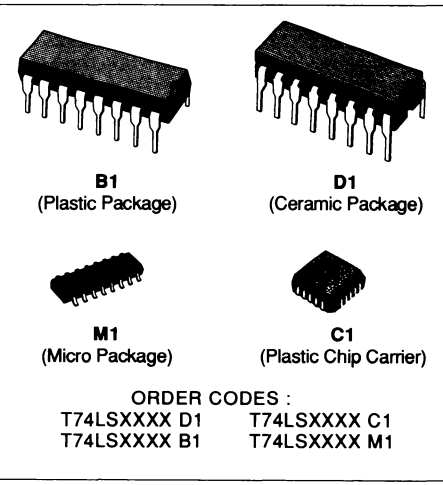
- SYNCHRONOUS COUNTING AND LOADING
- TWO COUNT ENABLE INPUTS FOR HIGH-SPEED SYNCHRONOUSLY EXPANSION
- EDGE-TRIGGERED OPERATION
- TYPICAL COUNT RATE OF 35 MHz
- FULLY TTL AND CMOS COMPATIBLE

DESCRIPTION

The LS160A/161A/162A/163A are high-speed 4-bit synchronous counters. They are edge-triggered, synchronously presettable, and cascadable MSI building, blocks for counting, memory addressing, frequency division and other applications. The LS160A and LS162A count modulo 10 (BCD). The LS161A and LS163A count modulo 16 (binary).

The LS160A and LS161A have an asynchronous Master Reset (Clear) input that overrides, and is independent of, the clock and all other control inputs. The LS162A and LS163A have a Synchronous Reset (Clear) input that overrides all other control inputs, but is active only during the rising clock edge.

	BCD Modulo 10	Binary (modulo 16)
Asynchronous Reset	LS160A	LS161A
Synchronous Reset	LS162A	LS163A



B1 (Plastic Package)

D1 (Ceramic Package)

M1 (Micro Package)

C1 (Plastic Chip Carrier)

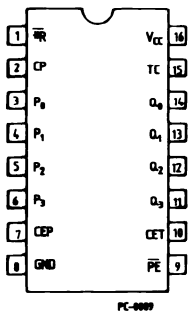
ORDER CODES :

T74LSXXXX D1 T74LSXXXX C1

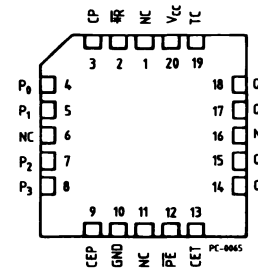
T74LSXXXX B1 T74LSXXXX M1

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



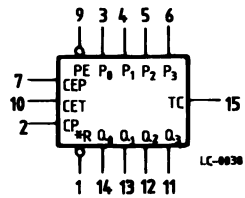
* $\overline{MR}$ for LS160A/161A
* $\overline{SR}$ for LS162A/163A
NC = No Internal Connection

PIN NAMES

$\overline{PE}$	PARALLEL ENABLE (active LOW) INPUT
$P_0 - P_3$	PARALLEL INPUTS
CEP	COUNT ENABLE PARALLEL INPUT
CET	COUNT ENABLE TICKLE INPUT
CP	CLOCK (avtive HIGH going edge) INPUT
$\overline{MR}$	MASTER RESET (active LOW) INPUT
$\overline{SR}$	SYNCHRONOUS RESET (active LOW) INPUT
$Q_0 - Q_3$	PARALLEL OUTPUTS
TC	TERMINAL COUNT OUTPUT

LOGIC SYMBOL AND TRUTH TABLE

* $\overline{MR}$ for LS160A/161A
* SR for LS162A/163A



V_{CC} = Pin 16
GND = Pin 8

*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge
L	X	X	X	Reset (clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (increment)
H	H	L	X	No Change (hold)
H	H	X	L	No Change (hold)

* For the LS162A and LS163A only

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS160A/161A/162A/163AXX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

FUNCTIONAL DESCRIPTION

The LS160A/161A/162A/163A are 4-bit synchronous counters with a synchronous Parallel Enable (Load) feature. These counters consist of four edge-triggered D flip-flops with the appropriate data routing networks feeding the D inputs. All changes of the Q outputs (except due to the asynchronous Master Reset in the LS160A and LS161A) occur as a result of, and synchronous with, the LOW to HIGH transition of the Clock input (CP). As long as the set-up time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs.

Three control inputs - Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) - select the mode of operation as shown in the tables. The Count Mode is enabled when the CEP, CET, and $\overline{PE}$ inputs are HIGH.

When the $\overline{PE}$ is LOW, the counters will synchronously load the data from the parallel inputs into the flip-flops on the LOW to HIGH transition of the clock. Either the CEP or CET inputs can be used to inhibit the count sequence. With the PE held HIGH, a LOW on either the CEP or CET inputs at least one set-up time prior to the LOW to HIGH clock transition will cause the existing output states to be retained. The AND feature of the two Count Enable inputs (CET-CEP) allows synchronous cascading without external gating and without delay accumulation over any pratical number of bits or digits.

The Terminal Count (TC) output is HIGH when the Count Enable Trickle (CET) input is HIGH while the counter is in its maximum count state (HLLH for the BCD counters, HHHH for the Binary counters). Note that TC is fully decoded and will, therefore, be HIGH only for one count state.

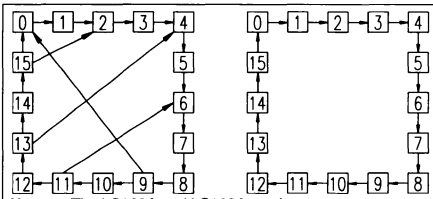
The LS160A and LS162A count modulo 10 following a binary coded decimal (BCD) sequence. They generate a TC output when the CET input is HIGH while the counter is in state 9 (HLLH). From this state they increment to state 0 (LLLL). If loaded with a code in excess of 9 they return to their legitimate sequence within two counts, as explained in the state diagram. States 10 through 15 do not generated a TC output.

The LS161A and LS163A count modulo 16 following a binary sequence. They generated a TC when the CET input is HIGH while the counter is in state 15 (HHHH). From this state they increment to state 0 (LLLL).

The Master Reset ($\overline{MR}$) of the LS160A and LS161A is asynchronous. When the $\overline{MR}$ is LOW, it overrides all other input conditions and sets the outputs LOW. The $\overline{MR}$ pin should never be left open. If not used, the $\overline{MR}$ pin should be tied through a resistor to V_{CC}, or to a gate output which is permanently set to a HIGH logic level.

The active LOW Sinchronous Reset ($\overline{SR}$) input of the LS162A and LS163A acts as an edge-triggered control input, overriding CET, CEP and $\overline{PE}$, and resetting the four counter flip-flops on the LOW to HIGH transition of the clock. This simplifies the design from race-free logic controlled reset circuits, e.g. to reset the counter synchronously after reaching a predetermined value.

STATE DIAGRAM



LOGIC EQUATIONS

Count Enable = CEP•CET•PE
TC for LS160A & LS162A = CET • Q_0 • $\overline{Q}_1$ • $\overline{Q}_2$ • Q_3
TC for LS161A & LS163A = CET • Q_0 • Q_1 • Q_2 • Q_3
Preset = $\overline{PE}$ • CP + (rising clock edge)
Reset = $\overline{MR}$ (LS160A & LS161A)
Reset = SR • CP + (rising clock edge (LS162A & LS163A))

Note : The LS160A and LS162A can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14 or 15, it will return to its normal sequence within two clock pulses.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current $\overline{MR}$, Data CEP Clock $\overline{PE}$ CET (LS160A/161A)			20 40	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	$\overline{MR}$, Data CEP Clock $\overline{PE}$ CET (LS160A/161A)			0.1 0.2	V_{CC} = MAX, V_{IN} = 7.0 V		mA
	Data, CEP, Clock PE, CET, $\overline{SR}$ (LS162A/163A)			20 40	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	Data, CEP, Clock $\overline{PE}$, CET, $\overline{SR}$ (LS162A/163A)			0.1 0.2	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current $\overline{MR}$, Data CEP Clock $\overline{PE}$ CET (LS160A/161A)			- 0.4 - 0.8	V_{CC} = MAX, V_{IN} = 0.4 V		mA
	Data, CEP, Clock PE, CET, $\overline{SR}$ (LS162A/163A)			- 0.4 - 0.8	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CCH} I_{CCL}	Power Supply Current		18 19	31 32	VCC = MAX		mA

Notes : 1. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions
2. Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Tests Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay, Clock to TC		20 18	35 35	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PLH} t_{PHL}	Propagation Delay, Clock to Q		13 18	24 27		ns
t_{PLH} t_{PHL}	Propagation Delay, CET to TC		9.0 9.0	14 14		ns
t_{PHL}	$\overline{MR}$ or $\overline{SR}$ to Q		20	28		ns
f_{MAX}	Maximum Clock Frequency	25	32			MHz

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_wCP	Clock Pulse Width	25			V_{CC} = 5.0 V	ns
t_w	$\overline{MR}$ or SR Pulse Width	20				ns
t_s	Set-up Time, any Input	20				ns
t_h	Hold Time, any Input	0				ns

DEFINITION OF TERMS

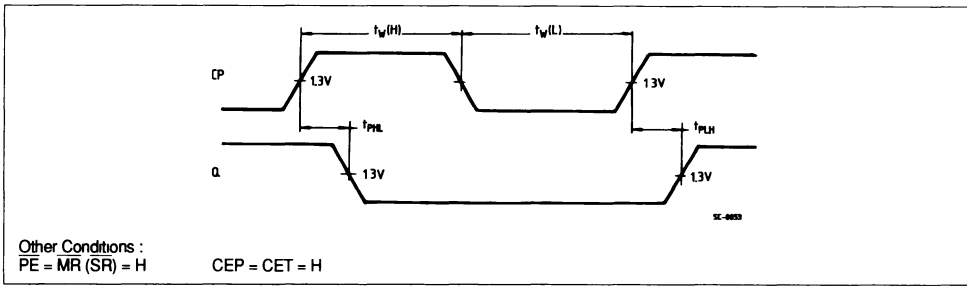
SET-UP-TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) - is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) - is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognized and transfer HIGH Data to the Q outputs.

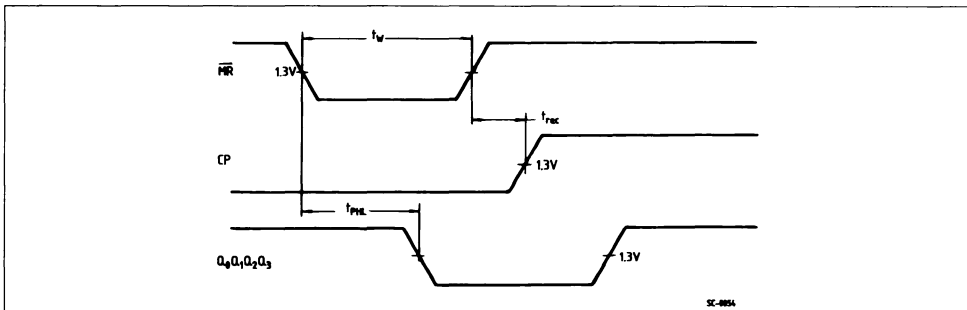
AC WAVEFORMS

Figure 1 :Clock to Output Delays, Count Frequency, and Clock Pulse Width.



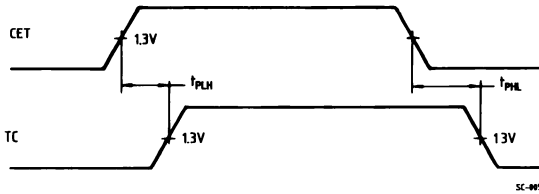
Other Conditions :
$\overline{PE}$ = $\overline{MR}$ (SR) = H CEP = CET = H

Figure 2 :Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery



Other Conditions : $\overline{PE}$ = L
$P_0 = P_1 = P_2 = P_3$ = H

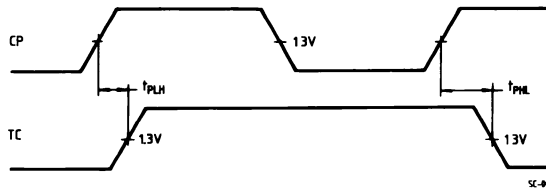
Figure 3 : Count Enable Trickle Input to Terminal Count Output Delays.



The positive TC pulse occurs when the outputs are in the ($Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3$) state for the LS160A and LS162A and the ($Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$) state for the LS161A and LS163A

Other Conditions :
$\overline{CP} = \overline{PE} = CEP = \overline{MR} = H$

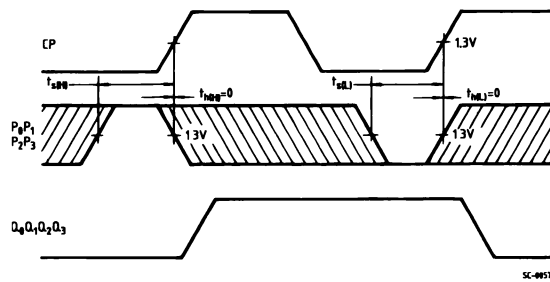
Figure 4 : Clock to Terminal Count Delays.



The positive TC pulse in coincident with the output state ($Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3$) state for the LS160A and LS162A and the ($Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$) state for the LS161A and LS163A.

Other Conditions :
$\overline{PE} = CEP = CET = \overline{MR} = H$

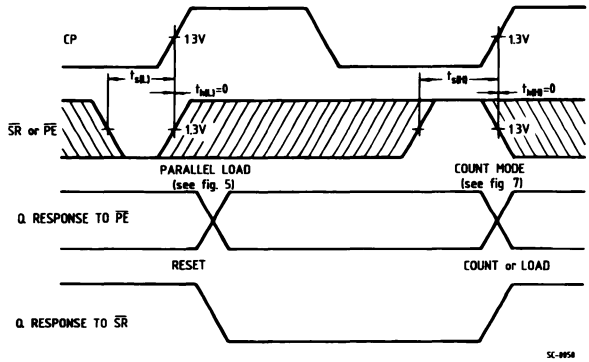
Figure 5 : Set-up Time (t_s) and Hold Time (t_h) for Parallel Data Inputs.



Other Conditions : $\overline{PE}$ = L, $\overline{MR}$ = H

The shaded areas indicate when the input is permitted to change for predictable output performance.

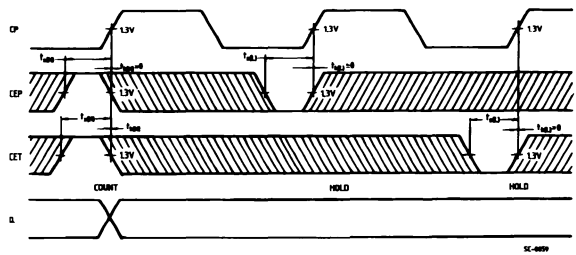
Figure 6 :Set-up Time (t_s) and Hold Time (t_h) for Count Enable (CEP) and (CET) and Parallel Enable ($\overline{PE}$) Inputs.



Other Conditions : $\overline{PE}$ = L, $\overline{MR}$ = H

The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 7.



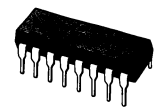
Other Conditions . $\overline{PE}$ = L, $\overline{MR}$ = H

SGS-THOMSON MICROELECTRONICS

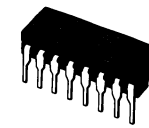
T74LS164

SERIAL-IN PARALLEL-OUT SHIFT REGISTER

- TYPICAL SHIFT FREQUENCY OF 35 MHz
- ASYNCHRONOUS MASTER RESET
- GATED SERIAL DATA INPUT
- FULLY SYNCHRONOUS DATA TRANSFERS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS164 D1 T74LS164 C1
T74LS164 B1 T74LS164 M1

DESCRIPTION

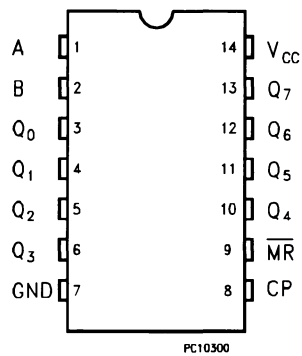
The T74LS164 is a 8-Bit Serial-In Parallel-Out Shift Register. Serial data is entered through a 2-Input AND gate synchronous with LOW to HIGH transition of the clock. The device features an asincronous Master Reset which clears the register setting all outputs LOW indipendent of the clock. It utilizes the Schottky diode clamped process to archive high sppeds and is fully compatible with all TTL roducts.

PIN NAMES

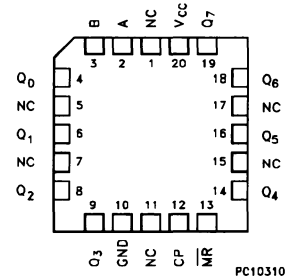
A, B	Data Input
CP	Clock (Active HIGH Going Edge) Input
MR	Master Reset (Active LOW) Input
Q_0-Q_7	Outputs

PIN CONNECTION (top view)

DUAL IN LINE

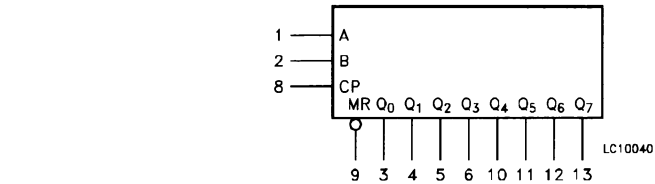


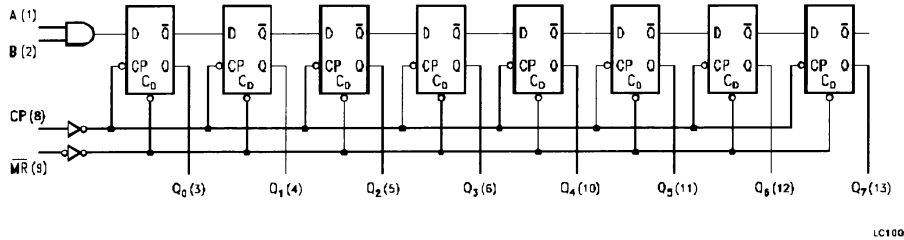
CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM





V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS164XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

FUNCTIONAL DESCRIPTION

The LS164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputss can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH, or both inputs connected together.

Each LOW to HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q0 the logoical AND of the two inputs (A B) that existed before the rising clock edge.

A LOW level on the Master Reset (MR) input overrides all other inputs and clears the register asynchronous, forcing all Q outputs LOW.

TRUTH TABLE

OPERATING MODE	INPUTS				
	$\overline{MR}$	A	B	Q_0	Q_1-Q_7
Reset (Clear)	L	X	X	L	L-L
Shift	H	l	l	L	q_0-q_6
	H	l	h	L	q_0-q_6
	H	h	l	L	q_0-q_6
	H	h	h	H	q_0-q_6

L (l) = LOW Voltage Levels
H (h) = HIGH Voltage Levels
X = Don't Care
q_n = Lower case letters indicate the state of the referenced input or output one set-up time pnor to the LOW to HIGH clock transition.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Input		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Input		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.5		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current (Note 3)		16	27	V_{CC} = MAX		mA

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
2. Not more than one output should be shorted at a time.
3. I_{CC} is measured with outputs open senal input at 2.4V, and a momentary ground, hen 4.5V applied to clear.
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C.

AC CHARACTERISTICS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
f_{MAX}	Maximum Clock Frequency	25	36		Figures 1	V_{CC} = 5.0 V C_L = 15 pF	MHz
t_{PLH} t_{PHL}	Propagation Delay, Positive Going Clock to Outputs		17 21	27 32	Figures 1		ns
t_{PHL}	Propagation Delay, Negative Going MR to Outputs		24	36	Figures 2		ns

AC SET-UP REQUIREMENTS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_s	Set-Up Time, A or B Input to Positive-Going CP	15			Figure 3	V_{CC} = 5.0 V C_L = 15 pF	ns
t_h	Hold Time, A or B Input to Positive-Going CP	5			Figure 3		ns
t_WCP(H)	CP Pulse Width (HIGH)	20			Figure 1		ns
t_WCP(L)	CP Pulse Width (LOW)	20			Figure 1		ns
t_WMR(L)	MR Pulse Width (LOW)	20			Figure 2		ns
t_{rec}	Recovery Time, Positive-Going MR to Positive-Going CP	20			Figure 2		ns

AC WAVEFORMS

Figure 1

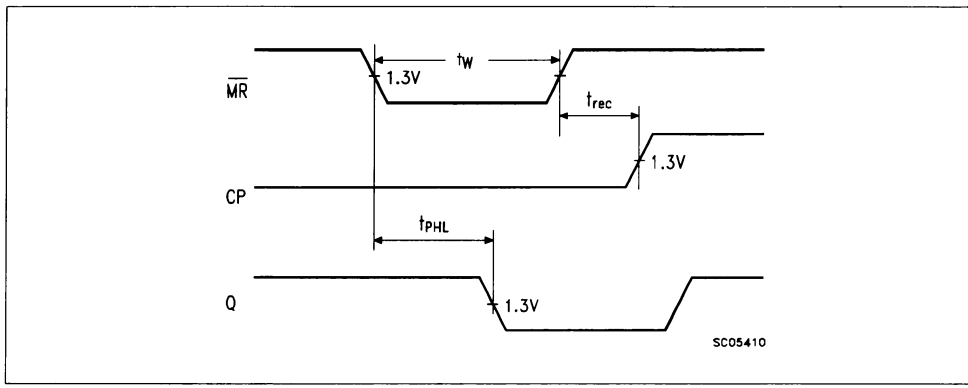


Figure 2

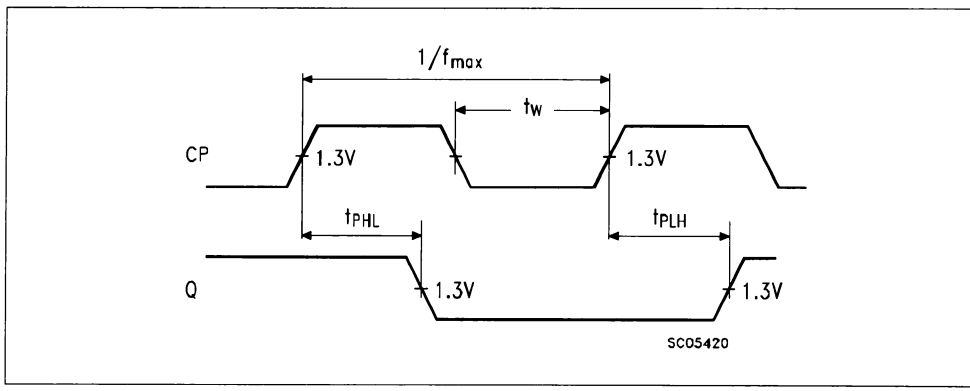
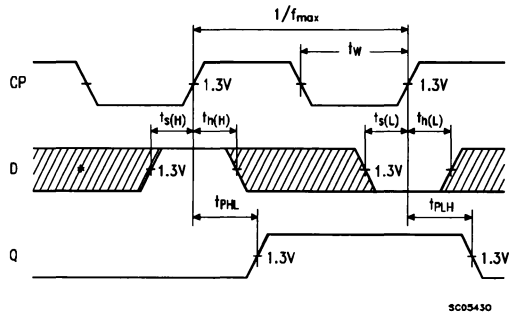


Figure 3


1/fmax
tw
CP
1.3V
1.3V
ts(H)
th(H)
ts(L)
th(L)
D
1.3V
1.3V
tPHL
tPLH
Q
1.3V
1.3V
SC03430

SGS-THOMSON MICROELECTRONICS

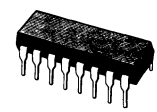
T74LS166

8-BIT SHIFT REGISTER

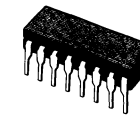
- DIRECT OVERRIDING CLEAR
- PARALLEL CONVERSION
- SYNCHRONOUS LOAD

DESCRIPTION

The T74LS166 is an 8-bit shift register. It consists of a parallel-in or serial-in, serial-out 8 bit shift register with gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are controlled by the SHIFT/LOAD input. When the SHIFT/LOAD input is held high, the serial data input is enabled and the eight flip-flop perform serial shifting with each clock pulse. When held LOW, the parallel data inputs are enabled and synchronous loading occurs on the next clock pulse. Clocking is accomplished on the low-to-high level edge of the clock pulse via a two input positive NOR gate. Clocking is inhibited when either of the clock inputs are held high, holding either input low enables the other clock inputs this will allow the system clock to be free running and the register stopped on command with the other clock inputs. The clock inhibit input should be changed to the high level only when the clock input is held high. A buffered direct input overrides all other inputs, including the clock, and sets all flip-flops to zero.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

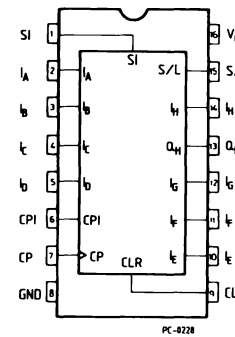
C1
(Plastic Chip Carrier)

ORDER CODES :

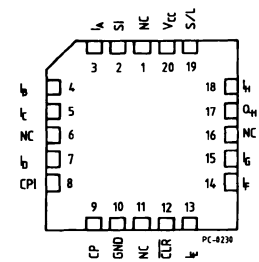
T74LS166 D1 T74LS166 C1
T74LS166 B1 T74LS166 M1

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER

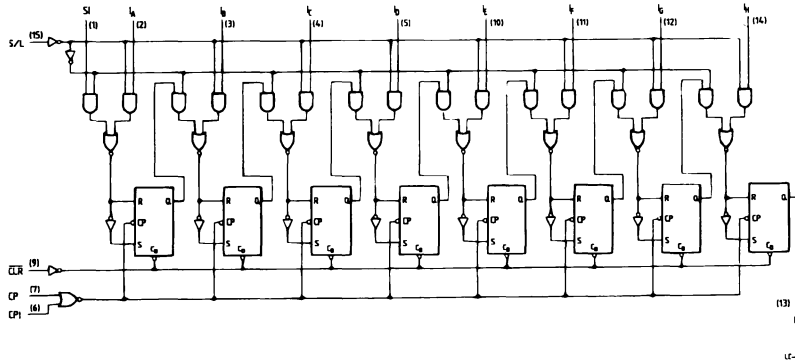


NC = No Internal Connection

PIN NAMES

A, B, C, D, E, F, G, H,	PARALLEL INPUTS
CLR	CLEAR
SIL	SHIFT LOAD
Q_H	OUTPUTS
SI	SERIAL INPUT
CP	CLOCK PULSE
CPI	CLOCK INHIBIT

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	0 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS166XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

TRUTH TABLE

Inputs						Internal Outputs		Output
Clear	Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{AO}	Q_{BO}	Q_{HO}
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{AO}	Q_{BO}	Q_{HO}

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX		mA
I_{CC}	Power Supply Current			38	V_{CC} = MAX		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Note more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

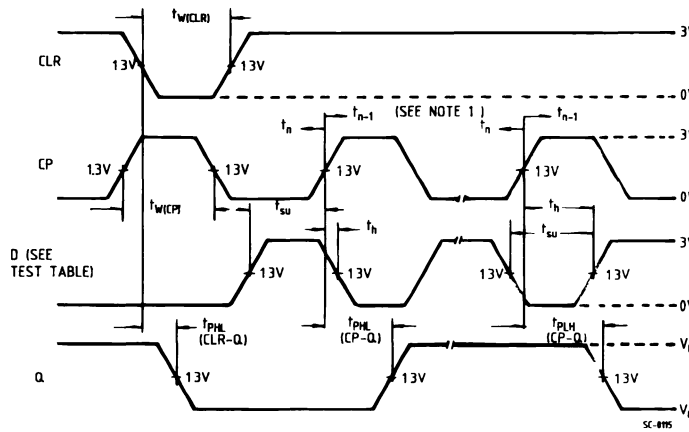
AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
f_{MAX}	Maximum Clock Frequency	25	35		V_{CC} = 5.0 V C_L = 15 pF	MHz
t_{PHL}	Clear to Output		19	30		ns
t_{PLH} t_{PHL}	Clock to Output		23 24	35 35		ns

AC WAVEFORMS

TEST TABLE
FOR SYNCHRONOUS INPUT

Data Input for Test	Shift/load	Output Tested
H	0 V	O_H at $t_n + 1$
Serial Input	4.5 V	O_H at $t_n + 8$

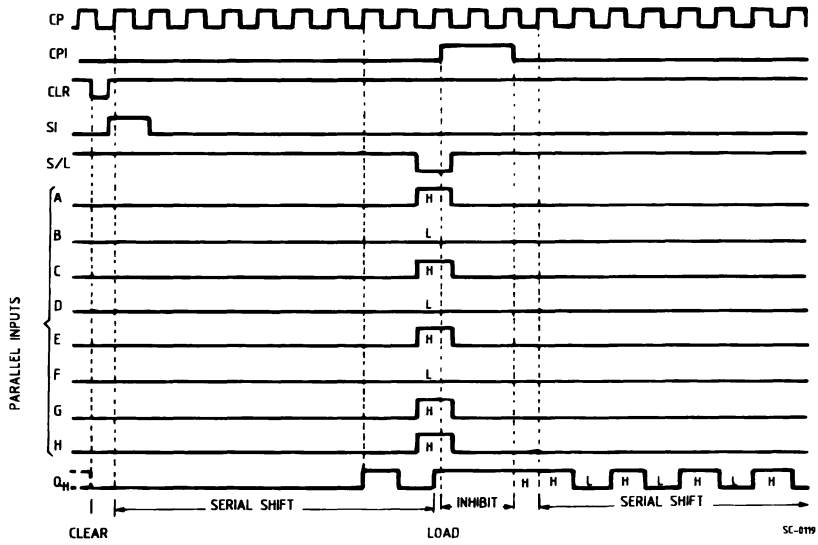


Notes : tn = bit time before clocking transition.
tn + 1 = bit time after one clocking transition
tn + 8 = bit time after eight clocking transitions.

AC SET-UP REQUIREMENTS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_W	Clock Clear Pulse Width	30			V_{CC} = 5.0 V	ns
t_s	Mode Control Set-up Time	30				ns
t_s	Data Set-up Time	20				ns
t_h	Hold Time, Any Input	15				ns

TYPICAL CLEAR, SHIFT, LOAD, INHIBIT, AND SHIFT SEQUENCES

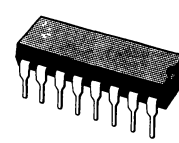


SGS-THOMSON
MICROELECTRONICS

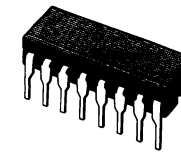
T74LS168
T74LS169

SYNCHRONOUS BI-DIRECTIONAL COUNTERS
LS168-BCD DECADE LS169-MODULO 16 BINARY

- LOW POWER DISSIPATION 100 mW TYPICAL
- HIGH SPEED COUNT FREQUENCY 30 MHz TYPICAL
- FULLY SYNCHRONOUS OPERATION
- FULL CARRY LOOKAHEAD FOR EASY CASCADING
- SINGLE UP/DOWN CONTROL INPUT
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE
- POSITIVE EDGE-TRIGGER OPERATION



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

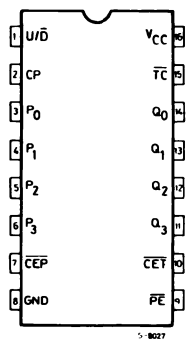
T74LSXXX D1	T74LSXXX C1
T74LSXXX B1	T74LSXXX M1

DESCRIPTION

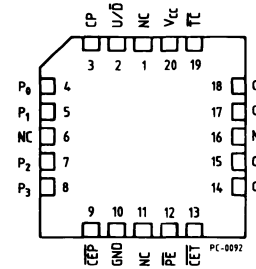
The T74LS168 and T74LS169 are fully synchronous 4-stage up/down counters featuring a present capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. The T54LS/T74LS168 counts in a BCD decade (8, 4, 2, 1) sequence, while the T54LS/T74LS169 operates in a Modulo 16 binary sequence. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

MODE SELECT TABLE

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load (Pn → Qn)
H	L	L	H	Count Up (increment)
H	L	L	L	Count Down (decrement)
H	H	X	X	No Change (hold)
H	X	H	X	No Change (hold)

H = HIGH Volyge Level
L = LOW Voltage Level
X = Don't Care

PIN NAMES

$\overline{CEP}$	COUNT ENABLE PARALLEL (active LOW) INPUT
$\overline{CET}$	COUNT ENABLE TRICKLE (active LOW) INPUT
CP	CLOCK PULSE (active positive going edge) INPUT
$\overline{PE}$	PARALLEL ENABLE (active LOW) INPUT
U/$\overline{D}$	UP-DOWN COUNT CONTROL INPUT
P_0 - P_3	PARALLEL DATA INPUTS
Q_0 - Q_3	FLIP-FLOP OUTPUTS
$\overline{TC}$	TERMINAL COUNT (active LOW) OUTPUT

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

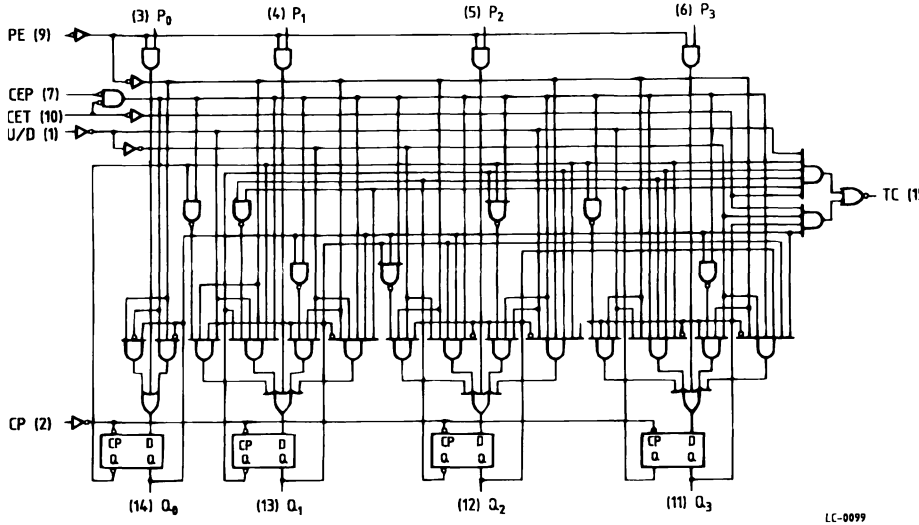
GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS1668/169XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

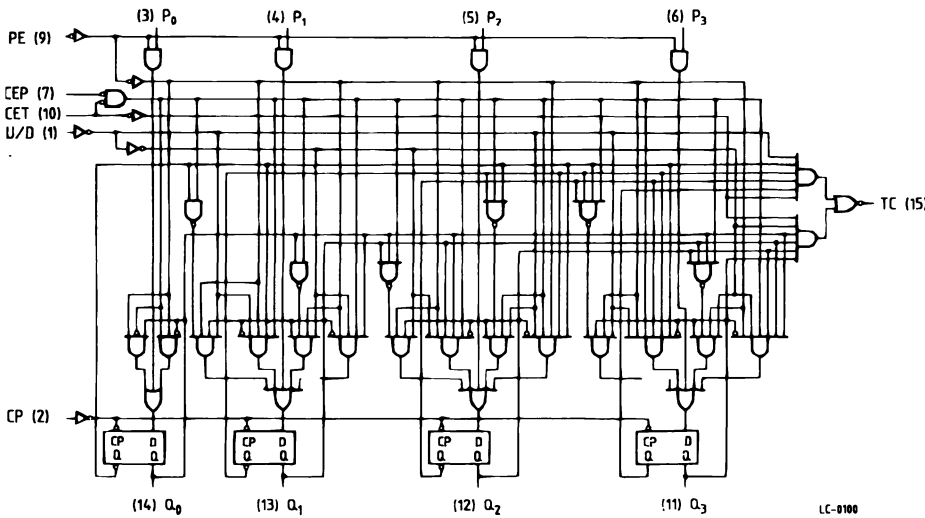
XX = package type

LOGIC DIAGRAM

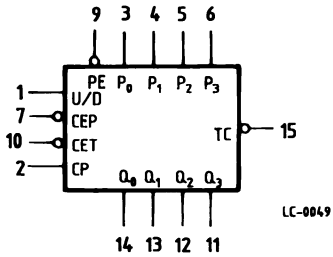
LS168



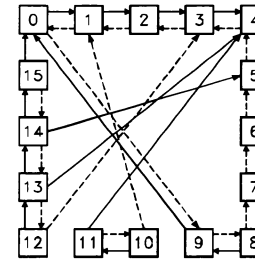
LS169



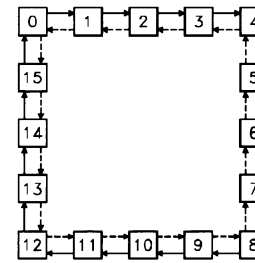
LOGIC SYMBOL AND STATE DIAGRAMS



74LS168
UP/DOWN DECADE COUNTER



74LS169



LS168
UP : TC = $Q_0 \bullet \overline{Q_3} \bullet (U/\overline{D})$
DOWN : TC = $\overline{Q_0} \bullet \overline{Q_1} \bullet \overline{Q2} \bullet \overline{Q_3} \bullet (U/D)$
LS169
UP : TC = $Q_0 \bullet Q_1 \bullet Q_2 \bullet \overline{Q_3} \bullet (U/\overline{D})$
DOWN : TC = $\overline{Q_0} \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet \overline{Q_3} \bullet (U/\overline{D})$

——→ Count up
----------> Count down

FUNCTIONAL DESCRIPTION

The LS168 and LS169 use edge-triggered D-type flip-flops and have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a set-up time before the rising edge of the clock and remain valid for the recommended hold time thereafter.

The parallel load operation takes precedence over the other operation, as indicated in the Mode Select Table. When $\overline{PE}$ is LOW, the data on the P_0-P_3 inputs enters the flip-flips on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be LOW an $\overline{PE}$ must be HIGH. The U/$\overline{D}$ input the, determines the direction of counting.

The terminal count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that $\overline{CET}$ is LOW, when a counter reaches zero in the COUNT DOWN mode or reaches 15 (9 for the T54LS/T74LS168) in the COUNT UP mode. The TC output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. The $\overline{TC}$ output of the LS168 decade counter can alsobe LOW in the illegal states 11.13 and via parallel loading. If an illegal state occurs, the LS168 will return to the legitmate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exist the possibility of decoding to spikes on $\overline{TC}$. For this reasons the use of $\overline{TC}$ as a clock signal is not recommended.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.5		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current $\overline{U/D}$, CP, $\overline{CEP}$, P_0-P_3, $\overline{PE}$ $\overline{CET}$			 20 40	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	Input HIGH Current $\overline{U/D}$, CP, $\overline{CEP}$, P_0-P_3, $\overline{PE}$ $\overline{CET}$			 0.4 0.2	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current $\overline{U/D}$, CP, $\overline{CEP}$, P_0-P_3, $\overline{PE}$ $\overline{CET}$			 - 0.4 - 0.8	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		20	34	V_{CC} = MAX		mA

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	CP to Q		15 15	20 20	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PLH} t_{PHL}	CP to $\overline{TC}$		22 22	30 30	Fig. 3		ns
t_{PLH} t_{PHL}	$\overline{CET}$ to $\overline{TC}$		10 15	15 20	Fig. 2		ns
t_{PLH} t_{PHL}	$\overline{U/D}$ to $\overline{TC}$		20 20	25 25	Fig. 6		ns
f_{MAX}	Maximum Clock Frequency	25	32		Fig. 1		MHz

AC SET-UP REQUIREMENTS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
$t_s(L)$ $t_s(H)$	Set-up LOW, Data to CP Set-up HIGH, Data to CP	15 15	12 12		Fig. 4	V_{CC} = 5.0 V	ns
$t_h(L)$ $t_h(H)$	Hold LOW, Data to CP Hold HIGH, Data to CP	5.0 5.0	0 0		Fig. 4		ns
$t_s(L)$ $t_s(H)$	Set-up LOW, $\overline{PE}$ to CP Set-up HIGH, $\overline{PE}$ to CP	15 15	12 12		Fig. 5		ns
$t_h(L)$ $t_h(H)$	Hold LOW, $\overline{PE}$ to CP Hold HIGH, $\overline{PE}$ to CP	5.0 5.0	0 0		Fig. 5		ns
$t_s(L)$ $t_s(H)$	Set-up LOW, $\overline{CET}$ or $\overline{CEP}$ to CP Set-up HIGH, $\overline{CET}$ or $\overline{CEP}$ to CP	15 15	12 12		Fig. 5		ns
$t_h(L)$ $t_h(H)$	Hold LOW, $\overline{CET}$ or $\overline{CEP}$ to CP Hold HIGH, $\overline{CET}$ or $\overline{CEP}$ to CP	15 15	12 12		Fig. 5		ns
$t_s(L)$ $t_s(H)$	Set-up LOW, U/$\overline{D}$ to CP Set-up HIGH, U/$\overline{D}$ to CP	25 25	20 20		Fig. 6		ns
$t_h(L)$ $t_h(H)$	Hold LOW, U/$\overline{D}$ to CP Hold HIGH, U/$\overline{D}$ to CP	0 0	− 4.0 − 4.0		Fig. 6		ns
$t_wCP(L)$ $t_wCP(H)$	Clock Pulse Width LOW Clock Pulse Width HIGH	20 10	18 5.0		Fig. 1		ns

DEFINITION OF TERMS

SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognizeed and transferred to the outputs.

HOLD TIME (t_h) - is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

AC WAVEFORMS

Figure 1 : Clock to Output Delays, Count Frequency, and Clock Pulse Width.

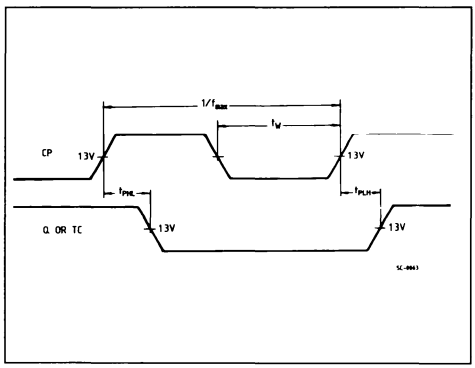


Figure 2 : Count Enable Trickle Input To Terminal Count Output Delays.

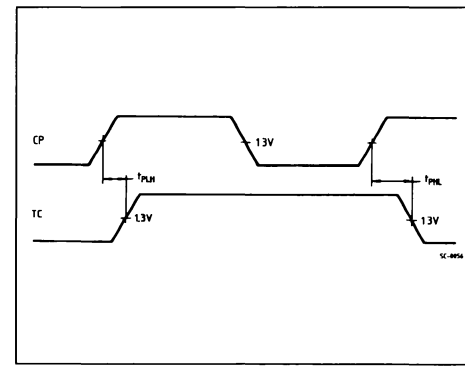


Figure 3 : Clock to Terminal Delays.

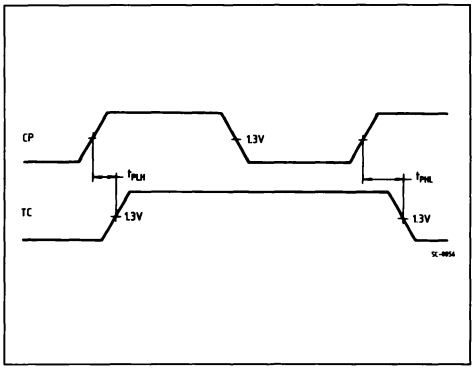


Figure 4 : Set-Up Time (t_s) and Hold (t_h) for Parallel Data Inputs.

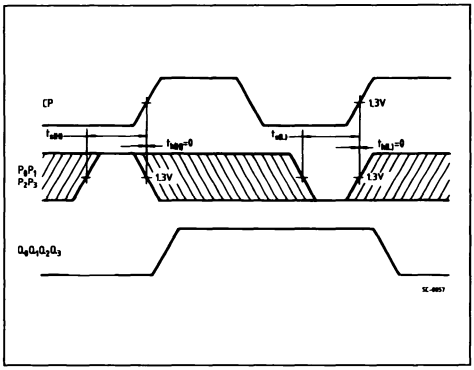
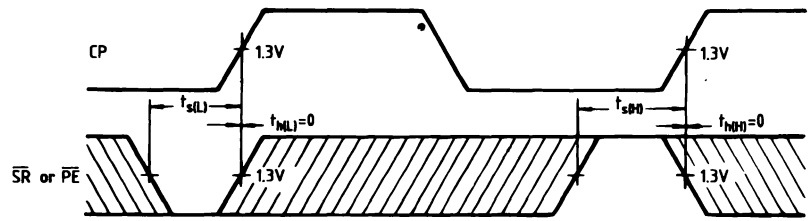


Figure 5 : Set-Up Time (t_s) and Hold Time (t_h) for Count Enable (CEP) and (CET), Parallel Enable (PE) Inputs, and Up-Down (U/D) Control Inputs.



The shaded areas indicate when the input is permitted to change for predictable output performance.

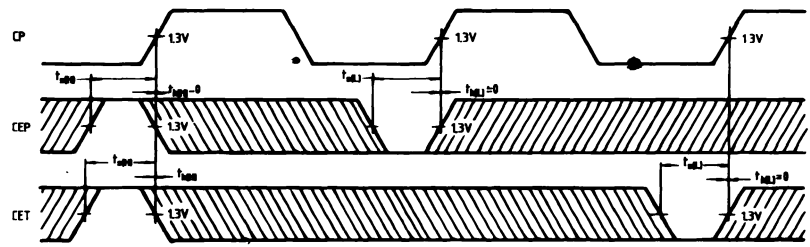
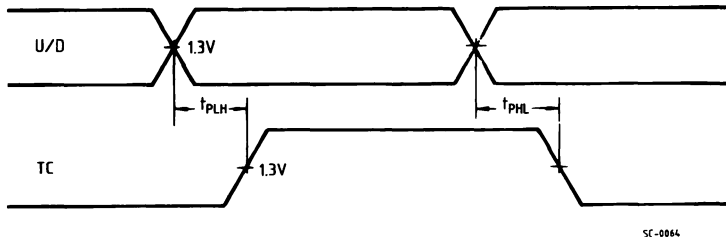


Figure 6 : Up-Down Input to Terminal Count Output Delays.

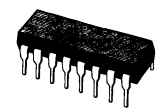


SGS-THOMSON MICROELECTRONICS

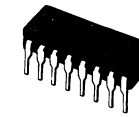
T74LS170

4 x 4 REGISTER FILE

- SIMULTANEOUS READ/WRITE OPERATION
- EXPANDABLE TO 512 WORDS OF n-BIT
- TYPICAL ACCESS TIME OF 20 ns
- LOW LEAKAGE OPEN COLLECTOR OUTPUTS FOR EXPANSION
- TYPICAL POWER DISSIPATION OF 125 mW
- INPUT CLAMP DIODE LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS170 D1 T74LS170 C1
T74LS170 B1 T74LS170 M1

DESCRIPTION

The T74LS170 is a high speed, low power 4 x 4 Register File organized as four word by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation.

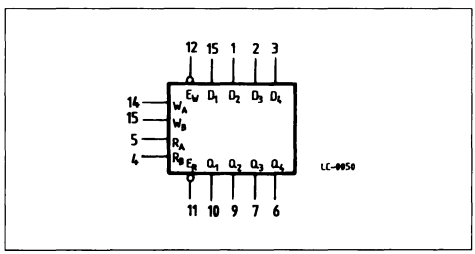
Open Collector outputs make it possible, to connect up to 128 outputs in a wired-AND configuration to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length.

The T74LS670 provides a similar function tothis device but it features 3-state outputs.

PIN NAMES

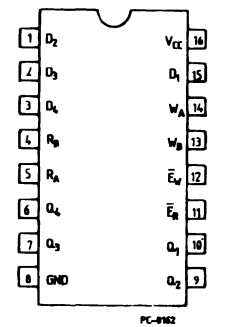
D_1-D_4	Data Inputs
W_A-W_B	Write Address Inputs
$\overline{E}_W$	Write Enable (Active LOW) Input
R_A-R_B	Read Address Inputs
$\overline{E}_R$	Read Enable (Active LOW) Input
Q_1-Q_4	Outputs

LOGIC DIAGRAM

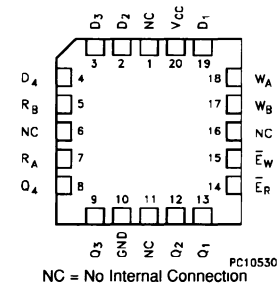


PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

WRITE TRUTH TABLE

WRITE INPUTS			WORD			
W_B	W_A	$\overline{E}_W$	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q0	Q0
H	L	L	Q_0	Q0	Q = D	Q0
H	H	L	Q_0	Q0	Q0	Q = D
X	X	H	Q_0	Q0	Q0	Q0

READ TRUTH TABLE

READ INPUTS			OUTPUTS			
R_B	R_A	$\overline{E}_R$	Q_1	Q_2	Q_3	Q_4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

NOTES: H= HIGH Level, L = LOW Level, X = Don't Care
(Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
Q0 = The level of Q before the indicated input conditions were established.
W0B1 = The first bit of word 0 etc.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	0 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

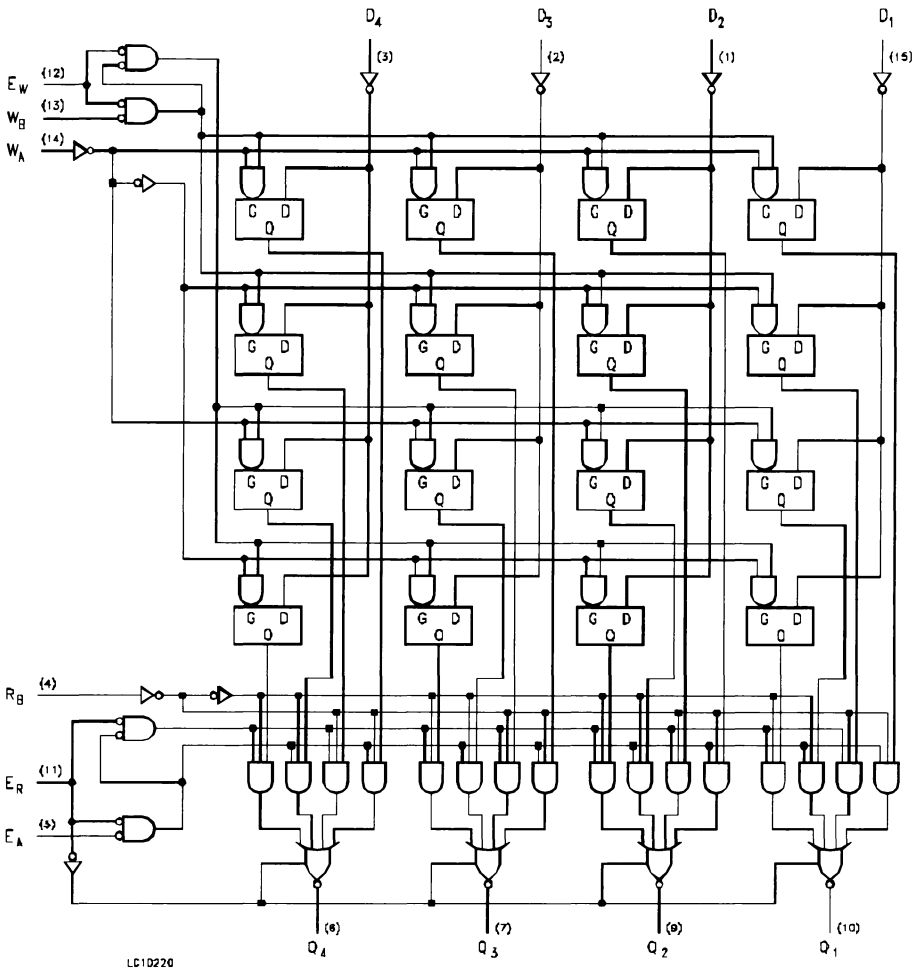
Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS170XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

LOGIC DIAGRAMS



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
I_{OH}	Output HIGH Current			20	V_{CC} = MIN, V_{OH} = - 5.5 V V_{IN} = V_{IH} or V_{IL} per Truth Table		µA
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current Any D, R or W $\overline{E_R}$ or $\overline{E_W}$			 20 40	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	Any D, R or W $\overline{E_R}$ or $\overline{E_W}$			0.1 0.2	VCC = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current Any D, R or W $\overline{E_R}$ or $\overline{E_W}$			 - 0.4 - 0.8	VCC = MAX, V_{IN} = 0.4 V		mA
I_{CC}	Power Supply Current (Note 2)		25	40	V_{CC} = MAX		mA

Notes : 1 For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges
2 I_{CC} is measured under the following worst case conditions 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C

AC CHARACTERISTICS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Negative Going $\overline{E_R}$ to Q Outputs		20 20	30 30	Figures 1	V_{CC} = 5.0 V C_L = 15 pF R_L = 2 KΩ	ns
t_{PLH} t_{PHL}	Propagation Delay, RA or R_B to Q Outputs		25 24	40 40	Figures 2		ns
t_{PLH} t_{PHL}	Propagation Delay, Negative Going $\overline{E_W}$ to Q Outputs		30 26	40 40	Figures 1		ns
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs to Q Outputs		30 22	45 35	Figures 1		ns

AC SET-UP REQUIREMENTS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
t_W	Clock Pulse Width (LOW) for $\overline{E}_W$	25			V_{CC} = 5.0 V Fig. 3	ns
t_sD (Note 3)	Set-up Time, Data Inputs whith Respect to Positive-Going $\overline{E}_W$	10				ns
t_hD (Note 4)	Hold Time, Data Inputs whith Respect to Positive-Going $\overline{E}_W$	15				ns
t_sW (Note 5)	Set-up Time, Write Select Input W_A and W_B whith Respect to Positive-Going $\overline{E}_W$	15				ns
t_hW (Note 4)	Hold Time, Write Select Input W_A and W_B whith Respect to Positive-Going $\overline{E}_W$	15				ns
t_{LATCH}	Latch Time	25				ns

Notes: 3) The Data to Enable Set-up Time is defined as the time required for the logic level to be present at the Data input prior to the enable transition for LOW to HIGH in order from the latch to recognize and store the new data.

4) The Hold Time (th) is defined as the minimum time following the enable transition from LOW to HIGH that the logic level must be maintained at the input inorder toensure continued recognition

5) The address to Enable Set-up Time is the time before the HIGH to LOW Enable transition the Address must be stable so that the crrect latch is addressed and the other latches are not affect.

AC WAVEFORM

Fig 1.

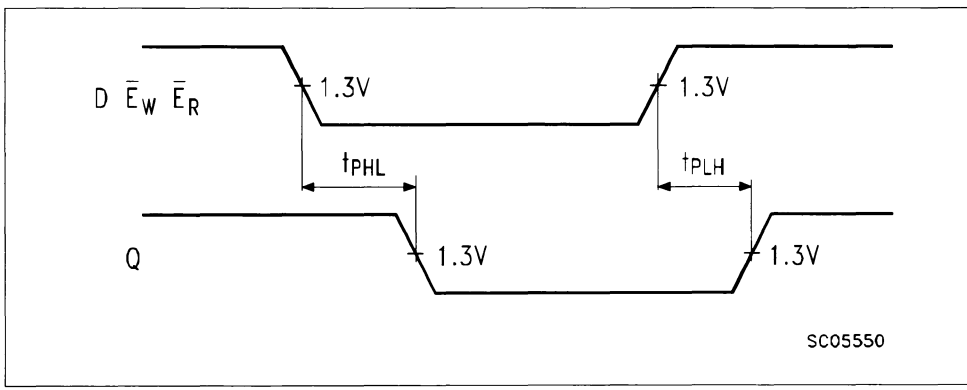


Fig 2.

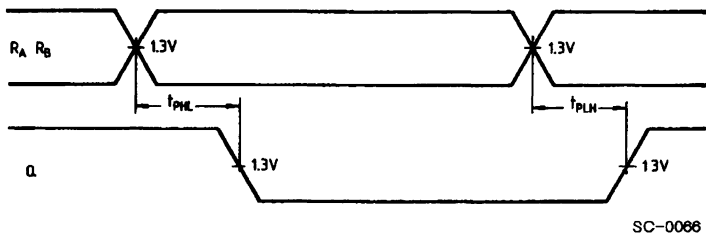
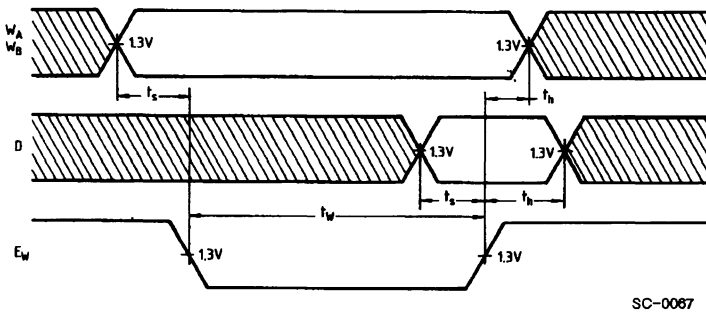


Fig 3.



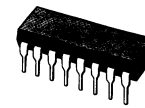
The shaded areas indicate when the inputs are permitted to change for predictable output performance

SGS-THOMSON MICROELECTRONICS

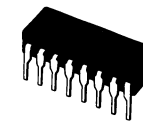
T74LS174

HEX D FLIP-FLOP

- EDGE-TRIGGERED D-TYPE INPUTS
- BUFFERERD-POSITIVE EDGE TRIGGERED CLOCK
- ASYNCHRONOUS COMMON RESET
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS174 D1
T74LS174 B1
T74LS174 C1
T74LS174 M1

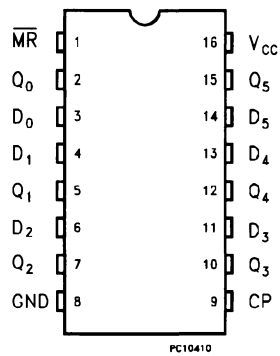
DESCRIPTION

The LSTTL/MSI T74LS174 is a high speed Hex D Flip-Flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW to HIGH clock transition. The device has a Master Reset to simultaneously clear all plip-flops.

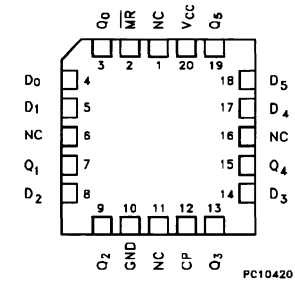
The LS174 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all TTL families

PIN CONNECTION (top view)

DUAL IN LINE

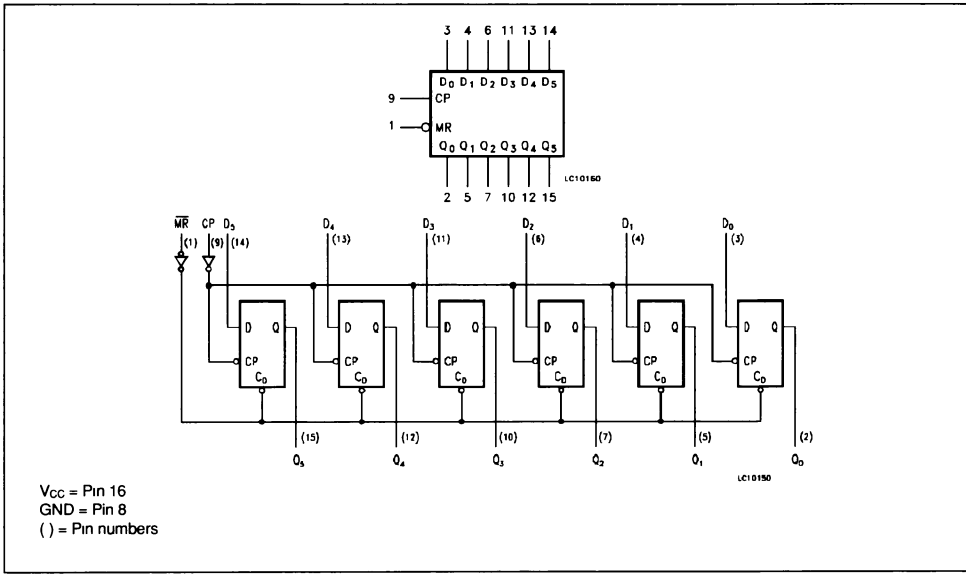


CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

TRUTH TABLE

Inputs (t = n, $\overline{MR}$ = H)	Outputs (t = n + 1) Note 1
D	Q
H	H
L	L

Note 1 t = n + 1 indicates conditions after next clock

PIN NAMES

D_0-D_5	Data Input
CP	Clock (Active HIGH Going-Edge) Input
$\overline{MR}$	Master Reset (Active LOW) Input
Q_0-Q_5	Outputs

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS174XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

FUNCTIONAL DESCRIPTION

The LS174 consist of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset (MR) are common to all flip-flops. Each D input's state is transferred to corresponding flip-flop'ss output following the LOW to HIGH Clock (CP) transition.

A LOW input to Master Reset (MR) will force all outputs LOW independent of Clock or Data inputs. The LS174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Input		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Input		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.36	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		16	26	V_{CC} = MAX		mA

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C

AC CHARACTERISTICS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Clock to Outputs		20 21	30 30	Figures 1	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PLH}	Propagation Delay, MR to Outputs		23	35	Figures 2		ns
f_{MAX}	Maximum Input Clock Frequency	30	40		Figures 1		MHz

AC SET-UP REQUIREMENTS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_wCP	Clock Pulse Width	20			Figure 1		ns
t_s	Set-Up Time, Data to Clock	20			Figure 1		ns
t_h	Hold Time, Data to Clock (HIGH or LOW)	5			Figure 1		ns
t_{rec}	Recovery Time for $\overline{MR}$	25			Figure 2		ns
$t_w(\overline{MR})$	Minimum $\overline{MR}$ Pulse Width	20			Figure 2		ns

DEFINITION OF TERMS:

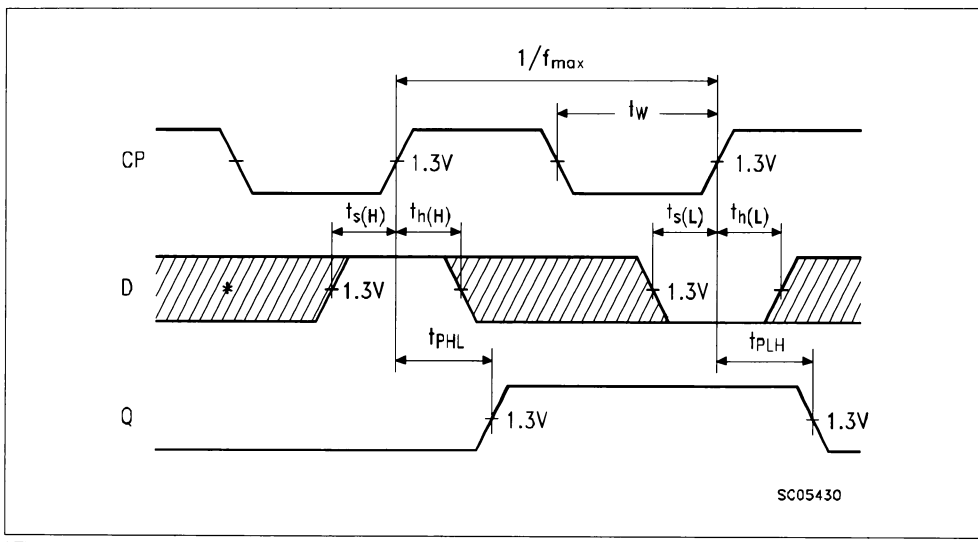
SET-UP TIME (t_s): is defined as the minimum time required for the corret logic level to be present at the logic input prior the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h): is defined as the minimum time following the clock transition from LOW to HIGH at which the logiclevel must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be relased prior to the clock transitio from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) : is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

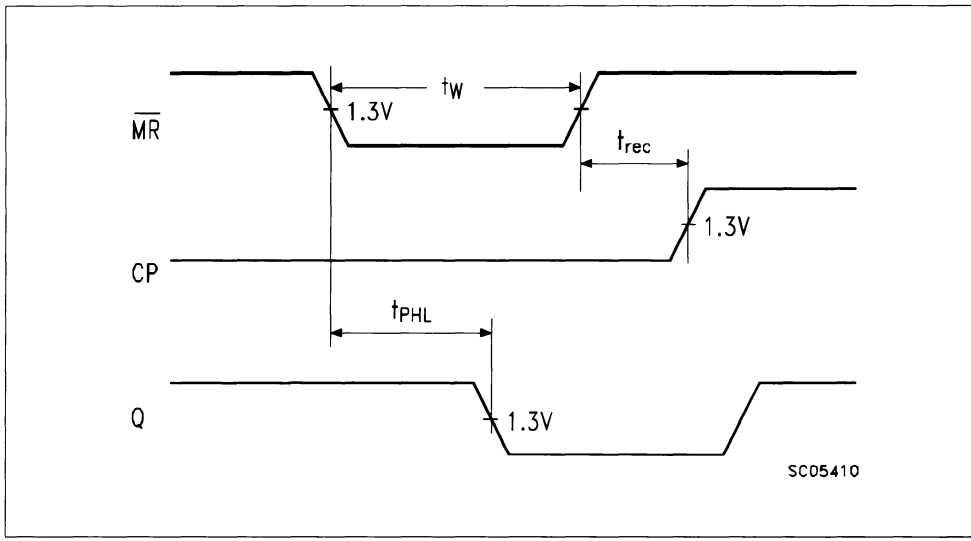
AC WAVEFORMS

Figure 1: Clock to Output Delays, Clock Pulse Width, Frequency Set-up and Hold Times Data to Clock :



* The shaded areas indicate when the input is permitted to chang for predictable output performance

Figure 2: Master Reset to Output Delay, Master Reset Pulse Width and Master Reset Recovery Time

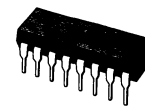


SGS-THOMSON MICROELECTRONICS

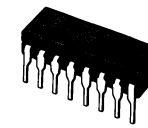
T74LS175

QUAD D FLIP-FLOP

- EDGE-TRIGGERED D-TYPE INPUTS
- BUFFERERD-POSITIVE EDGE TRIGGERED CLOCK
- ASYNCHRONOUS COMMON RESET
- TRUE AND COMPLEMENT OUTPUT
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS175 D1
T74LS175 B1
T74LS175 C1
T74LS175 M1

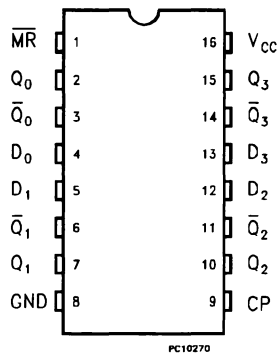
DESCRIPTION

The LSTTL/MSI T74LS175 is a high speed Quad D Flip-Flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW to HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input reset all flip-flop, independent of the Clock or D inputs, when LOW.

The LS175 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all TTL families

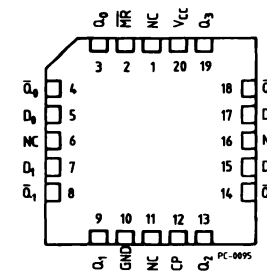
PIN CONNECTION (top view)

DUAL IN LINE



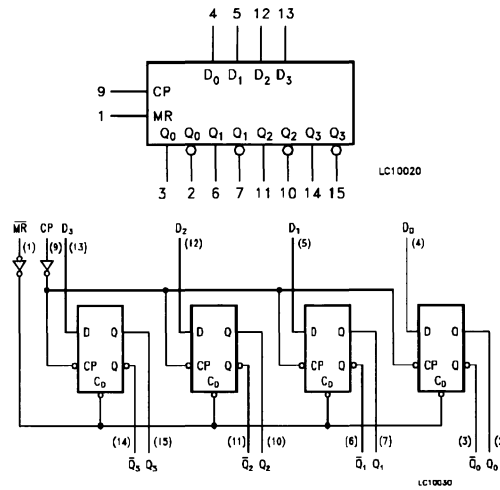
PC10270

CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

TRUTH TABLE

Inputs (t = n, $\overline{MR}$ = H)	Outputs (t = n + 1) Note 1	
D	Q	$\overline{Q}$
L	L	H
H	H	L

Note 1: t = n + 1 indicates conditions after next clock

PIN NAMES

D_0-D_3	Data Input
CP	Clock (Active HIGH Going-Edge) Input
MR	Master Reset (Active LOW) Input
Q_0-Q_3	True Outputs
$\overline{Q_0}$-$\overline{Q_3}$	Complemented Outputs

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS175XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

FUNCTIONAL DESCRIPTION

The LS175 consist of four edge-triggered D flip-flops with individual inputs and Q and $\overline{Q}$ outputs. The Clock and Master Resret are common. The four flip-flops will store the state of their individual D inputs on the LOW to HIGH Clock (CP) transition, causing individual Q and $\overline{Q}$ outputss to follow. A LOW input on the Master Reset (MR) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH indipendent of Clock or Data input.

The LS LS175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Input		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Input		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		11	18	V_{CC} = MAX		mA

Notes : 1 Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C.

AC CHARACTERISTICS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Clock to Outputs		13 16	25 25	Figures 1		ns
t_{PLH}	Propagation Delay, MR to Q Outputs		20	30	Figures 2		ns
t_{PLH}	Propagation Delay, MR to $\overline{Q}$ Outputs		20	30	Figures 2		ns
f_{MAX}	Maximum Input Clock Frequency	30	40		Figures 1		MHz

AC SET-UP REQUIREMENTS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
$t_{W(CP)}$	Clock Pulse Width	20			Figure 1	ns
t_s	Set-Up Time, Data to Clock	20			Figure 1	ns
t_h	Hold Time, Data to Clock (HIGH or LOW)	5			Figure 1	ns
t_{rec}	Recovery Time for $\overline{MR}$	25			Figure 2	ns
$t_{W(MR)}$	Minimum $\overline{MR}$ Pulse Width	20			Figure 2	ns

DEFINITION OF TERMS:

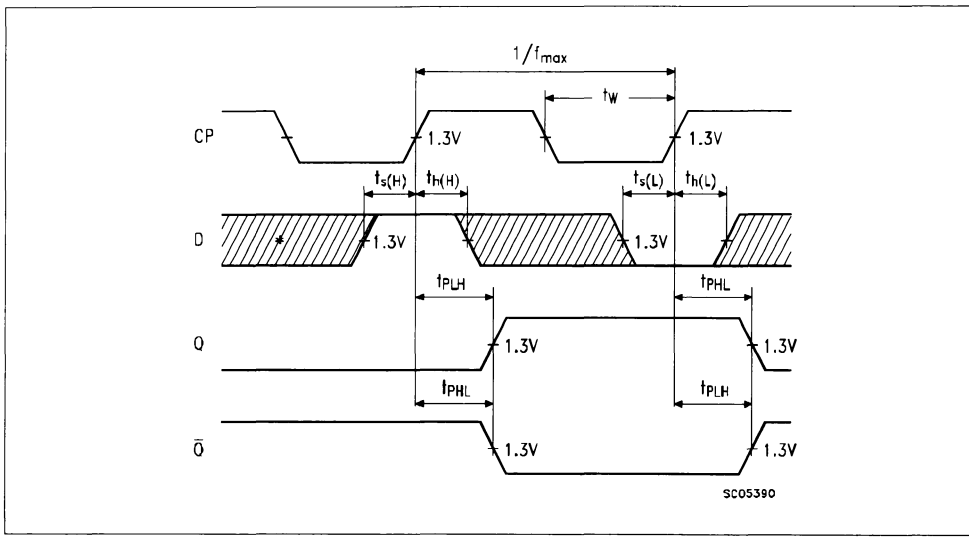
SET-UP TIME (t_s): is defined as the minimum time required for the corret logic level to be present at the logic input prior the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h): is defined as the minimum time following the clock transition from LOW to HIGH at which the logiclevel must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be relased prior to the clock transitio from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) : is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

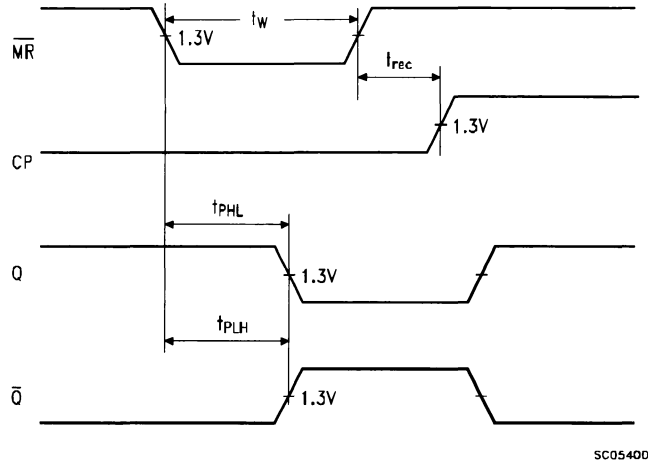
AC WAVEFORMS

Figure 1: Clock to Output Delays, Clock Pulse Width, Frequency Set-up and Hold Times Data to Clock



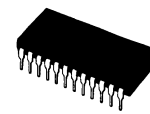
* The shaded areas indicate when the input is permitted to chang for predictable output performance

Figure 2: Master Reset to Output Delay, Master Reset Pulse Width and Master Reset Recovery Time



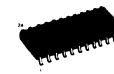
4-BIT ARITHMETIC LOGIC UNIT

- PROVIDES 16 ARITHMETIC OPERATIONS ADD, SUBTRACT, COMPARE, DOUBLE, PLUS TWELVW OTHER ARITHMETIC OPERATIONS
- PROVIDES ALL 16 LOGIC OPERATIONS OF TWO VARIABLES: EXCLUSIVE-OR COMPARE, AND, NAND, OR, NOR, PLUS TEN OTHER LOGIC OPERATION
- FULL LOOKAHEAD FOR HIGH SPEED ARITHMETIC OPERATION ON LONG WORDS
- INPUT CLAMP DIODES



B1
(Plastic Package)

D1
(Ceramic Package)



B1
(Plastic Package)

D1
(Ceramic Package)

ORDER CODES :

T74LS181 D1	T74LS181 C1
T74LS181 B1	T74LS181 M1

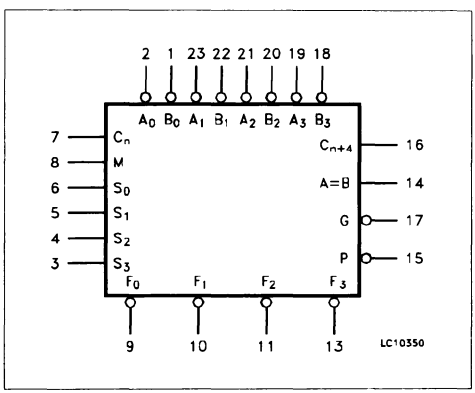
DESCRIPTION

The T74LS181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all possible 16 logic, operations on two variables and a variety of arithmetic operations.

PIN NAMES

$\overline{A}_1$-$\overline{A}_3$, $\overline{B}_0$-$\overline{B}_3$	Operand (ACTIVE low) Inputs
S_0-S_3	Function-Select Inputs
M	Mode Control Input
C_{IN}	Carry Input
$\overline{F}_0$-$\overline{F}_3$	Function (Active LOW) Outputs
$\overline{A}$ = B	Comparator Output
$\overline{G}$	Carry Generate (Active LOW) Output
$\overline{P}$	Carry Propagate (Active LOW) Output
C_{n+4}	Corry Output

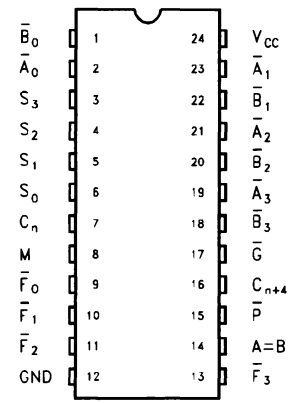
LOGIC SYMBOL



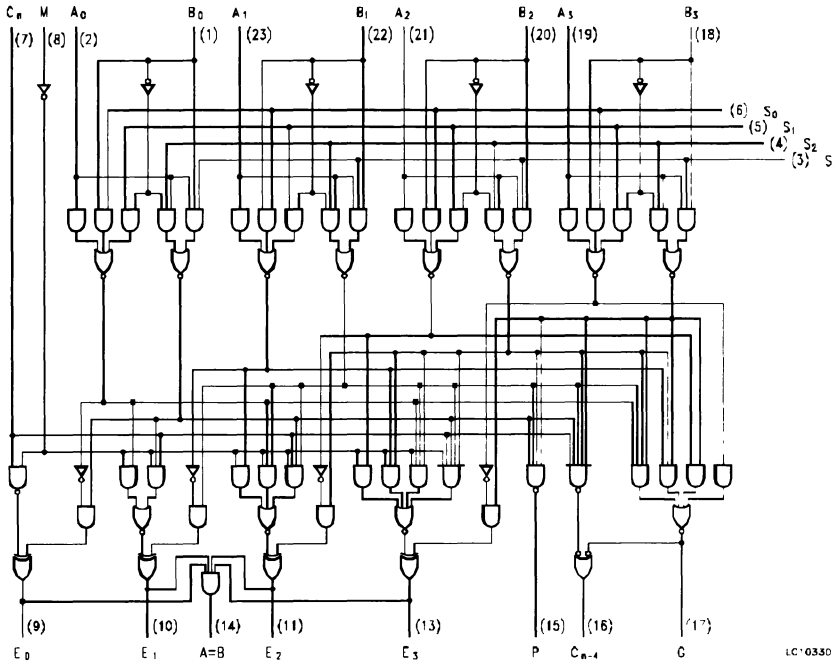
PIN CONNECTION

(top view)

DUAL IN LINE



LOGIC SYMBOL AND LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0 5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS181XX	4.75 V	5.0 V	5 25 V	0 °C to + 70 °C

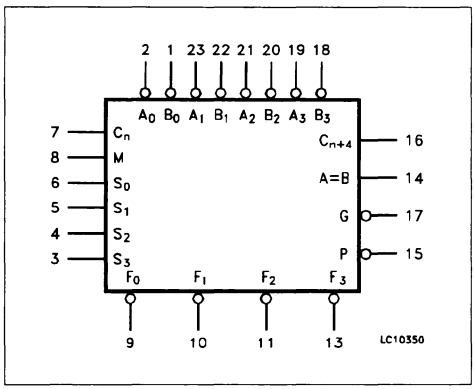
XX = package type.

TRUTH TABLE

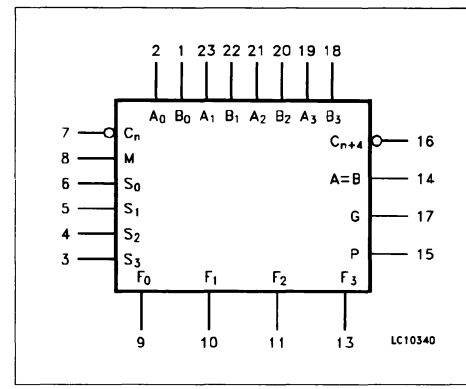
MODE SELECT INPUTS				ACTIVE LOW INPUTS & OUTPUS		ACTIVE HIGH INPUTS & OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M = H)	ARITHMETIC ** (M = L) (C_n = L)	LOGIC (M = H)	ARITHMETIC ** (M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A+B}$	A+B
L	L	H	L	$\overline{A+B}$	$A\overline{B}$ minus 1	$\overline{AB}$	$A+\overline{B}$
L	L	H	H	Logical 1	minus 1	Logical 0	minus 1
L	H	L	L	$\overline{A+B}$	A plus (A+B)	$\overline{AB}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	AB plus (A+B)	$\overline{B}$	(A+B) plus $A\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	$A+\overline{B}$	$A+\overline{B}$	AB	AB minus 1
H	L	L	L	$\overline{AB}$	A plus (A+B)	$\overline{A}+B$	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	$A\overline{B}$ plus (A+B)	B	$(A+\overline{B})$ plus AB
H	L	H	H	A+B	A+B	AB	AB minus 1
H	H	L	L	Logical 0	A plus A *	Logical 1	A plus A *
H	H	L	H	$A\overline{B}$	AB plus A	$A+\overline{B}$	(A+B) plus A
H	H	H	L	AB	$A\overline{B}$ plus A	A+B	$(A+\overline{B})$ plus A
H	H	H	H	A	A	A	A minus 1

L = LOW Voltage Level, H = HIGH Voltage Level
* Each bit is shifted to the next more significant position.
** Arithmetic operations expressed in 2s complement notation

ACTIVE LOW



ACTIVE HIGH



FUNCTIONAL DESCRIPTION

The T74LS181 is a 4-bit high speed Arithmetical Logic Unit (ALU). Controlled by the four Fuction Select Inputs (S_0, S_1, S_2, S_3) and the Mode Control Input (M), it can perform all the possible 16 logic operations or 16 different arithmetic operations or active HIGH or active LOW operands. The Function Table lists these operations.

When the Mode Control Input (M) is HIGH, all internal carriers are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control Input is LOW, the carriers are enabled and the device perform arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lokahead between packages using the signal $\overline{P}$ (Carry Proptage) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affect by carry in. When speed reqirements are not stringent, the LS181 can be used in a simple ripple carry mode by connecting the Carry Output (C_{n+4}) signal to the Carry Input (C_n) of the next unit. For high speed operation the LS181 is used in conjunction with other carry lookahead circuits. One carry lookahead package is required for each group of four LS181 devices. Carry lookahead can be provided at various levels and offers high spped capability over extremely long word lengths. The A=B output from the LS181 goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the substract mode. The A=B output is open collector and can be wired-AND with other A=B outputs to give a comparison for more than four bits. The A=B signal can also be used with the C_{n+4} signal to indicate A>B and A<B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A and B when carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry out means underflow and no carry is generated when there is underflow.

As indicated, the LS181 can be used with either active LOW input producing active LOW inputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Input		V
V_{IL}	Input LOW Voltage			-0.8	Guaranteed Input LOW Voltage for All Input		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.5		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
I_{OH}	Output HIGH Current			100	V_{CC} = MIN, V_{OH} = 5.5 V		µA
V_{OL}	Output LOW Voltage Except $\overline{G}$ and $\overline{P}$		0.25	0.4	I_{OL} = 4.0 mA	V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
	Output $\overline{G}$		0.47	0.7	I_{OL} = 1.6 mA		V
	Output $\overline{P}$		0.35	0.7	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current Mode Input A and B Inputs S Input Carry Inputs			 20 60 80 100	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	Mode Input A and B Inputs S Input Carry Inputs			0.1 0.3 0.4 0.5	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current Mode Input A and B Inputs S Input Carry Inputs			 - 0.36 - 1.08 - 1.44 - 2.0	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CC}	Power Supply Current Condition A (Note 3)		20	34	V_{CC} = MAX		mA
	Power Supply Current Condition B (Note 3)		21	37			mA

Notes : 1 Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
2. Not more than one output should be shorted at a time.
3 With output open, ICC is measured for the following conditions:
A. S_0 through S_3, M and A inputs are at 4 5 V, all other inputs are grounded
B. S_0 through S_3 and M are at 4 5 V, all other inputs are grounded
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C

AC CHARACTERISTICS: T_A = 25 °C

Symbol	Parameter	Limits		Test Conditions	Units
		Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay, (C_n to C_{n+4})	18 13	27 20	M = 0V, (Sum or Diff Mode) See Figure 1 and Tables I and II	ns
t_{PLH} t_{PHL}	Propagation Delay, (Cn to $\overline{F}$ output)	17 13	26 20	M = 0V, (Sum Mode) See Figure 1 and Table I	ns
t_{PLH} t_{PHL}	Propagation Delay, ($\overline{A}$ or $\overline{B}$ Inputs to $\overline{G}$ Outputs)	19 15	29 23	M = S_1 = S_2 = 0V, S_0 = S_3 = 4.5 V (Sum Mode) See Figure 1 and Table I	ns
t_{PLH} t_{PHL}	Propagation Delay, ($\overline{A}$ or $\overline{B}$ Inputs to $\overline{G}$ Outputs)	21 21	32 32	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5 V (Diff Mode) See Figure 2 and Table II	ns
t_{PLH} t_{PHL}	Propagation Delay, ($\overline{A}$ or $\overline{B}$ Inputs to $\overline{P}$ Outputs)	20 20	30 30	M = S_1 = S_2 = 0V, S_0 = S_3 = 4.5 V (Sum Mode) See Figure 1 and Table I	ns
t_{PLH} t_{PHL}	Propagation Delay, ($\overline{A}$ or $\overline{B}$ Inputs to $\overline{P}$ Outputs)	20 22	30 33	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5 V (Diff Mode) See Figure 2 and Table II	ns
t_{PLH} t_{PHL}	Propagation Delay, ($\overline{A}$ or $\overline{B}$ Inputs to any $\overline{F}$ Outputs)	21 13	32 20	M = S_1 = S_2 = 0V, S_0 = S_3 = 4.5 V (Sum Mode) See Figure 1 and Table I	ns
t_{PLH} t_{PHL}	Propagation Delay, ($\overline{A}$ or $\overline{B}$ Inputs to any $\overline{F}$ Outputs)	21 21	32 32	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5 V (Diff Mode) See Figure 2 and Table II	ns
t_{PLH} t_{PHL}	Propagation Delay, ($\overline{A}$ or $\overline{B}$ Inputs to any $\overline{F}$ Outputs)	22 6	32 38	M = 0V, (Logic Mode) See Figure 1 and Table III	ns
t_{PLH} t_{PHL}	Propagation Delay, ($\overline{A}$ or $\overline{B}$ Inputs to C_{n+4} Outputs)	25 25	38 38	M = S_1 = S_2 = 0V, S_0 = S_3 = 4.5 V (Sum Mode) See Figure 3 and Table I	ns
t_{PLH} t_{PHL}	Propagation Delay, ($\overline{A}$ or $\overline{B}$ Inputs to C_{n+4} Outputs)	27 27	41 41	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5 V (Diff Mode)	ns
t_{PLH} t_{PHL}	Propagation Delay, ($\overline{A}$ or $\overline{B}$ Inputs to A = B Outputs)	33 41	50 62	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5 V (Diff Mode) See Figure 2 and Table II	ns

AC WAVEFORMS

Figure 1

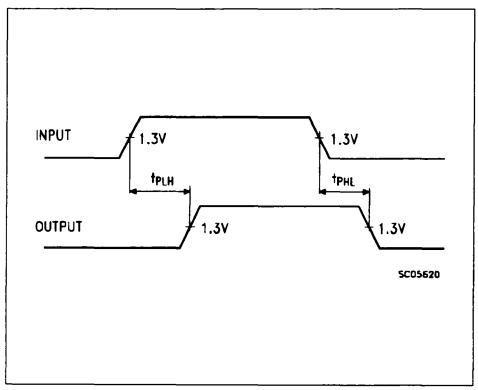


Figure 2

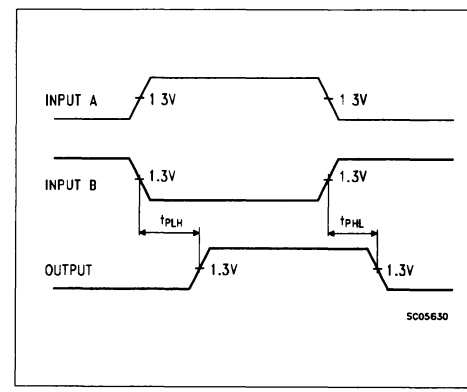
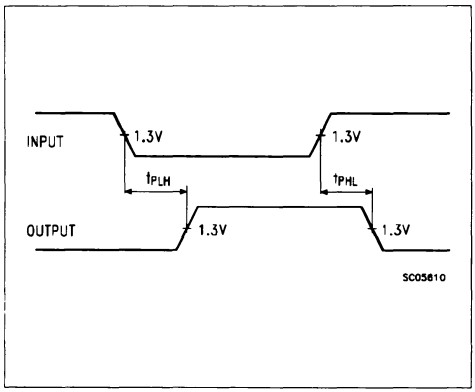


Figure 3



SUM MODE TEST TABLE I: $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = M = 0$V

Parameter	Input Under Test	OTER INPUT SAME BIT		OTHER DATA INPUTS		Output Under Test
		APPLY 4.5V	APPLY GND	APPLY 4.5V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}_I$	$\overline{B}_I$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_I$
t_{PLH} t_{PHL}	$\overline{B}_I$	$\overline{A}_I$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_I$
t_{PLH} t_{PHL}	$\overline{A}_I$	$\overline{B}_I$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	F_{I+1}
t_{PLH} t_{PHL}	$\overline{B}_I$	$\overline{A}_I$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	F_{I+1}
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	P
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	Cn+4
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	Cn+4
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

DIFF MODE TEST TABLE II: $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = M = 0$V

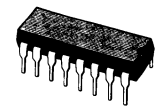
Parameter	Input Under Test	OTER INPUT SAME BIT		OTHER DATA INPUTS		Output Under Test
		APPLY 4.5V	APPLY GND	APPLY 4.5V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_I$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_I$
t_{PLH} t_{PHL}	$\overline{A}_I$	None	$\overline{B}_I$	Remaining B, C_n	Remaining $\overline{A}$	F_{I+1}
t_{PLH} t_{PHL}	$\overline{B}_I$	$\overline{A}_I$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	F_{I+1}
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	P
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Cn+4
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Cn+4
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4}

LOGIC MODE TEST TABLE III: $S_1 = S_2 = M = 4.5$ V, $S_0 = S_3 = 0$V

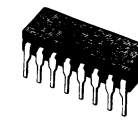
Parameter	Input Under Test	OTER INPUT SAME BIT		OTHER DATA INPUTS		Output Under Test
		APPLY 4.5V	APPLY GND	APPLY 4.5V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_I$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_I$

LS190 - PRESETTABLE BCD/DECADE UP/DOWN COUNTERS
LS191 - PRESETTABLE 4-BIT BINARY UP/DOWN COUNTERS

- LOW POWER 90 mW TYPICAL DISSIPATION
- SYNCHRONOUS COUNTING
- INDIVIDUAL PRESET INPUTS
- CASCADABLE
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- HIGH SPEED 35 MHz TYPICAL COUNT FREQUENCY
- ASYNCHRONOUS PARALLEL LOAD
- COUNT ENABLE AND UP/DOWN CONTROL INPUT
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

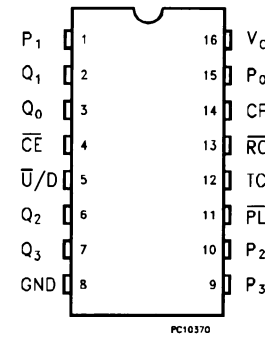
C1
(Plastic Chip Carrier)

ORDER CODES :

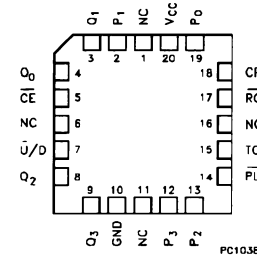
T74LSXXX D1	T74LSXXX C1
T74LSXXX B1	T74LSXXX M1

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

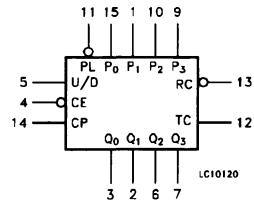
DESCRIPTION

The T74LS190 is a synchronous UP/DOWN BCD Decade (8421) Counter and the T74LS191 is a synchronous UP/DOWN Modulo-16 Binary Counter. State changes of the counters are synchronous with the LOW to HIGH transition of the Clock Pulse input.

An asynchronous Parallel Load ($\overline{PL}$) input overrides counting and loads the data present on the P_n inputs into the flip-flops, which makes it possible to use the circuits as programmable counters.

A Count Enable ($\overline{CE}$) input serves as the carry/borrow input in multi-stage counters. An Up/Down Count Control ($\overline{U}/D$) input determines whether a circuit count up or down. A Terminal Count (TC) output and a Ripple Clock ($\overline{RC}$) output provide overflow/underflow indication and make possible a variety of methods for generating carry/borrow signal in multi-stage counter applications.

LOGIC SYMBOL AND STATE DIAGRAM



LS190

UP : $TC = \overline{Q_0 \bullet Q_3 \bullet (\overline{U/D})}$

DOWN : $TC = \overline{Q_0} \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet \overline{Q_3} \ (\overline{U/D})$

LS191

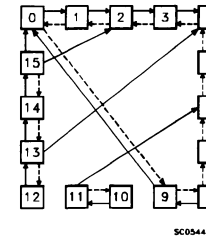
UP : $TC = \overline{Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet (\overline{U/D})}$

DOWN : $TC = \overline{Q_0} \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet \overline{Q_3} \ (U/D)$

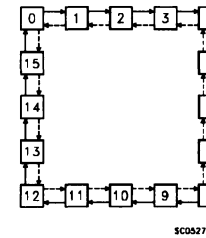
COUNT UP ⟶

COUNT DOWN ⟶

LS190



LS191



MODE SELECT TABLE

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U/D}$	CP	
H	L	L	⎍	Count Up
H	L	H	⎍	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

RC TRUTH TABLE

INPUTS			$\overline{RC}$ OUTPUT
$\overline{CE}$	TC *	CP	
L	H	⎍⎍	⎍⎍
H	X	X	H
X	L	X	H

* TC is generated internally

L = LOW Voltage Level, H = HIGH Voltage Level, X = Don't Care, ⎍ = LOW to HIGH transition. ⎍⎍ = LOW Pulse

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	0 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

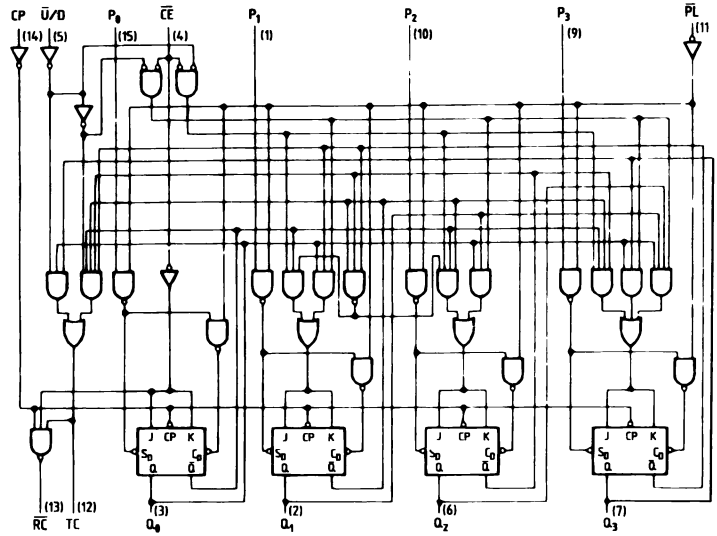
Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

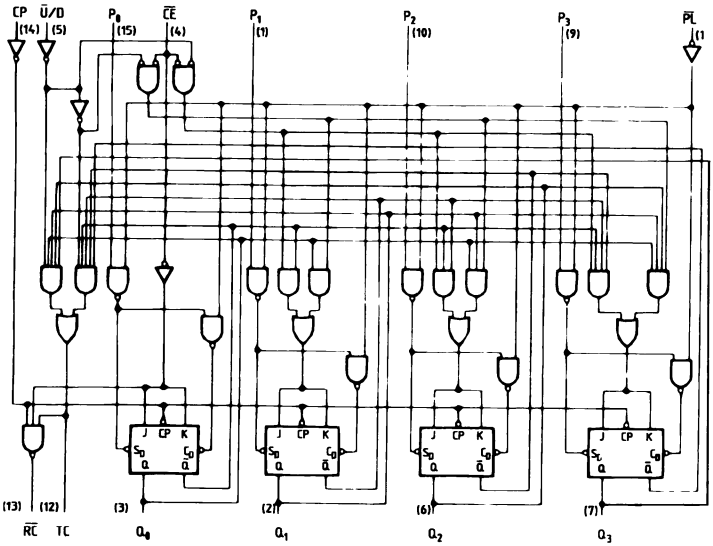
Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS190/191XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

LOGIC DIAGRAMS

DECADE COUNTER
LS190



BINARY COUNTER
LS191



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

FUNCTIONAL DESCRIPTION

The LS190 is a synchronous Up/Down BCD Decade Counter and the LS191 is a synchronous Up/Down 4-Bit Binary Counter. The operating modes of the LS190 decade counter and the LS191binary counterare identical, with the only difference being the count sequences as noted in the state diagrams. Each circuit contains four master slave flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has a n asynchronous parallel loas capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Data inputs (P_0-P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{CE}$ input inhibit counting. When $\overline{CE}$ is LOW, internal state changes are initiaded synchronously by thee LOW to HIGH transition of the clock input.. The direction of counting is determined by the U/D input signal, as indicate in the Mode Select Table. When counting is to be enabled, the $\overline{CE}$ signal can be made LOW when the clock is in either state.

However, when counting is to be inhibited, the LOW to HIGH $\overline{CE}$ transition must occur only while the clock is HIGH. Similary, the U/D signal should only be changed when either $\overline{CE}$ or the clock is HIGH.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or raches maximum (9 for LS190, 15 for the LS191) in the count-up mode. The TC output will then remain HIGH until a stage changeoccurs, wheter by counting or presetting or until U/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to be enable the Rpple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, the $\overline{RC}$ output will go LOW when the clock next goes HIGH again. This feature simplifies the design of multistage counters, as indicated in Figures a and b. In Figure a, each $\overline{RC}$ output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage,since a HIGH signals on $\overline{CE}$ inhibit the $\overline{RC}$ output pulse, as indicated in the $\overline{RC}$ Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages.

This represent the cumulative delay of the clock as it ripples through the preceding stages. A method of causing state changes to occur simultaneously in all stages is shown in Figure b. All Clock inputs are driven in parallel and the RC output propagate the carry/borrow signals ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative going edge of the of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{RC}$ output of any package goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure c avoids ripple delays and their associated restrictions. The $\overline{CE}$ input signal for a given stage is formad by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figure a and b doesn't apply, because the TC output of a given stage is not affect by its own $\overline{CE}$.

Fig. a: n-stage counter using ripple clock

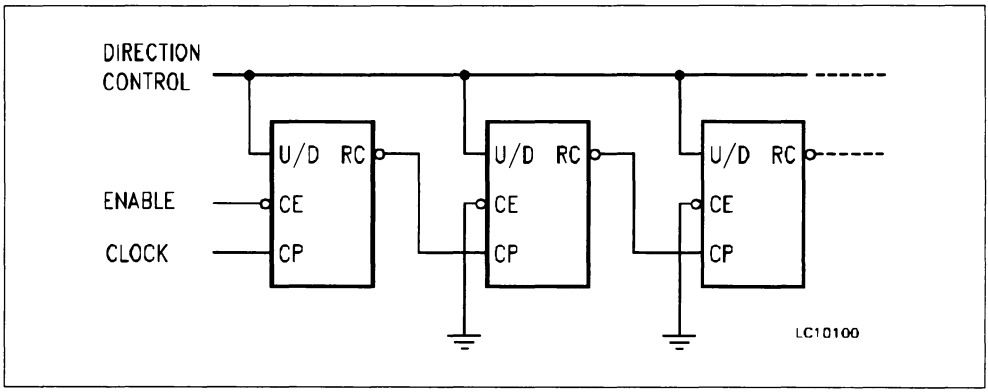


Fig.b: Synchronous n-stage counter using ripple carry/borrow

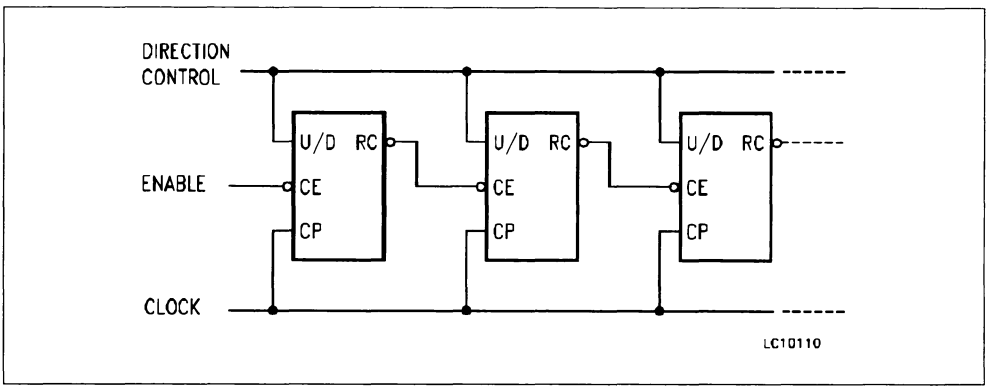
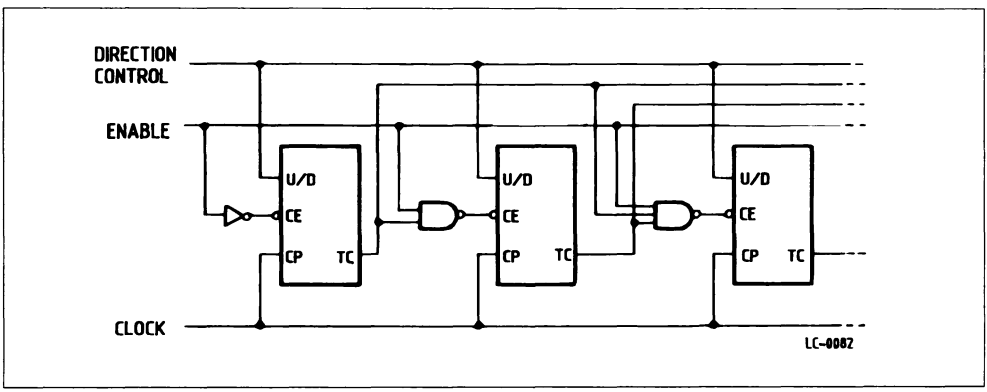


Fig. c: Synchronous n-stage counter with parallel gated carry/borrow



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current $\overline{P_0}$, $\overline{PL}$, CP, $\overline{U/D}$ $\overline{CE}$			 20 60	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	$\overline{P_0}$, $\overline{PL}$, CP, $\overline{U/D}$ $\overline{CE}$			0 1 0.3	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current $\overline{P_0}$, $\overline{PL}$, CP, $\overline{U/D}$ $\overline{CE}$			 - 0.4 - 1.08	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		20	35	V_{CC} = MAX, All Inputs 0V		mA

Notes : 1 For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Note more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C

AC CHARACTERISTICS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
f_{MAX}	Max Input Count Frequency	20	25		Figures 1	V_{CC} = 5.0 V C_L = 15 pF	MHz
t_{PLH} t_{PHL}	Propagation Delay, CP Input to Q Outputs		16 24	24 36	Figures 1		ns
t_{PLH} t_{PHL}	Propagation Delay, CP Input to $\overline{RC}$ Outputs		13 16	20 24	Figures 2		ns
t_{PLH} t_{PHL}	Propagation Delay, CP Input to TC Outputs		28 37	42 52	Figures 1		ns
t_{PLH} * t_{PHL} *	Propagation Delay, $\overline{U/D}$ Input to $\overline{RC}$ Outputs		30 30	45 45	Figures 7		ns
t_{PLH} t_{PHL} *	Propagation Delay, $\overline{U/D}$ Input to TC Outputs		21 22	33 33	Figures 7		ns
t_{PLH} t_{PHL}	Propagation Delay, P0-P_3 Inputs to Q_0-Q_3 Outputs		20 27	32 40	Figures 3		ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{PL}$ Input to Any Output		22 33	33 50	Figures 4		ns
t_{PLH} * t_{PHL}	Propagation Delay, $\overline{CE}$ Input to $\overline{RC}$ Output		21 22	33 33	Figures 2		ns

* It is possible to get these timing relationnship, but they should not occur during normal operation since the CP would be HIGH.

AC SET-UP REQUIREMENTS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_w	CP Pulse Width	25			Figure 1	V_{CC} = 5.0 V	ns
t_w	PL Pulse Width	35			Figure 4		ns
t_sL	Set-Up Time LOW, Data to PL	30					ns
t_hL	Hold Time LOW, Data to PL	5			Figure 6		ns
t_sH	Set-Up Time HIGH, Data to PL	30					ns
t_hH	Hold Time HIGH, Data to PL	5					ns
t_{rec}	Recovery Time, PL to CP	40			Figure 5		ns
t_sL	Set-Up Time LOW, CE to Clock	30			Figure 8		ns
t_hL	Hold Time LOW, CE to Clock	5					ns

DEFINITION OF TERMS:

SET-UP TIME (t_s): is defined as the minimum time required for the corret logic level to be present at the logic input prior the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h): is defined as the minimum time following the clock transition from LOW to HIGH at which the logiclevel must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be relased prior to the clock transitio from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) : is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORM

Fig 1.

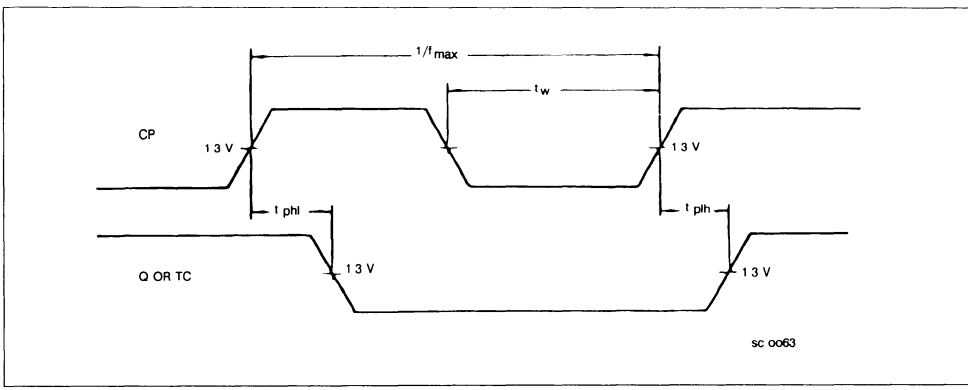


Fig 2.

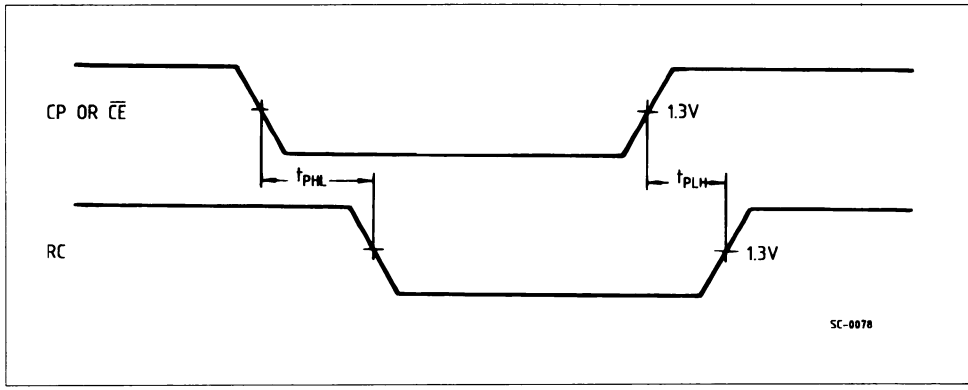


Fig 3.

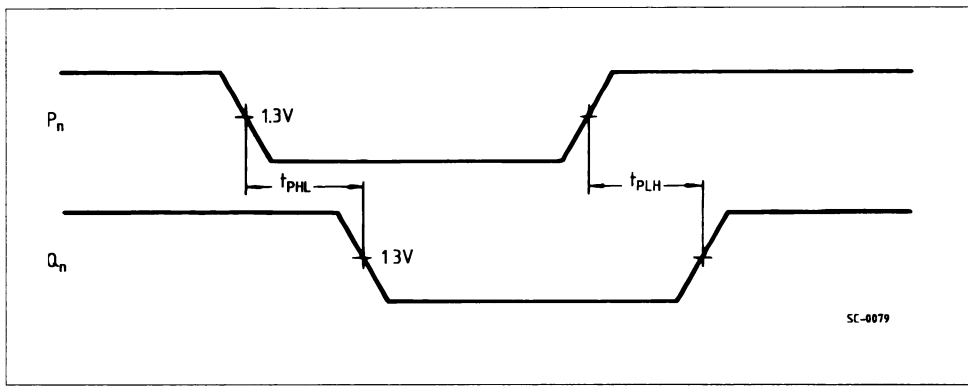


Fig 4.

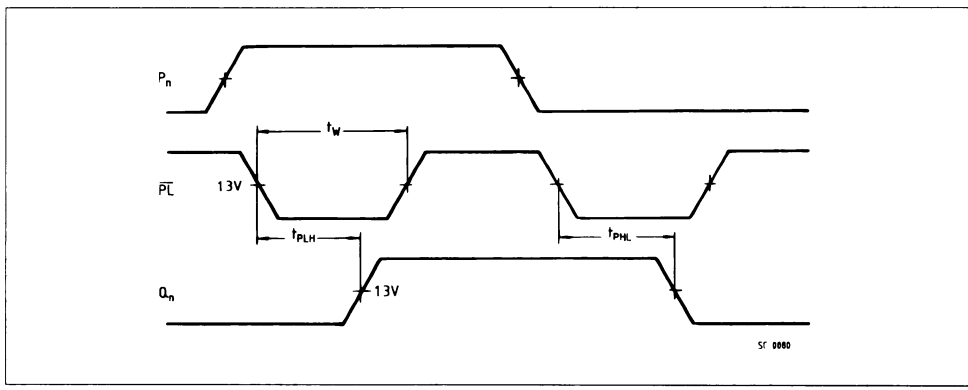


Fig 5.

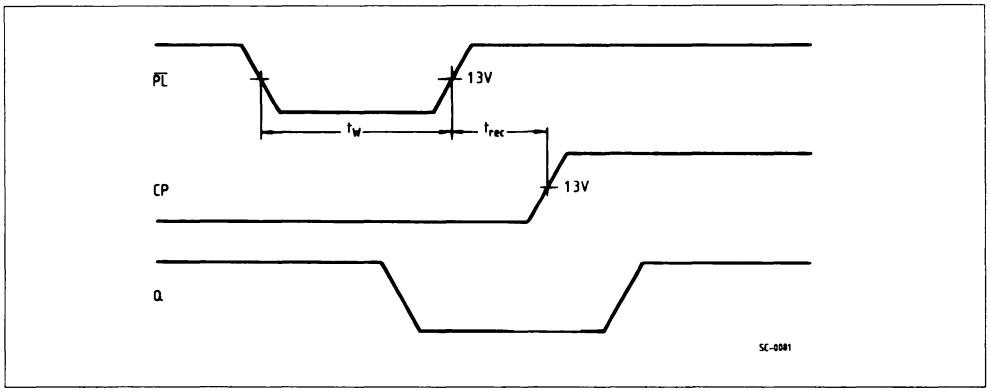
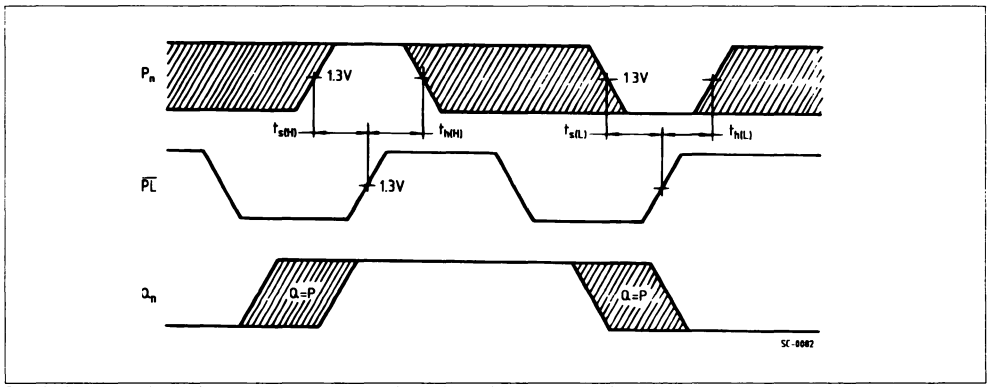


Fig 6.



The shaded areas indicate when the input is permitted to change for predictable output performance

Fig 7.

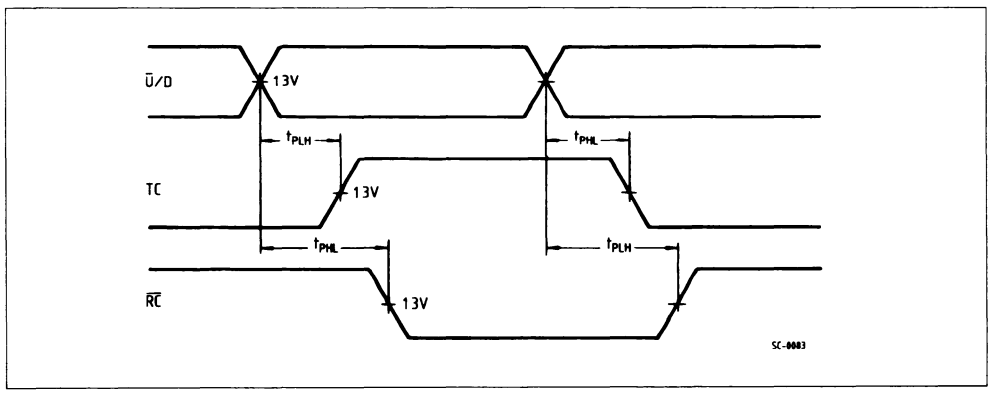
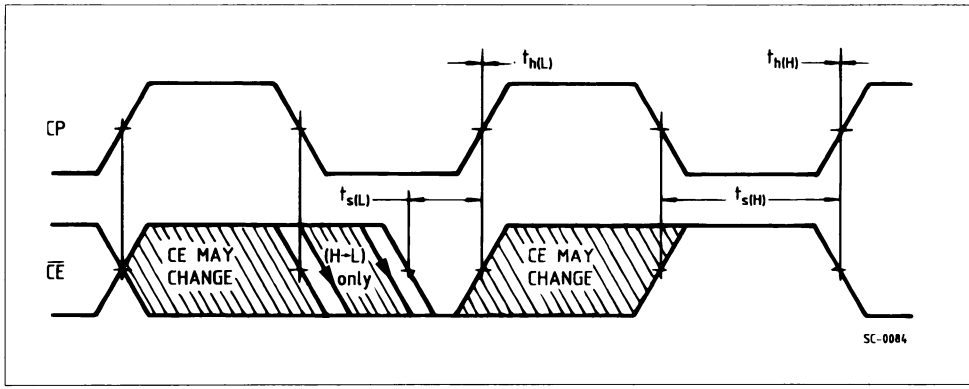


Fig 8.

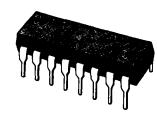

CP
$\overline{CE}$
$t_{h(L)}$
$t_{h(H)}$
$t_{s(L)}$
$t_{s(H)}$
CE MAY CHANGE
(H-L) only
CE MAY CHANGE
SC-0084

SGS-THOMSON MICROELECTRONICS

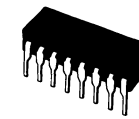
T74LS192
T74LS193

LS192 - PRESETTABLE BCD/DECADE UP/DOWN COUNTERS
LS193 - PRESETTABLE 4-BIT BINARY UP/DOWN COUNTERS

- LOW POWER 95 mW TYPICAL DISSIPATION
- SYNCHRONOUS COUNTING
- CASCADING CIRCUITRY INTERNALLY PROVIDED
- ASYNCHRONOUS MASTER RESET AND PARALLEL LOAD
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- HIGH SPEED 40 MHz TYPICAL COUNT FREQUENCY
- INDIVIDUAL PRESET INPUTS
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LSXXX D1 T74LSXXX C1
T74LSXXX B1 T74LSXXX M1

DESCRIPTION

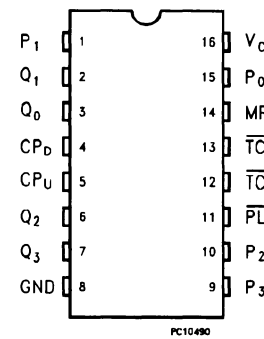
The T74LS192 is a synchronous UP/DOWN BCD Decade (8421) Counter and the T74LS193 is a synchronous UP/DOWN Modulo-16 Binary Counter. Separate Count Down Clocks are used as in eithes counting mode the circuits operate synchronously. The ouputs change state synchronous with the LOW to HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clock for subsequent stages without extra logic, thus simplifying multistage counter designs.

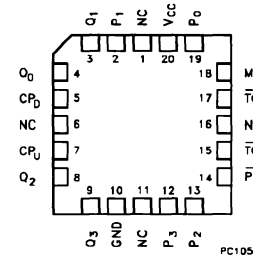
Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load ($\overline{PL}$) and the Master Reset inputs asynchronously override the clock.

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER

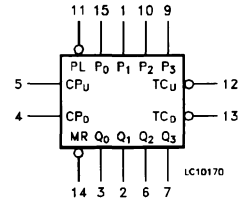


NC = No Internal Connection

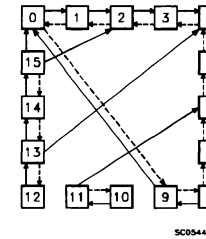
PIN NAMES

CP_U	Count Up Clock Pulse Input
CP_D	Count Down Clock Pulse Input
MR	Asynchronous Master Reset (Clear) Input
$\overline{PL}$	Asynchronous Parallel Load (Active LOW) Input
P_n	Parallel Data Inputs
Q_n	Flip-flop Outputs
$\overline{TC}_D$	Terminal Count Down (Borrow) Output
$\overline{TC}_U$	Terminal Count Up (Carry) Output

LOGIC SYMBOL AND STATE DIAGRAM



LS192



LS192

UP : $\overline{TC_U} = \overline{Q_0} \bullet \overline{Q_3} \bullet \overline{CP_U}$ ___

DOWN : = $\overline{Q_0} \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet \overline{Q_3} \bullet \overline{CP_D}$

LS193

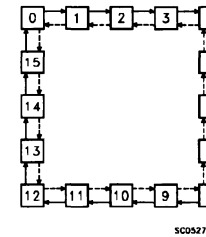
UP : $\overline{TC_U} = \overline{Q_0} \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet \overline{Q_3} \bullet \overline{CP_U}$

DOWN : $\overline{TC_D} = \overline{Q_0} \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet \overline{Q_3} \bullet \overline{CP_U}$

COUNT UP ⟶

COUNT DOWN ⟶

LS193



MODE SELECT TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asynchronous)
L	L	X	X	Preset (Asynchronous)
L	H	H	H	No Change
L	H	⌐	H	Count Up
L	H	H	⌐	Count Down

L = LOW Voltage Level, H = HIGH Voltage Level, X = Don't Care, ⌐ = LOW to HIGH transition.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	0 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

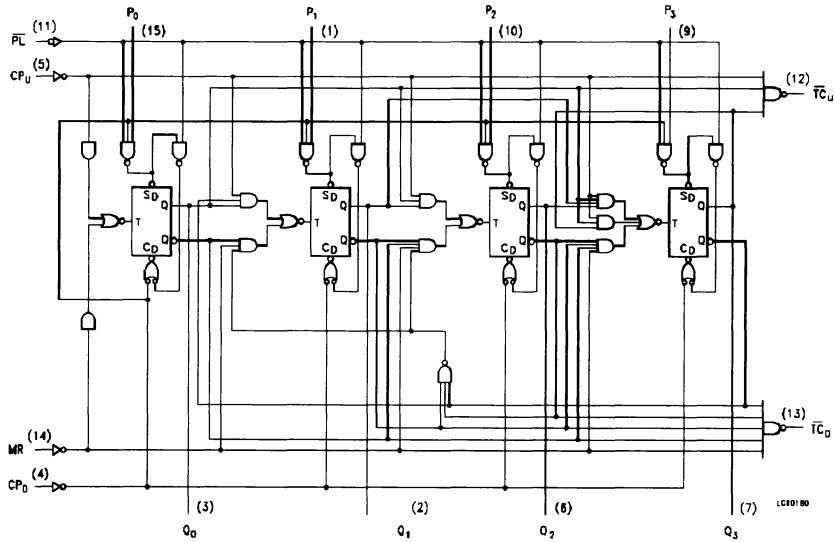
Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

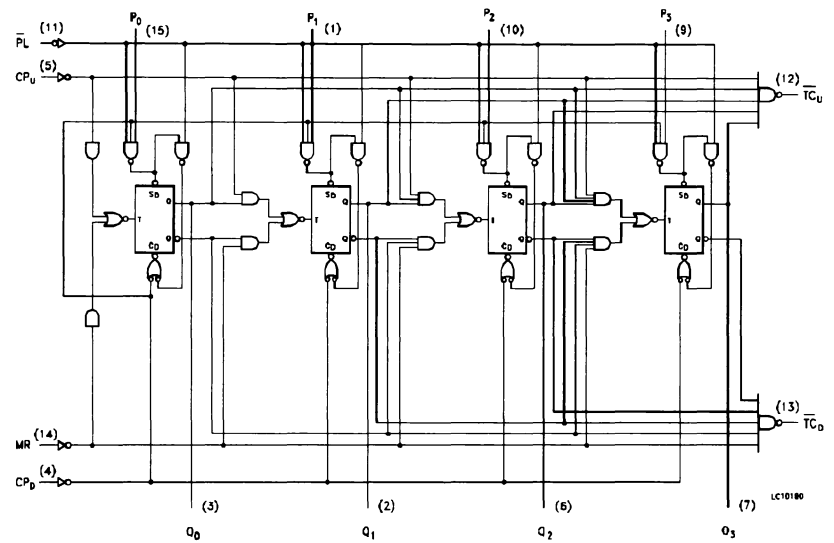
Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS192/193XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

LOGIC DIAGRAMS

DECADE COUNTER
LS192



BINARY COUNTER
LS193



FUNCTIONAL DESCRIPTION

The LS192 and LS193 are Asynchronously Presettable Decade and 4-Bit Binary Synchronous Up/DOWN (Reversable) Counter. The operating modes of the LS192 decade counter and the LS193 binary counterare identica, with the only difference being the count sequences as noted in the state diagrams. Each circuit contains four master slave flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each flip-flop contains JK feedback from slave to master such that a LOW to HIGH transition on its T input causes the slave, and thus the Q output to change state. Synchronous switching, as opposed to ripple counting, is achived by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW to HIGH transition on the Count-Up input will advance the count by one; asimilar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit, will either count by two or not at all, depending of the state of the first flip-flop, chich can not toggle as long as either Clock input is LOW. The Terminal Count Up ($\overline{TC_U}$) and Terminal Count Down ($\overline{TC_D}$) outputs are normally HIGH. When a circuit has reached the maximum count state (9 for the LS192, 5 for the LS193), the next HIGH to LOW transition of the Count Up Clock will cause $\overline{TC_U}$ to go LOW. $\overline{TC_U}$ will stay LOW until CPU goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays.

Similary, the $\overline{TC_D}$ output will go to LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the TC outputs repeat the clock waveforms, they can be used as the clock input signals to hte next higher order circuit in a multistage counter.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset.

When the Parallel Load ($\overline{PL}$) and the Master Resert (MR) inputs are LOW, information present on the Parallel Data inputs (P_0, P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the present gates, override both Clock inputs, and latch each Q output in the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW to HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		19	34	V_{CC} = MAX		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Note more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
f_{MAX}	Max Input Count Frequency	25	32		Figures 1	V_{CC} = 5.0 V C_L = 15 pF	MHz
t_{PLH} t_{PHL}	Propagation Delay, CP_U Input to $\overline{TC}_U$ Outputs		17 18	26 24	Figures 2		ns
t_{PLH} t_{PHL}	Propagation Delay, CPD Input to $\overline{TC}_D$ Outputs		16 15	24 24			ns
t_{PLH} t_{PHL}	Propagation Delay, CP_U or CP_D to Q_n Outputs		17 30	38 47			ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{PL}$ Inputs to Any Outputs		24 25	40 40	Figures 4		ns
t_{PHL}	Propagation Delay, MR Inputs to Any Outputs		23	35	Figures 7		ns

* It is possible to get these timing relationnship, but they should not occur during normal operation since the CP would be HIGH.

AC SET-UP REQUIREMENTS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_W	CP_U Pulse Width	20			Figure 1	V_{CC} = 5.0 V	ns
t_W	PL_D Pulse Width	20					ns
t_W	$\overline{PL}$ Pulse Width	20			Figure 4		ns
t_W	MR Pulse Width	20					ns
t_sL	Set-Up Time LOW, Data to $\overline{PL}$	20			Figure 6		ns
t_hL	Hold Time LOW, Data to $\overline{PL}$	5					ns
t_sH	Set-Up Time HIGH, Data to $\overline{PL}$	20					ns
t_hH	Hold Time HIGH, Data to $\overline{PL}$	5					ns
t_{rec}	Recovery Time	40			Figure 5		ns

DEFINITION OF TERMS:

SET-UP TIME (t_s): is defined as the minimum time required for the corret logic level to be present at the logic input prior the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h): is defined as the minimum time following the clock transition from LOW to HIGH at which the logiclevel must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be relased prior to the clock transitio from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) : is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORM

Fig 1.

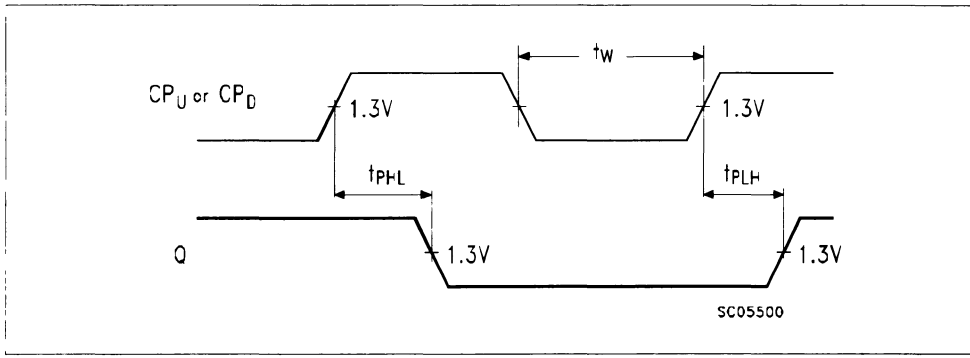


Fig 2.

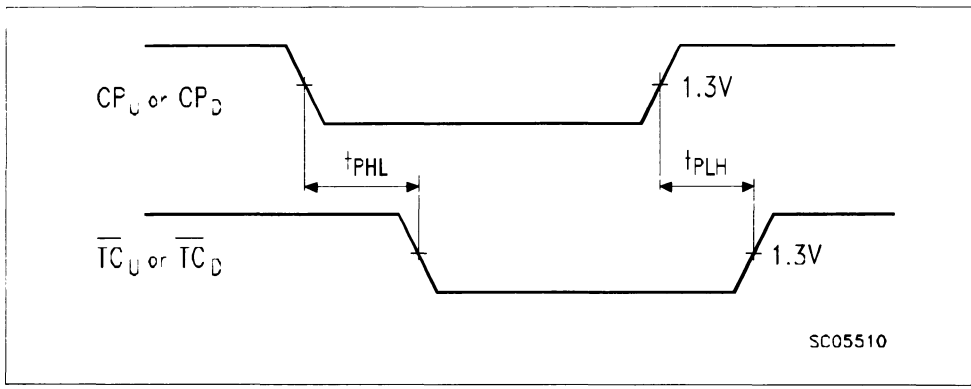


Fig 3.

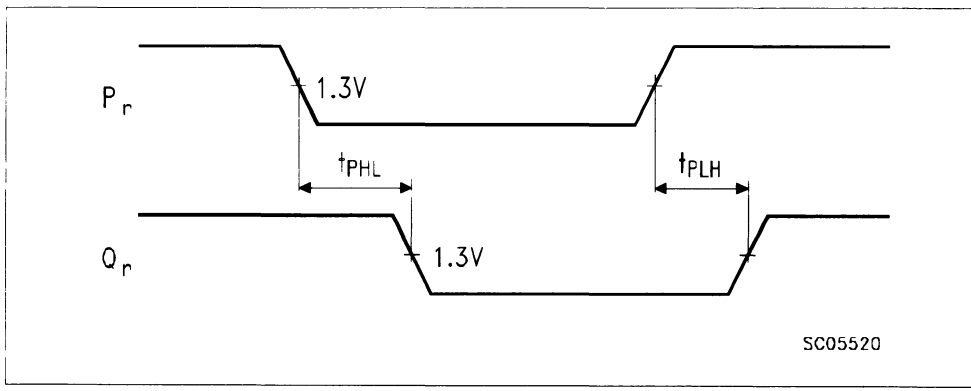


Fig 4.

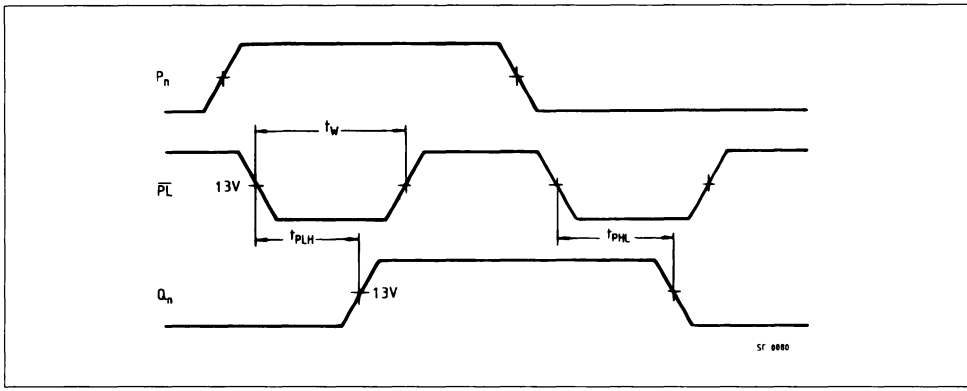


Fig 5.

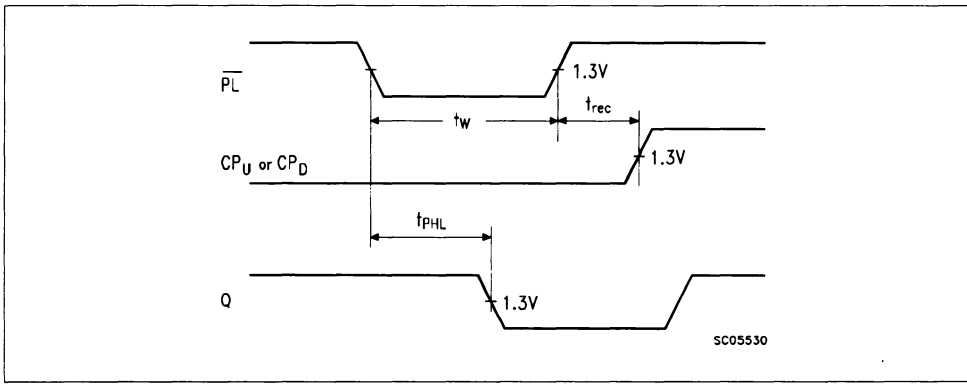


Fig 6.

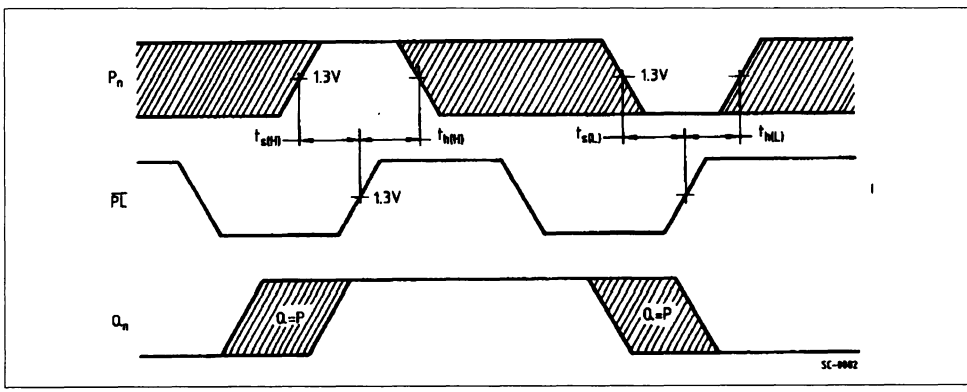
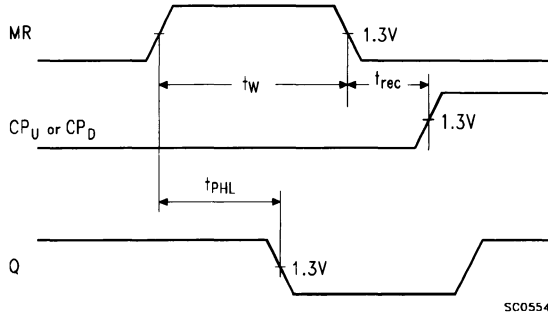
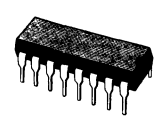


Fig 7.

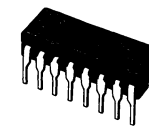


UNIVERSAL 4-BIT SHIFT REGISTER

- TYPICAL SHIFT REGISTER FREQUENCY OF 40 MHz
- ASYNCHRONOUS MASTER RESET
- HOLD (DO NOTHING) MODE
- FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

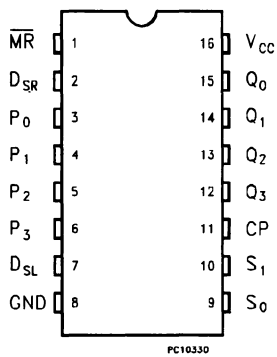
T74LS194A D1	T74LS194A C1
T74LS194A B1	T74LS194A M1

DESCRIPTION

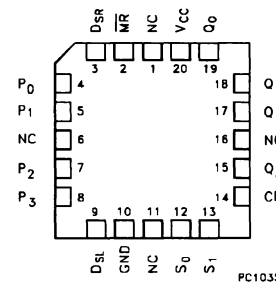
The T74LS194A is a High Speed Bidirectional Universal Shift Register. As a hgih spped multifuntional sequential bulding block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial and parallel-parallel data register transfers. The LS194A is similar in operation to be LS195 Universal Shift Register, with added features of shift left without external connections and hold (do nothing) modes of operation. It utilizes the Schottky diode clamped process to achieve high speed and is fully compatible with allTTL families.

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER

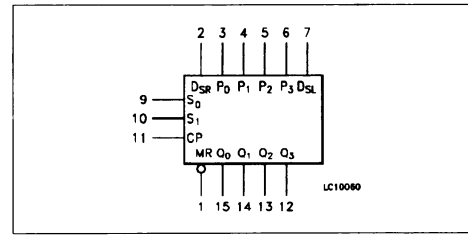


NC = No Internal Connection

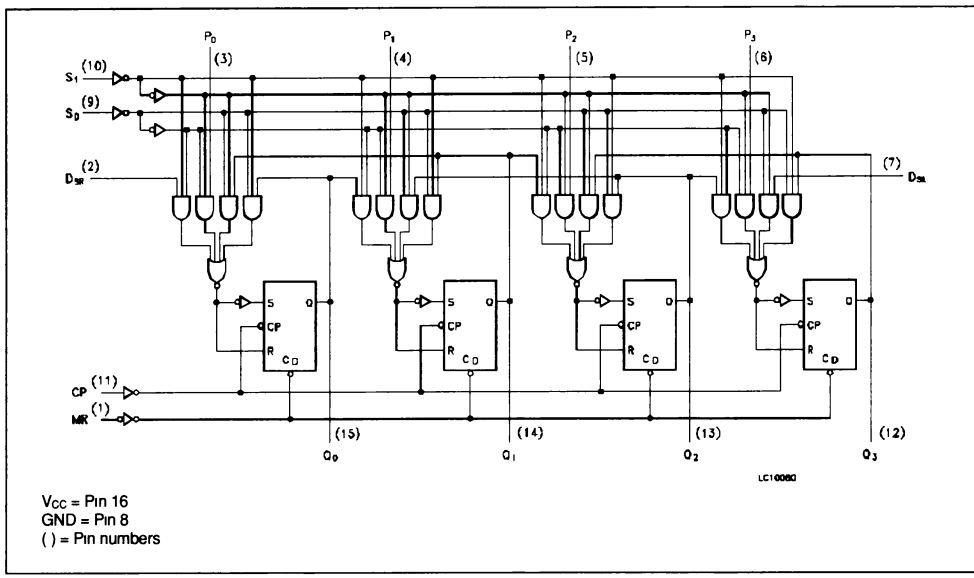
PIN NAMES

S_0-S_3	Mode Control to Input
P_0-P_3	Parallel Data Inputs
D_{SR}	Serial (Shift Right) Data Input
D_{SL}	Serial (Shift Left) Data Input
CP	Clock (Active HIGH Going Edge) Input
$\overline{MR}$	Master Reset (Active LOW) Input
Q_0-Q_3	Parallel Outputs

LOGIC SYMBOL



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

TRUTH TABLE

OPERATING MODE	INPUTS						OUTPUTS			
	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	P_n	Q_0	Q_1	Q_2	Q_3
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	q_0	q1	q_2	q3
Shift Left	H	h	l	X	l	X	q_1	q2	q3	L
	H	h	l	X	h	X	q_1	q_2	q_3	H
Shift Right	H	l	h	l	X	X	L	q_0	q_1	q_2
	H	l	h	h	X	X	H	q_0	q_1	q_2
Paralled Load	H	h	h	X	X	P_n	P_0	P_1	P_2	P_3

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition
h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition
Pn (qn) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

FUNCTIONAL DESCRIPTION

The Logic Diagram and Truth Table indicate the functional characteristics of the LS194A 4-Bit Bidirectional Shift Register. The LS194A is similar in operation to the LS195A Universal Shift Register when used in serial or parallel data register transfers. Some of the common features of the two devices are described below:

1) All data and mode control inputs are edge-triggered, responding only to the LOW to HIGH transition of the clock (CP). The only timing restriction, therefore, is that the mode control and selected data inputs must be stable one set-up time prior to the positive transition of the clock pulse.
2) The register is fully synchronous, with all operations taking place in less than 15 ns (typical) making the device especially useful for implementing very high speed CPUs, or the memory buffer registers.
3) The four parallel data inputs (P_0, P_1, P_2, P_3) are D-type inputs. When both S_0 and S_1 are HIGH, the data appearing on P_0, P_1, P_2 and P_3 inputs is transferred to the Q_0, Q_1, Q_2 and Q_3 outputs respectively following the next LOW to HIGH transition of the clock.
4) The asynchronous Master Reset ($\overline{MR}$), when LOW, overrides all other input conditions and forces the Q outputs LOW.

Special logic features of the LS194A design which increase the range of application are described below:

1) Two mode control inputs (S_0, S_1) determine the synchronous operation of he devices. As shown in the Mode Selection Table, data can be entered and shifted from left to righ (shift right, Q_0 -> Q_1, etc.) or right to left (shift left, Q_3 -> Q_2, etc.), or parallel data can be entered loading all four bits of the register simultaneously. When both S_0 and S_1 are LOW, the existing data is retained in a "do nothing" mode without restricting the HIGH to LOW clock transition.
2) D-type serial data inputs (D_{SR}, D_{SL}) are provided on both the first and last stages to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	- 0.5 to 7	V
V_I	Input Voltage, Applied to Input	- 0.5 to 15	V
V_O	Output Voltage, Applied to Output	- 0.5 to 10	V
I_I	Input Current, Into Inputs	- 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS194AXX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Input		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Input		V
V_{CD}	Input Clamp Diode Voltage		- 0 65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		15	23	V_{CC} = MAX		mA

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C

AC CHARACTERISTICS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
f_{MAX}	Shift Frequency	25	36		Figures 1	V_{CC} = 5.0 V C_L = 15 pF	MHz
t_{PLH} t_{PHL}	Propagation Delay, Clock to Outputs		14 17	22 26	Figures 1		ns
t_{PHL}	Propagation Delay, MR to Outputs		19	30	Figures 2		ns

AC SET-UP REQUIREMENTS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_WCP	Clock Pulse Width	20			Figure 1	V_{CC} = 5.0 V	ns
t_s(Data)	Set-Up Time Data to Clock	20			Figure 3		ns
t_h(Data)	Hold Time Data to Clock	0					ns
t_s(S)	Set-Up Time Mode Control to Clock	30			Figure 4		ns
t_h(S)	Hold Time Mode Control to Clock	0					ns
$t_w(\overline{MR})$	Master Reset Pulse Width	20			Figure 2		ns
$t_{rec}(\overline{MR})$	Recovery Time Mater Reset to Clock	25					ns

DEFINITION OF TERMS:

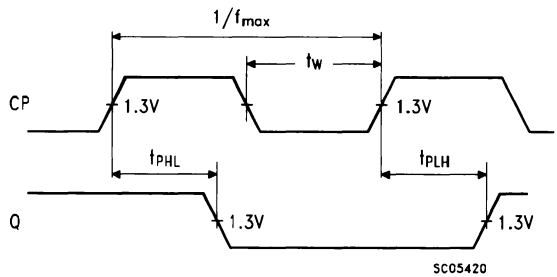
SET-UP TIME (t_s): is defined as the minimum time required for the corret logic level to be present at the logic input prior the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h): is defined as the minimum time following the clock transition from LOW to HIGH at which the logiclevel must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be relased prior to the clock transitio from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) : is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

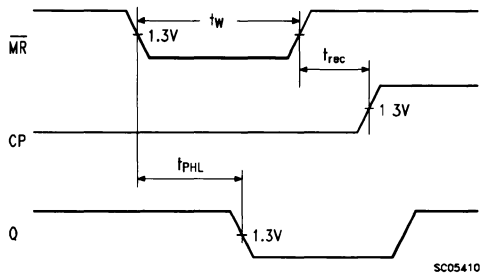
AC WAVEFORMS

Figure 1: Clock to Output Delays Clock Pulse Width and f_{max}



Other Conditions: S_1 = L, $\overline{MR}$ = H , S_0 = $\overline{K}$

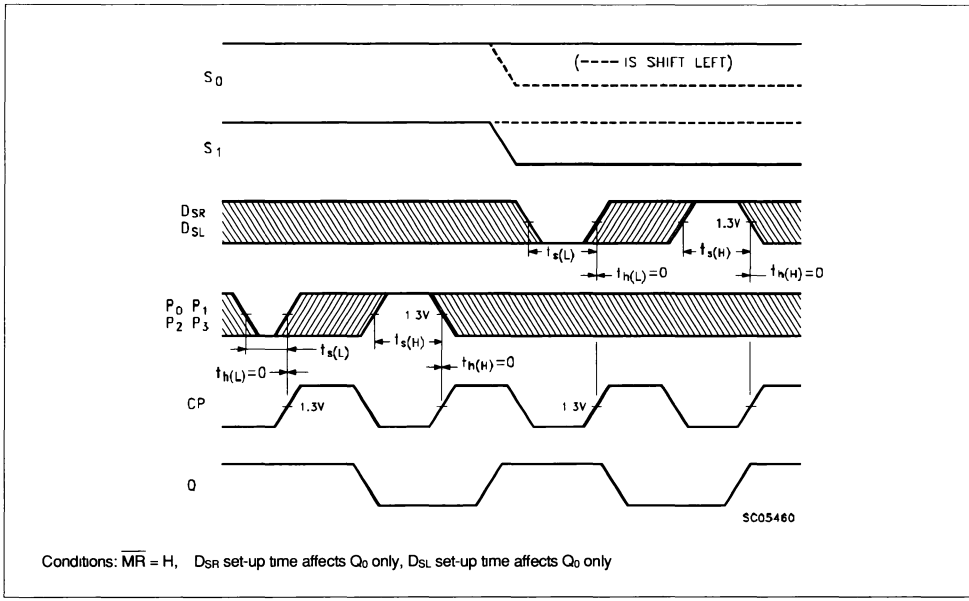
Figure 2: Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Other Conditions: S_0, S_1 = H, P_0 = P_1 = P_2 = P_3 = H

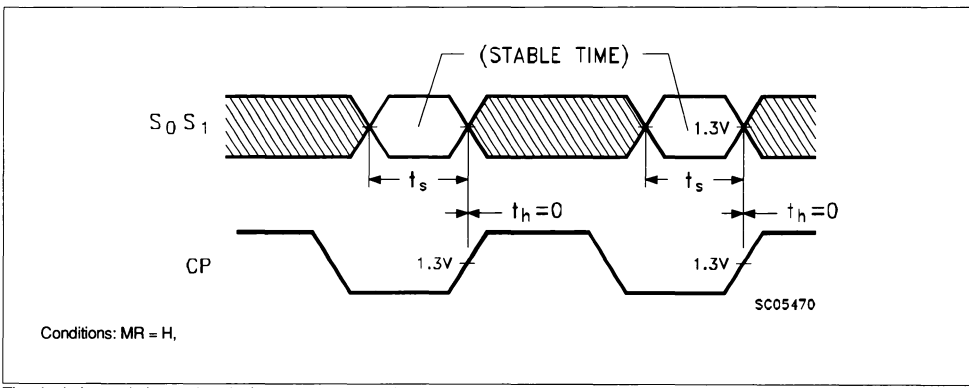
The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 3: Set-up (t_s) and Hold (t_h) Time for Serial Data (D_{SR}, D_{SL}) and Parallel Data (P_0, P_1, P_2, P_3)



Conditions: $\overline{MR}$ = H, D_{SR} set-up time affects Q_0 only, D_{SL} set-up time affects Q_0 only

Figure 4: Set-up (t_s) and Hold (t_h) Time for S Input

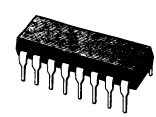


Conditions: MR = H,

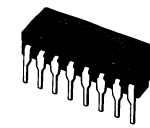
The shaded areas indicate when the input is permitted to change for predictable output performance.

UNIVERSAL 4-BIT SHIFT REGISTER

- TYPICAL SHIFT REGISTER FREQUENCY OF 40 MHz
- ASYNCHRONOUS MASTER RESET
- J, K INPUT TO FIRST STAGE
- FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

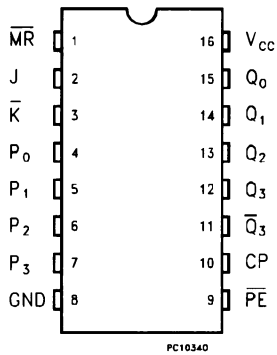
T74LS195A D1	T74LS195A C1
T74LS195A B1	T74LS195A M1

DESCRIPTION

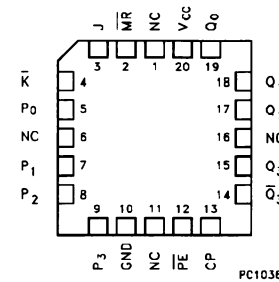
The T74LS194A is a High Speed Bidirectional Universal Shift Register. As a hgih spped multifuntional sequential bulding block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial and parallel-parallel data register transfers.

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER

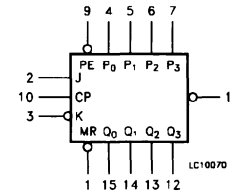


NC = No Internal Connection

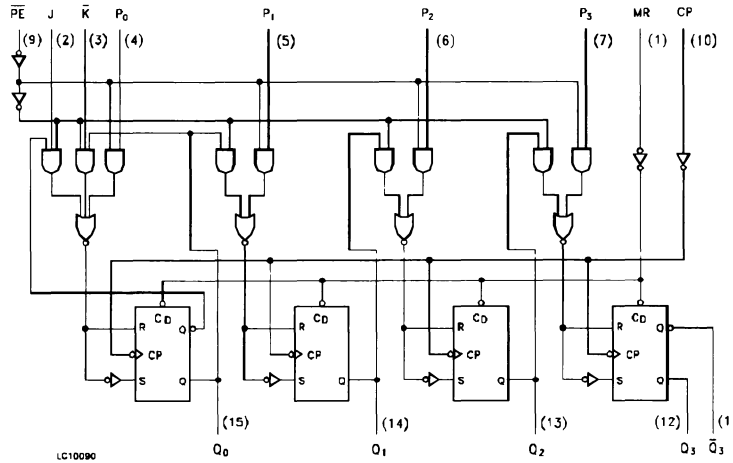
PIN NAMES

$\overline{PE}$	Parallel Enable (Active LOW) Input
P_0-P_3	Parallel Data Inputs
J	First Stage J (Active HIGH) Input
$\overline{K}$	First Stage K (Active LOW) Input
CP	Clock (Active HIGH Going Edge) Input
$\overline{MR}$	Master Reset (Active LOW) Input
Q_0-Q_3	Parallel Outputs
$\overline{Q}_3$	Complementary Last Stage Output

LOGIC SYMBOL



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

TRUTH TABLE

OPERATING	INPUTS					OUTPUTS				
	$\overline{MR}$	$\overline{PE}$	J	$\overline{K}$	P_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Asynchronous Reset	L	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, Reset First Stage	H	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, Toggle First Stage	H	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, Retain First Stage	H	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Paralled Load	H	l	X	X	p_n	p_0	p_1	p_2	p_3	$\overline{p}_3$

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition
h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transitio
Pn (qn) = Lower case letters indicate the state of the reference input (or output) one set-up time prior to the LOW to HIGH clock transition.

FUNCTIONAL DESCRIPTION

The Logic Diagram and Truth Table indicate the functional characteristics of the LS195A Shift register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The LS195A has not two primary modes of operation, shift right (Q_0 -> Q_1) and parallel load which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. When the PE input is HIGH, serial data enters the first flip-flop Q_0 via the J and $\overline{K}$ inputs and is shifted one bit in the direction Q_0 -> Q_1 -> Q_2 -> Q_3 following each LOW to HIGH clock transition. The J $\overline{K}$ inputs provide the flexibility of the J K type input for special applications, are the simple D type input for general applications by tying the two pins togheter. When the $\overline{PE}$ input is LOW, the LS195A appears as four common clocked D flip-flop. The data on the parallel inputs P_0, P_1, P_2, P_3 is transferred to the respective Q_0, Q_1, Q_2, Q_3 outputs to the P_{n-1} inputs and holding the $\overline{PE}$ input LOW. All serial and parallel data transfers are synchronous, occurring after each LOW to HIGH clock transition. Since the LS195A utilizes edge-triggering, there is no restriction on the activity of the J, K, P_n and $\overline{PE}$ inputs for logic operation - except for the set-up and release time requirements.

A LOW on the asynchronous Master Reser ($\overline{MR}$) input sets all Q outputs LOW, independent for any other input condition.

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	- 0.5 to 7	V
V_I	Input Voltage, Applied to Input	- 0.5 to 15	V
V_O	Output Voltage, Applied to Output	- 0.5 to 10	V
I_I	Input Current, Into Inputs	- 30 to 5	mA
I_O	Output Current, Into Outputs	30	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS195AXX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Input		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Input		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 12 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 24 mA		V
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7 0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		14	21	V_{CC} = MAX		mA

Notes : 1 Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
2 Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
f_{MAX}	Shift Frequency	30	40		Figures 1	V_{CC} = 5.0 V C_L = 15 pF	MHz
t_{PLH} t_{PHL}	Propagation Delay, Clock to Outputs		14 17	22 26	Figures 1		ns
t_{PHL}	Propagation Delay, MR to Outputs		19	30	Figures 3		ns

AC SET-UP REQUIREMENTS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_WCP	Clock Pulse Width	16	17		Figure 1	V_{CC} = 5.0 V C_L = 15 pF	ns
t_s(Data)	Set-Up Time Data to Clock	15	11		Figure 2		ns
t_h(Data)	Hold Time Data to Clock	0					ns
t_s(S)	Set-Up Time $\overline{PE}$ Control to Clock	25	18		Figure 4		ns
t_h(S)	Hold Time $\overline{PE}$ Control to Clock	0					ns
$t_W(\overline{MR})$	Master Reset Pulse Width	12	8		Figure 3		ns
$t_{rec}(\overline{MR})$	Recovery Time Mater Reset to Clock	25	6				ns
$t_{release}$	$\overline{PE}$			10			ns

DEFINITION OF TERMS:

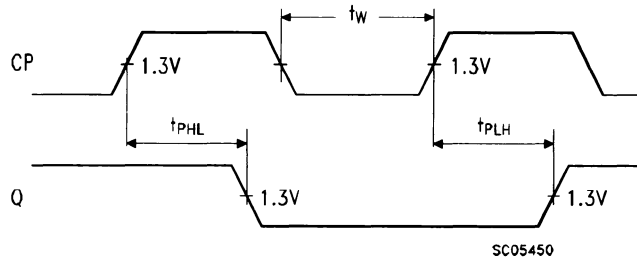
SET-UP TIME (t_s): is defined as the minimum time required for the corret logic level to be present at the logic input prior the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h): is defined as the minimum time following the clock transition from LOW to HIGH at which the logiclevel must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be relased prior to the clock transitio from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) : is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

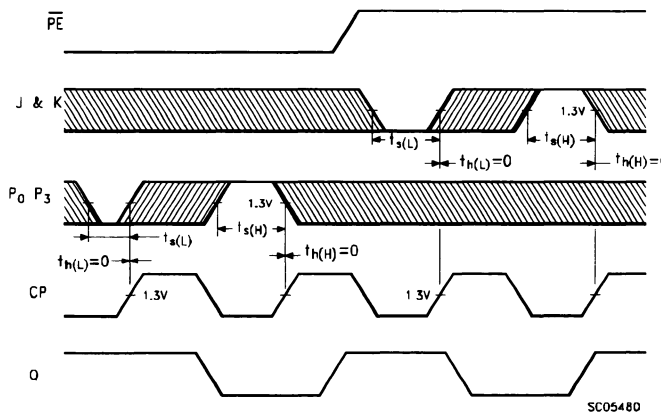
AC WAVEFORMS

Figure 1: Clock to Output Delays and Clock Pulse Width



Conditions: J = $\overline{PE}$ = $\overline{MR}$ = H = $\overline{K}$ = L

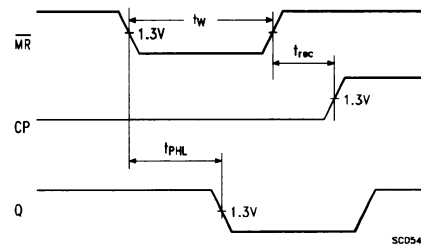
Figure 2: Set-up (ts) and Hold (th) Time for Serial Data (J & K) and Parallel Data (P_0, P_1, P_2, P_3)



Conditions: $\overline{MR}$ = H, J and K set-up time affects Q_0 only

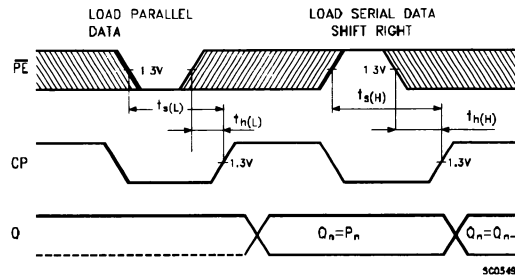
The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 3: Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Other Conditions: $\overline{PE}$ = L, $P_0 = P_1 = P_2 = P_3$ = H

Figure 4: Set-up (t_s) and Hold (t_h) Time for $\overline{PE}$ Input



Conditions: MR = H, Q_0 state will be determined by J and $\overline{K}$ input

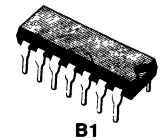
The shaded areas indicate when the input is permitted to change for predictable output performance.

SGS-THOMSON MICROELECTRONICS

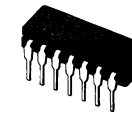
T74LS196
T74LS197

4-STAGE PRESETTABLE RIPPLE COUNTERS

- LOW POWER CONSUMPITION: TYPICALLY 80 mW
- ASYNCHRONOUS PRESETTABLE
- EASY MULTISTAGE CASCADING
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- HIGH COUNTING RATES: TYPICALLY 70 MHz
- ASYNCHRONOUS MASTER RESET
- CHOICE OF COUNTING MODES: BCD, BI-QUINARY, BINARY
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LSXXX D1	T74LSXXX C1
T74LSXXX B1	T74LSXXX M1

DESCRIPTION

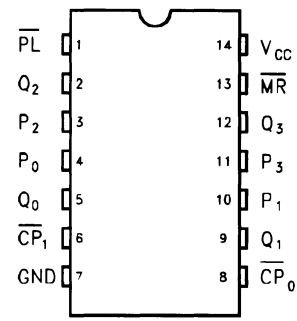
The T74LS196 decade counter is partioned into divide-by-two and divide-by five section which can be combined to count either in BCD (8, 4, 2, 1) sequence or in a bi-quinary mode producing a 50 % duty cycle output. The T74LS197 contains divide-by-two and divide-by-eight sections which can be combined to form a modulo-16 binary counter. Low Power Schottky technology is used to achive typical count rates of 70 MHz and power dissipation of only 80 mW. Both circuit types have Master Reset ($\overline{MR}$) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input ($\overline{PL}$) overrides clocked operations and asynchronously loads the data on the Parallel Data Inputs (P_n) into the flip-flops. This preset feature makes the circuits usable as programmable counters. The circuits can also be used as 4-bit latches, loading data from the Parallel Data inputs when $\overline{PL}$ is LOW and storing the data when $\overline{PL}$ is HIGH.

PIN NAMES

$\overline{CP}_0$	Clock (Active LOW Going Edge) Input to Divide-by-Two Section
$\overline{CP}_1$	Clock (Active LOW Going Edge) Input to Divide-by-Five Section (LS196)
$\overline{CP}_1$	Clock (Active LOW Going Edge) Input to Divide-by-Eight Section (LS197)
$\overline{MR}$	Master Reset (Active LOW) Input
$\overline{PL}$	Parallel Load (Active LOW) Input
P_0-P_3	Data Inputs
Q_0-Q_3	Outputs

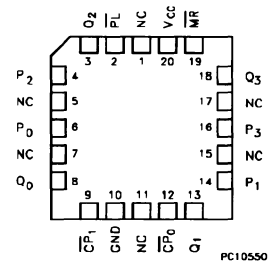
PIN CONNECTION (top view)

DUAL IN LINE



PC10540

CHIP CARRIER



PC10550

NC = No Internal Connection

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	- 0.5 to 7	V
V_I	Input Voltage, Applied to Input	- 0.5 to 15	V
V_O	Output Voltage, Applied to Output	- 0.5 to 10	V
I_I	Input Current, Into Inputs	- 30 to 5	mA
I_O	Output Current, Into Outputs	60	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS196/197XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

FUNCTIONAL DESCRIPTION

The LS196 and LS197 are asynchronous presettable decade and binary ripple counters. The LS196 Decade Counter is partitioned into divide-by-two and divide-by-five sections while the LS197 is partitioned into divide-by-two and divide-by-eight sections, with all section having a separate Clock input. In the counting modes, the state changes are initiated by the HIGH to LOW transition of the clock signals. State changes of the Q outputs, however, do not occur simultaneously bacause of the internal ripple delays. When using external logic to decode the Q outputs, designers should bear in mind that the unequal delays can lead to decoding spikes and thus a decoded signal should not be used as a clock or strobe. The $\overline{CP}_0$ input serves the Q_0 flip-flop in both circuit types while the $\overline{CP}_1$ serves the divide-by-five or divide-by-eight section. The Q_0 output is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input. With the input frequency connected to $\overline{CP}_0$ and Q_0 driving $\overline{CP}_1$, the LS197 form a strightforward module-16 counter, with Q0 the least significant output and Q_3 the most significant output.

The LS196 Decade Counter can be connecetd up to operate in two different count sequences, as indicated in the Table A. With the input frequency connected to $\overline{CP}_0$ and with Q_0 driving $\overline{CP}_1$, the circuit counts in the BCD (8, 4, 2, 1) sequence.

With the input frequency connected to $\overline{CP}_1$ and Q_3 driving $\overline{CP}_0$, Q_0 becomes the low frequency output and as a 50% duty cycle waveform. Note that the maximum counting rate is reduced in the later (biquinary) configuration because of the interstage gating delay within the divide-by-five section. The LS196 and LS197 have an asynchronous active LOW Master Reset input (MR) which overrides all other inputs and forces all outputs LOW. The counters are also asynchronously presettable. A LOW on the Parallel Load input (PL) overrides the clock inputs and loads the data from Parallel Data (P_0-P_3) inputs into flip-flops. While PL is LOW, the counters act as trasparent latches and any change in the P_n inputs will be reflected in the outputs.

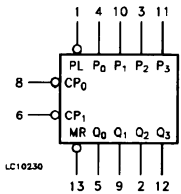
TRUTH TABLE

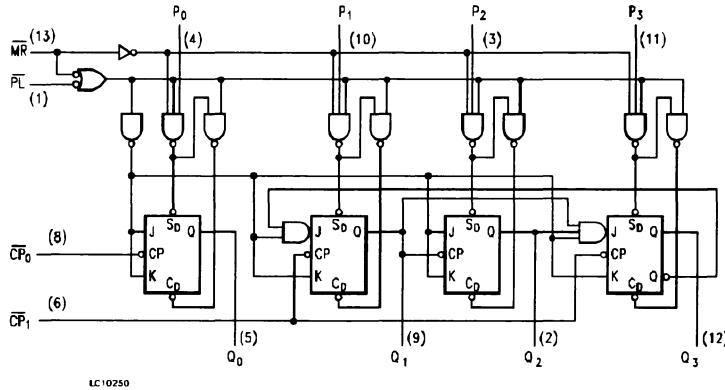
INPUTS			RESPONSE
$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	
L	X	X	Reset (Clear)
H	L	X	Parallel Load
H	H	⌐	Count

H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, ⌐ = HIGH to LOW Clock Transition

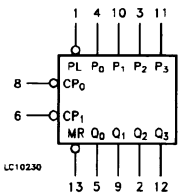
LOGIC DIAGRAMS

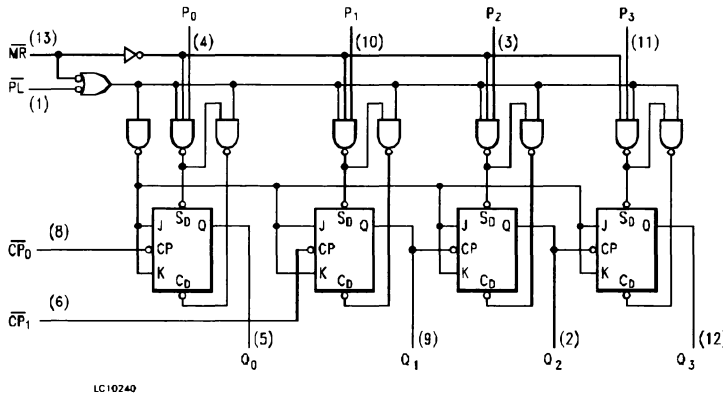
LS196





LS197





V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

TABLE A: LS196 COUNT SEQUENCES

DECADE (NOTE 1)					BI-QUINARY (NOTE 2)				
COUNT	Q_3	Q_2	Q_1	Q_0	COUNT	Q_0	Q_3	Q_2	Q_1
0	L	L	L	L	0	L	L	L	L
1	L	L	L	H	1	L	L	L	H
2	L	L	H	L	2	L	L	H	L
3	L	L	H	H	3	L	L	H	H
4	L	H	L	L	4	L	H	L	L
5	L	H	L	H	5	H	L	L	L
6	L	H	H	L	6	H	L	L	H
7	L	H	H	H	7	H	L	H	L
8	H	L	L	L	8	H	L	H	H
9	H	L	L	H	9	H	H	L	L

Notes: 1. Signal Applied to $\overline{CP_0}$, Q_0 connected to $\overline{CP_1}$
2. Signal Applied to $\overline{CP_1}$, Q_3 connecetd to $\overline{CP_0}$

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)	Unit
		Min.	Typ. (*)	Max.		
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs	V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs	V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA	V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table	V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
I_{IH}	Input HIGH Current $\overline{PL}$, P_0, P_1, P_2, P_3 $\overline{MR}$, $\overline{CP_0}$, $\overline{CP_1}$ (LS197) $\overline{CP_1}$ (LS196)			 20 40 80	V_{CC} = MAX, V_{IN} = 2.7 V	µA
	$\overline{PL}$, P_0, P_1, P_2, P_3 $\overline{MR}$, $\overline{CP_0}$, $\overline{CP_1}$ (LS197) $\overline{CP_1}$ (LS196)			0.1 0.2 0.4	V_{CC} = MAX, V_{IN} = 5 5 V	µA
I_{IL}	Input LOW Current $\overline{PL}$, P_0, P_1, P_2, P_3 $\overline{MR}$ $\overline{CP_0}$ $\overline{CP_1}$ (LS196) $\overline{CP_1}$ (LS197)			 - 0.36 - 0.72 - 2.4 - 2.8 - 1.3	V_{CC} = MAX, V_{IN} = 0 4 V	mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V	mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges
2. Note more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C

AC CHARACTERISTICS: T_A = 25 °C (L196)

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
f_{MAX}	Input Count Frequency	30	40		Figures 1	V_{CC} = 5.0 V C_L = 15 pF	MHz
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP_0}$ Input to Q_0 Outputs		8 13	15 20	Figures 1		ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP_1}$ Input to Q_1 Outputs		16 22	24 33			ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP_1}$ Input to Q_2 Outputs		38 41	57 62			ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP_1}$ Input to Q_3 Outputs		12 30	18 45			ns
t_{PLH} t_{PHL}	Propagation Delay, P_0, P_1, P_2, P_3 Inputs to Q_0, Q_1, Q_2, Q_3 Outputs		20 29	30 44	Figures 2		ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{PL}$ Inputs to Any Outputs		27 30	41 45	Figures 3		ns
t_{PHL}	Propagation Delay, MR Inputs to Any Outputs		34	51	Figures 4		ns

AC CHARACTERISTICS: T_A = 25 °C (LS197)

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
f_{MAX}	Input Count Frequency	30	40		Figures 1	V_{CC} = 5.0 V C_L = 15 pF	MHz
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP_0}$ Input to Q_0 Outputs		8 14	15 21	Figures 1		ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP_1}$ Input to Q_1 Outputs		12 23	19 35			ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP_1}$ Input to Q_2 Outputs		34 42	51 63			ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP_1}$ Input to Q_3 Outputs		55 63	78 95			ns
t_{PLH} t_{PHL}	Propagation Delay, P_0, P_1, P_2, P_3 Inputs to Q_0, Q_1, Q_2, Q_3 Outputs		18 29	27 44	Figures 2		ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{PL}$ Inputs to Any Outputs		26 30	39 45	Figures 3		ns
t_{PHL}	Propagation Delay, MR Inputs to Any Outputs		34	51	Figures 4		ns

AC SET-UP REQUIREMENTS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_W	$\overline{CP_0}$ Pulse Width	20			Figure 1	V_{CC} = 5.0 V	ns
t_W	$\overline{CP_1}$ Pulse Width	30					ns
t_W	$\overline{PL}$ Pulse Width	20			Figure 3		ns
t_W	$\overline{MR}$ Pulse Width	15			Figure 4		ns
t_sL	Set-Up Time LOW	15			Figure 6		ns
t_hL	Hold Time LOW	20					ns
t_sH	Set-Up Time HIGH	10					ns
t_hH	Hold Time HIGH	20					ns
t_{rec}	Recovery Time	30			Figure 5		ns

DEFINITION OF TERMS:

SET-UP TIME (t_s): is defined as the minimum time required for the corret logic level to be present at the logic input prior the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h): is defined as the minimum time following the clock transition from LOW to HIGH at which the logiclevel must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be relased prior to the clock transitio from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) : is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORM

Fig 1.

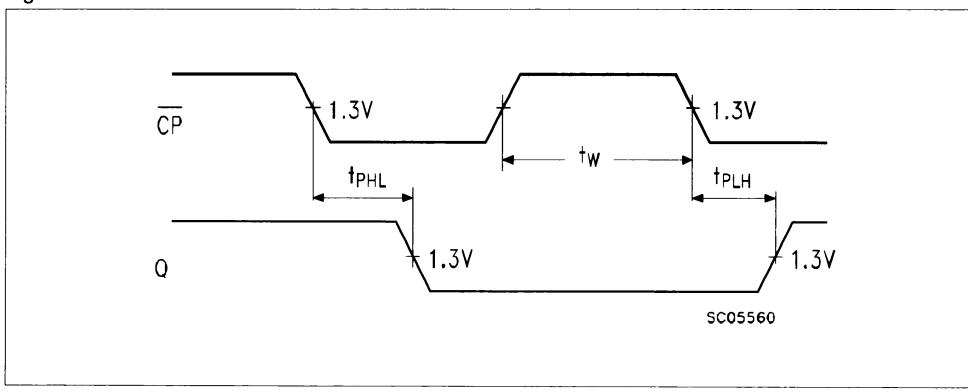


Fig 2.

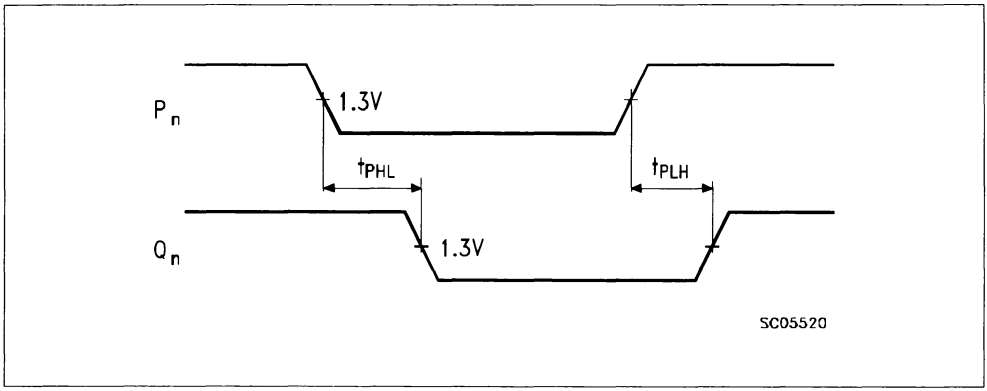


Fig 3.

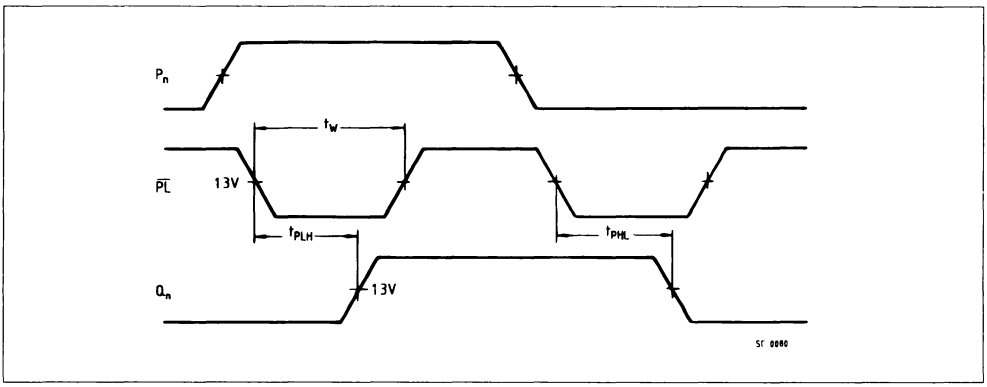


Fig 4.

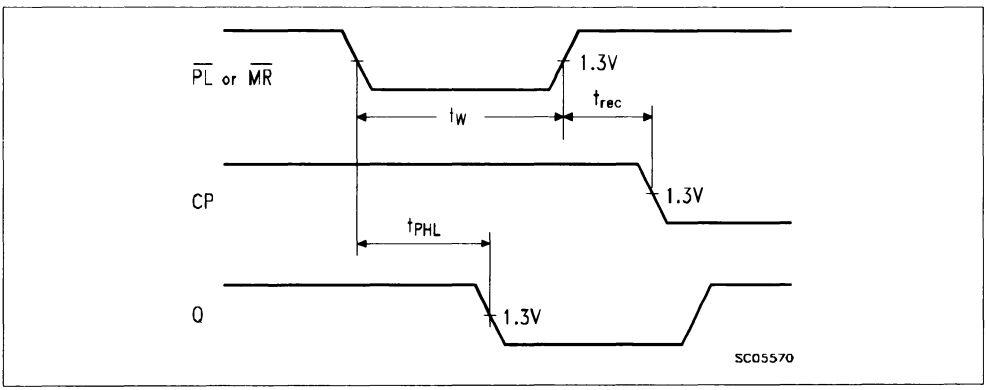
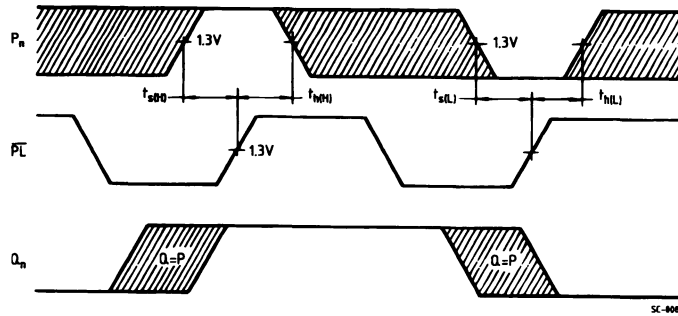


Fig 5.



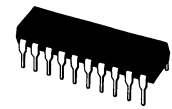
The shaded areas indicate when the input is permitted to change for predictable output performance

OCTAL BUFFER/LINE DRIVERS WITH 3-STATE OUTPUTS

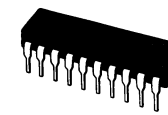
- 3-STATE OUTPUTS DRIVE BUS LINES OR BUFFER MEMORY ADDRESS REGISTERS
- HYSTERESIS AT INPUTS TO IMPROVE NOISE MARGING
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

DESCRIPTION

The T74LS240/241/244 are Octal Buffers and Line Drivers. These devices are designed to be used with 3-state memory address drivers, etc. They are organized as two lines of 4-bit with inverting or non-inverting data.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

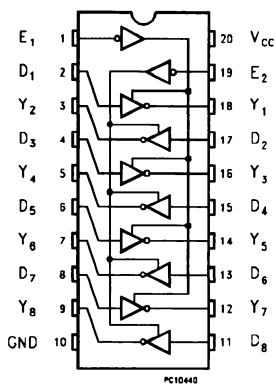
ORDER CODES :

T74LSXXX D1 T74LSXXX C1
T74LSXXX B1 T74LSXXX M1

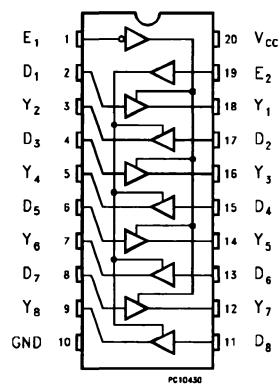
LOGIC DIAGRAM AND PIN CONNECTION (top view)

DUAL IN LINE

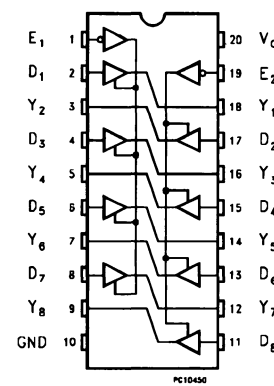
LS240



LS241



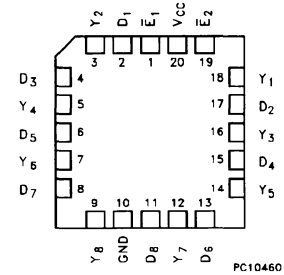
LS244



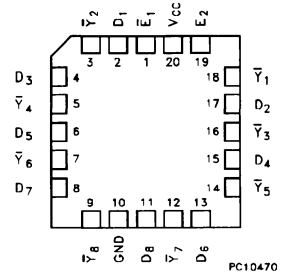
PIN CONNECTION (top view)

CHIP CARRIER

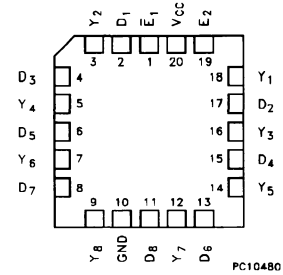
LS240



LS241



LS244



NC = No Internal Connection

T74LS240 TRUTH TABLE

INPUTS		OUTPUT
$\bar{E}_1$, $\bar{E}_2$	D	
L	L	H
L	H	L
H	X	(Z)

T74LS244 TRUTH TABLE

INPUTS		OUTPUT
$\bar{E}_1$, $\bar{E}_2$	D	
L	L	L
L	H	H
H	X	(Z)

T74LS241 TRUTH TABLE

INPUTS		OUTPUT	INPUTS		OUTPUTS
$\bar{E}_1$	D		E2	D	
L	L	L	H	L	L
L	H	H	H	H	H
H	X	(Z)	L	X	(Z)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	− 0.5 to + 7	V
V_I	Input Voltage, Applied to Input	− 0.5 to + 15	V
V_O	Output Voltage, Applied to Output	− 0.5 to + 10	V
I_I	Input Current, Into Inputs	− 30 to + 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS240/241/244XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for all Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for all Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.4 2.0	3.4		V_{CC} = MIN, I_{OH} = - 3.0 mA V_{CC} = MIN, I_{OH} = - 15 mA		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 12 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 24 mA		V
$V_{T+} - V_{T-}$	Hysteresis	0.2	0.4		V_{CC} = MIN		V
I_{OZH}	Output Off Current HIGH			20	V_{CC} = MAX, V_{IN} = 2.7 V		
I_{OZL}	Output Off Current LOW			- 20	V_{CC} = MAX, V_{IN} = 0.4 V		
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.2	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 40		- 225	V_{CC} = MAX		mA
I_{CC}	Power Supply Current Total, Output HIGH			27	V_{CC} = MAX		mA
	Total, Output LOW LS240 LS241/244			44 46			
	Total at HIGH Z LS240 LS241/244			50 54			

Notes : 1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C

AC CHARACTERISTICS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay, Data to Outputs LS240		9 12	14 18	CL = 45 pF RL = 667 Ω	ns
t_{PLH} t_{PHL}	Propagation Delay, Data to Outputs LS240/241/244		12 12	18 18		ns
t_{PZH}	Output Enable Time to HIGH Level		15	23		ns
t_{PZL}	Output Enable Time to LOW Level		20	30		ns
t_{PLZ}	Output Disable Time from LOW Level		15	25	CL = 5.0 pF	ns
t_{PHZ}	Output Disable Time from HIGH Level		10	18		ns

AC WAVEFORMS

Figure 1.

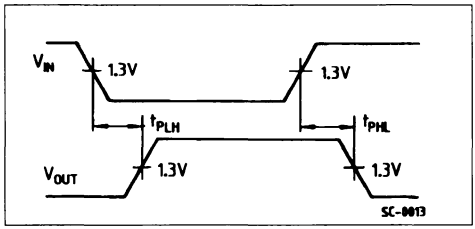


Figure 2.

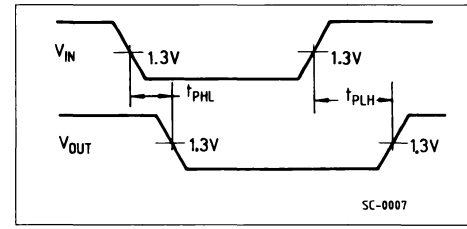


Figure 3.

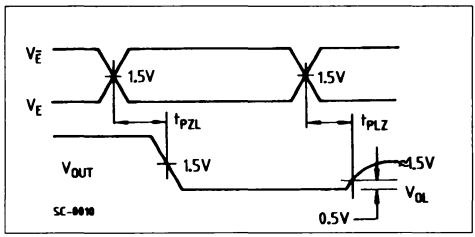
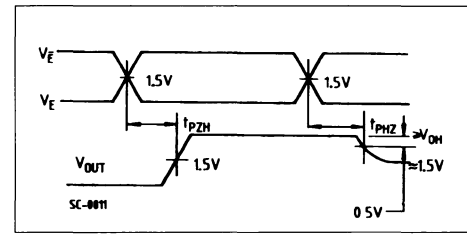
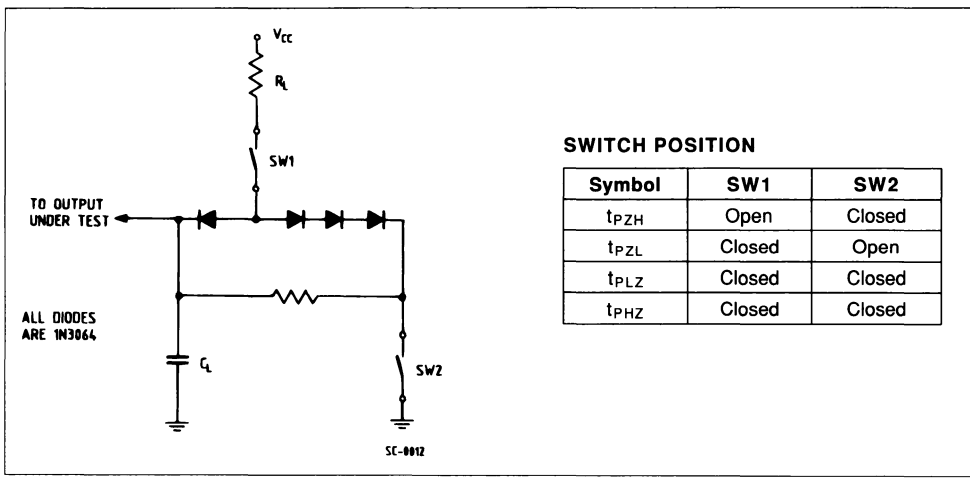


Figure 4.



AC LOAD CIRCUIT

Figure 5.



SWITCH POSITION

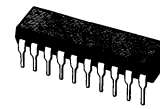
Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

OCTAL BUS TRANSCEIVER

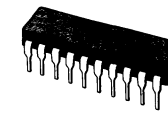
- 2-WAY ASYNCHRONOUS DATA BUS COMUNICATION
- HYSTERESIS INPUTS TO IMPROVE NOISE IMMUNITY
- INPUT DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS

DESCRIPTION

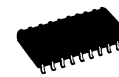
The T74LS245 is an Octal Bus Transceiver intended for 8-line asynchronous 2-way data communication between data buses. Direction Input (DR) takes over the transmission of Data from bus A to bus B or bus B to bus A depending on its logic level. Enable input is usable for isolation of the buses.



B1
(Plastic Package)



D1
(Ceramic Package)



M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS245 D1 T74LS245 C1
T74LS245 B1 T74LS245 M1

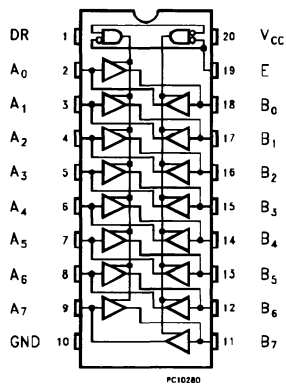
TRUTH TABLE

INPUTS		OUTPUT
E	DR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

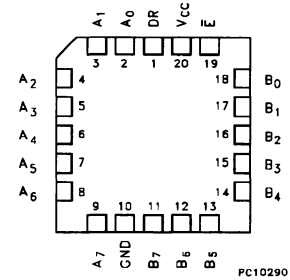
H= HIGH Voltage Level L = LOW Voltage Level X = Don't Care

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to + 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to + 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to + 10	V
I_I	Input Current, Into Inputs	– 30 to + 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS245XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for all Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for all Inputs		V
$V_{T+} - V_{T-}$	Hysteresis	0.2	0.4		V_{CC} = MIN		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.4 2.0	3.4		V_{CC} = MIN, I_{OH} = - 3.0 mA V_{CC} = MIN, I_{OH} = - 15 mA		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 12 mA	V_{CC} = MIN	V
			0.35	0.5	I_{OL} = 24 mA	$V_{IN} = V_{IH}$ or V_{IL} per Truth Table	V
I_{OZH}	Output Off Current HIGH			20	V_{CC} = MAX, V_{IN} = 2.7 V		µA
I_{OZL}	Output Off Current LOW			- 200	V_{CC} = MAX, V_{IN} = 0.4 V		µA
I_{IH}	Input HIGH Current A or B, DR or $\overline{E}$ DR or $\overline{E}$ A or B			 20 0.1 0.1	 V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V V_{CC} = MAX, V_{IN} = 5.5 V		 µA mA mA
I_{IL}	Input LOW Current			- 0.2	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 40		- 225	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW Total at HIGH Z			 70 90 95	V_{CC} = MAX		mA

Notes : 1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: T_A = 25 °C

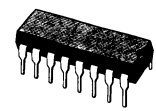
Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay, Clock to Outputs		8.0 8.0	12 12	CL = 45 pF RL = 667 Ω	ns
t_{PZH}	Output Enable Time to HIGH Level		25	40		ns
t_{PZL}	Output Enable Time to LOW Level		27	40		ns
t_{PLZ}	Output Disable Time from LOW Level		15	25	CL = 5.0 pF	ns
t_{PHZ}	Output Disable Time from HIGH Level		15	25		ns

SGS-THOMSON MICROELECTRONICS

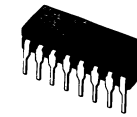
T74LS248

BCD TO SEVEN SEGMENT DECODER/DRIVES

- INTERNAL PULL-UPS ELIMINATE NEED FOR EXTERNAL RESISTORS
- LAMP-TEST PROVISION
- LEADING/TRAILING ZERO SUPPRESSION



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic CHip Carrier)

ORDER CODES :

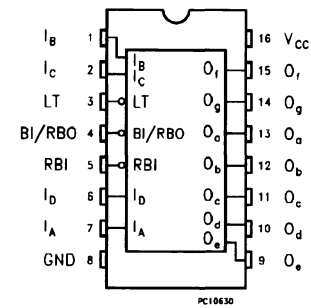
T74LS248 D1 T74LS248 C1
T74LS248 B1 T74LS248 M1

DESCRIPTION

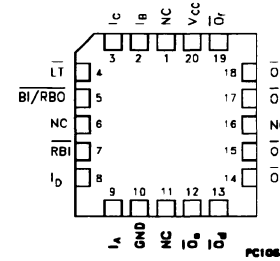
The T74LS248 are BCD to seven segment decoder/Drivers. They compose the and with the tails. It ha active high outputs for driving lamp buffers. Both types feature a lamp test input and full ripple blanking input/output controls. An automatic leading and/or trailing edge zero blanking control (RBI and RBO) is incorporated. An over-riding blanking input (BI) is incorporated. An over riding blanking input (BI) may be used to control the lamp intensity. Display pattern for BCD input counts above 9 are unique symbols to authenticate input conditions.

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

PIN NAMES

A, B, C, D	Inputs
a,b,c,d,e,f,g	Outputs
LT	Lamp test
RBO	Rubout Outputs
RBI	Rubuot Inputs
BI	Blanking Inputs

ALL CIRCUIT TYPES FEATURE LAMP INTENSITY MODULATION CAPABILITY

DRIVER OUTPUTS				TYPICAL POWER DISSIPATION
ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE	
High	2 KΩ pull-up	2.0 mA	5.5 V	125 mW
High	2 KΩ pull-up	6.0 mA	5.5 V	125 mW

TRUTH TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO *	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	H	L	H	H	H	H	H	1
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	H	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

H = HIGH Level L = LOW Voltage Level X = Don't Care

NOTES: 1) The Blanking input (BI) must be open or held at a high logic level when output functions) throught 15 are desired The ripple blanking input (RBI) must be open or high if blanking of a decimal zero is not desired

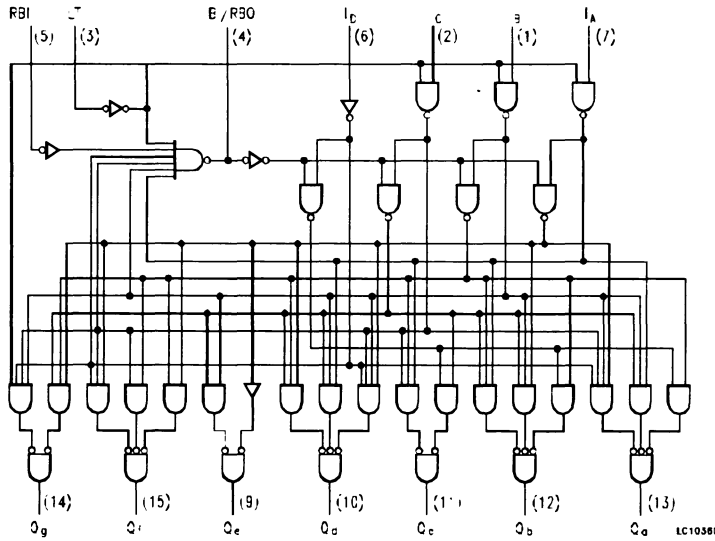
2) When a low logic level is applied directly to the blanking input (BI) all segment outputs are off regardless of the level of any other inputt

3) When ripple-blanking input (RBI) and inputs A, B, C and D are at low level with he lamp test input high, all segment outputs go off and the ripple -blanking output (RBO) goes to a low level (response condition)

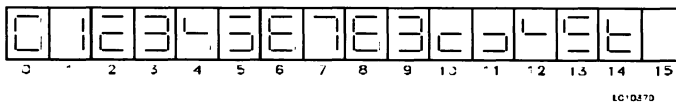
4) When the blanking input ripple blanking output (BI RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on

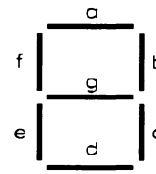
* BI RBO is wire-AND logic serving as blanking input (BI) and or ripple-blanking output (RBO)

LOGIC DIAGRAMS



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers





ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	0 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS248XX	4.75 V	5 0 V	5.25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.4	4.2		V_{CC} = MIN, I_{OH} = MAX ** V_{IN} = V_{IH} or V_{IL} per Truth Table		V
I_O	Output Current a-g	- 1.3	- 20		V_{CC} = MIN, V_O = 0.85 V Input Conditions as for V_{OH}		mA
V_{OL}	Output LOW Voltage a-g		0.25	0.4	I_{OL} = 2.0 mA	V_{CC} = MIN, V_{IN} = 2 0 V	V
			0.35	0.5	I_{OL} = 3.2 mA		V
	BI/RBO		0.25	0.4	I_{OL} = 1.6 mA	V_{IL} = per Truth Table	V
			0.35	0.5	I_{OL} = 3.2 mA		V
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current Any Input, except BI/RBO BI/RBO			 - 0 4 - 1.2	V_{CC} = MAX, V_{IN} = 0 4 V		mA
I_{OS}	Output SHort Circuit Current BI/RBO (note 2)	- 0.3		- 2.0	V_{CC} = MAX		mA
I_{CC}	Power Supply Current		25	38	V_{CC} = MAX		mA

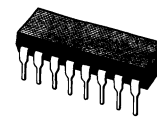
Notes : 1 For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges
2. Note more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C.
** I_{OH} = - 50 µA for BI/RBO, I_{OH} = - 100 µA for a-g

AC CHARACTERISTICS: T_A = 25 °C

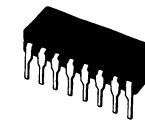
Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
t_{PHL} t_{PLH}	Propagation Delay, Output from A Input			100 100	C_L = 15 pF R_L = 4.0 KΩ	ns
t_{PHL} t_{PLH}	Propagation Delay, Output from RBI Input			100 100	C_L = 15 pF R_L = 6.0 KΩ	ns

8-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- ON-CHIP SELECT LOGIC DECODING
- INVERTING AND NON-INVERTING 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

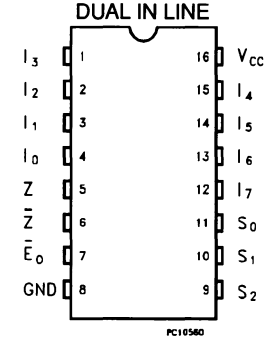
T74LS251 D1 T74LS251 C1
T74LS251 B1 T74LS251 M1

DESCRIPTION

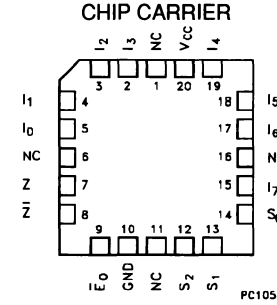
The TTL/MSI T74LS251 is a high speed 8-Input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. The LS251 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

PIN CONNECTION
(top view)

DUAL IN LINE



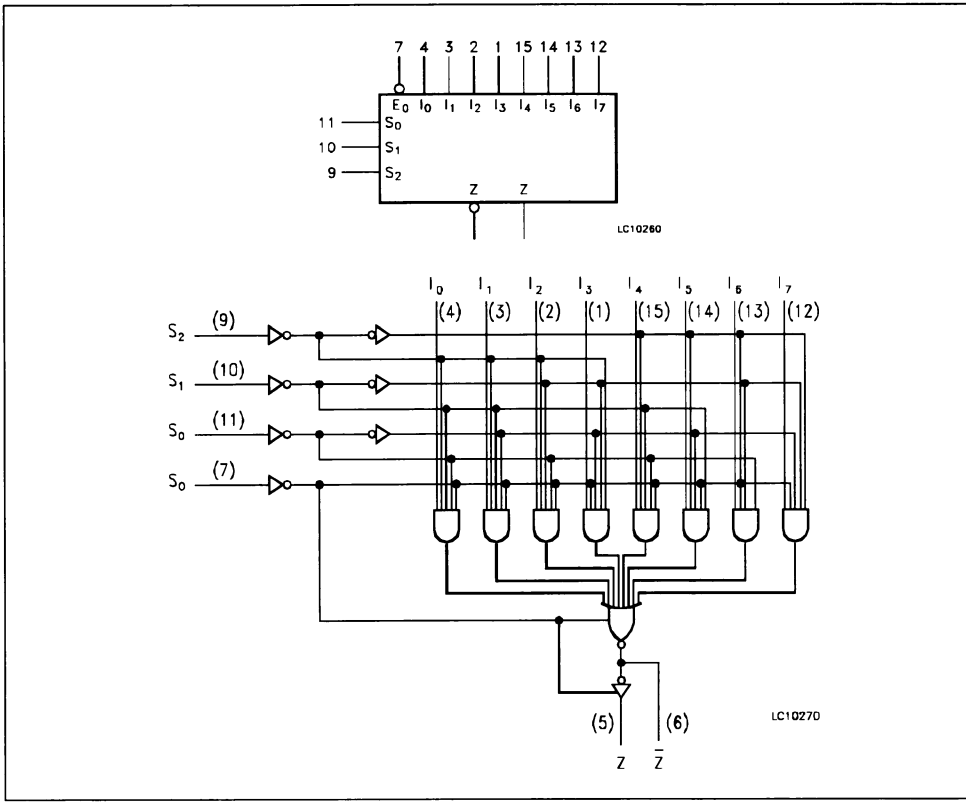
CHIP CARRIER



PIN NAMES

S_0-S_2	Select Input
$\bar{E}_0$	Output Enable (Active LOW) Input
I_0-I_7	Multiplexer Inputs
Z	Multiplexer Outputs
$\bar{Z}$	Complementary Multiplexer Output

LOGIC SYMBOL AND LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 5.5	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS251XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

FUNCTIONAL DESCRIPTION

The LS251 is a logical implementation of a single pole, 8-position switch the swith position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Output Enable input (E_0) is active LOW. When is is activated, the logic function provided a the output is :

$$Z = \overline{E} \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

When the output Enable is HIGH, both outputs are in the high impedance (high Z) state. This feature allows multiplexer expansion by tying the outputs of up the 128 devices together. When the output sof the 3-state devices are tied together, all but one, device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Outputs Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltage.

TRUTH TABLE

E_0	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	(Z)	(Z)
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(Z) = High impedance

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for all Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for all Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.4	3.4		V_{CC} = MIN, I_{OH} = - 2.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{OZH}	Output Off Current HIGH			20	V_{CC} = MAX, V_{OUT} = 2.7 V, $V_{\overline{E}}$ = 2.0 V		µA
I_{OZL}	Output Off Current LOW			- 20	V_{CC} = MAX, V_{OUT} = 2.7 V, $V_{\overline{E}}$ = 2.0 V		µA
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 30		- 130	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current Outputs LOW Outputs Off		6.0 7.0	10 12	V_{CC} = MAX, V_{OUT} = 4.5 V, $V_{\overline{E}}$ = 0 V V_{OUT} = 4.5 V, $V_{\overline{E}}$ = 4.5 V		mA

AC CHARACTERISTICS : (T_A = 25 °C)

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Select to $\overline{Z}$ Output		20 21	33 33	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PLH} t_{PHL}	Propagation Delay, Select to Z Output		28 28	45 45	Fig. 2		ns
t_{PLH} t_{PHL}	Propagation Delay, Data to $\overline{Z}$ Output		10 9.0	15 15	Fig. 1		ns
t_{PLH} t_{PHL}	Propagation Delay, Data to Z Output		17 18	28 28	Fig. 1		ns
t_{PZH} t_{PZL}	Output Enable Time to $\overline{Z}$ Output		17 24	27 40	Figs 4,5		ns
t_{PZH} t_{PZL}	Output Enable Time to Z Output		30 26	45 40	Figs 3,5		ns
t_{PHZ} t_{PLZ}	Output Disable Time to $\overline{Z}$ Output		37 15	55 25	Figs 3,5	V_{CC} = 5.0V C_L = 5 pF	ns
t_{PHZ} t_{PLZ}	Output Disable Time to Z Output		30 15	45 25	Figs 4,5		ns

Notes : 1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output be shorted at a time
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

3-STATE AC WAVEFORMS AC LOAD CIRCUIT

Figure 1.

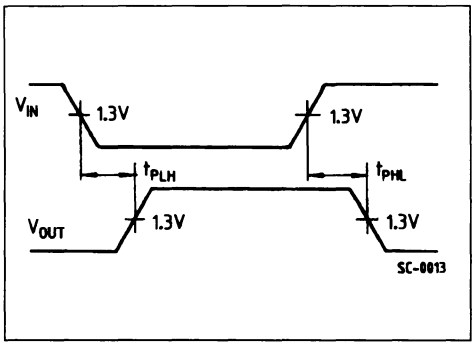


Figure 2.

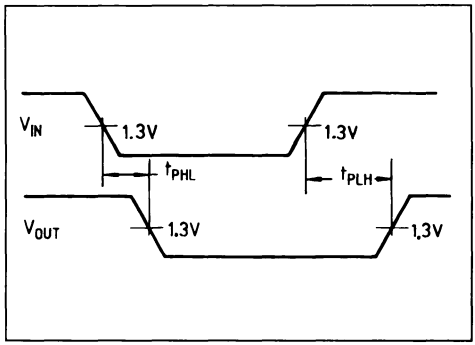


Figure 3.

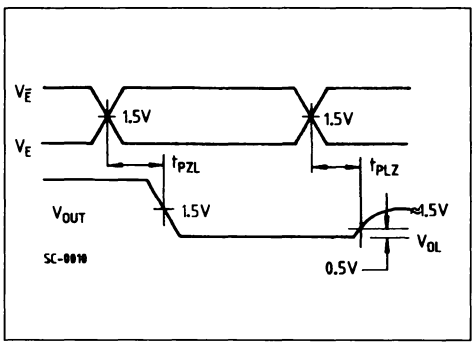


Figure 4.

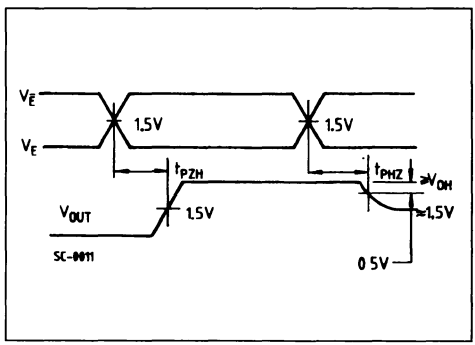
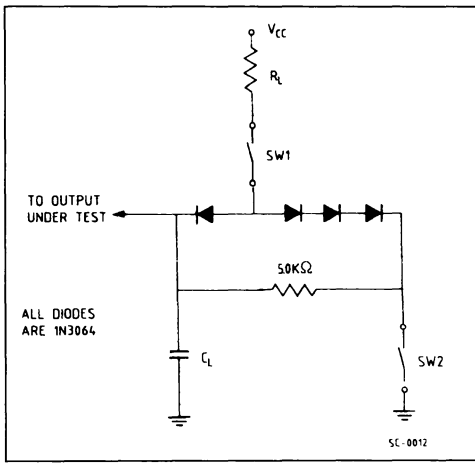


Figure 5.



SWITCHING POSITION

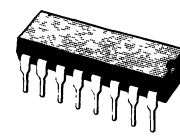
Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

SGS-THOMSON MICROELECTRONICS

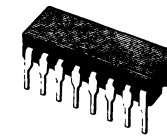
T74LS253

DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- NON INVERTING 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

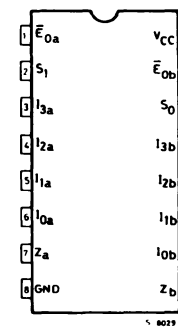
T74LS253 D1 T74LS253 C1
T74LS253 B1 T74LS253 M1

DESCRIPTION

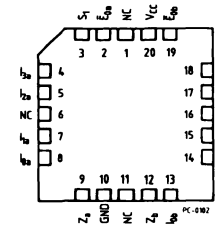
The LSTTL/MSI T74LS253 is a very high speed Dual 4-Input Multiplexer with 3-state outputs. It can select two bits data from four sources using commun select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable (E_0) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all TTL families.

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER

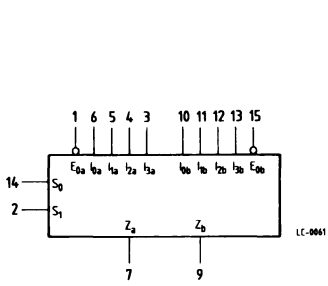


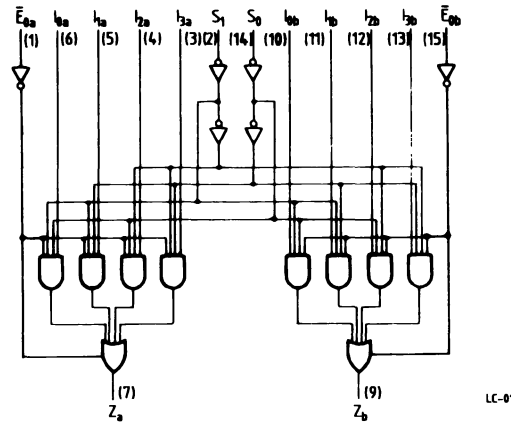
NC = No Internal Connection

PIN NAMES

S_0-S_1	COMMON SELECT INPUT
Multiplexer A	
E_{0a}	OUTPUT ENABLE (active LOW) INPUT
I_{0a}-I_{3a}	MULTIPLEXER INPUTS
Z_a	MULTIPLEXER OUTPUT
Multiplexer B	
E_{0b}	OUTPUT ENABLE (active LOW) INPUT
I_{0b}-I_{3b}	MULTIPLEXER INPUTS
Z_b	MULTIPLEXER OUTPUT

LOGIC SYMBOL AND LOGIC DIAGRAM





V_{CC} = Pin 16
GND = Pin 8
() = Pin numbers

TRUTH TABLE

Select Inputs		Data Inputs				Output Enable	Output
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{E}_0$	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(Z) = High Impedance (off)
Address inputs S_0 and S_1 are common to both sections.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.6 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS253XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

FUNCTIONAL DESCRIPTION

The LS253 contains two identical 4-Input Multiplexers with 3-state outputs. They select two bits from four sources selected by common select inputs (S0, S1). The 4-input multiplexers have individual Output Enable (E_{0a}, E_{0b}) inputs which when HIGH, forces the outputs to a high impedance (high Z) state.

The LS253 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select Inputs. The logic equations for the outputs are shown below.

$$Z_a = \overline{E}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1$$

$$Z_b = \overline{E}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Outputs Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.4	3.1		V_{CC} = MIN, I_{OH} = - 2.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{OZH}	Output Off Current HIGH			20	V_{CC} = MAX, V_{OUT} = 2.7 V $V_{\overline{E}}$ = 2.0 V		µA
I_{OZL}	Output Off Current LOW			- 20	V_{CC} = MAX, V_{IN} = 0.4 V $V_{\overline{E}}$ = 2.0 V		µA
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 30		- 130	V_{CC} = MAX		mA
I_{CC}	Power Supply Current Outputs LOW Outputs Off		 7.0 8.5	 12 14	 V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 2.0 V V_{CC} = MAX, V_{IN} = 4.5 V, $V_{\overline{E}}$ = 2.0 V		mA

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		17 13	25 20	Fig. 1	C_L = 15 pF	ns
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		30 21	45 32	Fig. 1		ns
t_{PZH}	Output Enable Time to HIGH Level		15	28	Figs. 4, 5	C_L = 15 pF R_L = 2 kΩ	ns
t_{PZL}	Output Enable Time to LOW Level		15	23	Figs. 3, 5		ns
t_{PLZ}	Output Disable Time from LOW Level		18	27	Figs. 3, 5	C_L = 5 pF R_L = 2 kΩ	ns
t_{PHZ}	Output Disable Time from HIGH Level		27	41	Figs. 4, 5		ns

STATE AC WAVEFORMS AND LOAD CIRCUIT

Figure 1.

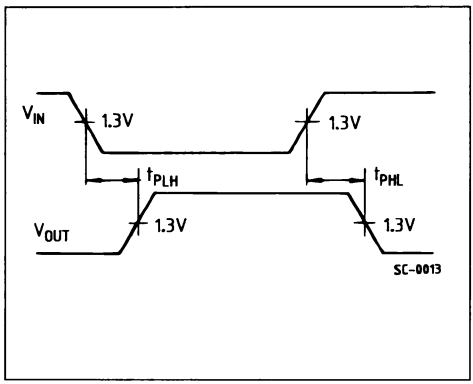


Figure 2.

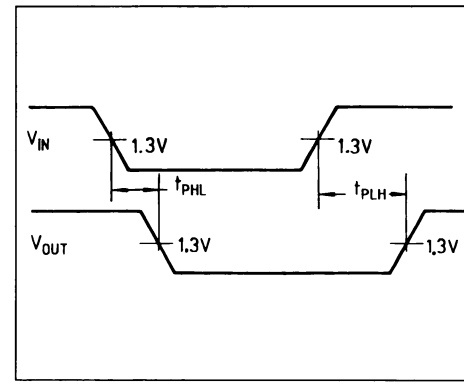


Figure 3.

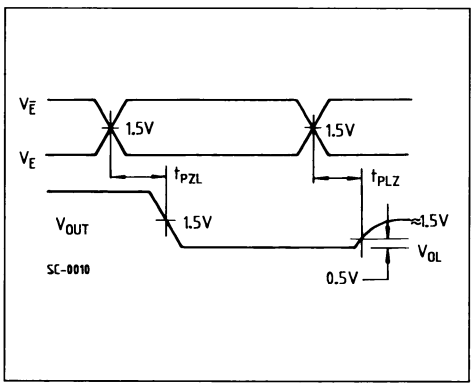


Figure 4.

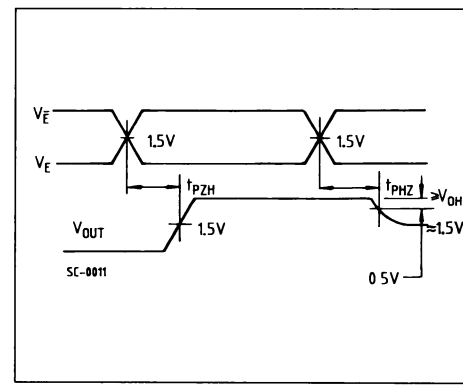
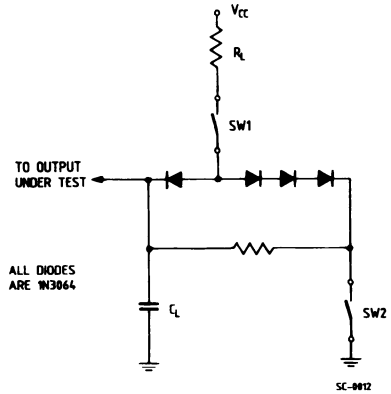


Figure 5.



SWITCHING POSITIONS

Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

DUAL 4-BIT ADDRESSABLE LACTH

- SERIAL-TO-PARALLEL CAPABILITY
- OUTPUT FROM EACH STORAGE BIT AVAILABLE
- RANDOM (addressable) DATA ENTRY
- EASILY EXPANDABLE
- ACTIVE LOW COMMON CLEAR
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

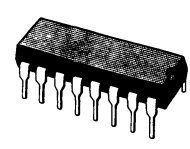
DESCRIPTION

The T74LS256 is a Dual 4-Bit Addressable Latch with common control inputs ; these include two Address inputs (A_0, A_1), an active LOW Enable input ($\overline{E}$) and an active LOW Clear input ($\overline{C}$). Each latch has a Data input (D) and four outputs (Q_0-Q_3).

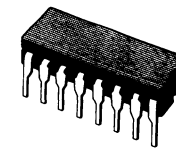
When the Enable ($\overline{E}$) is HIGH and the Clear input ($\overline{C}$) is LOW, all outputs (Q_0-Q_3),are LOW. Dual 4-channel demultiplexing occurs when the $\overline{C}$ and $\overline{E}$ are both LOW. When C is HIGH and $\overline{E}$ is LOW, the selected outputs (Q_0-Q_3), determined by the Address inputs, follows D. When the $\overline{E}$ goes HIGH, the contents of the lacth are stored. When operating in the addressable latch mode ($\overline{E}$ = LOW, $\overline{C}$ = HIGH), changing more than one bit of the Address (A_0, A_1) could impose a transient wrong address. Therefore, this should be done only while in the memory mode ($\overline{E}$ = $\overline{C}$ = HIGH).

PIN NAMES

A_0, A_1	ADDRESS INPUTS
D_a, D_b	DATA INPUTS
$\overline{E}$	ENABLE (active LOW) INPUT
$\overline{C}$	CLEAR (active LOW) INPUT
Q_{0a} - Q_{3a}, Q_{0b} - Q_{3b}	PARALLEL LATCH OUTPUTS



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

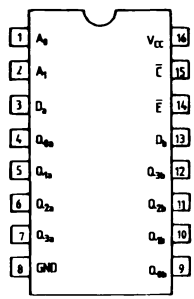
C1
(Plastic Chip Carrier)

ORDER CODES :

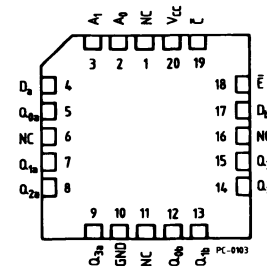
T74LS256 D1 T74LS256 C1
T74LS256 B1 T74LS256 M1

PIN CONNECTION (top view)

DUAL IN LINE

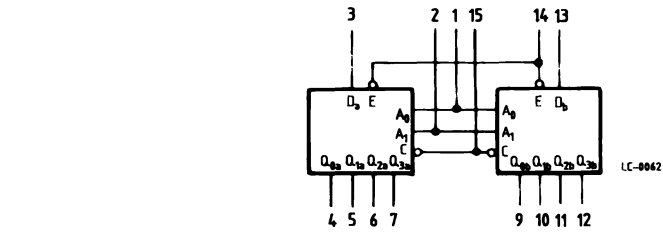


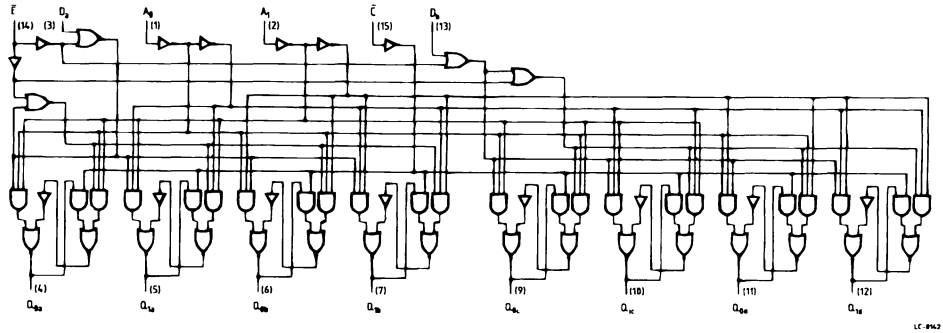
CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM





V_{CC} = Pin 16
GND = Pin 8
() = Pin numbers

MODE SELECTION

$\overline{E}$	$\overline{C}$	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Dual 4–Channel Demultiplexer
H	L	Clear

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	30	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS256XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

TRUTH TABLE

$\overline{C}$	$\overline{E}$	D	A_0	A_1	Q_0	Q_1	Q_2	Q_3	Mode
L	H	X	X	X	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	Demultiplexer
L	L	H	L	L	H	L	L	L	
L	L	L	H	L	L	L	L	L	
L	L	H	H	L	L	H	L	L	
L	L	L	L	H	L	L	L	L	
L	L	H	L	H	L	L	H	L	
L	L	L	H	H	L	L	L	L	
L	L	H	H	H	L	L	L	H	
H	H	X	X	X	Q_{n-1}	Q_{n-1}	Q_{n-1}	Q_{n-1}	Memory
H	L	L	L	L	L	Q_{n-1}	Q_{n-1}	Q_{n-1}	Addressable
H	L	H	L	L	H	Q_{n-1}	Q_{n-1}	Q_{n-1}	Latch
H	L	L	H	L	Q_{n-1}	L	Q_{n-1}	Q_{n-1}	
H	L	H	H	L	Q_{n-1}	H	Q_{n-1}	Q_{n-1}	
H	L	L	L	H	Q_{n-1}	Q_{n-1}	L	Q_{n-1}	
H	L	H	L	H	Q_{n-1}	Q_{n-1}	H	Q_{n-1}	
H	L	L	H	H	Q_{n-1}	Q_{n-1}	Q_{n-1}	L	
H	L	H	H	H	Q_{n-1}	Q_{n-1}	Q_{n-1}	H	

H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0 35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current $\overline{A_0}$, A_1, $\overline{C}$, D_a, D_b, $\overline{E}$			20 40	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	Input HIGH Current $\overline{A_0}$, A_1, $\overline{C}$, D_a, D_b, $\overline{E}$			0.1 0 2	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current $\overline{A_0}$, A_1, $\overline{C}$, D_a, D_b, $\overline{E}$			- 0.4 - 0.8	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX		mA
I_{CC}	Power Supply Current		20	25	V_{CC} = MAX		mA

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Turn-off Delay, Enab. to Out. Turn-on Delay, Enab. to Out.		20 16	27 24	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PLH} t_{PHL}	Turn-off Delay, Data to Out. Turn-on Delay, Data to Out.		20 13	30 20	Fig. 2		ns
t_{PLH} t_{PHL}	Turn-off Delay, Addr. to Out. Turn-on Delay, Addr. to Out.		20 14	30 24	Fig. 3		ns
t_{PHL}	Turn-on Delay, Clear to Output		12	23	Fig. 5		ns

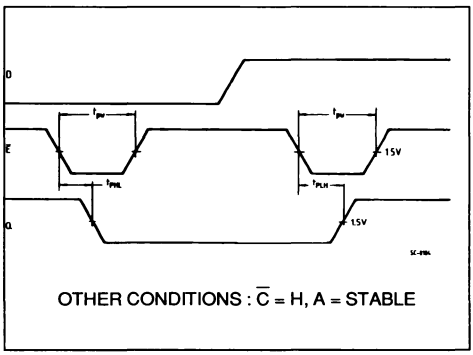
AC SET-UP REQUIREMENTS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
t_sH	Set-up Time HIGH, Data to Enable	20	13		V_{CC} = 5.0 V	Fig. 4	ns
t_hH	Hold Time HIGH, Data to Enable	0	– 7.0				
t_sL	Set-up Time LOW, Data to Enable	15	7.0				ns
t_hL	Hold Time LOW, Data to Enable	0	10				
t_sA-$\overline{E}$	Set-up Time, Address to Enable (note 4)	0	– 7.0		V_{CC} = 5.0 V	Fig. 6	ns
$t_w\overline{E}$	Enable Pulse Width	17	12		V_{CC} = 5.0 V	Fig. 1	ns

Notes : 4. The address to Enable Set-up Time is the time befor the HIGH to LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
5: The shaded areas indicate when the inputs are permitted to change for predictable output performance

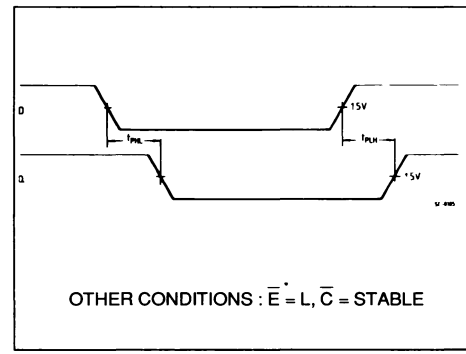
AC WAVEFORMS

Figure 1 : Turn-On and Turn-Off Delays, Enable to Output and Enable Pulse Width.



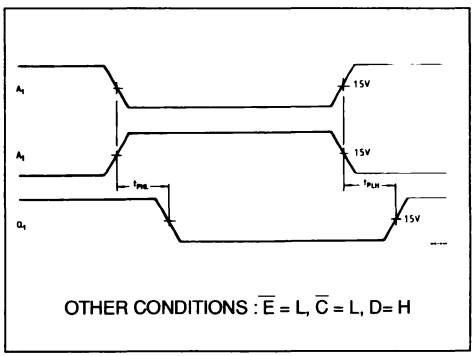
OTHER CONDITIONS : $\overline{C}$ = H, A = STABLE

Figure 2 : Turn-On and Turn-Off Delays, Data to Output.



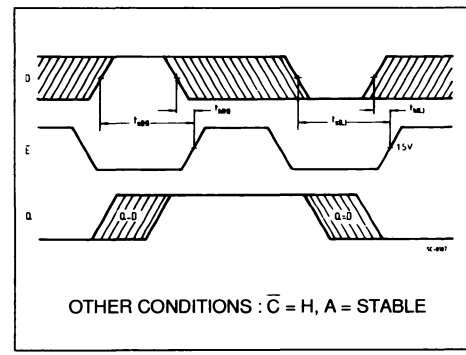
OTHER CONDITIONS : $\overline{E}$ = L, $\overline{C}$ = STABLE

Figure 3 : Turn-On and Turn-Off Delays, Address to Output.



OTHER CONDITIONS : $\overline{E}$ = L, $\overline{C}$ = L, D= H

Figure 4 : Set-up and Hold Time, Data toEnable.



OTHER CONDITIONS : $\overline{C}$ = H, A = STABLE

Figure 5 : Turn-On Delays, Clear to Output.

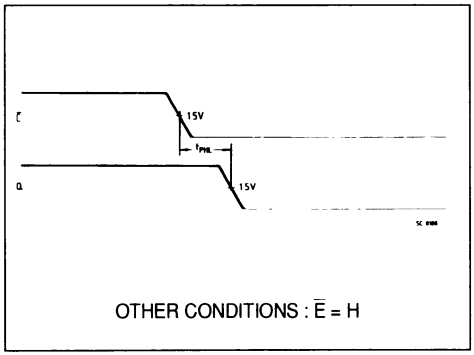
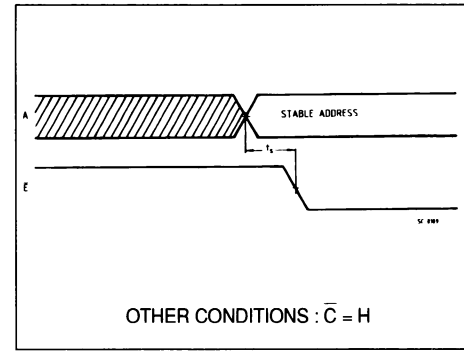


Figure 6 : Set-up Time, Address to Enable (see notes 4 and 5).

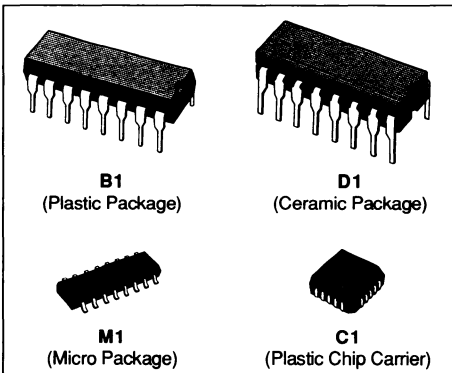


QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER
- NON-INVERTING 3 STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

DESCRIPTION

The LSTTL/MSI T74LS257A is a Quad 2-Input Multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Outputs Enable ($\overline{E}_0$) Input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all TTL families.



B1 (Plastic Package)

D1 (Ceramic Package)

M1 (Micro Package)

C1 (Plastic Chip Carrier)

ORDER CODES :

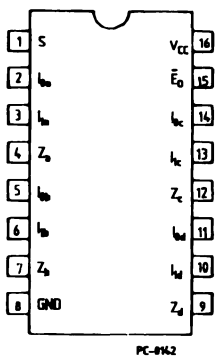
T74LS257A D1 T74LS257A C1
T74LS257A B1 T74LS257A M1

PIN NAMES

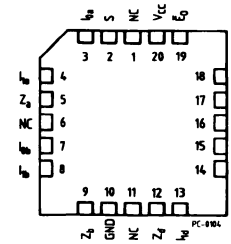
$\overline{S}$	COMMON SELECT INPUT
$\overline{E}_0$	Output Enable (active LOW) INPUT
I_{0a}-I_{0d}	DATA INPUTS FROM SOURCE 0
I_{1a}-I_{1d}	DATA INPUTS FROM SOURCE 1
Z_a-Z_d	MULTIPLEXER OUTPUT

PIN CONNECTION (top view)

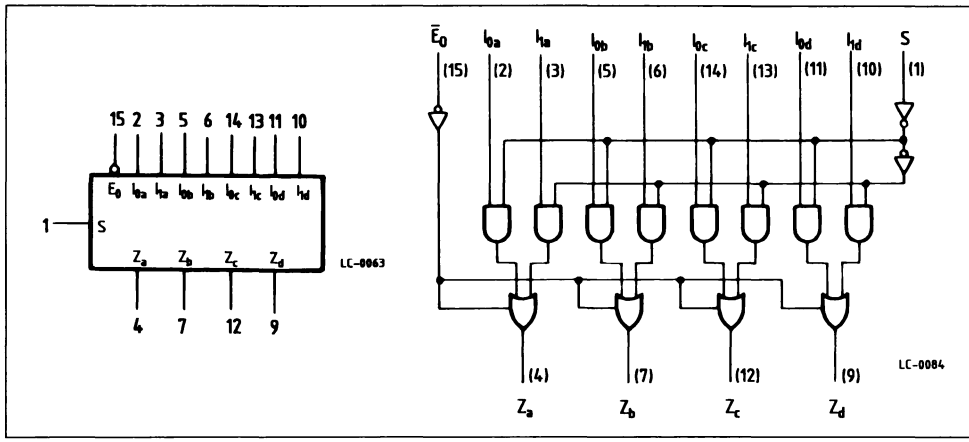
DUAL IN LINE



CHIP CARRIER



LOGIC SYMBOL AND LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	− 0.5 to + 7	V
V_I	Input Voltage, Applied to Input	− 0.5 to + 5.5	V
V_O	Output Voltage, Applied to Output	− 0.5 to + 5.5	V
I_I	Input Current, Into Inputs	− 30 to + 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS257AXX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

FUNCTIONAL DESCRIPTION

The LS257A is a Quad 2-Input Multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a Common Data Select Input. When the Select Input is LOW, the I_0 inputs are selected and when Selected is HIGH, the I_1 inputs are selected. The data on the selected inputs appear at the outputs in true (non-inverted) form. The LS257A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for outputs are show below:

$$Z_a = \overline{E}\ 0 \bullet (I1a \bullet S + I0a \bullet \overline{S}) Z_b = \overline{E}\ 0 \bullet (I1b \bullet S + I0b \bullet \overline{S})$$

$$Z_c = \overline{E}\ 0 \bullet (I1c \bullet S + I0c \bullet \overline{S}) Z_d = \overline{E}\ 0 \bullet (I1d \bullet S + I0d \bullet \overline{S})$$

When the Output Enable Input ($\overline{E}\ 0$) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

TRUTH TABLE

Output Enable	Select Input	Data Inputs		Outputs
$\overline{E}_0$	S	I_0	I_1	Z
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(Z) = High impedance (off)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits Min.	Typ. (*)	Max.	Test Condition (note 1)	Unit
V_{IH}	Input HIGH Voltage		2 0			Guaranteed Input HIGH Voltage for All Inputs	V
V_{IL}	Input LOW Voltage				0.8	Guaranteed Input LOW Voltage for All Inputs	V
V_{CD}	Input Clamp Diode Voltage			- 0 65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA	V
V_{OH}	Output HIGH Voltage		2.4	3 1		V_{CC} = MIN, I_{OH} = - 2.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table	V
V_{OL}	Output LOW Voltage			0.25	0.4	I_{OL} = 12 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
				0.35	0.5	I_{OL} = 24 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
I_{OZH}	Output Off Current HIGH				20	V_{CC} = MAX, V_{OUT} = 2.7 V	µA
I_{OZL}	Output Off Current LOW				- 20	V_{CC} = MAX, V_{IN} = 0.4 V	µA
I_{IH}	Input HIGH Current	Other Inputs			20	V_{CC} = MAX, V_{IN} = 2.7 V	µA
		S Input			40		
		Other Inputs			0.1	V_{CC} = MAX, V_{IN} = 7.0 V	mA
		S Input			0.2		
I_{IL}	Input LOW Current	Other Inputs			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V	mA
		S Input			- 0.8		
I_{OS}	Output Short Circuit Current (note 2)		- 30		- 130	V_{CC} = MAX	mA
I_{CC}	Power Supply Current						mA
	Total Output HIGH				10	V_{CC} = MAX	
	Total Output LOW				16		
	Total output 3-state				19		

Notes : 1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5 0 V T_A = 25 °C

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions (note 1)		Unit
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		9 11	18 18	fig. 1	V_{CC} = 5.0 V C_L = 45 pF R_L = 667 Ω	ns
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		16 19	21 25	fig. 1		ns
t_{PZH}	Output Enable Time to HIGH Level		17	30	figs. 4, 5		ns
t_{PZL}	Output Enable Time to LOW Level		17	30	figs. 3, 5		ns
t_{PLZ}	Output Disable Time from LOW Level		15	25	figs. 3, 5	V_{CC} = 5.0 V C_L = 5pF	ns
t_{PHZ}	Output Disable Time from HIGH Level		17	30	figs. 4, 5		ns

WAVEFORMS

Figure 1.

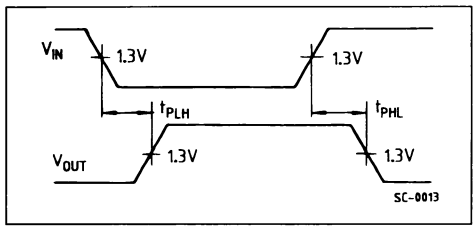


Figure 2.

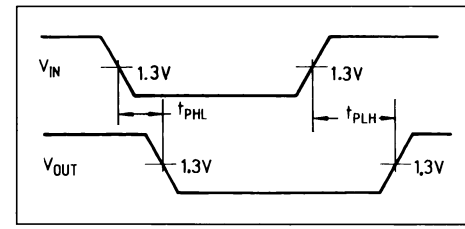


Figure 3.

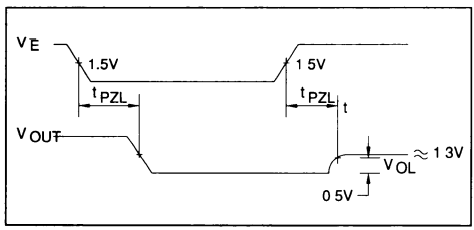


Figure 4.

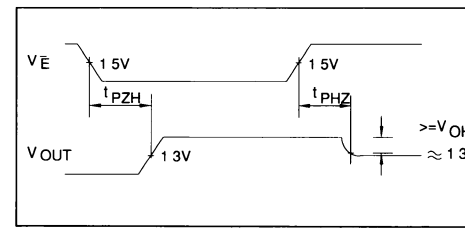
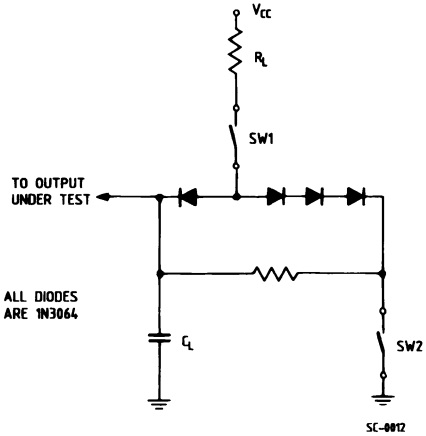


Figure 5.



SWITCHING POSITIONS

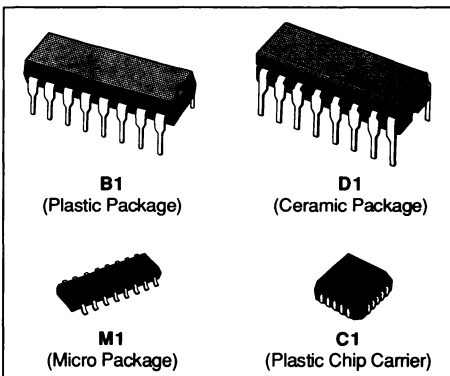
Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER
- INVERTING 3 STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

DESCRIPTION

The T74LS258A is a Quad 2-Input Multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select Input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Outputs Enable ($\overline{E}_0$) Input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all TTL families.



B1 (Plastic Package)

D1 (Ceramic Package)

M1 (Micro Package)

C1 (Plastic Chip Carrier)

ORDER CODES :

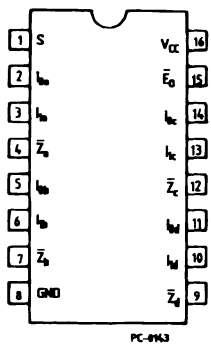
T74LS258A D1 T74LS258A C1
T74LS258A B1 T74LS258A M1

PIN NAMES

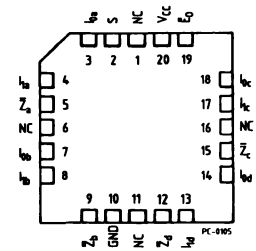
$\overline{S}$	COMMON SELECT INPUT
$\overline{E}_0$	Output Enable (active LOW) Input
I_{0a}-I_{0d}	DATA INPUTS FROM SOURCE 0
I_{1a}-I_{1d}	DATA INPUTS FROM SOURCE 1
Z_a-Z_d	Multiplexer Output

PIN CONNECTION (top view)

DUAL IN LINE

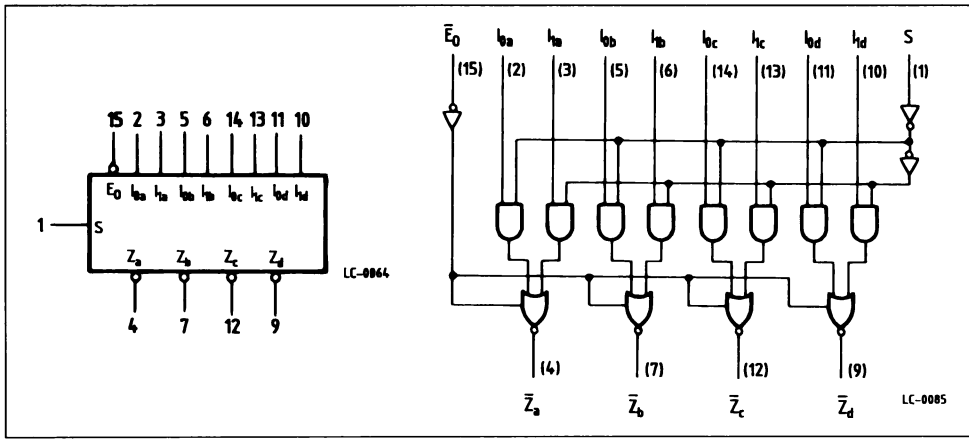


CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to + 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to + 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to + 5.5	V
I_I	Input Current, Into Inputs	– 30 to + 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS258XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

FUNCTIONAL DESCRIPTION

The LS258A is a Quad 2-Input Multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a Common Select Input (S). When the Select is LOW, the I_0 inputs are selected and when Selected is HIGH, the I_1 inputs are selected. The data on the selected inputs appear at the outputs in inverted form.

The LS258A Quad 2-Input Multiplexer is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The Logic equations for the outputs are show below :

$Z_a = \overline{E}\ 0 \bullet (I1a \bullet S + I0a \bullet \overline{S})$

$Z_b = \overline{E}\ 0 \bullet (I1b \bullet S + I0b \bullet \overline{S})$

$Z_c = \overline{E}\ 0 \bullet (I1c \bullet S + I0c \bullet \overline{S})$

$Z_d = \overline{E}\ 0 \bullet (I1d \bullet S + I0d \bullet \overline{S})$

When the Output Enable Input ($\overline{E}\ 0$) is HIGH, the out-

puts are forced to a high impedance "off" state. If the outputs of the 3-state are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers shoud ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

TRUTH TABLE

Output Enable	Select Input	Data Inputs		Outputs
$\overline{E}_0$	S	I_0	I_1	Z
H	X	X	X	(Z)
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(Z) = High impedance (off)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits Min.	Limits Typ. (*)	Limits Max.	Test Condition (note 1)	Unit
V_{IH}	Input HIGH Voltage		2.0			Guaranteed Input HIGH Voltage	V
V_{IL}	Input LOW Voltage				0.8	Guaranteed Input LOW Voltage	V
V_{CD}	Input Clamp Diode Voltage			- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA	V
V_{OH}	Output HIGH Voltage		2.4	3.1		V_{CC} = MIN, I_{OH} = - 2.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table	V
V_{OL}	Output LOW Voltage			0.25	0.4	I_{OL} = 12 mA; V_{CC} = MIN	V
				0.35	0.5	I_{OL} = 24 mA; V_{IN} = V_{IH} or V_{IL} per Truth Table	V
I_{OZH}	Output Off Current-HIGH				20	V_{CC} = MAX, V_{OUT} = 2.7 V,	µA
I_{OZL}	Output Off Current-LOW				- 20	V_{CC} = MAX, V_{OUT} = 0.4 V,	µA
I_{IH}	Input HIGH Current	Other Inputs			20	V_{CC} = MAX, V_{IN} = 2.7 V	µA
		S Inputs			40		
		Other Inputs			0.1	V_{CC} = MAX, V_{IN} = 7.0 V	mA
		S Inputs			0.2		
I_{IL}	Input LOW Current	Other Inputs			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V	mA
		S Inputs			- 0.8		
I_{OS}	Output Short Circuit Current (note 2)		- 30		- 130	V_{CC} = MAX, V_{OUT} = 0 V	mA
I_{CC}	Power Supply Current					V_{CC} = MAX	mA
	Total, Output HIGH				7		
	Total, Output LOW				14		
	Total, Output 3-state				19		

Notes : 1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		8 11	18 18	fig. 1	V_{CC} = 5.0 V C_L = 45 pF R_L = 667 Ω	ns
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		15 18	21 25	fig. 1		ns
t_{PZH}	Output Enable Time to HIGH Level		18	30	figs. 4, 5		ns
t_{PZL}	Output Enable Time to LOW Level		18	30	figs. 3, 5		ns
t_{PLZ}	Output Disable Time from LOW Level		16	25	figs. 3, 5	V_{CC} = 5.0 V C_L = 5 pF	ns
t_{PHZ}	Output Disable Time from HIGH Level		18	30	figs. 4, 5		ns

WAVEFORMS

Figure 1.

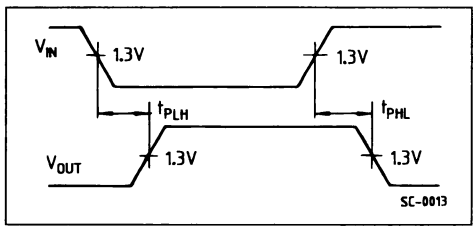


Figure 2.

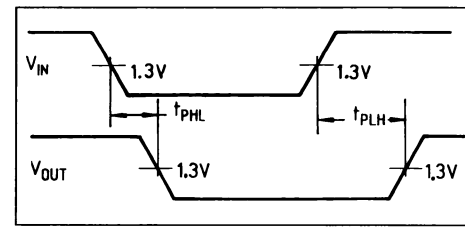


Figure 3.

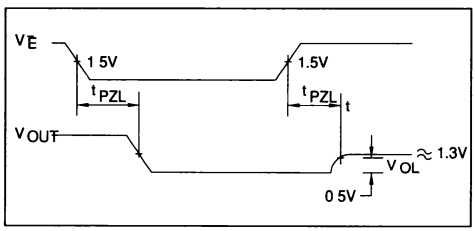


Figure 4.

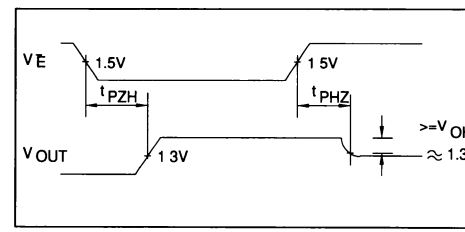
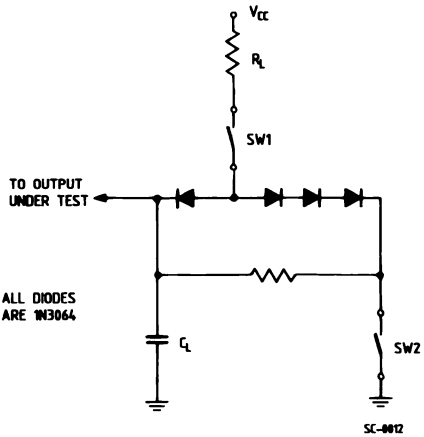


Figure 5.



SWITCHING POSITIONS

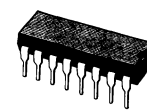
Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

SGS-THOMSON MICROELECTRONICS

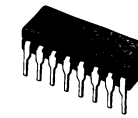
T74LS259

8-BIT ADDRESSABLE LATCH

- SERIAL-TO-PARALLEL CONVERSION
- EIGHT BITS OF STORAGE WITH OUTPUT OF EACH BIT AVAILABLE
- RANDOM (addressable) DATA ENTRY
- ACTIVE HIGH DEMULTIPLEXING OR DECODING CAPABILITY
- EASILY EXPANDABLE
- COMMON CLEAR
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

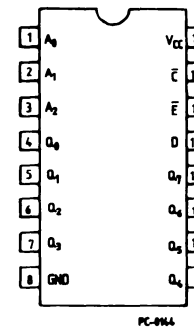
T74LS259 D1 T74LS259 C1
T74LS259 B1 T74LS259 M1

DESCRIPTION

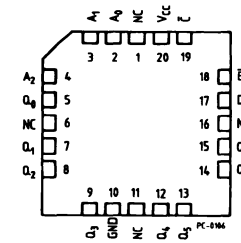
The T74LS259 is a high speed 8-bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunc- tional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW common Clear for resetting all latches, as well as, an active LOW Enables.

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER

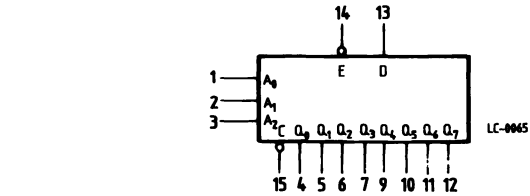


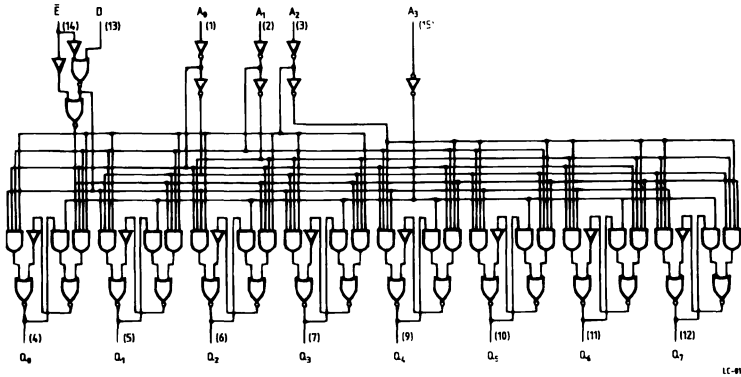
NC = No Internal Connection

PIN NAMES

A_0, A_1, A_2	ADDRESS INPUTS
$\overline{D}$	DATA INPUT
$\overline{E}$	ENABLE (active LOW) INPUT
$\overline{C}$	CLEAR (active LOW) INPUT
Q_0 to Q_7	PARALLEL LATCH OUTPUTS

LOGIC SYMBOL AND LOGIC DIAGRAM





V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	30	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only oand functional operation to the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS259XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

TRUTH TABLE - PRESENT OUTPUT STATES AND MODE SELECTION

$\overline{C}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Mode
L	H	X	X	X	X	L	L	L	L	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	L	L	L	L	L	Demultip
L	L	H	L	L	L	H	L	L	L	L	L	L	⊵	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
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L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{n-1} ⟶								Memory
H	L	L	L	L	L	L	Q_{n-1}	Q_{n-1}	Q_{n-1} ⟶					Addressa
H	L	H	L	L	L	H	Q_{n-1}	Q_{n-1} ⟶						Latch
H	L	L	H	L	L	Q_{n-1}	L	Q_{n-1} ⟶						
H	L	H	H	L	L	Q_{n-1}	H	Q_{n-1} ⟶						
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H	L	L	H	H	H	Q_{n-1} ⟶						Q_{n-1}	L	
H	L	H	H	H	H	Q_{n-1} ⟶						Q_{n-1}	H	

$\overline{E}$	$\overline{C}$	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH Eight-Channel Demultiplexer
H	L	Clear

X = Don't Care
L = LOW Voltage Level
H = HIGH Voltage Level
Qn-1 = Previous Output State

FUNCTIONAL DESCRIPTION

The LS259 has four modes of operation as shown in the mode selection table. In the addressable latch mode, data on the Data line (D) is written into the addressed latch. The address latch will follow three data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address input. In one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other inputs in the LOW stae. In the clear mode all outputs are LOW and unaffected by the address and data inputs.

When operating the LS259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode. The truth table below summarizes the operations of the LS259.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for all Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for all Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.4	3.1		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current $\overline{A_0}$, A_1, A_2, D, $\overline{C}$, $\overline{E}$			 20 40	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	Input HIGH Current $\overline{A_0}$, A_1, A_2, D, $\overline{C}$, $\overline{E}$			 0.1 0.2	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current $\overline{A_0}$, A_1, A_2, D, $\overline{C}$, $\overline{E}$			 - 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Supply Current		20	36	V_{CC} = MAX		mA

Notes: 1. Conditions for testing, notshown in the table are chosen to guarantee operationunder "worst case" conditions.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

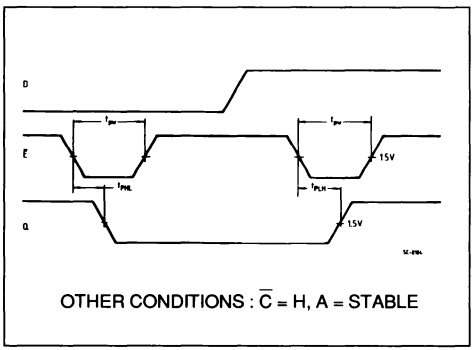
Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Turn-off Delay, Enab. to Out. Turn-on Delay, Enab. to Out.		22 15	35 24	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PLH} t_{PHL}	Turn-off Delay, Data to Output Turn-on Delay, Data to Output		 20 13	 32 21	Fig. 2		ns
t_{PLH} t_{PHL}	Turn-off Delay, Addr. to Out. Turn-on Delay, Addr. to Out.		24 18	38 29	Fig. 3		ns
t_{PHL}	Turn-on Delay, Clear to Output		 17	 27	Fig. 5		ns

AC SET-UP REQUIREMENTS: T_A = 25°C

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
t_sH	Set-up Time HIGH, Data to Enable	20	13		Fig.4	VCC = 5.0 V	ns
t_nH	Hold Time HIGH, Data to Enable	0	– 7.0				
t_sH	Set-up Time LOW, Data to Enable	15	7.0				ns
t_nH	Hold Time LOW, Data to Enable	0	10				
t_sA-$\overline{E}$	Set-up Time, Address to Enable (note 4)	0	– 7.0		Fig.6		ns
$t_{pw}\overline{E}$	Enable Pulse Widht	17	12		Fig.1		ns

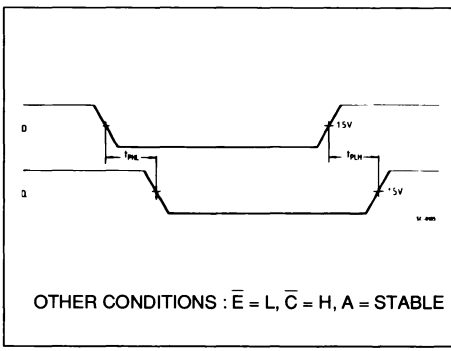
AC WAVEFORMS

Figure 1 : Turn-On and Turn-Off Delays, Enable Output and Enable Pulse Width.



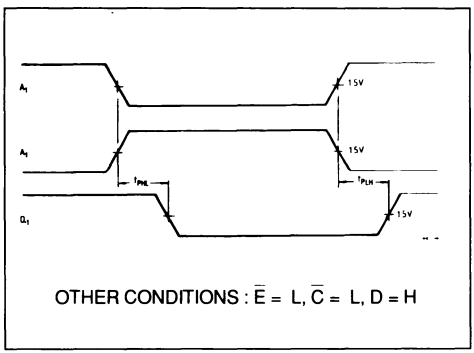
OTHER CONDITIONS : $\overline{C}$ = H, A = STABLE

Figure 2 : Turn-On and Turn-Off Delays, Data to Output.



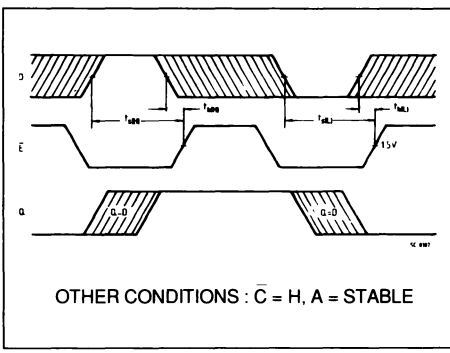
OTHER CONDITIONS : $\overline{E}$ = L, $\overline{C}$ = H, A = STABLE

Figure 3 : Turn-On and Turn-Off Delays, Address to Output.



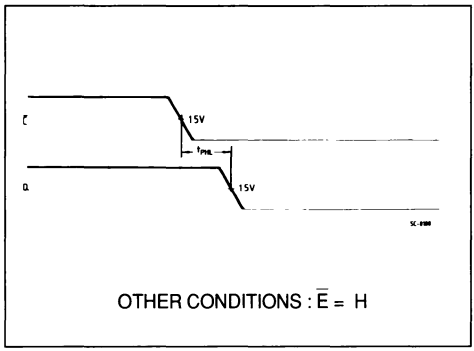
OTHER CONDITIONS : $\overline{E}$ = L, $\overline{C}$ = L, D = H

Figure 4 : Set-up and Hold Time, Data to Enable



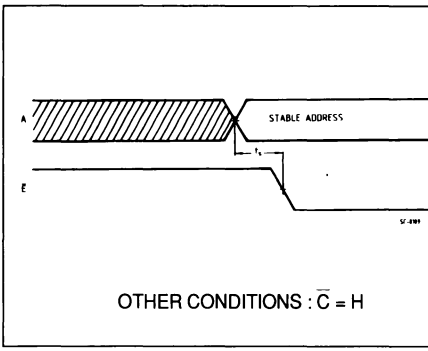
OTHER CONDITIONS : $\overline{C}$ = H, A = STABLE

Figure 5 : Turn-On Delay Clear to Output.



OTHER CONDITIONS : $\overline{E}$ = H

Figure 6 : Set-up Time, Address to Enable (see notes 4 and 5).



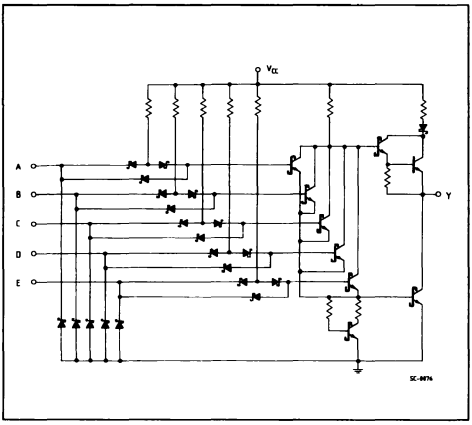
OTHER CONDITIONS : $\overline{C}$ = H

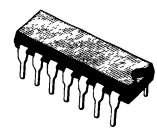
DUAL 5-INPUT NOR GATE

DESCRIPTION

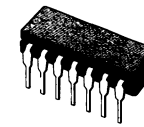
The T74LS260 is a high speed DUAL 5-INPUT NOR GATE fabricated in LOW POWER SCHOTTKY technology.

SCHEMATIC DIAGRAM





B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

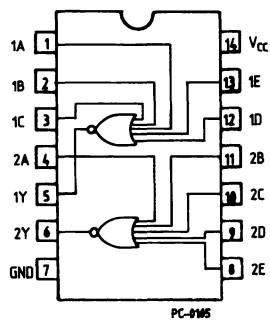
C1
(Plastic Chip Carrier)

ORDER CODES :

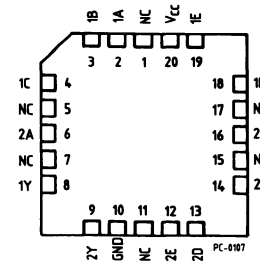
T74LS260 D1	T74LS260 C1
T74LS260 B1	T74LS260 M1

PIN CONNECTION (top view)

DUAL IN LINE

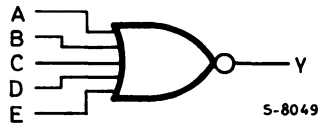


CHIP CARRIER



NC = No Internal Connection

SCHEMATIC DIAGRAM



A	B	C	D	E	Y
L	L	L	L	L	H
X	X	X	X	H	L
X	X	X	H	X	L
X	X	H	X	X	L
X	H	X	X	X	L
H	X	X	X	X	L

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS260XX	4 75 V	5 0 V	5 25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)	Unit
		Min.	Typ. (*)	Max.		
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Treshold Voltage for all Input	V
V_{IL}	Input LOW Voltage			0 8	Guaranteed Input LOW Treshold Voltage for all Input	V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA	V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IL}	V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = 2.0 V	V
			0 35	0.5	I_{OL} = 8.0 mA; V_{CC} = MIN, V_{IN} = 2.0 V	V
I_{IH}	Input HIGH Current		0.1	20	V_{CC} = MAX, V_{IN} = 2.7 V	µA
				0.1	V_{CC} = MAX, V_{IN} = 7.0 V	mA
I_{IL}	Input LOW Current			- 0.36	V_{CC} = MAX, V_{IN} = 0.4 V	mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V	mA
I_{CCH}	Supply Current HIGH			4.0	V_{CC} = MAX, V_{IN} = 0 V	mA
I_{CCL}	Supply Current LOW			5 5	V_{CC} = MAX, Inputs Open	mA

Notes : 1 Conditions for testing, not shown in the table, are chosen to guarantee under "worst case" conditions
2 Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

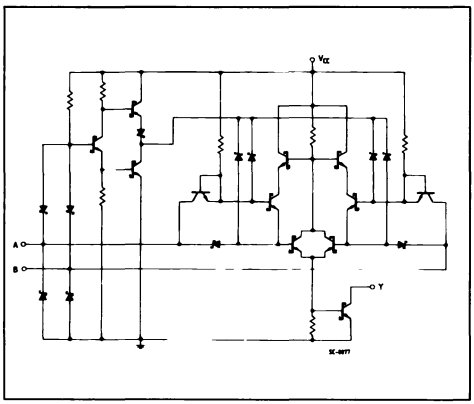
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		5.0	15	V_{CC} = 5.0 V	ns
t_{PHL}	Turn On Delay. Input to Output		6.0	15	C_L = 15 pF	ns

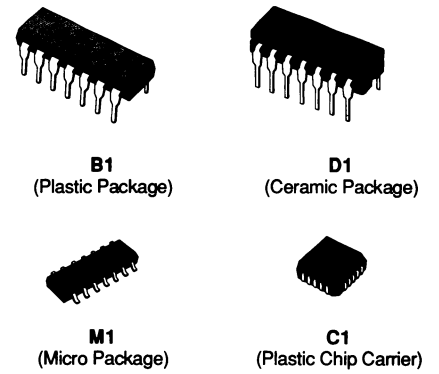
QUAD 2-INPUT EXCLUSIVE NOR GATE

DESCRIPTION

The T74LS266 is a high speed QUAD 2-INPUT EXCLUSIVE NOR GATE (with open collector output)fabricated in LOW POWER SCHOTTKY technology.

SCHEMATIC





B1
(Plastic Package)

D1
(Ceramic Package)

M1
(Micro Package)

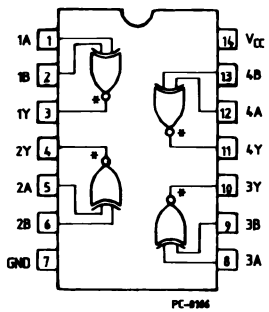
C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS266 D1	T74LS266 C1
T74LS266 B1	T74LS266 M1

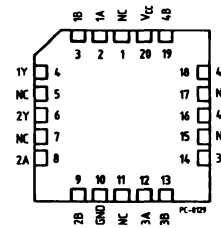
PIN CONNECTION (top view)

DUAL IN LINE



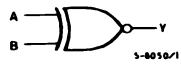
* Open Collector Output

CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE



In		Out
L	L	H
L	H	L
H	L	L
H	H	H

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 1.5 to 15	V
V_O	Output Voltage, Applied to Output	0 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	60	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS266XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
I_{OH}	Output HIGH Current			100	V_{CC} = MIN, V_{OH} = 5.5 V V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current			40 0.2	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.6	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{CC}	Power Supply Current		8.0	13	V_{CC} = MAX		mA

Notes : 1 For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating range.
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C

AC CHARACTERISTICS: $T_A = 25^{\circ}C$ (for AC test circuits and waveforms see databook introduction)

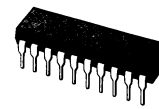
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay, Other Input LOW		18 18	30 30	VCC = 5.0 V C_L = 15 pF, R_L = 2 kΩ	ns
t_{PLH} t_{PHL}	Propagation Delay, Other Input HIGH		18 18	30 30		ns

8-BIT REGISTER WITH CLEAR

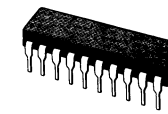
- 8-BIT HIGH SPEED REGISTER
- PARALLEL REGISTER
- COMMON CLOCK AND MASTER RESET
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

DESCRIPTION

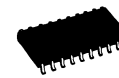
The T74LS273 is a high speed 8-Bit Register. The register consists of eight D-Type Flip-flops with a Common Clock and an asynchronous active LOW Master Reset. This device is supplied in a 20-pin package featuring 0.3 inch lead spacing.



B1
(Plastic Package)



D1
(Ceramic Package)



M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

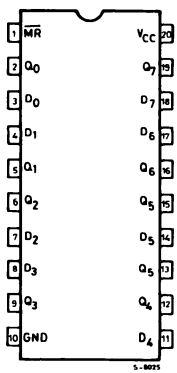
T74LS273 D1 T74LS273 C1
T74LS273 B1 T74LS273 M1

PIN NAMES

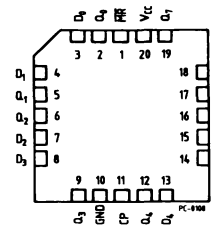
CP	CLOCK (active HIGH going edge) INPUT
$\underline{D_0}$-D_7	DATA INPUTS
$\overline{MR}$	MASTER RESET (active LOW) INPUT
Q_0-Q_7	REGISTER OUTPUTS

PIN CONNECTION (top view)

DUAL IN LINE

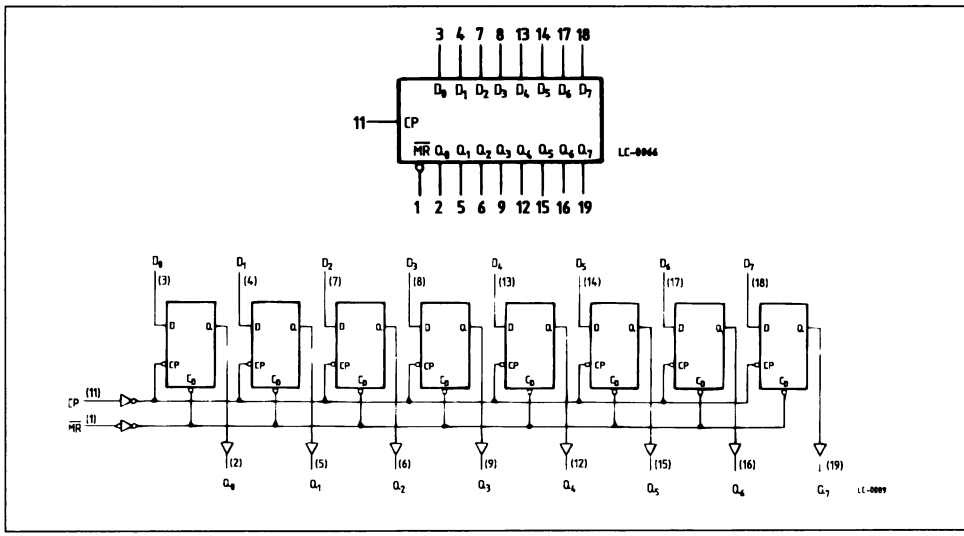


CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The LS273 is an 8-Bit Parallel Register with a common Clock and common Master Reset.

When the MR is LOW, the Q output are LOW, independent of the other inputs. Information meeting the set-up and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input.

TRUTH TABLE

$\overline{MR}$	CP	D_x	Q_x
L	X	X	L
H	⌐	H	H
H	⌐	L	L

H = HIGH Logic Level
L = LOW Logic Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	− 0 5 to + 7	V
V_i	Input Voltage. Applied to Input	− 0 5 to + 15	V
V_O	Output Voltage, Applied to Output	− 0.5 to + 10	V
I_I	Input Current. Into Inputs	− 30 to + 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS273XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for all Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for all Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN	V
			0 35	0.5	I_{OL} = 8.0 mA	V_{IN} = V_{IH} or V_{IL} per Truth Table	V
I_{IH}	Input HIGH Current			20	V_{CC} = MAX, V_{IN} = 2.7 V		µA
				0.1	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0 4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Supply Current		17	27	V_{CC} = MAX		mA

Notes : 1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
2) Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		17 18	27 27	fig. 1	V_{CC} = 5.0 V	ns
t_{PHL}	Propagation Delay, MR to Q Output		18	27	fig 1		ns
f_{MAX}	Maximum Input Clock Frequency	30	40		fig 2		MHz

AC SET-UP REQUIREMENTS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
t_w(CP)	Minimum Clock Pulse Width	20			fig. 1	V_{CC} = 5.0 V	ns
t_s	Set-up Data to Clock (high or low)	20			fig. 1		ns
t_h	Hold Time, Data to Clock (high or low)	5			fig. 1		ns
t_{rec}	Recovery Time	25			fig. 2		ns
t_WMR	Minimum MR Pulse Width	20			fig 2		ns

DEFINITION OF TERMS :

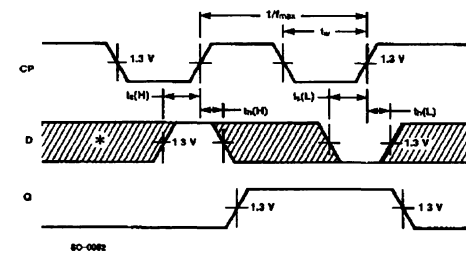
SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) - is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) - is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

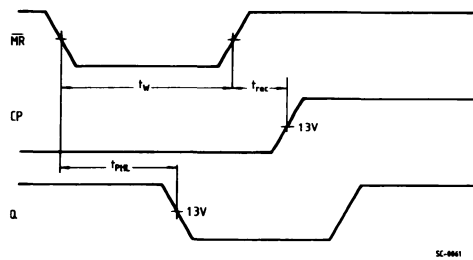
AC WAVEFORMS

Figure 1 :Clock to Output Delays, Clock Pulse Width, Frequency, Set-Up and Hold Times Data to Clock.



* The shaded areas indicate when the input is permitted to change for predictable output performance

Figure 2 :Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time.

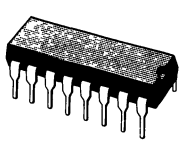


* The shaded areas indicate when the input is permitted to change for predictable output performance

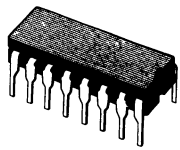
QUAD SET - RESET LATCH

DESCRIPTION

The T74LS279 is a high speed QUAD SET-RESET LATCH fabricated in LOW POWER SCHOTTKY technology.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

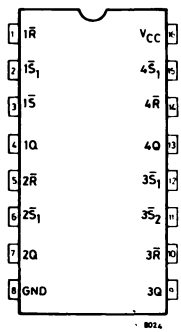
C1
(Plastic Chip Carrier)

ORDER CODES :

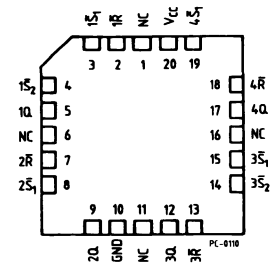
T74LS279 D1	T74LS279 C1
T74LS279 B1	T74LS279 M1

PIN CONNECTION (top view)

DUAL IN LINE

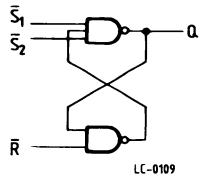


CHIP CARRIER

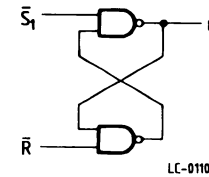


NC = No Internal Connection

LOGIC DIAGRAMS



LC-0109



LC-0110

TRUTH TABLE

INPUTS			OUTPUT
$\overline{S}_1$	$\overline{S}_2$	R	(Q)
L	L	L	h
L	X	H	H
X	L	H	H
H	H	L	L
H	H	H	No Change

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
h = T he output is HIGH as long as S_1 or S_2 is LOW If all inputs go HIGH simultaneously, the output state is indetermintate, otherwise, it follows the Truth Table.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0 5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS279XX	4.75 V	5 0 V	5 25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Input		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Input		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CC}	Power Supply Current		3.8	7.0	V_{CC} = MAX		mA

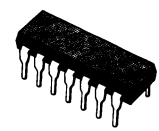
Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating conditions for the device type.
2. Not more that one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C

AC CHARACTERISTICS : T_A = 25 °C (see page 576 for AC test circuit and waveforms)

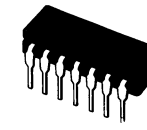
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{S}$ to Output		12 13	22 21	V_{CC} = 5.0 V	ns
t_{PHL}	Propagation Delay, $\overline{R}$ to Output		15	27	C_L = 15 pF	ns

9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

- GENERATES EITHER ODD OF EVEN PARITY FOR NINE DATA LINES
- CASCADABLE FOR n-BIT
- TYPICAL DATA TO OUTPUT DELAY OF ONLY 33 ns
- CAN BE USED TO UPGRADE SYSTEMS USING MSI PARITY CIRCUITS
- TYPICAL DISSIPATION = 80 mW



B1
(Plastic Package)



D1
(Ceramtic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

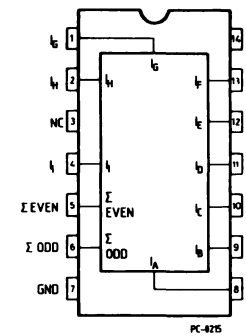
T74LS280 D1 T74LS280 C1
T74LS280 B1 T74LS280 M1

DESCRIPTION

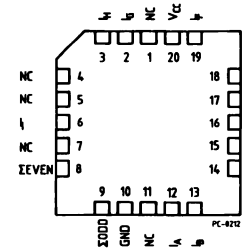
The T74LS280 is a (universal) 9-Bit Odd-Even Parity Generator/Checker. It is composed of odd/even outputs to facilitate either odd or even parity. By cascading, the word length can be easily expanded. The LS280 has no expander input implementation, but the corresponding function is supplied by an input at pin 4 and the absence of any connection at pin 3. This configuration allows the LS280 to be a replacement for the LS180 which results in improved performance. The LS280 has buffered inputs to reduce the drive requirements to onee LD unit load.

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



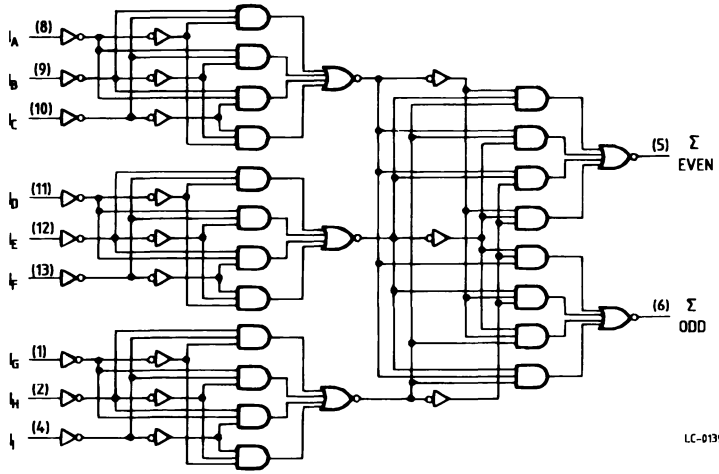
NC = No Internal Connection

FUNCTION TABLE

Number of Inputs a Thru 1 that are High	Outputs Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

FUNCTIONAL BLOCK DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stsress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS280XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Treshold Voltage for all Input		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Treshold Voltage for all Input		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX		mA
I_{CC}	Power Supply Current			27	V_{CC} = MAX		mA

Notes 1. For Conditions shown as MIN or MAX,use the appropriate value specified under guarantee operating range.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C

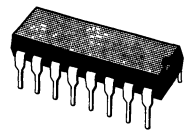
AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay, Σ EVEN		33 29	50 45	V_{CC} = 5.0 V Input not under test at 0.V C_L = 15 pF	ns
t_{PHL} t_{PLH}	Propagation Delay, Σ ODD		23 31	35 50		ns

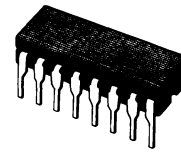
4–BIT BINARY FULL ADDER WITH FAST CARRY

DESCRIPTION

The T74LS283 is a high speed 4-bit Binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words (A_1 - A_4, B_1 - B_4) and a Carry Input (C_{IN}). It generates the binary Sum outputs (S_1 - S_4) and the Carry Output (C_{OUT}) from the most significant bit. The LS283 operates with either active HIGH or active LOW operands (positive or negative logic).



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

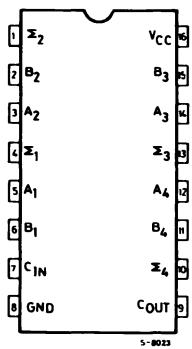
T74LS283 D1 T74LS283 C1
T74LS283 B1 T74LS283 M1

PIN NAMES

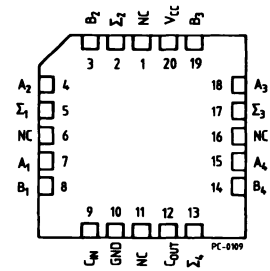
A_1-A_4	OPERAND A INPUTS
B_1-B_4	OPERAND B INPUTS
C_{IN}	CARRY INPUTS
Σ_1-Σ_4	SUM OUTPUTS
C_{OUT}	CARRY OUTPUTS

PIN CONNECTION (top view)

DUAL IN LINE

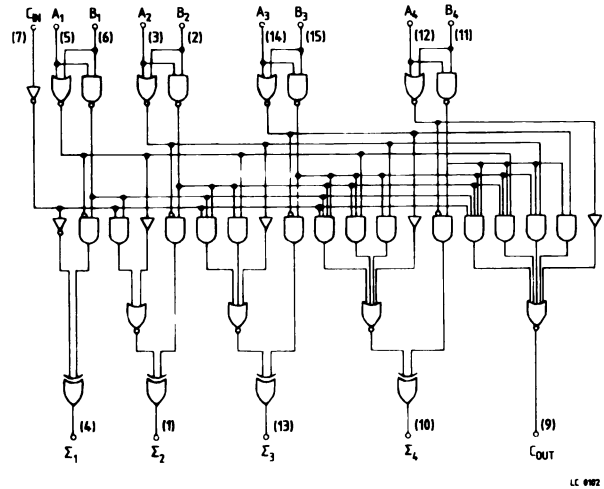


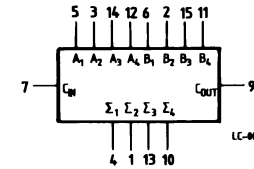
CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM





VCC=Pin 16

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS283XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

FUNCTIONAL DESCRIPTION

The LS283 adds two 4–bits binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs (Σ_1 - Σ_4) and outgoing carry (C_{OUT}) outputs.

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\,\Sigma_2 + 4\,\Sigma_3 + 8\,\Sigma_4 + 16\,C_{OUT}$$

Where : (+) = plus

Due to the symmetry of the binary add function the LS283 can be used with either all input and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH inputs, Carry In can not be left open, but must be held LOW when no carry in is intended.

Example :

	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

(10 + 9 = 19)
(carry + 5 + 6 = 12)
Interchanging inputs of equal weight does not affect operation, thus C_{IN}, A_1, B_1, can be arbitrarily assigned to pins 7, 5, or 3

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Input		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Input		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0 4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current C_{IN} Any A or B			 20 40	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	C_{IN} Any A or B			0.1 0.2	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current C_{IN} Any A or B			 - 0.4 - 0.8	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CC}	Power Supply Current		22 19	39 34	V_{CC} = MAX, All Inputs 0 V V_{CC} = MAX, A Input 4.5 V		mA

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
2. Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay, C_{IN} Input to Any Σ Output		16 15	24 24	V_{CC} = 5.0 V C_L = 15 pF Figures 1 and 2	ns
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to Σ Outputs		15 15	24 24		ns
t_{PLH} t_{PHL}	Propagation Delay, C_{IN} Input to C_{OUT} Output		11 11	17 22		ns
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to C_{OUT} Output		11 12	17 17		ns

AC WAVEFORMS

Figure 1.

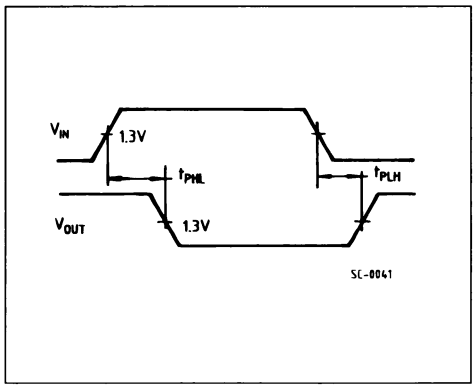
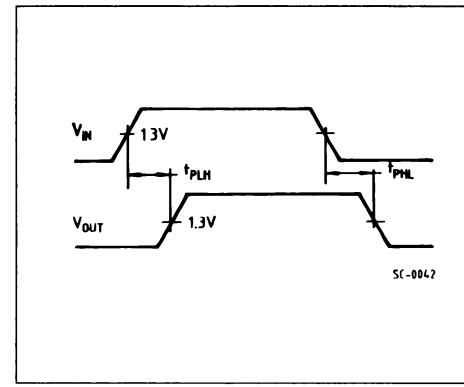


Figure 2.

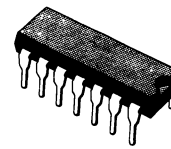


SGS-THOMSON
MICROELECTRONICS

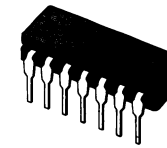
T74LS290
T74LS293

LS290-DECADE COUNTER
LS293-4-BIT BINARY COUNTER

- CORNER POWER PIN VERSION OF THE LS90 AND LS93
- LOW POWER CONSUMPTION... TYPICALLY 45mW
- HIGH CUNT RATES... TYPICALLY 50MHZ
- CHOICE OF COUNTING MODES... BCD, BI-QUINARY, BINARY
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :
T74LSXXX74LSXXX C1
T74LSXXX74LSXXX M1

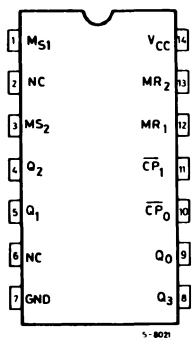
DESCRIPTION

The T74LS290 and T74LS293 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS290) or divided-by-eight (LS293) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to $\overline{CP}$) to form BCD, Bi-quinary, or Modulo-16 counters. Both of the counters have a 2-input gated Master Reset (Clear), and the LS90 also has a 2-input gated Master Set (Preset 9).

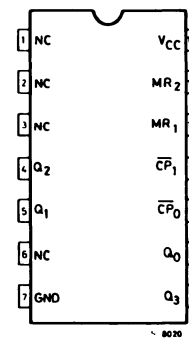
PIN CONNECTION (top view)

DUAL IN LINE

LS290



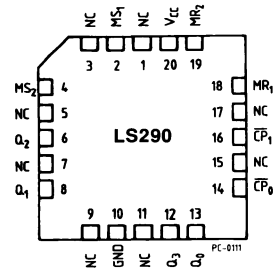
LS293

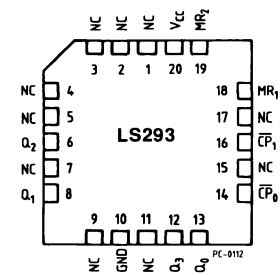


PIN NAMES

$\overline{CP}_0$	CLOCK (active LOW going edge) INPUT TO ÷ 2 SECTION
$\overline{CP}_1$	CLOCK (active LOW going edge) INPUT TO ÷ 5 SECTION (LS290)
$\overline{CP}_1$	CLOCK (active LOW going edge) INPUT TO ÷ 8 SECTION (LS293)
MR_1, MR_2	MASTER RESET (clear) INPUTS
MR_1, MR_2	MASTER RESET (preset-9 LS290) INPUTS
Q_0	OUTPUT FROM - 2 SECTION
Q_1, Q_2, Q_3	OUTPUTS FROM - 5 & - 8 SECTIONS

CHIP CARRIER





NC = No Internal Connection

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, for $\overline{CP}$	– 0.5 to 5.5	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

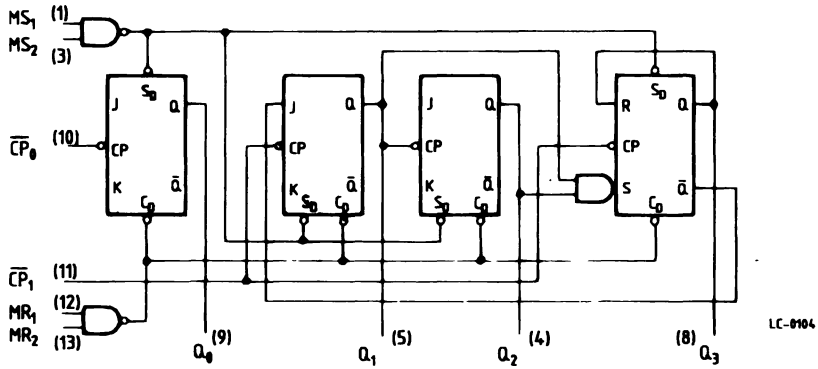
GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS290/293XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

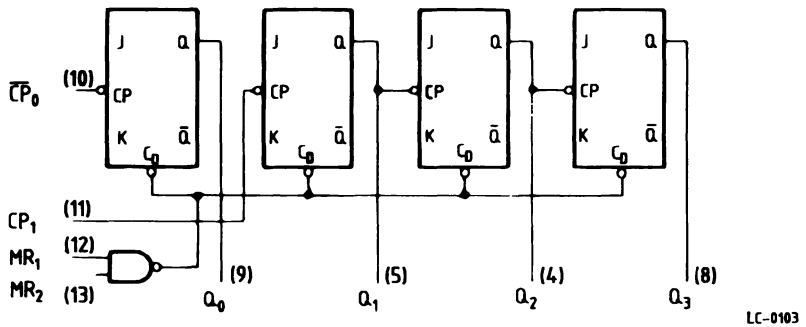
XX = package type

LOGIC DIAGRAMS

LS290

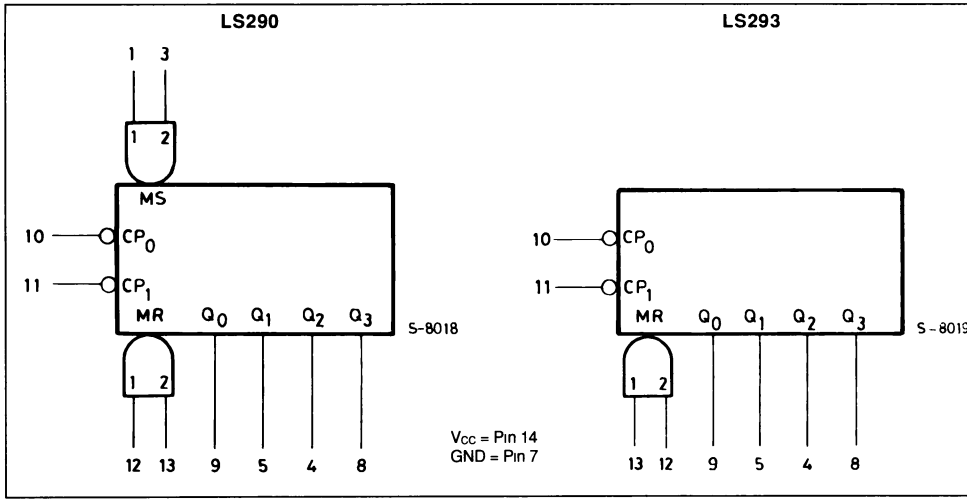


LS293



V_{CC} = Pin 14
GND = Pin 7
() = Pin numbers

LOGIC SYMBOL



FUNCTIONAL DESCRIPTION

The LS290 and LS293 are 4-bit ripple Decade, and 4-bit Binary counters respectively. Each device consists of four master/slave flip-flops wich are internally connected to provide a divide-by-two section and divide-by-five (LS290) or divide-by-eight (LS293) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outpouts do not occur simultaneously because of internal ripple delays. Therefore, decoded outpout signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 outpout of each device is designed and specified to drive the rated fan-out plus the $\overline{CP1}$ input of device.

A gated AND asynchronous Master Reset (MR1.MS2) is provided on both counters wich overrides the clocks and resets (clears) all the flip-flops. A gated AND asynchronous master Set ($MS_1.MS_2$) is provid on the LS290 which overrides the clocks and the MR inputs and sets the ouptuts to nine (HLLH).

Since the outpout from the devide-by-two section is not internally connected to the succeding stages, the devices may be operated in various counting modes :

LS290

A. BCD Decade (8421) Counter-the $\overline{CP_1}$ input mus tbe externally connected to the Q_0 outpout. The CP_0 input receives the incoming count and BCD count sequence is produced.

B. Symmetricel Bi-quinary Divide-By-Ten Counter -The Q_3 outpout must be externally connected to the $\overline{CP_0}$ input. The input count is then applied to the $\overline{CP_1}$ input and a divide-by-ten square is obtenaidat outpout Q_0.

C. Divide-By-Two and Divide-By-Five Counter-No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two functions ($\overline{CP_0}$ as the input and Q_0 as the outpout). The $\overline{CP_1}$ input is used to obtain binary divide-by-five operation at the Q_3 outpout.

LS293

A. 4-Bit Ripple Counter-The outpout Q_0 must be externally connected to input $\overline{CP_1}$ The input count pulses are applied to input $\overline{CP_0}$. Simultaneous division of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outpouts as shown in the truth table.

B. 3-Bit Ripple Counter-The input count pulses are applied to input $\overline{CP_1}$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_0, Q_1, Q_2, and Q_3 outpouts. Independent us of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

BCD COUNT SEQUENCE LS290

Count	Output			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

Note : Output Q_0 is Connected to Input CP1 for BCD Count.

MODE SELECTION LS290

Reset/Set Inputs				Outputs			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

TRUTH TABLE LS293

Count	Output			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Note : Output Q_0 is Connected to Input CP1

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

MODE SELECTION LS293

Reset Inputs		Outputs			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0 8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0 25	0 4	I_{OL} = 4 0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current MS, MR $\overline{CP_0}$ $\overline{CP_1}$ (LS290) $\overline{CP_1}$ (LS293)			 20 40 80 40	V_{CC} = MAX, V_{IN} = 2 7 V		µA
	MS, MR $\overline{CP_0}$ $\overline{CP_1}$ (LS290) $\overline{CP_1}$ (LS293)			0.1 0.2 0.4 0.2	V_{CC} = MAX, V_{IN} = 5.5 V		mA
I_{IL}	Input LOW Current MS, MR $\overline{CP_0}$ $\overline{CP_1}$ (LS290) $\overline{CP_1}$ (LS293)			 - 0.4 - 2.4 - 3.2 - 1.6	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		9	15	V_{CC} = MAX		mA

Notes : 1 Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
2 Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C

AC SET-UP REQUIREMENTS: T_A = 25 °C, V_{CC} = 5.0 V

Symbol	Parameter	Limits				Note	Units
		LS290		LS293			
		Min.	Max.	Min.	Max.		
t_W	$\overline{CP_0}$ Pulse Width	15		15		Fig. 1	ns
t_W	CP_1 Pulse Width	30		30		Fig 1	
t_W	MR Pulse Width	30		30		Fig. 2	
t_W	MS Pulse Width	30				Fig 2, 3	
t_{rec}	Recovery Time MR to $\overline{CP}$	25		25		Fig. 2	
t_{rec}	Recovery Time MS to $\overline{CP}$	25				Fig. 2, 3	

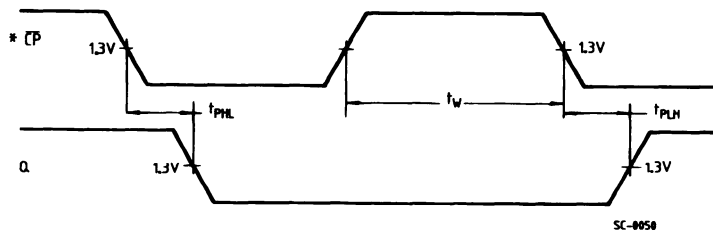
RECOVERY TIME (trec) - is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH to LOW in order to recognize and transfer HIGH data to Q output

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits				Test Conditions		Unit
		LS290		LS293				
		Min.	Max.	Min.	Max.			
f_{MAX}	$\overline{CP}_0$ Input Count Frequency	32		32		Fig. 1	V_{CC} = 5.0 V C_L = 15 pF	MHz
f_{MAX}	$\overline{CP}_1$ Input Count Frequency	16		16		Fig. 1		MHz
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_0$ Input to Q_0 Output		16 18		16 18	Fig. 1		ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_1$ Input to Q_1 Output		16 21		16 21			ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_1$ Input to Q_2 Output		32 35		32 35			ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_1$ Input to Q_3 Output		32 35		51 51			ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_0$ Input to Q_3 Output		48 50		70 70			ns
t_{PLH}	MS Input to Q_0 and Q_3 Outputs		30			Fig. 3		ns
t_{PHL}	MS Input to Q_1 and Q_2 Outputs		40			Fig. 2		ns
t_{PHL}	MR Input to any Output		40		40	Fig. 2		ns

AC WAVEFORMS

Figure 1.



* The number of the Clock Pulse Required between the t_{PHL} and t_{PLH} measurements can be determined from the Truth Table

Figure 2.

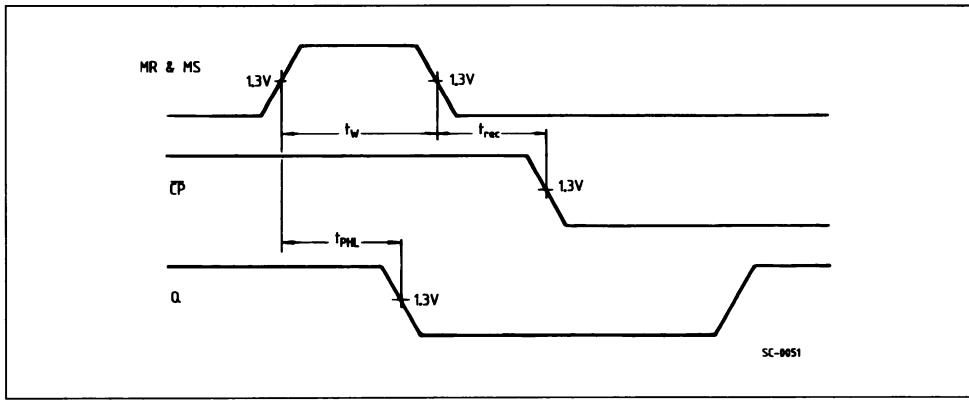
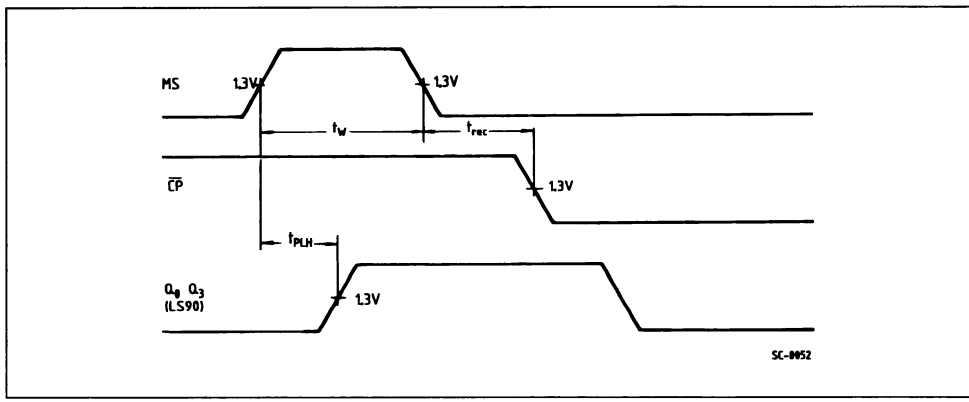
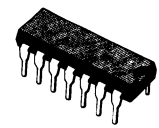


Figure 3.

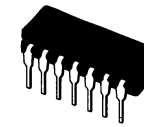


4-BIT SHIFT REGISTER WITH 3-STATE OUTPUTS

- FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS
- NEGATIVE EDGE-TRIGGERED CLOCK INPUT
- PARALLEL ENABLE MODE CONTROL INPUT
- 3-STATE BUSSABLE OUTPUT BUFFERS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS295A D1 T74LS295A C1
T74LS295A B1 T74LS295A M1

DESCRIPTION

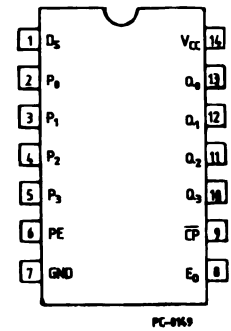
The T74LS295A is a 4-Bit Shift Register with serial and parallel synchronous operating modes, independent 3-state output buffers. The Parallel Enable input (PE) controls the shift-right or parallel load operation. All data transfer and shifting occur synchronously with the HIGH to LOW clock transition.

The 3-State output buffers are controlled by an active HIGH Output Enable input (EO).

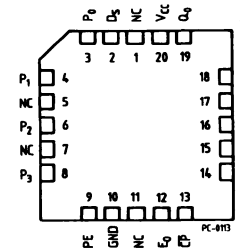
Disabling the output buffers does not affect the shifting or loading of input data, but it does inhibit serial expansion.

The LS295A is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all TTL families.

PIN CONNECTION (top view)
DUAL IN LINE



CHIP CARRIER

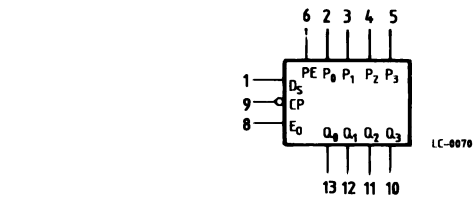


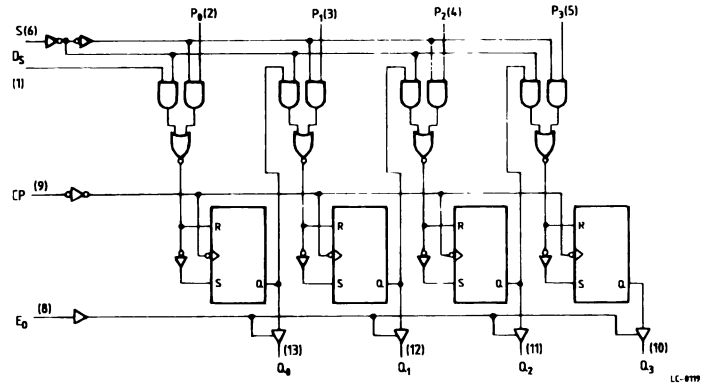
NC = No Internal Connection

PIN NAMES

PE	PARALLEL ENABLE INPUT
D_S	SERIAL DATA INPUT
P_0-P_3	PARALLEL DATA INPUTS
$\underline{E_0}$	OUTPUT ENABLE INPUT
$\overline{CP}$	CLOCK PULSE (active LOW going edge) INPUT
Q_0-Q_3	3-STATE OUTPUTS

LOGIC SYMBOL AND LOGIC DIAGRAM





V_{CC} = Pin 16
GND = Pin 7
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0 5 to 10	V
I_I	Input Current, Into Inputs	– 0.5 to 30	mA
I_O	Output Current, Into Outputs	60	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS295AXX	4 75 V	5 0 V	5.25 V	0 °C to + 70 °C

XX = Package type

TRUTH TABLE - PRESENT OUTPUT STATES AND MODE SELECTION

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS*			
	PE	$\overline{CP}$	D_S	P_n	Q_0	Q_1	Q_2	Q_3
Shift Right	l	⌐	l	X	L	q_0	q_1	q_2
	l	⌐	h	X	H	q_0	q_1	q_2
Parallel Load	h	⌐	X	P_n	P_0	P_1	P_2	P_3

* The indicated data appears at the Q outputs when E_O is HIGH. When E_O is LOW, the indicated data is loaded into the register, but the ouputs are all forced to the high impedance "off" state.

X = Don't Care
L = LOW Voltage Level
H = HIGH Voltage Level

Pn (Qn) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

l = LOW Voltage Level one set-up time prior to the HIGH to LOW clock transition

h = HIGH Voltage Level one set-up time prior to the HIGH to LOW

FUNCTIONAL DESCRIPTION

The LS295A is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a Serial (D_S) and four Parallel Data outputs (P_0-P_3) inputs and four parallel 3-State output buffers (Q_0-Q_3). When the parallel Enable (PE) input is HIGH, data is transferred from the Parallel Data Inputs (P_0-P_3) into the register synchronously with the HIGH to LOW transition of the Clock (CP). When the PE is LOW, a HIGH to LOW transition on the clock transfers the serial data on the D_S input to register Q_0, and shifts data from Q_0 to Q_1, Q_1 to Q_2 and Q_2 to Q_3. The input data and parallel enable are fully edge-triggered and must be stable only one set-up time before the HIGH to LOW clock transition.

The 3-State Output buffers are controlled by an active HIGH Output Enable input (E_0). When the E_0 is HIGH, the four register outputs appear at the Q_0-Q_3 outputs. When E_0 is LOW, the outputs are forced to high impedance "off" state. The 3-State output buffers are completely independent of the register operation, i.e. the input transition on the E_0 input do not affect the serial or parallel data transfers of the register. If the outputs are tied together, all but one devices must be in the high impedance state to avoid high currents that would exceed the maximum rating.

Designers should ensure that Output Enable signals to 3-State devices whose outputs are tied together are designed so there is no overlap.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.4	3.4		V_{CC} = MIN, I_{OH} = - 2.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8 mA		V
I_{OZH}	Output Off Current HIGH			20	V_{CC} = MAX, V_{OUT} = 2.7 V		µA
I_{OZL}	Output Off Current LOW			- 20	V_{CC} = MAX, V_{IN} = 0.5 V		µA
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current Output HIGH		14	23	V_{CC} = MAX, V_{CP} = ⎍⎍ V_E = 4.5 V		mA
	Power Supply Current Output HIGH		14	25	V_{CC} = MAX, V_{CP} = 0 V, V_E = 0 V		mA

Notes : 1. Conditions for testing, not shown in the table are chosen to guarantee operationunder "worst case" conditions.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
f_{MAX}	Shift Frequency	30	45		Fig. 1	V_{CC} = 5.0 V C_L = 15 pF	MHz
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		24 16	30 26	Fig. 1		ns
t_{PZH}	Output Enable Time to HIGH Level		12	18	Figs. 4, 5	C_L = 15 pF R_L = 2 kΩ	ns
t_{PZL}	Output Enable Time to LOW Level		14	20	Figs. 3, 5		ns
t_{PLZ}	Output Disable Time from LOW Level		17	24	Figs. 3, 5	C_L = 5 pF R_L = 2 kΩ	ns
t_{PHZ}	Output Disable Time from HIGH Level		15	20	Figs. 4, 5		ns
t_W(CP)	Clock Pulse Width	20			Fig. 1	V_{CC} = 5.0 V C_L = 15 pF	ns
t_s(Data)	Set-up Time, Data to Clock	20			Fig. 1		ns
t_s(Data)	Hold Time, Data to Clock	10					ns
t_S(PE)	Set-up Time, PE to Clock	20			Fig. 1		ns
t_h(PE)	Hold Time, PE to Clock	0					ns

DEFINITION OF TERMS

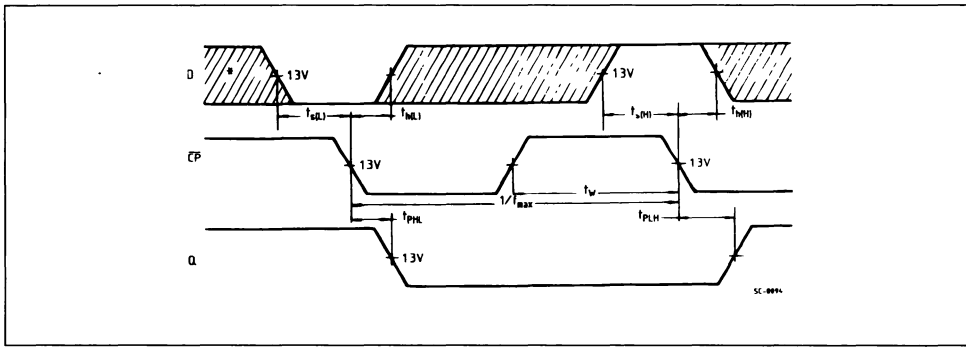
SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) - is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

AC WAVEFORMS

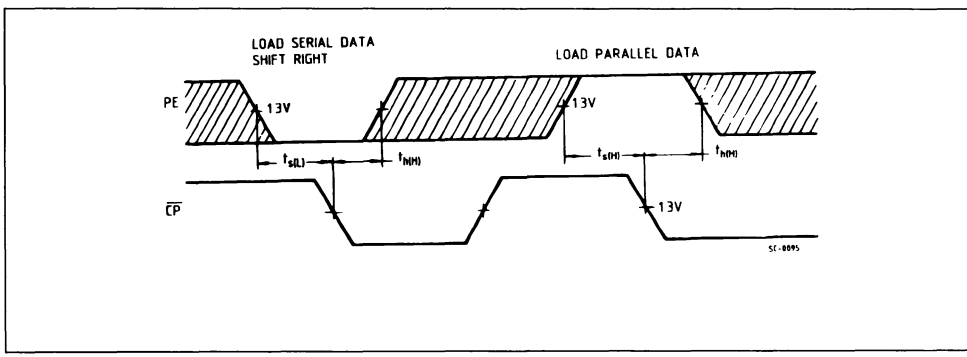
The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 1.



* The data input is D_S for PE = LOW and P_n for PE = HIGH.

Figure 2.



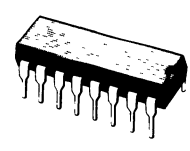
SGS-THOMSON MICROELECTRONICS

T74LS298

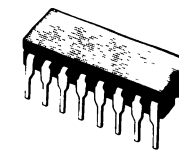
QUAD 2-PORT REGISTER (QUAD 2-INPUT MULTIPLEXER WITH STORAGE)

- SELECT FROM TWO DATA SOURCES
- FULLY EDGE-TRIGGERED OPERATION
- TYPICAL POWER DISSIPATION OF 65 mW
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

LS298 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all TTL families.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS298 D1 T74LS298 C1
T74LS298 B1 T74LS298 M1

DESCRIPTION

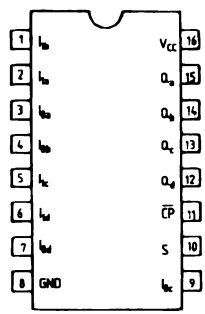
The T74LS298 is a Quad 2-Port Register. It is the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources). The selected data is transferred to the output register synchronously with the HIGH to LOW transition of the Clock input. The

PIN NAMES

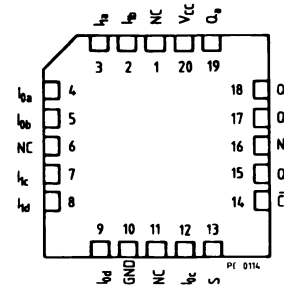
$\overline{S}$	COMMON SELECT INPUT
$\overline{CP}$	CLOCK (active LOW going edge) INPUT
I_{0a-0b}	DATA INPUTS FROM SOURCES 0
I_{1a-1b}	DATA INPUTS FROM SOURCES 1
Q_a-Q_b	REGISTER OUTPUTS

PIN CONNECTION (top view)

DUAL IN LINE

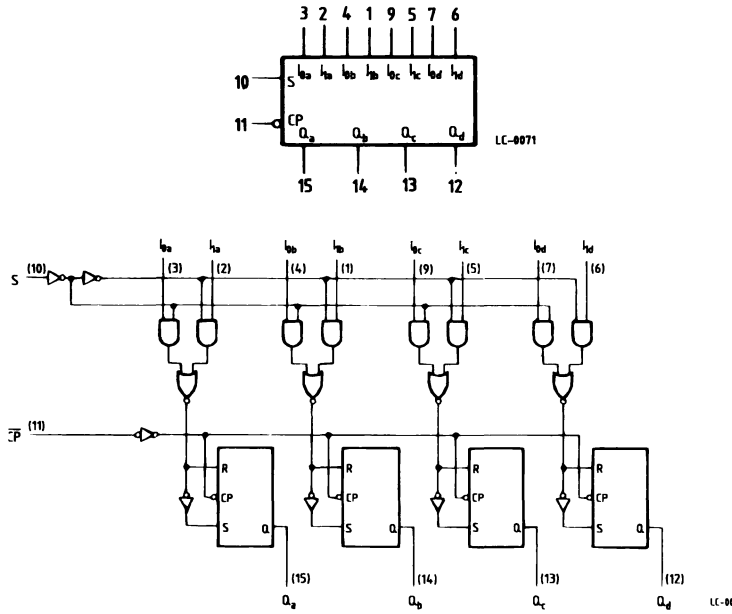


CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS298XX	4.75 V	5 0 V	5.25 V	0 °C to + 70 °C

XX = Package type

TRUTH TABLE - PRESENT OUTPUT STATES AND MODE SELECTION

TRUTH TABLE

Inputs			Output
S	I_0	I_1	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
l = LOW Voltage Level one set-up time prior to the LOW to HIGH clock transition.
h = HIGH Voltage Level one set-up time prior to the LOW to HIGH clock transition.

FUNCTIONAL DESCRIPTION

The LS298 is a high speed Quad 2-Port Register. It selects four bits of data from two sources (ports) under the control of a Common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH to LOW transition of the Clock input (CP). The 4-bit output register is fully edge-triggered. The Data inputs (I) and Select input (S) must be stable only one set-up time prior to the HIGH to LOW transition of the clock for predectable operation.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Treshold Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Treshold Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		13	21	V_{CC} = MAX		mA

Notes : 1 Conditions for testing, not shown in the table are chosen to guarantee operation under "worst case" conditions
2 Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C.

AC CHARACTERISTICS : $T_A = 25\ °C$

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
t_{PLH}	Propagation Delay, Clock to Output		18	27	Fig 1	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$	ns
t_{PHL}	Propagation Delay, Clock to Output		21	32	Fig 1		ns

DEFINITION OF TERMS :

SET-UP TIME (t_s - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

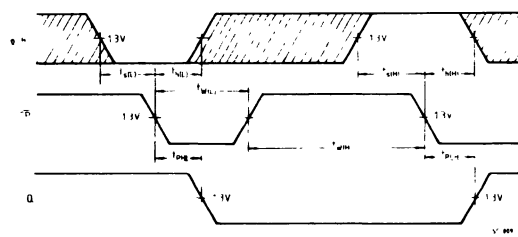
HOLD TIME (t_h) - is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

AC SET-UP REQUIREMENTS : $T_A = 25\ °C$

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
$t_{W(H)}$	Clock Pulse Width (HIGH)	20	11		Fig 1	$V_{CC} = 5.0\ V$	ns
$t_{W(L)}$	Clock Pulse Width (LOW) (HIGH or LOW)	20	11				ns
t_s(data)	Set-up Time, Data to Clock	15	10		Fig. 1		ns
t_h(data)	Hold Time, Data to Clock	5.0	1				ns
t_s(S)	Set-up Time, Select to Clock	25	20		Fig. 2		ns
t_h(S)	Hold Time, Select to Clock	0	− 2				ns

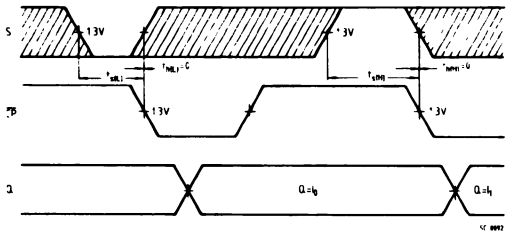
AC WAVEFORMS

Figure 1.



The shaded areas indicate when the input is permitted to change for predictable output performance

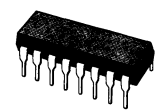
Figure 2.



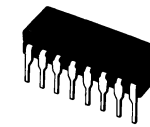
The shaded areas indicate when the input is permitted to change for predictable output performance.

DUAL 4-INPUT MULTIPLEXER

- INVERTED VERSION OF THE 54/74LS153
- SEPARATE ENABLES FOR EACH MULTIPLEXER
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS352 D1 T74LS352 C1
T74LS352 B1 T74LS352 M1

DESCRIPTION

The T74LS352 is a very high speed Dual 4-Input Multiplexer with Common Select inputs and individual Enable inputs for each section. It can select two bits data from the sources. The two buffered outputs present data in the inverted (complementary) form.

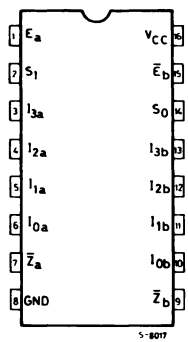
The T74LS352 is the functional equiva-lent of the T74LS153 except with inverted outputs.

PIN NAMES

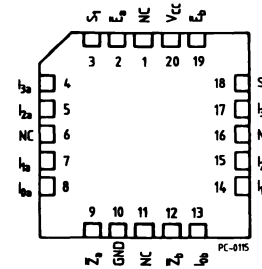
$\overline{S}_0$-S_1	COMMON SELECT INPUTS
$\overline{E}$	ENABLE (active LOW) INPUT
$\overline{I}_0$-I_1	MULTIPLEXER INPUTS
$\overline{Z}$	MULTIPLEXER OUTPUTS

PIN CONNECTION (top view)

DUAL IN LINE

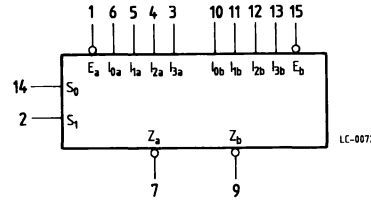


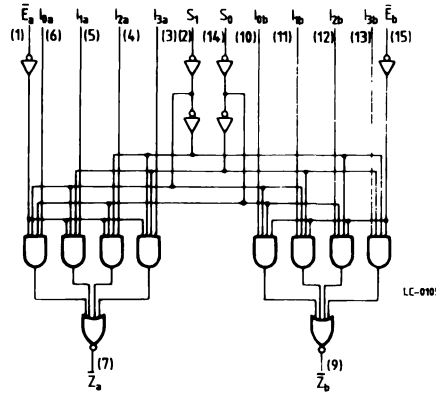
CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM





V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

TRUTH TABLE

Select Inputs		Inputs (a or b)					Ouputs
S_0	S_1	$\bar{E}$	I_0	I_1	I_2	I_3	$\bar{Z}$
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS352XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

FUNCTIONAL DESCRIPTION

The LS352 is a Dual 4-Input Multiplexer. It selects two bits of data from up to four sources under the control of the common Select Inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables (E_a, E_b) which can be used to strobe outputs independently. When the Enable (E_a, E_b) are HIGH, the corresponding outputs (Z_a, Z_b) are forced HIGH.

The logic equations for the outputs are shown below.

$$\overline{Z}_a = \overline{E}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$\overline{Z}_b = \overline{E}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

The LS352 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select Inputs. A less obvious application is a function generator. The LS352 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Input		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Input		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current		1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.36	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CC}	Power Supply Current		6.2	10	V_{CC} = MAX		mA

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
2. Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		19 25	29 38	Fig. 2	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PLH} t_{PHL}	Propagation Delay, Enable to Output		16 21	24 32	Fig. 1		ns
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		13 17	20 26	Fig. 2		ns

AC WAVEFORMS

Figure 1.

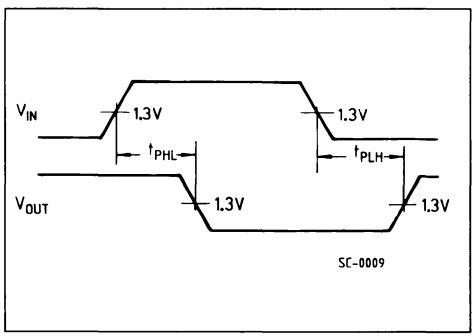
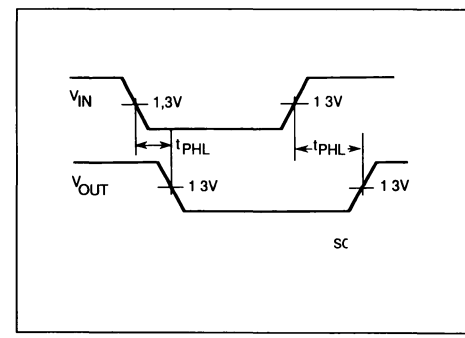
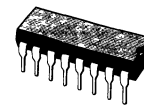


Figure 2.

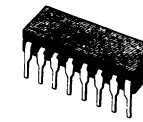


DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

- INVERTED VERSION OF T74LS253
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

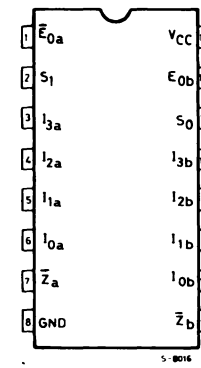
T74LS353 D1 T74LS353 C1
T74LS353 B1 T74LS353 M1

DESCRIPTION

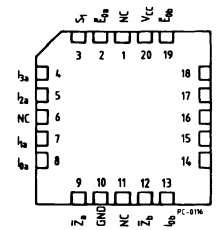
The LSTTL/MSI T74LS353 is a Dual 4-Input Multiplexer with 3-state outputs. It can select two bits data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable (E_0) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all TTL families.

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER

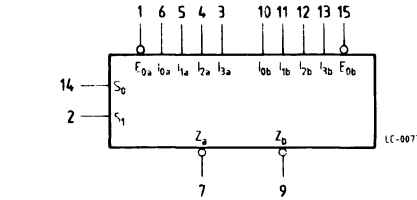


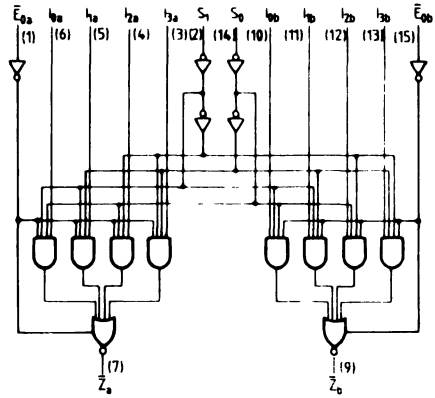
NC = No Internal Connection

PIN NAMES

S_0-S_1	COMMON SELECT INPUTS
MULTIPLEXER A	
E_{0a}	OUTPUT ENABLE (active LOW) INPUT
I_{0a}-I_{3a}	MULTIPLEXER INPUTS
Z_a	MULTIPLEXER OUTPUTS
MULTIPLEXER B	
E_{0b}	OUTPUT ENABLE (active LOW) INPUT
I_{0b}-I_{3b}	MULTIPLEXER INPUTS
Z_b	MULTIPLEXER OUTPUT

LOGIC SYMBOL AND LOGIC DIAGRAM





V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.6 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS353XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

TRUTH TABLE

Select Inputs		Data Inputs				Output Enable	Ouput
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{E}_0$	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(Z) = High Impedance (off)
Address inputs S0 and S1 are common to both sections

FUNCTIONAL DESCRIPTION

The LS353 contains two identical 4-Input Multiplexer with 3-state outputs. They select two bits from four sources selected by common select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable (E_{0a}, E_{0b}) inputs which when HIGH, forces the outputs to a high impedance (high Z) state.

The LS353 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select Inputs. The logic equations for the outputs are shown below.

$$\overline{Z}_a = \overline{\overline{E}_a \cdot (I_{oa} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)}$$

$$\overline{Z}_b = \overline{\overline{E}_b \cdot (I_{ob} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)}$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Outputs Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1 5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.1		V_{CC} = MIN, I_{OH} = - 2.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{OZH}	Output Off Current HIGH			20	V_{CC} = MAX, V_{OUT} = 2.7 V, $\overline{V_E}$ = 2.0 V		µA
I_{OZL}	Output Off Current LOW			- 20	V_{CC} = MAX, V_{OUT} = 0.4 V, $\overline{V_E}$ = 2.0 V		µA
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 30		- 130	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CC}	Supply Current Outputs LOW Outputs HIGH		 7.0 8.5	 12 14	 V_{CC} = MAX, V_{IN} = 0V, $\overline{V_E}$ = 0V V_{CC} = MAX, V_{IN} = 0V, $\overline{V_E}$ = 4.5V		mA

Notes : 1 Conditions for testing, not shown in the Table, are chosen to guarantee operation under "wrost case" conditions
2 Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		11 13	25 20	Fig 1	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		20 21	45 32	Fig 1		ns
t_{PZH}	Output Enable Time to HIGH Level		11	23	Figs. 4,5		ns
t_{PZL}	Output Enable Time to LOW Level		15	23	Figs. 3,5		ns
t_{PLZ}	Output Disable Time from LOW Level		12	27	Figs 3,5	V_{CC} = 5.0 V C_L = 5 pF	ns
t_{PHZ}	Output Disable Time from HIGH Level		27	41	Figs 4,5		ns

3-STATE AC WAVEFORMS AND LOAD CIRCUIT

Figure 1.

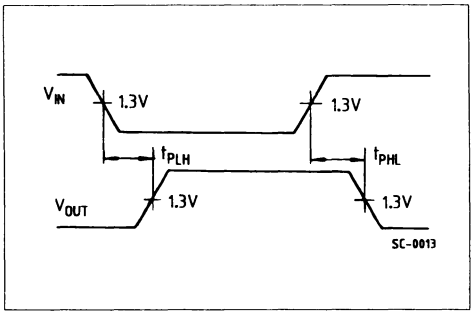


Figure 2.

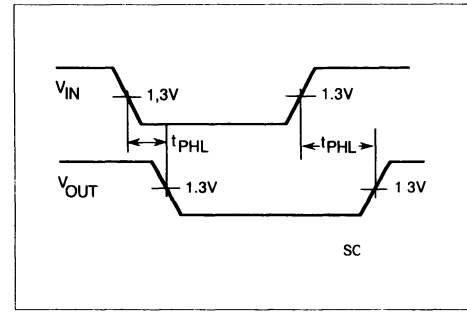


Figure 3.

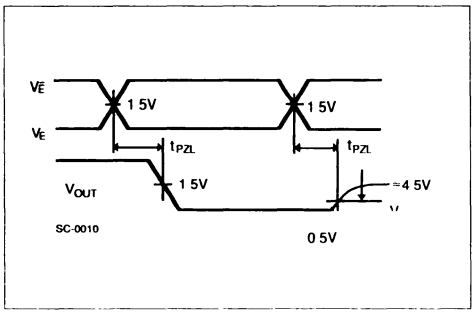


Figure 4.

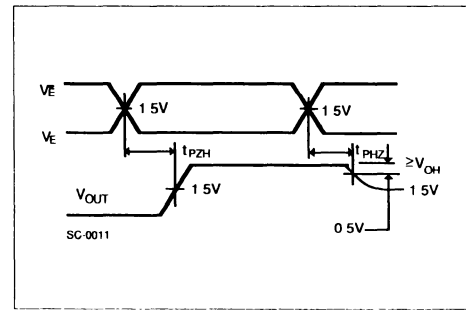
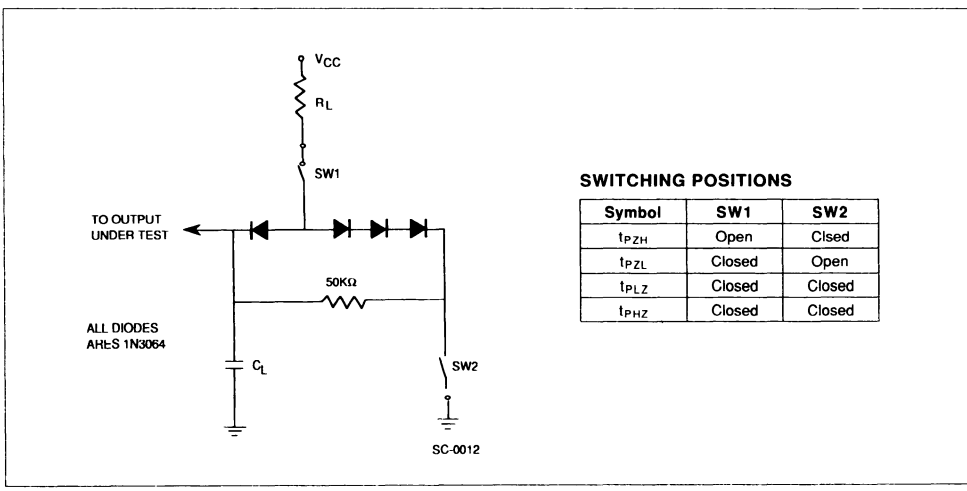


Figure 5.



SWITCHING POSITIONS

Symbol	SW1	SW2
t_{PZH}	Open	Clsed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

SGS-THOMSON MICROELECTRONICS

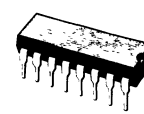
T74LS365A/366A T74LS367A/368A

3-STATE HEX BUFFERS

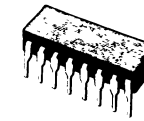
DESCRIPTION

These devices are high-speed Hex Buffers with 3-state outputs. They are organized as single 6-bit or 2-bit/4-bit, with inverting or non-inverting data (D) paths. The outputs are designed to drive 15 TTL Unit Loads or 60 Low Power Schottky loads when the Enable ($\overline{E}$) is LOW.

When the output Enable input ($\overline{E}$) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedence state to avoid high currents that woud exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices, whose outputs are tied together, are designed so there is no overlap.



B1
(Plastic Package)



D1
(Ceramic Package)

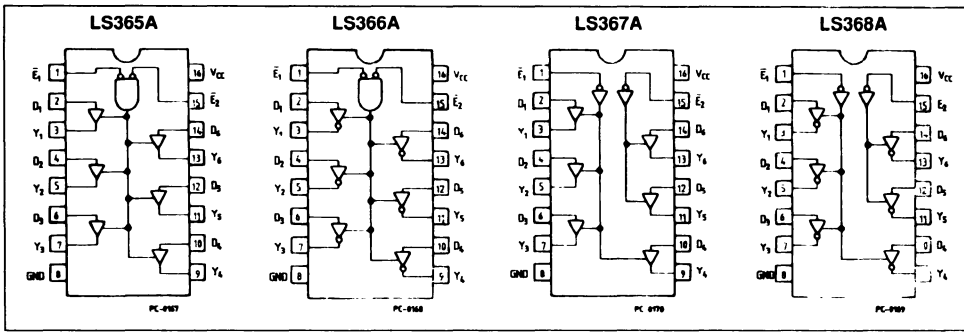
M1
(Micro Package)

C1
(Plastic Chip Carrier)

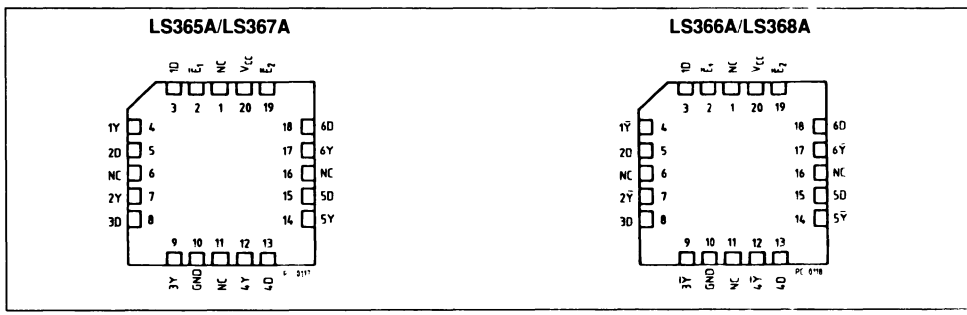
ORDER CODES :

T74LSXXXX D1	T74LSXXXX C1
T74LSXXXX B1	T74LSXXXX M1

PIN CONNECTION (top view) DUAL IN LINE



CHIP CARRIER



TRUTH TABLES

LS365A

Inputs			Output
$\overline{E}_1$	$\overline{E}_2$	D	
L	L	L	L
L	L	H	H
H	X	X	(Z)
X	H	X	(Z)

LS366A

Inputs			Output
$\overline{E}_1$	$\overline{E}_2$	D	
L	L	L	H
L	L	H	L
H	X	X	(Z)
X	H	X	(Z)

LS367A

Inputs		Output
$\overline{E}$	D	
L	L	L
L	H	H
H	X	(Z)

LS368A

Inputs		Output
$\overline{E}$	D	
L	L	H
L	H	L
H	X	(Z)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	0 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS365A/366A/367A/368AXX	4.75 V	5.0 V	5 25 V	0 °C to + 70 °C

XX = Package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Condition (note 1)		Unit
			Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage		2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage				0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage			- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage		2.4	3.1		V_{CC} = MIN, I_{OH} = - 2.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage			0.25	0.4	I_{OL} = 12 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
				0.35	0.5	I_{OL} = 24 mA		V
I_{OZH}	Output Off Current HIGH				20	V_{CC} = MAX, V_{OUT} = 2.7 V $\overline{V_E}$ = 2.0 V		µA
I_{OZL}	Output Off Current LOW				- 20	V_{CC} = MAX, V_{IN} = 0.4 V $\overline{V_E}$ = 2.0 V		µA
I_{IH}	Input HIGH Current				20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA
I_{IL}	Input LOW Current	D Inputs			- 20	V_{CC} = MAX, V_{IN} = 0.5 V Either E Input at 2 V		mA
					- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V Both E Inputs at 0.4 V		mA
		E Inputs			- 0.4			mA
I_{OS}	Output Short Circuit Current (note 2)		- 40		- 225	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current	LS365A/367A		13.5	24	V_{CC} = MAX, V_{IN} = 0.4 V $\overline{V_E}$ = 4.5 V		mA
		LS366A/368A		11.8	21			mA

Notes : 1. For Conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating conditions for the device type.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits						Test Conditions	Unit
		LS365A/367A			LS366A/368A				
		Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay,		10 9.0	16 22		7.0 12	15 18	V_{CC} = 5.0 V C_L = 45 pF R_L 667 Ω	ns
t_{PLH} t_{PHL}	Output Enable Time		19 24	35 40		18 28	35 45		ns
t_{PLH} t_{PHL}	Output Disable Time			30 35			32 35	V_{CC} = 5.0 V C_L = 5.0 pF	ns

AC WAVEFORMS

Figure 1.

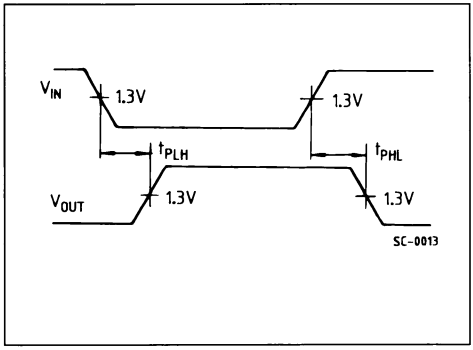


Figure 2.

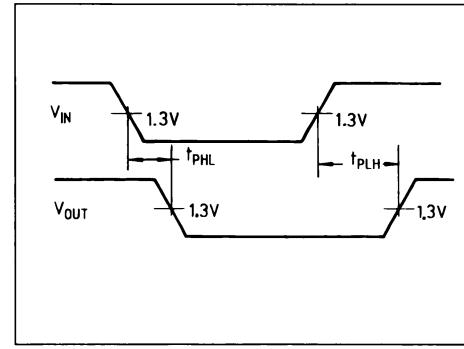


Figure 3.

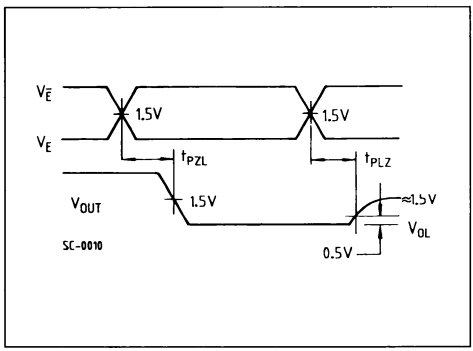
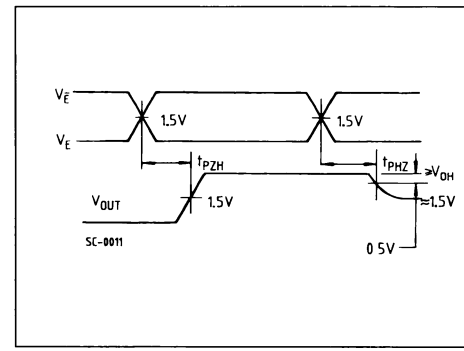
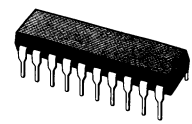


Figure 4.

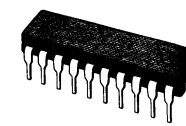


OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS

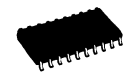
- EIGHT LATCHES IN A SINGLE PACKAGE
- 3-STATE OUTPUTS FOR BUS INTERFACING
- HYSTERESIS ON LATCH ENABLE
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)



M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS373 D1 T74LS373 C1
T74LS373 B1 T74LS373 M1

DESCRIPTION

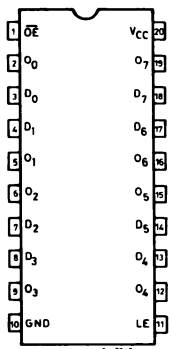
The T74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus outputs is in the high impedance state.

PIN NAMES

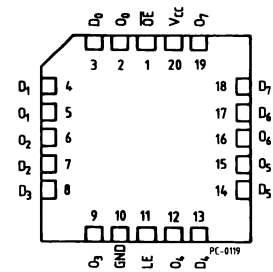
D_0-D_7	DATA INPUTS
$\overline{LE}$	LATCH ENABLE (active HIGH) INPUT
$\overline{OE}$	OUTPUT ENABLE (active LOW) INPUT
O_0-O_7	OUTPUTS

PIN CONNECTION (top view)

DUAL IN LINE

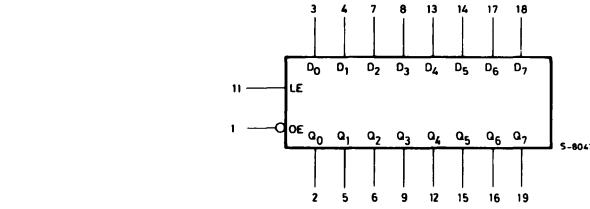


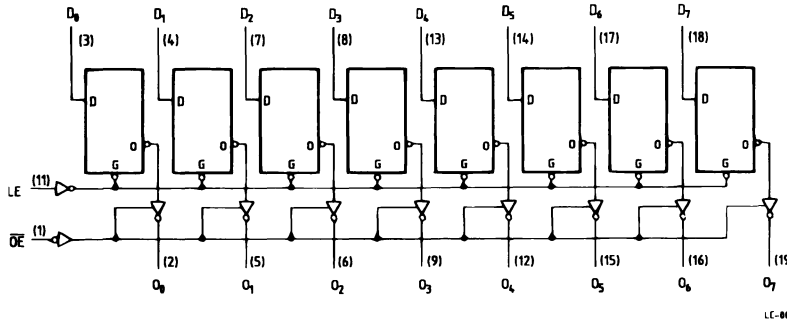
CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM





V_{CC} = Pin 20
GND = Pin 10
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS373XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.4	3.1		V_{CC} = MIN, I_{OH} = - 2.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 12 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 24 mA		V
I_{OZH}	Output Off Current HIGH			20	V_{CC} = MAX, V_{OUT} = 2.7 V V_E = 2.0 V		µA
I_{OZL}	Output Off Current LOW			- 20	V_{CC} = MAX, V_{OUT} = 0.4 V V_E = 2.0 V		µA
I_{IH}	Input HIGH Current			20	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	Input HIGH Current at MAX Input Voltage			0.1	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 30		- 130	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current Output Off		24	40	V_{CC} = MAX, V_{IN} = 0 V V_E = 4.5 V		mA

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "wrost case" conditions
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		12 12	18 18	Fig. 1	V_{CC} = 5.0 V C_L = 45 pF R_L = 667 Ω	ns
t_{PLH} t_{PHL}	Propagation Delay, Clock or LE to Output		20 18	30 30	Fig. 1		ns
t_{PZH}	Output Enable Time to HIGH Level		15	28	Figs. 3,4		ns
t_{PZL}	Output Enable Time to LOW Level		25	36	Figs. 2,4		ns
t_{PLZ}	Output Disable Time from LOW Level		15	25	Figs. 2,4	V_{CC} = 5.0 V C_L = 5 pF R_L = 667 Ω	ns
t_{PHZ}	Output Disable Time from HIGH Level		12	20	Figs. 3,4		ns

AC SET-UP REQUIREMENTS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
t_sD	Set-up Time Data to Negative Going LE	5			Fig. 1	V_{cc} = 5.0 V	ns
t_hD	Hold Time Data to Negative Going LE	20					ns
t_wLE	Minimum LE Pulse Width HIGH to LOW	15					ns

DEFINITION OF TERMS

SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input to LE transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following LE transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition.

AC WAVEFORMS

Figure 1 .

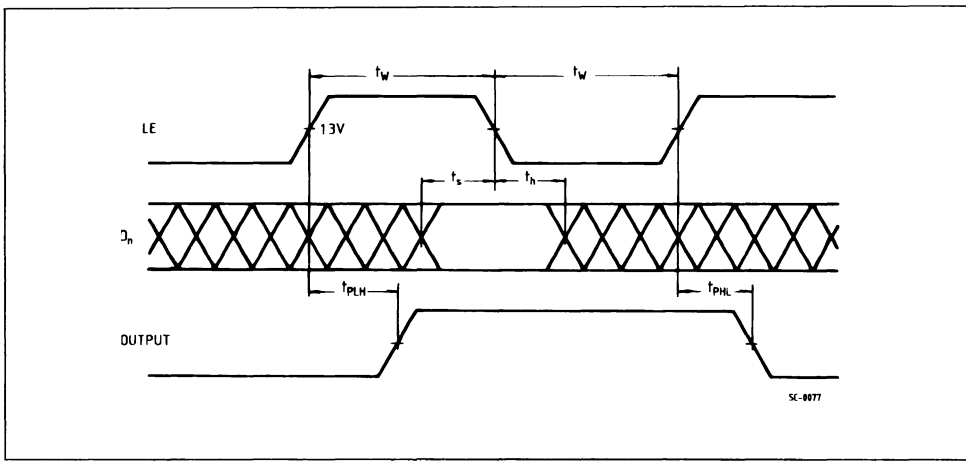


Figure 2 .

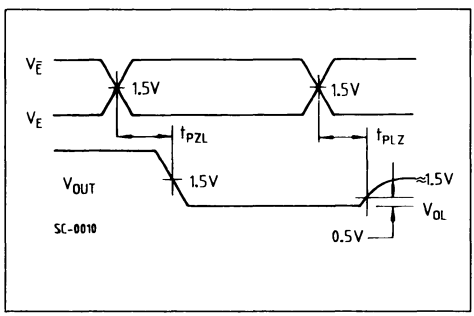
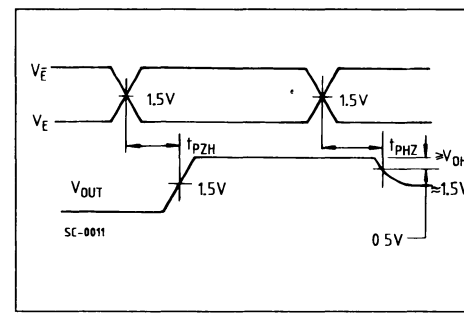
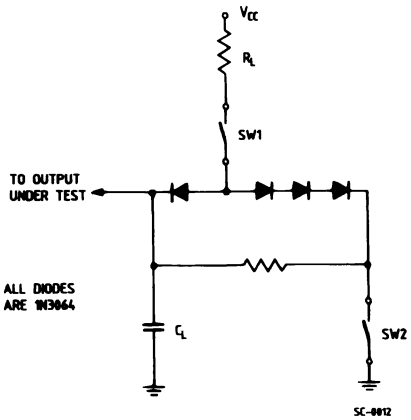


Figure 3 .



AC LOAD CIRCUIT

Figure 4.



SWITCHING POSITIONS

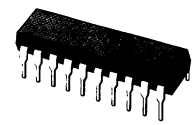
Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Close

SGS-THOMSON MICROELECTRONICS

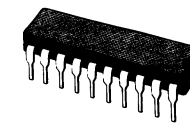
T74LS374

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

- EDGE-TRIGGERED D-TYPE INPUTS
- BUFFERED POSITIVE EDGE-TRIGGERED CLOCK
- 3-STATE OUTPUTS FOR BUS ORIENTED APPLICATIONS
- HYSTERESIS ON OUTPUT ENABLE INPUT TO IMPROVE NOISE MARGIN
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS374 D1 T74LS374 C1
T74LS374 B1 T74LS374 M1

DESCRIPTION

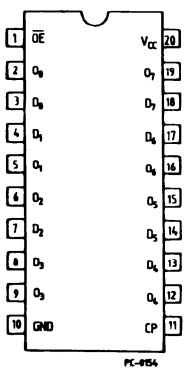
The T74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

PIN NAMES

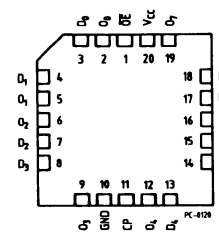
D_0-D_7	DATA INPUTS
$\underline{CP}$	CLOCK (active HIGH going edge) INPUT
$\overline{OE}$	OUTPUT ENABLE (active LOW) INPUT
O_0-O_7	OUTPUTS

PIN CONNECTION (top view)

DUAL IN LINE

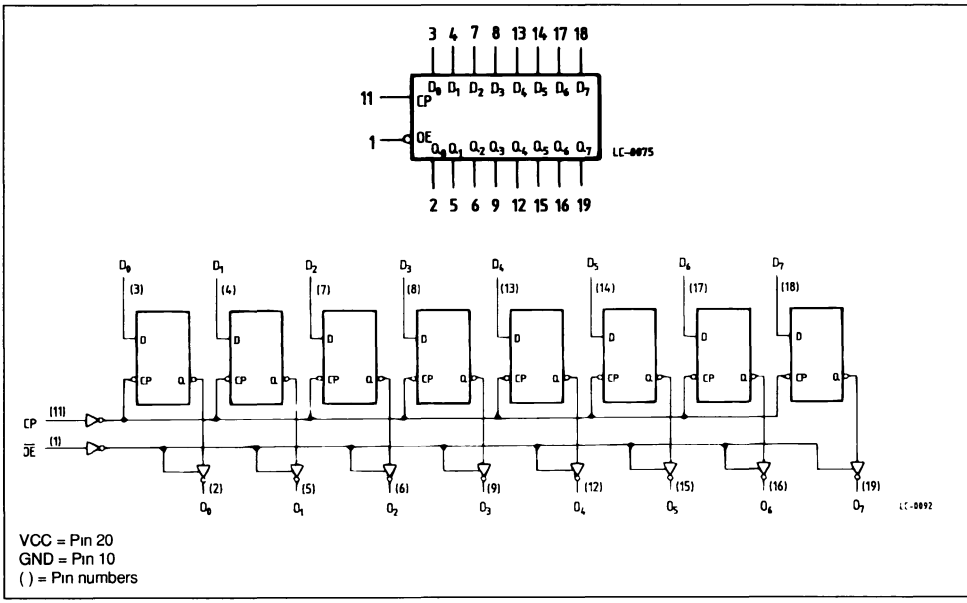


CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM



VCC = Pin 20
GND = Pin 10
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to + 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to + 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to + 10	V
I_I	Input Current, Into Inputs	– 30 to + 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS374XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

TRUTH TABLE

D_n	CP	$\overline{OE}$	Q_n
H	I	L	H
L	I	L	L
X	X	H	Z*

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(Z) = High impedance

* Note . Contents of flip-flops unaffected by the state of the Output Enable input ($\overline{OE}$).

FUNCTIONAL DESCRIPTION

The LS374 consist of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The Clock and Output Enable are common. The eight flip-flops will store the state of their individual D inputs that meet the set-up and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are refected on the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the OE input does not affect the state of the flip-flops.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.4	3.1		V_{CC} = MIN, I_{OH} = - 2.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 12 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 24 mA		V
I_{OZH}	Output Off Current HIGH			20	V_{CC} = MAX, V_{OUT} = 2.7 V V_E = 2.0 V		µA
I_{OZL}	Output Off Current LOW			- 20	V_{CC} = MAX, V_{OUT} = 0.4 V V_E = 2.0 V		µA
I_{IH}	Input HIGH Current			20	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	Input HIGH Current at MAX Input Voltage			0.1	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 30		- 130	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current Output Off		27	45	V_{CC} = MAX, V_{IN} = 0 V V_E = 4.5 V		mA

Notes : 1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions (note 1)		Unit
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, CP to Output		15 19	28 28	fig. 1	C_L = 45 pF R_L = 667 Ω	ns
t_{PZH}	Output Enable Time to HIGH Level		20	28	figs. 3, 4		ns
t_{PZL}	Output Enable Time to LOW Level		21	28	figs. 2, 4		ns
t_{PLZ}	Output Disable Time from LOW Level		12	20	figs. 2, 4	C_L = 5.0 pF R_L = 667 Ω	ns
t_{PHZ}	Output Disable Time from HIGH Level		15	25	figs. 3, 4		ns
f_{MAX}	Maximum Input Frequency	35	50		fig 1		MHz

AC SET-UP REQUIREMENTS : T_A = 25 °C

Symbol	Parameter	Limit			Test Conditions		Unit
		Min.	Typ.	Max.			
t_wCP	Minimum Clock Pulse Width HIGH or LOW	13	10		fig. 1	V_{CC} = 5.0 V	ns
t_s	Minimum Set-up Time, Data to CP	20	15				ns
t_n	Minimum Hold Time, Data to CP	0	− 3				ns

DEFINITION OF TERMS :

SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) - is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

AC WAVEFORMS AND LOAD CIRCUIT

Figure 1.

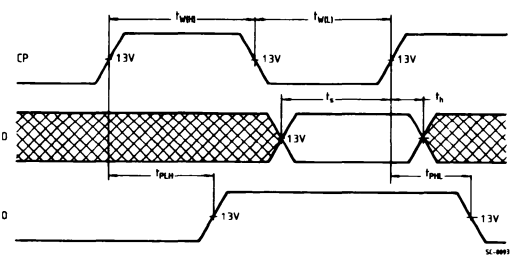


Figure 2.

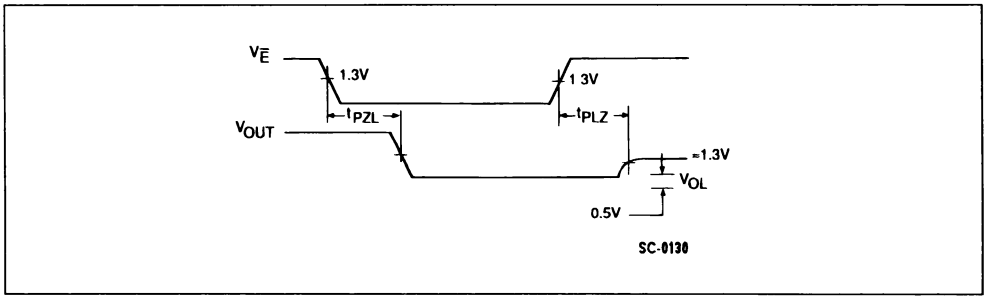


Figure 3.

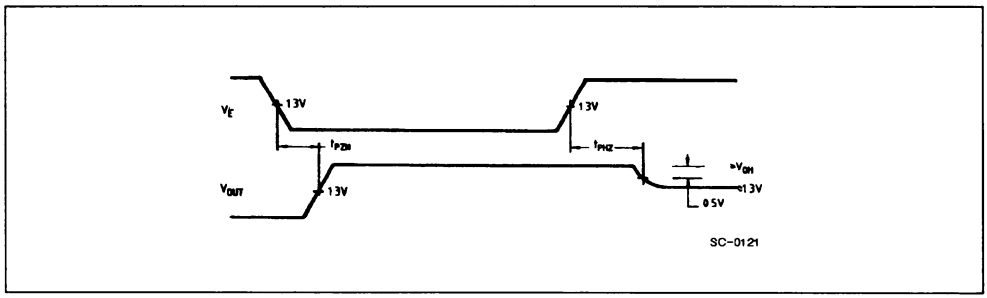
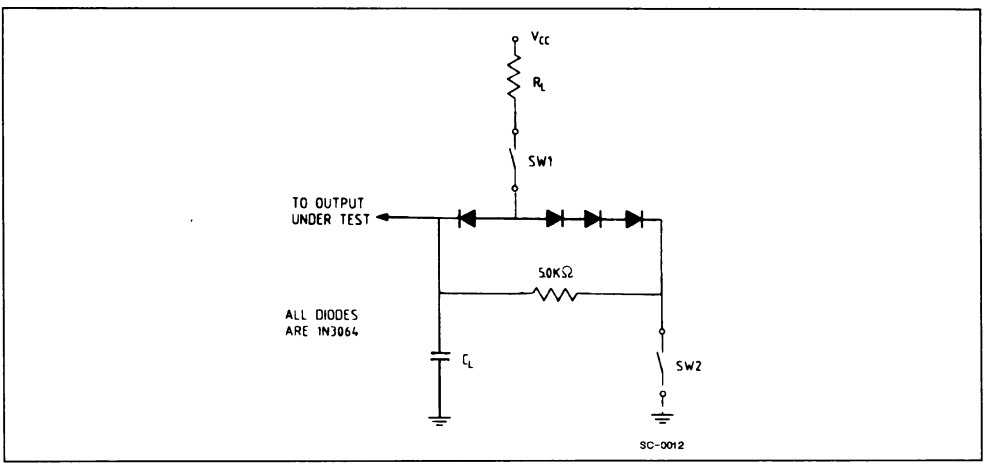
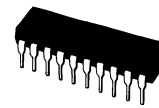


Figure 4.

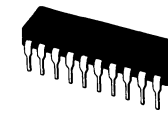


OCTAL D FLIP-FLOP WITH COMMON ENABLE AND CLOCK

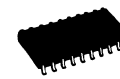
- 8-BIT HIGH SPEED PARALLEL REGISTERS
- POSITIVE EDGE-TRIGGED D-TYPE FLIP-FLOP
- FULLY BUFFERED COMMON CLOCK AND ENABLE INPUTS
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)



M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS377 D1 T74LS377 C1
T74LS377 B1 T74LS377 M1

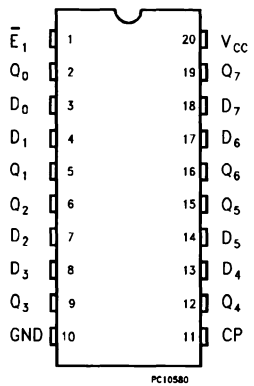
DESCRIPTION

The T54LS377 is an 8-Bit register built using advanced Low Power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common clock enable. The device is packaged in the spacesaving (0.3 inch row spacing) 20 pin package.

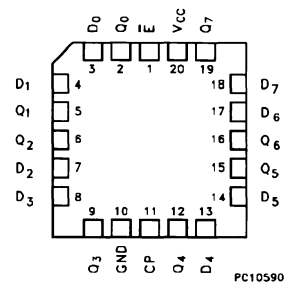
$\overline{E}$	Enable (Active LOW) Input
D_0-D_7	Data Inputs
CP	Clock (Active HIGH Going Edge) Input
Q_0-Q_7	True Outputs

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER

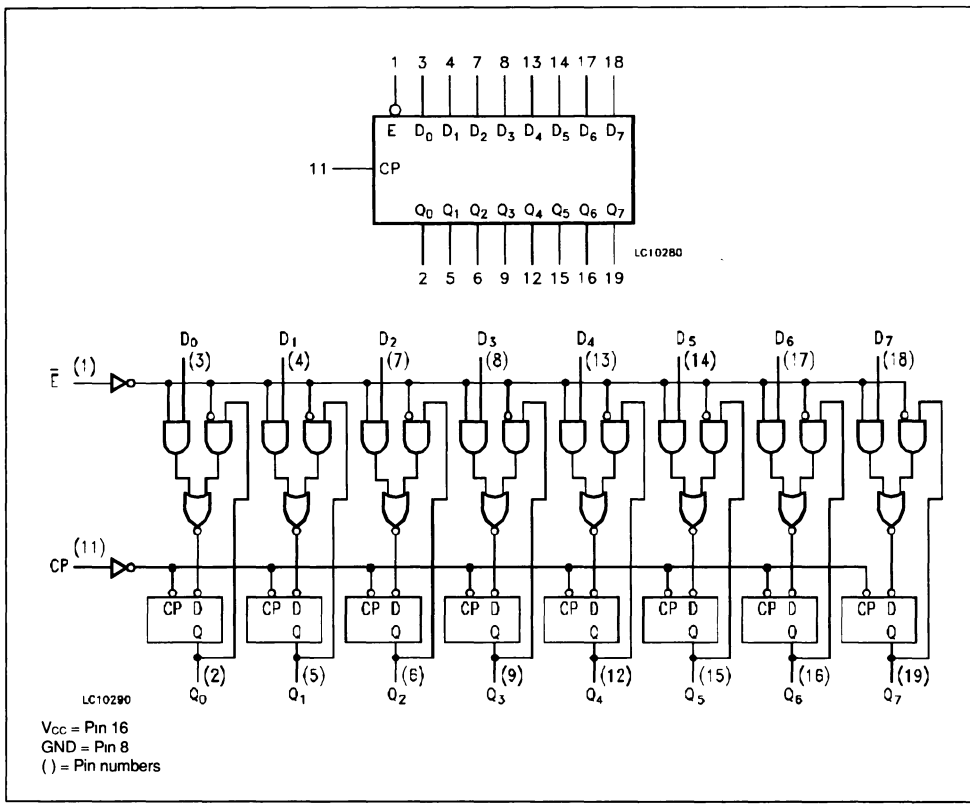


TRUTH TABLE

E	CP	D_n	Q_n
H	⎍	X	No Change
L	⎍	H	H
L	⎍	L	L

L = LOW Voltage Level
H = HIGH Voltage Level
X= Don't Care

LOGIC SYMBOL AND LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

FUNCTIONAL DESCRIPTION

The LS377 consists of eight edge-triggered D flip-flop with individual D inputs and Q outputs. The Clock (CP) and Enable input ($\overline{E}$) are common to all flip-flop.

When $\overline{E}$ is LOW, new datais entered into the register on the next LOW to HIGH transition of (CP).

When $\overline{E}$ is HIGH, the register will retaint the present data independent of the CP.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	− 0.5 to + 7	V
V_I	Input Voltage, Applied to Input	− 0.5 to + 15	V
V_O	Output Voltage, Applied to Output	− 0.5 to + 10	V
I_I	Input Current, Into Inputs	− 30 to + 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS377XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for all Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for all Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.5	3.5		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		18	28	V_{CC} = MAX		mA

Notes : 1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
f_{MAX}	Maximum Clock Frequency	30	40		Figures 1	V_{CC} = 5.0 V C_L = 15 pF R_L = 2 KΩ	MHz
t_{PLH}	Propagation Delay,Clock to Outputs		17	27	Figures 1		ns
t_{PHL}	Propagation Delay, Clock to Outputs		18	27	Figures 1		ns

AC SET-UP REQUIREMENTS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_W(CP)	Minimum Clock Pulse Width	20			Figure 1	V_{CC} = 5.0 V C_L = 15 pF R_L = 2 KΩ	ns
t_s	Set-Up Time, Data to Clock (HIGH or LOW)	20			Figure 1		ns
t_h	Hold Time, Data to Clock (HIGH or LOW)	5			Figure 1		ns
t_sH	Set-Up Time HIGH Enable to Clock	10			Figure 1		ns
t_hH	Hold Time HIGH Enable to Clock	5			Figure 1		ns
t_sL	Set-Up Time LOW Enable to Clock	25			Figure 1		ns
t_hL	Hold Time LOW Enable to Clock	5			Figure 1		ns

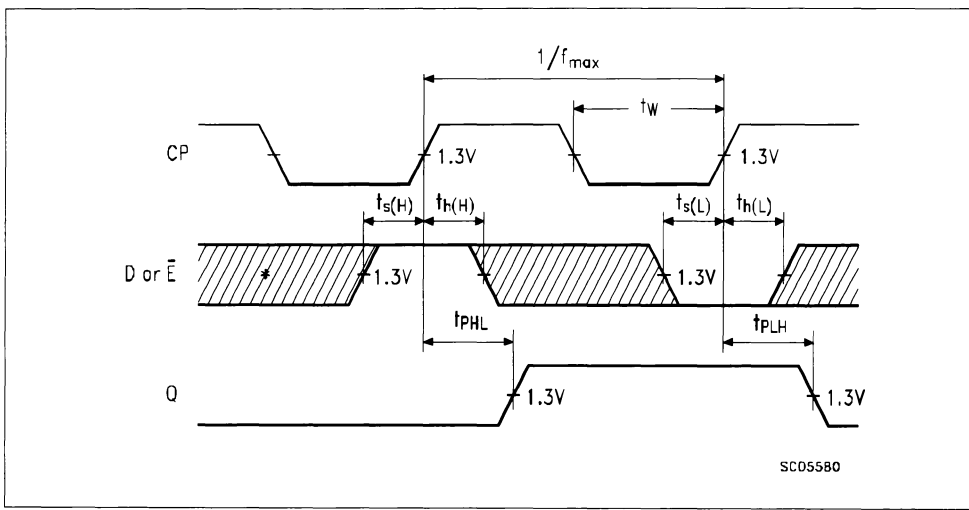
DEFINITION OF TERMS:

SET-UP TIME (t_s): is defined as the minimum time required for the corret logic level to be present at the logic input prior the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h): is defined as the minimum time following the clock transition from LOW to HIGH at which the logiclevel must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be relased prior to the clock transitio from LOW to HIGH and still be recognized.

AC WAVEFORMS

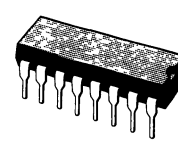
Figure 1: Clock to Output Delays, Clock Pulse Width, Frequency Set-up and Hold Times Data to Clock



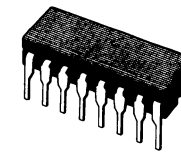
* The shaded areas indicate when the input is permitted to chang for predictable output performance

HEX PARALLEL D REGISTER WITH ENABLE

- 8-BIT HIGH SPEED PARALLEL REGISTER
- POSITIVE EDGE-TRIGGERED D-TYPE FLIP-FLOPS
- FULLY BUFFERED COMMON CLOCK AND ENABLE INPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS378 D1 T74LS378 C1
T74LS378 B1 T74LS378 M1

DESCRIPTION

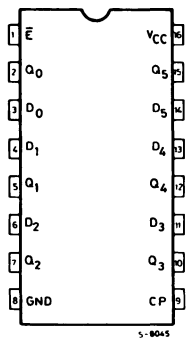
The T74LS378 is an 6-Bit Register with a buffered common enable. This device is similar to the T74LS174, but with common Enable rather than common Master Reset.

PIN NAMES

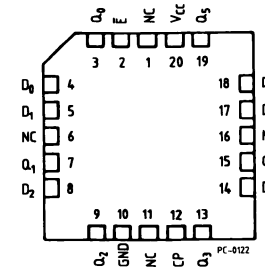
$\overline{E}$	ENABLE (active LOW) INPUT
D_0-D_5	DATA INPUTS
CP	CLOCK (active HIGH going edge) INPUT
Q_0-Q_5	TRUE OUTPUTS

PIN CONNECTION (top view)

DUAL IN LINE

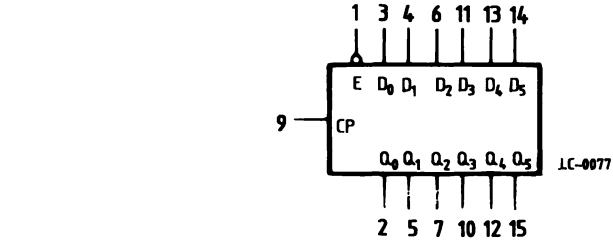


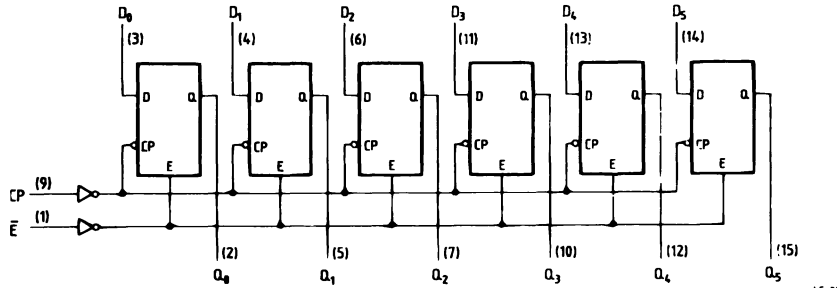
CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM





V_{CC} = Pin 16
GND = Pin 8
() = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS378XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

FUNCTIONAL DESCRIPTION

The LS378 consists of eight edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable ($\overline{E}$) input are common to all flip-flops.

When $\overline{E}$ input is LOW, new data is entered intothe register on the LOW-to-HIGH transition of CP input. When the $\overline{E}$ input is HIGH the register will retain the present data independent of the CP input.

TRUTH TABLE

$\overline{E}$	CP	D_n	Q_n
H	⊥⌜	X	No charge
L	⊥⌜	H	H
L	⊥⌜	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Treshold Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Treshold Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		16	27	V_{CC} = MAX		mA

Notes : 1. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
2. Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C

AC CHARACTERISTICS : T_A = 25 °C

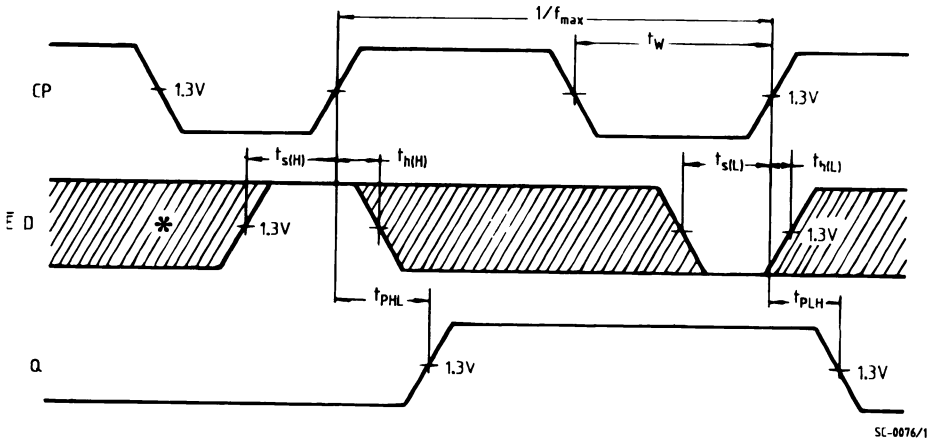
Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
f_{MAX}	Minimum Input Clock Frequency	30	40		Fig. 1	V_{CC} = 5.0 V	MHz
t_{PLH}	CP to Q Output		17	27	Fig. 1		ns
t_{PHL}	CP to Q Output		18	27	Fig. 1		ns

AC SET-UP REQUIREMENTS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
t_s	Set-up Time, Data to Clock (HIGH or LOW)	20			Fig. 1	V_{CC} = 5.0 V	ns
t_h	Hold Time, Data to Clock (HIGH or LOW)	5			Fig. 1		ns
t_s	Set-up Time, Enable to Clock (HIGH or LOW)	30			Fig. 1		ns
t_h	Hold Time, Enable to Clock (HIGH or LOW)	5			Fig. 1		ns
t_{wCP}	Minimum Clock Pulse Width	20					ns

AC WAVEFORMS

Figure 1 : Clock to Output Delays, Clock Pulse Width, Frequency, Set-up and Hold Times Data, Enable to Clock.



* The shaded areas indicate when the input is permitted to change for predictable output performance

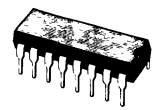
DEFINITION OF TERMS :

SET-UP TIME (ts)- is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

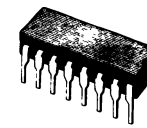
HOLD-TIME (th)- is defined as the minimum time following the clock transition from LOW to HIGH that the logic lecel muqt be maintained at the input in order to ensure continued recognition.A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

QUAD PARALLEL REGISTER WITH ENABLE

- EDGE-TRIGGERED D-TYPE INPUTS
- BUFFERED POSITIVE EDGE-TRIGGERED CLOCK
- BUFFERED COMMON ENABLE INPUT
- TRUE AND COMPLEMENT OUTPUT
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS379 D1 T74LS379 C1
T74LS379 B1 T74LS379 M1

DESCRIPTION

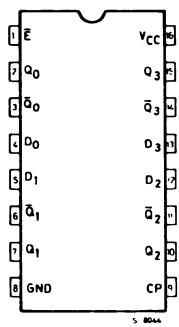
The T74LS379 is a 4-Bit Register with buffered common Enable. This device is similar to the T74LS175 but feature the common Enble rather than common Master Reset.

PIN NAMES

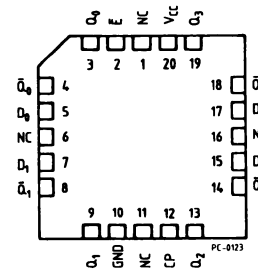
$\overline{E}$	ENABLE (active LOW) INPUT
D_0-D_3	DATA INPUTS
CP	CLOCK (active HIGH going edge) INPUT
Q_0-Q_3	TRUE OUTPUTS
$\overline{Q}_0$–$\overline{Q}_3$	COMPLEMENTS OUTPUTS

PIN CONNECTION (top view)

DUAL IN LINE

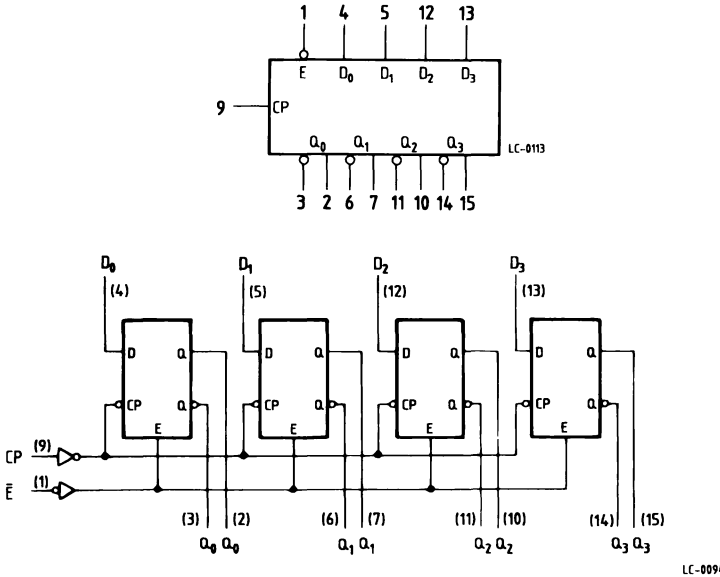


CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
() = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	60	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS379XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

FUNCTIONAL DESCRIPTION

The LS379 consist of four edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops.

When the $\overline{E}$ input is HIGH, the register will retain the present data independent of the CP input.

TRUTH TABLE

$\overline{E}$	CP	D_n	Q_n	$\overline{Q}_n$
H	⊥⌐	X	No change	No Change
L	⊥⌐	H	H	L
L	⊥⌐	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current			20	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	Input HIGH Current at MAX Input Voltage E, D_0-D_3, CP			0.1	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current E, D_0-D_3, CP			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		11	16	V_{CC} = MAX		mA

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

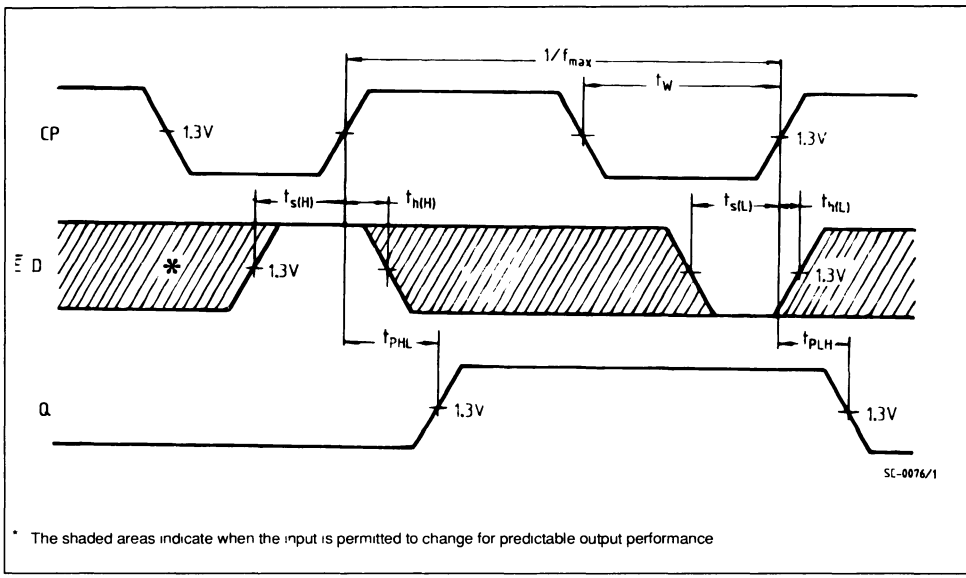
Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
t_{PLH}	CP to Output		17	27	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PHL}	CP to Output		18	27			ns
f_{MAX}	Maximum Clock Frequency	30	40				MHz

AC SET-UP REQUIREMENTS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
t_s	Set-up Time, Data to Clock (HIGH or LOW)	20			Fig. 1	V_{CC} = 5.0 V	ns
t_h	Hold Time, Data to Clock (HIGH or LOW)	5			Fig. 1		ns
t_s	Set-up Time, Enable to Clock	30			Fig. 1		ns
t_h	Hold Time, Enable to Clock	5			Fig. 1		ns
t_{WCP}	Minimum Clock Pulse Width	17	10				ns

AC WAVEFORMS

Figure 1 : Clock to Output Delays, Clock Pulse Width, Frequency, Set-up and Hold Times Data, Enable to Clock.



* The shaded areas indicate when the input is permitted to change for predictable output performance

DEFINITION OF TERMS :

SET-UP TIME (ts)- is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD-TIME (th)- is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition.A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

SGS-THOMSON
MICROELECTRONICS

T74LS390
T74LS393

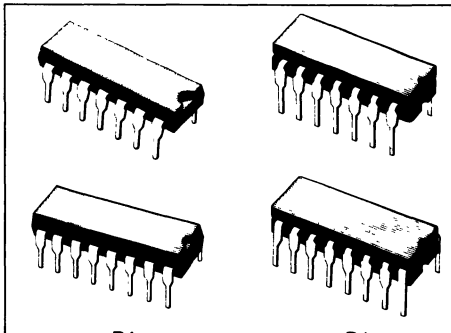
DUAL DECADE COUNTER
DUAL 4-STAGE BINARY COUNTER

- DUAL VERSION OF LS290 AND 293
- LS390 HAS SEPARATE CLOCKS ALLOWING ÷ 2, ÷ 2.5, ÷ 5
- INDIVIDUAL ASYNCHRONOUS CLEAR FOR EACH COUNTER
- TYPICAL MAX COUNT FREQUENCY OF 50 MHz
- INPUT CLAMP DIODES MINIMIZE HIGH SPEED TERMINATION EFFECTS

DESCRIPTION

The T74LS390 and T74LS393 each contain a pair of high-speed 4-stage ripple counters. Each half of the LS390 is partitioned into a divide-by-two section and a divide-by-five section, with a separate clock input for each section. The two section can be connected to count in the 8.4.2.1 BCD code or they can count in a biquinary sequence to provide a square wave (50 % duty cycle) at the final output.

Each half of the LS393 operates as a Modulo-16 binary divider, with the last three stages triggered in a ripple fashion. In both the LS390 and the LS393, the flip-flops are triggered by a HIGH-to-LOW transi-tion of their CP inputs. Each circuit type has a Master Reset input which responds to a HIGH signal by forcing all four outputs to the LOW state.



B1 (Plastic Package)

D1 (Ceramic Package)

M1 (Micro Package)

C1 (Plastic Chip Carrier)

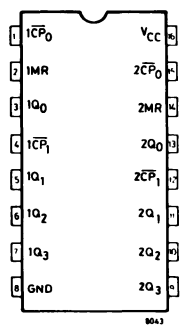
ORDER CODES :

T74LSXXX D1 T74LSXXX C1
T74LSXXX B1 T74LSXXX M1

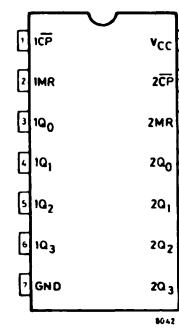
PIN CONNECTION (top view)

DUAL IN LINE

LS390

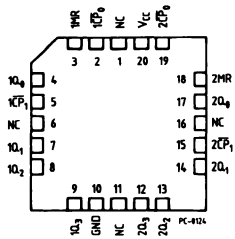


LS393

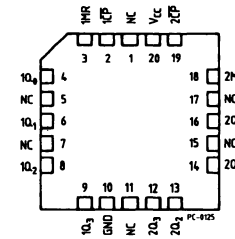


CHIP CARRIER

LS390



LS393



NC = No Internal Connection

PIN NAMES

$\overline{CP}$	CLOCK ACTIVE LOW GOING EDGE INPUT TO – 16 (LS393)
$\overline{CP_0}$	CLOCK ACTIVE LOW GOING EDGE INPUT TO – 2 (LS390)
$\overline{CP_1}$	CLOCK ACTIVE LOW GOING EDGE INPUT TO – 5 (LS390)
MR	MASTER RESET (active HIGH) INPUT
Q_0-Q_3	FLIP-FLOPS OUTPUTS

TRUTH TABLES

LS390 BCD
(Input on $\overline{CP}_0$; Q_0 $\overline{CP}_1$)

COUNT	OUTPUTS			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

LS390 ÷ 5
(Input on $\overline{CP}_1$)

COUNT	OUTPUTS		
	Q_3	Q_2	Q_1
0	L	L	L
1	L	L	H
2	L	H	L
3	L	H	H
4	H	L	L

LS393

COUNT	OUTPUTS			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

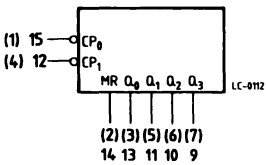
GUARANTEED OPERATING RANGE

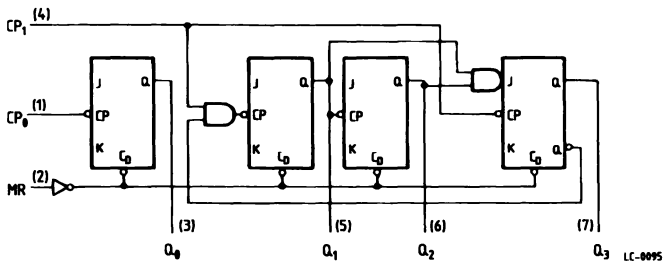
Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS390XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

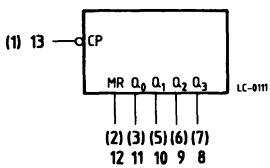
LOGIC SYMBOLS AND LOGIC DIAGRAMS

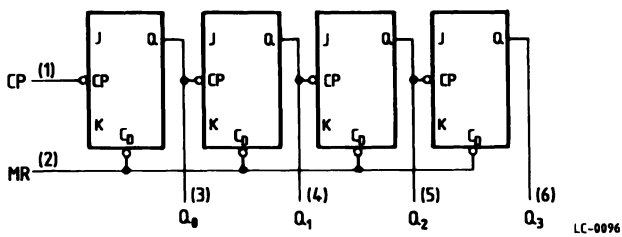
LS390 (one half shown)





LS393 (one half shown)





FUNCTIONAL DESCRIPTION

Each half of the LS393 Operates in the Modulo 16 binary sequences, as indicated in the ÷ 16 Truth Table. The first flip-flop is triggered by HIGH-to-LOW transitions of the CP input signal. Each of the other flip-flops is triggered by a HIGH-to-LOW transition of the Q output of the preceding flip-flop. Thus state changes of the Q outputs for not occur simultaneously. This means that logic signals derived from combinations of these outputs will be subject to decoding spikes and, therefore, should not be used as clocks for other counters, registers or flip-flops. A HIGH signal on MR forces all outputs to the LOW state and prevents counting.

Each half of the LS390 contains a ÷ 5 section that is independent except for the common MR function.

The ÷ 5 section operates in 4.2.1 binary sequence, as shown in the ÷ 5 Truth Table, with the third stage output exhibiting a 20 % duty cycle when the input frequency is constant. To obtain a ÷ 10 funtion having a 50 % duty cycle output, connect the input signal to CP_1 and connect Q_3 output to the CP_0 input ; the Q_0 output provides the 50 % duty cycle output. If the input frequency is connected to CP_0 and the Q_0 output is connected to CP_1, a decade divider operating in the 8.4.2.1 BCD code is obtained, as show in the BCD Truth Table. Since the flip-flops change state asynchronously, logic signal derived from combinations of LS390 outputs are also subject to decading spikes. A HIGH signal on MR forces all ouputs LOW and prevents counting.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Condition (note 1)		Unit
			Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage		2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage				0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage			- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage		2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage			0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
				0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current	$\overline{CP}$, $\overline{CP_0}$ CP_1 MR			40 80 20	V_{CC} = MAX, V_{IN} = 2.7 V		µA
		$\overline{CP}$, $\overline{CP_0}$ CP_1 MR			400 800 100	V_{CC} = MAX, V_{IN} = 7.0 V		µA
I_{IL}	Input LOW Current	$\overline{CP}$, $\overline{CP_0}$ CP_1 MR			- 2.4 - 3.2 - 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)		- 20		- 120	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current	LS290		20	30	V_{CC} = MAX		mA
		LS293		20	30			mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating conditions for the device type.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C, V_{CC} = 5.0 V

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
f_{MAX}	Maximum Clock Frequency $\overline{CP_0}$ to Q_0	25	35		C_L = 15 pF	MHz
f_{MAX}	Maximum Clock Frequency $\overline{CP_1}$ to Q_1	12.5	20			MHz
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}$ to Q_0 LS393		12 13	20 20		ns
t_{PLH} t_{PHL}	$\overline{CP_0}$ to Q_0 LS390		12 13	20 20		ns
t_{PLH} t_{PHL}	$\overline{CP}$ to Q_3 LS393		40 40	60 60		ns
t_{PLH} t_{PHL}	$\overline{CP_0}$ to Q_2 LS390		37 39	60 60		ns
t_{PLH} t_{PHL}	$\overline{CP_1}$ to Q_1 LS390		13 14	21 21		ns
t_{PLH} t_{PHL}	$\overline{CP_1}$ to Q_2 LS390		24 26	39 39		ns
t_{PLH} t_{PHL}	$\overline{CP_1}$ to Q_3 LS390		13 14	21 21		ns
t_{PHL}	MR to any Input LS390/393		24	39		ns

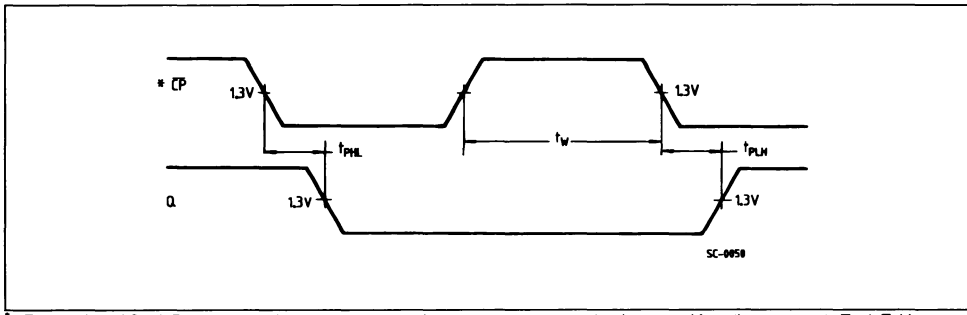
AC SET-UP REQUIREMENTS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_W	Clock Pulse Width LS390	20			V_{CC} = 5.0 V	ns
t_W	$\overline{CP_0}$ Pulse Width LS390	20				ns
t_W	CP_1 Pulse Width LS390	40				ns
t_W	MR Pulse Width LS390/393	20				ns
t_{rec}	Recovery Time LS390/393	25				ns

RECOVERY TIME (t_{rec}) - is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH to LOW in order to recognized and transfer HIGH Data to the Q outputs.

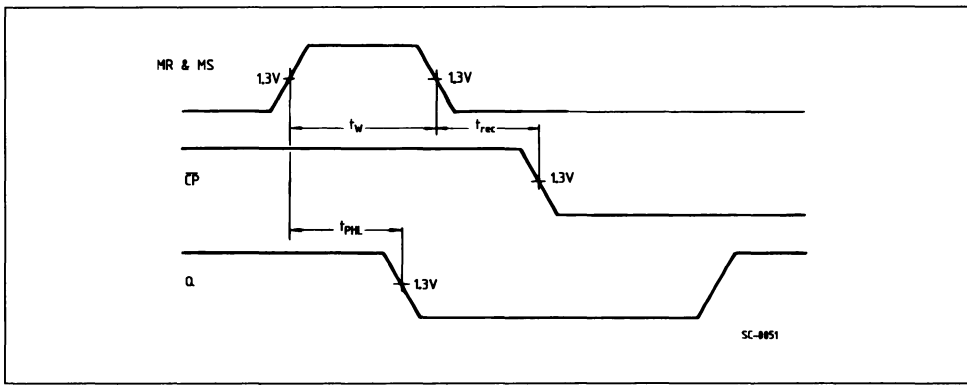
AC WAVEFORMS

Figure 1.



* The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Table.

Figure 2.

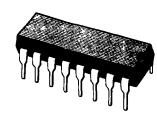


4-BIT SHIFT REGISTER WITH 3-STATE OUTPUTS

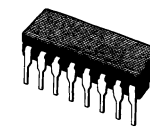
- SHIFT LEFT OR PARALLEL 4-BIT REGISTER
- 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

DESCRIPTION

The T74LS395A is a 4-Bit Registers with 3-state outputs and can operate in either a synchronous parallel load or a serial shift-right mode, as determined by the Select input. An asynchonous active LOW Master Reset (MR) input overrides the synchonous operations and clears the register. An active Low Outputs Enable (OE) input controls the 3-state output buffer, but does not interfere with the operations. The fourth stage also has a conventional output for linking purposes in multistage serial operations.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

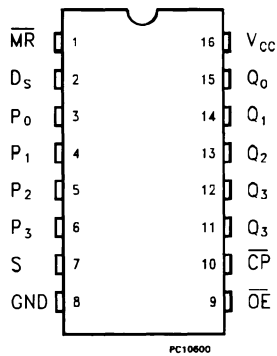
C1
(Plastic Chip Carrier)

ORDER CODES :

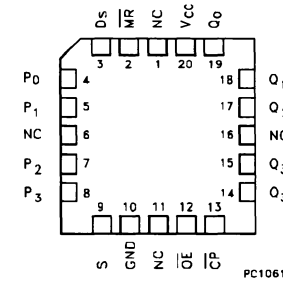
T74LS395A D1 T74LS395A C1
T74LS395A B1 T74LS395A M1

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER

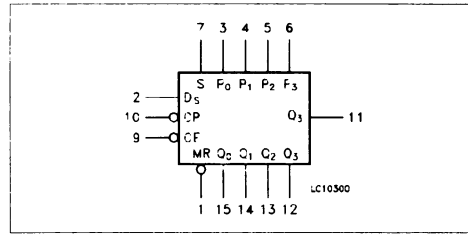


NC = No Internal Connection

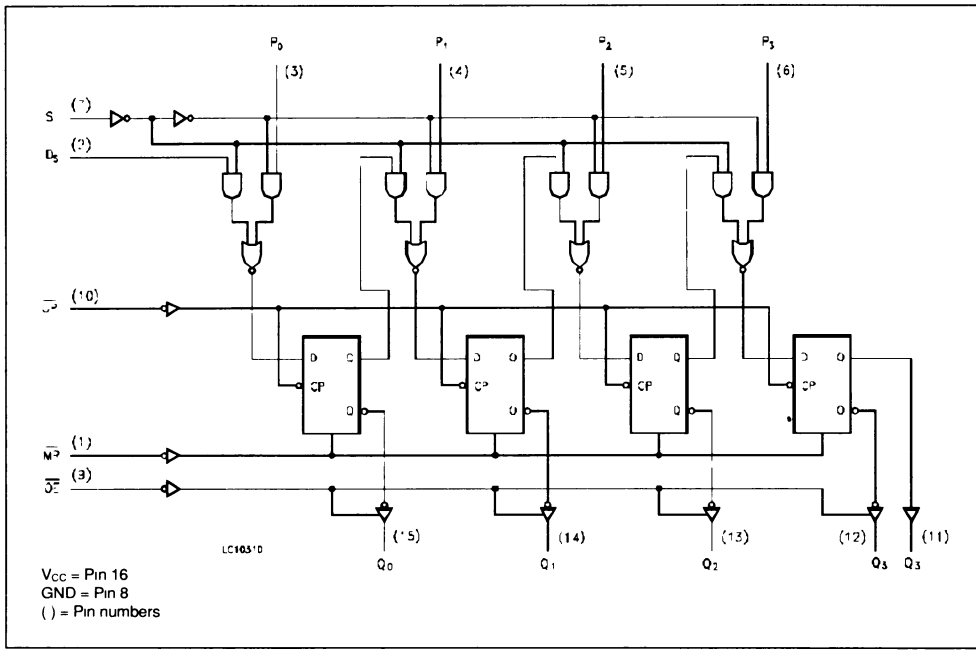
PIN NAMES

P_0-P_3	Parallel Inputs
D_S	Serial Data Inputs
S	Mode Select Input
$\overline{CP}$	Clock (Active LOW) Input
$\overline{MR}$	Master Reset (Active LOW) Input
$\overline{OE}$	Output Enable (Active LOW) Input
Q_0-Q_3	3-State Register Outputs
Q_3	Register Output

LOGIC SYMBOL



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

FUNCTIONAL DESCRIPTION

The LS395A contains four D-type edge-triggered flip-flop and auxiliary gating to select a D input either from a Parallel (P_n) input or from the preceding stage. When the Select input is HIGH, the P_n inputs are enabled. A lOW signal on the S input enables the serial inputs for shift-righ operations, as indicated in the Truth Table.

Stage changes are initiated by HIGH to LOW transitions on the Clock Pulse (CP) input. Signals on the P_n, D_s and S inputs can change when the Clock is in either state, provided that the recommended set-up and hold times are observed. When the S input is LOW, a CP HIGH-LOW transition transfers data Q_0 to Q_1, Q_1 to Q_2 and Q_2 to Q_3. A left-shift is accomplished by connecting the outputs back to the P_n inputs but offset one place to the left, i.e., O_3 to P_2, O_2 to P_1 and O_1 to P_0, with P_3 acting as the linking input from another package.

When the $\overline{OE}$ input is HIGH, the output buffers are disable and O_0 - O_3 outputs are in a high impedance condition. The shifting, parallel loading or resetting operations can still be accomplished, however.

MODE SELECT - TRUTH TABLE

Operating Mode	Inputs @ t_n					Outputs @ t_{n+1}			
	$\overline{MR}$	$\overline{CP}$	S	D_s	P_n	O_0	O_1	O_2	O_3
Asynchronous Reset	L	X	X	X	X	L	L	L	L
Shift, SET First Stage	H	⌐L	L	H	X	H	O_{0n}	O_{1n}	O_{2n}
Shift, RESET First	H	⌐L	L	L	P_n	L	O_{0n}	O_{1n}	O_{2n}
Stage Parallel Load	H	⌐L	H	X	X	P_0	P_1	P_2	P_3

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
tn, tn+1 = time before and after CP HIGH to LOW transition
NOTE: When $\overline{OE}$ is LOW, outputs O_0-O_3 are in the high impedance state, however, this does not affect other operation or the O_3 output.

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	- 0.5 to 7	V
V_I	Input Voltage, Applied to Input	- 0.5 to 15	V
V_O	Output Voltage, Applied to Output	- 0 5 to 10	V
I_I	Input Current, Into Inputs	- 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS395AXX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Condition (note 1)		Unit
			Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage		2.0			Guaranteed Input HIGH Voltage for All Input		V
V_{IL}	Input LOW Voltage				0.8	Guaranteed Input LOW Voltage for All Input		V
V_{CD}	Input Clamp Diode Voltage				- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	Q_0, Q_1, Q_2, Q_3	2.4			I_{OH} = -2.6 mA	V_{CC} = MIN, V_{IH} = 2.0 V V_{IL} = V_{IL}max	V
		Q_3	2.7			I_{OH} = -400 µA		
V_{OL}	Output LOW Voltage	Q_0, Q_1, Q_2, Q_3		0.35	0.5	I_{OL} = 24 mA	V_{CC} = MIN, V_{IH} = 2.0 V V_{IL} = V_{IL} max	V
		Q_3		0.35	0.5	I_{OL} = 8.0 mA		
I_{OZH}	Output Off Current HIGH	Q_0, Q_1, Q_2, Q_3			20	V_{CC} = MAX, V_{OUT} = 2.7 V V_E = 2.0 V		µA
I_{OZL}	Output Off Current LOW	Q_0, Q_1, Q_2, Q_3			- 20	V_{CC} = MAX, V_{OUT} = 0.5 V V_E = 2.0 V		µA
I_{IH}	Input HIGH Current				20 0 1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current				- 0 4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	Q_0, Q_1, Q_2, Q_3	- 30		- 130	V_{CC} = MAX, V_{OUT} = 0 V		mA
		Q_3	- 20		- 100			
I_{CC}	Power Supply Current				34 31	Cond. a Cond. b	V_{CC} = MAX (See Note 3)	mA

Notes : 1 Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
2. Not more than one output should be shorted at a time
3 I_{CC} is measured with the outputs open, DS input and S input at 4 5 V and Pn inputs grounded under the following conditions
a OE at 4 5 V and a 3 V positive pulse applied to CP input
b. OE and CP input grounded
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C

AC CHARACTERISTICS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
f_{MAX}	Maximum Clock Frequency	30	45		O_0, O_1, O_2, O_3 outputs: R_L = 667 Ω, C_L = 45 pF O_3 output: R_L = 2.0 KΩ, C_L = 15 pF	MHz
t_{PHL}	Propagation Delay, High to Low Level Output from Clear		22	35		ns
t_{PLH}	Propagation Delay Time Low to High Level Output		15	30		ns
t_{PHL}	Propagation Delay Time High to Low Level Output		20	30		ns
t_{PZH}	Output Enable Time to High Level		15	25		ns
t_{PZL}	Output Enable Time to Low Level		17	25		ns
t_{PHZ}	Output Disable Time from High Level		11	17	C_L = 5 pF	ns
t_{PLZ}	Output Disable Time from Low Level		12	20		ns

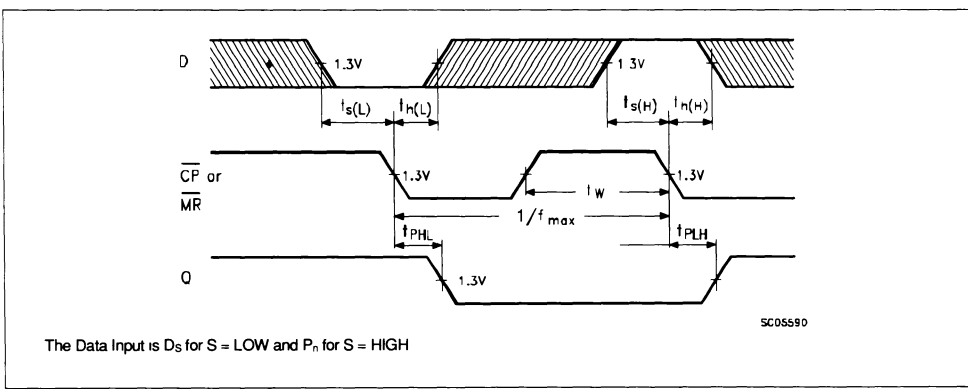
AC SET-UP REQUIREMENTS: T_A = 25 °C

Symbol	Parameter		Limits			Test Conditions	Units
			Min.	Typ.	Max.		
$t_W(CP)$	Clock Pulse Width		16			V_{CC} = 5.0 V	ns
t_s*	Set-up Time	Load/Shift Input	40				ns
		All other Inputs	20				
t_h*	Hold Time		10				ns

* High or Low Level Data

AC WAVEFORMS AND LOAD CIRCUIT

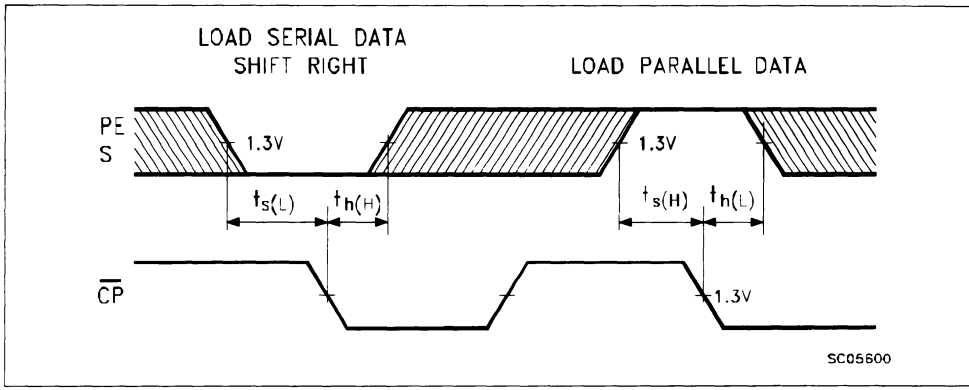
Figure 1



The Data Input is D_S for S = LOW and P_n for S = HIGH

The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 2



The shaded areas indicate when the input is permitted to change for predictable output performance

Figure 3

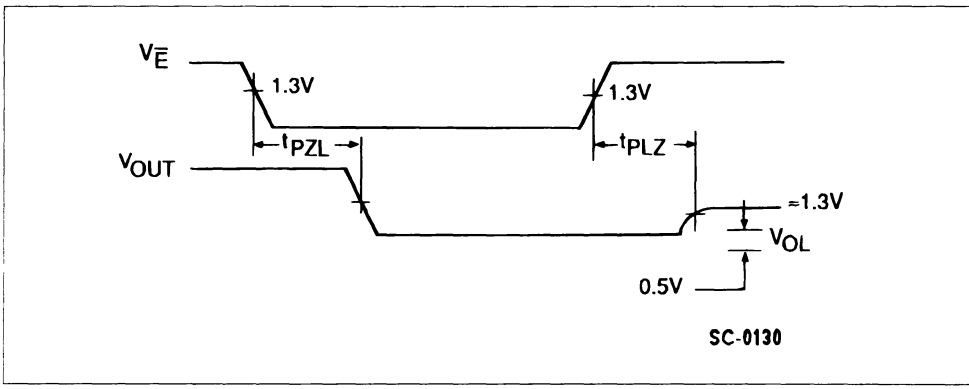


Figure 4

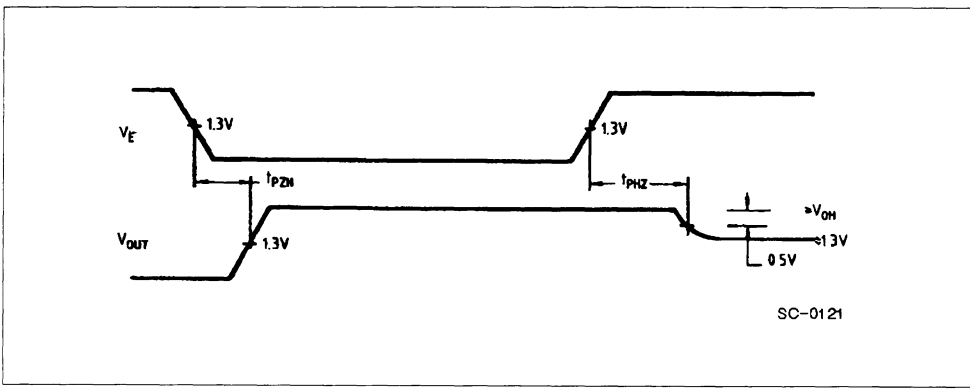
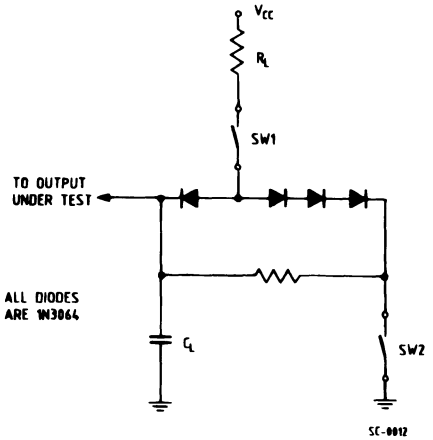


Figure 5.



SWITCH POSITION

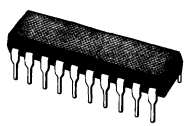
Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

SGS-THOMSON MICROELECTRONICS

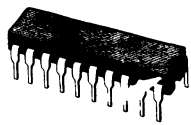
T74LS399

QUAD 2-PORT REGISTER

- FULLY POSITIVE EDGE-TRIGGERED OPERATION
- SELECT FROM TWO DATA SOURCES
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS399 D1 T74LS399 C1
T74LS399 B1 T74LS399 M1

DESCRIPTION

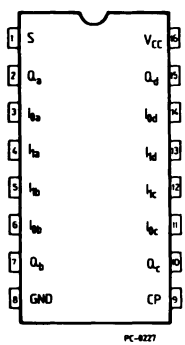
The T74LS399 is a Quad 2-Port Register. It is logical equivalent to a quad 2-input multiplexer followed by a 4-bit edge-triggered register. The selected data is transferred to the output register on the LOW-to-HIGH transition of the Clock input.

PIN NAMES

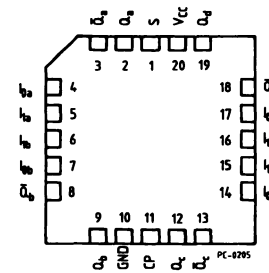
S	COMMON SELECT INPUT
CP	CLOCK (Active HIGH going edge) INPUT
I_{0a}–I_{0d}	DATA INPUT FROM SOURCE 0
I_{1a}–I_{1d}	DATA INPUT FROM SOURCE 1
Q_a–Q_d	REGISTER TRUE OUTPUTS
$\overline{Q}_a$–$\overline{Q}_d$	REGISTER COMPLEMENTARY OUTPUTS

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

FUNCTIONNAL DESCRIPTION

This high speed Quad 2-Port Register selects four bits of data from two sources (Port) under the control of a Common Select Input (S). The 4-bit Output Register where selected data are transferred is synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit RS type output register is fully edge-triggered. Predictable operation is assured if Data inputs (I) and select inputs (S) are kept stable only a set-up time prior to and hold time after the LOW-to-HIGH transition of the Clock input.

TRUTH TABLE

Inputs			Outputs
S	I_0	I_1	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't care
l = LOW Voltage Level one set–up Time Prior to the LOW–to–HIGH Clock Transition
h = High Voltage Level one set–up Time Prior to the LOW–to–HIGH Clock Transition

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	0 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS399XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for all Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for all Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current			20 40	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Supply Current			13	V_{CC} = MAX		mA

Notes : 1 For conditions shown as MIN or MAX, use the appropriate value specified under garanteed operating ranges.
2. Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output Q		18 21	27 32	V_{CC} = 5.0 V C_L = 15 pF	ns

AC SET-UP REQUIREMENTS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_w	Clock Pulse Width	20			V_{CC} = 5.0 V	ns
t_s	Data Set-up Time	25				ns
t_s	Select Set-up Time	45				ns
t_h	Hold Time, Any Input	0				ns

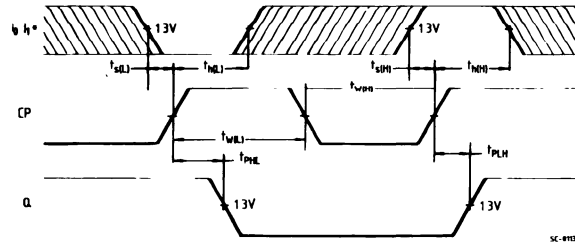
DEFINITION OF TERMS

SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

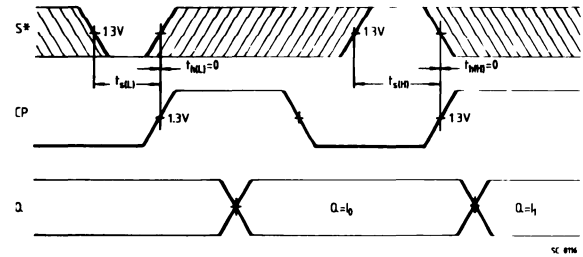
AC WAVEFORMS

Figure 1 .



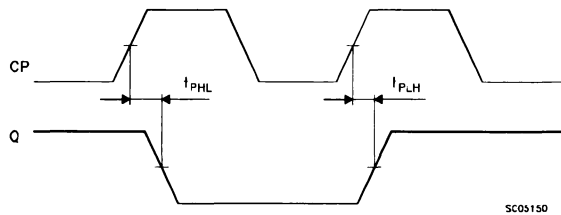
* The shaded areas indicate when the input is permitted to change for predictable output performance

Figure 2 .



* The shaded areas indicate when the input is permitted to change for predictable output performance

Figure 3 .

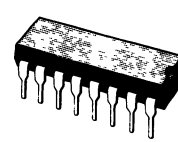


SGS-THOMSON MICROELECTRONICS

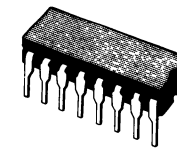
T74LS490

DUAL DECADE COUNTER

- DUAL VERSION OF 74LS90
- INDIVIDUAL ASYNCHRONOUS CLEAR AND PRESET TO 9 FOR EACH COUNTER
- COUNT FREQUENCY - TYPICALLY 35 MHz
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS490 D1
T74LS490 B1
T74LS490 C1
T74LS490 M1

DESCRIPTION

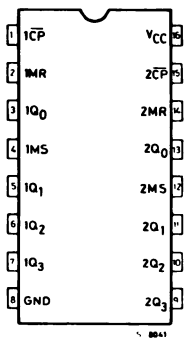
The T74LS490 contains a pair of high-speed 4-stage ripple counters. Each half of the T74LS490 has individual Clock, Master Reset and Master Set (Preset 9) inputs. Each section counts in 8, 4, 2, 1 BCD code.

PIN NAMES

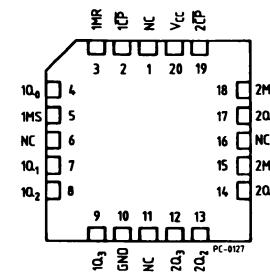
MS	MASTER SET (set to 9) INPUT
MR	MASTER RESET
CP	CLOCK INPUT (active HIGH going edge)
Q_0-Q_3	COUNTER OUTPUTS

PIN CONNECTION (top view)

DUAL IN LINE

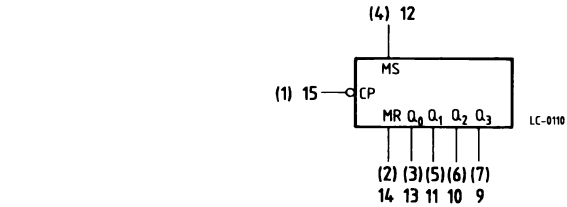


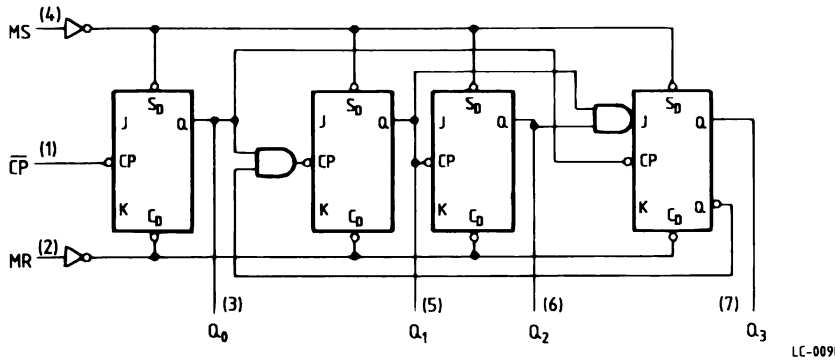
CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM





V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 5.5	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only oand functional operation to the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS490XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = Package type

TRUTH TABLE

Count	Outputs			
	Q3	Q2	Q1	Q0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Condition (note 1)		Unit
			Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage		2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage				0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage			- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage		2.7			V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage			0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
				0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current	MR, MS			20	V_{CC} = MAX, V_{IN} = 2.7 V		µA
		$\overline{CP}$			60			
		$\overline{CP}$			- 300	V_{CC} = MAX, V_{IN} = 7.0 V V_{IN} = 5.5 V $\overline{CP}$ Only		µA
		MR, MS			100			
I_{IL}	Input LOW Current	$\overline{CP}$			- 2.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
		MR, MS			- 0.4			
I_{OS}	Output Short Circuit Current (note 2)		- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current			19	30	V_{CC} = MAX		mA

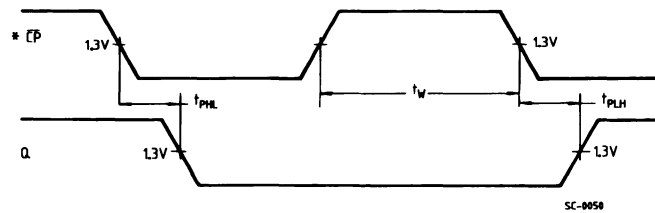
Notes : 1. For conditions shown as MIN or MAX, use the appropnate value specified under guaranteed operating conditions for the device type
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C

AC CHARACTERISTICS : $T_A = 25\ °C$

Symbol	Parameter		Limits			Test Conditions		Unit
			Min.	Typ.	Max.			
f_{MAX}	Maximum Input Count Frequency		25	35		Fig. 1	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ $R_L = 2\ k\Omega$	MHz
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}$ to Q_0			12 13	20 20	Fig. 1		ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}$ to Q_1 or Q_3			24 26	39 39	Fig. 3		ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}$ to Q_2			32 36	54 54	Fig. 2		ns
t_{PHL}	Propagation Delay, MR to Output			24	39	Fig. 2		ns
t_{PLH} t_{PHL}	Propagation Delay, MS to Output	Q_0, Q_3		24	39	Fig. 2		ns
		Q_1, Q_2		20	36			

AC WAVEFORMS

Figure 1.



The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the Truth Table

Figure 2.

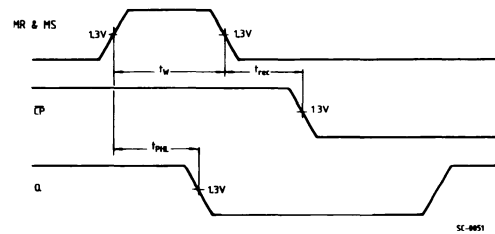
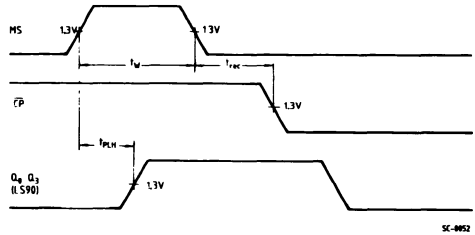


Figure 3.



SGS-THOMSON MICROELECTRONICS

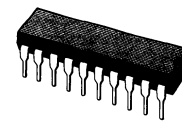
T74LS533
T74LS534

LS533 - OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS
LS534 - OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

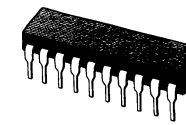
DESCRIPTION

The T74LS533 is an Octal Transparent latch with 3-State Outputs designed for bus organised sustem applications. When Latch Enable (LE) is High the data appears transparent to the flip-flop when it is Low the data is latched. When the output Enable goes HIGH the bus output is in the high impedance state. The LS533 is functionally indentical to the LS373, with the exception of the inverted outputs.

The T74LS534 is an octal D-Type flip-flop with 3-State Outputs designed for bus oriented applications. It is composed of a buffered clock and an output Enable common to all flip-flops. The LS534 is functionally identical to the LS374 with the exception that the outputs are inverted.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

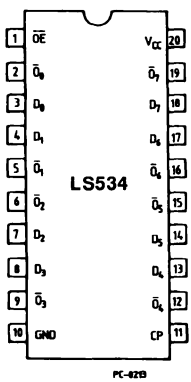
T74LSXXX D1 T74LSXXX C1
T74LSXXX B1 T74LSXXX M1

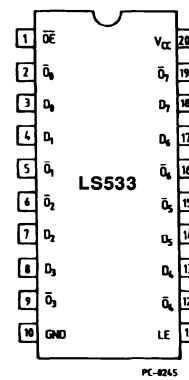
PIN NAMES

D_0–D_7	DATA INPUTS
LE	LACTCH ENABLE (active HIGH) INPUT
$\overline{CP}$	CLOCK (active HIGH going edge) INPUT
$\overline{OE}$	OUTPUT ENABLE (active LOW) INPUT
$\overline{O}_0$–$\overline{O}_7$	OUTPUTS

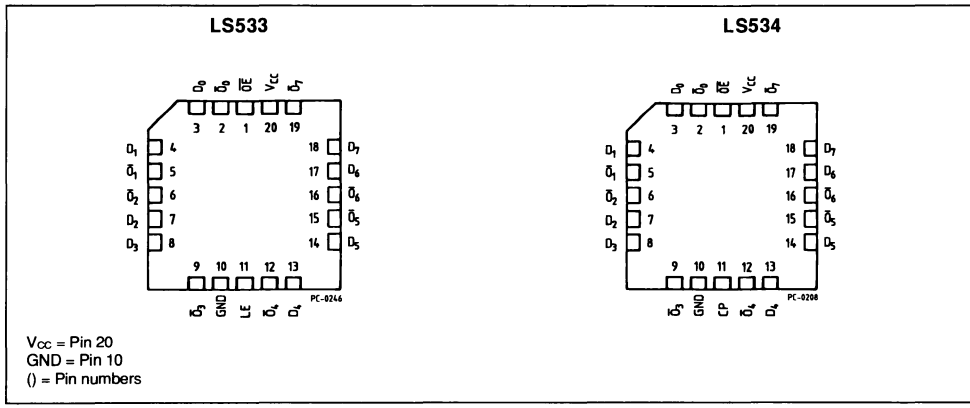
PIN CONNECTION (top view)

DUAL IN LINE

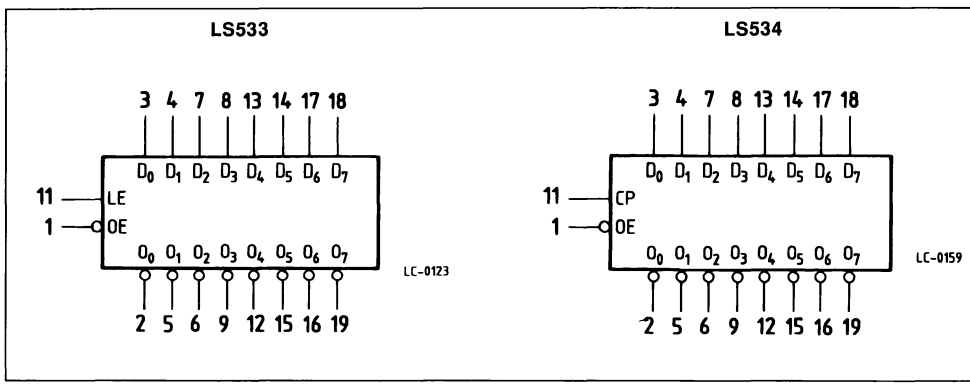




CHIP CARRIER



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS533/534XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.4	3.1		V_{CC} = MIN, I_{OH} = - 2.6 mA V_{IN} = V_{IH}		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 12 mA	V_{CC} = MIN V_{IN} = V_{IL}	V
			0.35	0.5	I_{OL} = 24 mA		V
I_{OZH}	Output Off Current HIGH			20	V_{CC} = MAX, V_{OUT} = 2.7 V		
I_{OZL}	Output Off Current LOW			- 20	V_{CC} = MAX, V_{OUT} = 0.4 V		
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 30		- 130	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current			40	V_{CC} = MAX		mA

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5 0 V, T_A = 25 °C.

AC CHARACTERISTICS: T_A = 25 °C

Symbol	Parameter	Limits			Test Condition	Unit
		Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay, Data to Output (LS533 Only)		15	25	V_{CC} = 5 V R_L = 667 Ω C_L = 45 pF	ns
t_{PLH}	Propagation Delay, LE to Ouptput (LS533 Only)		20	35		ns
t_{PHL}	Propagation Delay, LE to Ouptput (LS533 Only)		22	35		ns
t_{PLH}	Propagation Delay, Clock to Output (LS534 Only)		16	30		ns
t_{PHL}	Propagation Delay, Clock to Output (LS534 Only)		24	30		ns
t_{PZH}	Enable Time to High Level (LS533 Only)		16	30		ns
t_{PZL}	Enable Time to Low Level (LS533 Only)		19	36		ns
t_{PZH}	Enable Time to High Level (LS534 Only)		18	30		ns
t_{PZL}	Enable Time to Low Level (LS534 Only)		18	30		ns
t_{PLZ}	Disable Time from Low Level (LS533 Only)		13	29	V_{CC} = 5 V R_L = 667 Ω C_L = 5 pF	ns
t_{PLZ}	Disable Time from Low Level (LS533 Only)		12	29		ns
t_{PHZ}	Disable Time from High Level		11	24		ns

AC SET-UP REQUIREMENTS: T_A = 25 °C

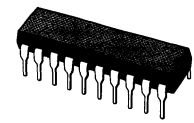
Symbol	Parameter	Limits			Test Condition	Unit
		Min.	Typ.	Max.		
t_s	Set-up Time (LS533 Only)	5			V_{CC} = 5 V	ns
t_s	Set-up Time (LS534 Only)	15	20			ns
t_h	Hold Time (LS533 Only)	20				ns
t_h	Hold Time (LS534 Only)	-3	0			ns
t_w	Minimum Pulse Width (LS533 Only)	15				ns
t_w	Minimum Pulse Width (LS534 Only)	10	13			ns

SGS-THOMSON MICROELECTRONICS

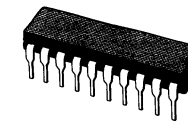
T74LS540
T74LS541

OCTAL BUFFER/LINE DRIVERS WITH 3-STATE OUTPUTS

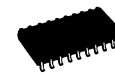
- PNP INPUTS REDUCE LOADING
- 3-STATE OUTPUTS DRIVE BUS LINES
- INPUTS AND OUTPUTS OPPOSITE SIDE OF PACKAGE, ALLOWING EASIERS INTERFACE TO MICROPROCESSOR
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS



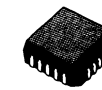
B1
(Plastic Package)



D1
(Ceramic Package)



M1
(Micro Package)



C1
(Plastic Chip Carrier)

ORDER CODES :

T74LSXXX D1	T74LSXXX C1
T74LSXXX B1	T74LSXXX M1

DESCRIPTION

The T74LS540/541 are Octal Buffers and Line Drivers. Although they have the same functions as LS240 and LS241, they offer a pinout with inputs and outputs on apposite sides of the package. These device are disigned to be used with 3-state memory address drivers, etc.

TRUTH TABLE

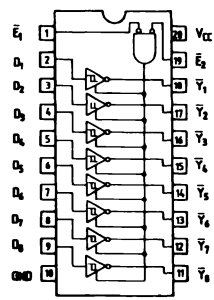
Inputs			Outputs	
$\overline{E}_1$	$\overline{E}_2$	D	LS540	LS541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
Z = HIGH Impedance

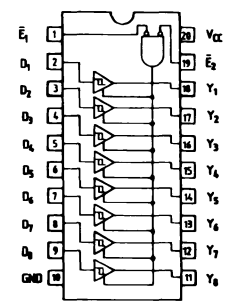
PIN CONNECTION (top view)

DUAL IN LINE

LS540

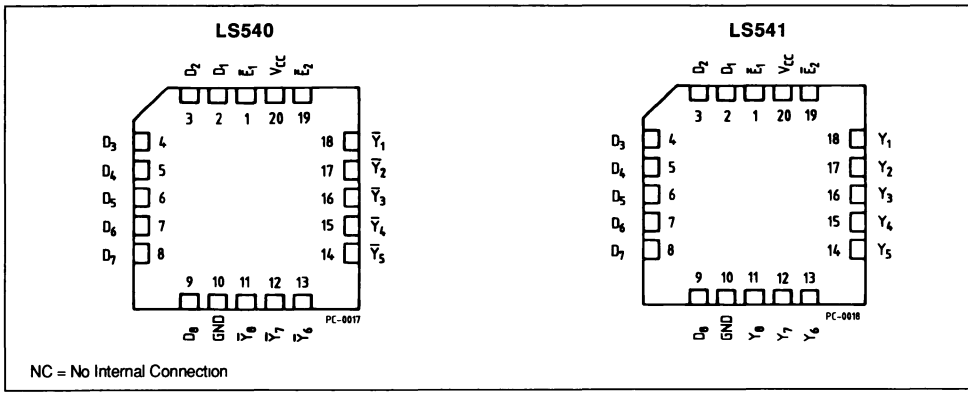


LS541

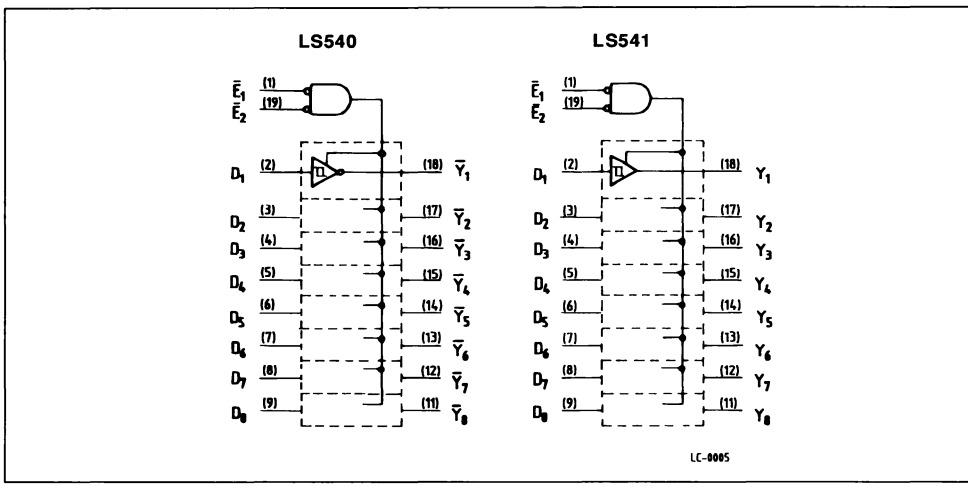


NC = No Internal Connection

CHIP CARRIER



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	0 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS540/541XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Input		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Input		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.4	3.4		V_{CC} = MIN, I_{OH} = - 3.0 mA		V
		2.0			V_{CC} = MIN, I_{OH} = - 15 mA V_{IL} = 0.5 V		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
V_{T+}-V_{T-}	Hysteresis	0.2	0.4		V_{CC} = MIN		
I_{OZH}	Output Off Current HIGH			20	V_{CC} = MAX, V_{OUT} = 2.7 V		µA
I_{OZL}	Output Off Current LOW			- 20	V_{CC} = MAX, V_{OUT} = 0.4 V		µA
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V VCC = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.2	VCC = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 40		- 225	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current Total, Output HIGH LS540 LS541			 25 32	V_{CC} = MAX		mA
	Total, Output LOW LS540 LS541			45 52			
	Total, Output 3-State LS540 LS541			52 55			

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS (T_A = 25 °C)

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Test Conditions (note 1)	Unit
t_{PLH}	Propagation Delay, Data to Output	LS540		9.0	15	V_{CC} = 5.0 V C_L = 45 pF R_L = 667 Ω	ns
		LS541		12	15		
t_{PHL}		LS540		12	15		ns
		LS541		12	18		
t_{PZH}	Output Enable Time to HIGH Level	LS540		15	25		ns
		LS541		15	32		
t_{PZL}	Output Enable Time to LOW LEvel	LS540		20	38		ns
		LS541		20	38		
t_{PHZ}	Output Disable Time from HIGH Level	LS540		10	18	C_L = 5.0 pF	ns
		LS541		10	18		
t_{PLZ}	Output Diable Time to LOW Level	LS540		15	25		ns
		LS541		15	29		

AC WAVEFORMS

Figure 1.

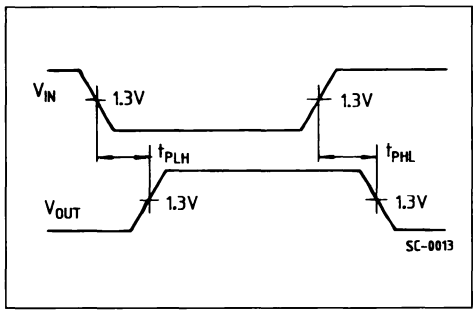


Figure 2.

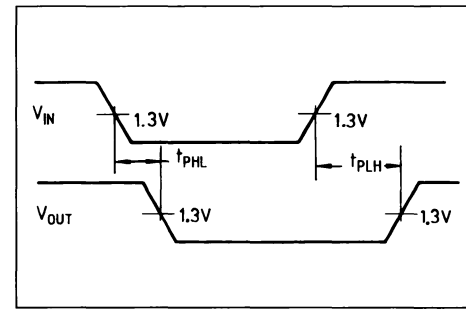


Figure 3.

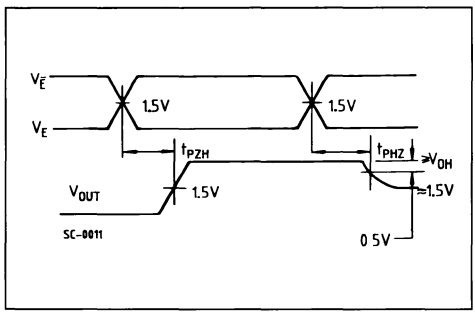
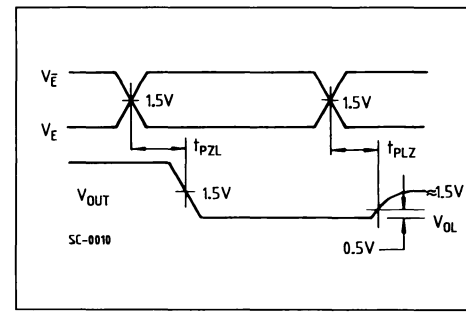
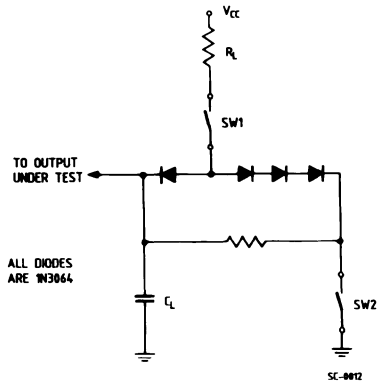


Figure 4.



AC LOAD CIRCUIT

Figure 5.



SWITCH POSITION

Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

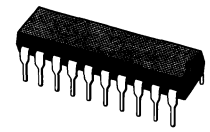
SGS-THOMSON MICROELECTRONICS

T74LS645

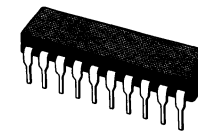
OCTAL BUS TRANSCEIVERS

DESCRIPTION

The T74LS645 is an octal bus transceiver designed for asynchronous two-way communication between data buses. Control function implementation reduces to a minimum external timing requirements. This circuit permits transmission of data from the A bus to B or from the B bus to A bus depending upon the logic level of the direction control (DIR) input. The device can be disabled by the Enable input (G) causing the buses to be effectively isolated.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

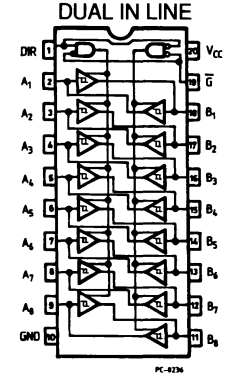
C1
(Plastic Chip Carrier)

ORDER CODES :

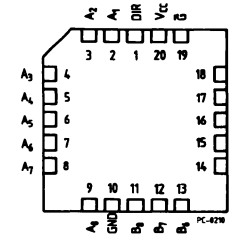
T74LS645 D1 T74LS645 C1
T74LS645 B1 T74LS645 M1

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

TRUTH TABLE

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS645XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for all Inputs		V
V_{IL}	Input LOW Voltage			0.6	Guaranteed Input LOW Voltage for all Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.4 2.0	3.4		V_{CC} = MIN, I_{OH} = - 3.0 mA V_{CC} = MIN, I_{OH} = - 15 mA		V V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 12 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 24 mA		V
I_{OZH}	Output Off Current HIGH			20	V_{CC} = MAX, V_{OUT} = 2.7 V		µA
I_{OZL}	Output Off Current LOW			- 400	V_{CC} = MAX, V_{OUT} = 0.4 V		µA
I_{IH}	Input HIGH Current DIR or $\overline{G}$ DIR or $\overline{G}$ A or B			 20 0.1 0.1	 V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V V_{CC} = MAX, V_{IN} = 5.5 V		 µA mA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 40		- 225	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Supply Current Total, Output HIGH Total, Output LOW Total at HIGH Z			 70 90 95	V_{CC} = MAX		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay, A to B		8.0 11	15 15	C_L = 45 pF R_L = 667 Ω	ns
t_{PLH} t_{PHL}	Propagation Delay, B to A		8.0 11	15 15		ns
t_{PZL} t_{PZH}	Output Enable Time, $\overline{G}$ DIR to A		31 26	40 40		ns
t_{PZL} t_{PZH}	Output Enable Time, $\overline{G}$ DIR to B		31 26	40 40		ns
t_{PLZ} t_{PHZ}	Output Disable Time, $\overline{G}$ DIR to A		15 15	25 25	C_L = 5.0 pF	ns
t_{PLZ} t_{PHZ}	Output Disable Time, $\overline{G}$ DIR to B		15 15	25 25		ns

4 X 4 REGISTER FILE WITH 3-STATE OUTPUTS

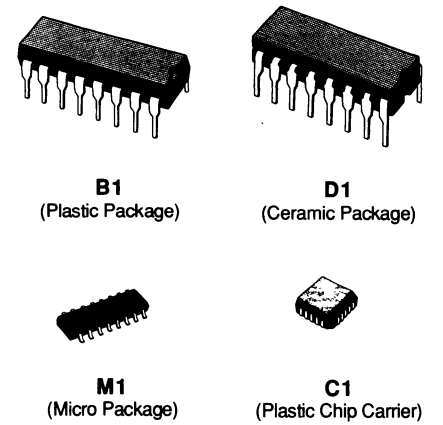
- SIMULTANEOUS READ/WRITE OPERATION
- EXPANDABLE TO 512 WORDS OF n-BIT
- TYPICAL ACCESS TIME OF 20 ns
- 3-STATE OUTPUTS FOR EXPANSION
- TYPICAL POWER DISSIPATION OF 125 mW

DESCRIPTION

The TTL/MSI T74LS670 is a high speed, low-power 4 x 4 Register File organized as four words by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation.

The 3-State outputs make it possible to connect up to 128 outputs to increase the word capacity up to 512 words. Any number of these device can be operated in parallel to generate an n-bit lenght.

The T74LS170 provides a simular function to this device but is features open-collector outputs.



B1 (Plastic Package)

D1 (Ceramic Package)

M1 (Micro Package)

C1 (Plastic Chip Carrier)

ORDER CODES :

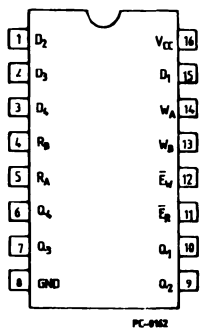
T74LS670 D1
T74LS670 B1
T74LS670 C1
T74LS670 M1

PIN NAMES

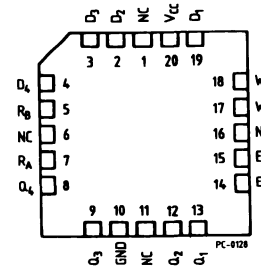
D_1-D_4	DATA INPUTS
$\overline{W}_A$, W_B	WRITE ADDRESS INPUTS
$\overline{E}_W$	WRITE ENABLE (active LOW) INPUT
$\overline{R}_A$, R_B	READ ADDRESS INPUTS
$\overline{E}_R$	READ ENABLE (active LOW) INPUT
Q_1-Q_4	OUTPUTS

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

WRITE FUNCTION TABLE AND READ FUNCTION TABLE

(see notes A, B and C)

Write Inputs			Word			
WB	WA	EW	0	1	2	3
L	L	L	Q = D	00	00	00
L	H	L	00	Q = D	00	00
H	L	L	00	00	Q = D	00
H	H	L	00	00	00	Q = D
X	X	H	00	00	00	00

(see notes A, and D)

Read Inputs			Outputs			
RB	RA	ER	01	02	03	04
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

Notes : A. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, Z = HIGH Impedance
B Q = D = The four selected internal flip-flops will assume the state applied to the 4 external data inputs
C. 00 = The level of 0 before the indicated input conditions were established.
D. W0B1 = The first bit word 0, etc.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 50 to 5	mA
I_O	Output Current, into Outputs	50	mA

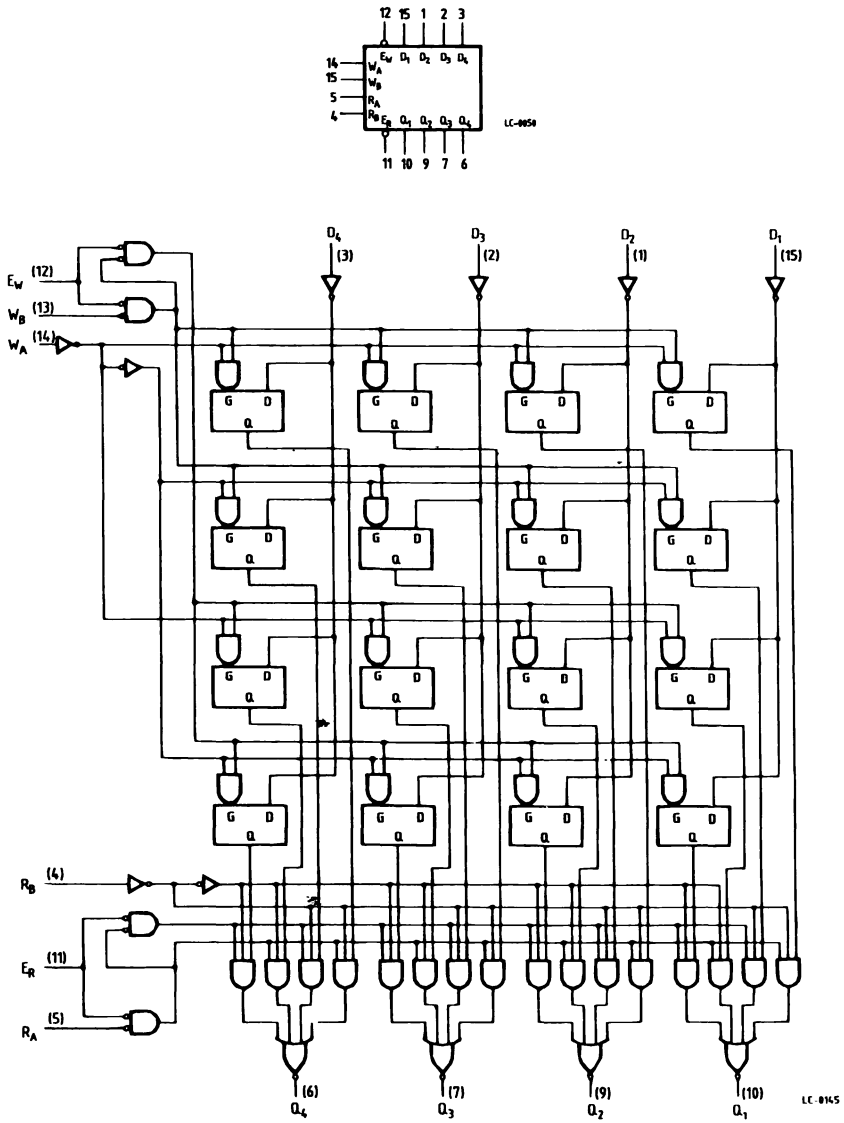
Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS670XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = Package type.

LOGIC SYMBOL AND LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Input		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Input		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.4	3.1		V_{CC} = MIN, I_{OH} = - 2.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{OZH}	Output Off Current HIGH			20	V_{CC} = MAX, V_{OUT} = 2.7 V V_{IH} = 2.0 V		µA
I_{OZL}	Output Off Current LOW			- 20	V_{CC} = MAX, V_{OUT} = 0.4 V V_{IH} = 2.0 V		µA
I_{IH}	Input HIGH Current Any D, R or W $\overline{E}_W$ $\overline{E}_R$			 20 40 60	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	Any D, R or W $\overline{E}_W$ $\overline{E}_R$			0.1 0.2 0.3	VCC = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current Any D, R or W $\overline{E}_W$ $\overline{E}_R$			 - 0.4 - 0.8 - 1.2	VCC = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 30		- 130	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current (note 3)		30	50	V_{CC} = MAX		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2 Not more than one output should be shorted at a time.
3. Maximum I_{CC} is guaranteed for the following worst-case conditions : 4 5 V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : $T_A = 25$ °C

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, R_A or R_B to Q Outputs		23 25	40 45	Fig. 2		ns
t_{PLH} t_{PHL}	Propagation Delay, Negative Going $\overline{E}_W$ to Q Outputs		26 28	45 50	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs to Q Outputs		25 23	45 40	Fig. 1		ns
t_{PZH}	Enable Time, Negative Going $\overline{E}_R$ to Q Outputs Going HIGH		15	35	Figs. 4, 5		ns
t_{PZL}	Enable Time, Negative Going $\overline{E}_R$ to Q Outputs Going LOW		22	40	Figs. 3, 5	V_{CC} = 5.0 V C_L = 5.0 pF	ns
t_{PHZ}	Disable Time, Positive Going $\overline{E}_R$ to Q Outputs Off from HIGH		30	50	Figs. 4, 5		ns
t_{PLZ}	Disable Time, Positive Going $\overline{E}_R$ to Q Outputs Off from LOW		16	35	Figs. 3, 5		ns

AC CHARACTERISTICS : $T_A = 25$ °C

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_W	Clock Pulse Width (LOW) for $\overline{E}_W$	25			V_{CC} = 5.0 V Fig. 3	ns
t_sD (note 5)	Set-up Time, Data Inputs with Respect to Positive-going $\overline{E}_W$	10				ns
t_hD	Hold Time, Data Inputs with Respect to Positive-going $\overline{E}_W$	15				ns
t_sW (note 7)	Set-up Time, Write Select Inputs W_A and W_B with Respect to Negative-going $\overline{E}_W$	15				ns
t_hW	Hold Time, Write Select Inputs W_A and W_B with Respect to Negative-going $\overline{E}_W$	5				ns
t_{rec}	Recovery Time	25				ns

Notes : 5. The data to Enable Set-up time is defined as the time required for the logic level to be present at the data input prior to the enable transition from LOW to HIGH in order for latch to recognize and store the new data.

6. The hold time (t_h) is defined as the minimum time following the enable transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition.

7. The address to Enable Set-up Time is the time before the HIGH to LOW Enable transition that the address must be stable so that the correct latch is addressed and the other latches are not affected.

8. The Shaded areas indicate when the input is permitted to change for predictable output performance.

AC WAVEFORMS

Figure 1.

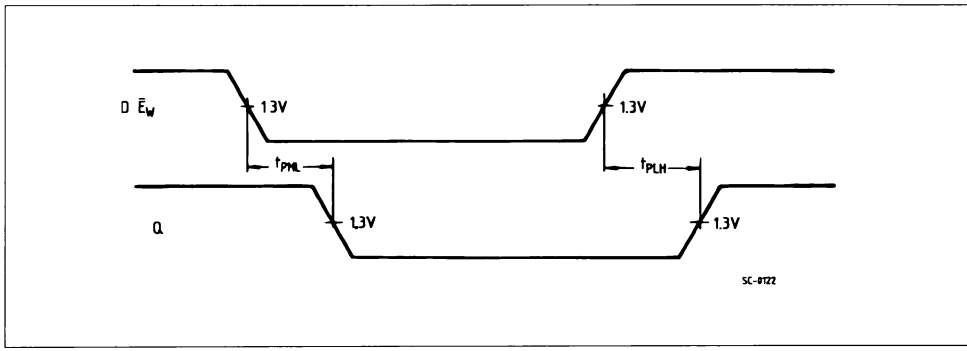


Figure 2.

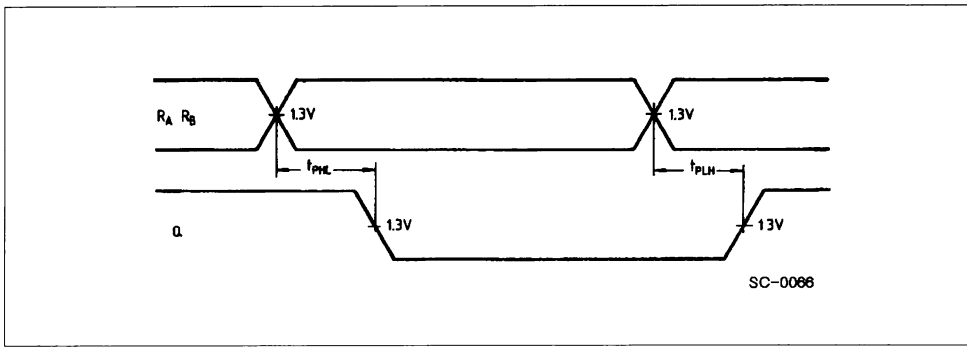
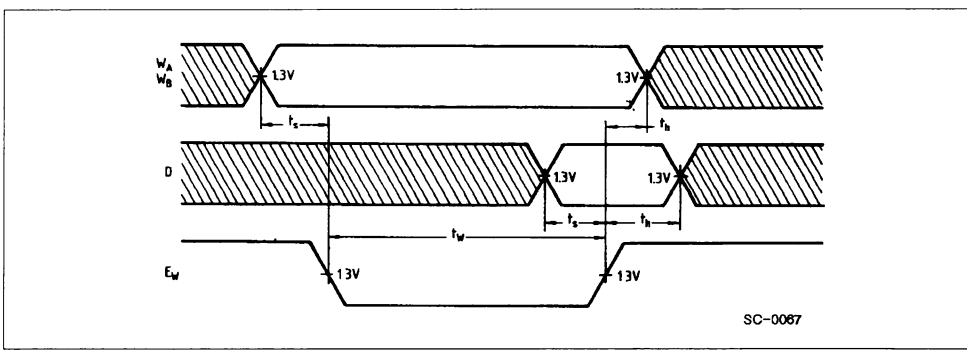


Figure 3.

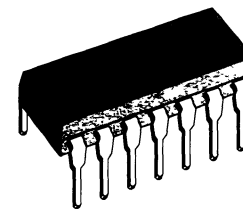


PACKAGES

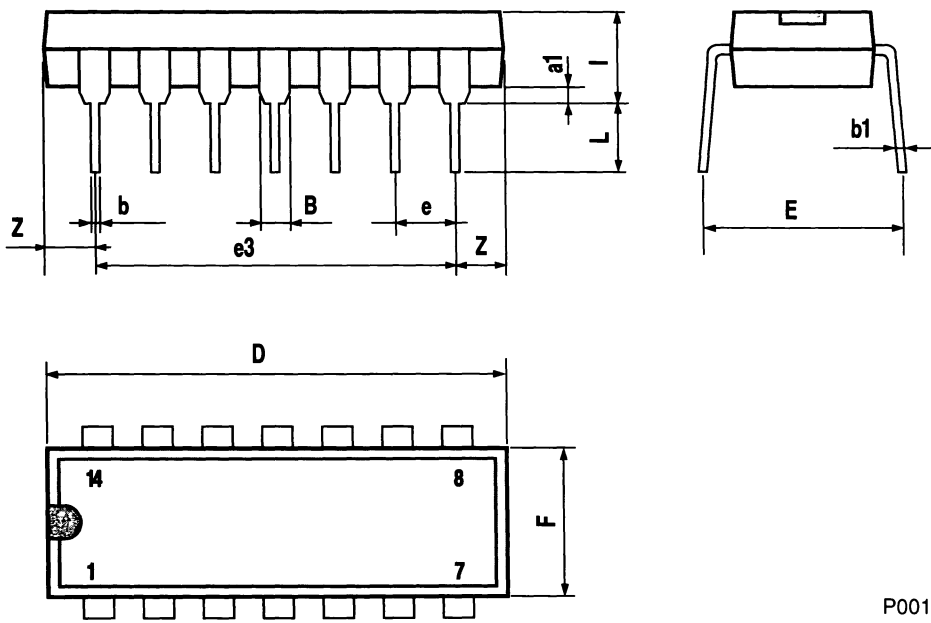
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Plastic DIP14

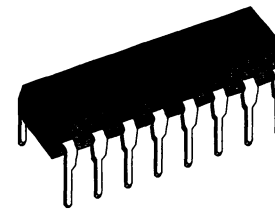


P001A

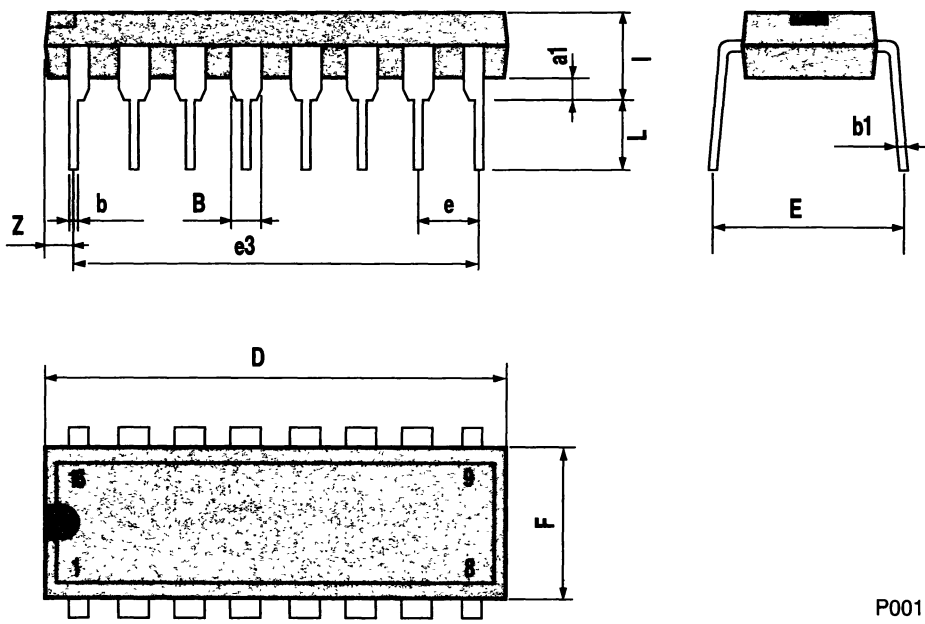
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Plastic DIP16 (0.25)

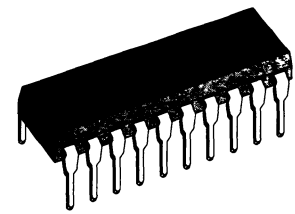


P001C

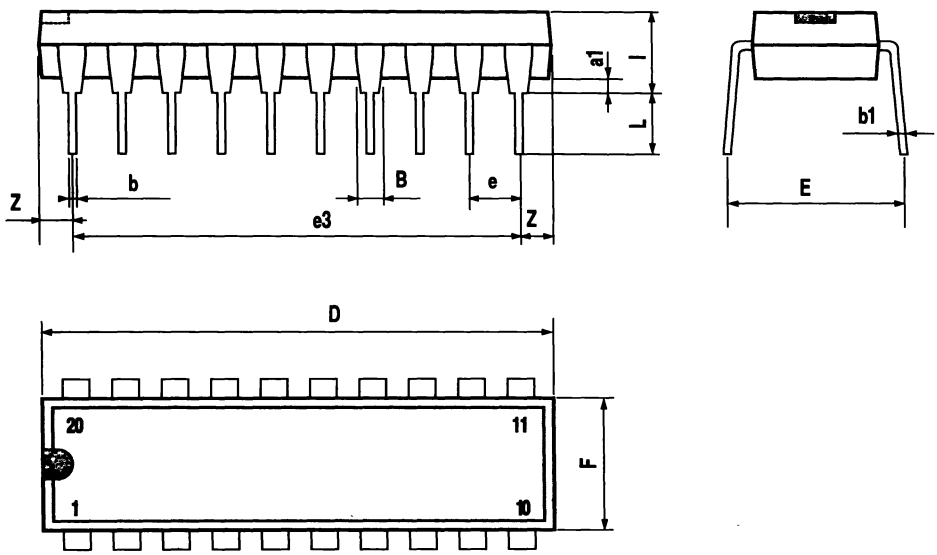
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Plastic DIP20 (0.25)

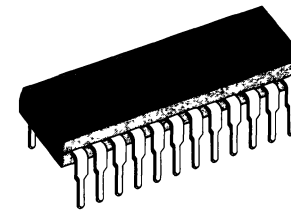


P001J

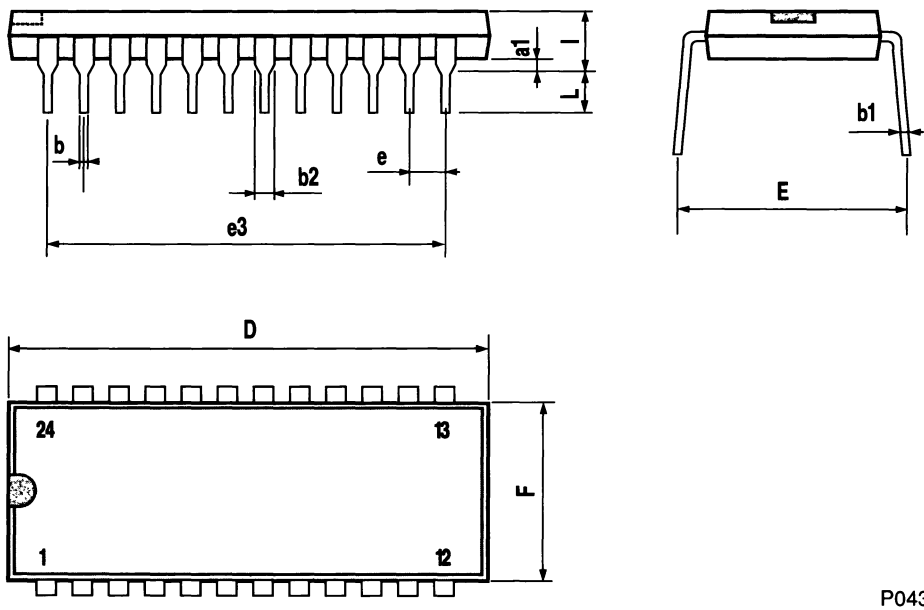
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Plastic DIP24 (0.25)

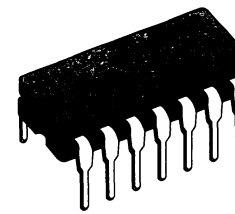


P043A

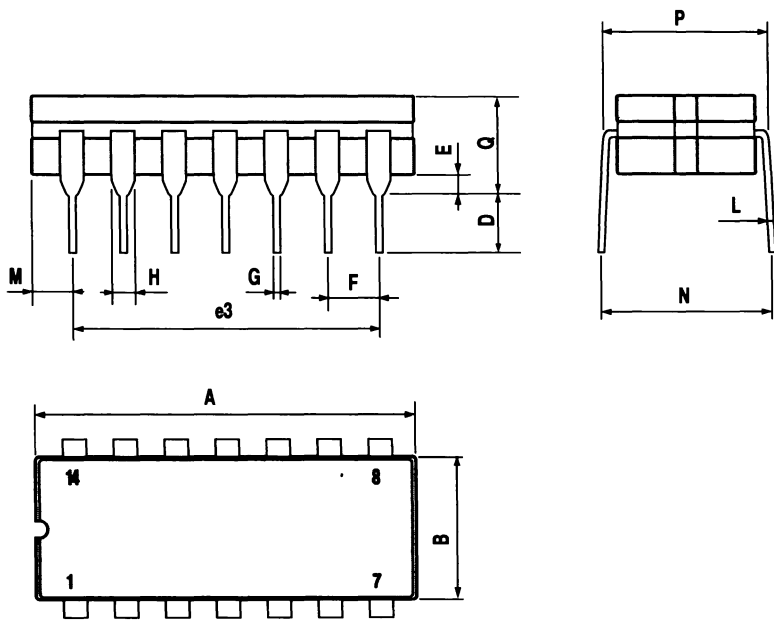
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7.0			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		15.24			0.600	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.54	0.060		0.100
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Ceramic DIP14/1

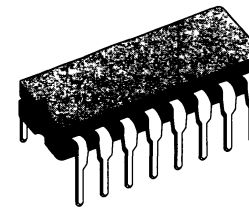


P053C

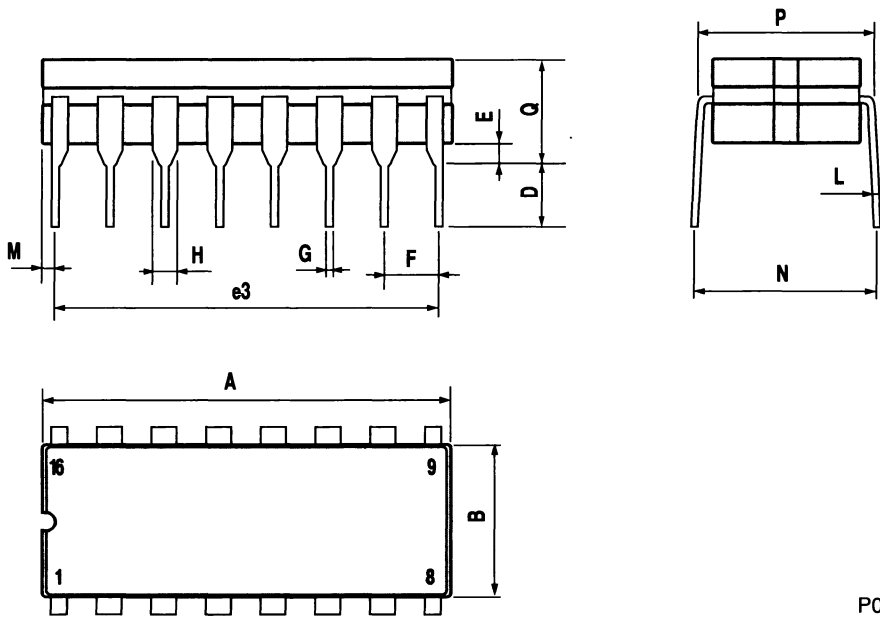
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		17.78			0.700	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



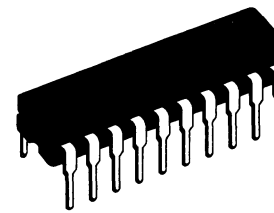
Ceramic DIP16/1

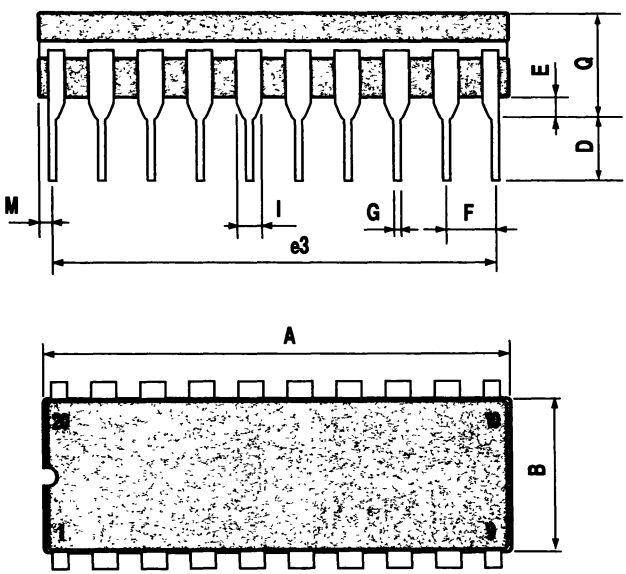


P053D

A			25			0.984
B			7.8			0.307
D		3.3			0.130	
E	0.5		1.78	0.020		0.070
e3		22.86			0.900	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
I	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N1	4° (min.), 15° (max.)					
P	7.9		8.13	0.311		0.320
Q			5.71			0.225

SGS-THOMSON MICROELECTRONICS



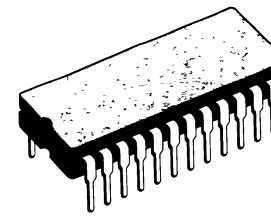


P057H

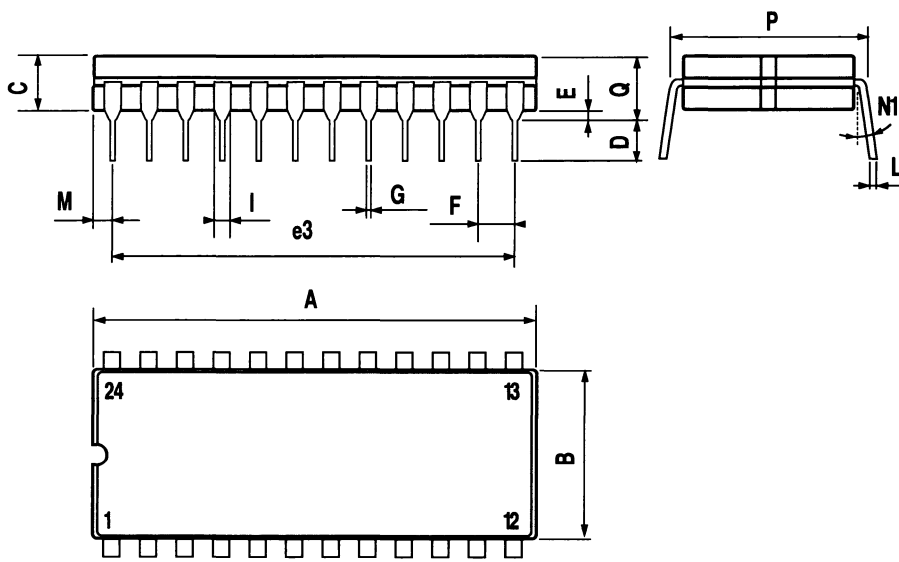
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			32.3			1.272
B	13 05		13.36	0 514		0.526
C	3.9		5.08	0.154		0.200
D	3			0.118		
E	0.5		1.78	0.020		0.070
e3		27 94			1.100	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0 022
I	1 17		1.52	0.046		0 060
L	0.22		0 31	0.009		0.012
M	1.52		2.49	0.060		0.098
N1	4° (mın.), 15° (max.)					
P	15.4		15.8	0.606		0.622
Q			5.71			0.225

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Ceramic DIP24

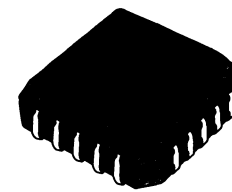


P058C

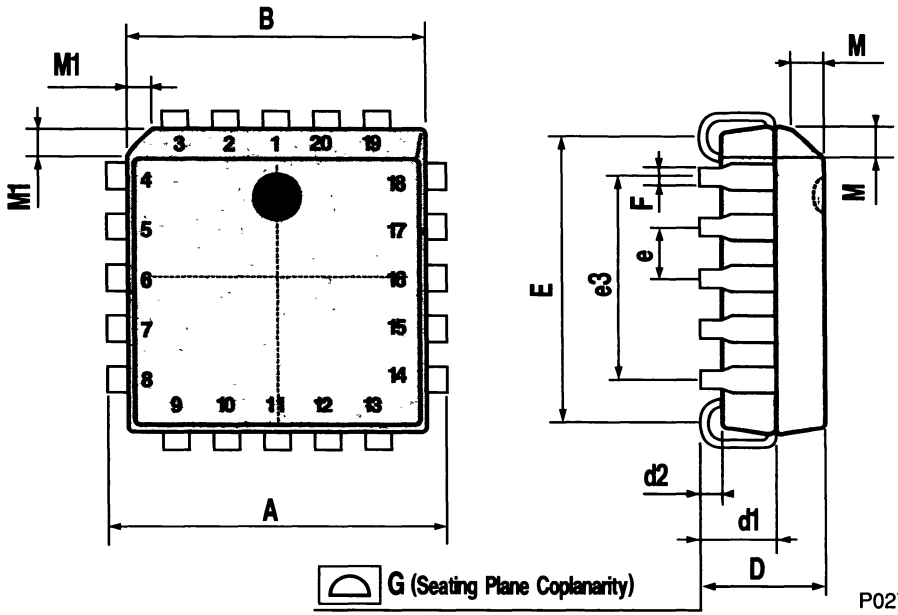
	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



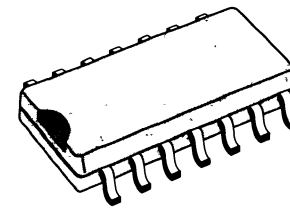
PLCC20



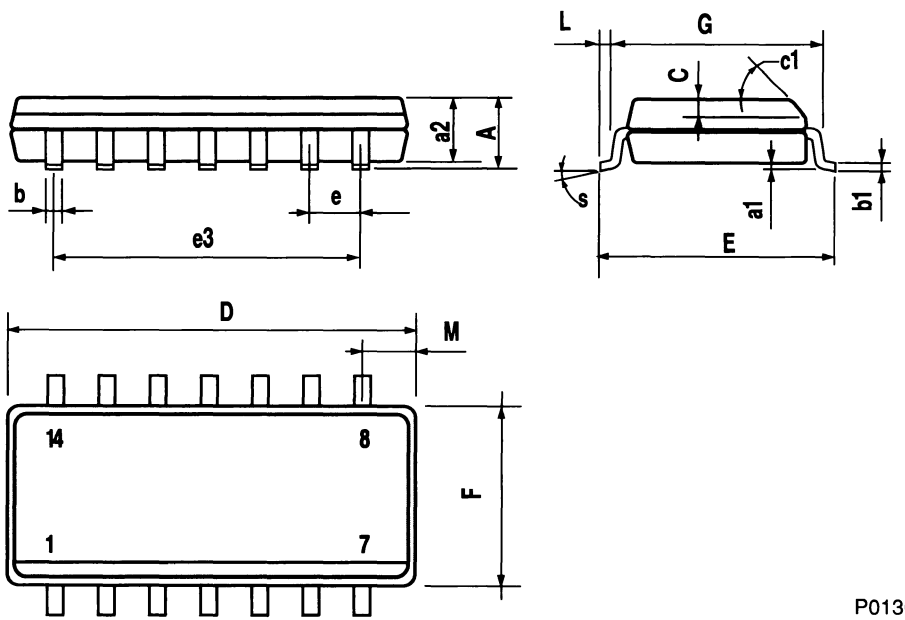
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.2	0.004		0.008
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.15		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0 020		0.050
M			0.68			0.027
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO14

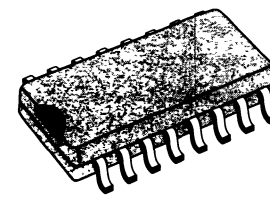


P013G

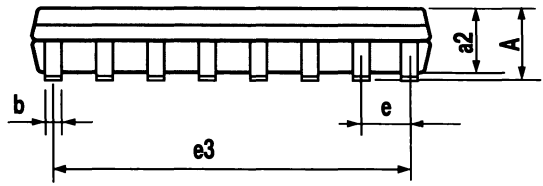
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.2	0.004		0.008
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.150		0.157
G	4.6		5.3	0.181		0.209
L	0.5		1.27	0.020		0.050
M			0.62			0.024
S	8° (max.)					

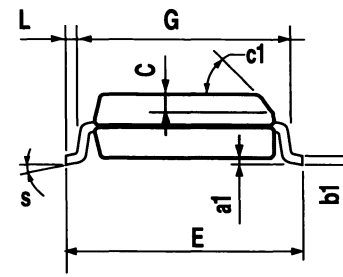
SGS-THOMSON MICROELECTRONICS

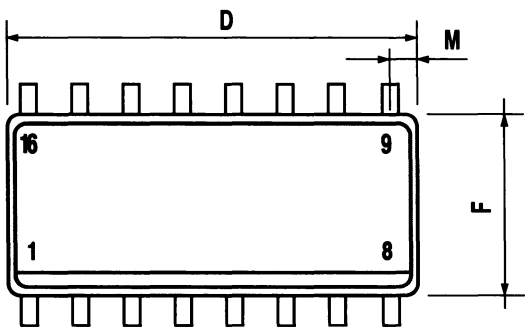
OUTLINE AND MECHANICAL DATA



SO16





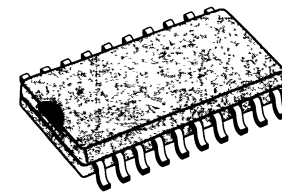


P013H

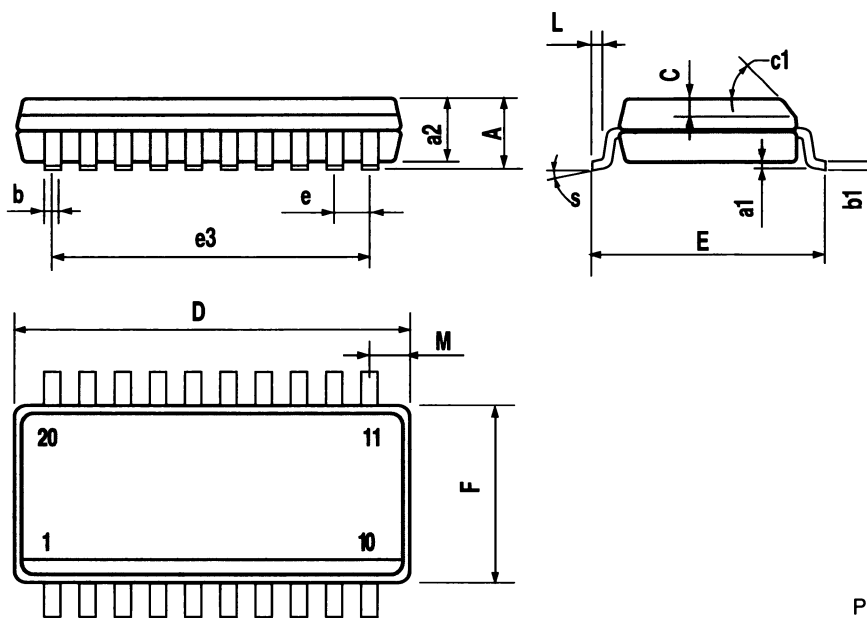
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	12.6		13.0	0.496		0.510
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.300
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO20

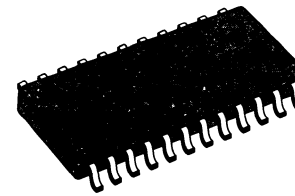


P013L

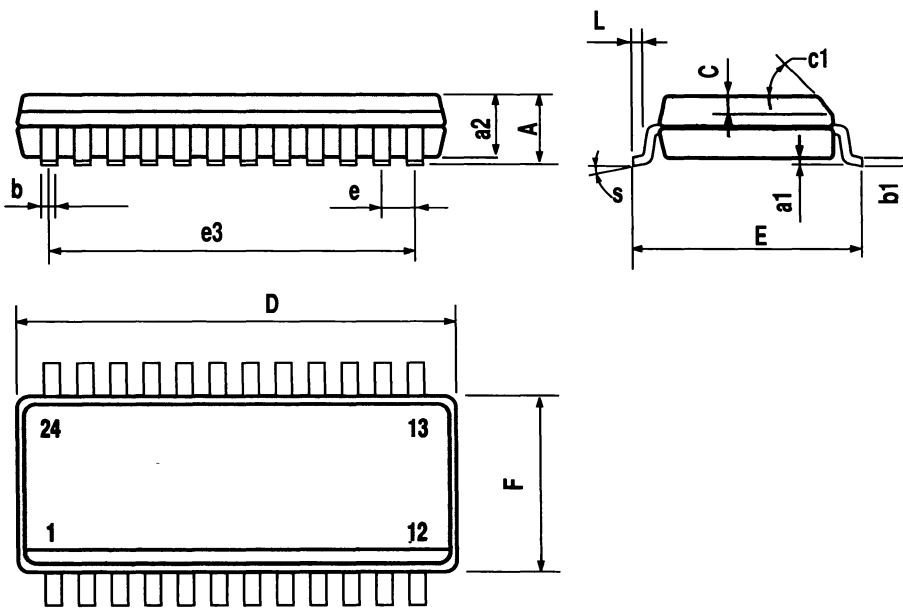
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	15.2		15.6	0.598		0.614
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		13.97			0.550	
F	7.4		7.6	0.291		0.300
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO24



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183 Queen's Road East
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NEW DELHI 110001
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62, Upper Ground Floor
World Trade Centre
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MALAYSIA

PULAU PINANG 10400
4th Floor - Suite 4-03
Bangunan FOP-123D Jalan Anson
Tel (04) 379735
Telefax (04) 379816

KOREA

SEOUL 121
8th floor Shinwon Building
823-14, Yuksam-Dong
Kang-Nam-Gu
Tel (82-2) 553-0399
Telex SGSKOR K29998
Telefax (82-2) 552-1051

SINGAPORE

SINGAPORE 2056
28 Ang Mo Kio - Industrial Park 2
Tel (65) 4821411
Telex RS 55201 ESGIES
Telefax (65) 4820240

TAIWAN

TAIPEI
12th Floor
571, Tun Hua South Road
Tel (886-2) 755-4111
Telex 10310 ESGIE TW
Telefax (886-2) 755-4008

JAPAN

TOKYO 108
Nisseki - Takanawa Bld 4F
2-18-10 Takanawa
Minato-Ku
Tel (81-3) 3280-4121
Telefax (81-3) 3280-4131

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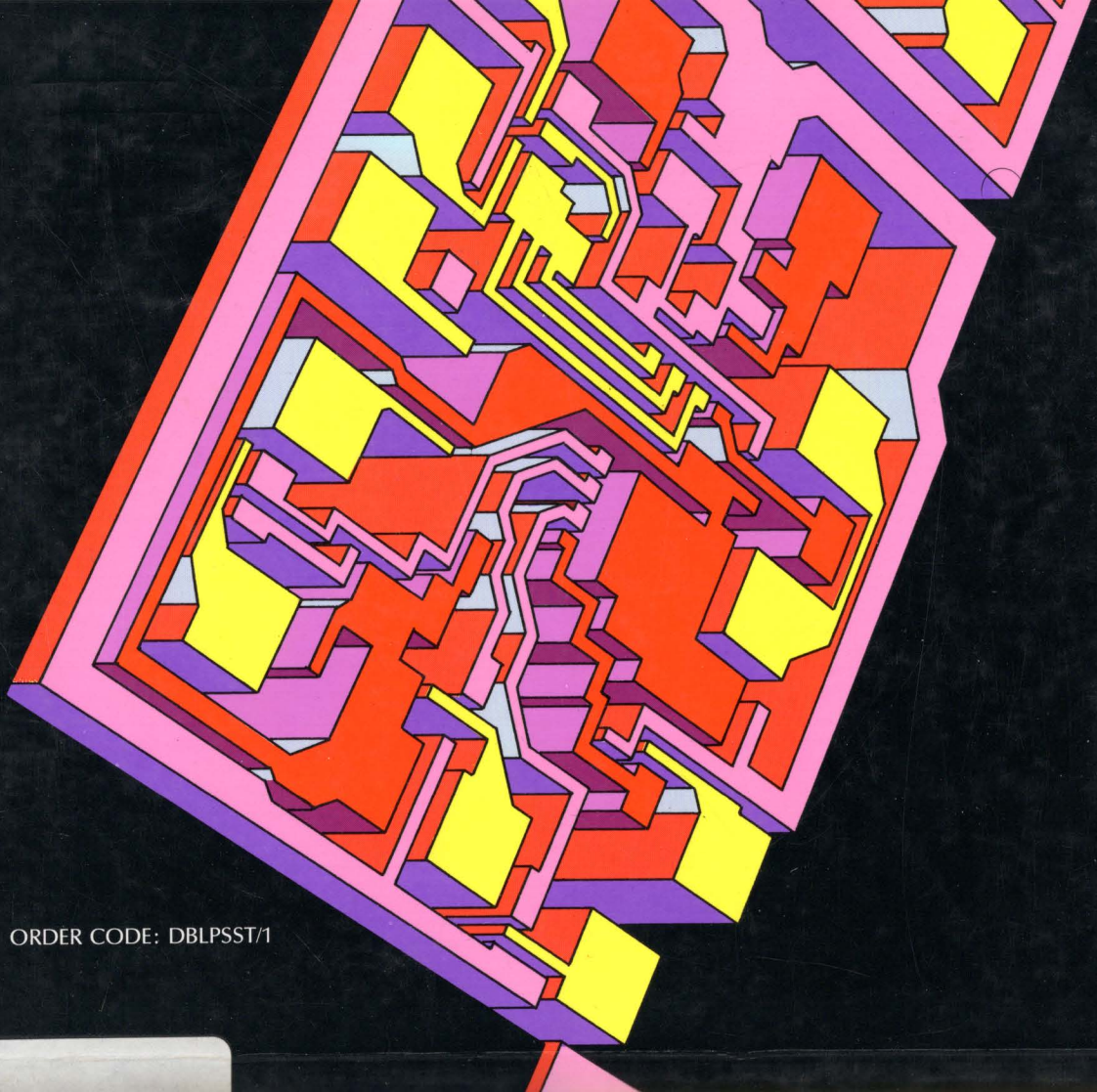

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