TELEPHONE LINE CARD

APPLICATION MANUAL

1st EDITION

SGS-THOMSON
MICROELECTRONICS

TELEPHONE LINE CARD

APPLICATION MANUAL

1st EDITION

JANUARY 1991

TABLE OF CONTENTS

SGS-THOMSON Microelectronics is a world leader in components for line card applications. Coupling vast system know-how, world class technologies and strong manufacturing experience, the company offers the most comprehensive range of solutions on the market-place.

Committed to offering solutions meeting all world standards, the company offers a complete family of single-chip codecs and filters, integrated first generation CMOS COMBO's, fully compatible with major manufacturers' families, and the programmable second generation COMBO® II.

Drawing on its world recognized bipolar capability SGS-THOMSON Microelectronics offers the most performant monolithic subscriber line interface circuits (SLIC) including the industry first internal ringing SLIC the L3000/L3XXX family.

Active in design at the system level the company offers a comprehensive family of switching matrix and special function devices, including our high performance conference call circuit, an industry first.

Active in a broad spectrum of application and technologies, the company employs state of the art processes including 3.0, 2.0 and 1.2 μm CMOS processes for mixed analog/digital functions and bipolar processes to 140V for high voltage applications such as SLICs. The company is also a world leader in BCD (Bipolar - CMOS - DMOS) technology providing the capability to mix low and high voltage applications on a single chip.

To simplify system design and application SGS-THOMSON Microelectronics offers comprehensive application support, including a full suite of application modules and software plus dedicated application support engineers and laboratories.
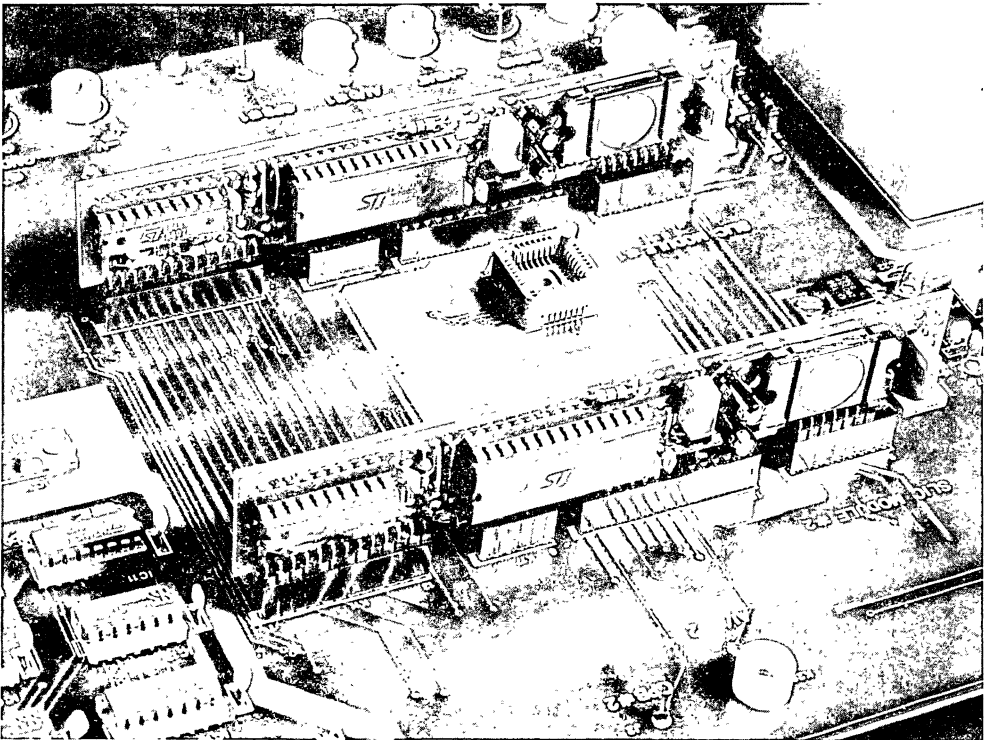
The SLIC-COMBO demo board allows design implementation and debug of line card using TS5070/1 COMBO II and SGS-THOMSON family of monolithic SLICs.

GENERAL INDEX

APPLICATION NOTES

M088 DIGITAL SWITCHING MATRIX

INTRODUCTION

The M088 DIGITAL SWITCHING MATRIX device can be used as a basic component in modern digital switching systems.

This Technical Note is a guide for designers who wish to use the M088 in their systems.

Section 1 contains introductory material in the field of digital switching and can be quickly passed over by experienced designers.

The main characteristics of the M088 are shown in Section 2.

Sections 3 and 4 describe, respectively, the internal structure, and the various functions which may be implemented.

Some detailed material concerning timing and some important services are examined in Section 5.

Section 6 is dedicated to applications. Another component, the M116, used in this field, are introduced in this section ; of particular note is the fact that the M116 is a digital device which realizes conference functions.
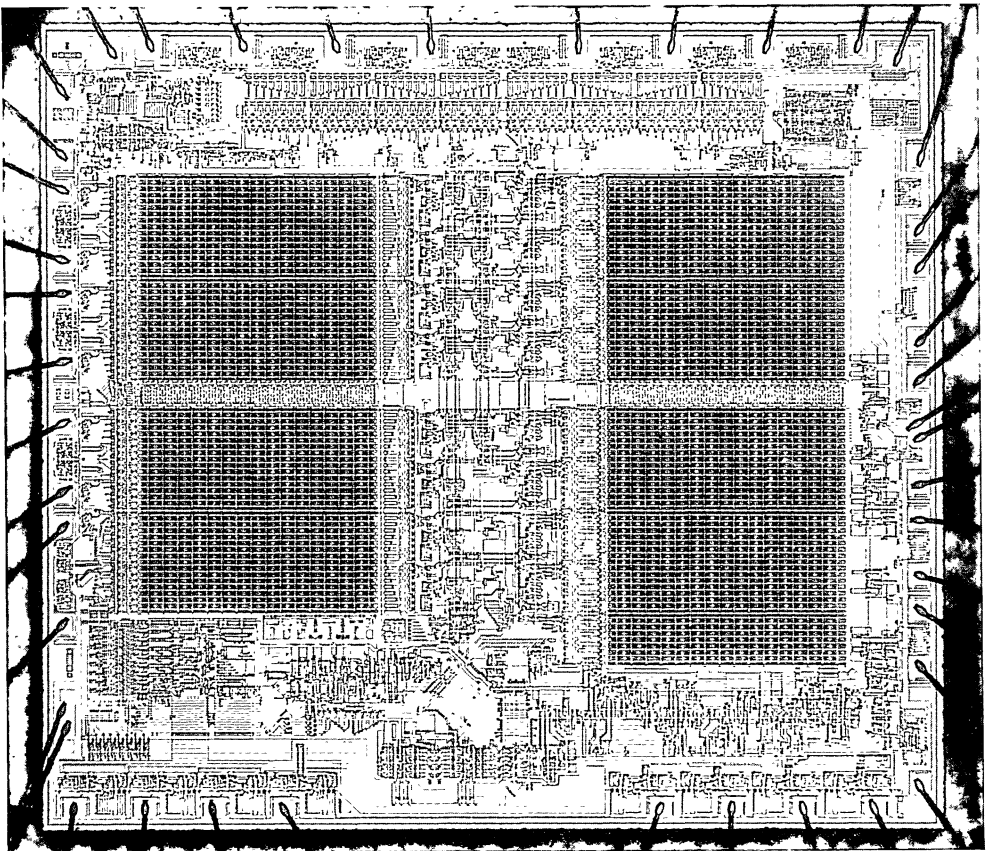
1. DIGITAL SWITCHING TUTORIAL

WHAT IS A DIGITAL SWITCHING MATRIX (DSM) ?

A Digital Switching Matrix is a device which permits switching a certain number of signals among themselves.

The signals to be switched can either be digital or analog ; in the latter case, digitalization of these signals must be provided before switching takes place.

Digitalization takes place in three stages :

a) band limiting (by a low pass filter) ;

b) sampling ;

c) digital coding.

PULSE CODE MODULATION (PCM)

The technique of digitalizing signals used in telephonic applications is called PCM.

The signal to be digitalized is sampled every 125 μs, in other words, with a frequency equal to 8 KHz since, according to the Nyquist law, the sampling frequency must be greater or equal to twice the maximum frequency of the analog signal being sampled. As is well known in telephony, this frequency is less than 4 KHz.

Based on input signal sampling (see fig. 1-1), the coding links a given sample to an 8-bit binary number.

Thus, the number of discrete levels becomes $2^8 = 256$.

Non-linear coding laws are used. The main ones are the two following :
- Mu law used in the USA, Canada and Japan ;
- A law used in Europe, South America, Australia and Africa (see fig. 1-2).

Since the sampling frequency is 8 KHz, the digitalized signal will be made up of a number of bits per second equal to $(8 \cdot 8000) = 64000$ bit/s.

TIME DIVISION MULTIPLEXER (TDM)

TDM is a technique which permits merging various digital signals into a single high velocity signal. Many stages of switching will, thus, become easier.

Fig. 1-3 presents a diagram of the TDM principle.

TDM is based on the serializer, which accepts PCM signals at the input, and provides them at the output, accessed cyclically.

Each input channel is linked to a time slot, and is thus fixed precisely in the serialized output stream.

Figure 1.1 : SAMPLING & CODING. The Analog Signal to be digitalized is First Bandwidth limited (fig. 1.1a) Then Sampled at a Frequency f_s (fig. 1.1b). The Resulting Periodic Sequence of Samples is shown in Fig. 1.1c. Each Sample is then replaced with an 8-Bit Word representing the Amplitude (fig. 1.1d).

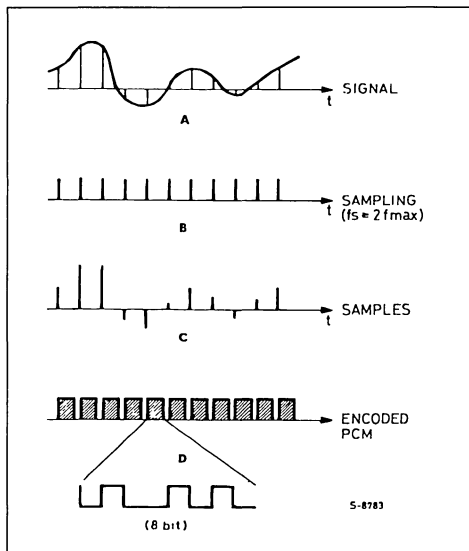**Figure 1.2 :** The Quantization Curve for A-law Limited to Positive Samples. Each Group of 16 Steps is Contained in a Segment and the Normalized Values of the Input Signal Corresponding to the Extremes of Each Segment are One Half of Each Other.
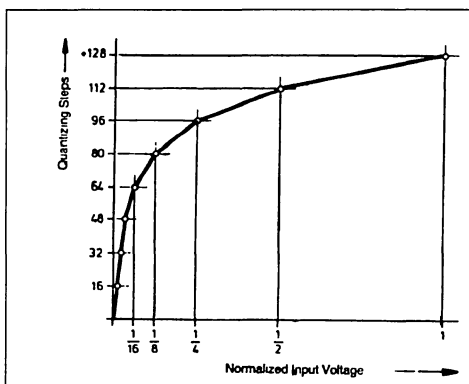
A very stable oscillator provides the master clock and all the timing functions used in the multiplexer.

The international standards for the TDM are two, namely :

a) the North American Standard (PCM 24 Transmission System) ;

b) the European Primary System (PCM 30 Transmission System) ;

Figure 1.3 : The Basic Principle of Time Division Multiplexing (TDM). Data from n Independent Channels are Compressed and Transferred to a Single Output. Each Channel Outputs Its Data in Separate Time Slots Defined by a Timing Circuit.
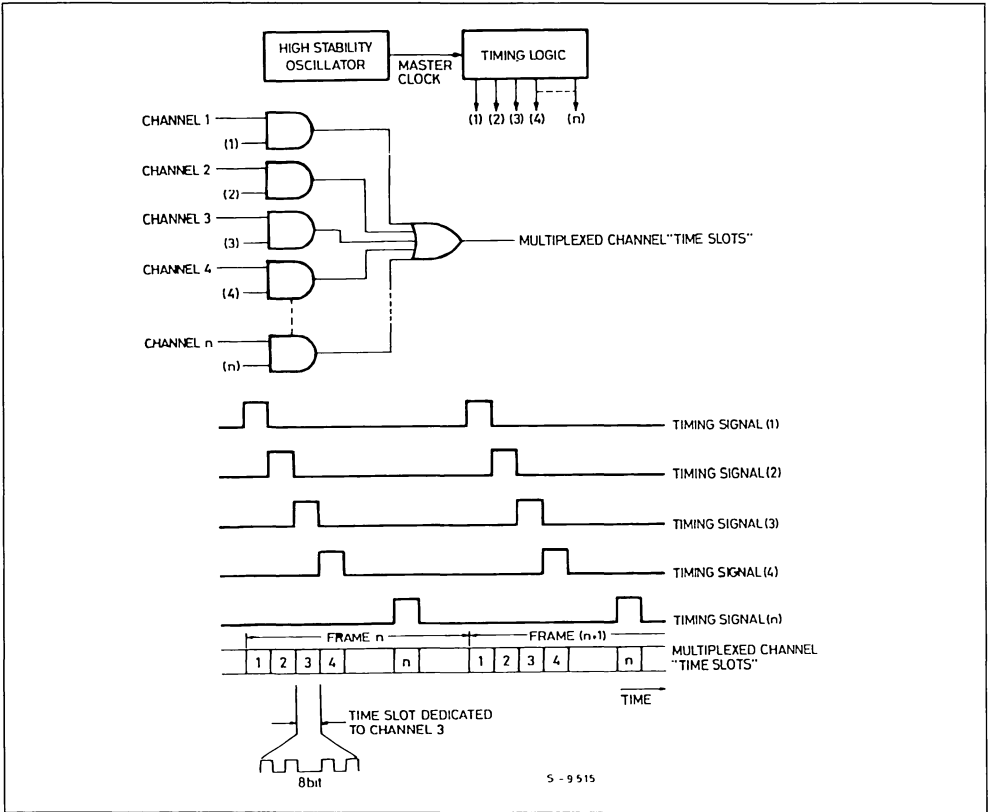
THE NORTH AMERICAN STANDARD (PCM 24)

Fig. 1-4 presents the PCM 24 Transmission System frame format.

Each of the 24 channels has already been sampled at 8 KHz and coded, using Mu law with 8-bit words.

Messages reaching the channels are word interleaved, forming an uninterrupted sequence of 192 bits.

A single alignment framing digit (bit X) is inserted at the beginning of each sequence ; thus the total number of digits in a frame is 193. The velocity of the signal in bit/s is thus (8000 · 193) = 1544 Kbit/s.

In certain applications, usually PABX, the Extra bit (bit X) is omitted. In this last case the velocity of the signal becomes (8000 · 192) = 1536 Kbit/s.

SGS-THOMSON
MICROELECTRONICS

Figure 1.4 : Frame Format of the Bell T1 (PCM24) System. Each Frame Contains 24 Channels PLus One Signalling Bit (bit X). This Format is Used in the USA, Canada and Japan.
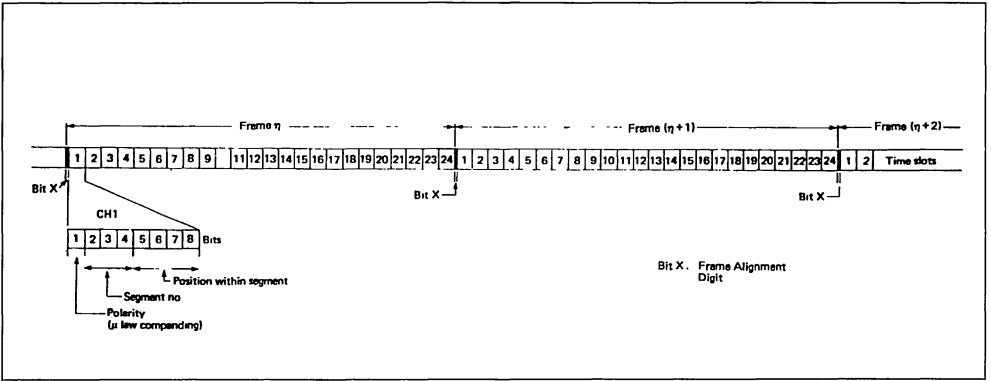
THE EUROPEAN PRIMARY SYSTEM (PCM 30)

Fig. 1-5 shows the European Primary System frame format.

TDM combines 30 voice channels, sampled at 8 KHz, and coded using A law with 8-bit words.

Various channels messages are combined by word interleaving ; thirty 8-bit words are inserted in a frame with 32 time slots, numbered from 0 to 31.

Two of the slots (0 and 16) are used for frame alignment and signalling.

Each frame has $(8 \cdot 32) = 256$ bits, and its velocity is $(8000 \cdot 256) = 2048$ Kbit/s.

Figure 1.5 : Frame Format of the European System (PCM30). Each Frame contains 32 Channels of which two are dedicated to signalling. This Format is used in Europe, Latin America, Australia and Africa.

4/24
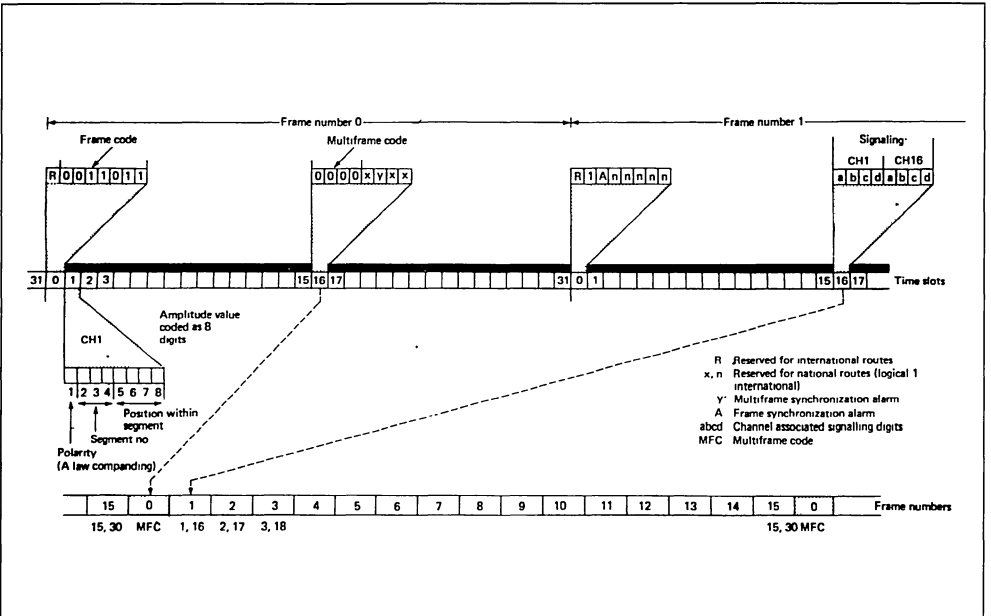
TIME AND SPACE DIVISION SWITCHING

Fig. 1-6 represents, using blocks, a digital switching system. Individual analog lines are applied to a multiplexer, which provides for their digitalization and merges them into a frame.

The various frames are transmitted to the switching matrix which carries out exactly the switching function, building various output frames as required.

These frames are transmitted to a demultiplexer which separates them into single channels, which, after conversion from digital to analog, are transmitted to the respective analog output lines.

Fig. 1-6 presents an example : subscriber S1-5 wishes to be connected to subscriber S8-11 ; S1-8

with S4-10.

The connection operation between S1-5 and S8-11 involves two operations :

1) transfer of information from layer F1 to layer F8 (space division switching) ;

2) transfer from position 5 to 11 (time division switching).

Likewise, the connection between S1-8 and S4-10 involves space switching between F1 and F4, and time switching between positions 8 and 10.

SGS THOMSON digital switching matrixes operate, using this technique of time and space division switching, permitting switching without blocking, in other words, simultaneously of 256 channels.

Figure 1.6 : Space-and-Time-switching Digitally encoded Signals.
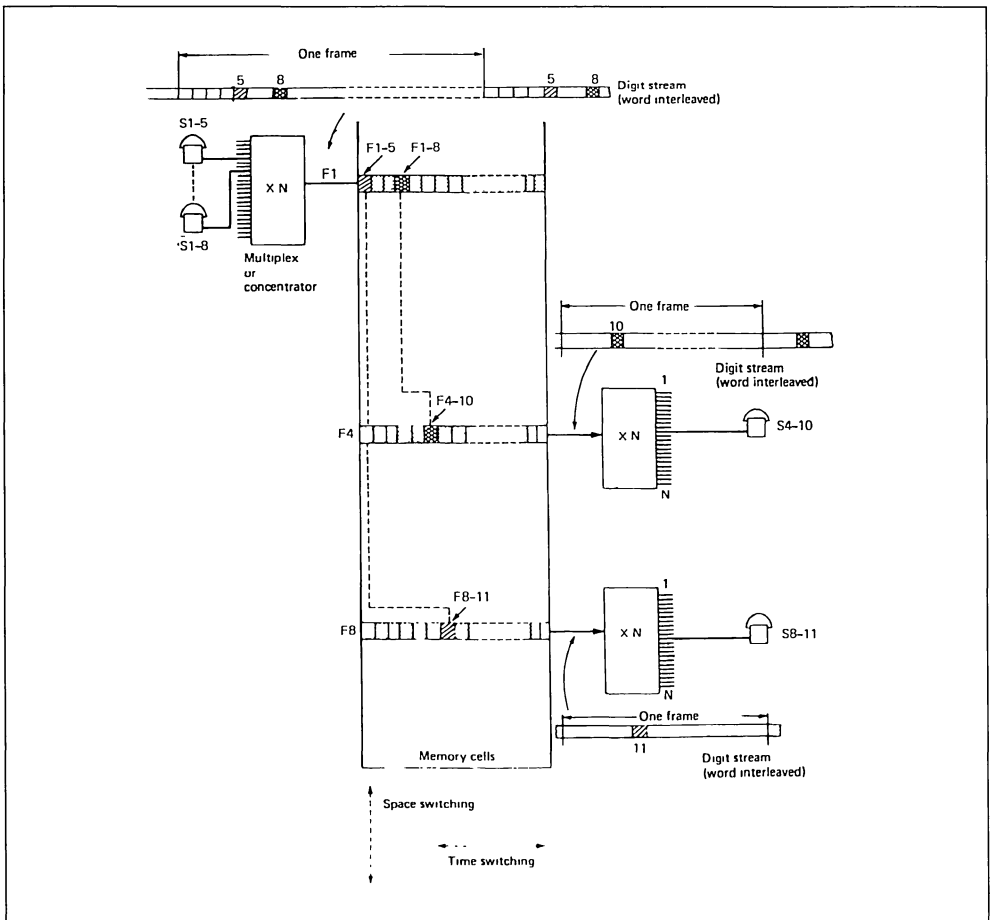
2. INTRODUCTION TO THE M088 DSM

GENERAL DESCRIPTION

The M088 device implements a non-blocking digital switching matrix, which operates with a maximum of 256 x 256 channels.

These channels are applied and extracted from the device, using 8 PCM frames at 2048 Kbit/s, each containing 32 channels.

The M088 can connect each input channel with, or disconnect it from, any output channel in addition to carrying out other functions described in Section 4.

It can also be used at lower velocity, for example, to switch 192 x 192 channels, organized in eight frames of 24 channels each, at 1544 Kbit/s, using the North American Standard (PCM 24) or at 1536 Kbit/s.

Finally, there is no prohibition against using the device for non-standard applications, for example, in the field of Data Communications. A few examples are cited in Section 6.

KEY FEATURES
- A 256 input and 256 output channels digital switching matrix ;
- A building block designed for large capacity electronic exchanges, subsystems, voice-data PABXs ;
- European Primary System compatible (32 channels per frame) ;
- North American Standard (T1 System) compatible (24 channels par frame) (*) ;
- PCM input and output mutually compatible ;
- Actual input-output channel connections stored and modified using an on-chip 8-bit parallel microprocessor interface.
- 6 main functions or instructions available ;
- 5-volt power supply with internal-generated bias voltage ;
- MOS and TTL input/output levels compatible ;
- Constructed with SGS THOMSON N-Channel silicon gate high-density MOS

(*) For further information, see below, Section 6.

3. M088 INTERNAL STRUCTURE

The component includes a Speech Memory, Control Memory, circuits for Serial to Parallel Conversion of incoming PCM links and for Parallel to Serial Conversion of the outgoing PCM links and a Bidirectional Interface for an 8-bit microprocessor (e. g., Z80 or Z8). In addition, the M088 performs other useful functions, such as Byte Insertion and Extraction, Addressing Memory Reading and 0 Channel

Extraction. Referring to Fig. 3-1, the following functional blocks can be distinguished :
- Time Base
- Serial Parallel Converter for the PCM input links
- Speech Memory
- Control Memory
- Internal PCM Bus
- Parallel Serial Converter for the PCM output links
- Control and Interface Logic to and from the μP

TIME BASE

The time base generates the internal synchronous timing signals, using only two external signals, the clock (4.096 MHz) and the frame synchronism (8 KHz), supplied to the corresponding external pins of the device (CK and SYNC pins). The time base provides two ring counters, generating two sets of timing signals (e1 to e8 and u1 to u8), used for Serial to Parallel Conversion of input time slots and Parallel to Serial reconversion of output PCM time slots, respectively.

The time base consists mainly of a fast synchronous parallel resettable counter of which stages are obtained by repeated clock division and grouped into three subsets : the first, CT1, starting from the 250ns rate, generates the time phases controlling the 4μs input and output time slot servicing ; in particular, the signal Q3 (4μs) specifies two working phases : one dedicated to the microprocessor interface operations, the other related to PCM operations. The other two subsets, CT2 and CT3, operating synchronously with respect to CT1, generate the sequential channel addresses for control memory reading and for speech memory reading, respectively.

The counter CT2 addresses the control memory, using the output PCM channel address increased by one ; the counter CT3 addresses the speech memory, using the input PCM channel address decreased by one. This address difference is necessary to compensate for the internal component delay due to input and output PCM conversion.

INPUT SERIAL TO PARALLEL PCM CONVERTER

During each time slot (4μs), the 8 serial PCM (2048 Kbit/s) input bits are regenerated and sampled using a 500 ns clock signal, $\overline{Q0}$, and then are stored in 8-bit latches clocked by the input ring counter's e1 to e8 signals. As soon as the 64 bits are updated, they are written, using a single write pulse, into the speech memory at the corresponding input channel address, selected by subset counter CT3, performing the parallel conversion in the same writing operation.

Figure 3.1 : The Fundamental Blocks are the Speech Memory (SM), which memorizes for Each Frame the Contents of All 256 Channels, and the Control Memory (CM) which contains Information on the Status of the 256 Output Channels (connected or not connected, loaded by the micro with a given byte).
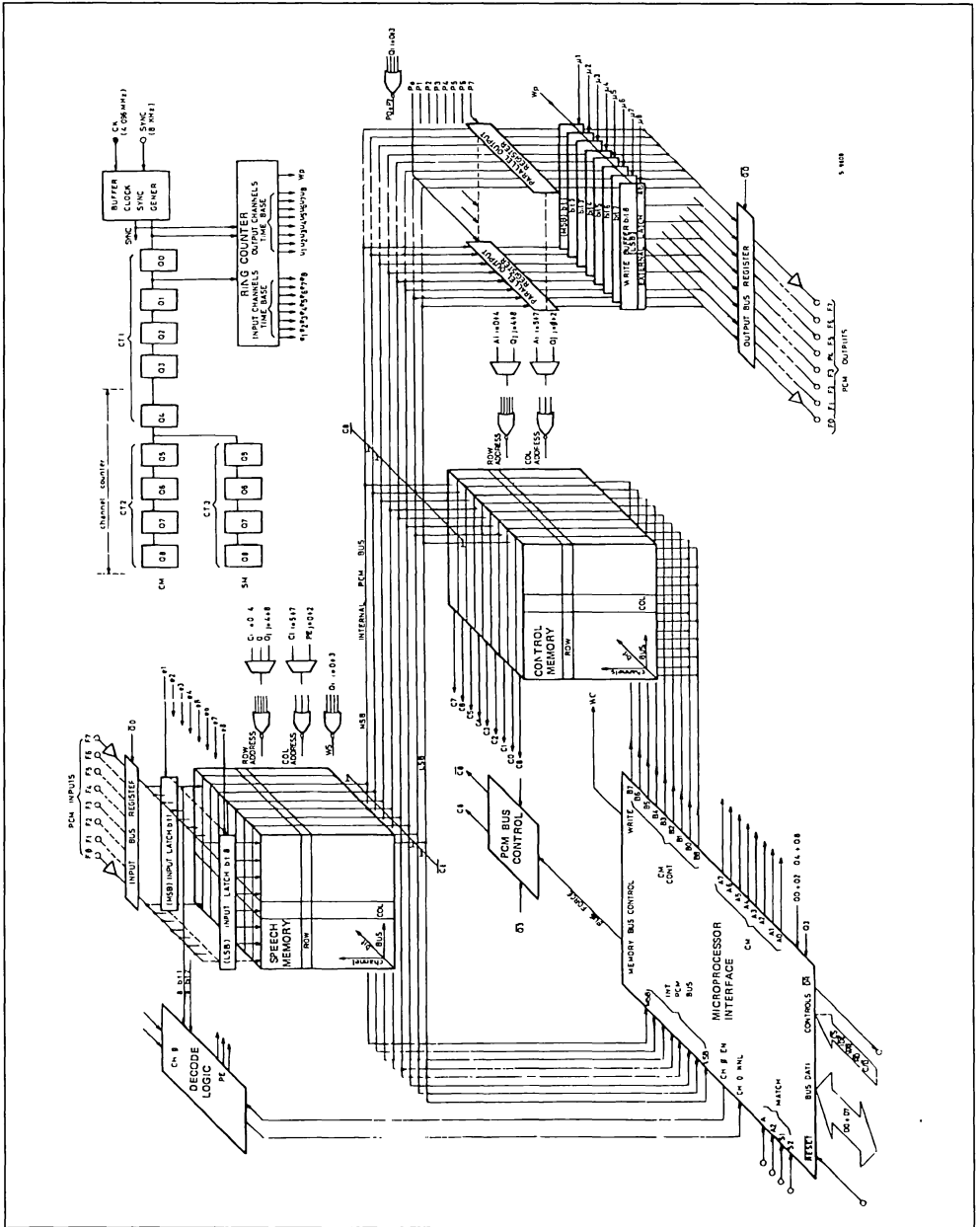
SPEECH MEMORY

The memory is organized as 32 planes of 8 rows and 8 columns each ; every plane corresponds to an input PCM channel, every row to a bit of content and every column to an input PCM line. The working cycle is about 4µs, with this time divided into 2µs phases. The first one consists of eight 250 ns cycles : one particular cycle is devoted to memory updating according to input channel data ; in the other cycles, functions engaged by the µP interface logic can be performed at random in the memory (that is the case of PCM output channel reading). In the second, memory is cyclically read 8 times, using the control memory addresses, C0 to C7 (switching function).

CONTROL MEMORY

Control Memory is organized in 32 planes of 9 rows and 8 columns each ; every plane corresponds to any output PCM channel, every row to a content bit and every column to an output PCM line. The Control Memory working cycle is similar to the Speech Memory.

During the first 2µs phase, the Control Memory is idle and normally accessible to µP interface. On occasion, because of network connection updating or µP requests, some cycles are stolen here for this purpose. During the latter 2µs phase, the memory is read eight times, using the addresses coming from the time base (subsets CT1 and CT2). The output contents of 9 bits each are used as addresses for Speech Memory (C0 to C7) and as a control signal for switching the internal PCM bus to the proper Control or Speech Memory output data (C8).

INTERNAL PCM BUS

Speech and Control Memories are connected to the internal 8-bit parallel bus. The 9th Control Memory bit controls each memory's output during the switch function ; otherwise, it is forced by the µP interface.

The internal bus is connected on one side to the µP interface to perform functions like memory content transfer. On the other side, the bus connects the PCM Parallel to Serial conversion unit.

OUTPUT PARALLEL TO SERIAL CONVERTER

The bytes of the internal PCM bus, belonging to the 8 cycles previously mentioned in Control Memory, are saved in a group of 8 temporary registers, each selected by the timing signals P0 to P7 (see fig. 3-1). When all bytes are stored, a single pulse transfer takes place in order to supply new PCM data to the output registers.

The proper time phases u1 and u8 sequentially scan the 8 output registers and simultaneously feed the output pins performing the Parallel to Serial conversion. The output PCM flows are resynchronized, using a 500ns clock signal (Q0). PCM outputs are open drain type.

MICROPROCESSOR INTERFACE LOGIC

The interface logic controls, asynchronously with respect to the PCM timing, the 8 bit data bus and the control bus to and from the microprocessor. It also stores, in a five byte stack, the data field and the opcode instruction. It gives the other internal blocks the necessary signals to perform the function in the right time phase. Moreover, it stores the status information, which can be read by the µP for diagnostic purposes, in two internal registers, OR1 and OR2.

The external control bus allows the component to be used as a standard 8-bit peripheral device, compatible with most $\overline{Ps}$, such as the Z80 and Z8. It consists of $\overline{RD}$ and $\overline{WR}$ signals for reading and writing into the M088 respectively, and the C/D signals, which selects between data and operating the code of command bytes to the written into the M088. Signals $\overline{CS1}$ and $\overline{CS2}$ activate the component when other peripheral devices are connected to the same bus.

Signals A1, S1, A2 and S2 allow more M088s to be connected in a simple way to obtain non-blocking matrix structures. An M088 in a match condition

4. FUNCTIONAL DESCRIPTION

The device, controlled by the microprocessor, implements six different instructions. A specific function is executed after the microprocessor has transmitted, using the data bus, the data bytes and the command bytes.

Two or four data bytes carry the information necessary for the correct interpretation of the function. The command byte follows these with the operative coding information necessary for M088 to execute the function.

Brief descriptions of individual functions are given here. For further information, the M088 data sheet for the device should be consulted.

FUNCTION 1 : CHANNEL CONNECTION/DIS-CONNECTION

This function permits the formation of a new connection between a given input channel (C_{IN}) and a given output channel (C_{OUT}). See fig. 4-1.

The message coming from the microprocessor consist of four data bytes plus a command byte.

The first two data bytes carry, respectively, information about the PCM input line and the input channel ; the third and fourth bytes carry information about the PCM output line and the output channel.

The first two bytes are loaded in the control memory cell (CM), the address of which is specified in the last two bytes.

It cases of switching systems of more than 256 x 256 channels some examples are given in Section 6 use is made of additional M088 chips, interconnected as required (multi-chip matrices).

In this case, the connection function is executed only by the M088 in match condition (A1 = S1 and A2 = S2) ; all the other M088s of the multi-chip matrix involved with channel C$_{OUT}$ will execute a disconnection operation from that selected output channel (C$_{OUT}$).

FUNCTION 2 : CHANNEL DISCONNECTION

Disconnect the selected output (C$_{OUT}$). See fig. 4-2.

The message coming from the microprocessor is made up of two data bytes plus a command byte.

The first and the second bytes carry, respectively, information about the PCM output line and the output channel which must be disabled.

FUNCTION 3 : BYTE INSERTION/CHANNEL DISCONNECTION

The function permits a byte furnished by the microprocessor to be inserted in an output data channel (C$_{OUT}$). See fig. 4-3.

The message is made up of four data bytes plus a command byte.

The first and second bytes contain information for transferral to the PCM output channel. This 8-bit information is memorized inside a control memory cell (CM).

The third and fourth data bytes contain, respectively, information on the PCM output lines and on the output channel in which the byte is to be inserted. These last bytes are used as an address to specify the CM cell in which to load the information contained in the first two data bytes.

As was the case for the first instruction examined, in the case of multi-chip matrices, this instruction is executed only by the selected M088 ; all the remaining M088s of the matrix will execute a disconnection operation on the selected output channel.

FUNCTION 4 : BYTE EXTRACTION

This function permits transferral of the byte contained in an output data channel to the microprocessor, using the data bus.

The message is made up of two data bytes plus a command byte.

The first and second bytes contain, respectively, the number of PCM output line and of the output channel, the contents of which are to be read by the microprocessor.

The PCM octet is memorized by the device in register OR1 ; thereafter, the microprocessor, using the aforementioned register's read cycle, transfers the PCM sample to the CPU.

If it is useful to read the PCM byte from an input data channel C$_{IN}$, C$_{IN}$ must be connected with a particular output channel C$_{OUT}$, and thus apply the extraction function to C$_{OUT}$. See fig. 4-4.

Figure 4.1 : Connection Any of the 256 Input Channels (C$_{IN}$) can be Permanently connected to any of the 256 Output Channels (C$_{OUT}$). It is Possible to have 256 Connections simultaneously.
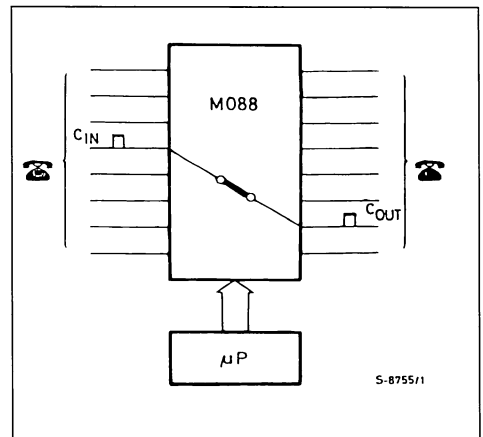
Figure 4.2 : Disconnection. Each Connection Pre-viously made can be interrupted at any Time.
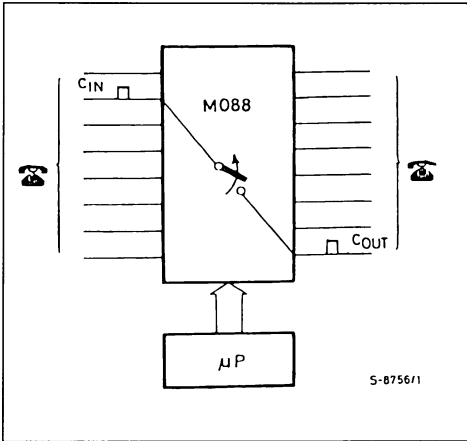
Figure 4.3 : Insertion of a Byte. The Control Micro-processor can send a given Byte to Any Output Channel.
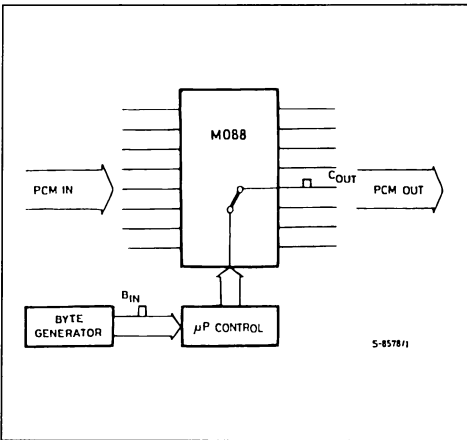
Figure 4.4 : Extraction of a Byte. The Micro Can Extract from Any Output Channel (C_{OUT}) the Contents (B_{OUT}) at the Time of the Request.
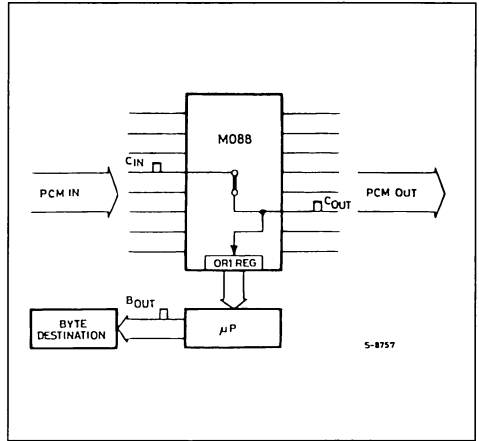
FUNCTION 5 : CONNECTION MAP READING

This function makes it possible to know, starting from a particular output channel C_{OUT}, the contents of the corresponding control memory cell CM, the address of which is exactly the same as C_{OUT}. See fig. 4-5.

As already explained in Section 3, each control memory cell CM is made up of nine bits (C8, C7.... C0).

If the ninth bit is equal to zero, the eight remaining bits (C7, C6.... C0) provide information concerning the input channel C_{IN} connected simultaneously with C_{OUT}. In particular, C7, C6 and C5 provide the PCM input line number, while C4, C3, C2, C1 and C0 provide the relevant C_{IN} channel number.

On the contrary, if bit C8 is equal to one, two possibilities can be examined :

a) byte C7, C6.... C0 is equal to 11111111 – in this case, output channel C_{OUT} is not connected to any input channel C_{IN}, and the microprocessor

SGS-THOMSON
MICROELECTRONICS

never loaded any byte on the basis of instruction 3 ;

b) byte C7, C6.... C0 is not equal to 11111111 – also, in this case, the C_{OUT} channel is not connected to any input channel C_{IN}, however, the aforementioned byte is a copy of the one which the microprocessor has already loaded in C_{OUT}.

The message coming from the microprocessor is made up of two data bytes plus a command byte.

The first and second bytes correspond, respectively, to the number of PCM output line and to the C_{OUT} channel, and, as already mentioned, correspond to the CM cell address whose contents the microprocessor must read.

Bits C7, C6.... C0 are memorized in the OR1 register, while bit C8 is memorized in the OR2 register.

With two read cycles, the microprocessor can thus transfer the contents of the two registers OR1 and OR2 into the CPU.

Figure 4.5 : Reading the Control Memory. Through This Operation the Microprocessor Can Read the Status of Every Output Channel.
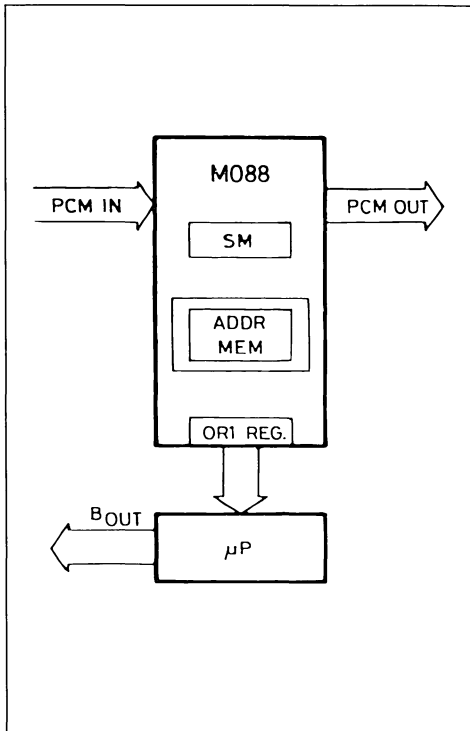
FUNCTION 6 : CHANNEL 0 CONNECTION MASK STORE/DATA TRANSFER

This last function is used to extract information rapidly from channel 0. See fig. 4-6. The indispensable requirement for the extraction to take place is that the two most significant bits of the byte contained in channel 0 not be equal to 01.

The PCM input lines from which the 0 channels are extracted are selected by using the microprocessor to load two data bytes, comprising the mask byte and a command byte.

The contents of channel 0 are available from the OR1 register, from which the microprocessor can transfer them externally by successive reads from the same register.

Experimental testing has shown that, with a CPU clock of 4.000 MHz in a time frame (125µs), it is possible to extract the 0 channels from all eight PCM lines.

Figure 4.6 : Rapid Extraction of Channel 0. Allows the Extraction of the Contents of the Active Channel Zeros and Channels with the Most Significant Bits Not Equal to 01.
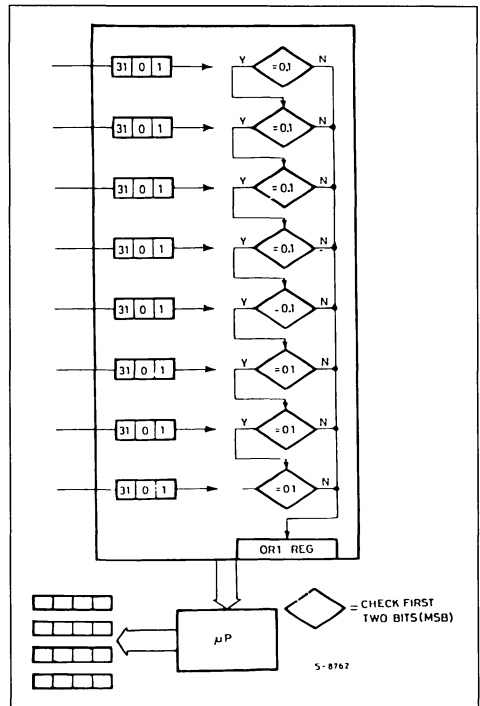
5. VARIOUS NOTES AND CONSIDERA-
TIONS ABOUT THE M088

In this section, certain aspects of the timing and operation of the device will be described in some detail.

In order to better understand the subject matter, it is recommended to have already read the component's data sheet.

SYNC TIMING

One of the aspects which should be handled with particular attention in the use of the component is the timing relation between the synchronization signal ($\overline{SYNC}$) and the clock signal (CK).

The $\overline{SYNC}$ signal, specifically its rising edge, specifies the beginning of the frame and, thus, bit 0 of channel 0.

The zone sketched in fig. 5-1 shows the areas of possible transition of the rising and falling edges of the $\overline{SYNC}$ signal with respect to the CK signal.

The absolute value of the width of this zone (t_V) is :

$$t_V\,(\overline{SY}) = t_{CK} - t_R - t_{HL}\,(\overline{SY}) - t_{SH}\,(\overline{SY})$$

in which :

$t_V\,(\overline{SY})$ ⸽ is the maximum time width of the area of the rising edge of SYNC ;

t_{CK} is the clock (CK) period ;

t_R is the maximum clock (CK) rise time

(= 25 ns) ;

$t_{HL}\,(\overline{SY})$ is the $\overline{SYNC}$ minimum low level hold time (= 40 ns) ;

$t_{SH}\,(\overline{SY})$ is the $\overline{SYNC}$ minimum high level set-up time (= 80 ns).

The falling edge of $\overline{SYNC}$ can take place anywhere if the length of level 1 is greater or equal to t_{CK} and the length of level 0 is greater than or equal to :

$$t_{SL}\,(SY) + t_R + t_{HL}\,(SY) = 145\ ns,$$

$t_{SL}\,(\overline{SY})$ being the $\overline{SYNC}$ min low level set-up time (80 ns).

PCM INPUT SIGNAL TIMING

Another very important point is the timing relationship between the PCM input signals and the SYNC signal.

In many cases, it is of major importance to know how much the eight PCM input signals can be mutually dephased with respect to the CK signal.

Fig. 5-2 presents an example of dephasing of the general PCM input signal with respect to CK. To better illustrate this aspect in the figure, the PCM input signal is represented both with the minimum, and with the maximum, permissible delay.

In the same figure, an extremely interesting aspect is evident, namely, that the various PCM input flows

Figure 5.1 : SYNC Signal Timing. The Shaded Zones are the Regions of Possible Transitions. The Rising Edge of SYNC Determines Bit 0 of Channel 0.

SGS-THOMSON
MICROELECTRONICS
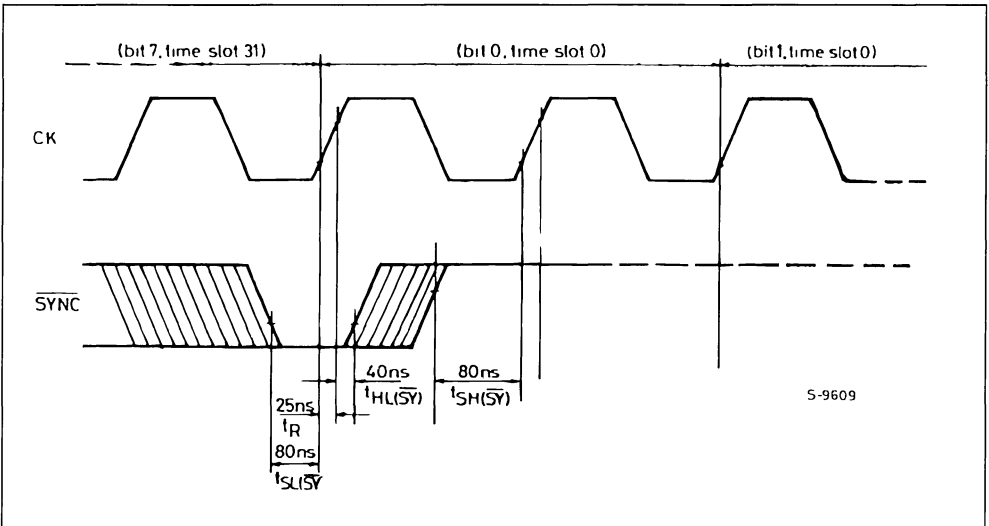
are able to mutually tolerate dephasing at a level of nearly one bit-time.

Indeed, the time variation between the PCM input signals with minimum and maximum permissible delays, t_V (PCM), is as follows :

t_V (PCM) = $(2 \cdot t_{CK}) - (t_H$ (PCM) + t_R (CK) $- t_S$ (PCM))

Therefore, referring to fig. 5-2 ;

t_V (PCM) = $(2 \cdot t_{CK})$ 65 ns.

In the case of the European PCM (2048 Kbit/s), t_V (PCM) = 423 ns, or 86 % of bit-time.

In the case of the North American PCM (1544 Kbit/s, t_V (PCM) = 582 ns, or 90 % of bit-time.

This fact suggests one of the component's possible alternative applications, namely that of the PCM flow rephaser for delays included in values which have already been mentioned.

Figure 5.2 : Timing of the PCM Input Signal (INP PCM). This Diagram Illustrates the Cases of (INP PCM) with the Minimum (b) and Maximum (c) Tolerated delay Referred to the Clock Period (a) Corresponding to Bit 0 of Channel 0. Note That the Regions of Possible Variation Correspond to Almost One PCM Bit Period.
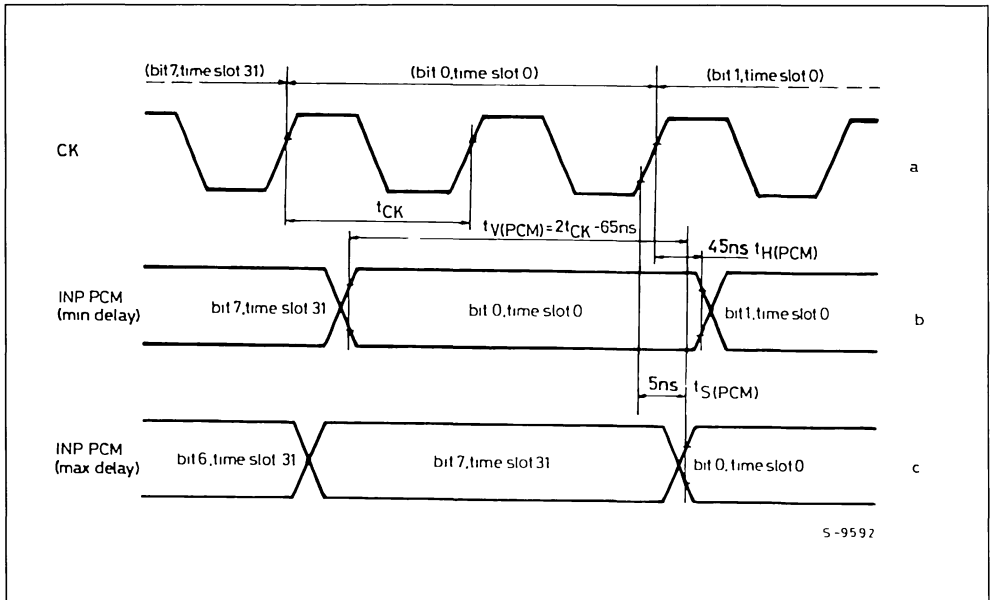
PCM OUTPUT SIGNAL TIMING

Fig. 5-3 shows the areas of variation of the edges of the PCM output signal with respect to the CK signal, the PCM input signal with maximum and minimum delay.

The width of such areas amounts to 155ns.

Also, the figure clearly indicates the possibility of using the PCM output flows as PCM input flows, in other words, to create a loop between the PCM outputs and inputs.

This could be used for test operations or for introducing frame delays into the PCM flow.

Figure 5.3 : Timing of the PCM Output Signal (OUT PCM). The Shaded Regions Indicate Where the Transitions May Take Place.
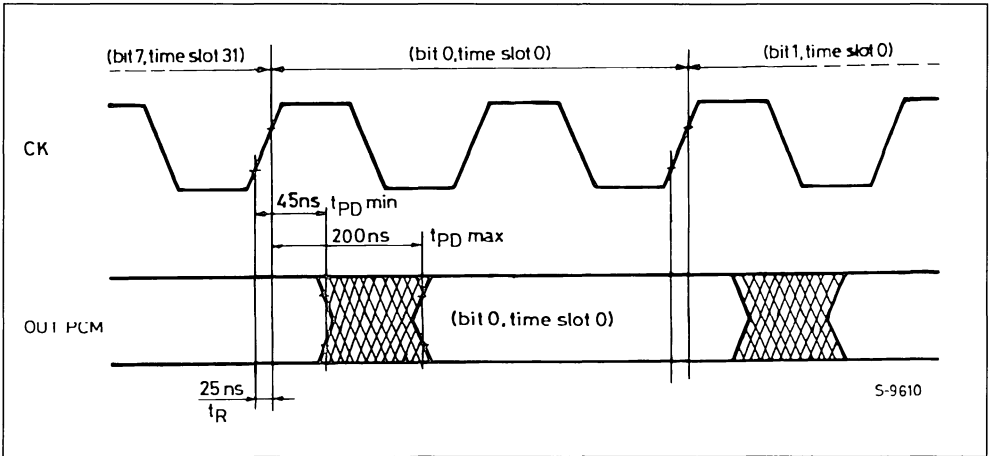
READ AND WRITE TIMING

The M088 device requires that the PCM signals be correlated with the CK signal.

In theory, the microprocessor interface signals could be completely asynchronous with the CK signal.

In reality, that is completely true only in cases where M088 is not inserted in a multi-chip matrix. In this last case, it is indeed to be recommended to link the RD and WR signals to the CK signal.

In particular, their rising edges must be delayed with respect to the falling edge of CK in a single phase, t_V (RW), in the range between 20ns and (20ns + t_{WL} (CK) = 120ns.

Fig. 5-4 presents an example of areas of transition among the rising edges of the aforementioned signals with respect to CK.

Given certain special conditions which are very difficult to deal with, problems could occur if the recommended synchronization for a multi-chip switching matrix is not respected. The connection of the relevant M088 will be carried out before the disconnection of the output channels of all the remaining M088s of the matrix.

This could cause an error in the correlation of the first bit in the first byte of the signal transferred.

Figure 5.4 : The Shaded Area Shows the Recommended Variation in the Rising Edge of the READ and WRITE Signals in the Case of Multi-chip Matrices.

SGS-THOMSON
MICROELECTRONICS
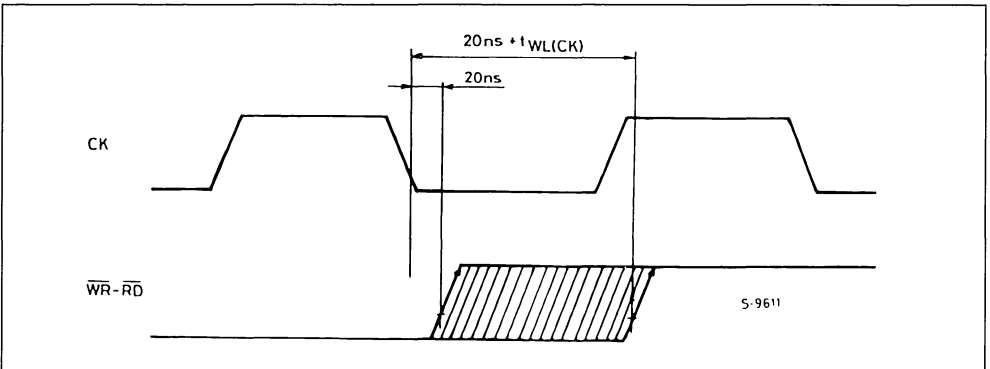
Anyhow, this only concerns the first byte transferred ; there will be no problem with those following. Another interesting parameter concerning the $\overline{RD}$ and $\overline{WR}$ signals is the minimum timing interval to maintain between two consecutive cycles, in other words, between the two rising edges.

The timing, t_{REP}, is a CK period function, namely :

$$t_{REP} = 40 \text{ ns} + 2 \ t_{CK} + t_{WL} \ (CK) + t_R \ (CK).$$

When $t_{CK} = 244$ns, $t_{REP} = 653$ns.

The reading operations of the OR1 and OR2 registers during instruction 6 are the only exceptions.

In this case, a request is indeed made for the minimum time between $\overline{RD}$ rising edges to be 3 CK periods for sequences from OR1 to OR2, and 13, for sequences from OR2 to OR1.

INSTRUCTION EXECUTION TIMING

Within a time slot (3.92µs for PCM input flows of 2048 Kbit/s), there are 16 CK periods. Each period corresponds to a machine cycle.

Of the 16 cycles contained in a time slot, 8 are free and are used to carry out instructions received from the microprocessor. Fig. 5-5 shows the internal distribution in a time slot with these cycles.

Figure 5.5 : The Division within Each Time Slot Between the Time Reserved for Internal Processing and That Reserved for the Execution of Commands Supplied by the Microprocessor.
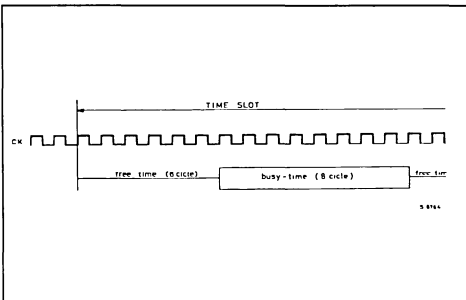
Physical time for internal execution of an instruction amounts to 5 cycles, excluding loading time for data bytes and commands coming from the microprocessor.

This time can be increased by 8 cycles if the instruction execution is not complete before the beginning of the block of 8 cycles reserved for internal operations.

Moreover, if instruction 6 is activated, all other instructions will be processed after instruction 6 has been completed or, at the latest, at the beginning of the new frame.

By activating instruction 1 (Connection/Disconnection) between a given input channel C_{IN} and an output channel C_{OUT}, the byte transferred to C_{OUT} corresponds to the byte taken from C_{IN} in the same or the preceding frame, based on the relative position of C_{OUT} with respect to C_{IN}.

In particular, if the number of C_{OUT} channels (NC_{OUT}) is greater than or equal to two units as compared with the number of C_{IN} channels (NC_{IN}), the connection occurs in the same frame.

6. APPLICATIONS

EXCHANGE NETWORK

The M088 device was designed to be used as a basic element in large-scale switching systems, with up to 65536 connections.

An example of a structure which could be used for this purpose is shown in fig. 6-1, which shows that a system of 64 K users (2048 PCM links, each having 32 channels) is made up of eight central modules, each with a capacity equal to 8 K connections (256 PCM links, each having 32 channels) and of (256 + 256) M088 peripherals.

Fig. 6-2 shows the internal organization of a central module with 8 K connections.

It should be noted that it is made up of eight switching units, each with a capacity equal to 1 K connections (32 PCM links, each having 32 channels) and of (32 + 32) M088 peripherals.

Figure 6.1 : Simplified Block Diagram of a Switching Matrix with 65536 Channels Concentrated in 2048 PCM Links at 2048 Kbit/s Each.
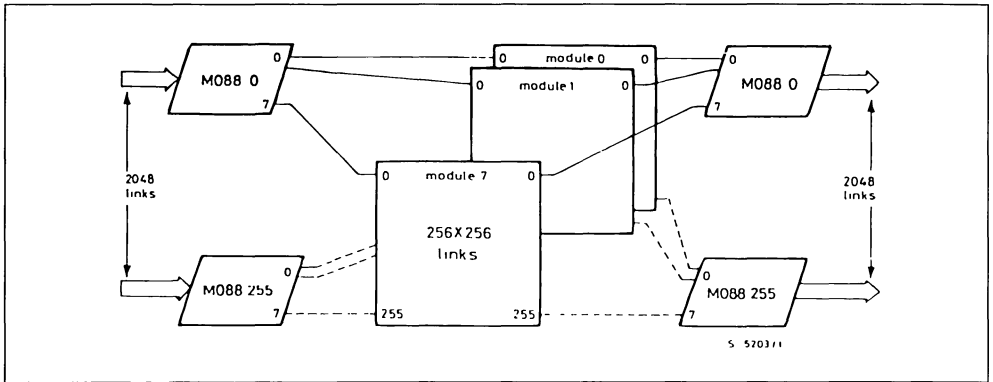
Figure 6.2 : Simplified Block Diagram of a Switching Module Four 8192 Channels Concentrated Into 256 PCM Links at 2048 Kbits/s.
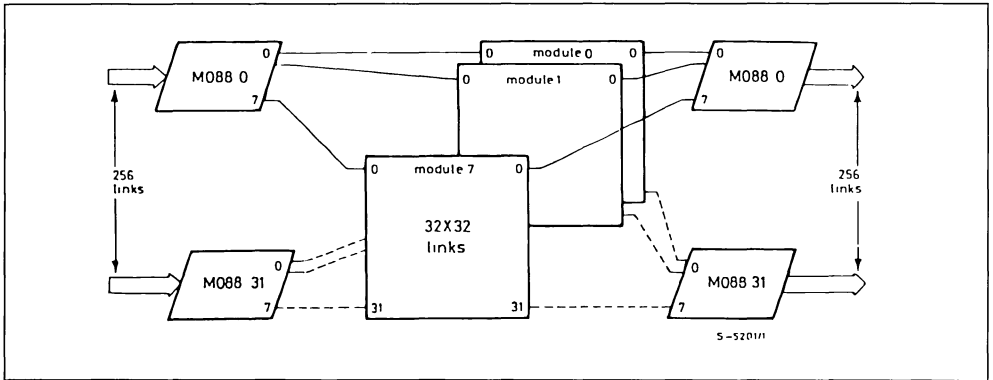
The internal structure of a switching unit with 1K connections is shown in fig. 6.3.

It is made up of 16 M088s organized in a square matrix (multi–chip matrix).

It is important to stop, finally, with this last structure, insofar as it could, without any variation, be used as a PABX switching matrix, up to 1000 lines.

The 1000 lines, or, more precisely, 1024, are concentrated in 32 PCM flows at 2048 Kbit/s.

All 16 M088s have microprocessor interface signals in common (D7 to D0, RD, WR, C/D, RESET), as well as CK, SYNC and selection pins A1, A2 and CS2.

Also, all 4 M088s belonging to the same column have the same output channels in common and all

4 M088s belonging to the same row have the same input channels. When the microprocessor needs to execute an operation on a certain output channel C_{OUT}, the relevant M088 column is chosen from among the chip select signals CS10, CS11, CS12 and CS13.

Thus, the microprocessor transmits the relevant bytes which, obviously, are received by all the M088s of the matrix.

However, only one of these M088s should execute the instruction.

The single M088 which should execute the function request is the one in which pins S1 and S2 have been connected to V_{CC} and V_{SS} in such a way as to correspond to the signals present, respectively, on the common wires A1 and A2.

SGS-THOMSON
MICROELECTRONICS

Figure 6.3 : Switching Matrix for 1024 Channels Concentrated Into 32 Links at 2048 Kbits/s.
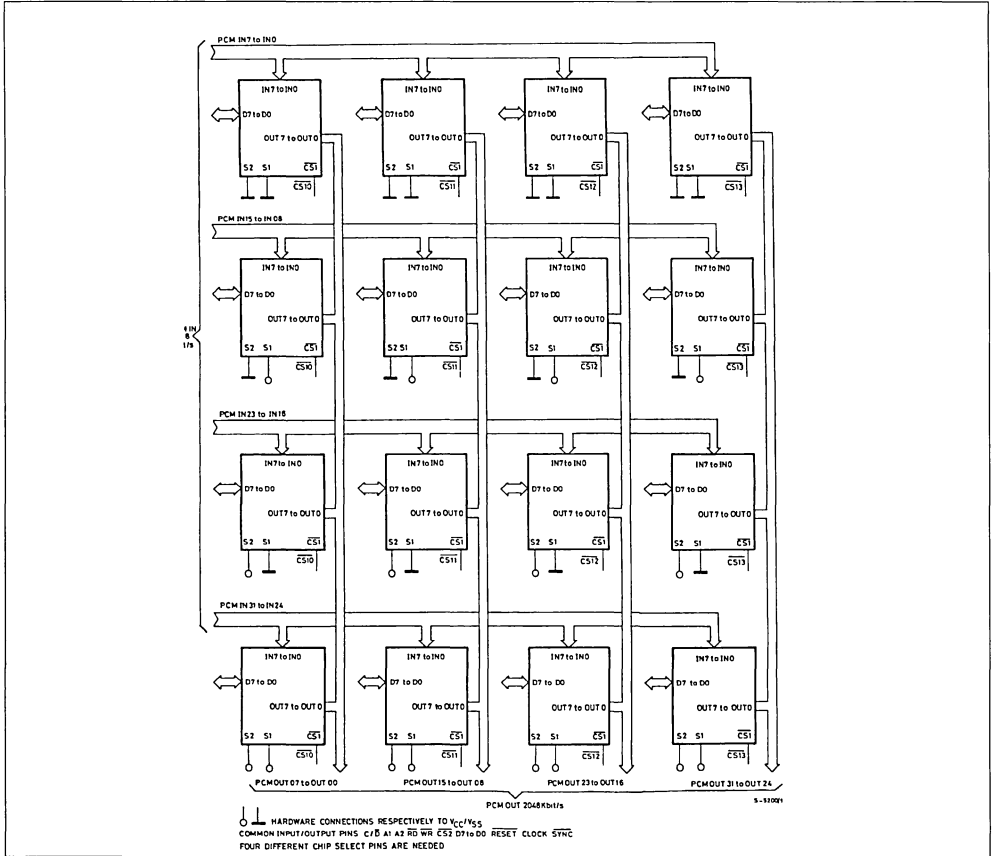
The other M088s in the column selected recognize that, even though having to do with an operation of a channel under their control, this operation must be carried out by another M088 in their column and they act on this basis.

In the case of instructions 1 and 3, they carry out a disconnection from the relevant output channel C_{OUT}, instruction 5 is unaffected and instructions 2, 4 and 6 are not executed.

*Bus reading only takes place on M088 in match condition (A1 = S1, A2 = S2).

This fact greatly simplifies the controlling software of the matrix insofar as, when a new connection needs to be executed or a byte loaded on a certain C_{OUT}, it is possible to ignore the same C_{OUT} disconnection from earlier connections because the disconnection is carried out automatically by the multichip matrix.

PABX

What was explained in the previous paragraph applies to switching systems up to 1024 lines.

The switching matrix for systems up to 512 users is represented in fig. 6-4.

Also, in this case, it is important to demonstrate the great simplification in the control software determined by the use of S1, S2, A1 and A2 for the choice of M088 involved in operations.

A single M088 will suffice for switching system up to 256 channels.

In the sphere of the PABX, regardless of its size, a function currently always in demand is the conference function, that is, the possibility to interconnect several users.

SGS-THOMSON
MICROELECTRONICS

Figure 6.4 : Switching Matrix for 512 Channels Concentrated Into 16 PCM Links at 2048 Kbits/s.
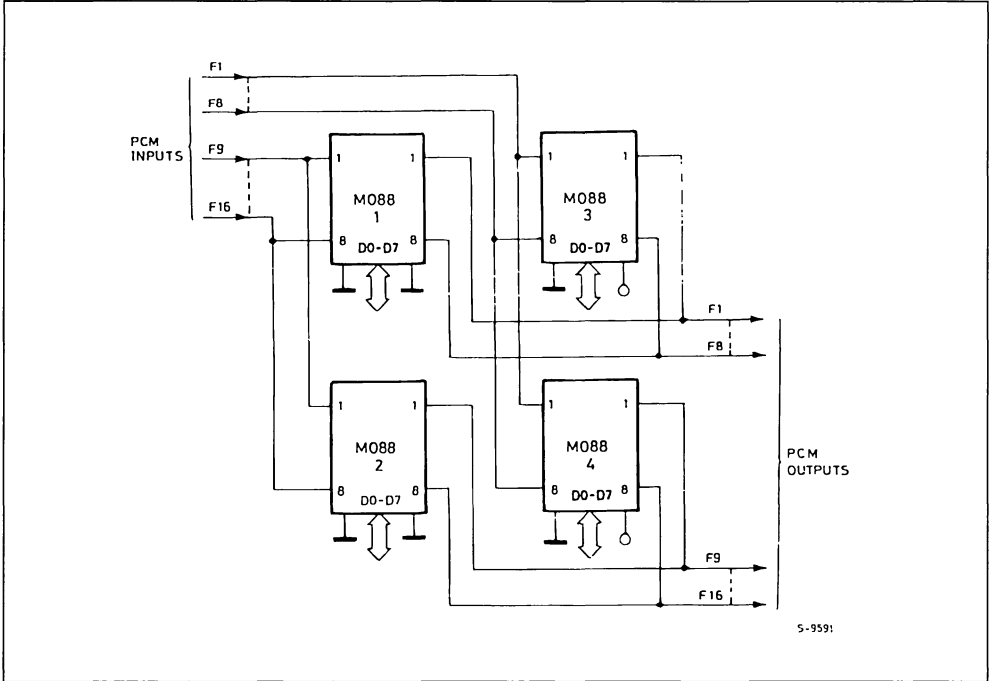
Figure 6.5 : Typical M088-M116-µP Configuration. One Output Stream of the M088 are Connected to the M116 and Dedicated to the Conference Function.
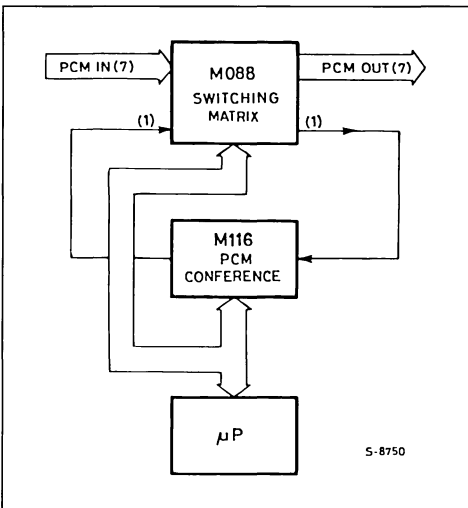
SGS-THOMSON has developped a device for this purpose, called CONFERENCE CALL (M116), which is used in conjunction with the M088 to carry out this function.

Fig. 6-5 demonstrates this application.

The M116 is also controlled by an 8-bit microprocessor, for example, the Z80 or the Z8, and, therefore, has been given a parallel interface for the microprocessor, using characteristics exactly the same as those available in the M088.

In order to carry out a conference operation, it is essential to reserve a PCM output and input in the matrix, for which, when using a single M088, switching capacity decreases to (224 x 224) users. With a single M116, it is possible to carry out from 1 to 10 conferences simultaneously, with the only limitation being that the total number of users involved in the conferences must be less than 32 ; fig. 6-6 illustrates this aspect.

With reference to fig. 6-7, in which the case of three users in conference is examinated, we can see which phases are required to bring about a conference :

1) the channels to use for the conference (A, B and C, in the example) are allocated in any channel

SGS-THOMSON
MICROELECTRONICS

position of the reserved PCM bus. The operation is carried out by the M088.

2) the supplementary channels are added together, in other words, the contents of channel B are replaced by the sum of channels (A and C) etc. This is carried out by the M116. These sum signals are loaded in the reserved PCM output bus.

3) the sum signal are withdrawn from the reserved PCM bus and switched into the relevant output channels. This operation is carried out by the M088.

Figure 6.6 : With a Single M116 It is Possible to Realize from 1 to 10 Independent Conferences with a Total of up to 32 Channels Conferenced.
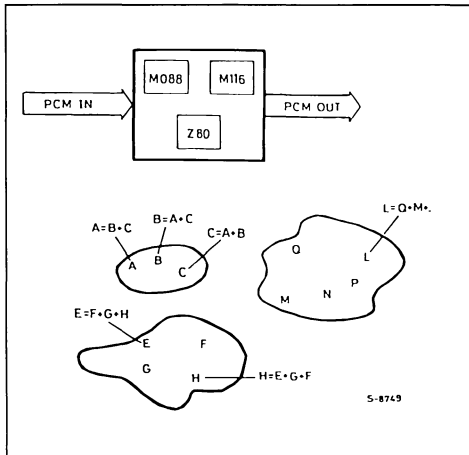
Figure 6.7 : Example of a conference with three channels ; A, B and C.

1) The M088 allocated A, B and C to the PCM stream applied to the M116.

2) The M116 processes the channels A, B and C, returning to the outputs B+C, A+C and A+B respectively.

3) The M088 allocates the signals B+C, A+C and A+B, to the outputs corresponding to the time slots of the channels A, B & C.
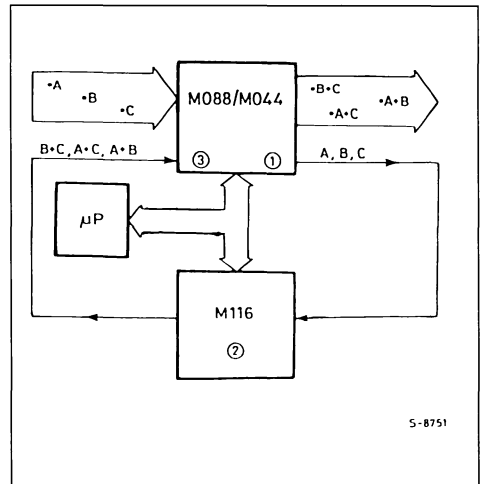
It is also possible to use the M116 in a multi-chip switching matrix - see fig. 6-8 - or use more than one M116 in the same matrix - see fig. 6-9.

Figure 6.8 : The M116 Can Also Been Used in Multichip Matrices.
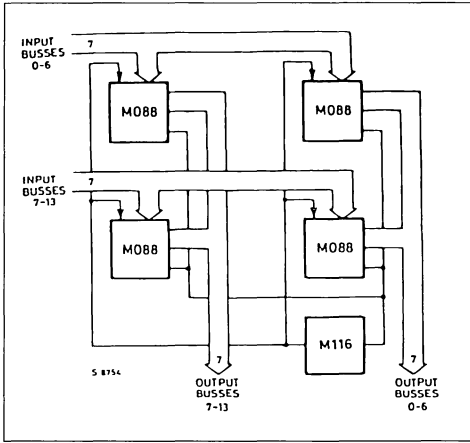
Figure 6.9 : More Than One M116 May be Added to Each Matrix to Increase the Number fo Conferences (10 per device).
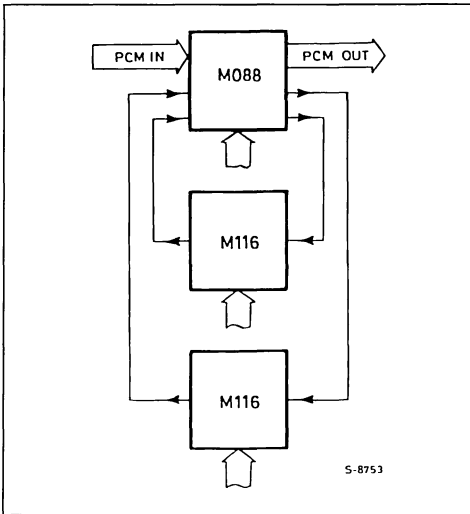
For more detailed information see the M116 datasheet.

Finally, it is interesting to note how the M116, on its own, can be used with other types of switching matrixes ; however, two considerations lead to recommending its use with the M088 ;

a) M116 PCM signal timing and microprocessor interface are exactly the same as those of the M088 ;

b) the command format that the microprocessor sends to the M116 to program the different operations is the same as the one used to program the M088.

To sum up, by using the M116 with the M088, complete compatibility is obtained, both with hardware and software, between switching matrices and the M116.

M088 WITH LESS PCM LINKS THAN 32 CHANNELS

It is also possible to use M088 when the PCM frames are made up of a number of channels other than 32.

Suppose that the PCM frames are made up of N-Channels, which will be numbered from 0 to (N-1).

Each PCM frame will thus be made up of a number of bits multiplied by 8 ; this exactly equal to (N · 8).

Also, in this case, it is necessary to respect the timing relationship between the different signals shown on the data sheet ; in particular, a relation-ship is always carefully made between the rising edge of SYNC and the first clock (CK) bit contained in the slot time for bit 0 of channel 0.

In order to use M088 with these frames, it is sufficient, using the data bytes sent by the microprocessor, to modify the numbering of a few channels.

In particular :

a) in all instructions in which reference is made to the input channel (N-1), the number 31 should be substituted for the number (N-1) ;

b) in all instructions in which reference is made to the output channel 0, the number N should be substituted for the number 0.

These variations can be made insofar as the M088 is internally programmed to execute the different operations using 32 channels.

In particular, during the time slot which corresponds to the last channel of the frame, channel (N-1), the M088 loads the bits corresponding to the next channel to be output in the next slot time into its registers.

We consider this last channel to be channel 0, but for the M088 it is Channel N ; indeed, the M088 draws the bits that it will successively output from the corresponding cells of Channel-N.

Likewise, during the general time slot X, M088 loads the PCM input frame bits corresponding to channel X ; simultaneously, it memorizes the bits loaded in the previous time slot into the Speech Memory (SM) memory location corresponding to channel (X-1).

SGS-THOMSON
MICROELECTRONICS

Therefore, during the time slot corresponding to channel 0, M088 memorizes the bits received in the previous time slot, which we consider to be channel (N-1), in the SM memory locations corresponding to channel 31.

For whoever wishes to connect the input channel (N-1) to any output channel, the same channel's PCM samples will be drawn from locations reserved for channel 31.

M088 WITH THE NORTH AMERICAN PCM STANDARD

The operation of the M088 with PCM frames using the North American standard can be considered a special case of the operating mode described in the previous paragraph.

The only variable in this case is the presence in each frame of an auxiliary bit (bit X), for which the total number of bits in a frame is :

(24 channels . 8 bits) + 1 bit = 193 bits/frame

As in the preceding case, in alteration in the numbering of the canals is introduced, in particular, the number 23 is replaced by the number 31 in every case in which reference is made to the last channel of the PCM input frame, and in every case where reference is made to output channel 0, the number 0 is replaced by the number 24.

Also, the signals for synchronization ($\overline{\text{SYNC}}$) and for clock (CK) are modified as shown in fig. 6-10.

In particular, the rising edge of the $\overline{\text{SYNC}}$ signal must appear in bit X's bit time (the 193rd of the PCM input frame). The single variation in the timing of this signal as far as the MCK and CK signals is concerned in that the minimum time for t_{WH} SYNC high

level width must be from 1 t_{CK} to 3 t_{CK} and thus with (3 . 324) ns = 972ns.

The clock (CK) signal to be applied to the M088 (pin 6) must be frozen for two clock periods during bit X's bit time. A scheme which is recommended for obtain CK beginning from the MCK and $\overline{\text{SYNC}}$ signals is shown in fig. 6-11.

The signal bits located in the PCM input frames are ignored, while, in the corresponding positions of the PCM output frames, they assume the same logical values of the 0 bits of channel 0.

If you use the M088 with an M116 the scheme recommended of fig. 6.11 is not necessary. In fact the "frozen clock" is provide by M116 itself (pin EC).

Therefore is enough to connect pin EC of M116 to pin CK of M088. Of course the $\overline{\text{SYNC}}$ signal must be the same as shown in Fig. 6.10 and must be connect both to M088 and M116.

DATA FLOW SWITCHING

A very simple, but very important, application of the M088 is that of using it to switch PCM or other high speed data links.

To enable this function, it suffices to switch all relevant input channels to their preselected output channels.

The data rate of these data flows can have any value less that the maximum permissible velocity (2048 Kbit/s).

Obviously, the CK frequency must be the double of the data rate chosen, while the $\overline{\text{SYNC}}$ frequency must be included between 1/16 and 1/256 of the same data rate.

Figure 6.10 : Timing of the CLOCK, $\overline{\text{SYNC}}$ and PCM IN Signals for 1544 Kbit/s PCM Streams. At the 193 rd Bit (bit X) the CLOCK Signal applied to the M088 is frozen for two Periods.
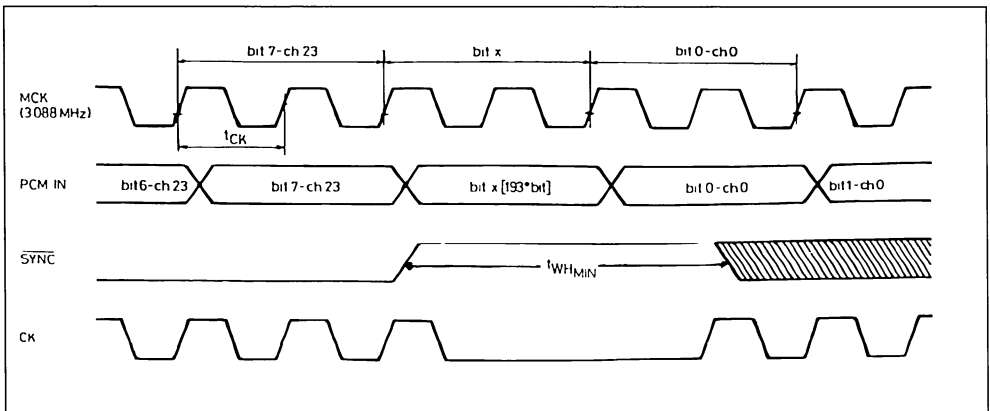
Figure 6.11 : Auxiliary Circuit to use the M088 with 1544 Kbits/s PCM Streams. This Circuit is not necessary if the M088 is used with an M116.
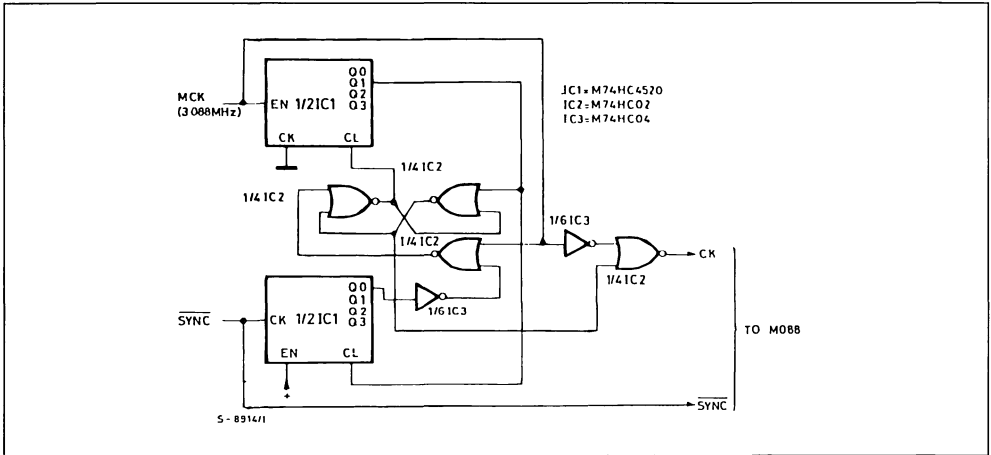
It is particularly interesting, in this application, to demonstrate a characteristic of the M088 which has already been mentioned and, therefore, of the fact that the device accepts that a certain delay can exist between one data flow and another.

The absolute value of the maximum acceptable delay is not constant, but depends on the velocity of the data flow ; in any case, it is always greater than 80 % of bit time.

This obviously means that when the data flows are not generated internally, but come from peripheral devices located at different distances - See fig. 6-12- within certain limits, it is not necessary to equalize the delays caused by variable arrival times.

RS232 C/V-24 DATA INTERFACE SWITCHING

One of the alternative fields for possible use of the M088 is that of DATA COMMUNICATIONS.

Fig. 6-13 presents the block diagram of one of the possible applications : a device which allows for switching between the V-24 interface of four DTEs and the V-24 of four DCEs.

As is well known, the RS232 C/V-24 is one of the most common connection interfaces between Data Terminal Equipment (DTE), i.e., computers and terminals, and Data Communication Equipment (DCE), i.e., modems, etc.

Figure 6.12 : Structure of a PABX with Peripheral Concentration Blocks. Note That the CE-PP Connections are PCM Links.

SGS-THOMSON
MICROELECTRONICS

Figure 6.13 : Switching Matrix for Parallel Data Interfaces (eg : RS232C/V24). Signals from the Parallel Interfaces are Serialized, Switched and Parallelized.

Fig 6-2 BLOCK DIAGRAM OF RS 232 C / V 24
DATA INTERFACE SWITCHING
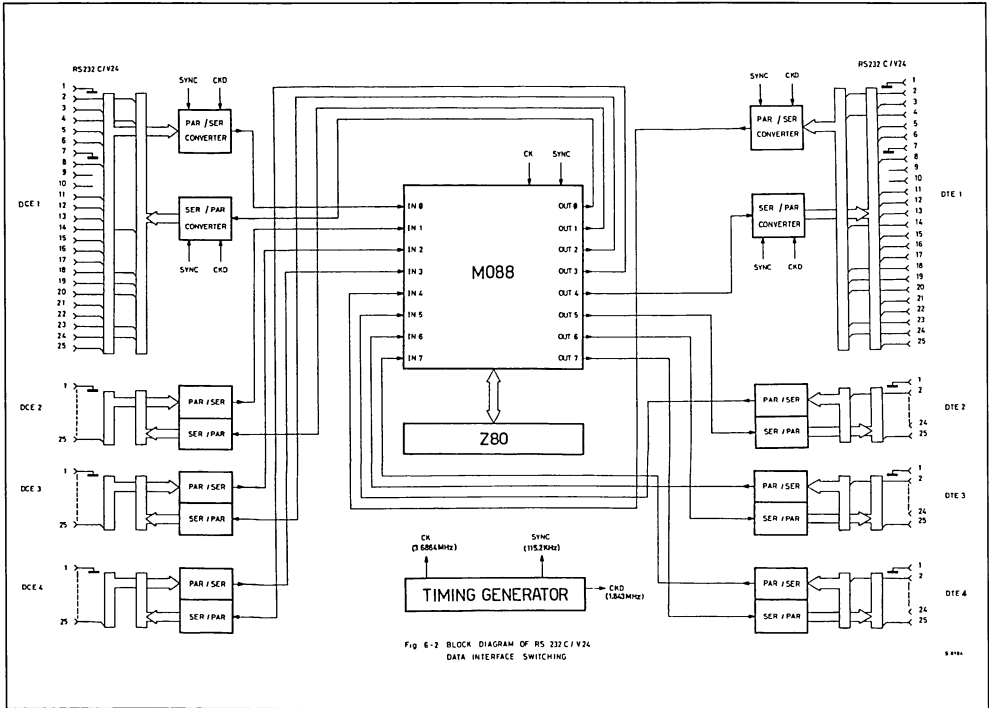
The table in fig. 6-14 presents the names of 25 distinct pins which determine the interface and the direction of the same signals (13 DCE → DTE and 8 DTE → DCE).

The basic idea of the device is to sample, using a frequency of 115.2 KHz, the 21 usable interface signals, serialized at a velocity of 1843.2 Kbit/s, and send or receive them through the switching matrix exactly as if they were PCM streams.

In the case of interfaces coming from DCE, of the 21 usable signals, 13 are signals inputting the device, and 8 outputting it, thus it is necessary to run a parallel/serial conversion on the first, and obviously, serial/parallel on the second.

For reasons of simplicity in the serialization phase for the 13 bits, three bits are added so that every sampling period (8.7 μs) will amount to exactly two octets ; in the parallel/serial conversion phase, the three additional bits are disregarded.

Concerning the DTE, the discussion is similar, with the obvious exception of the fact that the signals undergoing serial/parallel conversion are 13 and those which undergoing parallel/serial conversion are 8.

To these last 8 bits should be added, for the same reasons mentioned before, 8 bits so that, during each sampling period, exactly 16 bits are serialized.

An input and an output made available by the M088 are reserved for each interface.

The M088 views the data streams which are entering exactly if they were PCM frames at 1843 Kbit/s.

In this case, the difference is that the number of channels used is only two, thus each two octets require that the M088 internal channel counter be reset to zero.

This is obtained simply by raising the frequency of the SYNC signal from the usual 8 KHz to 115.2 Khz, in other words, to use as SYNC the same signal used to sample the interfaces (see fig. 6-13).

Wanting, for example, to switch the V-24 from DCE1 to that of DTE4 is sufficient through the microprocessor sending to the M088 instructions for connecting channels 0 and 1 of input 0 with channels 0 and 1 of output 7, channels 0 and 1 of input 7 with 0 and 1 of output 0.

Figure 6.14 : RS-232-C/V. 24 Data Interface Connector Pin Assignements.

Pin	Circuit		SIGNAL NAME	Direction
---	EIA	CCITT		DTE ———————— DCE
1	AA	101	Protective Ground	→
2	BA	103	Transmitted Data	→
3	BB	104	Received Data	←
4	CA	105	Request to Send	→
5	CB	106	Clear to Send	—
6	CC	107	Data Set Ready	←
7	AB	102	Signal Ground (Common Return)	←→
8	CF	109	Received Line Signal Detector	←
9			Unassigned	
10			Unassigned	
11		126	Select Tx Frequency	←
12	SCF	122	Secondary Received Line Signal Detector	←
13	SCB	121	Secondary Clear to Send	←
14	SBA	118	Secondary Transmitted Data	→
15	DB	114	Transmit Signal Element Timing (DCE Source)	←
16	SBB	119	Secondary Received Data	←
17	DD	115	Receiver Signal Element Timing (DCE Source)	←
18		141	Local Loopback	→
19	SCA	120	Secondary Request to Send	→
20	CD	108/2	Data Terminal Ready	→
21	CG	110	Signal Quality Detector	←
22	CE	125	Ring Indicator	←
23	CH	111	Data Signal Rate Selector (DTE Source)	→
24	DA	113	Transmit Signal Element Timing (DTE Source)	→
25		142	Test Indicator	←

Obviously, it is possible to carry out simultaneously all four connections in any combination.

Using M088 instead of standard analog cross-point besides switching, you can also implement addition functions as monitoring or programming by µP the status of the interfaces using the instruction 3 and 4 of the M088 itself.

Using more M088s extends at will the number of interfaces thus switchable due to their subdivision between DTE and DCE V-24s.

Finally, there are no limits to the use of this system for switching other interface types.

7. SUPPORT MATERIAL

To introduce users to the use of the M088 and M116, a demonstration board have been developed.

This board allows the user to study the behavoir of M088 and M116 without building any external hardware but using mnemonic and easy commands through a standard asynchronous terminal.

On the board there are also 4 SGS-THOMSON MICROELECTRONICS CMOS Combos M5914 that allow the test of the Conference function starting from analog signals.

There are two versions of the demoboard :
- Democonf
- Democonf-Plus

The second one is delivered in a specially-designed executive briefcase and consists of the board, four telephone handsets, a power supply and a user manual.

SGS-THOMSON MICROELECTRONICS

SGS-THOMSON
MICROELECTRONICS

HOW TO HANDLE SIGNALING WITH THE M088 DIGITAL SWITCHING MATRIX

INTRODUCTION

One of the main problems in the design of electronic systems, and in particular in the design of private electronic switches (PABX : Private Automatic Branch Exchange) is to make an architectural choice between a system that is expandable and flexible, and another one that is optimized in terms of hardware and software, but more rigid because it is dedicated to a specific application.

The architectural section that is more influenced by such an initial choice is that related to the "transfer and handling of signaling messages", in order words all circuits and procedures which allow the request of single users to communicate to the mainframe computer and, in a reverse process, to communicate to the single user the decisions taken by the computer.

The diagram in figure 1 shows a typical digital exchange. The users are either analog (traditional telephones) or digital ISDN terminals (Integrated Service Digital Network). The main difference between the signaling messages of analog users and those of digital users is that the first are generated and activated through the resident circuits on the exchange (user board) and have for end points the mainframe and the user board, while the second are generated in the user terminal and the dialogue occurs mainly between the mainframe and the ISDN terminal.

In this technical note we will give a detailed description of an original and very advantageous solution to the problem of transfer and handling of signaling messages in analog user systems.

The architectural choice, on which the proposal is based, is in favor of an optimized system in terms of hardware/software and is limited to a maximum of 180 users.

The basic idea can however be applied to the development of systems with a large number of users as mentioned at the end of this note.

TRADITIONAL SOLUTIONS

Various architectural solutions are implemented today in the handling of signaling messages and we will briefly analyse only two of them. The first solution is chosen between simple ones and the second between more complex and sophisticated ones.

In figure 2a block diagram shows a typical system in which the signaling messages are handled by various microprocessors through parallel buses for data and addresses.

Each microprocessor, which we identify with the name "peripheral μP", is placed an a "peripheral control card" and from one side it interfaces with a "central μP" while on the other side it carries on the conversation with a number of user boards through a data bus and an address bus. Each user board, which we suppose analog (subscriber card), is linked to a maximum of 16 telephones through two-wire transmission lines (telephonic pairs).

We consider the example of 4 boards, each of which refers to 16 users. The peripheral μP handles them with an address technique through a data bus and an address bus linked to each board.

A possible allocation of the wires of the buses is as follows :

- 2 wires of the address bus will be sufficient to select the single board ;

- 4 wires of the address bus will select the single subscriber ;

- 1 wire of the address bus will select the kind of operation to execute, i.e. the direction of the flow of data (read/write).

A certain number of wires of the data bus will allow the μP to carry on a dialog with the SLIC (Subscriber Line Interface Circuit) and COMBO (COMBined PCM codec and filter) devices placed on the subscriber board. These devices are respectively used for interfacing with the line and the 2/4 wires conversion and for the analog-to-digital conversion and viceversa of the message.

Appropriate comparison circuits will select the board with which the μP wants to carry on a conversation and will enable the single user circuitry inside the board itself to extract or insert information from and on the data bus.

The peripheral μP is usually able to execute a preprocessing of data received from the user circuits or of data which need to be sent to the user circuits, as, for example, to recognize selected digits in the case of rotary dial pulsing or to generate the timing of the ringing signals.

Figure 1 : A Typical Digital Exchange for Voice an Data Switching.

SGS-THOMSON
MICROELECTRONICS
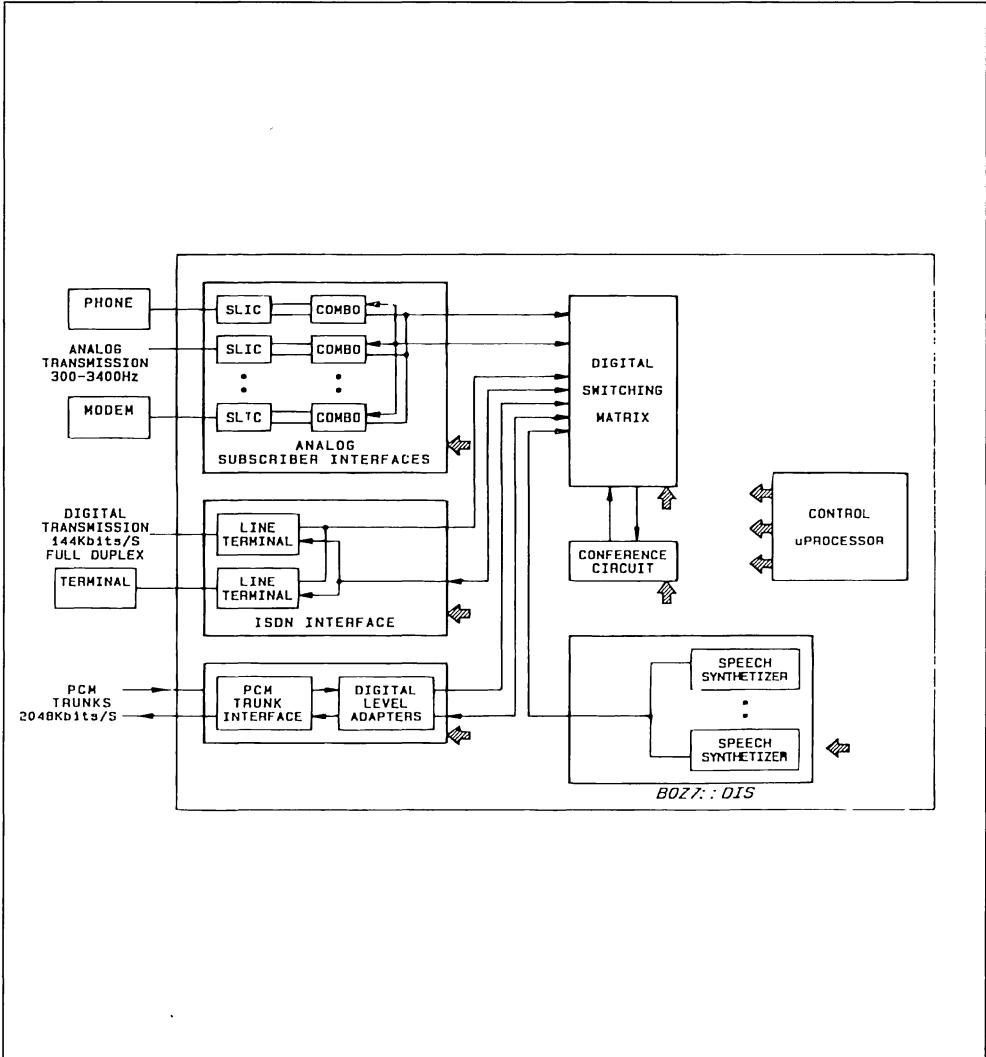
This solution, simple from the viewpoint of the system, has the advantage of being based on standard components, but at the same time it presents two real and not negligible disadvantages :

1. an additional peripheral control card must be inserted for every 4/8 subscriber cards ;

2. the number of wires to be connected between the control card and the subscriber card becomes rather high and this undermines the system in terms of overloading, reliability and consequently economy.

A surely more "elegant" solution is outlined in figure 3. On each user board or subscriber card there is a board controller known as PCB (Peripheral Board Controller) and it is identified in the diagram by the adjective "slave". The function of this PBC is to interface between the board circuitry which includes the SLIC and COMBO, and another PBC, identified as "master", which is directly managed by the mainframe (central P).

In this case, the signaling is assigned either to a well-defined channel of the TDM (Time Division Multiplexed) highways or to two of the highways dedicated only to the coded signaling according to a HDLC (High level Data Link Control) protocol. This second possibility is shown in figure 3.

The more obvious advantages which can be obtained with such a solution can be identified as :

a. reduction to two wires for signaling messages transfer (protocol HDLC) ;

b. no need for intermediate control board ;

c. well coded interface and consequently facility of expansion of the system itself.

On the other hand, the following evaluations cannot be ignored :

1. the solution is rather costly as it requires a PBC controller for each 8/16 users ;

2. many of COMBOs that are available on the market cannot interface directly with the PCM board controller.

NEW SOLUTION TO THE PROBLEM OF "HOW TO HANDLE THE SIGNALING"

The proposed solution tries to combine the positive factors associated with the system architectures described above :

1. auxiliary wires are not needed to transfer the signaling ;

2. the solution uses standard Ps and does not require dedicated components ;

3. it does not use architectures with intermediate control boards.

The idea that resolves the problem is based on the use of an auxiliary function provided by the Digital Switching Matrix (DSM) M088, the function 6 which permits the "fast extraction of 0 channels of the PCM input highways.

HOW TO HANDLE SIGNALING WITH THE M088 DSM

The M088 Digital Switching Matrix (DSM) (see appendix A "Main Characteristics of the M088 DSM" and "Functions of the M088 DSM"), beside the main switching operation in a non-blocking way of up to 256 channels and beside instructions pertaining to switching (disconnection, read/write on a channel of a PCM word, acquisition of the connection map), offers an auxiliary and particular function : the fast acquisition of 0 channels found on the 8 PCM inputs, function described in details in appendix B "The M088 function 6 : fast extraction from channels 0".

Once activated function 6, the M088 under control of an 8 bit microprocessor working with a 4 MHz clock, can perform the following operations during the time internal of one PCM frame (125 sec) :

a. extract the content of channels 0 of the 8 PCM input streams if the two most significant bits of the byte of channel 0 are not equal to "01" ;

b. provide them to the microprocessor through its internal registers ;

c. execute at least one more function among those available by the DSM, for example : the connecting function or the loading of a PCM byte on whatever output channel and in particular on the channels 0 of the output PCM streams.

M088 possibilities pointed out here together with the option of using channel 0 to transfer the "signaling" lead to the idea of using the DSM M088 not only as a switch "actuator" but also as device for the "handling of the signaling" i.e. for the extraction of the same from the PCM input streams and the insertion of the new signaling informations into the output PCM streams. The idea is more attractive in that the handling of the signaling is generally executed by circuits designed ad hoc, as described above.In brief, the M088 represents an ideal device capable of carrying on the multiple functions required in a modern switching system, functions all executed under the control of a standard microprocessor.

He will illustrate thereafter a system which, using a single M088 DSM, can manage the transfer of the signaling messages between the central processing "heart" of the system and the peripheral devices represented by the subscriber cards with up to 180 lines.

For systems of larger switching capacity, please refer to the paragraph on "How to Handle Signaling in Large Switching Systems" at the end of this note.

Figure 2 : Architectural Solution to Handle Signaling Messages Using Peripheral Control Cards.

SGS-THOMSON
MICROELECTRONICS
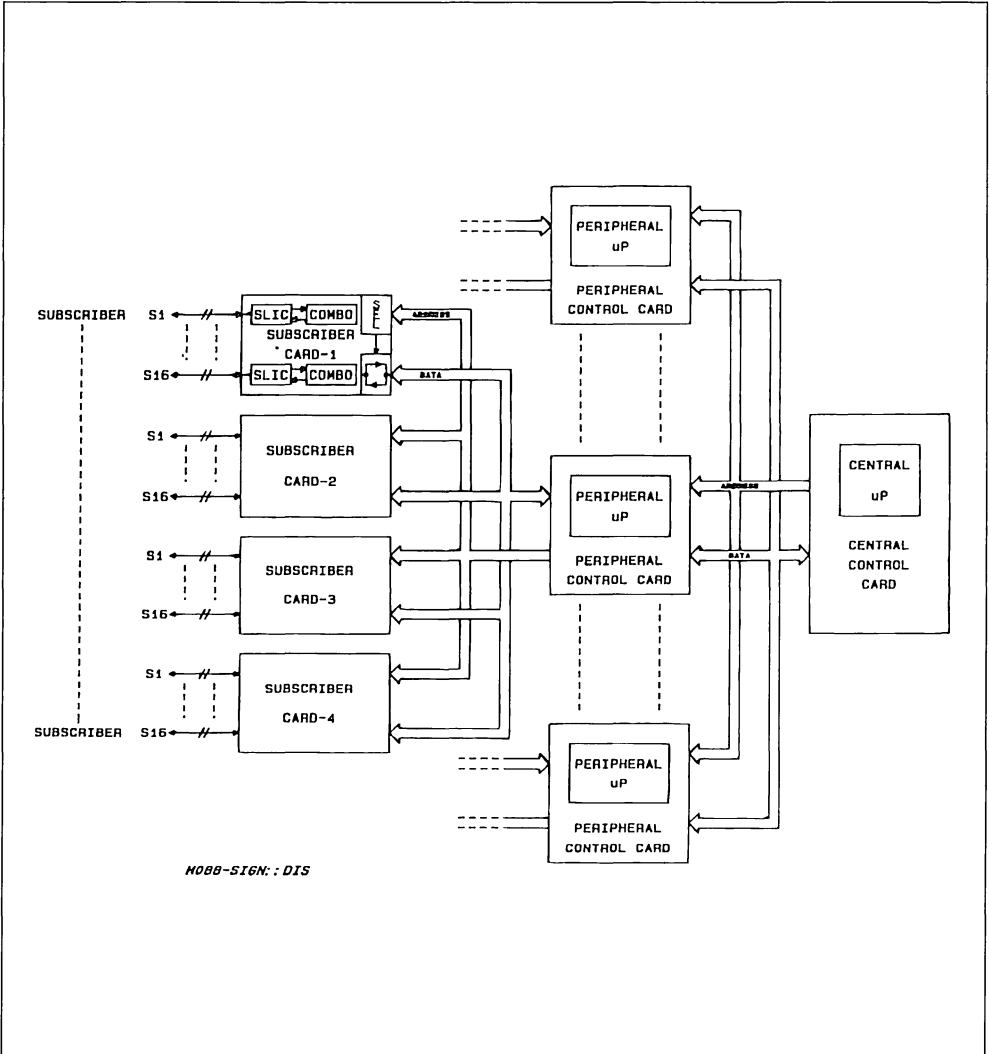
SYSTEM ARCHITECTURE AND RELATING PROCEDURES

To illustrate the architecture of the new system we specify two main sections : the peripheral equipment represented by the subscriber cards and the main section relating to switching and processing.

As shown in figure 4a, the peripheral architecture, of the system consists of a subscriber card physically connected to two PCM buses of the DSM, one for the data flow from the card to the switching section and the other for the flow in the opposite direction, and this is valid for six subscriber cards. In fact, of the 8 PCM highways available in each direction, 6 are used to communicate with the subscriber cards while the remaining 2 are kept for other functions relative to the switching section (Conference and Tone Generation).

Each card manages 30 users, each of which being assigned to a pair of SLIC-COMBO. Each of these pairs, through a simple digital circuit, will insert or extract its digitized message into or from one of the 30 channels of the PCM stream reserved for such function (voice channels). The remaining 2 channels and specifically the channel 0 and the channel 15 are respectively reserved to contain the signaling and to transfer the maintenance signals (test, control, etc).

At user card level, the logic of extracting and adding the switching informations representing the signaling from or into the 0 channels of each PCM frame is very simple, because the single pair of PCM streams from and for the DSM is rigorously assigned to a well identified user board. Each of the 30 users of the card, once every 30 temporal intervals, each of the time duration of a frame (125 μs), uses the channel 0 to insert or extract its own signaling, apart from having reserved for each frame the channel needed to insert or extract the coded voice.

Regarding the section for the managing and executing of the switching function, the system architecture can be represented as in figure 4b. The interaction between the various blocks and the necessity for the existence of the same blocks are easy to understand, analysing the procedures that must be put into action for the handling, the processing, and the executing of the signaling in the channels 0 of the PCM streams.

- the DSM activated by the microcomputer to handle function 6 extracts the bytes from the channels 0 and makes them available in its own OR1 internal registers.
- he microcomputer μP1 (for example Z80), which we will refer to as "extractor/actuator μP", reads the data of the DSM channels 0 and stores them into the RAM FIFO 1 only when the DSM requests an interruption to signal the presence of available data.

- the high processing capacity microcomputer μP2 (for example Z8000), which we will refer to as "processor μP", takes this data already stacked up by the μP1, processes the information and as a result generates other data which are stacked up in the RAM FIFO 2.

the microcomputer μP1 extracts the data from this second FIFO and generates appropriate commands towards the DSM (connections, disconnections, loading into the channels 0 or into other channels), or towards other circuits such as CC (Conference Circuit) and TG (circuit for the Generation of Tones), executing in such a way the functions requested by the previously extracted signaling.

The existence of two μPs, as will appear more clearly below, is related to the necessity of accomplishing concurrently more types of operations as above described. This is possible only if the tasks are appropriately distributed between the two processors, which must transfer the data to each other through common storage areas, the two RAM FIFOs and using these also as buffer memories they can operate at different speeds.

PROTOCOL OF COMMUNICATION BETWEEN THE TWO PROCESSORS

The architectural structure proposed for the realization of the system does not introduce specific limitations to the protocol used to synchronize the operations of the two processors.

In any case, it is appropriate to point out that :

a. after having activated functions 6, the MDC can extract, for a duration of 125 μs, all 0 channels from the 8 PCM input streams and execute at least one of the other functions.

b. the microprocessor μP1, interfaced with the DSM, in acquiring this data from the internal registers of the DSM, must respect the minimum temporal intervals between subsequent read operations (see appendix B) : therefore, there are no advantages, in terms of time saving during the read phases, either in using microprocessors more complex than the standard 8-bit ones (i.e. Z80) or in using clock frequences higher than 4 MHz.

c. the DSM selects all channels 0 with most significant bits not equal to "01". Channels 0 containing bytes of the 01XXXXXX type will be ignored.

d. it is possible to choose through a byte called "mask byte" which input flows the DSM must respect to extract the channels 0. In our example a mask byte of the 11111100 type will be needed to enable the extraction of the channels 0 of the input PCM streams from PCMIN7 to PCMIN2 (6 enabled streams).

e. the bytes are extracted from the channels 0 in a sequential way, starting from the PCM bus connected to the PCMIN7 input until the PCMIN2 input.

f. the byte extracted from each channel 0 is supplied to the OR1 register of the DSM.

From the point of view of the RAM FIFO 1, that is the memory which stores the data written from the microcomputer µP1 and read to the µP2, it is advisable to insert, at the beginning of each 6 bytes read by the µP1 from the OR1 registers of the DSM, a delimiter byte (FLAG1) which has the function of facilitating the synchronization between the processors. For example, based on the preceeding c. observation, FLAG1 can have the two most significant bits equal to 01 and reserve the other bits to define a multi/frame counter : in this way there would be no possible confusion between such a byte and a single useful data extracted from the channels 0.

If we now move to the RAM FIFO 2, the storage memory of the data written to the µP2 and read from the µP1, we find the data processed by µP2 which represent the bytes for the instructions to be sent from µP1 to the DSM or to other circuits (CC, TG). These bytes must be such as to avoid as many processing operations are possible for the µP1. One of the solutions consists of preceding each block of bytes with data relative to a specific function to be executed by the DSM or by other circuits with one control byte (CNTL), containing indications on the type of function and structured in such a way to activate in the program memory of the µP1 the routines dedicated to the single specific function executed. We will also need a separating byte (FLAG2) to allow an easy synchronization between µP1 and µP2 and such FLAG2 can be used as the "head" of a block of useful data.

Figure 5 represents a possible protocol of the communication between the two processors µP1 and µP2 through the two RAM FIFO.

Figure 3 : Architectural Solution to Handle Signaling Messages Using PBC (Peripheral Board Controller).
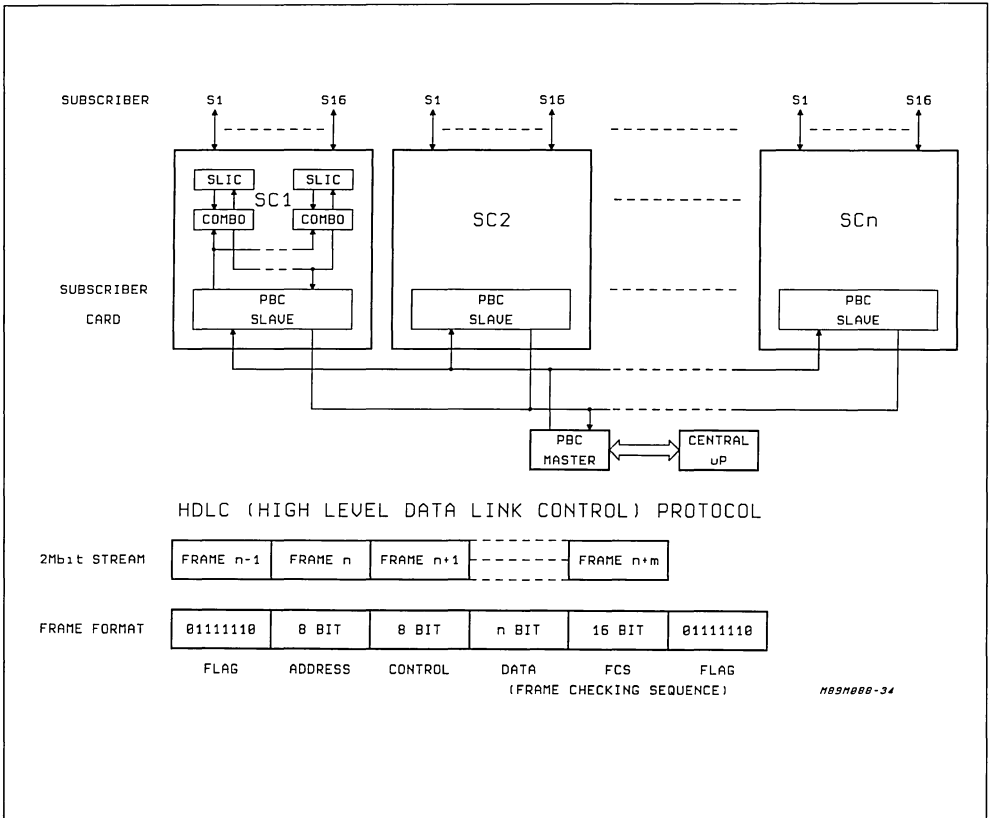
SGS-THOMSON
MICROELECTRONICS

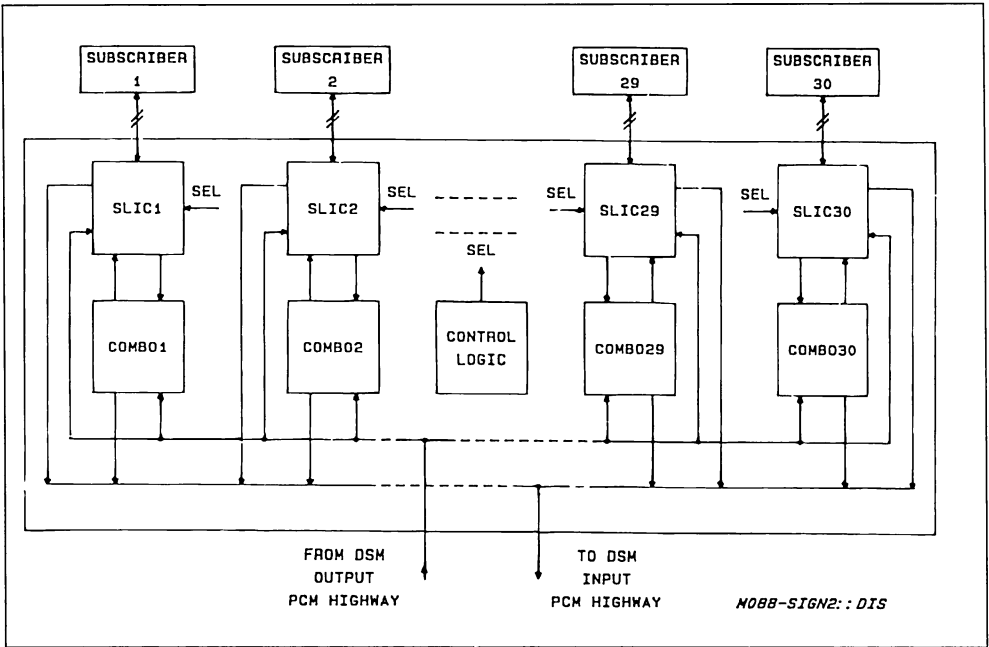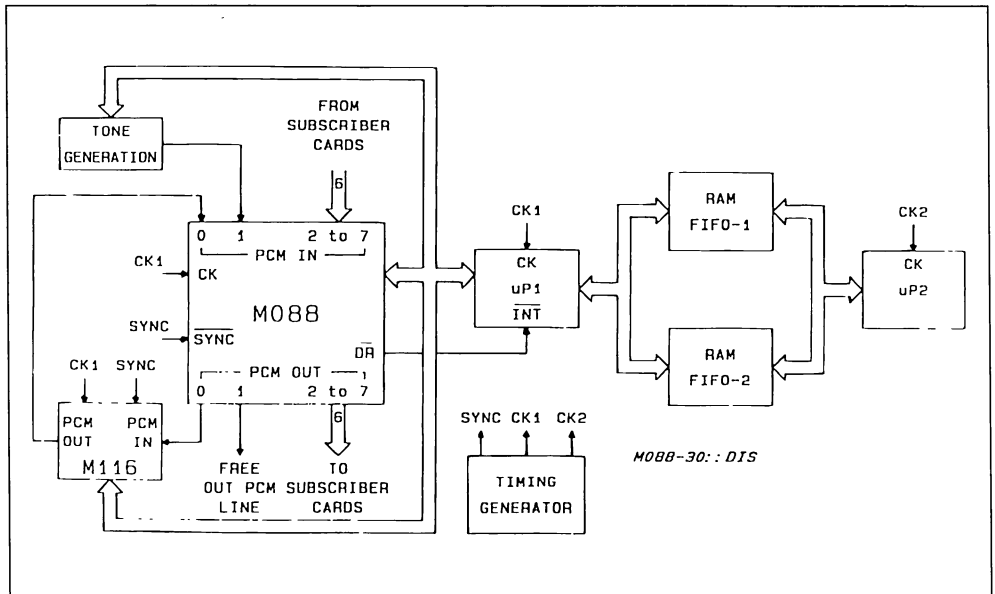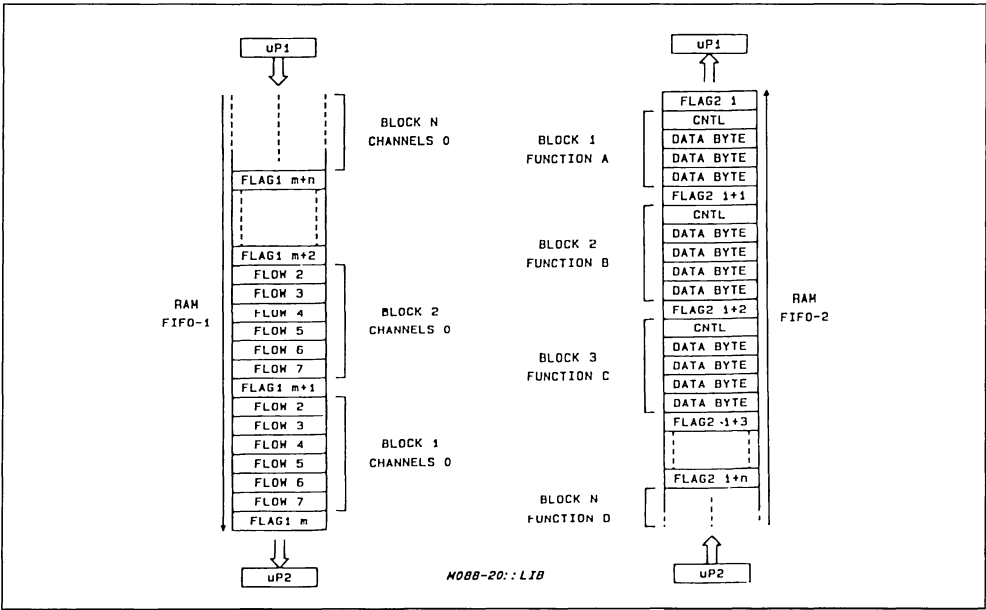**Figure 4a :** Subscriber Card of the Proposed Architectural Solution to Handle Signaling Messages.

Figure 4b : Switching and Processing Section of the Proposed Architectural Solution to Handle Signaling Messages (max. 180 users).

SGS-THOMSON
MICROELECTRONICS

Figure 5 : A Possible Protocol of the Communication between the two Processors through the two RAM-FIFO.

SIGNALING BETWEEN SUBSCRIBER CARD AND SWITCHING AREA

The information sent by the peripheral are (subscriber card) for each single user to the switching area are essentially the following two :

1. line condition (ON HOOK/OFF HOOK)
2. ground key (ON/OFF)

The 8 bits to load into channel 0 could be selected as follows :

	MSB							LSB
CHANNEL 0	D7	D6	D5	D4	D3	D2	D1	D0

D7 = 1. Remember that M088 does not read out bytes beginning with "01".
D6 = line condition.
D5 = ground key.
D4 - D0 = binary number of the user (1 - 30) to which the signaling in D6 and D5 refers.

The user number enables the processor μP2 to know which user is the source of information, while the board identification to which the user belongs can automatically be deduced from the fact that the PCM stream in which the information is loaded is unequivocally assigned to a specific single user board and from the fact that the extractions of the channels 0 of the 6 input streams are orderly and sequential.

Viceversa the 8 bits of channel 0 sent from the DSM to the subscriber card can be assigned as follows :

	MSB							LSB
CHANNEL 0	D7	D6	D5	D4	D3	D2	D1	D0

D7 = used to program an auxiliary function of the COMBO (for example the LOOP function).
D6 - D5 = used to program various operating states of the SLIC-COMBO (i.e. in the case of SLIC L3090 it is possible to choose between the following states : CONVERSATION/RINGING/STAND-BY/POWER-DOWN).
D4 - D0 = binary number of the user (1 - 30) to which the commands present in D7, D6 and D5 refer.

COMMUNICATION PROCEDURE MICRO μP1 - DSM

It has already been described above which operations must be run in the communication between the μP1 microprocessor and the DSM.

We must state that the procedure of reading/storing of the contents of the channels 0 is performed by μP2 only as a routine of response and service to the main program interruption requested by the DSM through the signal on its own output DR indicating the availability of bytes read out from channels 0. The main program of μP1 is dedicated to the sequential flow, towards the DSM and eventually towards the CC

SGS-THOMSON
MICROELECTRONICS

and TG circuits of the commands and the bytes of data necessary for them to execute the functions requested by the subscribers, using the data resulting from the processing of these requests executed by the μP2 processor.

Figure 6 represents a possible block diagram of the main program area which handles the interaction between μP1 and DSM.

We must pay attention to the fact that when the execution of a DSM function is requested, it is considered finished by the DSM only if the μP1 does a reading of the internal OR2 register of the DSM after the instruction opcode has been sent. It is only after this reading has been done that the DSM is re-enabled to execute new or pending functions, including function 6.

Reading and storing in RAM FIFO 1 of other data can then be done if there is a need to introduce procedures for controlling the status of the DSM device (using function 4 and function 5) and of the CC device. In such a case the FLAG1, header byte of the blocks memorized by μP1, must contain additional information to tell the μP2 if the following data block is relative to the extraction from channels 0 or if it contains other information and from what device they are read. A possible allocation of the FLAG1 bits can be the following : the two most significant bits equal to 00, the following bit reserved for the identification of the device to which the block of successive bytes refers, the remaining 5 bits used as a counter. One must pay special attention to the control of the interruptions in order to avoid, during the storing of these subsequent data, that an interruption occurs from the DSM as this would create confusion in the RAM-FIFO 1 data.

The FLAG2 byte used to synchronize the communication between μP2 and μP1 which is there to indicate the beginning of a useful datablock to be processed by μP1 will need have a bit configuration such as not to give rise to a wrong identification. One hypothesis is to use a byte equal to 11111111 since the configuration does not exist for any data byte or control byte nor DSM byte or CC byte.

The next CNTL byte can contain in its 4 most significant bits the binary number of the function to be executed (6 DSM functions, 6 CC functions and 4 TG functions), while the other 4 bits can be used for the cyclical numbering of the blocks.

Figure 7 shows the block diagram of the interrupt service routine.

In this routine, special attention is paid to respect the minimum time intervals between two successive readings of the OR1 and OR2 registers of the DSM. For the OR2-OR1 sequence especially an interval of at least 13 CLOCK periods (3.2 μs per CLOCK frequence equal to 4096 KHz) is necessary, while for the OR1-OR2 sequence an interval of 3 CLOCK periods (750 ns) is sufficient.

Note that the only OR1 registers containing bytes extracted from channels 0 are stored.

We would like to point out the fact that the procedures indicated here, relate to a system designed to serve 180 users distributed in 6 user boards. In case this potentiality is not all used, the mask sent by the DSM to activate function 6 must contain a number of "1s" equal to the actual number of user boards connected to the system, and additionally in the interrupt routine a corresponding number of readings of the pairs of registers of the DSM must be done with a consequent increase in the speed of execution of the routine itself.

HOW MUCH TIME IS NEEDED FOR THE μP1 - DSM INTERACTION

The use of a Z80 microprocessor such as P1, at a clock frequency of 4 MHz or at the same frequency as the DSM CLOCK (4.096 MHz) allows, withing a frame (125 μs), to extract the 6 channels 0 and to store in RAM the contents of the OR1 and OR2 DSM registers, to send and to execute a function and a half, like connection (instruction 1 of the DSM) or loading into a channel a PCM word (instruction 3 of the DSM). These are functions that require the highest number of bytes to be sent to the DSM (4 data bytes + 1 control byte).

ABOUT THE SYSTEM TIME RESPONSES

Based on the previous observations, the information relative to each subscriber is transferred to the microprocessor every 30 PCM frame, or within a time interval equal to :

125 μsec. (length of a frame) · 30 (subscribers per board) = 3.75 msec.

This interval is sufficiently reduced to correctly capture the line condition of the user also during the dialing operation.

As for the number of operations which can be executed by the DSM we have verified that this number is equal to :

1.5 (function per frame) · 8000 (frames per second) = 12000 functions per second.

From these considerations we can see that realizing the connections, sending information to the subscriber cards in the channels 0, and executing other auxiliary functions do not present any problem in relation to the time necessary to satisfy the requests of all the subscribers.

Among all the functions that can be executed, here are, as an example, the most significant ones :

- the loading into channel 0 of an appropriate PCM stream of the information necessary to activate the ringing signal of a subscriber to carry out a calling request from another subscriber.

- the connection between two subscribers after the busy signal (OFF-HOOK) has come from the called subscriber.

- the activation of conference call between a specific number of subscribers.

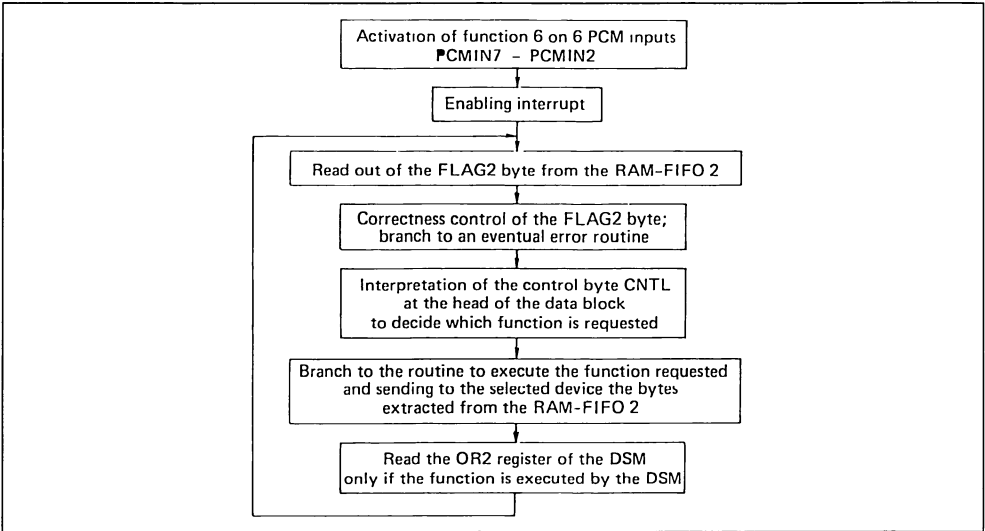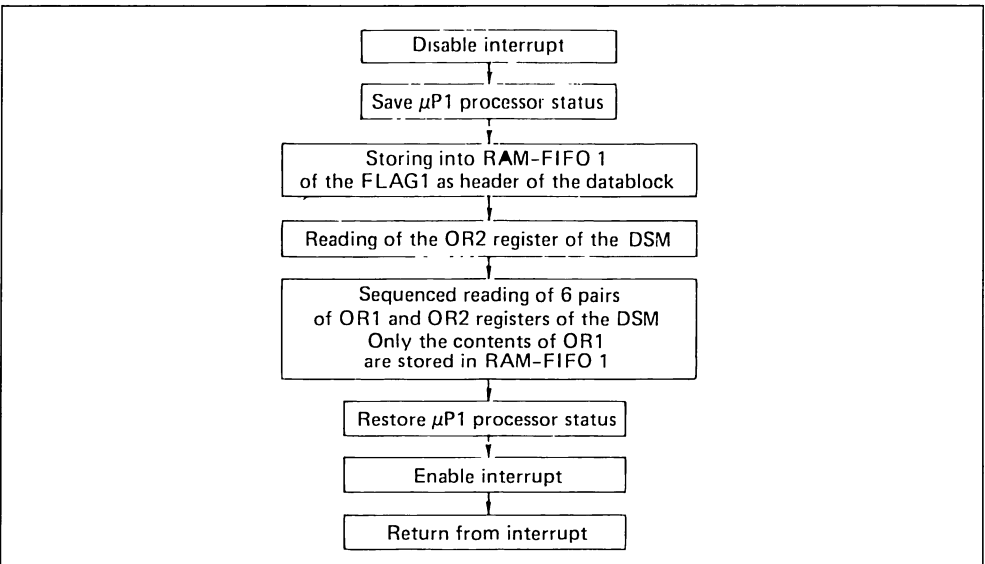**Figure 6 :** Main Program Flow-chart.

Figure 7 : Interrupt Service Routine Flow-chart.

SGS-THOMSON
MICROELECTRONICS

HOW TO HANDLE SIGNALING IN LARGE SWITCHING SYSTEMS

At the end of this technical note we want to mention the possibility of extending the illustrated solution to system using more SGS MO88 matrices.

We will present here a specific application, without wanting to preclude the adaptability and the applicability of the fundamental idea of how to handle the signaling developed previously, for systems with a larger switching capability.

We refer to figure 8 which shows four MO88s arranged in a 2 x 2 matrix, all controlled by the same µP1 microprocessor. Supposing here some additional Conference and Tone Insertion services and reserving for each PCM input and output flow the channel 0 for the transfer of the signaling from and to the subscriber card and channel 15 for the insertion/extraction of the maintenance service signals, the system represented can control up to a maximum of 420 users arranged on 14 PCM flows and having, furthermore, the possibility of a whole PCM highway output for other auxiliary services.

The µP1 micro also carries out here the functions of an "extractor/actuator". Here there is no restriction with the processing speed : in fact during the MO88 dead times, which are necessary in order to respect the minimum time interval between one operation and another, the micro µP1 can dialogue with another MO88.

In figure 8, since the PCM input flows a, b, c, d, e, f and g are shown in parallel with the MO88-A and the MO88-B, while the h, i, l, m, n, o and p flows are shown in parallel with the MO88-C and the MO88-D, it can be decided that only the DSM-A and C will perform the function of extracting the channels 0 from the input flows. As a result in the main µP1 program, it will be necessary to enable the function 6

only for the seven MO88-A IN PCM flows (11111110 mask) and for the seven MO88-C IN PCM flows (11111110 mask).

The block diagram of the interrupt service routine changes with respect to the case of a unique DSM, as shown in figure 9.

The block diagram shows the alternate reading of both matrices : this allows the functioning of µP1 at an 8 MHz frequency and the minimum time intervals between successive reading operations for each DSM are respected.

There is a similar situation in the phase of sending data bytes and control bytes from µP1 towards the DSM or other devices (CC and TG) to execute various functions : the write operations can be done by µP1 at its highest speed without performing two consecutive writings on the same device.

Regarding the response time of the system, the same considerations must be taken as for the system with a single DSM, since the number of PCM streams is substantially duplicated but at the same time it has been possible to duplicate the execution speed of the µP1 microprocessor which is interfaced with the DSMs.

For the system of the figure 8, there is an alternative solution to the one shown above for the acquisition of the input PCM flows from the channels 0, which consists in enabling function 6 in all of the four MO88s according to the following chart :

The interrupt service routine must read the OR1 and OR2 registers from the MO88 cyclically following the sequence A-C-B-D 6 times and on the seventh time only from A and C, as shown in the block diagram in figure 9 for the reading of only two MO88s. In this way the micro µP1 can use a 16 MHz clock frequency, since each MO88 is enabled one in four reading operations performed by µP1.

Device	Input PCM Flows Concerned				Mask
M088-A	a	b	c	d	11110000
M088-B		e	f	g	00001110
M088-C	h	i	i	m	11110000
M088-D		n	o	p	00001110

CONCLUSION

The process of integrating a greater number of sophisticated functions is a unique device opens the door to new architectural solutions in complex systems which are related to the problem of handling signaling and of switching.
The MO88 digital switching matrix belongs to this category of new devices.

The original architectural solution for switching systems outlined in this technical note is in fact based on using a function of this matrix definitely oriented towards the handling of the signaling.

Figure 8 : Example of Extension of the Proposed Architectural Solution for a Larger Switching Capacity (max. 420 users).
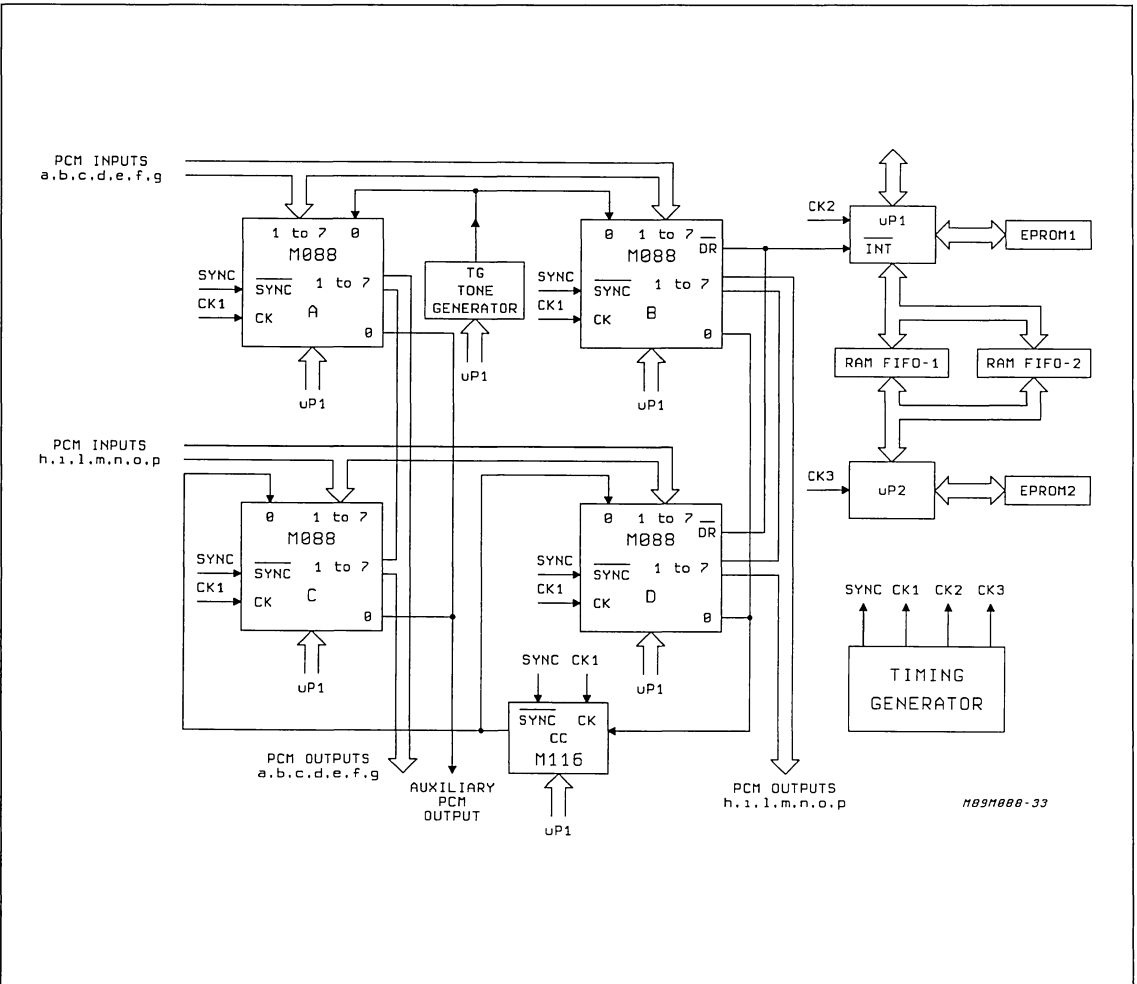

M89M088-33

Figure 9 : Interrupt Service Routine Flow-chart for the System Described in fig. 8.
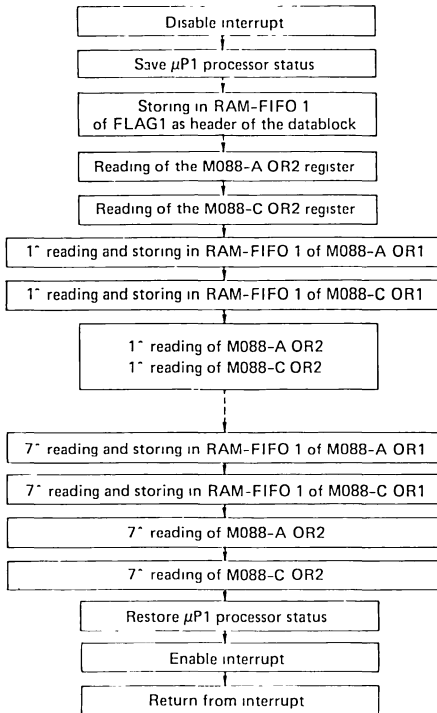
APPENDIX A

MAIN CHARACTERISTICS OF THE MO88 DSM

Figure A-1 gives a concise description of the DSM MO88.

The most significant signals are :

- 8 input PCM highways ;
- 8 output PCM highways ;
- one standard interface for an 8 bit microprocessor.

The DSM accepts in input and generated in output PCM highways in accordance either with the European standard (2048 Kbit/s) or with the Northern American one (1536, 1544 Kbit/s).

In the first case each input/output signal contains informations relative to 32 channels at 64 Kbit/s multiplexed with TDM (Time Division Multiplexing) techniques. In consequence, the MO88 DSM is capable of managing the informations coming from 256 input PCM channels.

The DSM interfacing with the microprocessor, can connect each of the 256 input PCM channels with whichever output channel among the 256 ones.

The DSM is "non-blocking", that is it is possible to obtain 256 connections simultaneously.

SGS-THOMSON
MICROELECTRONICS

Figure A1 : M088 Input/Output Signals.
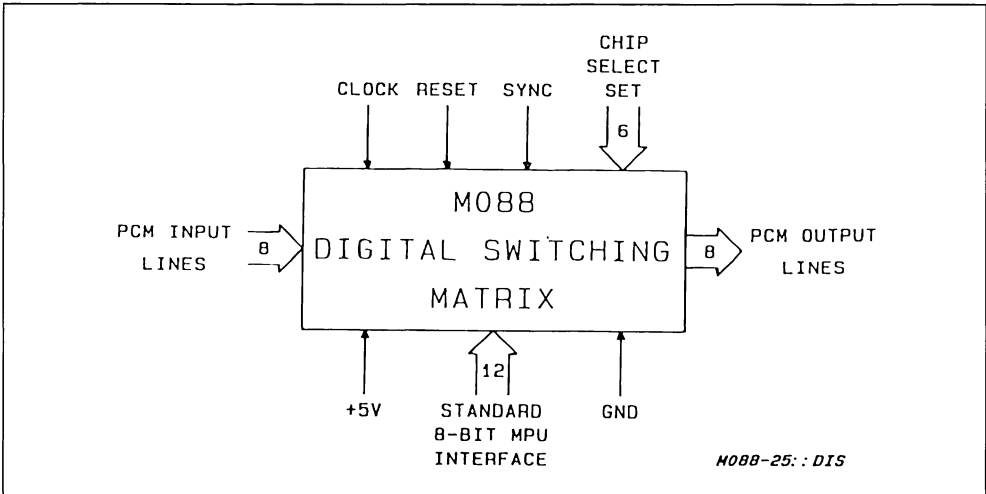
FUNCTIONS OF THE M088 DSM

Under the control of a microprocessor, the MO88 DSM can implement 6 different functions.

A generic function is executed after the microprocessor has sent some data bytes and a command byte through the data bus.

FUNCTION 1 :

Channel Connection/Disconnection. This is the main function. It allows making a new connection between an input PCM channel and an output PCM channel. The disconnection operation is valid only for the DSMs in a matrix structure.

FUNCTION 2 :

Channel Disconnection. It disconnects the selected output channel.

FUNCTION 3 :

Insertion of a Byte/Channel Disconnection. It is used to load a byte supplied by the microprocessor into a specific output channel. The disconnection operation is valid only for the DSMs in a matrix structure.

FUNCTION 4 :

Extraction of a Byte. It is used to transfer the byte contained in a selected output channel to the microprocessor through the data bus. Such a function is used to extract the only byte passing on the selected output channel at the moment of the request. Subsequent extractions are executed only after the new requests have been sent.

FUNCTION 5 :

Reading of the Control Memory. It allows the extraction of information about the status of an output channel : not connected to any input channel, loaded by the micro with a byte (the byte is also available), connect to a specific input channel (the number of the input channel and the number of the input highway to which this channel belonging are also available).

FUNCTION 6 :

Fast Extraction from Channels 0. See Appendix B : "The MO88 function 6".

NOTE : for more details on MO88 DSM see References.

APPENDIX B

THE MO88 FUNCTION 6 : FAST EXTRACTION FROM CHANNELS 0

Function 6 of the MO88 DSM is used to extract the content of the 0 channels belonging to the PCM highways or buses entering into the device on 8 input buses. A mask byte sent from the micro selects which highways the device must take into consideration and among these highways only those 0 channels whose digital word has the two most significant bits not equal to "01" are extracted. MO88 informs through an output signal (DR) the occurring of the extraction of a useful byte. The microprocessor retrieves such byte by reading the content of an internal register of the DSM.

SGS-THOMSON
MICROELECTRONICS

We will see step by step how these actions are performed.

1. Activation of Function 6 : the microprocessor sends the MASK to indicate which input buses or highways must be observed by the device. Then it sends the operation code of instruction 6.

In detail :

Control Signals				Data Buses								Notes
C/D̄	C̄S̄	W̄R̄	R̄D̄	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	1	X	X	X	X	X	M7	M6	M5	1^ Data Byte
0	0	0	1	X	X	X	M4	M3	M2	M1	M0	1^ Data Byte
1	0	0	1	X	X	X	X	1	1	1	0	Operation Code

Where :
M1 = mask bit relative to the nth bus (= 1 if it is the bus to observe or to enable)
X = bit whose value is of no interest

From the moment the operation code has been sent, at the beginning of each frame, the device executes function 6 in a repetitive way, always using the same mask and after having checked that there is not a pending instruction i.e. an instruction which would have been requested by the micro while the DSM was processing function 6. In this last case, before re-enabling the extraction from the channels 0, it executes the pending instruction. This operating way allows to keep function 6 constantly activated without sending again the three bytes mentioned above, but at the same time it allows the device to perform at least another function within a frame interval. Such function can be for example a connection.

2. Control of the Mask Stored by MO88 : it is possible to check if the DSM has correctly stored the mask by reading the internal register OR2 of the DSM. It is possible to obtain the information from MO88 only if the OR2 reading is done in the time interval between the moment when the opcode is sent and the instant in which the DSM makes the results of the extraction available (see below).

In detail :

Control Signals				Data Buses								Notes
C/D̄	C̄S̄	W̄R̄	R̄D̄	D7	D6	D5	D4	D3	D2	D1	D0	
1	0	1	0	N2	N1	N0	Tn	1	1	1	0	Reading of 0 R2

Where :
N2, N1, N0 = sum of the buses on which the device must activate function 6
Tn = bit of activation or suppression of function 6
If a mask has been sent which is not null or not composed only of 0, Tn = 1 : function activated.
If a null mask has been sent, Tn = 0 : function disactivated
1110 = operation code for instruction 6.

Since there are only three bits to indicate the sum of the activated buses, 7 activated buses maximum can be indicated when N1, N2, N3 = 111. The additional information supplied by Tn allows to discern between the case where all 8 buses have been activated (Tn = 1, N1, N2, N3 = 000) and the case where a null mask has been sent (Tn = 0, N1, N2, N3 = 000).

3. Extraction from Channels 0. Activating the extraction can lead to two different results :

3a. there is no useful information in the channels 0 belonging to the activated buses i.e. in all channels 0 tested the PCM words begin with "01". In such case, the DSM prepares itself to accept other instructions until the beginning of the next frame when it will re-activate function 6.

3b. at least in one of the channels 0 tested there is some useful information :

- a level 0 is sent on the DR output pin, level which remains for about two clock intervals (500 nsec. if the clock frequency is 4096 KHz), signaling in this way to the microprocessor that the information obtained on its channels 0 are available.

- the DSM makes available inside itself the contents of the 0 channels in sequential mode starting with the activated flow with the highest identification number.

- the procedure for the extraction of this information must begin with the reading of the OR2 register.

APPLICATION NOTE

Control Signals				Data Buses								Notes
C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
1	0	1	0	N2	N1	N0	Tn	1	1	1	0	Reading of OR2

Where ·
Tn = activation bit. Always = 1 because there are always informations to extract given that the DR has become low.

N2, N1, N0 = sum of the activated buses i.e. sum of those buses previously activated by the sending the mask and with 0 channel's words not beginning with "01". Such sum can only be inferior or equal to the one found previously in the OR2 register before the DR becom became low. Having only 3 bits, the maximum sum can be only 7. In the case in which all 8 input buses are active, the situation of the OR2

bits will be :

$$N2, N1, N0 = 000 \ Tn = 1$$

1110 = operation code of function 6
- the data transfer procedure from MO88 to micro continues by reading alternately OR1 and OR2 registers.

In detail :

Control Signals				Data Buses								Notes
C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	1	0	S7	S6	S5	S4	S3	S2	S1	S0	Reading of OR1
1	0	1	0	P2	P1	P0	Fn	1	1	1	0	Reading of OR2

Where .
S7 S0 = PCM word contained in the channel 0 extracted.
P2, P1, P0 = binary number of the bus on which the channel 0 has been read ; the content is present in the OR1 previously read.
Fn = bit indicating if there are other OR1/OR2 pairs to read or not , in detail
Fn = 1 there are other pairs to read in order to complete the execution of function 6
Fn = 0 there are no other pairs to read ; the pair read is the last one. Subsequent readings will supply meaningless data

The alternate reading of both registers is necessary in order to correctly empty the stack in which the PCM words of the extracted channels 0 are stored by MO88. Continuous readings of only one of the registers would mean repeated readings of same information.

During the reading of OR1 and OR2 registers by the micro, some minimum time intervals between two reading operations must be respect. An interval of at least 13 CLOCK periods (3.2 microseconds for CLOCK frequency equal to 4096 MHz) is necessary for the sequence OR2-OR1, while for OR1-OR2 an interval of 3 CLOCK periods (750 nanoseconds) is sufficient.

The conclusion of the procedure relative to function 6 is ratified by the reading of the OR2 register of the last useful pair (the first OR2 with the Fn bit = 0). It is only after the reading of such register that the DSM starts to process in the same frame the other functions which had been left waiting in the meantime and to re-active the same function 6 at the beginning of the next frame. Forgetting to read this register puts the DSM into a waiting state.

4. Deactivation of Function 6 : when the DSM receives a null mask i.e. made up of all 0s, it will deactivate the procedure of extraction from the channel 0. The deactivation will obviously occur also if the DSM is reinitiated with a RESET pulse.

SGS-THOMSON
MICROELECTRONICS

TS5070/5071 COMBO II PROGRAMMING AND HYBRID BALANCING WITH SOLID-STATE SLICs

by Bernard SABY

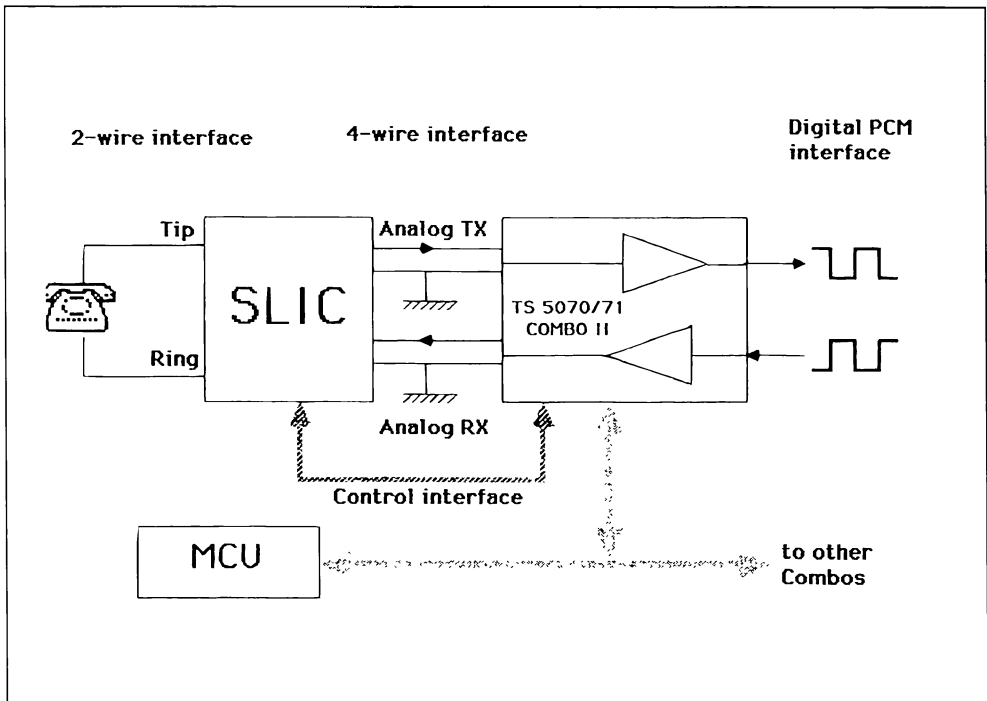## 1. INTRODUCTION

2. SCHEMATIC DIAGRAM

3. PROGRAMMING THE TS5070/71 COMBO II
- Control
- Latches
- Time-slot and Ports
- TX gain and RX gain

4. HYBRID BALANCING
- Echo path of the SLIC
- Optimization software

5. CONCLUSION

1. INTRODUCTION

The TS5070/71 COMBO II is a programmable Co-dec/Filter circuit especially developped for the subscriber line card applications in a central office or PABX.

Compared to the currently used first generation co-fidecs, such as : ETC 5054/57, M5913/14, ... the TS5070/71 COMBO II provides two major enhancements :

1) Several functions, previously assumed by external components, are now "on-chip" with the TS5070/71 COMBO II. Such features include :

- Gain adjustable transmit and receive amplifiers (25.4dB range).
- Time-slot assignment (one out of 64).
- PCM port assignment (2 transmit and receive ports, on the TS5070).
- Analog and digital loopback, for test mode.
- Hybrid balance cancellation filter.

2) All these added functions are programmed by the card-controller, through a 4-wire serial bus. Other programmable features include :

- A-law or μ-law selection.
- European (2.048 or 4.096MHz) or North American master clock (1.536 or 1.544MHz).
- 6 input/output interface latches (5 on the TS5071). These latches facilitate the logical interface with a transformer or an electronic parallel control SLIC, such as L3090 or any other function.

The programmable features of the TS5070/71 COMBO II simplify the design of the line card and provide more flexibility, especially when the same module must operate in different countries and must deal with the various telecom administrations requirements : only a few external components must be changed in the SLIC and the major adaptations are assumed by the TS5070/71 COMBO II programming.

As an example, this note describes briefly the design of a line card module, using a TS5070/71 COMBO II with a transformer SLIC and the solid state SLICs from SGS-THOMSON Microelectronics : the TDB7711 Central-office oriented SLIC, the L3090 PABX oriented SLIC and the adaptation of the line card kit to several telecom administrations requirements.

The TS5071 basic version of the COMBO II is packaged in a 20-pin DIL case. The TS5070 is a full feature version available in a 28-pin PLCC or 28-pin DIP package :

- Interface latch pin IL5 is bonded out : 6 input/output latches are available.

- Programmable ports : DX1, DR1, and TSX1 are bonded out : 2 PCM port are available.
- Serial interface : CI and CO are separated.
- Clock inputs : BCLK and MCLK are not bonded together, providing two separate clock inputs.

2. SCHEMATIC DIAGRAM

TRANSFORMER SLIC

The design of the transformer is greatly simplified, due to the on-chip hybrid balance cancellation filter : Only one single secondary winding is required (see fig. 1). ZT is the line termination impedance as reflected through the transformer (impedance measured between Tip and Ring) : its value is determined by the administration requirements and the transformer characteristics.

ZT provides an echo : a part of the receive signal on VFRO is injected into the transmit path VFXI. The internal hybrid balance filter is designed in order to replicate the echo path, and thus to cancel it.

In this application, the input/output latches are used as relay drivers (buffered through an external transistor) : ring relay, test relays... and line monitoring : off-hook detection, ground key detection. Thus, the card controller can monitor the whole line card module through the unique control port of the TS5070/71 COMBO II.

When the CS pin is held high by the card controller (chip disabled), the CO output of the TS5070 is placed in a high impedance state, allowing several TS5070/71 COMBO II to share the same data link.

SGS-THOMSON MICROELECTRONICS SLIC AND THE TS5070/71 COMBO II : A KIT APPROACH

SGS-THOMSON Microelectronics provides now solid-state monolithic SLICs. These chip-set (a high voltage line interface and a low voltage control unit), associated with the TS5070/71 COMBO II and the especially designed protection components, feature all the BORSCH functions (i.e. Battery feeding, Overvoltage protection, Ringing injection, Supervision of the loop, Codec/Filter and Hybrid 2-wire to 4-wire conversion). The versatility of these kits allows an easy adaptation for the different Telecom Administrations requirements throughout the world.

The schematic diagrams are detailed in fig. 2 and 3. When using the TDB7711, or the L3030, serial interface SLIC, the control interface must be directly connected to the card controller through a separate serial data link for informations exchange between the SLIC and the card controller (see fig. 2).

When using the L3090 PABX dedicated SLIC, its parallel control interface allows the use of the IL interface latches of the TS5070/71 COMBO II (see fig. 3).

The ZAC impedance synthesizes the output impedance of the SLIC on Tip & Ring ; hence, this network should be designed differently for each country. The structure of this network is a copy of the line impedance ; please, refer to the relevant SLIC data-sheet for more details. The "balancing" network, ZA and ZB is used by the SLIC to balance the 2-wire/4-wire conversion. When using the TS5070/71 COMBO II, this balancing network is reduced : 2 single resistors, the main part of the hybrid balancing is performed by the "Hybal" filter of the Combo.

3. PROGRAMMING THE TS5070/71 COMBO II

The control information of the TS5070/71 COMBO II require 2 bytes of informations, with the exception of a single-byte power-up/down command.

When CS is pulled low a first "instruction" byte is shifted into the TS5070 COMBO II, at pin CI (or CI/O for the TS5071) on the falling edge of each CCLK clock pulse, the most significant bit first. During the 8th (dummy) bit, the content of this instruction is decoded by the Combo and, depending wether a "read" or a "write" instruction is performed, a second "data" byte is shifted into or shifted out from the Combo.

* Bit #1 is the single-byte control bit : when 0, this is a single-byte power-up/down instruction, no data byte is expected.

* Bit #2 is the read/write control bit : when 0, the data byte will be written by the card controller into the Combo. When 1, the data byte will be read by the card controller from the Combo.

* Bit #3, 4, 5, 6 specify which one of the 10 registers of the TS5070/71 COMBO II is to be accessed.

* Bit #7 is the power control bit : when 0, the Combo is placed in power-up state ; when 1, the Combo is placed in power-down. Note that the power state can be set in any instruction.

* Bit #0, the last bit, is a dummy bit to allow for decoding of the 7 previously entered bits. Its value is not taken into account and has no influence on the TS5070/71 COMBO II operation.

When writing to the TS5070/71 COMBO II, the data byte may follow the instruction byte immediately, or CS may be pulled high between the 2 bytes. The data byte is shifted into the Combo in the same way as the instruction byte : MSB first, on the falling edge of each CCLK clock pulse.

When reading from the TS5070 COMBO II, the data byte is shifted out, onto the CO pin (CI/O pin for the TS5071), MSB first, on the rising edge of each CCLK clock pulse. As for the write operation, CS can be pulled high between the instruction and the data byte.

After a read or a write operation is completed, it is recommended, although this is not mandatory, that the CS pin should be put high to reset the control port logic.

The content of the instruction byte is detailed in table 1 :

Table 1 : Instruction Byte.

Bit #	7	6	5	4	3	2	1	0
Single Byte Power-up/down	P	X	X	X	X	X	0	X
Control Register	P	0	0	0	0	W	1	X
Latch Direction Register	P	0	0	1	0	W	1	X
Interface Latch Register	P	0	0	0	1	W	1	X
Receive Time-slot/port	P	1	0	0	1	W	1	X
Transmit Time-slot/port	P	1	0	1	0	W	1	X
Receive Gain Register	P	0	1	0	0	W	1	X
Transmit Gain Register	P	0	1	0	1	W	1	X
Hybrid Balance Register # 1	P	0	1	1	0	W	1	X
Hybrid Balance Register # 2	P	0	1	1	1	W	1	X
Hybrid Balance Register # 3	P	1	0	0	0	W	1	X

P = Power control bit . "0" = Power-up, "1" Power-down
W = Read/Write control bit : "0" = Write, "1" = Read
X = don't care (0 or 1)

APPLICATION NOTE

DATA BYTE : CONTROL REGISTER

The content of the control register is detailed in table 2 :

Table 2 : Control Register.

Bit Number								Function
7	6	5	4	3	2	1	0	
0	0							MCLK = 512KHz
0	1							MCLK = 1.536 or 1.544MHz
1	0							MCLK = 2.048MHz*
0	1							MCLK = 4.096MHz
		0	X					μ-255 Law*
		1	0					A-law, with Even Bit Inversion
		1	1					A-law, no Even Bit Inversion
				0				Delayed Data Timing
				1				Non-delayed Data Timing*
					0	0		Normal Operation*
					1	X		Digital Loopback
					0	1		Analog Loopback
							0	Power Amp Enabled in PDN
							1	Power Amp Disabled in PDN*

* = State at power-on initialization.

The * specifies the default value of the control register at the power-on initialization.

<u>MCLK</u> : Master clock used by the Combo's filters, encoder and decoder. It is necessary to indicate which frequency is beeing applied to the Combo, for a correct filter operation.

<u>COMPANDING LAW</u> : the μ-255 **com**pressing and ex**panding** law is used in USA & Japan, A-law in Europe. Usually, in A-law, even bits are inverted : 0000 0000 becomes : 0101 0101 ; if this even bit inversion is performed in another part of the switching system, a "No even bit inversion" is available.

<u>DATA TIMING</u> : In Non-delayed Data Timing mode, the time-slot always begin with the rising-edge of FSX or FSR ; Time-slot Assignment is not available in this mode.
In Delayed Data Timing mode, time-slot begins after a falling edge of BCLK, when FSX or FSR is set high ; the Time-slot Assignment feature of COMBO II can be used in this mode only.

Note that PCM port selection is available in both timing modes.

<u>LOOPBACK</u> : Test modes : In Analog Loopback, VFXI is isolated from input pin and internally connected to the VFRO output, providing a complete D to D test loop.

In Digital Loopback, the PCM byte written into the Receive register, can be read back in any Transmit Time-slot at DX0 (or DX1) pin.

<u>POWER AMP</u> : if "1", the power amplifier, at VFRO

output is disabled during the power-down state, i.e. VFRO pin is high impedance state.

It is very easy to set the TS5070/71 COMBO II configuration in any "U.S." or "European" environment.

In the following example, the line card module must be adapted to an european telecom administration specifications ; should be selected :

- Master clock = 2.048MHz
- A-law with even bit inversion
- Delayed data timing (which allows the Time-slot assignment feature)
- Normal operation (no loop back)
- Power amp disabled in power-down

Consequently, the instruction byte 10000010 (82 hexadecimal), followed by the data byte "10100001" (A1 hexadecimal) should be written into the COMBO II.

DATA BYTE : LATCH DIRECTION REGISTER

Bit Number							
7	6	5	4	3	2	1	0
L0	L1	L2	L3	L4	L5	X	X

* The bits #7 to #2 specify the function of each interface latch pin ; bit #0 and bit #1 are dummy bits.
* If Ln = 0 then ILn is a high-impedance input.
* If Ln = 1 then ILn is an output.

Notes : - unused pins should be programmed as outputs.
- When using the TS5071 the IL5 pin should be programmed as an output.

SGS-THOMSON
MICROELECTRONICS

In the case of a L3090 SLIC, as described in fig. 3, IL0 pin, IL1 and IL4 are connected to L3090 inputs : they must be programmed as outputs. IL2 and IL3 must be set as inputs, because they are connected to L3090 outputs and IL5 is not used : this pin should be set as output.

In this example a "11001100" (CC hexadecimal) code should be written into the Latch Direction Register.

DATA BYTE : INTERFACE LATCH REGISTER

Bit Number							
7	6	5	4	3	2	1	0
D0	D1	D2	D3	D4	D5	X	X

X = Don't Care.

* When writing to this register, the IL pins programmed as outputs assume the state of the corresponding bit Dn, in data byte.

* When reading from this register : for the IL pins programmed as outputs, the Dn bits correspond to the data previously written in this register ; for the IL pins programmed as inputs, the Dn bits correspond to the data read by these input pins.

In the case of the L3090 (fig. 3), if the SLIC must be put in "stand-by" mode, i.e. PWON and RNG pins = 0 and NCS = 1, "00001000" (08 hexadecimal) should be written into the Interface Latch Register. Note that bit #5 and bit #4 have no effect, since the IL2 and IL3 pins are programmed as input.

DATA BYTE : RECEIVE TIME-SLOT REGISTER AND TRANSMIT TIME-SLOT REGISTER

Bit Number and Name								
7 EN	6 PS	5 T5	4 T4	3 T3	2 T2	1 T1	0 T0	
0	1	X	X	X	X	X	X	Disable DX Outputs (in TX reg.) Disable DR Inputs (in RX reg.)
1	0	Time-slot (0-63)						Enable DX0 Output, Disable DX1 (in TX reg.) Enable DR0 Input, Disable DR1 (in RX reg.)
1	1	Time-slot (0-63)						Enable DX1 Output, Disable DX0 (in TX reg.) Enable DR1 Input, Disable DR0 (in TX reg.)

* The 6 bits T5-T0 assign one time-slot from 0 to 63 (111111 in binary) ; available in Delayed Data Timing only.

* The PS "Port Selection" bit #6 selects the DR0 input, when 0, or the DR1 input, when 1, in the Receive Time-slot register, and, respectively DX0 or DX1 output in the Transmit Time-slot register.

Note : On the TS5071 the DR1 and DX1 pins are not bonded out : the PS bit must always be set to 0.

* The EN bit enables (when 1) the PCM input or output selected by the PS bit or disables them (when 0).

Note : the disabled pins are in a high impedance state.

In the above example, "Delayed Data Timing" was selected in the Control Register : when using the DX0/DR0 PCM port, time-slot #5 for transmission and time-slot #27 for reception, the contents of the TX time-slot and RX time-slot registers must be : "10000101" (85 hexadecimal) and "10011011" (9B hexadecimal).

DATA BYTE : TRANSMIT GAIN AND RECEIVE GAIN REGISTER

The TS5070/71 COMBO II includes a transmit and a receive programmable amplifier ; these amplifiers allow an easy setting of the transmission level point (0TLP = 0dBm0) of the COMBO II, within the specified limits. The following formulas give the 2 bytes to be programmed in the TX and the RX gain registers :

$200 \times \log_{10}(V_{VFXI} / \sqrt{0.6}) + 191$, for the TX Gain Register, converted in binary.

$200 \times \log_{10}(V_{VFRO} / \sqrt{0.6}) + 174$, for the RX Gain Register, converted in binary.

V is the desired analog voltage, at VFXI pin for TX gain and VFRO pin for RX gain, expressed in Vrms, and corresponding to a digital 0dBm0 PCM level, as defined in CCITT G.711 ; the transmit input signal at VFXI must be in the range of 0.087 to 1.619Vrms, and the output receive amplifier at VFRO provides a signal from 0.106 to 1.96Vrms (for a 0dBm0 PCM signal).

The TX and RX gains can be also calculated from

the desired analog levels at VFXI and VFRO expressed in dBm into 600Ω ; in this case, the bytes to be programmed are calculated as follows :

10 X (VFXI level in dBm 600Ω) + 191, for the TX Gain Register, converted in binary.

10 X (VFRO level in dBm 600Ω) + 174, for the RX Gain Register, converted in binary.

Refer to the following example (fig. 4) :

Figure 4 : Example of TX and RX Levels.
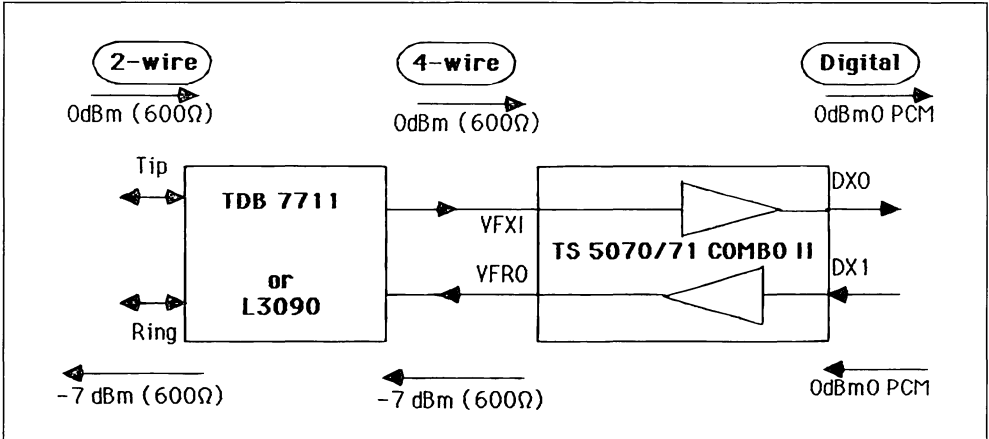
- the transmit signal is 0dBm (600Ω) on Tip-Ring wires for a 0dBm0 PCM level at the DX0 output.
- the receive signal is - 7dBm (600Ω) on Tip-Ring wires for a 0dBm0 PCM level at the DR0 input.

The 0dBm0 PCM level is the bit sequence defined in the CCITT recommendation G.711.

We must first determine the analog levels at VFXI input and VFRO output of the TS5070/71 COMBO II. Due to their "feedback loop" structure, the SGS-THOMSON SLICs always have a unity gain, in both transmit and receive direction. Consequently, the analog level at VFXI input will be : 0dBm (600Ω) = 0.7746Vrms, and the output level at VFRO : − 7dBm(600Ω) = 0.346Vrms.

The TX gain to be programmed in the TS5070/71 COMBO II will be :

10 X (0dBm) + 191 = 191 = BF hexa = 10111111 binary

this byte must be written in the TX gain register.

The RX gain will be :

10 X (- 7dBm) + 174 = 174 - 70 = 104 = 68 hexa = 01101000 binary

this byte must be written into the RX gain register.

These programmable gains provide more flexibility for the design of the line-card : if the transmit signal is - 8dBm instead of 0dBm, it is easy to re-program the TX gain register :

10 X (- 8dBm) + 191 = 191 - 80 = 111 = 6F hexa = 01101111 binary

In this case, TX gain must be set to 111 decimal = 6F hexadecimal = 01101111 binary. It is easy to adapt this example to any particular configuration. The designers shall notice that the gains are adjusted in 0.1dB steps. Consequently, the gain for - 8dBm will be 80 steps below the gain for 0dBm, i.e. 191 - 80 = 111.

Note that if the analog output level, at VFRO, exceeds 1.7Vrms, for a 0dBm0 PCM input at DR0, there are some restrictions on the value of the load connected at VFRO :

- if the level is less than 1.7Vrms, the load impedance must be greater than 300Ω
- if the level is between 1.7Vrms and 1.9Vrms, the load impedance must be greater than 600Ω
- if the level is between 1.9Vrms and 1.96Vrms, the load impedance must be greater than 15KΩ

SGS-THOMSON
MICROELECTRONICS

4. HYBRID BALANCING

The hybrid balance filter of the TS5070/71 COMBO II is entirely programmable : the "zero" and "pole" combinations for the low frequency Hybal filter #1 and the high frequency Hybal filter #2 can be set by the card controller ; in addition, a programmable attenuator adjust the amplitude of the cancellation signal (see fig. 5).

Figure 5 : Hybrid Balance Cancellation Filter.
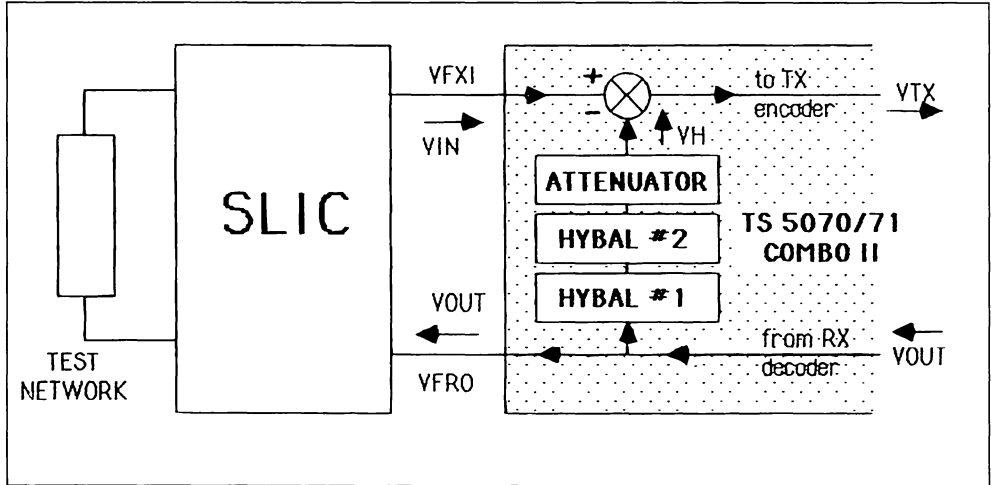
The Hybrid Balance Filter is set by the contents of 3 registers ; an optimization software (TS5077) determines the 3 bytes to be written in these registers.

ECHO PATH OF THE SLIC

The first step for the calculation of the Hybrid Balance Filter is the echo path of the SLIC : VIN/VOUT (see fig. 5). The amplitude and the phase of the echo signal must be determined for 14 frequencies, from 200 to 3500Hz. A "Hybrid Balance" test network must be connected between Tip and Ring wires.

The echo path can be measured or calculated by simulation of the transfer function of the SLIC. The TS5077 optimization software includes a simulation module for a transformer SLIC.

OPTIMISATION SOFTWARE

The echo path must be entered into the program, for each balancing network, then the optimization routine is run. This routine tests all the combinations of the Hybrid Balance Filter and selects the one which is the closest to the echo path, and then provides the three bytes to be programmed into the three Hybrid Balance registers. Some optimization examples with the different SLIC kits from SGS-THOMSON Microelectronics are described in the Application Note "COMBO II Hybal optimization with STM's SLIC kits".

5. CONCLUSION

These examples show the great flexibility of the TS5070/71 COMBO II in its adaptation with different line-cards, different SLICs and different countries. This flexibility, coupled with the programmable features, enhance the integration of the line-card : more subscribers per board, more reliability, easier adaptation, ... and, last but not least : a significant reduction of the total cost of the line card.

SGS-THOMSON Microelectronics/TS5070/71 COMBO II

Figure 1 : Interface with Transformer SLIC.

Transformer SLIC

2-wire interface

4-wire interface

Digital PCM interface

Tip

Battery

Ring

VFXI

Encoder   DX

Hybrid Balance Filter

TS 5070 COMBO II

ZT   VFRO

Decoder   DR

IL5...IL0   CS

(other detectors or actuators)

RING RELAY

OFF-HOOK DETECTOR

MCU

CI

CO

CCLK

CHIP SELECT for other COMBOs

CARD CONTROLLER
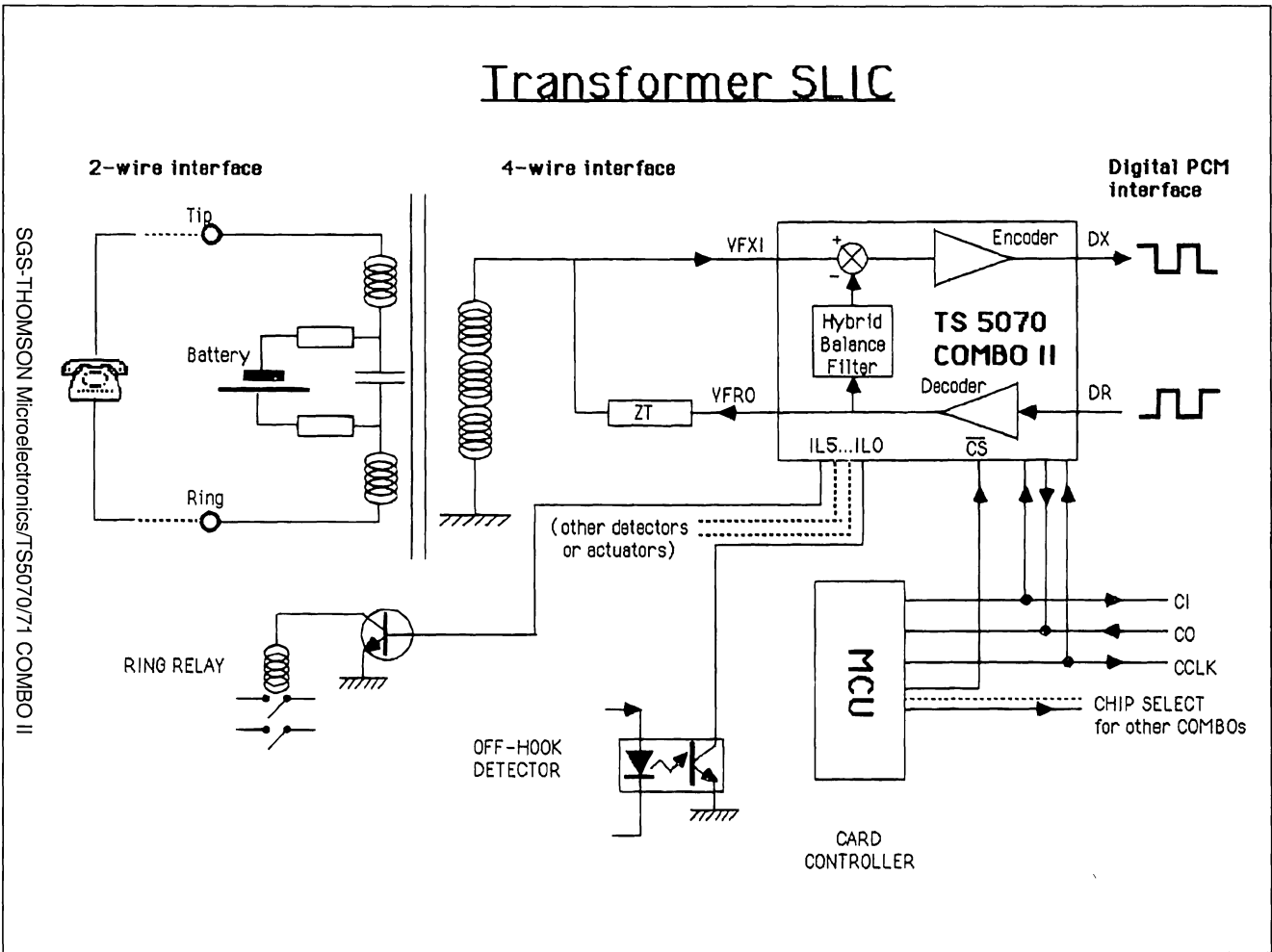
Figure 2 : Interface with TDB 7711 + 7722 Solid-state SLIC.

SGS-THOMSON Microelectronics/TS5070/71 COMBO II
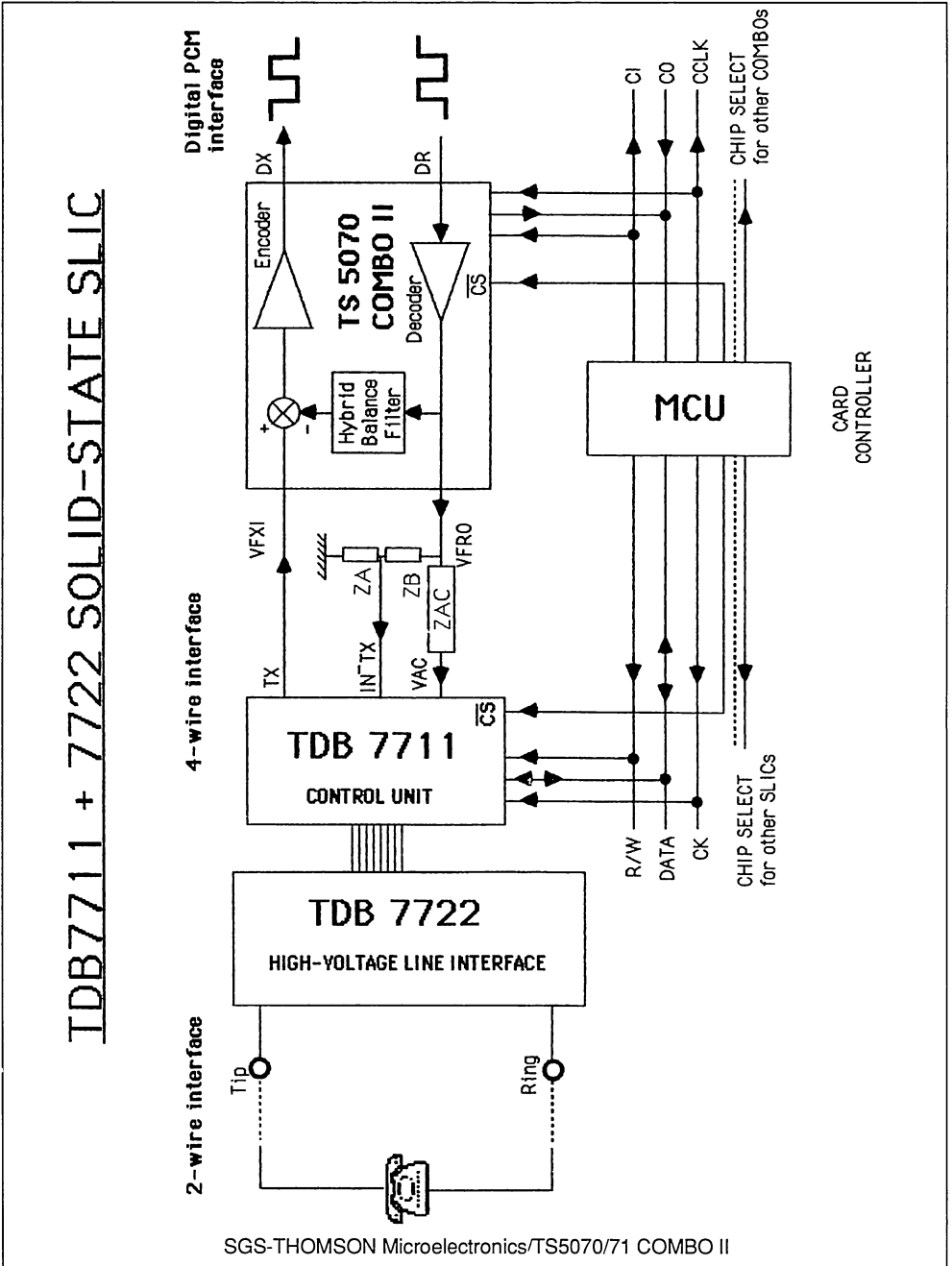
L3090 + L3000 SOLID-STATE SLIC

2-wire interface

4-wire interface

Digital PCM interface

Tip

Ring

L3000
HIGH-VOLTAGE LINE INTERFACE

L3090
CONTROL UNIT

TX

ZB

ZA

ZB

ACS

ZAC

NCS

NGDK

ONHK

RNG

PWON

VFXI

VFRO

IL4 IL3 IL2 IL1 IL0 CS

Hybrid
Balance
Filter

Encoder

DX

TS 5070
COMBO II

Decoder

DR

CI

CO

CCLK

CHIP SELECT
for other COMBOs

MCU
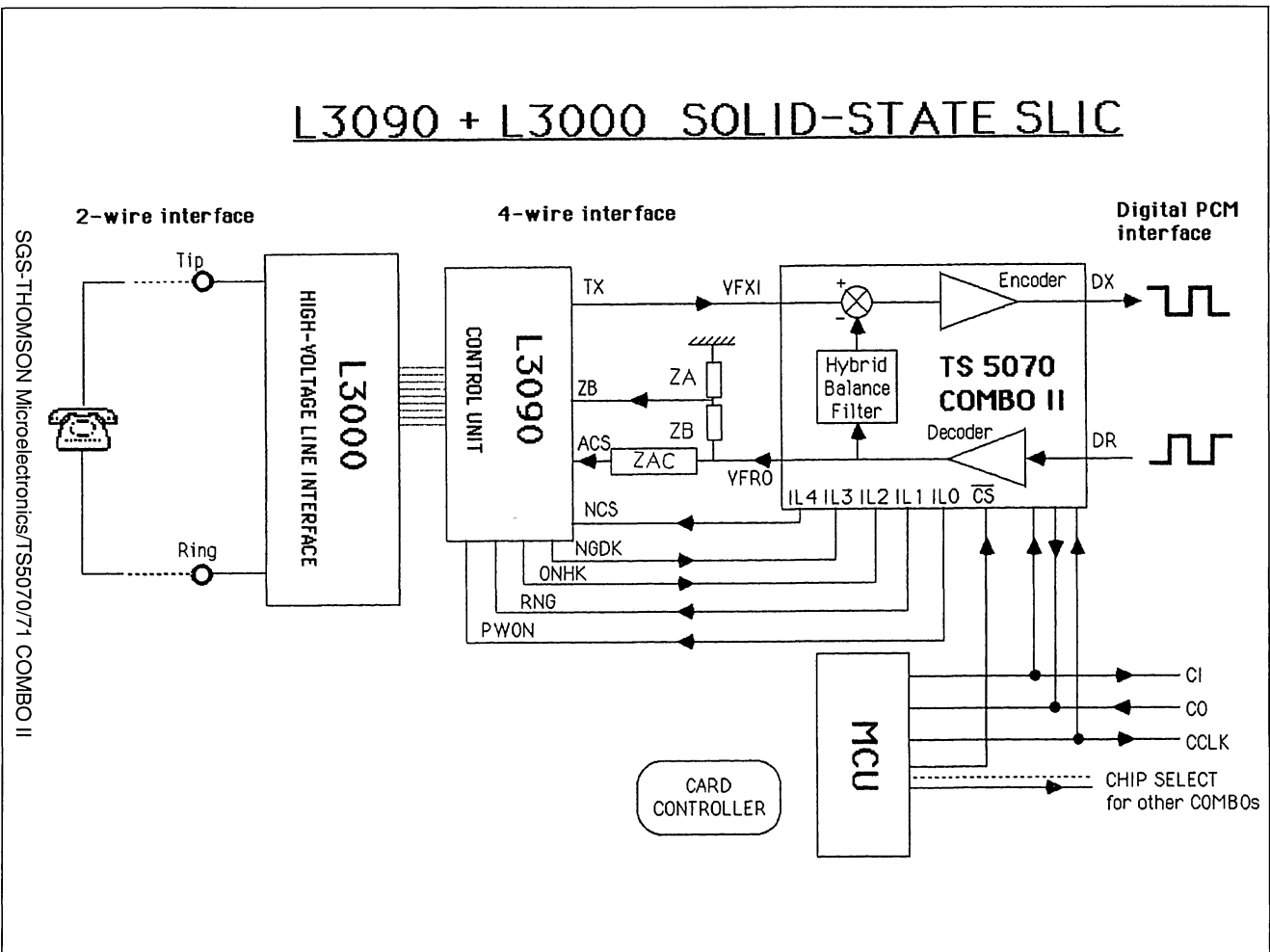
CARD
CONTROLLER

SLICOMBO   Line Card Demonstration Board
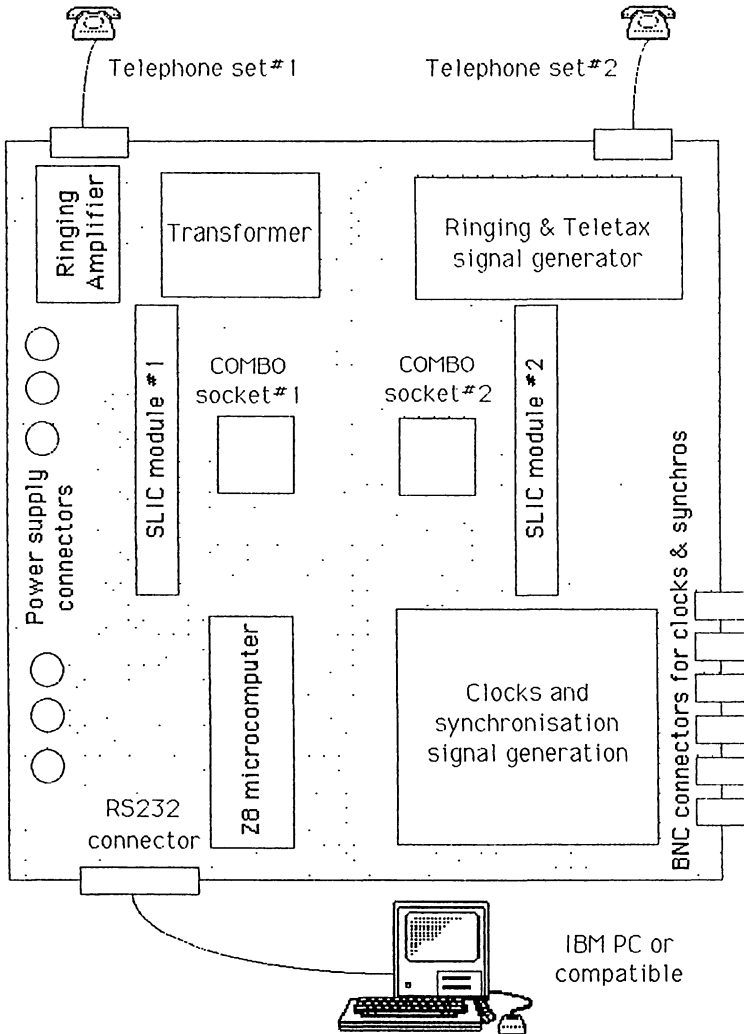
SLICOMBO is a conversational demonstration board for the subscriber line card oriented circuits developped by SGS-THOMSON Microelectronics. It includes two complete transmission modules, each of them made of a programmable codec/filter

COMBO II associated with a full silicon SLIC to achieve the "BORSCH" function (**B**attery feed, **O**vervoltage protection, **R**inging, **S**ignalling, **C**odec/filter, **H**ybrid 2-wire/4-wire conversion).

The 2-wire interface of each SLIC can be connected to a telephone set or to an appropriate test equipment. The PCM interface of the 2 COMBOs can also be connected to a PCM test equipment, or to the same PCM highway, thus allowing a real phone conversation between the 2 telephone sets through the 2 SLICs and the 2 COMBOs.

As SGS-THOMSON Microelectronics provides a wide range of SLICs, they are implemented on interchangeable modules ; 2 modules are available : one version is for the central office oriented SLIC TDB7711/7722, and one version for the PABX oriented SLIC L3090/L3000. SLICOMBO can operate either with 2 TDB7711 or with 2 L3090 SLIC modules.

The mother-board includes a ringing signal and teletax metering signal generator, a ringing signal amplifier, for the SLICs, a master clock, bit clock and frame synchronization signal generator for European (4096KHz and 2048KHz) and North-American frequencies (1536KHz).

The card controller is a single-chip Z8 microcomputer : the Z86E11A includes 4K bytes of on-chip EPROM, 48-bit I/O ports, a serial asynchronous I/O port and runs with a 11.0592MHz clock in order to provide a 9600 bits/sec baud rate to the SIO. The Z8 manages the programming of the internal registers of the 2 COMBOs and the 2 SLICs ; the Z8 also manages the different clocks and synchronization signals that must be applied to the COMBOs.

The user interface with the board is performed by an IBM Personnal Computer or true compatible. An interactive software inputs the commands from the user and displays the results on the screen ; a multi-menus approach is used by the software to make easy the programming of the SLICOMBO board. The PC sends the commands to the Z8 on the SLICOMBO board through a RS232 data link : the Z8 executes the command and sends back the result to the PC for checking.

For availability of this board, please contact your local SGS-THOMSON Microelectronics sales office.

SGS-THOMSON
MICROELECTRONICS

![SGS-THOMSON MICROELECTRONICS logo]

APPLICATION NOTE

SGS-THOMSON SLIC KITS AND COMBO II

BY W. ROSSI

1. INTRODUCTION

One of the main feature of COMBO II is the possibility to program TX and RX gains and to perform the two to four wire conversion (echo cancellation).

In particular the echo cancellation feature allows you to save external components in the SLIC circuitry.

In the following tables you can find different values for COMBOII hybrid balance filter in order to satisfy different administrations requirements.

Three SLIC KITS are analyzed :

> L3000/L3030
> L3000/L3090/91
> TDB7722/TDB7711

for each administration also the external components are specified.

If you need more specific informations the complete Application Note is available, ask for it to our sales office.

In the complete Application Note you can find all the details for each country in particular :

- Echo measurements
- Combo II simulation software results
- Bench measurements with PCM-4 Wandel & Goltermann

2. L3000/L3030 + COMBO II APPLICATION
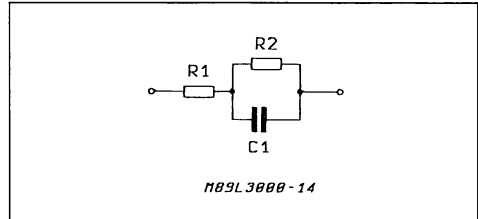
Test network :

M89L3000-14

Here below you can find the SLIC external components and the COMBO II programming coefficient for Germany, Austria and Swisse followed by the application diagram.

TX and RX gain are chosen in order to have :

0dBm0 ⇔ 0dBm   800 ohm (TXgain reg. = BF ; RXgain reg. = AE)

	Administration	R. L. Test Netw.	SLIC Ext. Comp.	THL. Test Netw.	COMBOII Hybal Coeff.
1.	Germany/Austria/ Swisse	R1 = 220Ω R2 = 820Ω C1 = 115nF	ZAC = (1) RPC = 60Ω ZA = 2K ZB = 6.19K CCOMP = 10nF (1) : 160Ω + (820Ω//115nF)	R1 = 220Ω R2 = 820Ω C1 = 115nF	EC ; 32 ; C4

Figure 1 : L3000+L3030 Appl. Diagram.
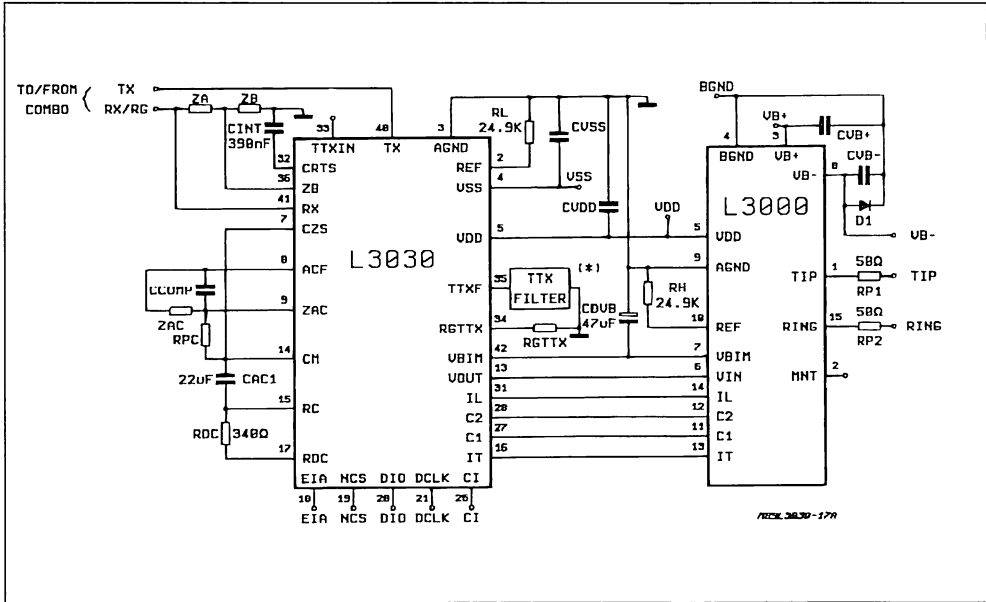
(*) All measurements were made substituting the TTX filter with 1K resistor and RGTTX with 10K. The 1K resistor is equivalent to TTX filter for speech band signals.

3. L3000/L3090 + COMBO II APPLICATION

Test network :

Here below you can find the SLIC external components and the COMBO II programming coefficient for different countries, in the next page is shown the application diagram.
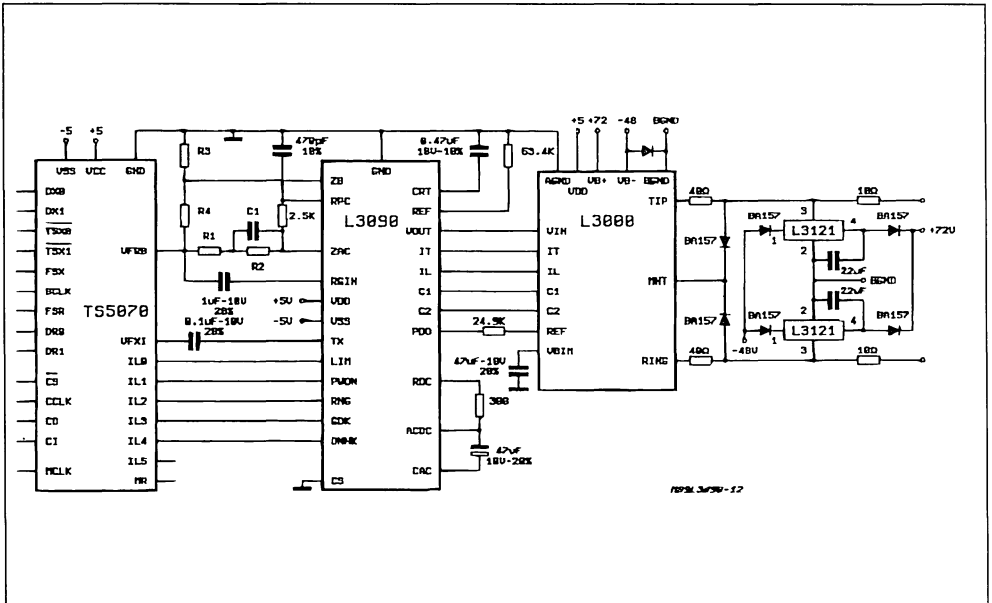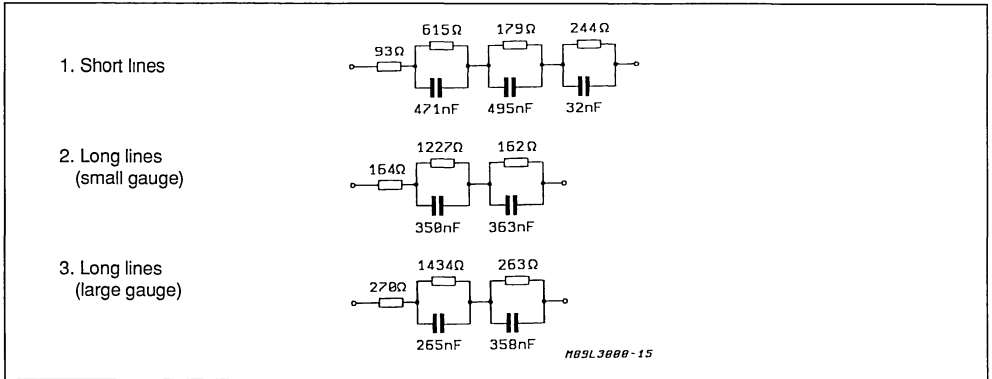
TX and RX gain are chosen in order to have :

0dBm0 ⇔ 0dBm   600 ohm (TXgain reg. = BF ; RXgain reg. = AE)

	Administration	R. L. Test Netw.	SLIC Ext. Comp.	THL. Test Netw.	COMBOII Hybal Coeff.
1.	Belgium Priv.	R1 = 150Ω R2 = 830Ω C1 = 72nF	R1 = 1.25K R2 = 20.75K R3 = 3.3K R4 = 15K C1 = 2.9nF	R1 = 150Ω R2 = 830Ω C1 = 72nF	E6 ; 12 ; AA
				R1 = 600Ω R2 = 0 ; C1 = 0	F4 ; 00 ; 03
2.	Korea/France Pub Portugal Priv./ USA Priv.	R1 = 600Ω R2 = 0 ; C1 = 0	R1 = 0 R2 = 12.5K R3 = 5.1K R4 = 15K C1 = 0	R1 = 600Ω R2 = 0 ; C1 = 0	EC ; 01 ; 48

SGS-THOMSON MICROELECTRONICS

	Administration	R. L. Test Netw.	SLIC Ext. Comp.	THL. Test Netw.	COMBOII Hybal Coeff.
3.	Finland	R1 = 270Ω R2 = 910Ω C1 = 120nF	R1 = 4.25K R2 = 22.75K R3 = 5.1K R4 = 15K C1 = 4.8nF	R1 = 270Ω R2 = 1200Ω C1 = 120nF	E9 ; 23 ; 39
				R1 = 390Ω R2 = 620Ω C1 = 100nF	F2 ; 11 ; AF
4.	Germany/Austria/ Swisse	R1 = 220Ω R2 = 820Ω C1 = 115nF	R1 = 3K R2 = 20.5K R3 = 5.1K R4 = 15K C1 = 4.7nF	R1 = 220Ω R2 = 820Ω C1 = 115nF	EE ; 12 ; AA
5.	Italy Priv.	R1 = 180Ω R2 = 630Ω C1 = 60nF	R1 = 2K R2 = 15.75K R3 = 5.1K R4 = 15K C1 = 2.4nF	R1 = 0 R2 = 750Ω C1 = 18nF	F1 ; 01 ; 6D
6.	U. K. Priv.	R1 = 370Ω R2 = 620Ω C1 = 310nF	R1 = 6.75K R2 = 15.5K R3 = 5.1K R4 = 15K C1 = 12.4nF	R1 = 370Ω R2 = 620Ω C1 = 310nF	EE ; 01 ; CC
				R1 = 300Ω R2 = 1000Ω C1 = 220nF	E8 ; 24 ; 9A

Figure 2 : L3000/L3090 + COMBOII.

4. TDB7722/TDB7711 + COMBO II APPLI-CATION

Test network :


```
M89L3000-14
```

Here below you can find the SLIC external components and the COMBO II programming coefficient for different countries, in the next page is shown the application diagram.

TX and RX gain are chosen in order to have :

0dBm0 ⇔ 0dBm   600 ohm (TXgain reg. = BF ; RXgain reg. = AE)

	Administration	R. L. Test Netw.	SLIC Ext. Comp. (*)	THL. Test Netw.	COMBOII Hybal Coeff.
1.	Finland	R1 = 270Ω R2 = 910Ω C1 = 120nF	ZAC = (1) RPC = 3K ZA = 91K ZB = 30K R_p = 30Ω CBW = 270pF (1) : 10.5K + (45.5K//2.2nF)	R1 = 270Ω R2 = 1200Ω C1 = 120nF	E9 ; 34 ; BF
				R1 = 390Ω R2 = 620Ω C1 = 100nF	B3 ; 00 ; 8F
2. ·	France Publ./ Korea/USA Priv./ Portugal Priv.	R1 = 600Ω R2 = 0 C1 = 0	ZAC = 27K RPC = 3K ZA = 91K ZB = 30K R_p = 30Ω CBW = 270pF	R1 = 600Ω R2 = 0 C1 = 0	EE ; 24 ; 0C
3.	Germany Publ.	R1 = 220Ω R2 = 820Ω C1 = 115nF	ZAC = (2) RPC = 3K ZA = 91K ZB = 30K R_p = 30Ω CBW = 270pF (2) : 8K + (41K//2.0nF)	R1 = 220Ω R2 = 820Ω C1 = 120nF	EE ; 00 ; 8C
4.	Italy Publ.	R1 = 600Ω R2 = 0 C1 = 0	ZAC = 27K RPC = 3K ZA = 91K ZB = 39K R_p = 30Ω CBW = 270pF	R1 = 0 R2 = 1100Ω C1 = 33nF	E3 ; 23 ; C0

(*) C'BW = 0.

SGS-THOMSON
MICROELECTRONICS

	Administration	R. L. Test Netw.	SLIC Ext. Comp. (*)	THL. Test Netw.	COMBOII Hybal Coeff.
5.	U. K. Public	R1 = 370Ω R2 = 620Ω C1 = 310Ω	ZAC = (1) RPC = 3K ZA = 80.5K ZB = 30K R_p = 30Ω CBW = 270pF (1) : 15.5K + (31K//6.2nF)	1. Short Lines	EF ; 25 ; DF
				2. Long Lines (s. g)	EE ; 3C ; 36
				3. Long Lines (l. g) (see note 1)	E3 ; 36 ; 31
6.	U. S. Public	R1 = 900Ω R2 = inf. C1 = 2.16µF	ZAC = (2) RPC = 8K ZA = 91K ZB = 51K (loaded) ZB = 10K (not loaded) R_p = 80Ω CBW = 150pF (2) : 37K + (47K//47nF)	1. Loaded Lines	E9 ; 50 ; DF
				2. Not Loaded l. (see note 2)	E1 ; 40 ; A8

Note : 1. U.K THL TEST NETWORKS :

1. Short lines

615Ω 179Ω 244Ω
93Ω
471nF 495nF 32nF

2. Long lines (small gauge)

1227Ω 162Ω
164Ω
350nF 363nF

3. Long lines (large gauge)

1434Ω 263Ω
270Ω
265nF 358nF

M89L3000-15

Note : 2. U.S. THL TEST NETWORKS :

1. Loaded line

1650Ω
100Ω 5nF

2. Not Loaded line

800Ω
100Ω 50nF

M89L3000-18
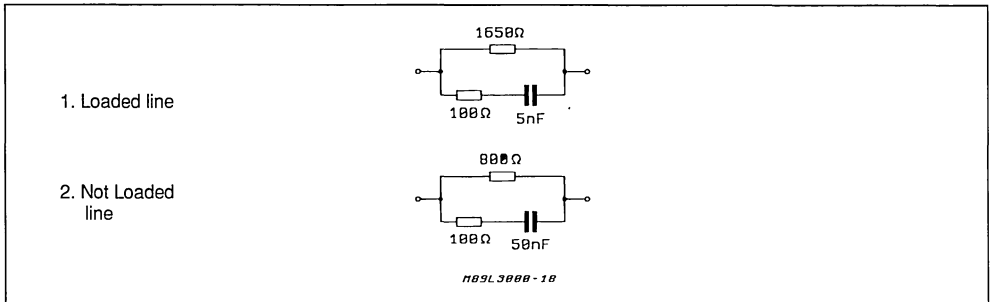
Figure 3 : TDB7722+TDB7711 Appl. Diagram.
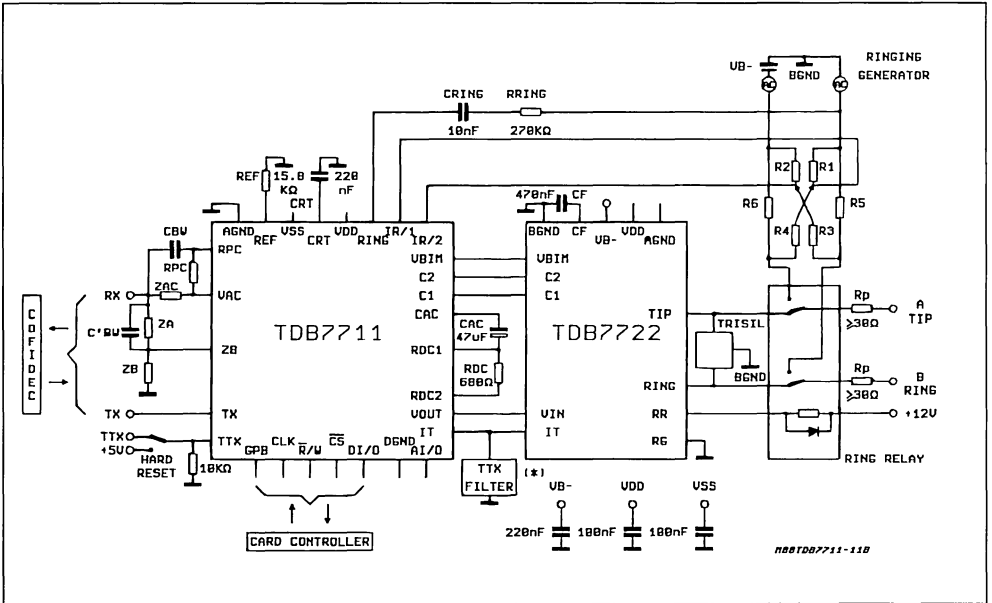
(*) All measurements were made without TTX filter being such filter equivalent to an open circuit for speech band signals.

SGS-THOMSON
MICROELECTRONICS

SLICs PROTECTION CIRCUITS

By W. Rossi

INDEX

APPLICATION NOTE

1. INTRODUCTION.

In this technical note are described different ways to protect L3000/L30XX and TDB7722/7711 SLIC KITs.

The L3000/L30XX are the more complex to protect because the positive battery can be either GND or VB+ (typ. + 72V) depending on the SLIC operating mode. In the following the first three protection solutions refers to L3000/L30XX KITs and the last one to TDB7722/7711.

The first solution in based on programmable transient suppressor L3121; and this is the most complete one: another simpler solution, based on standard transient suppressor like LS5120 or TRI-SIL is proposed. In addition a way to use only one transient suppressor for more subscribers is described. Finally a protection circuit for TDB7722/7711 SLIC KIT is proposed.

2. L3000/L30XX PROTECTION CIRCUIT BASED ON PROGRAMMABLE TRANSIENT SUPPRESSOR L3121.

In fig. 2.1. you can see the circuit configuration used

to protect the L3000/L30XX SLIC KITs with L3121. (The same structure is applied to the RING termination). When the voltage on the line increase above VB+ (typ +72V) or decrease below VB (typ. -48V) the transient suppressor L3121 intervenes and shorts the wire to ground.

For each wire we need one L3121 ; one 22nF capacitor to increase the intervention speed and three diodes : two to program the intervention voltage levels and one to pull up the supply voltage of the internal stages in order to avoid reverse voltage between line termination and supply voltage. In fact if you look at fig. 2.1. you can see that the internal output stage of the device can be fed either by GND or by VB+ depending on the status of the internal switch SW1. Since in normal operation the circuit is fed by GND and the protection intervenes when the line voltage exceeds VB+ it is evident that the reverse voltage between line termination and supply can damage the device. To avoid this fact a diode connected between line and supply increases the supply voltage when the line voltage increases (see fig.2.1.).

Figure 2.1 : Protection Circuit for L3000 (half section).

M88L3000-11

2/5

SGS-THOMSON MICROELECTRONICS
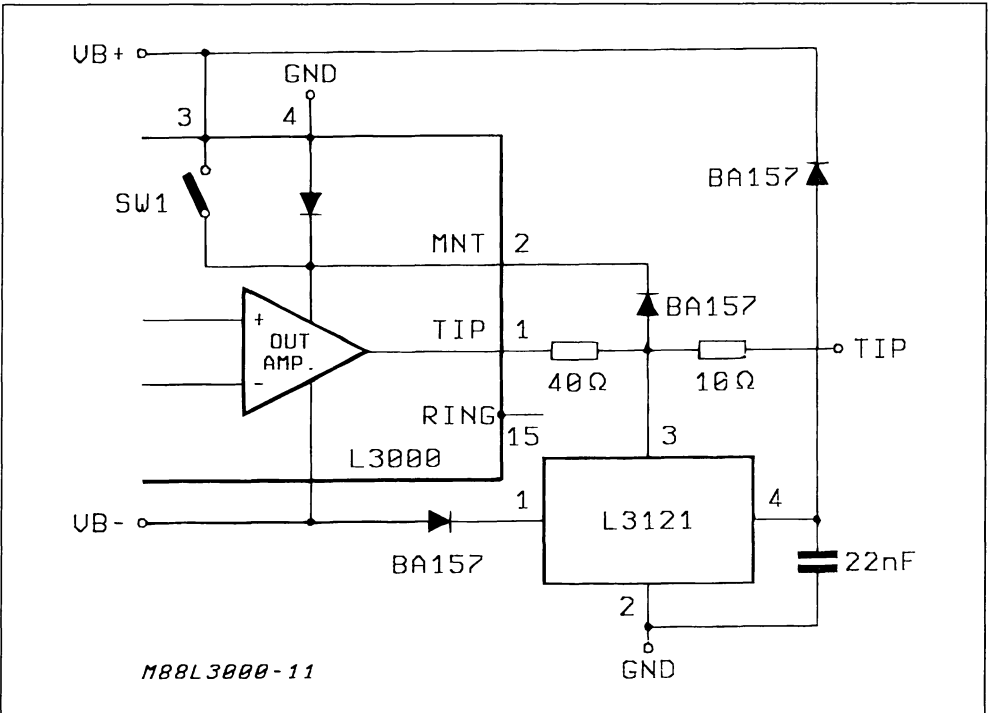
3. L3000/L30XX PROTECTION CIRCUIT BASED ON STANDARD TRANSIENT SUP-PRESSOR AS L5120 OR TRISIL.

In this paragraph is described a cheaper solution (respect to the one described in par. 2) to protect L3000/L30XX SLIC KITs.

The protection circuit is based on two LS5120 or TRISIL, a polarity guard and two diodes to avoid reverse voltages between line termination and internal stages supply (see par. 2). The two external 50ohm resistors are splitted in two parts.

The circuit diagram follows :

Figure 3.1 : L3000 Surge Protection Circuit Based on LS5120.
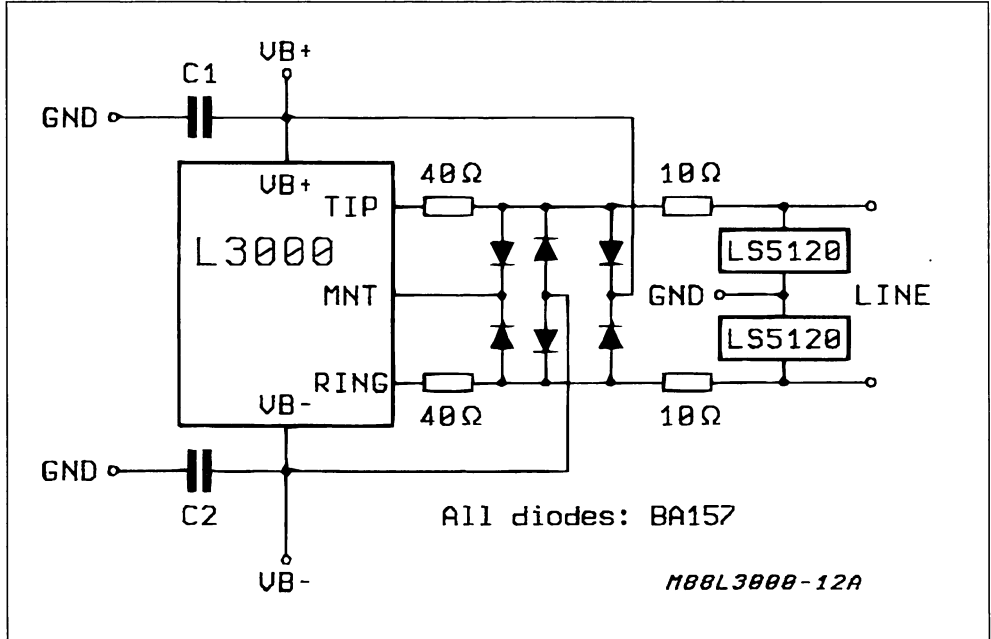
If a surge is induced on the line the LS5120 inter-venes and within 100ns it clamps the surge. During the first 100ns the LS5120 works like a 180V Zener Diode. The polarity guard avoid this 180V pulse to reach SLIC line terminations shorting it to the sup-ply voltage (see fig. 3.1.).

Two capacitors C1 and C2 guarantee that in presence of negative or positive surges the supply vol-tage remain constant enough. These capacitors can be easily dimensioned considering that the 100ns current peak flowing through the polarity guard is equal to about 110V/10Ω = 11A in the case of positive surges and about 130V/10Ω = 13A in the case of negative ones.

For negative surges (worst case) the charge Q in-

jected in the capacitor is 13A x 100ns=1.3µC (sup-posing that no current flows through the power sup-ply) therefore a 1µF capacitor is large enough to guarantee a less than 1.5V supply variation.

If instead of LS5120 another similar device is used the capacitors C1 and C2 have to be dimensioned depending on the clamping time of such device.

It should be noted that the diode type used in the polarity guard is important in order to guarantee good performances. The suggested diodes for this application are BA157. We observe that this kind of diodes in presence of a 10A, 200ns current pulse show a voltage drop of about 3V, while diodes as 1N4004 in presence of the same pulse shows a vol-tage drop ten times larger (30V).

4. L3000/L30XX COMMON PROTECTION CIRCUIT FOR MORE SUBSCRIBERS BASED ON PROGRAMMABLE TRANSIENT SUPPRESSOR L3100.

In this solution each SLIC is protected by means of a polarity guard that, in case of a surge, avoid the line terminations to exceed the supply voltages. In the following page you can see the circuit schematic of this solution.

Consider that in this application the current peak flowing through the polarity guard can reach 100A for 3KV surges ; therefore proper diodes must be used in order to avoid excessive voltage drop in presence of such current peak.

When a positive (negative) surge occurs on one line the common protection P1 (P2) clamps all the lines to ground.

Since when you short a line termination to ground the SLIC can source or sink (depending on the line termination status) up to 100mA, it can happens that once finished the surge the protection remain clamped because of the line currents.

If this fact happens all the SLICs connected to the same protection detect ground key, in this way the controller can recognize that one protection is clamped.

One possible way to open clamped protection (once the surge is finished) is to set all the SLICs connected to it in power down mode for a short time. In this way for a moment no current flow through protection allowing it to open.

Figure 4.1 : L3000 Common Protection Circuit .

SGS-THOMSON
MICROELECTRONICS
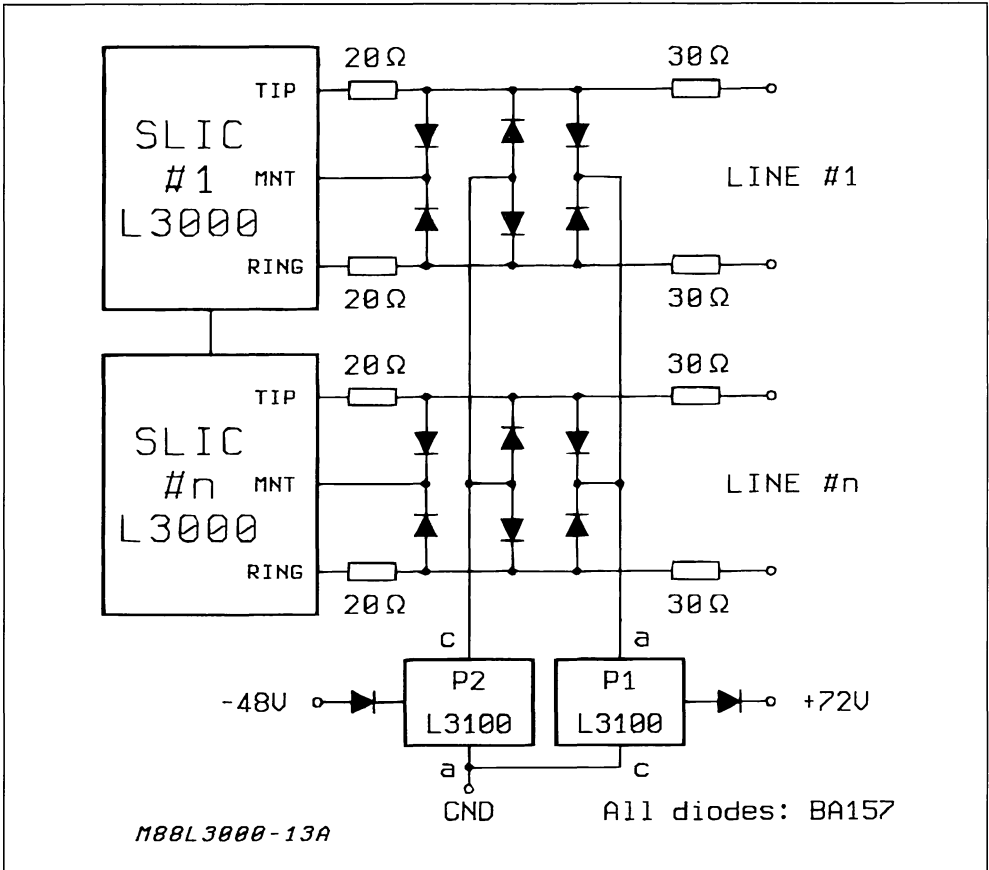
5. TDB7722/7711 PROTECTION CIRCUIT BASED ON DUAL TRISIL (THDT58D).

The fixed operating battery voltage (GND ; -VBAT) and the internal structure of the device allow to use a quite simple circuit to protect the TDB7722/7711 SLIC KIT against overvoltages induced on the line (see fig. 5.1.).

Positive surges on the line are clamped to GND by the DUAL TRISIL. In case of negative surges the

TRISIL works for a short time (hundreds of nano-seconds) as a -72V zener diode before clamping the overvoltage to GND.

Since such voltage peak is usually lower than the negative battery voltage (typ. -48V), by means of internal diodes the negative supply voltage for the device is automatically switched to the most negative between battery and line voltage in order to avoid damage to the device.

Figure 5.1 : Protection Circuit for TDB7722 .

M88TDB7722-03B

![SGS-THOMSON MICROELECTRONICS logo]
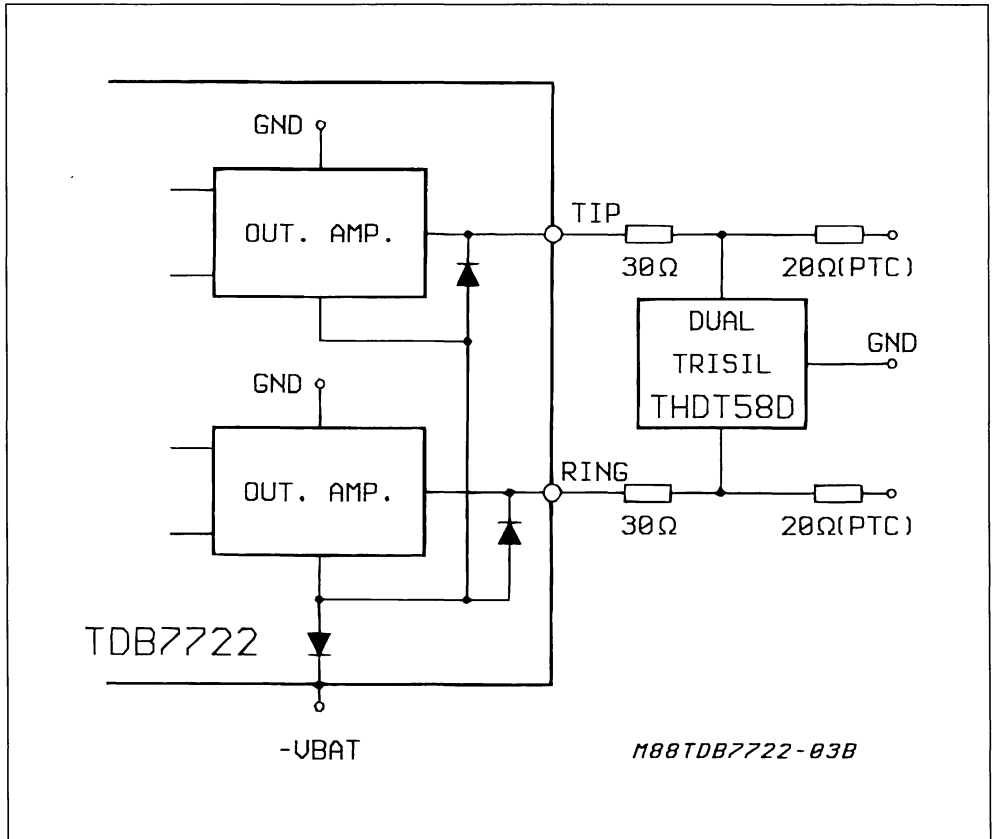
SGS-THOMSON SLIC KIT AC MODELS

BY W. ROSSI

INDEX

1. INTRODUCTION

In this note you can find the basic structure of all SGS-THOMSON Microelectronics SLIC KIT concerning AC performances.

In all these KITs are present two capacitors one for AC/DC path splitting and the other for loop stability. The effect of these capacitors is neglectible in speech band (300 - 3400Hz) therefore for each KIT are evaluated the typical AC performances not considering their influence.

If performances on a wider band or very high accuracy are requested the effect of these capacitors must be included.

Another possibility to study the effect of these capa-

citors is to enter the SLIC structure in a circuit simulator like SPICE, as shown at the end of this note with the L3000/L3090 SLIC KIT.

2. L3000/L3010 SLIC KIT BASIC STRUCTURE

Here below you can see the basic structure of the L3000/L3010 SLIC KIT concerning AC performances.

For an easier representation the high voltage part is drawn as a single ended amplifier with a gain of 40. Close to each node is written the corresponding pin number of L3010. The components names are the same used in the data sheet.

Figure 2.1 : L3000/L3010 SLIC Basic Structure.

SGS-THOMSON
MICROELECTRONICS
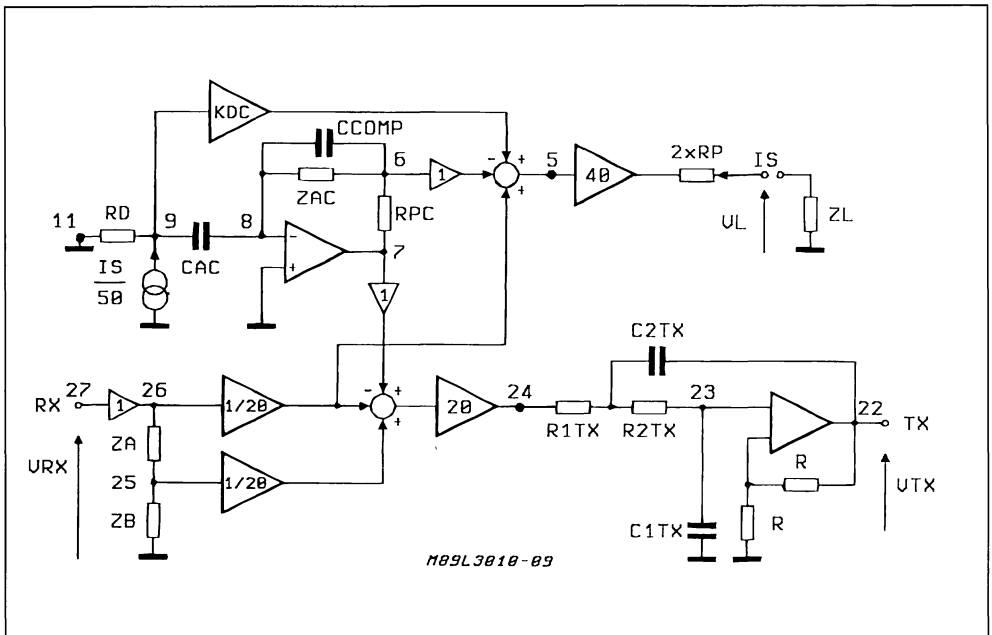
Figure 2.2 : L3000/L3010 DC Characteristic.
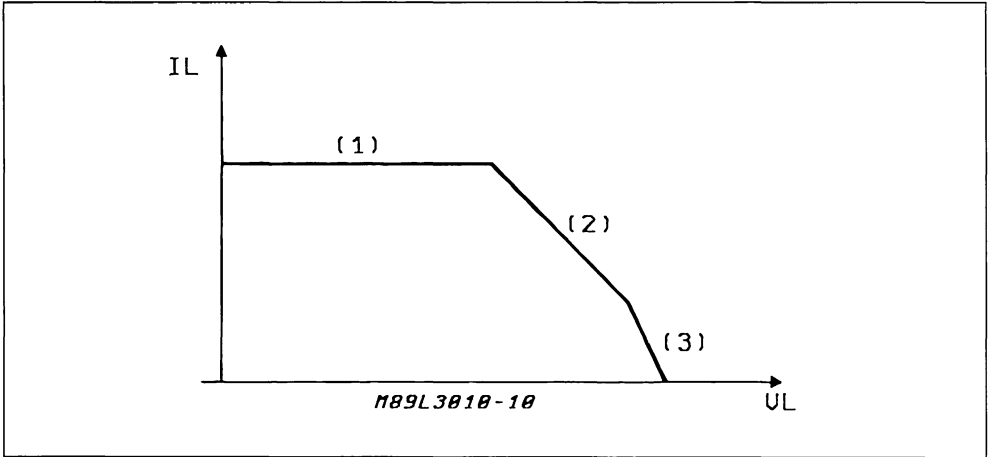
The RD and KDC values depends on the working point on DC characteristic, in particular :

RD = infinite ; KDC = 2   for region 1

RD = RDC ; KDC = 2   for region 2

RD = RDC ; KDC = 2/3   for region 3

CAC is a large capacitor (typ. 22µF) used to split AC and DC components of line current.

CCOMP is a small capacitor (typ. 8.2nF) used to guarantee loop stability.

CAC and CCOMP values are chosen in order to have a neglectible effect on speech band signals, therefore supposing CCOMP equivalent to an open circuit and CAC to a short circuit the following relationships can be easily obtained from the circuit diagram of fig. 2.1. Also the TTX filter influence in speech band is neglected.

2.1. SLIC IMPEDANCE AT LINE TERMINATIONS :

$$ZML = \frac{V_L}{I_S}\Bigg|_{V_{RX}=0} = (4/5) \times ZAC + 2 \times RP$$

2.2. RECEIVING GAIN :

$$G_R = \frac{V_L}{V_{RX}} = 2 \times \frac{ZL}{ZL + ZML}$$

therefore if ZL = ZML

$$G_R = 1$$

2.3. SENDING GAIN

$$G_S = \frac{V_{TX}}{V_L}\Bigg|_{V_{RX}=0} = -\frac{ZAC + RPC}{ZAC + (5/2) \times RP}$$

therefore if RPC = (5/2) x RP

$$G_S = -1$$

2.4. TRANS-HYBRID LOSS

$$THL = \frac{V_{TX}}{V_{RX}} = 2 \times \left(\frac{ZB}{ZA + ZB} - \frac{ZL + 2 \times RP - (4/5) \times RPC}{ZL + ZML}\right)$$

therefore if RPC = (5/2) x RP and ZA/ZB = ZML/ZL

$$THL = 0$$

If you need a more careful evaluation of AC performances you can include also the effect of CCOMP, CAC and TTX filter in the above relations or you can simulate the system behavior with SPICE or other circuit simulators (see example at par. 6).

3. L3000/L3030 SLIC KIT BASIC STRUCTURE

Here below you can see the basic structure of the L3000/L3030 SLIC KIT concerning AC performances.

For an easier representation the high voltage part is drawn as a single ended amplifier with a gain of 40. Close to each node is written the corresponding pin number of L3030 in PLCC package. The components names are the same used in the data sheet.

As you can see on the L3000/L3030 data sheet the large AC/DC splitting capacitor (typ. 22µF) can be avoided using the on chip capacitor multiplier. In the following you can see the basic structure in both cases.

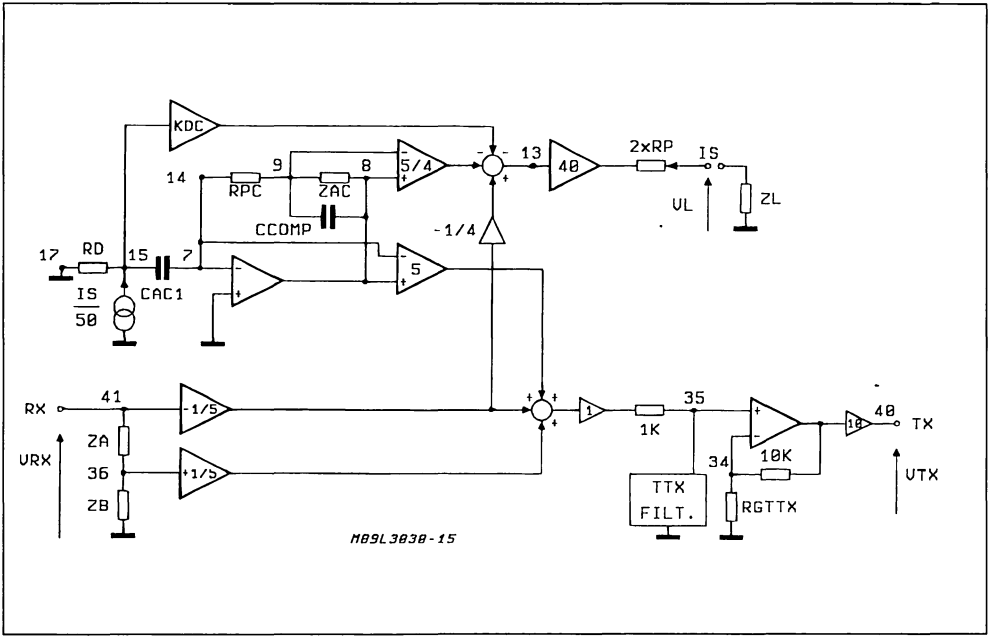**Figure 3.1 :** L3000/L3030 SLIC Configured without Capacitor Multiplier Basic Structure.

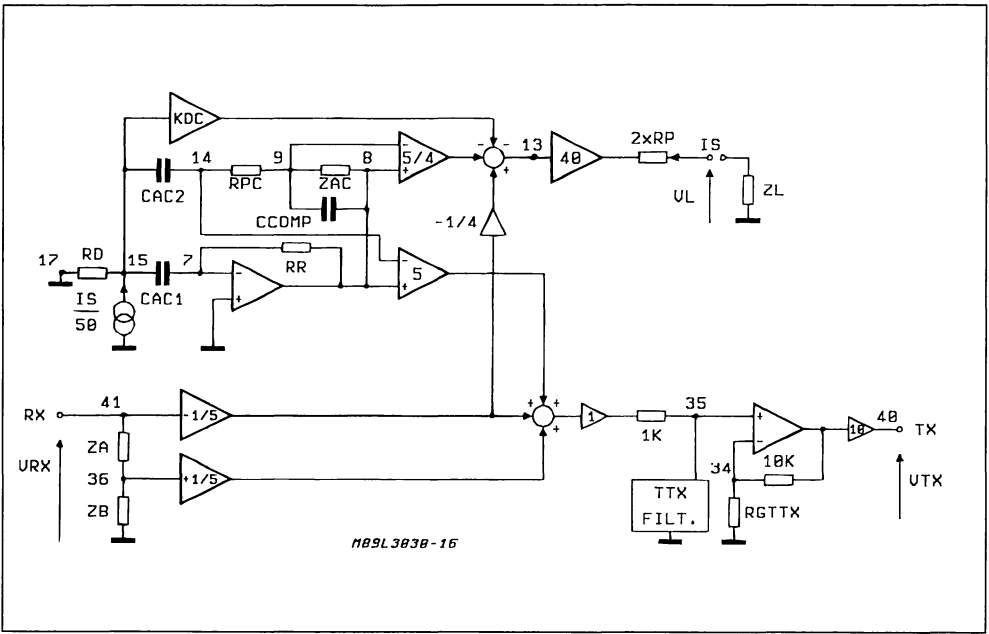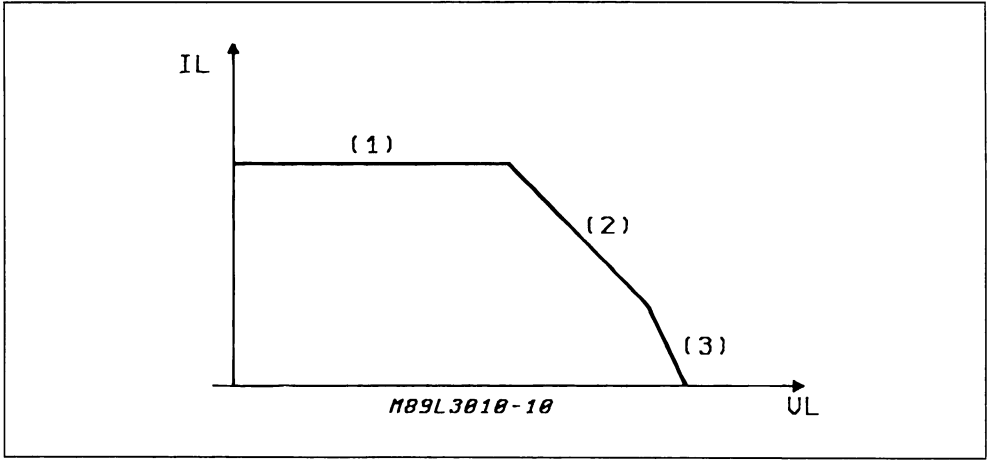**Figure 3.2 :** L3000/L3030 SLIC Configured with Capacitor Multiplier Basic Structure.
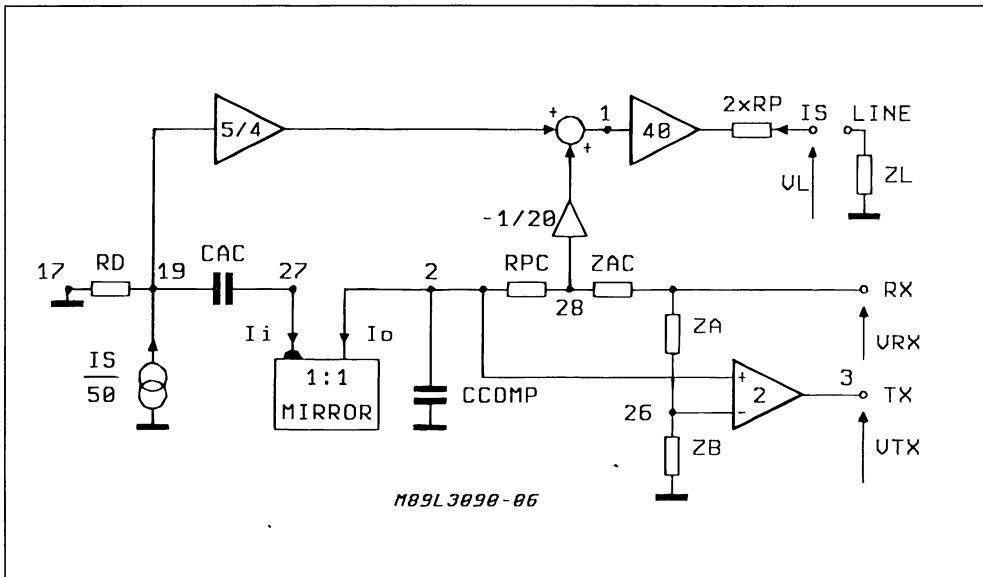
SGS-THOMSON
MICROELECTRONICS

Figure 3.3 : L3000/L3030 DC Characteristic.

The RD and KDC values depends on the working point on DC characteristic, in particular :

RD = infinite ; KDC = 5/4   for region 1

RD = RDC ; KDC = 5/4   for region 2

RD = RDC ; KDC = 5/12   for region 3

CAC1 or the sinthetized capacitor obtained with the capacitor multiplier is relatively large (typ. 22μF) and it is used to split AC and DC components of line current.

CCOMP is a small capacitor (typ. 10nF) used to guarantee loop stability.

CAC1, CAC2 and CCOMP values are chosen in order to have a neglectible effect on speech band signals, therefore supposing CCOMP equivalent to an open circuit and CAC1 or the sinthetized capacitor obtained with the capacitor multiplier equivalent to a short circuit the following relationships can be easily obtained from the circuit diagram of fig. 3.1. Also the TTX filter influence in speech band is neglected. The TTX filter impedance is supposed to be equal to RGTTX/10 in speech band and zero at the TTX frequency.

3.1. SLIC IMPEDANCE AT LINE TERMINATIONS :

$$ZML = \left. \frac{V_L}{I_S} \right|_{VRX = 0} = ZAC + 2 \times RP$$

3.2. RECEIVING GAIN :

$$G_R = \frac{V_L}{V_{RX}} = 2 \times \frac{ZL}{ZL + ZML}$$

therefore if ZL = ZML

$$G_R = 1$$

3.3. SENDING GAIN

$$G_S = \left. \frac{V_{TX}}{V_L} \right|_{VRX = 0} = - \frac{ZAC + RPC}{ZAC + 2 \times RP}$$

therefore if RPC = 2 x RP

$$G_S = -1$$

3.4. TRANS-HYBRID LOSS

$$THL = \frac{V_{TX}}{V_{RX}} = 2 \times \left(\frac{ZB}{ZA + ZB} - \frac{ZL + 2 \times RP - RPC}{ZL + ZML} \right)$$

therefore if RPC = 2 x RP and ZA/ZB = ZML/ZL

THL = 0

If you need a more careful evaluation of AC performances you can include also the effect of CCOMP, CAC and TTX filter in the above relations or you can simulate the system behavior with SPICE or other circuit simulators (see example at par. 6).

4. L3000/L3090 SLIC KIT BASIC STRUCTURE

Here below you can see the basic structure of the L3000/L3090 SLIC KIT concerning AC performances.

For an easier representation the high voltage part is drawn as a single ended amplifier with a gain of 40. Close to each node is written the corresponding pin number of L3090. The components names are the same used in the data sheet.

SGS-THOMSON
MICROELECTRONICS

Figure 4.1 : L3000/L3090 SLIC Basic Structure.

Figure 4.2 : L3000/L3090 DC Characteristic.

![SGS-THOMSON MICROELECTRONICS]
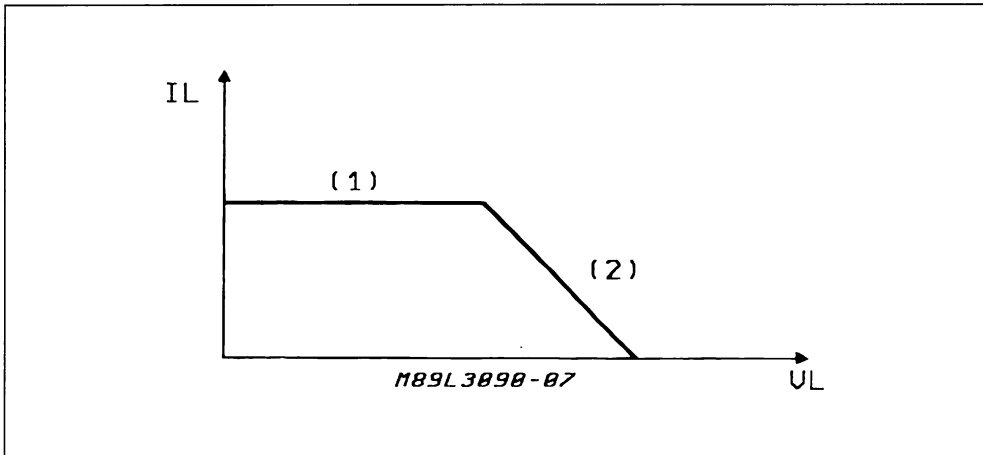
The RD value depends on the working point on DC characteristic, in particular :

RD = infinite　　　　　　　　for region 1

RD = RDC　　　　　　　　　for region 2

CAC is a large capacitor (typ. 47µF) used to split AC and DC components of line current.

CCOMP is a small capacitor (typ. 390pF) used to guarantee loop stability.

CAC and CCOMP values are chosen in order to have a neglectible effect on speech band signals, therefore supposing CCOMP equivalent to an open circuit and CAC to a short circuit the following relationships can be easily obtained from the circuit diagram of fig. 4.1.

4.1. SLIC IMPEDANCE AT LINE TERMINATIONS :

$$ZML = \frac{V_L}{I_S}\bigg|_{V_{RX}=0} = (ZAC/25) + 2 \times RP$$

4.2. RECEIVING GAIN :

$$G_R = \frac{V_L}{V_{RX}} = -2 \times \frac{ZL}{ZL + ZML}$$

therefore if ZL = ZML

$$G_R = -1$$

4.3. SENDING GAIN

$$G_S = \frac{V_{TX}}{V_L}\bigg|_{V_{RX}=0} = -\frac{ZAC + RPC}{ZAC + 25 \times (2 \times RP)}$$

therefore if RPC = 25 x (2 x RP)

$$G_S = -1$$

4.4. TRANS-HYBRID LOSS

$$THL = \frac{V_{TX}}{V_{RX}} = 2 \times \left(\frac{ZL + 2 \times RP - (RPC/25)}{ZL+ZML} - \frac{ZB}{ZA+ZB}\right)$$

therefore if RPC = 25 (2 x RP) and ZA/ZB = ZML/ZL

$$THL = 0$$

If you need a more careful evaluation of AC performances you can include also the effect of CCOMP and CAC in the above relations or you can simulate the system behavior with SPICE or other circuit simulators (see example at par. 6).

5. TDB7722/TDB7711 SLIC KIT BASIC STRUCTURE

Here below you can see the basic structure of the TDB7722/TDB7711 SLIC KIT concerning AC performances.

For an easier representation the high voltage part is drawn as a single ended amplifier with a gain of 40. Close to each node is written the corresponding pin number of TDB7711. The components names are the same used in the data sheet.

Figure 5.1 : TDB7722/TDB7711 SLIC Basic Structure.
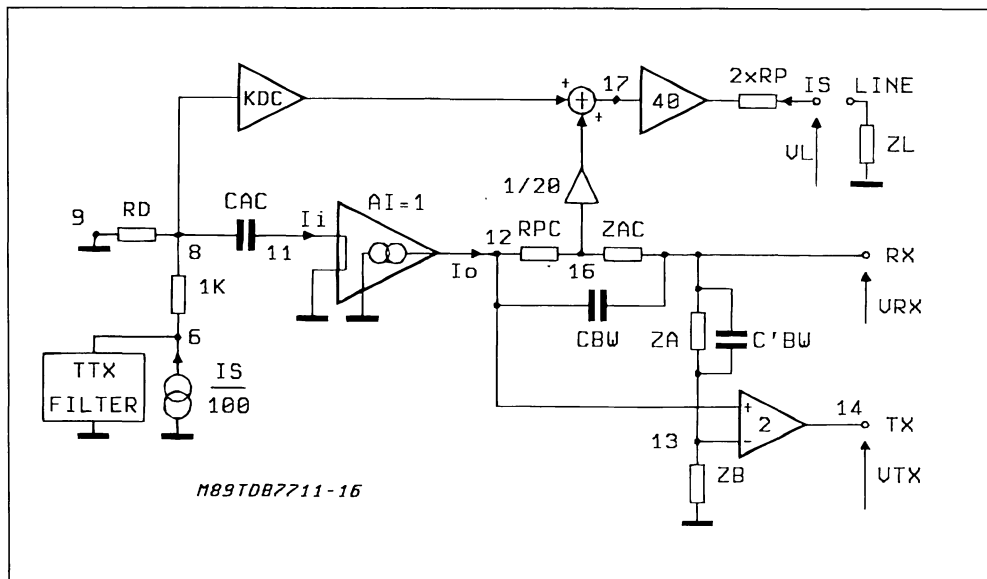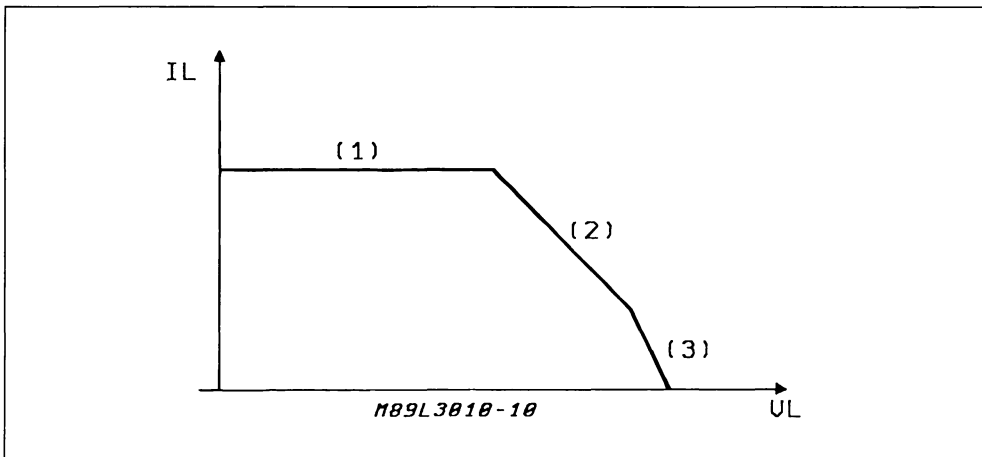
SGS-THOMSON
MICROELECTRONICS

Figure 5.2 : TDB7722/TDB7711 DC Characteristic.

The RD and KDC values depends on the working point on DC characteristic, in particular :

RD = infinite ; KDC = 5/4   for region 1

RD = RDC ; KDC = 5/4   for region 2

RD = RDC ; KDC = 0   for region 3

CAC is a large capacitor (typ. 47μF) used to split AC and DC components of line current.

CBW and C'BW are small capacitors (typ. 270pF and 120pF) used to guarantee loop stability and good THL performances.

CAC, CBW and C'BW values are chosen in order to have a neglectible effect on speech band signals, therefore supposing CBW equivalent to an open circuit and CAC to a short circuit the following relationships can be easily obtained from the circuit diagram of fig. 5.1. Also the TTX filter influence in speech band is neglected ; the TTX filter impedance is supposed to be very high in speech band and zero at the TTX frequency.

5.1. SLIC IMPEDANCE AT LINE TERMINATIONS :

$$ZML = \frac{V_L}{I_S}\bigg|_{V_{RX}=0} = (ZAC/50) + 2 \times RP$$

5.2. RECEIVING GAIN :

$$G_R = \frac{V_L}{V_{RX}} = 2 \times \frac{ZL}{ZL+ZML}$$

therefore if ZL = ZML

$$G_R = 1$$

5.3. SENDING GAIN

$$G_S = \frac{V_{TX}}{V_L}\bigg|_{V_{RX}=0} = \frac{ZAC + RPC}{ZAC + (100 \times RP)}$$

therefore if RPC = 100 x RP

$$G_S = 1$$

5.4. TRANS-HYBRID LOSS

$$THL = \frac{V_{TX}}{V_{RX}} = 2 \times \left(\frac{ZL + 2 \times RP - (RPC/50)}{ZL + ZML} - \frac{ZB}{ZA + ZB} \right)$$

therefore if RPC = 100 x RP and ZA/ZB = ZML/ZL

THL = 0

If you need a more careful evaluation of AC performances you can include also the effect of CBW, CAC and TTX filter in the above relations or you can simulate the system behavior with SPICE or other circuit simulators (see example at par. 6).

It should be noted that even if the CBW capacitor is relatively small it could have some effect on the return loss performances (anyway always within the specs.) at the higer frequencies. In order to obtain better return loss performances the CBW effect should be considered when the ZAC impedance is selected.

If for example the German return loss impedance (220Ω +(820Ω//115nF)) is requested supposing RP = 30Ω it should be : ZAC = 8K + (41K//2.3nF) as described in par. 5.1. If you look at the structure shown in fig. 5.1. you can see that CBW can be considered in parallel with ZAC therefore better return loss performances can be obtained considering the effect of CBW on ZAC. If you consider again the case of German network it shoul be : ZAC = 8K + (41K//2.0nF) supposing CBW about 300pF.

6. ONE EXAMPLE OF SPICE SIMULATION WITH L3000/L3090 SLIC KIT

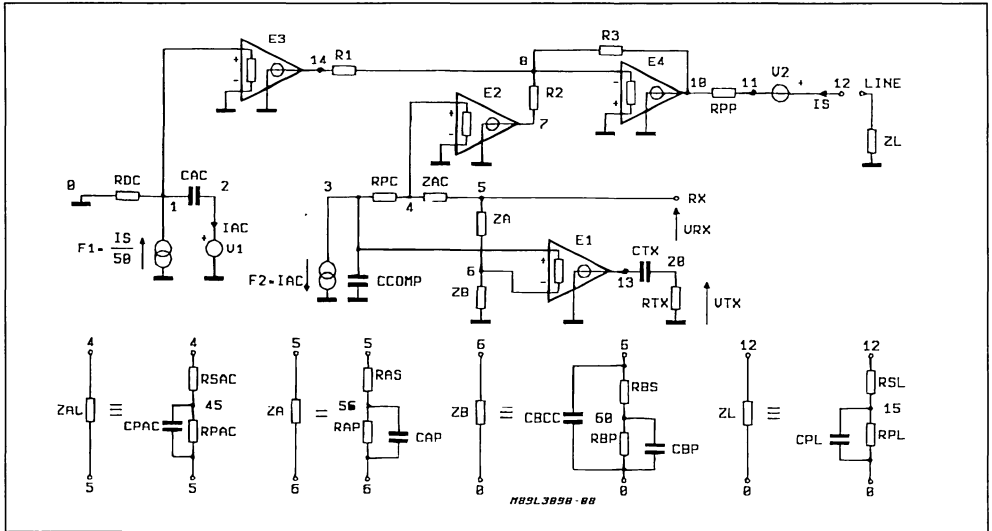**Figure 6.1 :** Circuit Diagram for L3000/L3090 SLIC KIT Spice Simulation.

Figure 6.2 : Network for RL Evaluation ; ZRL = Return Loss Test Impedance.
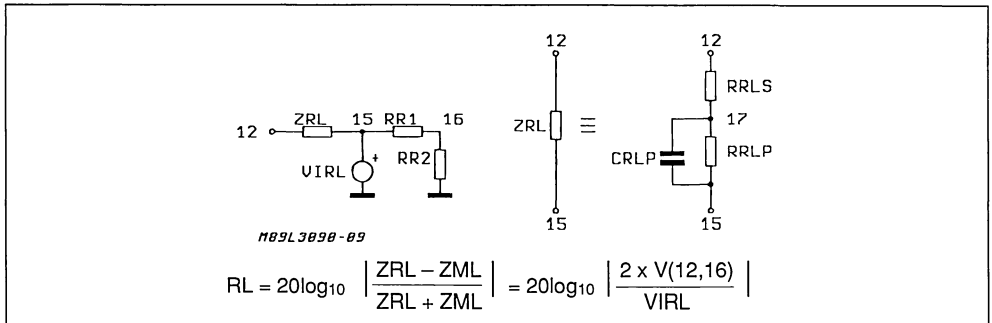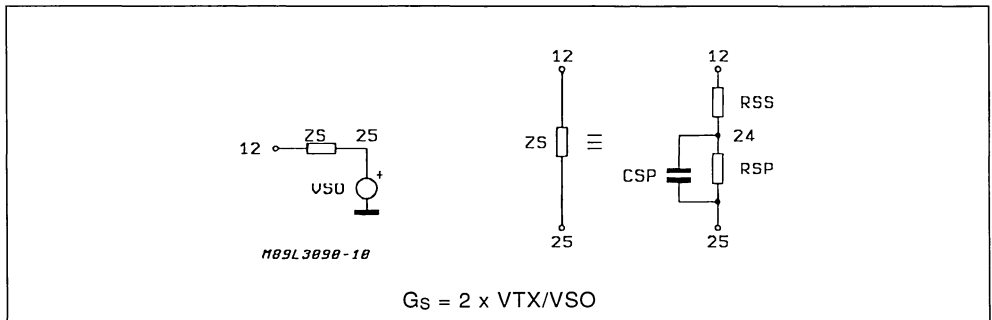

$$RL = 20\log_{10}\left|\frac{ZRL - ZML}{ZRL + ZML}\right| = 20\log_{10}\left|\frac{2 \times V(12,16)}{VIRL}\right|$$

Figure 6.3 : Network for TX Gain Evaluation with Sending Generator Series Impedance Equal to ZS.

$$G_S = 2 \times VTX/VSO$$

SPICE INPUT FILE FOR L3000/L3090 SLIC KIT SIMULATION

L3090 AC ANALYSIS

```
************** CIRCUIT CONFIGURATION USED ************************
*  PROT. RES. 2 x 50Ω → RPP = 100Ω ; RPC = 2.5 KΩ          *
*  FEEDING RES. 2 x 200Ω → RDC = 300Ω                      *
*  AC LINE IMPEDANCE 600Ω → RZAC = 12.5 KΩ                 *
*  (SAME CONFIGURATION OF L3000/L3090 TEST CIRCUIT)        *
**********************************************************************

************** EXTERNAL COMPONENTS *******************************

RPC 3 4 2.5K
RSAC 4 45.5K
RPAC 45 5 12K
*CPAC 45 5 1P
RAS 5 56 6K
RAP 56 6 6K
*CAP 56 6 1P
RBS 6 60 6K
RBP 60 0 6K
*CBP 60 0 1P
CBCC 6 0 470P
RPP 10 11 100
RTX 20 0 1MEG

CAC 1 2 47U
CCOMP 3 0 390P
CTX 13 20 10U

************** END EXT. COMPONENTS *******************************

************** MODEL COMPONENTS ************************************
R1 14 8 1K
R2 7 8 1K
R3 8 10 40K
R4 8 0 10MEG

E1 13 0 3 6 2
E2 7 0 4 0 + . 05
E3 14 0 1 0 − 1.25
E4 10 0 8 0 − 1MEG

V1 2 0
V2 12 11

F1 0 1 V2 .02
F2 3 0 V1 1

.AC LIN 40 100 4K
*.AC DEC 10 10 20K
.WIDTH IN = 80 OUT = 80
```

SGS-THOMSON
MICROELECTRONICS

```
****** INSERT ONLY ONE OF THE FOLLOWING BLOCKS DEPENDING ******
****** ON THE DC CHARACTERISTIC REGION                      ******

****** LIM. CURRENT REGION ******
**** RDC 1 0 10MEG
****** END LIM. REGION **************

****** RES. FEED REGION ***********
**** RDC 1 0 300
****** END RES. REGION *************

****** INSERT ONLY ONE OF THE FOLLOWING BLOCKS DEPENDING ******
****** ON WHICH ANALYSIS YOU WANT                         ******

***** TX GAIN EVALUATION VTX/VL WITH VRX = 0 *****
*VRX 5 0 DC 0
*VL 12 0 AC
*.PRINT AC VDB(20)   VP(20)
*.PLOT AC VDB(20)   VP(20)
*.STORE AC VDB(20)   VP(20)
***** END TX GAIN ***************************************

** TX GAIN EVALUATION 2VTX/VSO WITH VRX= 0 **
** (SERIES IMP. OF SENDING GENERATOR = ZS)
*VRX 5 0 DC 0
*VSO 25 0 AC 2
*RSS 24 12 300
*RSP 24 25 300
**CSP 24 25 1P
*.PRINT AC VDB(20)   VP(20)
*.PLOT AC VDB(20)   VP(20)
*.STORE AC VDB(20)   VP(20)
***** END TX GAIN ***************************************

** RX GAIN EVALUATION VL/VRX ***********************
*RSL 12 15 300
*RPL 15 0 300
**CPL 15 0 1P
*VRX 5 0 AC
*.PRINT AC VDB(12)   VP(12)
*.PLOT AC VDB(12)   VP(12)
*.STORE AC VDB(12)   VP(12)
***** END RX GAIN **************************************

** THL EVALUATION VTX/VRX ***************************
*RSL 12 15 300
*RPL 15 0 300
**CPL 15 0 1P
*VRX 5 0 AC
*.PRINT AC VDB(20)   VP(20)
*.PLOT AC VDB(20)   VP(20)
*.STORE AC VDB(20)   VP(20)
***** END THL EVALUATION ****************************
```

```
*** RETURN LOSS EVALUATION **************************
*VRX 5 0 DC 0
*VIRL 15 0 AC 2
*RCS 12 17 300
*RCP 17 15 300
**.CCP 17 15 1P
*RR1 15 16 1K
*RR2 16 0 1K
*.PRINT AC VDB(12.16)
*.PLOT AC VDB(12.16)
*.STORE AC VDB(12.16)
***** END RETURN LOSS EVALUATION ******************

*** INPUT IMPEDANCE EVAL. AT LINE TERMINALS ***
*VRX 5 0 DC 0
*IL 0 12 AC
*.PRINT AC VM(12)   VP(12)
*.PLOT AC VM(12)   VP(12)
*.STORE AC VM(12)   VP(12)
***** END INP. IMPED. EVALUATION **********************


.END
```

SGS-THOMSON
MICROELECTRONICS

EMI TEST EVALUATION WITH L3000/L3090 SLIC KIT

PRELIMINARY RESULTS

INTRODUCTION

EMI test were performed on SGS-THOMSON L3000/L3090 SLIC KIT using the same test circuit described in FTZ specs (12 TR1 Teil 21).

In order to cut high frequencies two capacitors (C_{RF}) were connected respectively between TIP and GND and RING and GND (no coils needed!).

The measurements were performed in the range of 10KHz to 8MHz giving good results. The same behavior is expected for higher frequencies with a proper layout and good H.F. filtering capacitors.

Laboratory activity is going on about this subject ; further informations will be available in the next months.

MEASUREMENTS RESULTS

Referring to the test procedure described in the FTZ specs an amplitude modulated signal (m = 0.8 ; f = 1kHz) was applied at TIP/RING termination ; the amplitude of this signal was 1.5Vrms from 10KHz to 100KHz and 3Vrms from 100KHz to 8MHz.

The signal at TX output was measured after a psophometric filter ; this signal was always below 1mVrms as required (see fig. 1). In fig. 1 is also represented the H.F. rejection of the device itself (without filtering capacitors C_{RF}). The good behavior of

the device itself at relatively low frequencies allow us to use smaller values for the C_{RF} capacitor reducing in this way also their influence in speech band.

AC PERFORMANCES

In fig. 2 is shown the SLIC circuit diagram with the two CRF capacitor. Of course these capacitors should produce some effects on the AC performances of the device. Anyway, thanks to the architecture of the L3000/L3090 SLIC KIT these effects can be very well compensated modifying properly the SLIC output impedance and the position of the compensation capacitor for the SLIC loop stability. In fig. 2 these modifications are already present. External components are selected in order to satisfy German requirements. Fig. 3 to 6 shown the AC performances measured with the SLIC configuration represented in fig. 2.

CONCLUSIONS

Using L3000/L3090 SLIC KIT it is possible to satisfy the FTZ requirements as described above simply using two 18nF capacitors, no coils are needed !

The eventual AC performances distortions can be compensated acting on the external components (see fig. 3 to 6).
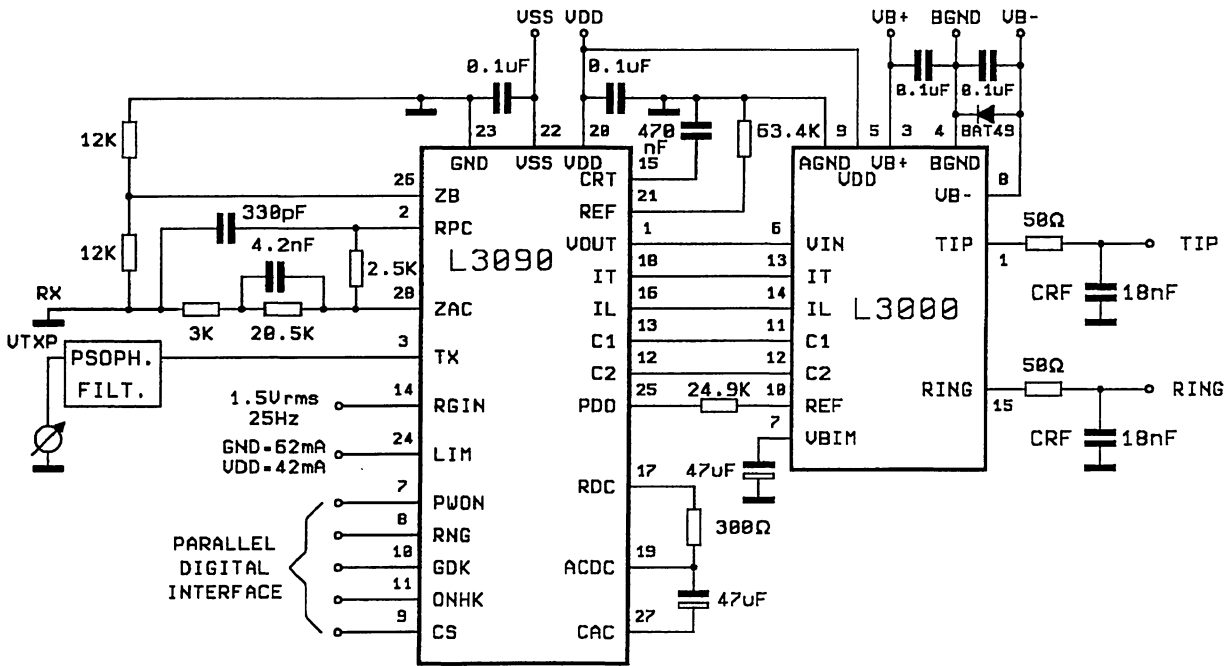
Figure 1 : L3000/L3090 EMI Measurements.

L3000/3090 EMI measurements
Test circuit: see FTZ 12 TR1 Teil 21
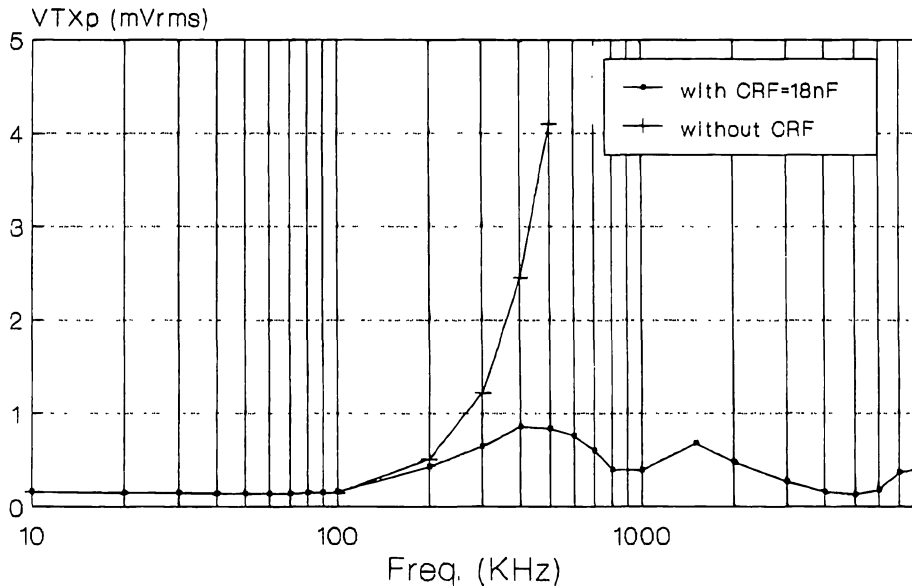
ST TELECOM APPLICATION LAB. - FEB. 89

SGS-THOMSON MICROELECTRONICS

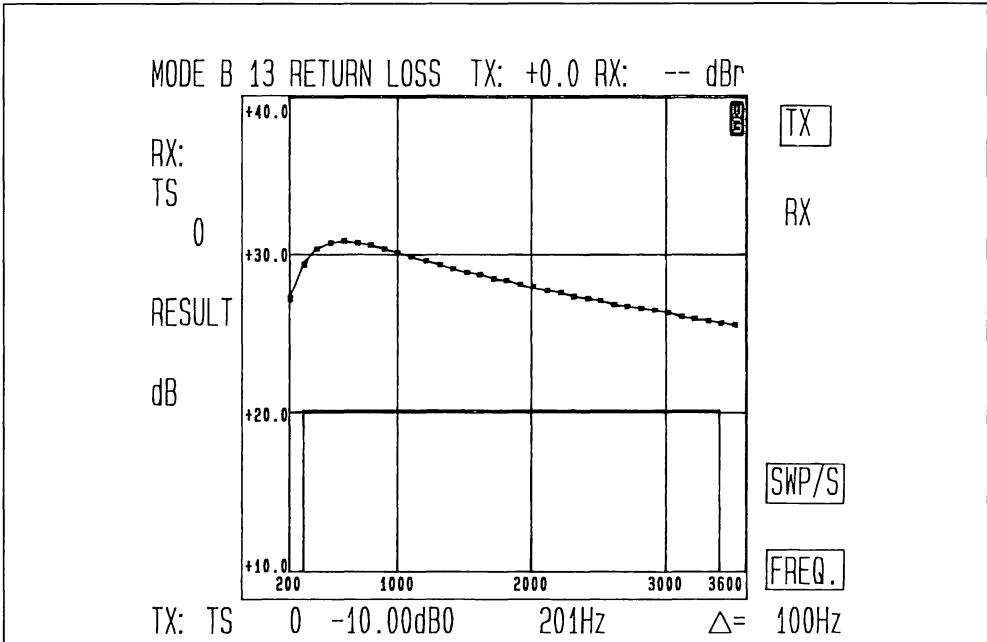**Figure 2 :** L3000/L3090 Circuit Arrangement for EMI Rejection.

M89L3090-11

Figure 3 : Return Loss Performances.

W & G PCM-4			20. FEB. 89 12 : 14
RETURN LOSS		TX	
B 13		TX : + 0.0dBr RX : -- dBr	
	PRINT MAN RESULTS		

TX-TSLOT	RX-TSLOT		
0	0	Level – 10.00dB0	

Freq./Hz	Result/dB	Freq./Hz	Result/dB
201	+ 27.17	301	+ 29.35
402	+ 30.35	502	+ 30.79
602	+ 30.89	703	+ 30.79
803	+ 30.61	903	+ 30.38
1004	+ 30.14	1104	+ 29.88
1205	+ 29.64	1305	+ 29.39
1405	+ 29.15	1506	+ 28.92
1606	+ 28.70	1706	+ 28.50
1807	+ 28.30	1907	+ 28.11
2008	+ 27.92	2108	+ 27.73
2208	+ 27.56	2309	+ 27.39
2409	+ 27.22	2509	+ 27.06
2610	+ 26.90	2710	+ 26.74
2811	+ 26.59	2911	+ 26.44
3011	+ 26.29	3112	+ 26.14
3212	+ 26.00	3312	+ 25.85
3413	+ 25.71	3513	+ 25.56

SGS-THOMSON
MICROELECTRONICS

Figure 4 : Tx Gain Flatness.


```
MODE A 34 VAR.GAIN/FRE.TX: +0.0 RX: +0.0dBr
```

RX:
TS
0

RESULT

dB

A-A
A-D
D-A
D-D
SWP/S
FREQ.

TX: TS   0   -10.00dB0   201Hz   △= 100Hz

W & G PCM-4			20. FEB. 89 12 : 28
VAR. OF GAIN WITH FREQUENCY		A-A	4-wire
A 34		TX : + 0.0dBr	RX : + 0.0dBr
	PRINT MAN RESULTS	Ri : cplx	Re : 30kΩ

TX-TSLOT   RX-TSLOT
   0   0   Level – 10.00dB0

Freq./Hz	Result/dB	Freq./Hz	Result/dB
201	+ 0.05	301	+ 0.07
402	+ 0.05	502	+ 0.05
602	+ 0.05	703	+ 0.04
803	+ 0.03	903	+ 0.02
1004	+ 0.00	1104	− 0.01
1205	− 0.02	1305	− 0.02
1405	− 0.04	1506	− 0.05
1606	− 0.06	1706	− 0.06
1807	− 0.07	1907	− 0.08
2008	− 0.08	2108	− 0.10
2208	− 0.10	2309	− 0.11
2409	− 0.12	2509	− 0.13
2610	− 0.14	2710	− 0.15
2811	− 0.16	2911	− 0.17
3011	− 0.18	3112	− 0.18
3212	− 0.19	3312	− 0.19
3413	− 0.20	3513	− 0.21

Figure 5 : Rx Gain Flatness.

W & G PCM-4			20. FEB. 89 12 : 34	
VAR. OF GAIN WITH FREQUENCY		A-A	4-wire	
A 34		TX : + 0.0dBr	RX : + 0.0dBr	
PRINT MAN RESULTS		Ri : 600Ω	Re : cplx	

TX-TSLOT	RX-TSLOT			
0	0	Level – 10.00dB0		
Freq./Hz	Result/dB	Freq./Hz	Result/dB
---	---	---	---
201	+ 0.05	301	+ 0.08
402	+ 0.06	502	+ 0.06
602	+ 0.06	703	+ 0.05
803	+ 0.03	903	+ 0.02
1004	+ 0.00	1104	− 0.01
1205	− 0.02	1305	− 0.04
1405	− 0.05	1506	− 0.07
1606	− 0.08	1706	− 0.09
1807	− 0.10	1907	− 0.11
2008	− 0.11	2108	− 0.13
2208	− 0.14	2309	− 0.14
2409	− 0.15	2509	− 0.17
2610	− 0.18	2710	− 0.19
2811	− 0.20	2911	− 0.20
3011	− 0.20	3112	− 0.21
3212	− 0.22	3312	− 0.22
3413	− 0.23	3513	− 0.23

SGS-THOMSON
MICROELECTRONICS

Figure 6 : THL Performances.

MODE A 11 LEVEL MEAS.   TX: +0.0 RX: +0.0dBr

RX:
TS
  0

RESULT

dB0

A-A

A-D

D-A

D-D

SWP/S

FREQ.

TX: TS   0 +0.00 dB0   201Hz   △= 100Hz

W & G PCM-4		20. FEB. 89 12 : 42	
LEVEL MEASUREMENT		**A-A**	**4-wire**
A 11		**TX : + 0.0dBr**	**RX : + 0.0dBr**
	PRINT MAN RESULTS	**Ri : 600Ω**	**Re : 30kΩ**

TX-TSLOT	**RX-TSLOT**		
0	**0**	**Level + 0.00dB0**	
Freq./Hz	**Result/dB0**	**Freq./Hz**	**Result/dB0**
201	− 31.62	301	− 33.13
402	− 33.61	502	− 33.57
602	− 33.31	703	− 32.96
803	− 32.57	903	− 32.18
1004	− 31.82	1104	− 31.46
1205	− 31.13	1305	− 30.83
1405	− 30.54	1506	− 30.29
1606	− 30.05	1706	− 29.84
1807	− 29.63	1907	− 29.44
2008	− 29.27	2108	− 29.10
2208	− 28.95	2309	− 28.80
2409	− 28.67	2509	− 28.54
2610	− 28.42	2710	− 28.30
2811	− 28.19	2911	− 28.08
3011	− 27.98	3112	− 27.87
3212	− 27.78	3312	− 27.68
3413	− 27.59	3513	− 27.50

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

SLIC L3000/L3090
MAXIMUM LOOP RESISTANCE ANALYSIS

By W. Rossi

1. INTRODUCTION

This evaluation was carried out in order to evaluate the maximum loop resistance allowed using the SLIC KIT L3000/L3090, the best for PABX applications.

The evaluation is performed in conversation mode ; it shows how the maximum loop resistance (Rl) is influenced by the battery voltage (Vb), the feeding resistance (Rfs) and the common mode current (Icm).

Figure 1 : SLIC Characteristic and Load Curve.

2. MAXIMUM LOOP RESISTANCE EVALUATION

In fig. 1 you can see the L3090 DC characteristic and the load curve. The load curve is obtained as the series of the loop resistance (Rl) and the subscriber telephone set. The subscriber telephone set is represented as the series of a 100Ω resistor and a 5V zener diode.
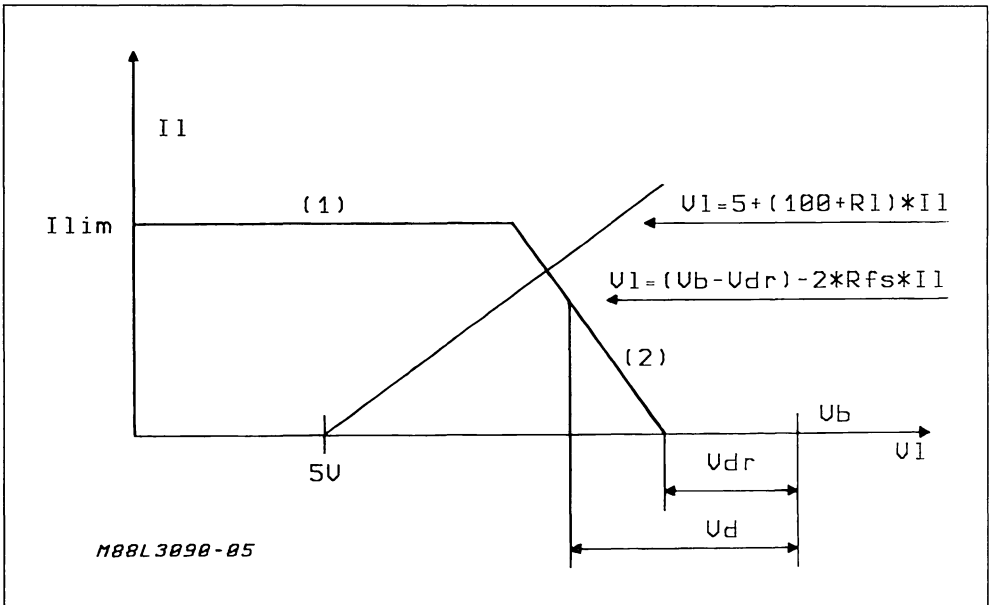
If the operating point is on region (1) its coordinates are :

$Il1 = Ilim$

$Vl1 = 5 + (100+Rl) \times Ilim$ (1)

Note : The slope of region (2) is 2xRfs where the feeding resistor Rfs is fixed by an external resistor.

If the operating point is on region (2) you can find its coordinates solving the system of two equations :

1) $Vl = (Vb-Vdr)-2 \times Rfs \times Il$

2) $Vl = 5+(100+Rl) \times Il$

obtaining :

$Il2 = (Vb-Vdr-5)/(100+Rl+2 \times Rfs)$

$Vl2 = 5+(100+Rl) \times (Vb-Vdr-5)/(100+Rl+2 \times Rfs)$ (2)

If you consider the DC characteristic of the device you can see that the longer is the line the lower is the voltage drop between the battery voltage (Vb)

AN294/01/89

1/2

and the line voltage (Vl). It can happens that for very long line the voltage drop is not large enough to guarantee the fully AC performance of the device. In such condition the device is still working, but large signal can appear slightly distorted on the line. If you want guarantee the optimum behavior of the device you must be sure that the operating point of the device (Il, Vl) satisfy the following condition :

$Vl \leq Vb-Vd$

with $Vd=5+100 \times Il+60 \times Il+2+Vdcm$

where :

5 : internal drop

$100 \times Il$: drop on sensing resistors ($2 \times 50\Omega$ max)

$60 \times Il$: drop on external resistors ($2 \times 30\Omega$)

2 : maximum AC signal peak

Vdcm : (=$100 \times Icm$) drop for common mode current (Icm)

You can obtain the maximum value for Rl (maximum loop length) imposing :

$Vl = Vb-Vd$

If the operating point is on region (1) solving the equation Vl1=Vb-Vd where Vl1 is given by the relation (1) you obtain :

$Rlmax= (Vb-12-260 \times Ilim-100 \times Icm)/Ilim$ (3)

If the operating point is on region (2) solving the equation Vl2=Vb-Vd where Vl2 is given by the relation (2) you obtain :

$Rlmax = ((100+2 \times Rfs) \times (Vb-12-100 \times Icm)-260 \times (Vb-Vdr-5))/(7-Vdr+100 \times Icm)$

In the following you can find graphical representations of Rlmax versus Icm in four different situations :

3. CONCLUSION

The above relations show the possibility to work with good performances also in presence of common mode current. With a battery voltage of −48V, Rfs = 200Ω and no common mode current, the maximum loop resistance is over 3KΩ ; in the same condition but with a common mode current of 20mA the maximum loop resistance is about 2KΩ. Higher loop resistance can be obtained increasing Rfs (see fig. 2).

The parameters of each curve are the battery voltage (Vb) and the feeding resistance (Rfs).

Figure 2 : Maximum Line Resistance Versus Common Mode Current (conversation mode).

SGS-THOMSON
MICROELECTRONICS

APPLICATION NOTE
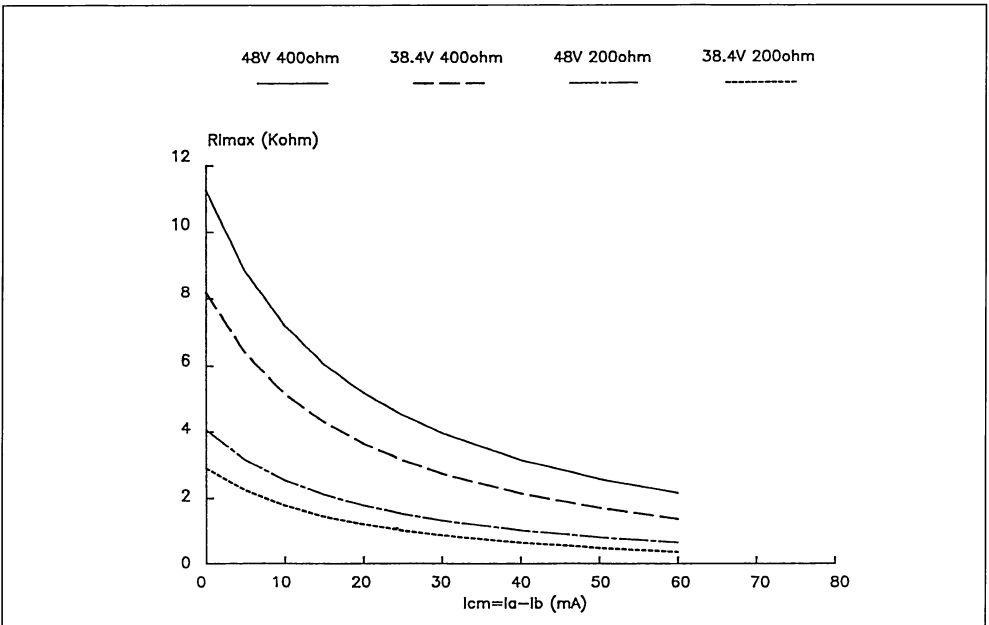
SLIC L3000/L3090
PERFORMANCE ANALYSIS WITH −24V BATTERY

By W. Rossi

1. INTRODUCTION

This technical note describes the L3000/L3090 SLIC performances when used with a battery voltage of − 24V. All the main characteristics are analyzed and compared with the results obtained with a standard battery voltage of − 48V.

The following data were obtained from a typical device in order to have an idea on how DC characteristic, power consumption, ringing voltage and AC performances are influenced by a reduced battery voltage.

2. POWER CONSUMPTION

Table 2.1 shows the L3000-L3090 current consumption with the battery voltage of − 48V and − 24V. The measurements are made in the different operating modes (Power Down ; Stand-By ; Conversation with IL = 0 ; IL = 44mA and Ringing without AC Line Load (Ringing Equivalent Number REN = 0).

Table 2.1 : Slic Current Consumption with Different Battery Voltages.

	Current Consumption (mA)			
	− 48V	+ 72V	− 24V	+ 72V
PW - DOWN	0	0	0	0
SBY (IL = 0)	3.3	0	3.1	0
CVS (IL = 0)	10.6	0	9.7	0
CVS (IL = 44mA)	61.1	0	60.9	0
RING (0 REN)	23.9	15.4	21.8	13.4

You can see that using − 24V of battery voltage we have a reduction of the power consumption of more than 50% in STD-BY and CVS and of about 35% in RING mode.

3. DC CHARACTERISTICS

In fig. 3.1. you can see the typical DC characteristics for the two battery voltages ; feeding resistance was set to 2x200Ω.

3.1. MAXIMUM LOOP LENGHT

Two are the parameters influenced by line length increment : the first is the DC line current and the second is the maximum AC signal that can be sent without distortion (THD 1%), see AN294. Here below are shown the maximum loop resistance values and the relative line current in correspondance of which distortion is still less than 1% for +4dBm (1.23 VRMS) AC signals. The SLIC feeding resistance is set to 2 x 200Ω.

Vbatt. = − 48V   Vbatt. = − 24V

Rmax. = 2200Ω   Rmax. = 940Ω

IL = 16.61mA   IL = 14.47mA.

3.2. ON/OFF HOOK CURRENT THRESHOLDS

Here below are reported the typical values of the DC current thresholds used by the SLIC to detect the ON hook and OFF hook line conditions.

Vbatt. = − 48V

ON/OFF Hook commutation.

IL = 8.10mA VL = 40.58V RL = 5KΩ

OFF/ON Hook commutation.

IL = 5.91mA VL = 41.30V RL = 7KΩ

Vbatt. = − 24V

ON/OFF Hook commutation.

IL = 8.24mA VL = 16.52V RL = 2KΩ

OFF/ON Hook commutation.

IL = 5.82mA VL = 17.44V RL = 3KΩ

Figure 3.1 : DC Characteristic with a 2 x 200Ω Feeding Resistance.
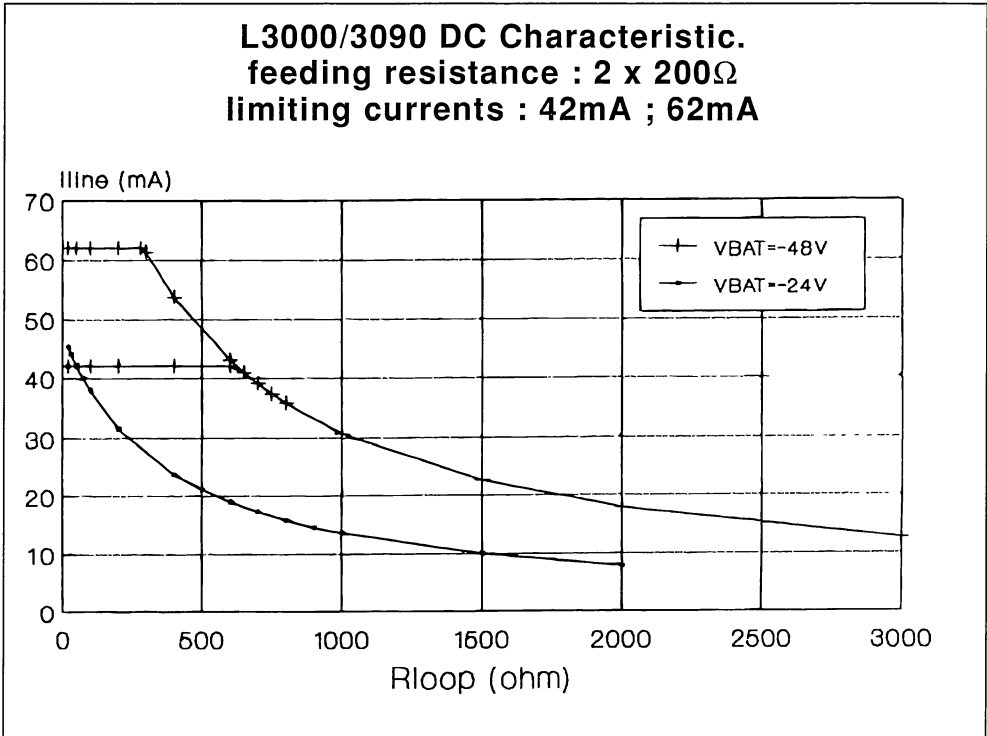
4. AC PERFORMANCES

All the AC performances : TXgain, RX gain, Return Loss, Transhybrid Loss and Longitudinal Balance were measured and no significative variations were found changing from − 48V to − 24V of battery voltage.

GRX, GTX and THL variation were inside .03dB ; RL inside .07dB and longitudinal balance inside .9dB.

5. RINGING PERFORMANCES

L3000/L3090 SLIC injects directly the ringing signal into the line. The ringing signal has a DC component superimposed with the AC one. Here below you can see the measured values of these DC and AC voltages with a positive supply of + 72 and a battery voltage of -48V and -24V.

5.1. DC LEVEL

Vbatt. = − 48V

Vdc = + 21.06V

Vbatt. = − 24V

Vdc = + 17.68V

5.2. MAX AC LEVEL (Volts RMS) WITH A DISTORTION THD < 4%

Vbatt. = − 48V

Vac = 70.58V (RMS)

Vbatt. = − 24V

Vac = 47.30V (RMS)

6. CONCLUSIONS

The measurements carried on show that it is possible to make the SLIC working also with reduced battery voltage (down to − 24V) without any degradation in terms of AC performances.

It should be noted that with − 24V battery voltage you can get good performances up to 950Ω of loop length. In case you need higher line currents you can increase the battery voltage of the amount you need, optimizing in this way power dissipation.

SGS-THOMSON
MICROELECTRONICS

SLIC L3000/L3090
USED IN KEY SYSTEM AND ANALOG PABX

By W. Rossi

1. L3000/L3090 SLIC KIT ; MAIN CHARACTERISTICS :

* Programmable DC feeding resistance and limiting current (two values available).

* Four operating modes (PW-DOWN/SBY/CVS/RNG).

* Signalling function (OFF-HOOK/GND-KEY).

* Hybrid function.

* Possibility to work with reduced battery voltage (- 24V).

* **Possibility to work in two-wire configuration**.

* Ringing generation with quasi zero output impedance, zero crossing injection (no external relay needed) and ring trip detection.

* Automatic ringing stop when OFF-HOOK is detected.

* Parallel latched digital interface (5 pins).

* Low number of standard tolerance external components, only 9 1% resistors and 4 10-20% capacitors (for 600Ω appl.)

* Possibility to work also with high common mode currents.

* Integrated thermal protection.

2. L3090/L3000 INTERNAL STRUCTURE

Here below you can see the simplified internal structure of the L3090/L3000 SLIC KIT and how it is possible to make it working in a two wire configuration. The output stage (L3000) is represented as single ended only to have a simplified model.

- Rac ; R1 ; R2 ; and Rs are external components, can be real or complex and are chosen in order to set the desired AC performances of the system.

- Rp is equal to the sum of the two external series resistor on the line.

- Z2w is the load impedance at the two wire termination and represents the input impedance at the same point of another SLIC in the same configuration.

If you look at fig. 2.1 it is evident that both the transmit and receive signals are present at the 2W point (typical for a two wire configuration). In fact if you suppose to inject a signal in the 2W point it will be transferred to the line through the A amplifier after a partition on the R1 ; R2 network. On the other side if a signal is applied at the line termination it will produce a current Is that scaled by 50 is fed back and injected on Rac, finally through the B amplifier the line signal is transferred at the 2W termination.

Figure 2.1 : L3090/L3000 Simplified AC Model.
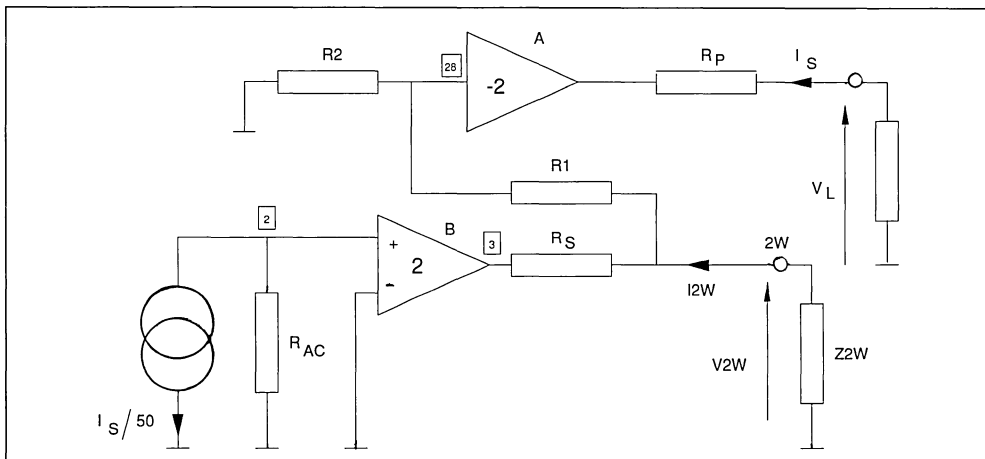
3. HOW TO CHOOSE EXTERNAL COMPONENTS FOR EACH APPLICATION

Analyzing the circuit configuration shown in fig. 2.1

it is possible to obtain all the typical parameters of the system ; in particular, defining

$G = 2 \times R2 / (R1 + R2)$ the results are :

- Z2w defined as V2w/I2w is the input impedance at the two wire termination :

$$Z2w = \cfrac{Rs}{1 + G \times Rac/(25 \times (Rp + Rl))} \tag{1}$$

- Zin defined as Vl/Is is the input impedance at the line termination :

$$Zin = Rp + Rac \times (G/25) \times \cfrac{Z2w}{Rs + Z2w} \tag{2}$$

Substituting the (1) in the (2) you obtain :

$$Zin = Rp + G \times Rac \times \cfrac{Rp + Rl}{50 \times (Rp + Rl) + G \times Rac} \tag{3}$$

- GTX defined as V2w/Vl is the transmit gain and can be evaluated applying Vl at the line termination and measuring V2w :

$$GTX = \cfrac{1}{G \times (1 + (Rp/(Rp + Rl))) + 50 \times (Rp/Rac)} \tag{4}$$

- GRX defined as Vl/V2w is the receive gain and can be evaluated applying V2W at the 2W termination and measuring Vl :

$$GRX = - G \times \cfrac{Rl}{Rl + Rp} \tag{5}$$

The problem is now how to choose the external components in order to obtain the desired value for the above parameters.

Solving the equations (1) ; (3) ; (4) and (5) you can obtain :

From the (5) :

$$R2 = K \times (Zl + Rp) \tag{6}$$
$$R1 = K \times ((2/GRX) -1) \times Rl - K \times Rp$$

The value of K must be chosen in order to have R1, R2 > Z2w.

From the (4) :

$$Rac = \cfrac{50 \times Rp \times Zl/GRX}{((1 - GRX \times GTX)/(GRX \times GTX)) \times Rl - 2 \times Rp} \tag{7}$$

From the (3) :

$$Rp = \cfrac{(1 - GRX \times GTX) \times Zin \times Rl}{Rl + GRX \times GTX \times Zin} \qquad (*) \tag{8}$$

From the (1) :

$$Rs = Z2w \times \left(1 + G \times \cfrac{Rac}{25 \times (Rp + Rl)} \right) \tag{9}$$

If you want to try a different approach in the Appendix you can find the input file for SPICE simulation of the circuit. The components names are the same used in fig. 2.1 and fig. 4.1.

(*) : If you want to keep the possibility to choose Rp not depending on the desired AC parameters of your system you can add a resistor Ro between the 2W termination and Z2w and select its value in the proper way.

SGS-THOMSON
MICROELECTRONICS

4. ONE APPLICATION EXAMPLE

4.1. EXTERNAL COMPONENTS DEFINITION

Once defined the desired specs. (Zin, Z2w, GTX, GRX) from the (6) to (9) it is possible to define all the external components.

Let's suppose you want :

GTX = - 3dB   (= .708)

GRX = - 3dB

Zin = 600Ω

Z2w = 600Ω

Substituting in the above relations you obtain :

Rp = 200Ω   (from the (8))

Rac = 42.4 KΩ   (from the (7))

R1 = 43.6 KΩ   (from the (6))

R2 = 39 KΩ

Rs = 1800Ω   (from the (9))

Here below you can see the complete application diagram for the two wire configuration :

Figure 4.1 : L3090/L3000 SLIC KIT in Two Wire Configuration.
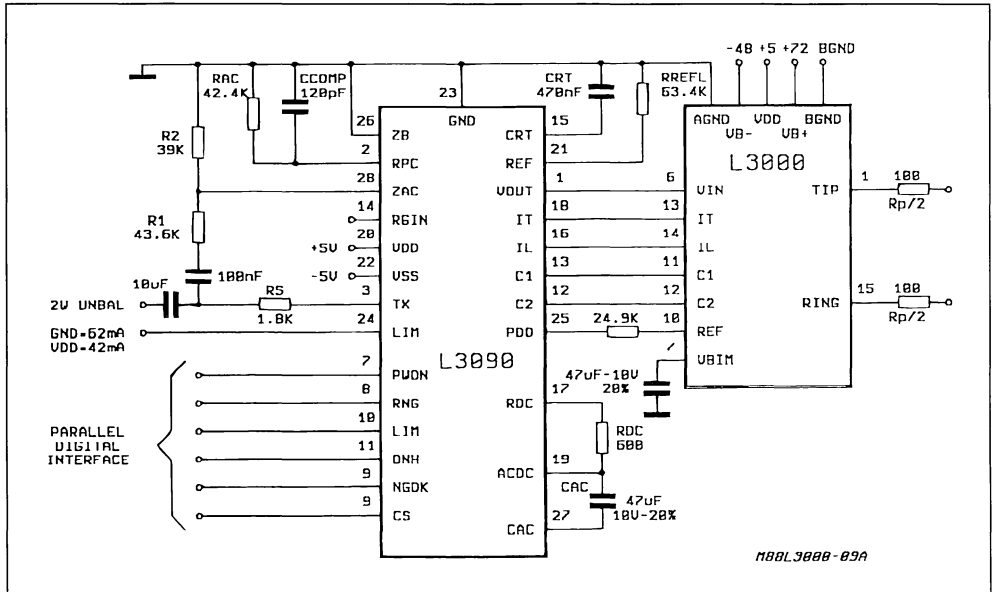
4.2. MEASUREMENTS

Here below you can see the results of some mea-surements on the application shown in fig. 4.2. The 2w termination is loaded with 600 ohm ; the line impedance is 600 ohm.

Figure 4.2 : Return Loss at Line Termination (Rref = 600Ω).

Figure 4.3 : Return Loss at the 2W Termination (Rref = 600Ω).

Figure 4.4 : TX Gain Flatness (GTX (1KHz) = −3dB).
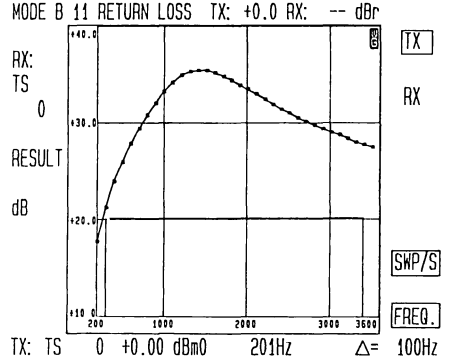
Figure 4.5 : RX Gain Flatness (GRX (1KHz) = −3dB).

SGS-THOMSON
MICROELECTRONICS
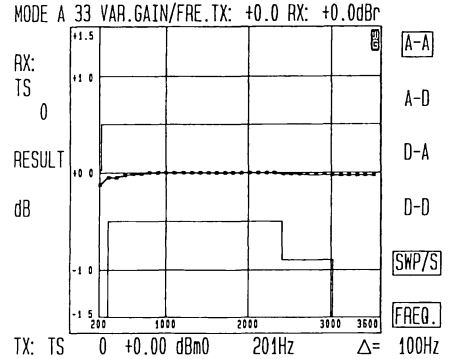
```
L3090 2 WIRE AC ANALYSIS

********************************************
*                                          *
*  SLIC DEFINITION IN 2W CONFIGURATION     *
*                                          *
********************************************


.SUBCKT SLIC 7 8

******** SLIC EXTERNAL COMPONENTS ***********

RAC 1 0 42.4K
RS 2 3 1.8K
R1 9 4 43.6K
R2 4 0 39.0K
RP 5 6 200
C1 3 8 10U
C2 3 9 100N
CCOMP 1 0 120P

********* END SLIC EXTERNAL COMPONENTS ******


********* SLIC INTERNAL CHARACTERISTICS *****
********* DO NOT MODIFY THESE VALUES !! *****

V1 7 6

F1 1 0 V1 .02

E1 2 0 1 0 2
E2 5 0 4 0 -2

********* END SLIC INTERNAL CHARACTERISTICS *

.ENDS SLIC

********************************************
*           END SLIC DEFINITION            *
********************************************


.AC DEC 10 10 10K
.WIDTH IN=80 OUT=80

***** INSERT ONLY ONE OF THE FOLLOWING BLOKS  DEPENDING ********
***** ON WHICH ANALYSIS YOU WANT                       ********

****************************************************************
*                                                              *
*    ANALYSIS ON ONLY ONE SLIC TERMINATED ON RL (LINE SIDE)    *
*    AND ON R2W (TWO WIRE SIDE)                                *
*                                                              *
****************************************************************

**** INPUT IMPEDANCE EVALUATION ******************************
*X1 1 2 SLIC
*R2W 2 0 600
*IL 0 1 AC
*.PRINT AC VM(1) VP(1)
*************************************************************

**** 2W IMPEDANCE EVALUATION ********************************
*X1 1 2 SLIC
```

```
*RL 1 0 600
*RG 0 2 10MEG
*I2W 0 2 AC
*.PRINT AC VM(2) VP(2)
*************************************************************

**** SINGLE TX GAIN EVALUATION ******************************
*X1 1 2 SLIC
*VL 1 0 AC
*R2W 2 0 600
*.PRINT AC VM(2) VP(2)
*************************************************************

**** SINGLE RX GAIN EVALUATION ******************************
*X1 1 2 SLIC
*RL 1 0 600
*V2W 2 0 AC
*.PRINT AC VM(1) VP(1)
*************************************************************

*************************************************************
*                                                           *
* ANALYSIS ON TWO SLIC CONNECTED TOGETHER AT THE 2W TERMINATION *
*                                                           *
*************************************************************

**** INPUT IMPEDANCE EVALUATION *****************************
*X1 1 2 SLIC
*X2 3 2 SLIC
*R2W 2 0 10MEG
*IL 0 1 AC
*RL 3 0 600
*.PRINT AC VM(1) VP(1)
*************************************************************

**** TX GAIN EVALUATION *************************************
*X1 1 2 SLIC
*X2 3 2 SLIC
*R2W 2 0 10MEG
*VL 1 0 AC
*RL 3 0 600
*.PRINT AC VM(2) VP(2)
*************************************************************

**** OVERALL GAIN EVALUATION ********************************
*X1 1 2 SLIC
*X2 3 2 SLIC
*R2W 2 0 10MEG
*VL 1 0 AC
*RL 3 0 600
*.PRINT AC VM(3) VP(3)
*************************************************************

.END
```

SGS-THOMSON
MICROELECTRONICS

SGS-THOMSON MICROELECTRONICS

PABX BIG COST REDUCTION AND PERFORMANCE IMPROVEMENT ARE OBTAINED WITH A NEW SLIC CHIP SET

by W. Rossi

The new L3000/L3091 SLIC need very few external components, very low power in ON-HOOK and provide innovative functions like Ringing injection, message waiting, line length measurement for autoadaptive systems.

Abstract

The new SGS-THOMSON SLIC (Subscriber Line Interface Circuit) kit L3000/L3091 suitable for PABX (Private Automatic Branch Exchange), low end C.O. (Central Office) and ISDN terminal adaptor applications is described. The two chip approach allows the integration of innovative functions as ringing generation and injection, line length evaluation, message waiting, loop extension all software programmable. High level DC/AC performances are provided and very low power is requested in on hook condition (less than 10mW from battery and typ. 50mW from +/- 5V supplies).

1. INTRODUCTION

The '90 years will represent a transition period from fully analog solution to fully digital (ISDN) one in PABX systems design. In particular in this new systems generation analog and digital line cards will coexist. The SLICs for this new systems should satisfy the following requirements:

- do not degrade the transmission performances of the digital part (ex: noise due to relay bounces during ringing injection).

- Software programmability of the DC/AC characteristics in order to have an easy adaptation to different countries requirements.

- Signaling self management in order to simplify the card controller software.

- Low number of external components.

- High reliability and low cost.

In order to satisfy the above requirements a complex circuit structure is necessary. Such a structure cannot be integrated in a single chip because high voltage technology is required to interface the subscriber line. Single chip solutions based on present H.V. Technology are possible only giv-

ing up most of the above requirements or increasing too much the device size and the external components number. The SGS-THOMSON SLIC family actually in production and based on a two chip approach is able to satisfy the above requirements. In fact only the circuit directly connected to the line is realized in High Voltage Technology while all the control and signal management functions are performed in the control chip realized in high density, Low Voltage Technology. (15V). In addition this approach allows an easy adaptation to different applicative situation only selecting the proper low voltage control chip. In the following the L3000/L3091 kit will be deeply described.

2. L3000-L3091 GENERAL DESCRIPTION

The SLIC KIT L3000/L3091 integrate all the functions, except the overvoltage protection, needed to interface a subscriber line. As shown in fig.1 the L3000 chip is a directly connected to the telephone line. On the L3091 chip two interfaces are present. The first is an analog interface (4W) connected to the analog input/output of a Codec/Filter. The second one is a parallel digital interface that allows to set different operating modes of the kit and to transfer information about line status. Because of the internal latches circuit this interface can be connected to a SLIC common control bus driven by the Line Card Controller (see fig. 1). In alternative this interface can be directly connected to the I/O control port of a second generation COMBO as SGS-THOMSON TS5070/TS5071 (see fig. 2). The main features of the L3000/L3091 are the following :

- Programmable DC feeding resistance and limiting current (25/40/60mA)

- Low power dissipation (50mW) in on hook condition (off-hook detector active).

- Loop extension / Integrated message waiting function.

- Signaling function (ON-HOOK/OFF-HOOK; GROUND-KEY/GROUND-START detection)

- Line length evaluation

- Hybrid function

- Line impedance synthesis (real/complex)

- Balanced ringing signal generation with zero crossing injection

- Automatic ringing stop with zero crossing when

OFF-HOOK is detected.

- Parallel latched digital interface for direct connection with 2nd generation COMBO or Card Controller

- Low number of external standard tolerance components.

- Integrated thermal protection that disable output stages when junction temperature exceeds 140°C

Figure 1: The latched parallel digital interface of L3091 allows an easy common bus control structure. The card controller select the proper SLIC via the corresponding CS pin.

SGS-THOMSON
MICROELECTRONICS
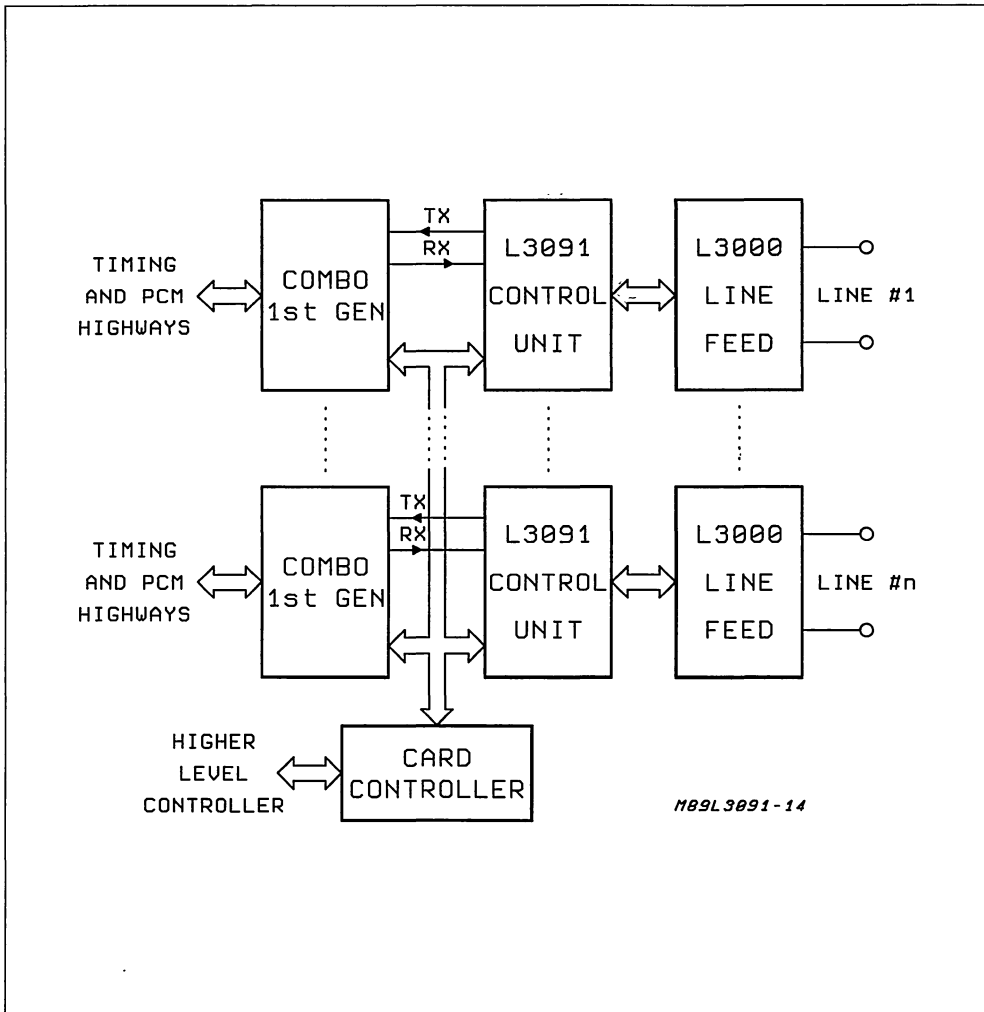
Figure 2: The digital interface of L3091 is directly connected to the COMBOII I/O ports. The card controller manage this I/O digital interface via a 2Mbit serial control port.
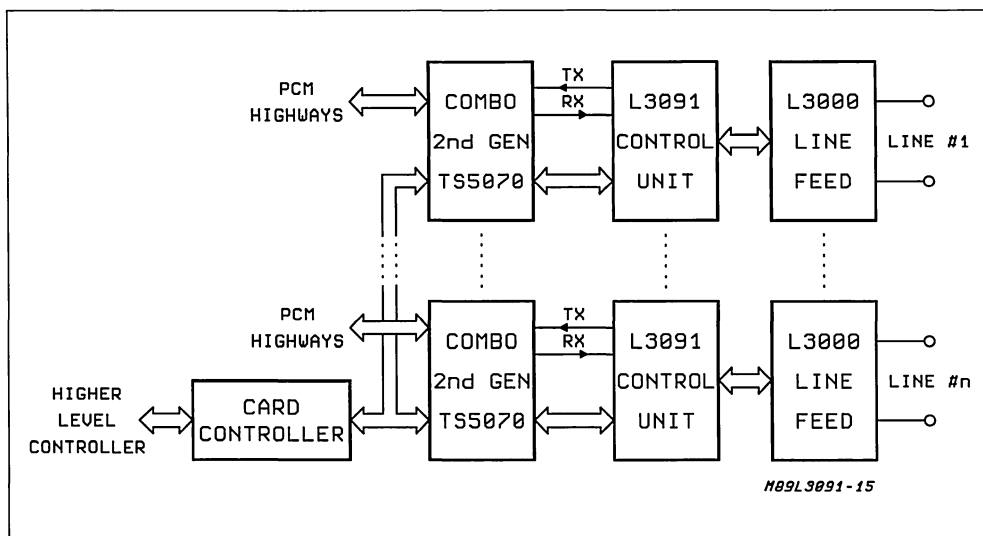
3. OPERATING MODES

Three input and two output pins represent the parallel digital interface. In addition a CS pin allows to connect the digital interfaces of all the SLICs on the Line Card to the same control bus; the digital datas applied to this interface selects one of the following operating modes:

- Conversation or Active Mode
- Stand-by or On-Hook Mode
- Power Down or Disable Mode
- Ringing Mode

4. CONVERSATION OR ACTIVE MODE

The SLIC is setted in this mode when the off-hook condition has been detected and the communication must be activated; the main functions performed in this mode are:

1) DC current feeding into subscriber loop.

2) Signaling recognition (OFF-HOOK; GND-KEY; DIAL PULSES)

3) Bidirectional transfer of speech band signals between line (2wire) and COMBO (4wire) interfaces.

4.1 DC CHARACTERISTIC

One of the main SLIC function is to provide a DC current to the subscriber loop in order to feed

properly the connected telephone set. In fig. 3 different DC characteristics Line Current (II) versus loop resistance (Rl) are shown. The (a) curve represents the DC characteristic obtained with traditional line interface based on transformer; as you can see it is a purely resistive characteristic (II=VBAT/(2xRFS)) where typical RFS values are 200ohm and 400ohm. The (b), (c), (d) curves represent the three different programmable DC characteristics that can be obtained with the L3000/L3091 SLIC kit in conversation mode. Each curve is composed by two regions the first with constant line current and the second resistive were the RFS value is programmed by means of one external resistor. The constant current region allows a big power dissipation reduction with short lines if compared with the transformer solution. In addition the possibility to program by software different limiting currents (25,40,60mA) make the system more flexible allowing an easy adaptation to the different administration requirements and the possibility of the line length measurement. In fact when TEST MODE function is activated one of the digital interface output will show if the actual line current is equal or lower than the programmed limiting current value. The possibility to program three different limiting current values allows to distinguish four different line resistances ranges as shown in fig. 3; this information is very useful in order to optimize the transmission performances for each line length.

SGS-THOMSON
MICROELECTRONICS

Figure 3: The (a) curve represents the DC characteristic obtained with traditional line interface based on transformer. The (b), (c), (d) curves represent the three different programmable DC characteristics that can be obtained with the L3000/L3091 SLIC kit in conversation mode.

L3000/3091 DC Characteristic.

feeding resistance: 2 x 200Ω;
batt. voltage 48V
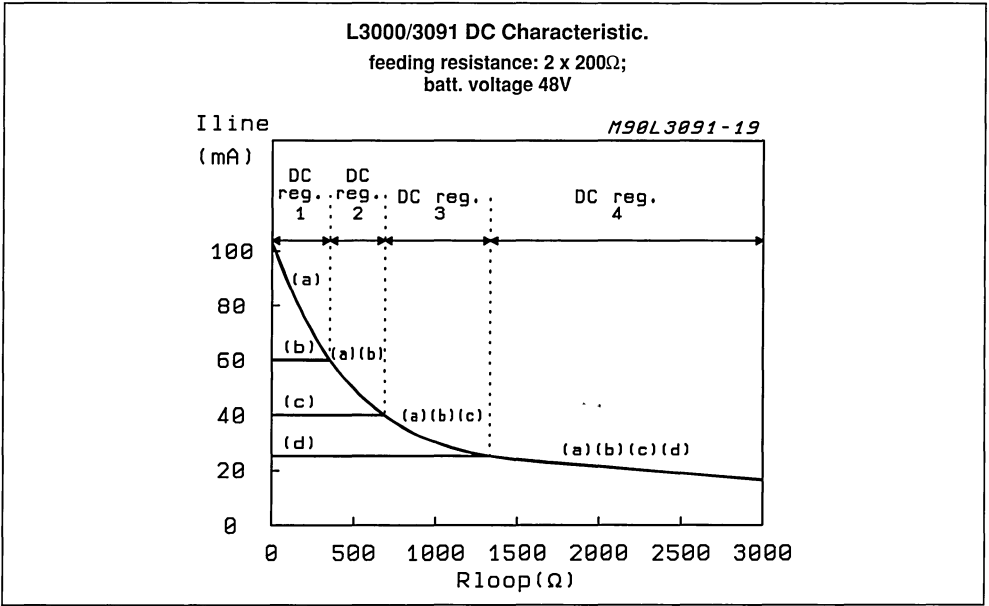
In particular if a second generation COMBO, as SGS-THOMSON TS5070/71 is adopted the line length can be used to select by software proper transmit/receive gains and balance impedances obtaining in this way an autoadaptive system at four states. Another important feature consists in the balanced line feeding circuit; it means that line current variations will produce equal and opposite voltage variations on the A, B, or TIP, RING SLIC line terminations. This characteristic is very important because during dial pulse selection the line current change from zero to the maximum value producing large line voltage variations. The balanced structure avoid high common mode signals generation with very short rise/fall time. It should be noted that this problem is always present when monolithic SLICs with integrated DC/DC converter are adopted in fact in this case doesn't exist voltage symmetry between the two line terminations. This kind of common mode signals produce serious transmission problems on the ISDN line present in the same system; in addition they are also noise sources for the other analog lines. The L3000/L3091 SLIC kit has been studied not only in order to avoid common mode noise on the line, but also to be less sensitive to the noise present on the battery voltage typically generated

by dial pulse selection and ringing injection operations. In particular the noise on the battery voltage is transferred to the line with an attenuation higher than 20dB for low frequency components (10Hz) and with more than 40dB for speech band components (typ. 1kHz).

4.2 LONG LINES FEEDING.

The L3000/L3091 SLIC kit is also suitable for public central office, since in this application is sometimes required to feed very long lines a particular operating mode (Boost Battery) is provided. When the boost battery mode is activated the DC characteristic is modified allowing 20mA of feeding current for 4Kohm of loop resistance equivalent to more than 10Km (see fig.4). Considering PABX dedicated to Hotel applications this operating mode can be used to perform the "MESSAGE WAITING" function. In fact when the Boost Battery mode is selected and the line current is zero the line voltage is greater than 100V; this voltage is high enough to switch on the neon lamp on the telephone set typically used to inform the subscriber to call back the operator. During Boost Battery operation the L3000 line interface circuit fed its internal output stages between the negative battery (typ -48V) and the positive bat-

4/9

Figure 4: DC characteristic in Boost Battery mode allows to feed very long lines (20mA/4Kohm) and to perform the "message waiting" function. For line current close to zero the TIP/RING voltage is greater than 100V.

L3000/3091 DC Characteristic.

feeding resistance: 2 x 200Ω;
Boost Battery mode (tot. batt.: 120V)

NOTE: For Iline=0V(TIP-RING)=105V
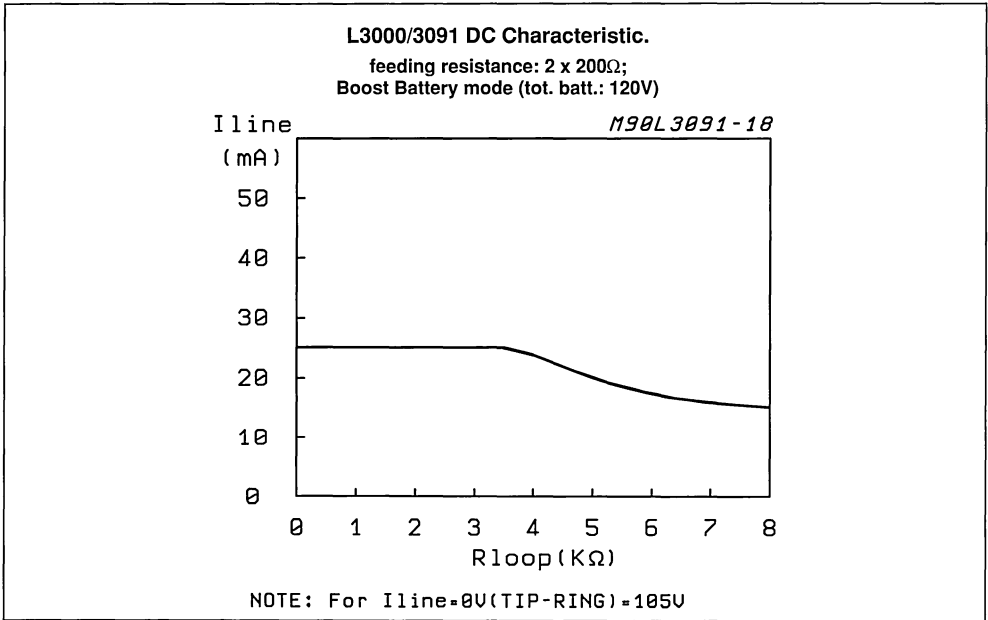
tery voltage (typ. +72V) already present for the ringing operation.

4.3 SIGNALING.
When the Conversation operating mode is selected on the two output pins of the digital interface the following informations are provided:
1) ON-HOOK/OFF-HOOK detection
2) GROUND KEY / GROUND START detection.
In addition the off-hook detection delay is very low allowing dial pulse detection with a distortion lower than 1% . On the contrary the ground key information is filtered with a time constant in the range of 100ms.

4.4 AC CHARACTERISTIC.
The L3000/L3091 SLIC kit provide excellent AC characteristics, in addition its internal structure allows an easy programming of the line and balance impedances both real or complex by means of external scaled (by 25) components. It means that in case of complex impedances the external capacitors values will be 25 time lower than the synthetized values. Another peculiarity of the L3000/L3091 SLIC kit is the possibility to recover the insertion loss due to the external protection resistors connected between the SLIC TIP and

RING (A, B) output pins and the line; such resistors cannot be avoided being necessary to limit the line current when surges or other causes produces overvoltages on the line. The major part of the monolithic SLICs available on the market requires low values for the external protection resistors (< 20ohm) being not able to recover the attenuation produced by such components.

This attenuation become a problem in presence of complex line impedance because its value depends also on the frequency. If protection resistors higher than 20ohm are adopted the correspondent amplitude distortion with frequency will not be acceptable and external complex equalizing circuit required.

On the contrary the L3000/L3091 SLIC kit allows to use protection resistors in the range from 30 to 100ohm increasing in this way the system protection level. In this condition the guaranteed insertion loss flatness (including external protection resistors) between 2W (line) and 4W (COMBO) interfaces is +/- 0.1dB for both real or complex line impedances.

Another important L3000/L3091 SLIC kit feature for the overall system performances is the capability to work also in presence of high induced lon-

SGS-THOMSON
MICROELECTRONICS

gitudinal line current. The longitudinal current can be generated by the following causes:

1) Magnetic/capacitive coupling between the subscriber line and the AC main power distribution network (110/220V; 50/60Hz).

2) Magnetic/capacitive coupling with adjacent subscriber line on which large voltage/current variations are present (ex: dial pulse selection; ringing injection..)

3) Magnetic/capacitive coupling with high frequency electromagnetic waves.

For a proper SLIC operation in presence of the above conditions the following characteristics are necessary:

1) High value of Longitudinal to Transversal Conversion (LTC)

2) High value of Longitudinal to Transversal Conversion also in presence of high common mode current.

3) High value of Longitudinal to Transversal Conversion also in presence of high frequency common mode current.

The L3000/L3091 SLIC kit is able to satisfy all the above requirements; in particular the LTC guaranteed value is 52dB; the typical is 60dB. This value remain nearly unchanged also for high common mode current (ex. 65mA peak on each wire with 25 mA of transversal DC line current or 50mA peak with 40mA of transversal DC line current).

In addition the high gain-bandwidth product of the L3000 integrated operational amplifiers allows to keep the LTC value very high also for common mode current frequencies up to 200/300kHz. Higher frequencies common mode current can be easily attenuated connecting between the line terminations and ground small capacitors (10/20nF). The low effect of such capacitors on the SLIC AC parameters (gains, impedances, two to four wire conversion....) can be easily recovered acting on the SLIC external components thanks to the high flexibility of the two chip architecture.

In fig.5 are shown the test circuit used for EMI evaluation up to 10MHz and the results obtained with and without the filtering capacitors on line terminations. This excellent result show that the L3000/L3091 SLIC kit provide very high rejection to EMI signals without requiring expensive H.F. coils.

Figure 5a: Test circuit for EMI evaluation.
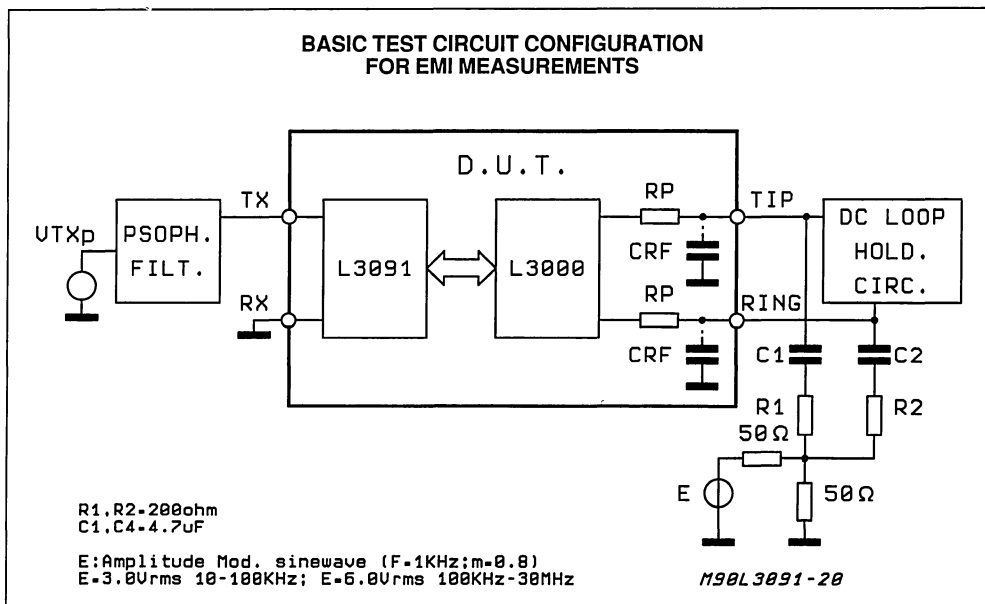
Figure 5b: The high bandwidth and high current capability of L3000 output operational amplifier allows an excellent rejection to longitudinal EMI signals up to 200kHz (a) curve. This good performances are maintained for higher frequencies using two inexpensive small capacitors (Crf=10/20nF).
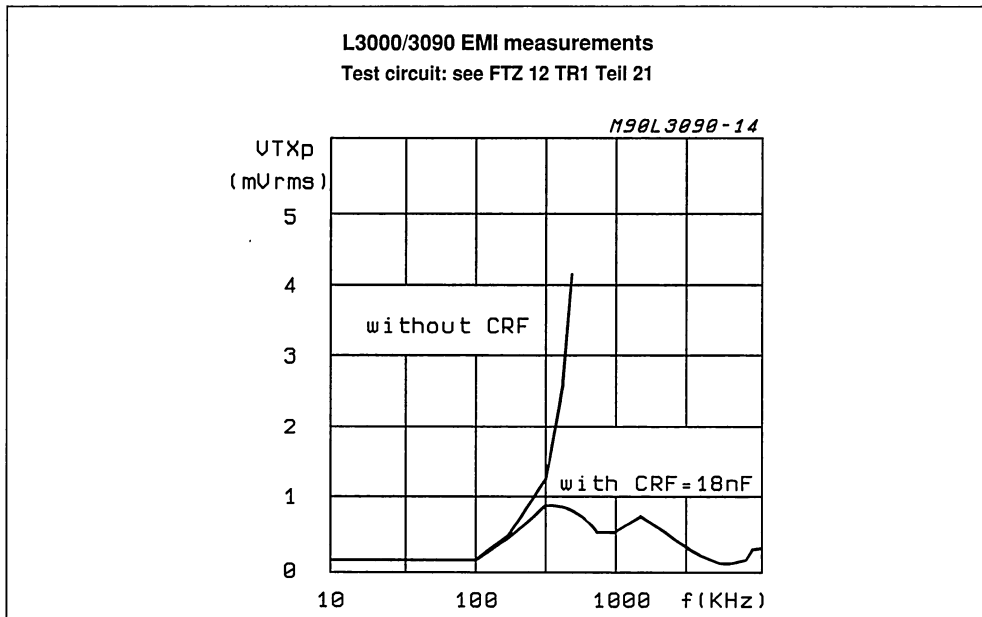
5. STAND-BY OR ON-HOOK MODE

The L3000/L3091 SLIC kit is usually programmed in Stand-By mode when the connected telephone set is in on-hook condition; the only functions performed in this mode are:

1) DC line feeding with low limiting current value (10mA)

2) OFF-HOOK detection This second function is performed by a sophisticate circuit that allows a proper off-hook detection also in presence of high common mode currents induced on the line therefore the off-hook information provided by the SLIC doesn't need additional processing by the card controller. The reduced number of functions provided in this mode allows a significative SLIC power dissipation reduction (250mW).

6. POWER DOWN MODE

This mode is used in all those condition in which it is necessary to reduce to zero the power delivered to the line (power failure, emergency, line not connected ....). In power down mode the line interface circuit L3000 is completely switched off therefore not able to detect OFF-HOOK, its im-pedance at line terminations is 1Mohm and the current sinked from the battery is reduced to zero. In this mode the power dissipation from the +/-5V supplies is typ. 50mW. In case a very low power dissipation is requested also when the telephone is in on-hook and in such condition it doesn't sink more than 500uA the Automatic Stand-by Mode can be selected. The Automatic Stand-by Mode combine the advantages of the two previous operating modes, in particular:

1) Accurate OFF-HOOK detection

2) Low power consumption (50mW from +/-5V and <10mW from battery).

When this mode is selected the L3000 is normally in Power-Down Mode. A dedicated circuitry inside L3091 will sense the line voltage and will automatically program in Stand-by Mode the L3000 if a possible off-hook condition is detected.

7. RINGING MODE

One of the L3000/L3091 SLIC kit main characteristic is the possibility to inject directly the ringing signal on the line without request of external electromechanical relay and high level ringing genera-

tor. In order to obtain from the L3000 the proper level for the ringing signal an additional positive voltage source is requested (typically +72V).

The ringing signal is obtained amplifying a low level signal (1.5Vrms) applied to the SLIC, this low level oscillation can be obtained either from a local oscillator or from the COMBO RX path. The ringing signal is injected on the line in balanced mode with a nominal amplitude of 60Vrms that can be increased up to 70Vrms.

During the ringing injection the SLIC output impedance is just equal to the two series protection resistors (dohm); this characteristic allows to use lower ringing signal amplitude compared with the standard solutions where the ringing generator series impedance is typically 800ohm. In fig.6 is represented the effect of the low output impedance with different ringer load and compared with the traditional solution with a source voltage of 75Vrms and 800ohm of output impedance.

A dedicated circuitry guarantee that the ringing signal is injected and disconnected from the line always in presence of the zero voltage crossing transition, avoiding the generation of very fast voltage transition on the line.

During ringing injection a sophisticate circuit will perform a complete ring trip detection; when off-hook condition is recognized the SLIC will automatically stop the ringing signal without waiting for the card controller command.

In conclusion the L3000/L3091 SLIC kit allows to save:

- The centralized H.V. ringing generator

- all the ringing relays

- all the zero crossing circuitry

- all the software for ring trip detection.

Figure 6: Comparison between L3000/L3091 SLIC kit and standard solutions ringing performances. The voltage across the ringer load after 1Km line (280ohm) is shown for different REN (Ringer Equivalent Number). The L3000 low output impedance in ringing mode allows to recover the lower source voltage (60Vrms versus 75Vrms) and to be better than standard solution when the REN increase.
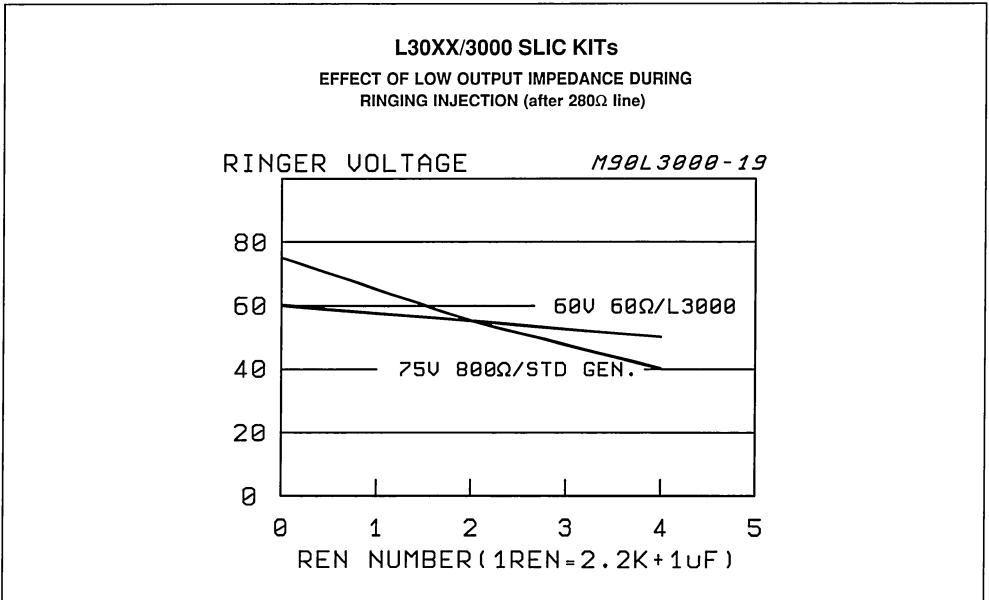
8. CONCLUSIONS

The complete circuitry needed to interface the PCM system highways to the subscriber line is shown in fig.7. The SLIC two chip approach allows to reduce drastically the number of external components, to save the centralized ringing generator, the ringing relay, the zero crossing ringing control and to implement the "message waiting" function. In addition the combination of the

SGS-THOMSON
MICROELECTRONICS

the L3000/L3091 SLIC with COMBOII increase the system flexibility and performances. In particular the card controller can select by software:

- DC feeding currents (25/40/60mA)
- TX and RX gains (25dB range; 0.1dB step) -

Balance networks

- Time slot assignment (up to 64x2 slots)

In addition the Test Mode implemented on L3091 in conjunction with COMBOII allows to realize a four step autoadaptive balance system.

Figure 7: Complete application circuit needed to interface a subscriber line with system PCM highways. Very low number of external components and high flexibility are achieved due to the SLIC two chip architecture.

SGS-THOMSON
MICROELECTRONICS

SGS-THOMSON
MICROELECTRONICS
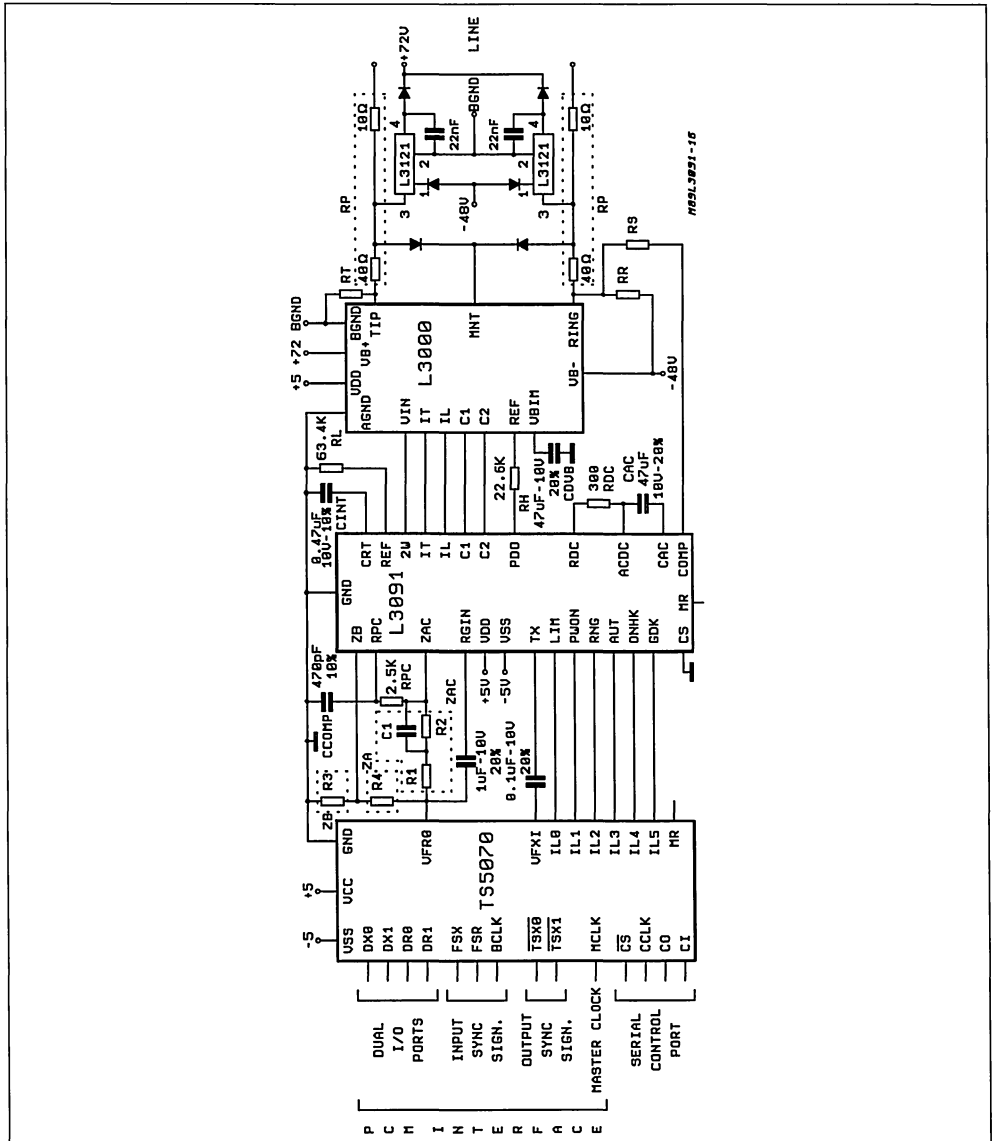
TDB7711-TDB7722
SUSCRIBER LINE INTERFACE CIRCUIT KIT

TABLE OF CONTENTS

1. HIGH VOLTAGE CIRCUIT DESCRIPTION (TDB7722)

(Refer to diagram of fig. 1)

1.1. VOLTAGE AMPLIFIERS

The input voltage of the circuit V_{IN} is symmetrically amplified by 2 voltage amplifiers, whose transfer functions are :

$$V_{S1} = 20\ V_{IN}\ ;\ V_{S2} = V_{(ref)} - 20\ V_{IN}$$

$V_{(ref)}$ is the filtered battery voltage. The outputs of these amplifiers drive, at very low impedance, the line (tip wire and ring wire).

The symmetry of the two gains is very good to provide high longitudinal balance.

1.2. LONGITUDINAL AND TRANSVERSE CURRENTS SEPARATION

The circuit makes the sum and difference of the two wire currents to provide the transverse and longitudinal components to the LV SLIC (Scaled down : 1/100).

The scaled down transverse current flows by I_T pin.

The scaled down longitudinal current flows by C1 pin.

1.3. OTHER FUNCTIONS (figure page 12 of data sheet)

1.3.1. RING RELAY DRIVER. A transistor, used as a switch, can drive a 5V or 12V relay.
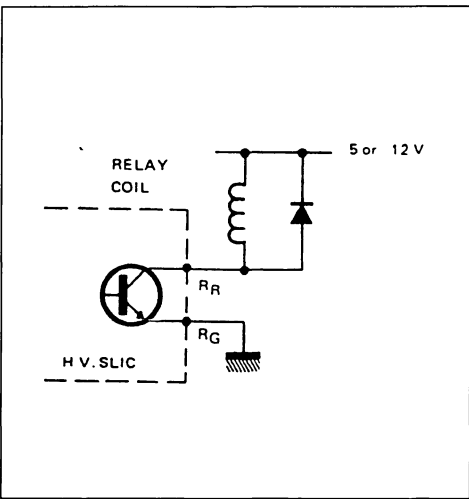
1.3.2. THERMAL WARNING. If the temperature of the IC reaches 150°C a thermal shut down sets the circuit in "HIGH IMPEDANCE" mode and warns the LV SLIC by modifying ILT current (via C2 pin).

1.3.3. STAND-BY. In standby mode, most of the functions are shut down.

Line voltage is set at about $|VB| - 10V$

The currents of the 2 wires are sensed, and the scaled down transverse current is provided to low voltage SLIC TDB7711 for off-hook detection.

1.3.4. POWER DOWN. Under software control, via LV SLIC, or when thermal warning is activated, the circuit is set in power down mode.

In this mode, tip and ring outputs are in high impedance status, and most of the functions are shut down. No line current is provided.

1.3.5. DEVICE CONTROL. The LV circuit controls HV circuit, via C1 and C2 pins, thanks to three different voltage levels.

The HV circuit provides longitudinal current and thermal warning current via the same pins.

The controls are described page 14 of data sheet.

1.3.6. SCALED DOWN BATTERY VOLTAGE. An output provides the LV SLIC with a $V_{(ref)}/40$ voltage ($V_{(ref)}$ is the filtered battery voltage).

This pin is V_{BIM}.

1.3.7. REFERENCE VOLTAGE $V_{(ref)}$. It is the filtered battery voltage. Its value is :

$$[\ |VB| - 2.1V\ ]$$

2. LOW VOLTAGE CIRCUIT DESCRIPTION (TDB7711)

2.1. TRANSMISSION CHARACTERISTICS

(Refer to diagram of fig. 2)

2.1.1. IMPEDANCE SYNTHESIS AND HYBRID BALANCE. The transverse current provided by the HV SLIC is splitted into DC and AC components. The AC currents flows across C_{AC} (C_{AC} pin is a virtual ground) and the DC component across R_{DC}.

The $-2.7V$ voltage on C_{AC} allows for the use of a polarized low voltage capacitor.

IAC current flows through ZAC, and gives a voltage divided by 20 (or -20 in reverse battery) before driving the HV circuit input. This feedback gives the output impedance of the SLIC, between tip and ring wires

Figure 1 : Simplified Block Diagram.

Figure 1 : Simplified Block Diagram.
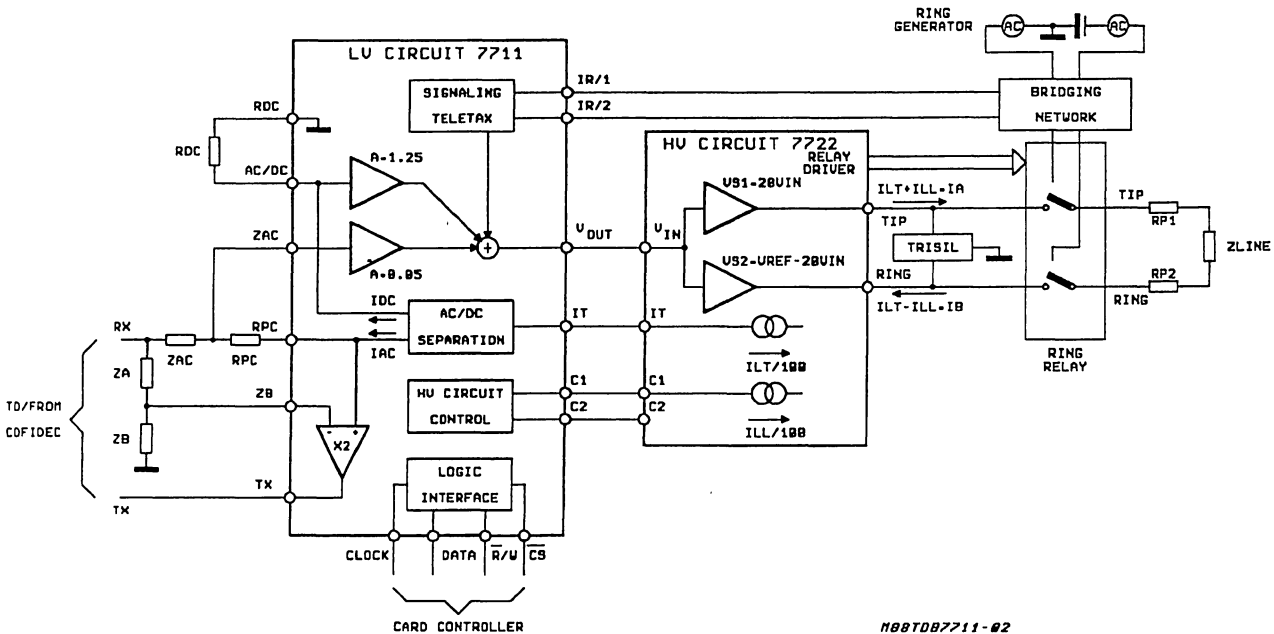
C_{BW} capacitor insures the stability of the feedback. C'_{BW} compensates the C_{BW} effect on hybrid balance. Hybrid balance is done by the input circuitry of TX differential amplifier.

EXTERNAL COMPONENTS ARE DEFINED AS FOLLOWS :
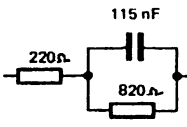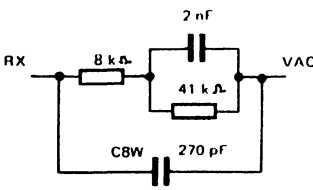
If the required SLIC output impedance is Zline, Z_1 value is such that :

$$Z_{AC}//C_{BW} = 50 \ (Z_{LINE} - 2 \ rp)$$

. Hybrid balance

| $Z_B = K^*ZML$ | $Z_A = K^*Zline$ | $RPC = 100rp$ |

Examples of Output Impedances (with Z_{ML} = Zline)

For example, when K = 100

ZML = termination impedance between TIP and Ring

. Stability capacitor

$$C_{BW} = 8 \ \mu s/ \ |Z_{AC} + R_{PC}|$$
$$C'_{BW} = 8 \ \mu s/ \ |Z_A|$$

* (Can be lightly different, according to the teletax filter).

z_0	z_2		z_1	C' BW $(Z_3 = Z_4 = R = 60k)$
⊏ 600 ⋏	⊏ 30 Ω	⊏ 3 kΩ	⊏ 27 kΩ	120 pF
115 nF / 220Ω / 820Ω	⊏ 30 Ω	⊏ 3 kΩ	2 nF / RX / 8 kΩ / 41 kΩ / VAC / C8W / 270 pF	47 pF

2.1.2. GAINS. The voltage gain of the LV circuit is 1/20.

Then the total SLIC (LV + HV circuits) voltage gain is 2 (1/20 x 40).

As the SLIC output impedance is Z_{LINE}, the RX ⇒ line gain is unity when $Z_{LINE} = Z_{HL}$.

LINE ⇒ TX GAIN

The TX differential amplifier gain is 2.

Then the voltage gain between the line and the TX output is unity.

2.1.3. BANDWIDTHS.
■ Low cut off frequency.

The C_{AC} value gives the low frequency cut off of :
■ the return loss. At low frequency, the return loss is :

$$\rho = \sqrt{1 + 4 \ R^2_{DC} \ C^2_{AC} \ \omega^2} \ \# \ 2 \ R_{DC} \ C_{AC} \ \omega$$

■ the transhybrid loss (=HYBRID BALANCE). At low frequency, the transhybrid loss is :

$$R_{DC} \ CAC \ \omega$$

Then, the value of the product $C_{AC} \ R_{DC}$ is defined by the return loss and transhybrid loss performances needed at low frequency.

R_{DC} is defined in "FEEDING CHARACTERISTICS"

Then :

$$(C_{AC}) \ min = \frac{(R_{DC} \ C_{AC}) \ min}{R_{DC}}$$

■ High cut off frequency

This frequency is given by the stabilization capacitor C_{BW} (see 2.1.1.). Its value is 34kHz.

Note : Improving desaturation time of AC path.

Large DC line current variations may overload the AC path. The recovery time depends on the C_{AC} x R_{DC} time constant.

This time can be lowered by decreasing the C_{AC} value.

4/12

Figure 2 : Functional Diagram (AC path).

M88TDB7711-04
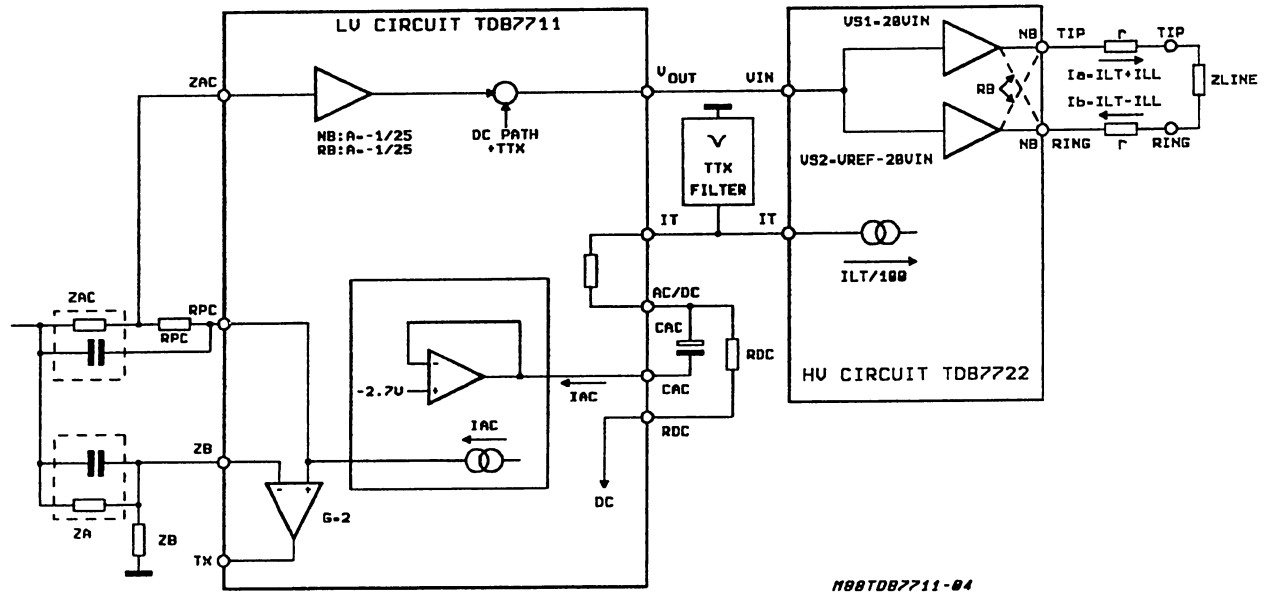
In this case, in order to keep a good hybrid rejection at low frequencies, the Z_A Z_B network should be modified as follows :

R Z_A 60 kΩ

R Z_B 60 kΩ

C_{LF}

$$CLF = \frac{C_{AC} \times R_{DC}}{R4}$$
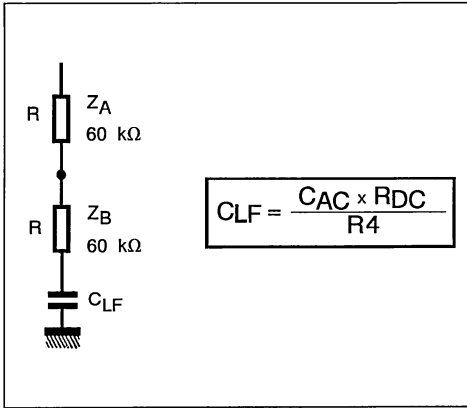
Example : $R_{DC} = 850\Omega$; $C_{AC} = 4.7\mu F$; $Z_B = 60k\Omega$; CLF # 68nF.

Desaturation time for IL = 30mA : 10ms.

2.2. FEEDING CHARACTERISTICS

(See diagram page 10 of the data sheet)

The DC component of the transverse current provided by the HV SLIC flows through R_{DC}.

For DC current I_{DC}, R_{DC} presents a virtual ground.

Then the AC/DC pin voltage is $V_{AC/DC} = I_{DC} \times R_{DC}$.

This voltage is amplified (x1, 25), before driving the HV circuit input.

It can be seen that the DC voltage at LV SLIC output is always :

$$V_{DROP}$$

Then, there are 3 possibilities :
■ Low line current :

$$|V_{AC/DC}| < V_D \Rightarrow V_{OUT} = -V_D$$

The slic is in waste voltage mode.
■ Middle line current :

$$V_{OUT} = V_{AC/DC} = R_{DC} \times I_{DC}$$

The SLIC is in feed resistance mode.

If R_F is the desired feed resistance of the line :

$$R_{DC} = 2 (R_F - 2 R_P)$$

■ Line current = Limitation current :

The voltage on R_{DC} varies quickly when line current is lightly higher than limitation current.

The line current is regulated at the limitation current value.

There are several working modes :
  _ Apparent battery :
    In this mode, a correcting voltage, depending on the current battery voltage, allows the line to see a dummy $-48V$ battery ; otherwise, the line "sees" a voltage $V_{(ref)}$ (= current battery voltage $- 2.1V$).
  _ Real battery :
    Same as apparent battery except for the standard resistive mode where the voltage value is
    $$|V_{LINE}| = |V_{REF}| - R_{feed} \times I_{LINE}$$
  _ Special DC characteristics :
    A low value R_{DC} resistance is simulated to have a rectangular feeding characteristic.
  _ Reverse battery :
    In this mode, the DC current is inverted. Then, the phase of the 1.25 gain amplifier is also inverted, to insure stability of the feedback.

2.3. SIGNALLING (see pages 10 and 12 of data sheet)

2.3.1. OFF-HOOK THRESHOLD AND RESPONSE TIME (SLOW LOOP DETECTION).
In stand-by mode, the line is fed in "normal battery" (non-reserved). The off-hook threshold is 6.5 ± 1.5mA.

The hysteresis is 1mA. The response time for a given current I_{LTO} is :

$$t = (R_{DC} + 1 \ k\Omega) . C_{AC} . LOG \left[1 \ \frac{6.5}{I_{LTO} \ (mA)} \right]$$

(because, in standby, R_{DC}^2 is no longer a virtual ground).

2.3.2. ROTARY DIAL PULSES DETECTION (QUICK LOOP DETECTION).
In power up mode, the loop detection is quick : <1ms.

The threshold is the same as in power down mode :

$$6.5mA \pm 1.5mA$$

The hysteresis is 1mA also.

2.3.3. TELETAX (TTX)

■ Gain

The gain between TTX input (on LV SLIC), and line output (TIP and RING on HV SLIC) is 18dB $\pm$ 1dB.

The line level depends on PTC (or protection resistance) value and line impedance at TTX frequency (Z_{LTTX}).

SGS-THOMSON
MICROELECTRONICS

The level of the sinus signal to set at TTX input, for a given line level V_{LTTX} is :

$$V_{TTX} = VLTTX \left(\frac{Z_{LTTX} + 2r}{Z_{LTTX}} \right) \frac{1}{8}$$

Software control : $\dfrac{1}{0}$

Line signal.
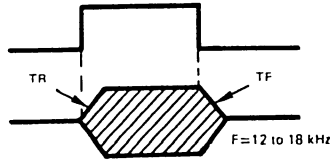
The shaping is done by sending a $\pm 80\mu A$ current in the capacitor C_{RT}, whose voltage varies from $-2V$ to $+2V$ (or from $+2V$ to $-2V$).

Then :

$$T_R = T_F = \frac{C_{RT} \times 4}{80} 10^6$$

i.e. : 10ms for $C_{RT} = .22\mu F$

■ TTX filter

An external TTX filter allows the SLIC to have a low output impedance at TTX frequency, and a low leakage level at TX output.

This filter must have a low impedance (compared to 1kΩ at TTX frequency, and a high impedance in speech band (in order to avoid transmission performances degradation).

If Z_F is the filter impedance at the telefax frequency F_{TTX} :

 - output SLIC impedance at F_{TTX} :

$$(Z_{T-R}) \text{ } _{TTX} \# Z_{T-R} \cdot \frac{Z_F}{Z_F + 1k\Omega} \cdot$$

With Z_{T-R} = Speech band output impedance :

■ TX level at F_{TTX} :

$$V_{TX} \# \frac{V_{LTTX}}{Z_{LTTX} + 2r} \cdot Z_{T-R} \cdot \frac{Z_F}{Z_F + 1 k\Omega}$$

■ TTX drop voltage

The drop voltage value depends on the TTX drop voltage bit (TWV). If TWV = 0, the drop voltage is about 12V (13 max). During sending TTX (TTX BIT = 1) this value becomes 18V.

If TWV = 1, the drop voltage is 18V, whatever the TTX BIT.

■ Shaping
The line signal is as follows :

2.3.4. RING TRIP. When ringing, the SLIC must be in normal battery mode.

■ Principle

An external circuit applies ringing through the ringing network and the ring relay. This circuit consists of a balanced or unbalanced sinus generator (70 to 100 V_{RMS}) in series with the battery (48V). The line current has, then, an AC component (there is a capacitor in series with the ring circuitry) with or without DC component, according to the hook state. So, the off-hook detection is done by sensing the DC component of the line current.

The following principle is used :

A fraction of the line current is sent into a capacitor (C_{RT}). At time t1, the voltage of this capacitor is set at a given value : V_O.

The voltage of this capacitor is sensed at times :

$t1 + T_R$, $t1 + 2 T_R$ ..... $t1 + nT_R$. (T_R = ringing period).

If the voltage sensed is V_O, that means there was no DC component in the line current (on hook).

More precisely, the following tasks are made : when the ringing control is operating (software) :
 - ring relay is energized at the zero crossing point of the ring generator = time t0,
 - C_{RT} voltage is set at $-70mV$ during one ringing period,
 - a scaled down line current is sent (after having substracted a threshold current into C_{RT}.
 - at times t0 + 2T_R, ... , t0 + nT_R, the C_{RT} voltage is sensed :
   · if $V_{CRT} < -70mV$ (i.e. DC line current < I threshold) : V_{CRT} is set t0 − 70mV,
   · if $-70mV < V_{CRT} < 70mV$: V_{CRT} is unmodified,

- if V_{CRT} + 70mV, the off hook is detected : ring relay is desenergized and hook status bit is set on 1 state.
- Ringing network

The following networks are insensitive to longitudinal currents :

Figure 3 : Balanced Ringing.
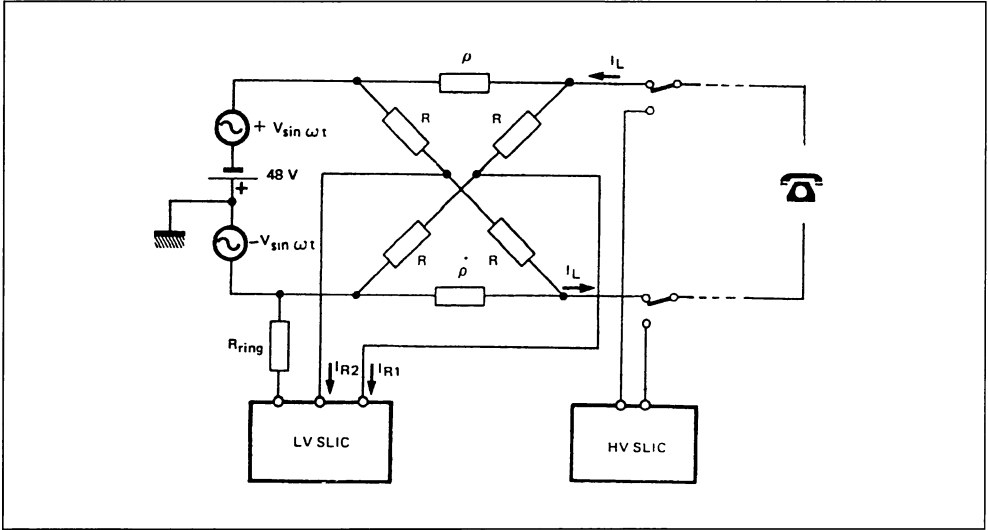
Figure 4 : Unbalanced Ringing.

$$\rho = 200\Omega$$
$$R = 500k\Omega$$

$$I_{R1} - I_{R2} = I_L \times \frac{2\rho}{R}$$

SGS-THOMSON
MICROELECTRONICS
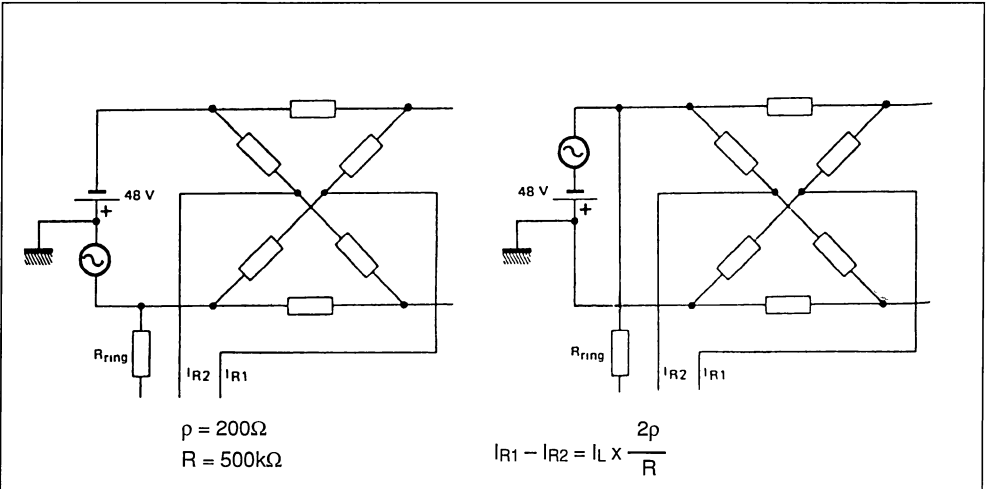
■ Ring trip threshold and response time

We have seen :

$$I_{R1} - I_{R2} = I_L \times \frac{2\rho}{R}$$

The threshold current on LV SLIC input 6.8µA, i.e. :

$$6.8µA \times \frac{R}{2\rho} = 8.5mA$$

on the line with the network above.

The ring trip capacitor should be :

$$C_{RT} = \frac{220nF \times 50Hz}{F_R}$$

$$(\frac{1}{T_R} = F_R = \text{ringing frequency})$$

Then, the ring trip response time for a DC loop current I_{LTO} is :

*

*

That's

■ $I_{R/1}$ and $I_{R/2}$ inputs compliance
The compliances of these inputs are : $> + 350µA$ & $< - 500µA$.
These compliances allow, with the ringing network above, the use of balanced or unbalanced ringing with the limits :

$$- 72V < V_B- < - 20V$$

$$V_{ring} < 88 \ V_{RMS}$$

If other values are needed, the equations above allow to find the values of ρ and R.

■ Bridging network accuracy
According to the desired ring trip accuracy, it is possible to find the resistors ratio accuracy, using the equations above. For example, a 1% ratio accuracy induces a 3mA accuracy in the threshold current (for $V_B- = 60V$).

■ R_{ring} value
It depends on the ringing generator level. The LV circuit requires a 70µArms minimum current.

■ Ring relay response time (tRR)
This time can be compensated by adding a capacitor in series with R_{ring} :

$$C_{ring} = \frac{tg \ [\ 90° - 360° \ t_{RR} \ F_R]}{2 \ \pi \ F_R \ R_{ring}}$$
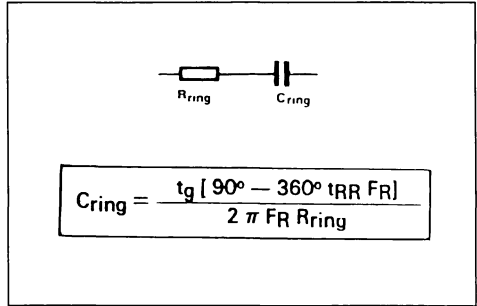
2.3.5. GROUND KEY. The HV SLIC provides a scaled down $(\frac{1}{100})$ line longitudinal current.

A threshold current is substracted from this current, in the LV SLIC and the differential current is sent, after dividing

$(\frac{1}{9})$ to the ring trip capacitor C_{RT} (except when ringing or sending teletax). Then, if the DC component of the longitudinal line current is lower than the threshold current, the C_{RT} voltage is lower than a threshold voltage (+ 2V). Otherwise, ground key is detected.

The treshold longitudinal current is 50µA (i.e. 5mA on each wire, ring and trip).

The response time, for a line current I_{LLO} (each wire) is :

$$T = \frac{4 \times C_{RT}}{\frac{1}{9} \ \left[\ \frac{I_{LLO}}{100} - 50 \ 10^6 \ \right]}$$

Example : $I_{LLO} = 10mA$, $C_{RT} = 0.22µF \Rightarrow r = 160ms$.

2.4. ANALOG INPUT - OUTPUT PIN

This pin is programmed by soft as an input or an output.

■ As an input

An external voltage $\frac{V_{EXT}}{40}$ is set on the pin.

The SLIC compares V_{EXT} voltage and the DC line voltage.

If : $V_{LINE} > V_{EXT} \Rightarrow C_{RB} = 0$
$V_{LINE} < V_{EXT} \Rightarrow C_{RB} = 1$

This can be used to feed the SLIC with a low voltage battery and offer power saving capability.
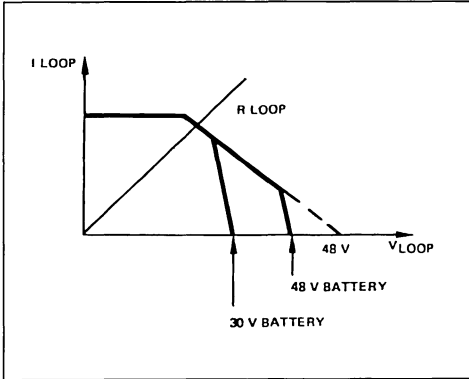
■ As an output

The voltage of this pin is 1/40 the DC line voltage.

This can be used to detect line short circuits.

2.5. DIGITAL CONTROL INTERFACE

The programmable functions of the SLIC are set by the contents of two 8-bit registers in the TDB7711, LV chip. This circuit communicates with the card controller through a 4-wire serial bus. The interface is described pages 17 and 18 of the data sheet.

Figure 5 : Timing Diagram.

M88TDB7711-12

LATCH IF B7-1
LOADING OUTPUT REGISTER
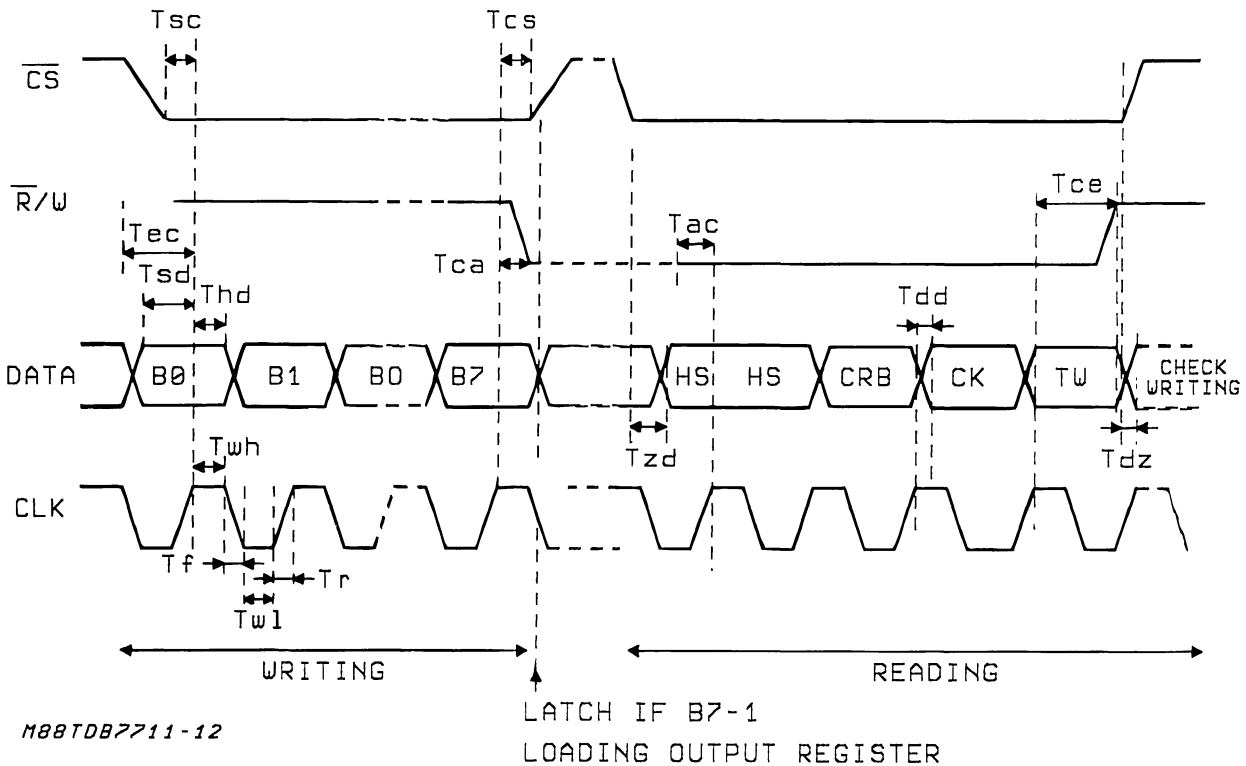
3. OVERVOLTAGE PROTECTIONS

The HV circuit is protected against overvoltages with a pair of PTC or fuse resistors (matched to meet lon-gitudinal requirements), plus a dual trisil with inte-grated diode.

Figure 6 : Protection Circuits.
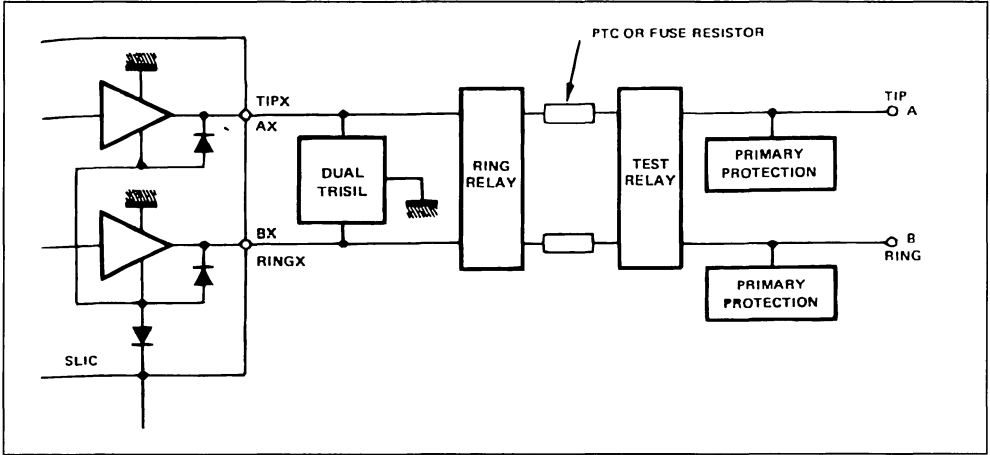
Figure 7 : Trisil Characteristics
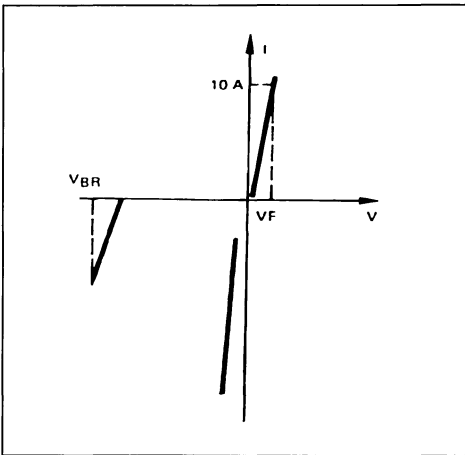
The trisil diode insures line voltage :
< 3V for positive voltage.
< | V$_{BR}$ | for negative voltage.

On surges, negative voltages on trisil falls to a low value, (a couple of volts) keeping it in safety area.

■ Behaviour of the high voltage SLIC when light-ning surges
  • Positive surges < + 3V
    Current in wires are limited by the SLIC itself
    (− 150mA).

Negative surges
The voltage on the line can be more negative than the battery voltage.
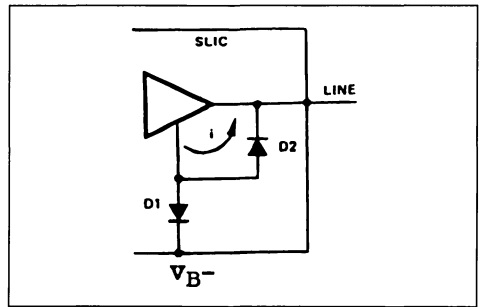
In this case, diodes D1 and D2 act as if the supply voltage of the SLIC was − Vsurge instead of − V$_{b-}$

Then, we must have :

| V$_{surge}$ | < 72V

(i.e. : maximum battery voltage allowed)

| VBR |< 72V

Note : Diodes D1 and D2 are integrated on the chip.

SGS-THOMSON MICROELECTRONICS

TDB 7722/7711 SLIC KIT COMPARISON WITH ERICSSON PBL376X

by W. Rossi

In the following are deeply compared the main functions and performances of TDB and ERICSSON SLIC; in particular:

1 – DC LIMITING CURRENT
2 – LINE LENGHT CONTROL
3 – BATTERY REVERSE
4 – TTX INJECTION
5 – OFF-HOOK DETECTION
6 – ON-HOOK TRANSMISSION
7 – HYBRID FUNCTION
8 – PROTECTION RESISTANCES INSERTION LOSS COMPENSATION
9 – RINGING ZERO CROSSING
10 – RING TRIP FUNCTION
11 – AUTOMATIC RING SIGNAL DISCONNECTION
12 – LONGITUDINAL BALANCE
13 – POWER SUPPLY REJECTION RATIO
14 – SURGE PROTECTION
15 – THERMAL RESISTANCE
16 – THERMAL SHUTDOWN

1 – DC LIMITING CURRENT

This function allows to limit the line current to a fixed value in order to reduce power dissipation in presence of short lines.

TDB	PBL
7 values software programmable through digital interface, from 12mA to 60mA.	1 fixed value hardware programmable by external resistor.

With TDB SLIC solution, the software programmability allows an easy adaptation to different applicative conditions.

2 – LINE LENGHT CONTROL

This function allows to distinguish between long or short line, comparing the line voltage(tip to ring) with a reference voltage.

TDB	PBL
Yes. It provide a software information comparing the line voltage with the voltage applied to the AI/O pin (pin 18 of TDB7711).	Not implemented.

With TDB solution:

– If also a reduced battery voltage is available on card, depending on the line lenght it is possible to select the proper supply in order to optimize the power dissipation.

– If a second generation COMBO is adopted, it is ossible to adjust the AC performances (gains, hybrid function) depending on the line lenght.

3 – BATTERY REVERSE

This function is typically used to generate metering pulses.

TDB	PBL
Yes. It is software programmable.	Not implemented.

In systems where this function is required, the TDB solution allows to save one external relay.

4 – TTX INJECTION

It consists in sending of a metering signal with a frequency from 12 to 16Khz.

TDB	PBL
Yes. It can send a 2Vrms signal with pulse shaping.	Not implemented.

In systems where this signal is required, the TDB SLIC allows to save the external circuitry otherwise necessary for pulse injection and shaping. Fig.1 shows the typical TTX pulse provided by TDB SLIC.

Figure 1: TBB 7722/11 Teletax Injection

Trace 1:
Digital Commnd
(Bit 3)
2V/div; 20ms

Trace 2:
TTx Pulse
On Line Terminals
1V/div; 20ms
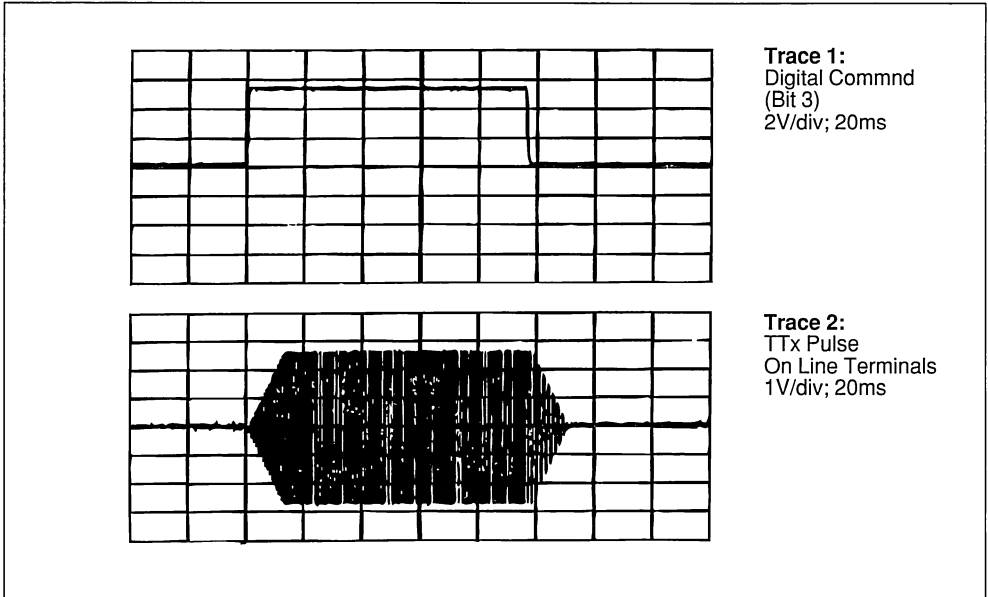
5 – OFF-HOOK DETECTION

This function monitors the loop current.

TDB	PBL
RESPONSE TIME IN SBY MODE	
On/Off transition T = 5msec Off/On transition T = 100msec No additional filtering needed.	On/Off transition T = 5usec Off/On transition T = 15usec Need software filtering
RESPONSE TIME IN CVS MODE	
On/Off transition T = 100usec Off/On transition T = 100usec Dial pulse distortion<1%	On/Off transition T = 1.5msec Off/On transition T = 50usec Dial pulse distortion=1.5%

If the TDB solution is adopted, when the SLIC is in sby mode (on-hook) the off-hook information has a response time (5msec) sufficient to filter the eventual spikies presents on the line. Therefore no software filtering is necessary. On the contrary in cvs mode TDB SLIC has an off-hook response time very short, in order to provide a very low dial pulse distortion.

6 – ON-HOOK TRANSMISSION

This function gives the possibility to transmit signals also when the telephone is in on-hook. Typically it is used for data transmission.

TDB	PBL
Yes, with no variation of AC performances.	Yes, with no variation of AC performances.

The TDB voltage drop between battery and line allows the on-hook transmission of AC signals without any distortion;also all the other trasmission characteristics (Gains, Return Loss, Longitudinal Balance) are unchanged.

7 – HYBRID FUNCTION

This function allows to perform the echo cancellation (2 to 4 wire conversion) between Rx and Tx terminals.

TDB	PBL
Yes. It needs only two scaled impedances.	No. Need external op. ampl. With complex line impedances, inductive components are needed.

SGS-THOMSON
MICROELECTRONICS

TDB solution allow to perform a good echo cancellation with any kind of line impedances, simply using scaled impedances based on resistive and capacitive components.

Typical TDB trans-hybrid loss values are >30dB (300Hz < f < 3400Hz).

ERICSSON solution requires, with complex line impedances, expensive inductive components, in order to provide proper echo cancellation. In addition, also with purely resistive line impedances, the echo signal is slightly phase distorted(5.2 degrees at 3400Hz).This means that, if nominal values components are used in the two-to-four wire conversion circuit, it is not possible to obtain trans-hybrid loss values better than 20dB at 3.4Khz. Higher values can be obtained using a phase equalizing network.

8 – PROTECTION RESISTANCES INSERTION LOSS COMPENSATION

This function allows to use different values for the protection resistances without any modification of the AC performances.

TDB	PBL
Yes, from 30 to 100 ohm with automatic insertion loss compensation.	Not implemented.

The ERICSSON SLIC use 20 ohm for these external resistors. For complex impedance also this little value already introduce an insertion loss that is a function of the frequency. (Ex. for German network: Prot.Res.=20ohm, ins.loss.=0.33dB@300Hz, 0.53dB@3400Hz).

If this protection resistors is increased,also the introduced insertion loss increases in value and in dependance from frequency; therefore the protection resistors values of the ERICSSON SLIC must be as low as possible.

On the contrary with TDB SLIC this problem doesn't exist because, thanks to its internal architecture, it is able to make the compensation of this insertion loss. With TDB SLIC the possibility to use higher protection resistors with no problem, allows to reduce the current flowing through the clamping device (ex. THDT58D) during overvoltage on the line.In this way an higher protection level is guaranteed.

9 – RINGING ZERO CROSSING

This function allows to insert and to stop the ringing signal only at the first zero crossing. In this way we avoid sharp voltage transitions that can induce common mode voltages on the near lines.

TDB	PBL
Yes, with relay delay compensation.	Not implemented.

TDB SLIC solution allows to save external components (ex:TRIACs) and to semplify controller software.

10 – RING TRIP FUNCTION

It allows to detect the off-hook condition during the ringing injection.

TDB	PBL
Yes, with filtered ring trip signal. Less than 2 periods of the ringing signal for stable off-hook condition.	Yes. No filtered ring trip signal. More than 3.5 periods of ringing signal for stable off-hook condition.

In the figures 2 and 3 you can see the results of the ring trip performance comparison. The test conditions are:

- ringing voltage: 90Vrms
- ringing frequency: 50Hz
- loop resistance: 1880ohm
- ringing load: 2REN (1REN=1µF+2.2Kohm)

Fig.2 shows how the ring trip signal on pin 14 of the ERICSSON SLIC is not filtered, therefore it needs to be processed by software; you can also see how a stable off-hook condition is detected only 70msec (3.5 periods) after the telephone has gone in off-hook.

From fig.3 it's important to note how the TDB has an excellent ring trip performance.It detects the off-hook condition in only two periods of the ringing signal(40msec).

In addition fig. 4 to fig 9 show how the ERICSSON SLIC ring trip signal is affected by longitudinal current present on the line and how, on the contrary, the TDB SLIC shows a very good immunity to this kind of current.

Figure 2: Ring Trip Delay – PBL 3762 ($R_L = 2K\Omega$; 2REN; $F_{RING} = 50Hz$)

Trace 1:
On Hook/Off
Hook Output
(Pin 14)
2V/div; 20ms

Trace 2:
Signal Between
Ground and One
Terminal of the
Ringing Load
50V/div; 20ms

ON HOOK ──✕── OFF HOOK
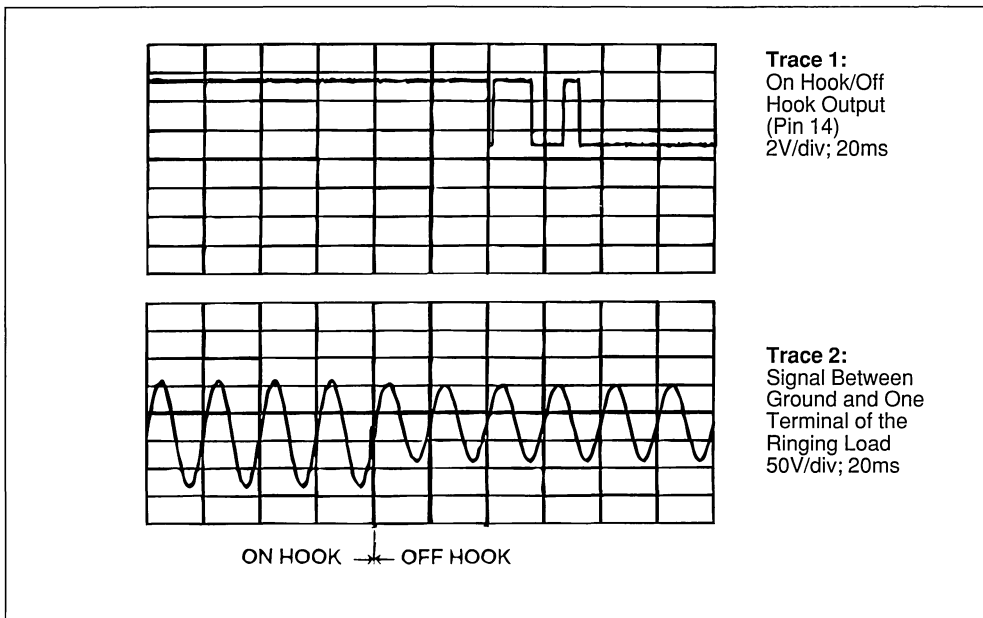
Figure 3: Ring Trip Delay – TDB 7722/11 ($R_L = 2KW$; 2REN; $F_{RING} = 50Hz$)

Trace 1:
On Hook/Off
Hook Information
(Bit 0)
2V/div; 20ms

Trace 2:
Signal Between
Ground and One
Terminal of the
Ringing Load
50V/div; 20ms

ON HOOK ──✕── OFF HOOK

SGS-THOMSON
MICROELECTRONICS
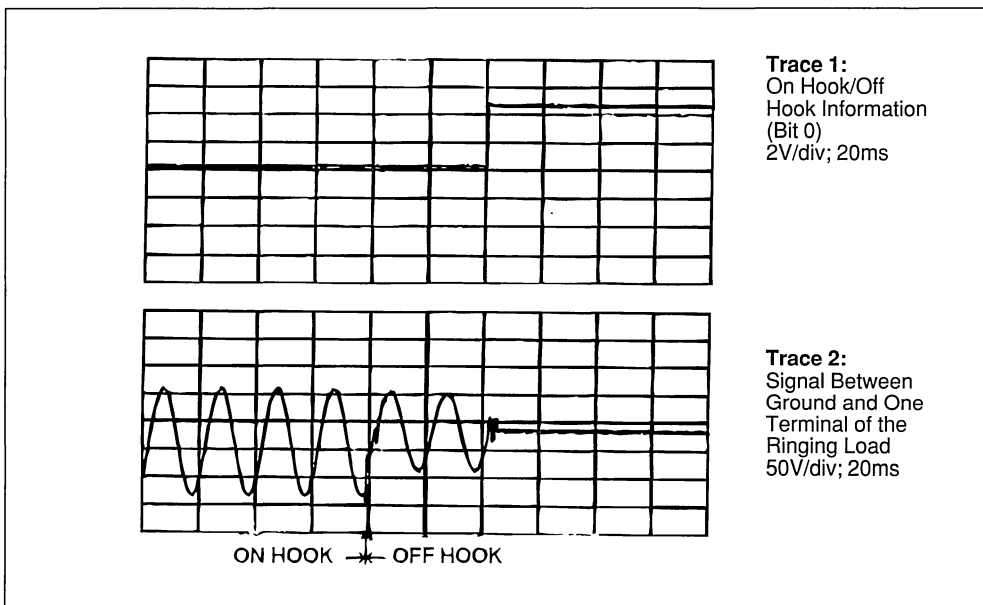
Figure 4: Ring Trip Detection – PBL 3762 – in presence of Longitudinal Current I_L = 2.5mArms/wire; F_{IL} = 25Hz; (R_L = 2KΩ; 2REN; F_{RING} = 50Hz)

Trace 1:
On Hook/Off
Hook Output
(Pin 14)
2V/div; 10ms

Trace 2:
Signal at
Ringing Load
50V/div; 10ms
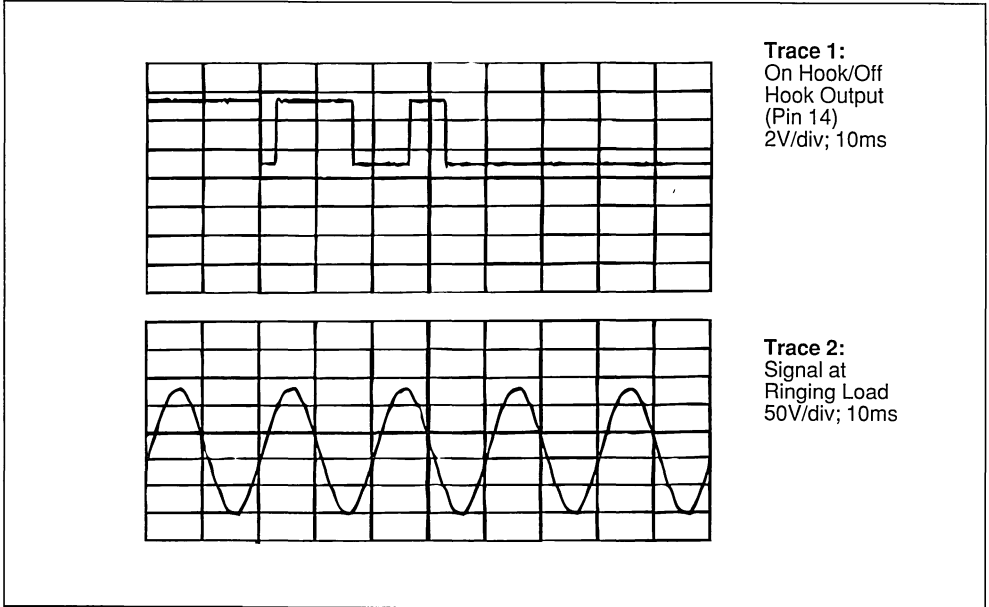
Figure 5: Ring Trip Detection – TDB 7722/11– in presence of Longitudinal Current I_L = 2.5mArms/wire; F_{IL} = 25Hz; (R_L = 2KΩ; 2REN; F_{RING} = 50Hz)

Trace 1:
On Hook/Off
Hook Signal
(Bit 0)
2V/div; 10ms

Trace 2:
Signal at
Ringing Load
50V/div; 10ms
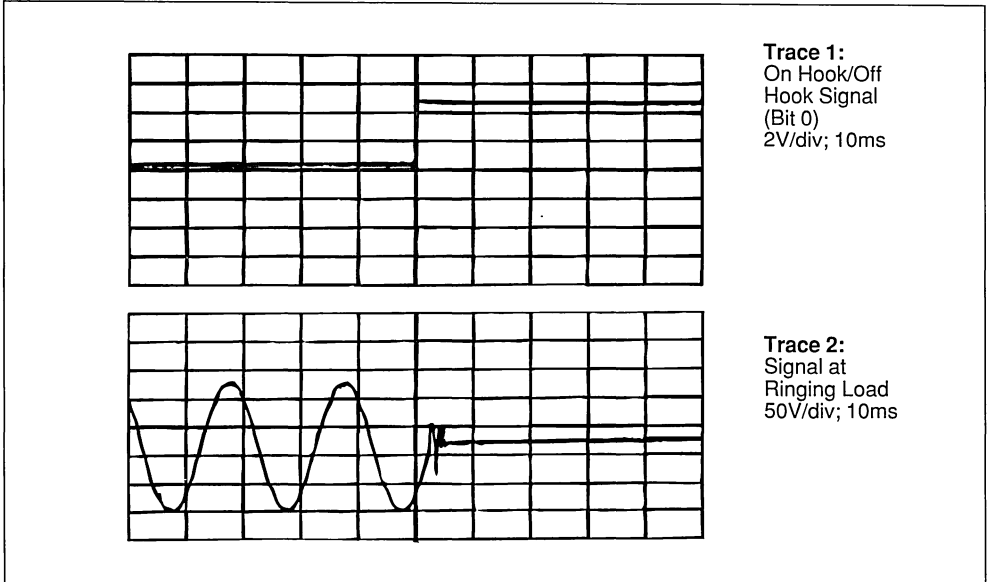
Figure 6: Ring Trip Detection – PBL 3762 – in presence of Longitudinal Current I_L = 5mArms/wire; F_{IL} = 25Hz; (R_L = 2KΩ; 2REN; F_{RING} = 50Hz)

Trace 1:
On Hook/Off
Hook Output
(Pin 14)
2V/div; 10ms

Trace 2:
Signal at
Ringing Load
50V/div; 10ms
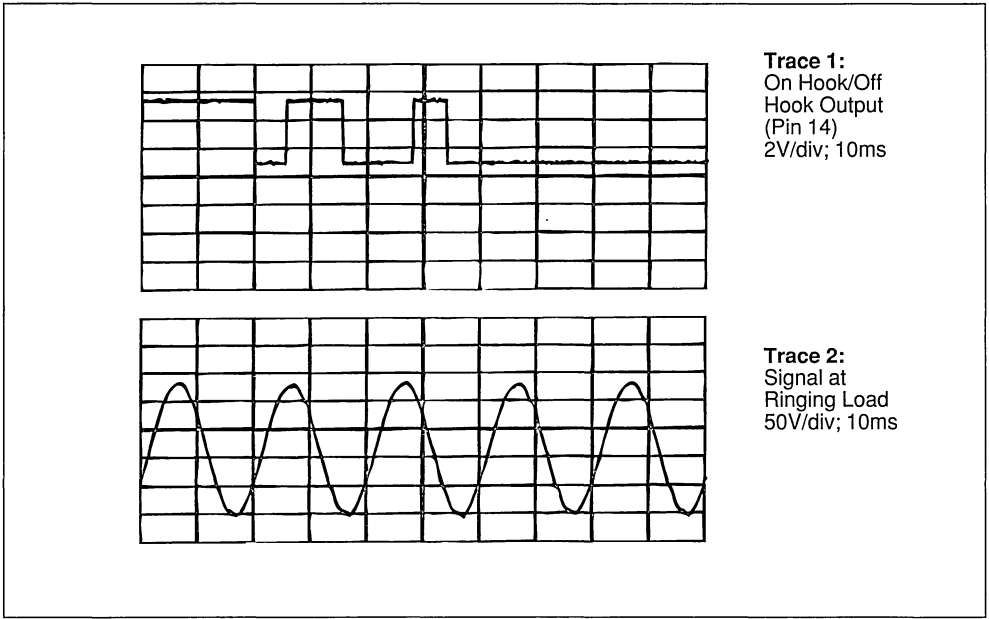
Figure 7: Ring Trip Detection – TDB 7722/11 – in presence of Longitudinal Current I_L = 5mArms/wire; F_{IL} = 25Hz; (R_L = 2KΩ; 2REN; F_{RING} = 50Hz)

Trace 1:
On Hook/Off
Hook Signal
(Bit 0)
2V/div; 10ms

Trace 2:
Signal at
Ringing Load
50V/div; 10ms

SGS-THOMSON
MICROELECTRONICS
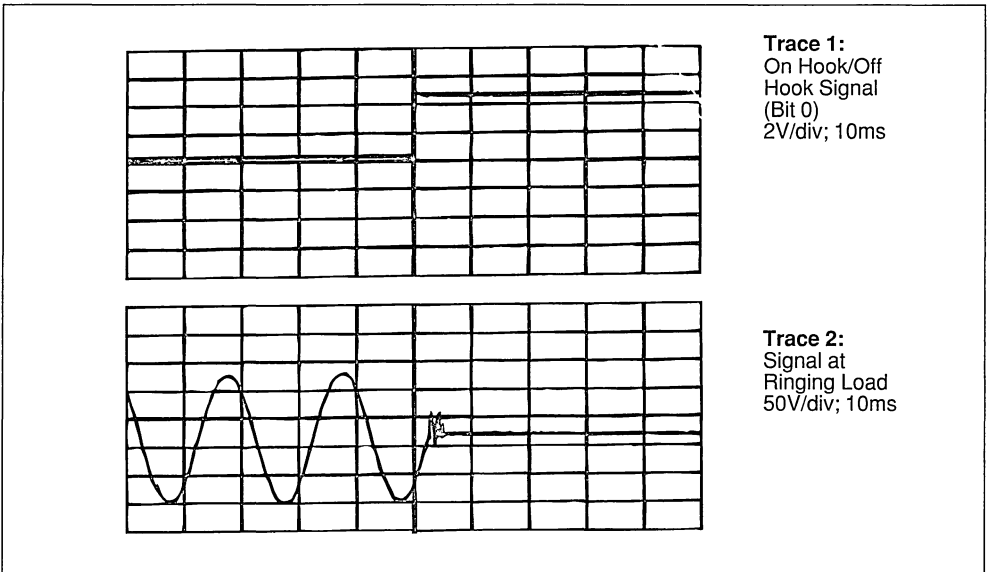
Figure 8: Ring Trip Detection − PBL 3762 −in presence of Longitudinal Current I_L = 15mArms/wire; F_{IL} = 25Hz; (R_L = 2KΩ; 2REN; F_{RING} = 50Hz)

Trace 1:
2V/div; 10ms

Trace 2:
50V/div; 10ms
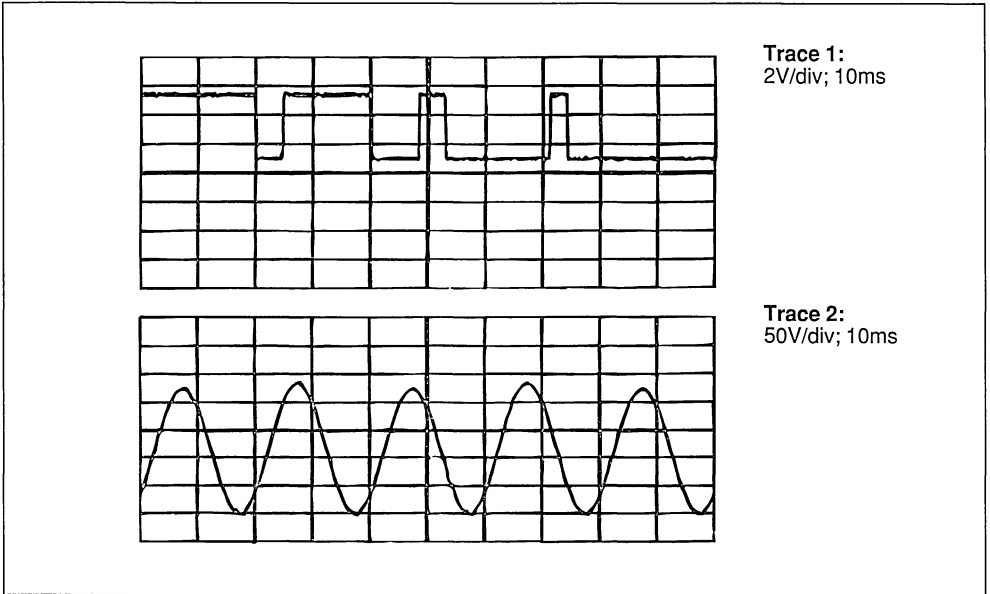
Figure 9: Ring Trip Detection − TDB 7722/11− in presence of Longitudinal Current I_L = 15mArms/wire; F_{IL} = 25Hz; (R_L = 2KΩ; 2REN; F_{RING} = 50Hz)

Trace 1:
On Hook/Off
Hook Signal
(Bit 0)
2V/div; 10ms

Trace 2:
Signal at
Ringing Load
50V/div; 10ms
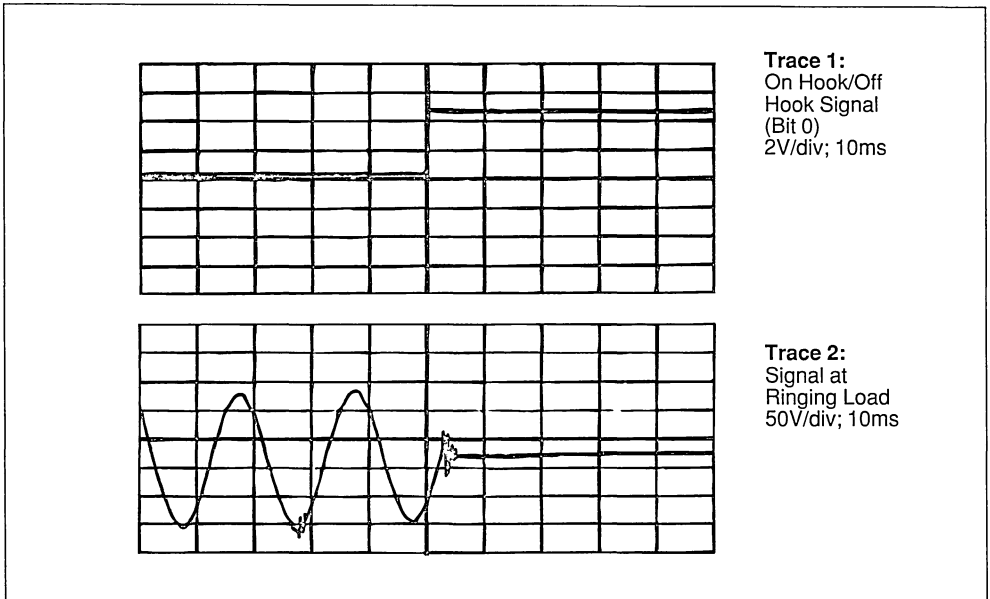
11 – AUTOMATIC RING SIGNAL DISCONNECTION

This function allows to interrupt the ringing signal at the first zero crossing when the off-hook condition is detected without any software control. (see fig. 3)

TDB	PBL
Yes.	Not implemented. It must be performed by software.

TDB SLIC solution allows to semplify controller software and to improve ring trip performances.

12 – LONGITUDINAL BALANCE

This function concerns the possibility for the SLIC to reject common mode signal present on the line.

TDB	PBL
Yes. Max longitudinal current = 70mAp/wire	Yes. Max longitudinal current = 20mAp/wire

From our test we have seen that for ERICSSON SLIC the electrical characteristic remains unchanged with longitudinal current less than 20mAp/wire; over 25/30mAp the performances of ERICSSON decrease drammatically and the device can't be used. For example fig.10 shows how the distortion becomes unacceptable when longitudinal current reaches about 25mAp.

With TDB SLIC solution, also in presence of current inversion on each wire, the performances are unchanged and no significative distortion is introduced, as fig.11 evidently shows. TDB SLIC allows to shift the threshold of correct working for longitudinal current up to 70mAp for each wire(with Itr=30mA).

Figure 10

SGS-THOMSON
MICROELECTRONICS
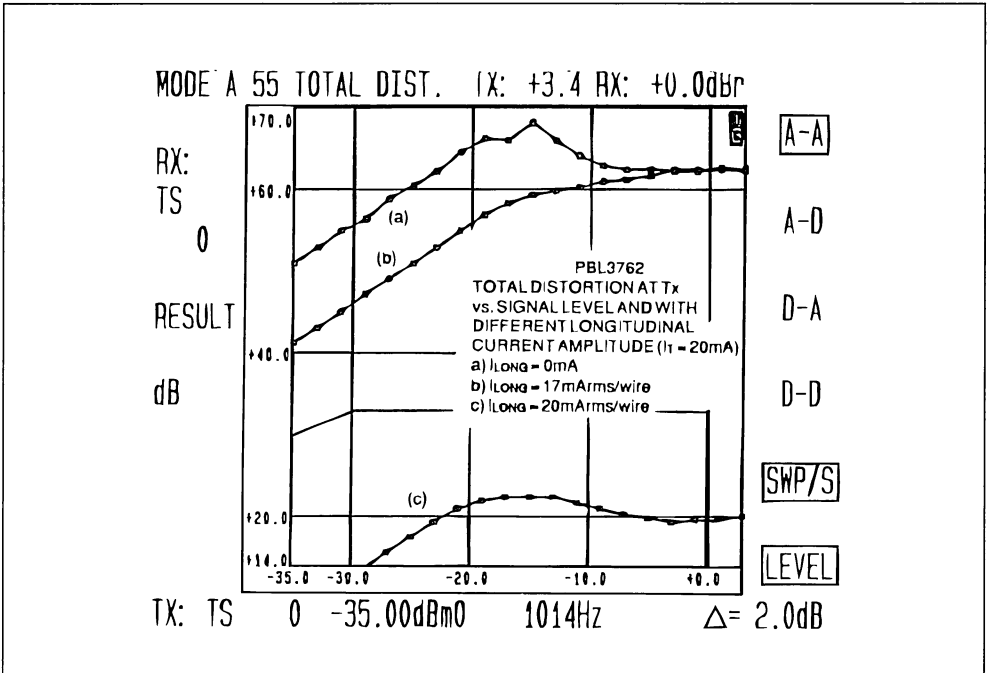
Figure 11
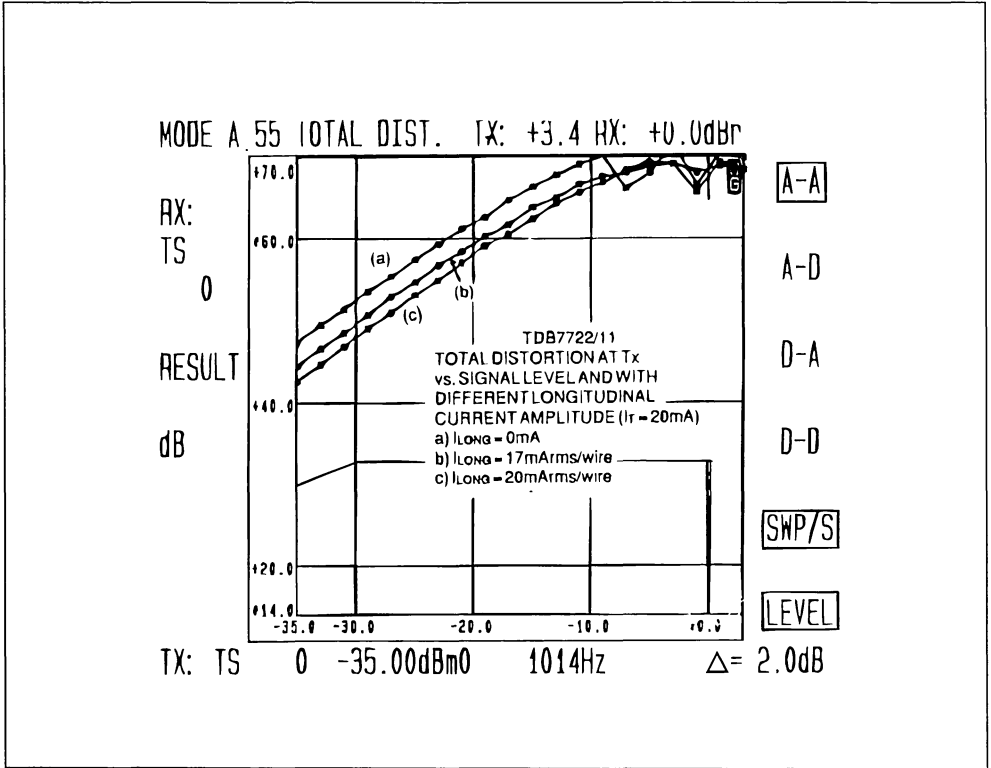
13 – POWER SUPPLY REJECTION RATIO

This function allows the rejection of noises that are present on the battery voltage.

TDB	PBL
Yes. The signal are rejected both in transversal and common mode. (typ. 50dB @ 20 Hz)	Yes, but the signal is transferred to tip/ring wires as a common mode signal with only 6dB of attenuation.

In the figures from 12 to 17 you can see the comparison results about PSRR. The test was realized superimposing 100mVrms (20Hz < f < 3600Hz) to the battery voltage and measuring the spurious signal at line, at Tx terminals, and between one Line terminal and ground. Fig. 12 and 13 show that ERICSSON SLIC has better performances in transversal respect to TDB, but from fig.14 you can see that with ERICSSON SLIC the

noise is simply transferred to each Line terminals as common mode signal with a little attenuation of 6dB.

On the contrary fig.14 shows that TDB realizes a real rejection both in Transversal way (between tip and ring) and in Common Mode way (between tip or ring and ground).

Fig.15,16,17 show the rejection for a 200mVpp square wave of 10Hz and a 200mVpp sinusoidal wave of 20KHz.Once again you can see how only TDB realize a real noise rejection. That means that for ERICSSON SLIC the noise that is present on the battery voltage is transferred into the line as common mode signal; this can be dangerous for two reasons:

- can induce transversal signal on the closer lines
- every unbalancement present on line generates a transversal signal.

Figure 12

SGS-THOMSON
MICROELECTRONICS
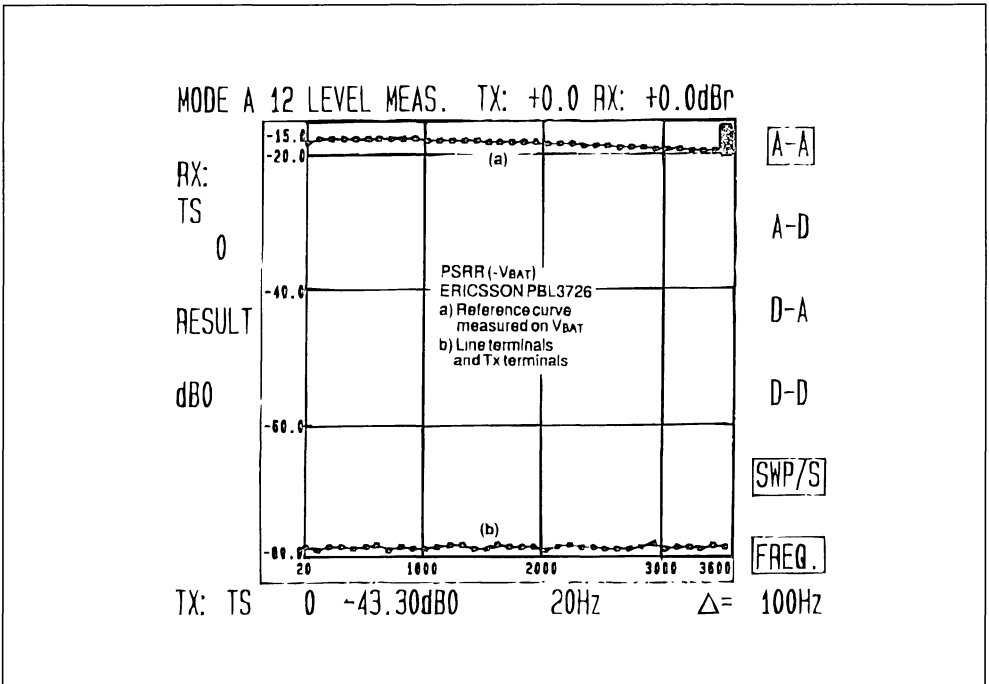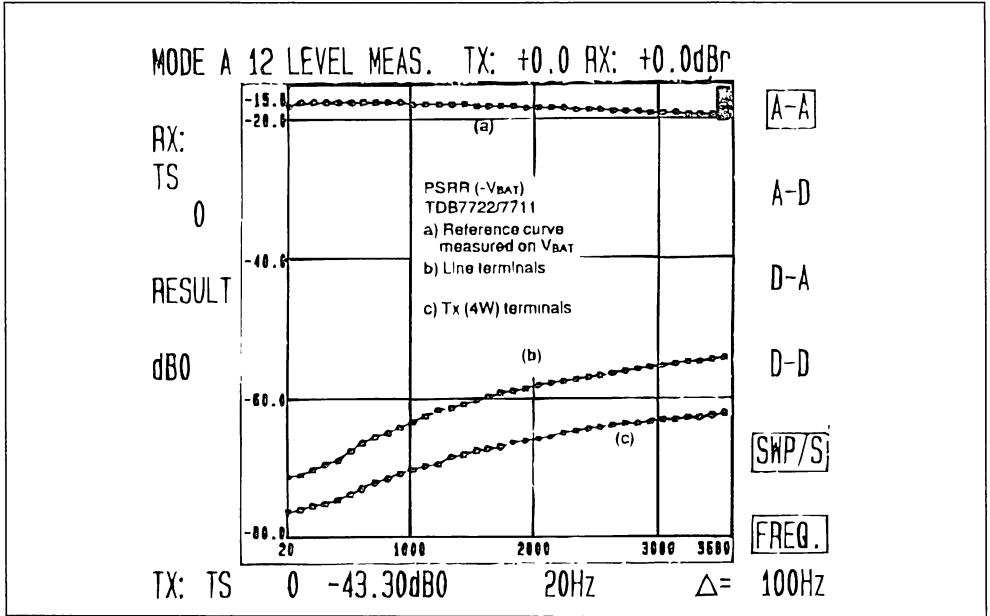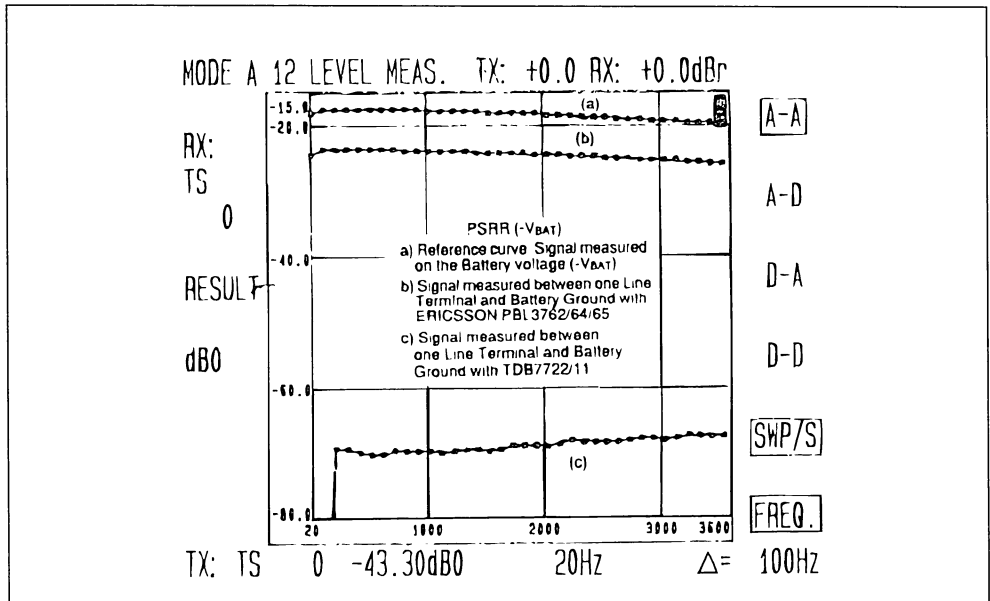
Figure 13

Figure 14

Figure 15: PSRR - ERICSSON PBL3762/64/65 (V_{BAT} = -48V +200mVpp (10Hz) square wave)

Trace 1:
Signal between
Tip and
Battery Ground
50V/div; 20ms

Trace 2:
Signal between
Ring and
Battery Ground
50V/div; 20ms
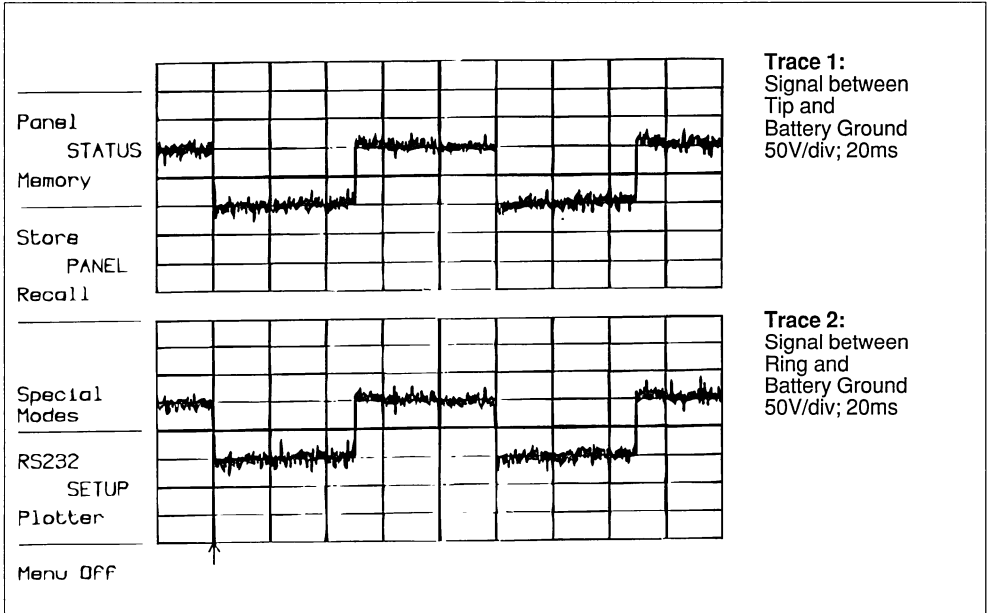
Figure 16: PSRR - ERICSSON PBL3762/64/65 (V_{BAT} = -48V +200mVpp (20KHz))

Trace 1:
Signal between
Tip and Battery Ground
50mV/div; 10μs

Trace 2:
Signal between
Ring and Battery Ground
50mV/div; 10μs

SGS-THOMSON
MICROELECTRONICS
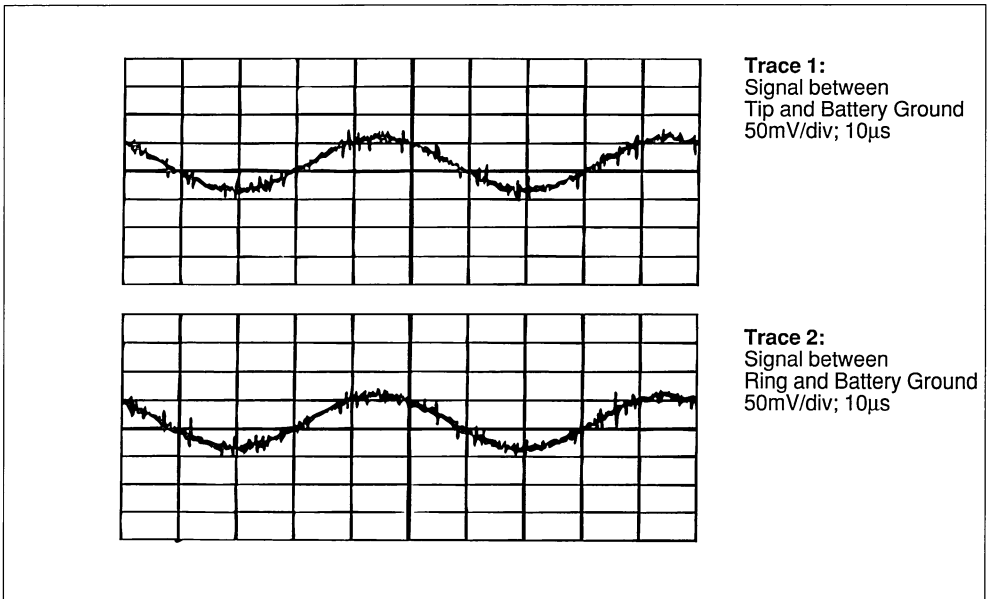
Figure 17: PSRR - TDB7722/7711 (V_{BAT} = -48V +200mVpp (20KHz))

Trace 1:
Signal between Tip
and Battery Ground
50mV/div; 10µs

Trace 2:
Signal between Ring
and Battery Ground
50mV/div; 10µs
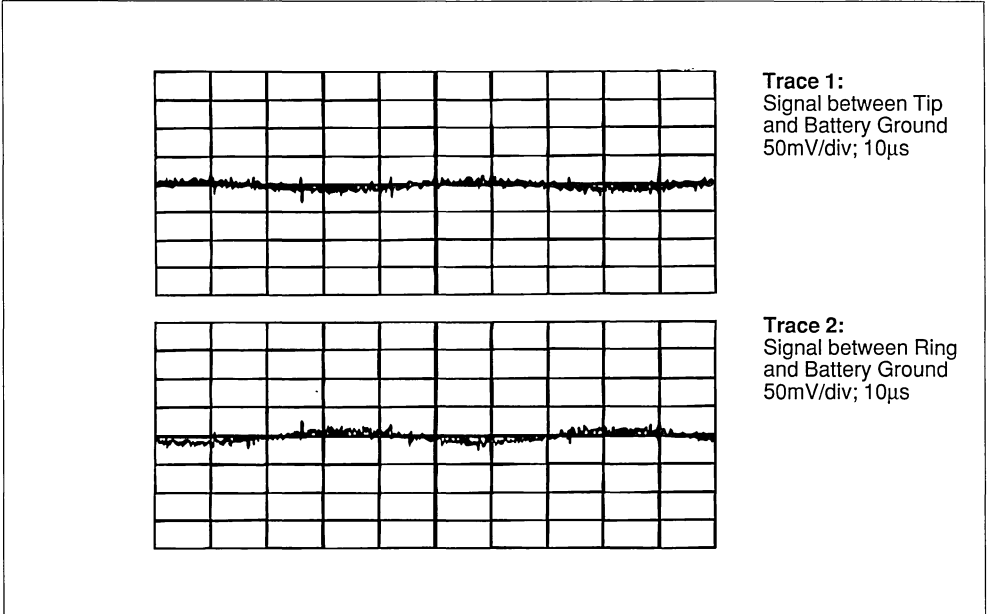
14 – SURGE PROTECTION

This function provide the SLIC to tolerate over-voltage on Tip or Ring wire.

TDB	PBL
Yes. Tolerate permanent negative voltages up to -80V. Protection circuit is built in. Difference between BGND and AGND=+/-2V	Yes. Do not tolerate permanent voltages more negative than VBat. Difference between BGND and AGND = +/- 0.3V

Both TDB and ERICSSON SLIC need external protections. TDB solution doesn't require expensive protection allowing to use greater values of external resistors and tolerating also permanent overvoltages.

Batt.Ground - Analog Ground=2V in TDB permits not to damage the device when in presence of surges the battery ground moves respect to the analog ground.

15 – THERMAL RESISTANCE

This performance allows to determine the quantity of power that the device can manage with no problem.

TDB	PBL
RTHj-a = 35/40° C/W	RTHj-a = 50° C/W
RTHj-c = 3° C/W	RTHj-c = 15/20° C/W

The junction to case Thermal Resistance (RTHj-c) is very low for TDB. This is an excellent performance of the Multiwatt package that allows to manage high values of power.This performance allows to keep as low as possible the junction temperature, and the case temperature almost equal to it.

ERICSSON SLIC has a RTHj-c much higher than TDB, SLIC therefore also if the case temperature is almost the same of TDB, the junction temperature will be higher.

Let's make an example:

The SLICs are dissipating 1Watt with TAmb.=50°C.

Calculate the case and junction temperature.

$$TJ = TA + PD*RTHj\text{-}a$$
$$TC = TJ - PD*RTHj\text{-}c$$

For TDB SLIC: TJ = 115°C   TC = 112°C

For ERICSSON SLIC: TJ = 130°C   TC = 110°C

SGS-THOMSON
MICROELECTRONICS

As you can see the junction temperature of the ERICSSON SLIC is much higher than TDB, and this reduce the reliability and the life lenght of the ERICSSON compared to TDB SGS-THOMSON SLIC.

Infact generally the life lenght of the semiconductor devices is reduced to the 50% for every increment of 20°C of the junction temperature.

16 – THERMAL SHUTDOWN

This function allows the SLIC to reduce to zero the current when the device reaches a temperature guard value. In this way it avoids to damage permanently the device.

TDB	PBL
Yes. A software information is provided (BIT3)	Yes.

The thermal shutdown of the TDB and ERICSSON SLIC happens when the internal junction temperature reaches 150°C and 145°C respectively.

The power that the SLIC must dissipate to reach this temperature is a function of the thermal resistance between the junction and the ambient (RTHj-a) and of the ambient temperature. At a case temperature higher than 100°C the RTHj-a is 35C/W for TDB and 50°C/W for ERICSSON. That means that at 25°C the SLICs can dissipate:

For TDB SLIC: $\dfrac{150°C - 25°C}{35° C\backslash W} = 3.6\ Watt$

For ERICSSON SLIC: $\dfrac{145°C - 25°C}{50°C\backslash W} = 2.4\ Watt$

From this it's important to say that TDB SLIC can manage higher power before interrupting the operative mode and to go in shutdown. In particular this is important with the allowed highest ambient temperature 85°C. In this condition TDB SLIC can manage up to 1.85 Watt before going in shutdown, while the ERICSSON SLIC only 1.2 Watt. This will limit the maximum value of the limiting current. Infact in order to allow the service also with a short line, with TAmb.=85°C the following condition must be verified:

$$VBatmax * (ITmax + IBiasmax) < \begin{matrix} 1.2W \text{ with ERICCSON} \\ 1.8W \text{ with TDB} \end{matrix}$$

where:

- VBatmax is the maximum battery voltage
- ITmax is the maximum transversal current delivered to the line.
- IBiasmax is the maximum bias current that the slic needs for its internal operations.

Assuming VBatmax = 48 + 10%   = 52.8V
          TDB   IBTiasmax = 7mA
          ERICSSON   IBiasmax   = 4mA

you obtain
          ERICSSON   ITmax   = 18.6mA
          TDB   ITmax   = 27mA

You can clearly see that with ERICSSON SLIC you have to program the limiting current lower than 19mA in order to guarantee the operation with a short line at 85°C. With TDB SLIC this value can increase up to 27mA.

SGS-THOMSON
MICROELECTRONICS

LINE CARD CIRCUITS FOR U.S. MARKET

by W. Rossi

HIGHLIGHTS

- CONFORMANT TO BELLCORE TRANSMISSION SPECIFICATIONS

- OUTSTANDING RELIABILITY BASED ON HV/LV PARTITIONING

- -40 TO +85°C OPERATION

- 61dB MIN. GUARANTEED LONGITUDINAL/TRANSVERSAL CONVERSION

- CONFORMANT TO BELLCORE SURGE & POWER CROSS SPECIFICATIONS

- OUTSTANDING ON-HOOK TRANSMISSION CHARACTERISTICS

- MINIMAL EXTERNAL COMPONENT COUNT

- VERY LOW POWER CONSUMPTION

This application note describes subscriber application circuits that meet the U.S. specification explained in Technical Reference TR-TSY-000057, Issue 1, April 1987 and TR-TSY-00050, Issue 3, March 1989 by Bell Communications Research. This application is based on :

- SLIC KIT TDB7711/7722
- ETC5054 CODEC/FILTER or TS5070/1 PROGRAMMABLE 2nd GENERATION CODEC/FILTER
- Solid state protections SMTHDT58 and SMTHDT200

The main subjects analyzed in the following pages are:

- DC characteristic
- AC performances
- ON/HOOK transmission
- Longitudinal Balance
- Protections

Fig.1 and 2 show two applications using respectively a 1st or a 2nd generation Codec/Filter.

Additional informations can be found in the SGS-THOMSON Line Card databook (1st edition,October 89).

Figure 1: TDB7722/7711 Application with 1st Generation Codec/Filter
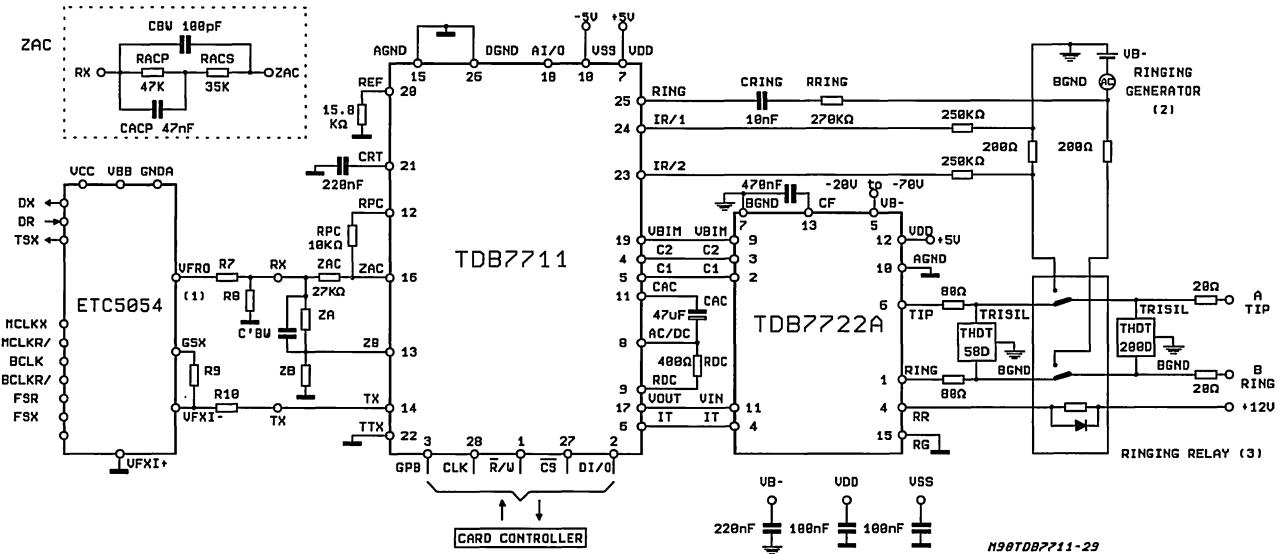
(1) RESISTORS FROM R7 to R10 PROGRAM TX/RX GAINS

(2) THE RINGING GENERATOR CAN BE CONNECTED
ALSO IN WITH BALANCE CONFIGURATION

(3) THE RINGING RELAY CAN BE DRIVEN EITHER BY
POSITIVE VOLTAGE (+5V/+12...)V OR BY NEGATIVE VOLTAGE (-24/-48...)V

M98TDB7711-29

Figure 2: TDB7722/7711 Application with 2nd Generation Codec/Filter

ZAC

CBW 100pF

RX — RACP — RACS — ZAC
47K   35K

CACP 47nF

-5V +5V

AGND DGND AI/O VSS VDD
15   26   18   10   7

REF
20

15.8 KΩ

CRT
21

220nF

TTX
22

RPC
12

RPC 10KΩ

ZAC 16

ZAC 27KΩ

ZA 91KΩ ZB 13

ZB 34KΩ

CTX 0.1uF

TX 14

(3)

TDB7711

VSS VCC GND

DX0   IL0
DX1 (3) IL1
DR0   IL2
DR1   IL3
         IL4
FSX   IL5
FSR   MR
BCLK

TSX0 TS5070 VFRO
TSX1

MCLK
CS
CCLK
CO   VFXI-
CI

GPB CLK R/W CS DI/O
3   20   1   27 2

CARD CONTROLLER

RING
25

CRING RRING
10nF   270KΩ

IR/1
24

250KΩ

IR/2
23

250KΩ 200Ω 200Ω

470nF -20V to -70V
BGND   CF   VB-
7   13   5

VBIM VBIM
19 9
C2   C2
4   3
C1   C1
5   2
CAC
11
47uF CAC
AC/DC
8
400Ω RDC
RDC
9
VOUT VIN
17   11
IT   IT
6   4

TDB7722A (3)

VDD
12 +5V
AGND
10
TIP
6   80Ω
RING
1   80Ω
RR
4
RG
15

VB-
220nF

VDD
100nF

VSS
100nF

M98TDB7711-30

VB-
RINGING GENERATOR
(1)

BGND AC

TRISIL THDT 50D BGND
TRISIL THDT 200D BGND

20Ω A TIP
20Ω B RING

+12V

RINGING RELAY (2)

(1) THE RINGING GENERATOR CAN BE CONNECTED
    ALSO IN WITH BALANCE CONFIGURATION
(2) THE RINGING RELAY CAN BE DRIVEN EITHER BY
    POSITIVE VOLTAGE (+5V/+12...)V OR BY NEGATIVE VOLTAGE (-24/-48...)V

DC FEEDING CHARACTERISTIC

In active mode TDB SLIC can work with three different kinds of DC characteristic; for this specific application the "Apparent Battery" characteristic is suggested. In this mode three feeding conditions are available: current limiting region (1)(seven software programmable values), resistive feeding region(2) and a nearly constant voltage region (3). In the region (2) TDB SLIC shows an apparent voltage of 48V whatever the actual battery voltage is.

Feeding resistance value is a function of external protection resistors Rp and of one programming resistor RDC connected between pin 8 and 9 of TDB7711.In our application a 2x200ohm feed resistance is provided using two 100ohm external protection resistors and a 400ohm RDC resistor (see fig1 and 2).

Fig.3 shows the line current vs the loop resistance for two different battery voltages, 48V and 52V,and a programmed current limitation of 30mA.We can note that with 48V of battery voltage the line current is higher than 20mA for loop resistance up to 1550ohm and with 52V of battery voltage the line current is greater than 18mA for 1930ohm loop resistance.

Informations about the other two DC characteristics (Real Battery and Special Characteristic) can be found on the Line Card databook.

Figure 3: TDB7711/7722 SLIC KIT Line Current vs Loop Resistance Ilim = 30mA; RFS = 200ohm; Rp = 100ohm
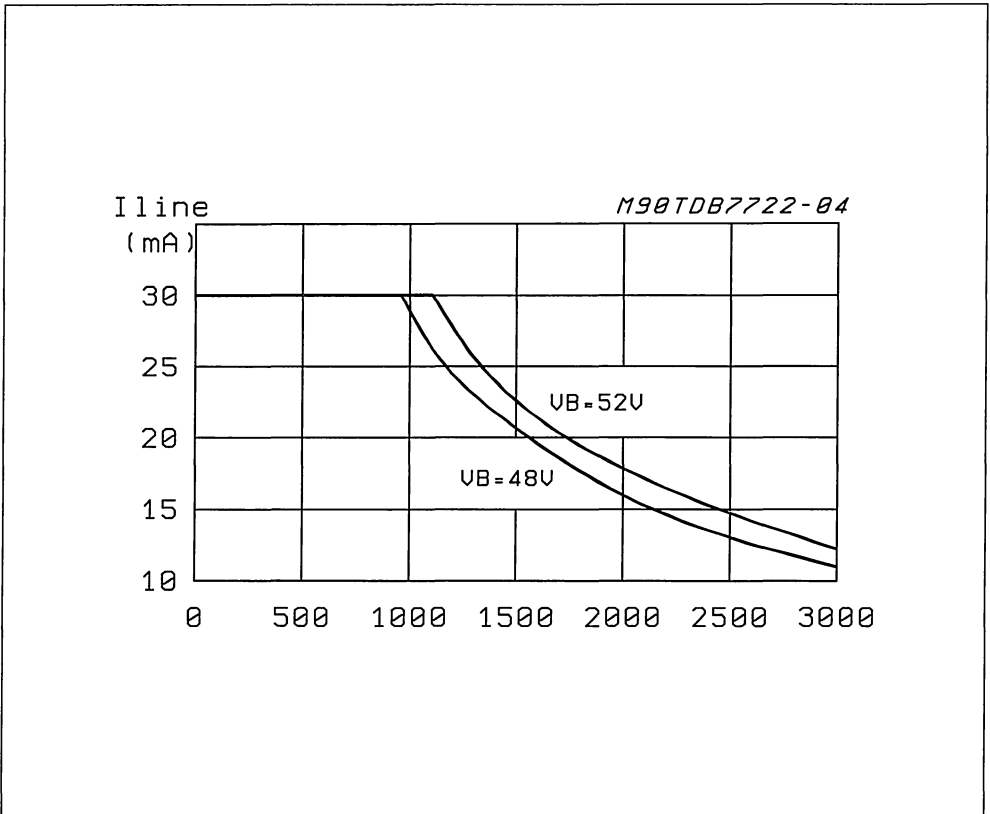
AC PERFORMANCES

1- Return Loss

Fig.4 shows the typical Return Loss measurement, obtained with our application,working with a 900ohm+2.16uF test network.

In particular the following values are guaranteed:

>20dB for 200Hz < f < 500Hz
>26dB for 500Hz < f < 3400Hz

4/12

SGS-THOMSON
MICROELECTRONICS

Figure 4: TDB7722/7711 Return Loss Measurement with 900Ω = 2.16µF Test Network
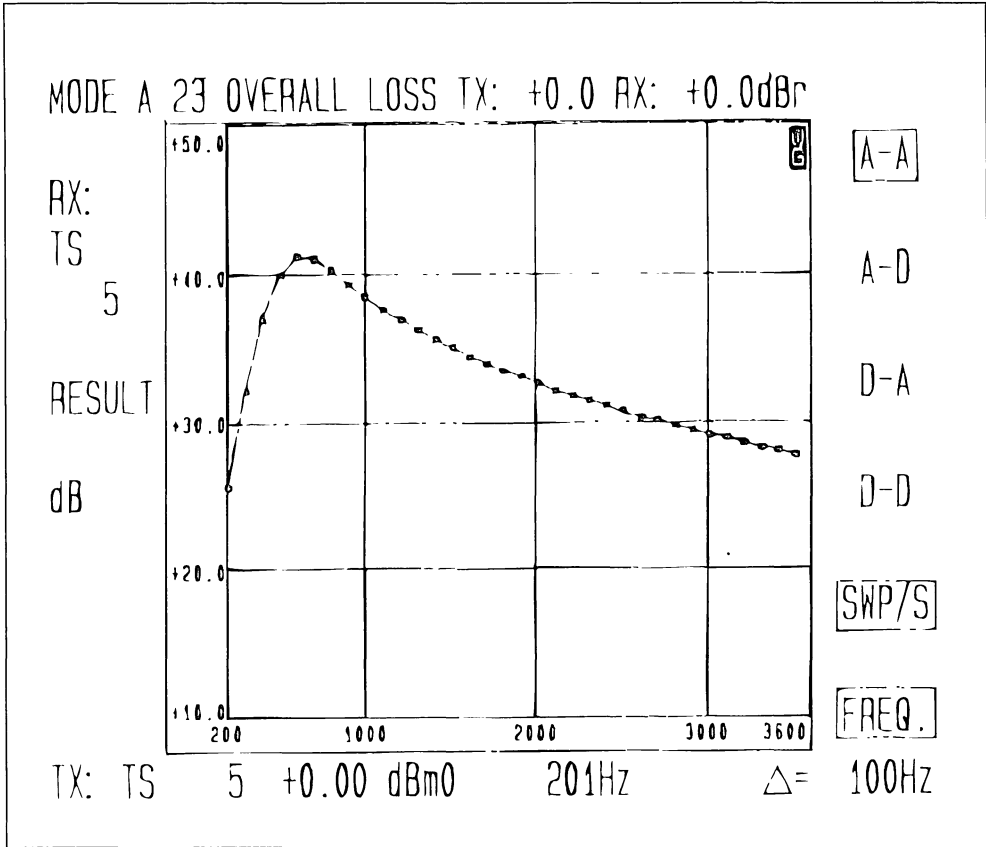
The proper output impedance is sinthetyzed by one external scaled network ZAC(x50), connected between Rx input and pin 16 of TDB7711 and by a RPC resistor(between pin 12 and pin 16 of TDB7711) that depends on the external protection resistors. CBW is a compensation capacitor needed for system loop stability (inserted between Rx and pin 16 of TDB7711).

2- Trans Hybrid Loss

For U.S. market the echo cancellation performances have been analyzed using four different test networks:

-Loaded line ZLL
1650ohm // (0.005µF+100ohm)

-Not loaded line ZL
800ohm // (0.05µF+100ohm)

-Special service line and remote terminal ZT (900ohm+2.16µF)

-Remote terminal/2 ZR (900ohm)

When the TDB SLIC is used with a 1st generation CODEC/FILTER (ETC5054) the hybrid function is performed by the SLIC by two external network impedances.These impedances are constituited by a ZA impedance (between Rx input and pin 13 of TDB7711) with a C'BW capacitor in parallel, and by a ZB impedance (connected between the analog ground and pin 13 of TDB7711).

Table 1 describes in particular how these impedances are organized in the different working situations we have explained before.

Figure 5 shows the different typical Trans-Hybrid Loss measured performances.

If you use a SGS-THOMSON TS5070/1 2nd generation CODEC/FILTER, you can save a lot of

Table 1

T.H.L. TEST NETWORK		ZA	C'BW	ZB
1650Ω / 100Ω 5nF	NON LOADED LINE	82nF / 45K 47K	150pF	39K / 1.05nF
800Ω / 100Ω 50nF	LOADED LINE	82nF / 45K	100pF	79K / 110pF
900Ω 2.16uF	SPECIAL SERVICE LINE AND REMOTE TERMINAL	92K	NOT MOUNTED	92K
900Ω	REMOTE TERMINAL/2	47K / 45K 47nF	100pF	45K

M90TDB7711-32

Figure 5: T.H.L. Measurements with Different Test Networks; (1) Loaded Line; (2) Not Loaded Line; (3) Special Service Line and Remote Terminal; (4) Remote Terminal/2
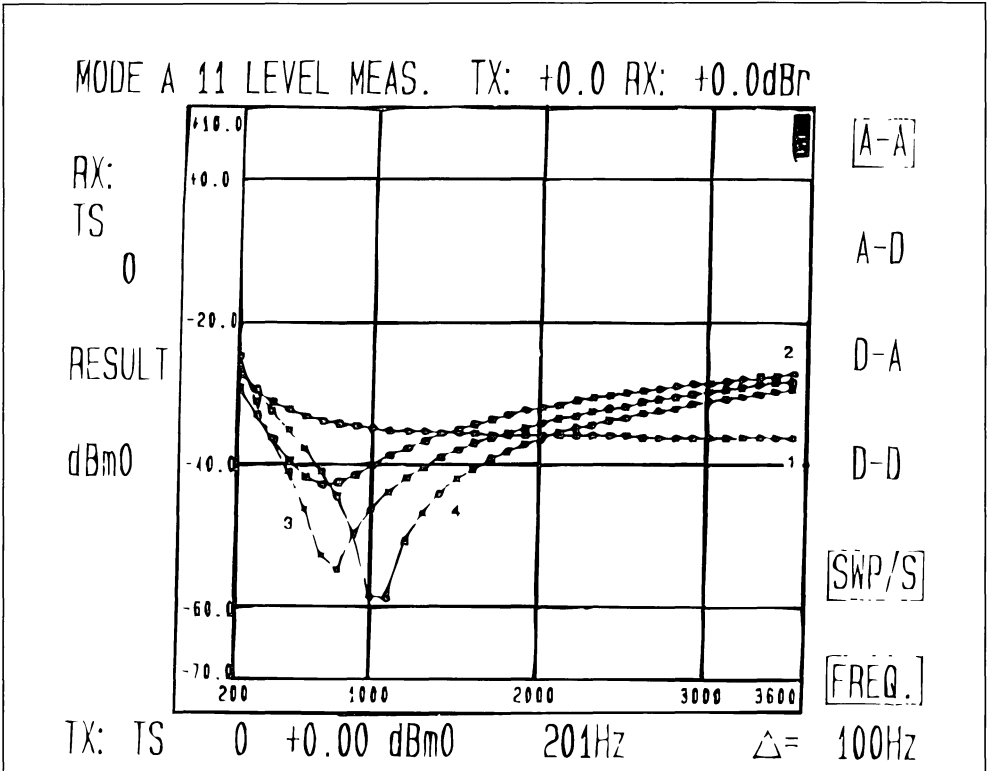
external components: in fact the hybrid function is performed into the TS5070/1 using a programmable hybrid balance (HYBAL) filter. Therefore the four different configurations are simply programmed by software and no external component changement are necessary, in particular ZA is only a resistor of 91Kohm and ZB a resistor of 34Kohm(see fig.2). Table 2 shows the hybrid balance coefficients that are used to program the HYBAL filter and the corresponding typical results.

In addition fig.6 shows the measurements we have obtained with the four different test networks, using a 2nd generation Codec/Filter and the same external components for all the different situations.

Table 2

T.H.L test network	TS5070/1 HYBAL Programming Coefficients	ERL [dB]	SRLLO [dB]	SRLHI [dB]
Loaded Line	E0; 30; 44	41	32	45
Not Loaded Line	F4; 60; 90	35	30	26
Special Service line and remote terminal	F2; 05; 8C	42	32	37
Remote Terminal/2	F2; 50; 8C	39	37	38

Figure 6: T.H.L. typical results with the TS5070/1 using ZA = 91KΩ, ZB = 34KΩ and four different test network; (1) Loaded Line; (2) Not Loaded Line; (3) Special Service Line and Remote Terminal; (4) Remote Terminal/2
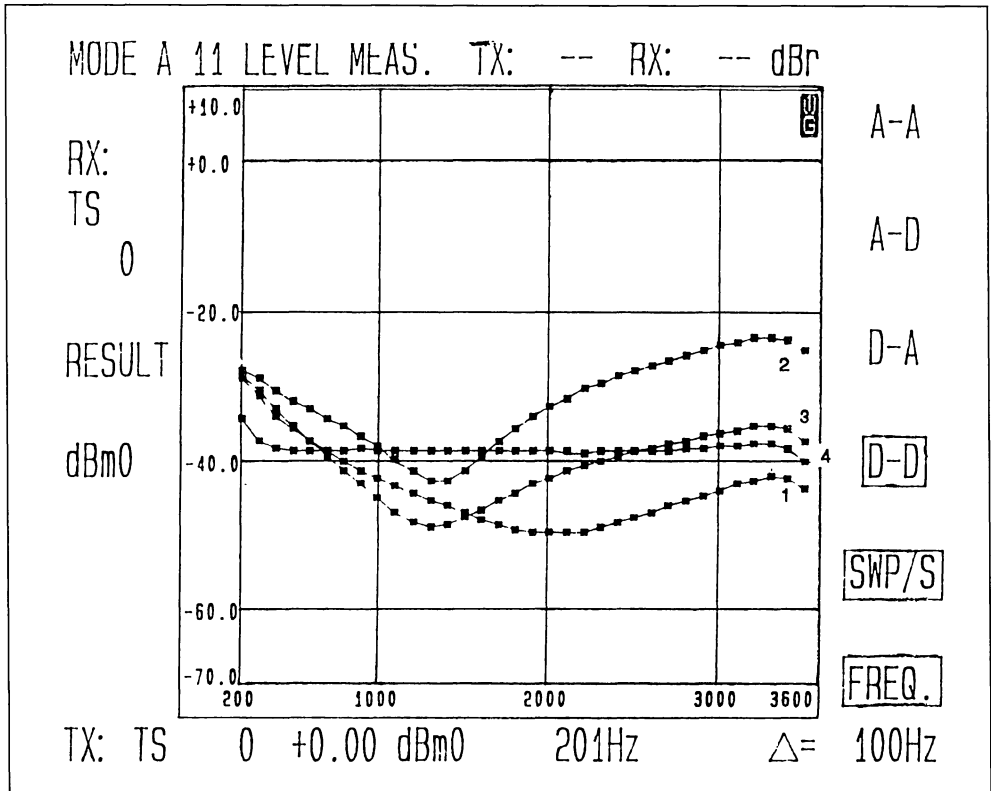
3- Tx and Rx gains

Guaranteed values for Tx and Rx gains are:

absolute value   0+/-0.15 dB   f=1020Hz VRx=VTx=0dBm

linearity(f=1020Hz)
   +/-0.05dB, VRx or Vtx -3 to -40dBm
   +/-0.1dB -40 to -50dBm
   +/-0.2dB -50 to -55dBm

flatness +/-0.15 dB   300Hz < f < 3400Hz   respect to f = 1020Hz

It's important to note that the gain loss due to the external protection resistors, is recovered by RPC resistor inserted between pin 12 and pin 16 of TDB7711.

Additional informations can be found on Line Card databook.

ON/HOOK TRANSMISSION

This function allows the transmission of signals also when the DC line current is equal to zero.

Due to the voltage drop between the battery and the Tip/Ring SLIC terminal, it is possible to transmit AC signals in on/hook condition without significative modification of all the AC performances guaranteed in off/hook condition.In particular:

-Tx and Rx gain: variation within 0.1dB
-Return Loss: no variation
-Trans-Hybrid Loss: variation within 3dB
-Long/Trans conversion: better than 58dB
-Distortion: no variation

LONGITUDINAL BALANCE

TDB SLIC (TDB 7722A) guarantees a L/M conversion performance better than 61dB measured with test circuit IEEE-Std 455-1976, Zml=900ohm.

It should be noted that the overall L/M conversion measured at line termination, beside the intrinsic SLIC L/M performance, depends on different factors:

- External protection resistors Rp tolerance
- External protection resistors Rp absolute value
- Impedance Zml that the SLIC shows to the line.

Fig.7 shows the worst case of L/M conversion in function of the protection resistors absolute value and their tolerance working with the TDB7722A SLIC. As we said before, a 100ohm RP value is suggested and in this case the maximum tolerance to be used to guarantee a L/M conv. better than 58dB is +/-0.3% in the worst case.

Figure 7: TDB7722A/7711 SLIC KIT L/M CONV. worst case versus Rp (Zml = 900)
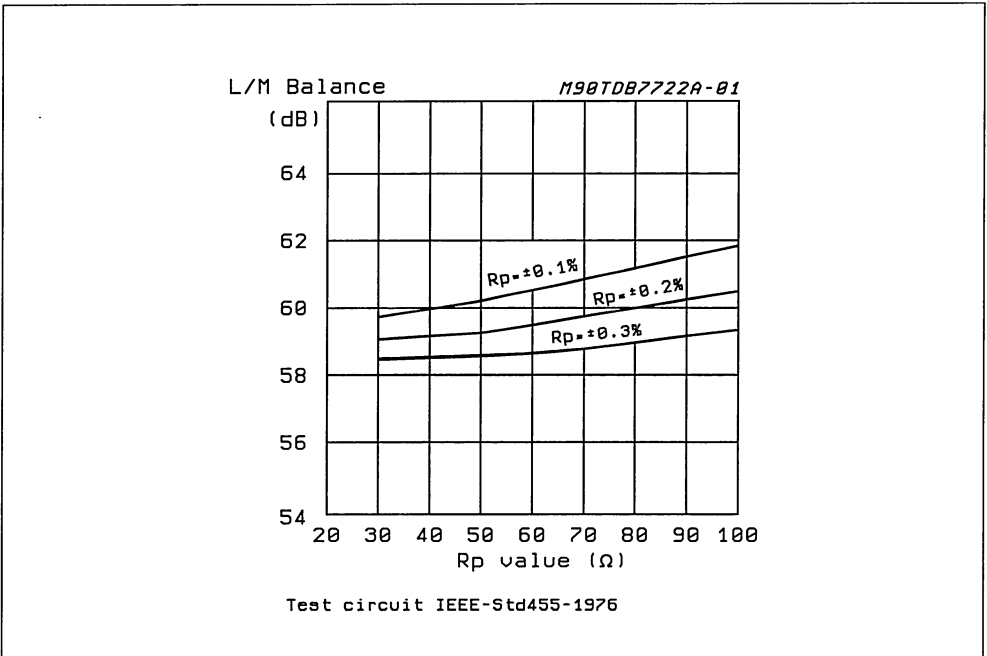
Fig.7 shows that the L/M conv. improves if the tolerance of Rp decreases.In addition, with very tight tolerance resistor, the L/M performance can be improved by increasing the external protection resistors value.

Finally, from the comparison between fig.7 and fig.8, you can note that longitudinal balance is better with Zml=600ohm rather than with Zml=900ohm. In particular, with Zml=600ohm and Rp=100ohm, can be obtained a L/M conversion greather than 64 dB and the maximum tolerance of Rp can increase to 0.7% still guaranteing a L/M

conv. better than 58dB in the worst case.

It's important to note that TDB SLIC has outstanding performances as immunity from high longitudinal current. It means that it can operate without degradation of the AC performances also in presence of high longitudinal current values. In particular fig.9 shows the L/M conversion as function of the longitudinal current peak value used to measure the L/M conversion. It's fundamental to point out that there is no significative degradation of L/M conv. up to 50mApeak per wire of longitudinal current.

Figure 8: TDB7722A/7711 SLIC KIT L/M CONV. worst case versus Rp (Zml = 600)
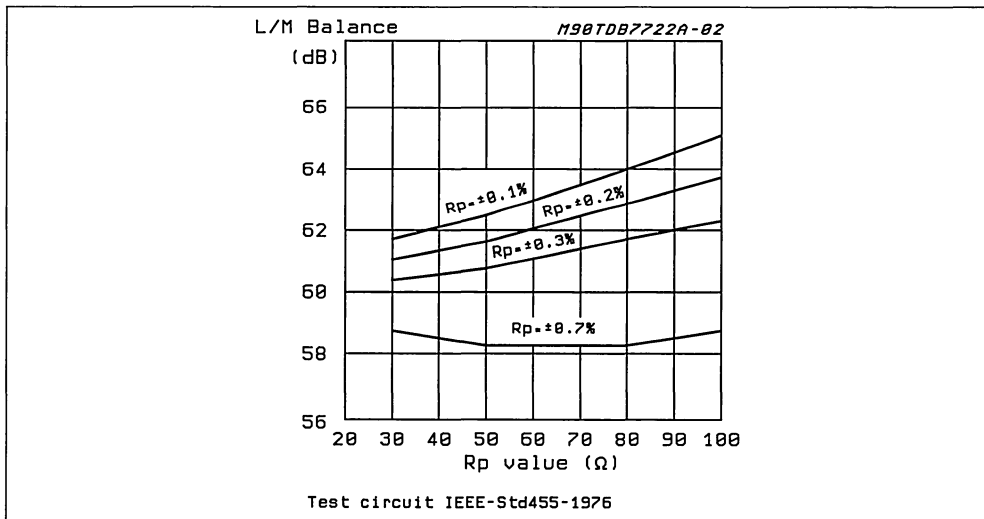
Figure 9: TDB7722A/7711 SLIC KIT L/M CONV. with 30mA loop current
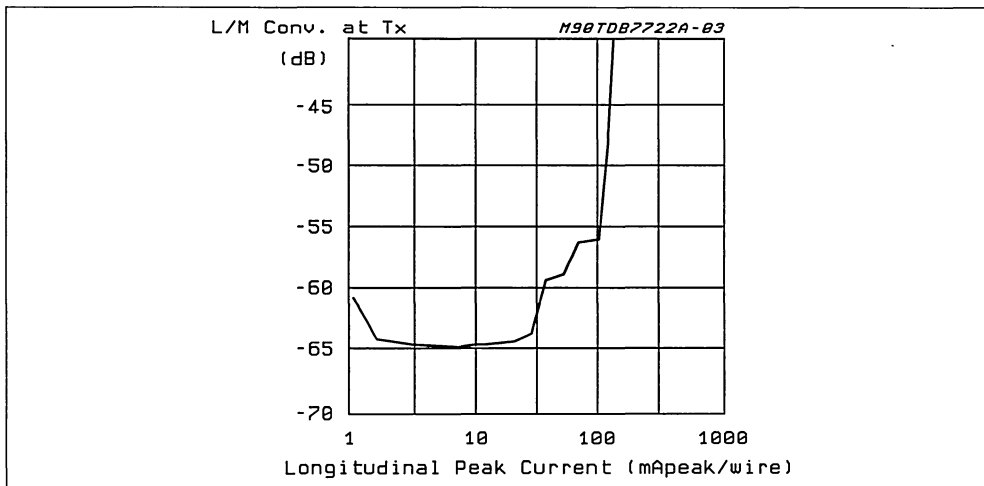
Additional informations on L/M conversion are shown in fig. 10. In particular you can see how the L/M balancement that improves at very low frequencies (20Hz), and it is still very good (45dB) at high frequencies(50KHz); in this way an exellent E.M.I. performance can be obtained.

Figure 10: TDB7722/7711 L/M conversion in 20Hz to 70KHz
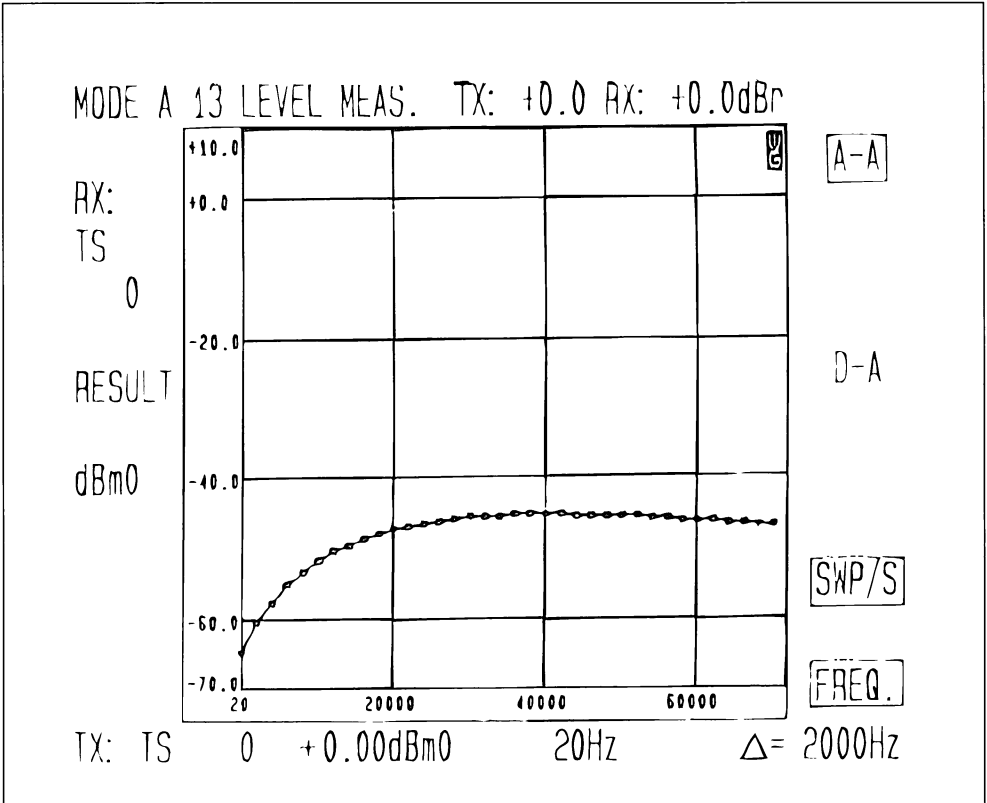
PROTECTIONS

The goal of this chapter is to show a protection diagram for TDB SLIC to withstand the lightning and the 60Hz disturbances of U.S. standard (Tr-TSY-000057 Issue 1, April 1987 of the functional criteria for digital loop carrier systems. Bell Communication Research).

TDB 7722 chip has integrated a protection circuit that allows the device not to be damaged when the line voltage is between battery voltage and -80Volts.In particular if the battery voltage is, for example, -48V, at the line terminals can be permanently connected negative voltages between -48 and -80 without that the device is damaged. For this reason the role of the external protection circuit will be to suppress all overvoltages greater than the ground and more negative than -80V.

The electrical protection of this standard defines two kinds of surge generators:

- A: lightning surge.
- B: 60Hz disturbances.

For these disturbances there are two test levels:

- The first level does not cause a damage on the protected module and the system must operate after the test.
- The second level can damage but without fire or electrical shock hazard.

A) Table 3 shows the tests with the lightning surges.

SGS-THOMSON
MICROELECTRONICS

Table 3

FIRST LEVEL SURGE TESTS (NO DAMAGE TO DEVICE)

Surge	Peak Voltage (V)	Waveshape (µs)	Peak Current (A)	Repetitions Each Polarity	Internal Serial Resistance
1	±600	10/1000	100	50	6
2	±1000	10/360	100	50	10
3	±1000	10/1000	100	50	10
4	±2500	2/10	500	10	5

SECOND LEVEL SURGE TESTS (DAMAGE BUT WITHOUT FIRE)

Surge	Peak Voltage (V)	Waveshape (µs)	Peak Current (A)	Repetitions Each Polarity	Internal Serial Resistance
1	±1000	10/2500	200	10	5
2	±5000	2/10	500	1	10

Lightning surges generate a current that is equal to peak voltage/(internal series resistance + protection resistance of the SLIC).

The first level of lightning surges standard shows that the most agressive is the surge number 3:it causes a current of 33A(1000V/(10ohm+20ohm) on the line.To withstand this kind of surge we suggest the SMTHDT58 which can suppress:

-75A for a surge of 10\1000usec waveform
-150A for a surge of 8\20usec waveform

In fig.11 you can find the protection configuration based on two SMTHDT58,each connected between one line terminal and ground.

Figure 11: Protections (1) These devices are the protections for the ringing circuit: for this reason they depend on the ringing generator and ringing relays characteristics

(1) THESE DEVICES ARE THE PROTECTIONS FOR THE RINGING CIRCUIT:
FOR THIS REASON THEY DEPEND OU THE RINGING GENERATOR AND
RINGING RELAYS CHARACTERISTICS
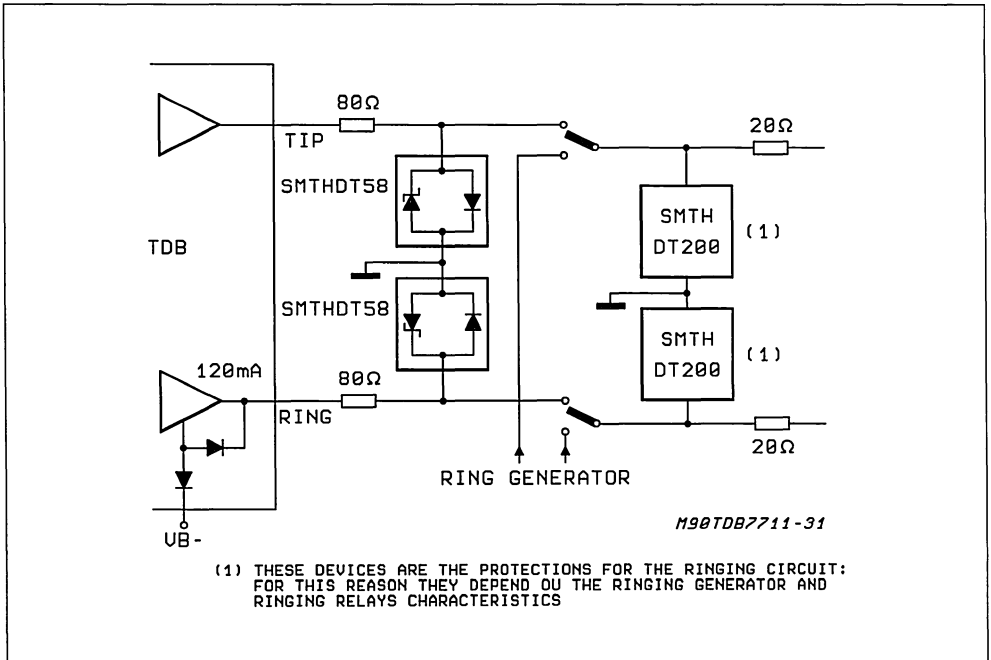
APPLICATION NOTE

SMTHDT58 protections are composed by a rectifier diode and a trisil.In this way:

- for positive overvoltages the rectifier diode clamps this wave to ground
- for negative overvoltages the trisil will fire

when a voltage falls under -80V(maximum breakdown voltage).

B) Table 4 shows the AC tests with 60Hz disturbances.

Table 4

FIRST LEVEL AC TESTS (NO DAMAGE TO DEVICE)

AC Test	60Hz Voltage (Vrms)	Resistance Per Line Conductor (Ω)	Duration	Primary Protectors
1	0 - 50	150	15 min	Removed
2	50 - 100	600	15 min	Removed
3	100 - 600	600	60 1 sec applications	Removed
4	1000	1000	60 1 sec applications	Operative Protector in place
5			60 5 sec applications	Removed

SECOND LEVEL AC TEST (DAMAGE WITH NO FIRE)

AC Test	Test For	60 Hz Voltage (Vrms)	Source Resistance (Ω)	Duration
1	Secondary Power Contact	0 - 300	3	15 min
2	Primary Power Contact	300 - 600	3	5 sec
3	Fault Induction	0 - 600	600 per conductor	15 min
4	High Impedance Induction			15 min

The first level AC test shows:

- Long duration surges 1 and 2
- Short duration surges 3,4 and 5

For short duration surges, SMTHDT58s withstand these surges without problem.

For long duration surges, there are two cases:

- The peak voltage of the wave don't exceed the breakdown value(VBR) and there is no power dissipated on the SMTHDT58.
- The peak voltage of the wave goes over the breakdown point(VBR) and there is power on the SMTHDT58.

The worst case is obtained with the AC test n.2(100Vrms).For this application the calculation of the maximum RTH accetable and the graphic of fig.12(Thermal resistance junction-ambient versus CU surface) allows to know that SMTHDT58 protections can withstand this surge with Copper surface of 2.5 cm^2 on the printed board for each of the protection device.

Figure 12: Thermal Resistance Junction - ambient vs. Copper Surface (printed circuit).

SGS-THOMSON MICROELECTRONICS
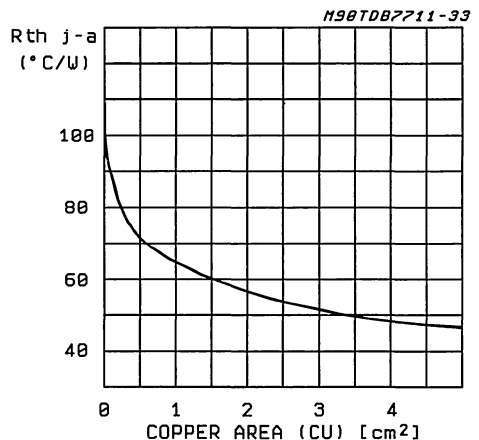
L 3845 FOR PABX AND MODEM LINE INTERFACE APPLICATIONS

by D. Salomoni

1 INTRODUCTION

The L3845 is used for MODEM and PABX Line Interface applications. The circuit provides DC loop termination for analog trunk lines. The V/I characteristic is equivalent to a fixed voltage drop (zener characteristic) in series with an external resistance that determines the slope of the DC characteristic. An external low voltage electrolytic capacitor causes the circuit to exibit high impedance to all AC signal in the voice band frequency range (>20 Kohm). The OFF-HOOK status is detected when the Line Current is higher than 8 mA. In this condition a constant current generator is activated to supply an external device (typically an optocoupler) without affecting the DC/AC characteristics of the circuit. An additional function is provided in order to reduce the DC fixed voltage drop and the AC impedance (PULSE MODE) This function can be used to respect some European Countries specifications during Pulse Dialling Operation.

2 GENERAL APPLICATION DESCRIPTION

Figure 1 shows the block diagram of L 3845. Figure 2 and figure 3 give two typical circuits for analog or digital applications. It is worth to note that the TRUNK TERMINATION CIRCUIT, together with the LS 5018 transient suppressor provides a compact and low cost module fully protected against lighting or overvoltage frequently present of telephone lines. When it is not necessary to make the protection against high energy pulses the LS 5018 can be replaced with two zeners of 16 V connected in series back to back. With the use of this circuit it is possible to terminate an analog trunk so that the DC current component is flowing in the TRUNK TERMINATION CIRCUIT. The AC signal through a low voltage capacitor it is provided to a low cost audio transformer and to the internal circuits. In figure 2 is indicated as example a simple hybrid circuit to made the 2 wire / 4 wire convertion. In figure 3 is indicated an application circuit with the SGS-THOMSON TS 5070 second generation COMBO that provide a programmable 2 wire / 4 wire convertion in addition to CODEC FILTER and other functions. In some European Countries it is requested that when the system is in PULSE DIALLING OPERATION the DC voltage at the Line Terminals during the MAKE pulses must be lower than the DC Line voltage in OFF-HOOK condition. By connecting the PULSE input (pin 3) to the reference ground V- (pin 2) the device reduces the DC charcteristic of about 1.5 V and the same time the AC impedance will decrease from 20 Kohm to a value equal to the external resistor (56 ohm typical). The PULSE function will be automatically set by the device if one capacitor is connected between pin 3 and pin 2 as will be explain in deep in the paragraf 3.2.d.

Figure 1: L3845 Trunk Interface

Figure 2

SGS-THOMSON
MICROELECTRONICS
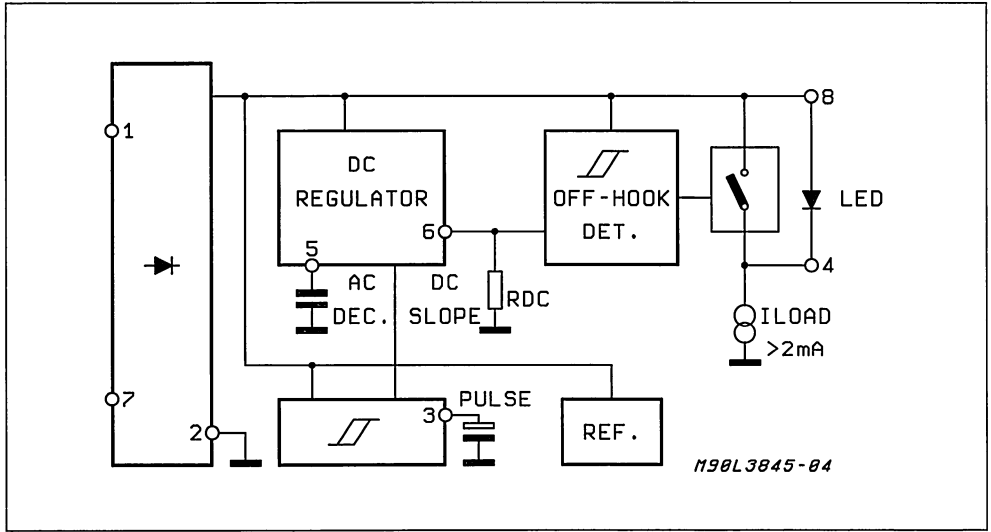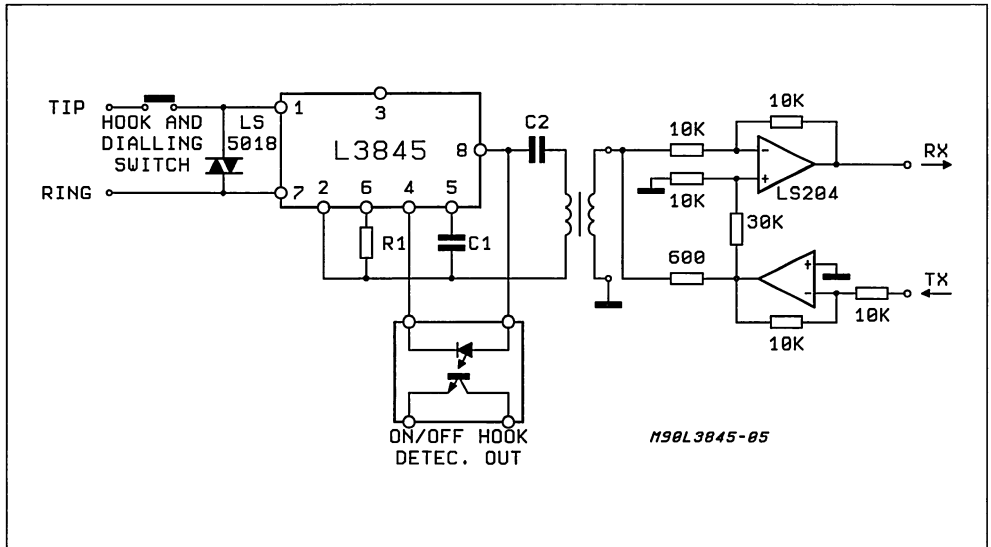
Figure 3
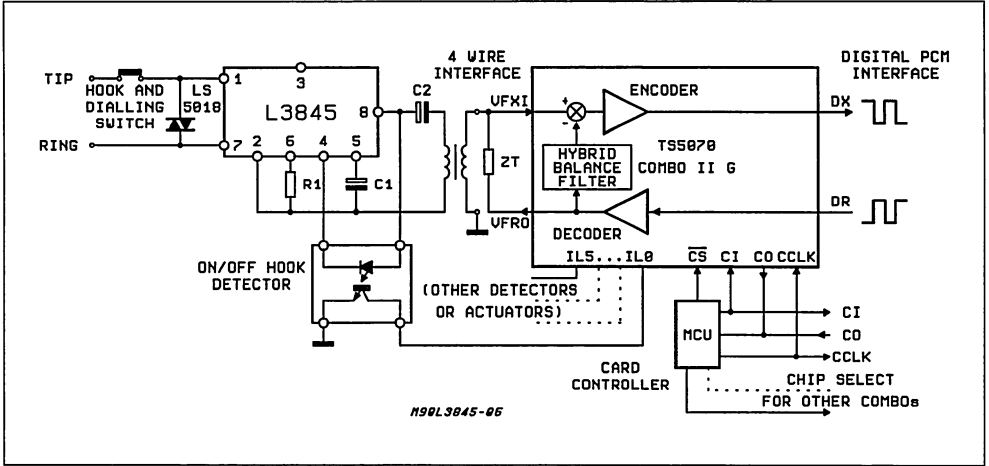
3 GENERAL CHARACTERISTIC DESCRIPTION

In this chapter are described the characteristics of L 3845.

3.1 DC CHARACTERISTICS

The DC characteristic are divided in three parts:

- DC characteristic in NORMAL MODE
- DC characteristic in PULSE MODE
- OFF-HOOK DETECTION.

Figure 4: DC Characteristics

3.1.a DC CHARACTERISTIC IN NORMAL MODE

The NORMAL MODE is set when pin 3 is left open. In this mode the AC impedance is high (typical 20 Kohm).
Figure 4 shows the typical DC characteristic for different R1 values. With a good approximation, the characteristic is linear for values of IL greater that 6 mA. The slope (ΛV_L / ΛI_L) of this characteristic is programmable and it is equivalent to the external resistor value. The test circuit is shown in figure 5.

Figure 5


```
M98L3845-87
```

S1 OPEN = NORMAL MODE
S1 CLOSED = PULSE MODE
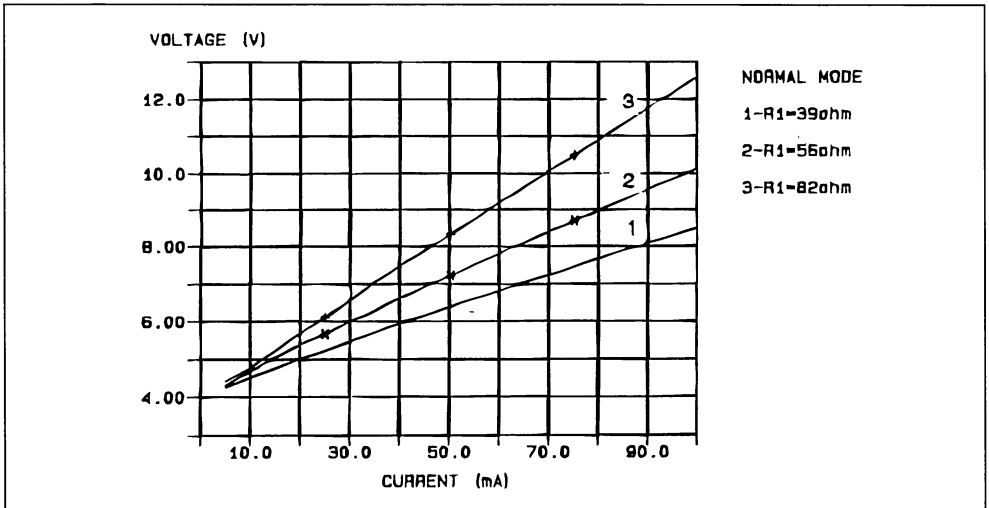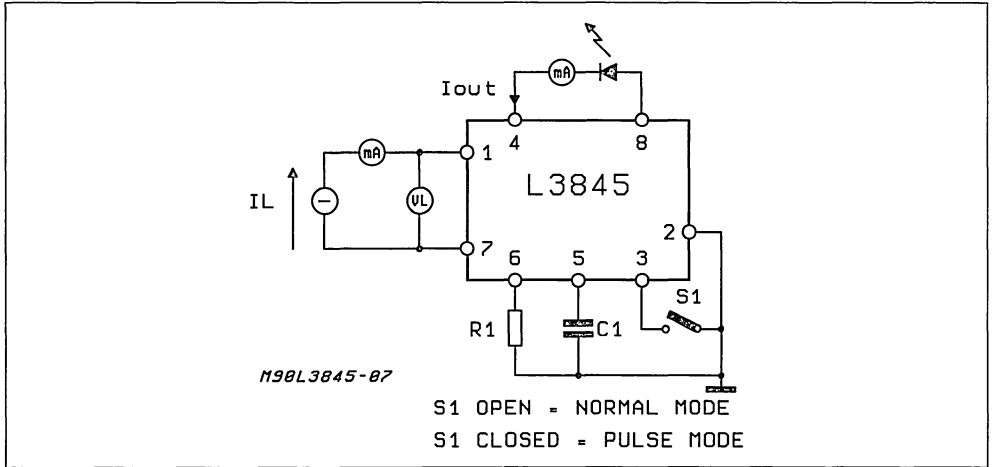
3.1.b DC CHARACTERISTIC IN PULSE MODE

This mode is set by connecting the PULSE input (pin 3) to V- (pin 2). In this mode the DC Line Voltage is reduced of about 1.5 V and the slope of the DC characteristic (ΛVL / ΛIL) is the same of the slope of the DC characteristic in NORMAL MODE, and equal to the external resistor R1 value. The test circuit is shown in figure 5 with S1 closed. Figure 6 shows the typical characteristic for different R1 resistor values.

Figure 6: DC Characteristics

SGS·THOMSON
MICROELECTRONICS
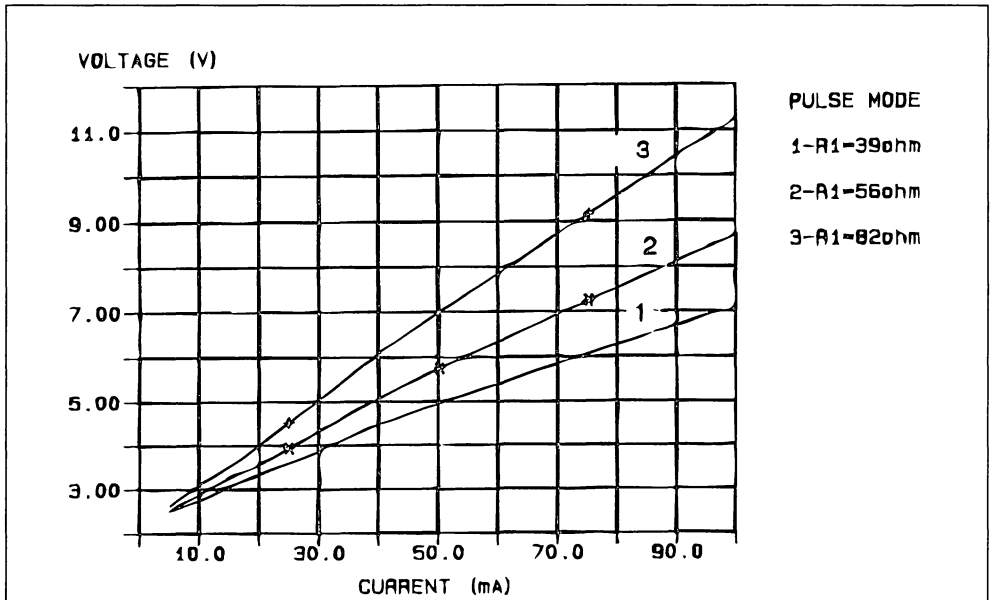
3.1.c OFF-HOOK DETECTION CIRCUIT

The L 3845 has a circuit to detect the OFF-HOOK condition. When the Line Current is over than 8 mA the constant current generator at pin HDO (pin 4) is activated. Figure 7 shows the Output Drive Current at the output HDO (pin 4) versus the Line Current IL. This circuit has the same characteristic both in NORMAL and in PULSE MODE. The test circuit is shown in figure 5.

Figure 7: DC Characteristics
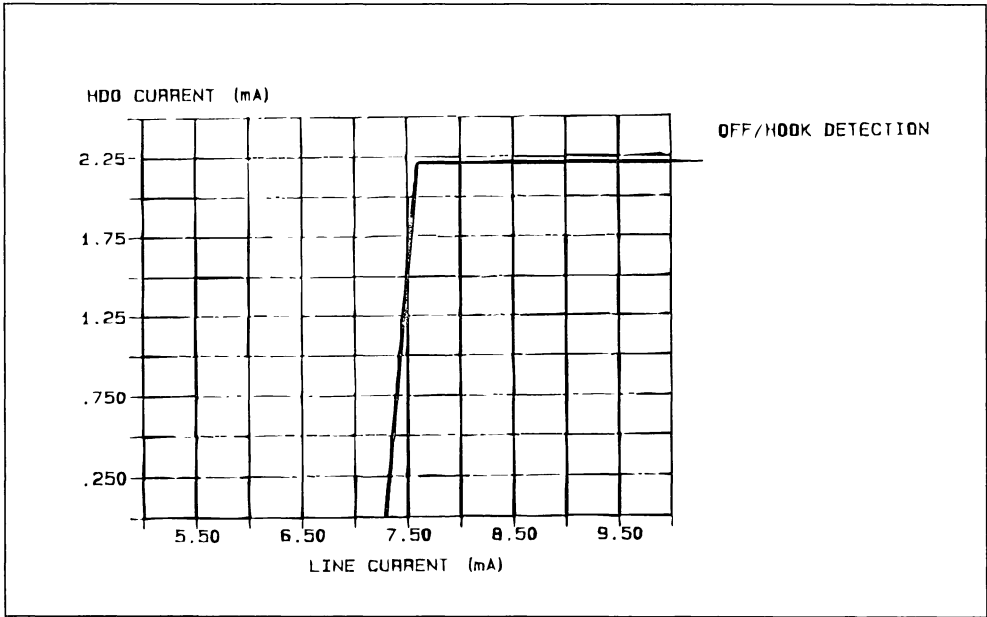
3.2 AC CHARACTERISTICS

The AC characteristics are divided in four parts:
- AC IMPEDANCE
- RETURN LOSS
- DISTORTION
- AUTOMATIC PULSE MODE

3.2.a AC IMPEDANCE

Figure 8 shows the AC IMPEDANCE of the device L 3845 for different Line Current values. Figure 9 shows the AC IMPEDANE for different C1 capacitor values and figure 10 shows the AC IMPEDANCE for different R1 resistor values. The test circuit is shown in figure 11.

Figure 8: Impedance
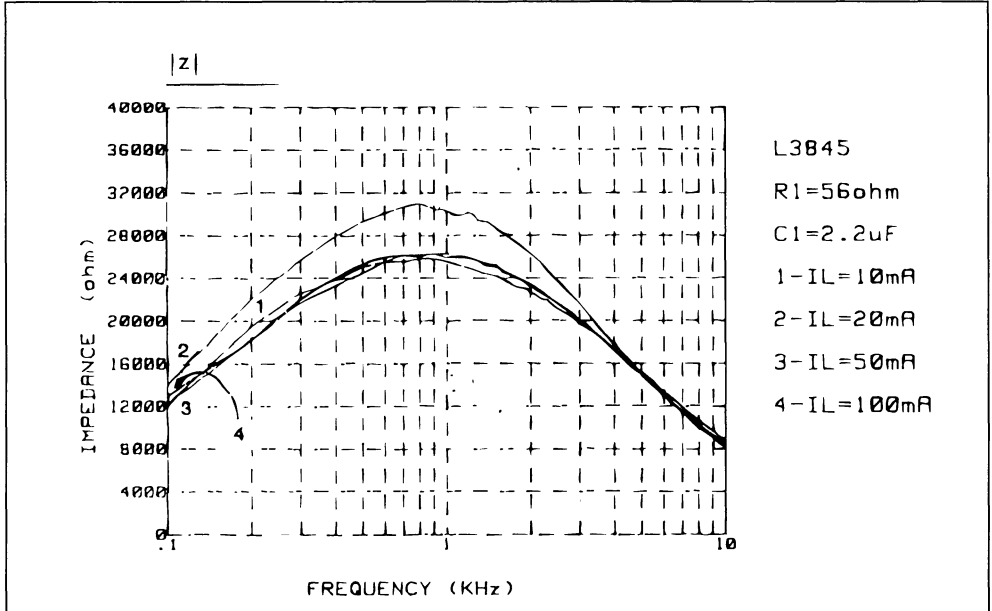
Figure 9: Impedance
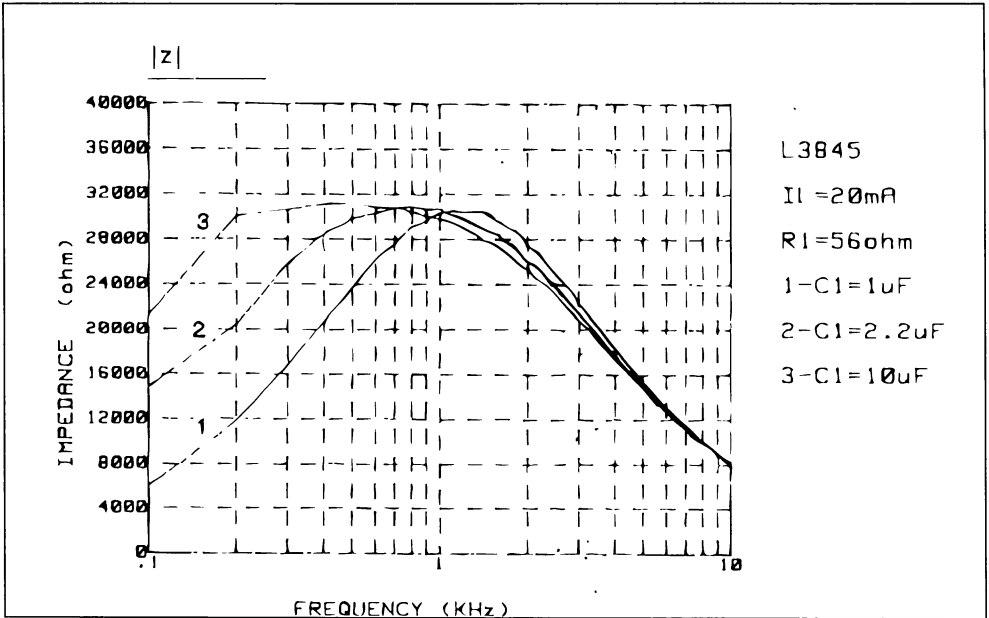
Figure 10: Impedance

Figure 11


```
                                          10u
                         10u
IMPEDENCE                              1  4    8       S1
ANALYZER        IL                          L3845    600
                                       7            2
                                         6    5
                         R1         C1

                    S1 OPEN = FOR AC IMPEDENCE
     M90L3845-00    S1 CLOSED = FOR RETURN LOSS
```
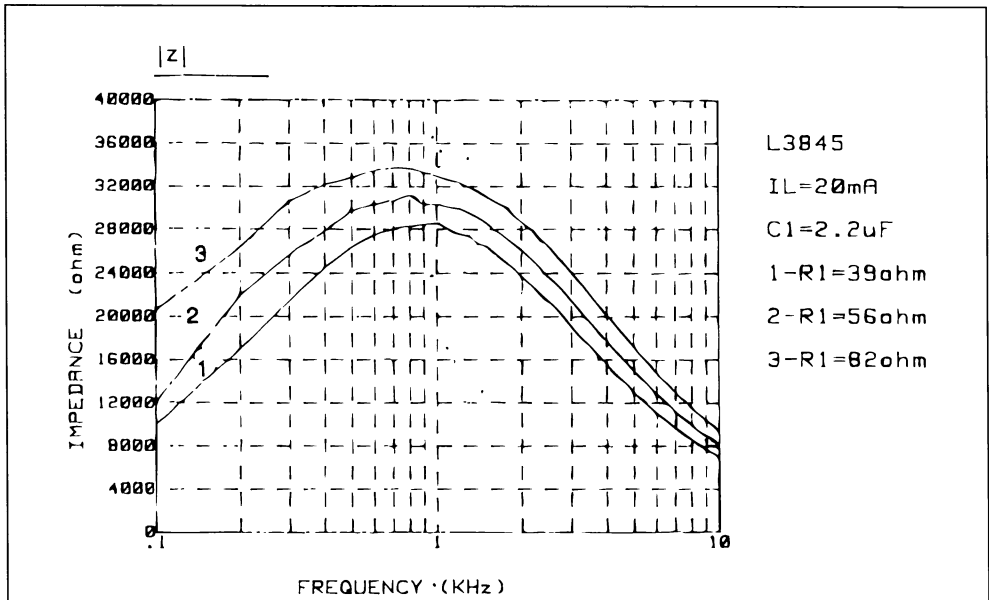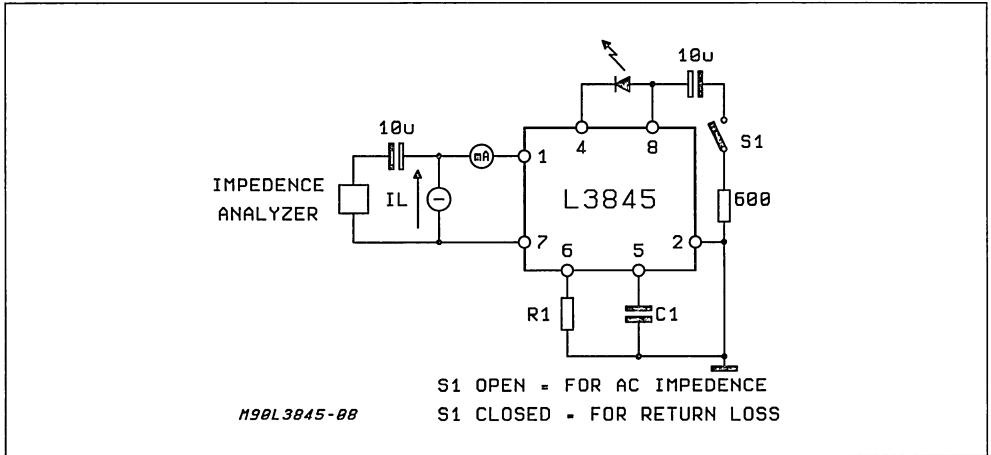
3.2.b RETURN LOSS

Figure12 shows the RETURN LOSS referred to 600 ohm impedance for different C1 capacitor values. Figure 13 shows the RETURN LOSS referred to 600 ohm impedance for different R1 resistor values. The test circuit is shown in figure 11 with S1 closed. The definition of the RETURN LOSS is:

$$RL = 20 \log \frac{|\ Zout + 600\ |}{|\ Zout - 600\ |}$$

Figure 12: Return Loss


```
L3845
REF  IMP=600 ohm
IL=20mA
R1=56 ohm
1-C1=1uF
2-C1=2.2uF
3-C1=10uF
```

SGS-THOMSON
MICROELECTRONICS
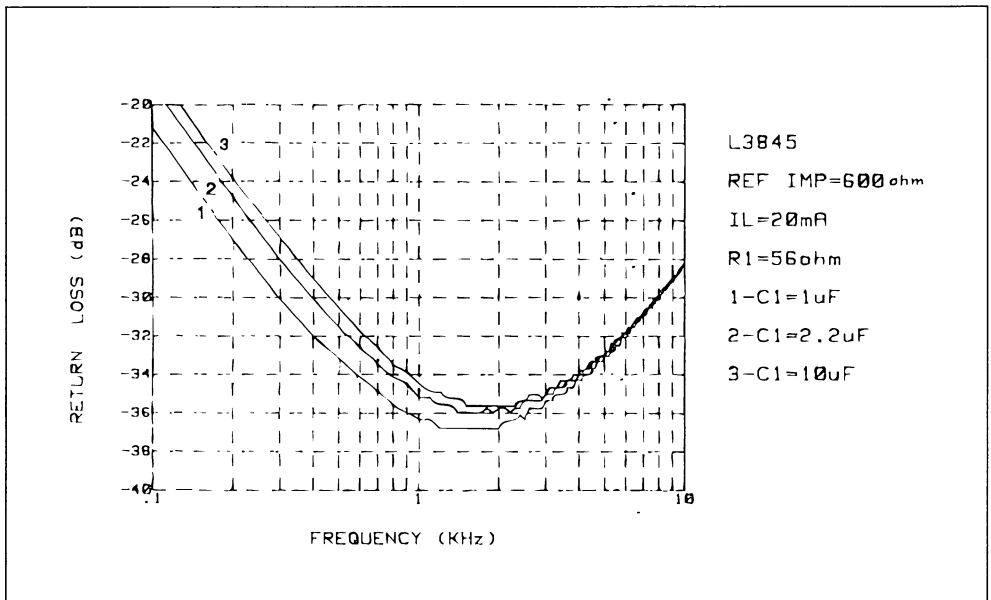
Figure 13: Return Loss
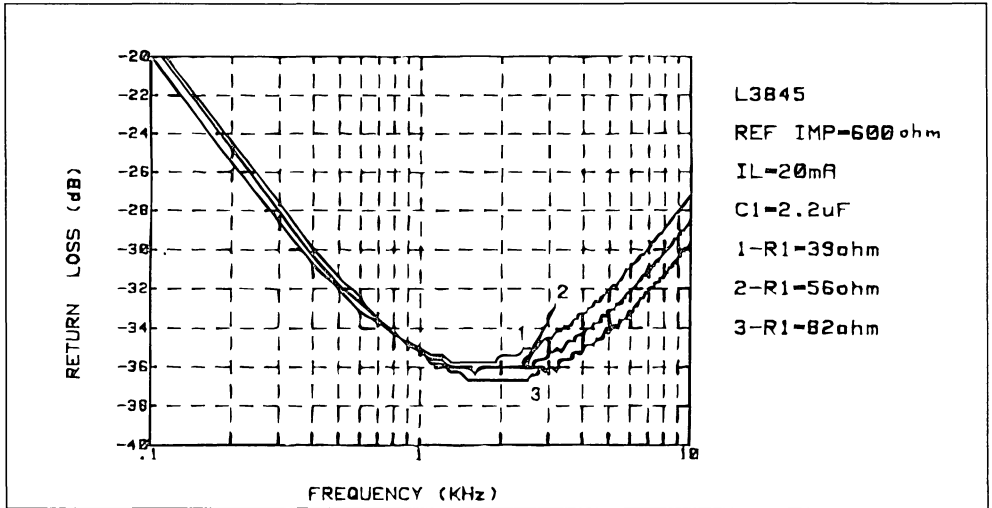
3.2.c DISTORTION

The measurements had been performed using the test circuit of figure 14. Figure 15 shows the maximum amplitude of the input signal between the pins 1-7 in order to measure a Total Harmonic Distortion less than 2%. It is possible to improve this performance connecting a resistor R2 in parallel to capacitor C1. A typical value for R2 is 300 Kohm. By this way, it is possible to increase the DC characteristic and therefore to improve the signal swing. The resistor R2 will influence also the slope of the DC characteristic, that will become:

$$\frac{/\backslash V_L}{/\backslash I_L} = R_1 \left(1 + \frac{150 \text{ Kohm}}{R_2} \right)$$

and the value of the AC impedance in the low frequency range.

Figure 14
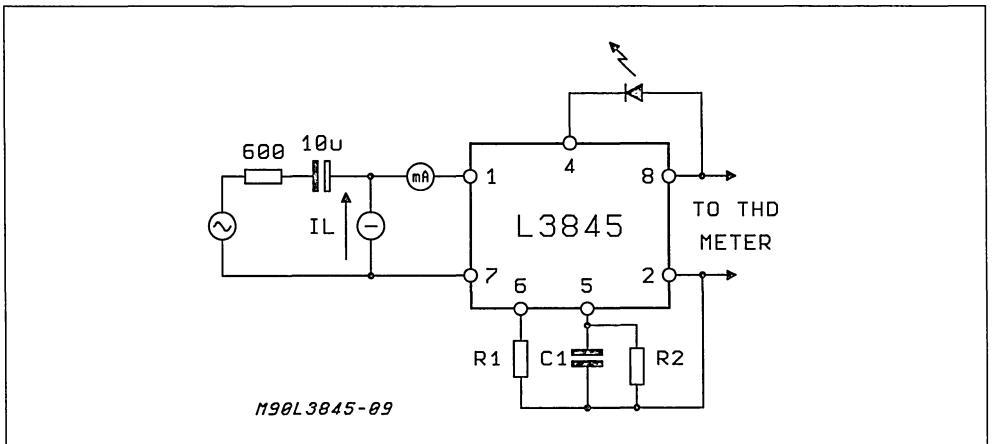
Figure 15: Max. Line Voltage
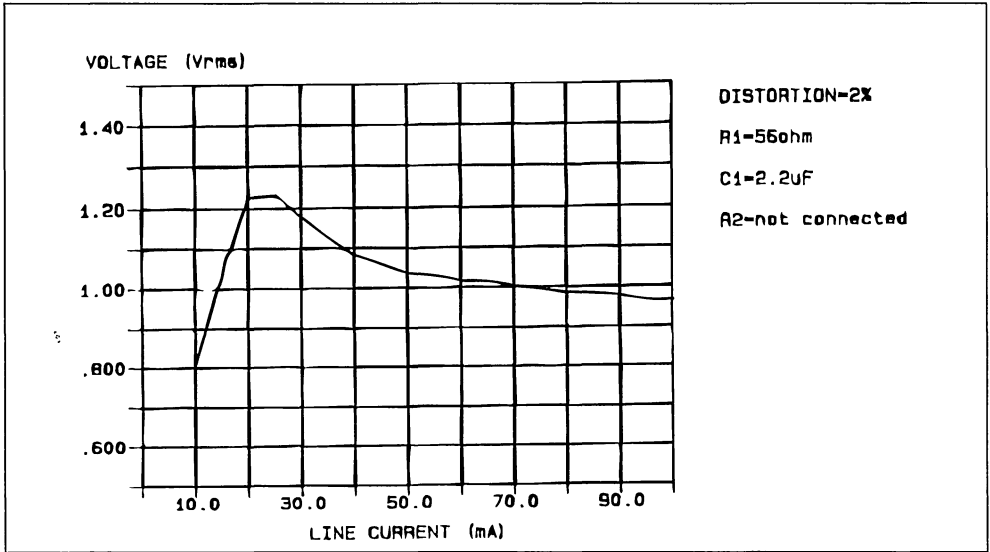
Figure 16 shows the MAX. Line Voltage versus Line Current for a THD = 2% and with R2 = 300 Kohm and different R1 resistor values. Figure 17 shows the DC characteristic with R2 = 300 Kohm and for different R1 values. Figure 18 shows the AC impedance with R2 = 300 Kohm and for different R1 values. When the signal is applied between the pins 8-2 and the THD is measured at pins 1-7 the results are exactly the same.

Figure 16: Max. Line Voltage
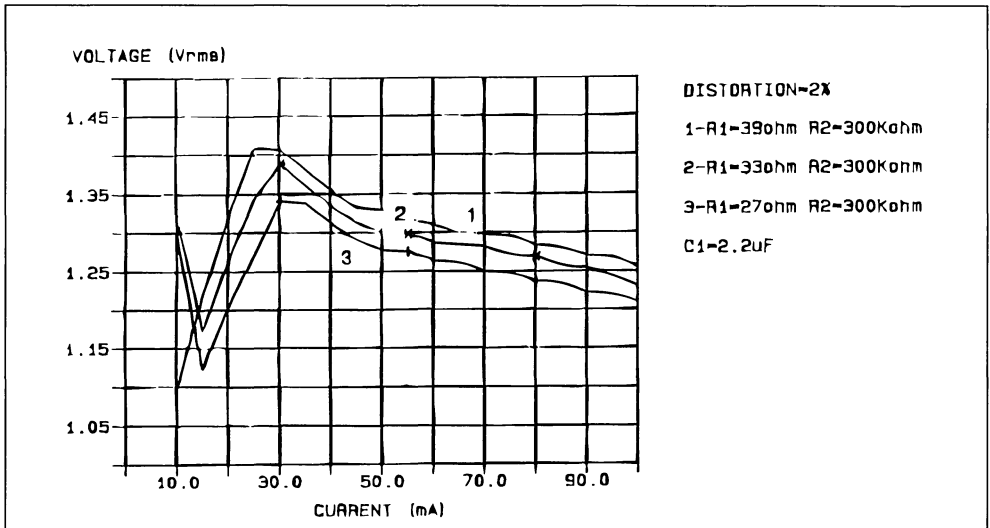
Figure 17: DC Characteristics
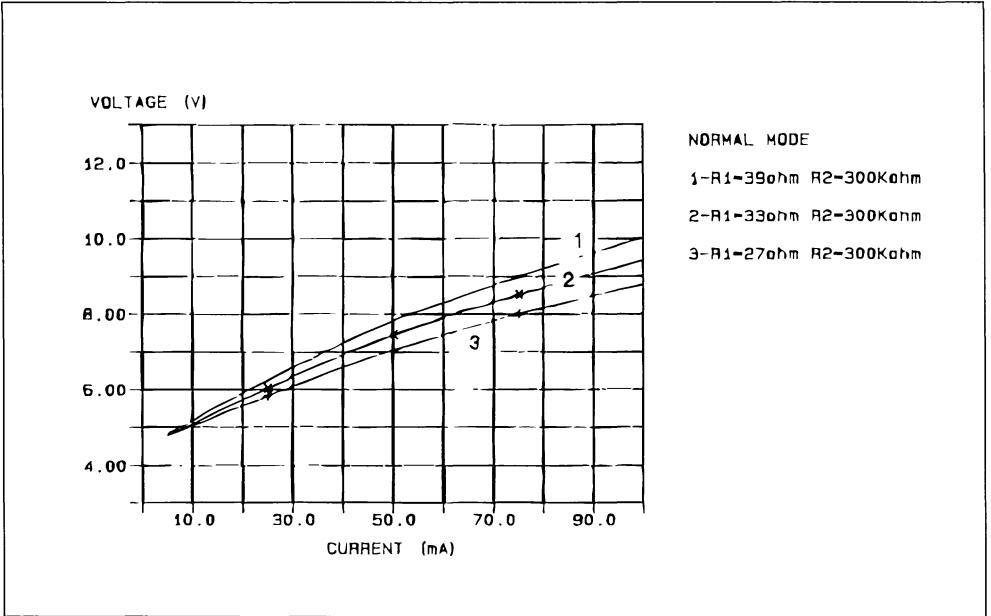
Figure 18: Impedance

SGS-THOMSON
MICROELECTRONICS
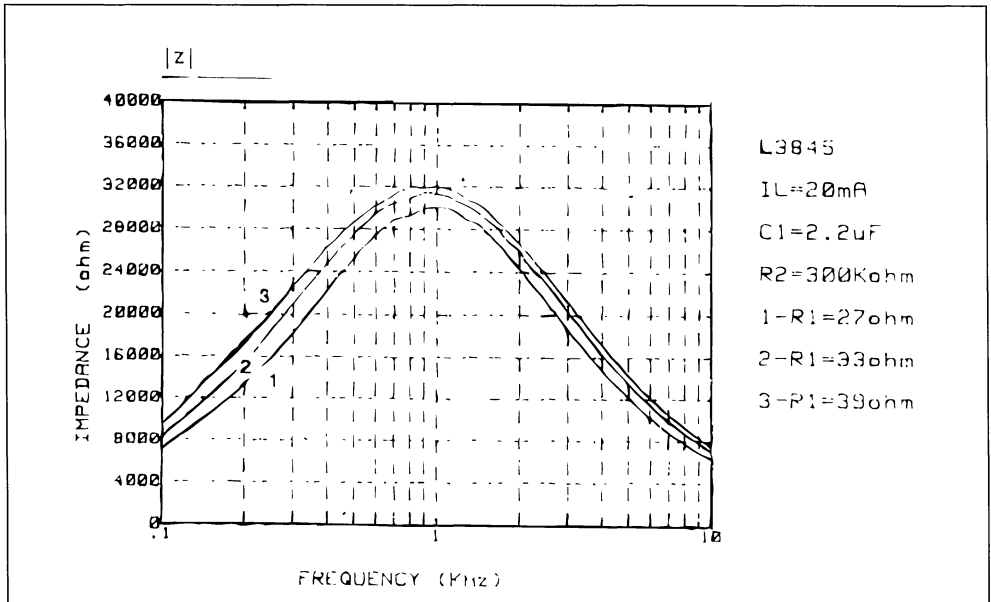
3.2.d AUTOMATIC PULSE MODE

The PULSE MODE is set by connecting the input PULSE (pin 3) to the reference ground V- (pin 2). To set L3845 in NORMAL MODE the PULSE input (pin 3) must be open. The device is able to set automatically the PULSE MODE, without any external operation, by connecting a capacitor C2 between pin 3 and pin 2, the suggested value for C2 is 1 μF. In this case when the device recognise an ON-HOOK condition ($I_L < 8$ mA) automatically it goes in PULSE MODE. The delay time t1 to go from NORMAL MODE to PULSE MODE is about 0.8 mSec with C2 = 1 μF. When the Line Current returns higher than 8 mA the device will stay in PULSE MODE for a time t2 fixed by external C2 capacitor. This time is long enough in order to keep in PULSE MODE the device during PULSE DIALLING at 10 Hz. The delay time t2 is determinate by the relationship:

$$t_2 = \frac{C_2 * (V_T - V_{BE})}{I_T}$$

Where VT is a voltage threshold of an internal comparator (VT = 1.4 V) and IT = 10 μA is the value of the internal current generator that charge the external capacitor C2 connected between pin 3 and reference ground V- (pin 2). For: C2 = 1 μF, t2 will be = 80ms. Figure 19 shows the waveforms at pins 8 and 3 for the function "AUTOMATIC PULSE MODE". Figure 20 shows the waveform between pins 1 and 7. Figure 21 shows the test circuit. From figure 20 you can see that the DC voltage at pin 1 during the MAKE pulses is 1.5V lower than the voltage in NORMAL MODE. In conclusion, how you can see, the device performs automatically the pulse function without any external device.

Figure 19: Automatic Pulse Mode

SGS-THOMSON
MICROELECTRONICS
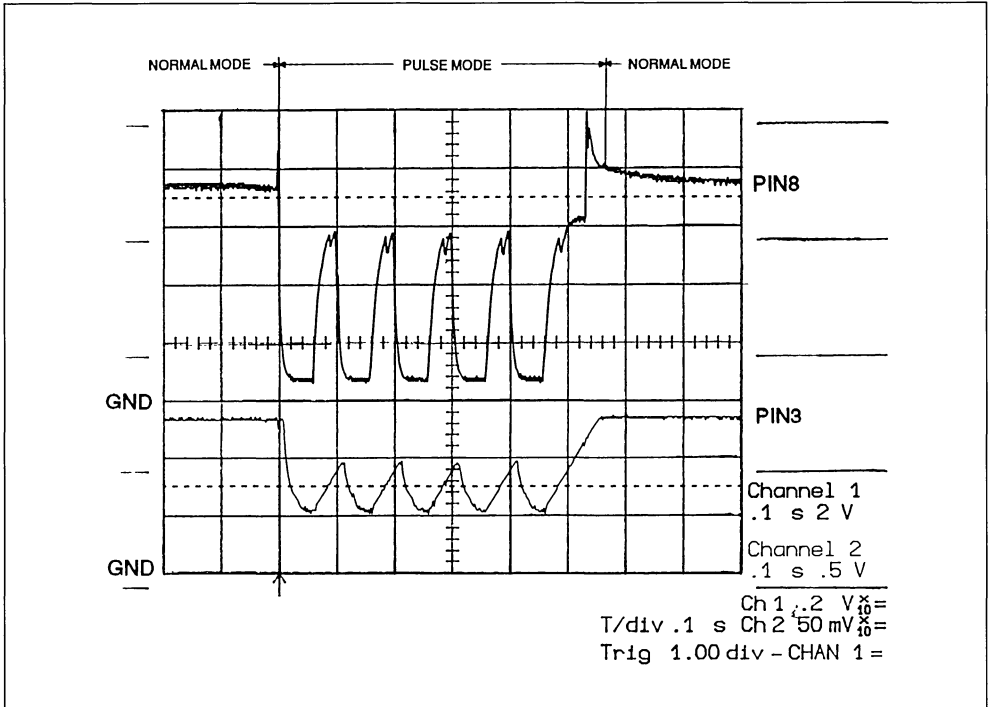
Figure 20: Automatic Pulse Mode
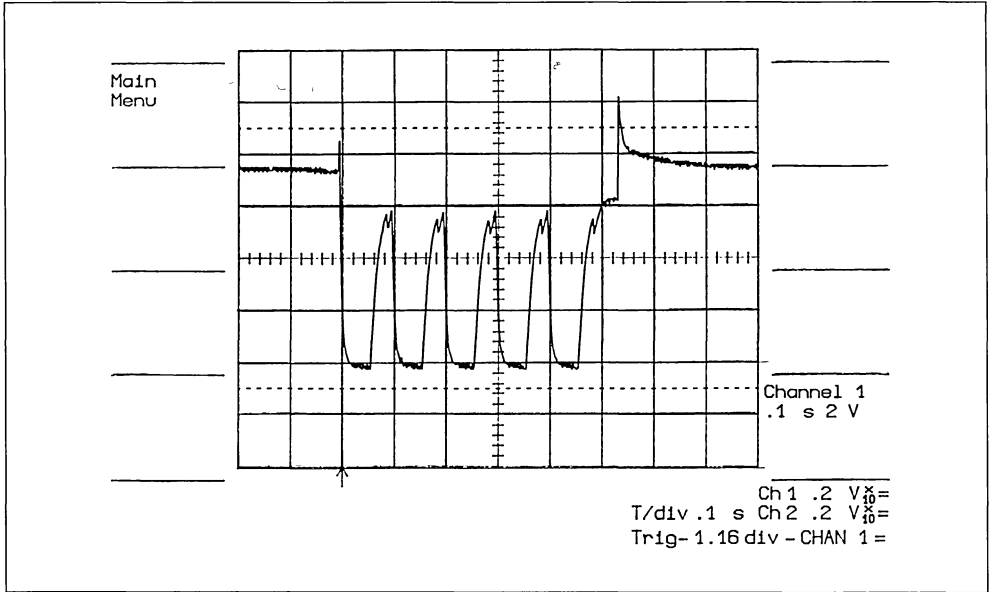
Figure 21
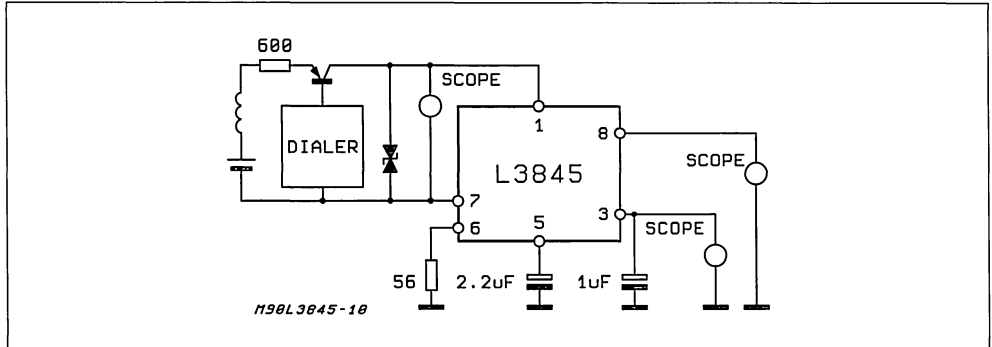
CLOCK EXTRACTION
AND TERMINAL SWITCHING ICS (EF73321 and EF7333)

1. CLOCK EXTRACTION CIRCUIT

1.1. DESCRIPTION

The EF73321 circuit provides the interface between a 2048 Kbit/s or 1544 Kbit/s PCM trunk and the switching equipment.

PCM junction time recovery as defined by the CCITT generally requires a damped oscillator sustained by logic 1's detected by the PCM junction.

Generally the oscillator consists of coils, capacitors, basic capacitors, and varicaps whose wiring diagram is not easily integrated.

The solution retained is the use of a digital integrated circuit for PCM junction transmission and reception (fig. 1).

The receiving side amplifies and reshapes the bipolar signals from the receive transformer.

From these signals it recovers the distant clock $\overline{HD}$ by means of a local 16384kHz (or 12352kHz) oscillator. The circuit also accepts external clock frequencies lower than or equal to 16384kHz for in line outputs smaller than or equal to 2048Kbits/s. The 16384kHz signal is asynchronous and can be common for different EF73321 circuits. Receive signals are buffered and synchronized with the HD clock.

On the transmitting side, it calibrates the applied signal in terms of duration and amplitude by means of a power output stage directly coupled to the primary winding of the transmit transformer.

1.2. BIPOLAR AND HDB3 CODES

Figure 2A shows a series of NRZ (non return to zero) linear data to be transmitted.

The logic 1 or 0 is present throughout the transmission of a bit. There is no return to zero for a logic 1 during this time.

Figure 2B shows this signal converted to bipolar form, logic 0's remain as they are but 1's alternately take a positive and a negative value.

In figures 2C and D this same signal is converted to HDB3 ; not more than three 0's may be received in line. A fourth 0 would systematically be transmitted as a 1 whose bipolarity has been violated with respect to the last 1 transmitted but whose bipolarity is respected compared to the last violation.

Two cases are possible :

- In figure 2C, the preceding violation (not represented) was positive, the first 4-bit word fill-in sequence will be :

$$0\ 0\ 0\ V$$

where V is negative, the following fill-in sequence will be :

$$B\ 0\ 0\ V$$

where B is a signal element different from zero, in this case positive since B should respect the polarity with respect to the last logic 1.

- In figure 2D, the preceding violation (not represented) was negative. In this case the first fill-in sequence will be :

$$B\ 0\ 0\ V$$

where V is positive since the preceding violation was negative, and in order that this polarity really be a bipolarity violation, B is also positive. The value of the second sequence is :

$$B\ 0\ 0\ V$$

where V is negative since the preceding bit V was positive and B is also negative and not equal to zero to ensure violation.

Then, it is verified that the sequences described are such that the in-line dc component is really equal to zero. Thus it is possible to use pulse transformers for galvanic insulation between line and terminals.

1.3. APPLICATION N°. 1 : EF73321 WITH FREE RUNNING OSCILLATOR

The crystal oscillator shown in the upper part of figure 3 is of the stand-alone type, t61 frequency in this application is in the order of 16384kHz, frequency accuracy is 50ppm.

One oscillator delivers t61 signals to different EF73321 circuits. Fan out of each 74LS04 gate is 8.

An alternative is to build this oscillator using HCMOS gates, in this case the 6.8 kW pull-up resistors can be ommitted.

The line signal is HDB3 coded with an attenuation of 6dB max for a 3V pulse delivered by a remote transmitter. Figure 4 shows the pulse for PCM CEPT junction.

Transmit and receive transformers are the same type. The transformation ratio between the single winding on the line side and each of both windgins on the circuit side is 2/3 (figure 3).

In this application, transmit and receive sides operate independently, transmission and reception are asynchronous.

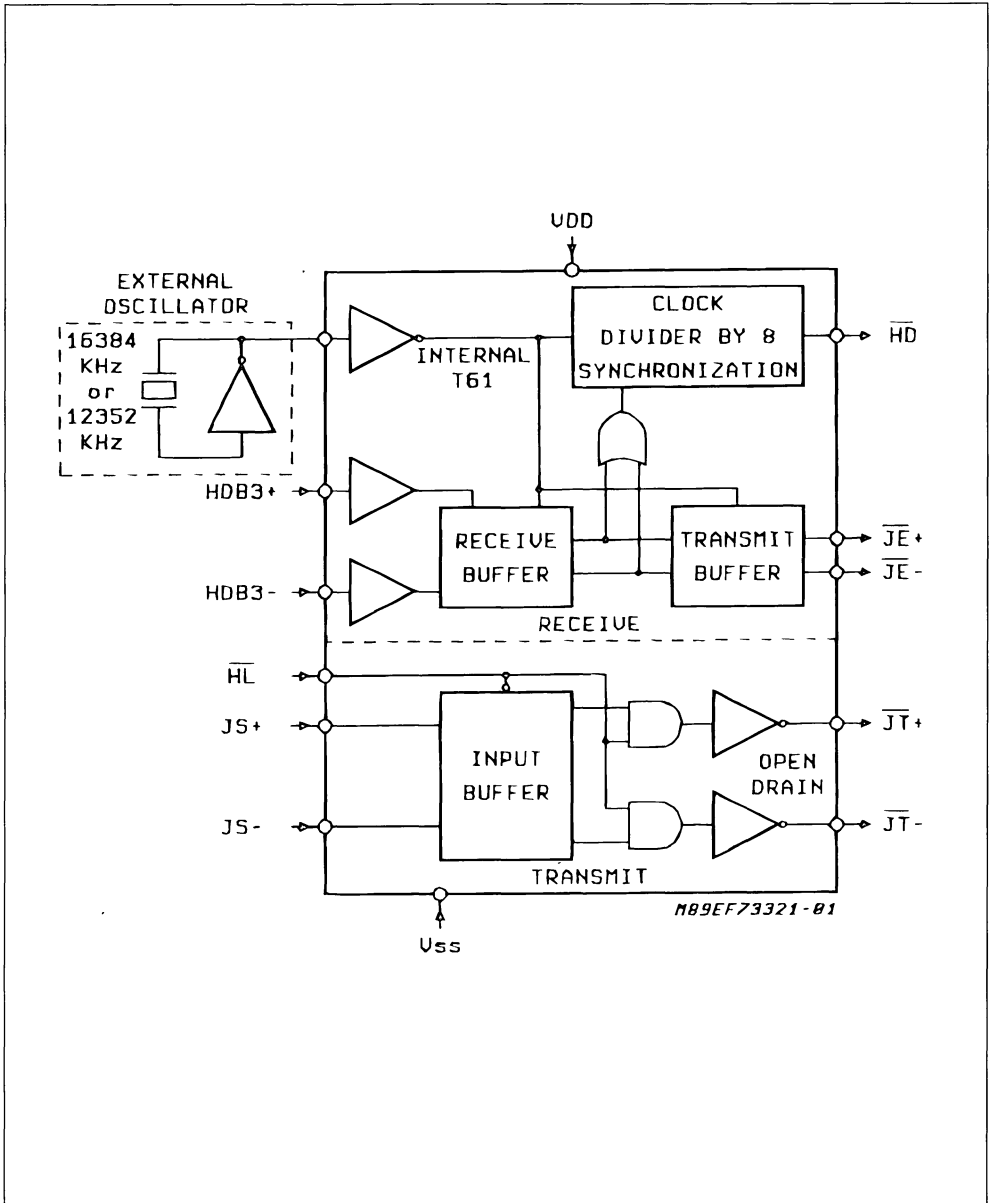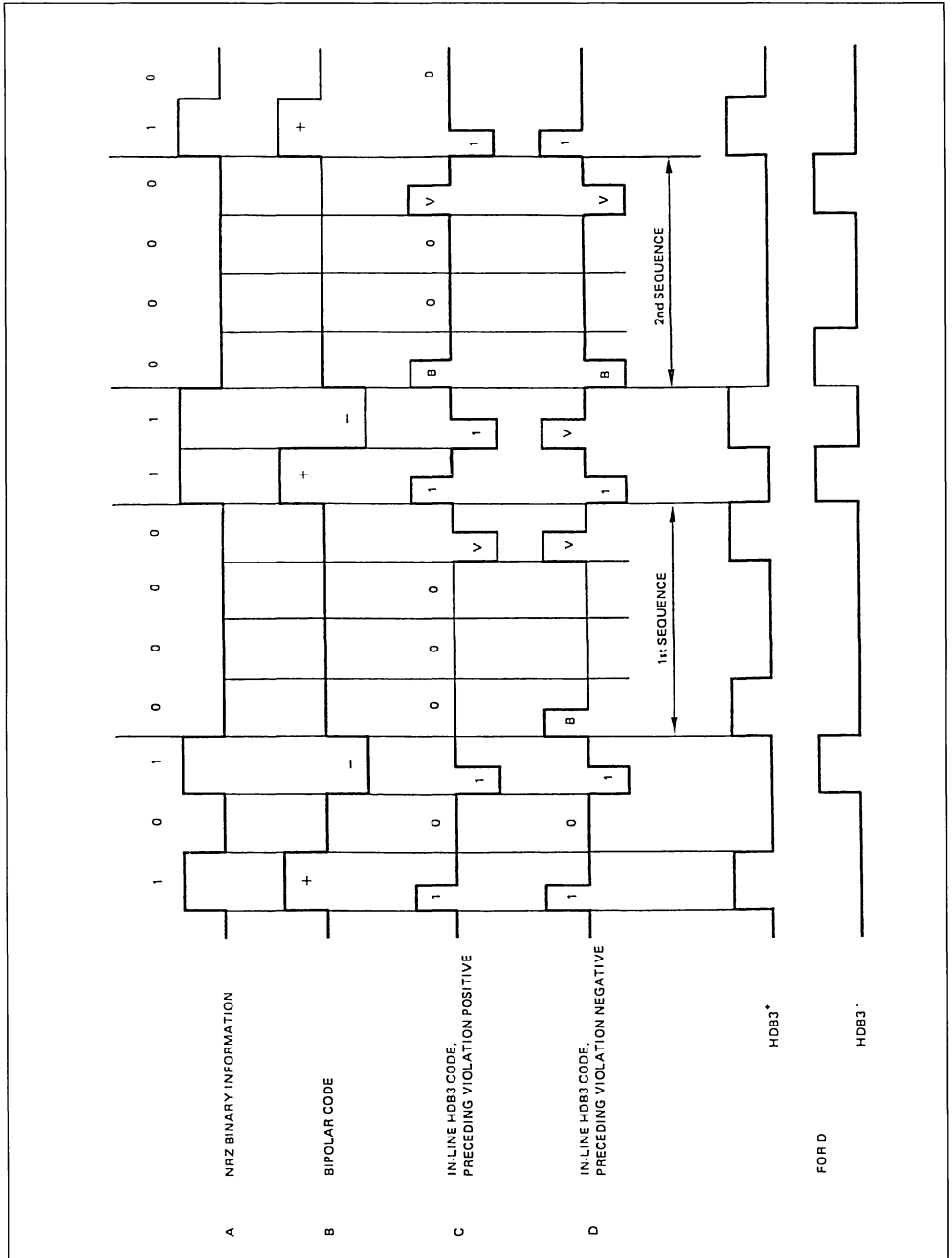**Figure 1 :** EF73321 Block Diagram.

Figure 2 : EF73321 Receive Codes.

1.3.1. RECEIVE SECTION. The information delivered in the form $\overline{JE}+$ and $\overline{JE}-$ at the receive inputs of EF73321 (which are the HDB3 signal rectified signals) have a constant phase relationship with the recovered clock signal HD. The HD clock period will be :

$$8t \pm - 2t$$

where t is the period of the t61 signal in this application. The delay caused at the input by the receive logic between HDB3+, HDB3– and $\overline{JE}+$, $\overline{JE}-$ is 2t (122ns).

1.3.2. TRANSMIT SECTION. The phase relationship between the information at the JS+ and JS– inputs and the local clock $\overline{HL}$ should be constant. The positive pulse width defines the line pulse width of the $\overline{HL}$ signal on the $\overline{JT}+$ and $\overline{JT}-$ outputs.

$\overline{JT}+$ and $\overline{JT}-$ are open drain outputs. Output protection is achieved by sensing the output voltage when low (fig. 6).

Proper operation of the circuit is guaranteed for output currents below 35mA, i.e. as long as the voltage drop on the output is below the protection threshold. Therefore the output current should be limited by design to values below 35mA (see note).

Calculation of the corresponding minimum load resistance at $\overline{JT}+$ and $\overline{JT}-$ is as follows :

$$R_L \geq \frac{V_{BB} - 0.25V}{35mA}$$

$$V_{BB} \leq 12V$$
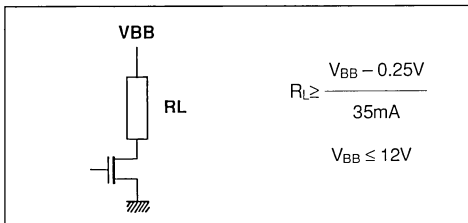
Note : This protection does not make the output acting as a current source but switches out the output. For properly selected output loads, maximum power dissipation in each output transistor will be about 30mW

1.4. APPLICATION No. 2 : USING EF73321 WITH SLAVED OSCILLATOR

A buffer memory is used to overcome the differences in the information bit durations caused by the transmission and circuit EF73321. The information is latched by HD and read at the rate of the local clock from the oscillator slaved by HD. The buffer memory capacity only depends from the jitter characteristics and the slaved oscillator correction speed. Figure 7 gives the block diagram of such a memory associated with circuit EF73321. The functions represented are :
• HDB3/BIN code conversion,
• slaved Crystal oscillator,

• frequency dividers,
• buffer memory and its write/read control.

1.4.1. HDB3/BIN CONVERSION. This circuit is used to convert the two HDB3 components to one NRZ signal with the same jitter as the two original components.

1.4.2. CRYSTAL OSCILLATOR. The crystal oscillator frequency is 16.384kHz. It delivers t61 in the form of a square signal with a 61ns period driving the internal logic of circuit EF73321 and the oscillator-associated frequency divider. A submultiple of the crystal frequency is slaved by a submultiple of the distant clock recovered by EF73321.

1.4.3. FREQUENCY DIVIDER ASSOCIATED WITH THE CRYSTAL (read counter). This is a counter in which each stage divides the input signal frequency by 2. After 3 stages a 2048kHz signal is obtained corres-ponding to HD frequency whose jitter amplitude was reduced by the extreme values taken by the slaved oscillator.

The following two bits A' and B' are used to select the buffer memory reading time (see timing diagram of figure 8). The n following bit should be chosen by the user to set the crystal oscillator correction frequency. If n = 6, the oscillator frequency will be corrected every 125 µs.

1.4.4. FREQUENCY DIVIDER ASSOCIATED WITH HD (write counter). The first two bits A and B define the reading time in the buffer memory. If HD shows no jitter, counters A' B' and A, B are in phase and reading takes places with a time delay of 2 bits after writing.

Note : If 3 bits (A, B and C) define the writing time and 3 bits the reading time, reading will take place with a time delay of 4 bit-durations compared to the writing time.

1.4.5. BUFFER MEMORY. This memory consists of a number of bistable circuits depending on the jitter to be recovered. In this example the 4 latches circuits are used to recover a signal with a jitter of ± 2 bits in amplitude without loosing information.

When the write counter A, B defines 2 as writing time, the read counter A' B' defines 0 as reading time and so on.

The residual jitter on the local clock $\overline{HL}$ and the data are determined by the selected slave crystal oscillator .

1.4.6. TRANSMIT SECTION. In this application the local clock signal $\overline{HL}$ can be used to sample the data to be transmitted (fig. 7).

Residual jitter is small enough to drive BIN/HDB3 decoder logic and to calibrate line pulse width.

SGS-THOMSON
MICROELECTRONICS

Figure 3 : Application No. 1 - EF73321 Using Free Crystal Oscillation.
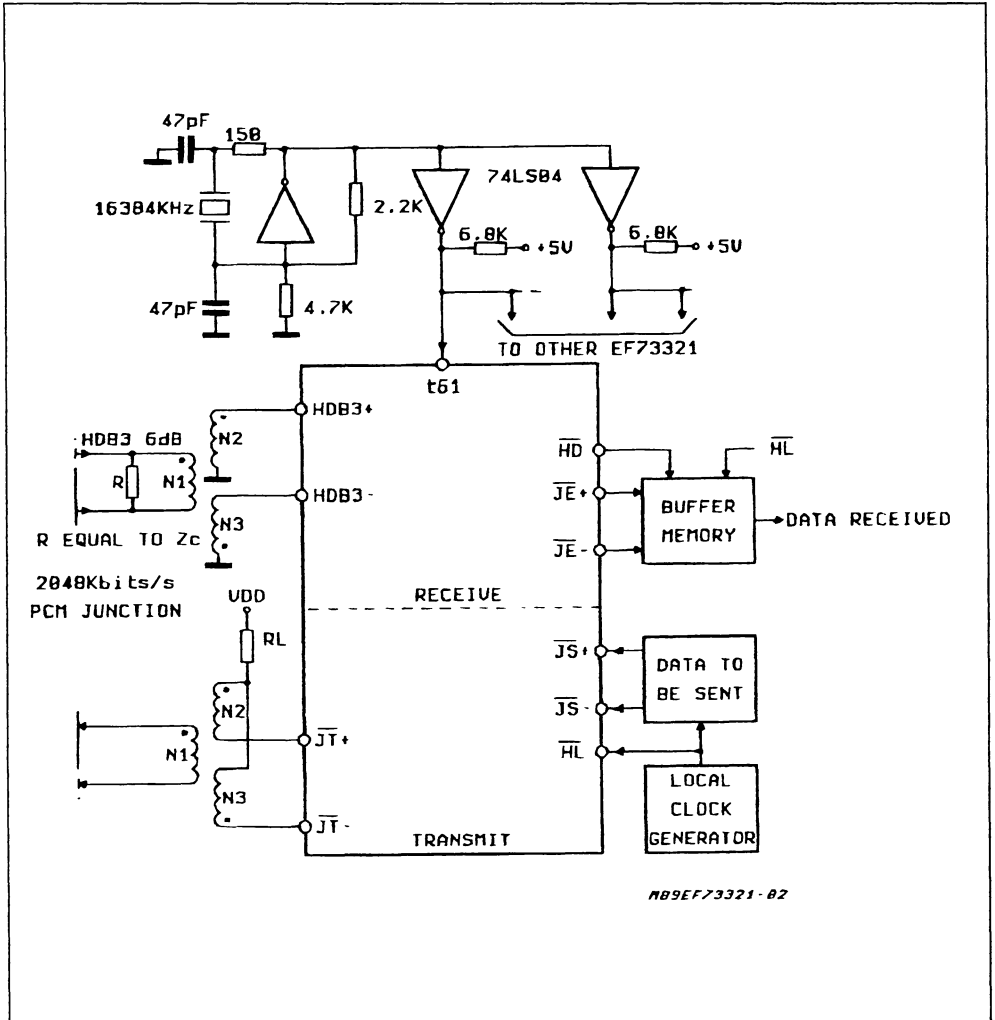
Note : A 100nF capacitor must be connected between V_DD and V_SS as close as possible to the supply pins.

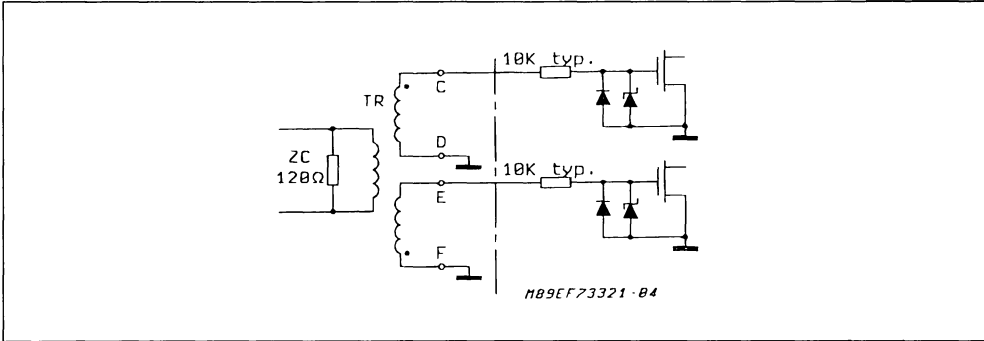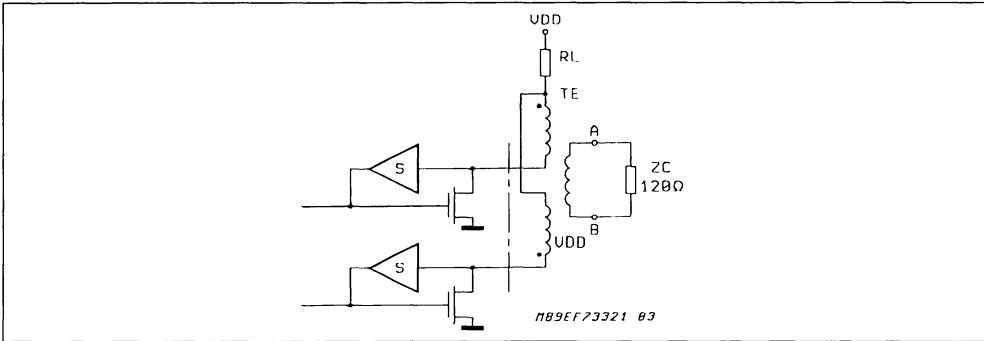**Figure 4 :** EF73321 Output Stage.

Figure 5 : EF73321 Input Stage.

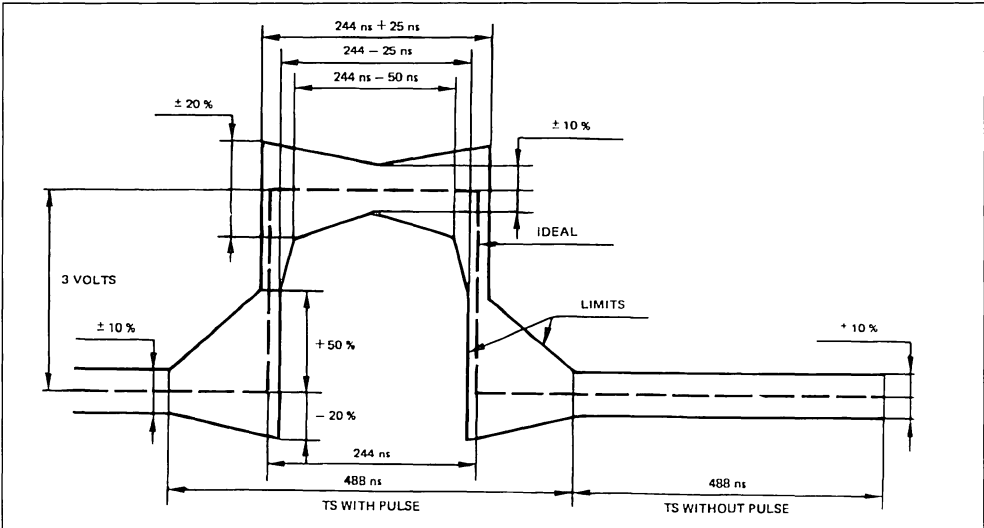**Figure 6 :** Pulse Shape for 2048 Bits/s Cept PCM Junction.

SGS-THOMSON
MICROELECTRONICS

Figure 7 : Application No. 2 - EF73321 with Slaved Oscillator.
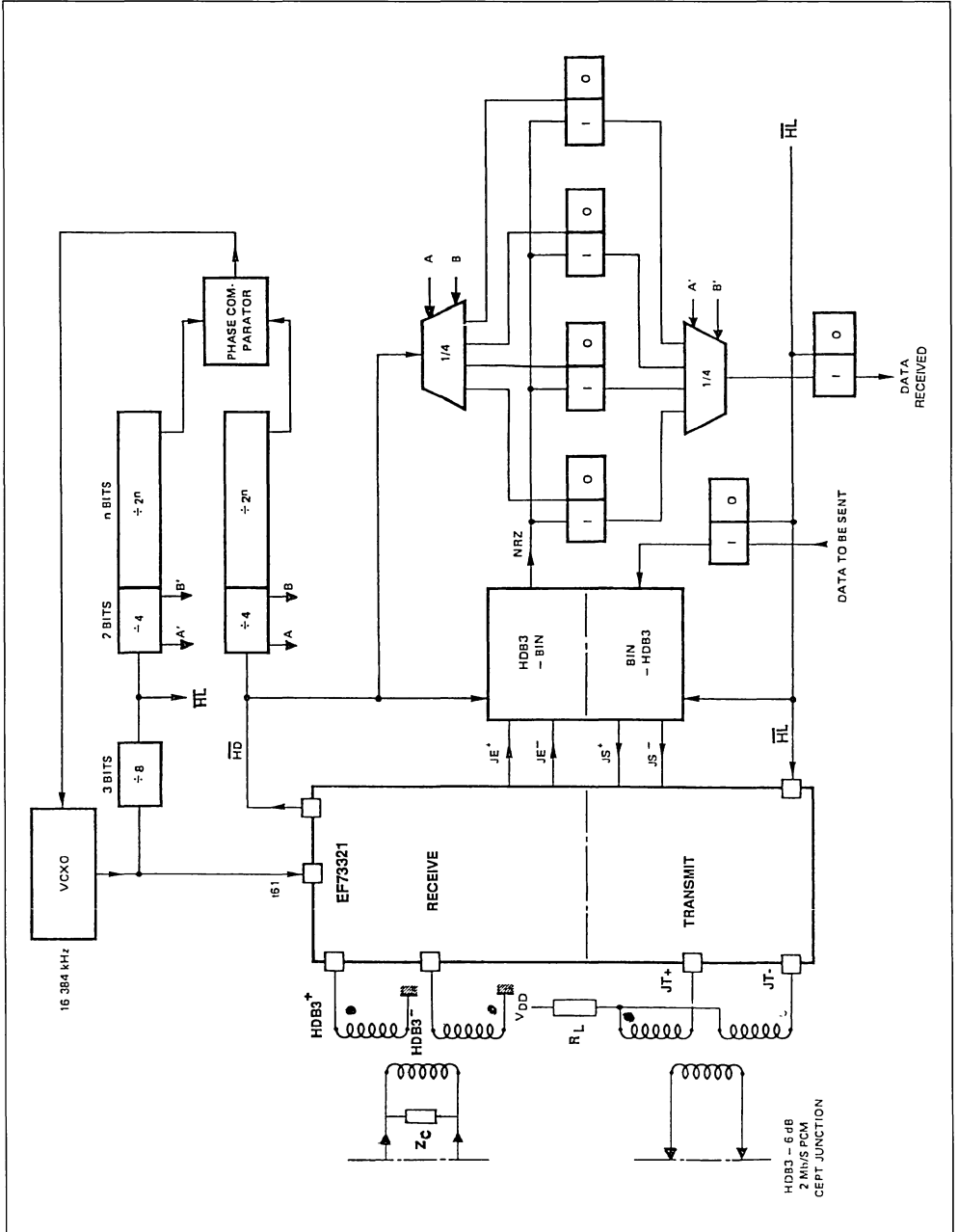
Note : A 100nF decoupling capacitor must be connected between V_{DD} and V_{SS} and located as close as possible to the supply pins.

Figure 8 : Application Timing Diagram - EF73321 with Slaved Oscillator.

SGS-THOMSON
MICROELECTRONICS
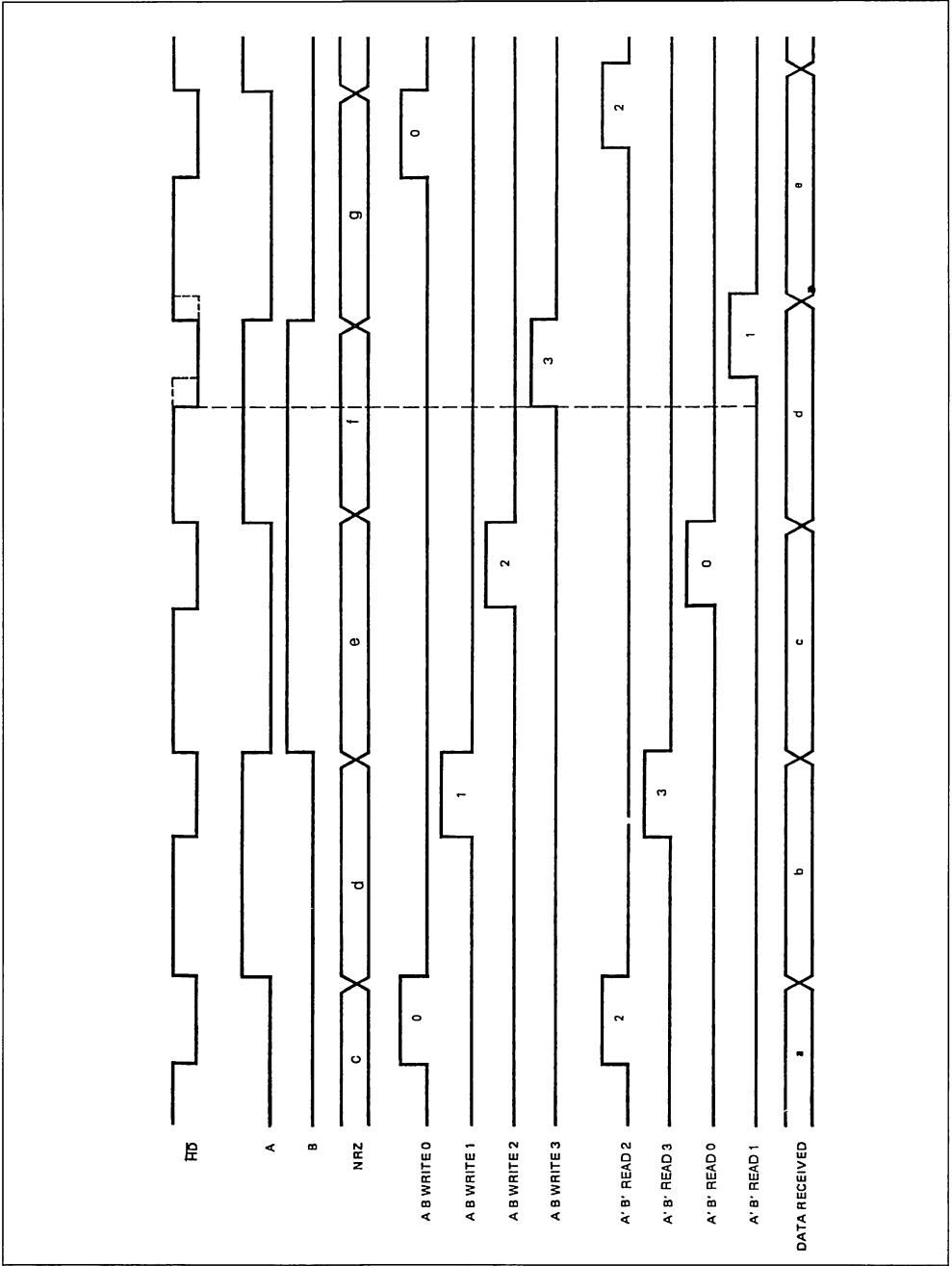
2. TERMINAL SWITCHING CIRCUIT
(EF7333)

2.1. CIRCUIT DESCRIPTION

The EF7333 conforms to CCITT recommendation G737. In most applications it is connected between a clock extraction circuit of a PCM junction and multiplex switching circuits at 2.048Mbits/s.

The EF7333 basic functions are :
- frame synchronization of PCM junction input section with local clock,
- absorption of line jitter whose amplitude and frequency are given in EF7333 specifications.

In addition to these basic functions, the device also features :

– Incoming link processing functions :
- input signal HDB3, binary or bipolar decoding
- frame skip or doubling
- receive errors detection and alarms generation
- remote alarm extraction

– Outgoing link processing functions :
- insertion of synchronisation words into outgoing frames

- output signal binary, HDB3 or bipolar coding
- receive fault alarm transmission

The receive function provides a multiplex signal at 2.048Mbit/s synchronized with local center clock (fig. 10). The local center can be a connection network, a time concentrator, a computer interface, etc.

So, the PCM junctions from various centers in a plesiochronous network can be synchronized with the local center clock. Figure 9 shows that whatever the phase relationship between remote clocks HD1, HD2,...HDn, circuit EF7333 associated with remote centers can set in phase not only time slots but also incoming multiplex frames.

If distant and local centers are synchronized by a common clock (not represented on fig. 9). The EF7333 circuit resynchronizes the multiplex signal without loss of information accepting a peak-to-peak jitter of several time slots for very low jitter frequencies.

If remote centers are asynchronous, circuits EF7333 synchronizes the multiplex by skipping or doubling frames without loss of synchronisation.

Figure 9 : Plesiochronous Network.
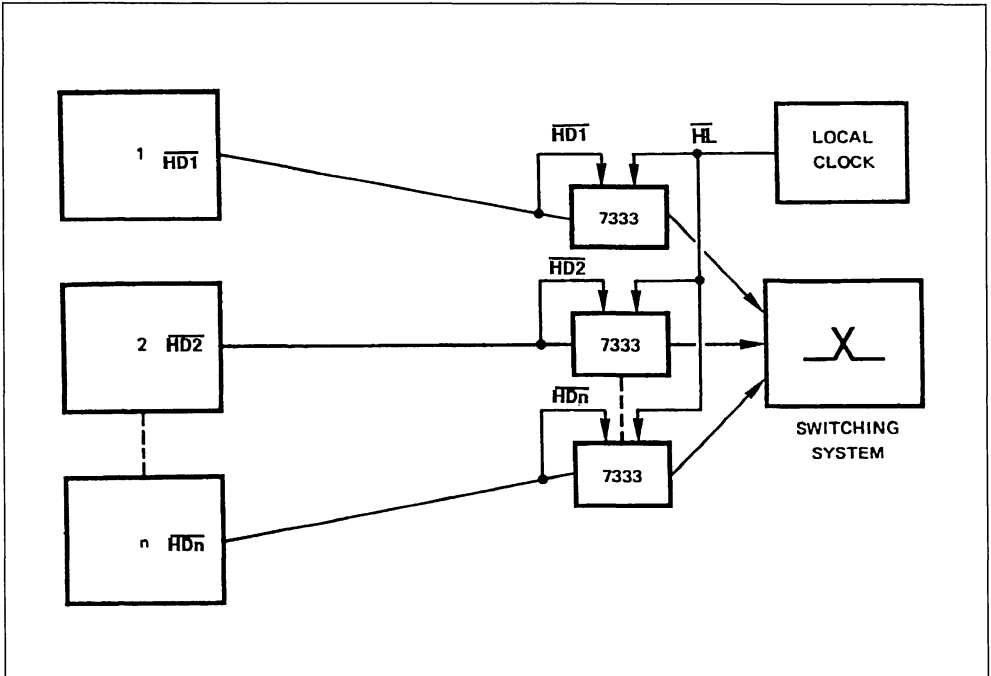
Figure 10 : Switching Terminal Module.
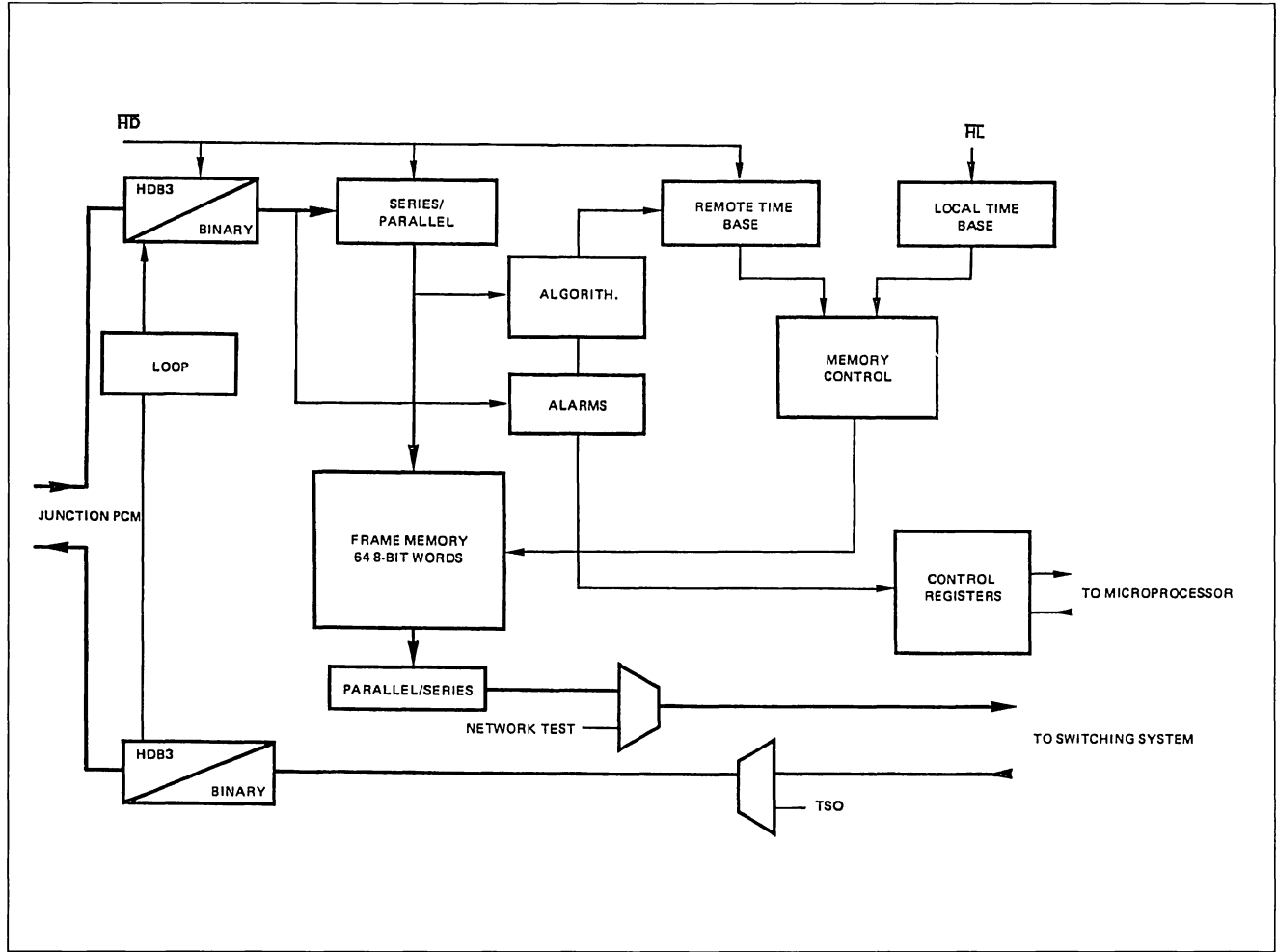
2.2. APPLICATION No. 3 : BINARY INPUTS - BINARY OUTPUT

Figure 11 shows an environment where the EF7333 incoming and outgoing data are binary. Pin AMI is used to select the incoming data code. The incoming signal can be applied either on JE+ or JE– but the unused pin must be tied to VDD. The output signal is available on JS+ and JS–. In the receive mode a device external to circuit EF7333 should deliver :
- the clock signal recovered from an amplifier that has reshaped the signal likely to have been attenuated during line propagation,

- the associated information which has been converted (from HDB3 to binary).

In the same way, in the transmission mode circuit EF7333 receives a multiplex signal from the line, processes the 0 time slot content (TSO) in accordance with CCITT recommendations. A device external to the EF7333 circuit receives the processed multiplex signal and can convert it from binary to HDB3 before transmitting it in line.

This application enables the user to select line reception and transmission amplifiers depending on transmission characteristics.

Figure 11 : Binary Incoming and Outgoing Information.
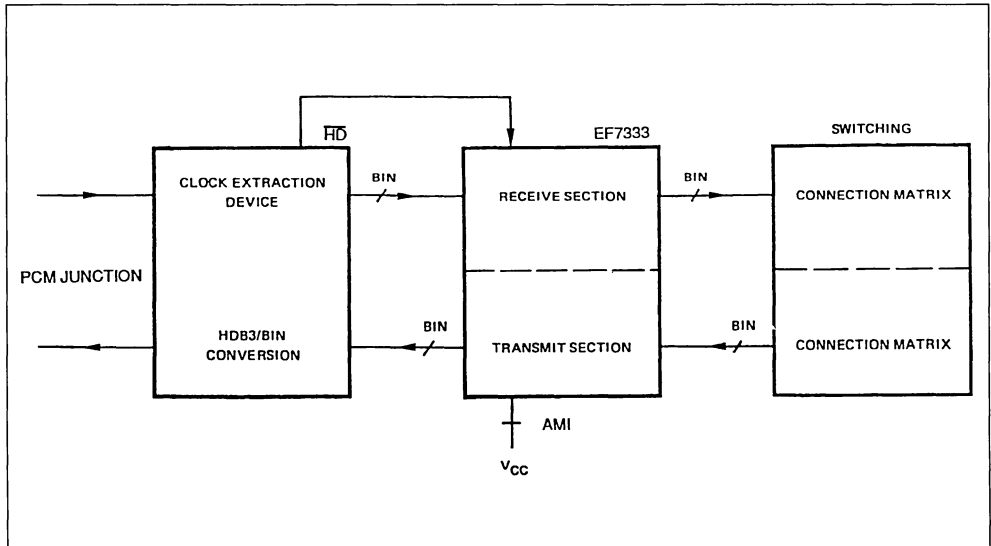
2.3. APPLICATION No. 4 : EF73321 - EF7333 ASSOCIATION USED WITH MARKER INTERFACE.

The diagram in figure 12 shows the whole switching terminal function. No additional circuitry is required between circuits EF73321 and EF7333. They are designed for direct interface.

Figure 12 : EF73321 and EF7333 Association.

t61 : 16384kHz clock
R x T : Line receive transformer
T x T : Line transmit transformer
HL : Local 2048kHz clock
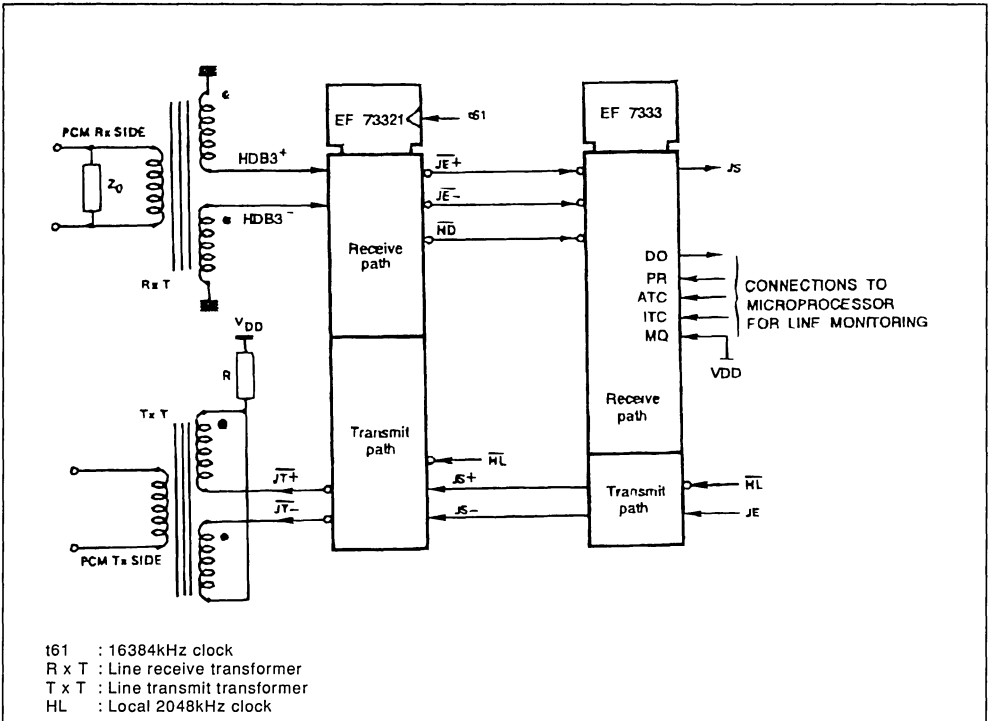
Note : EF73321 layout considerations : for correct operation of transmission drivers, a 100nF decoupling capacitor must be connected between V_{DD} and V_{SS} and located as close as possible to the supply pins.

In this application MQ is wired to V_{DD}. A microprocessor can access the six internal registers R1 to R6. These registers are accessed by pins ITC, ATC, D0 and PR.

Pin ATC receives the register address and pin ITC receives the code to be written into the address register. The last bit of ATC is a read bit and the last bit of ITC is a write bit. The register content may be read serially at D0. PR valids data on ITC state, ATC and D0. D0 is in high impedance when PR is low.

SGS-THOMSON
MICROELECTRONICS

Registers functions :

Register R1 : contains the outgoing junction even frame TS0 value. Only bit 1 can be accessed by the micro-processor interface. The content of this register will be transmitted in line if the circuit is not operating in looped mode.

Register R2 : contains the outgoing junction odd frame TS0 value. Only bit 2 cannot be modified, it remains at "1". Bit 3 can either be at "0" or "1" as a result of a logic OR with the 3 alarms JDSY, TE and MQHX. The content of this register will be transmitted in line only if the circuit is not operating in looped mode.

Register R3 : will contain a value to be introduced into even frame TS0 (8 bits). Its content is transmitted in looped mode.

Register R4 : will contain a value to be introduced into odd frame TS0. Its content is transmitted in looped mode.

Register R5 : is a read only register containing the alarms. It is controlled by receive function of EF7333 circuit.
   • bit 1 contains the value of bit 3 of incoming junction odd frame TS0. When the value of this bit is "1", this means that the remote end does not control the frame it receives any more. (PVTD alarm - remote frame locking loss).
   • bit 2 indicates that the EF7333 synchronous device has found no frame locking code (PVTL alarm - local frame locking loss).
   • bit 3 indicates that clock $\overline{HD}$ is missing (MQHX alarm).
     In this application oscillator t61 has stopped operating.
   • bit 4 indicates that the synchronous device is no more synchronized (JDSY alarm - synchronization loss)
   • bit 5 indicates that a SIA signal is received (SIA alarm - remote alarm indication signal).
     When JDSY = 0, the junction is synchronized and SIA = 0.
     When JDSY = 1, the junction is not synchronized and SIA = 1 during two frames.
   • bit 6 indicates an excessive error rate higher than 10^{-3} detected on the frame locking codes (TE alarm).
   • bit 7 indicates local clock lead or delay compared to remote clock (AV alarm).
     - AV = 1 : frame skip ($\overline{HD}$ faster than $\overline{HL}$).
     - AV = 0 : frame doubling ($\overline{HD}$ slower than $\overline{HL}$).
   • bit 8 indicates frame skip or doubling on reading of internal frame memory. Its state changes on each frame skip or doubling operation (SAUT alarm).

Register R6 : Contains only 1 bit for selecting the looped mode ;
   • if R6 = 0, normal operation, the contents of R1 and R2 are in line.
   • if R6 = 1, looped mode operation. JS+ and JS– are internally connected to JE+ and JE–, and $\overline{HD}$ is internally connected to $\overline{HL}$. The contents of R3 and R4 are in line.

TSO	R6	
	R6 = 0	R6 = 1
Output JS + and JS −	Content of R1 and R2	Content of R3 and R4
Input Reception	Content of $\overline{JE+}$ and $\overline{JE-}$	Content of R3 and R4

Note : Registers R1 to R6 are not initialized when powering-up the EF7333.

2.4. APPLICATION No. 5 : EF7333 WITHOUT MARKER INTERFACE

In this application, pin MQ is wired to V_{SS}. The alarms are directly available on real time on the alarm register outputs. The free bits of register R1 and R2 are set to "1".

Bit 3 of register R5 resulting of the logic OR of three alarms JDSY, TE and MQHX is internally set to "1" and transferred on the line by register 2 bit 3.

Caution :

When MQ = 0, PR, ITC and ATC inputs must also be tied to "0".

2.5. APPLICATION No. 6 : EXTRACTION OF TS16 CONTENT WITHOUT LOSS OF INFORMATION

We have seen that when the remote device was asynchronous with the local EF7333 circuit. Frames may be skipped or repeated between transmit and receive clocks.

For 64 Kbit voice channels, the suscriber will not be aware of frame skips or doubling, but for data channels, OSI system levels 2 (or 3) ensuring the exchange protocol between the two units will request repetition of the message. The following device avoids message repetition although the units are of the plesiochronous type.

Figure 13 : Remote TS16 Extraction.

SGS-THOMSON
MICROELECTRONICS
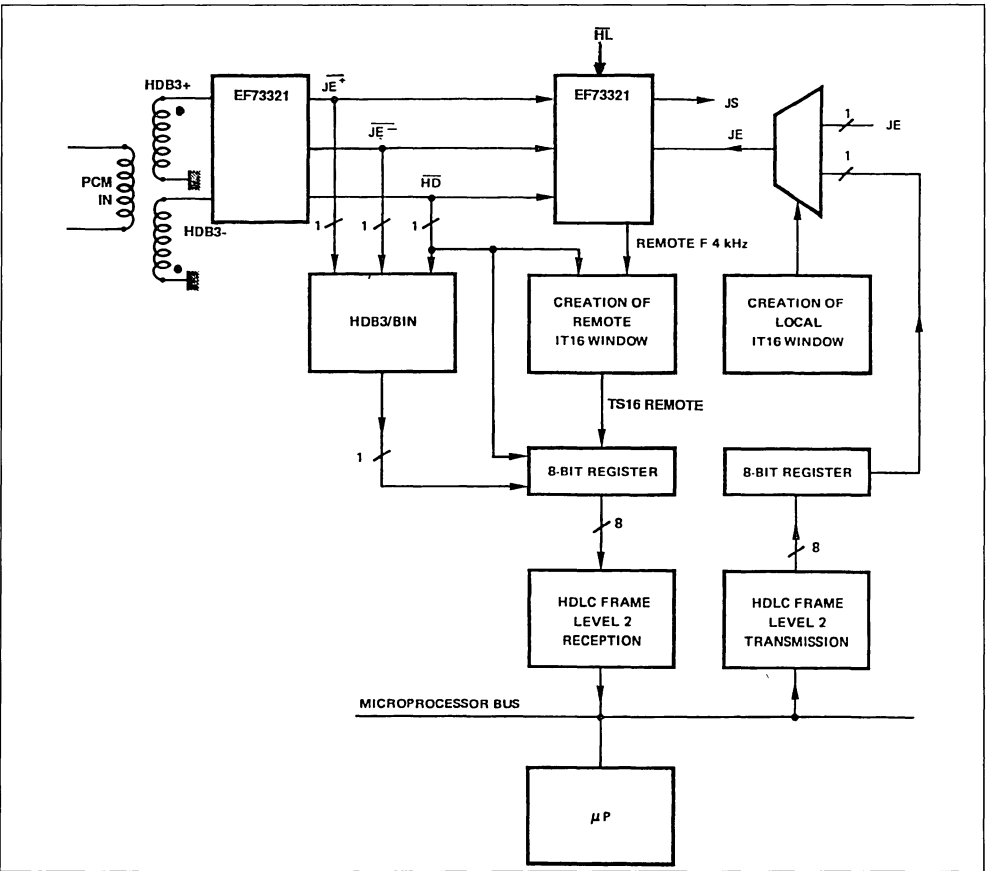
Device description

One of the EF7333 outputs labeled F4kHz (pin 15) delivers 4kHz for the remote clock. The EF7333 extracts the 4kHz remote clock from the incoming junction in the same way as the EF73321 extracts the HD 2MHz remote clock from the incoming junction.

It is possible to extract a TS content, for example TS16 content from incoming signals $\overline{HD}$, $\overline{JE+}$, $\overline{JE-}$ and from signal F 4kHz (fig. 13).

An 8-bit word is delivered to a series-parallel register by a HDB3 converter operating at $\overline{HD}$ clock rate. This word is selected by a device giving the time slot chosen, for example TS16. At the end of TS16 the register content is loaded into a parallel-parallel register ; a microprocessor can read this word after an interrupt for example. In the transmit mode, the microprocessor of figure 13, delivers a HDLC frame that can be inserted in TS16 of circuit EF7333 local multiplex JE (transmit side).

Position of signal F 4kHz with respect to $\overline{JE+}$, $\overline{JE-}$, $\overline{HD}$.

The EF7333 internal logic works on $\overline{HD}$ falling edge (receive side). Figure 14 shows the 250μs period F 4kHz signal with respect to :
- recovered remote clock (pin 12),
- $\overline{JE+}$, $\overline{JE-}$,

The 4kHz signal switches to another state on $\overline{HD}$ falling edge when bit 5 of TS0 arrives on $\overline{JE-}$, $\overline{JE+}$ (pins 7 and 8).

The delay (tpd) compared to $\overline{HD}$ falling edge is 250ns max for a 50pF load.

Figure 14 : F 4kHz Position with Respect to $\overline{HD}$ and Bit Duration of $\overline{JE+}$ / $\overline{JE-}$.

Note : if JDSY = 1, F 4kHz = 0.
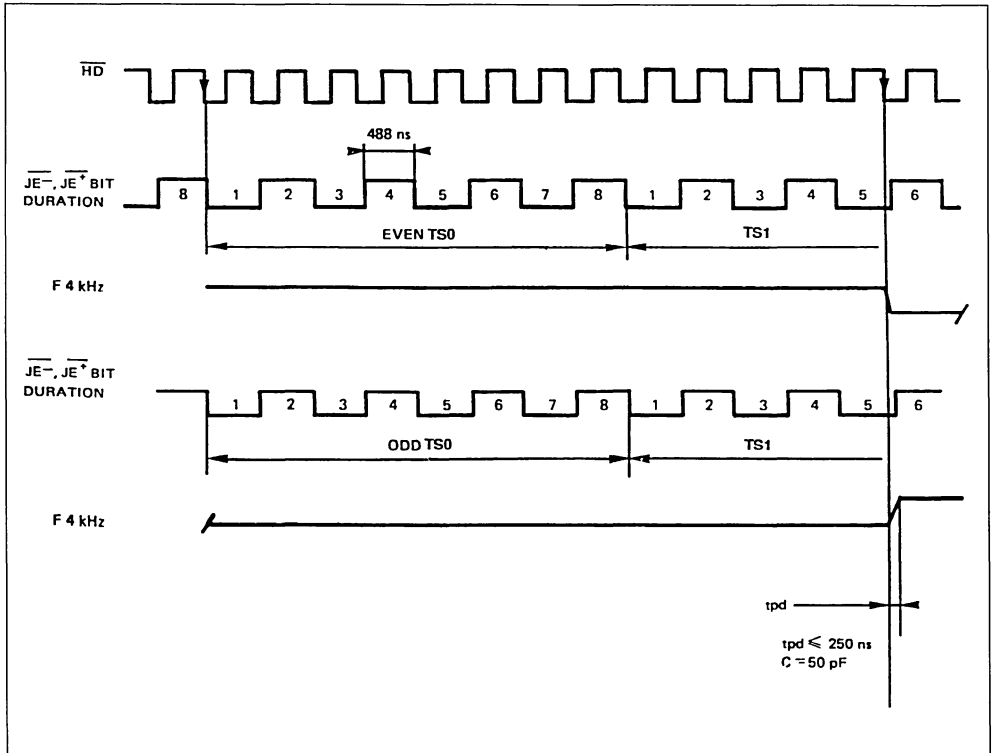
SGS-THOMSON
MICROELECTRONICS

SLIC EVALUATION KIT

This kit is provided in order to give the possibility to make a quick evaluation of all the SGS-THOMSON Microelectronics SLIC KITs.

It consists of one CONTROL BOARD (order code: SLICDEMOBOARD) and different SLIC modules.

The main purpose of the CONTROL BOARD is to provide an easy read/write of the SLICs digital interface that except for L3090/91 are all serial. Data are written by means of eight switches and read by means of five LEDs ; two additional LEDs are provided in order to read the L3090/91 parallel interface. In addition it provides an easy connection for TIP/RING and TX/RX terminations of diferent SLIC

MODULES that can be plugged in proper connectors provided on the board. This board, being very simple, allows to obtain good results also for very accurate measurements (like noise or distortion).

Concerning the SLIC MODULES the following are today available :

L3000/L3030 (order code: L3030EVAL)

L3000/L3090 (order code: L3090EVAL) (*)

L3000/L3091 (order code: L3091EVAL) (*)

TDB7722/TDB7711 (order code: TDB7722/11EVAL) (*)

(*) the same used with the "SLICOMBO" demoboard.

Figure 1 : SLIC Evaluation KIT.
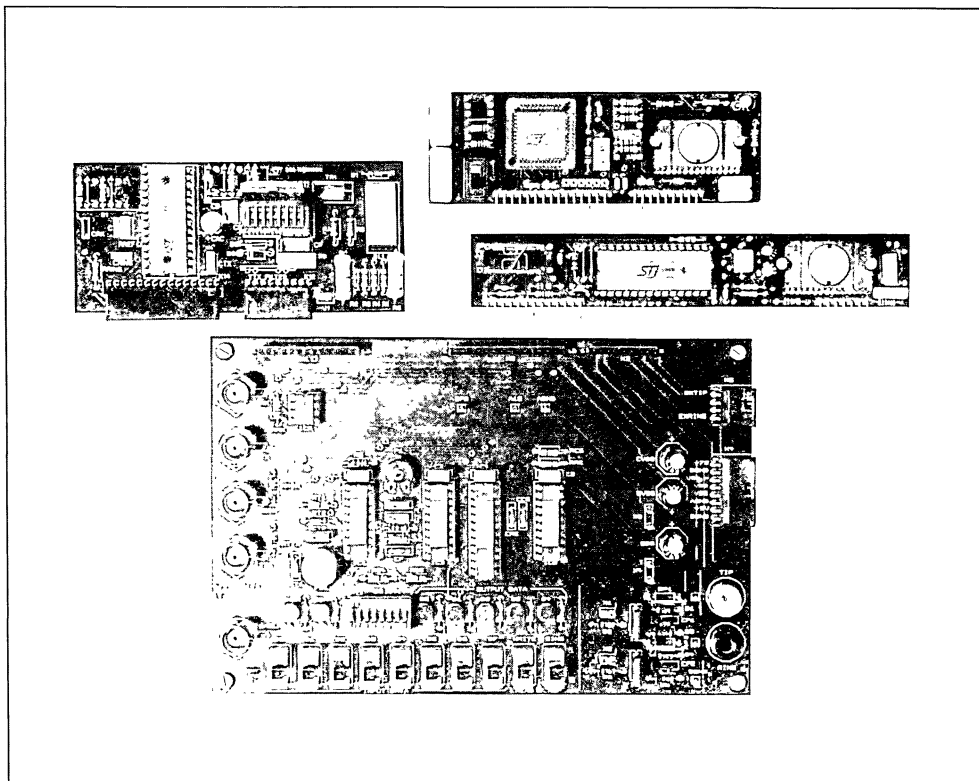
SLICOMBO LINE CARD DEMONSTRATION BOARD

SLICOMBO (order code: COMSLICEVAL) is a conversational demonstration board for the subscriber line card oriented circuits developped by SGS-THOMSON Microelectronics. It includes two complete transmission modules, each of them made of a programmable codec/filter COMBOII associated with a full silicon SLIC to achieve the "BORSCH" function (Battery feed, Overvoltage protection, Ringing, Signalling, Codec/filter, Hybrid 2-wire/4-wire conversion).

The 2-wire interface of each SLIC can be connected to a telephone set or to an appropriate test equipment. The PCM interface of the 2 COMBOs can also be connected to a PCM test equipment, or to the same PCM highway, thus allowing a real phone conversation between the 2 telephone sets through the

2 SLICs and the 2 COMBOs.

As SGS-THOMSON Microelectronics provides a wide range of SLICs, they are implemented on interchangeable modules; 2 modules are available: one version is for the central office oriented SLIC TDB7711/7722, and one version for the PABX oriented SLIC L3090/L3000. SLICOMBO can operate either with 2 TDB7711 or with 2 L3090 SLIC modules.

The user interface with the board is performed by an IBM Personnal Computer or true compatible. An interactive software inputs the commands from the user and displays the results on the screen; a multi-menus approach is used by the software to make easy the programming of the SLICOMBO board.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE
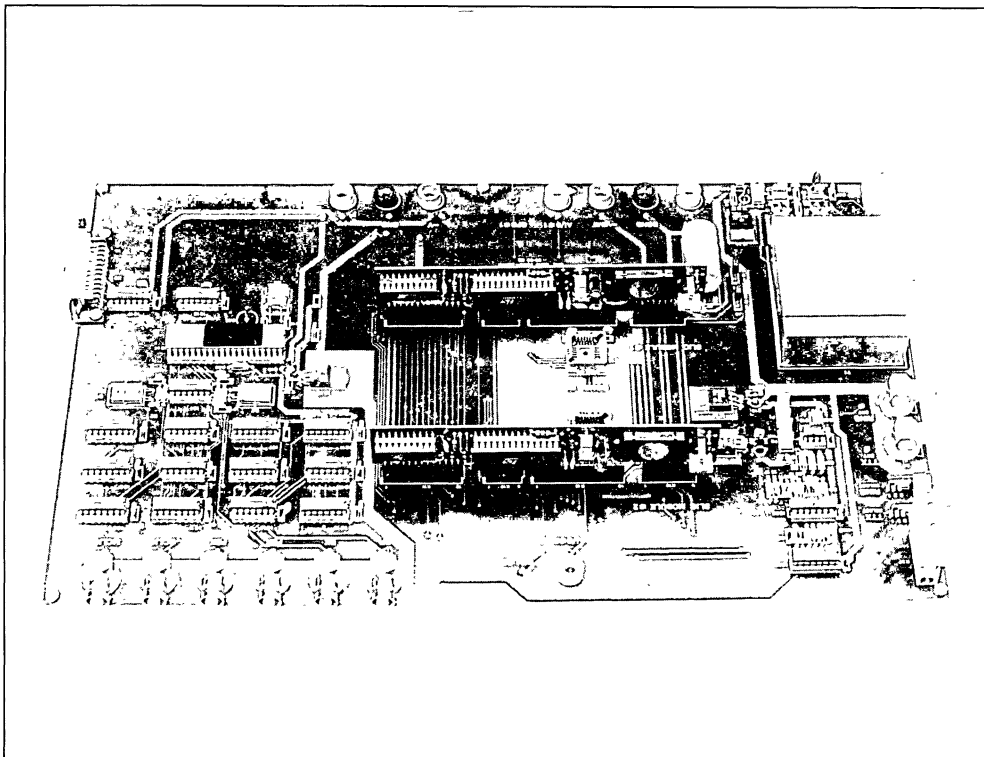
RELIABILITY REPORT : ETC5040 FILTER, ETC5057 AND ETC5067 COMBOS

1 . RELIABILTY TEST MATRIX

The reliability evaluation program designed for the ETC5040 FILTER, ETC5057 and ETC5067 COMBOS requires the following tests :

- Operating life test
- Temperature cycling

2 . TEXT DESCRIPTION

2.1. HIGH TEMPERATURE OPERATING LIFE TEST

The basic test used to evaluate device reliability is high temperature operating life test.

Failure mecanisms from the random area of the reliability life are accelerated at 125 °C.

The devices are loaded on boards and they are dynamically exercised as shown in the following figure.
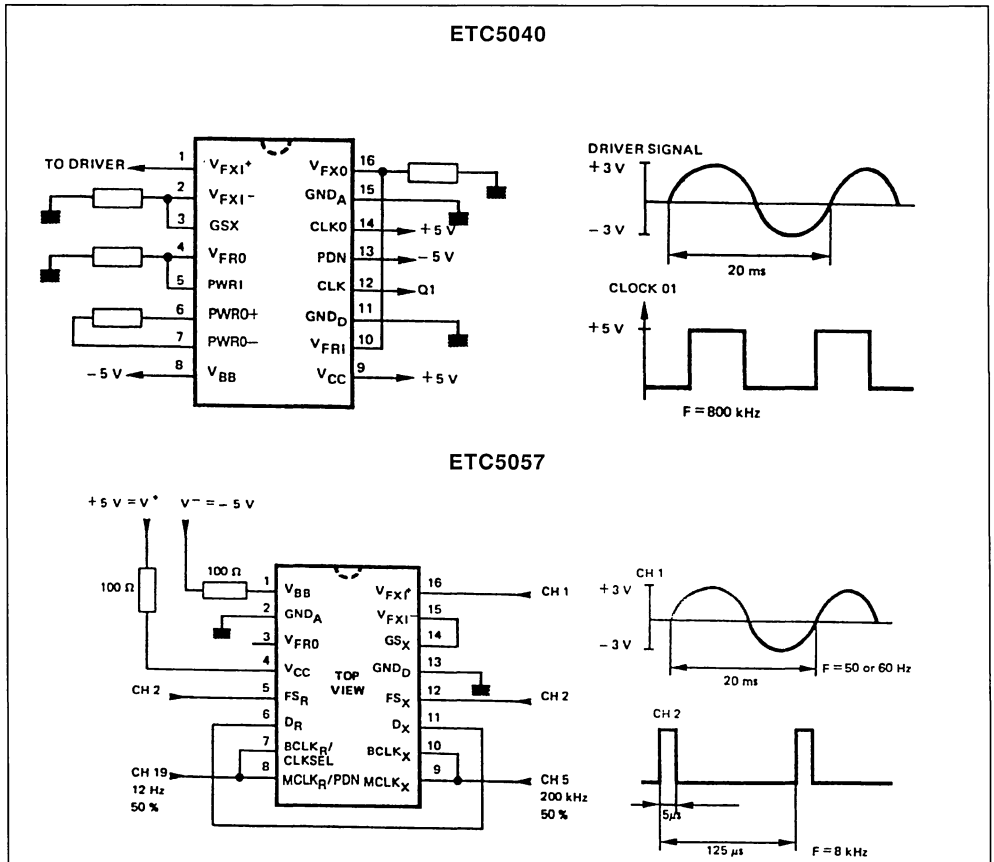
2.2 OPERATING LIFE TEST FAILURE RATE COMPUTATION

The degradation processes affecting the reliability of electronic devices is such that the failure rate can be described by the Arrhenius model.

$\lambda (T) = K \exp \dfrac{-E_A}{kT}$ (2)

E_A : Activation energie (e)

k : Boltzmann's constant
$(8.63 \times 10^{-5} \, eV \, K^{-1})$

T : Absolute temperature (K)

K : Constant

At a given temperature, the failure rat is defined as :

$\lambda (T) = \dfrac{N}{N_D \cdot T_H}$ (3)

N : Number of failures

N_D : Number of devices tested

T_H : Number of test hours

To determine the corresponding failure at other temperatures, an acceleration factor given by the Arrhenius Relationship is used :

$F (T1, T2) = \dfrac{\lambda (T1)}{\lambda (T2)} \left[\dfrac{-E_A}{K} \left(\dfrac{1}{T1} - \dfrac{1}{T2} \right) \right]$ (4)

T_1 : Junction temperature during test (K)

T_2 : Desired junciton temperature (K)

Shows the acceleration factor for different thermal activation energies (Arrhenius plot)

Arrhenius plot, used for the calculation of the acceleration factor for a given activation energy
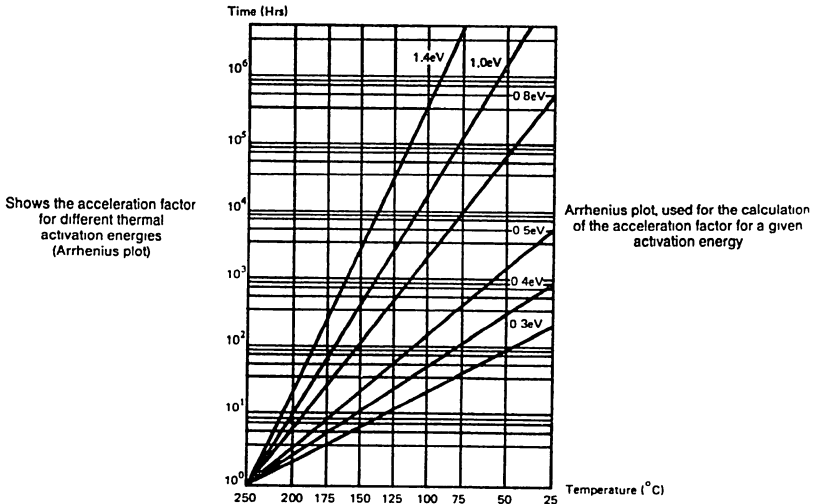
Using equation), we can determine the equivalent device-hours E_{ND} T_H at temperature T_2 for a given activation energy :

$EN_{D. \, TH} (2) = F (T_1, T_2) \times N_D \cdot T_H (T_1)$ (5)

Thus the equivalent failure rate at temperature T_2 comes as :

$\lambda (T_2) = \dfrac{N}{EN_D \, T_H (T_2)}$ (6)

The failure rate of a device showing failures with different activation energies is computed by summing equation (6) on all the activation energies :

$$\lambda \, (T_2) = E_i \quad \frac{N_i}{(EN_D \, T_H) \, i \, (T_2)} \qquad (7)$$

Where N_i is the number of detects with an activation energy of E_{Ai}.

In this report, failure rate computations on high temperature operating life test data are performed with a confidence level) of 60 %, using the CHI-SQUARE (X^2) distribution as shown in (8).

$$\lambda \, (T) = \frac{X^2 \, (1 - CL), \, (2N + 2)}{2 \, N_D \cdot T_H} \qquad (8)$$

CL : Confidence level

For high temperature life test data, CL = 0.6 (60 %)

2.3 TEMPERATURE CYCLING

This test evaluates the devides ability to withstand both extermes of temperatures and rapid changes in temperature.

Temperature cycling is effective in testing thermal expansion compatibility of the various mechanical interfaces present on the device.

Test Conditions :

Ceramic encapsuled devices are submitted to temperature cycling specified by Mil Std 883C Method 1010.1 condition C which states a sequence of 100 cycles (air to air) from 65°C up to 150°C, with a transfer time less than 5 mn.

3 . RELIABILITY TEST RESULTS

ETC 5040
HIGH TEMPERATURE OPERATING LIFE TEST (HTOL)
TEMP. 125'C

Lot	168 H	500 H	1000 H	2000 H	3000 H
A	0/80	0/80	0/80		
B	1/100	0/99	0/99	0/99	0/99
C	0/59	0/59	0/59	0/59	
D	0/70	0/70	0/70	1/70	
E	0/70	0/70	0/70	0/70	
F	0/80	0/80	0/80	0/80	
G	0/80	0/80	1/80		
H	0/80	0/80	0/80		
I	0/80	0/80	1/80	0/79	
J	0/80	0/80	0/80	0/80	
K	1/80	0/79	0/79	0/79	
L	0/80	0/80	0/80		
M	0/80	0/80	0/77		
N	0/80	0/80	0/79		
O	0/80	0/80	0/80		
P	0/80	0/80	0/79		
Q	0/79	0/79	0/79		
R	0/80	0/80	0/80		
S	0/80	0/80	0/80		
T	0/80	0/78	0/78		
U	0/80	0/80	0/75		
V	0/76	0/76	0/76		
W	0/80	0/80	0/80		
X	0/77	0/77	0/77		
Y	0/80	0/80	0/80		
Z	0/80	0/80	0/80		
AA	0/77	0/77	0/77		
AB	0/80	0/80	0/80		
AC	0/80	0/80	0/80		
AD	0/80	0/80	0/80		
AE	0/78	0/78	0/77		
AF	0/80	0/79	1/79		
AG	0/80	0/80	0/80		
AH	0/39	0/39	0/39		
AI	0/40	1/40	0/39		
AJ	0/45	0/45	0/45		
AK	0/80	0/80	0/80		
AL	0/44	0/44	0/44	0/44	
AM	0/45	0/45	0/45	0/44	
AN	0/45	0/45	0/45	0/45	
AP	0/39	0/39	0/39		
AQ	0/50	0/50	0/50		

SGS-THOMSON
MICROELECTRONICS

ETC 5057
HIGH TEMPERATURE OPERATING LIFE TEST
TEMP. 125' C

Lot	168 H	500 H	1000 H	2000 H
A	0/74	1/74	0/73	
B	2/80	0/78	0/78	
C	0/70	0/70	0/70	
D	0/83	0/83	0/83	
E	0/80	0/80	0/80	
F	0/80	0/80	0/80	
G	0/77	0/77	0/77	
H	0/75	0/75	0/75	
I	0/75	0/75	0/75	
J	0/80	0/80	0/80	
K	0/80	0/80	0/80	
L	0/80	0/80	0/80	
M	0/80	0/80	0/80	
N	0/80	0/80	0/80	
O	0/80	0/80	0/80	
P	0/80	0/80	0/80	
Q	0/80	0/80	0/80	
R	0/80	0/80	0/80	
S	0/80	0/80	0/80	
T	0/80	0/80	0/80	
U	0/80	0/80	0/80	
V	0/75	0/75	0/75	
W	0/80	0/78	0/78	
X	0/80	0/80	0/80	
Y	0/80	0/80	0/78	
Z	0/80	0/75	0/75	
AA	0/70	0/70	0/70	
AB	0/79	0/79	0/79	
AC	0/79	0/79	0/79	
AD	0/79	0/79	0/79	
AE	0/79	0/79	0/78	
AF	0/80	0/79	0/79	
AG	0/80	0/80	0/80	
AH	0/79	0/79	0/79	
AI	0/78	0/78	0/78	
AJ	0/80	2/80	0/78	
AK	0/80	0/80	0/80	
AL	0/78	0/78	0/77	
AM	0/80	0/80	0/73	
AN	0/79	0/79	0/77	
AO	0/76	0/76	0/72	
AP	0/80	0/79	0/79	
AQ	1/43	0/42	0/42	0/42
AR	0/48	0/48	0/48	0/48
AS	0/40	0/40	0/40	
AT	0/45	0/45	1/45	0/43
AU	0/80	0/80	0/80	
AV	0/80	0/80	0/80	
AW	0/45	0/45	0/45	0/45
AX	1/45	0/44	0/44	
AY	0/45	0/45	1/45	
AZ	1/45	0/43	0/43	
BA	0/45	0/45	0/45	0/45
BB	0/80	0/80	0/80	

ETC 5067
HIGH TEMPERATURE LIFE TEST
TEMP. 125'C

Lot	168 H	500 H	1000 H	2000 H
A	0/80	0/80	0/80	0/80
B	0/80	0/80	0/80	0/80
C	0/80	0/79	0/79	0/79
D	0/80	0/80	0/80	
E	0/72	1/72	0/71	
F	0/72	0/72	0/72	
G	0/80	0/80	0/80	
H	0/72	0/72	0/69	
I	0/72	0/72	0/72	
J	1/80	0/79	0/79	
K	1/45	0/44	0/44	
L	0/80	0/80	0/80	
M	0/44	0/44	0/44	0/44

TEMPERATURE CYCLING
(100 CY)

Lot	ETC 5040	Lot	ETC 5057	Lot	ETC 5067
A	0/40	A	0/38	A	0/47
B	0/23	B	0/40	B	0/40
C	0/50	C	0/40	C	0/40
D	0/40	D	0/45	D	1/40
E	0/40	E	0/39	E	0/40
F	0/37	F	0/40	F	0/40
G	0/36	G	0/40	G	0/40
H	0/39	H	0/40	H	0/40
I	0/40	I	0/40	I	0/40
J	0/40	J	0/40	J	0/40
K	0/40	K	0/37	K	0/40
L	0/40	L	0/38	L	1/40
M	0/40	M	0/40		
N	0/40	N	0/39		
O	0/40	O	0/40		
P	0/40	P	0/40		
Q	0/40	Q	0/40		
R	0/40	R	0/40		
S	0/40	S	0/40		
T	0/40	T	0/45		
U	0/40	U	0/40		
V	0/40	V	0/40		
		W	0/40		
		X	0/38		
		Y	0/38		
		Z	0/38		

SGS-THOMSON
MICROELECTRONICS

4 . FAILURE RATE PREDICTION FOR ETC5040 / ETC5057 / ETC5067

4.1. OPERATING LIFE TEST FAILURE RATE :

Test estimation was made by assiging to all failures the average activation energy for MOS devices, defined by standards such as the MIL-HDBK 217B ($E_A = 0.7$ eV).

The acceleration factor was computed using junction temperatures taking into account the package thermal resistance and device power dissipation.

Results of this estimation are summarized in the following table :

	Device Hours at 125'C	EA (EV)	Equivalent Device Hours at 55'C	Life Test Failures	Failure Rate in Fits (60 % C. L.)
ETC5040J	3.85×10^6	0.7	2.77×10^8	7	30
ETC5057J	4.06×10^6	0.7	2.92×10^8	10	39
ETC5067J	1.21×10^6	0.7	8.71×10^8	3	48

5 . CONCLUSION

- This report summarizes updated reliability data for MCOS ETC5040 Filter and ETC5057 and ETC5067 COMBOS from SGS-THOMSON Micro-electronics.
- Using operating life test results, a failure of 30 fits may be predicted at 55 C (60 % C.L., EA = 0.7 eV) for ETC5040 and 39 for ETC5057. The failure rate for ETC5067 is expected to decrease since currently tested devices will generate additional devices hours.

SLIC PROTECTION

A. BREMOND

I INTRODUCTION

The goal of the telecommunication network (fig.1) is to permit the data exchange (speech or digital) between two (or more) subscribers.

The network is made up of different parts which are subject to various disturbances.

The most susceptible elements are the lines, due to their lenght and their geographical location.

Disturbances strike the lines and are then propagated to the extremities of the lines at which lie telephone set and the subscriber line interface card (SLIC).

So the lines receive two kinds of overvoltages :

Surges of short duration with high peak voltage value (a few hundred micro-seconds for a few thousand volts). These are generated by atmospheric phenomena.

Surges of long duration with medium voltage value (greater than one second for a few hundred volts RMS) which are due to the mains AC power networks.

Fig.1 Classical telecommunication network topology.
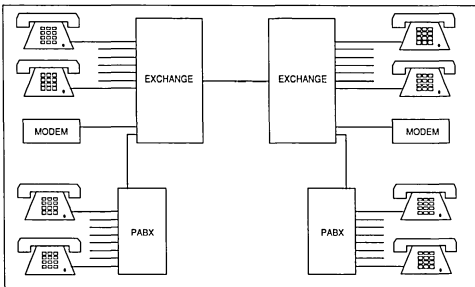
The purpose of this application note is to analyse these 2 kinds of overvoltages and to propose different protection solutions dedicated to the SLIC.

II OVERVOLTAGES ACROSS TELECOMMUNICATION LINES :

II.1 Atmospheric effects :

Fig.2 Lightning phenomenum
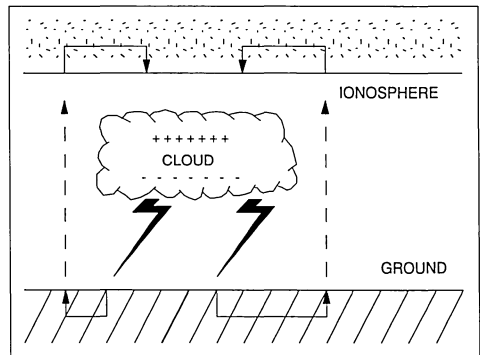
Lightning phenomena are the most common surge causes. They are mainly due to a voltage difference between the ground and the clouds (a few 100 kV). Two kinds of strikes may occur. Negative discharge with a peak current of 50 kA, rise time of 10μs to 15μs and 100μs duration.

Positive discharge with a peak value of 150 kA, rise time between 20μs and 50μs and a duration between 100ms and 200ms.

The lightning effect appears on the lines in two ways.

– Direct shock.
– Induced shock.

Fig.3 Direct lightning strike.
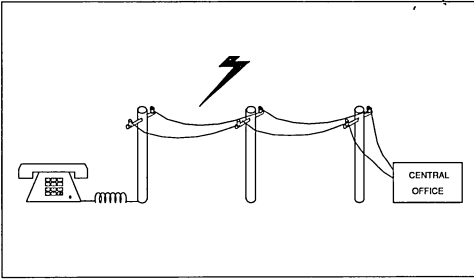
The Fig.3 shows the first case which is produced mainly on overhead lines.

Induced shock is more frequent than a direct shock. Lightning strike the ground and a current flows in the cable shield. This current produces a voltage gradient which in some places is above the insulation capability of the cable material (Fig.4).

Fig.4 induced strike.
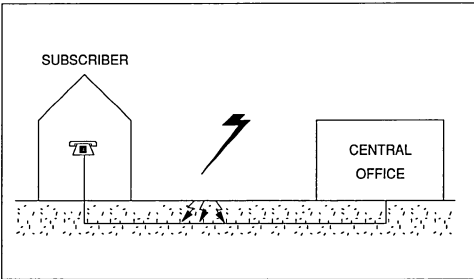
II.2 Proximity and crossing with AC mains lines :

For these kinds of surges two cases may be seen :

The first one is due to the falling of an AC mains cable on a telephone line.

The second case is produced by the proximity of a subcriber line with an AC mains line or equipment (mainly capacitive coupling).

It is interesting to note for these types of disturbances a RMS value of a few Amps for a duration of between 1 s and 15 mn.

III PRIMARY AND SECONDARY PROTECTION :

The figures in chapter II give us an idea of the energy which may appear on the lines. (so in the field these surge values are lower due to the losses of ground resistance, the capacitive coupling and so on, but are signifiant nevertheless).

We have to divide these disturbances into two families :

High peak value and short duration (lightning)

Short peak value and long duration (crossing with AC power).

For both cases the present state of the art of silicon protection devices does not permit the suppression of these levels of energy.

A second parameter to keep in mind is the very low clamping factor (1) needed by the IC's used to realize the line interface. This fact necessitates the designer to use a protection solution with silicon (fast response time/low clamping factor).

High energy values and low clamping factor impose two protection levels.

Fig.5 Primary/secondary protection topology.
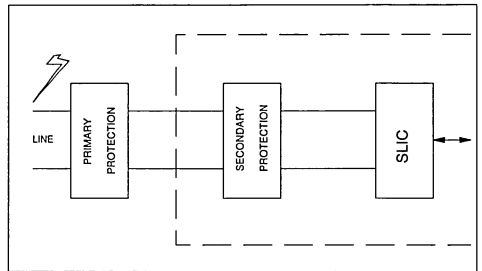
The first level called primary protection (fig.5) located on the connecting terminal of the exchange, suppresses the major part of the disturbance. The second level called secondary protection reduces the remaining overvoltage.

(1) the clamping factor is the ratio of the normal operating voltage over the maximum clamping voltage.

![SGS-THOMSON MICROELECTRONICS]

Fig.6 Primary/secondary protection levels effects

A/ Overvoltage across the line without protection
B/ Remaining voltage after the primary level action.
C/ Remaining voltage after the secondary level action
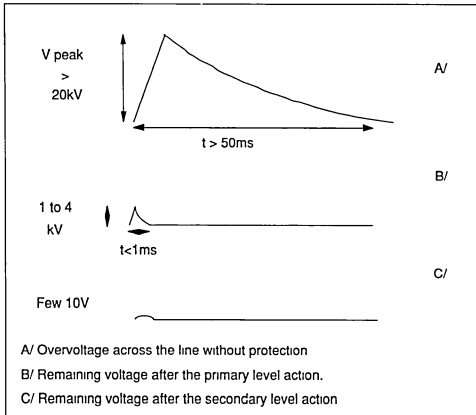
The figure 6 shows the goal of both protection levels.

In this example the surge across the line without protection will be a few 10 kV peak value for a few 10 ms length (Fig.6A)

After the primary protection the major part of the energy is cancelled (Fig.6.B). The remaining overvoltage may be a few kV (depend on the dv/dt of the surge and the surge arrestor technology used).

Across the second level protection the voltage does not exceed a few 10 Volts.

III.1 Primary protection :

Actually two kinds of primary protection are used :
 – carbon gaps.
 – gas tubes.

III.1.A Carbon gaps :

Fig.7 Carbon gap based primary protection.
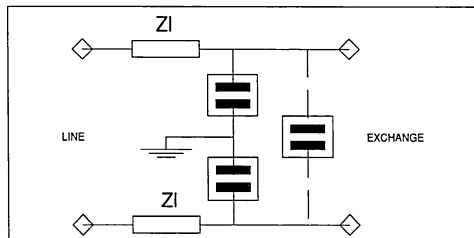
These components are made by two carbon electrodes. In fact the carbon gap is the low cost primary protection but it has two major disadvantages :
 – its short life duration
 – its variable spark threshold.

III.1.B Gas tubes :

Fig.8 Gas tube based primary protection.
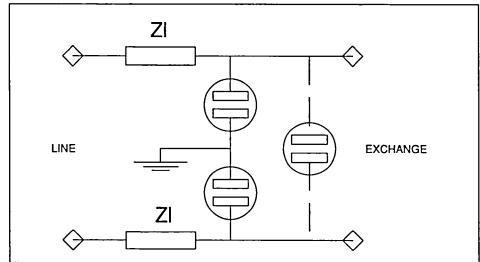
These components are made by two metallic electrodes in a sealed case. Generaly the sealed tub contains a low pressure gas.

Fig.9 Gas tube characteristics.

1/ Sparkover voltage
2/ Glow discharge voltage
3/ Remaining voltage in switch on mode
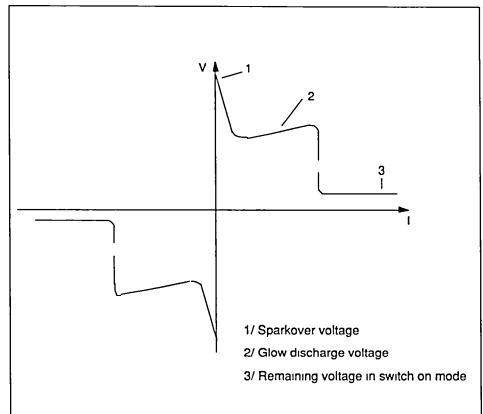
The major disadvantage of this kind of device is its response time, in fact the maximum voltage across the gas tube depends on the dv/dt of the surge.

III.2 Secondary protection :

III.2.A Series and parallel protection :

Fig.10 Series and parallel protection.

1/ Series protection.
2/ Parallel protection.
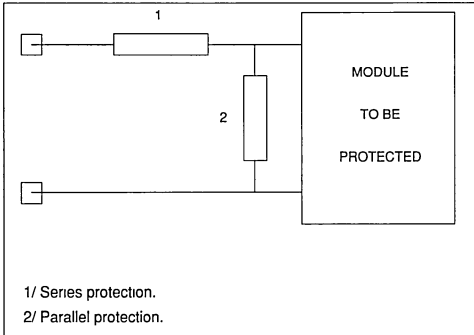
The secondary protection level is generaly achieved with two types of devices :

The series protection ensures the protection against the proximity or the crossing with AC power lines.

The parallel protection operates to suppress the overvoltages due to the lightning effects.

* Series devices :

Series devices operate by opening of the circuit or by an increment of the resistance.

Fig.11 Fuse protection.
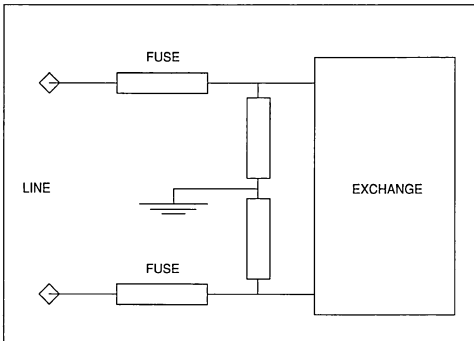
The fuse is classical case of protection by opening of the circuit. Figure 11 shows an exchange protected by fuses and figure 12 represents an example of the limit curve of the fusing action.

Fig.12 Fuse fusion function.
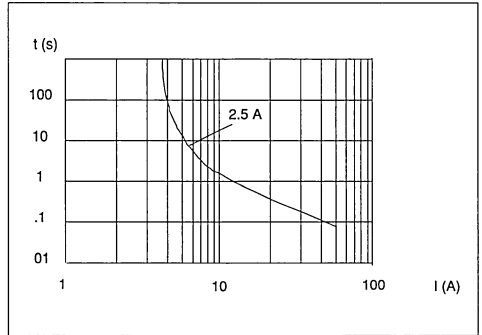
These components provide an absolute security after action, but their major disadvantage is the need for maintenance.

Fig.13 PTC based protection.
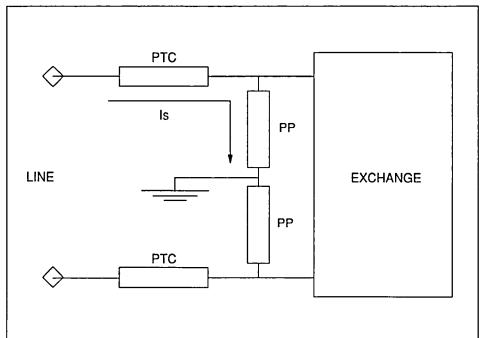
The PTC thermistor is a device which operates by very rapid resistance increase as a function of the temperature.

When the surge occurs across the line, the parallel protection PP is activated.

The surge current Is, generated by PP action, flows through the PTC and increases its internal temperature. As shown on the figure 14 the resistance value of the PTC rises quikly with the temperature.

SGS-THOMSON
MICROELECTRONICS

Fig.14 Resistance versus temperature.
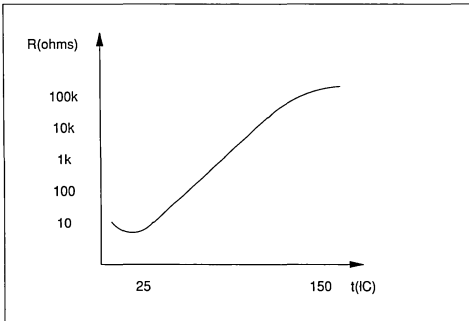
The major disadvantage of the fuse does not exist with the PTC. Unfortunatly this kind of component presents a big tolerance, a long time to return to its stand off point and a drift of its value.

An other series device is the resistance which permits to limit the current through the parallel protector.

* Parallel devices :

The parallel protection function may be assumed by different devices based on different technologies.

In fact it is clear that the future in term of SLIC topology is based on the use of IC.So the consequent requirement for good response times and high clamping factor necessitates the use of silicon protection.

Parallel silicon protection functions in two different modes.

Fig.15 Clamping characteristics.
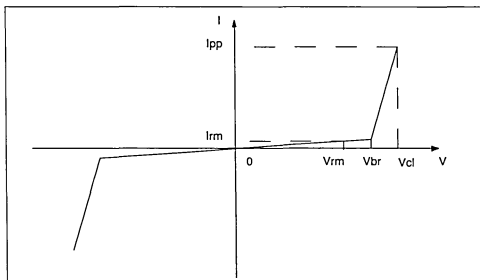
* Clamping mode :

This device named TRANSIL is based on the breakdown effect. During the stand off time the working point is located between 0 and V_{RM} (see curve of fig.15) and the device draws a very low leakage current (< 5 μA at 25°C). When a surge occurs across the line the working point is located between V_{BR} and V_{CL} the increase of the voltage is low (good clamping factor) and the current drawn very high.

Fig.16 TRANSIL symbols.

UNIDIRECTIONAL   BIDIRECTIONAL
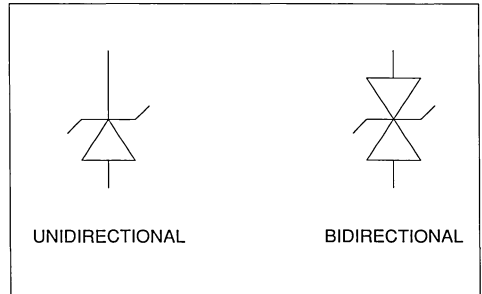
The TRANSIL may be uni or bidirectional.

During the clamping action the major part of the energy is dissipated in the TRANSIL.

Fig.17 CROWBAR characteristics.
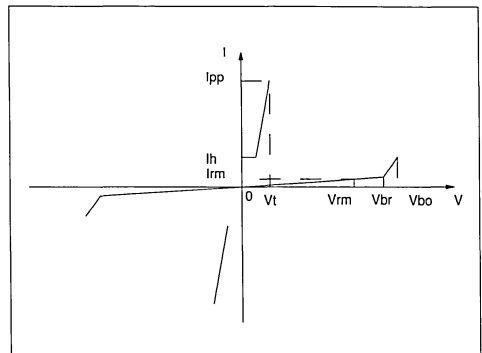
* Crowbar mode :

The CROWBAR device named TRISIL is based on the breakover effect. In fact in normal operating the device operates in the area between 0 and V_{RM} (see curve fig.17) and the bias current through the protection is very low (< a few μA at 25°C).

When the surge occurs the TRISIL begins to work in the clamping mode between V_{BR} and V_{BO}. After that the device fires and operates like a short circuit.

After the surge, the current decreases and falls below the holding current IH. This condition causes the TRISIL to switch off and the return to the stand off area.

Fig.18 TRISIL symbols.

FIXED VBO   AJUSTABLE VBO
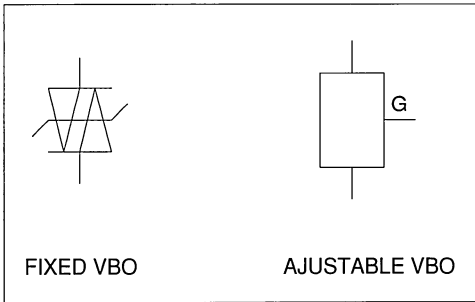
There are two kinds of TRISIL, the fixed breakover voltage type and the device with adjustable breakover voltage.

During the surge suppression action of the TRISIL the major part of the energy is dissipated in the series elements of the line.

This last fact makes the TRISIL better adapted to protect againt the high energy of the lightning overvoltages.

IV STANDARDS :

These standards define the two kinds of overvoltage (lightning and crossing).

IV.1 Lightning simulation :

The lightning overvoltage is simulated by a bi-exponentional wave, which are defined by the rise time t1 and the duration t2 between the start and the passage of the deacrising edge at half peak value (fig.19).

Fig. 19 Standard wave.
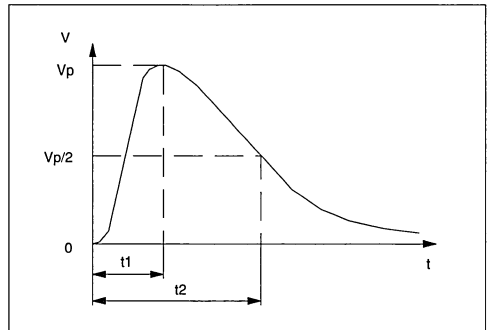
Each country published its standard, which can be summarized by the times t1 and t2, the peak voltage of the wave and the surge generator diagram.

The table here after gives a unexhaustive list of the standard :

COUNTRY	AUTORITY	WAVEFORM (µs)
ENGLAND	BRITISH TELECOM	10/700
FRANCE	PTT	0.5/700
GERMANY	BUNDESPOST	10/700
ITALY	SIP	0.5/700 1/100
SPAIN	COMPANY TELEPHONICA DE ESPANA	1/1000
SWEDEN	TELEVERKET	10/700
SWITZERLAND	PTT - BETRIEBE	10/700 1.2/50
USA	BELL	10/1000 10/360 2/10
	FCC	10/560 10/160 2/10

The following figures give us the diagram of the surge generators mainly used :

SGS-THOMSON MICROELECTRONICS

Fig. 20 10/700µs wave generator.
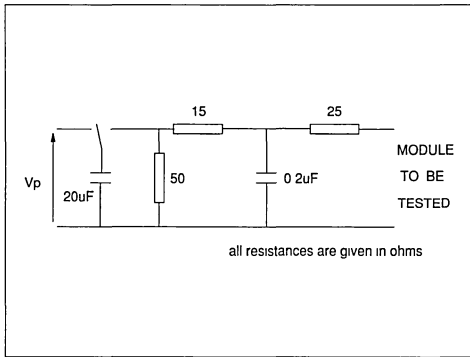
Fig. 23 1.2/50µs wave generator.
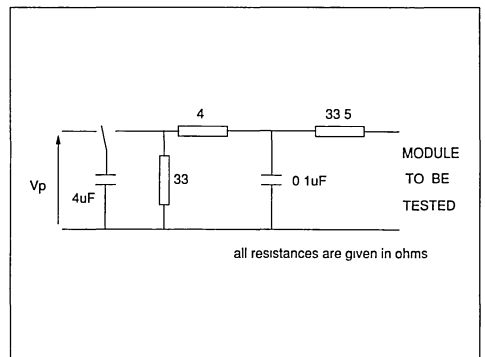
Fig. 21 0.5/700µs wave generator.
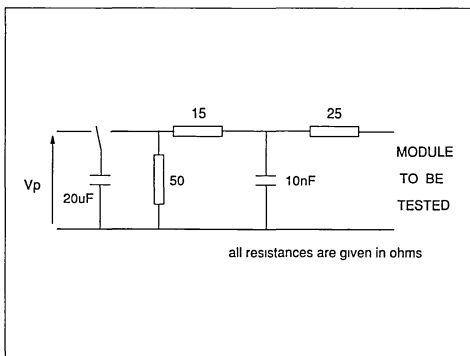
Fig. 24 10/560µs wave generator.
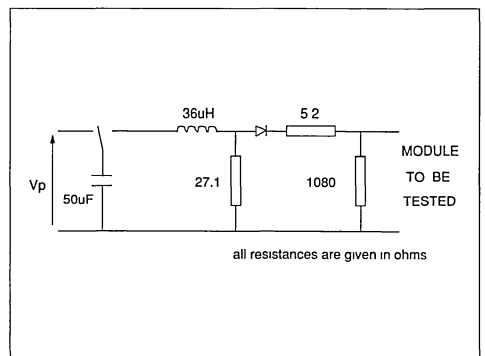
Fig. 22 1/1000µs wave generator.
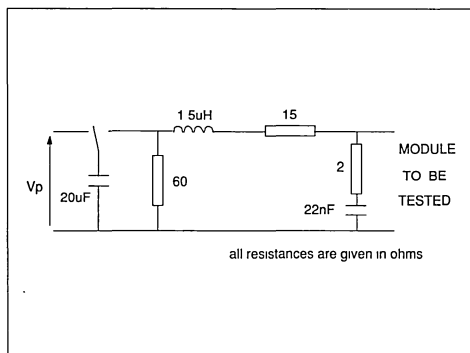
Fig. 25 10/160µs wave generator.
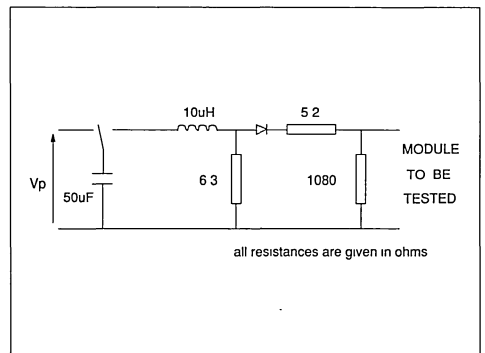
Fig. 26 2/10μs wave generator.

all resistances are given in ohms
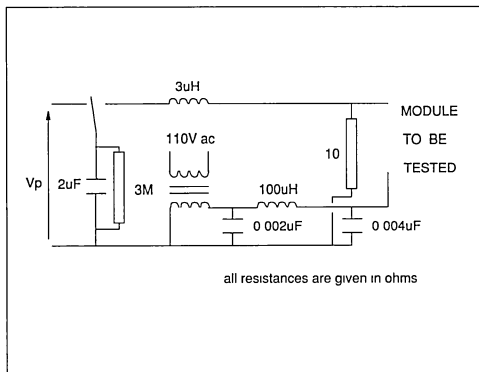
IV.2 Crossing or proximity with main ac lines :

Crossing or proximity are simulated by a sinus generator (50 or 60 Hz) which injects through a series resistor during a defined time (fig.27).

Fig. 27 Crossing simulation generator.
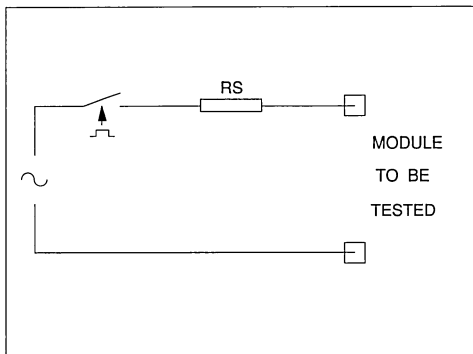
Here after are given some examples of crossing simulation

COUNTRY	VOLTAGE Volts RMS	SERIES RESIS-TOR (Ohms)	DURATION
ENGLAND	0 TO 250 0 TO 650 0 TO 430 (50 Hz)	40 TO 400 150 150	15 mn 1 s 2 s
FRANCE	O TO 1000 > 1000 (50 Hz)	20 3000	trains of 1 s "ON" 2 s "OFF" 10 times with 3 mn be-tween each trains
GERMANY	300 (50 Hz or 16.6 Hz)	600	200 ms
ITALY	300 650 220	600 200 10 or 600	500 ms 500 ms 15 mn
USA	0 - 50 50 - 100 100 - 600	150 600 600	15 mn 15 mn 60 x 1 s application

.V SLIC FUNCTION :

V.1 SLIC generalities :

The SLIC function is defined by the nemotechnic word BORCHT :
- Battery feeding
- Overvoltage protection
- Ringing
- Signalling
- Cofidec
- Hybrid
- Test

The important parameters to define the OVERVOLTAGE PROTECTION are the battery feeding and the ringing signal.

V.1.A Battery feeding :

This sub-function of the SLIC is characterized by :
- the battery voltage typical value (generaly between 45 and 65 V)
- the tolerance of the voltage value
- the possibility to switch from one value to another one (case of line cards designed to operate equally on normal and long lines)

V.1.B Ringing signal :

For the ringing two parameters are to be taken into account :
- the voltage value (generaly between 70 and 100 V RMS)
- the ringing configuration (fig.28)

Fig. 28 Different ringing configurations.
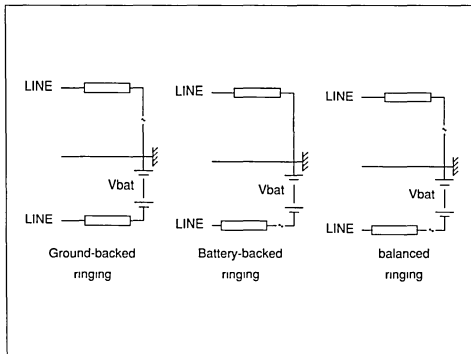
V.2 Different kinds of SLIC :

There are two SLIC families :
- the SLIC without integrated ring generator.
- the SLIC with integrated ring generator.

Fig. 29 SLIC without integrated ring generator.
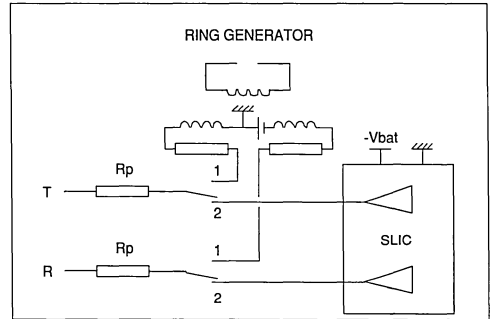
V.2A SLIC without integrated ring generator :

For this case the SLIC IC is supplied between the ground and the battery voltage (- Vbat).

The relay operates the selection of functions, ringing mode in position 1 and the other modes in position 2.

Fig. 30 SLIC with integrated ring generator.
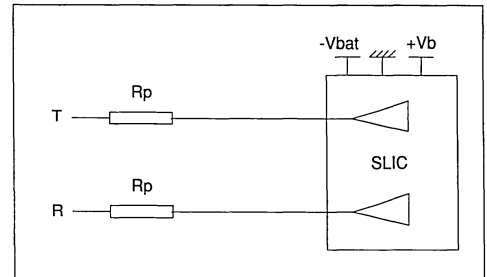
V.2 B SLIC with integrated ring generator :

This kind of SLIC, only composed by the L3000 family of SGS THOMSON, is supplied between the ground, the battery (-Vbat) and a positive voltage (+VB) up to +72 V.

V.3 Goal of the SLIC protection :

The purpose of the protection is to suppress all overvoltages out of the normal operating range voltage of the SLIC.

We have to take into account the two kinds of SLIC seen in paragraph V.2.

Fig. 31 Goal of the protection for the SLIC without integrated ring generator.
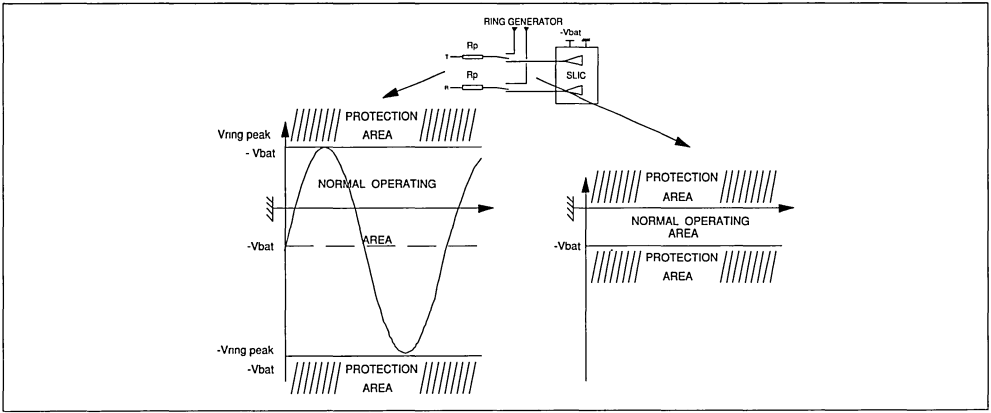
V.3.A SLIC without integrated ring generator :

As shown in the Fig.31 the protection areas are located differently before and after the ring relay.

Before the relay the protection must operate over the peak value of the ring signal (generally +90V and -190V). As the relay protection does not require a very precise clamping threshold, we usually use a symetrical overvoltage suppressor (generaly + or - 200V).

After the relay the protection acts to suppress all spikes over the ground and under the battery voltage (-Vbat).

It is important to note that the integrated circuit needs a protection threshold closest than the supply voltage.

Fig. 32 Internal diodes network of the TDB7722.

In certain cases (the TDB7711/7722 of SGS THOMSON) an internal network of diodes permits to oversupply the output stages of the SLIC (see Fig.32).

V.3.B SLIC with integrated ring generator :

The integrated circuit L3000 of SGS THOMSON is presently the only SLIC of this kind. It operates between ground and battery voltage for all the modes except for the ringing where the normal area is included between +VB (up to 72V) and battery voltage (-VBat) (see Fig.33). The protection will take into account this fact and operates over +VB and under -VBat.

Fig. 33 External diodes network used with the L3000.

SGS-THOMSON
MICROELECTRONICS
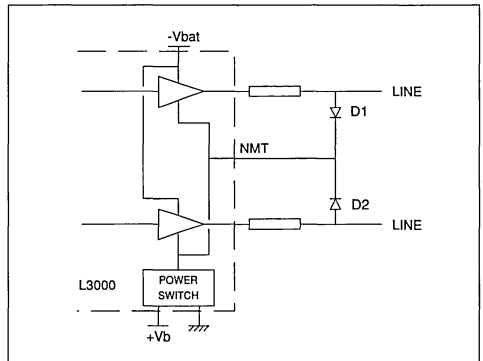
The diodes D1 and D2 (fig 33) act when the L3000 operates out of the ringing mode and when a positive overvoltage is clamped at +VB. The output stages are then temporarily oversupplied at +VB.

VI APPLICATION DIAGRAMS :

VI.1 SLIC without integrated ring generator

Fig. 34 Axial leaded solution
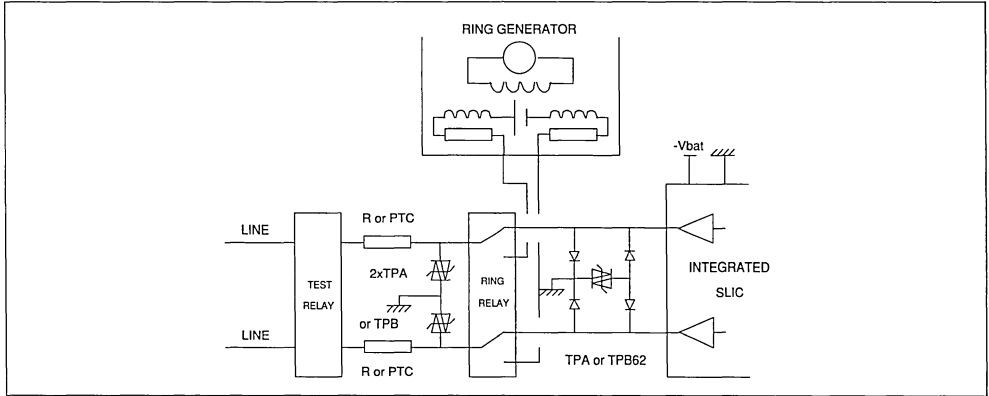
This basic diagram (fig 34) uses TRISIL TPA or TPB solution. Before the ring relay both lines are protected to the ground by 200 V bidirectional devices.

After the relay the positive surges are clamped to the ground by two diodes (one per line). For the negative one two diodes switch the overvoltage to a 62 V TRISIL.

Remark : The diodes choice is very important in order to minimize their peak forward voltage (V_{FP}).

Fig. 35 TO 220 or SIP 3 version
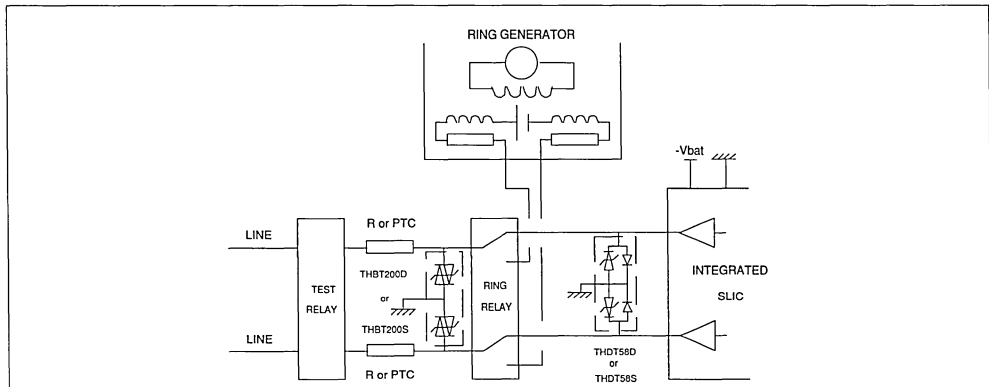
This topology (fig. 35) assumes the same protection function as precedent one with the following advantages :
- Only two packages.
- Reduction of printed board area used by the protection.
- Cost effective solution.

Fig. 36 Surface mount solution
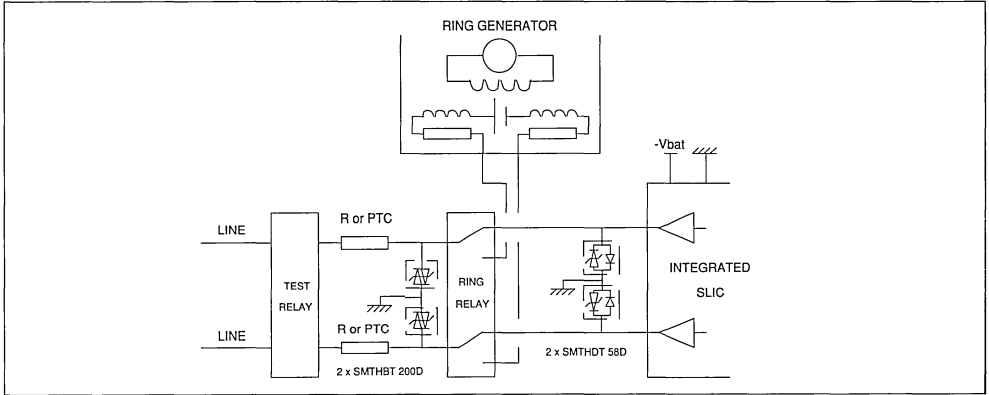
The figure 36 is exactly the same silicon solution with :
- Surface mount packages (SOD 15).
- Better cost solution in SMD version.
- Same cost as the TO 220 version.

Fig. 37 Programmable breakover voltage solution (2 x L3100B1)
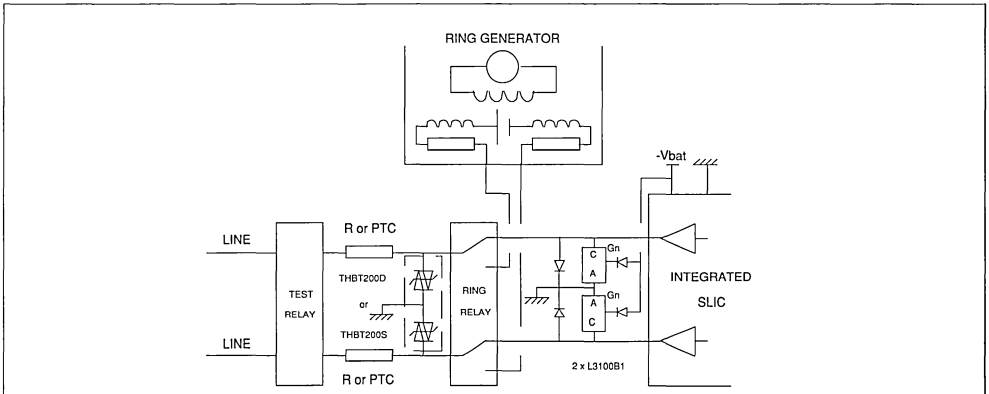
The protection behaviour is improved by a breakover value very close to the battery voltage (fig. 37).

This kind of solution is well adapted to the variable battery voltage application, for example short / long line switching.

Fig. 38 Programmable breakover voltage solution (1 x L3100B1)
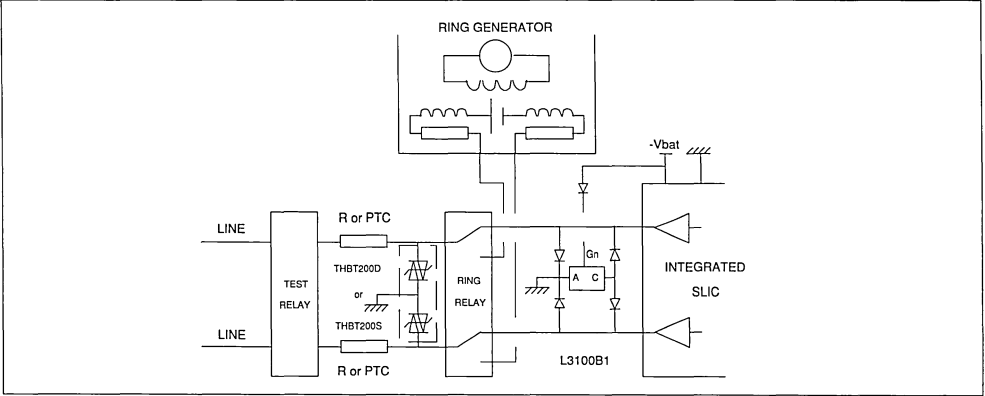
The figure 38 has the same electrical behaviour as the precedent one with.
  – Lower cost
Remark : The maximum voltage across the line during the device firing is increased by the V_{FP} of the diode.

Fig. 39 Monochip programmable breakover voltage solution
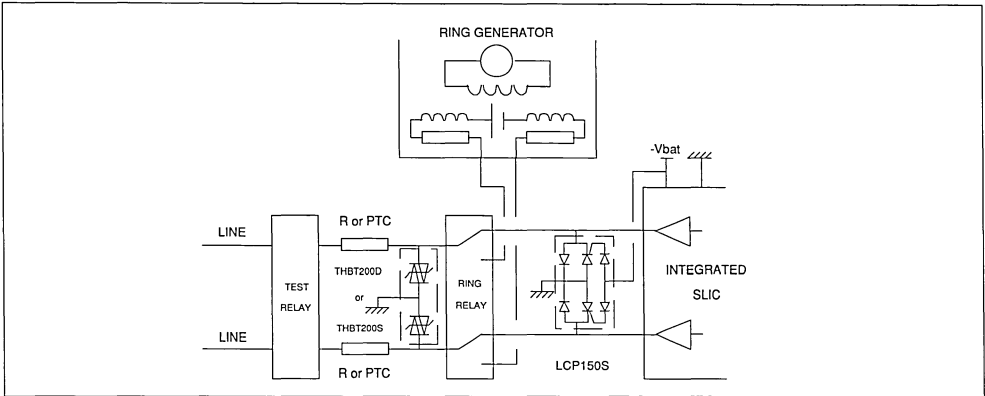
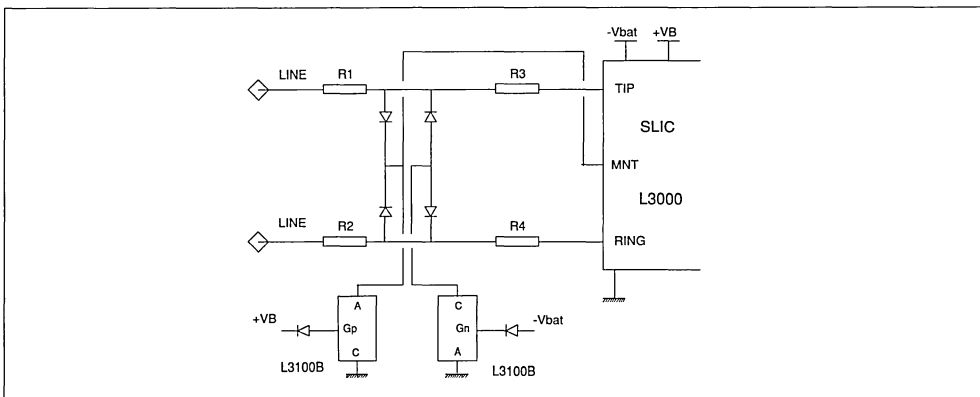This solution (fig. 39) performs the new generation of SLIC protection. It is the full integration of protection devices and peripherical diodes.

Fig. 40 L3000 protection with 2 L3121B
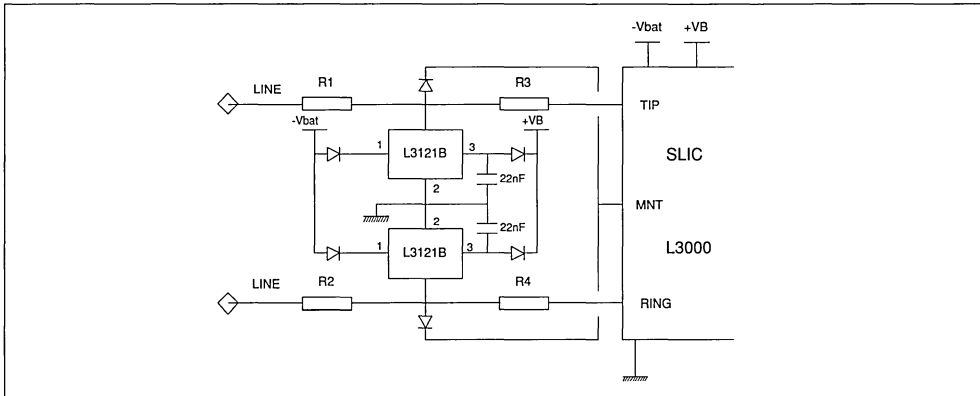
.VI.2 SLIC with integrated ring generator (L3000).

This topology (fig. 40) is the most efficient one for this kind of SLIC.

Fig. 41 L3000 protection with 2 L3100B

The figure 41 has the same electrical behaviour as previous one but with low cost.

VI.3 Common protections for several SLIC

These types (fig. 42 and 43) of application allow to decrease the cost of the protection per line. The major problems of these solutions are.
- The short circuit of all the lines when the protection fire

- The remaining current through the protection device after the surge is too high to permit the automatic switch off of the protection. In fact only a software action (low power state) permits to assume the switch off.

SGS-THOMSON
MICROELECTRONICS

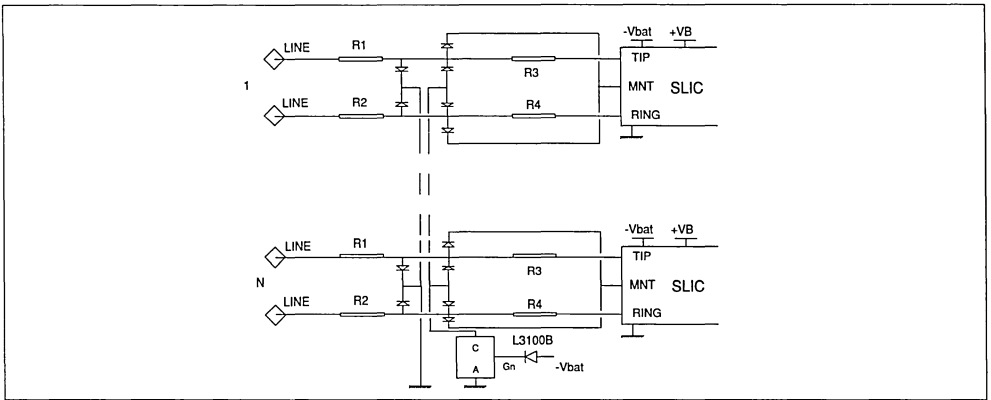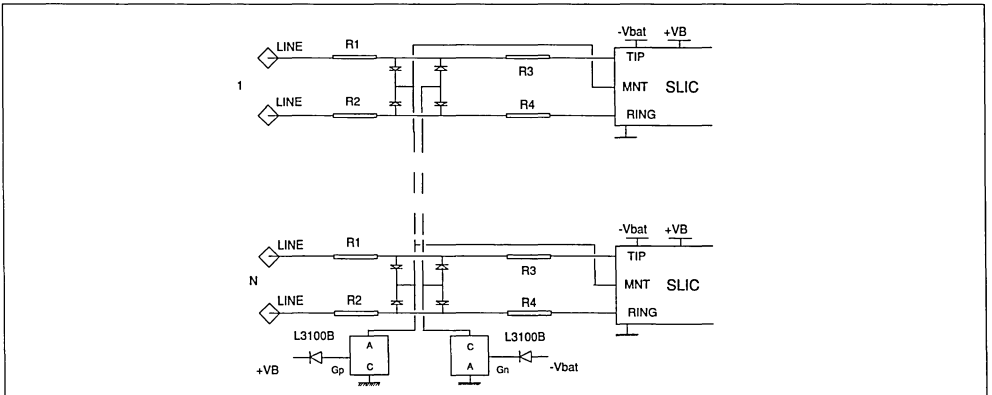**Fig. 42** Common protection for SLIC without integrated ring generator

Fig. 43 Common protection for SLIC with integrated ring generator

In conclusion SGS-THOMSON have got a large range of protection solutions in order to optimize your application diagram. These solutions take into account.

The type of SLIC.

The battery voltage.

The pc board surface.

The cost.

And will permit you to solve your SLIC protection problem.

SGS-THOMSON
MICROELECTRONICS

NOTES

NOTES

NOTES

NOTES

NOTES

SALES OFFICES

EUROPE

DENMARK

2730 HERLEV
Herlev Torv, 4
Tel (45-42) 94 85 33
Telex. 35411
Telefax. (45-42) 948694

FINLAND

LOHJA SF-08150
Karjalankatu, 2
Tel 12 155 11
Telefax 12 155 66

FRANCE

94253 GENTILLY Cedex
7 - avenue Gallieni - BP 93
Tel (33-1) 47.40 75 75
Telex. 632570 STMHQ
Telefax (33-1) 47 40.79 10

67000 STRASBOURG
20, Place des Halles
Tel (33) 88 75 50 66
Telex. 870001F
Telefax (33) 88 22 29 32

GERMANY

6000 FRANKFURT
Gutleutstrabe 322
Tel (49-69) 237492
Telex· 176997 689
Telefax· (49-69) 231957
Teletex. 6997689=STVBP

8011 GRASBRUNN
Bretonischer Ring 4
Neukeferloh Technopark
Tel. (49-89) 46006-0
Telex 528211
Telefax (49-89) 4605454
Teletex· 897107=STDISTR

3000 HANNOVER 1
Eckenerstrasse 5
Tel (49-511) 634191
Telex 175118418
Teletex. 5118418 csfbeh
Telefax. (49-511) 633552

8500 NÜRNBERG 20
Erlenstegenstrasse, 72
Tel (49-911) 59893-0
Telex 626243
Telefax· (49-911) 5980701

5200 SIEGBURG
Frankfurter Str 22a
Tel (49-2241) 660 84-86
Telex 889510
Telefax (49-2241) 67584

7000 STUTTGART
Oberer Kirchhaldenweg 135
Tel (49-711) 692041
Telex. 721718
Telefax (49-711) 691408

ITALY

20090 ASSAGO (MI)
V le Milanofiori - Strada 4 - Palazzo A/4/A
Tel (39-2) 89213.1 (10 linee)
Telex 330131 - 330141 SGSAGR
Telefax (39-2) 8250449

40033 CASALECCHIO DI RENO (BO)
Via R Fucini, 12
Tel (39-51) 591914
Telex· 512442
Telefax (39-51) 591305

00161 ROMA
Via A. Torlonia, 15
Tel (39-6) 8443341
Telex 620653 SGSATE I
Telefax. (39-6) 8444474

NETHERLANDS

5652 AR EINDHOVEN
Meerenakkerweg 1
Tel (31-40) 550015
Telex 51186
Telefax (31-40) 528835

SPAIN

08021 BARCELONA
Calle Platon, 6 4th Floor, 5th Door
Tel (34-3) 4143300-4143361
Telefax (34-3) 2021461

28027 MADRID
Calle Albacete, 5
Tel (34-1) 4051615
Telex: 27060 TCCEE
Telefax. (34-1) 4031134

SWEDEN

S-16421 KISTA
Borgarfjordsgatan, 13 - Box 1094
Tel (46-8) 7939220
Telex· 12078 THSWS
Telefax (46-8) 7504950

SWITZERLAND

1218 GRAND-SACONNEX (GENEVA)
Chemin Francois-Lehmann, 18/A
Tel (41-22) 7986462
Telex· 415493 STM CH
Telefax (41-22) 7984869

UNITED KINGDOM and EIRE

MARLOW, BUCKS
Planar House, Parkway
Globe Park
Tel (44-628) 890800
Telex· 847458
Telefax. (44-628) 890391

AMERICAS

BRAZIL

05413 SÃO PAULO
R Henrique Schaumann 286-CJ33
Tel (55-11) 883-5455
Telex: (391)11-37988 "UMBR BR"
Telefax 11-551-128-22367

CANADA

BRAMPTON, ONTARIO
341 Main St North
Tel (416) 455-0505
Telefax 416-455-2606

U.S.A.

NORTH & SOUTH AMERICAN
MARKETING HEADQUARTERS
1000 East Bell Road
Phoenix, AZ 85022
(1)-(602) 867-6100

SALES COVERAGE BY STATE .

ALABAMA
Huntsville - (205) 533-5995

ARIZONA
Phoenix - (602) 867-6340

CALIFORNIA
Santa Ana - (714) 957-6018
San Jose - (408) 452-8585

COLORADO
Boulder (303) 449-9000

ILLINOIS
Schaumburg - (708) 517-1890

INDIANA
Kokomo - (317) 459-4700

MASSACHUSETTS
Lincoln - (617) 259-0300

MICHIGAN
Livonia - (313) 462-4030

NEW JERSEY
Voorhees - (609) 772-6222

NEW YORK
Poughkeepsie - (914) 454-8813

NORTH CAROLINA
Raleigh - (919) 787-6555

TEXAS
Carrollton - (214) 466-8844

FOR RF AND MICROWAVE
POWER TRANSISTORS CON-
TACT
THE FOLLOWING REGIONAL
OFFICE IN THE U.S.A.

PENNSYLVANIA
Montgomeryville - (215) 362-8500

ASIA / PACIFIC

AUSTRALIA

NSW 2027 EDGECLIFF
Suite 211, Edgecliff centre
203-233, New South Head Road
Tel (61-2) 327 39 22
Telex· 071 126911 TCAUS
Telefax· (61-2) 327 61.76

CHINA

BEIJING
Liason Office
Beijing No 5 Semiconductor
Device Factory
14 Wu Lu Tong Road
Da Sheng Man Wai
Tel (861) 2024378
Telex 222722 STM CH

HONG KONG

WANCHAI
22nd Floor - Hopewell centre
183 Queen's Road East
Tel (852-5) 8615788
Telex· 60955 ESGIES HX
Telefax (852-5) 8656589

INDIA

NEW DELHI 110001
LiasonOffice
62, Upper Ground Floor
World Trade Centre
Barakhamba Lane
Tel 3715191
Telex 031-66816 STMI IN
Telefax· 3715192

MALAYSIA

PULAU PINANG 10400
4th Floor - Suite 4-03
Bangunan FOP-123D Jalan Anson
Tel (04) 379735
Telefax (04) 379816

KOREA

SEOUL 121
8th floor Shinwon Building
823-14, Yuksam-Dong
Kang-Nam-Gu
Tel (82-2) 553-0399
Telex· SGSKOR K29998
Telefax (82-2) 552-1051

SINGAPORE

SINGAPORE 2056
28 Ang Mo Kio - Industrial Park 2
Tel (65) 4821411
Telex RS 55201 ESGIES
Telefax (65) 4820240

TAIWAN

TAIPEI
12th Floor
571, Tun Hua South Road
Tel (886-2) 755-4111
Telex. 10310 ESGIE TW
Telefax. (886-2) 755-4008

JAPAN

TOKYO 108
Nisseki - Takanawa Bld 4F
2-18-10 Takanawa
Minato-Ku
Tel (81-3) 280-4121
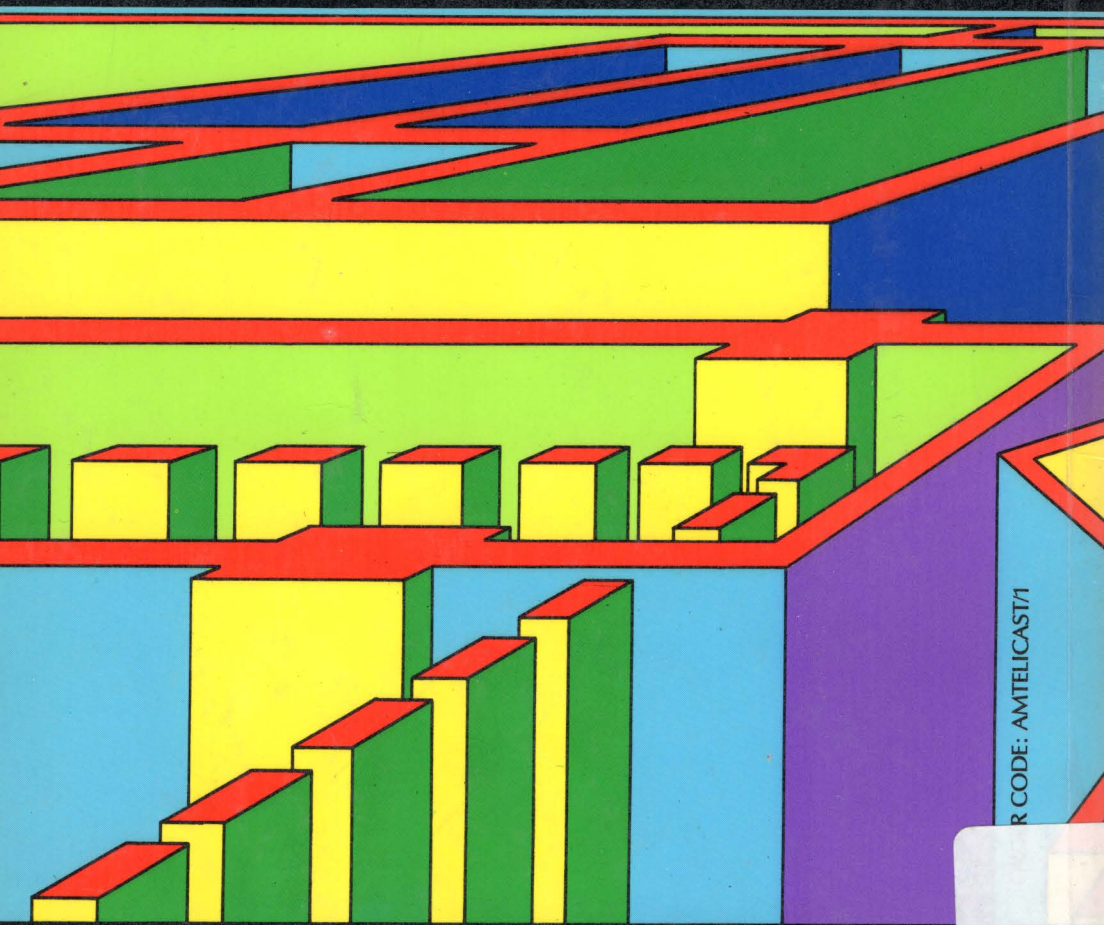Telefax (81-3) 280-4131